SIEMENS

INFORMATION NOTE

16M - Bit DYNAMIC MEMORIES

(Fourth Generation)

General Information
Products
Design and technology highlights
Packing

12.95
Weidlich, Technical Marketing Memories
INFO16M9.FRM

This information note is intended to provide technical information on the SIEMENS fourth generation 16M-bit DYNAMIC ACCESS MEMORIES.

GENERAL INFORMATION

The SIEMENS fourth generation 16 Megabit dynamic RAMs ("LUNA ES 3") are organized by 4 , by 8 and by 16 bits, assembled in industry standard SOJ and TSOPII packages, operating from a 5V or 3.3V power supply and support both fast page mode and hyper page mode (extended data out - EDO) functionality. The Burst-EDO- function („pipelined nibble mode") will be implemented later.

The 16M-Bit DRAMs utilise a 0.4 micron twin-well CMOS process on a p-type Epi/p+ substrate with a Substrate Plate Trench Cell and ONO dielectric jointly developed by IBM and SIEMENS, as well as advanced circuit techniques to provide wide operation margins , both internally and to the system user.

The chip design incorporates all organisations, different addressing schemes , fast page mode and hyper page mode (EDO) and all standard refresh operations (CAS-before-RAS, RAS-only, Hidden and Self Refresh). The chip internally operates at 3.3V and has a built-in voltage regulator for 5 V operation. Table 1 & 2 highlight the process and design related data.

PRODUCT SPECTRUM

All functions are implemented on the same die and the various organisations and features are selected by bonding options. Only the 5V / 3.3V power supply versions have different metal 2 masks. The following table shows the actual product spectrum: .

TYPE	SIEMENS Number	Speed Sorts [ns]	Package Type and Width	Description Functions and Refresh	Power Supply
4M x 4	HYB 5116400 BJ	-50/-60/-70	300mil SOJ 26/24-1	fast page mode 4k-refresh	5 V
	HYB 5117400 BJ	-50/-60/-70	300mil SOJ 26/24-1	fast page mode 2k-refresh	5 V
	HYB 5117405 BJ	-50/-60/-70	300mil SOJ 26/24-1	EDO mode 2k-refresh	5 V
	HYB 3116400 BJ	-50/-60/-70	300mil SOJ 26/24-1	fast page mode 4k-refresh	3.3 V
	HYB 3116400 BT	-50/-60/-70	300mil TSOPII- 26/24-1	fast page mode 4k-refresh	3.3 V
	HYB 3117400 BJ	-50/-60/-70	300mil SOJ 26/24-1	fast page mode 2k-refresh	3.3 V
	HYB 3116405 BJ	-50/-60/-70	300mil TSOPII-26/24-1	EDO mode 4k-refresh	3.3 V
2M x 8	HYB 5117800 BSJ	-50/-60/-70	400mil SOJ 28 -3	fast page mode 2k-refresh	5 V
	HYB 5117805 BSJ	-50/-60/-70	400mil SOJ 28-3	EDO mode 2k-refresh	5 V
1Mx16	HYB 5118160 BSJ	-50/-60/-70	400mil SOJ-42-1	fast page mode 1k-refresh	5 V
	HYB 5118165 BSJ	-50/-60/-70	400mil SOJ-42-1	EDO mode 1k-refresh	5 V
	HYB 3118165 BSJ	-50/-60/-70	400mil SOJ-42-1	EDO page mode 1k-refresh	3.3V
	HYB 3118165 BST	-50/-60/-70	400mil TSOPII-50/44	EDO mode 1k-refresh	3.3V

PACKAGE OUTLINE DRAWINGS

The SIEMENS 16M-DRAMs are available in industrial standard 400 and 300 mil wide SOJ and TSOPII plastic packages, appropriate for surface-mounting techniques. Package related data are shown in table 3. All SIEMENS packages meet JEDEC standards.

CODES FOR MARKING

The marking on the top side of every 16M-DRAM device gives information as to the device type, which access time specification is met and the country of origin. In addition, a weekcode indicates in which week of the year the part was tested. The letter "D" besides the country of origin is the indicator for the fourth generation 16M-DRAM design as shown as an example below:

A SIEMENS internal number is printed on the bottom side which represents the wafer production lot number, the date of final assembly and a code for the assembly line. Laser equipment is used for top and bottom side marking.

PACKING

Before packing, all devices are baked in metal tubes at 125 °C in ovens with circulating hot air for 24 hours. Within 12 hours the devices are seal packed. All sealed dry-pack boxes contain a pouch of desiccant and a humidity indicator.For SOJ & TSOPII packaged devices SIEMENS recommends not to exceed a 168 hours time frame between unpacking and vaporphase or reflow soldering. SIEMENS 16M-DRAMs are available in either tubes or tape & reel. The following table shows the number of devices per tubes and or reel.

Package Type	Delivery in Tubes		
	DRAMS per tube	Tubes per box	DRAMs per box
P-SOJ-26/24-1	25	40	1000
P-SOJ-28 - 3	27	50	1350
P-SOJ-42-1	18	50	900

Package Type	Delivery in Tape & Reel	
	DRAMS per reel	Tape Width [mm]
P-SOJ-26/24-1	1500	24 mm
P-TSOPII-26/24-1	3000	24 mm
P-SOJ-28 - 3	1000	24 mm
P-SOJ-42-1	1000	44 mm
P-TSOPII-50/44	1000	32 mm

16M-bit DRAM
PROCESS RELATED DATA

PROCESS	0.45 µm twin well CMOS on a p -type Epi/p+ substrate 1 tungsten silicide layer 2 aluminium layers	
SIEMENS PROCESS NAME	C6D	
TYPICAL DESIGN RULES	0.4m	
LITHOGRAPHY	i-line	
CHANNEL LENGTH	N-channel P-channel	0.5 m LDD 0.6 m LDD
OXIDE THICKNESS	13.5 nm	
JUNCTION DEPTH	N-channel P-channel	0.25 m 0.35 m LDD
THRESHOLD VOLTAGE	N-channel P-channel	0.6 V -0.7 V
CONTACT	0.45 m x 0.45 m , CVD tungsten refill	
CELL TYPE	Substrate Plate Trench Cell 10 nm eff ONO 7,5 m depth	
CELL CAPACITANCE	> 70 fF	
BITLINE TO CELL CAPACITANCE RATIO	3 : 1	
ALUMIMIUM 1 & 2 THICKNESS CONTENT	 500 nm / 1265 nm Al / Cu (0.5%)	
PASSIVATION THICKNESS / CONTENT	 450 nm SiO_2 + 400 nm SiN	

table 1

16M-Bit DRAM
DESIGN RELATED DATA

SIEMENS CODENAME	LUNA ES 3	
ORGANIZATION	4M x 4, 2M x 8, 1M x 16	
POWER SUPPLY	5V (± 10 %) & 3.3 V (± 0.3 V)	
OPERATION MODES	FAST PAGE MODE HYPER PAGE MODE (Extended Data Out - EDO)	
REFRESH	4M x 4 2M x 8 1M x 16	4k / 64 ms & 2k / 32 ms 4k / 64 ms & 2k / 32 ms 4k / 64 ms & 1k / 16ms
SPECIFICATIONS		
TRAC	50 / 60 / 70 ns	
TCAC	13 / 15 / 20 ns	
TAA	25 / 30 / 35 ns	
CHIP SIZE	5.73 mm x 13.65mm = 78.2mm^2 (diced)	
CELL SIZE	1.04 m x 2.30 m = 2.39 m ^{2}	
SENSE LINE	FOLDED BITLINE CONCEPT with 64 blocks of 256k cells	
WORDLINE PITCH	1.15 m	
BITLINE PITCH	1.04 m	
REDUNDANCY		
ROWS	128	
COLUMNS	128	
METHOD	Laser	
NUMBER OF DEVICES		
transistors	20.53 Mio.	

table 2

16M-Bit DRAM
ASSEMBLY RELATED DATA

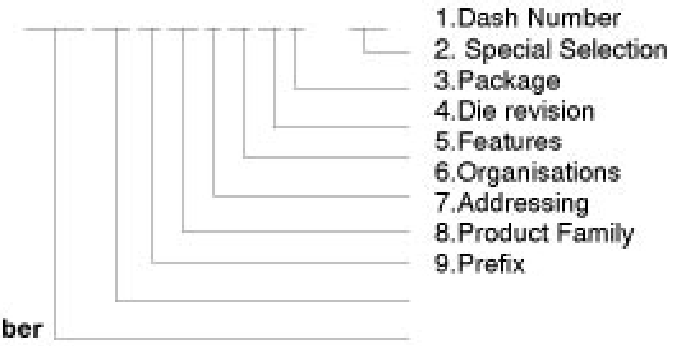
PACKAGE TYPE	Surface mount package LOC - Lead on Chip Technology
PACKAGE	300 mil wide SOJ 26/24 package for 4M x 4 300 mil wide TSOPII-26/24 package 4M x 4 400 mil wide SOJ 28 package for 2M x 8 400 mil wide SOJ 42 package for 1M x 16 400 mil wide TSOPII-50/44 for 1M x 16 JEDEC-standard
LEAD FRAME	ALLOY 42 / Ag spot
FINISH	SnPb 80/20
WIRE BOND	24 m Au wires, thermosonic
CHIP PROTECTION	Polyimid layer
MOLDING COMPOUND	MP 7220 V (Nitto)

table. 3

fig. 1

CODES FOR MARKING

Example: HYB 5116400 BSJL - 60



1.Dash number

-50	part meets 50 ns tRAC access time specification
-60	part meets 60 ns tRAC access time specification
-70	part meets 70 ns tRAC access time specification

2.Special selection

_	none, standard specification and temperature range (0°C to 70°C)
L	Low Power Version with extended refresh

3.Package

J	300mil wide SOJ 26/24 packages for 4M x 4 DRAMs
T	300mil wide TSOPII-26/24 packages 4M x 4 DRAMs
SJ	400mil wide SOJ 28 package for 2M x 8 DRAMs and 400mil wide SOJ 42 package for 1M x 16 DRAMs

4.Die revision

B	Design revision "third generation"

5. Operation Modes

0	Fast Page Mode
5	Hyper Page Mode (Extended Data Out Function - EDO)
7	Burst-EDO Mode („pipelined nibble")

6.DRAM Organisation

10	x 1 organisation
40	x 4 organisation
80	x 8 organisation
16	x 16 organisation

7.Addressing

15	4k-refresh
17	2k-refresh
18	1k-refresh

8.Product Family

51	SIEMENS CMOS DRAMs with 5 Volt operation
31	SIEMENS CMOS DRAMs with 3.3V operation

9.Prefix

HYB	SIEMENS standard prefix
HYF	SIEMENS prefix for extended temperature range products

fig.4