INFORMATION NOTE

TEST MODE IN 16M-GENERATION

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Test Mode

The 16M-DRAM offers a 16-bit test-time saving parallel test mode. Test mode is set by performing a $\overline{WE}$-and $\overline{CAS}$-before-$\overline{RAS}$ (WCBR) cycle. Row addresses A0 through A9 have to kept **high** to perform a testmode entry cycle. All other addresses are don't care. The test mode requires that the value of $t_{CHRT(min.)}$ is 30ns when performing a test mode entry cycle.

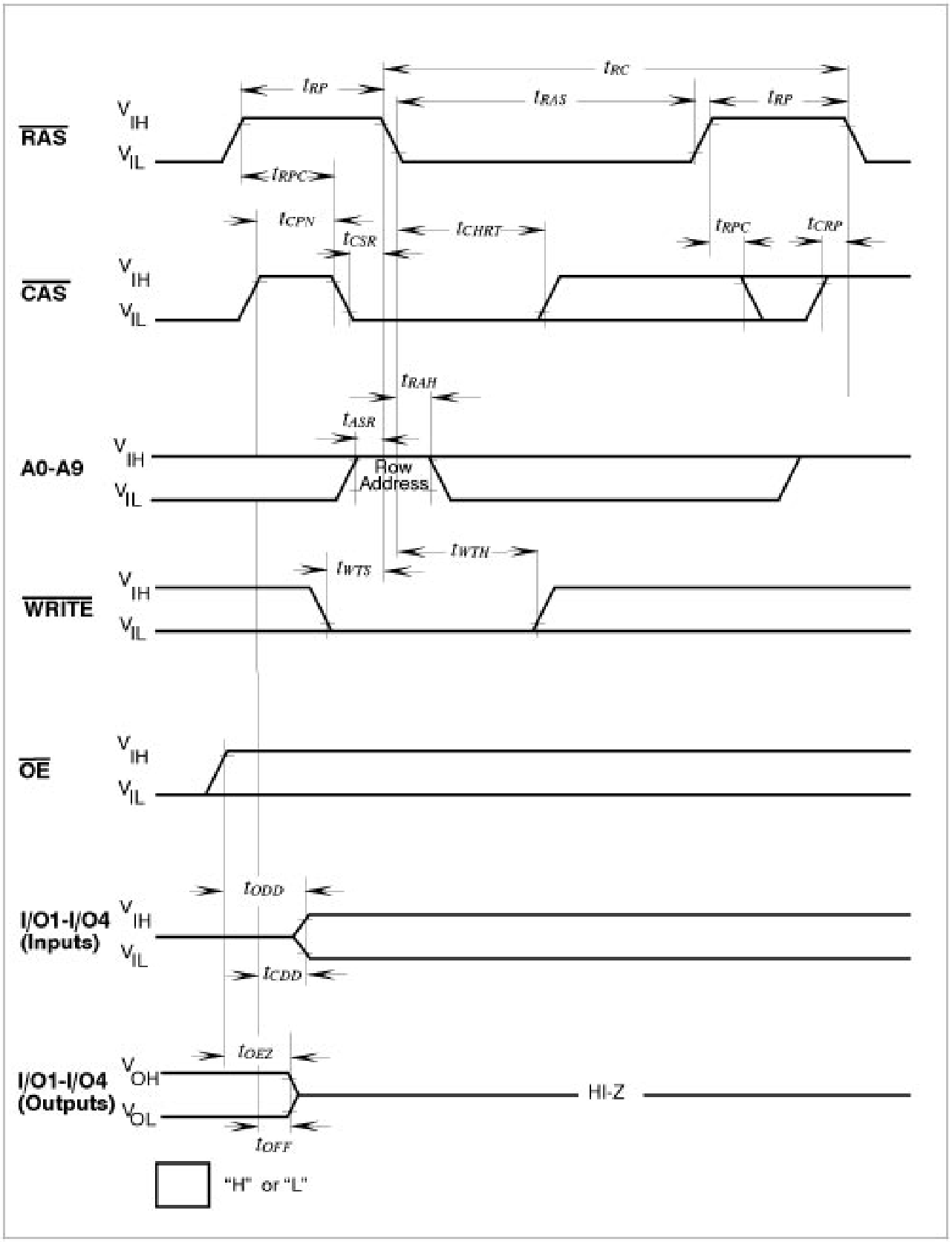
In 16-bits parallel test mode, data is written into 16 bits in parallel at Din and read out from Dout for x1 organized devices. In x4 organized devices data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O. Column addresses A0 & A1 are don't care during the test mode.

To get out of test mode and enter a normal operation mode, a regular CAS-before-RAS refresh cycle, RAS-only refresh cycle or Hidden refresh cycle can be used. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles.

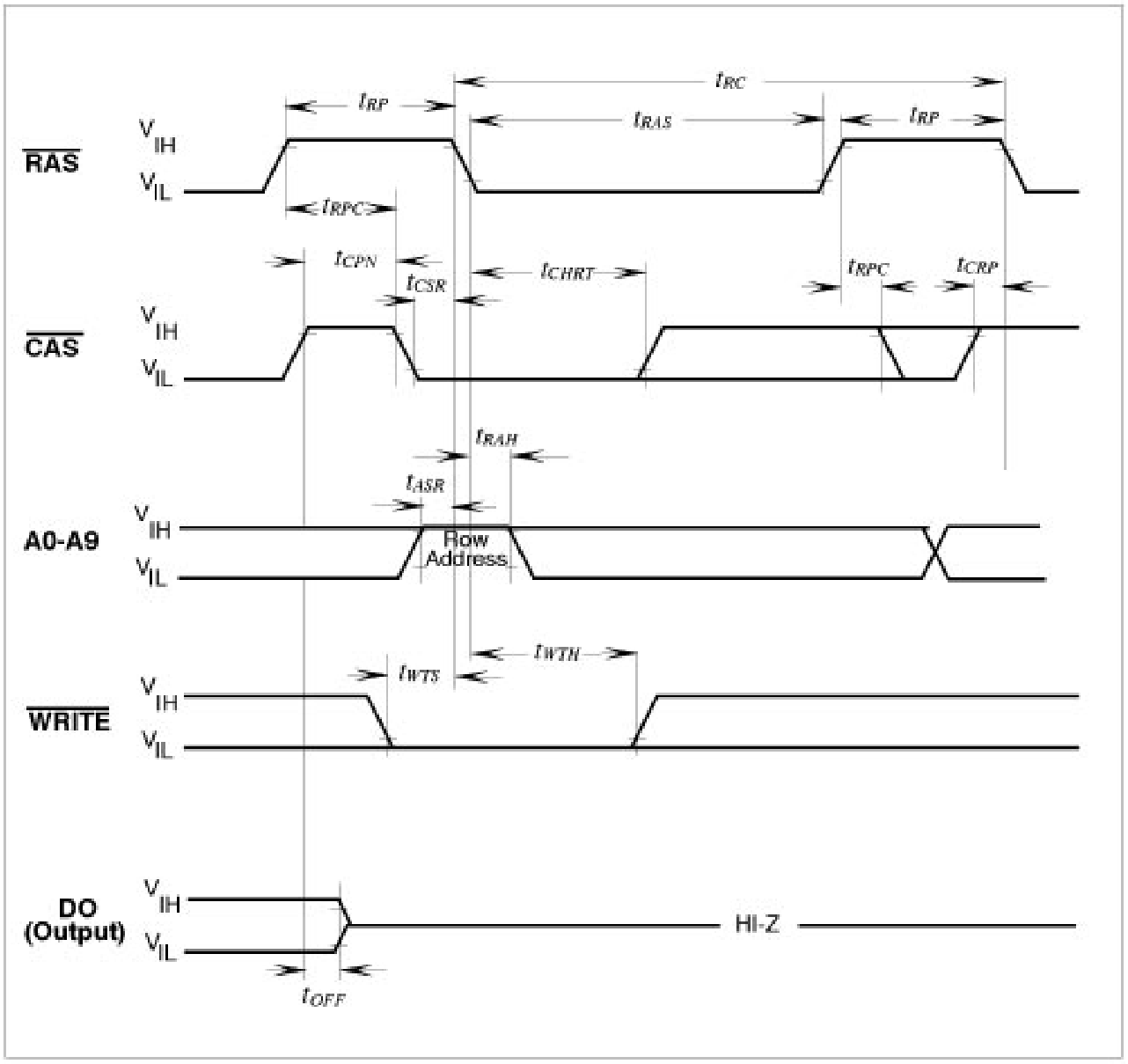
For 4Mx4 devices in a test mode "write" the data from each I/O pin is written into four 1M blocks simultaneously (all "1" s or all "0" s). In test mode "read" each I/O output is used for indicating the test mode result. If the internal four bits are equal, the I/O would indicate a "1". If they were not equal, the I/O would indicate a "0".

If 16 bits are equal (all "1"s or all "0" s) in a 16Mx1 device, the data output pin is a high state during test mode read cycle, then the device has passed. If they are not equal , data output pin is a low state, the the device has failed.

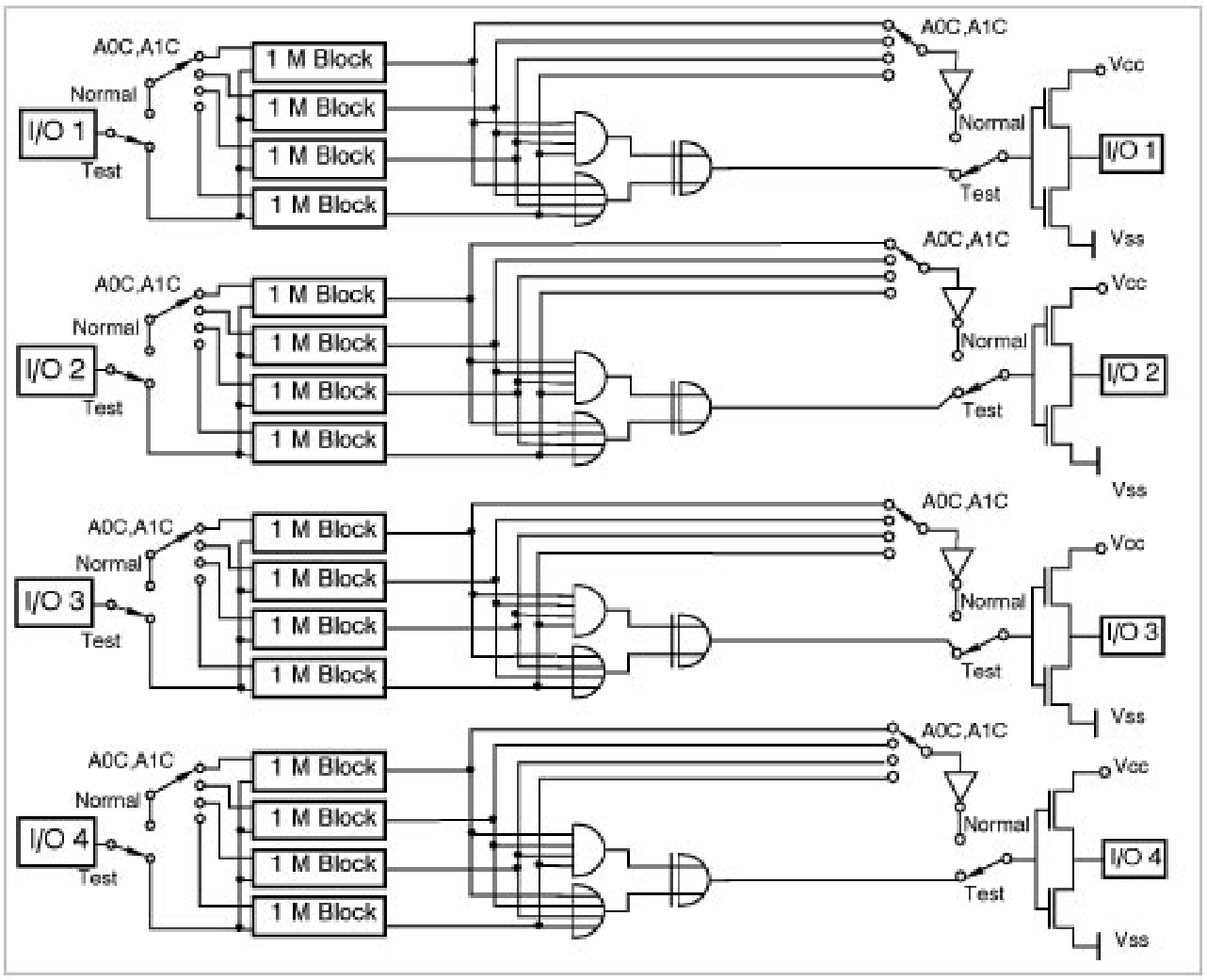
As the testmode is organized internally as 1M x 16-bits, a test mode cycle using 4:1 compression can be used to improve test time. Note that in the 4M x 4 version the test time is reduced by 1/4 and by a factor of 1/16 in the 16M x 1 version for a N test pattern.



Test Mode Entry (4M x 4 device)



Test Mode Entry Cycle (16M x 1 device)



Block Diagram in Test Mode (4M x 4 device)

The 16M DRAM is divided into sixteen 1M blocks. In test mode, information from four of the sixteen blocks is compared as shown in the diagram above.