SIEMENS

16M - Bit Dynamic RAMs

# INFORMATION NOTE

## Fourth Generation 16M - Bit DRAMs
## Accelerated Soft Error Sensitivity (ASER)

5.96

Info16M12.Doc

This information note is intended to provide technical information on the SIEMENS 16M-DRAM fourth generation product family.

## DEFINITION OF SOFT ERRORS

Soft errors are random nonrecurring single bit fails of Integrated Circuits especially known with memory products. They are ultimately caused by $\alpha$ - particles originating from materials used to fabricate the component, e.g. moulding compound, leadframes or the aluminium on the die itself.

The functional failure is strictly temporary than permanent and does not influence the long term reliability of the product.

## PHYSICAL FAILURE MECHANISM

Alpha particles ( $\alpha$'s ) are doubly charged helium nuclei emitted in the radioactive decay of heavy elements. Naturally occurring $\alpha$'s range in energy from about 2 to 9 MeV and are treated as classical particles.

An $\alpha$ interacts with silicon creating a track of electron - hole pairs along the 25 $\mu$m straight line path of the particles.

The digital information is stored as charge on the trench-capacitor and must be periodically refreshed as usual.

Whether or not sufficient charge is collected from the track to upset either cells or sensing depends on the total stored charge, noise margins, $\alpha$ - particle energy and collection efficiency.

## DESIGN FOR LOW SOFT ERROR RATE

The memory cell array is built up with subtrate plate trench-type storage capacitors with a capacitance in the range of 80 femtoFarads. The chip is additionally coated with a thin Polyimid layer and a low stress moulding compound with low radiation is used.

Consequently much care has to be taken to control the radioactivity from process materials as aluminium or silicides. Periodic sampling of all materials used in the process guarantees comparable low contamination.

## SOFT ERROR TESTING METHODS

Two practical methods to test for Soft Error Sensitivity are known:

### *1. Soft Error Lifetest*

Hundreds of memory parts are run in a Monitoring Burn-In System for a total of several million device hours under realistic operation conditions. As a result the specific **S**oft **E**rror **R**ate (SER) can be given in FIT ( events per $10^9$ device hours).

### *2. Accelerated Soft Error Test*

Few chips assembled in open ceramic packages are submitted to the irradiation of an artificial $\alpha$ - source while the functionality of the device is continuously monitored by an automated test equipment.

As a result only relative comparison between different parts can be obtained. However this test can also be used to derive the **A**ccelerated **S**oft **E**rror **R**ate (ASER) and accelerating factors for different voltages, temperatures, cycle times, data pattern or other operation parameters and can be compared with results from previous DRAM generations.

## SOFT ERROR LIFETEST RESULTS

A soft error lifetest was performed using a MBT/MTT monitoring burn-in system from Aehr. 16M DRAM devices were randomly selected from three different production lots and tested up to two million device hours. No "soft error" occured within this test period. The following test conditions were used :

| | Read cycle time | Supply voltage | Amb. Temp. |
|---|---|---|---|
| Test condition | 300 ns | 4.5 V | 45°C |

The SER (system soft error rate) for standard conditions (VCC = 5V and $t_{RC}$ = 1µs) and a confidence level of 60% can now be calculated to

**SER < 130 FIT**

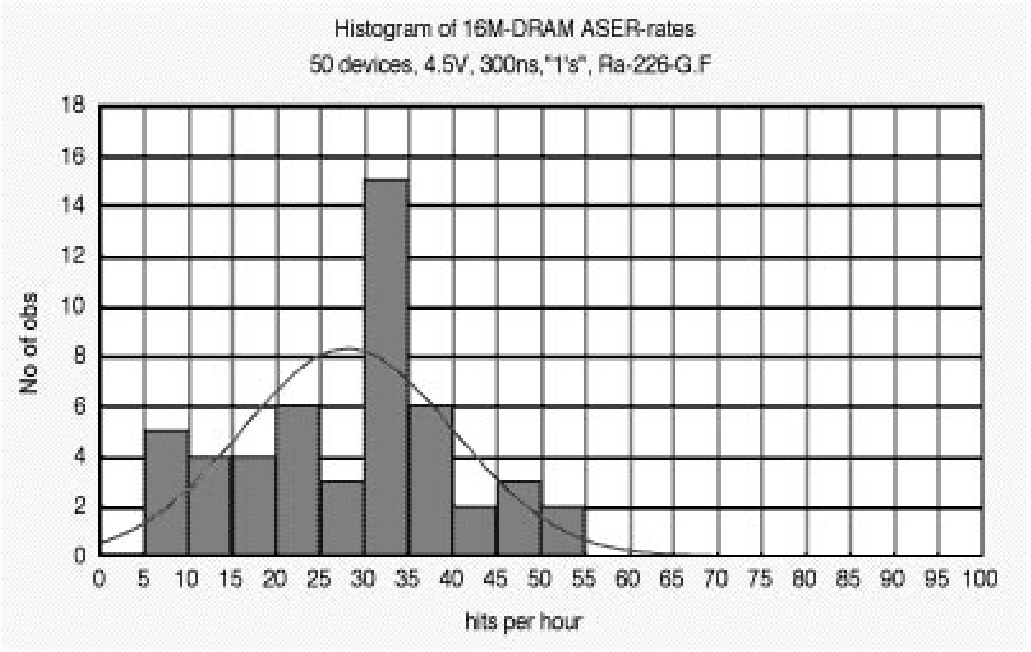
## ASER RESULTS OF 16M - DRAM's

50 16M - chips out of five different wafer lots were assembled in ceramic packages and an RA - 226 thin foil $\alpha$ - particle source was placed above the die. The chips were tested with two different voltages (4.5V & 5.5V) and various data pattern and different cycle times (300ns, 500ns & 1$\mu$s) for 1 hours and the soft error due to $\alpha$ - particle hits were counted.

The worst case condition was found with low VCC , 300ns fast cycle time and a physical "1" pattern. Under this condition the following numbers of hits per hours have been found :

| | | |
|---|---|---|
| **min:** | **6.0** | **hits / hour** |
| **mean:** | **28.0** | **hits / hour** |
| **max:** | **50** | **hits / hour** |

Fig.1 shows the distribution of the hit-rates of these 50 devices




## Influence of Voltage, Pattern and Cycle Time

At short cycle times the ASER-rate is at its worst case. Longer cycle times show a decrease.

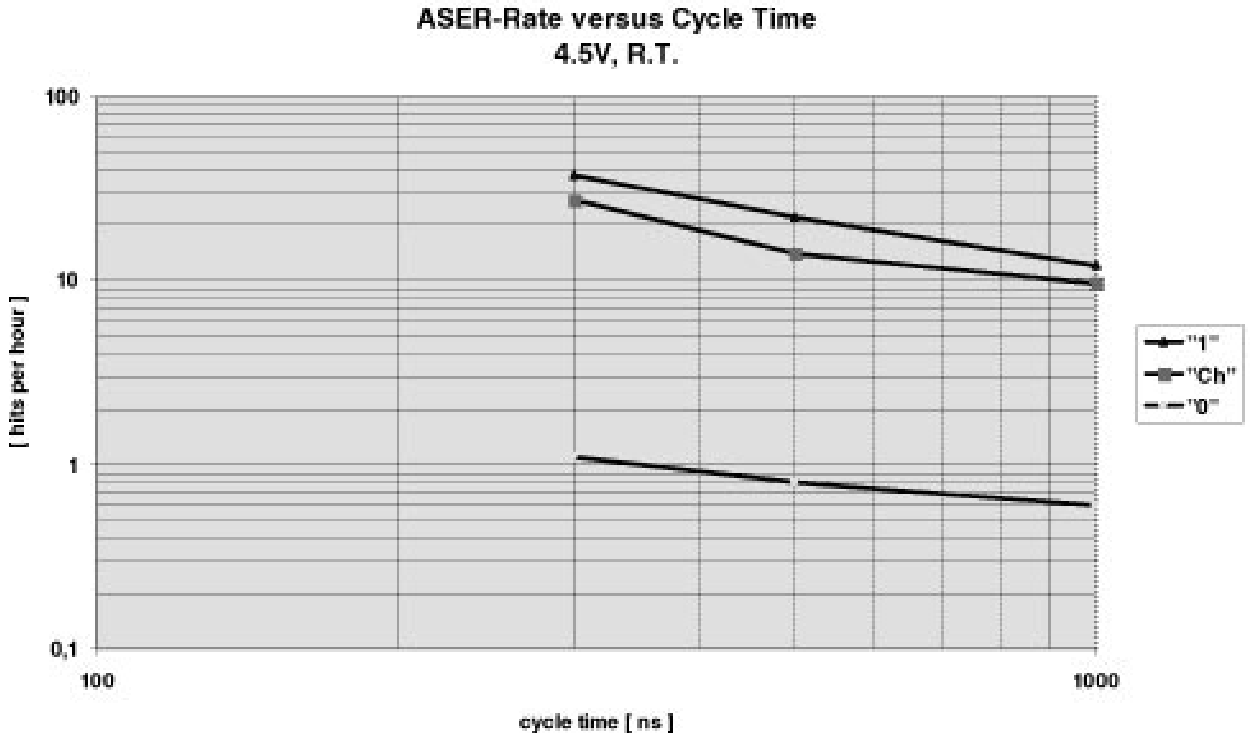
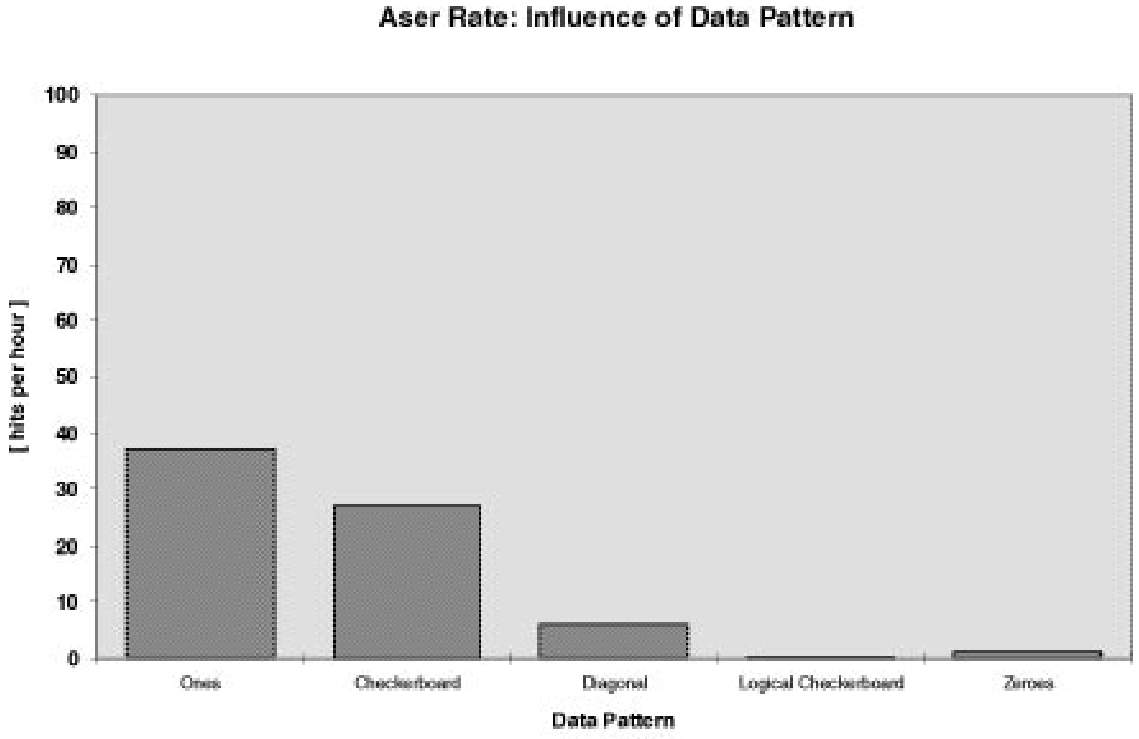



fig.2

The ASER-rate is depended on the data-pattern used to perfom this test . Tests have been performed with different data pattern. Their influence is shown in fig.3:




ASER-Rates depend on VCC. Low VCC ist the worst case, for higher VCC values the ASER-rate decreases :

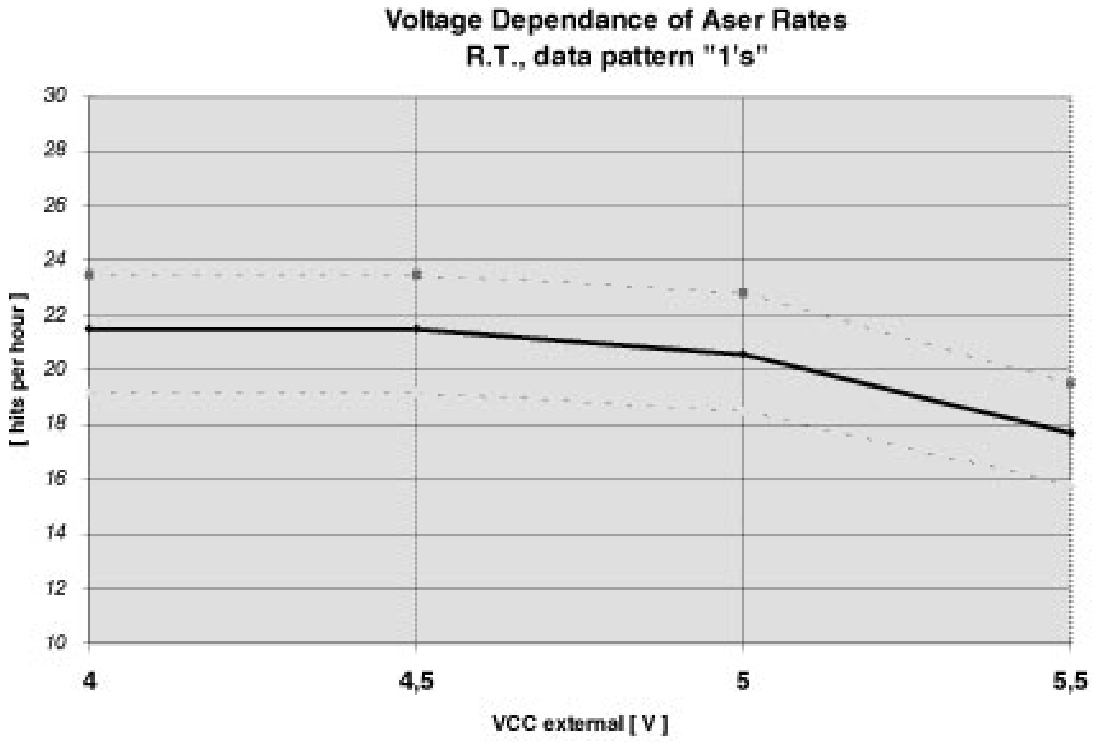

Voltage Dependance of Aser Rates
R.T., data pattern "1's"
[ hits per hour ]
30
28
26
24
22
20
18
16
14
12
10
4
4,5
5
5,5
VCC external [ V ]

fig.4