SIEMENS

16M - Bit DRAMs

INFORMATION NOTE

4M x 4 DYNAMIC MEMORIES

2k versus 4k - Refresh

12.93

INFO16M2.DOC

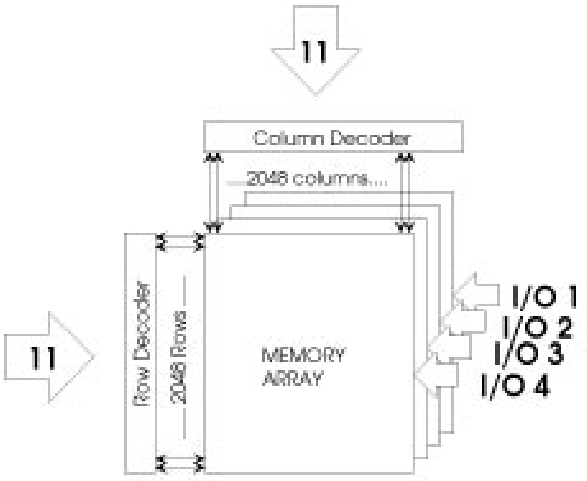
This information note is intended to provide technical information on the SIEMENS 4Mx4 DYNAMIC ACCESS MEMORIES HYB 5116400BJ/BT and HYB 5117400BJ/BT.

4M x 4 DRAMS

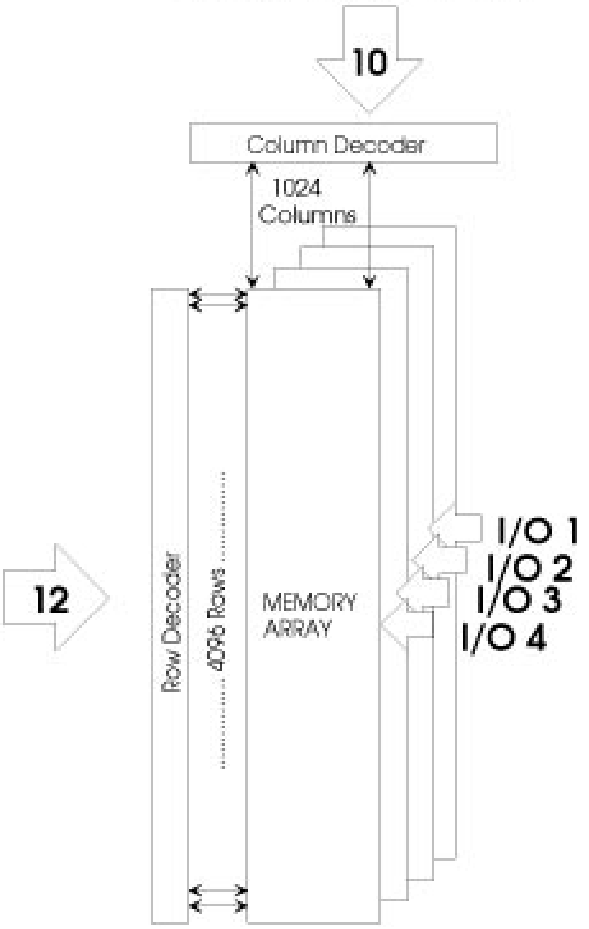
The JEDEC standardisation committee has approves two version of the 4M x 4 DRAMs , one with 4096 (4k) cycle refresh in 64 ms and a second with 2048 (2k) cycle refresh in 32ms. Excluding this difference, the timing and performance of the two devices are identical.

Industry demand for decreased power consumption led JEDEC to approve 4k refresh in addition to 2k refresh at the 4Mx4 DRAM level. A 4Mx4 device with 4k refresh draws about 30-40% less operating current than a device with 2k refresh. The current is decreased by increasing the number of rows and decreasing the number of columns, whereas one with 2k refresh has 2048 rows and 2048 columns. The number of columns defines the "depth" of a page. The drawing below shows how 2k and 4k refresh devices are different. Notice that the 2k device has a page depth of 2048, while the 4k device has a page depth of 1024, or half the page depth of the 2k device.

4M x 4 with 2K Refresh



4M x 4 with 4K Refresh



CHOOSING 2k or 4k REFRESH

There are several factors to consider when deciding which refresh standard is best for an application :

1. Refresh standard supported by the DRAM controller -- 2k,4k, or both ?
2. Frequency of page accesses
3. Need for low power consumption

Some DRAM controllers are limited to 2k refresh. If this is the case, 2k devices have to be used. Newer DRAM controllers are being designed to support both standards, so this limitation should be short-lived.

The choice of 2k or 4k refresh 4Mx4 DRAMs will probably be based on the importance of power consumption versus page depth. A system requiring frequent page accesses may not benefit by sacrificing page depth in exchange for the power savings of a 4k refresh. In a portable system, the benefits of about 30 - 40% less current may easily override concerns about decreased page depth.

DRAM MODULES

Modules may use both 2k and 4k refresh depending on whether or not they accommodate parity. Modules that don't use parity could use either 2k or 4k refresh. Most modules that have parity will use the 2k refresh standard in order to accommodate the use of 4M-DRAMs for the parity bits. As shown in fig. 2, when a 4Mx4 with 2k refresh is used, the number of rows and column match the 4Mx1, allowing the usage of 4Mx1 DRAMs for parity.

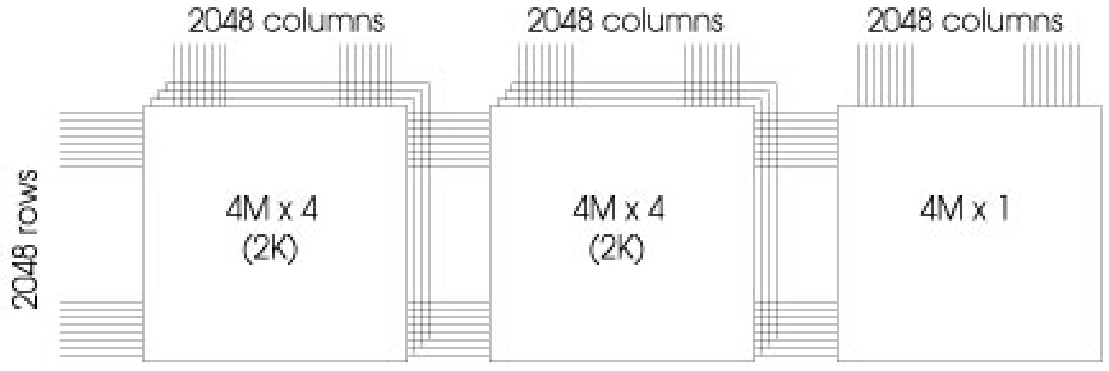


fig.2

If 4Mx4 with 4k refresh are used, 4Mx1 DRAMs can't be used for parity because the number of rows and columns does not match. The shaded area shown in fig. 3 are the portions of the DRAM that can't be used because of the difference in the number of rows and columns.

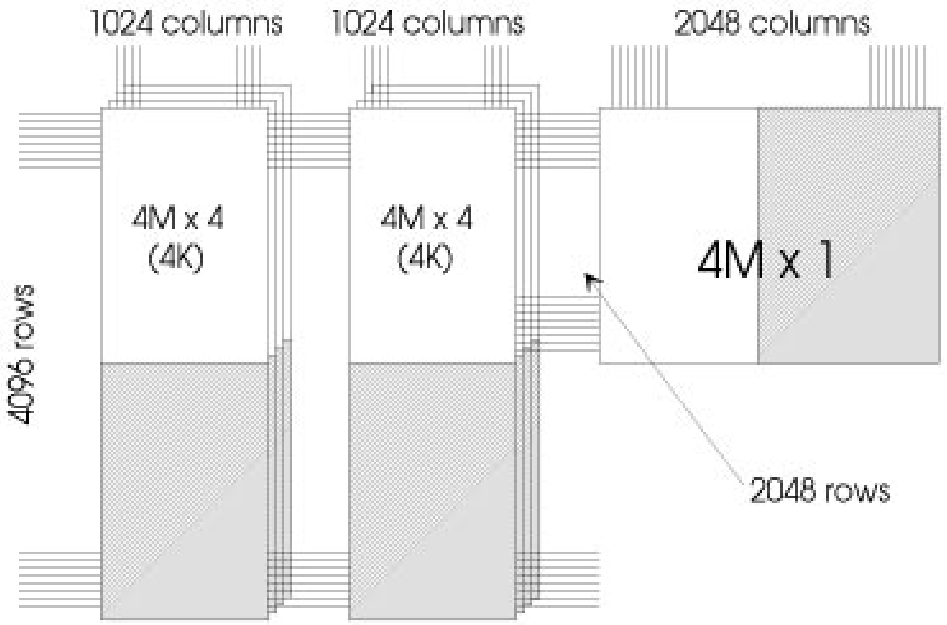


fig.3