# PTS 160 SYSTEM SECTION

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## TABLE OF CONTENTS

## INTRODUCTION

This manual covers the PTS 160 Frequency Synthesizer and contains information necessary to install, operate and service the instrument.

The PTS 160 is a precision frequency generator. It uses the accuracy and stability of a frequency standard operating at 5.0 or 10.0 MHz, either built-in or external, to produce output frequencies between 0.1 and 159.999 999 9 MHz, with up to 10 significant figures. All output frequencies are coherent with the standard frequency and reflect its stability and accuracy. Any frequency within the above band may be selected by manual dial or by remote control with resolution as fine as 0.1 Hz. The output from the levelled system is +3 to +13 dBm into 50 ohms and may be adjusted manually by the front panel control and meter or remotely by analog voltage.

The PTS 160 is a direct frequency synthesizer capable of providing signals for many uses requiring stable and accurate sine-wave signals with low attendant spurious outputs, low phase noise and fast transfer between selected frequencies. Typical applications include communications, spectrum analysis and surveillance, radar and automatic test systems with both narrow and wideband coverage.

### Manual Organization

The PTS 160 is a complete and integrated system using up to 13 modules installed on a deck inside the instrument mainframe. All data pertaining to the total instrument as a system are presented in the System Section of this manual. This section also covers items which are integral parts of the mainframe, such as power supply, front panel, rear panel and crystal oscillator. Modules which are mounted on the deck are covered in subsequent sections. **The GPIB interface which mounts to the rear panel, like the PE 1121 board, is treated in a separate section.**

## SPECIFICATIONS

**Frequency**

| | |
|---|---|
| Range: | 0.1 MHz to 159.999 999 9 MHz |
| Resolution: | 0.1 Hz to 100 KHz steps (optional) |
| Control: | Local by 10-position switches with dial; remote by TTL-Logic, 1,2,4,8; parallel-entry BCD; (hexadecimal for 0–15, 10 MHz steps). Neg true. 8-bit byte storage. IEEE 488 GPIB interface optional. |
| Switching Time: | 20 microsec (within 0.1 rad at new frequency); 3 microsec with TLU-section for six least significant decade steps (optional) |

**Output**

| | |
|---|---|
| Level: | +3 to +13 dBm, (1V) into 50 Ω, metered in dBm and volt. |
| Flatness: | ±0.5 dB |
| Impedance: | 50 Ω |
| Control: | Manual by F/P-control, remote by voltage (+ 0.63 to 2.00V); RMS-output voltage into 50Ω equals 1/2 positive DC-control voltage. |

**Spurious Outputs**

| | |
|---|---|
| Discrete: | –75 dB; –55 dB with TLU-section "J" |
| Harmonics: | –35 dB at full output (improved at lower level) |
| S/N (phase): | –63 dBc (0.5 Hz to 15 KHz), incl. effects of int. std.; –55 dBc with TLU-section "J" |
| Noise Floor: | –135 dBc/Hz |

**Frequency Standard**

| | |
|---|---|
| Internal (option): | $3 \times 10^{-9}$/day, or $1 \times 10^{-8}$/day |
| External Drive: | 5.000 or 10.000 MHz, 0.5V into 300 Ω |
| Aux. Output: | 10.000 MHz, 0.4V into 50 Ω |
| Oper. Ambient: | 0 to 55°C, 95% R.H. |
| Power: | 105 to 125V, 50 to 400 Hz, 40 Watts (200–230V avail.) |
| Dimensions: | 19x5-1/4x18" (Relay rack or bench cabinet) |
| Weight: | 35 lbs |



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# INSTALLATION

**CAUTION:** Refer to **Primary Power** below, before connecting instrument to line.

## Unpacking

Your instrument has been built, tested and packed carefully and should reach you in perfect mechanical and electrical condition. Please inspect both the carton and the cabinet upon receipt for evidence of damage that might have occurred in transit. In case of damage or defect, a claim must be filed with the carrier immediately.

## Dimensions

Outside cabinet dimensions of the instrument for both the rack and bench versions are given in Figure 1.

## Primary Power

The PTS 160 is designed to operate from power lines with 115 or 220 VAC, +5%–10%, 50–400 Hz. Before operating your instrument, be certain that it has been connected and fused for your line voltage; this is indicated on the rear panel. Improper setting may lead to damage of the instrument.

Proper grounding of the mainframe to the neutral or ground of the power system is accomplished via the NEMA-approved receptacle and the 3-wire power cord supplied. For the safety of the operator, an approved adapter must be used with 2-wire outlets; such adapter must provide positive connection to the electrical conduit or other low resistance ground. Depending on module complement (resolution), the power consumption of the PTS 160 is approximately 40 Watts.

### Bench Use

For bench use the PTS 160 is equipped with a fold-down tilt stand. Stacking of the instrument is permissible, provided convection cooling of the heat-sink on the rear panel is not prevented by deep, overhanging cabinets.

### Rack Mounting

The instrument may be mounted to a standard 19-inch relay rack, if ordered with the rack mounting option. Where shock or vibration are encountered, it is suggested that rear or side supports be provided for the instrument.

## OPERATION

### Power Connection

Before attempting to connect the instrument to the primary power, verify proper line voltage connection and fusing; refer to **Primary Power** under **INSTALLATION.**

### Warm-Up

The PTS 160 is operative on turn-on. If the instrument is equipped with an oven-type crystal oscillator, a period of 20 minutes is required at 25°C ambient for the frequency to be within $\pm 1 \times 10^{-7}$ of nominal. In general, it is desirable to operate the equipment continuously for best frequency stability.

### External-Internal Frequency Standard

The synthesizer may be operated from either the internal or an external frequency standard (5.0 or 10.0 MHz). If no external standard is used, the standard frequency selector switch (rear panel) has to be set to INT. STD.; otherwise no output is generated.

### Controls, Front Panel

Figure 2 identifies all controls provided on the front panel for local operation.

(a) *Frequency Selector Switches with Dial* – A 2-position switch controls the 100 MHz step, and 10-position switches control the 10 MHz to 0.1 Hz steps. Instruments with less than full resolution have blank dial-switches for steps which are not equipped. The highest output frequency obtainable from the PTS 160 is 159.999 999 9 MHz. The first two dials can be set to numbers in excess of 15; these positions are not valid, however.



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(b) *Local/Remote Indicators* — LEDs indicate the mode in which the instrument is operated. The remote mode is enabled via the program connector on the rear panel; see **Rear Panel Controls and Connectors**, below. Manual dial settings indicate frequency only when operating in the local mode.

(c) *Level* — Continuously variable control to set output to desired level between +3 and +13 dBm into 50 ohms, with the aid of the meter. (The fully ccw position disconnects this control for remote level setting.)

(d) *Meter* — The meter indicates voltage or power in dBm delivered to a 50-ohm load. Voltage behind a 50-ohm source resistor is monitored, and the meter indicates one-half of this value. Calibration is valid for 50-ohm loads only.

(e) *Output Connector* — BNC jack supplies instrument main output.

(f) *Power Switch* — When non-continuous operation is desired, the primary power may be interrupted by this switch. Local/remote indicators serve as line-power indicators.

With these controls any frequency between 100 KHz and 159.999 999 9 MHz may be selected, subject to the resolution (option) of the instrument. When a power output of less than +3 dBm is desired, the use of 50-ohm attenuators is recommended.

**Rear Panel Controls and Connectors**

Figure 3 shows rear panel controls and connectors for programming and auxiliary inputs and outputs.

(a) *Primary Power Receptacle, 3-wire* — Accepts power cord supplied with instrument.

(b) *Fuse Holder* — Fuse rating and primary supply voltage for the instrument are indicated beside the fuse holder.

(c) *Optional Location for Instrument Main Output Jack* — If equipped, the front panel output connector is inactive.

(d) *External Frequency Standard Input* — Accepts 5.000 000 or 10.000 000 MHz of 0.4-0.6V into 300 ohms to control instrument in connection with the following slide switch.

(e) *Slide Switch* — Selects the internal or an external frequency standard. It must be set to INT. STD if no external input is provided.

(f) *10 MHz Standard Frequency Output of 0.4V into 50 ohms* — This output may be used to drive other synthesizers without internal standard as *slaves.*

> **NOTE:** Either the 5/10 MHz input or the 10 MHz output can be used to synchronize a counter in a checkout of the instrument. For complete correspondence of dial settings and counter readings, synchronization is required or the difference in the two frequency standards will show up.

(g) *Program Connector* — Amphenol 57-40500 requires 57-30500 to control. The pin-out of the connector is given in Table 1. All functions connect directly to 74 type ICs. Connection to ground will enable all functions, which are negative true. To set the instrument to the local control mode for front-panel frequency-selection, either remove the remote control connector or make certain that pin 42 is *high.* This connector, via pin 22 and associated ground pin 21, also permits control of the output amplitude.

*Program Connector, GPIB:* See separate GPIB section.

(h) *Access Hole for Output Level Control* — (Remote units only)

**Remote Frequency/Level Control**

Both frequency and amplitude of the output can be remotely programmed. Further, the mode of frequency control, local or remote, is also programmable. If it is desired to go to remote frequency control, but do this locally, a switch from ground to pin 42 in the program connector will permit it. Table 1 lists all pertinent data for remote programming by parallel entry.

Amplitude programming by analog voltage is under front panel potentiometer control, but pin 22 of the program connector is wired in parallel. The panel pot is disconnected when the ccw end-switch is actuated. Units without manual (front panel) controls are supplied with a screwdriver-adjust 10 KΩ potentiometer to pre-set level, accessible from the rear panel.

Frequency programming is BCD-parallel *transparent* if the Latch Enable lines are left *high*. A TTL *low* on these lines will store the last command. The full control word may be broken up into separate bytes, such that serial loading is feasible. (Also see **Parallel Entry Board PE 1121,** page 16.)

**Frequency and amplitude programming via the IEEE 488 Bus is accomplished with the GPIB option, described in a separate section.**

## PRINCIPLES OF OPERATION

### General

An overview of the system is presented here by discussing the block diagram in Figure 4. Detailed module descriptions are found in subsequent sections. This material is essential for efficient service, and familiarity with it is assumed in the service instructions.

All output frequencies of the PTS 160 are derived from the crystal oscillator by arithmetic operations and are fully coherent with the standard 10 MHz frequency. The instrument uses a simplified direct synthesis in which all auxiliary fixed frequencies are produced from a 10 MHz pulse. The final output frequency comes from a beat-frequency system, as follows:

> A signal of 365 to 355 MHz, which carries all 0.1 Hz to 1 MHz steps, is subtracted from a 365 to 515 MHz signal which carries the 10 MHz steps. The resultant output ranges from 0.1 MHz to 160 MHz. The 0.1 MHz is the practical cutoff in the output amplifier; lower frequencies could otherwise be obtained. Strictly speaking, 160 MHz is not a settable output, but for simplicity in discussing bandwidths the 0.1 Hz difference is neglected.

The block diagram shows a crystal oscillator which is the prime reference in the system and three sections: a standard frequency section, a fine resolution section and a 10 MHz step section. An output amplifier completes the system.

### Standard Frequency Section

This section consists of the SGA and SGB modules; they provide all fixed standard frequencies needed and operate from an input of 10.000 MHz (or 5 MHz which is automatically doubled). For either input a filtered 10 MHz signal is fed to a pulse generator, where harmonics of 10 MHz up to 140 MHz are generated



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with equal amplitude. This *picket fence* is the basis for all fixed standard frequencies. The SGA and SGB modules supply: 112 and 113 MHz; 14, 16, 18, 20 and 22 MHz for use in the fine resolution section. The 10 MHz picket fence from the SGA module is also fed to the 10 MHz step section. The above frequencies all come from arithmetic operations on the original 10 MHz multiples.

**Fine Resolution Section**

This section may contain up to 7 DM modules ($10^{-1}$ to $10^5$ Hz steps), and most of the synthesis process is accomplished in these repetitive modules which are identical in design. They all operate *in series*, meaning that the output of a lower-order digit feeds the input of the next higher order digit-module. One further module is included in this section because it is nearly identical to the DM modules: The DMA module produces the 1 MHz steps. All DM modules use 112,113 MHz and 14 to 22 MHz.

The function of the series-connected DM modules is to produce frequency increments on a 14 MHz *carrier* in accordance with dial settings (or remote program) up to the 100 KHz step. If, for instance, a frequency of 0.543 210 MHz has been selected, the output of the DM which feeds the DMA is 14.543 210 MHz. The DMA module adds the 1 MHz steps and also transfers the information to a frequency which can carry a 10 MHz bandwidth more readily. The *carrier* at the output of the DMA is 140 MHz, and, if the above selection is expanded to, say, 6.543 210 MHz, then the output of the DMA is 146.543 210 MHz. A more complete description of this process is found in the DM module section of the manual.

**10 MHz Step Section**

In this section frequencies are used which are not standard-frequency-derived. Frequencies mentioned in previous paragraphs were all as accurate as the standard 10 MHz frequency. In this section the VCO frequencies from 365 to 515 MHz (in 10 MHz steps) may differ from their nominal values by as much as



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1 MHz; as will be shown, such deviation from the absolute value has no effect on the output frequency. The Stepped Oscillator operates in a drift cancelled loop which serves two functions:

1. Selection and filtering of one of fourteen 10 MHz pickets by a fixed 505 MHz filter.

2. Supply of frequencies high enough for the final mixer, with a high degree of coherence in the two mixer inputs.

The block diagram shows some of the VCO frequencies corresponding to certain 10 MHz steps as examples. These will be helpful in recognizing the complete synthesis process via a sample frequency.

If we return to our previously chosen sample frequency in the fine resolution section of 146.543 210 and assume that we have set the 10 MHz dials to 10, our complete frequency setting is 106.543 210 MHz. As shown in the block diagram for the *10* step the VCO will produce a frequency of 465 MHz, which is fed to two different mixers. In the mixer near the 505 MHz filter, the picket fence line of 40 MHz will add to the 465 MHz and feed 505 MHz through the filter and into the next mixer. After that mixer the lower sideband of 505 and 146.543 210 is filtered out by a 355 to 365 MHz bandpass filter; in this case the frequency is 358.456 790 MHz. This frequency enters the output mixer where it is subtracted from the VCO frequency of 465 MHz. The resultant difference is 106.543 210, our selected output frequency. After a low-pass filter the output frequency is amplified and fed to the output connector.

As can be seen, the VCO feeds both inputs to the final mixer, one directly and one after one intermediate mix. Therefore, if the VCO frequency deviates from nominal, *both* mixer inputs move up or down in frequency together by the same frequency increment. This obviously does not alter the difference of these two frequencies, which is the desired output frequency.



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## SERVICE

### General

No preventive maintenance is required for the PTS 160 frequency synthesizer. For convenience of service all modules are easily removed from the deck and replaced. It is the purpose of this section to provide information which, in case of malfunction, permits the identification of a defective module.

The preferred service procedure is the exchange and factory-service of the module. The individual module sections provide information for module service, should spare modules not be available for exchange.

### System Troubleshooting

Test equipment recommended for troubleshooting:

| | |
|---|---|
| RF-Voltmeter<br>V | 1-600 MHz, 10 mV - 1V, High Impedance Probe (3 pF, DC Res. 100 KΩ) |
| HF-Counter<br>C | 0-200 MHz or 0-20 MHz, 10 mV Sensitivity, High Impedance or 50 Ω input, 10 Hz Resolution; input for External Drive for Synchronization with 10 MHz, 0.5V into 50 Ω |
| Spectrum Analyzer<br>SA | 10-600 MHz, 50 Ω; min. 60 dB on-screen dyn. range. Max. BW 1 MHz; min. Sensitivity -40 dBm |
| Multimeter | Analog or Digital, 0-15V; 0.1V Resolution; 0-2A; 0.1A Resolution |

Test equipment is referenced in Table 2 as noted above (V, C, SA). The Voltmeter and Counter must have high DC input resistance since connection is made to points with +5.4V potential. The RF-Voltmeter probe connects directly to test points. The Counter is connected via a RG 174 or similar RF Cable equipped with small alligator clips.

If the instrument output is absent, proceed as follows. With instrument connected to line, power switch in the ON position, either the REMOTE or LOCAL indicator light should be on. Check fuse if no indication is obtained. Use only fuse of proper rating to replace. If indicator light is on, set instrument to the local mode (see **PRINCIPLES OF OPERATION**) and dial desired frequency; if no output is obtained, check rear panel output Standard Frequency, 10 MHz output. 0.4V into 50 ohms should be obtained. If no output is present (and the instrument is equipped with an internal standard and set to INT. STD.), the bottom cover of the instrument has to be removed. Disconnect unit from power line. Remove two screws holding the lip on the rear panel, two screws in the front of the case, and carefully withdraw cover. To fully withdraw from case, cover has to be deflected in the middle so that fold-down stand screws clear rear panel.

After unit is powered again, check for presence of supply voltages -12.4V (blue wire) and +5.4V (green wire) at the terminals of the power supply on the rear panel. If voltages are within ±0.2V, proceed; if voltage is absent or low, measure current in the leads from the supply. The proper 5.4V current is 1-1.25A; the proper 12.4V current is 0.8-1.0A, depending on resolution and crystal oven temperature. This test will isolate a faulty power supply, a short, or an overload in the instrument.

If the output is still absent or incorrect, the following tests are made with the aid of Table 2 which lists test points, signal frequencies and levels. Figure 5 shows location of test points.

To run a full diagnostic check, all test instruments with the upper frequency limits are required. It is possible, however, to test most of the instrument with the RF-Voltmeter and the 20 MHz Counter.

Proceeding from the crystal oscillator through the Standard Frequency Section and the Fine Resolution Section, most tests for presence of signal and proper frequency can be made *bridging*, without opening connections. These checks cover the bulk of the instrument. To check signals in the 10 MHz step section and the output amplifier, 50-ohm SMA connections will have to be made.



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## MAINFRAME COMPONENTS

### Power Supply

The power supply, operating from commercial power lines, generates DC voltages of +5.4V and −12.4V. The former is used for TTL and MECL logic (fed by decoupling networks), and the 12.4V powers the transistor amplifiers. Total current is 1.25A at 5.4V and 1.0A at 12.4V, approximately.

Both regulators operate from capacitor input filters, fed by silicon rectifier bridges. The series-pass transistor, gain- and reference-elements are integrated in a TO-3 package which is heat-sunk to the rear-panel. Both supplies are short circuit-proof with fold-back.

The transformer uses paralleled primaries for 120V use and switch-selected 100V, 120V, 220V and 240V inputs.

In case of malfunction use the schematic which lists essential DC voltages for both supplies to locate the faulty component or replace the supply-board as a unit.

### Crystal Oscillator

The PTS 160 may be supplied with a built-in oven-type or TCXO crystal oscillator operating at 10 MHz. It is mounted on the instrument rear panel and has the following charactersics:

| Type: | Oven Type | Moderate Stability TCXO |
|---|---|---|
| Frequency: | 10.000 000 MHz | |
| Aging: | $3 \times 10^{-9}$/day | $1 \times 10^{-8}$/day |
| Temperature Coefficient: | $\pm 2 \times 10^{-10}/^{o}C$ | $2 \times 10^{-8}/^{o}C$ |
| Output: | 1V RMS into 500 Ω | 1V RMS into 500 Ω |
| Warm-Up Time: | 24 hrs for $1 \times 10^{-8}$ | – |
| DC Supply: | −12.4V, 250 mA (500 mA turn-on) | −12.4V, 20 mA |



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### Parallel Entry Board PE 1121

This board, which is mounted to the rear panel and directly connected with the Amphenol 57 type program input connector, contains circuitry to interface the outside programming signals for frequency control with the digit modules in the instrument. It also effects the transfer from local to remote frequency control with the remote enable command. The programming format is parallel entry, 1, 2, 4, 8 BCD for each digit. TTL logic levels are used and all commands are negative true. The 74ALS533 type latches provide storage when this mode of operation is desired. To store a program input, Storage Enable pins must be brought to the *low* state. Table 1 indicates pin assignments in the last column. Note that five enable lines "LE" are provided so that serial operation with separate bytes is possible. With reference to Figure 7, U7 is used to control a switch consisting of two transistors. U7 accepts the remote enable signal which is normally negative true. In the Local mode, latches are set to the "off" (third) state, and 5.1V is supplied to the front-panel switches. Pin assignment in the 57-40500 connector is shown in Table 1.

**The GPIB interface which mounts to the rear panel, like the PE 1121 board, is treated in a separate section.**

### 505 MHz Filter (390-1000)

This 5-section cavity filter forms part of the 10 MHz step section. It is fixed-tuned and cannot be retuned in the field. The 390-1000 is bolted to the back lip of the deck.



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## TABLE 1. PTS 160 REMOTE FREQUENCY/LEVEL CONTROL

Amphenol 57-40500—On Equipment
Amphenol 57-30500—Required to Control

| Digit | | **Weight:** 1 | 2 | 4 | 8 | **Latch Enable** |
|---|---|---|---|---|---|---|
| | | *Pin Numbers* | | | | |
| 10 MHz | (0-15, Hexadecimal) | 15 | 16 | 40 | 41 | 23 |
| 1 MHz | (0-9, BCD; 10-15 Invalid) | 17 | 18 | 19 | 20 | 24 |
| 100 KHz | (0-9, BCD; 10-15 Invalid) | 1 | 2 | 26 | 27 | 24 |
| 10 KHz | (0-9, BCD; 10-15 Invalid) | 3 | 4 | 28 | 29 | 25 |
| 1 KHz | (0-9, BCD; 10-15 Invalid) | 5 | 6 | 30 | 31 | 25 |
| 100 Hz | (0-9, BCD; 10-15 Invalid) | 7 | 8 | 32 | 33 | 46 |
| 10 Hz | (0-9, BCD; 10-15 Invalid) | 9 | 10 | 34 | 35 | 46 |
| 1 Hz | (0-9, BCD; 10-15 Invalid) | 11 | 12 | 36 | 37 | 47 |
| 0.1 Hz | (0-9, BCD; 10-15 Invalid) | 13 | 14 | 38 | 39 | 47 |

Remote Enable = Pin 42
Ground = Pin 50
All functions are negative true, TTL.
Levels: Low, +0.7V max
High, +2.0-5.0V

ANALOG LEVEL CONTROL

Remote-Level = Pin 22
(Ground = Pin 21)

RMS output = 0.5 × pos. DC Control voltage
(e.g. 1VRMS output ÷ 2.0VDC)

NOTE: Remote level input impedance is approximately 10K ohms (front panel pot end switch actuated). Remote only units approximately 1.5K ohms, see page 8 and PE 1121 schematic.



b

## TABLE 2. SYSTEM TROUBLESHOOTING

| Step | Test Point | Frequency (MHz) | Level | Test Equipment | Module Checked | Notes |
|---|---|---|---|---|---|---|
| 1 | SGA, 51 | 10.000 | 0.4V | V, C | Freq. Std. Drive | |
| 2 | SGA, 49 | 10.000 | 0.4V | V, C | SGA | |
| 3 | SGA, 20 | 18.000 | 0.1V | V, C | SGA | |
| 4 | SGA, 43 | 20.000 | 0.1V | V, C | SGA | |
| 5 | SGA, 6 | 22.000 | 0.1V | V, C | SGA | |
| 6 | SGA, 2 | 33.000 | 90 mV | V, C | SGA | |
| 7 | SO, J1 | 10-140 | -17 dBm | SA | SGA | 4 |
| 8 | SGB, 10 | 14.000 | 0.1V | V, C | SGB | |
| 9 | SGB, 24 | 16.000 | 0.1V | V, C | SGB | |
| 10 | DMA, 1 | 112.000 | 0.1V | V, C | SGB | 2 |
| 11 | DMA, 10 | 113.000 | 0.1V | V, C | SGB | 3 |
| 12 | DM, 50 (all) | 14.000 | 0.25V | V, C | DM | 2 |
| 13 | DMA, 50 | 140.000 | 0.40V | V, C | DMA | 2 |
| 14 | Filter-Output | 505 ± 1 | -35 dBm | SA | SO, F | 5 |
| 15 | IM, J3 | 365 ± 1 | -16 dBm | SA | IM | 2 |
| 16 | SO, J3 | 100.000 | -25 dBm | SA | SO | 2 |
| 17 | OA, J1 | 100.000 | +13 dBm | SA | OA | 2 |

Notes:

1. Test point designations show the module type and the pin number (position) of the board-edge connector, as used on the module schematic and Figure 5.
2. Set instrument to 100.000 000 0 MHz
3. Set instrument to 101.000 000 0 MHz

   1V output (set-level volt. = +2 VDC

4. Remove SO module, connect SA in place of SO, J1. Each 10 MHz multiple from 10 to 140 MHz to be displayed.
5. Set instrument to all 10 MHz steps (0 - 150).

# PS-1019 PARTS LIST

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 4,700$\mu$F, 25V | 31-5104 |
| C2 | 6.8$\mu$F, 16V | 30-5101 |
| C3 | 6.8$\mu$F, 16V | 30-5101 |
| C4 | 10,000$\mu$F, 16V | 31-5102 |
| C5 | 6.8$\mu$F, 16V | 30-5101 |
| C6 | 6.8$\mu$F, 16V | 30-5101 |
| | **RESISTORS** | |
| R1 | 1.5 K$\Omega$, 5%, ¼W | 11-0152 |
| R2 | 243$\Omega$, 1%, ¼W | 14-5105 |
| R3 | 1 K$\Omega$, Pot., 10%, .75W | 17-5104 |
| R4 | 590$\Omega$, 1%, ¼W | 14-5112 |
| R5 | 243$\Omega$, 1% ¼W | 14-5105 |
| R6 | 500$\Omega$, Pot., 10%, .75W | 17-5103 |
| | **DIODES** | |
| CR1 | 3A, 100V | 74-5100 |
| CR2 | 3A, 100V | 74-5100 |
| CR3 | 3A, 100V | 74-5100 |
| CR4 | 3A, 100V | 74-5100 |
| CR5 | 3A, 100V | 74-5100 |
| CR6 | 3A, 100V | 74-5100 |
| CR7 | 3A, 100V | 74-5100 |
| CR8 | 3A, 100V | 74-5100 |
| | **INTEGRATED CIRCUITS** | |
| U1 | LM350K | 64-0350K |
| U2 | LM350K | 64-0350K |
| | **TRANSFORMERS** | |
| T1 | 50-400 Hz | 83-5102 |



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# PE-1121 PARTS LIST

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1-C7 | 50 nF, 80/20, 50V, Z5V | 23-0503 |
| C8 | 6.8 $\mu$F, 25V | 30-5101 |
| | **RESISTORS** | |
| R1 | 2.2 $\Omega$, 5%, 1/4W | 11-1220 |
| R2 | 2.2 $\Omega$, 5%, 1/4W | 11-1220 |
| R3 | 10K $\Omega$, Pot., 10%, 1/2W (For remote-only units) | 16-5101 |
| R4 | 4.7K $\Omega$, 5%, 1/4W | 11-0472 |
| R5 | 1K $\Omega$, 5%, 1/4W | 11-0100 |
| R6 | 4.7K $\Omega$, 5%, 1/4W | 11-0472 |
| R7 | 2.2K $\Omega$, 5%, 1/4W | 11-0222 |
| R8-R10 | 2.2K $\Omega$, 5%, 1/4W (Optional-attenuator) | 11-0222 |
| R11 | 680 $\Omega$, 5%, 1/4W (Optional-attenuator) | 11-0681 |
| A1-A9 | Resistor Network, 2.2K $\Omega$, 2%, | 66-5002 |
| | **TRANSISTORS** | |
| Q1-Q2 | 2N 2905 | 42-2905 |
| | **INTEGRATED CIRCUITS** | |
| U1-U6 | 74ALS533 | 61-5102 |
| U7 | 74LS05 | 63-0005 |
| | **CONNECTORS** | |
| J1 | 50 pos. conn. (series 57 compatible) | 78-1000 |
| J2 | 50 pos. conn. (Optional) | 78-1000 |



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## CABINET DIMENSIONS

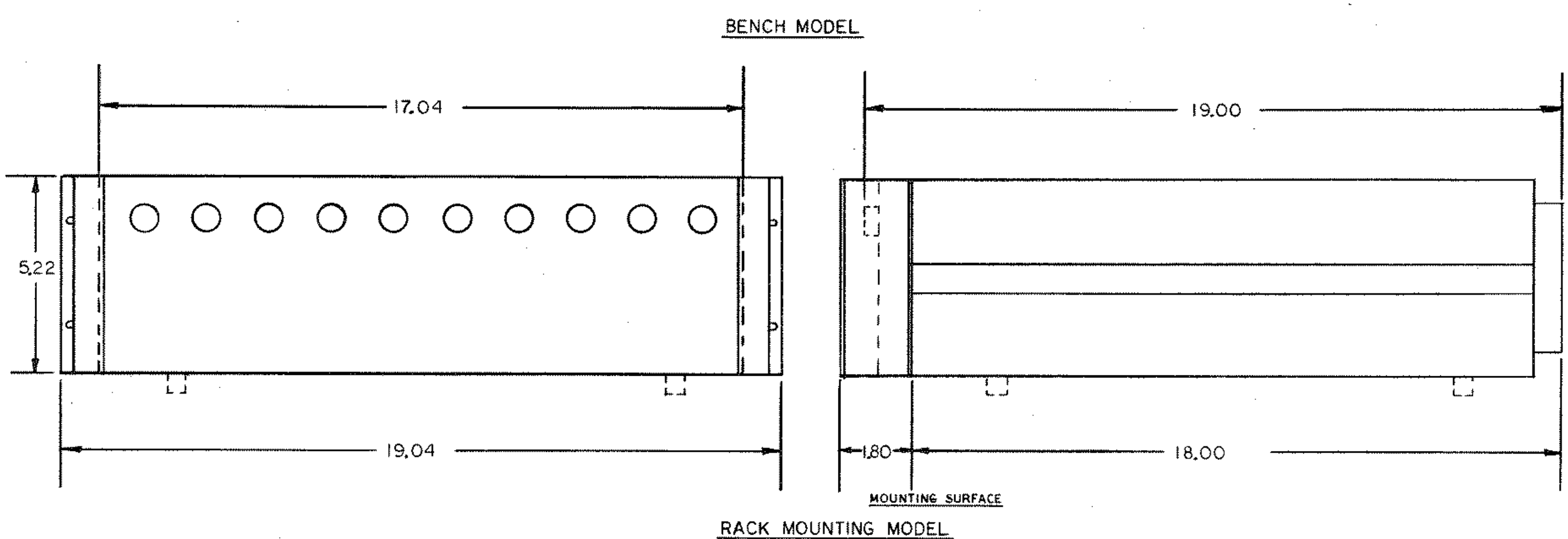


Figure 1



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## FRONT PANEL

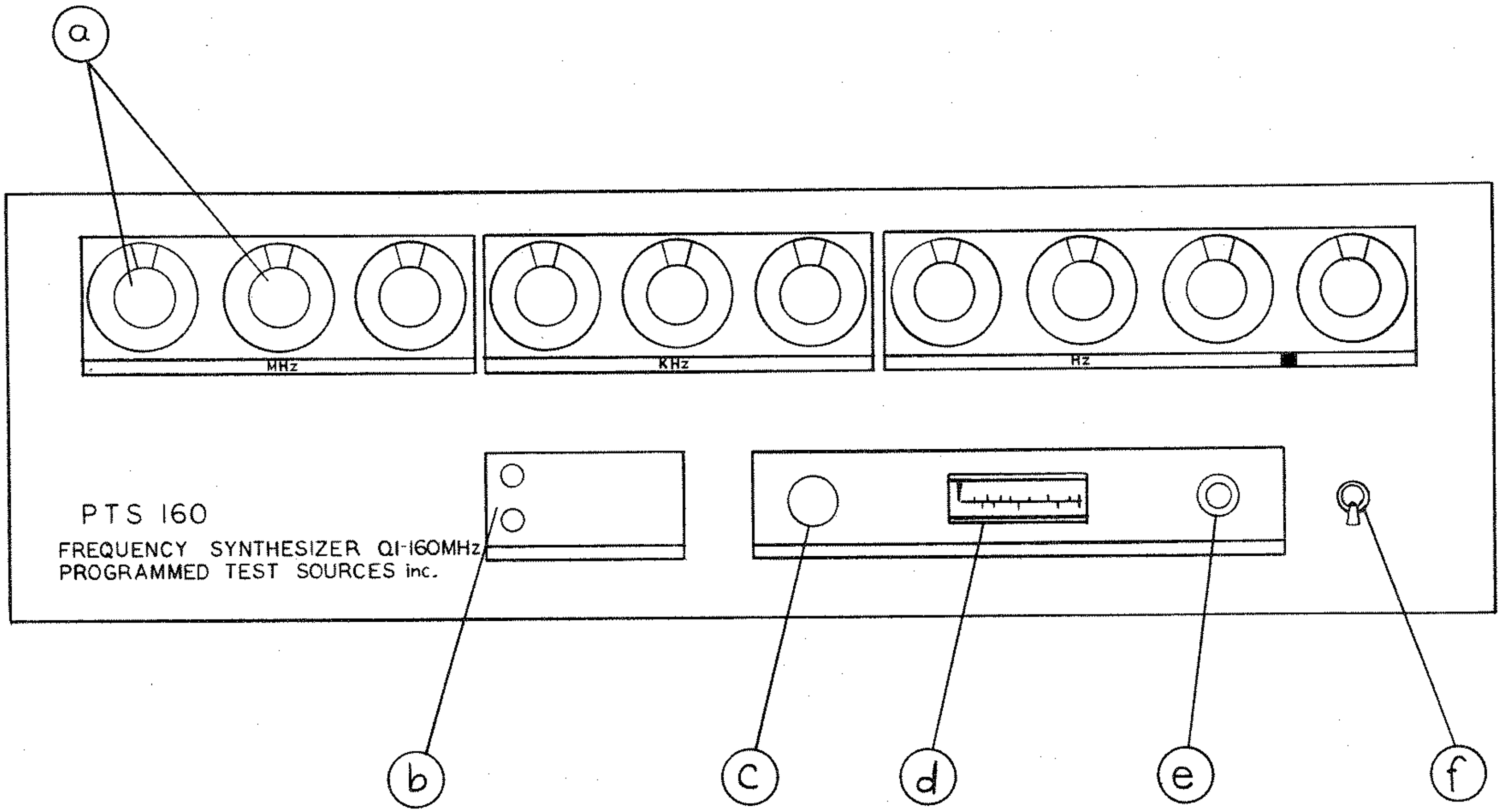



**Figure 2**

# REAR PANEL CONTROLS

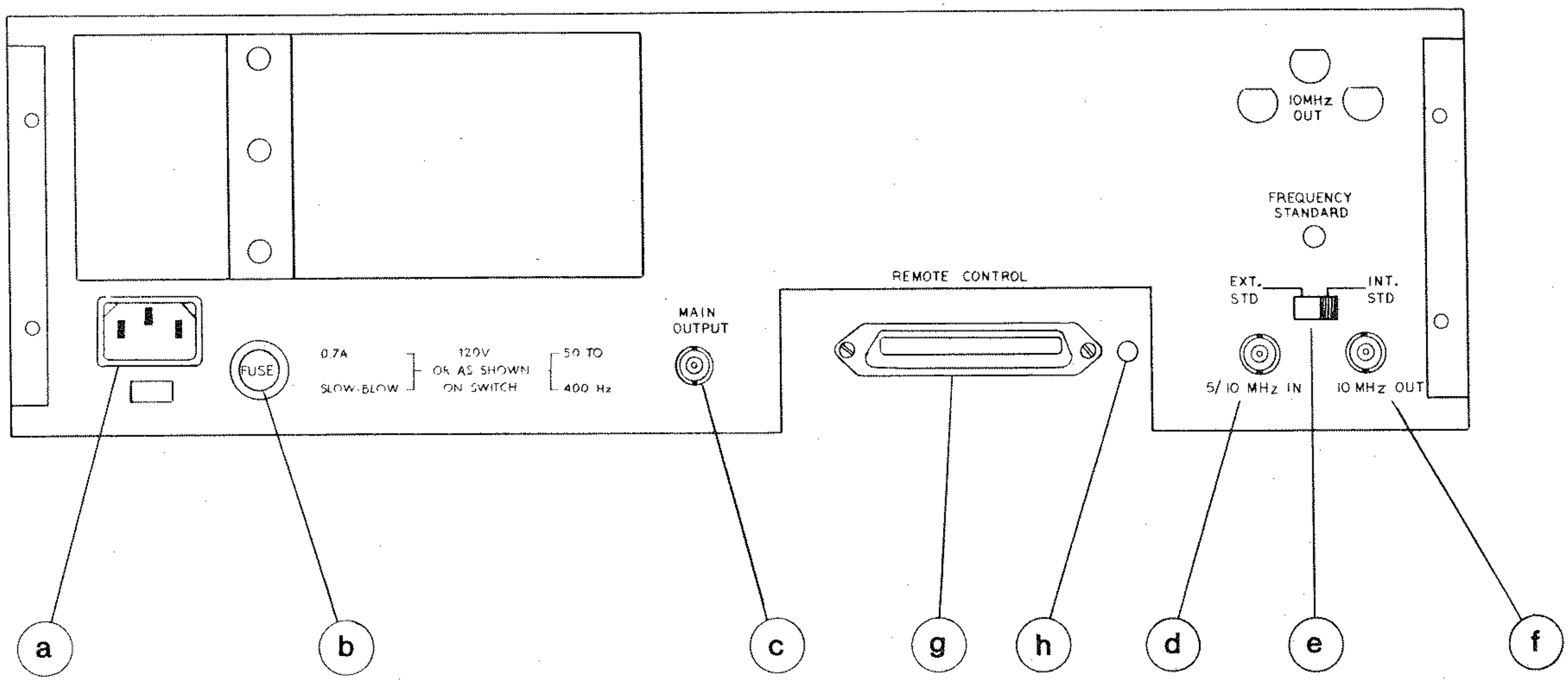
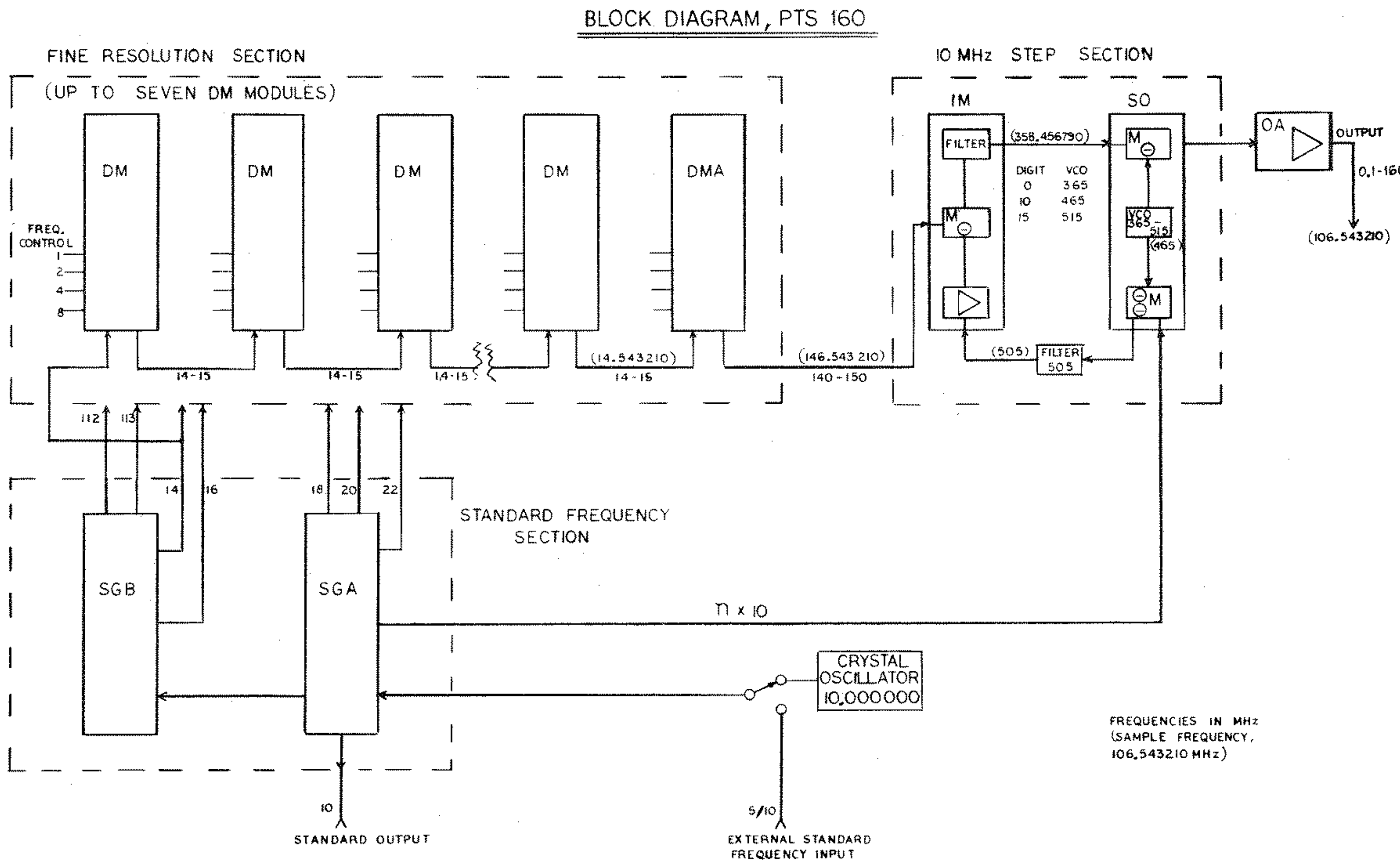



Figure 3



c



BLOCK DIAGRAM, PTS 160
FINE RESOLUTION SECTION
(UP TO SEVEN DM MODULES)
DM
DM
DM
DM
DMA
FREQ. CONTROL
1
2
4
8
14-15
14-15
1,4-15
(14.543210)
14-15
(146.543 210)
140-150
10 MHz STEP SECTION
IM
SO
FILTER
(358.456790)
DIGIT VCO
0 365
10 465
15 515
VCO 365-515
(465)
(505)
FILTER 505
OA
OUTPUT
0,1-160
(106.543210)
112
113
14
16
18
20
22
STANDARD FREQUENCY SECTION
SGB
SGA
n x 10
CRYSTAL OSCILLATOR 10,000000
FREQUENCIES IN MHz (SAMPLE FREQUENCY, 106.543210 MHz)
10
STANDARD OUTPUT
5/10
EXTERNAL STANDARD FREQUENCY INPUT


Figure 4



a

LOCATION OF TEST POINTS
(BOTTOM VIEW OF DECK)

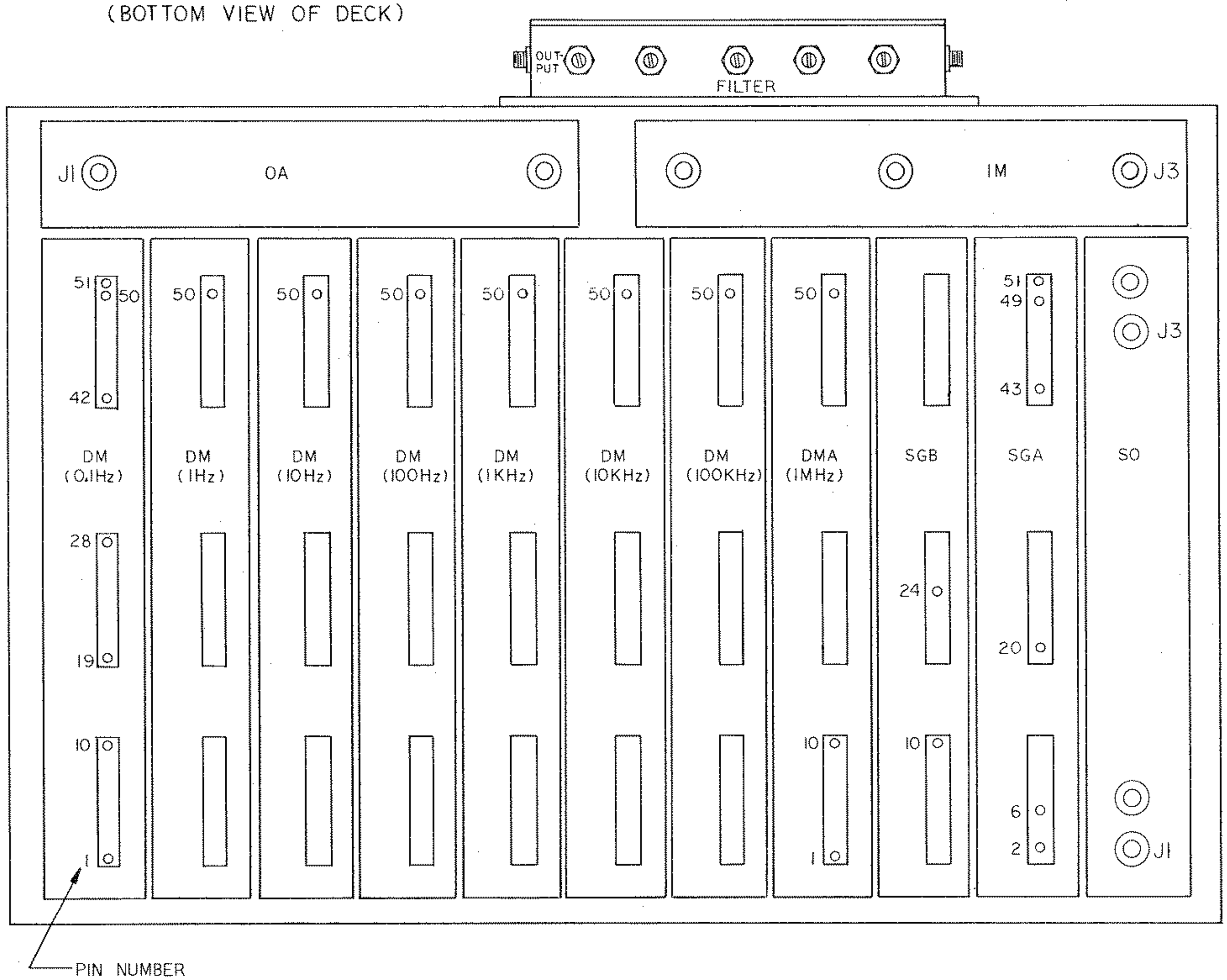



Figure 5



a

## SCHEMATIC, PS-1019

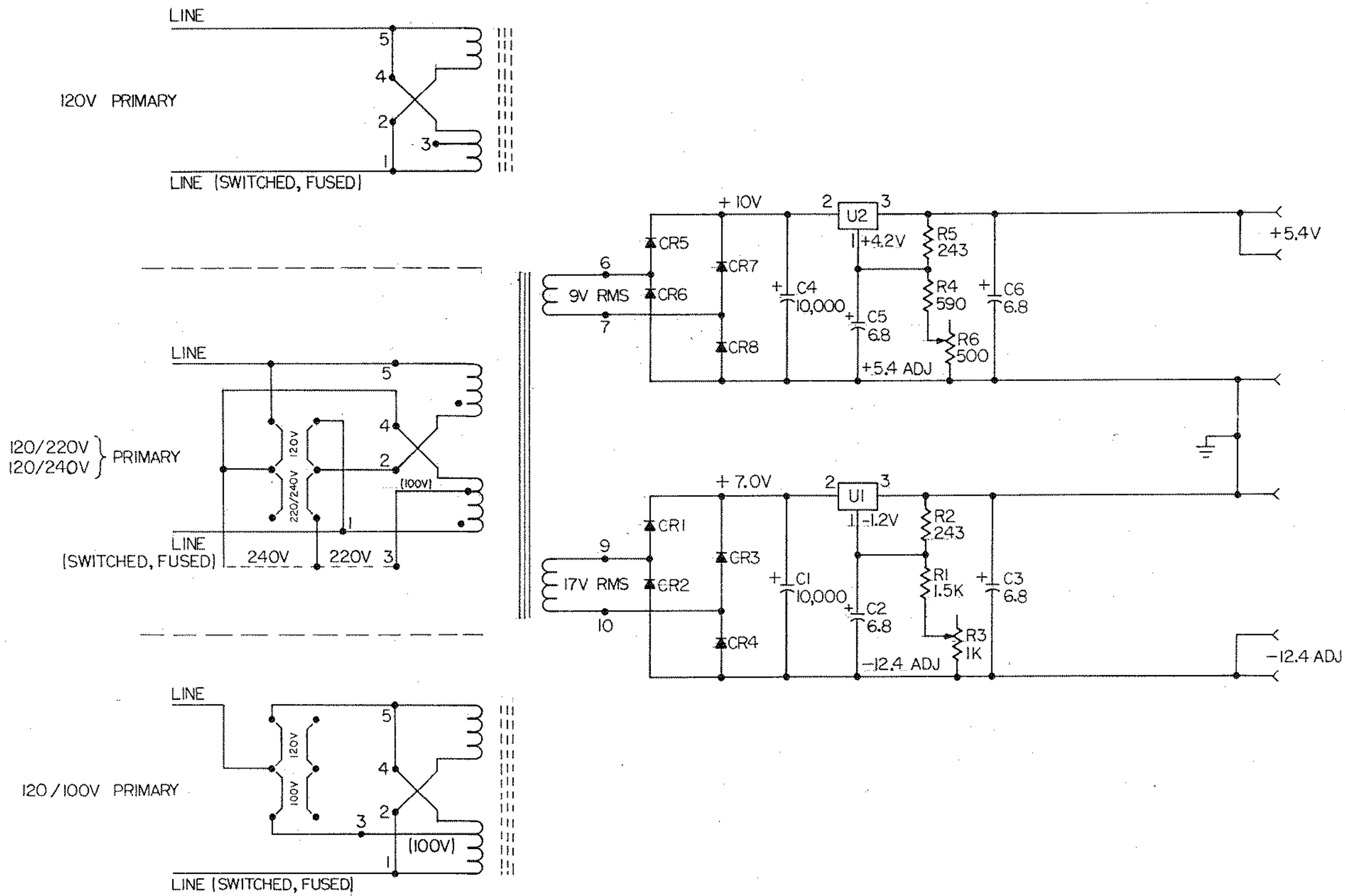
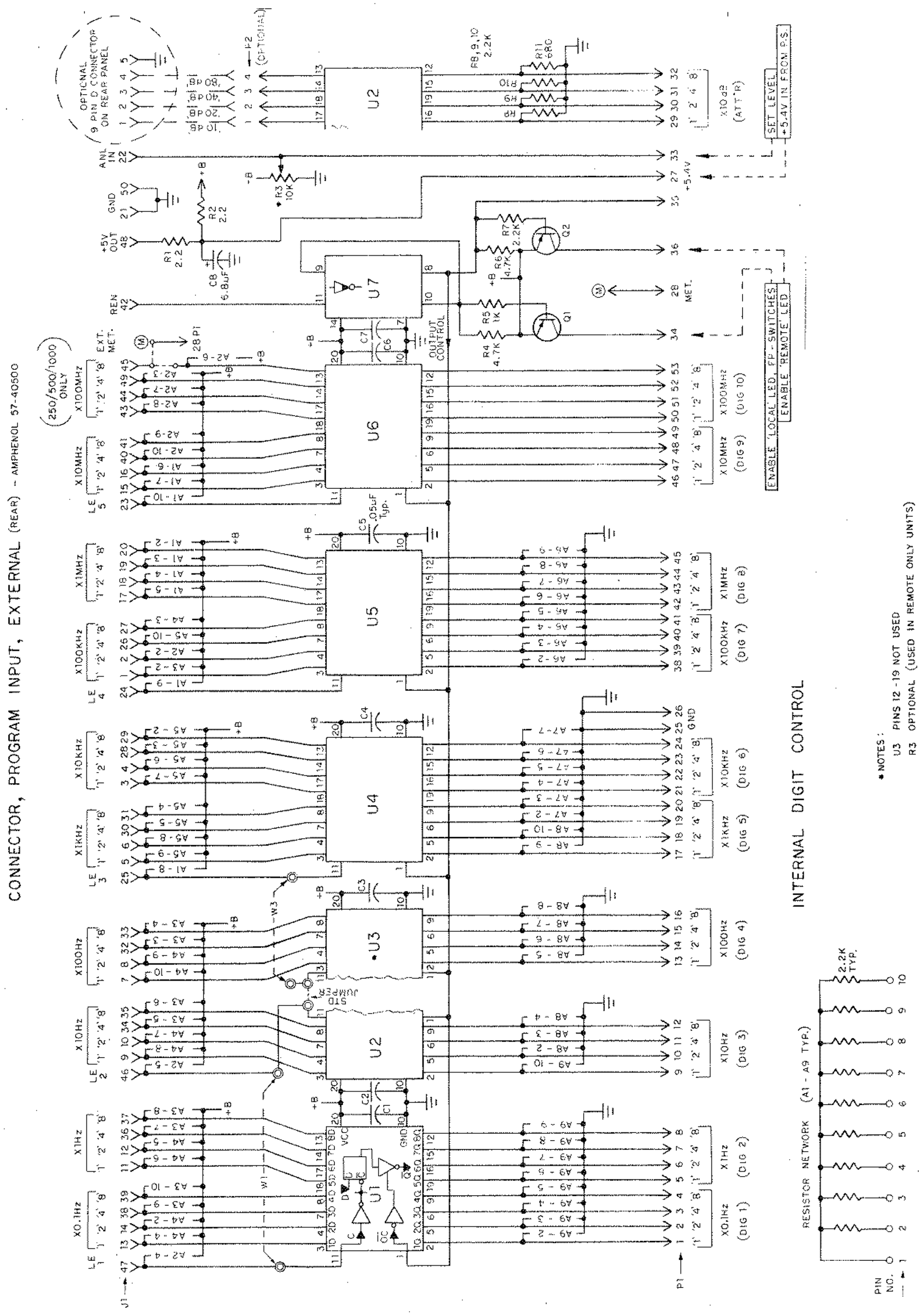



Figure 6



b



CONNECTOR, PROGRAM INPUT, EXTERNAL (REAR) - AMPHENOL 57-40500
INTERNAL DIGIT CONTROL
OPTIONAL 9 PIN D CONNECTOR ON REAR PANEL
RESISTOR NETWORK (A1 - A9 TYP.)
• NOTES:
U3 PINS 12-19 NOT USED
R3 OPTIONAL (USED IN REMOTE ONLY UNITS)
ENABLE 'LOCAL' LED, FP SWITCHES
ENABLE 'REMOTE' LED
SET LEVEL
+5.4V IN FROM P.S.


Figure 7



a

## NON-RF WIRING DECK

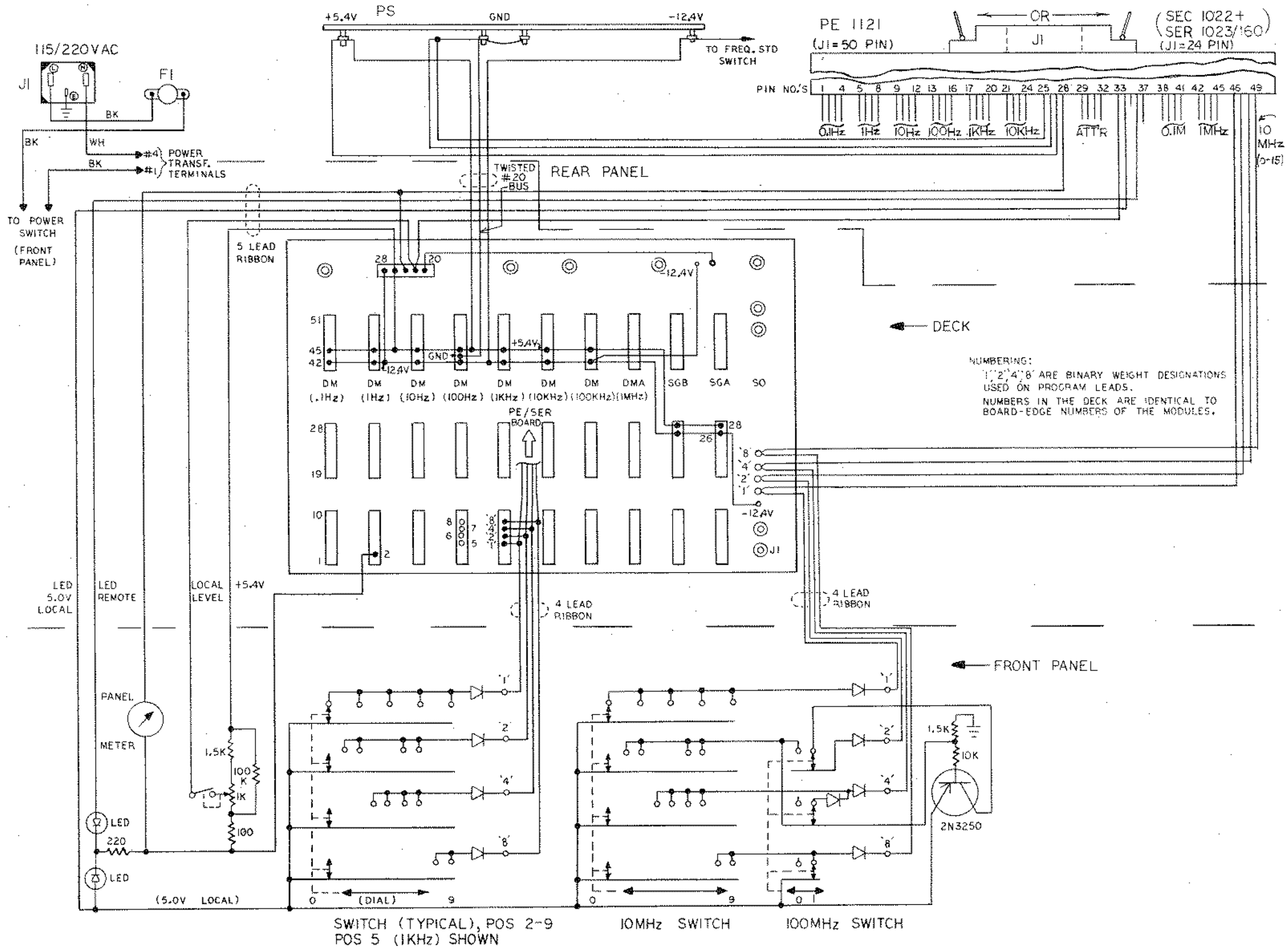
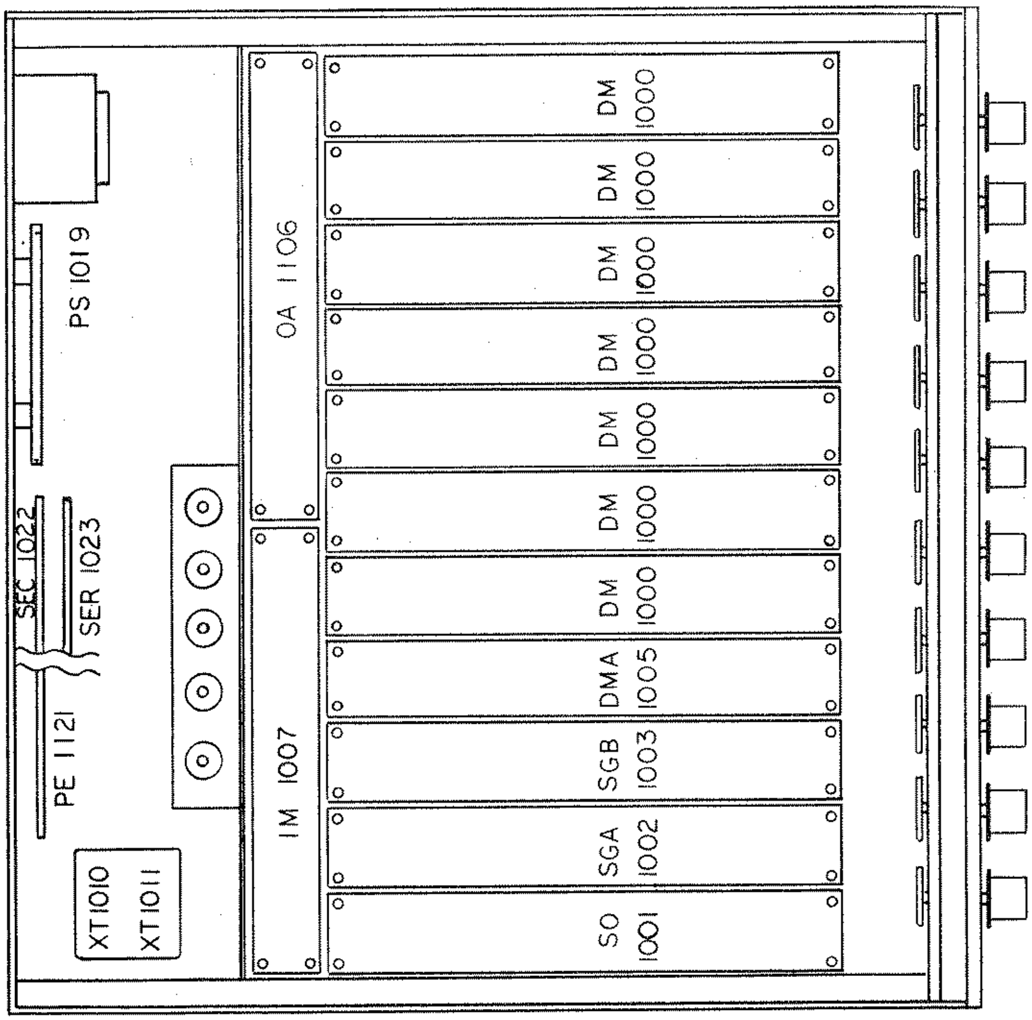



Figure 8



b

PTS 160 MODULE LOCATION






a

## TABLE OF CONTENTS

## INTRODUCTION

The DM-1000 is used repetitively, up to seven times per instrument, to synthesize, according to external command, all digits from the 0.1 Hz to the 100 KHz step. The actual number of DMs used is dependent on the resolution option (smallest frequency step) of the synthesizer: For 0.1 Hz steps seven DMs are needed; for reduced resolution the number decreases by one DM for each digit.

All DMs in the instrument operate in series; each module restores the signal to a normal output level independent of the level of input signals above a threshold. Although all DMs are identical and produce at their output 100 KHz steps, these steps are reduced to the proper significance by the repeated division in the chain. The module combines analog, VHF and digital techniques. It is programmed through four parallel lines in BCD. All inputs and outputs are fed through card-edge connectors with multiple low-inductance grounds provided for the RF signals. All DM-1000s are interchangeable; however, they are not interchangeable with the DMA-1005 or any other module in the synthesizer.

The digit module is of plug-in design and uses three ten-pin connectors with asymmetric spacing assuring proper orientation; it is secured with three 6-32 screws from the bottom of the deck. Housed in a frame and U-cover enclosure, the DM-1000 can be removed as a complete unit after releasing the 6-32 pan-head screws. The printed-circuit board may also be removed separately from the enclosure, after the four cover screws (4-40) on top have been released and the cover has been lifted off. Holes near the top corners of the board facilitate prying the board up and free of the connectors by using a small tool alternately on both sides.



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## PRINCIPLES OF OPERATION

The block diagram of Figure 1 shows a series-string of DM modules, which produce digit steps in a PTS synthesizer. The direction of signal flow in this string of modules is from the least significant to the most significant digit. The input to the first DM in the chain is 14.000 MHz from the 14 MHz bus in the deck; as the frequency is processed, it always remains between 14 and 15 MHz passing from one DM to the next.

The DM module has the following arithmetic capabilities: When receiving a frequency of 14.xyz . . . MHz from the predecessor, it will produce an output frequency of 14.axyz . . . MHz, where "a" directly corresponds to the dial setting (digit control) of the module. In other words, all digits behind the decimal point are moved to the right by one position (reduced in significance by ten), and a new 100 KHz step, as selected by the digit control (manual or remote), is placed ahead of the received digits.

The block diagram of Figure 2 shows the DM-1000 module. Apart from the input and output, the module is connected to the following fixed bus frequencies: 112 MHz, 113 MHz, 14, 16, 18, 20, 22 MHz, which are all crystal-oscillator-derived and coherent. For any one digit selection, the DM uses either 112 or 113 MHz and one of the five lower frequencies. 112 or 113 MHz is used to make even or odd digits; 14 MHz is used with digits 0,1; 16 MHz with digits 2,3; 18 MHz with digits 4,5, and so on.

To illustrate the operation, the block diagram (Figure 2) shows as a sample all frequencies which are internally produced in a DM, if it receives an input of 14.210 MHz and is set to digit "3". With the aid of the schematic of Figure 3, the circuitry used to effect the arithmetic may be traced.

14.210 MHz as received on pin 3 is fed to the base of Q10, an additive mixer. Digit control pins 5 and 6 (weight 1 and 2) are "high" if a "3" is selected, and decoder-ICs U1 and U2 furnish two DC outputs: "3" being odd, Q2, the 113



a

MHz switch, is turned on; and, since "3" belongs to the second pair of ten frequencies (2,3), Q5, which controls 16 MHz, is turned on.

113 MHz reaches the base of Q10 via C28. The upper sideband (sum) of the two inputs to Q10, 14.210 MHz and 113 MHz, is 127.210 MHz. Two double-tuned filters and amplifier Q11, which have a passband of 126-128 MHz, deliver this frequency to the input of the second mixer Q8/Q9.

T1 is connected to the output of switch-transistors Q3 to Q7, and, since Q5 is turned on, 16 MHz is the other input to the second mixer. Again, the circuits following are tuned to select the upper sideband, which is between 140 and 150 MHz. Our specific sample signal is 127.210 MHz plus 16 MHz, or 143.210 MHz. The filters suppress the lower sideband and other unwanted products. After amplification, the signal reaches U3, which is a digital divide-by-ten IC. The output is filtered by a tuned circuit, and a signal of 14.3210 MHz is fed to pin 50. As we see, a "3" has been placed ahead of "210", and the latter digits have moved one position to the right. In this fashion, a multi-digit number is synthesized.

## MODULE SPECIFICATIONS

| | | |
|---|---|---|
| Inputs: | 14 - 15 MHz | 0.20 - 0.35V |
| | 112, 113 MHz | 0.10 - 0.17V |
| | 14,16,18,20,22 MHz | 90 - 125 mV |
| Output: | 14 - 15 MHz | 0.25 - 0.31V nominal |
| | | 0.20V minimum |
| | | Load: 1.3 KΩ parallel 30 pF |
| Programming: | 1,2,4,8 BCD, positive true | |
| | High: 3.0V minimum | Low: 0.5V maximum |
| Spurious Outputs: | –75 dB | |
| Power: | +5.4V, 100 mA ±10% | –12.4V, 38 mA ±10% |
| Operating Temp: | 0 - 60°C | |



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## SERVICE

### Maintenance

No preventive maintenance is required for DM modules. The presence of an output signal of correct frequency and level indicates that the module is operating properly. The output of the module is produced directly by an IC divider. A 10 dB window exists at the divider input, and minor aging effects will, therefore, not impair operation.

Replacement of faulty components requires careful use of printed-circuit repair techniques as applicable to double-sided boards with plated-through holes.

### Alignment

Complete alignment of this module is made at the factory with a special test-set. Restoring the alignment after replacement of individual parts in the field is possible. It is recommended that voltages given in the Troubleshooting Procedure be used and that, in general, touch-up alignment be performed only on those tuned circuits which may have been altered by the parts replacements. Replacement of semiconductors will not necessitate realignment of tuned circuits in general.

### Troubleshooting Procedure

The System Section of this manual provides information to isolate faulty modules. It is important to follow the procedure given in detail to ensure that all the common supply frequencies are present before attempting to repair modules.

If a DM module has been isolated as faulty, the preferred service mode is exchange and factory repair. When immediate service is needed, the following procedure may be used.

Test Equipment Required:

| | |
|---|---|
| RF Voltmeter | 1 - 300 MHz, 10 mV - 1V, High Impedance Probe (3 pF, DC Res 100 KΩ) |
| HF Counter | 0 - 200 MHz, 10 mV Sensitivity, High Impedance or 50 Ω Input |

The output of the DM module is on pin 50, which is also the test point designation used in the System Section and the running number of the board-edge connector as shown on the schematic (Figure 3). The module produces 14.000 MHz at a level of 0.2 - 0.35V into the next DM module if all instrument dials have been set to zero. As the dial of the module under test is changed through successive numbers 0 to 9, the output frequency should change in 100 KHz steps from 14.000 MHz to 14.900 MHz. If the output is of the proper frequency but low in level, the output tank L10/C62 or the tuning should be checked. C62 is peaked at a setting of 5 (14.500 MHz). Only the voltmeter probe must remain connected to pin 50 for final tuning.

Absence of output for some dial settings points to specific causes:

1. No output on *two* successive even-odd digits (e.g., 2,3) indicates that the second mixer, Q8, Q9 does not receive one of the low bus frequencies from 14 to 22 MHz, and the fault is likely located in the switch section (Q3 to Q7). 14 MHz is used for digit 0,1; 16 MHz for digit 2,3, and so on.

2. No output on either *all odd* or *all even* digits will result from failure in the 112/113 MHz switches Q1 or Q2, since 112 MHz is used to produce all even digits and 113 MHz to make the odd digits.

3. If no output is obtained on any digit, if random digits are missing, or if an unsteady counter reading (noise) is present, the divider (U3) is



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faulty or the input on pin 7 is low. 0.2V minimum is to be read at this point with only the voltmeter connected. If the above checks (1 and 2) were positive, then part of the circuitry that is used on all digits must be faulty. The active devices are Q10, Q11, Q8, Q9 and Q12. DC operating conditions on all of these transistors are such that 1.1 to 1.5V should be measured across their emitter resistors R40, R45, R34 and R48.

RF voltages at various stages are given to permit further localization of the trouble. The previously indicated level of 0.2V into pin 7 of the divider is a minimum; other voltages may differ from normal by ±3 dB.

| | |
|---|---|
| Base Q10 | 0.10V |
| Base Q11 | 0.05V |
| C23/C24 | 0.50V |
| Base Q12 | 0.07V |
| U3, Pin 7 | 0.28V |

The 126-128 MHz signal at C23/C24 peaks at digit setting "5" and drops approximately 2 dB for settings "0" and "9" on the preceding DM module (less significant digit). Voltage at pin 7 of U3 responds to digit settings on the DM under test, and the minimum voltage must be obtained for all settings.



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## PARTS LIST

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C2 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C3 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C4 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C5 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C6 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C7 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C8 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C9 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C10 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C11 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C12 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C13 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C14 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C15 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C16 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C17 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C18 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C19 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C20 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C21 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C22 | 68 pF, 5%, 500V, N750 | 21-0680 |
| C23 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C24 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C25 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C26 | 27 pF, 5%, 500V, NPO | 20-0270 |
| C27 | 1-10 pF, Trimmer | 26-5100 |
| C28 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C29 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C30 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C31 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C32 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C33 | 1-10 pF, Trimmer | 26-5100 |
| C34 | 0.68 pF, .25 pF, 500V, NPO | 24-2680 |
| C35 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C36 | 1-10 pF, Trimmer | 26-5100 |
| C37 | 5 pF, .25%, 500V, NPO | 20-1500 |
| C38 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C39 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |



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## PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS (continued)** | |
| C40 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C41 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C42 | 1-10 pF, Trimmer | 26-5100 |
| C43 | 0.68 pF, .25 pF, 500V, NPO | 24-2680 |
| C44 | 1-10 pF, Trimmer | 26-5100 |
| C45 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C46 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C47 | 1-10 pF, Trimmer | 26-5100 |
| C48 | 3.3 pF, 5%, 500V, NPO | 20-1330 |
| C49 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C50 | 1-10 pF, Trimmer | 26-5100 |
| C51 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C52 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C53 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C54 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C55 | 1-10 pF, Trimmer | 26-5100 |
| C56 | 2.2 pF, .25 pF, 500V, NPO | 20-1220 |
| C57 | 5.0 pF, 25%, 500V, NPO | 20-1500 |
| C58 | 1-10 pF, Trimmer | 26-5100 |
| C59 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C60 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C61 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C62 | 1-10 pF, Trimmer | 26-5100 |
| C63 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C64 | 68 pF, 5%, 500V, N750 | 21-0680 |
| | **INDUCTORS** | |
| L1 | 50 nH, nom. | 35-5100 |
| L2 | 50 nH, nom. | 35-5100 |
| L3 | 50 nH, nom. | 35-5100 |
| L4 | 50 nH, nom. | 35-5100 |
| L5 | 50 nH, nom. | 35-5100 |
| L6 | 50 nH, nom. | 35-5100 |
| L7 | 50 nH, nom. | 35-5100 |
| L8 | 50 nH, nom. | 35-5100 |
| L9 | 50 nH, nom. | 35-5100 |
| L10 | 5.6 μH, 20% | 36-5100 |



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# PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **RESISTORS** | |
| R1 | 10 KΩ, 5%, ¼W | 11-0103 |
| R2 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R3 | 15 Ω, 5%, ¼W | 11-0150 |
| R4 | 680 Ω, 5%, ¼W | 11-0681 |
| R5 | 47 Ω, 5%, ¼W | 11-0470 |
| R6 | 1 KΩ, 5%, ¼W | 11-0102 |
| R7 | 10 KΩ, 5%, ¼W | 11-0103 |
| R8 | 15 Ω, 5%, ¼W | 11-0150 |
| R9 | 680 Ω, 5%, ¼W | 11-0681 |
| R10 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R11 | 1 KΩ, 5%, ¼W | 11-0102 |
| R12 | 47 Ω, 5%, ¼W | 11-0470 |
| R13 | 47 Ω, 5%, ¼W | 11-0470 |
| R14 | 680 Ω, 5%, ¼W | 11-0681 |
| R15 | 10 KΩ, 5%, ¼W | 11-0103 |
| R16 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R17 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R18 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R19 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R20 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R21 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R22 | 1 KΩ, 5%, ¼W | 11-0102 |
| R23 | 1 KΩ, 5%, ¼W | 11-0102 |
| R24 | 1 KΩ, 5%, ¼W | 11-0102 |
| R25 | 1 KΩ, 5%, ¼W | 11-0102 |
| R26 | 1 KΩ, 5%, ¼W | 11-0102 |
| R27 | 330 Ω, 5%, ¼W | 11-0331 |
| R28 | 330 Ω, 5%, ¼W | 11-0331 |
| R29 | 330 Ω, 5%, ¼W | 11-0331 |
| R30 | 330 Ω, 5%, ¼W | 11-0331 |
| R31 | 330 Ω, 5%, ¼W | 11-0331 |
| R32 | 47 Ω, 5%, ¼W | 11-0470 |
| R33 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R34 | 220 Ω, 5%, ¼W | 11-0221 |
| R35 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R36 | 15 Ω, 5%, ¼W | 11-0150 |
| R37 | 680 Ω, 5%, ¼W | 11-0681 |
| R38 | 1.5 KΩ, 5%, ¼W | 11-0152 |

PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | RESISTORS (continued) | |
| R39 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R40 | 330 Ω, 5%, ¼W | 11-0331 |
| R41 | Not Used | ----- |
| R42 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R43 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R44 | 15 Ω, 5%, ¼W | 11-0150 |
| R45 | 330 Ω, 5%, ¼W | 11-0331 |
| R46 | 6.8 KΩ, 5%, ¼W | 11-0152 |
| R47 | 1.5 KΩ, 5%, ¼W | 11-0682 |
| R48 | 150 Ω, 5%, ¼W | 11-0151 |
| R49 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R50 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R51 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R52 | 680 Ω, 5%, ¼W | 11-0681 |
| R53 | 470 Ω, 5%, ¼W | 11-0471 |
| R54 | 470 Ω, 5%, ¼W | 11-0471 |
| R55 | 15 Ω, 5%, ¼W | 11-0150 |
| R56 | 15 Ω, 5%, ¼W | 11-0150 |
| R57 | 33 Ω, 5%, ¼W | 11-0330 |
| R58 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R59 | 100 Ω, 5%, ¼W | 11-0101 |
| R60 | 100 Ω, 5%, ¼W | 11-0101 |
| R61 | 100 Ω, 5%, ¼W | 11-0101 |
| R62 | 1.0 KΩ, 5%, ¼W | 11-0102 |
| R63 | 330 Ω, 5%, ¼W | 11-0331 |
| | TRANSISTORS | |
| Q1 | 2N 3250 | 41-3250 |
| Q2 | 2N 3250 | 41-3250 |
| Q3 | 2N 3250 | 41-3250 |
| Q4 | 2N 3250 | 41-3250 |
| Q5 | 2N 3250 | 41-3250 |
| Q6 | 2N 3250 | 41-3250 |
| Q7 | 2N 3250 | 41-3250 |
| Q8 | 2N 2369 | 40-2369 |



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PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **TRANSISTORS (continued)** | |
| Q9 | 2N 2369 | 40-2369 |
| Q10 | 2N 2369 | 40-2369 |
| Q11 | 2N 5179 | 40-5179 |
| Q12 | 2N 5179 | 40-5179 |
| | **TRANSFORMERS** | |
| T1 | Transformer, RF | 84-5100 |
| | **DIODES** | |
| CR1 | BA 244 | 71-0244 |
| CR2 | BA 244 | 71-0244 |
| CR3 | BA 244 | 71-0244 |
| CR4 | BA 244 | 71-0244 |
| CR5 | BA 244 | 71-0244 |
| CR6 | BA 244 | 71-0244 |
| | **INTEGRATED CIRCUITS** | |
| U1 | 74L20 | 61-5101 |
| U2 | 74L00 | 61-5100 |
| U3 | MC10138 | 62-5100 |

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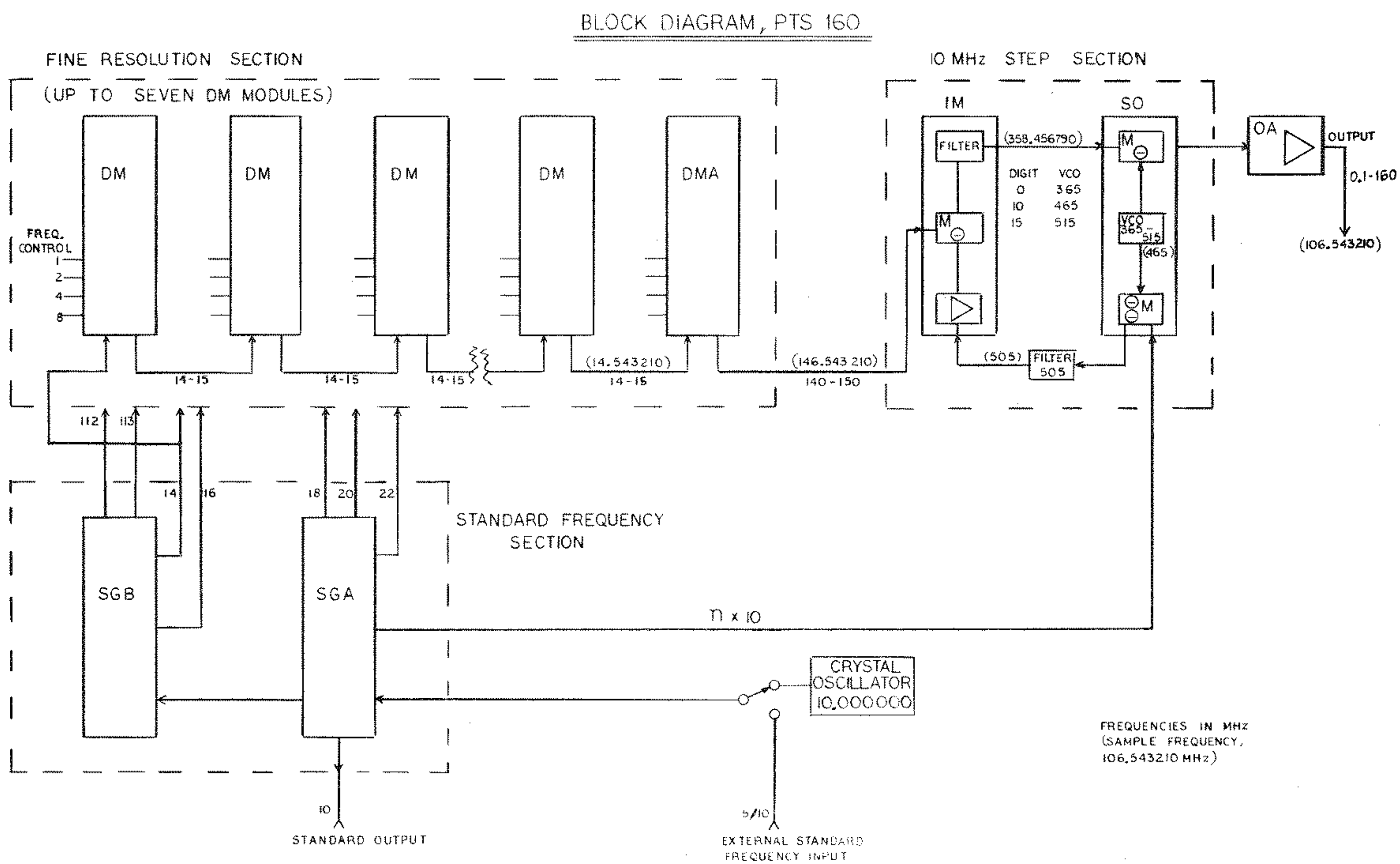
BLOCK DIAGRAM, PTS 160
FINE RESOLUTION SECTION
(UP TO SEVEN DM MODULES)
DM
DM
DM
DM
DMA
FREQ. CONTROL
1
2
4
8
14-15
14-15
14-15
(14.543210)
14-15
(146.543 210)
140-150
10 MHz STEP SECTION
IM
SO
FILTER
(358.456790)
DIGIT VCO
0 365
10 465
15 515
VCO 365-515
(465)
(505)
FILTER 505
OA
OUTPUT
0.1-160
(106.543210)
112
113
14
16
18
20
22
STANDARD FREQUENCY SECTION
SGB
SGA
n x 10
CRYSTAL OSCILLATOR 10.000000
10
STANDARD OUTPUT
5/10
EXTERNAL STANDARD FREQUENCY INPUT
FREQUENCIES IN MHz (SAMPLE FREQUENCY, 106.543210 MHz)

Figure 1

## BLOCK DIAGRAM

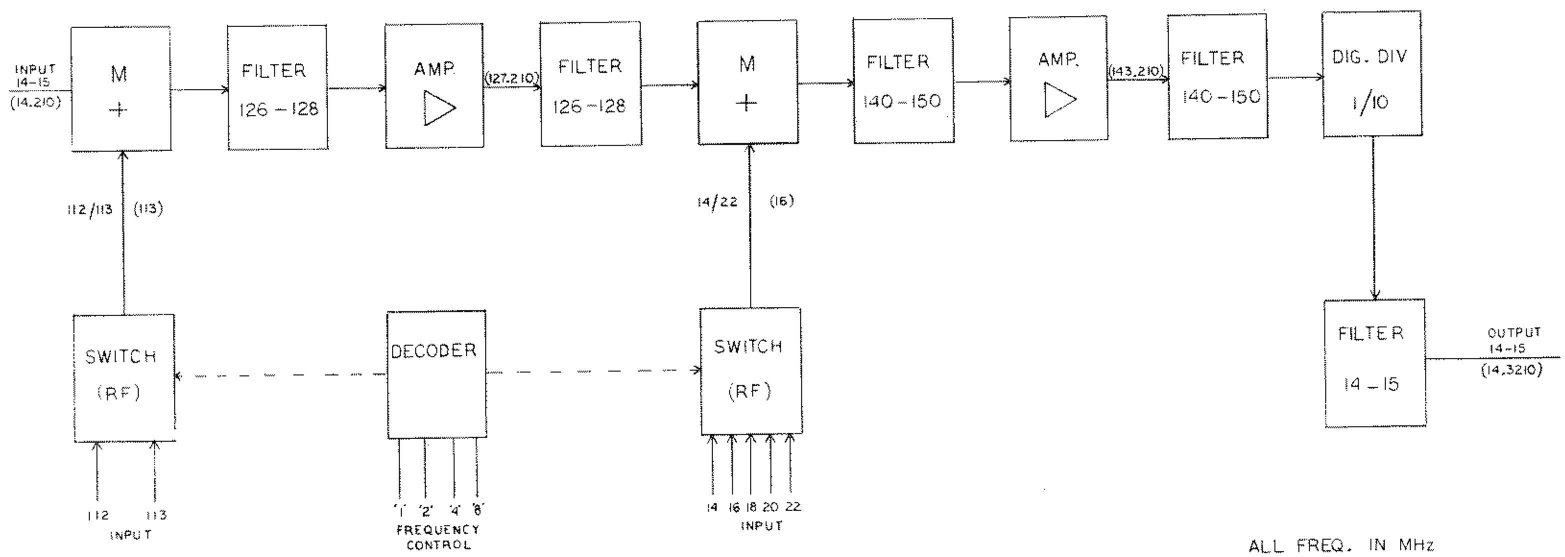


Figure 2



b

## SCHEMATIC, DM-1000

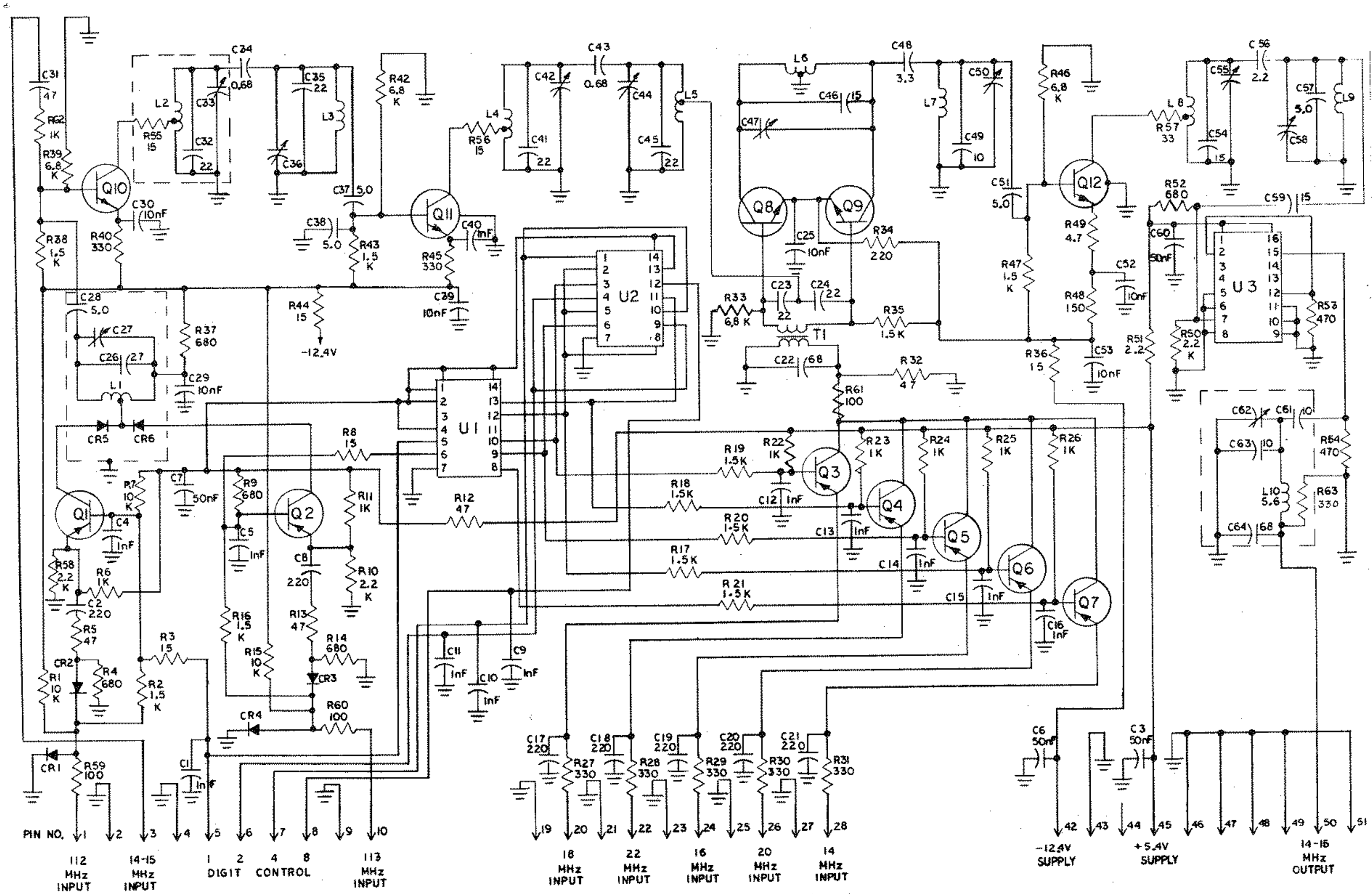


Figure 3



b

## PC ASSEMBLY

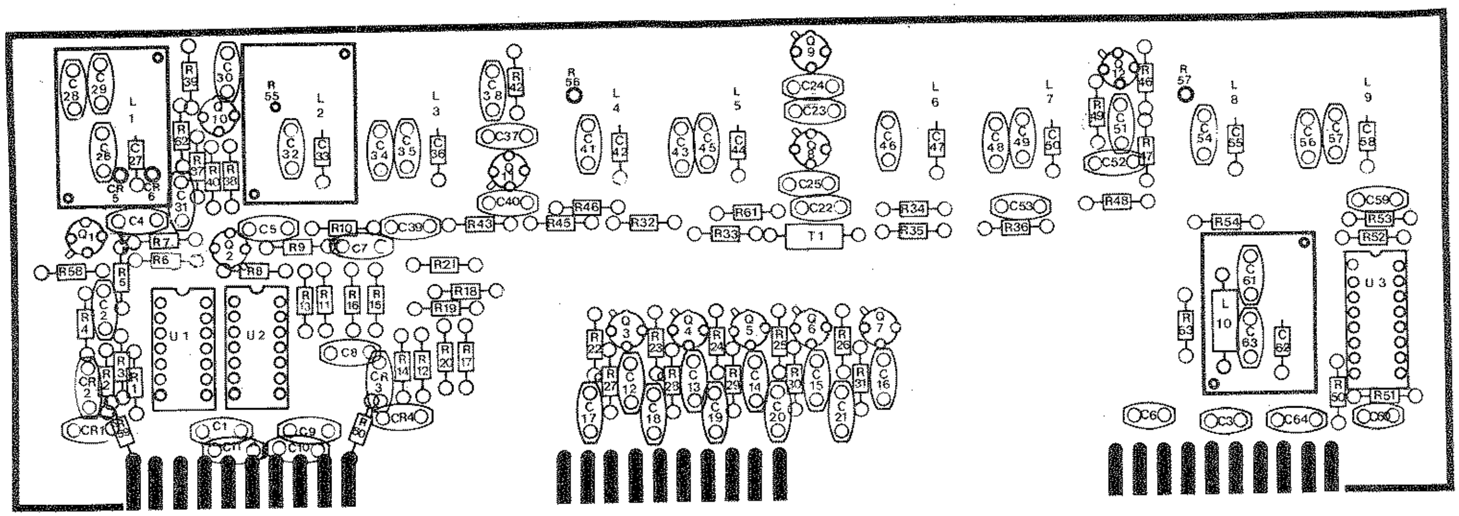


Figure 4



b

## TABLE OF CONTENTS

## INTRODUCTION

The DMA-1005, digit module-A, is used once per instrument and generates the 1 MHz steps. It is very similar to the DM-1000 module and is fed by the string of all DMs in the instrument. As the last unit of this series, it's output at 140-150 MHz contains the 1 MHz steps and all finer steps for which the instrument is equipped, down to 0.1 Hz.

This manual should be seen as supplemental and must be used in conjunction with the DM-1000 portion.

This digit module is of plug-in design and uses three 10-pin connectors with asymmetric spacing assuring proper orientation; it is secured with three 6-32 screws from the bottom of the deck. Housed in a frame and U-cover enclosure, the DMA-1005 can be removed as a complete unit after releasing the 6-32 pan-head screws. To gain access to the PC board, 4-40 top screws and all 2-56 side screws must be removed from the module U-cover. The PC board cannot be removed without first removing the module from the deck.

## PRINCIPLES OF OPERATION

The main difference between the DM and DMA modules is the absence of the final division-by-ten in the DMA. As a result, the arithmetic function of the DMA-1005 can be described as follows:

When receiving a frequency of 14.xyz from the preceding DM, it will produce an output frequency of 14A.xyz MHz, where A directly corresponds to the DMA dial setting. In other words, all digits behind the decimal point are retained, and a 1 MHz step, as selected by the digit control (manual or remote), is placed ahead of the received digits.

All other observations made in the DM *Principles of Operation* apply here as well, and the frequencies shown in the block diagram (Figure 1) at the output of the DMA, namely 146.543210, would be obtained if the DMA had been instructed to produce a "6" digit.

Figure 2 shows the schematic of the DMA-1005, and, apart from the absence of the final divider, it may be noted that there are additional components used in the execution of the 14 to 22 MHz selection switch. This added, switched selectivity removes unwanted frequencies before they can enter the balanced mixer. These frequencies are not attenuated by division or a narrow-band output as they are in the DM-1000 module. All input levels to the DMA are identical with the levels for the DM modules. The output level of the DMA, however, at 140-150 MHz is +2 to +6 dBm into a 50 ohm load. The module feeds a mixer in the IM-1007 module through a 50 ohm pad.

# SERVICE

## Maintenance

No preventive maintenance is required for DMA modules. The presence of an output signal of correct frequency and level indicates that the module is operating properly. The output of the module is included in the leveling loop, and minor aging effects will, therefore, not impair operation.

Replacement of faulty components requires careful use of printed-circuit repair techniques as applicable to double-sided boards with plated-through holes.

## Alignment

Complete alignment of this module is made at the factory with a special test-set. Restoring the alignment after replacement of individual parts in the field is possible. It is recommended that voltages given in the Troubleshooting Procedure be used and that, in general, touch-up alignment be performed only on those tuned circuits which may have been altered by the parts replacements. Replacement of semiconductors will not necessitate realignment of tuned circuits in general.

## Troubleshooting Procedure

The System Section of this manual provides information to isolate faulty modules. It is important to follow the procedure given in detail to ensure that all the common supply frequencies are present before attempting to repair modules.

If a DMA module has been isolated as faulty, the preferred service mode is exchange and factory repair. When immediate service is needed, the following procedure may be used.

Test Equipment Required:

| | |
|---|---|
| RF Voltmeter | 1 - 300 MHz, 10 mV - 1V, High Impedance Probe (3 pF, DC Res 100 KΩ) |
| HF Counter | 0 - 200 MHz, 10 mV Sensitivity, High Impedance or 50 Ω Input |

The output of the DMA module is on pin 50, which is also the test point designation used in the System Section and the running number of the board-edge connector as shown in the schematic (Figure 2). The module produces 140.000 MHz at a level of +2 to +6 dBm into the IM module if all instrument dials have been set to zero. As the dial of the DMA module is changed through successive numbers 0 to 9, the output frequency should change in 1 MHz steps from 140.000 MHz to 149.000 MHz. If the output is of the proper frequency but low in level, the fault is in the 14-22 MHz switch, the mixer (M1), or the 140-150 MHz output filters L6 to L10 and transistor Q11. Alignment of this section cannot be restored in the field, but active devices are generally replaceable without need for realignment. See DC operating conditions listed below.

Absence of output for some dial settings points to specific causes:

1. No output on *two* successive even-odd digits (e.g., 2,3) indicates that the second mixer, M1, does not receive one of the low bus frequencies from 14 to 22 MHz, and the fault is likely located in the switch section (Q3 to Q7). 14 MHz is used for digit 0,1; 16 MHz for digit 2,3; and so on.

2. No output on either *all odd* or *all even* digits will result from failure in the 112/113 MHz switches Q1 or Q2, since 112 MHz is used to produce all even digits and 113 MHz to make the odd digits.



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3. If no output is obtained on any digit, if random digits are missing, or if an unsteady counter reading (noise) is present, part of the circuitry that is used on all digits must be faulty. The active devices are Q8, Q9, Q10 and Q11. DC operating conditions on all of these transistors are such that 1.1 to 1.5V should be measured across their emitter resistors R40, R45, R69 and R48. Bases of switch transistors Q3 to Q7 are at +5.2V when inactive and at +3.3V when turned on.

RF voltages at various stages are given to permit further localization of the trouble. Voltages may differ from nominal by ±3 dB.

| | |
|---|---|
| Base Q8 | 0.20V |
| Base Q9 | 0.05V |
| Tap, L5 | 0.30V |
| Base Q11 | 0.10V |

The 126-128 MHz signal at the tap of L5 peaks at digit setting "5" and drops approximately 2 dB for settings "0" and "9" on the preceding DM module (less significant digit).



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## DMA-1005 PARTS LIST

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C2 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C3 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C4 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C5 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C6 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C7 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C8 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C9 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C10 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C11 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C12 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C13 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C14 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C15 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C16 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C17 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C18 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C19 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C20 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C21 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C23 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C24 | 1.5 nF, 10%, 500V, X5F | 22-0152 |
| C26 | 27 pF, 5%, 500V, NPO | 20-0270 |
| C27 | 1-10 pF, Trimmer | 26-5100 |
| C28 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C29 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C30 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C31 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C32 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C33 | 1-10 pF, Trimmer | 26-5100 |
| C34 | 0.68 pF, .25 pF, 500V | 24-2680 |
| C35 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C36 | 1-10 pF, Trimmer | 26-5100 |
| C37 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C38 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C39 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C40 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C41 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C42 | 1-10 pF, Trimmer | 26-5100 |
| C43 | 0.68 pF, .25 pF, 500V | 24-2680 |
| C44 | 1-10 pF, Trimmer | 26-5100 |
| C45 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C46 | 12 pF, 5%, 500V, NPO | 20-0120 |

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS (continued)** | |
| C47 | 1-10 pF, Trimmer | 26-5100 |
| C48 | 2.2 pF, .25 pF, 500V, NPO | 20-1220 |
| C49 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C50 | 1-10 pF, Trimmer | 26-5100 |
| C51 | 6.8 pF, .25 pF, 500V, NPO | 20-1680 |
| C52 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C53 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C54 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C55 | 1-10 pF, Trimmer | 26-5100 |
| C56 | 1.5 pF, .25 pF, 500V, NPO | 24-1150 |
| C57 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C58 | 1-10 pF, Trimmer | 26-5100 |
| C59 | 1.5 pF, .25 pF, 500V, NPO | 24-1150 |
| C60 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C61 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C62 | 1-10 pF, Trimmer | 26-5100 |
| C63 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C65 | 2.2 pF, .25 pF, NPO | 20-1220 |
| C66 | 91 pF, 5%, 500V, N750 | 21-0910 |
| C67 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C68 | 56 pF, 5%, 500V, NPO | 20-0560 |
| C69 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C70 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C71 | 3-13 pF, Trimmer | 26-5101 |
| C72 | 3-13 pF, Trimmer | 26-5101 |
| C73 | 3-13 pF, Trimmer | 26-5101 |
| C74 | 3-13 pF, Trimmer | 26-5101 |
| C75 | 3-13 pF, Trimmer | 26-5101 |
| C76 | 27 pF, 5%, 500V, NPO | 20-0270 |
| C77 | 150 pF, 10%, 500V, X5F | 22-0150 |
| *C78 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| | **INDUCTORS** | |
| L1 | 50 nH, nom. | 35-5100 |
| L2 | 50 nH, nom. | 35-5100 |
| L3 | 50 nH, nom. | 35-5100 |
| L4 | 50 nH, nom. | 35-5100 |
| L5 | 50 nH, nom. | 35-5100 |
| L6 | 50 nH, nom. | 35-5100 |
| L7 | 50 nH, nom. | 35-5100 |
| L8 | 50 nH, nom. | 35-5100 |
| L9 | 50 nH, nom. | 35-5100 |
| L10 | 50 nH, nom. | 35-5100 |
| L11 | 1.0 μH, 5% | 36-5105 |

*Optional



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## DMA-1005 PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **RESISTORS** | |
| R1 | 10 KΩ, 5%, ¼W | 11-0103 |
| R2 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R3 | 15 Ω, 5%, ¼W | 11-0150 |
| R4 | 680 Ω, 5%, ¼W | 11-0681 |
| R5 | 47 Ω, 5%, ¼W | 11-0470 |
| R6 | 1 KΩ, 5%, ¼W | 11-0102 |
| R7 | 10 KΩ, 5%, ¼W | 11-0103 |
| R8 | 15 Ω, 5%, ¼W | 11-0150 |
| R9 | 680 Ω, 5%, ¼W | 11-0681 |
| R10 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R11 | 1 KΩ, 5%, ¼W | 11-0102 |
| R12 | 47 Ω, 5%, ¼W | 11-0470 |
| R13 | 47 Ω, 5%, ¼W | 11-0470 |
| R14 | 680 Ω, 5%, ¼W | 11-0681 |
| R15 | 10 KΩ, 5%, ¼W | 11-0103 |
| R16 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R17 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R18 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R19 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R20 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R21 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R22 | 1 KΩ, 5%, ¼W | 11-0102 |
| R23 | 1 KΩ, 5%, ¼W | 11-0102 |
| R24 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R25 | 1 KΩ, 5%, ¼W | 11-0102 |
| R26 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R27 | 470 Ω, 5%, ¼W | 11-0471 |
| R28 | 470 Ω, 5%, ¼W | 11-0471 |
| R29 | 470 Ω, 5%, ¼W | 11-0471 |
| R30 | 470 Ω, 5%, ¼W | 11-0471 |
| R31 | 330 Ω, 5%, ¼W | 11-0331 |
| R32 | 220 Ω, 5%, ¼W | 11-0221 |
| R33 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R34 | 220 Ω, 5%, ¼W | 11-0221 |
| R35 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R36 | 15 Ω, 5%, ¼W | 11-0150 |
| R37 | 680 Ω, 5%, ¼W | 11-0681 |
| R38 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R39 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R40 | 470 Ω, 5%, ¼W | 11-0471 |
| R42 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R43 | 1.5 KΩ, 5%, ¼W | 11-0152 |

NOTE: 11-xxxx Carbon Film



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## DMA-1005 PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **RESISTORS (continued)** | |
| R44 | 15 Ω, 5%, ¼W | 11-0150 |
| R45 | 150 Ω, 5%, ¼W | 11-0151 |
| R46 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R47 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R48 | 150 Ω, 5%, ¼W | 11-0151 |
| R49 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R50 | 68 Ω, 5%, ¼W | 11-0680 |
| R55 | 15 Ω, 5%, ¼W | 11-0150 |
| R56 | 15 Ω, 5%, ¼W | 11-0150 |
| R57 | 15 Ω, 5%, ¼W | 11-0150 |
| R58 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R59 | 150 Ω, 5%, ¼W | 11-0151 |
| R60 | 150 Ω, 5%, ¼W | 11-0151 |
| R62 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R63 | 15 Ω, 5%, ¼W | 11-0150 |
| R64 | 22 KΩ, 5%, ¼W | 11-0223 |
| R65 | 22 KΩ, 5%, ¼W | 11-0223 |
| R66 | 22 KΩ, 5%, ¼W | 11-0223 |
| R67 | 22 KΩ, 5%, ¼W | 11-0223 |
| R68 | 22 KΩ, 5%, ¼W | 11-0223 |
| | **TRANSISTORS** | |
| Q1 | 2SA 711 | 41-0711 |
| Q2 | 2SA 711 | 41-0711 |
| Q3 | 2N 3250 | 41-3250 |
| Q4 | 2N 3250 | 41-3250 |
| Q5 | 2N 3250 | 41-3250 |
| Q6 | 2N 3250 | 41-3250 |
| Q7 | 2N 3250 | 41-3250 |
| Q8 | 2N 5179 | 40-5179 |
| Q9 | 2N 5179 | 40-5179 |
| Q10 | 2N 5179 | 40-5179 |
| Q11 | 2N 5179 | 40-5179 |

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **DIODES** | |
| CR2 | BA 244 | 71-0244 |
| CR3 | BA 244 | 71-0244 |
| CR5 | IN 4151 | 70-4151 |
| CR6 | IN 4151 | 70-4151 |
| CR7 | BA 244 | 71-0244 |
| CR8 | BA 244 | 71-0244 |
| CR9 | BA 244 | 71-0244 |
| CR10 | BA 244 | 71-0244 |
| CR11 | BA 244 | 71-0244 |
| | **INTEGRATED CIRCUITS** | |
| U1 | 74L20N | 61-5101 |
| U2 | 74L00N | 61-5100 |
| M1 | MD108 | 65-5102 |



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BLOCK DIAGRAM, PTS 160

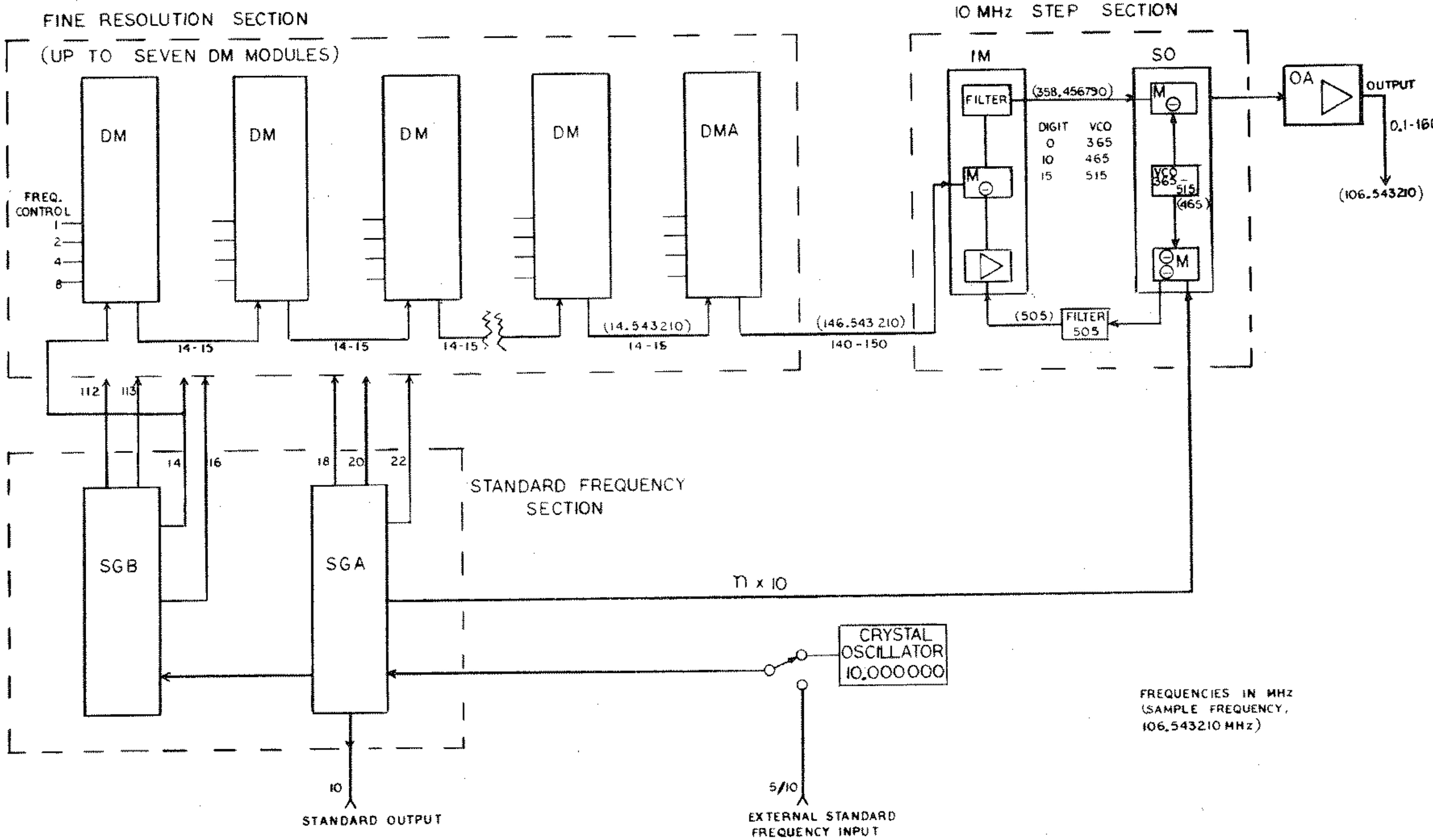


Figure 1



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# SCHEMATIC, DMA-1005

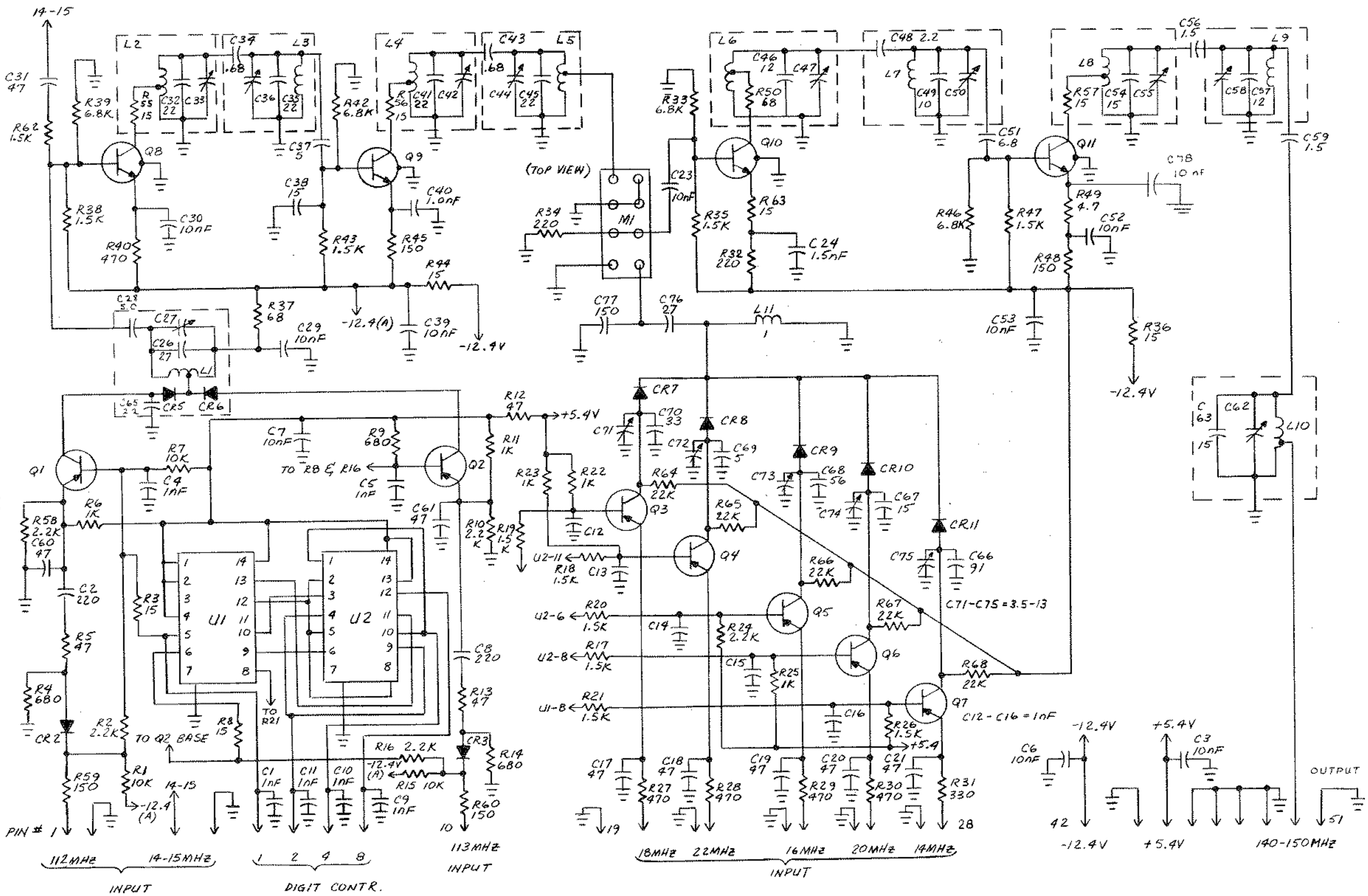


Figure 2



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## PC ASSEMBLY, DMA-1005

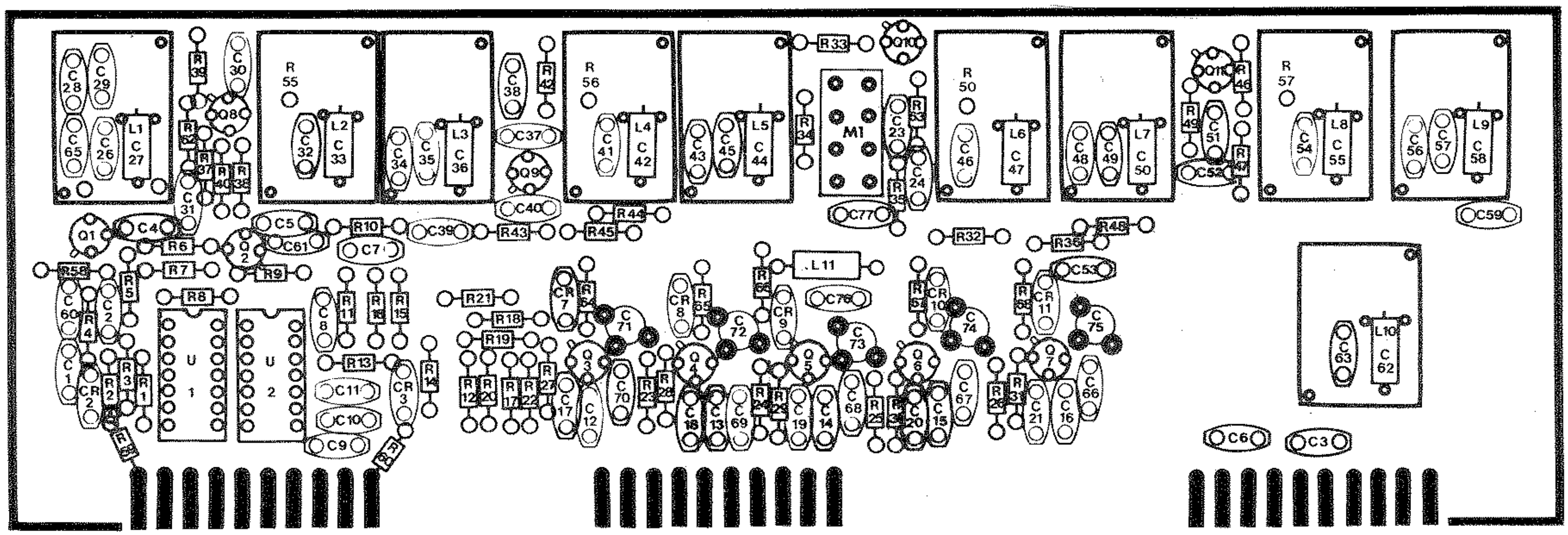

Figure 3



b

## TABLE OF CONTENTS

## INTRODUCTION

The SGA-1002 and SGB-1003 are standard generators used in PTS synthesizers. They operate together from a crystal-oscillator input and, by direct arithmetic operations, produce common supply frequencies. These standard frequencies are distributed in the deck and used by most other modules in the synthesizer.

The SGA module can operate from either 5 or 10 MHz, and with this input it produces: discrete frequencies of 18, 20, 22 and 33 MHz on separate outputs; further all harmonics of 10MHz from 10 to 140 MHz with equal amplitude on one output. These frequencies are used by the SGB, DMs, DMA and SO modules in the synthesis process.

The SGB receives the 10 to 140 MHz *picket fence* from the SGA module and produces 14 and 16 MHz, 112 and 113 MHz, all on separate outputs. These frequencies are used by the DMs and DMA modules.

The SGA and SGB modules use DC power at +5.4V and -12.4V; since the outputs are constant and not subject to selection or control, no programming inputs are provided. These modules combine analog, VHF and digital techniques. All inputs and outputs are fed through card-edge connectors with multiple grounds provided for the RF signals.

These modules are unique; they are not interchangeable with any other module in the synthesizer. Both units are of plug-in design using three 10-pin connectors with asymmetric spacing, which assure proper orientation.

They are secured with three 6-32 pan-head screws from the bottom of the deck. Housed in a frame and U-cover enclosure, the SGA-1002 and SGB-1003 can be removed after releasing the three 6-32 screws.

To gain access to the PC boards, 4-40 top screws and 2-56 side screws have to be removed from the module U-cover. Printed circuit boards cannot be removed without first removing the modules from the deck.

## PRINCIPLES OF OPERATION

The SGA-1002 and SGB-1003, standard generators which operate together, are depicted in the block diagram of Figure 1.

An input of 5 or 10 MHz and a level of 0.4V is received from an external or internal frequency standard and fed to the input amplifier/multiplier. This block is followed by a narrow crystal filter. The pulse generator receives its input from this crystal filter and produces a spectrum, which is the basis for *all* fixed or standard frequencies in the synthesizer. Of these, the five low frequencies of 14, 16, 18, 20 and 22 MHz are all produced by division of a specific spectrum-line through an amplifier-filter circuit, a digital divider, and a filter at the output frequency. The two higher standard frequencies of 112 and 113 MHz also use one specific spectrum line each. Mixers (M) add derivatives of certain low standard frequencies, as shown, to obtain the final frequencies. Thus, by multiplication, division and addition, the SGA and SGB produce seven standard frequencies which are completely coherent with the input frequency of 5 or 10 MHz.

According to Schematic 1002-S (Figure 2), the 5/10 MHz input signal drives Q7, which amplifies or multiplies, and a 10 MHz single-pole crystal filter Y1 follows, which removes noise (and attenuates 5 MHz). The resulting 10 MHz signal can be used externally (to drive slave instruments) from the output of emitter-follower Q6. It is applied internally to pulse generator Q5/Q4.

At the output of the pulse generator (R23/R24) a spectrum of n x 10 MHz multiples from 10 to 140 MHz is available. These frequencies are the source of all standard frequencies in the instrument. Three of the lower frequencies are produced in the SGA.

Since the three sections are identical, a description of one – the 20 MHz generator – shall suffice to illustrate the process. Loosely coupled to the *spectrum bus* by C16, transistor Q3 amplifies the 100 MHz line, and this signal, after filtering in L16, C17, C18, reaches the divider U3. The divide-by-five section of U3 is used, and a 20 MHz signal from pin 4 is connected to a tuned circuit. A low impedance output, taken across C35 is fed to pin 43 and then to the 20 MHz bus in the deck.



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A frequency of 33 MHz is needed to produce 113 MHz in the SGB module. This signal is produced by U1, where the 22 MHz output is divided by 2 and the third harmonic, after filtering, is fed to pin 2 and then to the SGB module.

As shown on Schematic 1003-S (Figure 3), the SGB receives the 10 to 140 MHz spectrum from the SGA module on pin 20. The schematic shows, starting from the middle, on the left-hand side the generation of 14 MHz and 112 MHz signals, and in the right half the generation of 16 MHz and 113 MHz. The low frequencies are produced by the same divide-by-five process which is used in the SGA module: The 70 MHz line is pre-filtered, amplified and filtered in L4, C13, C14, from where it enters divider U1; the resulting 14 MHz signal, after filtering, reaches pin 10, the output.

The same IC also supplies a third harmonic of 14 MHz to Q3. After amplification this 42 MHz signal serves as injection to Q1, which is the final mixer producing 112 MHz by adding a 70 MHz input from Q2.

The 16 MHz generation is identical to the 14 MHz circuits, and 80 MHz is filtered and amplified further to drive mixer Q7 on the 113 MHz side. The 33 MHz signal, coming from the SGA, is amplified in Q8 and then fed to the mixer. Double-tuned filters are employed on both sides to filter the 112 and 113 MHz mixer outputs.

# SERVICE

## Maintenance

No preventive maintenance is required for the SGA or SGB modules. The presence of standard output signals of correct frequency and level indicates that the modules are operating properly.

All outputs of the SGA and SGB modules, with the exception of the 112 and 113 MHz signals, are produced directly by IC digital dividers. A 10 dB window exists at the divider inputs and minor aging effects will, therefore, not impair operation.

Replacement of faulty components requires careful use of PC repair techniques as applicable to double-sided boards with plated-through holes.

## Alignment

Complete alignment of this module is made at the factory with a special test set. Restoring the alignment after replacement of individual parts in the field is possible. It is recommended that voltages given in the Troubleshooting procedure be used, and that in general touch-up alignment be performed only on those tuned circuits which may have been altered by the parts replacements. Replacement of semiconductors will not generally necessitate realignment of tuned circuits.

## Troubleshooting

The System Section of this manual provides information necessary to isolate faulty modules. It is important to follow the procedure step by step to ensure proper identification of failure before attempting to repair modules.

If an SGA or SGB module has been isolated as faulty, the preferred service mode is exchange and factory repair. When immediate service is needed, the following procedure may be used.

Test Equipment Required:

| | |
|---|---|
| RF Voltmeter | 1 - 300 MHz, 10 mV - 1V, High Impedance Probe (3 pF, DC Res. 100 KΩ) |
| HF Counter | 0 - 200 MHz, 10 mV Sensitivity, High Impedance or 50 Ω Input |
| Spectrum Analyzer | 10 - 600 MHz, 50 Ω Input, 60 dB min Dynamic Range, Resolution 1 MHz |

System Section troubleshooting isolates failure in the SGA and SGB to specific outputs. In addition, the block diagram (Figure 1) and schematics (Figure 2 and 3) are structured such that individual circuit-sections are recognizable, and this will aid in the search for the failure.

DC checks of suspected active devices are the proper first step. Voltage drops across the emitter-resistors of the transistors are all 1.2 - 1.5V, except in the SGA across R36 and R25, where 1.9 - 2.3V are normal (R25 with RF drive).

Basic to all output signals is the presence of the *picket fence* of 10 - 140 MHz. The spectrum analyzer connected in place of the SO module (J1) must show each frequency with a level of -16 to -19 dBm. Instruments *not* using an SO module will have a termination on pin 45 (SGA); the S/A connected in place of the termination will show -8 to -11 dBm of spectrum signals.

**Note:** Avoid S/A signal overloads.

The active devices in the pulse generation are Q7, Q5, Q4. Crystal-filter Y1 output is 0.4 - 0.5V across R31.

If the picket fence is normal, low level or absence of a specific frequency may be traced as follows: Connect the S/A to the output in question. Total absence of output in a 14 to 22 MHz frequency generally indicates that the divider is not triggered. All injection voltages, which are connected to pin 7 of the IC (MC-10138), are accessible to the voltmeter probe from the component side of the board. A minimum level of 0.3V is required there. The input and output trimmer capacitors may be identified and retuned (e.g., the trimmers for the 90 MHz circuits feeding the 18 MHz divider are C10 and C12).

If a specific low frequency (14 to 22 MHz) is displayed on the S/A, but the level is low, output circuits are defective or detuned. Every output circuit is tuned by a single trimmer (e.g., C42 tunes the 18 MHz output).

The 112 and 113 MHz outputs are the result of mixing two frequencies. In both cases the first step in tracing trouble is checking the 14 or 16 MHz outputs as detailed before. If these low frequencies are present, connect the S/A to the faulty output (112 or 113 MHz) and attempt to tune: C9, C19, C4, C1 for the 112 MHz output and C46, C53, C56, C60 for the 113 MHz output. At the bases of Q1 and Q7, 0.4V min should be obtained; this is a composite of both injections. This level and its variation with tuning both injections will locate the fault in either one of the mixer inputs or the output circuits following the mixer.



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# SGA-1002 PARTS LIST

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C2 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C3 | 3-13 pF, Trimmer | 26-5101 |
| C4 | 1.0 pF, .25 pF, 500V, NPO | 24-1100 |
| C5 | 1-10 pF, Trimmer | 26-5100 |
| C6 | 27 pF, 5%, 500V, NPO | 20-0270 |
| C7 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C8 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C9 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C10 | 3-13 pF, Trimmer | 26-5101 |
| C11 | 1.0 pF, .25 pF, 500V, NPO | 24-1100 |
| C12 | 1-10 pF, Trimmer | 26-5100 |
| C13 | 47 pF, 5%, 500V, NPO | 20-047 |
| C14 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C15 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C16 | 1.0 pF, .25 pF, 500V, NPO | 24-1100 |
| C17 | 1-10 pF, Trimmer | 26-5100 |
| C18 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C19 | 3-13 pF, Trimmer | 26-5101 |
| C20 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C21 | 3-13 pF, Trimmer | 26-5101 |
| C22 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C23 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C24 | 100 pF, 10%, 500V, X5F | 22-0101 |
| C25 | 110 pF, 5%, MICA | 27-5100 |
| C26 | 1-10 pF, Trimmer | 26-5100 |
| C27 | 6.8 $\mu$F, El., Tant., 16V | 30-5101 |
| C28 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C29 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C30 | 120 pF, 10%, 500V, X5F | 22-0121 |
| C31 | 3-13 pF, Trimmer | 26-5101 |
| C32 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C33 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C34 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C35 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C36 | 3-13 pF, Trimmer | 26-5101 |
| C37 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C38 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C39 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C40 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C41 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C42 | 3-13 pF, Trimmer | 26-5101 |
| C43 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C44 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C45 | 1 nF, 10%, 500V, X5F | 22-0102 |



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| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS (continued)** | |
| C46 | 3-13 pF, Trimmer | 26-5101 |
| C47 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C48 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C49 | 3-13 pF, Trimmer | 26-5101 |
| C50 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C51 | 560 pF, 10%, 500V, X5F | 22-0561 |
| C52 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C53 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C54 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C55 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C56 | 91 pF, 5%, 500V, NPO | 20-0910 |
| | **INDUCTORS** | |
| L1 | 0.33 µH, 10% | 36-5104 |
| L2 | 0.33 µH, 10% | 36-5104 |
| L3 | 0.33 µH, 10% | 36-5104 |
| L4 | 0.20 µH, nom. | 35-5101 |
| L5 | 2.2 µH, 10% | 36-5103 |
| L6 | 1.0 µH, 10% | 36-5105 |
| L7 | 22 µH, 10% | 36-5106 |
| L8 | 5.6 µH, 10% | 36-5100 |
| L9 | 22 µH, 10% | 36-5106 |
| L10 | 5.6 µH, 10% | 36-5100 |
| L11 | 22 µH, 10% | 36-5106 |
| L12 | 5.6 µH, 10% | 36-5100 |
| L13 | 5.6 µH, 10% | 36-5100 |
| L14 | 50 nH, nom. | 35-5106 |
| L15 | 50 nH, nom. | 35-5106 |
| L16 | 50 nH, nom. | 35-5106 |
| | **RESISTORS** | |
| R1 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R2 | 330 Ω, 5%, ¼W | 11-0331 |
| R3 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R4 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R5 | 330 Ω, 5%, ¼W | 11-0331 |
| R6 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R7 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R8 | 330 Ω, 5%, ¼W | 11-0331 |
| R9 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R10 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R11 | 220 Ω, 5%, ¼W | 11-0221 |
| R12 | 220 Ω, 5%, ¼W | 11-0221 |
| R13 | 220 Ω, 5%, ¼W | 11-0221 |
| R14 | 680 Ω, 5%, ¼W | 11-0681 |
| R15 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R16 | 680 Ω, 5%, ¼W | 11-0681 |

Note: 11-XXXX carbon film



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## SGA-1002 PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **RESISTORS (continued)** | |
| R17 | 220 Ω, 5%, ¼W | 11-0221 |
| R18 | 680 Ω, 5%, ¼W | 11-0681 |
| R19 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R20 | 15 Ω, 5%, ¼W | 11-0150 |
| R21 | 220 Ω, 5%, ¼W | 11-0221 |
| R22 | 15 Ω, 5%, ¼W | 11-0150 |
| R23 | 100 Ω, 5%, ¼W | 11-0101 |
| R24 | 15 Ω, 5%, ¼W | 11-0150 |
| R25 | 680 Ω, 5%, ¼W | 11-0681 |
| R26 | 1 KΩ, 5%, ¼W | 11-0102 |
| R27 | 4.7 KΩ, 5%, ¼W | 11-0472 |
| R28 | 100 Ω, 5%, ¼W | 11-0101 |
| R29 | 680 Ω, 5%, ¼W | 11-0681 |
| R30 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R31 | 100 Ω, 5%, ¼W | 11-0101 |
| R32 | 47 Ω, 5%, ¼W | 11-0470 |
| R33 | 15 Ω, 5%, ¼W | 11-0150 |
| R34 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R35 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R36 | 100 Ω, 5%, ¼W | 11-0101 |
| R37 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R38 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R39 | 47 Ω, 5%, ¼W | 11-0470 |
| R40 | 330 Ω, 5%, ¼W | 11-0331 |
| R41 | 47 Ω, 5%, ¼W | 11-0470 |
| R42 | Ω, 5%, ¼W | 11-0470 |
| R43 | 15 Ω, 5%, ¼W | 11-0150 |
| R44 | 15 Ω, 5%, ¼W | 11-0150 |
| | **TRANSISTORS** | |
| Q1 | 2N 5179 | 40-5179 |
| Q2 | 2N 5179 | 40-5179 |
| Q3 | 2N 5179 | 40-5179 |
| Q4 | 2N 5179 | 40-5179 |
| Q5 | 2N 3250 | 41-3250 |
| Q6 | 2N 2369 | 40-2369 |
| Q7 | 2N 2369 | 40-2369 |
| | **DIODES** | |
| CR1 | 1N 4151 | 70-4151 |
| | **INTEGRATED CIRCUITS** | |
| U1 | MC10138 | 62-5100 |
| U2 | MC10138 | 62-5100 |
| U3 | MC10138 | 62-5100 |
| Y1 | Crystal, Filter (or Resistor) | 85-5100 (10-0150) |



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## SGB-1003 PARTS LIST

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 1-10 pF, Trimmer | 26-5100 |
| C2 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C3 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C4 | 1-10 pF, Trimmer | 26-5100 |
| C5 | 0.5 pF, .25 pF, 500V, NPO | 24-2500 |
| C6 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C7 | 2.2 pF, 5%, 500V, NPO | 20-1220 |
| C8 | 56 pF, 5%, Mica | 27-5101 |
| C9 | 1-10 pF, Trimmer | 26-5100 |
| C10 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C11 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C12 | 1.5 pF, .25 pF, 500V, NPO | 24-1150 |
| C13 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C14 | 1-10 pF, Trimmer | 26-5100 |
| C15 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C16 | 3.3 pF, 5%, 500V, NPO | 20-1330 |
| C17 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C18 | 27 pF, 5%, 500V, NPO | 20-0270 |
| C19 | 3-13 pF, Trimmer | 26-5101 |
| C20 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C21 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C22 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C23 | 560 pF, 10%, 500V, X5F | 22-0561 |
| C24 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C25 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C26 | 3-13 pF, Trimmer | 26-5101 |
| C27 | 1.5 nF, 10%, 500V, X5F | 22-0152 |
| C28 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C29 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C30 | 6.8 pF, 5%, 500V, NPO | 20-1680 |
| C31 | 3-13 pF, Trimmer | 26-5101 |
| C32 | 1.5 pF, .25 pF, 500V, NPO | 24-1150 |
| C33 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C34 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C35 | 2.2 pF, 5%, 500V, NPO | 20-1220 |
| C36 | 3-13 pF, Trimmer | 26-5101 |
| C37 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C38 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C39 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C40 | 1-10 pF, Trimmer | 26-5100 |
| C41 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C42 | 3.3 pF, 5%, 500V, NPO | 20-1330 |
| C43 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C44 | 3.3 pF, 5%, 500V, NPO | 20-1330 |
| C45 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |



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| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS (continued)** | |
| C46 | 1-10 pF, Trimmer | 26-5100 |
| C47 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C48 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C49 | 5.0 pF, 5%, 500V, NPO | 20-1500 |
| C50 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C51 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C52 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| C53 | 3-13 pF, Trimmer | 26-5101 |
| C54 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C55 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C56 | 1-10 pF, Trimmer | 26-5100 |
| C57 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C58 | 0.5 pF, .25 pF, 500V, NPO | 24-2500 |
| C59 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C60 | 1-10 pF, Trimmer | 26-5100 |
| C61 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C62 | 3-13 pF, Trimmer | 26-5101 |
| C63 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C64 | 1.5 nF, 10%, 500V, X5F | 22-0152 |
| C65 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C66 | 50 nF, 80/20%, 50V, Z5V | 23-0503 |
| | **INDUCTORS** | |
| L1 | 50 nH, nom. | 35-5100 |
| L2 | 50 nH, nom. | 35-5100 |
| L3 | 90 nH, nom. | 35-5107 |
| L4 | 90 nH, nom. | 35-5107 |
| L5 | 90 nH, nom. | 35-5107 |
| L6 | 90 nH, nom. | 35-5107 |
| L7 | 50 nH, nom. | 35-5100 |
| L8 | 50 nH, nom. | 35-5100 |
| L9 | .33 μH, 10% | 36-5104 |
| L10 | 5.6 μH, 10% | 36-5100 |
| L11 | .33 μH, 10% | 36-5104 |
| L12 | .33 μH, 10% | 36-5104 |
| L13 | 5.6 μH, 10% | 36-5100 |
| L14 | 22 μH, 5% | 36-5106 |
| L15 | 22 μH, 5% | 36-5106 |
| L16 | .33 μH, 10% | 36-5104 |
| L17 | 1.0 μH, 5% | 36-5105 |
| | **RESISTORS** | |
| R1 | 150 Ω, 5%, ¼W | 11-0151 |
| R2 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R3 | 6.8 KΩ, 5%, ¼W | 11-0382 |
| R4 | 330 Ω, 5%, ¼W | 11-0331 |
| R5 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R6 | 6.8 KΩ, 5%, ¼W | 11-0682 |

Note: 11-XXXX carbon film



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| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **RESISTORS (continued)** | |
| R7 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R8 | 470 Ω, 5%, ¼W | 11-0471 |
| R9 | 680 Ω, 5%, ¼W | 11-0681 |
| R10 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R11 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R12 | 680 Ω, 5%, ¼W | 11-0681 |
| R13 | 15 Ω, 5%, ¼W | 11-0150 |
| R14 | 220 Ω, 5%, ¼W | 11-0221 |
| R15 | 220 Ω, 5%, ¼W | 11-0221 |
| R16 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R17 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R18 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R19 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R20 | 220 Ω, 5%, ¼W | 11-0221 |
| R21 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R22 | 680 Ω, 5%, ¼W | 11-0681 |
| R23 | 220 Ω, 5%, ¼W | 11-0221 |
| R24 | 150 Ω, 5%, ¼W | 11-0151 |
| R25 | 15 Ω, 5%, ¼W | 11-0150 |
| R26 | 330 Ω, 5%, ¼W | 11-0331 |
| R27 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R28 | 150 Ω, 5%, ¼W | 11-0151 |
| R29 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R30 | 6.8 KΩ, 5%, ¼W | 110682 |
| R31 | 220 Ω, 5%, ¼W | 11-0221 |
| R32 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R33 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R34 | 6.8 KΩ, 5%, ¼W | 11-0682 |
| R35 | 15 Ω, 5%, ¼W | 11-0150 |
| R36 | 15 Ω, 5%, ¼W | 11-0150 |
| R37 | 15 Ω, 5%, ¼W | 11-0150 |
| R38 | 15 Ω, 5%, ¼W | 11-0150 |
| R39 | 15 Ω, 5%, ¼W | 11-0150 |
| R40 | 15 Ω, 5%, ¼W | 11-0150 |
| R41 | 15 Ω, 5%, ¼W | 11-0150 |
| | **TRANSISTORS** | |
| Q1 | 2N 5179 | 40-5179 |
| Q2 | 2N 5179 | 40-5179 |
| Q3 | 2N 5179 | 40-5179 |
| Q4 | A 400 | 40-A400 |
| Q5 | 2N 5179 | 40-5179 |
| Q6 | 2N 5179 | 40-5179 |
| Q7 | 2N 5179 | 40-5179 |
| Q8 | 2N 5179 | 40-5179 |
| | **INTEGRATED CIRCUITS** | |
| U1 | MC10138 | 62-5100 |
| U2 | MC10138 | 62-5100 |



a

# BLOCK DIAGRAM

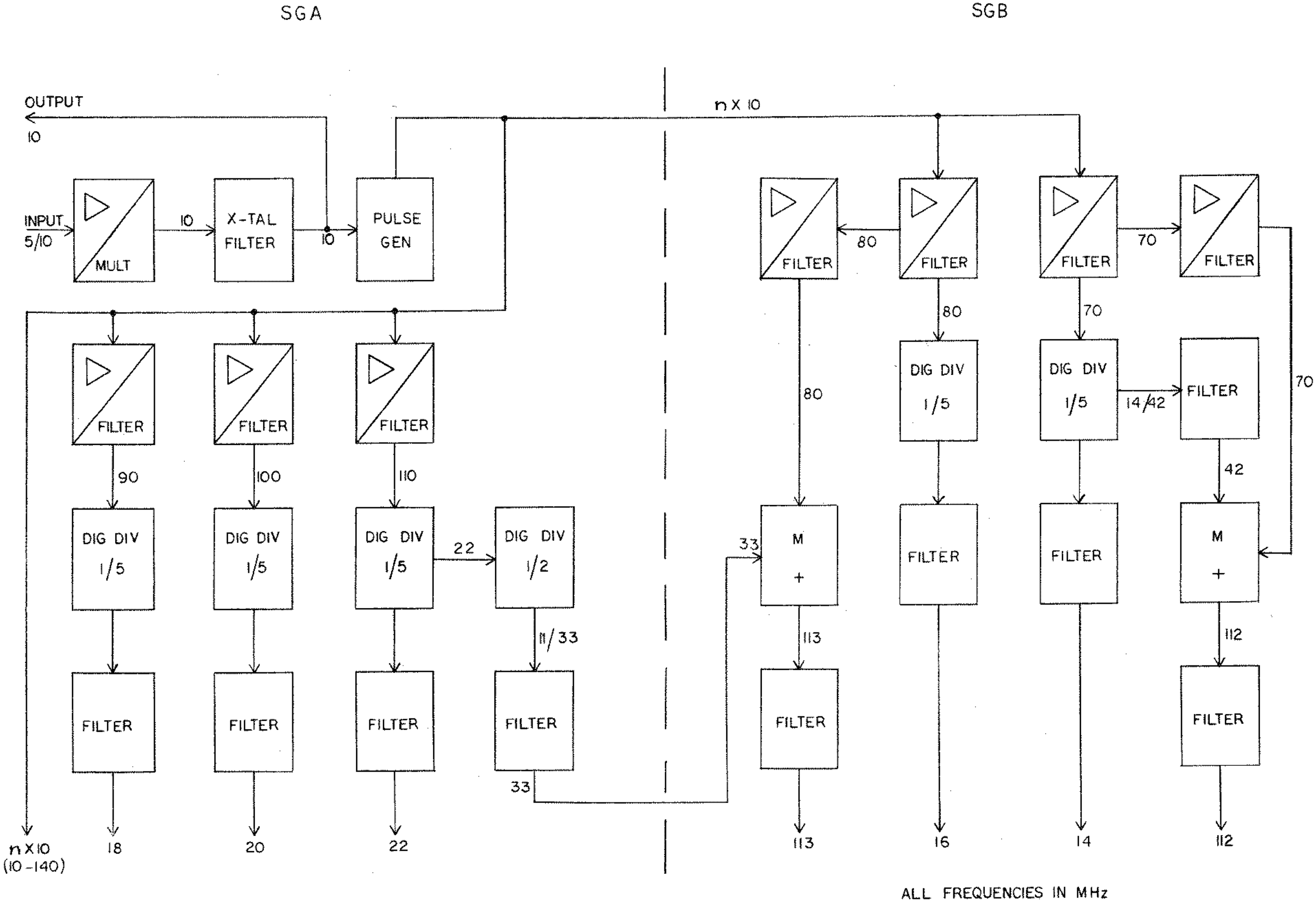
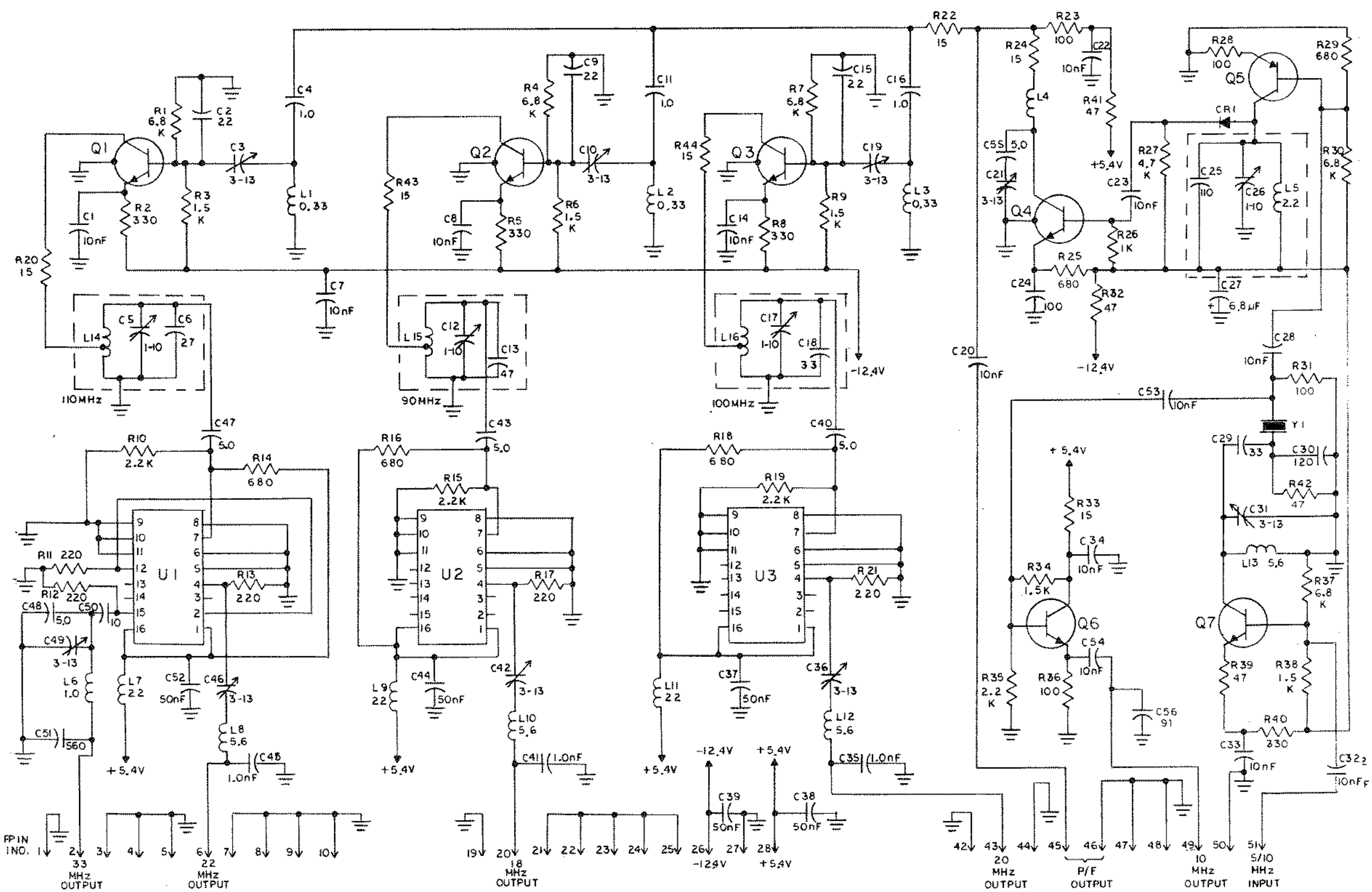



Figure 1



b

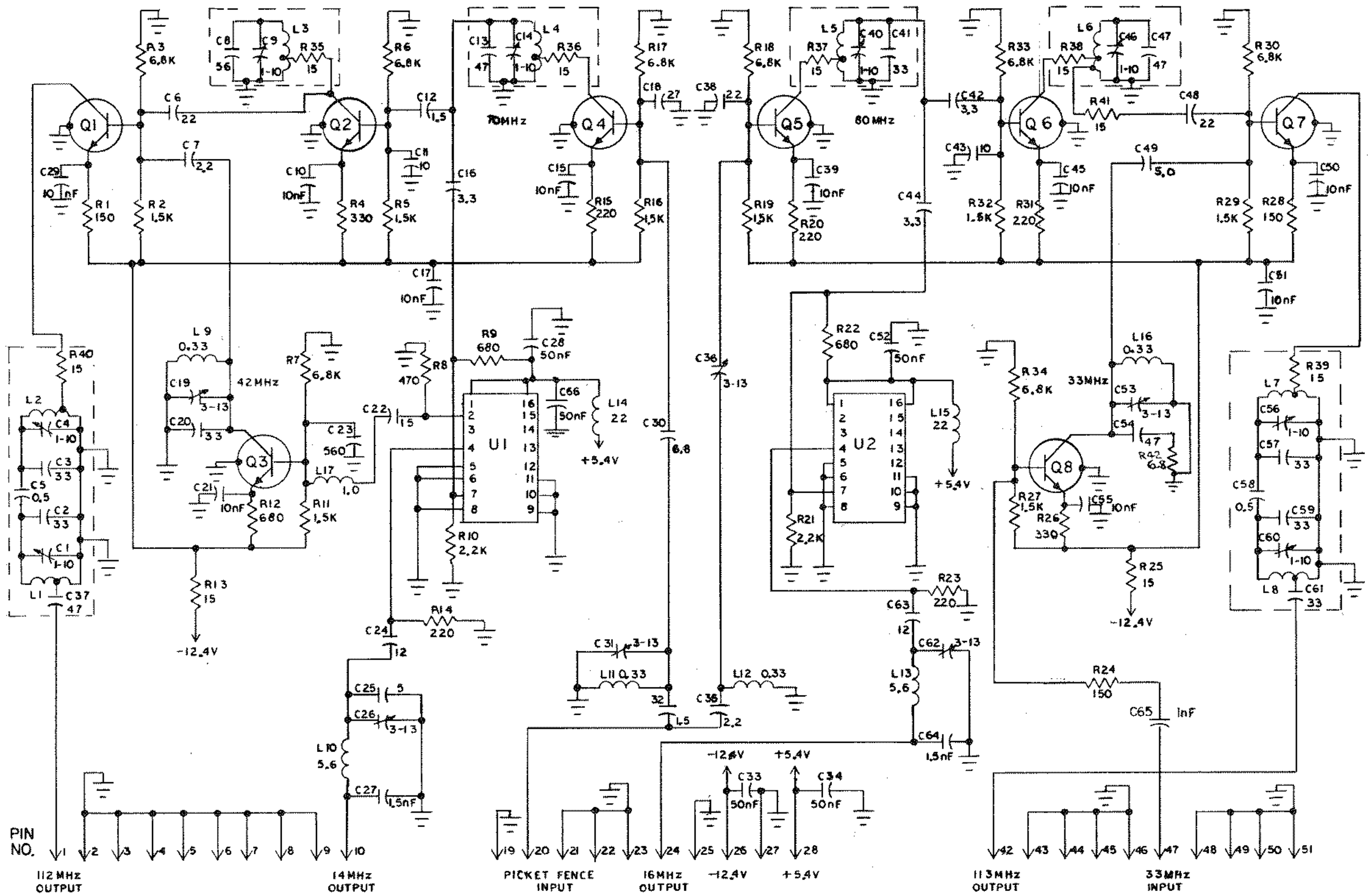
# SCHEMATIC, SGA-1002




SGA-1002

Figure 2

## SCHEMATIC, SGB-1003



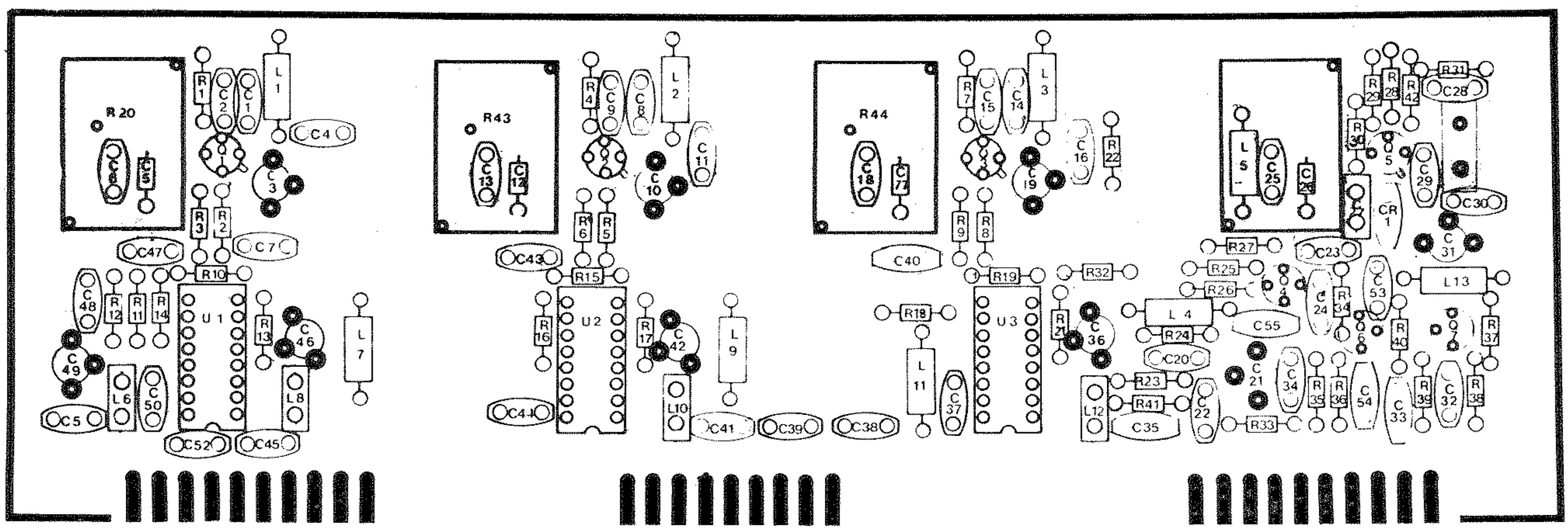

SGB-1003

Figure 3



b

## PC ASSEMBLY, SGA-1002



SGA-1002

Figure 4



b

# PC ASSEMBLY, SGB-1003

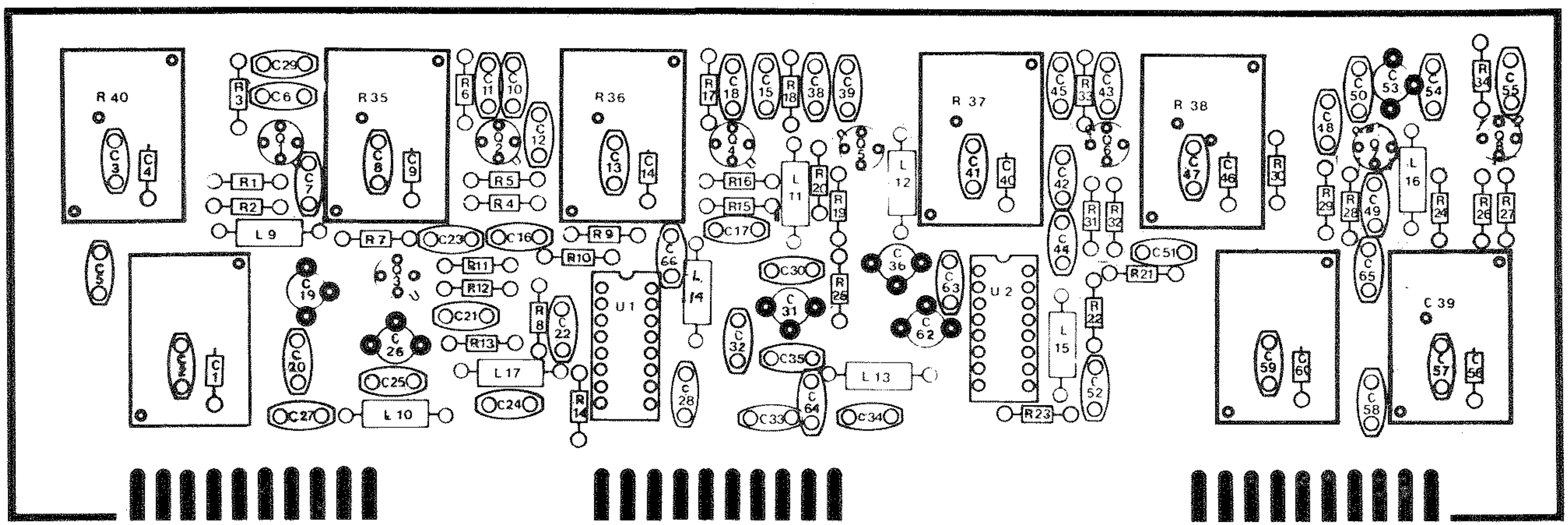



Figure 5



b

## TABLE OF CONTENTS

## INTRODUCTION

The 10 MHz Step Section consists of three separate modules, the SO-1001, the IM-1007 and the OA-1106. They work in conjunction with the 505 MHz bandpass filter (390-1000) as the final functional block of the synthesizer. This block performs frequency translations to obtain the selected 10 MHz decade within the 160 MHz range and also provides the desired output level over a 10 dB range up to +13 dBm.

The heart of the 10 MHz Step Section is the SO-1001, switched oscillator, whose digitally controlled frequency spans a 150 MHz range in 10 MHz increments. Together with the intermediate mixer module, IM-1007, it performs a drift-cancelling double-conversion process, which negates any frequency fluctuations of this oscillator but adds or subtracts the appropriate 10 MHz harmonic from the basic reference source picket-fence to the signal supplied by the DMA module (140-150 MHz). The end result is simply expressed by: Output Frequency = DMA Frequency + (n x 10 MHz) with n = -14 through 0 to +1 depending on the selected 10 MHz multiple. The output amplifier, OA-1106 brings this signal to a level of 20 mW. Level control is accomplished through a feedback loop involving a "PIN"-diode modulator in the IM module as the variable gain element. The controlling signal is derived from a level-sensing detector and comparator in the OA module.

The modules of this section are unique, not interchangeable with each other or other modules in the synthesizer. All three modules employ coax connectors which must be released before removal from the deck is possible. In addition, the IM and SO modules use push-on connectors for various supply and programming inputs. The OA module uses a 10-pin card-edge connector. The modules are secured from the bottom of the deck by 6-32 pan-head screws; the SO uses three, the OA and IM two each. The PC boards of these modules are not accessible without removal of the module from the deck and subsequent removal of the covers. The 505 MHz filter is permanently mounted to the deck structure.

## PRINCIPLES OF OPERATION

The two main functions of the 10 MHz step section are:

1. Generation of the final 10 MHz step in the synthesis process.
2. Output amplification and level control.

A detailed description of how these functions are implemented follows. Use block diagram PTS 160 (Figure 1), schematic SO-1001 (Figure 2), schematic IM-1007 (Figure 3) and schematic OA-1106 (Figure 4) for reference.

### The 10 MHz Step Function

In order to obtain the desired output frequency, a 10 MHz multiple must be added or subtracted from the 140-150 MHz signal provided by the DMA module. This is done in a drift cancelled loop involving the SO and the IM modules and a narrow bandpass filter centered at 505 MHz. A major element in this scheme is the switched oscillator in the SO module, which can be set to one of 16 frequencies spaced 10 MHz by a 4-bit control word.

The program input in hexadecimal code and TTL level is first transposed by zener diodes CR1-4 by approximately -12V. The 1-of-16 decoder (U1, U2, Q8) operates from -6.8V to -11.4V; the latter is a stabilized and filtered voltage, produced by regulator CR8, Q9/Q10, Q11. Stabilization and low ripple are needed since this voltage is eventually applied to the oscillator varactors. The output of the decoder, by connecting one of the divider-resistors R1-R16 to -11.4V, produces proper voltages to set oscillator Q7 to frequencies from 365-515 in 10 MHz steps.

The oscillator frequency is changed by means of varactor diodes CR6, CR7. Control voltage ranges from -1.9V (365 MHz) to -11.0V (515 MHz), approximately.

The oscillator output is fed to two separate three-stage amplifiers for gain and isolation; at both mixers M1 and M2 this signal is used as the switching (LO) signal with a level of +10 to +16 dBm. M1 is connected through an attentuator in the deck and a low-pass filter (L1, L2, L3 and capacitors) to the picket fence signal (n x 10 MHz, 10-140 MHz). At each setting of the VCO one of the sum or difference frequencies equals 505 MHz. This signal is filtered by the bandpass filter connected to J2. The output of the filter feeds the IM module.

Mixer M2 produces the instrument output signal, which is amplified in the OA module. The low level input to M2 at J4 (365-355 MHz), which carries all digits except the 10 MHz steps, comes from the IM module. Any frequency drift of the VCO affects the two inputs to M2 in the same direction and by the same amount which cancels completely in the final output (0.1 to 160 MHz), which is the difference between the two mixer inputs.

The IM-1007 module contains the other elements of the drift cancelled loop. It consists of a 505 MHz broadly tuned amplifier, a mixer, a pin-diode attenuator and a 3-pole bandpass filter for 365-355 MHz.

The unit receives a 505 MHz signal from the SO module via the 505 MHz bandpass filter located in the deck. Five-stage amplifier Q1-5 increases this signal to drive mixer M1 at approximately +15 dBm.

The low-level signal to M1 is the 140-150 MHz input which comes from the DMA through a matching pad. Mixer M1 produces 365-355 MHz, the difference between 505 MHz and 140-150 MHz. It is fed to the pin-modulator CR1-CR4, which is driven from the OA and is a part of the output levelling loop. Minimum attenuation is obtained with a −11.5V input. The signal is then filtered in the 3-pole filter (L1, L2, L3) and fed back to the SO via J3, thereby closing the drift cancelling loop.



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**Output Amplification and Level Control**

The final output (0.1-160 MHz) from M2 in the SO module is a low-level signal of nominally -24 dBm. The output amplifier OA module provides the necessary wideband gain and levelling of amplitude to produce instrument outputs up to +13 dBm across the band from a 50 ohm source-impedance with substantially flat response. See schematic 1106-S (Figure 4).

The RF gain portion from input J2 to output J1 provides insertion gain in a 50-ohm system of approximately 40 dB from .1 MHz to 160 MHz. The gain is produced by four bi-polar transistors in C/E configuration. The amplifiers use emmitter degeneration at low frequencies to obtain a flat response. Two stages of pre-amplification are followed by a driver and an output stage. The module input, which is connected to the final mixer output in the SO module, contains a low-pass filter to reduce levels of signals above 160 MHz.

To operate the levelling loop, the RF output signal is detected by CR1/CR2. The resulting DC voltage, after suitable amplification, is compared to the "set-level" voltage in the differential pair Q9/Q10. The output of this amplifier through Q11 regulates the current of the PIN-diode attenuator in the IM module, which controls the amplifier input signal such that only a minute error-voltage exists between the "set-level" voltage and the collector voltage of Q8. This means that the RF voltage at the detector is stabilized at a constant set level. The actual output voltage into a matched load impedance (50 ohms) is one-half of the detector voltage with R26 providing the 50 ohm source impedance. The unterminated output can reach a level of twice the voltage shown by the meter on the front panel.

# SERVICE

## Maintenance

No preventive maintenance is required for the three modules of this section. The presence of output signals of correct frequency and level indicates that the modules are operating properly. Minor aging effects will not impair performance. Detailed verification of systems and module operation is made with the system troubleshooting table in the system section.

## Alignment/Calibration

Modules are tested and calibrated at the factory in special test fixtures. Complete alignment of the SO and IM modules is beyond the scope of this manual; most active and passive components of these modules, however, can be replaced if they become defective, without any recalibration. The only calibration in the OA module is the adjustment of the meter circuit, described below.

## OA Module, Meter Calibration

Remove module from deck after carefully releasing coax connectors and 6-32 screws. Remove cover, reinstall module without cover, connect power or level meter (50 ohm terminated) directly to the output jack, i.e., the level sensing head should see no additional attenuation. Set frequency to 100 MHz and adjust level control to obtain +13 dBm reading on front panel meter. If necessary, readjust R33 to obtain +13 dBm on power or level meter. Reset level to +3 dBm on panel meter. Adjust R26 if needed to match reading on power meter. Repeat sequence several times to eliminate effects of interaction. Reinstall cover and recheck.

**Troubleshooting**

The system section of this manual has the necessary information to isolate a faulty module in the 10 MHz Step Section. It is important to follow the procedure in detail to ensure proper identification of the faulty module. Further tests here require the same test equipment as detailed under System Troubleshooting.

Aspects of the generation of the proper frequency are all covered in the system troubleshooting chart. This leaves the checks concerning the levelling loop. Meter recalibration in the OA module is detailed above.

A normally functioning instrument will produce a PIN-modulator voltage (white lead, OA pin 20 of −4 to −11.0V at an output setting of +13 dBm into a 50 ohm load. This voltage (PIN-voltage) is an easily accessible monitor for loop problems. It permits diagnosis of most troubles. If it saturates to - 11.0V, insufficient gain is available to produce the output demanded.

The first step in the system troubleshooting chart that involves the PIN-voltage is No. 15. To obtain -16 dBm output from the IM requires a PIN-voltage of 11.0V; since the loop is open (SA connected to IM output), the OA will produce this voltage unless it is faulty. The OA, however, must see +2.0V at its pin 22. This voltage comes from the front panel level pot. A built-in voltage divider or an external feed through programming connector pin 22 supplies this voltage in instruments without front panel controls. If no positive voltage is available on OA pin 22, check these sources.

An *apparent* lack of output can obviously result from a failure of the meter or the meter resistor R43 in the OA. If the spectrum analyzer or level meter record output, but no meter indication is obtained, a check of the 1 mA, 100 ohm, front panel meter or the resistor is in order. The PIN-voltage will not indicate post-detector faults in the system. If the voltage is normal, but no output is available, check output coax cable, connectors and R22,C22 in the OA module.

## Module Checks

After one of the three modules has been found suspect or defective, it is recommended to return the module to the factory for repair. In emergency situations a number of checks are detailed below, which may enable a skilled technician to locate the specific fault.

Most failures of active devices result in drastic changes of the DC voltages of the semiconductor. For this reason DC checks are always the proper first step. Further, a careful examination of the PC board may reveal overheated components, bad solder joints, broken track, etc.

Replacement of faulty components requires careful use of printed-circuit repair techniques as applicable to double-sided boards with plated-through holes.

## OA Module Tests

Carefully remove module after releasing 6-32 screws and coax connectors below the deck. Remove cover from module. To perform DC tests, the module has to be powered, preferably through a 10-pin, card-edge connector (0.156 spacing) with: -12.4V at pin 28, current 100mA; +5.4V at pin 26, current 45 mA. Ground return is pin 19.

Transistor currents in the RF part of the OA are best checked by measuring the drop across the emitter resistors.

| Q | Res | Voltage |
|---|---|---|
| 1 | R5 | 90mV |
| 2 | R6 | 140mV |
| 3 | R14 + 15 | 4.0V |
| 4 | R23 + 24 | 3.4V |

Deviations of over 20% are not normal. Replacement of any of the above transistors will not require recalibration. Part or transistor replacement in the detector-op-amp part of the OA calls for recalibration of the meter circuit; see page 5.



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**SO Module Tests**

Check -12.4V current with ammeter (in blue lead). Normal values are 180-200 mA for digit 10 MHz; and 230-250 mA for digit 150 MHz. Any significant deviation confirms some component or wiring fault, which might be detectable by careful inspection of the open module.

Unplug bottom connections, coax and feed-through clips, remove module and remove cover. Do not change any pot settings. Power module with -12.4V through C44 and check:

1. -11.4V regulator voltage at pin 8-U1. Non-compliance indicates trouble in regulator section around Q9-Q11.

2. Verify mixer input levels at L4, R82 for M1 and L10 , R81 for M2 to be +13 dBm. (Use RF voltmeter.) If both are off, oscillator section is suspect. If only one is off, associated amplifier section is suspect, Q1-Q3 or Q4-Q6. Emitter resistor voltage drops across R21, R27, R32, R55, R60, R66 are 1.7 -2.3V.

Generally no recalibration is required after replacement of transistors and components in the amplifier and regulator sections.

**IM Module Tests**

Check -12.4V current with ammeter (in blue lead). Normal value is 65 mA. Reconnect blue lead, remove white lead and apply –12.4V through ammeter to this capacitor, normal current is 10 mA. Any significant deviation confirms a major component or wiring fault. Release coax connector and remove module after releasing the 6-32 screws; remove cover. If inspection does not provide any clues, power module with -12.4V through C41 and measure voltage drops in the emitter resistors:



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| Q | Res. | Voltage |
|---|---|---|
| 1 | R33 | 1.3V |
| 2 | R27 | 1.3V |
| 3 | R22 | 1.3V |
| 4 | R16 | 1.3V |
| 5 | R13 | 1.5V |

Replacements of transistors or components in the amplifier section Q1-Q5 can be done without recalibration.



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## SO-1001 PARTS LIST

### CAPACITORS

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| C1 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C2 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C3 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C4 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C5 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C6 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C7 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C8 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C9 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C10 | 27 pF, 5%, 500V, NPO | 20-0270 |
| C11 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C12 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C13 | 6.8 pF, 5%, 500V, NPO | 24-1680 |
| C14 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C15 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C16 | 5 pF, 5%, 500V, NPO | 20-1500 |
| C17 | 1.0 pF, 5%, 500V, NPO | 24-1100 |
| C18 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C19 | 6.8 µF, El.-Tant. 16V | 30-5101 |
| C20 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C21 | 3.3 pF, 5%, 500V, NPO | 20-1330 |
| C22 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C23 | 2.2 pF, 5%, 500V, NPO | 20-1220 |
| C24 | 10pF, 5%, 500V, NPO | 20-0100 |
| C25 | 1.5 nF, +50-20%, 500V | 28-5100 |
| C26 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C27 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C28 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C29 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C30 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C31 | 6.8 µF, El.-Tant. 16V | 30-5101 |
| C32 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C33 | 6.8 µF, El.-Tant. 16V | 30-5101 |
| C34 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C35 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C36 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C37 | 6.8 µF, El.-Tant. 16V | 30-5101 |
| C38 | 1.5 nF, +50-20%, 500V | 28-5100 |
| C39 | 1.5 nF, +50-20%, 500V | 28-5100 |
| C40 | 1.5 nF, +50-20%, 500V | 28-5100 |
| C41 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C42 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C43 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C44 | 1.5 nF, +50-20%, 500V | 28-5100 |



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| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **INDUCTORS** | |
| L1 | 50 nH, nom. | 35-5104 |
| L2 | 50 nH, nom. | 35-5103 |
| L3 | 50 nH, nom. | 35-5104 |
| L4 | 50 nH, nom. | 35-5105 |
| L5 | 50 nH, nom. | 35-5105 |
| L6 | 50 nH, nom. | 35-5105 |
| L7 | 25 nH, nom. | 35-5112 |
| L8 | 30 nH, nom. | 38-5100 |
| L9 | 80 nH, nom. | 35-5122 |
| L10 | 50 nH, nom. | 35-5105 |
| L11 | 50 nH, nom. | 35-5105 |
| L12 | 50 nH, nom. | 35-5105 |
| L13 | 20 nH, nom. | 35-5121 |
| L14 | 20 nH, nom. | 35-5120 |
| L15 | .15 nH, 10% | 36-5120 |
| | **RESISTORS** | |
| R1 | 500 Ω, 10%, 1W | 17-5103 |
| R2 | 500 Ω, 10%, 1W | 17-5103 |
| R3 | 500 Ω, 10%, 1W | 17-5103 |
| R4 | 1.0 KΩ, 10%, 1W | 17-5104 |
| R5 | 1.0 KΩ, 10%, 1W | 17-5104 |
| R6 | 1.0 KΩ, 10%, 1W | 17-5104 |
| R7 | 1.0 KΩ, 10%, 1W | 17-5104 |
| R8 | 1.0 KΩ, 10%, 1W | 17-5104 |
| R9 | 1.0 KΩ, 10%, 1W | 17-5104 |
| R10 | 2.0 KΩ, 10%, 1W | 17-5100 |
| R11 | 2.0 KΩ, 10%, 1W | 17-5100 |
| R12 | 2.0 KΩ, 10%, 1W | 17-5100 |
| R13 | 5.0 KΩ, 10%, 1W | 17-5102 |
| R14 | 5.0 KΩ, 10%, 1W | 17-5102 |
| R15 | 5.0 KΩ, 10%, 1W | 17-5102 |
| R16 | 5.0 KΩ, 10%, 1W | 17-5102 |
| R17 | 1.0 KΩ, 1%, ¼W | 14-5103 |
| R18 | 1.5 KΩ, 1%, ¼W | 14-5104 |
| R19 | 1.0 KΩ, 1%, ¼W | 14-5103 |
| R20 | 332 Ω, 1%, ¼W | 14-5114 |
| R21 | 220 Ω, 5%, ¼W | 11-0221 |
| R22 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R23 | 470 Ω, 5%, ¼W | 11-0471 |
| R24 | 22 Ω, 5%, ¼W | 11-0220 |
| R25 | 4.7 KΩ, 5%, ¼W | 11-0472 |
| R26 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R27 | 220 Ω, 5%, ¼W | 11-0221 |
| R28 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R29 | 4.7 KΩ, 5%, ¼W | 11-0472 |
| R30 | 470 Ω, 5%, ¼W | 11-0471 |



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| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **RESISTORS (continued)** | |
| R31 | 22 Ω, 5%, ¼W | 11-0220 |
| R32 | 330 Ω, 5%, ¼W | 11-0331 |
| R33 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R34 | 4.7 KΩ, 5%, ¼W | 11-0472 |
| R35 | 680 Ω, 5%, ¼W | 11-0681 |
| R36 | 680 Ω, 5%, ¼W | 11-0681 |
| R37 | 1.0 KΩ, 5%, ¼W | 11-0102 |
| R38 | 680 Ω, 5%, ¼W | 11-0681 |
| R39 | 47 Ω, 5%, ¼W | 11-0470 |
| R40 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R41 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R42 | 3.3 KΩ, 5%, ¼W | 11-0332 |
| R43 | 4.7 KΩ, 5%, ¼W | 11-0472 |
| R44 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R45 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R46 | 22 Ω, 5%, ¼W | 11-0220 |
| R47 | 22 Ω, 5%, ¼W | 11-0220 |
| R48 | 220 Ω, 5%, ¼W | 11-0221 |
| R49 | 220 Ω, 5%, ¼W | 11-0221 |
| R50 | 3.3 KΩ, 5%, ¼W | 11-0332 |
| R51 | 1.0 KΩ, 5%, ¼W | 11-0102 |
| R52 | 47 Ω, 5%, ¼W | 11-0470 |
| R53 | 470 Ω, 5%, ¼W | 11-0471 |
| R54 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R55 | 330 Ω, 5%, ¼W | 11-0331 |
| R56 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R57 | 22 Ω, 5%, ¼W | 11-0220 |
| R58 | 470 Ω, 5%, ¼W | 11-0471 |
| R59 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R60 | 220 Ω, 5%, ¼W | 11-0221 |
| R61 | 4.7 KΩ, 5%, ¼W | 11-0472 |
| R62 | 22 Ω, 5%, ¼W | 11-0220 |
| R63 | 470 Ω, 5%, ¼W | 11-0471 |
| R64 | 15 Ω, 5%, ¼W | 11-0150 |
| R65 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R66 | 220 Ω, 5%, ¼W | 11-0221 |
| R67 | 4.7 KΩ, 5%, ¼W | 11-0472 |
| R68 | 470 Ω, 5%, ¼W | 11-0471 |
| R69 | 470 Ω, 5%, ¼W | 11-0471 |
| R70 | 2.0 KΩ, 10%, 1W | 17-5100 |
| R71 | 150 Ω, 5%, ¼W | 11-0151 |
| R72 | 100 Ω, 5%, ¼W | 11-0101 |
| R73 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R74 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R75 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R76 | 2.2 Ω, 5%, ¼W | 11-1220 |



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## SO-1001 PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **RESISTORS (continued)** | |
| R77 | 15 KΩ, 5%, ¼W | 11-0153 |
| R78 | 15 KΩ, 5%, ¼W | 11-0153 |
| R79 | 15 KΩ, 5%, ¼W | 11-0153 |
| R80 | 15 KΩ, 5%, ¼W | 11-0153 |
| R81 | 22 Ω, 5%, ¼W | 11-0220 |
| R82 | 33 Ω, 5%, ¼W | 11-0330 |
| | **TRANSISTORS** | |
| Q1 | 2N 5179 | 40-5179 |
| Q2 | 2N 5179 | 40-5179 |
| Q3 | 2N 5179 | 40-5179 |
| Q4 | 2N 5179 | 40-5179 |
| Q5 | 2N 5179 | 40-5179 |
| Q6 | 2N 5179 | 40-5179 |
| Q7 | 2N 5179 | 40-5179 |
| Q8 | 2N 2369 | 40-2369 |
| Q9 | 2N 3250 | 41-3250 |
| Q10 | 2N 3250 | 41-3250 |
| Q11 | 2N 2218 | 42-2218 |
| | **DIODES** | |
| CR1 | 1N 963BF | 73-0963 |
| CR2 | 1N 963BF | 73-0963 |
| CR3 | 1N 963BF | 73-0963 |
| CR4 | 1N 963BF | 73-0963 |
| CR5 | 1N 3829A | 73-3829 |
| CR6 | BB 141B | 72-0141 |
| CR7 | BB 141B | 72-0141 |
| CR8 | 1N 751A | 73-0751 |
| CR9 | 1N 4151 | 70-4151 |
| | **INTEGRATED CIRCUITS** | |
| U1 | 74145 | 60-5101 |
| U2 | 74145 | 60-5101 |
| M1 | SRA-1H | 65-5100 |
| M2 | SRA-1H | 65-5100 |

*NOTE: 11-xxxx carbon film



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# IM-1007 PARTS LIST

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 1-6 pF, Trimmer | 26-5102 |
| C2 | 1.0 pF, .25 pF, 500V, NPO | 24-1100 |
| C3 | 1-6 pF, Trimmer | 26-5102 |
| C4 | 1.0 pF, .25 pF, 500V, NPO | 24-1100 |
| C5 | 1-6 pF, Trimmer | 26-5102 |
| C6 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C7 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C8 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C9 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C10 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C11 | 3-13 pF, Trimmer | 26-5101 |
| C12 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C13 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C14 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C15 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C16 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C17 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C18 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C19 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C20 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C21 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C22 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C23 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C24 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C25 | 10 pF, 5%, 500V, NPO | 20-0100 |
| C26 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C27 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C28 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C29 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C30 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C31 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C32 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C33 | 22 pF, 5%, 500V, NPO | 20-0220 |
| C34 | 10 nF, 80/20%, 50V, Z5V | 23-0103 |
| C35 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C36 | 1.0 pF, .25 pF, 500V, NPO | 24-1100 |
| C37 | 1.5 pF, .25 pF, 500V, NPO | 24-1150 |
| C38 | 3.3 pF, .25 pF, 500V, NPO | 20-1330 |
| C39 | 2.2 pF, .25 pF, 500V, NPO | 20-1220 |
| C40 | 1.5 nF, +50-20%, 500V | 28-5100 |
| C41 | 1.5 nF, +50-20%, 500V | 28-5100 |
| C42 | 3-13 pF, Trimmer | 26-5101 |
| C43 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C44 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C45 | 5 pF, .25 pF, 500V, N750 | 21-1500 |
| C46 | 5 pF, .25 pF, 500V, NPO | 20-1500 |
| C47 | 5 pF, 25 pF, 500V, NPO | 20-1500 |



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## IM-1007 PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **INDUCTORS** | |
| L1 | 20 nH, nom. | 35-5114 |
| L2 | 20 nH, nom. | 35-5113 |
| L3 | 20 nH, nom. | 35-5113 |
| L4 | .33 μH, 10% | 36-5104 |
| L5 | .33 μH, 10% | 36-5104 |
| L6 | 50 nH, nom. | 35-5104 |
| L7 | 40 nH, nom. | 35-5111 |
| L8 | 40 nH, nom. | 35-5110 |
| | **RESISTORS** | |
| R1 | 10 KΩ, 5%, ¼W | *11-0103 |
| R2 | 10 KΩ, 5%, ¼W | 11-0103 |
| R3 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R4 | 10 KΩ, 5%, ¼W | 11-0103 |
| R5 | 1.5 KΩ, 5%, ¼W | 11-0152 |
| R6 | 15 Ω, 5%, ¼W | 11-0150 |
| R7 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R8 | 220 Ω, 5%, ¼W | 11-0221 |
| R9 | 22 Ω, 5%, ¼W | 11-0220 |
| R10 | 220 Ω, 5% ¼W | 11-0221 |
| R11 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R12 | 15 Ω, 5%, ¼W | 11-0150 |
| R13 | 100 Ω, 5%, ¼W | 11-0101 |
| R14 | 220 Ω, 5% ¼W | 11-0221 |
| R15 | 15 Ω, 5%, ¼W | 11-0150 |
| R16 | 150 Ω, 5%, ¼W | 11-0151 |
| R17 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R18 | | |
| R19 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R20 | 470 Ω, 5%, ¼W | 11-0471 |
| R21 | 15 Ω, 5%, ¼W | 11-0150 |
| R22 | 150 Ω, 5%, ¼W | 11-0151 |
| R23 | 15 Ω, 5%, ¼W | 11-0150 |
| R24 | 470 Ω, 5%, ¼W | 11-0471 |
| R25 | 220 Ω, 5%, ¼W | 11-0221 |
| R26 | 15 Ω, 5%, ¼W | 11-0150 |
| R27 | 150 Ω, 5%, ¼W | 11-0151 |
| R28 | 2.2 KΩ, 5%, ¼W | 11-0222 |
| R29 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R30 | 2.2 KΩ, 5%,¼W | 11-0222 |
| R31 | 470 Ω, 5%, ¼W | 11-0471 |
| R32 | 15 Ω, 5%, ¼W | 11-0150 |
| R33 | 150 Ω, 5%, ¼W | 11-0151 |
| R34 | 15 Ω, 5%, ¼W | 11-0150 |
| R35 | 470 Ω, 5%, ¼W | 11-0471 |
| R36 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R37 | 470 Ω, 5%, ¼W | 11-0471 |



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## IM-1007 PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **TRANSISTORS** | |
| Q1 | 2SC 1260 | 40-1260 |
| Q2 | 2SC 1260 | 40-1260 |
| Q3 | 2SC 1260 | 40-1260 |
| Q4 | 2SC 1260 | 40-1260 |
| Q5 | A400 | 40-A400 |
| | **DIODES** | |
| CR1 | 5082-3080 | 71-3080 |
| CR2 | 5082-3080 | 71-3080 |
| CR3 | 5082-3080 | 71-3080 |
| CR4 | 5082-3080 | 71-3080 |
| | **INTEGRATED CIRCUITS** | |
| M1 | SRA 1H | 65-5100 |

*NOTE: 11-xxxx carbon film



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# OA-1106 PARTS LIST

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 5 pF, 5%, 500V, NPO | 20-1500 |
| C2 | 6.8 pF, 5%, 500V, NPO | 20-1680 |
| C3 | 1.5 pF, 5%, 500V, NPO | 20-1150 |
| C4 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C5 | 20 pF, 5%, 500V, NPO | 20-0200 |
| C6 | 18 pF, 5%, 500V, NPO | 20-0180 |
| C7 | 12 pF, 5%, 500V, NPO | 20-0120 |
| C8 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C9 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C10 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C11 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C12 | 100 pF, 5%, 500V, N750 | 21-0101 |
| C13 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C14 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C15 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C16 | 47 pF, 5%, 500V, NPO | 20-0470 |
| C17 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C18 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C19 | 6.8 μF, El.-Tant. 16 V | 30-5101 |
| C20 | .33 μF, 10%, 100V, X7R | 29-5105 |
| C21 | 10 nF, 80/20%, 50V, Z5U | 23-0103 |
| C22 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C23 | 5 pF, 5%, 500V, NPO | 20-1500 |
| C24 | 2.2 nF, 10%, 500V, X5F | 22-0222 |
| C25 | 220 pF, 10%, 500V, X5F | 22-0221 |
| C26 | 10 nF, 80/20%, 50V, Z5U | 23-0103 |
| C27 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C28 | 50 nF, 80/20%, 50V, Z5U | 23-0503 |
| C29 | 10 nF, +80/20%, 50V, Y5U | 23-0103 |
| C30 | 6.8 μF, El.-Tant. 16V | 30-5101 |
| C31 | 1 nF, 10%, 500V, X5F | 22-0102 |
| C32 | 33 pF, 5%, 500V, NPO | 20-0330 |
| C33 | 20 pF, 5%, 500V, NPO | 20-0200 |
| C34 | 15 pF, 5%, 500V, NPO | 20-0150 |
| C35 | 6.8 μF, El.-Tant. 16V | 30-5101 |
| C36 | 6.8 μF, El.-Tant. 16V | 30-5101 |
| C37 | 10 nF, 80/20%, 50V, Z5U | 23-0103 |
| C38 | 10 nF, 80/20%, 50V, Z5U | 23-0103 |
| C39 | 10 nF, 80/20%, 50V, Z5U | 23-0103 |
| C40 | 2.2 pF, 5%, 500V, NPO | 20-1220 |
| | **INDUCTORS** | |
| L1 | 20 nH, nom. | 35-5143 |
| L2 | 20 nH, nom. | 35-5143 |
| L3 | 20 nH, nom. | 35-5143 |
| L4 | 150 μH, 5% | 36-5121 |
| L5 | 22 μH, 10% | 36-5106 |



c

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **INDUCTORS (continued)** | |
| L6 | 150 µH, 5% | 36-5121 |
| L7 | 46 nH, nom. | 35-5135 |
| L8 | 22 µH, 10% | 36-5106 |
| L9 | 32 nH, nom. | 35-5131 |
| L10 | 43 nH, nom. | 35-5153 |
| | **RESISTORS** | |
| R1 | 15 Ω, 5%, ¼W | 11-0150 |
| R2 | 220 Ω, 5%, ¼W | 11-0221 |
| R3 | 470 Ω, 5%, ¼W | 11-0471 |
| R4 | 330 Ω, 5%, ¼W | 11-0331 |
| R5 | 10 Ω, 5%, ¼W | 11-0100 |
| R6 | 6.8Ω, 5%, ¼W | 11-1680 |
| R7 | 6.8 Ω, 5%, ¼W | 11-1680 |
| R8 | 330 Ω, 5%, ¼W | 11-0331 |
| R9 | 470 Ω, 5%, ¼W | 11-0471 |
| R10 | 220 Ω, 5%, ¼W | 11-0221 |
| R11 | 10 Ω, 5%, ¼W | 11-0100 |
| R12 | 1K Ω, 5%, ¼W | 11-0102 |
| R13 | 680 Ω, 5%, ¼W | 11-0681 |
| R14 | 22 Ω, 5%, ¼W | 11-0220 |
| R15 | 150Ω, 5%, ¼W | 11-0151 |
| R16 | 10K Ω, 10%, ½W | 16-5101 |
| R17 | 1K Ω, 5%, ¼W | 11-0102 |
| R18 | 470 Ω, 5%, ¼W | 11-0471 |
| R19 | 470Ω, 5%, ¼W | 11-0471 |
| R20 | 100 Ω, 5%, ¼W | 11-0101 |
| R21 | 330 Ω, 5%, ¼W | 11-0331 |
| R22 | 47 Ω, 5%, ¼W | 11-0470 |
| R23 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R24 | 47 Ω, 5%, ¼W | 11-0470 |
| R25 | 4.7 Ω, 5%, ¼W | 11-1470 |
| R26 | 10K Ω, 10%, ½W | 16-5101 |
| R27 | 100 Ω, 5%, ¼W | 11-0101 |
| R28 | 2.2K Ω, 5%, ¼W | 11-0222 |
| R29 | 1.5K Ω, 5%, ¼W | 11-0152 |
| R30 | 100K Ω, 5%, ¼W | 11-0104 |
| R31 | 100K Ω, 5%, ¼W | 11-0104 |
| R32 | 220 Ω, 5%, ¼W | 11-0221 |
| R33 | 500 Ω, 10%, ½W | 16-5102 |
| R34 | 1.5KΩ, 5%, ¼W | 11-0152 |
| R35 | 2.2K Ω, 5%, ¼W | 11-0222 |
| R36 | 47 Ω, 5%, ¼W | 11-0470 |
| R37 | 1.91K Ω, 1%, ¼W | 14-5115 |
| R38 | 1.91K Ω, 1%, ¼W | 14-5115 |
| R39 | 4.32K Ω, 1%, ¼W | 14-5113 |
| R40 | 4.32K Ω, 1%, ¼W | 14-5113 |



b

## OA-1106 PARTS LIST (continued)

| Schem. Desig. | Description | PTS P/N |
|---|---|---|
| | **RESISTORS (continued)** | |
| R41 | 330Ω, 5%, ¼W | 11-0331 |
| R42 | 10KΩ, 5%, ¼W | 11-0103 |
| R43 | 1.91KΩ, 1%, ¼W | 14-5115 |
| R44 | 220Ω, 5%, ¼W | 11-0221 |
| R45 | 22Ω, 5%, ¼W | 11-0220 |
| R46 | 220Ω, 5%, ¼W | 11-0221 |
| | **TRANSISTORS** | |
| Q1 | A400 | 40-A400 |
| Q2 | A401 | 40-A401 |
| Q3 | A401 | 40-A401 |
| Q4 | BFR95 | 42-FR95 |
| | **DIODES** | |
| CR1 | 5082-2810 | 71-2810 |
| CR2 | 5082-2810 | 71-2810 |
| CR3 | 5082-2810 | 71-2810 |
| CR4 | 5082-2810 | 71-2810 |
| | **INTEGRATED CIRCUIT** | |
| U1 | LM324 | 64-0324 |



C

## BLOCK DIAGRAM, PTS 160

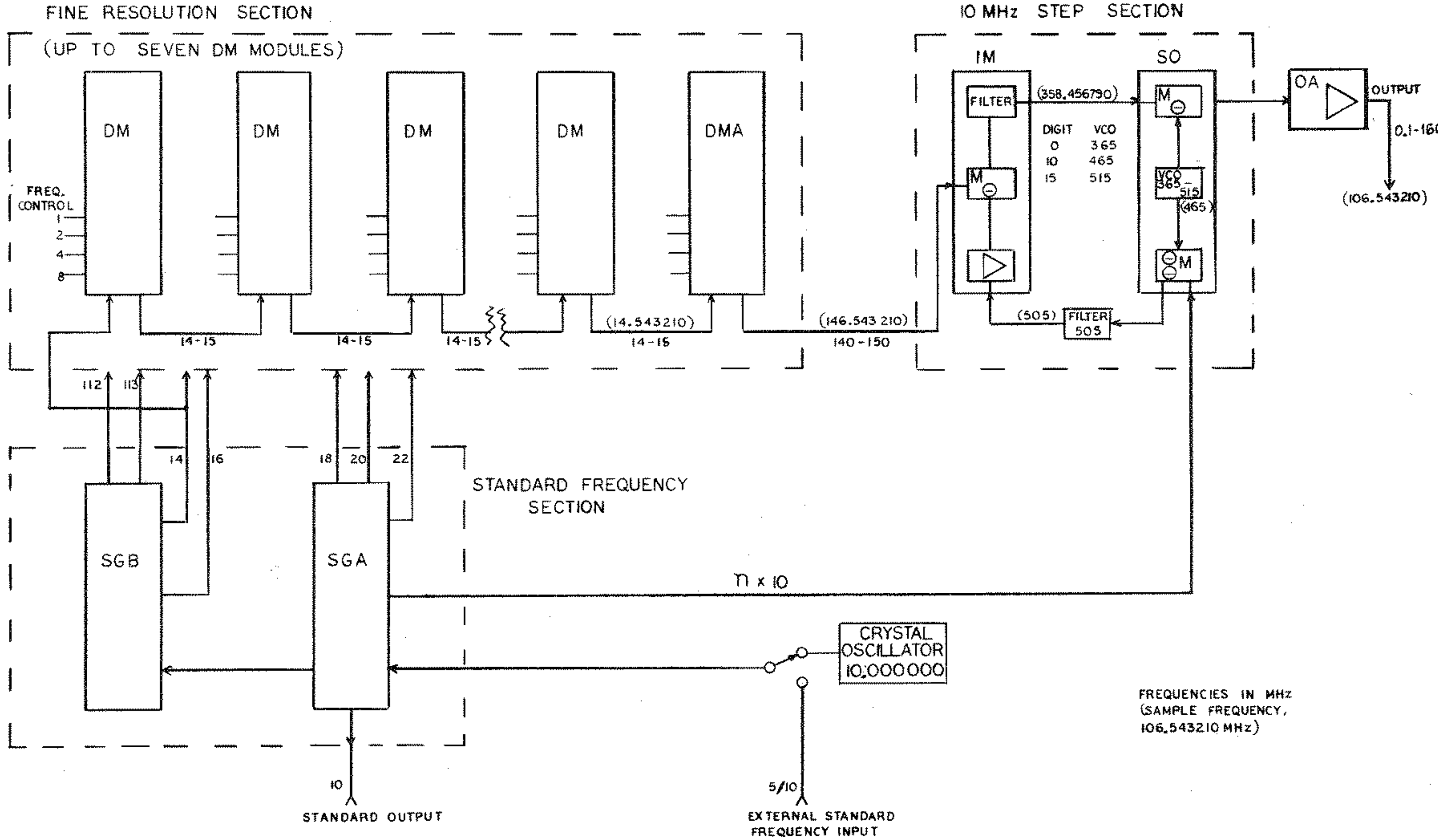



Figure 1



a

# SCHEMATIC, SO-1001

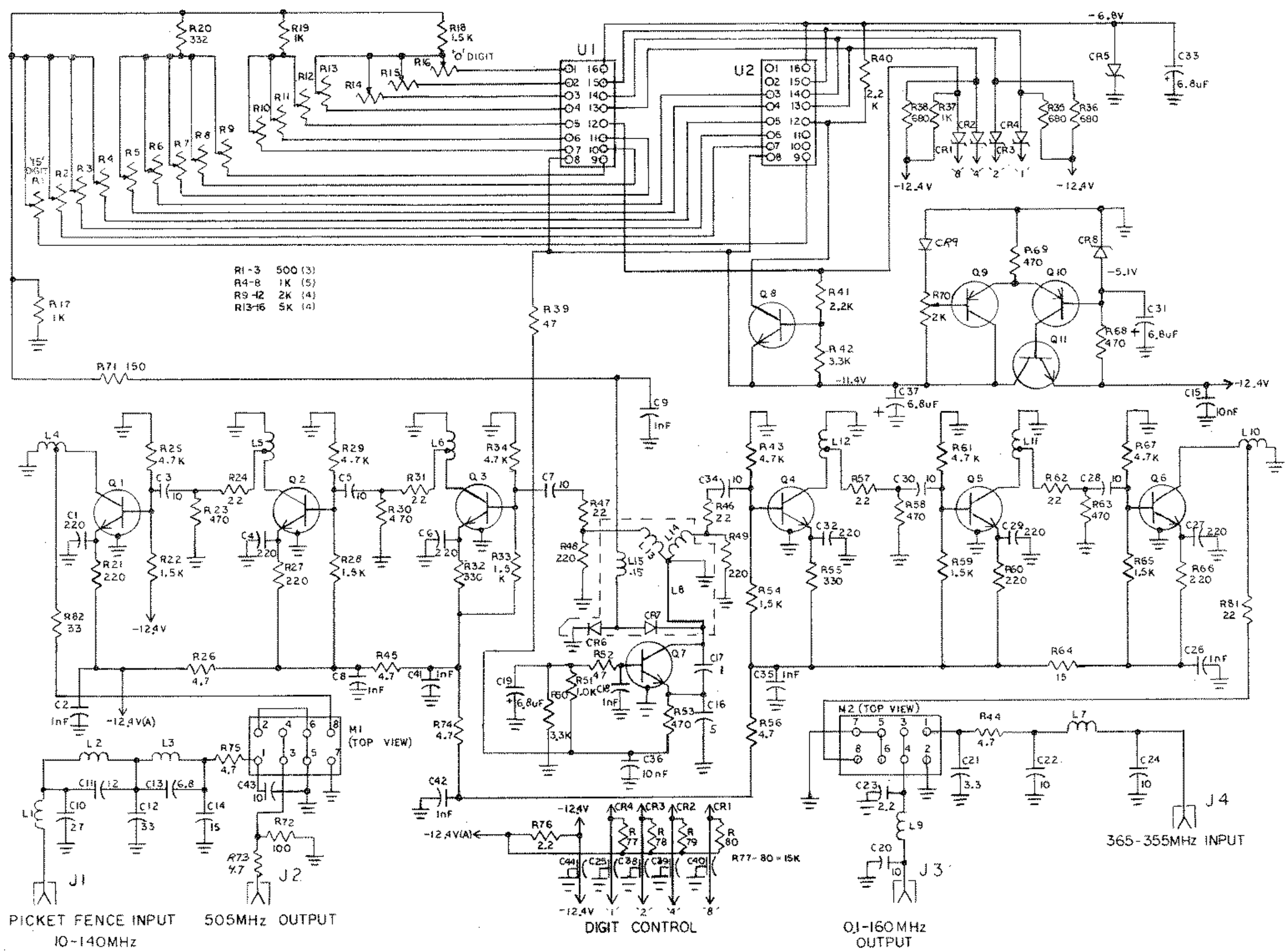



Figure 2



b

b

# SCHEMATIC, IM-1007

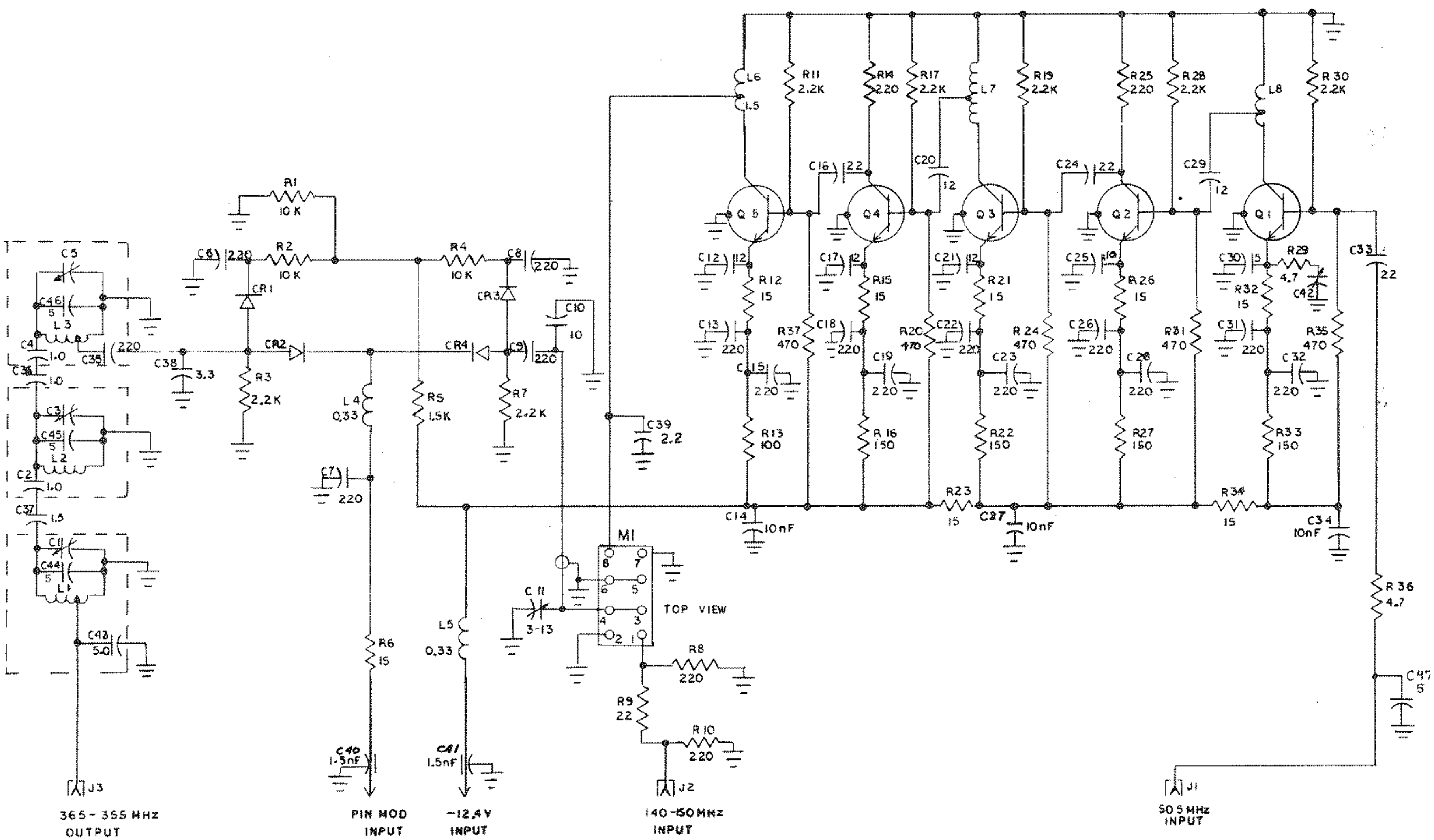



Figure 3

d

## SCHEMATIC, OA-1106

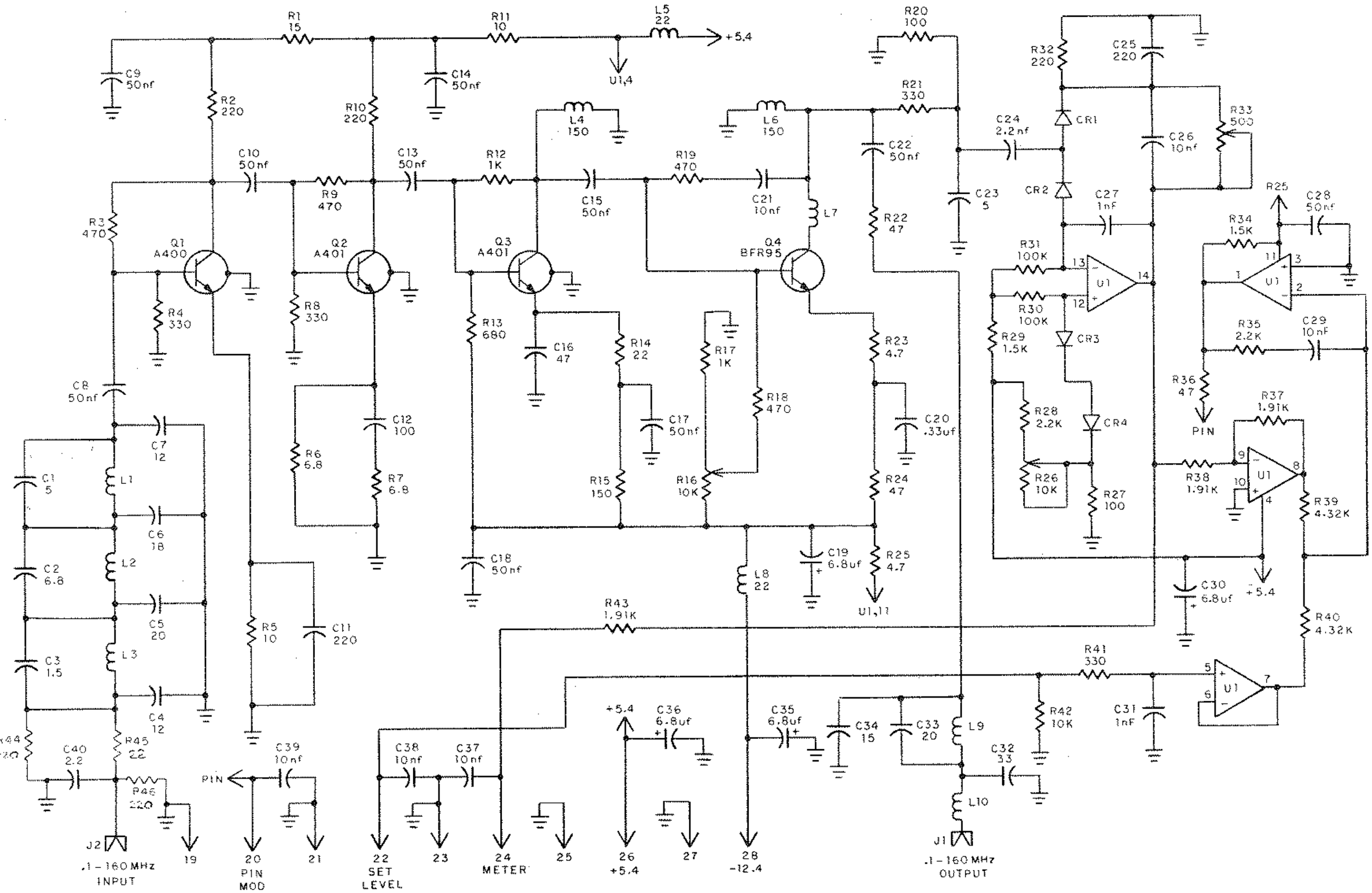



Figure 4

## PC ASSEMBLY, SO-1001

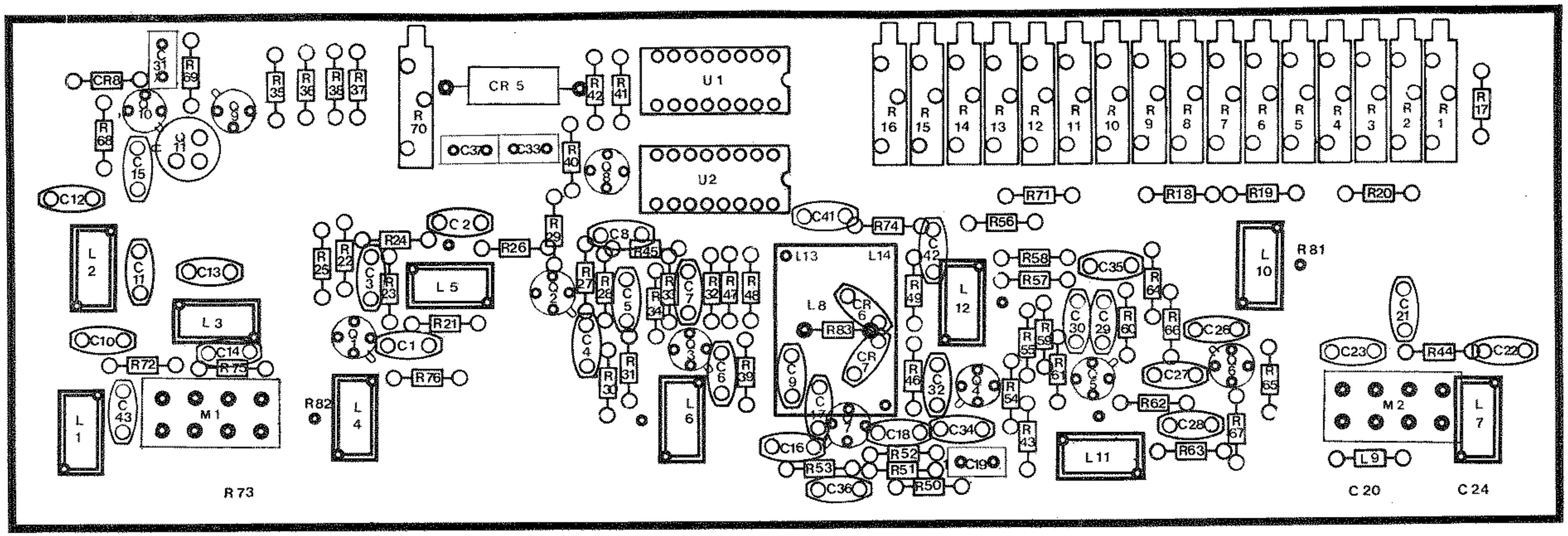


Figure 5

# PC ASSEMBLY, IM-1007

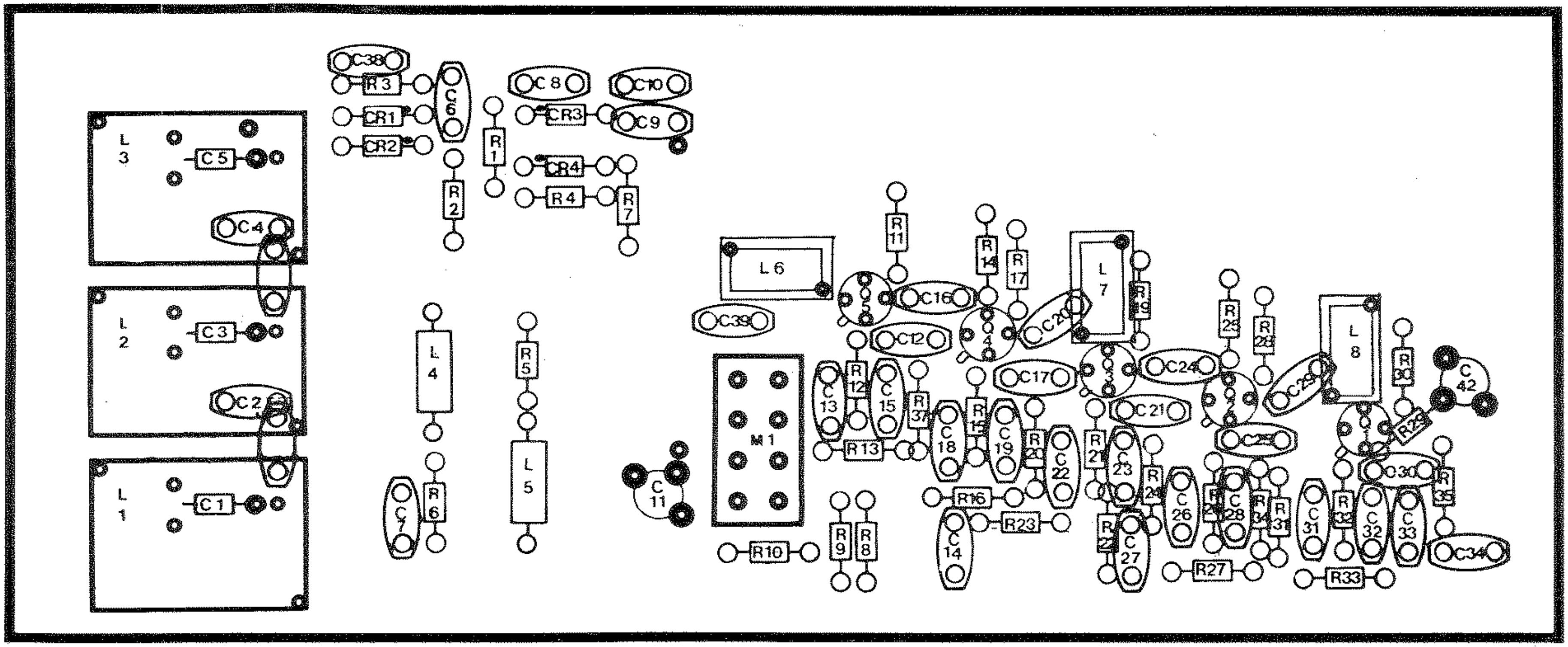



Figure 6

# PC ASSEMBLY, OA-1106

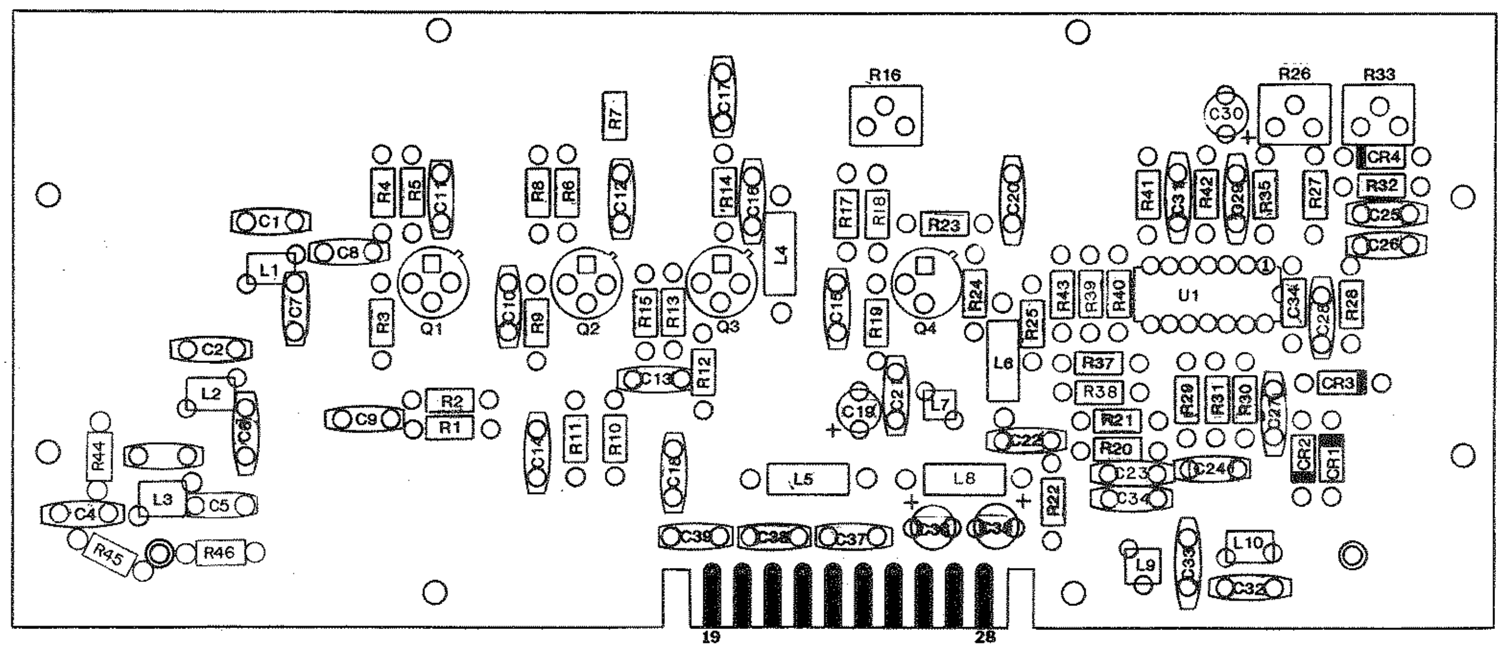



Figure 7

# TABLE OF CONTENTS

## INTRODUCTION

The GPIB interface implements a standardized form of serial remote control and provides the necessary hardware to connect an instrument to the GPIB, also referred to as the 488-bus.

### Functional Purpose

The GPIB interface allows remote programming of the synthesizer via the GPIB (General Purpose Interface Bus) in accordance with the IEEE Std 488-1978.

The following subset describes the specific capabilities.

| | | |
|---|---|---|
| SH0 | Source handshake | None |
| AH1 | Acceptor handshake | Complete |
| T0 | Talk | None |
| L1 | Listen | Basic listener; Listen Only |
| SR0 | Service request | None |
| RL2 | Remote/Local | No local lockout |
| PP0 | Parallel poll | None |
| DC0 | Device clear | None |
| DT0 | Device trigger | None |
| C0 | Controller | None |
| E1 | Driver type | Open collector drivers |

Three basic functions are accessible through appropriate commands: frequency, output level and Local/Remote mode. In the "LISTEN ONLY" mode **all** valid commands are accepted without regard to the device address, but in the "ADDR'D" mode only commands preceded by the selectable "LISTEN" address.

## Physical Aspects

Two piggy-backed and interconnected boards the SEC 1022 and the SER 1023 make up an interface unit.

They are mechanically attached to the rear panel by 4 screws: the SEC facing to the rear with the standard bus connector, a switch for address and listen mode, a "LISTEN" LED, and a second connector intended for an external attenuator or another BCD controlled device.

Internally all ("parallel") connections are made through a single-row header/plug arrangement located on the SER board. These are compatible with the pinout of the PE 1021 (parallel interface) board.

The physical interconnection to the GPIB through the 23 pin rear panel connector has the standard pinout:

| PIN | SIGNAL | FUNCTION | |
|---|---|---|---|
| 1 | DIO1 | Bit 1 | data bus |
| 2 | DIO2 | Bit 2 | data bus |
| 3 | DIO3 | Bit 3 | data bus |
| 4 | DIO4 | Bit 4 | data bus |
| 5 | EOI | End or Identify | management bus —inactive— |
| 6 | DAV | Data Valid | byte transfer bus (handshake) |
| 7 | NRFD | Not Ready for Data | byte transfer bus (handshake) |
| 8 | NDAC | Not Data Accepted | byte transfer bus (handshake) |
| 9 | IFC | Interface Clear | management bus |
| 10 | SRQ | Service Request | management bus —inactive— |
| 11 | ATN | Attention | management bus |
| 12 | Shield | Shield | |
| 13 | DIO5 | Bit 5 | data bus |
| 14 | DIO6 | Bit 6 | data bus |
| 15 | DIO7 | Bit 7 | data bus |
| 16 | DIO8 | Bit 8 | data bus —inactive— |
| 17 | REN | Remote Enable | management bus |
| 18 | GND(6) | Ground return for DAV | |
| 19 | GND(7) | Ground return for NRFD | |
| 20 | GND(8) | Ground return for NDAC | |
| 21 | GND(9) | Ground return for IFC | |
| 22 | GND(10) | Ground return for SRQ | |
| 23 | GND(11) | Ground return for ATN | |
| 24 | GND,LOGIC | Logical ground | |

**Setup**

Connect bus cable.

Set rear panel switch "S6" to desired mode: LISTEN ONLY or "ADDR'D".

If the addressed mode of operation is selected, check and set if necessary the 5 bit address switch to the chosen one of 31 numbers.

To set a desired address from 0 to 30 follow this table:

| ADDRESS (5bits) | Equivalent character | 7bit dec. | ASCII codes | Switch Settings A5 | A4 | A3 | A2 | A1 |
|---|---|---|---|---|---|---|---|---|
| 0 | SP | 32 | | 0 | 0 | 0 | 0 | 0 |
| 1 | ! | 33 | | 0 | 0 | 0 | 0 | 1 |
| 2 | " | 34 | | 0 | 0 | 0 | 1 | 0 |
| 3 | # | 35 | | 0 | 0 | 0 | 1 | 1 |
| 4 | $ | 36 | | 0 | 0 | 1 | 0 | 0 |
| 5 | % | 37 | | 0 | 0 | 1 | 0 | 1 |
| 6 | & | 38 | | 0 | 0 | 1 | 1 | 0 |
| 7 | ' | 39 | | 0 | 0 | 1 | 1 | 1 |
| 8 | ( | 40 | | 0 | 1 | 0 | 0 | 0 |
| 9 | ) | 41 | | 0 | 1 | 0 | 0 | 1 |
| 10 | * | 42 | | 0 | 1 | 0 | 1 | 0 |
| 11 | + | 43 | | 0 | 1 | 0 | 1 | 1 |
| 12 | , | 44 | | 0 | 1 | 1 | 0 | 0 |
| 13 | - | 45 | | 0 | 1 | 1 | 0 | 1 |
| 14 | . | 46 | | 0 | 1 | 1 | 1 | 0 |
| 15 | / | 47 | | 0 | 1 | 1 | 1 | 1 |
| 16 | 0 | 48 | | 1 | 0 | 0 | 0 | 0 |
| 17 | 1 | 49 | | 1 | 0 | 0 | 0 | 1 |
| 18 | 2 | 50 | | 1 | 0 | 0 | 1 | 0 |
| 19 | 3 | 51 | | 1 | 0 | 0 | 1 | 1 |
| 20 | 4 | 52 | | 1 | 0 | 1 | 0 | 0 |
| 21 | 5 | 53 | | 1 | 0 | 1 | 0 | 1 |
| 22 | 6 | 54 | | 1 | 0 | 1 | 1 | 0 |
| 23 | 7 | 55 | | 1 | 0 | 1 | 1 | 1 |
| 24 | 8 | 56 | | 1 | 1 | 0 | 0 | 0 |
| 25 | 9 | 57 | | 1 | 1 | 0 | 0 | 1 |
| 26 | : | 58 | | 1 | 1 | 0 | 1 | 0 |
| 27 | ; | 59 | | 1 | 1 | 0 | 1 | 1 |
| 28 | < | 60 | | 1 | 1 | 1 | 0 | 0 |
| 29 | = | 61 | | 1 | 1 | 1 | 0 | 1 |
| 30 | > | 62 | | 1 | 1 | 1 | 1 | 0 |

**Note** that 31 is reserved for the "UNLISTEN" command, and cannot be used as a valid Listen address.

**Programmable Instrument Functions**

The GPIB interface will respond to the following "ADDRESS" (AD) and "ADDRESSED COMMANDS" (AC) which are sent in the command mode with ATN true:

| | | | ASCII | | |
|---|---|---|---|---|---|
| Mnemonic | Command | Class | char. | dec.code | Resulting action |
| MLA | My Listen Address | AD | SP to > | 32 to 62 | Device listens and goes remote on 1st numeric character |
| UNL | Unlisten | AD | ? | 63 | Device unlistens, but stays in remote. |
| GTL | Go to local | AC | SOH | 1 | Returns to local, if in remote. No action if in local. |

The following device dependent functions can be controlled by the "DD" type commands with ATN false when in the "LISTEN" state:

| FUNCTION | ASCII coded command string (characters) | Notes |
|---|---|---|
| (1) Frequency, all 10 digits | F, 10 numerals, LF | 1st numeral = MSD |
| (2) Frequency, N least significant digits | F,N numerals, LF | 1st numeral = MSD |
| (3) Output level only in -dbV, 9 db range in 1 db steps | A, one numeral, LF | numeral = x 1 db |
| (4) Output level with optional attenuator in -dbV in 1dB steps, range 00 to 99 | A, two numerals, LF | 1st numeral = x 10 db<br>2nd numeral = x 1 db |
| (5) Return to local mode | GTL (SOH) | |
| (6) Transfer data to output registers | LF | SEE NOTE BELOW |

The last character in a command string (LF) affects internal transfer of the stored data word. It is usually appended automatically by the controller.

**Note** that the additional ASCII characters used in the command strings have these code values:

| Character | Dec. code | Character | Dec. code |
|---|---|---|---|
| GTL | 1 | 0 | 48 |
| LF | 10 | 1 | 49 |
| A | 65 | 2 | 50 |
| F | 70 | 3 | 51 |
| | | 4 | 52 |
| | | 5 | 53 |
| | | 6 | 54 |
| | | 7 | 55 |
| | | 8 | 56 |
| | | 9 | 57 |

## CONDENSED PROGRAMMING INSTRUCTIONS

1. **General:** The GPIB interface option provides remote control of PTS synthesizers via the GPIB bus. Both frequency and level can be set by appropriate bus commands. The following subsets are implemented: SHO, AH1, TO, L1, SRO, RL2, PPO, DCO, DTO, CO, E1 according to IEEE Standard 488-1978.

2. **Data Format:**

 2.1 **Listen Address:** Switch-selectable to any one of 31 standard ASCII codes 32 to 62 (decimal)

 2.2 **Frequency Command:** A string starting with letter F (ASCII 70) followed by 10 numerals. After initial frequency command, less than 10 numerals can be used to update less significant digits of frequency.

| **Examples:** | Wanted | Command String |
|---|---|---|
| | 101.51 MHz | F 1 0 1 5 1 0 0 0 0 0 |
| | 125.4 KHz | F 0 0 0 1 2 5 4 0 0 0 |
| Change last 3 digits to 10.4 Hz | | F 1 0 4 |

 2.3 **Level Command:** A string starting with letter A (ASCII 65) followed by 2 numerals. The first numeral (of two) represent 10dB steps. The second numeral 1dB steps. The complete number is interpreted as dB below 1V into 50 ohms (or +13dBm).

| **Examples:** | Wanted | Command String | |
|---|---|---|---|
| | −67dBV | A 6 7 | 10dB steps available only with 90dB optional step attenuator. |
| | − 9dBV | A 0 9 | |
| | − 3dBV | A 0 3 | |

Both strings can be combined in any sequence into one command word, such as:

F 1 2 5 0 0 0 0 0 0 0 A 0 6 For −6dBV at 125 MHz

OR

A 2 5 F 0 0 0 5 0 0 0 0 0 0 For −25dBV at .5 MHz

 2.4 **Other Commands:** Go Local (GTL) is implemented (Subset RL2), but also as device dependant command (DD) by transmitting ASCII Decimal Code 1 as data byte.

 2.5 **Terminator:** Any command must be terminated by LF (LINEFEED) ASCII Decimal Code 10. This character effects internal transfer.

**NOTE:** String characters other than A and F within a command string are disregarded, except GTL.

3. **Transfer Rate:** Internally limited to 20$\mu$s minimum for each Command. Generally slower depending on controller and programming software.

4. **External Connections/Outputs:**

 4.1 BUS INTERFACE according to 488 standard by 24 PIN receptacle, Amphenol type 57-20240 or equivalent.

5. **Mechanical Requirements:** This option is an integral part of the PTS instrument and takes the place of the BCD-TTL parallel interface.

## Programming Examples

Keep in mind that the basic data transfer on the bus is bit parallel byte serial, one byte at a time. Any program therefore has to generate data words made up of a string of ASCII characters. Each character represents a specific control code. The required characters for a desired function are listed under Programmable instrument functions (page 00). Specific details for using them depend upon the programming language of the particular controller.

However, in any case, when executing a program the controller has to send the following sequence to the instrument:

| | |
|---|---|
| 1st byte: | MLA (ASCII code range 32-62). Not needed for "LISTEN ONLY". |
| 2nd byte: | ASCII character code for desired function (1, 65 or 70) |
| 3rd byte: | ASCII character code for 1st digit of associated numerical value, if any (between 48 and 57) |
| 4th byte: | ASCII character code for 2nd digit, if any |
| ith byte: | ASCII character code for last digit, if any |
| (i + 1)th byte: | ASCII code for other function if any |
| (i + 2)th byte: | ASCII code for 1st digit relating to "other" function if any |
| nth byte: | ASCII code for last digit, if any |
| (n + 1)th byte: | ASCII code for LF (10) |
| optional byte: | ASCII code for UNL (63) |

To give a numerical example, assume we want to set the instrument to: 123.4567890 MHz at a level of -3dbV and use address 13.

The command string would be: (expressed in ASCII decimal code.)

| | | | | | | |
|---|---|---|---|---|---|---|
| Byte 1 | : | 45 | (-) | MLA | with ATN true | = AD type command |
| Byte 2 | : | 70 | (F) | DAB 1 | with ATN false | = DD type command |
| Byte 3 | : | 49 | (1) | DAB 2 | with ATN false | = DD type command |
| Byte 4 | : | 50 | (2) | DAB 3 | with ATN false | = DD type command |
| Byte 5 | : | 51 | (3) | DAB 4 | with ATN false | = DD type command |
| Byte 6 | : | 52 | (4) | DAB 5 | with ATN false | = DD type command |
| Byte 7 | : | 53 | (5) | DAB 6 | with ATN false | = DD type command |
| Byte 8 | : | 54 | (6) | DAB 7 | with ATN false | = DD type command |
| Byte 9 | : | 55 | (7) | DAB 8 | with ATN false | = DD type command |
| Byte 10 | : | 56 | (8) | DAB 9 | with ATN false | = DD type command |
| Byte 11 | : | 57 | (9) | DAB 10 | with ATN false | = DD type command |
| Byte 12 | : | 48 | (0) | DAB 11 | with ATN false | = DD type command |
| Byte 13 | : | 65 | (A) | DAB 12 | with ATN false | = DD type command |
| Byte 14 | : | 51 | (3) | DAB 13 | with ATN false | = DD type command |
| Byte 15 | : | 10 | (LF) | DAB 14 | with ATN false | = DD type command |
| optional | : | 63 | (?) | UNL | with ATN true | = AD type command |

(Commentary notations)

This example implemented in BASIC with a PET controller would require these program lines:

```
10 OPEN 200, 13   or   OPEN 200, 45
20 PRINT #200, "F1234567890A03"
```

A subsequent change in level to 0dbV would be commanded by

```
30 PRINT #200, "A00"
```

A return to local would be affected by

```
40 PRINT #200, CHR$(1)
```

**Note** that in this example with PET/BASIC language, the PRINT #200 portion generates the MLA byte, also the LF and UNL bytes are automatically appended.

Using an HP model 9825A calculator as controller would require the following program:

```
0 : wrt713, "F1234567890A03"          (equivalent of line 20)
1 : wrt713, "A00"                     (equivalent of line 30)
```

It should also be noted that the sequential order of dual function commands is immaterial.

**Note:**

A frequency command string with less than the full 10 digits will update only the least significant digits.

**Example:**

Assume previous setting : 125000680.0 Hz

Next command string containing: F1234

The resulting new frequency setting is: 125 000 123.4 Hz

Note: Only the 4 least significant digits were changed.

## PRINCIPLES OF OPERATION

In order to follow the later part better, a general understanding of the GPIB concept is more or less assumed. A very brief summary is included here with the intent to help clarify the other part.

### Condensed GPIB Concept

It is a standardized form of a serial digital data transfer system. Messages (addresses, addressed commands and data) are being sent over an 8 bit wide bus from a designated "Talker" to one or more "Listeners" supervised by a controller, usually a computer. The controller uses a set of 5 management lines to keep order and to maintain priorities. One of these lines called ATN (attention) determines how data on the bus are to be interpreted. A Low (also TRUE) state signifies commands of various kinds whereas the high state (False) identifies the message bytes as data, typically functions and related values. Any actual transfer of a message byte is also verified through a 3-line handshake procedure, which is to ensure that no new data are being sent until the last and slowest listener has accepted them and is ready for new data. The rate of transfer is both variable and asynchroneous. Theoretically, rates up to 1MHz are possible.

There can be up to 15 devices on one bus, however, address space is provided for up to 31 talkers and listeners.

Bus connections can be either star-like or in tandem, but are limited in total length to 20m.

The physical connector is a 24 contact ribbon connector with metric hardware. Standard cable plugs have a male/female configuration to facilitate through-connections. The logic convention for all bus signals is negative true, i.e.,

a low state = true = Logic 1 (< 0.8V)
a high state = false = Logic 0 (> 2.0V)

In summary there are:

| Line | Mnemonic | Origin of signal |
|---|---|---|
| 8 lines for data byte | DAB | controller, talker |
| 5 management lines: | | |
| Attention | ATN | controller |
| Interface clear | IFC | controller |
| End or Identify | EOI | controller, talker |
| Service request | SRQ | talker, listener |
| Remote enable | REN | controller |
| 3 handshake lines: | | |
| Data valid | DAV | talker |
| Not data accepted | NDAC | listener |
| Not ready for data | NRFD | listener |

**Execution of a Valid Bus Command**

All data transfers from the GPIB involve an "acceptor handshake" operation. The interface will handshake only under two conditions:

1. when ATN is true (low), which is a universal command in anticipation of an "addressed command".

2. when it is in the "LISTEN" state, set by either S6 to position "LISTEN ONLY", or by the listen flipflop U19. (See schematics Fig. 1 and Fig. 2.)

Either of these conditions forces HSE high and gates NRFD and NDAC signals to be sent out in response to an incoming DAV low signal, which indicates the presence of a valid data byte on the D10 lines. DAV triggers a 1 $\mu$s strobe pulse STR from U18 which acts as a master clock within the module. If the handshake is enabled, as described before then STR sets NRFD low and NDAC high, subject to a possible delay by the INH signal from U21. Finally, when DAV goes high again indicating the end of valid data, NDAC clears first, then NRFD is released (goes high).

The associated data byte on the DIO lines is processed depending on the state of ATN. When ATN is low (true) incoming data are handled as addresses or addressed commands. If the received byte matches the address register (switches S1 through S5), the comparator U2, U16 set the MLA line high which allows the listen clock pulse LCK to set the listen flipflop U19, which in turn enables subsequent data acceptance.

Once set to listen, and with ATN high (false), incoming bytes are now handled as functional data in various ways through the STR derived data clock DCK. Comparator U11 discriminates against any other characters but numerals 0 through 9 and gates DCK to become the number clock pulse NCK. Also the remote ff U17 is set by NCK and DAV, putting the module in the REMOTE mode. An UNL byte decoded by U5 does the opposite and clears the listen ff without affecting the remote ff. A GTL command (DD or AC-type) will clear the remote ff U17.

NCK is gated once more and turns into the frequency clock FCK following receipt of the ASCII"F" byte, or becomes the A-clock ACK after receiving the "A" character. Only one of these two clocks can be active at a time. The "A" and "F" characters are decoded by U6 and U14 and cause proper gating of the A & F dual ff U8.

**Note** that ACK or FCK has as many pulses or transitions as the number of numerals following the "A" or "F" character.

The end of a data string is recognized by the LF character. Decoder U10 and DCK generate the transfer pulse TRA, which in turn triggers reset signals ARES and FRES, all being used eventually in the serial to parallel conversion process on the SER board. The previously mentioned INH signal, also triggered by TRA in U21 is timed to ensure a minimum waiting period of 20 $\mu$s before another transmission cycle.

A few more signals are derived from REM. One is called OC for output control and affects the tristate output registers. Another, called FPE for front panel enabling, involves U15 and Q1 and generates nominally 5V in the LOCAL mode. Q2 produces similarly 5V in the REMOTE mode, the signal is called REL for remote LED. Also a monitor signal LIL provides a low state in the LISTEN state.

The circuits described so far are all located on the SEC 1022 board (Serial entry control). The serial to parallel conversion takes place on the SER 1023 (serial register) board as follows.

Four bits of the 7bit (ASCII) byte, called SB1, 2, 4, 8 are passed on for conversion. Since only numerals enable the applicable serial clock nothing else can be converted. Numerical data following "F" are clocked into a set of 10 bit shift registers U11, 19, 14, 22, 4 by FCK, those following "A" are clocked into a set of 2 bit shift registers U6, 13 by ACK. The respective clock pulse also generates an enabling signal, FE1 - 10 in the F-channel with U1, 2, 3, and AE1 - 2 in the A-channel with U5. When the output registers, U9, 17, 10, 18, 12, 20, 15, 23, 24 of the F-channel and U7, 21 of the A-channel are thus enabled, the following transfer pulse TRA stores the available data from the shift registers in the output registers, overwriting any previously stored data. Finally the stored data appear at the output lines whenever OC is low, i.e., being in the REMOTE mode. Otherwise, with OC high, the outputs are in a high impedance state, but stored data are not affected.

Responding to the last digit in the A-channel is a D to A converter implemented by the 10 to 1 decoder U8 and a bank of resistors. The resulting analog voltage ANL is tailored to produce 1db incremental changes in the rf output level of the instrument.

Option 1023/160 uses a BCD to BIN converter U16A to convert the 4 digit #9 lines to a hexadecimal format, equivalent to decimal 0 to 15. (0-150MHz)

Option 1023/200 uses another output register U16B to provide one least significant bit of the 10th digit. (100MHz)

Option 1023/500 (1023 Rev. 2) uses a different enlarged shift register U4 and provides additional output lines for handling the '200' and '400' MHz bits through U16B.

The following list in section 2.3 summarizes the key signals and associated functions.

## List of Key Signals

| Name | Origin board/IC | Quiesc. State | Comments |
|---|---|---|---|
| AB1 | SER/U21 | x | Bit weight 1 of A lines, for attenuator control |
| AB2 | SER/U21 | x | Bit weight 2 of A lines |
| AB4 | SER/U21 | x | Bit weight 4 of A lines |
| AB8 | SER/U21 | x | Bit weight 8 of A lines |
| ACK | SEC/U1 | L | STR derived clock pulse for A-channel conversion |
| AE1 | SER/U5 | H | ACK triggered enabling signal for digit #1 of A-channel, reset by ARES |
| AE2 | SER/U5 | H | ACK triggered enabling signal for digit #2 of A-channel |
| ANL | SER/U8 | x | Analog voltage for level control, appr. range 2V |
| ATN | Bus,SEC/U7 | x | Low in "command mode", high in "DD mode" |
| ARES | SEC/U1 | H | TRA triggered reset pulse for A-channel |
| DAV | Bus,SEC/U7 | H | Goes low after talker has valid data on bus |
| DCK | SEC/U16 | L | STR derived pulse, occurs for each byte in DD mode |
| FCK | SEC/U1 | L | NCK derived pulse, enabled after "F" byte |
| FE1-10 | SER/U1,2,3 | H | FCK triggered enabling signal for F-channel |
| FPE | SEC/Q1 | H | Feeds front panel switches & local light. Goes low in remote |
| FRES | SEC/U18 | H | TRA triggered reset pulse for F-channel |
| GTL | SEC/U12 | L | Goes high on data byte with code value 1, clears REMOTE in either AC or DD command mode |
| HSE | SEC/U20 | L | Goes high in command mode (ATN Low) or LISTEN state, enables NDAC and NRFD for handshake |
| IFCI | Bus,SEC/U1 | H | Clears Listen ff on either power-on or bus command |
| INH | SEC/U21 | L | 20 μs pulse, TRA triggered, inhibits handshake |
| LIL | SEC/U13 | H | Listen monitoring signal low when in LISTEN mode |
| LIST | SEC/U19 | L | Goes high when addressed, enables DD mode, clears when receiving UNL command |
| LOC | SEC/U17 | H | Goes low when REM is set (high) by NCK, resets high on GTL command or REN high or power-on |
| MLA | SEC/U16 | L | Goes high when receiving address = switch settings |
| NCK | SEC/U6 | L | DCK derived clock pulse, enabled by numerals, one pulse per digit, also sets REM. |
| NDAC | SEC/U13 | x | Controlled by all Listeners, low when enabled by HSE, temporarily high = Data accepted following DAV if LISTENER responds. |
| NRFD | SER/U13 | H | Controlled by all Listeners on bus, pulled Low = Not Ready following DAV, if listener responds. Released high again after NDAC gone low. |
| OC | SEC/U15 | H | Goes low in REMOTE mode, enabling output registers |
| PUR | SEC/U9 | H | Goes temporarily low on power-on. |
| QHS | SEC/U19 | L | Controls handshake signals, goes temp. high in normal handshake cycle. |
| RCL | SEC/U15 | H | Initializing signal, temporarily low only on power-on. |
| REL | SEC/Q2 | L | Feeds REMOTE light on front-panel, goes high in remote. |
| REM | SEC/U17 | L | Complementary signal to LOC, high in REMOTE Mode |
| REN | Bus,SEC/U9 | x | Low in remote enable state, set by controller |
| SB1 | SEC/U4 | x | DIO1 derived data bit, weight 1, high when true |
| SB2 | SEC/U4 | x | DIO2 derived data bit, weight 2, high when true |
| SB4 | SEC/U4 | x | DIO3 derived data bit, weight 4, high when true |
| SB8 | SEC/U4 | x | DIO4 derived data bit, weight 8, high when true |
| STR | SEC/U18 | L | DAV derived master clock pulse, one per byte |
| TRA | SEC/U13 | L | DCK derived, LF enabled pulse, stores outputs. |

a

## SPECIFICATIONS

The interface consists of the SEC 1022 board and the SER 1023 board.

1. **Interface Functions:**

   Subset implemented as per IEEE-Std 488-1978.

   SH0, AH1, T0, L1, SR0, RL2, PP0, DC0, DT0, C0

   Output driver type E1 = Open collector

2. **Inputs:**

   GPIB signals via J1 as per standard with DIO8, EOI and SRQ inactive.

3. **Internal Decoding:**

| Name | ASCII char. | ASCII dec. | Function |
|---|---|---|---|
| GTL | SOH | 1 | Local mode |
| LF | LF | 10 | Transfer data |
| LAD | SP...> | 32-62 | Listen addresses |
| Numerals | 0-9 | 48-57 | Control parameter |
| UNL | ? | 63 | Unlisten |
| A | A | 65 | Level control code |
| F | F | 70 | Frequency control code |

4. **Outputs via P1:**

   For **frequency** control, tristate, LS-TTL compatible

   Option/160: 36 parallel bits, digit #1 through digit #8

   BCD coded, digit #9 hexadecimal coded: 0-F

   Option/200: 37 parallel bits, all digits BCD coded, digit #10 one bit only: 0-1

   Option/500: 39 parallel bits, all digits BCD coded,

   digit #10 three bits only: 0-7, (4)

   For **level** control, all options:

   4 parallel bits, BCD coded for attenuator control

   LSTTL compatible, tristate, also available via J2.

   + analog level control voltage, 2V maximum.

   Controlled voltage for panel switches, 5V max. (FPE)

   Monitor signals for REMOTE, LOCAL and LISTEN status.

5. **Power requirements:**

   5.4 V @ 520-540 mA typical

# SERVICE

## Maintenance

No maintenance is normally required. Only components subject to wear are the external connectors and the address switches. They are expected to outlast the normal life expectancy of the instrument.

## Trouble Shooting

### General

The interface circuitry is essentially digital, involving basically TTL type integrated circuits. Generally speaking, fault finding techniques require the use of logic probes and or logic analyzers, since many of the digital processes are sequential in nature.

Furthermore, with any bus controlled instrument, malfunctions may also be caused by the controller, by program errors (software) and possibly by other devices on the bus. Such possible causes have to be eliminated first:

Verify, if possible the proper operation of the bus controller. Suitable bus testers are available from several sources.

Check operation without any other devices on the bus to eliminate possible hangup problems caused by another device.

Check operation of the instrument in the "LOCAL" mode with the bus cable disconnected. If this mode cannot be established, as evidenced by the front panel LED, trouble could also be elsewhere in the instrument. If "LOCAL" is O.K., then the interface is most likely at fault.

For most of the following checks we require access to the inside. Remove both covers which allows limited probing on many key points.

Before performing any digital tests, check first:

The 5.4V rail at the power supply board. If O.K., check the supply voltages on pin #6 interconnecting SEC and SER to be the same as on the rail, on an accessible Vcc pin #16 of each board: A1 on SEC, U1 on SER. These voltages are typically 5.0 ± 0.2V. If less than 4.7V, decoupling resistors R23 on SEC and R33, 34 on SER are suspect. Any required repair requires removal of the interface. Proceed further only after the power supply conditions are normal.

**Digital Fault Tracking**

The following covers a few major fault conditions and related fault finding checks, but limited to what can be diagnosed without removing the interface. Probing points are therefore restricted to those on the bus connector, the contact points on J1, SER, on some IC's at the edge of SER and the output connections P1, SER.

If these tests are inconclusive, return of the suspect unit for factory test repair is recommended. If test results and inspection indicate specific defects, repair may be attempted after removing and disassembling the interface.

In the following test procedures we try first static checks using simple logic probes or a voltmeter. Dynamic test are necessary to check on sequential logic and require at least a pulse indicating probe; a transition counter would be useful in tracing more subtle faults. When a signal name is referred to in capital letters, consult also the list of key signals for more information which should prove helpful in diagnosing the problem.

For static tests good/bad limits are:

| State | Good | Bad |
|---|---|---|
| Low | >0V, <.8V | >0.8V |
| High | >2.4V | <2.4V |

unless otherwise noted. Note that with a good Low, there is a small positive voltage, never 0. A 0 voltage indicates a **short.**

**Major Faults**

1: No "LOCAL" control function

Disconnect bus cable. Static tests. Check progressively.

| Signal | At | On | Good State | Possible defects if test result is bad |
|---|---|---|---|---|
| FPE | Coll. Q1 | SEC | >4V | short, Q1, U15, R22, OC stuck low |
| FPE | 17J1 | SER | >4V | interconnection open, shorts |
| FPE | 34P1 | SER | >4V | track on SER, shorts |
| FPE | common rail on front panel switches | | >4V | track on SER, shorts |
| OC | 16J1 | SER | High | U15, shorts (SEC,SER) |
| LOC | 19J1 | SER | High | Shorts, U17 |
| RCL | R29, C7 | SEC | Low | U7, 9, 15 |

The following tests are done with bus connected, but no other devices on bus.

2: No response to commands, does not go remote

Verify first proper match of address setting on rear panel switch with address used by controller/talker.

If O.K., set switch to "LISTEN ONLY" and execute a command sequence. If instrument responds, trouble could be in address related circuits on SEC; suspects are S1-5, U2, 3, 4, 5, 9, 16. However, there could also be a controller problem, not sending the correct address. If no response, reset switch to "ADD'D" position, and try first:

**Static Tests**, with controller idling, but REN asserted (low).

Check progressively.

| Signal | At | On | Good State | Possible defects, if bad | Comments |
|---|---|---|---|---|---|
| REN | pin 17 | bus | Low | controller | |
| | 15A1 | SEC | Low | connection | |
| RCL | R29,C7 | SEC | High | U7, 9, U15, C7 | |
| IFC | pin 9 | bus | High | controller, short | |
| IFCI | 14U9 | SEC | High | C2,U19 | |
| ATN | pin 11 | bus | High | controller, short | |
| $\overline{ATN}$ | 2U20 | SEC | Low | U7, open | |
| ATN | 3U16 | SEC | High | U7, short | |
| NRFD | pin 7 | bus | High | controller, short, U13 | Handshake |
| QHS | 5U19 | SEC | Low | U19, U9 | related |
| PUR | 4U19 | SEC | High | U9, 19, C1, shorts | related |
| HSE | 11U20 | SEC | Low | U20, 7 | related |
| DAV | pin G | bus | High | controller, short | |
| NDAC | pin 8 | bus | High | controller, short, U13 | related |
| $\overline{DAV}$ | 2U18 | bus | Low | U7 | related |
| DIO7 | pin 15 | bus | High | controller, short | affects: |
| D7 | 1U165 | SEC | High | U3, 7, Open | Listen address |
| Clock | 13U19 | SEC | High | U20, short | Listen Clock |

If earlier test in LISTEN ONLY mode was good, but addr'd mode was not, check also other data lines.

| | | | | | |
|---|---|---|---|---|---|
| DIO6 | pin 14 | bus | High | controller, short | may impair |
| D6 | 2U3 | SEC | High | U3,U4, Open | |
| DIO5 | pin 13 | bus | High | controller, short | proper addressing |
| D5 | 4U3 | SEC | High | U3, U4, Open | |
| DIO4 | pin 4 | bus | High | controller, short | proper addressing |
| $\overline{D4}$ | 10J1 | SER | Low | U4, Open | |
| DIO3 | pin 3 | bus | High | controller, short | proper addressing |
| $\overline{D3}$ | 9J1 | SER | Low | U4, Open | |
| DIO2 | pin 2 | bus | High | controller, short | proper addresssing |
| $\overline{D2}$ | 8J1 | SER | Low | U4, open | |
| DIO1 | pin 1 | bus | High | controller short | proper addressing |
| $\overline{D1}$ | 7J1 | SER | Low | U4, open | |

If static tests indicate normal conditions proceed with:

**Dynamic Tests**

Send a command string containing at least **one** numeral and monitor with a pulse indicating probe at the same time progressively. Command string assumed to end with UNL.

| Signal | At | On | Good Condition | Possible defects, if bad | Comments |
|---|---|---|---|---|---|
| DAV | pin 6 | bus | one ‾\|_\|‾ each byte | controller | All |
| $\overline{DAV}$ | 2U18 | SEC | one _\|‾\|_ each byte | U7, conn | functions |
| STR | 5U16 | SEC | same as $\overline{DAV}$ | U1R, R45, C3 | impaired |
| MLA | 11U19 | SEC | _\|‾\|_ once/mes. | U2, U16 | Listening |
| LIST | 9U19 | SEC | _\|‾\|_ once/mes. | U19, 20 | impaired |
| HSE | 11U20 | SEC | _\|‾\|_ once/mes. | U20, U13 | impaired |
| LIL | 20J1 | SER | ‾\|_\|‾ once/mes. | U13 | Impaired |

3: No data transfer (goes remote, but no data transfer or only partial)

**Static tests**, with interface set to remote state.
Controller idle. Check progressively.

| | | | | |
|---|---|---|---|---|
| OC | 10U15 | SEC | Low | U15 |
| OC | 16J1 | SER | Low | connection |
| TRA | 8U13 | SEC | Low | U13 |
| TRA | 13J1 | SER | Low | connection |
| FRES | 12U18 | SEC | High | U18, short |
| FRES | 14J1 | SER | High | connection |
| FCK | 11J1 | SER | Low | U1,8, connection |

If O.K. so far, proceed with:

**Dynamic Tests**

Send a frequency command with 10 digits, monitor simultaneously progressively.

| Signal | At | On | Good | Possible defects, if bad | Comments |
|---|---|---|---|---|---|
| TRA | 13J1 | SER | _⎍_ once per command | U10,13,R24,49, connection | impairing transfer |
| TRA | 7U9 | SER | _⎍_ once per command | track | to output registers |
| FRES | 12U18 | SEC | ¯⊔¯ once per command | U18, connection | |
| FRES | 14J1 | SER | ¯⊔¯ once per command | connection | |
| FRES | 1U4 | SER | ¯⊔¯ once per command | track | |
| FCK | 11J1 | SEC | _⎍_ 10 times each | U1, 8, 6, 14 | impairing serial |
| FCK | 9U4 | SER | command | track | conversion |
| FE2 | 8U1 | SER | ¯⊔¯ once per command | U1, Conn. | impairing output |
| FE2 | 15U17 | SER | | | registers |
| FE6 | 14U2 | SER | ¯⊔¯ once per command | U2, U1 | |
| FE6 | 15U20 | | | | |
| FE100 | 14U3 | SER | ¯⊔¯ once per command | U3, 2, 1 | |
| FE100 | 9U16 | SER | ¯⊔¯ once per command | | |

If all of these checks prove O.K., check continuity of TRA line to all points on SER. If this is O.K., problem is more deep seated.

4: Single digit in error, otherwise OK

Most likely cause if faulty output register or an open control line FEx, TRA or OC to the particular digit. Check operation of these control lines **at the associated pins** of the IC in question, as indicated before. Check also the 4 output bit lines for possible-connection problems, open or shorts.

5: Same bit error in all digits

Example: Only even numbers would implicate bit 1, originating from **SB1** through U11, SER.

Check suspected **SB**xLine for activity. If dead, suspect SEC or interconnection. If O.K., check D1 line for activity. If bad, suspect associated IC, U11 for bit "1", U19 for bit "2", U14 for bit "4", U22 for bit "8".

Most any other problem is likely to be more complex and not expected to be resolved or repaired in the field.

## SEC-1022 Parts List

| Schematic Design | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 47uF, El. Tant. 6V | 30-5102 |
| C2 | 10nF, 80/20%, 50V, 25V | 23-0103 |
| C3 | 100pF, 10%, 500V, X5F | 22-0470 |
| C4 | 100pF, 10%, 500V, X5F | 22-0101 |
| C5 | 1nF, 10%, 500V, X5F | 22-0102 |
| C6 | 6.8uF, El. Tant. 16V | 30-5101 |
| C7 | 10nF, 80/20%, 50V, Z5V | 23-0103 |
| C8 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| C9 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| C10 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| C11 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| C12 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| C13 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| | **DIODES** | |
| CR1 | LED, green | 88-4955 |
| | **CONNECTORS** | |
| J1 | 24 contact, PC mount | 78-1024 |
| J2 | 5 contact, receptacle | 79-1005 |
| P1 | header strip, 20 contacts | 79-1002 |
| | **TRANSISTORS** | |
| Q1 | 2N2905 | 42-2905 |
| Q2 | 2N2905 | 42-2905 |
| | **RESISTORS** | |
| A1 | Resistor network, 28 resistors | 66-5001 |
| R5 | 2.2, 5%, ¼W | 11-0220 |
| R12 | 4.7K, 5%, ¼W | 11-0472 |
| R16 | 100, 5%, ¼W | 11-0101 |
| R18 | 1.5K, 5%, ¼W | 11-0152 |
| R19 | 150, 5%, ¼W | 11-0151 |
| R20 | 4.7K, 5%, ¼W | 11-0472 |
| R21 | 2.2K, 5%, ¼W | 11-0222 |
| R22 | 1K, 5%, ¼W | 11-0102 |
| R23 | 2.2, 5%, ¼W | 11-0220 |
| R24 | 2.2K, 5%, ¼W | 11-0222 |
| R29 | 330, 5%, ¼W | 11-0331 |
| R42 | 4.7K, 5%, ¼W | 11-0472 |
| R43 | 220, 5%, ¼W | 11-0221 |
| R44 | 4.7K, 5%, ¼W | 11-0472 |
| R45 | 6.8K, 5%, ¼W | 11-0682 |
| R46 | 10K, 5%, ¼W | 11-0103 |
| R47 | 6.8K, 5%, ¼W | 11-0682 |

## SEC-1022 Parts List (continued)

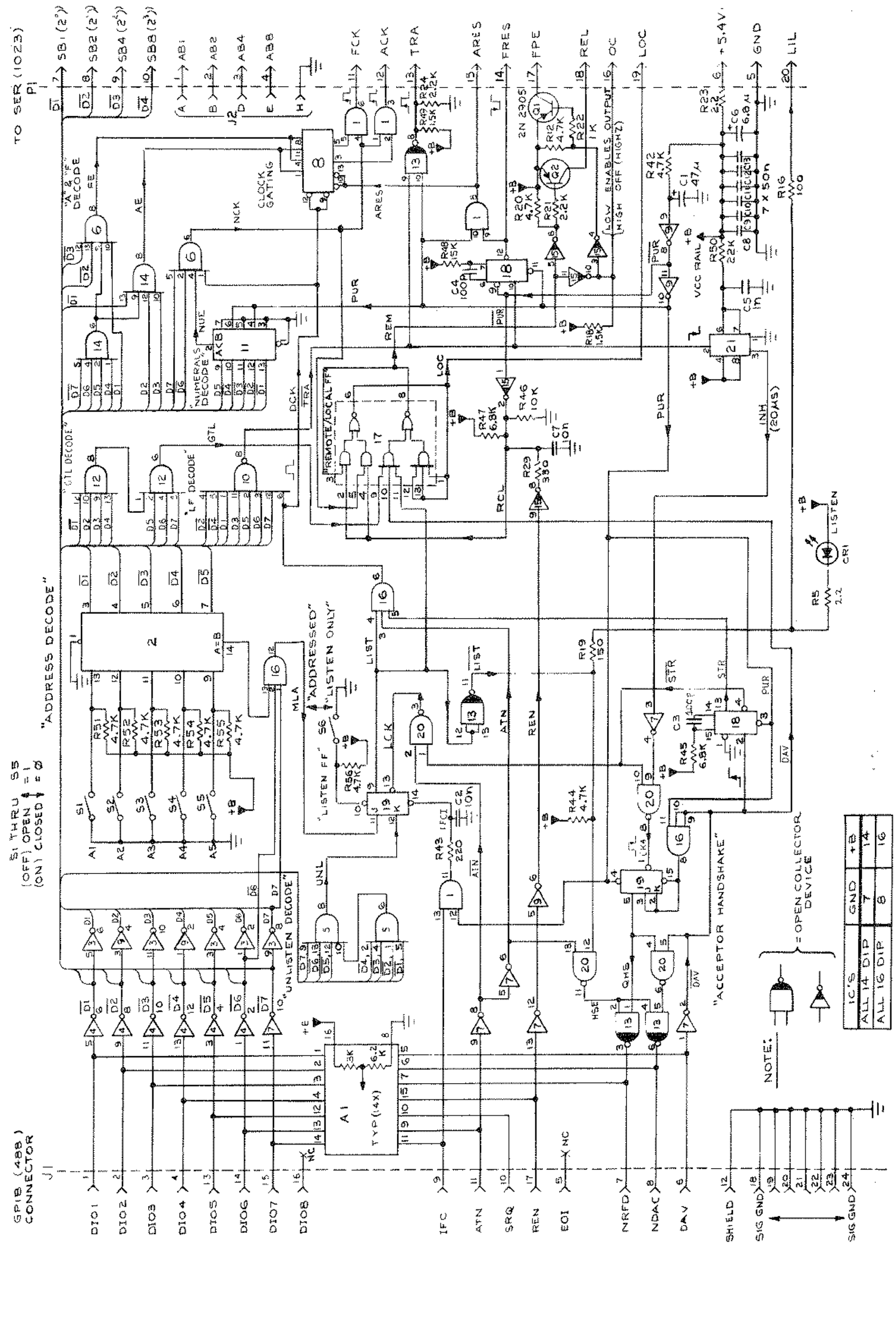
| Schematic Design | Description | PTS P/N |
|---|---|---|
| | **RESISTORS** (cont.) | |
| R48 | 15K, 5%, ¼W | 11-0153 |
| R49 | 1.5K, 5%, ¼W | 11-0152 |
| R50 | 22K, 5%, ¼W | 11-0223 |
| R51 | 4.7K, 5%, ¼W | 11-0472 |
| R52 | 4.7K, 5%, ¼W | 11-0472 |
| R53 | 4.7K, 5%, ¼W | 11-0472 |
| R54 | 4.7K, 5%, ¼W | 11-0472 |
| R55 | 4.7K, 5%, ¼W | 11-0472 |
| R56 | 4.7K, 5%, ¼W | 11-0472 |
| | **SWITCHES** | |
| S1-S6 | 6 PST DIP | 87-1008 |
| | **INTEGRATED CIRCUITS** | |
| U1 | 74LS08 | 63-0008 |
| U2 | 93L24 | 61-0024 |
| U3 | 74LS04 | 63-0004 |
| U4 | 74LS14 | 63-0014 |
| U5 | 74LS21 | 63-0021 |
| U6 | 74LS21 | 63-0021 |
| U7 | 74LS14 | 63-0014 |
| U8 | 74LS107 | 63-0107 |
| U9 | 74LS04 | 63-0004 |
| U10 | 74LS30 | 63-0030 |
| U11 | 93L24 | 61-0024 |
| U12 | 74LS21 | 63-0021 |
| U13 | 7438 | 60-0038 |
| U14 | 74LS21 | 63-0021 |
| U15 | 7405 | 60-0005 |
| U16 | 74LS11 | 63-0011 |
| U17 | 74LS51 | 63-0051 |
| U18 | 74LS123 | 63-0123 |
| U19 | 74LS112 | 63-0112 |
| U20 | 74LS00 | 63-0000 |
| U21 | 555 | 64-0555 |

## SER-1023 Parts List

| Schematic Design | Description | PTS P/N |
|---|---|---|
| | **CAPACITORS** | |
| C1 | 6.8uF, El. Tant. 16V | 30-5101 |
| C2 | 6.8uF, El. Tant., 16V | 30-5101 |
| C3 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| C4 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| C5 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| C6 | 50nF, 80/20%, 50V, Z5V | 23-0503 |
| | **CONNECTORS** | |
| J1 | Connector strip, female, 20 cont. | 79-1004 |
| P1 | Header strip, 25 contacts | 79-1003 |
| | Header strip, 25 contacts | 79-1003 |
| | **RESISTORS** | |
| R1-R32 | 2.2KΩ, 5%, ¼W (32x) | 11-0222 |
| R33-R34 | 2.2Ω, 5%, ¼W (2x) | 11-1220 |
| R35 | 1.21KΩ, 1% | 14-5110 |
| R36 | 1.21KΩ, 1% | 14-5110 |
| R37 | 1KΩ, 10%, .75W | 17-5104 |
| R38 | 100KΩ, 5%, ¼W | 11-0104 |
| R39 | 4.7KΩ, 5%, ¼W | 11-0472 |
| R40 | 2.2KΩ, 5%, ¼W | 11-0222 |
| R41 | 1.3KΩ, 1% | 14-5111 |
| R42 | 866Ω, 1% | 14-5109 |
| R43 | 634Ω, 1% | 14-5108 |
| R44 | 470Ω, 5% | 11-0471 |
| R45 | 365Ω, 1% | 14-5107 |
| R46 | 301Ω, 1% | 14-5106 |
| R47 | 243Ω, 1% | 14-5105 |
| R48 | 2.2KΩ, 5%, ¼W | 11-0222 |
| R49 | 2.2KΩ, 5%, ¼W | 11-0222 |
| R50 | 2.2KΩ, 5%, ¼W | 11-0222 |
| R51 | 2.2KΩ, 5%, ¼W | 11-0222 |
| R52-R54 | 2.2KΩ, 5%, ¼W | 11-0222 |
| R55 | 680Ω, 5%, ¼W | 11-0681 |
| R56 | 4.7Ω, 5%, ¼W | 11-1470 |

## SER-1023 Parts List (continued)

| Schematic Design | Description | PTS P/N |
|---|---|---|
| | **INTEGRATED CIRCUITS** | |
| U1 | 74LS74 | 63-0074 |
| U2 | 74LS175 | 63-0175 |
| U3 | 74LS175 | 63-0175 |
| U4 | 74LS273 | 63-0273 |
| U5 | 74LS74 | 63-0074 |
| U6 | 74LS174 | 63-0174 |
| U7 | 74LS173 | 63-0173 |
| U8 | 74LS145 | 63-0145 |
| U9 | 74LS173 | 63-0173 |
| U10 | 74LS173 | 63-0173 |
| U11 | 74LS164 | 63-0164 |
| U12 | 74LS173 | 63-0173 |
| U13 | 74LS174 | 63-0174 |
| U14 | 74LS164 | 63-0164 |
| U15 | 74LS173 | 63-0173 |
| U16A (160 MHz) | 74184 | 60-0184 |
| or | | |
| U16B (250 MHz) | 74LS173 | 63-0173 |
| U17 | 74LS173 | 63-0173 |
| U18 | 74LS173 | 63-0173 |
| U19 | 74LS164 | 63-0164 |
| U20 | 74LS173 | 63-0173 |
| U21 | 74LS173 | 63-0173 |
| U22 | 74LS164 | 63-0164 |
| U23 | 74LS173 | 63-0173 |
| U24 | 74LS173 | 63-0173 |



TO SER (1023) P1
GPIB (488) CONNECTOR J1
"ADDRESS DECODE"
"UNLISTEN DECODE"
"ACCEPTOR HANDSHAKE"
"GTL DECODE"
"LF DECODE"
"NUMERALS DECODE"
"A & F" DECODE
CLOCK GATING
REMOTE/LOCAL FF
"LISTEN FF"
"ADDRESSED"
"LISTEN ONLY"
S1 THRU S5 (OFF) OPEN = 1 (ON) CLOSED = Ø
LOW ENABLES OUTPUT (HIGH OFF (HIGHZ))
VCC RAIL
LISTEN CR1
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
IFC
ATN
SRQ
REN
EOI
NRFD
NDAC
DAV
SHIELD
SIG GND
FCK
ACK
TRA
ARES
FRES
FPE
REL
OC
LOC
+5.4V
GND
LIL
NOTE:
= OPEN COLLECTOR DEVICE
IC'S GND +B
ALL 14 DIP 7 14
ALL 16 DIP 8 16


Figure 1

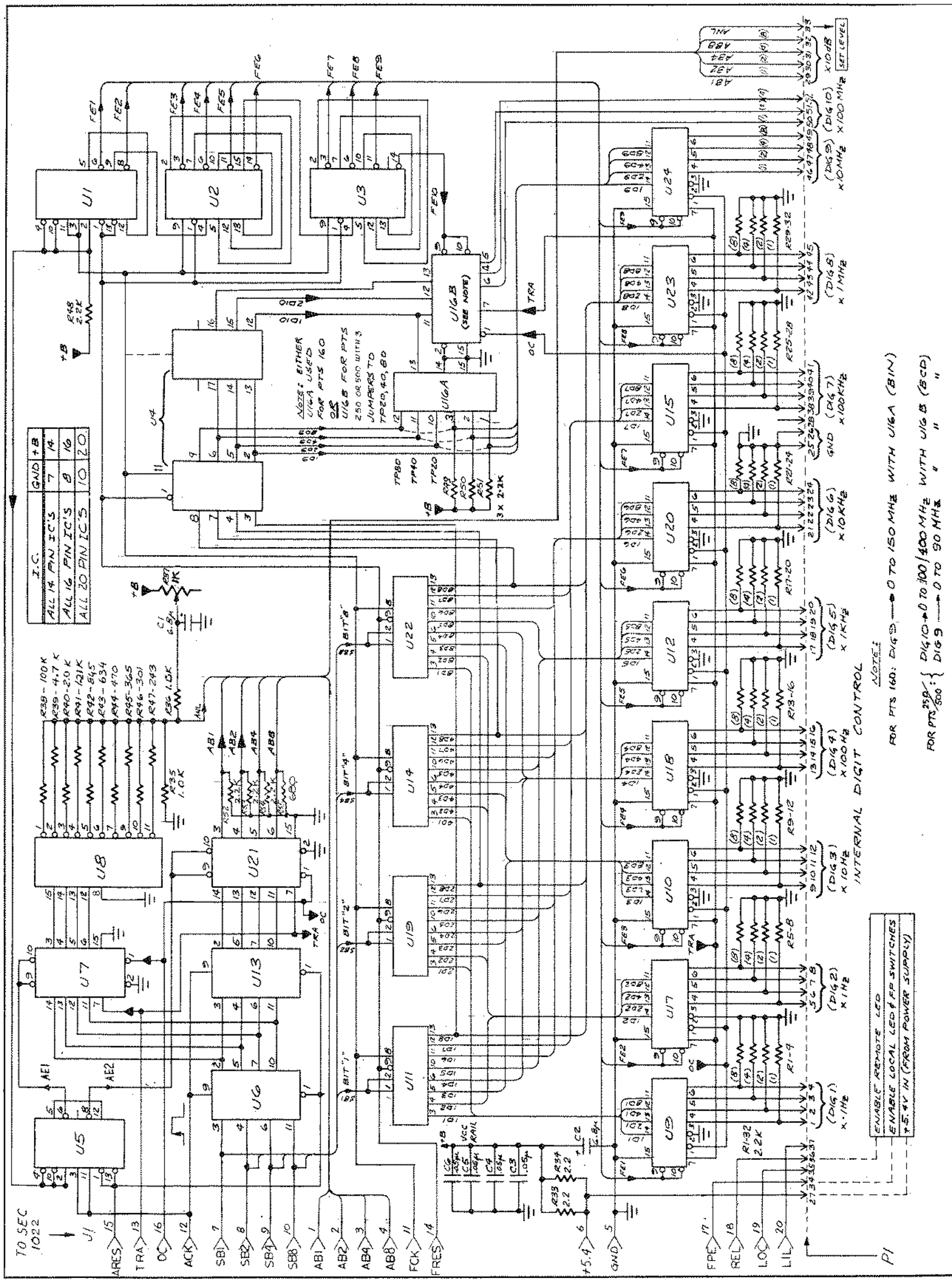

TO SEC 1022
J1
ARES
TRA
OC
ACK
SB1
SB2
SB4
SB8
AB1
AB2
AB4
AB8
FCK
FRES
+5.4
GND
FPE
REL
LOC
LIL
P1
INTERNAL DIGIT CONTROL
The Draftboard, Inc.

Figure 2

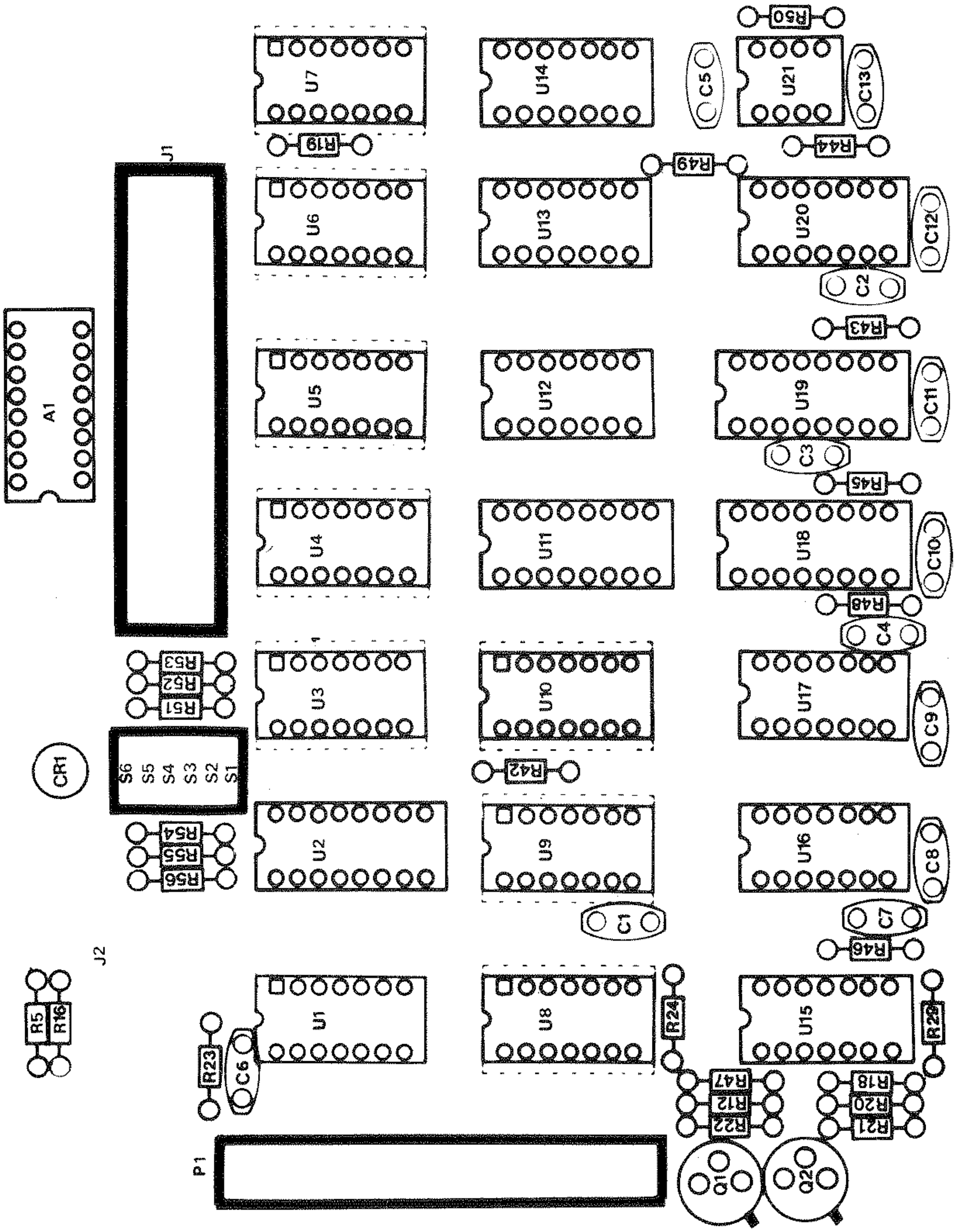
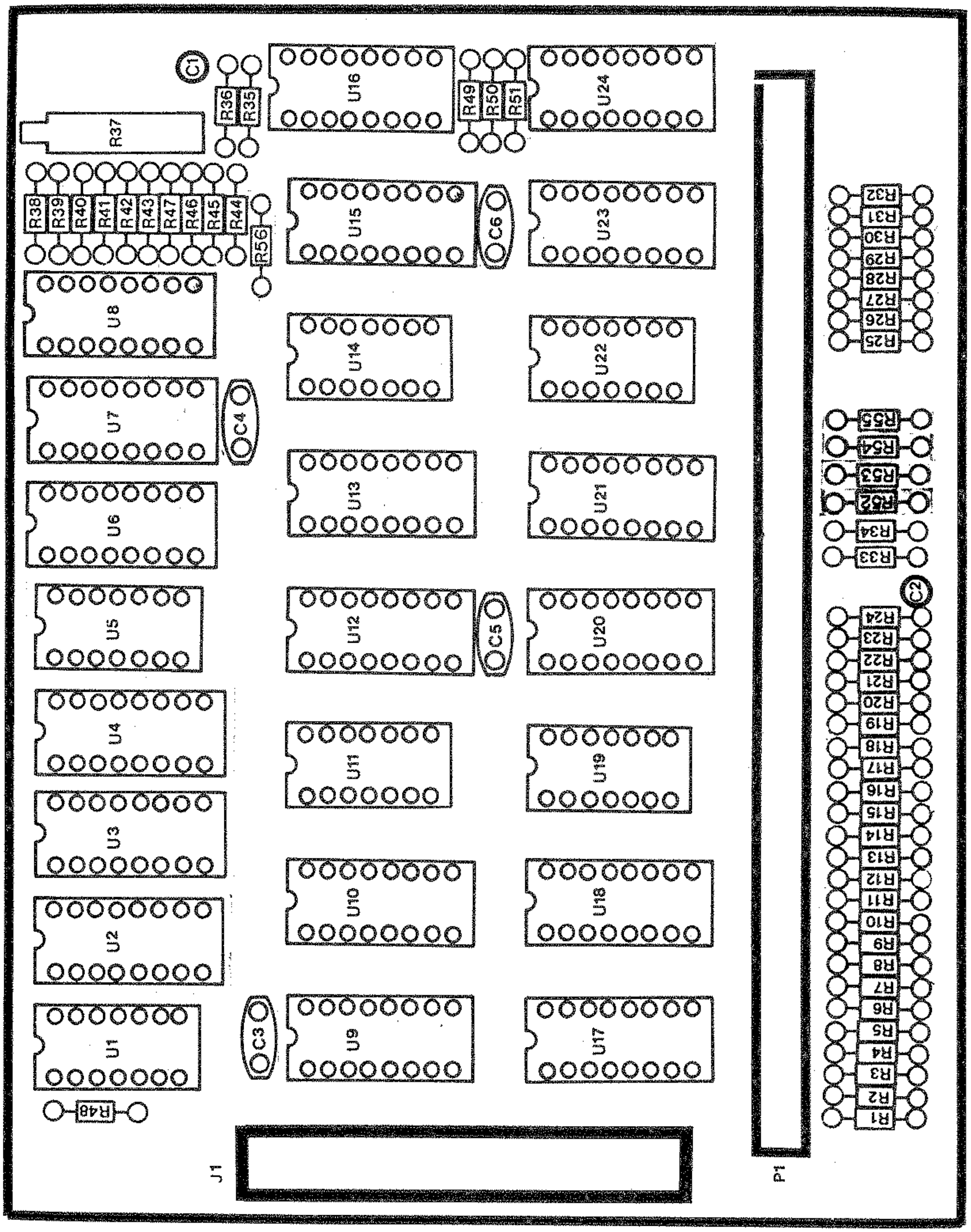

J1
J2
P1
A1
CR1
S6 S5 S4 S3 S2 S1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
Q1
Q2
R5
R16
R12
R18
R19
R20
R21
R22
R23
R24
R42
R43
R44
R45
R46
R47
R48
R49
R50
R51
R52
R53
R54
R55
R56

Figure 3

a



C1
R36
R35
R37
U16
R49
R50
R51
U24
R38
R39
R40
R41
R42
R43
R47
R46
R45
R44
R56
U15
C6
U23
R32
R31
R30
R29
R28
R27
R26
R25
U8
U14
U22
U7
C4
U13
U21
R55
R54
R53
R52
R34
R33
U6
U5
U12
C5
U20
C2
R24
R23
R22
R21
R20
R19
R18
R17
R16
R15
R14
R13
R12
R11
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
U4
U11
U19
U3
U10
U18
U2
U1
C3
U9
U17
R48
J1
P1


Figure 4

a