KINEMETRICS

TRUE TIME INSTRUMENTS

OPERATING AND SERVICE MANUAL

Model 468-DC

Satellite Synchronized Clock

TRUE TIME DIVISION, 3243 SANTA ROSA AVE., SANTA ROSA, CA 95401, PHONE (707) 528-1230

SECTION I

GENERAL INFORMATION

1-1 INTRODUCTION

1-2 This manual has been designed and written to provide the owner of the Model 468-DC "GOES" Satellite Synchronized Clock with all the data and information needed to operate and utilize all its features.

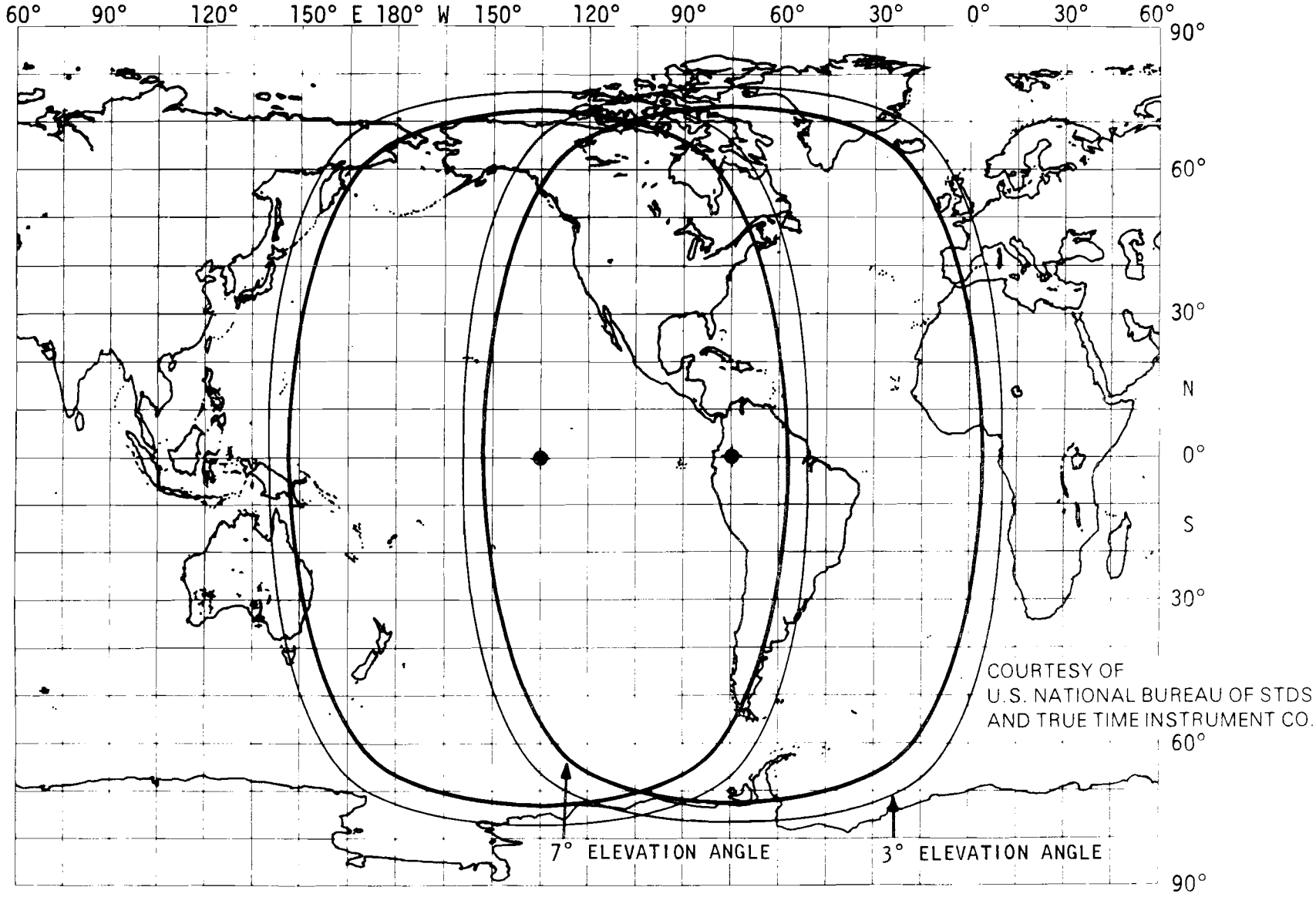
1-3 The information included in this manual is as complete as possible and includes normal maintenance and adjustment data that may be required to facilitate field repair of the unit.

1-4 The Model 468-DC has been designed to receive the NOAA "GOES" Satellite which transmits on a frequency of 468 MHz and decode the time information from the broadcasts as well as display outputs for supplying the time information to other equipment. The Synchronized Clock in its standard configuration provides a front panel display of days, hours, minutes, and seconds with five rear panel BNC connectors with IRIG B, 1Hz, 1 kHz, Precision 60 Hz, and Slow Code locked to the electrically outputted time (and options if ordered), may be in either Universal Coordinated Time (UTC), more commonly referred to as Greenwich Mean Time (GMT), or in local time. This is done through the proper time zone offset selected by the rear panel thumbwheel switches. The Model 468-DC is shipped to display the time of year in the twenty-four hour format. By simply removing the cover and switching the position of the small switch on the microprocessor circuit board, the unit can be converted to display and output time in the more conventional twelve hour format.

1-5 This instrument has been designed to be completely automatic requiring only antenna installation and connection of the unit to the power source. Once the instrument is installed and turned on, the microprocessor will lock to the signal from the "GOES" Satellite (either East or West Satellite by sweeping for lock), decode and display the time. From that point on, the unit will require no further attention and will provide time to an accuracy of ± 1.0 ms, continually updated by and phase locked to the transmissions of the "GOES" Satellite. In the event of loss of signal, the unit will continue operation on its internal crystal time base. If power should fail, upon restoration, the unit will again read the time signals and start displaying the time transmitted.

1-6 The Model 468-DC Synchronized Digital Clock is guaranteed to operate at any location within the 7^{o} viewing angle of the satellite as shown on the map enclosed.

GOES SATELLITE LOCATIONS AS OF JUNE 1st, 1980



There are three GOES satellites in orbit, two in operation and the third serving as an in-orbit spare. The two operational units are located as shown above and covering the areas indicated.

1-7 WARRANTY

TRUE TIME INSTRUMENTS warrants each instrument it manufactures to be free from defects in its material and workmanship for a period of two years from the date of delivery. Under this warranty any instrument which is returned to us (freight pre-paid) and is found by us to be defective in material or workmanship will be repaired or replace (at our option) and returned at no charge to the customer.

Our obligation under this warranty is limited to servicing or adjustment of any instrument returned. Items not covered by this warranty are: fuses, batteries, and any illuminated parts or damage caused by accident or physical destruction of the instrument.

This warranty is expressly in lieu of all other obligations or liabilities on the part of TRUE TIME INSTRUMENTS. TRUE TIME INSTRUMENTS neither assumes nor authorizes any other person to assume for them any other liability in connection with our sales.

This warranty is applicable in the United States and Canada only. For other areas, consult "KINEMETRICS, INC."

1-8 SPECIFICATIONS

RECEIVER FREQUENCY:	468.8250 and 468.8375 MHz Automatic or Manual select.
SYSTEM SENSITIVITY:	The sensitivity is suitable for proper operation with satellite viewing angle 7^{o} or more above the horizon. When using the A-468MS Antenna. (~.2μV/m)
SYSTEM NOISE MARGIN:	Operates with 9db attenuator inserted between A-468MS flat plate and preamp input in locations which have a Satellite elevation of greater than 15^{o}.
TIMING ACCURACY:	1) ±1.5 ms of UTC/NBS Time when corrected for propagation delay through on board switches and using the A-468MS Antenna. 2) The time difference between neighboring clocks locked to the same satellite is considerably improved over UTC timing accuracy. Consult the factory for specification and conditions.
PROPAGATION DELAY CORRECTION:	Two internal decade switches provide ±50 ms correction capability in 1 ms steps.
TIME BASE STABILITY:	When not phase locked, crystal controls to $\pm 6 \times 10^{-6}$. For higher stability time base when not phase locked to satellite, see "External Oscillator Input" Option.
DISPLAY:	½" high planar gas discharge. Displays day of year, hours, minutes and seconds.
DISPLAY ACCURACY:	-0 to +100 ms, anytime colons are not flashing.
NOMINAL TURN-ON TIME:	Three minutes from power on and signal reception with 90% confidence under average signal conditions.
OPERATING TEMP:	0^{o} to 50^{o} C.

REAR PANEL OUTPUTS:

1Hz: Rising edge on time, drives ten TTL loads or CMOS. High 10%, Low 90%. See Section 3-24.

1kHz Rising edge on time, drives two TTL loads or CMOS. High 10%, Low 90%. See Section 3-26.

REMOTE DISPLAY DRIVING (IRIG B): IRIG B Time Code is provided on a rear panel BNC connector. Standard IRIG B Time Code is an amplitude modulated 1kHz carrier. This output can also be easily field converted to TTL compatable D.C. level shift time code. See Section 3-28.

SLOW CODE: BNC output of 1 pulse per minute (1ppm), 1 pulse per hour (1pph), and 1 pulse per day (1ppd). The pulses go high on time and remain high for 2 seconds for minute mark, 4 seconds for hour mark and 6 seconds for day mark. Capable of sourcing 40 MA at 4.0 volts minimum, and pulled to ground by a 1k Ω resistor. See Section 3-36.

60 HZ: Provided on BNC connector as frequency source to drive a synchronous motor through a power amplifier. Capable of sourcing 100μa @ 2.4V and sinking 1.6 MA @ .4V. (TTL Load). The output square wave has an unusual duty cycle. The 60 Hz is a 50% duty cycle over 50 ms (3 cycles).

Cycle #1	High 9ms, Low 8ms
Cycle #2	High 8ms, Low 9ms
Cycle #3	High 8ms, Low 8ms

See Section 3-41.

EXTERNAL OSCILLATOR (*OPT.*): Input level of less than 4V and greater than 2.4 volts (TTL) sine wave or square wave is required. Any frequency from 100 kHz to 10mHz in multiples of 100kHz is satisfactory. No unit adjustment is needed regardless of frequency. Used as clock timebase when not phase locked to the satellite. See Section 3-45.

IRIG H (*OPTION*): BNC output of standard IRIG H format TTL DC level shift supplied unless otherwise requested. If 1kHz amplitude modulated carrier requested, IRIG B will automatically be supplied in D.C. Level Shift format. See Section 3-52.

PARALLEL BCD TIME (*OPTION*): If ordered, Parallel BCD time of year is provided on rear panel 50 pin "D" connector. Days, hours, minutes, seconds and milliseconds are provided. Lines indicating worst-case time error of +1, +5, ±50 and +500ms drives 2 standard "TTL" loads or "CMOS". See Section 3-56.

RS-232 (*OPTION*): The displayed time of year is outputted in EIA Standard RS-232C configuration via a "Motorola ACIA". Output format is D D D H H M M S S and an indicator of the time quality, CR/LF. Baud Rate and "ACIA" options are dip switch selectable. See Section 3-67.

IEEE-488 (*OPTION*): IEEE Buss interface is also available. The time is outputted in ASCII format, with the most significant digit first (100's of days). Among operating modes is time on demand to the millisecond level, or marked time to the milliseconds level. See Section 3-99.

HOURS OFFSET: Rear panel thumbwheel switch allows adjustment of + or - "0" to "11" hours from transmitted UTC time.

12/24-HR. OPERATION: Dip Switch located inside unit allows use as 12 hour clock in place of 24 hour format as shipped.

468-DC SYNCHRONIZED DIGITAL CLOCK

SIZE: 1-3/4" x 17" x 10½" (4.4 x 43.2 x 26.7cm) behind panel. Mounts in standard 19" (48.9cm) EIA rack system, hardware included. 24" (60.9) hardware available.

WEIGHT: 7¼ lbs. (3.5kg) Ship Wt. 12 lbs. (5.4kg).

POWER: 95-135VAC, 60-400Hz, less than 25 volt amps. Others available on request.

A-468MS ANTENNA

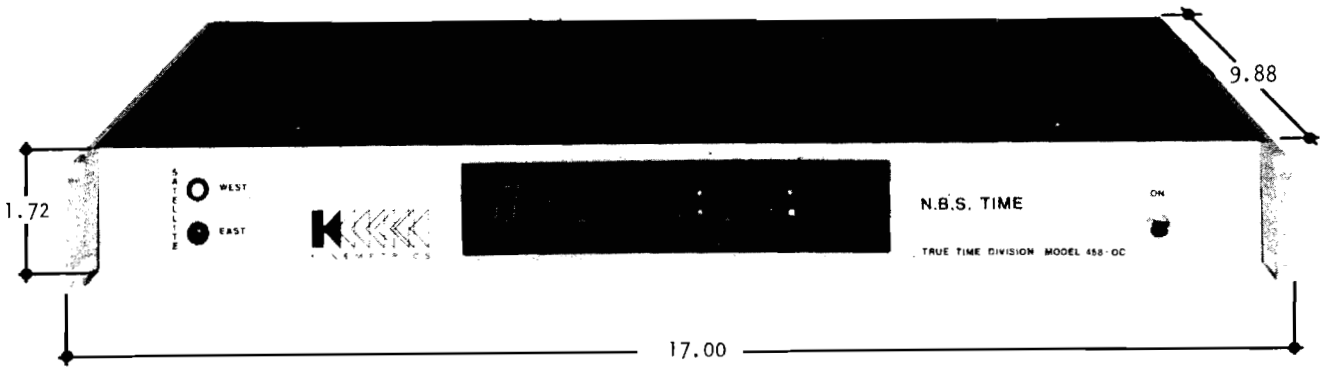
SIZE: 12" x 12" x 7½" high (30.5cm x 30.5cm x 19.5cm) provided with universal mounting and hardware.

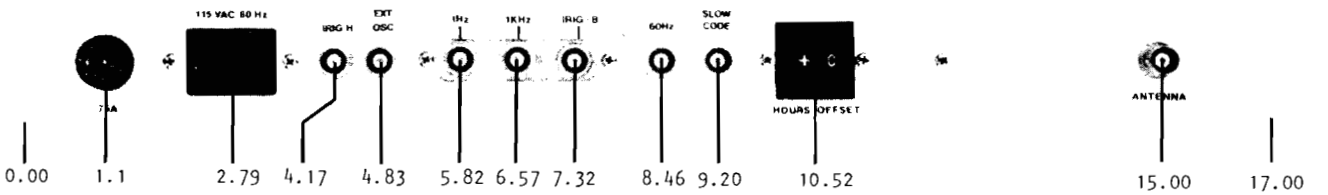
WEIGHT: 9-3/4 lbs. (4.4kg) Ship Wt. 13 lbs. (5.9kg).

A-468HX ANTENNA

SIZE: 12" x 12" x 3'6" high (30.5cm x 30.5cm x 196.6cm) provided with a universal mounting system and hardware.

WEIGHT: 14½ lbs. (6.5kg) Ship Wt. 19 lbs. (8.6kg).





SECTION II

INSTALLATION

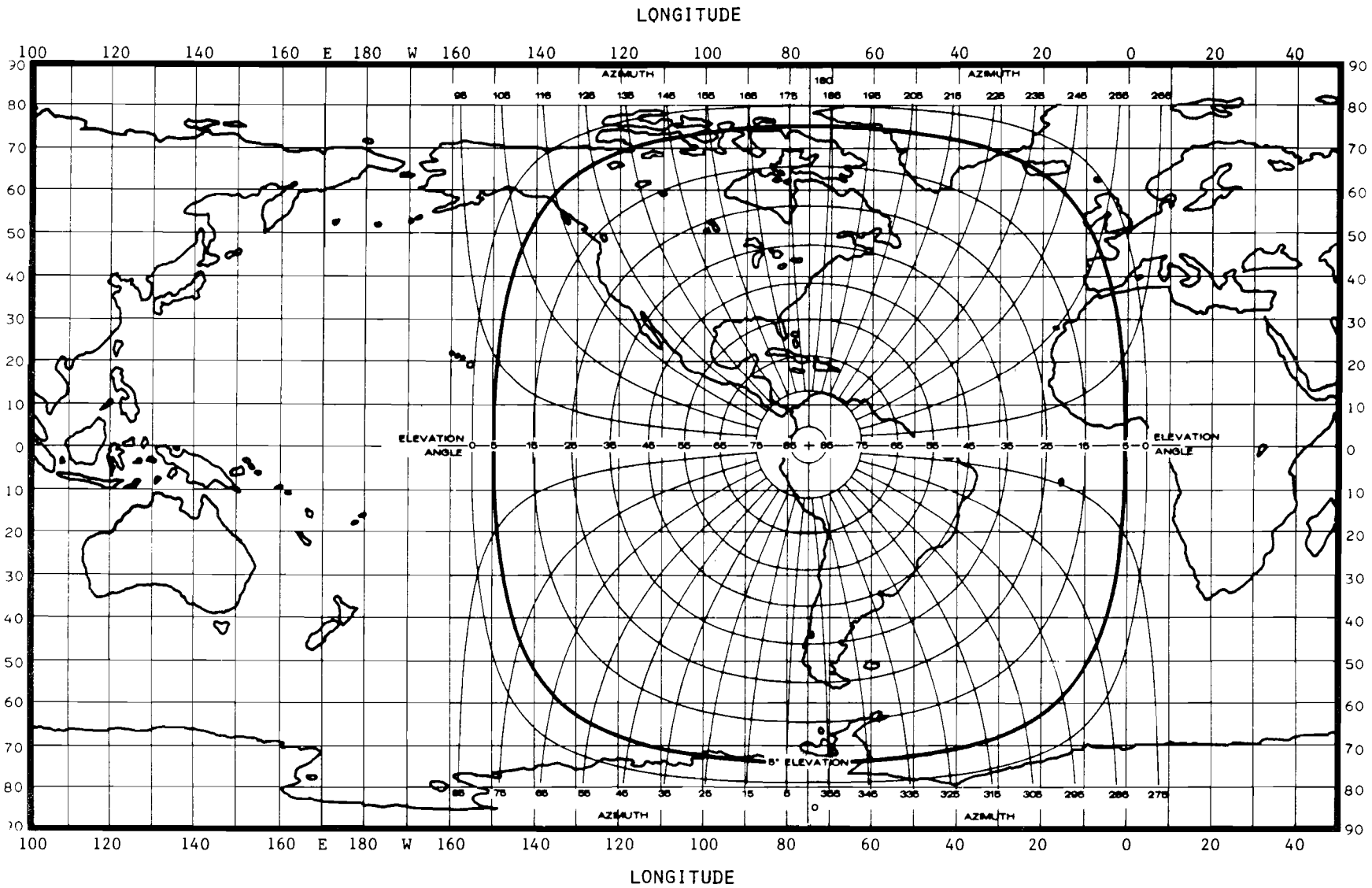
2-1 ANTENNA INSTALLATION

2-2 The Model 468-DC Synchronized Clock is shipped ready for operation and will require no adjustments. The first step in set-up and operation of the unit is to install the antenna included with the unit. An antenna supplied by True Time for use with the Model 468-DC must be used in conjunction with this receiver/clock as the antenna includes not only a preamp, but receiver controlled frequency conversion circuits. The use of "in antenna conversion" of the 468 MHz frequency to a lower frequency for transmission down the coax allows up to 1000 feet of RG-58/U lead in coax to be used.

2-3 Since the Model 468-DC can be used to automatically switch from one satellite to the other (EAST or WEST) the user must first determine if the unit is to be allowed to automatically select either satellite or to be locked to either the East or the West satellite. If the propagation delay must be calculated and preset on the internal switches to obtain the ultimate unit accuracy with respect to another 468-DC in the field or with respect to the transmitted time, it will be required to lock the clock onto one satellite. If only basic time is required and a change in received satellite which might result in a worst case error in propagation delay of 9 ms. is acceptable, the advantage of automatic scanning of the satellites can be maintained. This scanning allows the receiver to select either receivable satellite in the case of poor or no reception from one. A second consideration is if the user is within the reception range of one or both satellites, and if a common pointing direction will be suitable for reception of both satellites. This can be evaluated by the use of the pointing angle maps, figure 2-1 and 2-2. The beamwidth of the A-468MS antenna is approximately 90^{o}.

2-4 Once it is determined which satellite will be received (or if both are to be received) the attached maps can be used to determine the besting pointing direction for the users location. In the case of the A-468MS, the antenna should be physically pointed such that the signal from the satellite comes onto the antenna receiving plate through the top of the plastic bubble. The axis of the A-468HX, the Helix should be pointed at the satellite for best results. Thus, if the user was directly under the satellite, the antenna would be set with it facing straight up. If the satellite was at a 7^{o} angle above the horizon, the antenna must be tipped at 83^{o}.

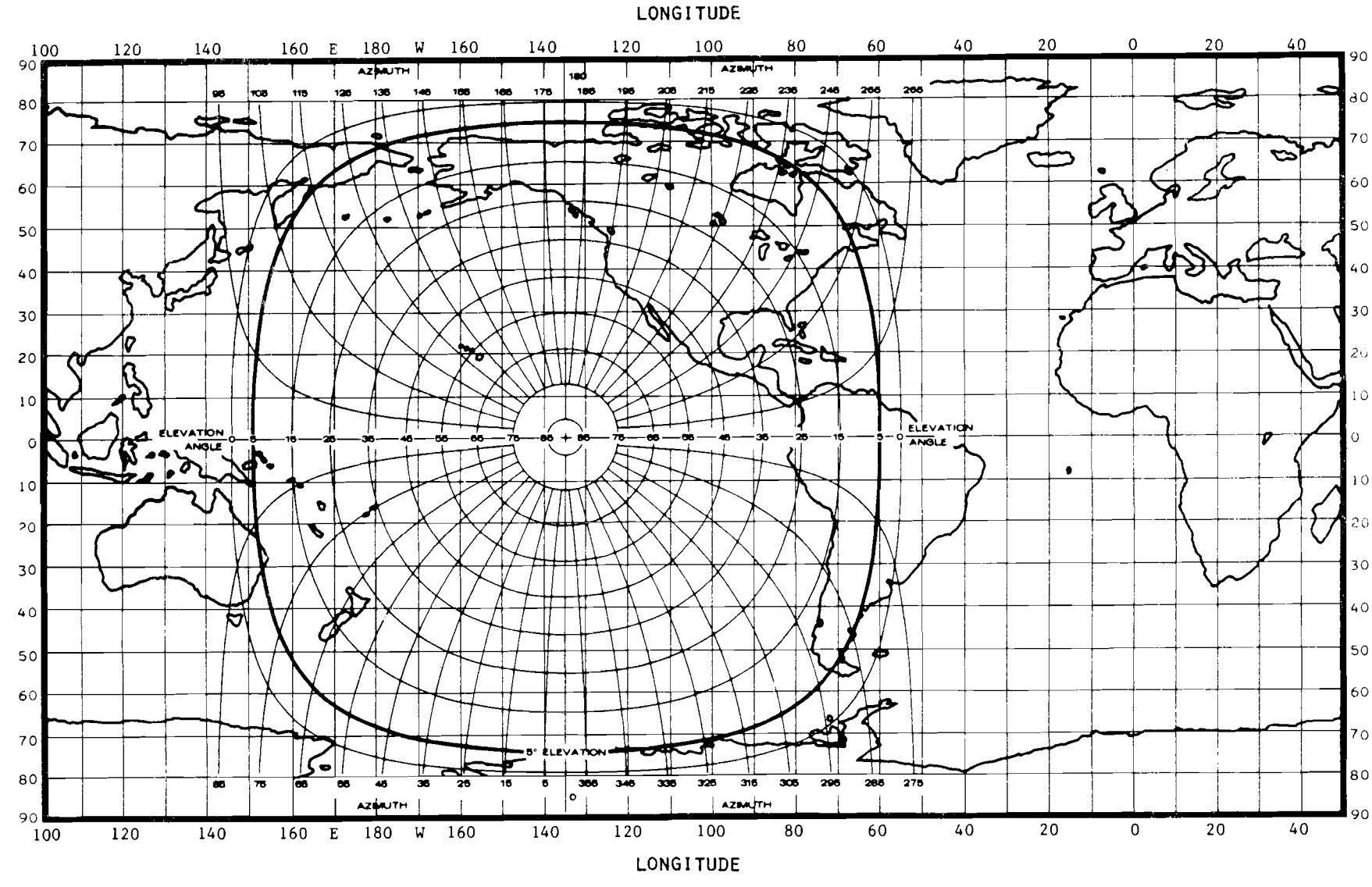
2-5 Included with the antenna is a mounting flange with a shaft attached to allow versatile tipping as well as rotation for proper antenna pointing. The stand also allows attachment of this antenna to a flat surface for mounting. See SECTION VI.



EASTERN SATELLITE POINTING ANGLES.

FIGURE 2-1

EASTERN SATELLITE POINTING ANGLES.



WESTERN SATELLITE POINTING ANGLES.

FIGURE 2-2

WESTERN SATELLITE POINTING ANGLES.

2-6 Once the mounting and pointing of the antenna is complete, attach a lead in coax. For this purpose RG-58/U is available from True Time at 50' and 100' lengths.

2-7 RACK MOUNTING

2-8 If it is desired to mount the Model 468-DC in a standard 19" rack system, use the rack mounting ears provided with the unit. These ears may be attached to the side of the cabinet by removing the two 8-32 flat head screws on the side of the instrument and placing the screws through the counter-sunk hole in the bracket and re-installing the screw. The unit now may be mounted in a 1-3/4" opening in any EIA Standard 19" rack system.

2-9 INSTRUMENT START-UP

2-10 After the antenna installation is complete, as described in SECTION 2-2 above, the lead-in coax should be connected to the rear panel BNC connector labeled "ANTENNA". Connect the power cord to the socket on the rear panel and plug the unit into an appropriate power source. The power switch on the front panel may now be turned on.

2-11 When the power is turned on, the initial indication of proper operation of the Model 468-DC is the colons on the display. The colons will blink off and on at about once per second. This indicates to the user that the unit is operating properly and that the receiver is looking for phase lock to the carrier of the signal and then to the 100 Hz data rate of the information broadcast. Next, after the 468-DC has read and recognized the maximum length sequence (MLS) transmitted each ½ second, the colons will be locked on solid.

2-12 Following this data lock, the synchronized clock will recognize that it is reading data, a satellite location (as transmitted in the message) will be read. From this information, the 468-DC can determine if it is locked to the "EAST" or "WEST" Satellite and light the appropriate "LED" on the front panel.

2-13 Finally, after two 30 second long time frames of information of the time of year have been read which agree as to the time, the front panel display will light indicating the correct time of year. At this same time, any options which have been ordered to electrically output the time will begin to function.

2-14 One of the most often overlooked and yet most important factors in the installation and operation of the Model 468-DC is proper antenna installation. Without a proper antenna installation, the signal from the satellite will not be received and thus the unit cannot possible function properly. In many cases "just to try it out", an attempt will be made to operate the unit without determining the proper antenna pointing or inside of the building. This, as often as not, results in inability to lock to the satellite signal, and failure to decode the time.

SECTION III

OPERATION

3-1 INTRODUCTION

3-2 The Model 468-DC Synchronized Clock provides the user with a means of obtaining time traceable to the U.S. National Bureau of Standards with an accuracy of +1.5 ms. For stability, the time base is phase-locked to the satellite data rate. The time of year information broadcast by the National Oceanic and Atmospheric Administration through the "GOES" Satellite is displayed in days, hours, minutes and seconds on the front panel. Also available are outputs of this time information in the form of Remote Display Driving Output (IRIG B, Parallel BCD Time, or RS-232C compatable interface, or IEEE-488 compatability). The Model 468-DC has been specifically designed to minimize operator set-up and will provide many years of service without attention.

3-3 SATELLITE EAST-WEST LED

3-4 Located on the lower left hand corner of the front panel are two LED's labeled "Satellite", "WEST" or "EAST". These green LEDs will light any time the unit is receiving a sufficient signal from one of the satellites to allow the internal time base to phase lock to the data frequency of 100Hz. When the unit is initially turned on, if adequate signal is present, this LED will light within 30 to 45 seconds. If during the course of operation phase lock with the satellite is lost long enough for the R.F. Circuits to sweep for phase lock, (about 150 seconds), this light will go out. When phase lock is regained and a satellite position is recognized in the data, the appropriate LED will again light.

3-5 Phase lock will be maintained continually in most areas and the only occasion for loss of lock will be experienced due to local noise interference. The most common source is "land mobile" transmitters on a frequency of 468.8250 MHz which is directly on the Western Satellite frequency.

3-6 The Satellite LED also provides information as to the Satellite position. If the 468-DC is able to read the time of year information but the satellite position information read in code does not agree with the position shown on the propagation determination maps, (Figure 3-2 and 3-3), the LED will blink. If the R.F. carrier on which the time data was found is on the 468.8250 MHz frequency, the West LED will blink, if on 468.8375 MHz, the East Led will blink. This indicates to the user which Satellite is being received, but that paopagation delay information may be incorrect and exact satellite position should be determined if accuracies to the millisecond level are desired. Satellite LED blinking also occur when the unit is in "Automatic" satellite selection, the 468 DC has swept to the other satellite, but complete time synchronization is not complete. This usually requires less than 15 minutes to accomplish and then clears the blinking.

3-7 DISPLAY

3-8 The front panel display of time is blanked when the unit is initially turned on, because the correct time is not known. The time information broadcast by the "GOES" Satellite is repeated every 30 seconds. The time information is broadcast in the first 11 seconds of each ½ minute. Requirements for the display to light are: 1) the unit must obtain phase lock with the carrier of satellite, 2) phase lock with the 100Hz data rate must be obtained, and 3) two consecutive frames of time code must be read which agree as to the time. When these 3 criteria are met, the display will light showing the correct time in days, hours, minutes and seconds, Universal Coordinated time (UTC) more commonly referred to as Greenwich Mean time (GMT). Correction to local time, conversion to a 12-hour clock in place of the 24-hour time base as transmitted and correction for propagation delay are covered in the following sections.

3-9 The display has been designed to indicate to the user the accuracy of the time information being displayed and on the time output lines if ordered. After the display turns on, it will indicate the worst case accumulated drift of the time information should phase lock with the satellite be lost. When the unit has accumulated loss of lock for 2½ hours since the last synchronization to ±5ms., the colons will flash. The flashing colons indicate that the estimate of the worst-case error of the display and outputted time is ±50ms. of N.B.S. time. When the unit has been in operation for fifteen hours without phase lock since the last synchronization, the complete display will flash. This flashing is certain to attract the operators attention and indicates that the time as displayed and outputted may have a worst case error of more than ±500 ms. (½ seconds).

3-10 Display or colon flashing will stop when the signal from the satellite is regained, phase locked to and the time code is read. Under normal operation, this will occur without operator attention. It is very unlikely that either of these conditions will occur under normal conditions. Due to the ability of the unit to phase lock to the carrier frequency down to very low signal levels, persistant flashing of the colons or display may be an indication of poor reception due to local interference or antenna location and/or installation. Refer to SECTION V "Maintenance and Troubleshooting" for additional information on this subject.

3-11 HOURS OFFSET

3-12 Located on the rear panel is a thumbwheel switch labeled "HOURS OFFSET". This switch is set for "0" at the factory which means that the displayed time will be Coordinated Universal Time as broadcast. To change the hours on the display to read local time, set the switch to the number of hours your location is offset from Greenwich, England. For example, if you are located in the Eastern Time Zone and desire to display Local Standard Time, the switch should be set for "-5", or for

Daylight Savings Time set for "-4". If, in this case, the display was indicating 1800 UTC, the clock would subtract 5 hours and display 1300 hours for Local Standard Time. If the unit has electrically outputted time, (IRIG B, Parallel BCD, RS-232 or IEEE-488) the time supplied on these outputs will agree with the display. Additonal information on these outputs is included in the following sections.

3-13 12/24-HOUR CLOCK OPERATION

3-14 The Model 468-DC is shipped from the factory for operation on the 24-hour clock system as broadcast by the National Bureau of Standards. If it is desired to convert the clock to a 12-hour clock display, a small internal switch can be turned.

3-15 To convert a clock to the 12-hour format refer to Figure 3-1. Remove the four screws retaining the lid and slide the switch indicated in the photograph to the 12-hour position. Replace the cover and reinstall the screws.

3-16 AUTOMATIC/MANUAL SATELLITE SELECTION

3-17 As described in Section 2-3, the Model 468-DC can be used to automatically select the "EAST" or the "WEST" satellite, or can be set manually for lock to either satellite. The receiver, as shipped from the factory is set for "Automatic" scanning of the satellites. If it is desired to lock the receiver onto either satellite, remove the four screws retaining the lid. By referring to Figure 3-1, locate the "EAST" and "WEST" Satellite Switch. If it is desired to lock to the East Satellite, turn the "EAST" Switch "ON", if the "WEST" Satellite is desired, turn the "WEST" Switch to "ON". With both switches "OFF" the unit will be returned to automatic scanning operation.

3-18 PROPAGATION DELAY

3-19 This feature is included with the Model 468-DC to allow the microprocessor to compensate for the delay in the displayed and outputted time and timing marks due to the time required for the signal to travel to the receiver from the transmitter.

3-20 This feature consists of two switches on the Digital Board Assembly. To adjust these switches, first remove the four screws which hold the top cover in place, remove the lid and set it aside. Refer to Figure 3-1 for identification of the "Prop. Delay Switches". The two switches can be combined to provide for a total of 99 ms, propagation delay for the unit. The switch toward the rear panel provides 0 to 9 ms. and the switch toward the fron adds to this in steps of ten from 0 to 90 ms. Therefore, if it is desired to compensate for 59 ms. propagation delay, the front switch would be turned to 5 (for 50 ms) and the rear switch to 9 (for 9 ms).

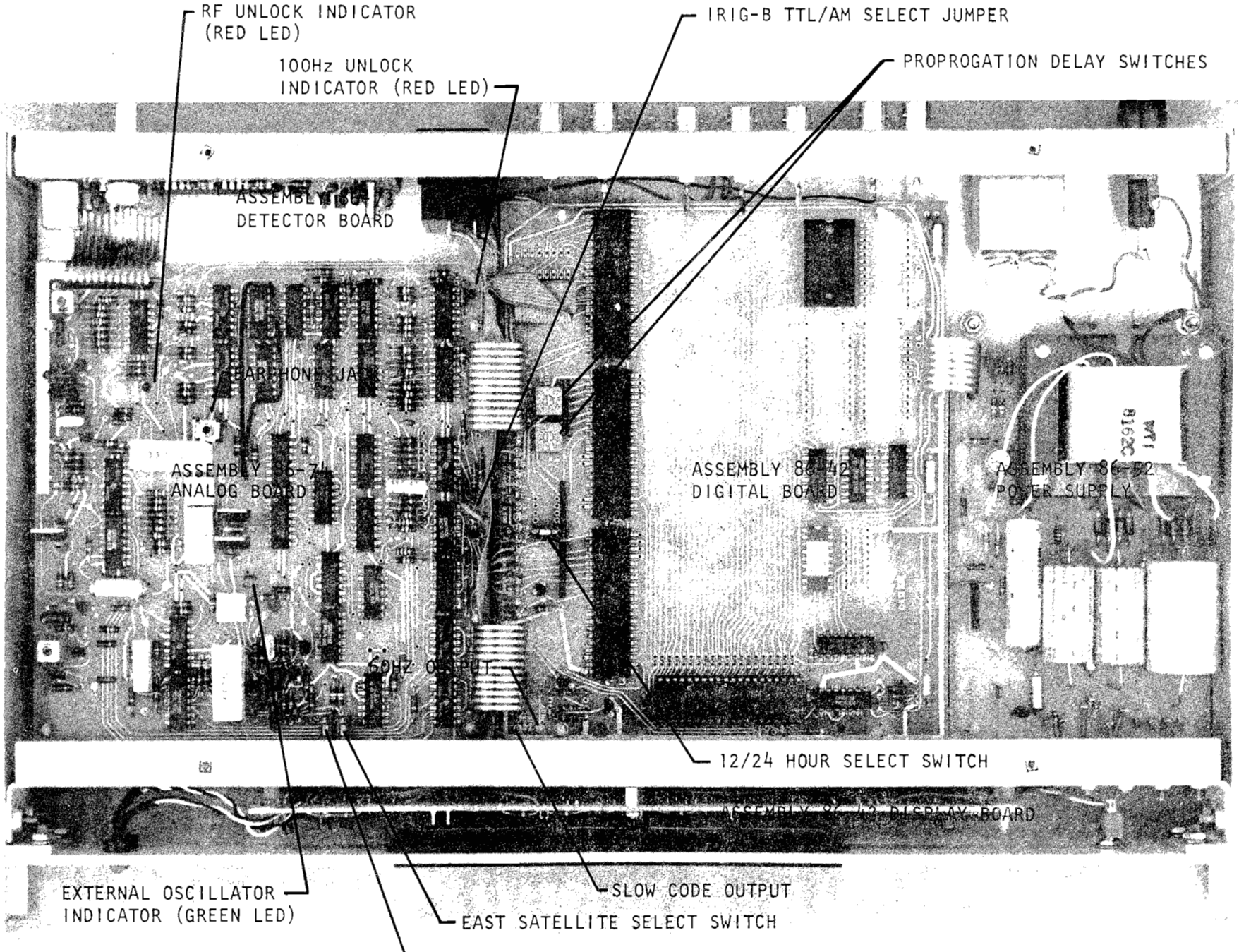


FIGURE 3-1

PARTS LOCATION - MODEL 468-DC

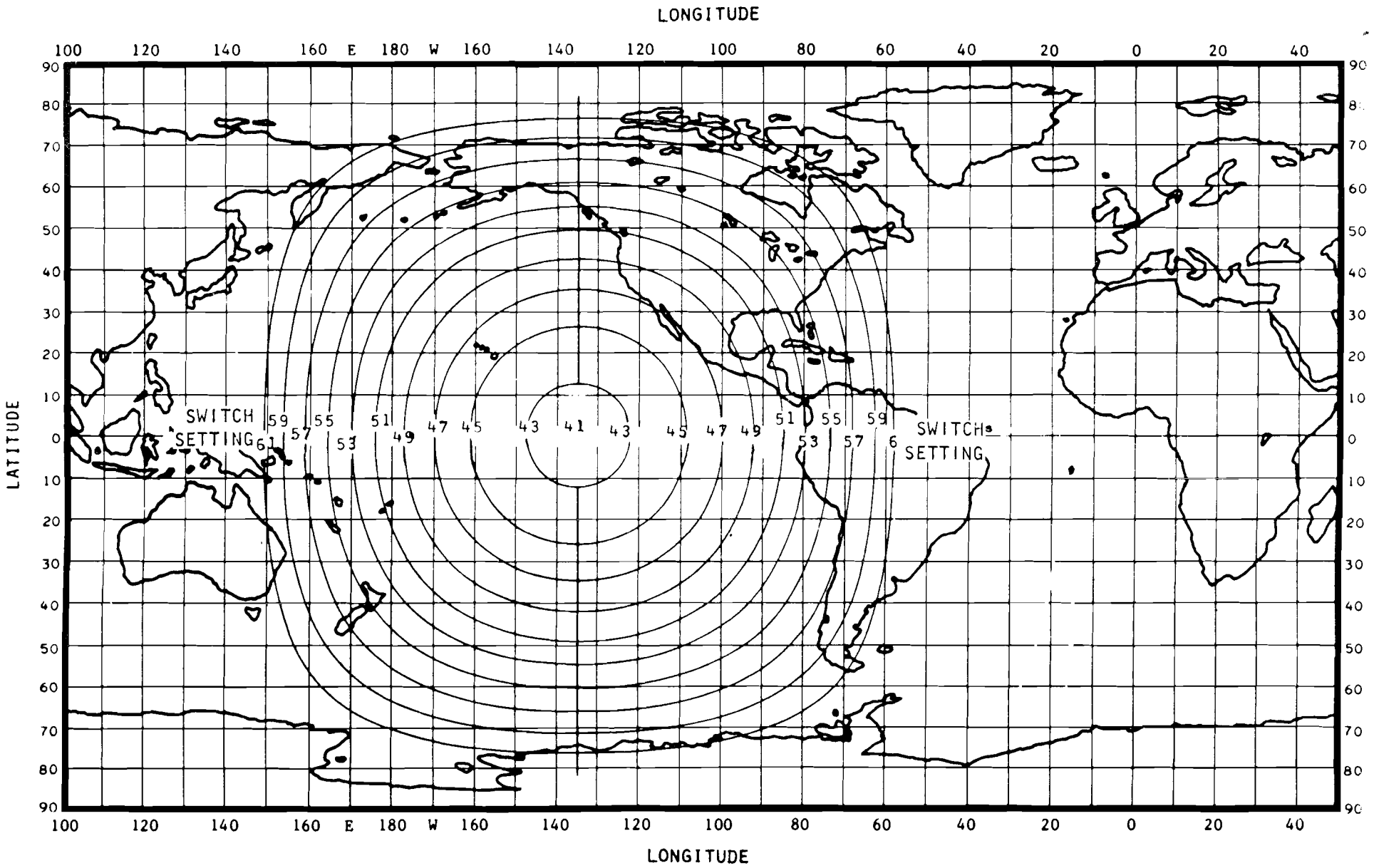


FIGURE 3-2

WESTERN SATELLITE MEAN DELAYS.

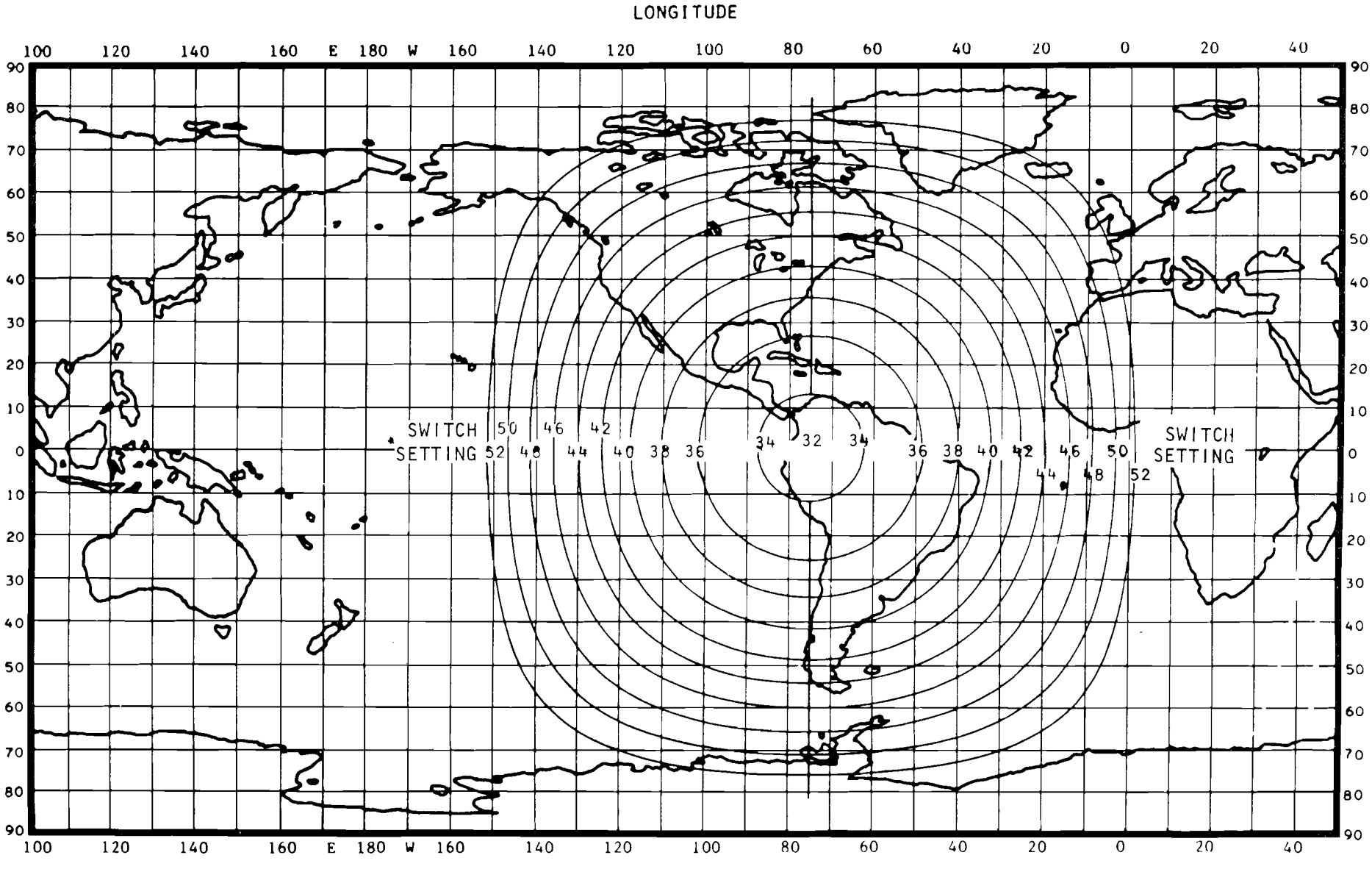


FIGURE 3-3

EASTERN SATELLITE MEAN DELAYS.

3-21 Through the ground station at Wallops Island, the National Bureau of Standards advances the time sent to the satellite by 260.000 ms. Propagation delay from Wallops Island to the Satellite and back to earth varies between 242.50 and 271.50 ms. depending on satellite position and the receiving location. This results in the receiver signal being advanced up to 17.50 ms. or retarded by 11.50 ms relative to UTC-NBS depending on receiver location and satellite being received.

3-22 This offset can be conpensated for by the propagation delay switches described above. A switch setting of 50 as shipped from the factory, sets the output time of the synchronized clock simultaneous with the received time of the signal. Increasing the propagation delay switch setting advances the output time relative to the received time by 1.0 ms per step. Thus, a switch setting of 62 advances the time output by 12 ms. as a setting of 32 on the switches retards the output time by 18 ms.

3-23 The appropriate setting of the propagation delay switches can be determined by the use of the attached maps, Figure 3-2 and 3-3. If the clock is locked to the "EAST" or "WEST" satellite as described in SECTION 3-16, the delay can be determined relatively accurately. If the unit is left on the "automatic" mode, the best compromise must be determined depending on the receiver location.

EXAMPLE:

1) A user located in the southern tip of Florida, USA and having his unit locked to the "EAST" satellite should set the switches to read 36 ms, "3" on the 10's of milliseconds switch and "6" on the units of millisecond switch.

2) If a unit is located at 120^{o} West longitude and 40^{o} north latitude and left in "automatic" mode, the switches should be set to read 46 or 47 milliseconds at the users option. This would be obtained by setting the 10's of milliseconds switch to "4" and the units switch to "6" or "7".

3-24 1 HZ

3-25 The 1 Hz is provided as a rear panel BNC connector and can be used for a wide variety of timing functions. This output is a pulse going high as the second remains high for 100 milliseconds and going low for the remaining 900 milliseconds. This output is driven from a 2N3904 (Q3) on the microprocessor board (Assy. 86-42, see SECTION V). The collector of Q3 is pulled up to +5VDC with a 3.3K Ω resistor. This output is taken off of pin #3 of assembly 86-42 and capable of driving 10 TTL loads.

3-26 1 KHZ

3-27 The 1kHz rear panel output is similar in form to the 1Hz above. It is a square wave going high on time, remaining high for 100 microseconds and low the remaining 900 microseconds. This output is driven by U23 on assembly 86-74 (See SECTION V) which is a CMOS part number 4050. This output is fed to assembly 86-42 in interconnecting wire(s) and to the rear panel from 86-42 pin number 17

3-28 IRIG B (REMOTE DISPLAY DRIVING OUTPUT)

3-29 The primary purpose of the IRIG B time code output is to drive slave displays manufactured by True Time Instruments. This output consists of the standard IRIG B time code. Refer to SECTION VII for a full description of this code.

3-30 When using this code for other than driving the True Time Model RD-B, it should be noted that four "Control Functions" are used. These control functions encode estimated time accuracy as fully described in SECTION VII

3-31 This output is supplied on a rear panel BNC connector. When shipped, this output is in a 1kHz carrier amplitude modulated format but can be field converted to D.C. level shift code format. In addition to driving remote displays, this output can be used to synchronize commercially available Time Code Generators or direct recording on magnetic tape.

3-32 The modulated 1 kHz format is a sine wave driven by two sections of a Texas Instrument part number "TL084" in series with 50Ω located on assembly 86-74. The high level of the code is 3.3 volt peak to peak $\pm$.5V, at the low level it is 1 Volt peak to peak $\pm$.2V. This output is then fed to assembly 86-42 via the jumber wire (pin number "P") and to the rear panel from terminal number 18.

3-33 If it is desired to convert the IRIG B Time Code from the amplitude modulated 1kHz form as shipped, to a level shift output, it is necessary to remove the lid and move one wire. To remove the lid, take out the four screws in the cover and set the lid aside. Locate the Analog Board, Assembly 86-74 which can be identified with the assistance of the photograph in Figure 3-1 of this manual.

3-34 After locating the Analog Board, Assembly 86-74, note on the right side of the board near the edge of a red jumper wire has been installed in two of three holes in a triangular shape pattern. the rear point to which the wire is soldered, labeled "AM", should be unsoldered ans swung forward and resoldered into the hold, labeled "TTL" toward the front of the instrument. This connects the lead from the 2N3904 transistor near this hole to pin "P" of the edge connector. Replace the lid and the IRIG B output will now be in level shift format.

3-35 The Level Shift format is driven by Q100 (2N3904) on assembly 86-74 with 2.2K Ω pull up to +5VDC. This will drive about 10 TTL loads. After leaving Q100, the IRIG B is transferred to assembly 86-42 on jumper wire pin "P" and to the rear panel connector via pin 18 on this assembly.

3-36 SLOW CODE

3-37 The "Slow Code" output from the Model 468-DC has been provided primarily for the purpose of providing timing marks on drum recorders such as the Kinemetrics Inc. Model VR-1. This output is a single line which goes high once per minute. On minute marks the output remains high for two seconds, on hour marks the line is held high for 4 seconds and for the day mark, a six second high is provided.

3-38 This output is driven by Q1 on assembly 86-42. This is a MPS3702 transistor and will source 40 ma. at 4.0 VDC. This drive is provided from pin #2 on the assembly 86-42 through a wire to the rear panel BNC.

3-39 A second format of this slow code is provided and can be easily field converted. If the wire from pin #2 of assembly 86-42 is connected to pin #1 on the assembly, the complement of pin #2 described above is provided. (See Figure 3-1). Pin #1 output is driven by Q2 (2N3904) with approximately 6K Ω pull up to 5VDC. This will drive 2 TTL loads. When wired in this manner, the output on the rear panel BNC will be normally high. On the minute it will go low 2 seconds, 4 seconds on the hour and 6 seconds for a day indicator.

3-40 NOTE: If "External Oscillator" option is ordered in conjunction with Parallel BCD, RS-232 or IEEE-488 output options, the "Slow Code" output is not on a rear panel connector but the user is free to lift the lid and obtain this output from pin #1 or #2 of assembly 86-42 for use.

3-41 60 HZ

3-42 The precision 60 Hz output on the rear panel BNC, like the Slow Code, has been provided primarily for the purpose of supplying a known 60 Hz signal to drive synchronous motors. This output, when supplied through a power amplifier such as the Kinemetrics Model PA-1, will provide a constant 60 Hz signal for driving drum recorders independent of local power line variations.

3-43 A quasi-square wave is provided for this purpose with transitions on exact milliseconds. The half cycle periods are 8ms, 8ms, 9ms, 8ms, 8ms and 9ms, etc., then repeating the pattern. This provides exactly a 60 Hz square wave after the average of three cycles.

3-44 Driven by U_{11} on assembly 86-42 (74LS00) this output is capable of driving 5 TTL loads. The output is from the front edge of assembly 86-42 from a bifurcated terminal labeled "60 Hz", through a wire to the rear panel connector.

3-45 EXTERNAL OSCILLATOR (*Special Order Option*)

3-46 If optionally ordered, this rear panel input provides for a local lab standard type of oscillator to be utilized as a clock time base during periods when phase lock with the satellite is lost.

3-47 The input frequency for this option may be anywhere between 100kHz and 100MHz in increments of 100kHz. The signal can be a sine wave or square wave with the low level less than .4V and the peak greater than 2.4 (TTL). This input is presented from the rear panel BNC through a coax to an input of U_7 (74LS74) which has a 10KΩ pull up to +5VDC. This input therefore is one TTL load.

3-48 Operationally, anytime the Model 468-DC is unable to phase lock to the 100 Hz data rate from the satellite, the clock time base will utilize the provided input in the "External Oscillator" BNC connector. If frequency is not provided on this BNC, the 468-DC will continue to operate on its own internal crystal.

3-49 On Assembly 86-74, a green LED has been provided (See Figure 3-1) to show the user that the 468-DC recognizes the presence of his external oscillator. If the LED is not lit, the unit does not recognize the input signal and further investigation will be necessary for proper operation of this option.

3-50 When the situation arises that lock to the satellite is lost, even if a cesium oscillator is used for the external oscillator, the indications of time drift continue. Therefore, the colons on the display and whole display will blank and flash in the usual manner to indicate loss of satellite reception even in case of a "perfect" external time base. The output time error message in IRIG B, Parallel BCD, RS-232 and IEEE-488 also function to indicate loss of accuracy.

3-51 IRIG H (*Special Order Option*)

3-52 When ordered, IRIG H is provided on a rear panel BNC. If this is ordered in conjunction with Parallel BCD or RS-232 or IEEE-488, the 1Hz described in Section 3-24 is deleted in favor of this output. The 1Hz is available on assembly 86-42 as described but is not on a rear panel connector. The user can easily open the the lid and obtain this 1Hz if desired.

3-53 The format of the IRIG H time code is covered in Section VII

3-54 As shipped from the factory, the IRIG H Code is in D.C. Level Shift format. This output is provided through a 2N3904 (on Assembly 86-42) with a 3.3K Ω pull up to +5VDC. On request, this output can be supplied as a 1kHz amplitude modulated carrier. In this case, the IRIG B will be supplied as DC level shift (See Section 3-35). The 1kHz generations and modulation system, originally used for the IRIG B (Section 3-32), will then be used for the IRIG H, providing a 1kHz carrier amplitude modulated in IRIG H format as described in SECTION 3-32.

3-55 PARALLEL BCD TIME OUTPUT (*Special Order Option*)

3-56 The Parallel BCD Time Output option is designed to synchronize other equipment at the time provided by the National Bureau of Standards. This output consists of 42 lines of BCD data from 100's of days to units of milliseconds as shown in FIGURE 3-4. Also, included with this option are four lines to indicate the worst case error on the time outputted. One line indicates error of more than ±500ms, ±50ms, ±5ms and one indicated ±1ms. A 1Hz and 1kHz are available on the output connector which can be used to indicate to the user when the BCD time data on the lines are changing states. If this option is included, a 50 pin "D" connector has been installed on the rear panel.

3-57 All of the 42 BCD lines are driven by #CD4050B's and are capable of driving two TTL loads or multiple CMOS loads. These lines are high to indicate a one in that position in the BCD code. For further information regarding the output of these lines and their capabilities, refer to SECTION V.

3-58 The pin of each output is shown in FIGURE 3-4 on the following page.

3-59 During normal operation, after start-up and synchronization with the Satellite, the four time quality lines will be in a low state. When phase lock with the transmitter is lost, the Model 468-DC will provide the user with a worst-case estimate of the accumulated clock drift based on the VCXO drift rate. This estimate is provided by each of the four lines changing to the high state in turn as the clock time base drifts from synchronization with N.B.S. When the time could be worse than ±1.0ms the output on pin #50 will go high, at ±5.0ms. Pin #14 will go high and on through pin #17 for worse than ±0.5 second accuracy. Each of these lines is driven by a RCA #CD4050 and is capable of driving two TTL loads or multiple CMOS loads. It will be noted that when the +50ms line goes high, the colons on the display will flash and when the ±500ms line goes high, the complete display will flash.

3-60 When phase lock is regained, the lines will again go low as the unit re-corrects to the proper time. On initial turn-on of

PIN #	OUTPUT DATA	PIN #	OUTPUT DATA	PIN #	OUTPUT DATA
1	GROUND	18	2's of 10's of hrs.	34	8's of seconds
2	IRIG B Time Code	19	1's of 10's of hrs.	35	4's of seconds
3	2's of 100's of days	20	8's of hrs.	36	2's of seconds
4	1's of 100's of days	21	4's of hrs.	37	1's of seconds
5	8's of 10's of days	22	2's of hrs.	38	8's of 100's M-sec.
6	4's of 10's of days	23	1's of hrs.	39	4's of 100's M-sec.
7	2's of 10's of days	24	4's of 20's of mins.	40	2's of 100's M-sec.
8	1's of 10's of days	25	2's of 10's of mins.	41	1's of 100's M-sec.
9	1 kHz	26	1's of 10's of mins.	42	8's of 10's of M-sec.
10	8's of units of days	27	8's of minutes	43	4's of 10's of M-sec.
11	4's of units of days	28	4's of minutes	44	2's of 10's of M-sec.
12	2's of units of days	29	2's of minutes	45	1's of 10's of M-sec.
13	1's of units of days	30	1's of minutes	46	8's of units of M-sec.
14	$\pm$5ms. (See Note #3)	31	4's of 10's of sec.	47	4's of units of M-sec.
15	$\pm$50ms. (See Note #3)	32	2's of 10's of sec.	48	2's of units of M-sec.
16	1 Hz	33	1's of 10's of sec.	49	1's of units of M-sec.
17	$\pm$500ms. (See Note #3)			50	$\pm$1.0ms. (See Note 3#)

NOTES: 1) Mating Connector TRW #DD-50S or equivalent.

2) Time accuracy lines in high state indicates time accuracy worse than level specified.

FIGURE 3-4 - PIN OUT CONFIGURATION - PARALLEL BCD TIME DATA - MODEL 468-DC

the instrument or after a power failure, the +500ms line will remain in the high state until the display is turned on, thus indicating that the time on the parallel output lines is not correct to the accuracy indicated by the other lines, regardless of their state. This line can therefore be used as a read-inhibit line since the data should not be read when when this line is in the high state. Refer to the 1 Hz and 1 kHz description below for additional parameters on reading the time of the Parallel Output option.

3-61 The 1 Hz output line on Pin #16 is driven by a #CD4050B and is capable of driving two TTL loads or multiple CMOS loads. This line goes to the high state on time and remains high for 900ms. At any time the 1 Hz line is high, the data on the parallel output lines from the seconds level up is not changing states and is available for reading.

3-62 If it is desired to read the milliseconds lines as well as the seconds through days, the 1 kHz line should be utilized as an indicator that the lines are not changing states. The 800's of milliseconds down to 1's of milliseconds are driven by synchronous counters and may be changing states during the first ½ microsecond of any millisecond.

3-63 The 1kHz line is driven by a #CD4049B and is capable of driving two TTL loads or multiple CMOS loads. The 1 kHz output can provide information to the user in two formats. The first format is as shipped from the factory. The second output format can be converted to in the field by two simple internal modifications.

3-64 As supplied from the factory, the 1 kHz output on pin #9 of the "D" connector goes high on the millisecond for 500 microseconds and then goes low for the remaining 500 microseconds. Since the state of the Parallel Output Time data may be changing state during the first ½ microsecond of any millisecond, the transition from the low to the high state has been delayed to allow the milliseconds counter to stabilize. The rising edge of the 1 kHz signal may be used as a Data Strobe. If, rather than one point in time, a time period of when it is "OK" to read is desired, the time period starting at the rise in level of the 1 kHz line and continuing for the next 500 microseconds can be used. This 1 kHz line should be used in conjunction with the +500ms line as described above to determine if the time data is correct and readable.

3-65 The second format for the 1 kHz output line will provide an output which will go to the high state approximately 3.0 microseconds before the millisecond and low 2 microseconds later. This line will not go to the low state if the estimated time error of the instrument is worse than +500ms and will also stay in the high state after initial turn-on until the data on the parallel output lines are correct. This line, therefore, provides one line which, when in the low state indicates that the time data is "OK" to read. To

convert the Model 468-DC to this configuration on the 1 kHz line, remove the bottom cover of the instrument and locate assembly 86-44. For identification of this Assembly and its parts, see FIGURE 3-5 of this manual. Locate the jumper wires (looks like a ¼ watt resistor with one black band) labeled JPR3. Unsolder the end connected to the hole labeled "A" and solder it into the hole labeled "B". Unsolder the jumper marked JPR2 and remove it from the board. In the place of JPR2, solder in a 33k Ω resistor (¼ watt ±5% carbon resistor preferred). Replace the cover and the screws, the conversion is now complete.

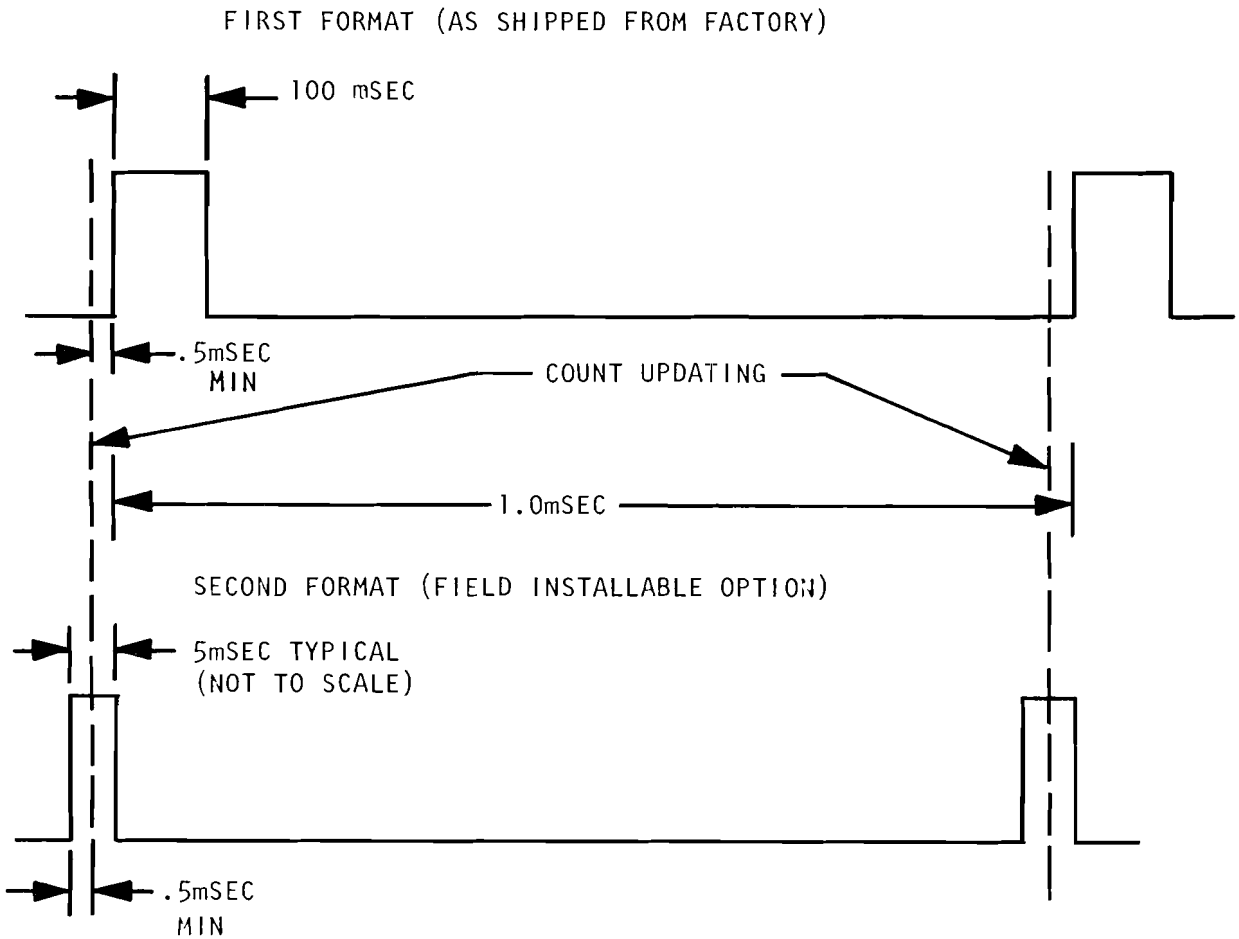


FIGURE 3-5 MILLISECOND COUNTER TIMING DIAGRAM 1KHz SIGNAL SHOWN PIN 9 OF OUTPUT CONNECTOR

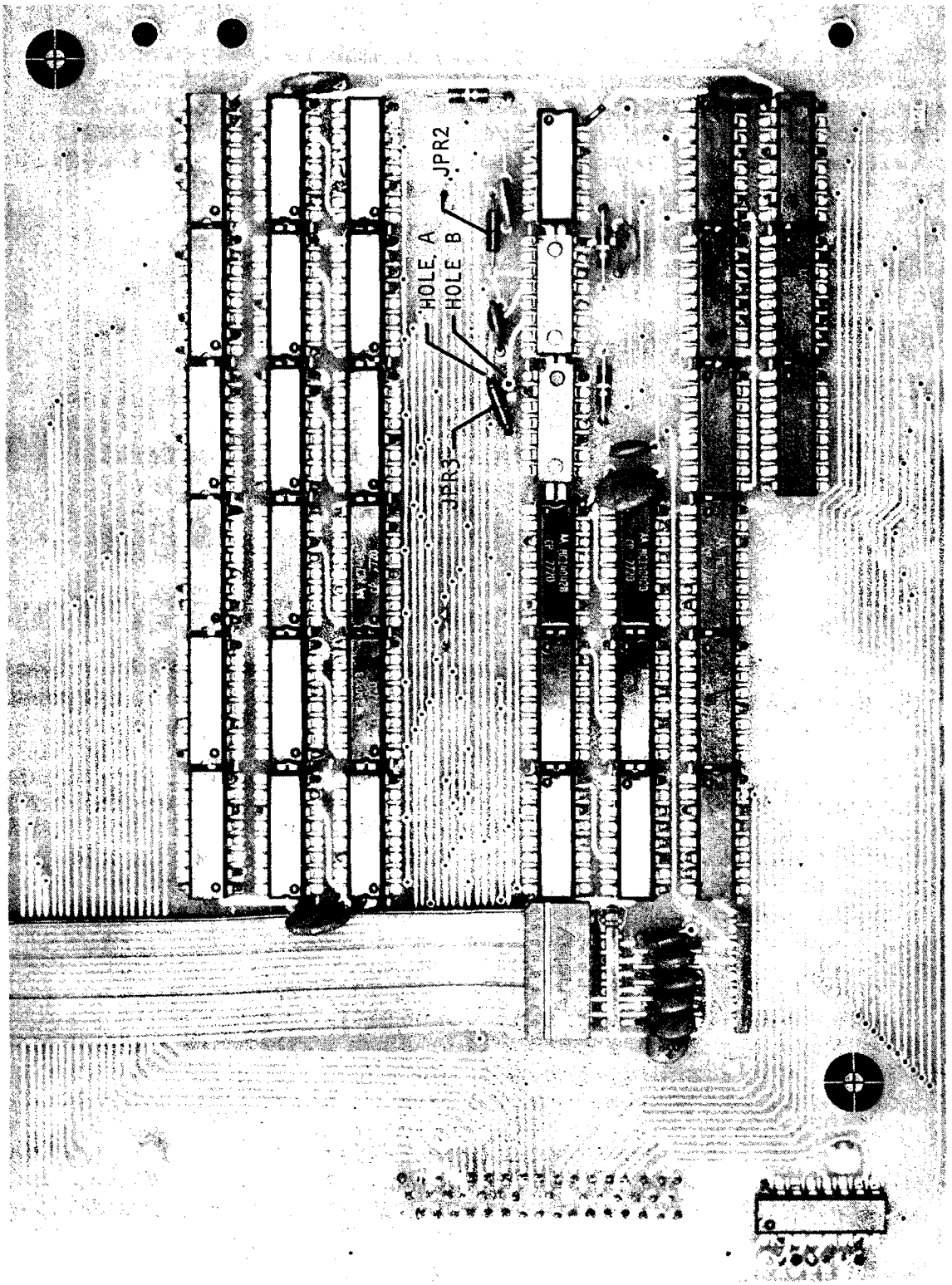


FIGURE 3-5

PARTS LOCATION - PARALLEL BCD OUTPUT OPTION

3-66 RS-232 TIME OUTPUT (*Options*)

3-67 The RS-232 Time Output option, available on Model 468-DC, provides time communication to the user via a bi-directional asynchronous RS-232 port. The output is compatable electrically and mechanically with the E.I.A. Standard RS-232 C as described for a data terminal. Thus, the rear panel connector is a TRW #DC-25P or equivalent. Messages are sent and received using ASCII coded characters in most standard data rates and formats.

3-68 Units supplied with this option have a real panel mounted 25 pin "D" connector with the following pinout:

PIN #	DESCRIPTION
1	Chassis Ground
2	Transmitted Data
3	Received Data
4	*Request to send (internally connected to Pin #5)
5	*Clear to send
6	Not Used
7	Signal Ground
8-24	Not Used
25	*Remote Display Driving (IRIG B)

*These are non-standard connections which are nonetheless compatable with most data terminal equipment.

3-69 The unit as shipped is set for a baud rate of 300, odd parity, one stop bit, and a word length of 8 bits. If it is desired to change these functions, it will be necessary to remove the bottom cover. Remove the four screws which hold on the bottom lid, remove the lid and set it aside. Located on this board are two eight position switch assemblies. One assembly is for the baud rates of 110 to 9600 and the other is to set the parity, number of stop bits, the work length, and other functions as described in "NOTES", SECTION 3-97. (See FIGURE 3-6)

3-70 The baud rate switch is shipped from the factory set for 300 and to change the rate simply slide that switch to the off position. Select the desired rate and slide the appropriate switch to the "ON" position. Energize only one switch position at a time.

3-71 Format selection of the parity (odd or even), number of stop bits (1 or 2) and the word length (7 or 8 bits) can be accomplished by the use of the second eight position switch assembly.

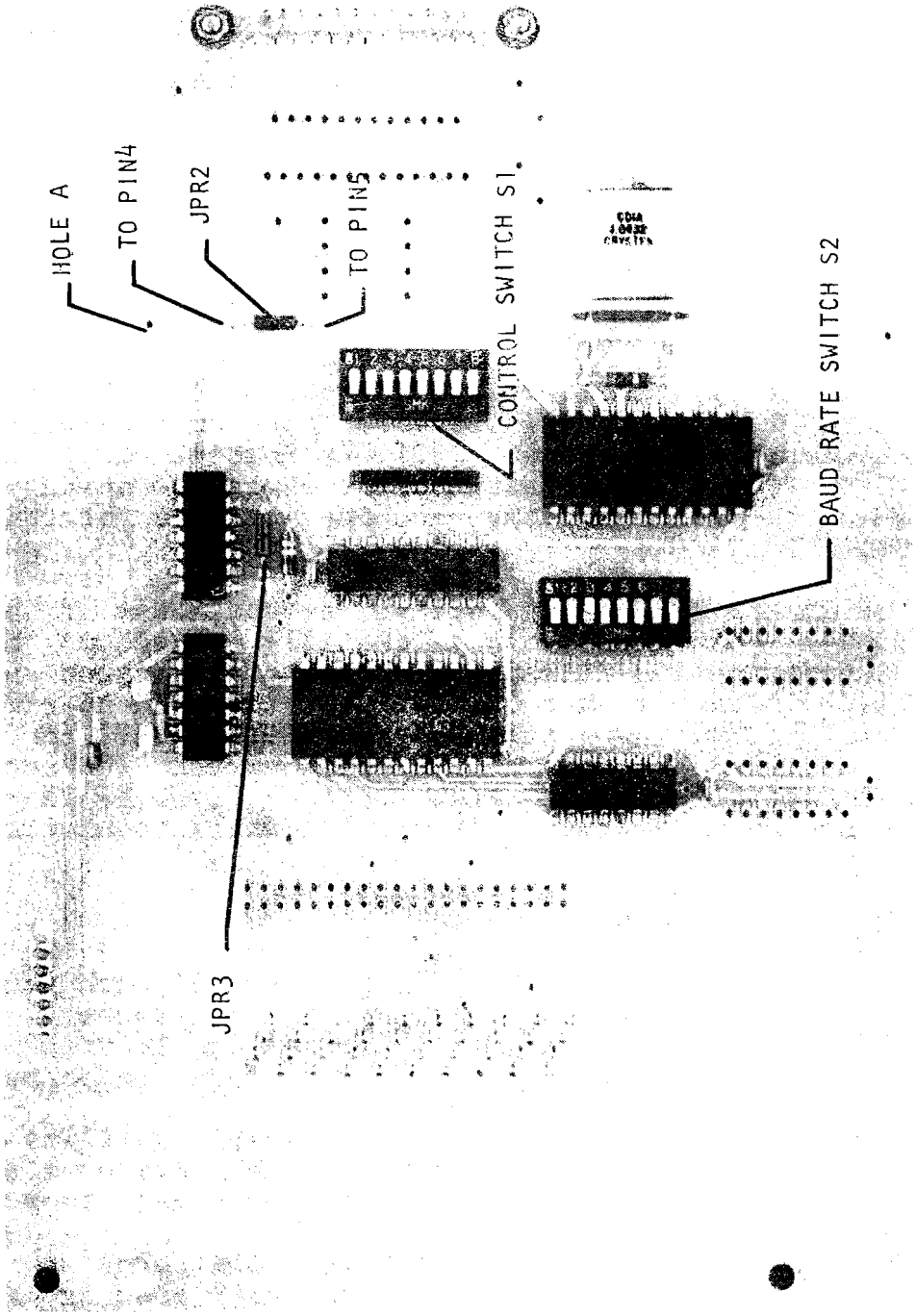


FIGURE 3-6

PARTS LOCATION - RS-232C OUTPUT OPTION

PARITY ODD-EVEN	NO. OF STOP BITS 1-2	WORD LENGTH 7-8	FORMAT
ON	ON	ON	Even Parity + 2 Stop Bits + 7 Bits
OFF	ON	ON	Odd Parity + 2 Stop Bits + 7 Bits
ON	OFF	ON	Even Parity + 1 Stop Bit + 7 Bits
OFF	OFF	ON	Odd Parity + 1 Stop Bit + 7 Bits
ON	ON	OFF	2 Stop Bits + 7 Bits
OFF	ON	OFF	1 Stop Bit + 8 Bits
ON	OFF	OFF	Even Parity + 1 Stop Bit + 8 Bits
OFF	OFF	OFF	Odd Parity + 1 Stop Bit + 8 Bits

3-72 Electrically, the levels of the outputted ASCII code is per EIA Standard RS-232 C as available from Electronic Industries Association, Engineering Department, 2001 Eye Street, N.W., Washington, D.C. 20006. This reference is suggested for any user of this system as it is the industry accepted standard for this interface system.

3-73 With the RS-232 output option, several modes of operation are possible. When the clock is initially turned on, the RS-232 option automatically defaults to the once per second output mode of operation. Refer to Mode C, SECTION 3-75. The RS-232 output option will always (exceptions as in SECTION 3-97, note #4, Position 6 and SECTION 3-80) stay in its then current mode until one of the ASCII control characters (C, T, F, M, P, A, R) is received to override the previous command. Below is a description of these modes.

MODE	FORMAT
C	Transmission of the time once each second.
T	Transmission of the time on request.
F	Selection of the format for the time message.
M	Transmission of a mark signal at a pre-programed time.
P	Transmission of the current satellite position.
A	Display and periodic transmission of the data collection platform addresses relayed by the "GOES" Satellite.
R	Reset Mode, which sets the format to the "Default Format" and then goes automatically to Mode C.

3-74 RS-232 MODE DESCRIPTIONS

3-75 MODE C

When the clock is turned on, the RS-232 option automatically defaults to the once per second output mode of operation in a format as described below:

(CTRL A) DDD:HH:MM:SS Q (CR) (LF)

Where: DDD is the three digits representing day-of year
HH is the two digits representing hours
MM is the two digits representing minutes
SS is the two digits representing seconds
Q is a time quality indicator

The time quality indicators are:

?	indicates a possible error of +500 milliseconds
#	indicates a possible error of ∓50 milliseconds
*	indicates a possible error of ∓5 milliseconds
.	indicates a possible error of ∓1 millisecond
SPACE	indicates a possible error of less than 1 millisecond

3-76 When in Mode "C" the carriage return (CR) start bit begins on the second, +0 to 1 bit time. If the maximum timing precision is desired from this output, it is recommended that Mode "M" be used. See SECTION 3-86

3-77 See Note 1 and 2, SECTION 3-97

3-78 MODE T

When a "T" is received, the time as of the end of the first stop bit of the "T" is saved in a buffer. It is then immediately outputted in the current format. The unit then awaits further instructions.

3-79 A mode similar to mode "T" can also be initiated by an external trigger. When the external trigger is used, the current time is stored when the "Clear to Send" line (Pin #5) goes low (TTL or RS-232 levels). No further action occurs until "Clear to Send" goes high, at which point the stored time is outputted in the current format. The unit then awaits further instructions.

3-80 Since this external trigger takes precedence over the other modes, it is normally locked out by a jumper wire on the option board. If it is desired to use this mode, remove the bottom cover of the instrument. The printed circuit board with the parts facing you is the RS-232 option card. See FIGURE 3-6. Cut out or unsolder the jumper labeled "Trigger Mode". This mode is now in operation. Remember when this jumper is cut, the external trigger takes precedence over all other modes and all other normal commands are locked out, whenever "CTS" is held low.

3-81 It may also be desireable to remove the jumper at the rear edge of the circuit which connects the "Request to Send" and "Clear to Send" lines together (Pin 4 and 5). This will not affect the operation of the output option but may have an effect on other equipment in the system.

3-82 MODE F

After an "F" is received, the unit is placed in the "Format Mode", awaiting a time message format string. This format string consists of a 17 character dummy time message consisting of day-of-year through time quality character. As each character is received, it controls its respective position in the output format. An "X" in any position suppresses the output of its respective position. In the delimiter positions, any character received for that position will be outputted. In the other non-delimiter positions, any character other than "X" or any of the ASCII control characters, (see SECTION 3-73), since the clock will see them as a command, allows that position to be outputted as understood by the clocks time system. Be certain not to use a "M" as the unit will see this as a mode change command to mode "M". The format can be selected within the limits of the maximum format described below:

(CTRL A) DDD__HH__MM__SS__SSS Q (CR) (LF)

3-83 Each __ represents a single delimiter position which can be almost any ASCII character, typically colons, a decimal point, etc.

3-84 This format will now be the format of the outputted time. It should be noted that the milliseconds is not available in Mode "C" even if so formatted.

3-85 EXAMPLE

If the option receives: F 123/12:34:56.789Q, the result will be printing a slash between the days and hours with colons separating hours from minutes and minutes from seconds. A decimal point will be in the seconds between the seconds and hundreds of milliseconds. This string will be preceded by (CTRL A) and followed by a time quality indicator (Q) and (CR) (LF).

Secondly, if F XXXXXXXXXXXXX124X is received, the result will be printing only the fractional part of the seconds, preceide by (CTRL A) and followed by (CR) (LF).

As a check of the entered format, the current time will be sent in the new format after the completion of the 17 character format string.

3-86 MODE M

This mode allows the user to preset a time in the future and to be notified when this time occurs. An "M" followed by the desired alarm time presets the time into the unit. The desired time is then echoed, and then the option waits for that time to occur. When the desired time occurs, an "M" is sent (this may be suppressed by the dipswitch position 1 on the option board -- See Note 4, SECTION 3-97.

3-87 As a second indication that the alarm time is present, the unit can be converted to pull Pin #4 low during the alarm time. This is done by moving the jumper connector Pin #4 to Pin #5, to connect Pin #4 to hole "A". See FIGURE 3-6. When this change is made, Pin #4 will be held low through the alarm time and high otherwise. This form of time indication is suggested when the user desires the highest possible time precision from the RS-232 output on the Model 468-DC.

3-88 When one inputs the string for the alarm time, all the delimiters must be included for place holding. An "X" in any position makes that digit a "don't care" digit. If a "Line Feed" is placed in any position, this terminates the string and sets successive set time digits to 0, otherwise all 16 characters including the milliseconds digits of the time must be sent.

3-89 EXAMPLE

M185*11:06:04.387

This would trip the alarm festure at 11:06:04.387 on the 4th of July and an "M" would be sent. If the request to send line had been converted as described above, this would be held low for that millisecond.

M185*11:XX:XX.XXX

This would transmit an "M" at eleven o'clock on the same day and the "Request to Send" line would stay low for the hour (through 11:59:59.999)

MXXX*XX:XX:XX (LF)

This input alarm configuration would provide for an "M" at the start of each second and the "Request to Send" line would be held low for one millisecond.

3-90 MODE P

When ASCII "P" is received on the Model 468-DC, the current position as received from the "GOES" Satellite will be outputted.

An example of the format is:

13523+013-062

Where in this example:

13523 Represents the longitude of 135.23°
+ can be + or -
013 represents the latitude of +0.13°
+ can be + or -
062 represents +62 microseconds difference in the radius of the satellite from the nominal position.

3-91 MODE A

When this "Address Display" mode is selected by sending an "A", the most recent active address received from "GOES" satellite will be displayed. An address is transmitted each half second. Most addresses are the dummy address (34 85 76 3E) which is not displayed, but is indicated by flashing the hundreds of days digits and by sending a null character over the RS-232 link. Any other address is displayed immediately after it is received, and also output over the RS-232 link, followed by a space. After each 8 address are sent, a CR-LF sequency is inserted.

3-92 If the MLS code is not being correctly read and decoded, the colons on the display will blink at a 2Hz rate and the displayed characters will not change. There will also be no output on the RS-232 interface, which is the best available indication of poor or erroneous data reception.

3-93 Typical Address: B605321D

"B" and "D" are displayed lower case - don't confuse 'b' with "6".

3-94 This mode can be forced by dipswitch position 6, see Note 4, SECTION 3-97.

3-95 MODE R

This mode, when used, is similar to the initial turn on sequency of the instrument. When "R" is received, the unit automatically goes to the "default format" and into Mode "C".

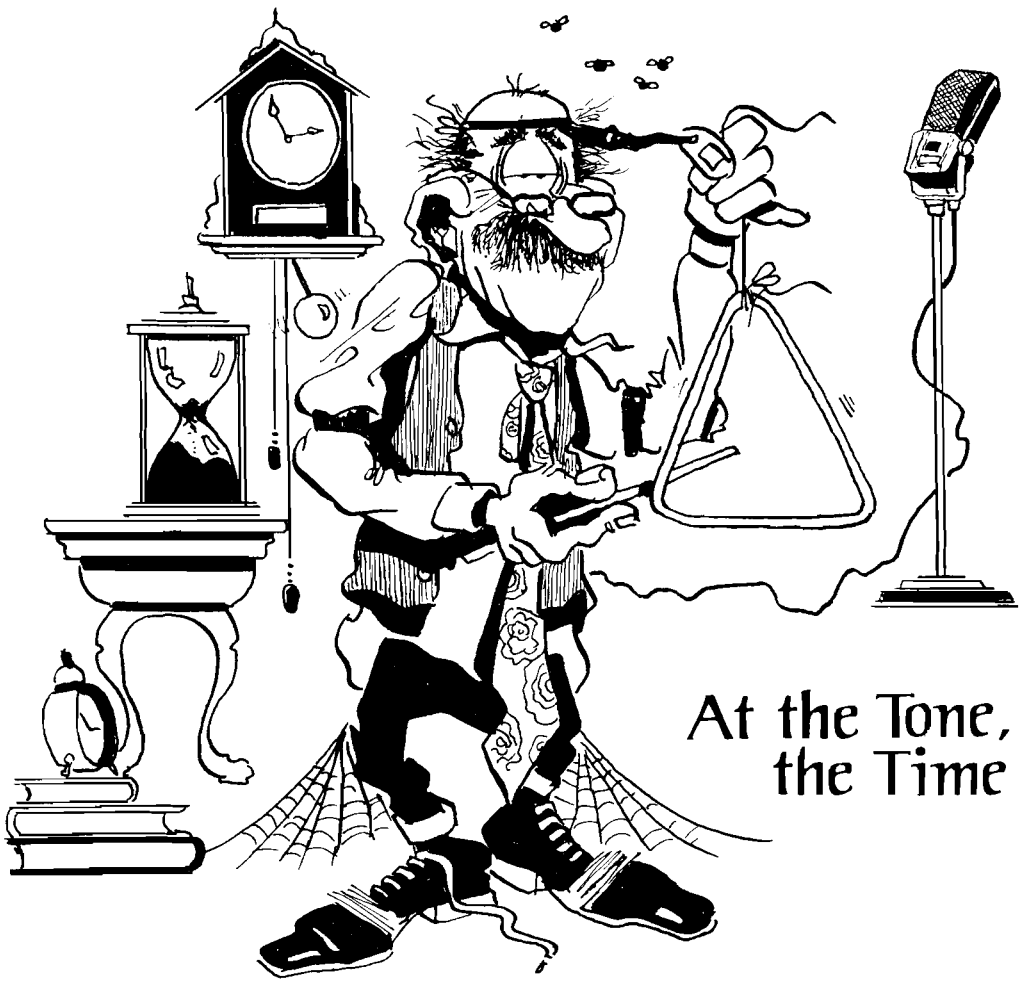
3-96 The initial output string after an "R" command is received by the synchronized clock is not reliable either as to data, time or carriage return. This is due to internal synchronization with the data rate. This is also true when the baud rate is changed in the "R" and "C" modes.

3-97 NOTES

1. (CTRL A), (CR) and (LF) are the ASCII characters 01, OD, and OA in hexadecimal form. They are not under format mode control. (CTRL A) is also known as a start of header.

2. During output, Transmissions are continuous, with the end of the stop bit of one character coinciding with the begining of the start bit of the next character.

3. The RS-232 output option will stay in the current mode it is in (default mode at turn on) until one of the valid ASCII control characters (C,T,F,M,P,A, or r) is received to override the previous command.



At the Tone,
the Time will be...

4. As described in the previous sections of this manual, the dipswitch on this option printed circuit card has several functions. The positions and the functions they control are:

POSITION	FUNCTION
1	Output of and ASCII "M" at the present time, as described form Mode M, is suppressed when "ON".
2	Not used
3	Parity
4	Number of Stop Bits
5	Number of Data Bits
6	Force continous display of satellite address as described for Mode A "ON".
7	Suppress (CTRL A) in default format when "ON"
8	Suppress colons in default format when "ON"

5. Input and output is via an MC6850 ACIA. Refer to manufacturers (Motorola) data sheet for further information.

3-98 IEEE-488 OUTPUT (option)

3-99 INTRODUCTION

The IEEE-488 output option is available on the Model 468-DC to provide the user with a communication port via the IEEE-488 bus. This option is compatible electrically and mechanically with the IEEE-488 standard 488-1978. Messages are sent and received using strings of ASCII coded charcters.

3-100 HARDWARE

The user interface with the option is through a standard IEEE-488 connector. The "BUS ADDRESS" is set by a dipswitch on the output option circuit card. To access this switch, remove the four screws which hold the bottom cover in place, remove the cover. Note the circuit board in the center with the components facing you. On the board end toward the front panes you will find the 8 position switch. The "Address" is set using positions 1-5 of this switch. This switch encodes the address in binary format:

WHEN POSITION #1 IS "ON" A BINARY 1 IS ENCODED
WHEN POSITION #2 IS "ON" A BINARY 2 IS ENCODED
WHEN POSITION #3 IS "ON" A BINARY 4 IS ENCODED
WHEN POSITION #4 IS "ON" A BINARY 8 IS ENCODED
WHEN POSITION #5 IS "ON" A BINARY 16 IS ENCODED
POSITION #6 NOT USED
POSITION #7 NOT USED
POSITION #8 NOT USED

THE ADDRESS OF THE INSTRUMENT IS THEN THE SUM OF THE ENCODED BITS.

The Model 468-DC is shipped from the factory with an address of " 5 ". Therefore switch number 1 and 3 are "on" and all others are in the "off" position.

3-101 EXTERNAL TRIGGER

Also located on this circuit board are two terminals. One is provided for "EXTERNAL TRIGGER IN" and the other "EXTERNAL TRIGGER OUT". These are not provided on rear panel connectors but are available for the user to bring out if he desires. The use of these triggers will be covered in Section

3-102 SOFTWARE

Communications over the bus take place using strings of ASCII characters as mentioned earlier. The output strings from the clock are always terminated by a Carriage Return, Line Feed sequence. The Bus management "EOI" is asserted for the line feed character. The longest string of characters output by the clock on the bus is 20 characters including the carriage return and line feed.

Inputs to the Model 468-DC are also strings of ACSII characters. Whenever a string is input to the unit a Line Feed or EOI will terminate the string and no action is taken on that string until this termination is received. Input strings are stored in a 32 character buffer which wraps around when overflowed. This will cause the 33rd character received to be stored in the first position and so on.

Operation of the clock outputs on the bus is organized by six different modes. A particular mode is initiated by sending the clock a string containing a mode defining character. The first valid mode defining character in the string received defines the mode the clock will be set in.

The valid mode characters are:

A	DATA COLLECTION PLATFORM ADDRESS DISPLAY
F	FORMATTING OF THE TIME MESSAGE
M	MARKED TIME (ALARM CLOCK MODE)
N	VERIFICATION OF MARKED TIME IN MEMORY
P	POSITION INFORMATION OF GOES SATELLITE
T	TIME

3-103 MODE A

The Mode A is used for the purpose of displaying on the front panel display the last transmitted Date Collection Platform (DCP) address as well as obtaining these addresses over the bus port.

When the Model 468-DC receives an "A" the clock display is converted from displaying the time of year to displaying the eight digit address. The 9th digit is blinked to indicate the reception of the dummy address (34 85 76 3E). Each 1/2 second an address is transmitted, most of which are the dummy address as a place holder. Note that "B" and "D" are displayed in lower case and is easily confused with "6".

Once the Model 468-DC has been placed in this mode it will remain in the mode until another valid mode command is received. When in this mode reading the clock with the bus will get the last transmitted address as a response. Any address received by the unit from the satellite is considered valid if the "MLS" is not being received correctly the colons on the display are blinked at the two hertz rate as an indicator of possible bad reception.

If "AS" is sent to the clock instead of "A" for the address mode a service request will be provided whenever a new address appears on the display (dummy address's are ignored). Also a serial poll will return an ASCII "A" in this case. It should also be noted by the user that when the unit is removed from the address mode and returned to the clock mode for time purposes the time is not valid for one second.

3-104 MODE F

This mode allows the user to establish a desired format for the time message. The format is determined by the strings of characters sent to the unit following the receipt of the "F". This format string consists of 17 characters to format the time response of the clock. Each character in the string controls its respective position in the new output format of the clock.

An "X" in any position of this string suppresses the output of its respective position of the time message. The positions between the days and hours, the hours and minutes, the minutes and seconds, and seconds and thousandths are referred to as delimiter positions. Any character inserted in the input string to format the clock in these positions will be repeated in that position.

The format of the unit can be selected within the limits of the maximum format:

DDD_HH_MM_SS_tttQ

Each "_" above represents a delimiter position and can by any ASCII character except "X".

EXAMPLE:
If the option port receives: F123/12:34:56.789Q the resulting response by the clock will be the day of year, a slash, the hours colons, the minutes, colons, the seconds, a period, the thousandths carriage return and line feed.

Secondly, if FXXXXXXXXXXXXX124X is received by the unit, the resulting response will be printing only the fractional part of the second followed by a carriage return and line feed.

If the format string is terminated short of the 17 characters, the positions in the time string after the termination of the format message will be unchanged by the format operation.

3-105 MODE M

This mode allows the user to preset a time in the future and to be notified when that time occurs. An "M" followed by the desired alarm time presets that time into the unit. When the desired time occurs, a service request is initiated and the external trigger output line (see

Section 3-101) is set low. When the preset time has passed the external trigger line is returned to the high state.

The service request will be cleared by a device clear command, by setting a new alarm time, by reading the alarm time using mode "N" (see Section 3-106), or by a serial poll. The status byte returned in a serial poll is an ASCII "M". NOTE: This is in conflict with at least tektronix standards for the IEEE-488 bus.

When an alarm string is input, all of the delimiters must be included as place holders. An"X" in any position makes that digit a "don't care" digit. If a line feed is placed in any position the string is terminated and sets the successive digits to "0".

EXAMPLE:
M185*!!:06:04.387
This input to the unit would trip the alarm feature at 11:06:04.387 on the 4th of July and the external trigger would be held low for that millisecond.

MXXX*XX:XX:XX (line feed)
This program configuration would provide a service request at the start of each second and the external trigger output line would be held low for one millisecond.

3-106 MODE N

Mode "N" is provided for the purpose of verifying the alarm time programmed into the unit. When the Model 468-DC receives a "N" the response will be the previously programmed time in the "M" mode. After transmitting the complete time string, the model 468-DC returns to "M" mode.

3-107 MODE P

When the unit is placed in the "P" mode the current position of the satellite being received is outputted on the bus. This position information is provided over the satellite link by the National Bureau of Standards for the purpose of determining propagation delay of the received signal at the users site. This position information is based on predictions of the satellite 30 days in advance and as such has obvious limitations. Currently the National Bureau of Standards only provides certanity that this information is accurate to $\pm$100us for propagation delay calculations.

True Time makes no claims as to the accuracy of this information but does provide it as an output for the user interested in this information.

EXAMPLE OF CLOCK RESPONSE:
10523+013-062 Carraige Return Line Feed
Where:
10523 represents the longitude of 105.23° West
+ can be + or -
013 represents the latitude of +0.13°
- can be + or -
062 represents -62 microseconds difference in the radius of the satellite from the nominal position.

3-108 MODE T

When a "T" is received the time as of the completetion of the hand shake of the string terminator (LF or EOI) is saved in a buffer. This saved time can then be read out by addressing the clock as a talker and retrieving the time message. If the unit has not has a format specified by the "M" Mode the default format of the time response will be:

DDD HH MM SS.tttQ carriage return line feed

This format being day of year, hours, minutes, seconds, milliseconds and time quality character. This is 19 characters including the carriage return and line feed.

"Q" is the time quality character showing the estimate of worst case time error:

WORST CASE ERROR	ASCII CHARACTER
MORE THAN + 500 ms.	?
MORE THAN ∓ 50 ms.	#
MORE THAN ∓ 1 ms.	*
MORE THAN ∓ 1 ms.	
MORE THAN ∓ 1 ms.	(ASCII SPACE)

If a format change is desired see Section 3-104.

Either a Group Execute Trigger command or a positive transition on the External Trigger In line will also catch the time for output when read. If a "T" or a Group Execute Trigger is received the time will be caught whether or not any previously caught time has been read. The External Trigger In line will ignore the positive transitions after the first one, until the time has been completely read out.

SECTION IV

THEORY OF OPERATION MAINTENANCE AND TROUBLESHOOTING

4-1 THEORY OF OPERATION MODEL 468-DC

4-2 The 468-DC receiver, decodes and outputs the time, using the NBS supported time code transmitted via the "GOES" (Geostationary Operational Environmental Satellite: Satellites, which are operated by NOAA (National Oceanic and Atmospheric Administration).

4-3 The transmission which carries the time code is at a frequency near 468 MHz. The data is encoded by phase shift modulation of the carrier (Manchester encoding) at a 100 bit per second rate. The code format breaks each second down into two ½ second sections, each consisting of 50 bits (½ of the available 100 bits in the second). During this ½ second the first 4 bits [1] are used by the National Bureau of Standards for their controlled information.

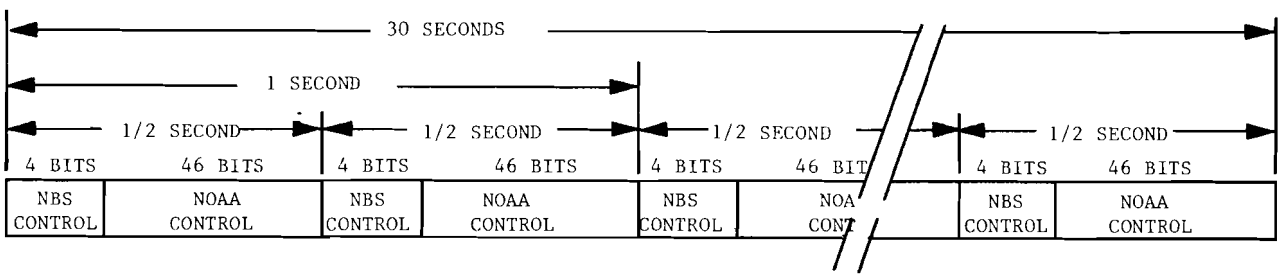


FIGURE 4-1 GOES TRANSMISSION FORMAT

4-4 The N.B.S. Information consist of:

1. Synchronization word
2. Days, hours, minutes, second
3. UT_1 correction
4. Predicted satellite position
5. Remaining space is used for experimental purposes

1. The remaining 46 of the 50 available bits are used by N.O.A.A. for the purpose of "Maximum length sequence" (MLS) which is a synchronization word and for data collection platform "Interrogation Address" which is the main purpose of their channel.

This information obviously cannot be conveyed in a single 4 bit character of a ½ second, therefore one character each ½ second for 30 seconds is utilized. This data in items 1-5 above is repeated every 30 seconds.

4-5 A phase locked receiver is used to receive and recover raw data from the satellite signal. The raw data is processed by analog circuitry and then passed to a microprocessor for conversion to useful outputs; among which are a visual display, one Hertz and one kilohertz timing pulses, and several optional communication ports. An overall block diagram of the hardware involved is given in FIGURE 4-2

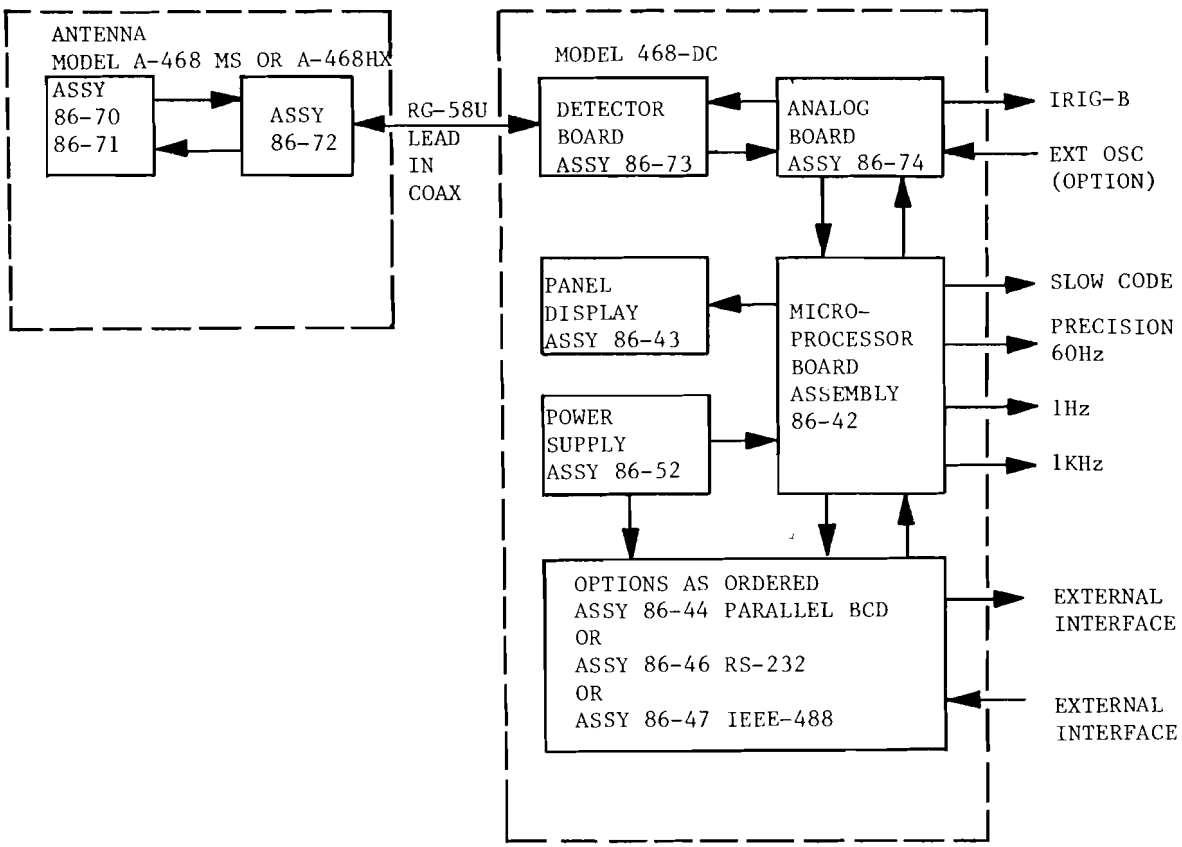


FIGURE 4-2 OVERALL BLOCK DIAGRAM - MODEL 468-DC

4-6 The receiver portion of the clock consists of the active antenna, the detector board (Assembly 86-73), and

part of the analog board (Assembly 86-74) - all under the control of the program on the digital board (Assembly 86-42). The active antenna receives the satellite signal, amplifies it by about 140db, and translates it in frequency to 4.5 MHz, using the first local oscillator frequency generated on the analog board in the main instrument and sent up the connecting coax together with the 12VDC power. The second local oscillator is contained in the antenna. A block diagram of the active antenna is shown in FIGURE 4-3.

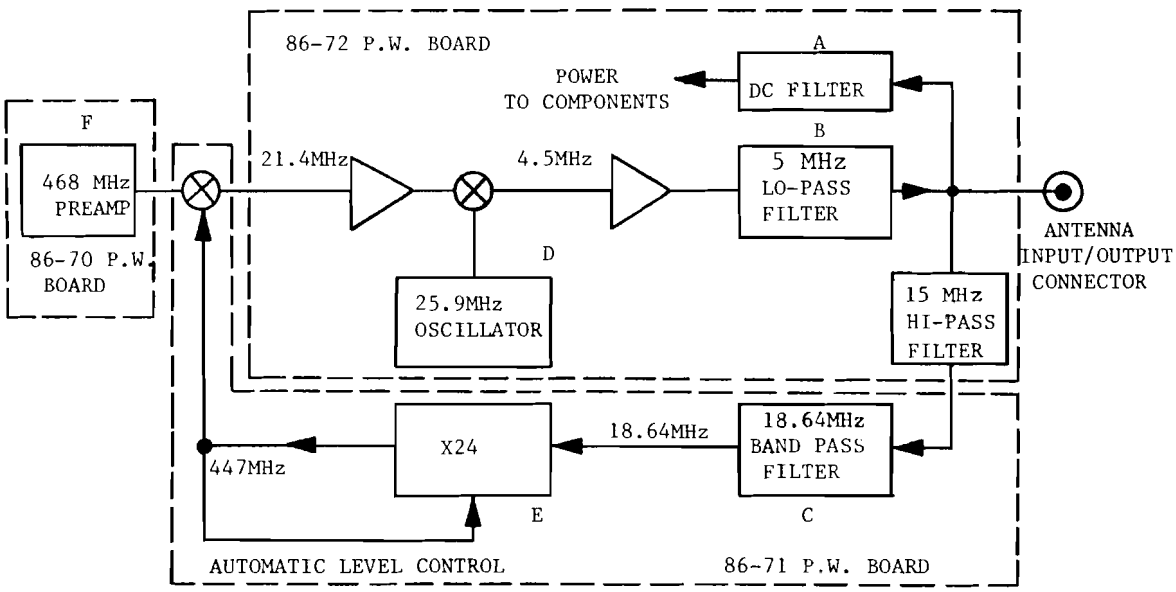


FIGURE 4-3 ACTIVE ANTENNA BLOCK DIAGRAM - MODEL A-468

4-7 The 4.5 MHz output of the active antenna comes down the coax to the detector board (Assembly 86-73), where it is translated to baseband using the third local oscillator in conjunction with two balanced modulator/demodulators; one in phase, the other in quadrature with the satellite signal.

4-8 On the analog board, the in phase baseband signal is an indication of signal strength, and is compared with a reference level to decide whether a satellite signal is being received, this information is passed on to the digital board, as well as being displayed by the LED RF unlock indicator.

4-9 The quadrature baseband signal constitutes the raw manchester data and goes to the data phase locked loop. It is also used by the RF phase locked loop as the error signal to force the RF loop to stay in lock.

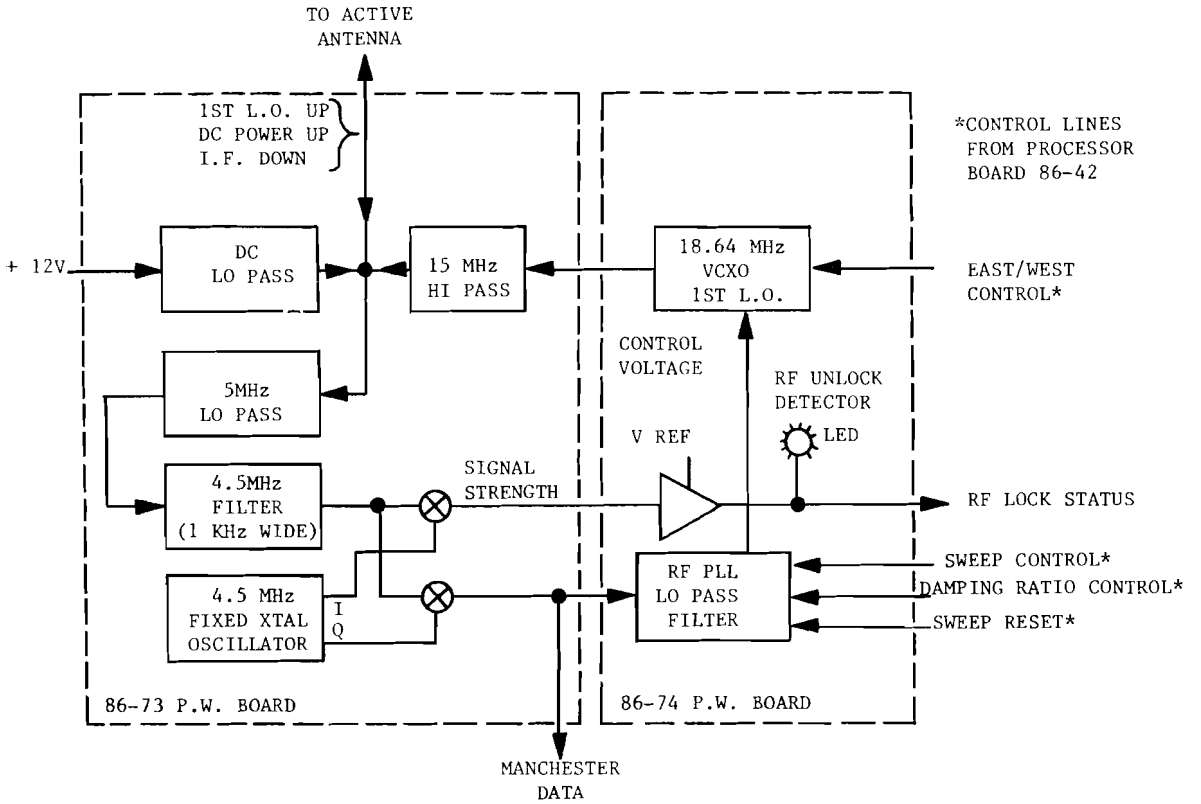


FIGURE 4-4 PHASE LOCK LOOP BLOCK DIAGRAM - MODEL 468-DC

4-10 In order to recover manchester coded data, two functions must be performed, synchronization, or data clock recovering and data decoding. The data PLL circuitry does both. There are two data PLL circuits, a coarse and a fine. The coarse PLL allows rapid sync to data at turn on while the fine loop serves for precise sync once coarse sync is obtained. One or the other of these PLL's is always operating, under processor control. Whichever data PLL is selected runs the timing circuitry which supplies the timing for the processor and hence, all clock functions. Data clock recovery is performed by a PLL. At turn on, a coarse PLL is used to quickly sync to the data. Thereafter, a fine PLL refines and maintains this sync. The fine PLL has three configurations, under processor control:

1. In normal operation, the PLL locks to the incoming data using the fine data phase detector.

2. If satellite signal is lost and if an external oscillator signal is supplied, the PLL locks to

the external oscillator. Otherwise, it freezes its present frequency.

3. On re-acquiring satellite signal, the PLL seeks data lock using the coarse data phase detector. See FIGURE 4-5.

4-11 The data detector which decodes the raw manchester data is an integrate and dump type, (which constitutes a matched filter for the code) is located on the analog board, the output of the data detector goes to the processor for further analysis.

4-12 Also on the analog board is the external oscillator input, allowing use of a stable external oscillator during periods of interrupted signal reception; and the modulation circuitry for the IRIG B time code output.

4-13 The microprocessor Board (Assembly 86-42) controls the whole instrument by means of the program stored in its memory. The program is discussed in the section on software, SECTION 4-86. All information in the instrument flows through this board. In addition to controlling and receiving controls the front panel display, generates the several timing outputs of the clock, controls the timebase for the clock, and optionally communicates with the rest of the world via the RS-232, IEEE-488, or Parallel BCD interface.

4-14 The display board is controlled by the digital board. It contains a multiplexed planar gas discharge display and their drivers, providing an easily visible visual display of the time.

4-15 The output options also controlled by this board are the communications options. These boards (only one of which can be installed in an instrument) provide the ability to communicate the time to other instruments finding application in larger systems. Presently available options include Parallel BCD outputs, RS-232 Link, and IEEE-488 Bus capability.

4-16 DETAILED DESCRIPTION OF OPERATION

4-17 ACTIVE ANTENNA

4-18 The active antenna, A468MS or A468HX, contains a preamplifier an IF amplifier, and a first L.O. multiplier/mixer, as indicated in FIGURE 4-3 the active antenna block diagram.

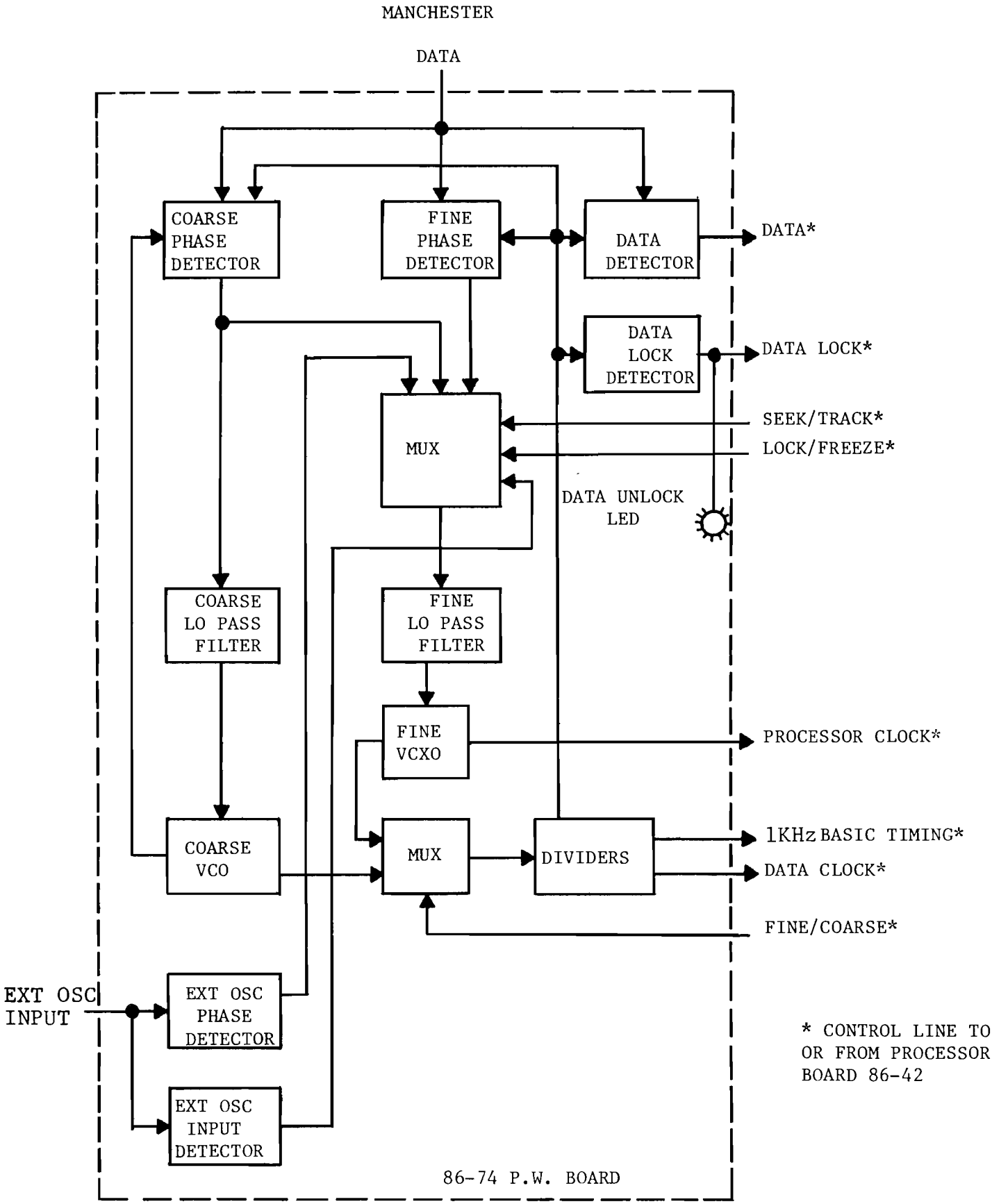


FIGURE 4-5 BASEBAND DATA PHASE LOCK BLOCK DIAGRAM, MODEL 468-DC

4-19 PREAMPLIFIER ASSEMBLY 86-70

4-20 See SECTION 5-4 for schematic of Assembly 86-70/71. The 50Ω stripline tuned amplifier has greater than 16db gain at 468.8 MHz with a noise figure of better than 3db typically. Gain at the image frequency, 426 MHz, is down greater than 20db. Q1 is the gain transistor, Q2 stablizes bias current at 5 MA to provide consistent optimum operation.

4-21 The schematic of the local oscillator multiplier and mixer Assembly 86-71, is also shown in SECTION 5-4.

4-22 This board, Assembly 86-71, accepts the 18.64 MHz first L.O. signal from the main instrument and multiplies it by 24 to provide the actual first local oscillator frequency. 468.8MHz (signal frequency) -21.4MHz (first intermediate frequency) =447.4MHz (first local oscillator frequency) automatic level control maintains the first L.O. power level at +3dbm.

4-23 When the 18.64 MHz signal enters the board it first passes through a bandpass filter, T1, T2, C1, C2, and C3. This removes undesired frequency components from the signal. Q1, Q2 is a variable gain linear stage driving Q3 and Q4, a push-push quadrupler stage (output frequency = 74.56MHz). TP1 and TP2 provide convenient points for monitoring the emitter currents of Q3 and Q4. Q5 and Q6 are a push-push doubler stage multiplying from 74.56 to 149MHz. TP3 and TP4 serve to monitor their emitter currents. Q7 is a single ended tripler stage producing 447 MHz from its 149 MHz input. TP5 allows monitoring of Q7's emitter current. C25, C26, C27, with their associated striplines, comprise a 447 MHz filter to eliminate spurious signals, which could cause undesired responses in the output of the mixer. Typically, undesired components are down by at least 60db. D1 samples the 447 MHz level for the ALC circuitry.

4-24 Of the four sections of U1, one is the ALC amplifier, one drives the red first L.O. unlevel indicator LED, and the remaining two form a window comparator which lights the green "preamp active" indicator, if the preamp supply current demand is between 3 and 7 MA.

4-25 The balanced mixer takes the 447.4MHz L.O. and the 468.8MHz satellite signal and converts them to a signal at the 21.4MHz first IF. Q8, Q9 are a current mirror to control current thru the variable gain stage, Q1, Q2, and thus close the ALC loop.

4-26 INTERMEDIATE FREQUENCY AMPLIFIER BOARD ASSEMBLY 86-72

4-27 See 86-72 Schematic SECTION 5-7, and block diagram SECTION 4-3. The 21.4MHz signal from the 86-71 board passes first through a 13 KHz wide monolithic quartz crystal filter centered on 21.4 MHz, (Y3 and Y4). This provides the primary protection against strong nearby signals, which can be common in the 468 MHz land mobile band. Q1, Q2, Q3, and their associated components provide up to 50db gain at 21.4 MHz. Y5, Y6 are a second 21.4MHz monolithic quartz filter which further reduces undesired signals, primarily internal receiver noise at this point.

4-28 Q4 is the second mixer. In conjunction with Q7 and Y7, the second local oscillator, operating at 25.9 MHz, shifts the satellite signal down to 4.5 MHz, while providing 15db gain. Q5 and Q6 are the 4.5 MHz amplifier, which provide up to 60db gain. D1 and D2 are signal strength samplers, used during alignment. D3 is the AGC rectifier. It samples the received signal, and by applying this sample to the AGC line, maintains a constant output level from the IF amplifier, just short of saturating Q6.

4-29 U1 has one section used as a signal strength amplifier. It is intended for use as an antenna pointing aid for highly directional antennas by monitoring the voltage on terminal #6.

4-30 L1, L2, C43 match the high impedance 4.5MHz output of the IF amplifier to 50 Ω for transmission down line, and at the same time filter 18.6MHz power to keep it out of the IF amplifier. C45, L4, C46 similarly direct the 18.64 MHz first local oscillator signal to the 86-71 board. L3 serves to allow DC power to flow to supply the 86-70, 86-71, and 86-72 boards.

4-31 DETECTOR BOARD ASSEMBLY 86-73

4-32 Signals pass in both directions through the Detector Board. The 18.64 MHz first L.O. comes from the Analog Board Assembly 86-74, goes through the high pass filter, C2, L4, C3 and then goes up the coax to the antenna. See schematic SECTION 5-10, and block diagram SECTION 4-4.

4-33 The 4.5 MHz signal from the antenna proceeds through the low pass filter L1, C4, L2, into the 4.5 MHz crystal filter T1, Y1, Y2, T2, R4 and then to the two balanced modulator/demodulators U2 and U3. The band-

width of this filter is narrow, about 1 KHz. Q1, Q2, with Y3 are the third L.O., running at 18 MHz. U1 divides this by four to provide both in phase and quadrature reference signals for U2 and U3. The frequency of the oscillator is trimmed by C9 to center the received signal in the 4.5 MHz filter passband. U2 and U3 phase detect the signal and output balanced baseband signals to the analog board.

4-34 ANALOG BOARD ASSEMBLY 86-74

See FIGURES 4-4 and 4-5 for a block diagram and SECTION 5-12 for the schematic of Assembly 86-74.

4-35 RF Lock Detector

4-36 The inphase signal from U3 on the detector board is converted to a single ended signal by U15 pins 12, 13, 14. It can be examined at TP2. Typically, this point is at -2.4V when locked to a satellite. Reliable decoding requires less than -1.0v. U15 pins 1, 2, 3 is the signal strength comparator. The inphase signal from U15 pin 14 goes through a low pass filter to reduce the effects of modulation and noise, and is then compared with a reference level fixed at -0.6V. If the in phase signal is more negative than the reference level, U15 pin 14 extinguishes the RF unlock indicator (D7) and, through U25 pins 7, 6, it sends this information to the processor board. U25 serves merely as a level translator for signals going to the processor board from the analog board.

4-37 RF Lock Loop

4-38 The Quadrature signal from U23 on the detector board is converted to single ended by U15 pins 8, 9, 10,

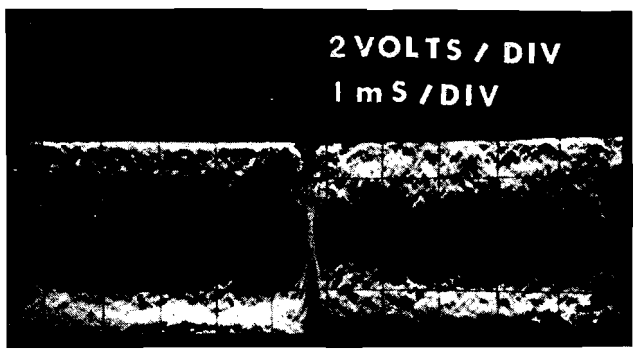


FIGURE 4-6 RAW MANCHESTER DATA (SHOWS APPROXIMATELY 50 BITS SUPERIMPOSED)

and can be examined on TP3. This is the raw Manchester data from the satellite, used by the data PLL's and the data detector. See FIGURE 4-6 below which depicts approximately 50 bits of superimposed data.

4-39 The Manchester data is then inverted and level shifted to compensate for offset voltage by U11 pins 1, 2, 3 and by R45, the symmetry control. The signal then goes to the RF loop low pass filter, U11 pins 5, 6, 7.

4-40 The RF loop low pass filter is an integrator with two inputs. One is the satellite data as described above, the other is a sweep/reset input via U12 pins 1, 2, 13. When the receiver is locked to a satellite signal, U12 pins 1, 2, is an open switch, allowing undisturbed phase lock, but when phase lock is not present, the processor can close the switch, allowing current to flow out of the summing node through R31. This forces the output of the integrator, U11, pin 7, to ramp more positive at about 150mV per second. If a satellite signal is acquired, the processor stops the sweep by opening the switch. If, on the other hand, no satellite signal is detected after the sweep has continued long enough for U11 pin 7 to approach +5V (it takes 40 seconds), the processor issues a reset pulse through U10 pins 1, 2, 3. This causes U11 pin 8 to go high, forcing current into the summing node through R25. This much larger current (than that through R31) rapidly drives U11 pin 7 negative. The reset ends when the node at R27 and R28 becomes negative enough to pull U11 pin 10 below ground, thus driving U11 pin 8 negative, and removing the source of reset current. Meanwhile, the processor, subject to manual override by S1 or S2, can select the other satellite as the target by opening one and closing the other of the analog switches U12 pins 6, 8, 9 and U2 pins 3, 4, 5. These switches select one or the other of two DC voltages set by R37 and R38, to be averaged with the output of the RF loop low pass filter to control the frequency of the first local oscillator, V2, Q5, Q6, D6. The output of this oscillator is sent up to the antenna, thus closing the RF phase locked loop.

4-41 Data Detector

4-42 See FIGURE 4-5 the baseband Data Phase Lock block diagram and FIGURE 5-12 schematic. Also see FIGURE 4-7 for a timing diagram showing T0.0, T4.5, T5.5, T9.5.

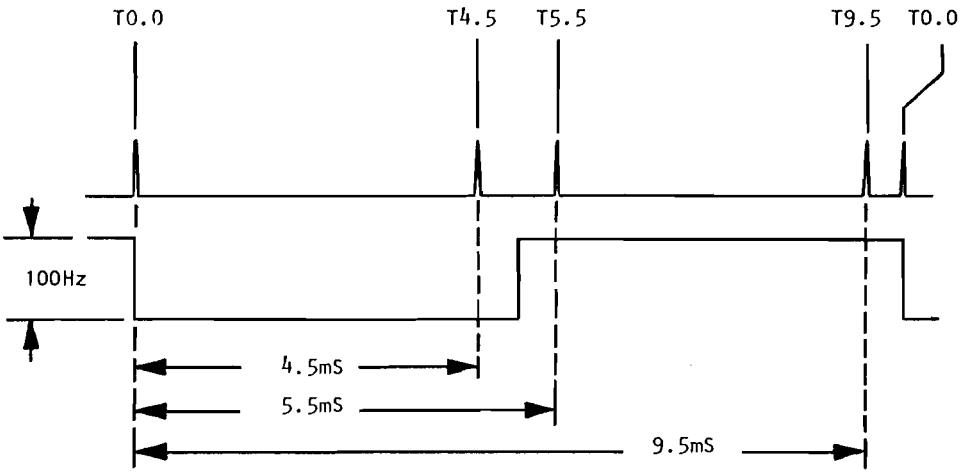


FIGURE 4-7 ANALOG BOARD TIMING

The heart of the data detector is U30 pins 12, 13, 14, the data integrator. Its output is available at TP4. The data integrator is reset by switch U29 pins 6, 8, 9, at the beginning of each data bit time. Its input for the first half of the data bit time is the raw Manchester data, which for a "1", is positive during the first half of the data bit time and negative for the last half. A "0" is negative first, positive last. For the second half of each data bit time, the inverted Manchester data from U28 pin 1 is applied to the data integrator input. Thus, for a "1" the input is always positive, while for a "0" always negative. The resulting data integrator output is a negative going ramp for a "1" and a positive going ramp for a "0". FIGURE 4-8 shows the data integrator output on the top line, and the raw Manchester data on the bottom.

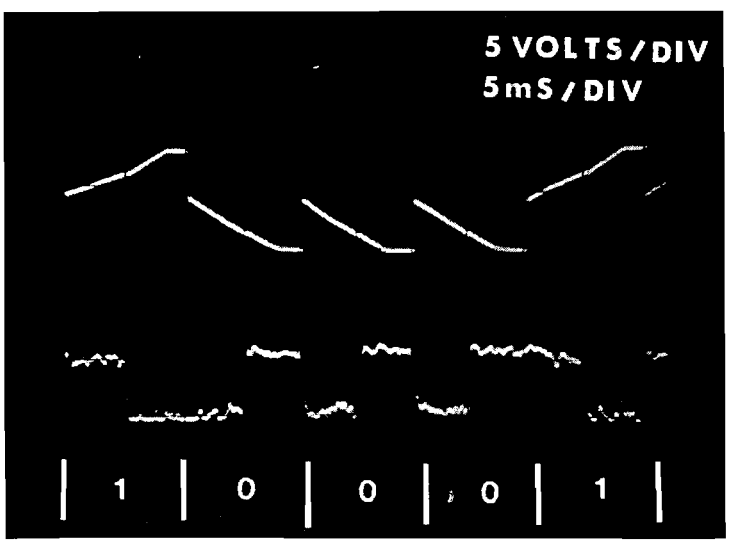


FIGURE 4-8 DATA INTEGRATOR OUTPUT

4-43 The data integrator output is sliced by U30 pins 1, 2, 3, and sampled near the end of the data bit time by U26 pins 3, 4, 5 together with C34 and U30 pins 5, 6, 7.

4-44 U24 inverts the sample so a "1" is positive, U25 pins 9, 10 buffers the data to the processor and U24 pins 1, 2, 3 provides inverted data for the data phase detectors.

4-45 Data Lock Detector

4-46 There are two slicers operating on the output of the data integrator. They have small opposite offsets so that both have high outputs for zero volts in. U27 pin 7 is high for "1"s, while U30 pin 1 is high for "0"s. These outputs are each anded with a timing pulse, T9.5, near the end of the data bit time and used to sample the output of the data integrator. If the data integrator output is positive at sample time, (data = "0") U26 pins 10, 11, 12 direct the sample to C32, while if the output is negative (then, data = "1") U26 pins 6, 8, 9 directs the sample to C31. Thus C31 accumulates the average final value of the data integrator output for "1"s and C32 for "0"s.

4-47 The diode-resistor networks between each switch and its capacitor serve to weight small (bad) values more heavily than large ones. U27 pins 8, 9, 10 and pins 12, 13, 14 are followers to prevent loading of C31 and C32. U27 pins 1, 2, 3 is a comparator with offset which determine whether the difference between "1"s and "0"s is greater than a threshold value set by R81. If so, D10 is extinguished and the processor is notified via buffer U25 pins 14, 15 that reliable data lock is obtained. (see FIGURE 4-9).

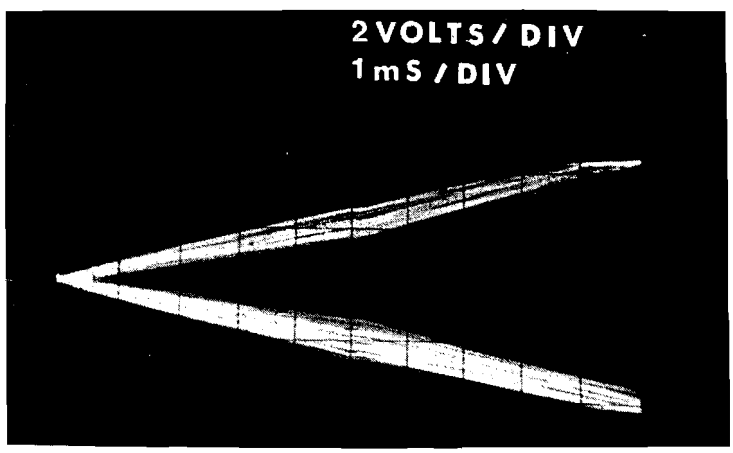


FIGURE 4-9 "CLEAR SIGNAL"

4-48 If the signal-to-noise ratio drops too low, the data integrator output ramps will no longer cleanly separate the "1"s from the "0"s, and the voltages on C31 and C32 will both move in towards zero, eventually causing an out of lock condition to be indicated, if the signal becomes too poor for reliable decoding. (See FIGURE 4-10).

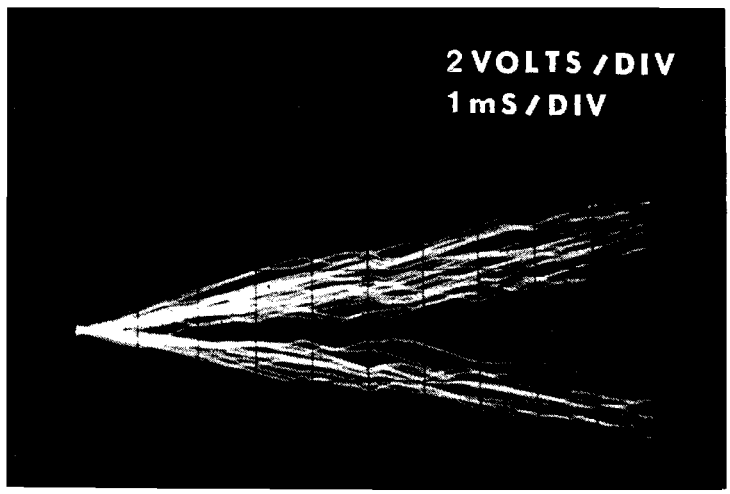


FIGURE 4-10 "POOR SIGNAL"

4-49 If no antenna is connected, the data integrator output is close to zero and both slicers U27 pins 5, 6, 7 and U30 pins 1, 2, 3 have high outputs causing both C31 and C32 to discharge, rapidly causing an out of lock indication.

4-50 Coarse Phase Locked Loop

4-51 The coarse phase detector begins with U28 pins 5, 6, 7 which slices the Manchester data. This improves the phase detector gain a little for weak dignals. Next comes U28 pins 12, 13, 14, an integrator, reset at the start of each bit time, T0.0 by U31 pins 6, 8, 9. The output of this integrator is sampled at T9.5, near the end of the data bit time by U31 pins 10, 11, 12, onto C36. Follower U32 pins 5, 6, 7 minimizes loading while U32 pin 8, 9, 10 provides an inverted version of the sample value. Switches U32 pins 1, 2, 13 and U33 pins 3, 4, 5 select either the sample or the inverted sample, based on whether the data bit was a "1" or a "0". This results in the desired error voltage, proportional to the phase difference between the local data clock and the incoming data.

4-52 When timing is exactly in phase with incoming data, the output of U28 pin 14 is a triangle wave; for a "1",

starting out in a positive direction, than at mid bit turning back negative going, and just reaching zero at end of bit time; a "0" gives the mirror image. Thus when data and clock are in phase, the detector output is OV. See FIGURE 4-11.

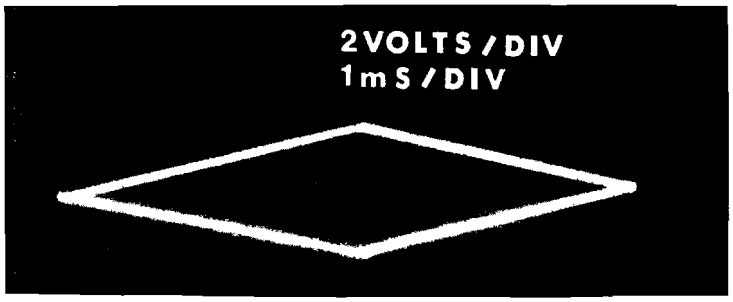


FIGURE 4-11

FIGURE 4-11 Coarse Data Phase Detector Integrator Output (in lock condition)

4-53 If timing is advanced with respect to data, a "1" will contain some contribution from the previous bit, which is un-correlated and provides no average output, so U28 pin 14 will on the average have insufficient time to get back to zero, and a net positive charge will be stored on C36. A "0" will leave a negative charge, for this timing. A data "1" will, however, select the inverted sample for output, while a "0" uses the non-inverted sample; the end result for either case is a negative output for timing advanced with respect to data. A similiar argument shows that for timing retarded with respect to data a positive output results.

4-54 The above argument strictly holds only for the second of two same bits, a bit following its complement produces no net contribution. The coding scheme on the satellite has been designed with this in mind. The complete coarse phase detector characteristic is shown in FIGURE 4-12.

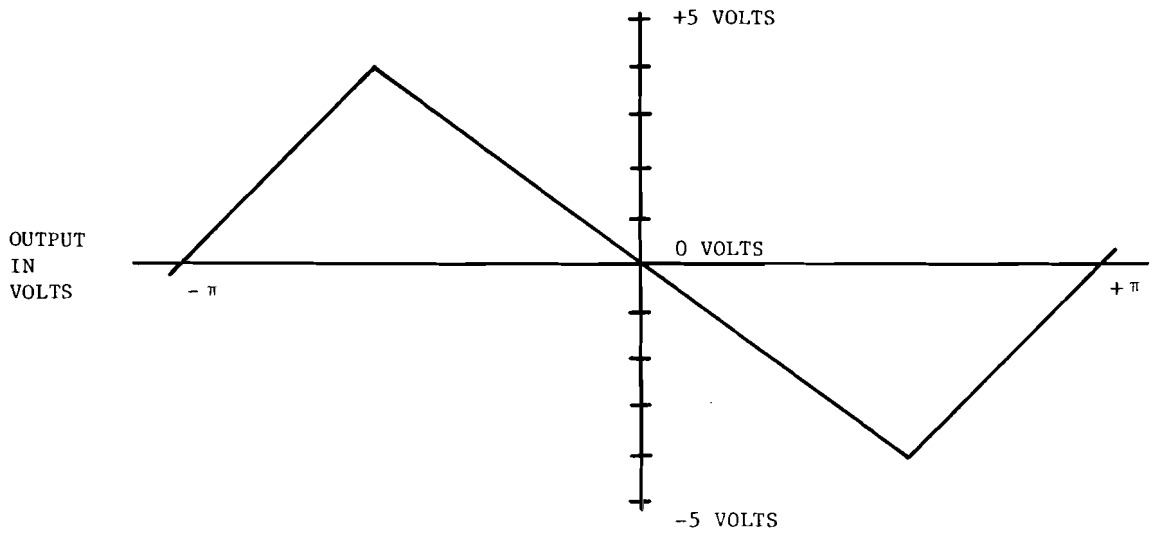


FIGURE 4-12 COARSE DATA PHASE DETECTOR CHARACTERISTIC

4-55 Pins 8, 9, 10 of U4 is the coarse low pass filter. Its output is clamped at zero by the processor via U3 pins 8, 9, 10 and U3 pins 1, 2, 13 until the coarse time-base is selected. This speeds coarse data lock acquisition by guaranteeing an initial frequency close to the correct value. Q1, Q2, D1 comprise the coarse data clock oscillator. It is controlled in frequency by the output of U4 pin 8 and runs at 1MHz±2%. When the coarse oscillator is selected by the processor, it provides all the timing for the analog board and for program execution on the processor board. Selection is controlled via U5 pins 3, 4, 5 and U6 pins 6, 8, 9.

4-56 Fine Data Phase Locked Loop

4-57 The fine phase detector operates similarly to the coarse detector, but with two notable exceptions; it has no slicer at the input, and its timing is such that integration takes place only during the central millisecond of the data bit time. These differences tend to reduce the effects of noise and of op-amp offsets on the systematic sync error; but they also destroy the detector's effectiveness far away from lock. FIGURE 4-12 shows the output of the fine phase detector integrator for many cycles, all superimposed. It is clamped until T4.5 and sampled at T5.5. These times correspond to 4.5 and 5.5 divisions on the scope. The fine phase detector's characteristic is shown in FIGURE 4-13.

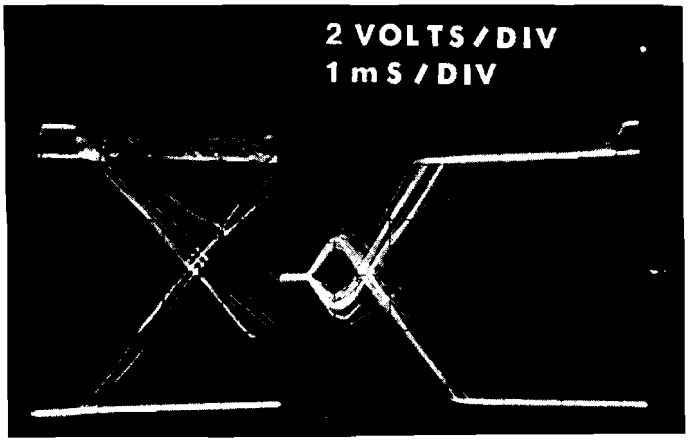


FIGURE 4-13 FINE DATA PHASE DETECTOR INTEGRATOR OUTPUT

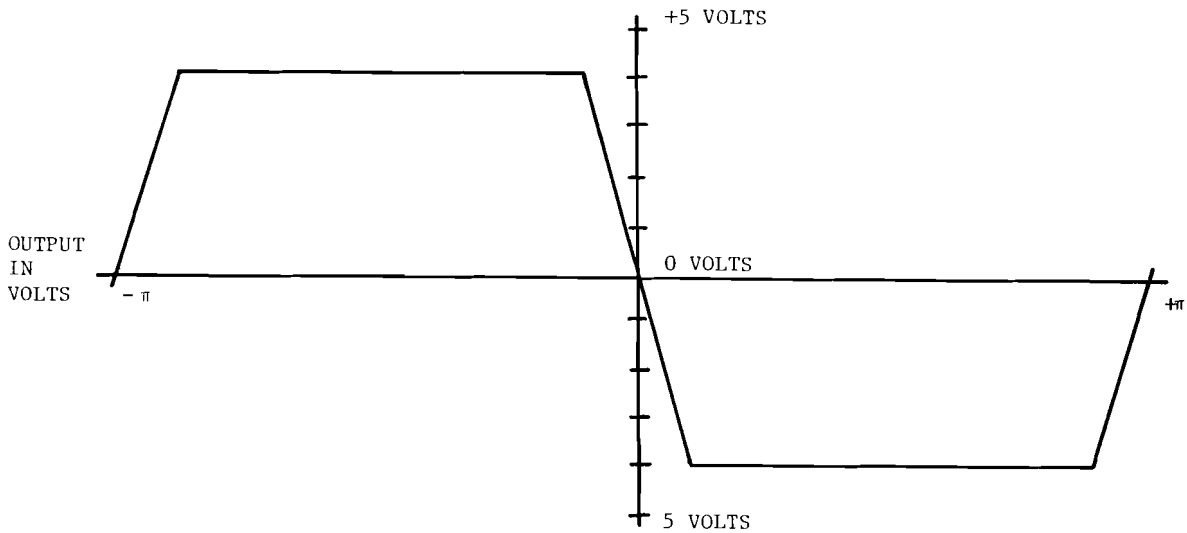


FIGURE 4-14 FINE DATA PHASE DETECTOR CHARACTERISTIC

4-58 The output of the fine phase detector can be applied to the input of the fine PLL low pass filter through U6 pins 1, 2, 13 and U3 pins 10, 11, 12. Opening this switch enables the processor to open the loop and freeze the data clock oscillator frequency at its present value, in case of interference.

4-59 External Oscillator Input (Option)

4-60 As an alternative, the output of the coarse phase detector, or an external input phase detector can be selected as the input to the fine loop via U6 pins 10, 11, 12, or U3 pins 3, 4, 5 respectively. The coarse detector is used to re-acquire data lock after it has been lost. The external input phase detector will be selected during a "freeze" condition, but only if an

external oscillator is connected. This is accomplished by gating in U9 pins 1-10 and Q500 the "External Oscillator" in detector. Q7 pins 8, 9, 12 serves to provide a 50% duty cycle for pins 2, 3, 5, 6 the external input phase detector. U4 pins 12, 13, 14 converts the balanced output of this detector to single ended form. The external input phase detector is edge sensitive and locks to even harmonics of its reference frequency of 10kHz.

4-61 U4 pins 1, 2, 3 with R13, R14, and C10 is the fine loop low pass filter. Its output (available at TP8) is averaged with the fine trim voltage from R17 to control the frequency of the fine data clock oscillator. The fine data clock oscillator consists of Q3, Q4, Y1 and D2. It runs at 10MHz+7PPM, and is divided by two, in U8, to provide 5MHz for the processor and also is divided by ten in U8 to provide 1MHz for the timing chain.

4-62 Timing Chain

4-63 U18 divides whichever 1MHz source is selected by 100 to provide 10kHz. Its output is level shifted by C26, R63 and R64 from 5V/0V levels to ±2.5V levels which drive U19. U19 provides a further division by 10, and provides timing for generation of a stepwise approximation of the 1kHz sinewave carrier, using R107 through R116, used in generation of IRIG B. This stepwise approximation is smoothed and buffered by U100 pins 12, 13, 14 and then modulated by the processor using U102 pins, 1, 2, 13, R104 and R105. This modulated code is buffered by U100 pins 1, 2, 3 and U100 pins 5, 6, 7 for output.

4-64 If level shift code is desired output transistor Q100 provides TTL signal levels. One kHz timing for the processor also comes from U19. This is the basic timing for all processor activity. This output, along with all other outputs to the processor, is buffered by U21.

4-65 U20 divides the 1kHz output of U19 by ten to provide the 100Hz timing for the processor and also, with U21, timing for data lock and detection circuitry.

4-66 DIGITAL BOARD ASSEMBLY 86-42

4-67 See SECTION 5-16 for schematic of the digital board. The digital board utilizes a M6802 microprocessor as the central processor. The processor controls data flow over a multiline bus in a typical microprocessor configuration as a controller, stored program memory, read wirte data memory, and input/output interface. U2, U3, U4 are the I/O interface devices. All communications

with the other areas flow thru them. U12, U13 are type 2114 rams and comprise the read/write memory used for storage of program variables. U5, U6, U8, 2716 eproms, are used for program storage. U9, U10, U11, U15, TTL, MSI chips perform address decoding to direct data flow to and from the proper devices. U14 generates a reset pulse to ensure orderly start of operating at turn on.

4-68 The function of the 86-42 board is determined within a wide range, by the program stored in U5-U8. It is beyond the scope of this document to describe in detail the operation of this program, however, a general outline is provided in the software section to aid in understanding of the clock's behavior.

4-69 POWER SUPPLY ASSEMBLY 86-52

4-70 See SECTION 5-31 for schematic of power supply assembly.

4-71 The power supply itself is a standard design and needs no explanation.

4-72 The reset circuit, U6, senses ripple on either of the +5V supplies and generates a negative going pulse which goes to the reset flip-flop on Assembly 86-42, forcing a program reset as long as ripple is resent on either +5V line. This protects against erratic operation during times of low line voltage.

4-73 DISPLAY BOARD ASSEMBLY 86-43

4-74 See SECTION 5-19 for schematic of display board assembly. The display board provides a visual display controlled by the processor. The display is multiplexed by pairs of digits. A given pair is selected by the processor via Q1-Q10 driving the anode to +180V. At the same time, the desired digits are presented in BCD to the decoder-drivers, U1 and U2. Unblanking, colon, and satellite LED indicator drives are encoded and latched by U5 as the absent left hand digit of the pair of digits of which the 100's of days is the right hand digit.

4-75 PARALLEL OUTPUT OPTION ASSEMBLY 86-44

4-76 See SECTION 5-22 for schematic of Assembly 86-44. The parallel output option provides logic level output of the same time as shown on the display. It does this

by demultiplexing the display data lines and latching the data in a buffer consisting of U19-U23. On the second, the data in this buffer is strobed into the output buffer, U10-U18. The data in the output buffer is sent to the outside world thru drivers U1-U9 to provide increased drive capability.

4-77 A millisecond counter, U31-U33, together with drivers U28-U30, provide milliseconds output, and also control loading of time into the output buffer. This counter is synchronized with NBS time via the "time ok" line thru trigger latch U35.

4-78 The function of U37 and its associated circuitry, is to provide either an edge or a level for controlling sampling of the BCD output lines. U36 is an output driver for several miscellaneous outputs. A timing diagram, showing the relationship of the 1 KHZ line to the data output lines is shown in SECTION 3, to assist in reading the lines during the time when they are stable.

4-79 RS 232 INTERFACE ASSEMBLY 86-46

4-80 See SECTION 5-25 for schematic of Assembly 86-46. U1, a Motorola MC6850 ACIA, handles the conversion between processor bus data and serial data. U4 and U5, line driver and receiver type 1488 and 1489 respectively, convert between NMOS and RS232 signal levles. U6, a Motorola MC 14411 BAUD rate generator with Y1 provides an assortment of clock rates, one of which is selected by S2 to drive the ACIA. U3, a 74LS138 decodes addresses, to direct information flow, while U2, an 81LS96, permits reading of the option switches, S1.

4-82 Use of this option is covered in SECTION 3-66.

4-83 IEEE-488 INTERFACE ASSEMBLY 86-47

4-84 See SECTION 5-28 for schematic of Assembly 86-47. The IEE-488 (GPIB, HPIB) interface uses U1, a Motorola MC68488 GPIA, to handle the handshaking and other bus management activities. Interface to the bus is thru U4-U7, MC3448 bus tranceivers, with U4, a 74LS138, provides address decoding, while U2, an MC6821, allows reading the device address switches, and sending and receiving external triggers.

4-85 Use of the option is under program control and is described separately. See SECTION 3-98.

4-86 SOFTWARE

4-87 PROGRAM DESCRIPTION

4-88 The Model 468-DC program can be divided into three broad areas. All of course being controlled by the microprocessor on the Assembly 86-42.

1. Control of the receiver and processing of satellite data
2. Generation of the various timing outputs
3. Communications via an optional interface board (RS-232 or IEEE-488)

4-89 RECEIVER CONTROL AND DATA PROCESSING

4-90 Receiver control can be considered as three levels of synchronization:

Synchronization to the RF carrier
Synchronization to the 100HZ data rate
Synchronization to the transmitted time code

There is no clean division between synchronization to the time code and decoding the time. Each level of Sync is contingent on the preceding levels. A series of state diagrams attempts to describe these levels. See FIGURE 4-15 and 4-16.

4-91 DESCRIPTION OF THE STATE DIAGRAMS

4-92 The state diagrams present a view of the internal states of the program along with the conditions for transitions between the states. Also shown are the external effects of the internal states. A state definition is represented by information enclosed by a line. The format is:

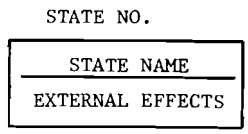


FIGURE 4-15 STATE DIAGRAM

Transitions between states are represented by lines connecting two states with an arrow indicating the direction of the transition and with the condition causing the transition indicated alongside the line.

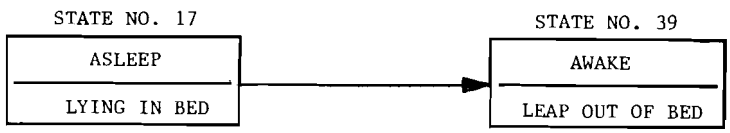


FIGURE 4-16 STATE DIAGRAM

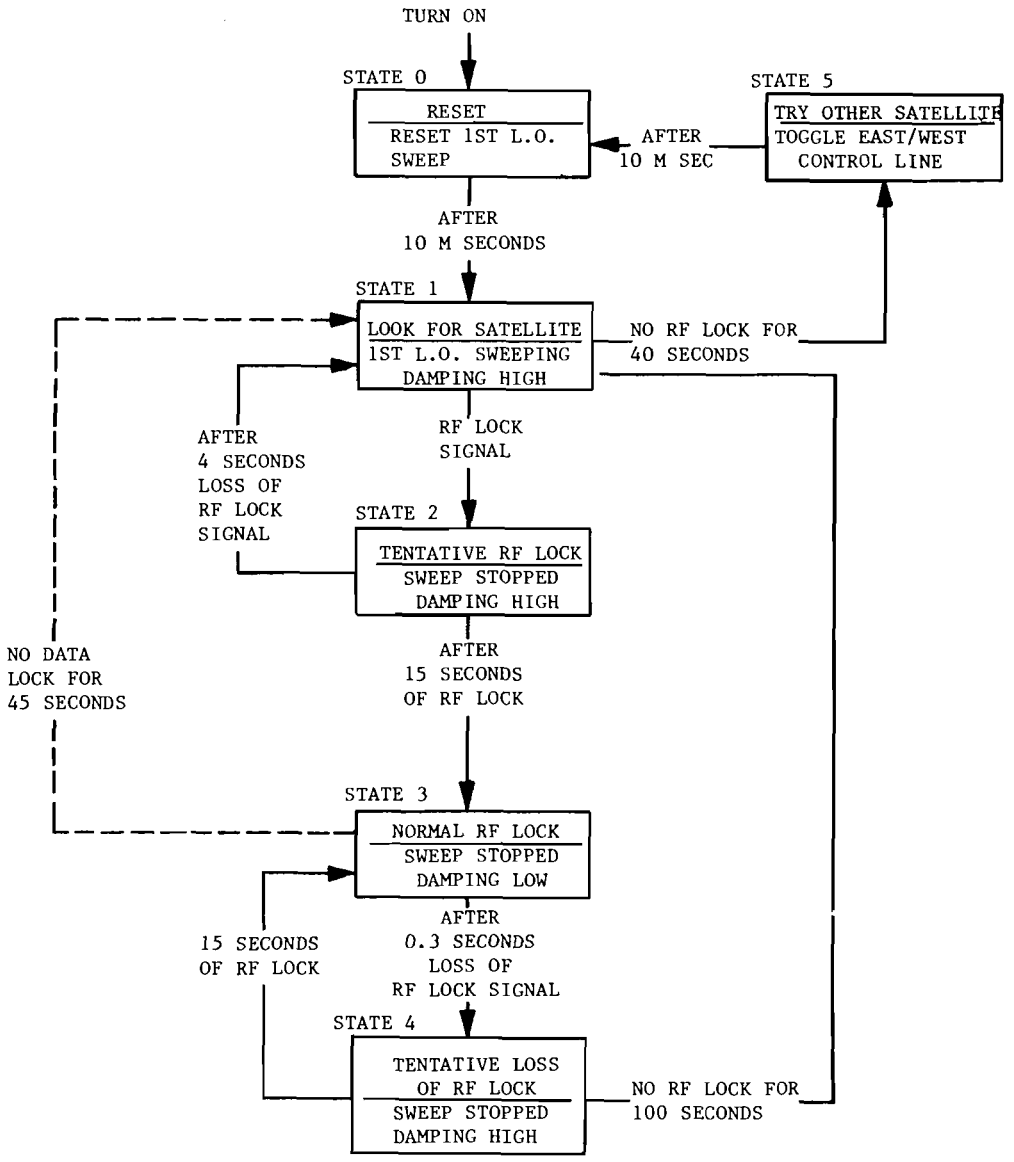


FIGURE 4-17 RF LOCK STATE DIAGRAM

4-93 Normally, the clock will start at state 0 and quickly pass to state 1. RF lock will be obtained usually in about 20 seconds, causing a transition to state 2, which allows the RF lock loop to stabilize. Fifteen seconds later, state 3 will be entered, and normal operation proceeds.

4-94 The reverse linkages in the diagram are there to recover from problems that may arise, primarily interference by land mobile service. The link from state 3 to state 1 prevents lock to unmodulated carriers. State 4 faciliates RF lock after a short burst of interference.

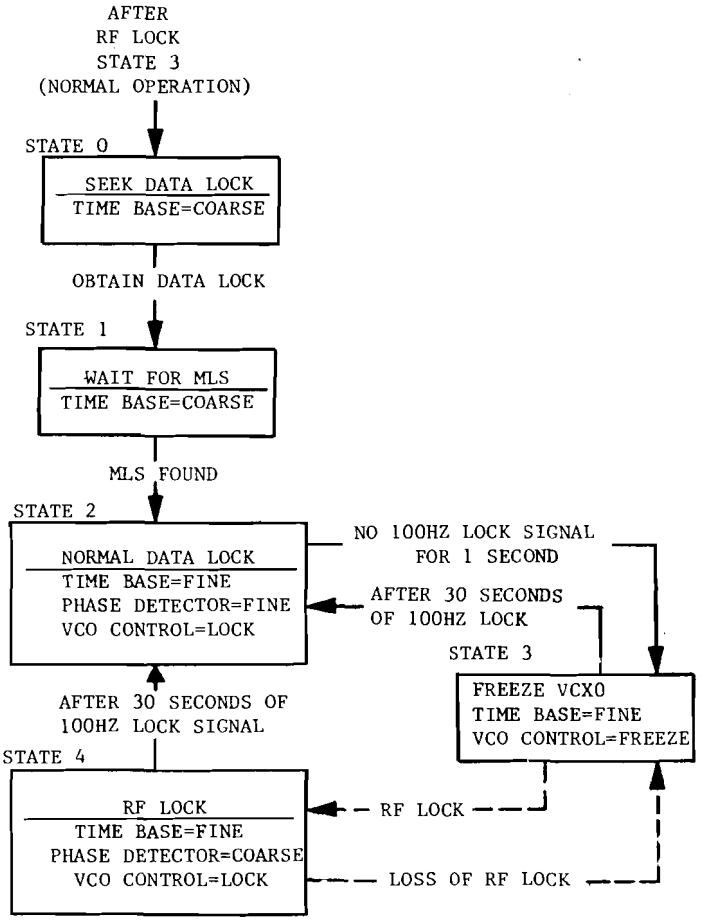


FIGURE 4-18 100HZ DATA LOCK STATE DIAGRAM

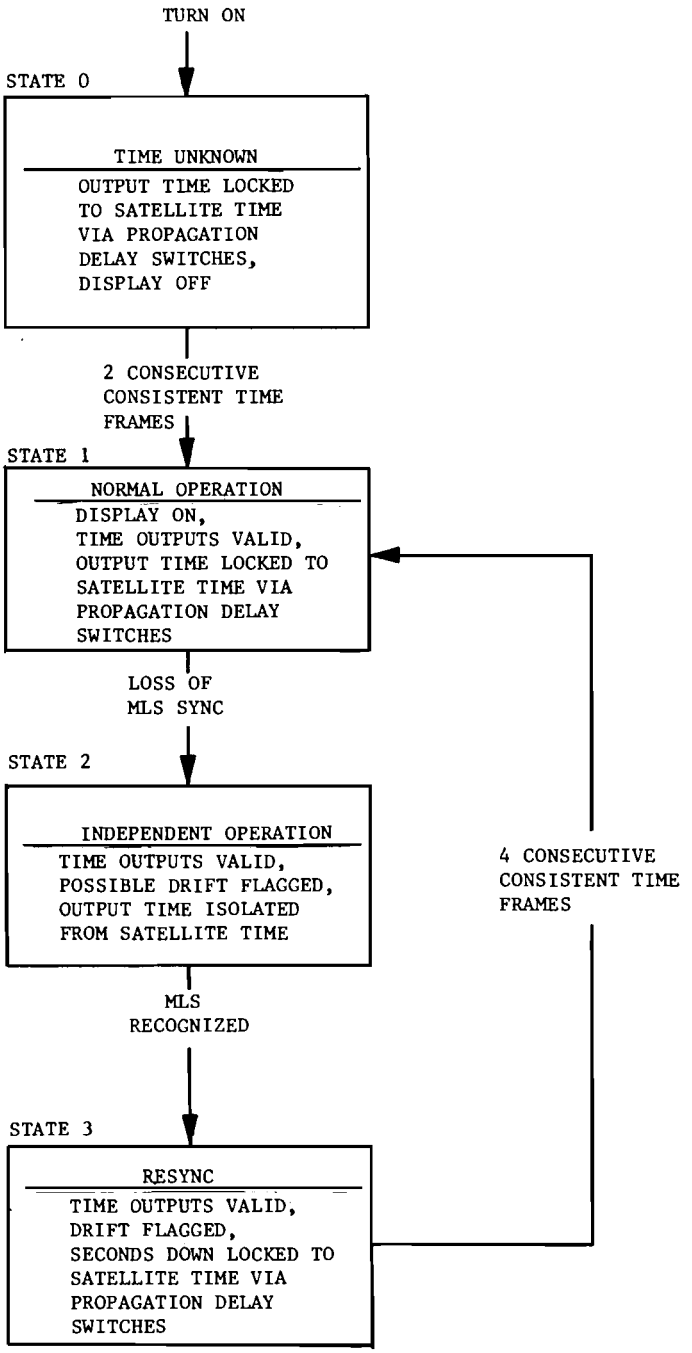
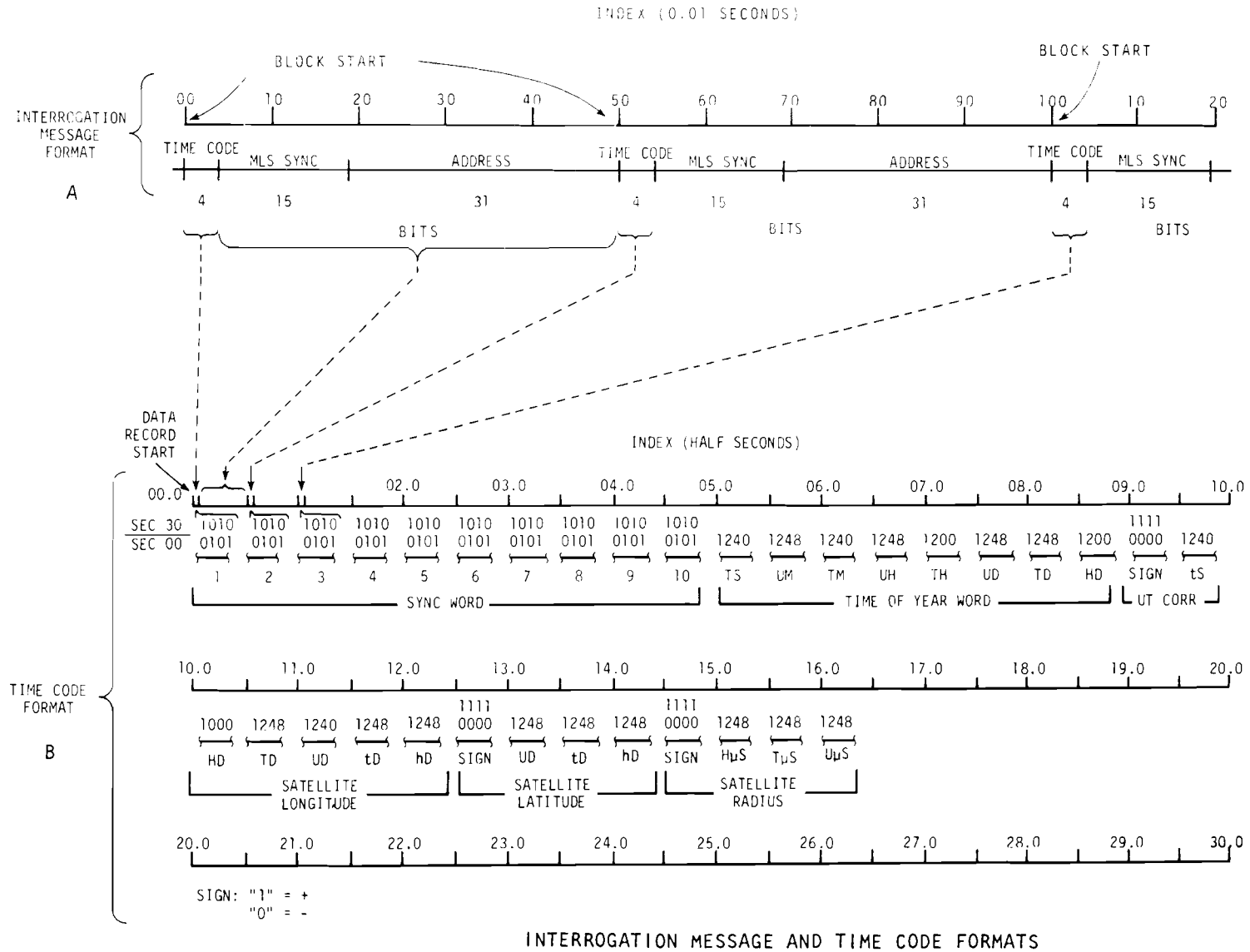


FIGURE 4-19 FRAME SYNC CONTROL STATE DIAGRAM

4-95 Understanding of FIGURE 4-18 and 4-19 will be faciliated by reference to FIGURE 4-20, which is a description of the format of the satellite signal.



INTERROGATION MESSAGE AND TIME CODE FORMATS

FIGURE 4-20 INTERROGATION MESSAGE AND TIME CODE FORMATS FROM N.B.S. TECHNICAL NOTE 681

4-96 State 0, is entered a few seconds after normal RF lock is attained. The detection of MLS is an almost certain indication that lock to a functioning satellite has been obtained. There is no return to state 1, so the coarse timebase will not be used again.

4-97 When interference causes loss of lock during normal operation, state 3 is entered, freezing the timebase oscillator at its present frequency (or switching to an external timebase if one is provided). State 4 permits relock to the data after protracted loss of data lock has caused the timebase to drift out of the acquisition range of the fine data phase detector.

4-98 In state 0 at turn on "output time" commences from zero, indicating elapsed time, but is not displayed on the front panel. When two successive time frames agree, this time replaces the elapsed time, the time quality flags are brought low, and the display comes on.

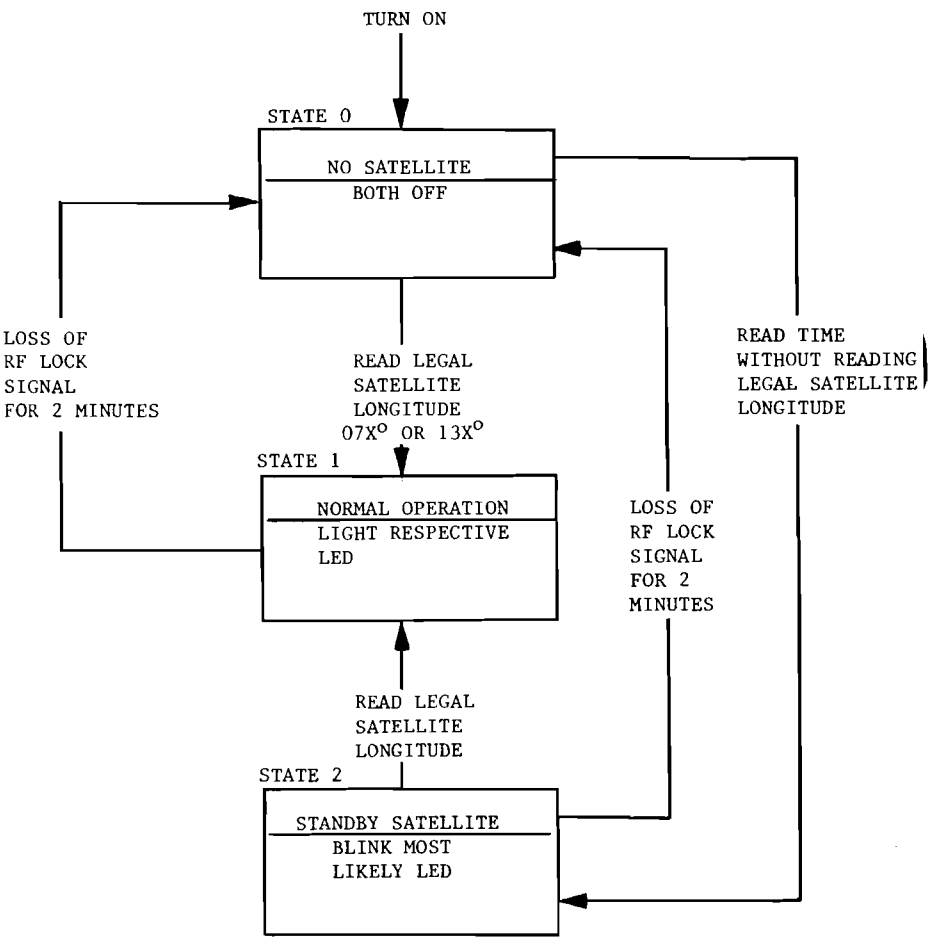


FIGURE 4-21 SATELLITE LED STATE DIAGRAM

4-99 If satellite signal is lost, output time continues to update via the internal (or external) timebase. Meanwhile the clock searches for the satellite signal and resyncs to it without affecting the output time. This independence is achieved by not applying the propagation delay correction while in mode 2 unless the switch setting is changed. Since the timebase oscillator must still gain phaselock with the data, a slow drift of up to five milliseconds can occur during this time.

4-100 Once data lock is re-established, no further adjustments to the output time will occur until four (4) consecutive frames agree. At this point the time quality flags go low and a time jump of an integral number of milliseconds can occcur, to bring output time in sync with the new frame. Resync to the time frame requires four consistent frames to reduce the probability of incorrect time during adverse conditions.

4-101 The satellite LEDS are controlled by the received satellite longitude data. A position between 70 and 79 degrees west will light the east LED, while 130 to 139 degrees west lights the west LED.

4-102 A blinking LED indicates time lock without a legal longitude. The commonest cause of this condition is reception of the backup satellite at 105 degrees west during problems with one of the main satellites. East or west blinking merely indicates which sweep the processor is attempting, if the manual override switch on the analog board is in effect no significance attaches to which of the two LEDS is blinking.

4-103 TIMING OUTPUTS

4-104 The timing outputs under software control are:
One Hertz
Slow code
60 Hertz
IRIG B
IRIG H (optionally)

4-105 One Hertz, the slow code, and 60 Hertz are all present beginning at power on. The IRIG time code outputs start after NBS time has been acquired. The IRIG B time code transitions are within 40μSEC. of the data clock, the other outputs may lag by up to 300μSEC. This difference arises from the fact that the IRIG B output is precomputed and output immediately after the data clock interrupt occurs, while the others are output as they are computed during the interrupt service.

4-106 Operation of the communications options, RS-323C and IEEE-488 are described separately. The program controlling these options runs with lowest priority on the 1kHz interrupt, so there may be up to 300μSEC. jitter in these outputs.

4-107 MAINTENANCE, MODEL 468-DC

4-108 Equipment needed:

1. RF Sweep Generator---HP8601A or equivalent
2. Oscilloscope---------1MHz or greater bandwidth
3. Digital voltmeter----Greater than 10 meg.Ω input impedance
4. Frequency counter----Fluke 1900A or equivalent
5. Spectrum analyzer----HP 8558B/182T or equivalent

4-109 The Model 468-DC has been designed to provide maintenance free operation. The main instrument contains only seven adjustments, most of which will never require resetting. They are:

1. Third IF trim, a ceramic trimmer capacitor on Assembly 86-73, C9.
2. Data symmetry, a trimpot on Assembly 86-74, R45.
3. East sweep trim, a trimpot on Assembly 86-74, R38.
4. West sweep trim, a trimpot on Assembly 86-74, R37.
5. 10 MHz fine timebase trim, a trimpot on Assembly 86-74, R17.
6. 1 MHz coarse timebase trim, a tunable coil on Assembly 86-74, L1.
7. First L.O. peaking, a tunable coil on Assembly 86-74, T1.

4-110 THIRD IF TRIM, ASSEMBLY 86-73

The sweep generator and the scope are needed for this adjustment which sets the third intermediate frequency to the center of the passband of the 4.5 MHz crystal filter T1, Y1, Y2, etc.

4-111 Connect the sweeper RF output through a blocking capacitor (0.1 UF) to the antenna input BNC. Set up the scope so the sweep output gives full scale horizontal deflection connecting the X axis to the sweep output, and 2V to 5V gives full vertical deflection. Connect the scope vertical input to TP3 on Assembly 86-74, the Analog Board. Set the sweeper to 4.500 MHz, 10kHz sweep width, about 5 sweeps per second sweep rate, and -40dbm output level. A faster sweep rate will distort the picture.

4-112 The display should appear as in FIGURE 4-22. The zero beat must occur in the center of the filter passband. If the zero beat is outside the -3db points, C9 on Assembly 86-73 must be adjusted to bring it back into the center. This adjustment also affects receiver delay by up to 100μSEC.

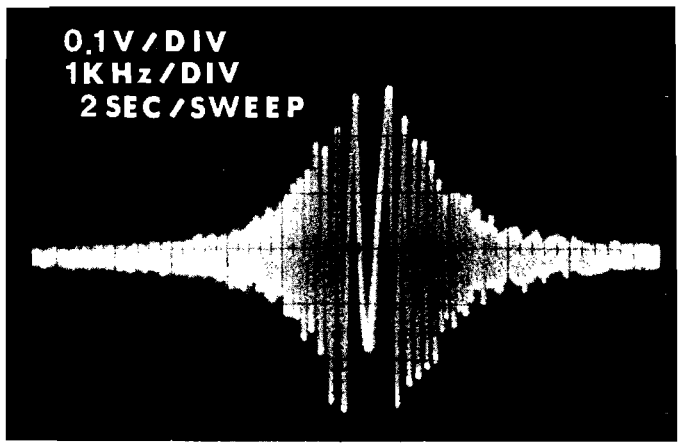


FIGURE 4-22 THIRD LOCAL OSCILLATOR ADJUSTMENT

4-113 Data Symmetry Adjustment, Assembly 86-74

4-114 To adjust data symmetry, R45, the clock must be locked to a satellite. Connect the voltmeter to TP3, on Assembly 86-74 (see SECTION 5-11). A 6 second lowpass is helpful for this adjustment. The FIGURE 4-23 shows the low pass filter which can be used. Adjust R45 Assembly 86-74, for 0±0.2V. This adjustment also affects receiver delay up to 100μSEC.

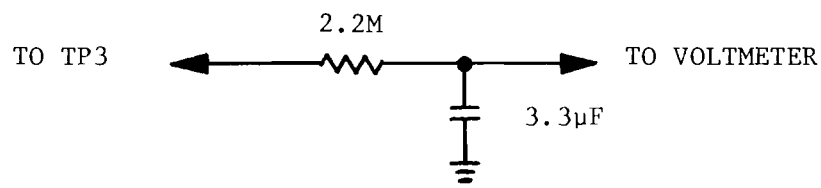


FIGURE 4-23 "LOW PASS FILTER"

4-115 East Sweep Trim, Assembly 86-74

4-116 Connect the frequency counter to the antenna input BNC (after removing the sweeper). Ground TP6 on the Analog Board Assembly 86-74 and select the east satellite with S2 (labelled "E"). Adjust R38, the center of the three-in-a-row trimpots, for a frequency of

18,642,230±50Hz. See SECTION 5-11 for parts location of TP6, R38 and S2.

4-117 West Sweep Trim, Assembly 86-74

4-118 Select the west sweep with S1 (labelled "W") and adjust R37 for a frequency of 18,642,700±50Hz.

4-119 10 MHz Fine Timebase Trim, Assembly 86-74.

4-120 Ground TP8, attach the counter to TP12. Adjust R17 for 10,000,000±10Hz (1 PPM). See SECTION 5-11 for parts location.

4-121 1 MHz Coarse Timebase, Assembly 86-74.

4-122 Ground the coarse oscillator control voltage at TP13. Connect the counter TP11. Adjust L1 (the can nearer the front of the instrument) for 1.000MHz ±.001MHz.

4-123 First Local Oscillator Peaking, Assembly 86-74

4-124 If a spectrum analyzer convering 18-40 MHz with 50ΩAC coupled input is available, see 4-125 if not, 4-126.

4-125 Connect the spectrum analyzer to the antenna input BNC connector. Tune T1 (the can near the back of the instrument) to minimize 37.3 MHz output while maximizing the 18.64 MHz output. The 18.64 MHz component will be about +15dbm, the 37.3MHz component about -15dbm.

4-126 If no analyzer is available, make a dummy load using a 50Ω resistor in series with a 0.1uF capacitor (see FIGURE 4-26). Connect this load to the antenna input BNC. Look at TP1 with a scope capable of responding to 20MHz and tune T1 for maximum output.

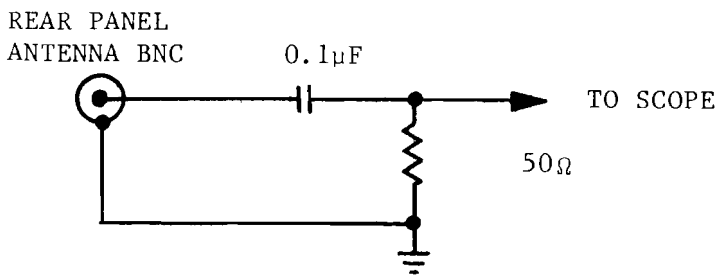


FIGURE 4-24 50 Ω DUMMY LOAD

4-127 TROUBLESHOOTING

4-128 No exhaustive troubleshooting tree has been prepared. It is believed that a more effective approach is to give some hopefully useful hints to be used in conjunction with the Theory of Operation Section. The circuitry in the instrument is relatively straightforward. Interaction with the program may vary with the options supplied. Therefore, in case of trouble:

4-129 First, make sure that suitable power is supplied to the instrument (fuse, switch).

4-130 Second, verify that an antenna is connected and that it has a relatively clear view of a satellite. (Trees can obstruct the signal, as will buildings). A DC voltmeter should read approximately +12V at the antenna end of the lead in coax.

4-131 In some location, land-mobile service interference on the west satellite frequency greatly delays time acquisition. Try the east.

4-132 When the clock is first turned on, the colons should blink; on one second, off one second etc. If they don't, the program is probably not running. Take the cover off. Check that all connectors inside are making proper contact. With no antenna, both unlock LED's on the analog board should be lit.

4-133 At this point check all eleven power supply voltages:
On the digital board--two +5V, one -5V, one+12V, one -12V.
On the analog board---+12V, +8V, two+5V, one-6V.
On the display board--+180V (Red Wire).

4-134 If the processor board is running, as evidenced by blinking colons, go to 4-139: if not: 4-135.

4-135 Check for 1kHz interrupt at U4 pin 19 on the processor board. If none present, look for trouble in the timing chain on the analog board.

4-136 Check that the processor clock on U1 pins 38 and 37 are present at 5.0 and 1.24 MHz respectively.

4-137 Check that reset, pin 40, is low for a fraction of a second at turn-on, then goes cleanly high and stays high.

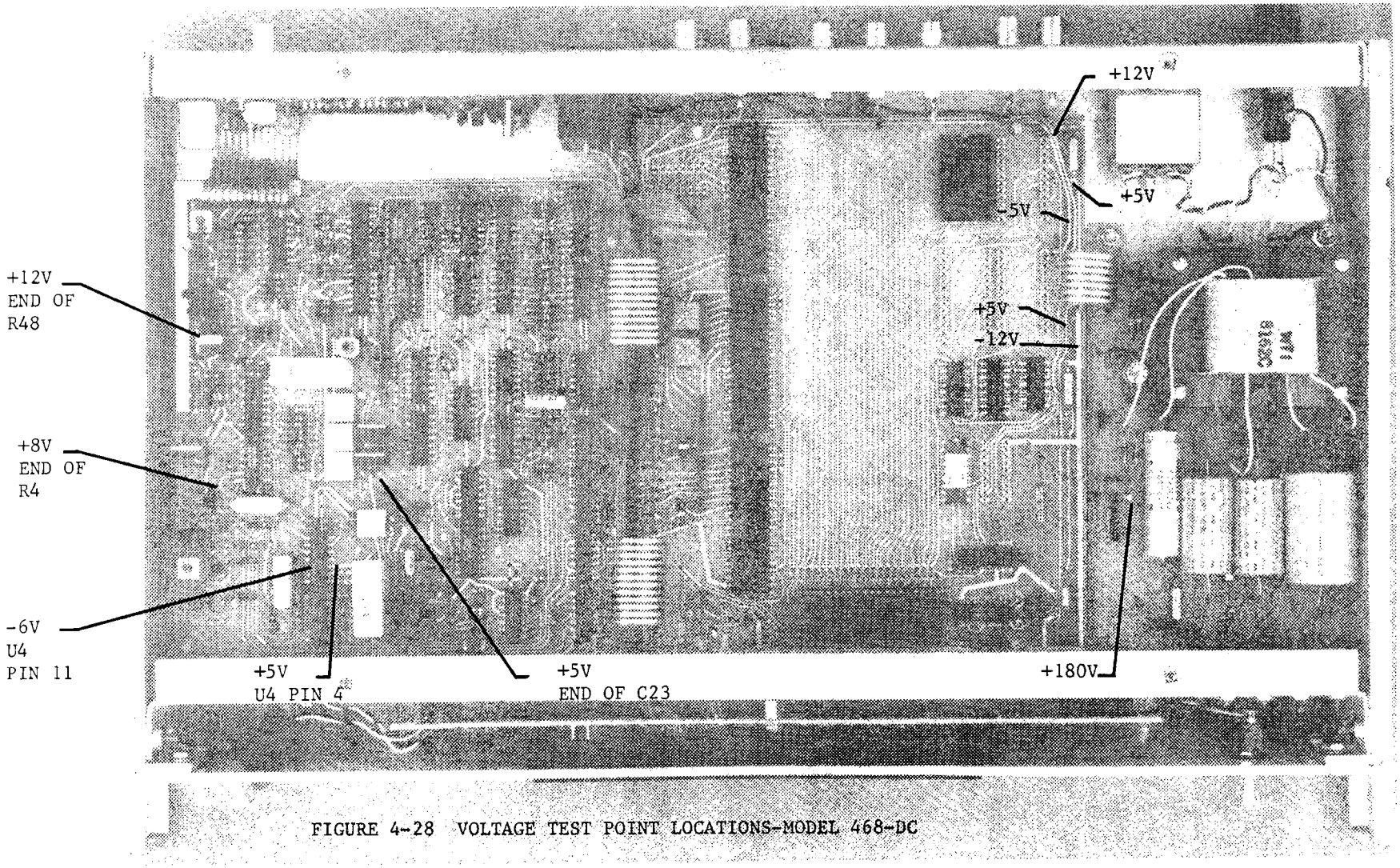


FIGURE 4-28 VOLTAGE TEST POINT LOCATIONS-MODEL 468-DC

4-138 Wiggle the socketed chips in their sockets.

4-139 If the program is running, but no time comes on the display after a few minutes, look at or listen to J2 on the analog board.

4-140 At turn on there should be a few volts of audible noise present. You can easily see/hear the satellite signal as the receiver sweeps to it and locks. A marginally weak signal is hard to discern on the scope but easily audible on the speaker. Listen to the cassette tape supplied with the clock. A cassette tape of typical signal and interference condition with earphone is available from the factory for this checkout. Contact True Time directly for this tape and earphone set. If no signal is present there is probably a problem in the antenna. If a strong signal is observed, the antenna is ok, and the problem is probably on the analog board, see SECTION 4-153.

4-141 If the antenna appears to be malfunctioning, and you don't want to return it to the factory, it is possible to open and check it. To open the antenna, cut the silicone rubber seal around the edge of the plastic bubble, then take out all 16 screws around the bubble. Now, gently pry off the bubble and take the flat plate antenna off the metal box, too. You should be looking at the 86-70/71 and 86-72 boards.

4-142 If the green LED is lit and the red LED is not, the 86-70/71 board is probably ok. Also if no noise was apparent at TP3 on the analog board, the problem is likely on the 86-72 board.

4-143 Use of an RF sweeper greatly eases diagnosis and treatment of the 86-72 board.

4-144 Remove one end of the coax that runs between the balanced mixer on the 86-70/71 board and the input of the 86-72 board. Ground the AGC line on the 86-72 board. (end of R32 near edge of board).

4-145 Inject 21.4MHz into the input of the 86-72 board through the coax whose other end you just lifted. Sweep width 100kHz, sweep rate 5/second, level sufficient to provide 1V peak response at TP2. You should get a nicely rectangular passband 13kHz wide with about -47dbm (1mV) in.

4-146 If that's ok, look at TP1. Here you should get a similar passband with about -57dbm (.3mV) input. If the second L.O. isn't running no signal will be observed here.

4-147 If gain is ok to TP1, check the last two 4.5MHz stages by looking at signal strength output on terminal #6. With no signal and with AGC still grounded, it should be 0V. Removing the AGC ground should bring that up to about 2V, noisy.

4-148 If all the above is ok, the 86-72 board is working, if not, the trouble has been located.

4-149 If the problem is on the 86-70/71 board, it can be isolated by reference to the voltage chart FIGURE 4-26. If normal operation cannot be obtained by replacing defective transistor, it is recommended that the unit be returned to the factory for repair, since tuning of the UHF circuits on these boards is critical and interactive. To use FIGURE 4-26, it is necessary to disable the ALC on the multiplier chain. Do this by grounding R27 at the end away from TP6.

Supply volts = 12.0
18.64 MHz Level = +12dbm

Point	Voltage	Tolerance
TP1	+2.5V	0.5V
TP2	+2.5V	0.5V
TP3	+0.7V	0.2V
TP4	+0.5V	0.2V
TP5	+2.3V	0.5V
TP6	+0.5V	0.2V
Q1 Collector	+12V	0.5V
Q1 Base	+2.5V	0.2V
Q1 Emitter	+2.0V	0.2V
Q2 Base	+1.2V	0.2V
Q2 Emitter	+0.25V	0.2V

FIGURE 4-26 - ASSEMBLY 86-71 VOLTAGE CHART

4-150 To continue, you will need the sweeper and spectrum analyzer.

4-151 Inject 18.64 MHz, sweep width 1MHz, level 0dbm into the multiplier input. First check the input bandpass filter. It should show a slightly overcoupled response about a third of a MHz wide. Next look successively at the emitter current test points for the multiplier

stages. Adjust each stage for widest peak of emitter current in the succeeding stage. Then adjust the trimmer capacitors in the 447MHz filter for widest levelled response at TP6. Use of a spectrum analyzer is almost imperative to avoid the possibility of spurious responses, and also to locate the approximate positions for the filter trimmers, if they are far out of adjustment.

4-152 Troubles on the detector board Assembly 86-73 will show up as loss of signal going one direction or the other, and as mistuning of the third L.O., covered under maintenance.

4-153 Troubles on the analog board generally are due to op-amp outputs being stuck high or low, or analog switches latching up or leaking excessively. These kinds of problems can often be isolated by feeling the IC's for hot ones and by looking for stuck op-amp outouts with inputs inconsistent with the output state. Refer also to the "Theory of Operation" section for description of proper waveforms on the test points.

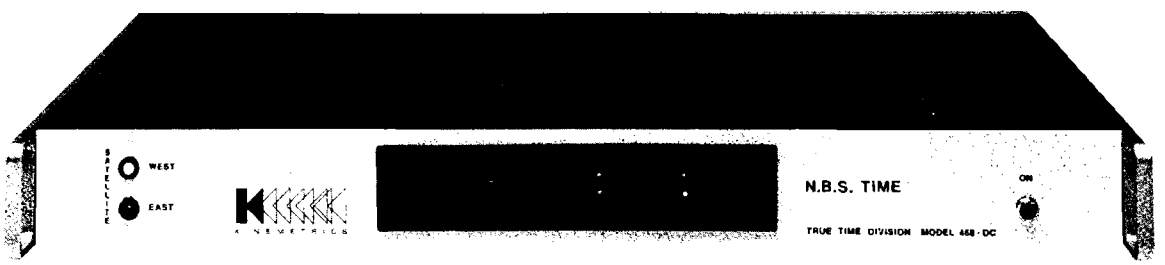
4-154 Troubleshooting the External Oscillator option

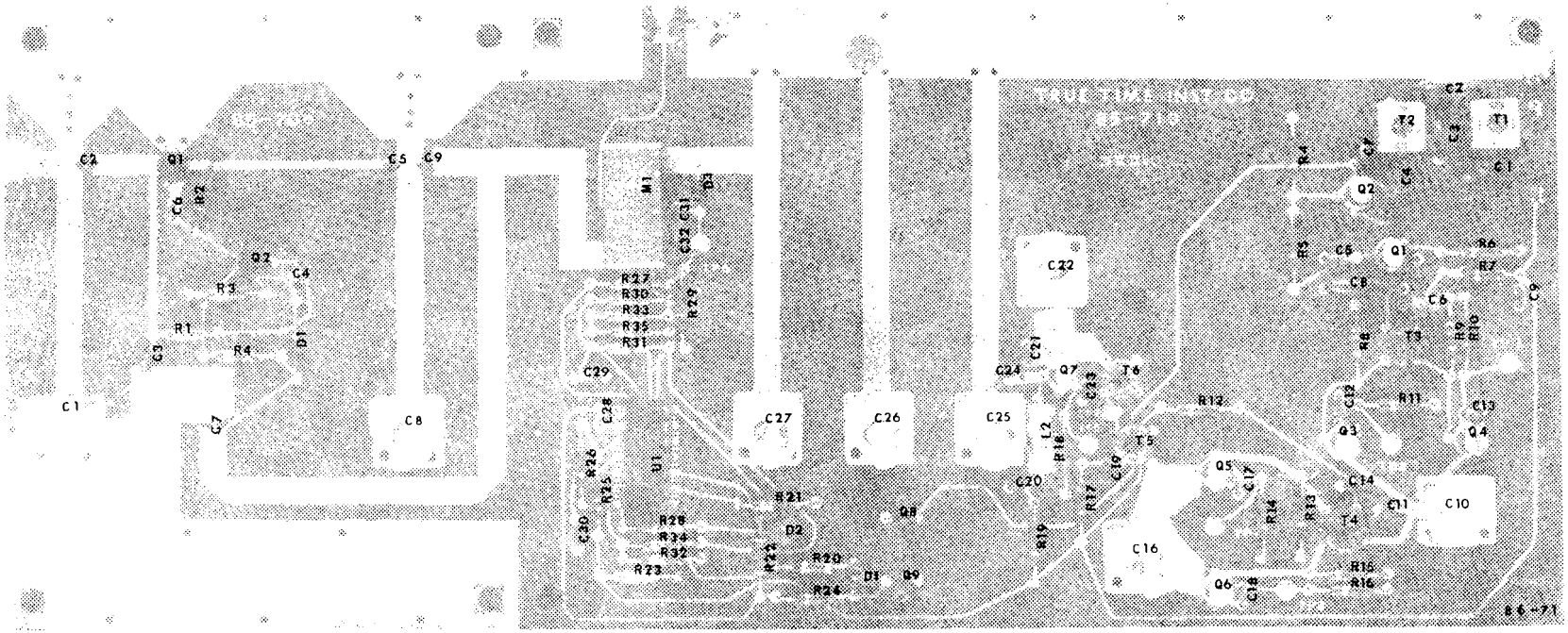
4-155 If D500 won't light when the external oscillator is connected, look at U7 pin 9. You should see approximate TTL levels at half frequency. If D500 lights, but the clock doesn't appear to lock to the external oscillator when the antenna is pulled, check for drift between the waveforms at U7 pin 3 (10 kHz) and U7 pin 8 (ext/2). Also check that U3 pins 5 and 12 both go high.

SECTION V

SCHEMATIC AND PARTS LISTS

MODEL 468-DC





5-2 SYMBOL DESIGNATION REFERENCE 86-70

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	34-2	Cap. Air Variable 2-10pf
C2	36-18	Cap. Monolithic 27pf
C3	36-58	Cap. Monolithic 1000pf
C4	36-58	Cap. Monolithic 1000pf
C5	36-18	Cap. Monolithic 27pf
C6	36-58	Cap. Monolithic 1000pf
C7	36-58	Cap. Monolithic 1000pf
C8	34-2	Cap. Air Variable 2-10pf
C9	36-18	Cap. Monolithic 27pf
D1	55-1	Diode, 1N5231
J1	381-2	Connector, Jack, Right Angle
PWB	85-70/71	Printed Wiring Board
Q1	175-901	Transistor MRF 901
Q2	175-4	Transistor MPS 3702
R1	2-107	Resistor Carbon 27K
R2	2-49	Resistor Carbon 100Ω
R3	2-97	Resistor Carbon 10K
R4	2-71	Resistor Carbon 820Ω

Note: All resistors are 1/4W ± 5%

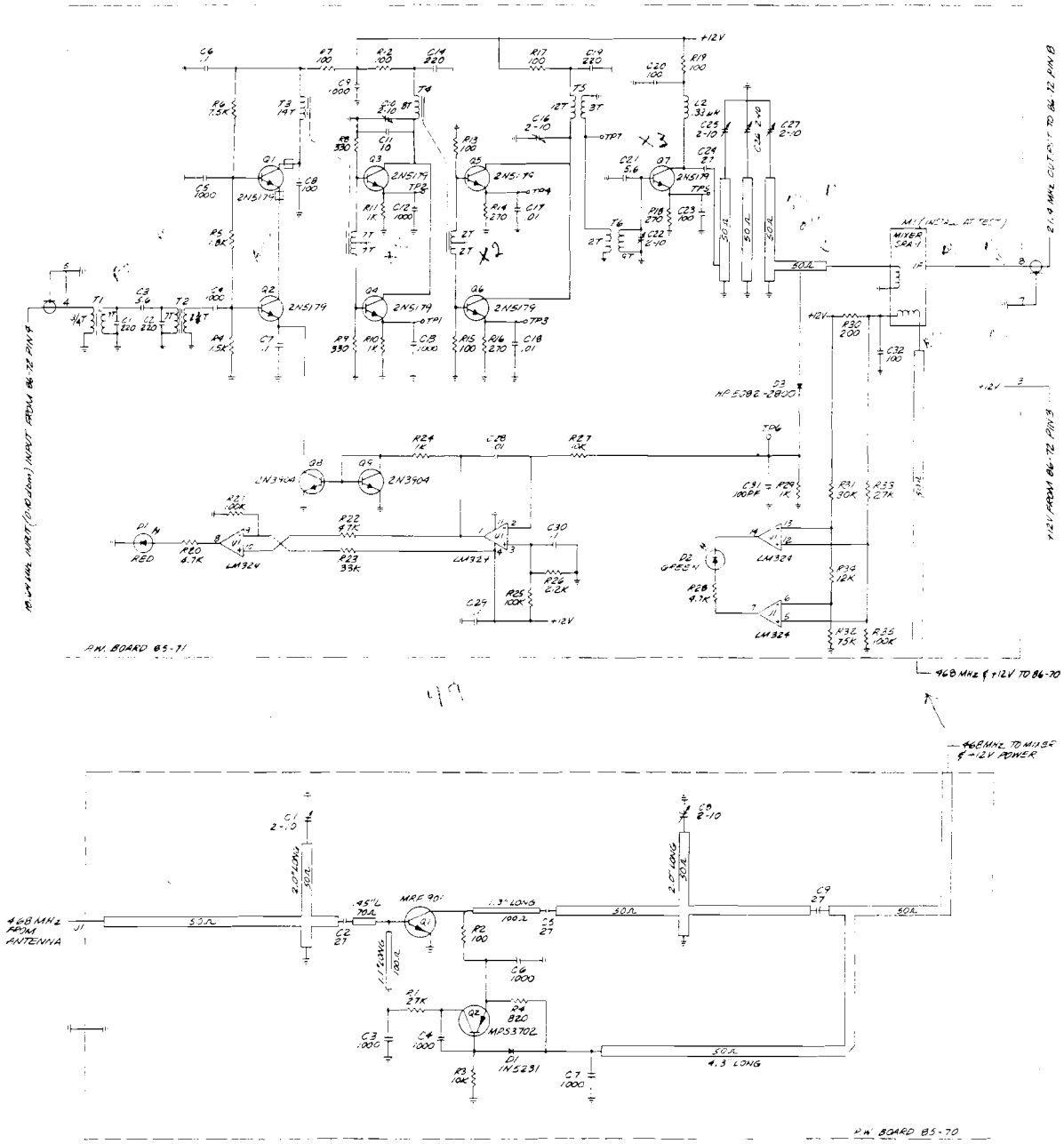
5-3 SYMBOL DESIGNATION REFERENCE 86-71

SYMBOL	TRUE TIME PART #	DESCRIPTION	
BEAD	41-0	Ferrite Bead	
C1	29-41	Cap. Dipped Mica	220PF
C2	29-41	Cap. Dipped Mica	220PF
C3	36-5	Cap. Monolithic	5.6F
C4	36-58	Cap. Monolithic	1000PF
C5	36-58	Cap. Monolithic	1000PF
C6	36-95	Cap. Monolithic	.1uf
C7	36-95	Cap. Monolithic	.1uf
C8	29-33	Cap. Dipped Mica	100PF
C9	36-58	Cap. Monolithic	1000PF
C10	34-2	Cap. Air Variable	2-10PF
C11	36-10	Cap. Monolithic	10PF
C12	36-58	Cap. Monolithic	1000PF
C13	36-58	Cap. Monolithic	1000PF
C14	36-41	Cap. Monolithic	220PF
C15		NOT USED	
C16	34-2	Cap. Air Variable	2-10PF
C17	36-83	Cap. Monolithic	.01uf
C18	36-83	Cap. Monolithic	.01uf
C19	36-41	Cap. Monolithic	220PF
C20	36-33	Cap. Monolithic	100PF
C21	36-5	Cap. Monolithic	5.6PF
C22	34-2	Cap. Air Variable	2-10PF
C23	36-33	Cap. Monolithic	100PF
C24	36-18	Cap. Monolithic	27PF
C25	34-2	Cap. Air Variable	2-10PF
C26	34-2	Cap. Air Variable	2-10PF
C27	34-2	Cap. Air Variable	2-10PF
C28	36-83	Cap. Monolithic	.01uf
C29	36-95	Cap. Monolithic	.1uf
C30	36-95	Cap. Monolithic	.1uf
C31	36-33	Cap. Monolithic	100PF
C32	36-33	Cap. Monolithic	100PF

SYMBOL	TRUE TIME PART #	DESCRIPTION
D1	58-4	Led, Red
D2	58-1	Led, Green
D3	57-4	Diode,HP#5082-2800
L1		NOT USED
L2	45-27	Coil Assembly (45-27)
M1	50-1	Balanced Mixer
PWB	85-71	Printed Wiring Board
Q1	175-2N5179	Transistor, 2N5179
Q2	175-2N5179	Transistor, 2N5179
Q3	175-2N5179	Transistor, 2N5179
Q4	175-2N5179	Transistor, 2N5179
Q5	175-2N5179	Transistor, 2N5179
Q6	175-2N5179	Transistor, 2N5179
Q7	175-2N5179	Transistor, 2N5179
Q8	175-2	Transistor, 2N3904
Q9	175-2	Transistor, 293904
R1		NOT USED
R2		NOT USED
R3		NOT USED
R4	2-77	Res. Carbon 1.5K
R5	2-79	Res. Carbon 1.8K
R6	2-94	Res. Carbon 7.5K
R7	2-49	Res. Carbon 100Ω
R8	2-61	Res. Carbon 330Ω
R9	2-61	Res. Carbon 330Ω
R10	2-73	Res. Carbon 1K
R11	2-73	Res. Carbon 1K
R12	2-49	Res. Carbon 100Ω
R13	2-49	Res. Carbon 100Ω
R14	2-59	Res. Carbon 270Ω
R15	2-49	Res. Carbon 100Ω
R16	2-59	Res. Carbon 270Ω
R17	2-49	Res. Carbon 100Ω
R18	2-59	Res. Carbon 270Ω
R19	2-49	Res. Carbon 100Ω
R20	2-89	Res. Carbon 4.7K
R21	2-121	Res. Carbon 100K
R22	2-113	Res. Carbon 47K
R23	2-109	Res. Carbon 33K
R24	2-73	Res. Carbon 1K
R25	2-121	Res. Carbon 100K
R26	2-81	Res. Carbon 2.2K
R27	2-97	Res. Carbon 10K
R28	2-89	Res. Carbon 4.7K
R29	2-73	Res. Carbon 1K
R30	2-56	Res. Carbon 200Ω
R31	2-108	Res. Carbon 30K
R32	2-118	Res. Carbon 75K
R33	2-107	Res. Carbon 27K
R34	2-99	Res. Carbon 12K
R35	2-121	Res. Carbon 100K
T1	41-6A	Transformer 42-46
T2	41-6A	Transformer 42-56
T3	43-2	Toroid 42-26
T4	43-2	Toroid 42-27
T5	43-4	Toroid 42-28
T6	43-4	Toroid 42-29
U1	176-324	I.C. LM324

Note: All resistors are 1/4W ± 5%

5-3 SYMBOL DESIGNATION REFERENCE 86-71 CONT



5-4 SCHEMATIC-ASSEMBLY 86-70/71

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	29-20	Cap. Dipped Mica 33pf
C2		NOT USED
C3		NOT USED
C4	29-10	Cap. Dipped Mica 10pf
C5	29-7	Cap. Dipped Mica 7pf
C6	29-20	Cap. Dipped Mica 33pf
C7	29-3	Cap. Dipped Mica 3pf
C8	36-58	Cap. Monolithic .001uf
C9	36-83	Cap. Monolithic .01uf
C10	36-83	Cap. Monolithic .01uf
C11	29-20	Cap. Dipped Mica 33pf
C12	36-58	Cap. Monolithic .001uf
C13	36-83	Cap. Monolithic .01uf
C14	36-83	Cap. Monolithic .01uf
C15	29-20	Cap. Dipped Mica 33pf
C16	36-58	Cap. Monolithic .001uf
C17	36-58	Cap. Monolithic .001uf
C18	36-83	Cap. Monolithic .01uf
C19	36-95	Cap. Monolithic .1uf
C20	36-83	Cap. Monolithic .01uf
C21	29-20	Cap. Dipped Mica 33pf
C22	29-10	Cap. Dipped Mica 10pf
C23	29-20	Cap. Dipped Mica 33pf
C24	36-83	Cap. Monolithic .01uf
C25	36-83	Cap. Monolithic .01uf
C26	29-41	Cap. Dipped Mica 220pf
C27	36-58	Cap. Monolithic .001uf
C28	36-83	Cap. Monolithic .01uf
C29	36-58	Cap. Monolithic .001uf
C30	36-83	Cap. Monolithic .01uf
C31	36-83	Cap. Monolithic .01uf
C32	29-41	Cap. Dipped Mica 220pf
C33	36-83	Cap. Monolithic .01uf
C34	29-24	Cap. Dipped Mica 47pf
C35	29-13	Cap. Dipped Mica 15pf
C36	29-7	Cap. Dipped Mica 7pf
C37	29-20	Cap. Dipped Mica 33pf
C38	36-83	Cap. Monolithic .01uf
C39	29-41	Cap. Dipped Mica 220pf
C40	36-83	Cap. Monolithic .01uf
C41	36-58	Cap. Monolithic .001uf
C42	36-83	Cap. Monolithic .01uf
C43	29-38	Cap. Dipped Mica 160pf
C44	36-83	Cap. Monolithic .01uf

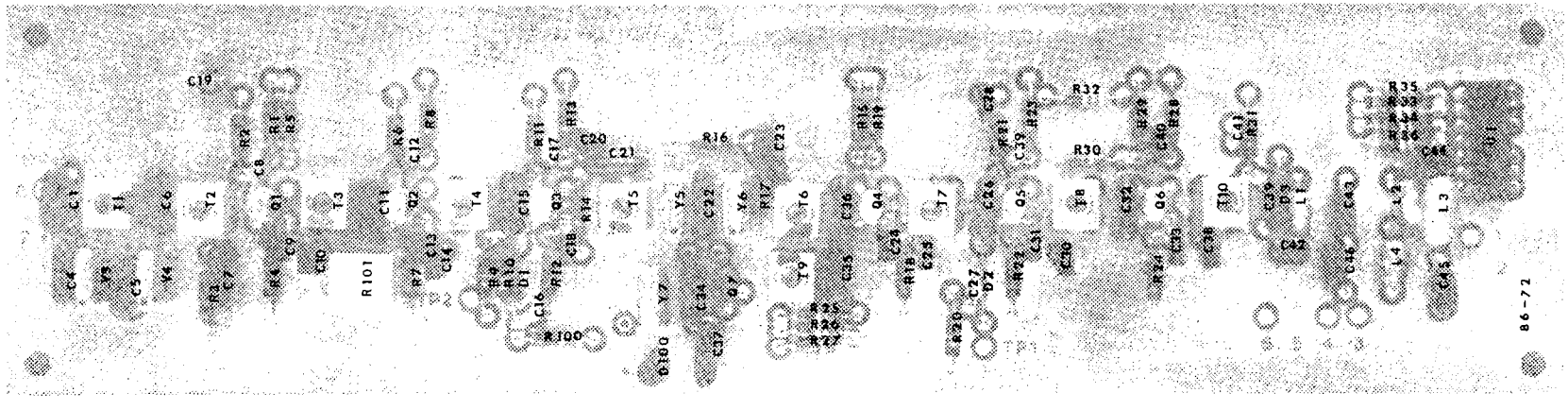
SYMBOL	TRUE TIME PART #	DESCRIPTION
C45	29-39	Cap. Dipped Mica 180pf
C46	29-39	Cap. Dipped Mica 180pf
D1	57-1	Diode 1N4148
D2	57-1	Diode 1N4148
D3	57-1	Diode 1N4148
D100	35-12	Diode MV2112
L1	43-5	Coil Assembly 42-37
L2	43-5	Coil Assembly 42-36
L3	43-3	Coil Assembly 42-38
L4	43-2	Coil Assembly 42-35
PWB	85-72	Print Wiring Board,
Q1	175-1	Transistor 40822
Q2	175-1	Transistor 40822
Q3	175-1	Transistor 40822
Q4	175-1	Transistor 40822
Q5	175-1	Transistor 40822
Q6	175-1	Transistor 40822
Q7	175-3	Transistor MPS2369
R1	2-169	Res. Carbon 10M
R2	2-145	Res. Carbon 1.0M
R3	2-145	Res. Carbon 1.0M
R4	2-59	Res. Carbon 270Ω
R5	2-49	Res. Carbon 100Ω
R6	2-145	Res. Carbon 1.0M
R7	2-59	Res. Carbon 270Ω
R8	2-49	Res. Carbon 100Ω
R9	2-107	Res. Carbon 27K
R10	2-107	Res. Carbon 27K
R11	2-145	Res. Carbon 1.0M
R12	2-59	Res. Carbon 270Ω
R13	2-49	Res. Carbon 100Ω
R14	2-77	Res. Carbon 1.5K
R15	2-153	Res. Carbon 2.2M
R16	2-145	Res. Carbon 1.0M
R17	2-77	Res. Carbon 1.5K
R18	2-59	Res. Carbon 270Ω
R19	2-49	Res. Carbon 100Ω
R20	2-107	Res. Carbon 27K
R21	2-145	Res. Carbon 1.0M
R22	2-59	Res. Carbon 270Ω
R23	2-49	Res. Carbon 100Ω

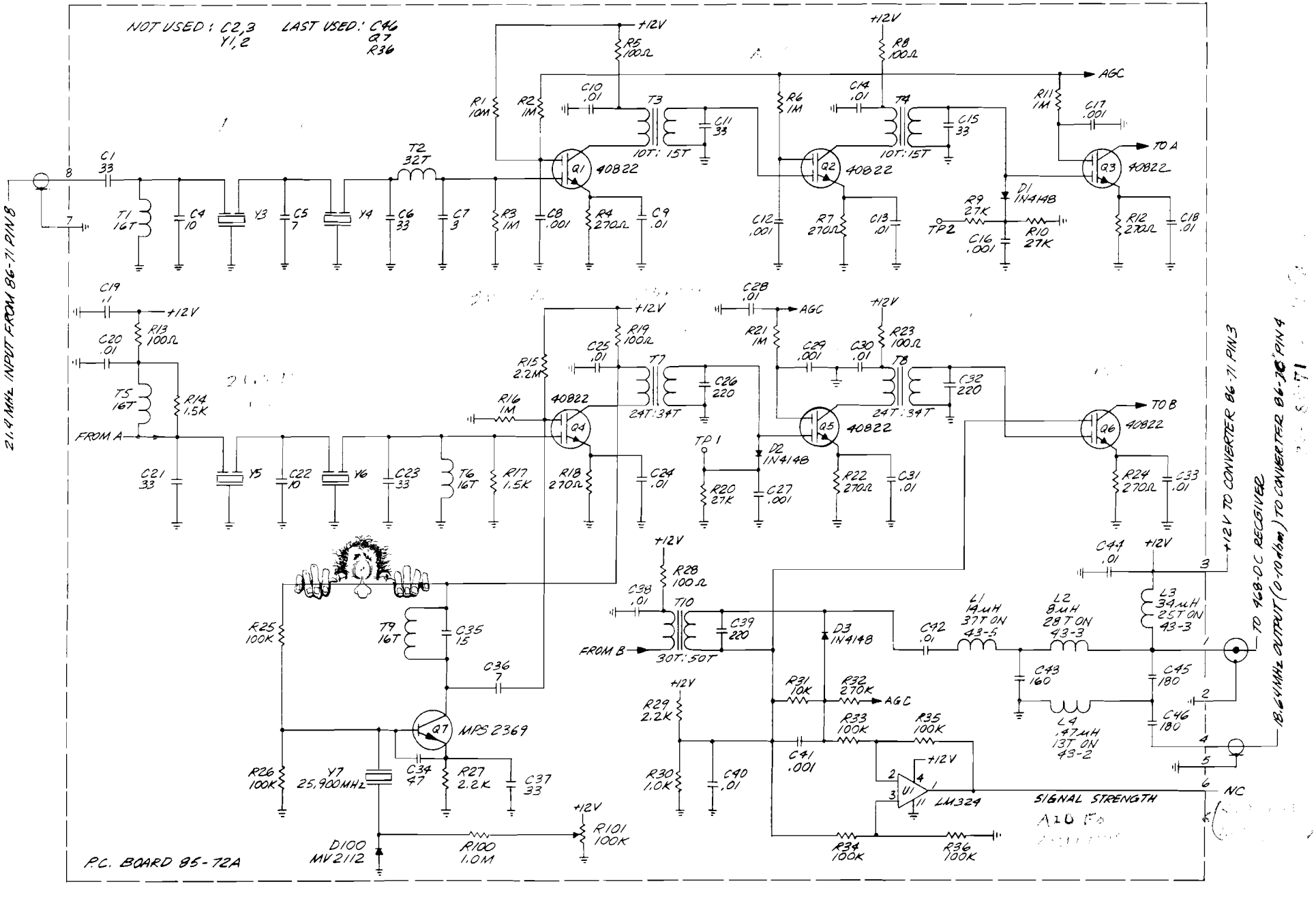
SYMBOL	TRUE TIME PART #	DESCRIPTION
R24	2-59	Res. Carbon 270Ω
R25	2-121	Res. Carbon 100K
R26	2-121	Res. Carbon 100K
R27	2-81	Res. Carbon 2.2K
R28	2-49	Res. Carbon 100Ω
R29	2-81	Res. Carbon 2.2K
R30	2-73	Res. Carbon 1k
R31	2-97	Res. Carbon 10K
R32	2-131	Res. Carbon 270K
R33	2-121	Res. Carbon 100K
R34	2-121	Res. Carbon 100K
R35	2-121	Res. Carbon 100K
R36	2-121	Res. Carbon 100K
R100	2-145	Res. Carbon 1.0M
R101	20-7	Pot. Trim 100K
T1	41-6A	Coil Assembly 42-30
T2	41-6A	Coil Assembly 42-31
T3	41-6A	Coil Assembly 42-32
T4	41-6A	Coil Assembly 42-32
T5	41-6A	Coil Assembly 42-30
T6	41-6A	Coil Assembly 42-30
T7	41-6A	Coil Assembly 42-33
T8	41-6A	Coil Assembly 42-33
T9	41-6A	Coil Assembly 42-30
T10	41-6A	Coil Assembly 42-34
U1	176-324	I.C. LM324
Y1		NOT USED
Y2		NOT USED
Y3	59-21400	Crystal Filter *
Y4	59-21400	Crystal Filter *
Y5	59-21400	Crystal Filter *
Y6	59-21400	Crystal Filter *
Y7	59-25900	Crystal 25.900 MHz

* Piezo Tech. P/N 1617, each part consists of one pair of crystals.

Note: all resistors are 1/4W ± 5%

5-5 SYMBOL DESIGNATION REFERENCE 86-72





5-7 SCHEMATIC-ASSEMBLY 86-72

5-8 SYMBOL DESIGNATION REFERENCE 86-73

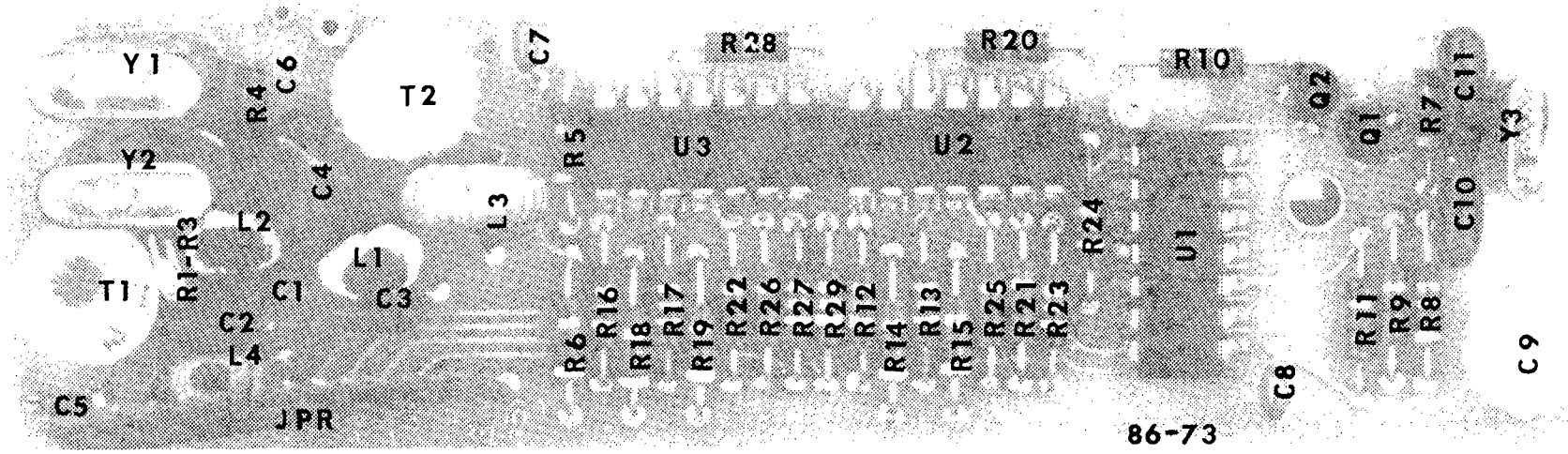
SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	36-95	Cap. Monolithic .luf
C2	29-39	Cap. Dipped Mica 180pf
C3	29-39	Cap. Dipped Mica 180pf
C4	29-54	Cap. Dipped Mica 680pf
C5	36-95	Cap. Monolithic .luf
C6		NOT USED
C7	36-95	Cap. Monolithic .luf
C8	36-95	Cap. Monolithic .luf
C9	33-60	Cap. Ceramic 10-60pf
C10	29-39	Cap. Dipped Mica 180pf
C11	29-33	Cap. Dipped Mica 100pf
JPR	317-12	Jumper Wire, 12 leads
L1	43-2	Coil Assembly (42-40)
L2	43-2	Coil Assembly (42-40)
L3	43-3	Coil Assembly (42-38)
L4	43-2	Coil Assembly (42-35)
PWB	85-73	Printed Wiring Board
Q1	175-4	Transistor MPS3702
Q2	175-3	Transistor MPS2369

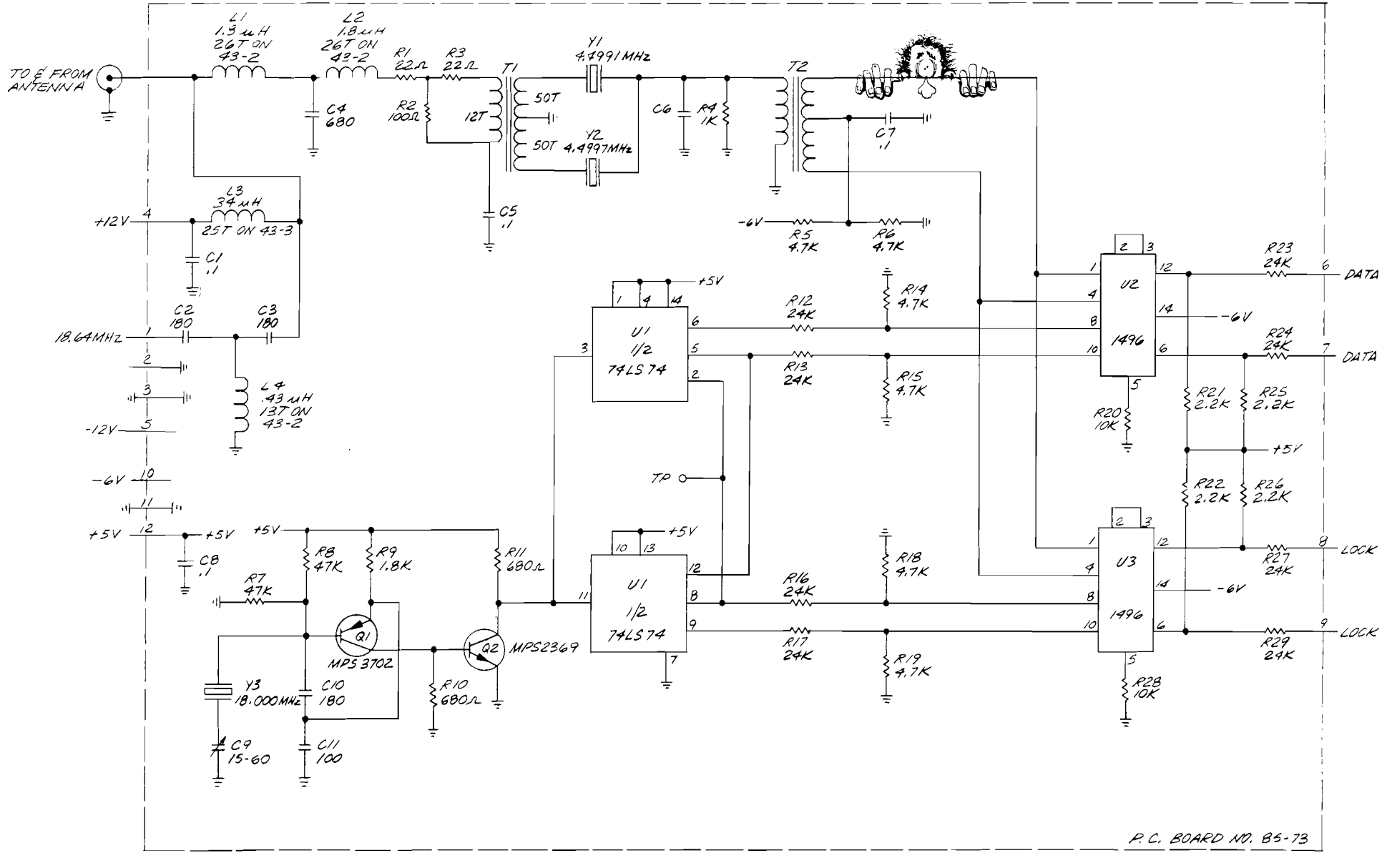
SYMBOL	TRUE TIME PART #	DESCRIPTION
R1	2-33	Resistor Carbon 22Ω
R2	2-49	Resistor Carbon 100Ω
R3	2-33	Resistor Carbon 22Ω
R4	2-73	Resistor Carbon 1K
R5	2-89	Resistor Carbon 4.7K
R6	2-89	Resistor Carbon 4.7K
R7	2-113	Resistor Carbon 47K
R8	2-113	Resistor Carbon 47K
R9	2-79	Resistor Carbon 1.8K
R10	2-69	Resistor Carbon 680Ω
R11	2-69	Resistor Carbon 680Ω
R12	2-106	Resistor Carbon 24K
R13	2-106	Resistor Carbon 24K
R14	2-89	Resistor Carbon 4.7K
R15	2-89	Resistor Carbon 4.7K
R16	2-106	Resistor Carbon 24K
R17	2-106	Resistor Carbon 24K
R18	2-89	Resistor Carbon 4.7K
R19	2-89	Resistor Carbon 4.7K
R20	2-97	Resistor Carbon 10K
R21	2-81	Resistor Carbon 2.2K
R22	2-81	Resistor Carbon 2.2K
R23	2-106	Resistor Carbon 24K
R24	2-106	Resistor Carbon 24K

SYMBOL	TRUE TIME PART #	DESCRIPTION
R25	2-81	Resistor Carbon 2.2K
R26	2-81	Resistor Carbon 2.2K
R27	2-106	Resistor Carbon 24K
R28	2-97	Resistor Carbon 10K
R29	2-106	Resistor Carbon 24K
T1	43-3	Toroid (42-42)
T2	43-3	Toroid (42-43)
U1	176-74LS74	I.C. 74LS74
U2	176-1496	I.C. 1496
U3	176-1496	I.C. 1496
Y1	59-4499A	Crystal 4.4991 MHz
Y2	59-4499	Crystal 4.4997 MHz
Y3	59-18000	Crystal 18.000 MHz
	43-100	Base, Toroid

Note: All resistors are 1/4W ± 5%

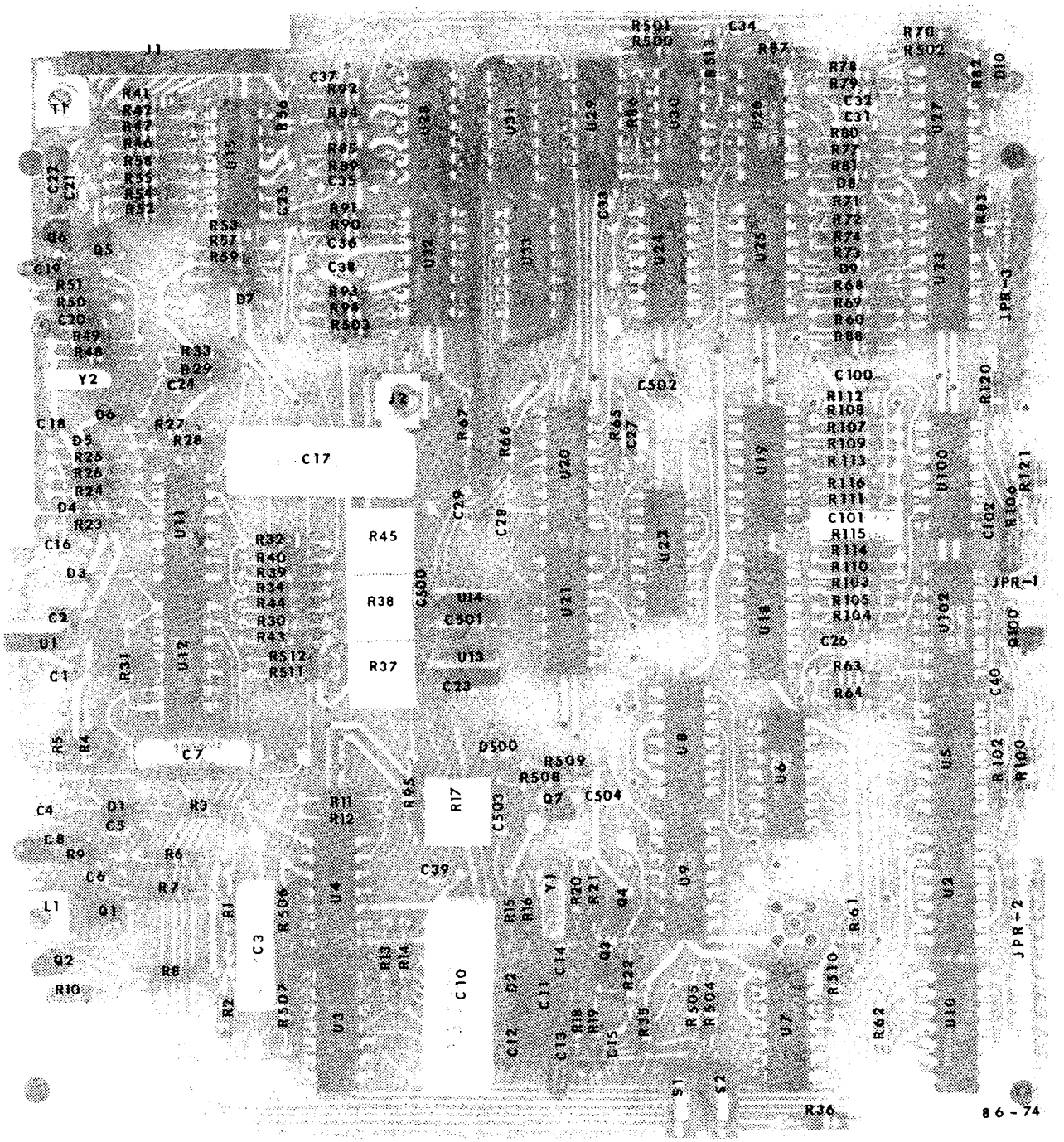
5-9 PARTS LOCATION-ASSEMBLY 86-73

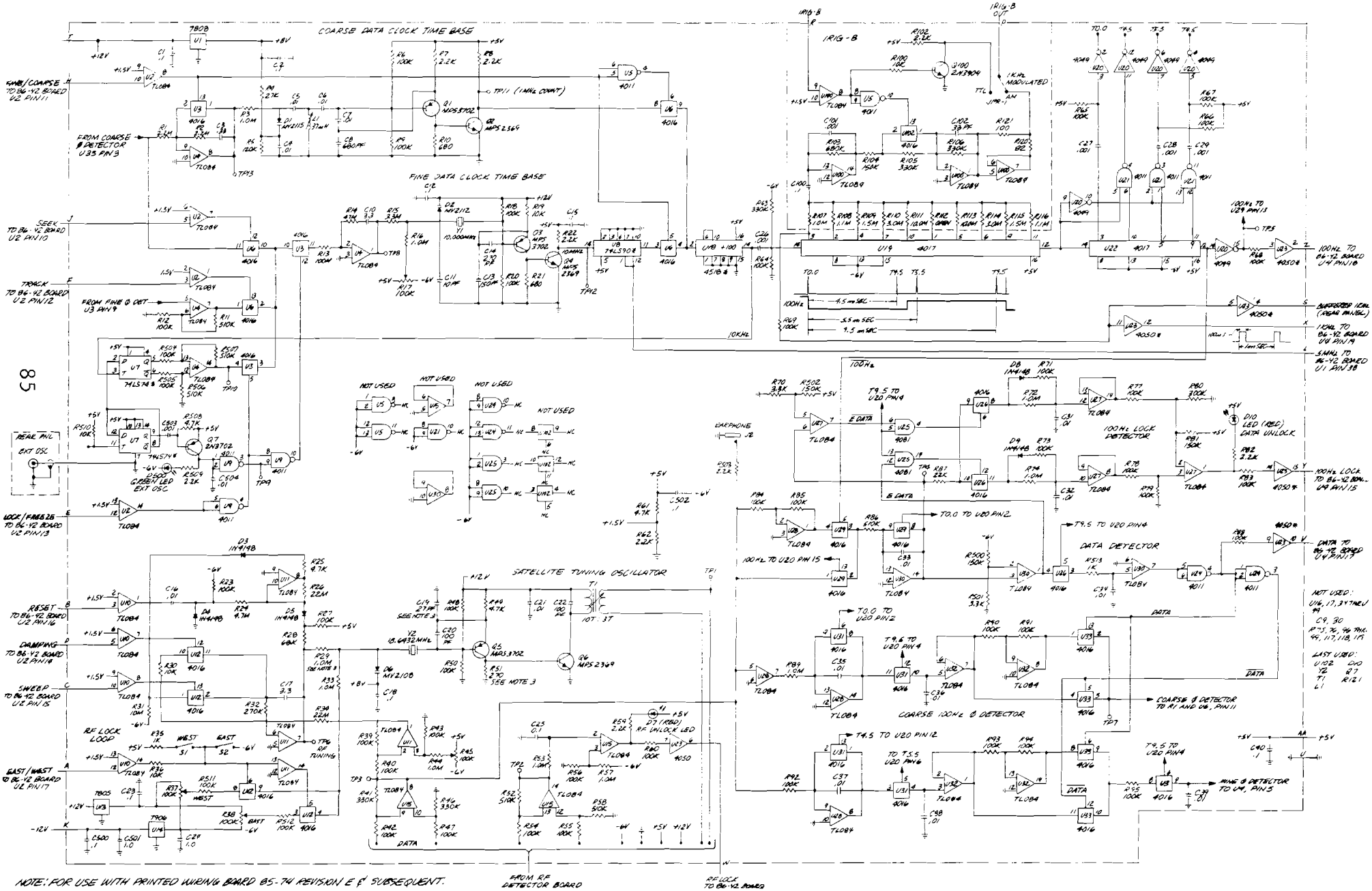




5-10 SCHEMATIC-ASSEMBLY 86-73

5-11 PARTS LOCATION-ASSEMBLY 86-74





85

5-12 SCHEMATIC-ASSEMBLY 86-74

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	36-95	Cap. Monolithic .1uf
C2	36-95	Cap. Monolithic .1uf
C3	28-19	Cap. Plastic Film .33uf
C4	36-83	Cap. Monolithic .01uf
C5	36-83	Cap. Monolithic .01uf
C6	36-83	Cap. Monolithic .01uf
C7	24-13	Cap. Polystyrene .01uf
C8	29-54	Cap. Dipped Mica 680pf
C9		NOT USED
C10	28-43	Cap. Plastic Film 3.3uf
C11	29-10	Cap. Dipped Mica 10pf
C12	36-95	Cap. Monolithic .1uf
C13	29-37	Cap. Dipped Mica 150pf
C14	29-44	Cap. Dipped Mica 270pf
C15	36-95	Cap. Monolithic .1uf
C16	36-83	Cap. Monolithic .01uf
C17	28-43	Cap. Plastic Film 3.3uf
C18	36-95	Cap. Monolithic .1uf
C19	29-18	Cap. Dipped Mica 27pf
C20	29-33	Cap. Dipped Mica 100pf
C21	36-83	Cap. Monolithic .01uf
C22	29-33	Cap. Dipped Mica 100pf
C23	36-95	Cap. Monolithic .1uf
C24	32-59	Cap. Tant. 1.0uf
C25	36-95	Cap. Monolithic .1uf
C26	36-58	Cap. Monolithic .001uf
C27	36-58	Cap. Monolithic .001uf
C28	36-58	Cap. Monolithic .001uf
C29	36-58	Cap. Monolithic .001uf
C30		NOT USED
C31	36-83	Cap. Monolithic .01uf
C32	36-83	Cap. Monolithic .01uf
C33	36-83	Cap. Monolithic .01uf
C34	36-83	Cap. Monolithic .01uf
C35	36-83	Cap. Monolithic .01uf
C36	36-83	Cap. Monolithic .01uf
C37	36-83	Cap. Monolithic .01uf
C38	36-83	Cap. Monolithic .01uf
C39	36-83	Cap. Monolithic .01uf
C40	36-95	Cap. Monolithic .1uf
C100	36-95	Cap. Monolithic .1uf
C101	24-1	Cap. Polystyrene .001uf
C102	29-20	Cap. Dipped Mica 33pf
C500	36-95	Cap. Monolithic .1uf
C501	32-29	Cap. Tant. 1.0uf
C502	36-95	Cap. Monolithic .1uf
C503	36-58	Cap. Monolithic .001uf
C504	36-83	Cap. Monolithic .01uf

SYMBOL	TRUE TIME PART #	DESCRIPTION
D1	35-15	Varicap MV2115
D2	35-12	Varicap MV2112
D3	57-1	Diode 1N4148
D4	57-1	Diode 1N4148
D5	57-1	Diode 1N4148
D6	35-8	Varicap MV2108
D7	58-4	LED-Red
D8	57-1	Diode 1N4148
D9	57-1	Diode 1N4148
D10	58-4	LED-Red
D500	58-1	LED-Green
J1	318-12	Socket, 12 Pin Strip
J2	369-2	Jack, Earphone
JPR-1	315-26-2	Jumper
JPR-2	317-12	Jumper
JPR-3	317-12	Jumper
L1	41-6A	Coil, R.F. (42-44)
PWB	85-74	Printed Wiring Board
Q1	175-4	Transistor MPS3702
Q2	175-3	Transistor MPS2369
Q3	175-4	Transistor MPS3702
Q4	175-3	Transistor MPS2369
Q5	175-4	Transistor MPS3702
Q6	175-3	Transistor MPS2369
Q7	175-4	Transistor MPS3702
Q100	175-2	Transistor 2N3904
R1	2-153	Resistor Carbon 2.2M
R2	2-153	Resistor Carbon 2.2M
R3	2-145	Resistor Carbon 1.0M
R4	2-107	Resistor Carbon 27K
R5	2-123	Resistor Carbon 120K
R6	2-121	Resistor Carbon 100K
R7	2-81	Resistor Carbon 2.2K
R8	2-81	Resistor Carbon 2.2K
R9	2-121	Resistor Carbon 100K
R10	2-69	Resistor Carbon 680Ω
R11	2-138	Resistor Carbon 510K
R12	2-121	Resistor Carbon 100K
R13	2-203	Resistor Carbon 100M
R14	2-186	Resistor Carbon 47M
R15	2-157	Resistor Carbon 3.3M
R16	2-145	Resistor Carbon 1.0M
R17	20-7	Res.Carbon 100K Pot.

Note: All resistors are 1/4W + 5%

SYMBOL	TRUE TIME PART #	DESCRIPTION
R18	2-121	Resistor Carbon 100K
R19	2-97	Resistor Carbon 10K
R20	2-121	Resistor Carbon 100K
R21	2-69	Resistor Carbon 680Ω
R22	2-81	Resistor Carbon 2.2K
R23	2-121	Resistor Carbon 100K
R24	2-161	Resistor Carbon 4.7M
R25	2-89	Resistor Carbon 4.7K
R26	2-177	Resistor Carbon 22M
R27	2-121	Resistor Carbon 100K
R28	2-117	Resistor Carbon 68K
R29	2-145	Resistor Carbon 1.0M
R30	2-97	Resistor Carbon 10K
R31	2-169	Resistor Carbon 10M
R32	2-131	Resistor Carbon 270K
R33	2-145	Resistor Carbon 1.0M
R34	2-177	Resistor Carbon 22M
R35	2-73	Resistor Carbon 1K
R36	2-97	Resistor Carbon 10K
R37	20-7	Res.Carbon 100K Pot.
R38	20-7	Res.Carbon 100K Pot.
R39	2-121	Resistor Carbon 100K
R40	2-121	Resistor Carbon 100K
R41	2-133	Resistor Carbon 330K
R42	2-121	Resistor Carbon 100K
R43	2-121	Resistor Carbon 100K
R44	2-145	Resistor Carbon 1.0M
R45	20-7	Res.Carbon 100K Pot.
R46	2-133	Resistor Carbon 330K
R47	2-121	Resistor Carbon 100K
R48	2-121	Resistor Carbon 100K
R49	2-89	Resistor Carbon 4.7K
R50	2-121	Resistor Carbon 100K
R51	2-59	Resistor Carbon 270Ω
R52	2-138	Resistor Carbon 510K
R53	2-145	Resistor Carbon 1.0M
R54	2-121	Resistor Carbon 100K
R55	2-121	Resistor Carbon 100K
R56	2-121	Resistor Carbon 100K
R57	2-145	Resistor Carbon 1.0M
R58	2-138	Resistor Carbon 510K
R59	2-81	Resistor Carbon 2.2K
R60	2-121	Resistor Carbon 100K
R61	2-89	Resistor Carbon 4.7K
R62	2-81	Resistor Carbon 2.2K
R63	2-133	Resistor Carbon 300K
R64	2-121	Resistor Carbon 100K
R65	2-121	Resistor Carbon 100K

Note; All resistors are 1/4W ± 5%

5-13 SYMBOL DESIGNATION REFERENCE 86-74

SYMBOL	TRUE TIME PART #	DESCRIPTION
R66	2-121	Resistor Carbon 100K
R67	2-121	Resistor Carbon 100K
R68	2-121	Resistor Carbon 100K
R69	2-121	Resistor Carbon 100K
R70	2-85	Resistor Carbon 3.3K
R71	2-121	Resistor Carbon 100K
R72	2-145	Resistor Carbon 1.0M
R73	2-121	Resistor Carbon 100K
R74	2-145	Resistor Carbon 1.0M
R75		NOT USED
R76		NOT USED
R77	2-121	Resistor Carbon 100K
R78	2-121	Resistor Carbon 100K
R79	2-121	Resistor Carbon 100K
R80	2-132	Resistor Carbon 300K
R81	2-125	Resistor Carbon 150K
R82	2-81	Resistor Carbon 2.2K
R83	2-121	Resistor Carbon 100K
R84	2-121	Resistor Carbon 100K
R85	2-121	Resistor Carbon 100K
R86	2-138	Resistor Carbon 510K
R87	2-105	Resistor Carbon 22K
R88	2-121	Resistor Carbon 100K
R89	2-145	Resistor Carbon 1.0M
R90	2-121	Resistor Carbon 100K
R91	2-121	Resistor Carbon 100K
R92	2-121	Resistor Carbon 100K
R93	2-121	Resistor Carbon 100K
R94	2-121	Resistor Carbon 100K
R95	2-121	Resistor Carbon 100K
R96		NOT USED
R97		NOT USED
R98		NOT USED
R99		NOT USED
R100	2-97	Resistor Carbon 10K
R101		NOT USED
R102	2-81	Resistor Carbon 2.2K
R103	2-141	Resistor Carbon 680K
R104	2-125	Resistor Carbon 150K
R105	2-133	Resistor Carbon 330K
R106	2-133	Resistor Carbon 330K
R107	2-145	Resistor Carbon 1.0M
R108	2-146	Resistor Carbon 1.1M
R109	2-149	Resistor Carbon 1.5M
R110	2-156	Resistor Carbon 3.0M
R111	2-169	Resistor Carbon 10M
R112		Selected in test
R113	2-169	Resistor Carbon 10M

Note: All resistors are 1/4W ± 5%

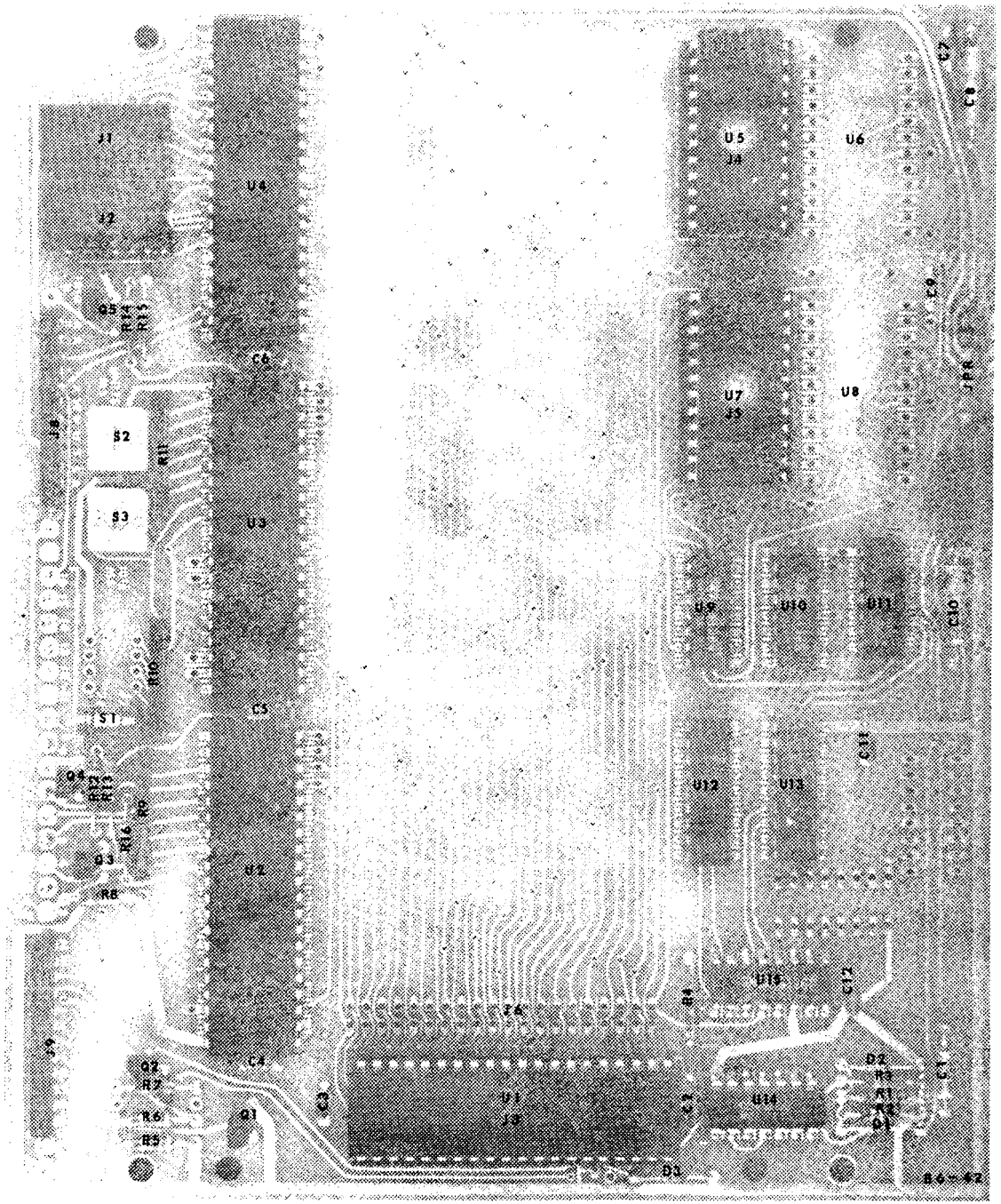
SYMBOL	TRUE TIME PART #	DESCRIPTION
R114	2-156	Resistor Carbon 3.0M
R115	2-149	Resistor Carbon 1.5M
R116	2-146	Resistor Carbon 1.1M
R117		NOT USED
R118		NOT USED
R119		NOT USED
R120	2-47	Resistor Carbon 82Ω
R121	2-49	Resistor Carbon 100Ω
R500	2-125	Resistor Carbon 150K
R501	2-85	Resistor Carbon 3.3K
R502	2-125	Resistor Carbon 150K
R503	2-81	Resistor Carbon 2.2K
R504	2-121	Resistor Carbon 100K
R505	2-121	Resistor Carbon 100K
R506	2-138	Resistor Carbon 510K
R507	2-138	Resistor Carbon 510K
R508	2-89	Resistor Carbon 4.7K
R509	2-81	Resistor Carbon 2.2K
R510	2-97	Resistor Carbon 10K
R511	2-121	Resistor Carbon 100K
R512	2-121	Resistor Carbon 100K
R513	2-73	Resister Carbon 100K
S1	65-1	Switch, 1 pos. Dip
S2	65-1	Switch, 1 pos. Dip
T1	41-6A	Transformer (42-45)
U1	176-7808	I.C. 7808
U2	176-TL084	I.C. TL084 (LM324 may be used)
U3	176-4016	I.C. 4016
U4	176-TL084	I.C. TL084 (only)
U5	176-4011	I.C. 4011
U6	176-4016	I.C. 4016
U7	176-74LS74	I.C. 74LS74
U8	176-74LS90	I.C. 74LS90
U9	176-4011	I.C. 4011
U10	176-TL084	I.C. TL084 (LM324 may be used)
U11	176-TL084	I.C. TL084 (only)
U12	176-4016	I.C. 4016
U13	176-7805	I.C. 7805
U14	176-7906	I.C. 7906
U15	176-TL084	I.C. TL084 (LM324 may be used)
U16		NOT USED
U17		NOT USED
U18	176-4518	I.C. 4518

Note: All resistors are 1/4W ± 5%

SYMBOL	TRUE TIME PART #	DESCRIPTION
U19	176-4017	I.C. 4017
U20	176-4049	I.C. 4049
U21	176-4011	I.C. 4011
U22	176-4017	I.C. 4017
U23	176-4050	I.C. 4050
U24	176-4011	I.C. 4011
U25	176-4081	I.C. 4081
U26	176-4016	I.C. 4016
U27	176-TL084	I.C. TL084
U28	176-TL084	I.C. TL084
U29	176-4016	I.C. 4016
U30	176-TL084	I.C. TL084
U31	176-4016	I.C. 4016
U32	176-TL084	I.C. TL084
U33	176-4016	I.C. 4016
U100	176-TL084	I.C. TL084
U102	176-4016	I.C. 4016
Y1	59-10.000	Crystal 10.000MHz
Y2	59-18.6432	Crystal 18.6432MHz

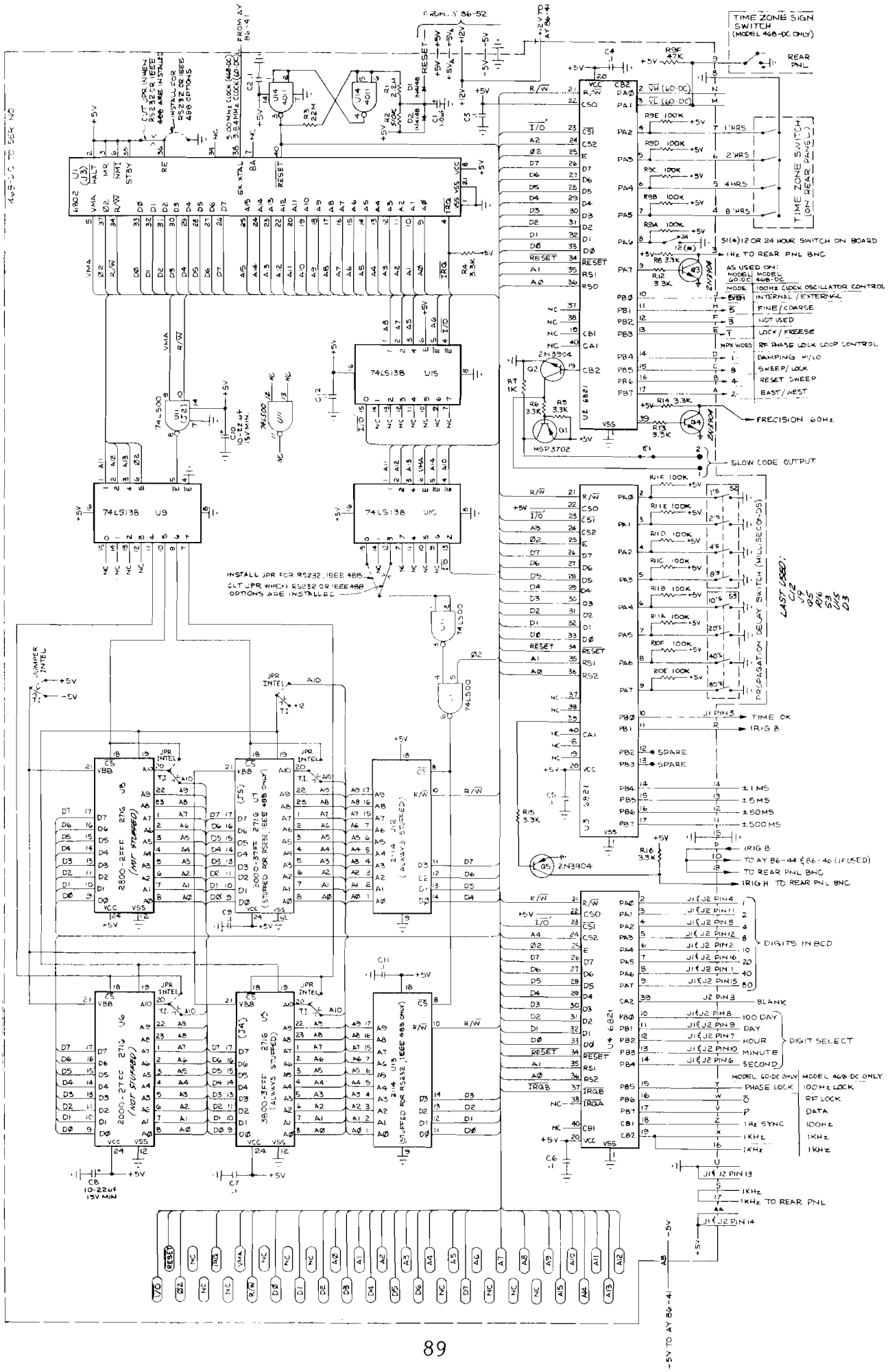
5-13 SYMBOL DESIGNATION REFERENCE 86-74 CONT

5-14 PARTS LOCATION-ASSEMBLY 86-42



5-15 SYMBOL DESIGNATION REFERENCE 86-42

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	32-29	Cap. Tant. 1.0uf 35V
C2	36-95	Cap. Monolithic .luf
C3	36-95	Cap. Monolithic .luf
C4	36-95	Cap. Monolithic .luf
C5	36-95	Cap. Monolithic .luf
C6	36-95	Cap. Monolithic .luf
C7	36-95	Cap. Monolithic .luf
C8	27-8-25*	Cap. Alum Electro 10uf 25V
C9	36-95	Cap. Monolithic .luf
C10	27-8-25*	Cap. Alum Electro 10uf 25V
C11	36-95	Cap. Monolithic .luf
C12	36-95	Cap. Monolithic .luf
	*32-45	Cap. Tant 22uf 15V may be used
D1	57-1	Diode, 1N4148
D2	57-1	Diode, 1N4148
D3	57-1	Diode, 1N4148
J1		NOT USED
J2	379-16	Socket, 16 Pin I.C.
J3	379-40	Socket, 40 Pin I.C.
J4	379-24	Socket, 24 Pin I.C.
J5	379-24	Socket, 24 Pin I.C.
J6	384-40	Connector, 40 Pin Male
J7		NOT USED
J8	318-12	Socket, 12 Pin Strip
J9	318-12	Socket, 12 Pin Strip
JPR	317-14	Jumper
Q1	175-4	Transistor, MPS3702
Q2	175-2	Transistor, 2N3904
Q3	175-2	Transistor, 2N3904
Q4	175-2	Transistor, 2N3904
Q5	175-2	Transistor, 2N3904
R1	2-153	Resistor Carbon 2.2M
R2	2-138	Resistor Carbon 510M
R3	2-177	Resistor Carbon 22M
R4	2-85	Resistor Carbon 3.3K
R5	2-85	Resistor Carbon 3.3K
R6	2-85	Resistor Carbon 3.3K
R7	2-73	Resistor Carbon 1K
R8	2-85	Resistor Carbon 3.3K
R9	11-121	Res.Carbon 100K SIP
R10	11-121	Res.Carbon 100K SIP
R11	11-121	Res.Carbon 100K SIP
R12	2-85	Resistor Carbon 3.3K
R13	2-85	Resistor Carbon 3.3K
R14	2-85	Resistor Carbon 3.3K
R15	2-85	Resistor Carbon 3.3K
R16	2-85	Resistor Carbon 3.3K
Note: All resistors are 1/4W ± 5%		
S1	65-1	Switch, 1 Pos. Dip
S2	63-2	Switch 10 Pos. Rotary
S3	63-2	Switch 10 Pos. Rotary
U1	176-6802	I.C. Motorola #MC6802
U2	176-6821	I.C. Motorola #MC6821
U3	176-6821	I.C. Motorola #MC6821
U4	176-6821	I.C. Motorola #MC6821
U5		NOT USED
U6		NOT USED
U7	176-2716	I.C. Intel #2716
U8		NOT USED
U9	176-74LS138	I.C. 74LS138
U10	176-74LS138	I.C. 74LS138
U11	176-74LS00	I.C. 74LS00
U12	176-2114	I.C. Intel #2114
U13	176-2114	I.C. Intel #2114
U14	176-4011	I.C. 4011
U15	176-74LS138	I.C. 74LS138
PWB	85-42	Printed Wiring Board


TIME ZONE SIGN SWITCH (MODEL 468-DC ONLY)
REAR PNL
TIME ZONE SWITCH (ON REAR PANEL)
1 HRS
2 HRS
4 HRS
8 HRS
SI(#)12 OR 24 HOUR SWITCH ON BOARD
1Hz TO REAR PNL BNC
AS USED ON: MODEL 468 MODEL 60-DC 468-DC
100Hz CLOCK OSCILLATOR CONTROL
INTERNAL / EXTERNAL
FINE/COARSE
NOT USED
LOCK/FREESE
RF PHASE LOCK LOOP CONTROL
DAMPING HI/LO
SWEEP/LOCK
RESET SWEEP
EAST/WEST
PRECISION 60Hz
SLOW CODE OUTPUT
PROPAGATION DELAY SWITCH (MILLISECONDS)
TIME OK
IRIG B
SPARE
SPARE
±1MS
±5MS
±50MS
±500MS
IRIG B
TO AY 86-44 & 86-46 (IF USED)
TO REAR PNL BNC
IRIG H TO REAR PNL BNC
DIGITS IN BCD
BLANK
DIGIT SELECT
100 DAY
DAY
HOUR
MINUTE
SECOND
MODEL 60-DC ONLY
PHASE LOCK
100Hz LOCK
RF LOCK
DATA
1Hz SYNC
100Hz
1KHz
1KHz
1KHz
1KHz TO REAR PNL
FROM AY 86-41
FROM AY 86-52
TO AY 86-41
+5V TO AY 86-41
INSTALL JPR FOR RS232 IEEE 488
CUT JPR WHEN RS232 OR IEEE 488 OPTIONS ARE INSTALLED
CUT JPR WHEN RS232 OR IEEE 488 ARE INSTALLED
INSTALL FOR RS232 OR IEEE 488 OPTIONS
LAST USED: C12 U15 R6 R5 U16 D3

5-17 SYMBOL DESIGNATION REFERENCE 86-43

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	36-58	Cap. Monolithic .001uf
C2	36-58	Cap. Monolithic .001uf
C3	36-58	Cap. Monolithic .001uf
C4	36-58	Cap. Monolithic .001uf
C5	36-95	Cap. Monolithic .1uf
C6	36-95	Cap. Monolithic .1uf
D1	58-4	LED, Red, H.P. #5082-4684
D2	58-4	LED, Red, H.P. #5082-4684
D3	58-4	LED, Red, H.P. #5082-4684
D4	58-4	LED, Red, H.P. #5082-4684
D5	58-4	LED, Red, H.P. #5082-4684
D6	58-4	LED, Red, H.P. #5082-4684
D7	58-1	LED, Green
D8	58-1	LED, Green
PWB	85-43	Printed Wiring Board
Q1	175-MPS A43*	Transistor MPS A43
Q2	175-2N4889	Transistor 2N4889
Q3	175-MPS A43*	Transistor MPS A43
Q4	175-2N4889	Transistor 2N4889
Q5	175-MPS A43*	Transistor MPS A43
Q6	175-2N4889	Transistor 2N4889
Q7	175-MPS A43*	Transistor MPS A43
Q8	175-2N4889	Transistor 2N4889
Q9	175-MPS A43*	Transistor MPS A43
Q10	175-2N4889	Transistor 2N4889
Q11	175-2	Transistor 2N3904
Q12	175-2	Transistor 2N3904
Q13	175-2	Transistor 2N3904
Q14	175-2	Transistor 2N3904
Q15	175-2	Transistor 2N3904

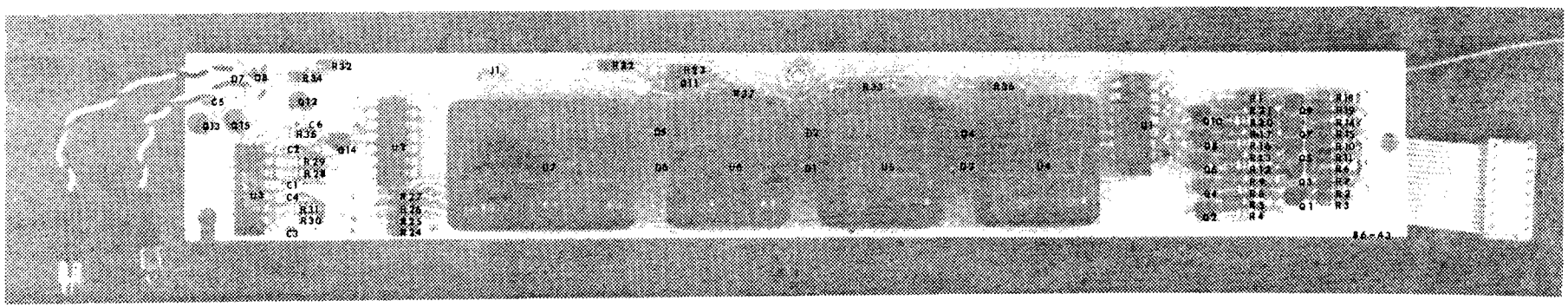
SYMBOL	TRUE TIME PART #	DESCRIPTION
R1	2-81	Res. Carbon 2.2K
R2	2-117	Res. Carbon 68K
R3	2-105	Res. Carbon 22K
R4	2-136	Res. Carbon 430K
R5	2-93	Res. Carbon 6.8K
R6	2-117	Res. Carbon 68K
R7	2-105	Res. Carbon 22K
R8	2-136	Res. Carbon 430K
R9	2-93	Res. Carbon 6.8K
R10	2-117	Res. Carbon 68K
R11	2-105	Res. Carbon 22K
R12	2-136	Res. Carbon 430K
R13	2-93	Res. Carbon 6.8K
R14	2-117	Res. Carbon 68K

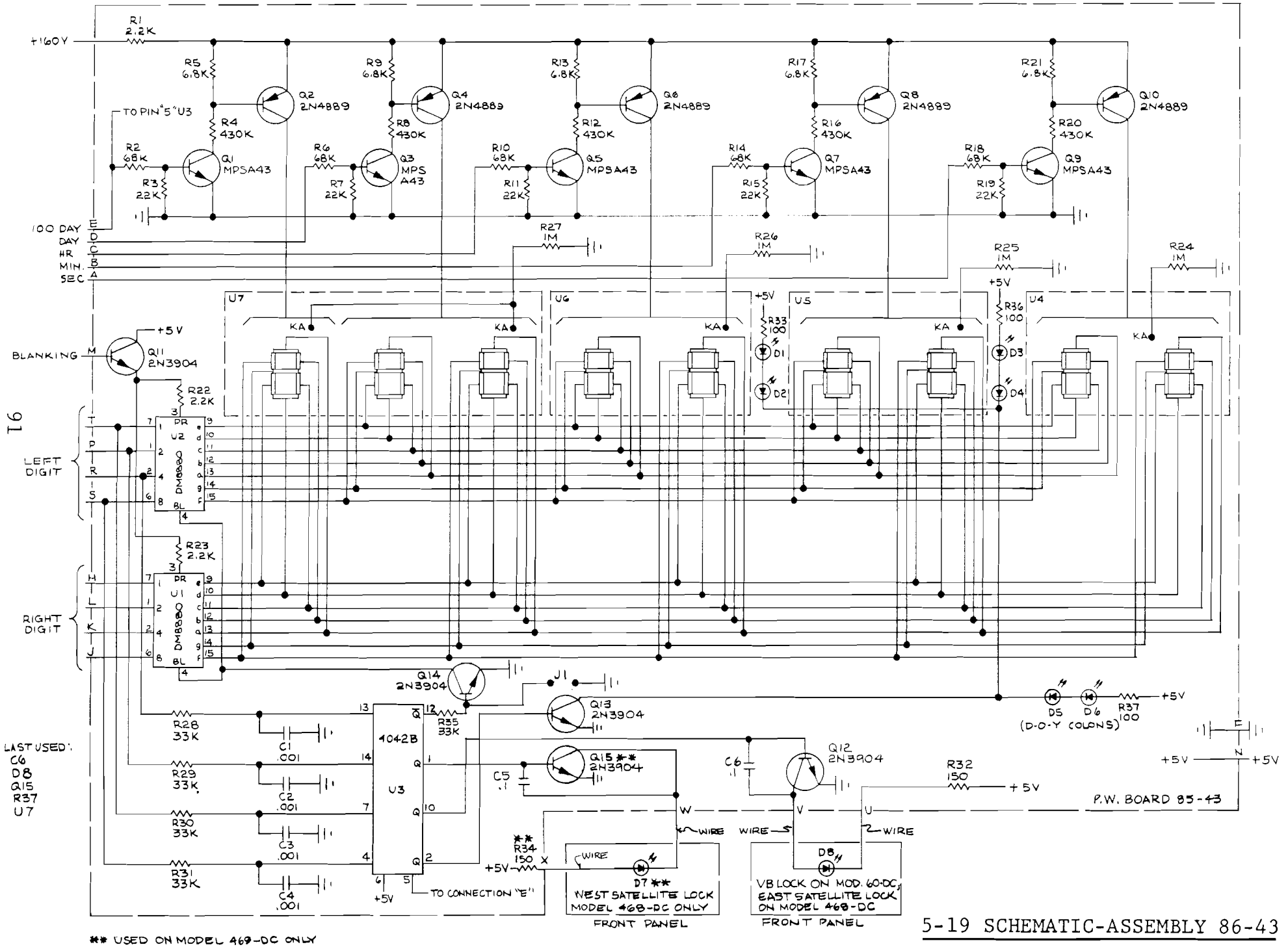
* Motorola Only

SYMBOL	TRUE TIME PART #	DESCRIPTION
R15	2-105	Res. Carbon 22K
R16	2-136	Res. Carbon 430K
R17	2-93	Res. Carbon 6.8K
R18	2-117	Res. Carbon 68K
R19	2-105	Res. Carbon 22K
R20	2-136	Res. Carbon 430K
R21	2-93	Res. Carbon 6.8K
R22	2-81	Res. Carbon 2.2K
R23	2-81	Res. Carbon 2.2K
R24	2-145	Res. Carbon 1 M
R25	2-145	Res. Carbon 1 M
R26	2-145	Res. Carbon 1 M
R27	2-145	Res. Carbon 1 M
R28	2-109	Res. Carbon 33K
R29	2-109	Res. Carbon 33K
R30	2-109	Res. Carbon 33K
R31	2-109	Res. Carbon 33K
R32	2-53	Res. Carbon 150Ω
R33	2-49	Res. Carbon 100Ω
R34	2-53	Res. Carbon 150Ω
R35	2-109	Res. Carbon 33K
R36	2-49	Res. Carbon 100Ω
R37	2-49	Res. Carbon 100Ω
U1	176-8880	I.C. National #DM8880
U2	176-8880	I.C. National #DM8880
U3	176-4042	I.C. RCA #4042B
U4	189-1	Digit Display, Beckman SP352
U5	189-1	Digit Display, Beckman SP352
U6	189-1	Digit Display, Beckman SP352
U7	189-2	Digit Display, Beckman SP353

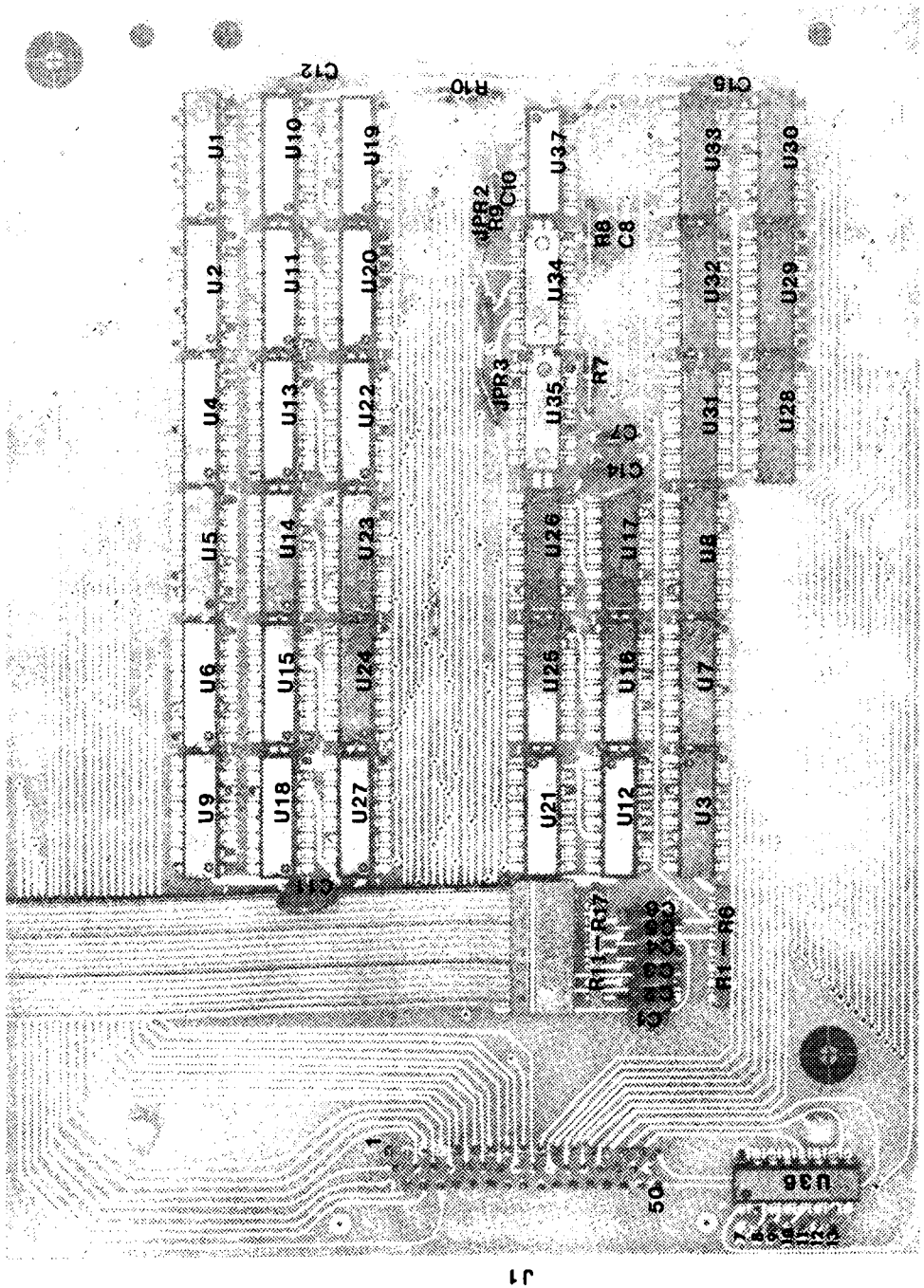
Note: All resistors are 1/4W ± 5%

5-18 PART LOCATION-ASSEMBLY 86-43




+160V
R1 2.2K
R5 6.8K
R9 6.8K
R13 6.8K
R17 6.8K
R21 6.8K
Q2 2N4889
Q4 2N4889
Q6 2N4889
Q8 2N4889
Q10 2N4889
TO PIN "5" U3
R4 430K
R8 430K
R12 430K
R16 430K
R20 430K
R2 68K
R6 68K
R10 68K
R14 68K
R18 68K
Q1 MPSA43
Q3 MPS A43
Q5 MPSA43
Q7 MPSA43
Q9 MPSA43
R3 22K
R7 22K
R11 22K
R15 22K
R19 22K
100 DAY
DAY
HR
MIN.
SEC
E
D
C
B
A
R27 1M
R26 1M
R25 1M
R24 1M
+5V
U7
U6
U5
U4
KA
R33 100
R36 100
D1
D2
D3
D4
BLANKING
M
Q11 2N3904
R22 2.2K
R23 2.2K
U2
U1
DM8880
PR
BL
LEFT DIGIT
RIGHT DIGIT
T
P
R
S
H
F
K
J
Q14 2N3904
J1
Q13 2N3904
R28 33K
R29 33K
R30 33K
R31 33K
R35 33K
C1 .001
C2 .001
C3 .001
C4 .001
4042B
U3
Q15 ** 2N3904
C5 .1
C6 .1
Q12 2N3904
R32 150
+5V
D5
D6
R37 100
(D-O-Y COLONS)
P.W. BOARD 85-43
N
WIRE
W
V
U
R34 150
**
X
D7 **
D8
TO CONNECTION "E"
WEST SATELLITE LOCK MODEL 468-DC ONLY
FRONT PANEL
VB LOCK ON MOD. 60-DC, EAST SATELLITE LOCK ON MODEL 468-DC
FRONT PANEL
LAST USED:
C6
D8
Q15
R37
U7
** USED ON MODEL 469-DC ONLY

5-20 PARTS LOCATION-ASSEMBLY 86-44



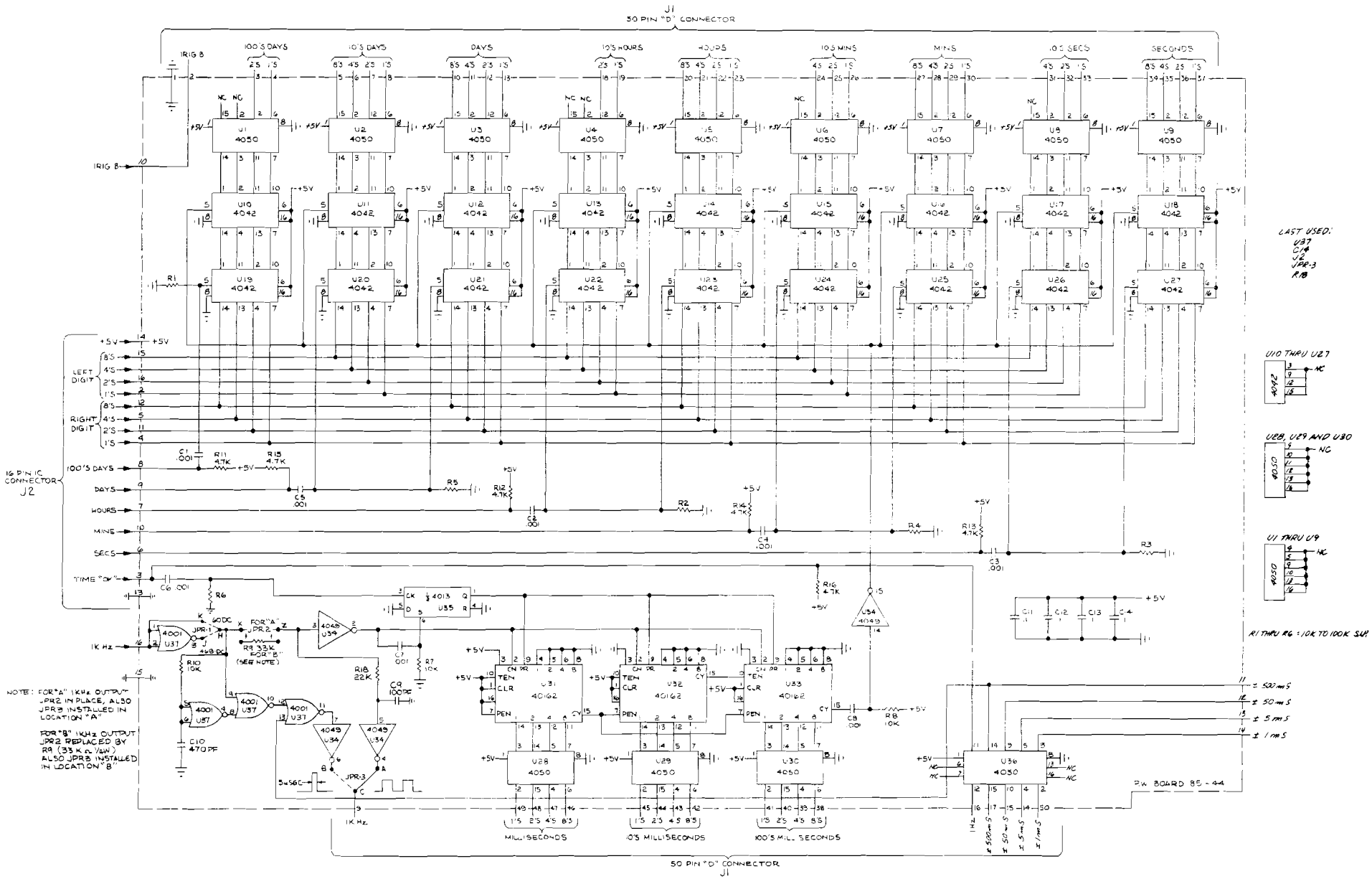
5-21 SYMBOL DESIGNATION REFERENCE 86-44

SYMBOL	TRUE TIME PART #	DESCRIPTION	SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	36-58	Cap. Monolithic .001uf	U14	176-4042	I.C. RCA #4042
C2	36-58	Cap. Monolithic .001uf	U15	176-4042	I.C. RCA #4042
C3	36-58	Cap. Monolithic .001uf	U16	176-4042	I.C. RCA #4042
C4	36-58	Cap. Monolithic .001uf	U17	176-4042	I.C. RCA #4042
C5	36-58	Cap. Monolithic .001uf	U18	176-4042	I.C. RCA #4042
C6	36-58	Cap. Monolithic .001uf	U19	176-4042	I.C. RCA #4042
C7	36-58	Cap. Monolithic .001uf	U20	176-4042	I.C. RCA #4042
C8	36-58	Cap. Monolithic .001uf	U21	176-4042	I.C. RCA #4042
C9	29-33	Cap. Dipped Mica 100pf	U22	176-4042	I.C. RCA #4042
C10	36-50	Cap. Monolithic 470pf	U23	176-4042	I.C. RCA #4042
C11	36-95	Cap. Monolithic 0.1uf	U24	176-4042	I.C. RCA #4042
C12	36-95	Cap. Monolithic 0.1uf	U25	176-4042	I.C. RCA #4042
C13	36-95	Cap. Monolithic 0.1uf	U26	176-4042	I.C. RCA #4042
C14	36-95	Cap. Monolithic 0.1uf	U27	176-4042	I.C. RCA #4042
J1	372-50S	Connector 50 Pin D	U28	176-4050	I.C. RCA #4050
J2	379-16	16 Pin I.C. Connector	U29	176-4050	I.C. RCA #4050
JPR1	2-0	Jumper	U30	176-4050	I.C. RCA #4050
JPR2	2-0	Jumper	U31	176-40162	I.C. RCA #40162
JPR3	2-0	Jumper	U32	I76-40162	I.C. RCA #40162
PWB	85-44	Printed Wiring Board	U33	176-40162	I.C. RCA #40162
R1-R6	11-121	Res. S.I. Package 100K	U34	176-4049	I.C. RCA #4049
R7	2-97	Res. Carbon 10K	U35	176-4013	I.C. RCA #4013
R8	2-97	Res. Carbon 10K	U36	176-4050	I.C. RCA #4050
R9	2-109*	Res. Carbon 33K	U 37	176-4001	I.C. RCA #4001
R10	2-97	Res. Carbon 10K			
R11-R17	11-89	Res. S.I.P. 4.7K			
R18	2-105	Res. Carbon 22K			

*Option replacing JPR-2 (Special Order Only)

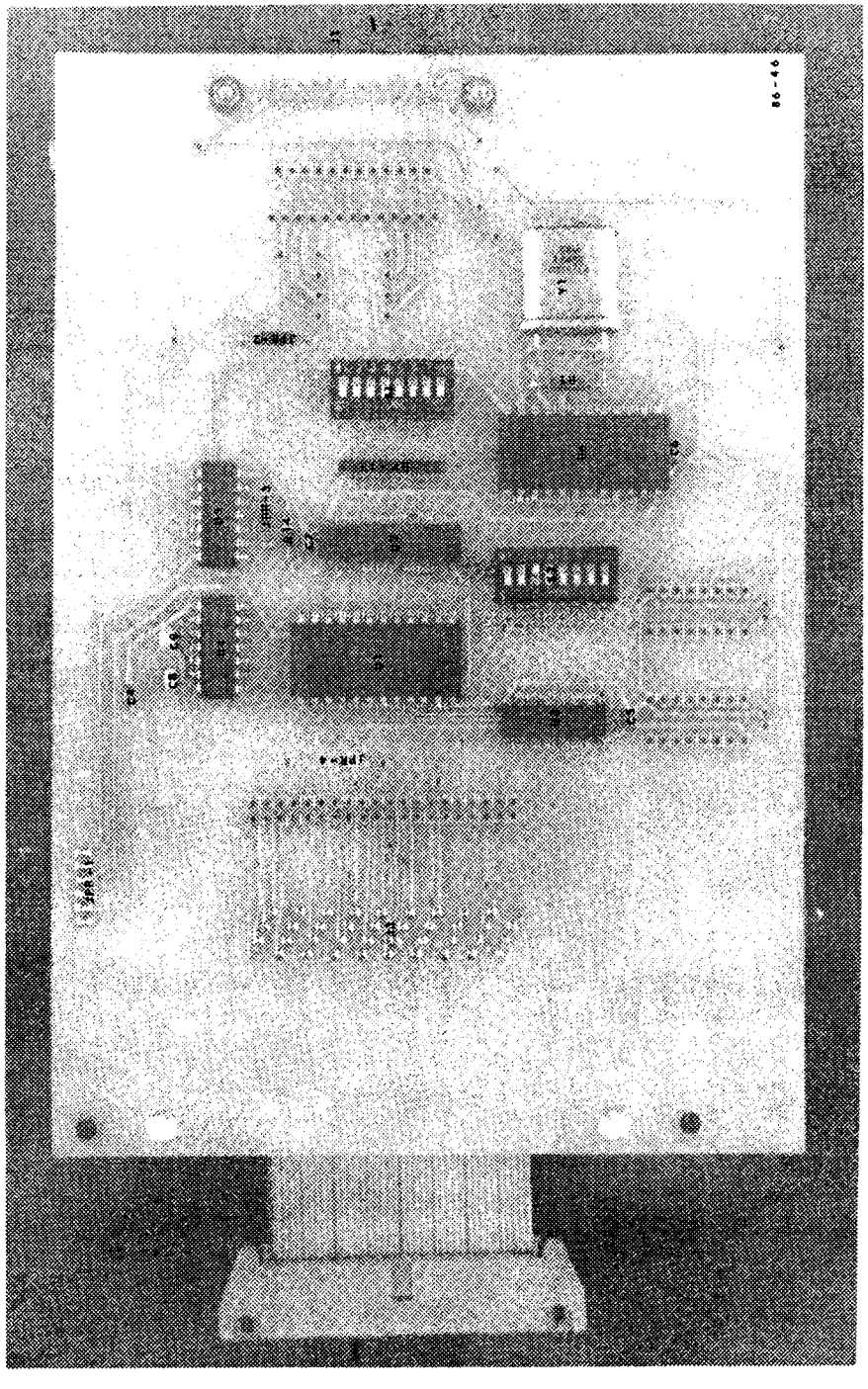
U1	176-4050	I.C. RCA #4050
U2	176-4050	I.C. RCA #4050
U3	176-4050	I.C. RCA #4050
U4	176-4050	I.C. RCA #4050
U5	176-4050	I.C. RCA #4050
U6	176-4050	I.C. RCA #4050
U7	176-4050	I.C. RCA #4050
U8	176-4050	I.C. RCA #4050
U9	176-4050	I.C. RCA #4050
U10	176-4042	I.C. RCA #4042
U11	176-4042	I.C. RCA #4042
U12	176-4042	I.C. RCA #4042
U13	176-4042	I.C. RCA #4042

Note: All resistors are 1/4W ± 5%



5-22 SCHEMATIC-ASSEMBLY 86-44

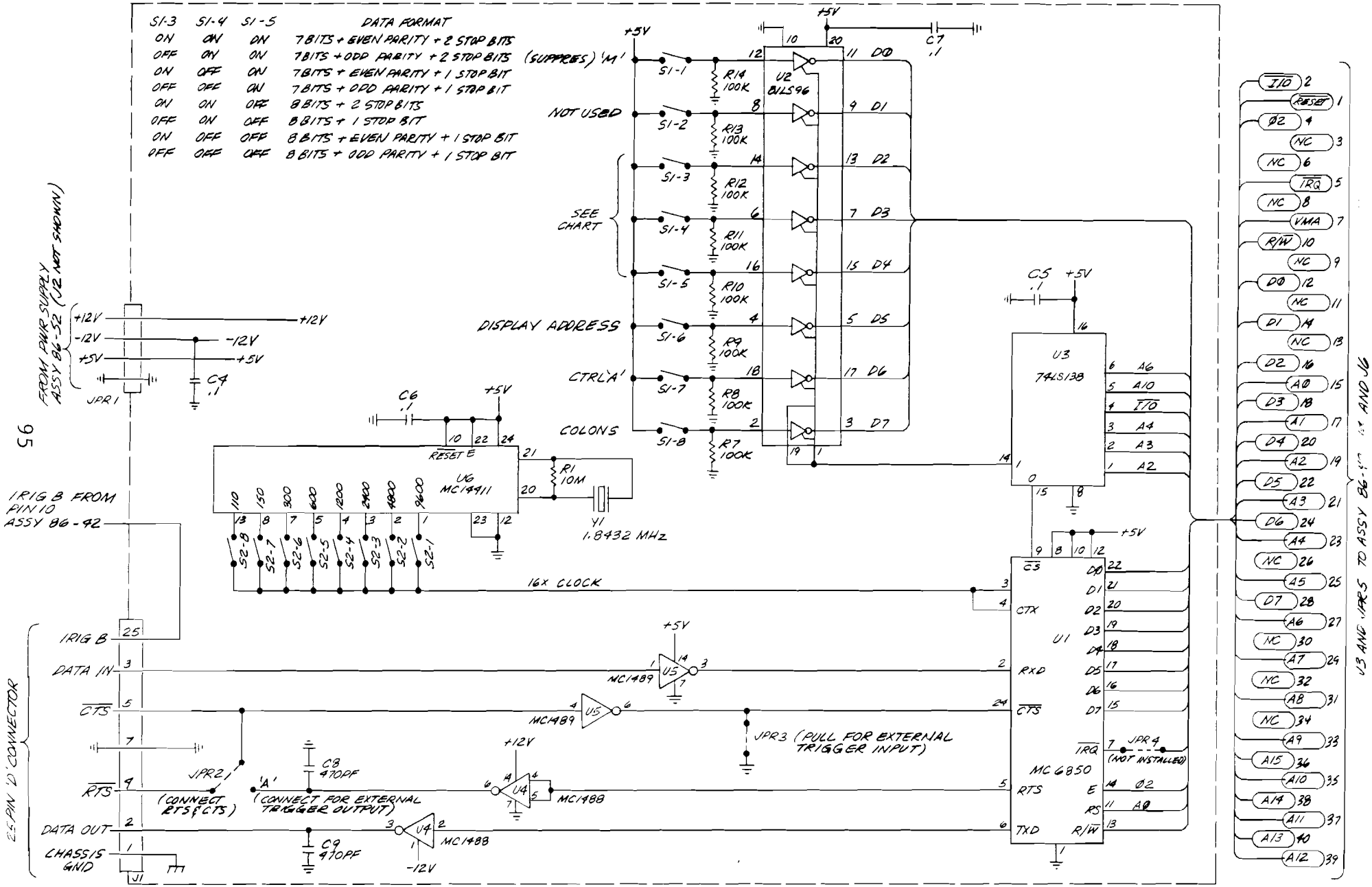
5-23 PARTS LOCATION-ASSEMBLY 86-46



5-24 SYMBOL DESIGNATION REFERENCE 86-46

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1		NOT USED
C2		NOT USED
C3		NOT USED
C4	36-95	Cap. Monolithic .luf
C5	36-95	Cap. Monolithic .luf
C6	36-95	Cap. Monolithic .luf
C7	36-95	Cap. Monolithic .luf
C8	36-50	Cap. Monolithic 470pf
C9	36-50	Cap. Monolithic 470pf
J1	372-25P	Socket 25 Pin 'D'
J2		NOT USED
J3	386-40	Connector, Male, 40pin
J4	385-40	Connector,Female,40pin
JPR-1	317-12	Jumper ½
JPR-2	2-0	Jumper
JPR-3	2-0	Jumper
JPR-4		NOT USED
JPR-5	387-40	Cable,40 cond, 10" long
PWB	85-46	Printed Wiring Board
Q1	175-4	Transistor, MPS 3702
Q2	175-3	Transistor, MPS 2369
R1	2-169	Res. Carbon 10M
R2		NOT USED
R3		NOT USED
R4		NOT USED
R5		NOT USED
R6		NOT USED
R7-R13	11-121	Res. S.I.P. 100K
R14	2-121	Res. Carbon 100K
S1	65-8	Switch, 8 Pos. SPST Dip
S2	65-8	Switch, 8 Pos. SPST Dip
U1	176-6850	I.C. 6850
U2	176-81LS96	I.C. 81LS96
U3	176-74LS138	I.C.74LS138
U4	176-MC1488	I.C. MC1488
U5	176-MC1489	I.C. MC1489
U6	176-MC14411	I.C. MC14411
Y1	59-1843.2	Crystal 1.8432 MHz

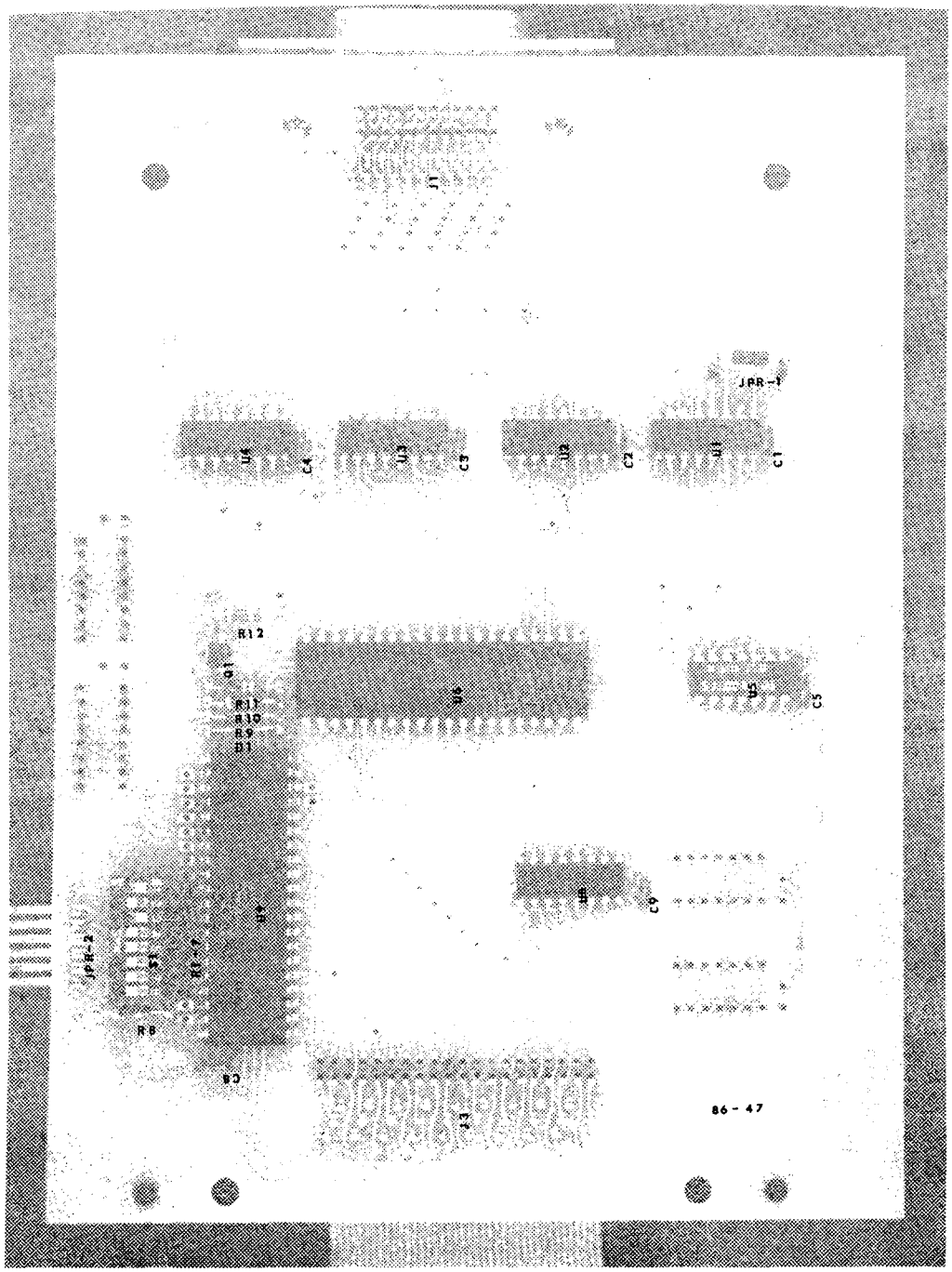
Note: All resistors are 1/4W ± 5%



95

5-25 SCHEMATIC-ASSEMBLY 86-46

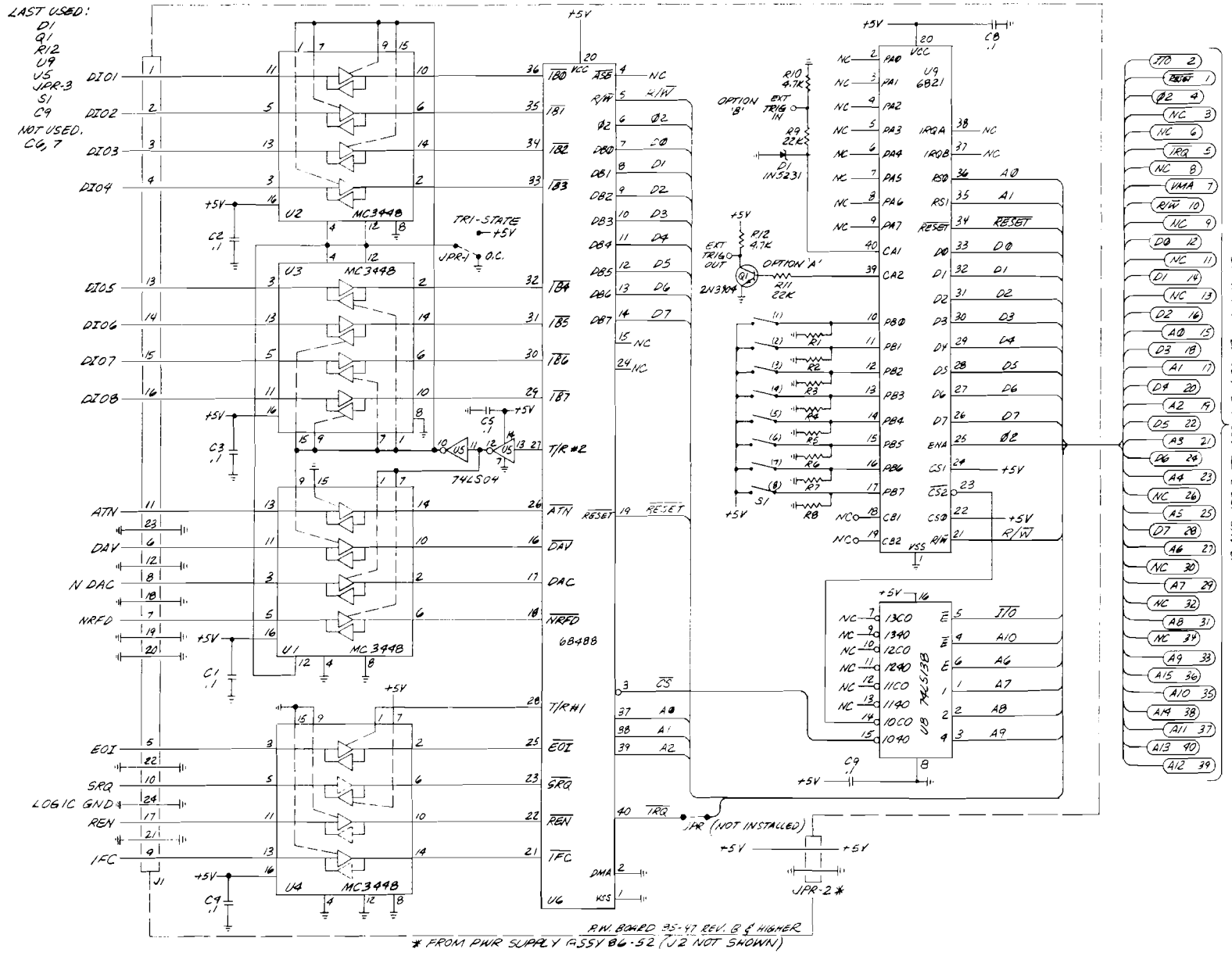
5-27 SYMBOL DESIGNATION REFERENCE 86-47



5-26 PARTS LOCATION-ASSEMBLY 86-47

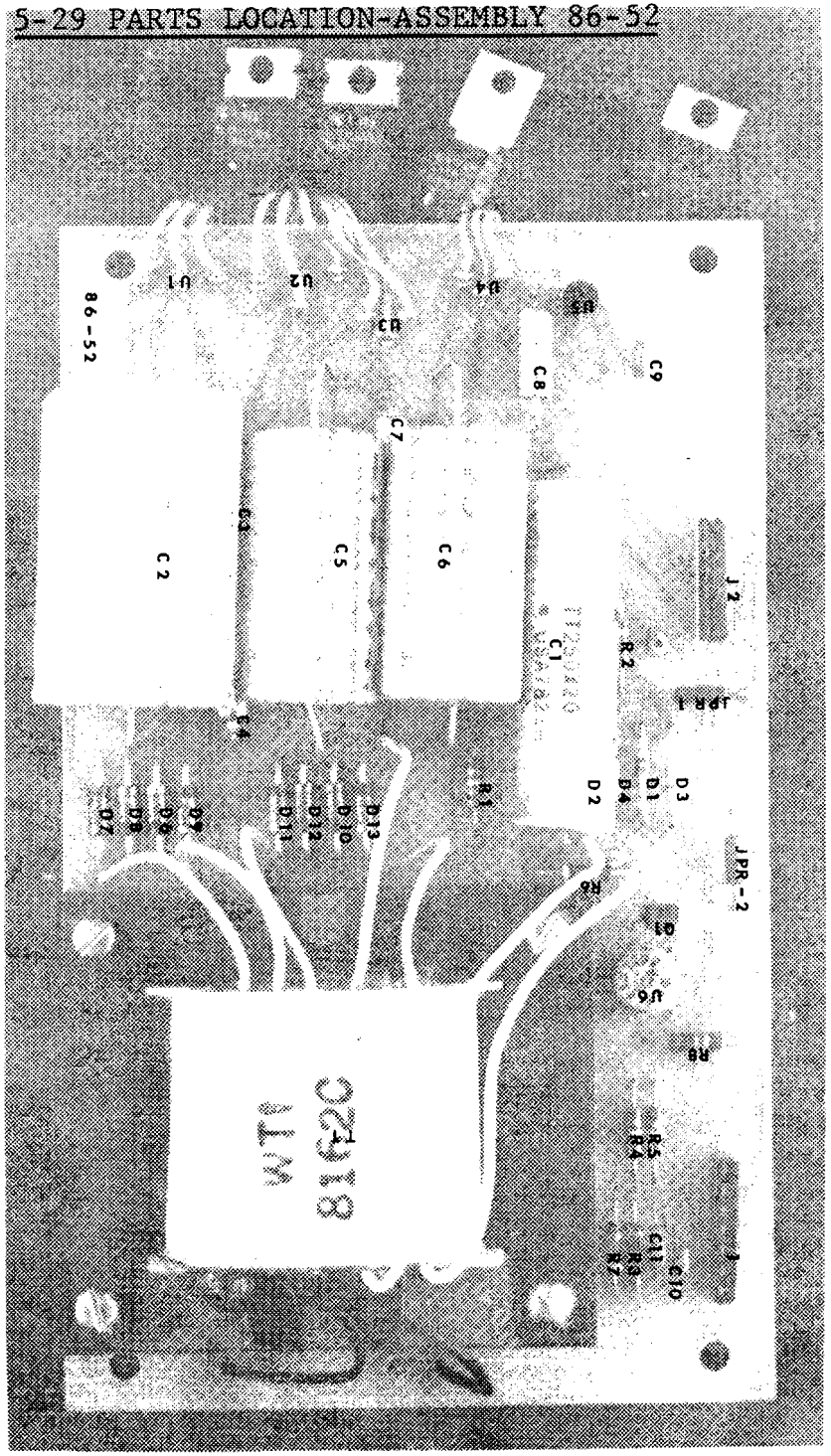
SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	36-95	Cap. Monolithic .luf
C2	36-95	Cap. Monolithic .luf
C3	36-95	Cap. Monolithic .luf
C4	36-95	Cap. Monolithic .luf
C5	36-95	Cap. Monolithic .luf
C6		NOT USED
C7		NOT USED
C8	36-95	Cap. Monolithic .luf
C9	36-95	Cap. Monolithic .luf
D1	55-1	Diode IN5231
J1	388-24	Connector, 24 PIN
JPR-1	2-0	Jumper
JPR-2	317-12	Jumper ½
JPR-3	387-40	Ribbon Cable 40 Cond. 10" long
PWB	85-47	Printed Wiring Board
Q1	175-2	Transistor 2N3904
R1-R7	11-89	Res. S.I. Package 4.7K
R8	2-89	Res. Carbon 4.7K
R9	2-105	Res. Carbon 22K
R10	2-89	Res. Carbon 4.7K
R11	2-105	Res. Carbon 22K
R12	2-89	Res. Carbon 4.7K
S1	65-8	Switch, 8POS SPST DIP
U1	176-3448	I.C. 3448
U2	176-3448	I.C. 3448
U3	176-3448	I.C. 3448
U4	176-3448	I.C. 3448
U5	176-74LS04	I.C. 74LS04
U6	176-68488	I.C. 68488
U7		NOT USED
U8	176-74LS138	I.C. 74LS138
U9	176-6821	I.C. 6821

Note: All resistors are 1/4W ± 5%



5-28 SCHEMATIC-ASSEMBLY 86-47

5-29 PARTS LOCATION-ASSEMBLY 86-52

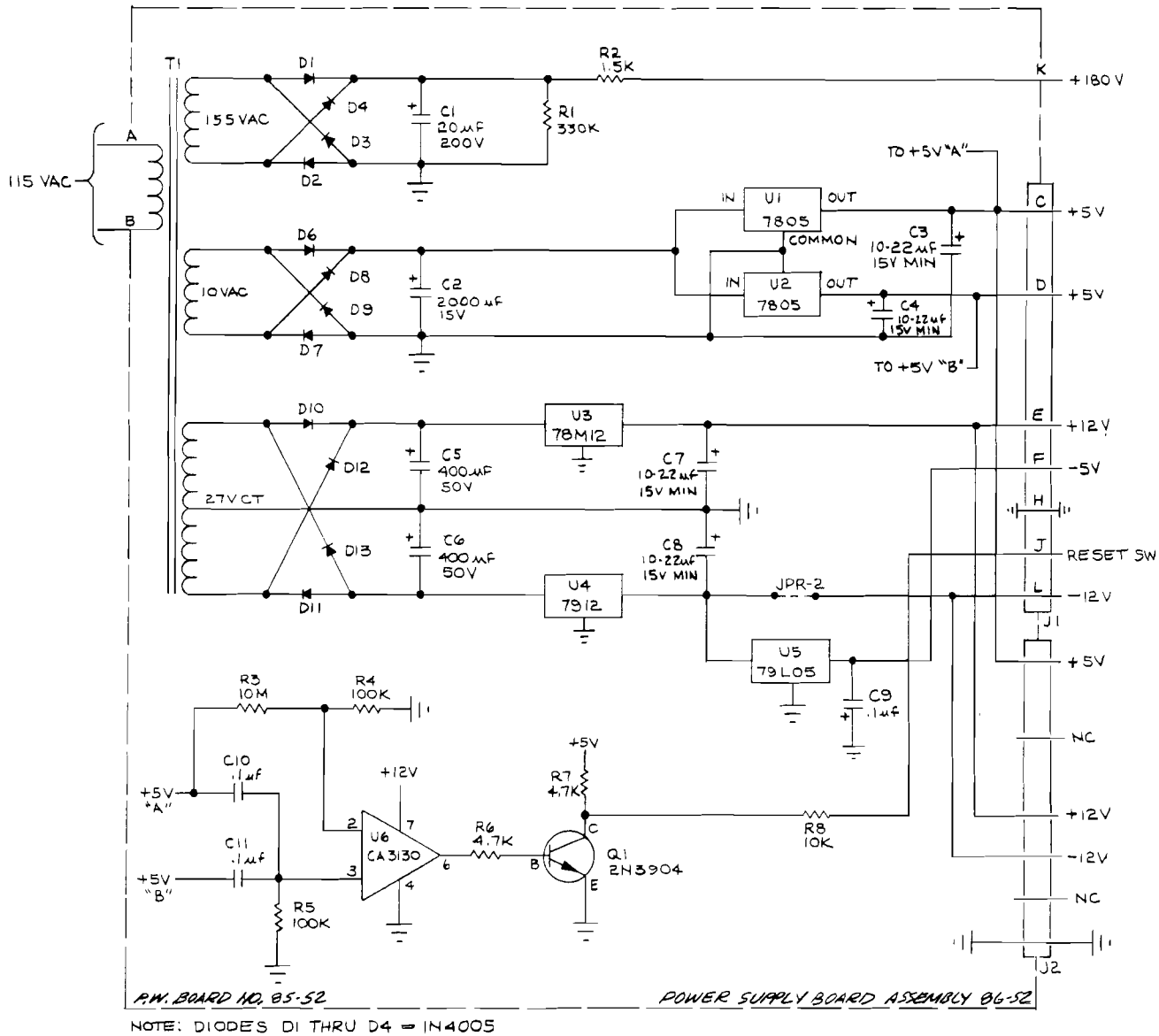


5-30 SYMBOL DESIGNATION REFERENCE 86-52

SYMBOL	TRUE TIME PART #	DESCRIPTION
C1	27-12	Cap. Electro 20uf 200V
C2	28-77	Cap. Electro 2000 uf 15V
C3	27-8-25*	Cap. Alum Electro, 10uf 25V
C4	27-8-25*	Cap. Alum Electro, 10uf 25V
C5	27-28	Cap. Electro 400uf 50V
C6	27-28	Cap. Electro 400uf 50V
C7	27-8-25*	Cap. Alum Electro, 10uf 25V
C8	27-8-25*	Cap. Alum Electro, 10uf 25V
C9	36-95	Cap. Monolithic .1uf
C10	36-95	Cap. Monolithic .1uf
C11	36-95	Cap. Monolithic .1uf
D1	57-3	Diode 1N4005
D2	57-3	Diode 1N4005
D3	57-3	Diode 1N4005
D4	57-3	Diode 1N4005
D5		NOT USED
D6	57-2	Diode 1N4002
D7	57-2	Diode 1N4002
D8	57-2	Diode 1N4002
D9	57-2	Diode 1N4002
D10	57-2	Diode 1N4002
D11	57-2	Diode 1N4002
D12	57-2	Diode 1N4002
D13	57-2	Diode 1N4002
J1	318-7	Socket, 7 Pin Strip
J2	318-6	Socket, 6 Pin Strip
JPR-1	2-0	Jumper
JPR-2	2-0	Jumper
PWB	85-52	Printed Wiring Board
Q1	175-2	Transistors 2N3904
R1	2-133	Resistor Carbon 330K
R2	2-77	Resistor Carbon 1.5K
R3	2-169	Resistor Carbon 10MEG
R4	2-121	Resistor Carbon 100K
R5	2-121	Resistor Carbon 100K
R6	2-89	Resistor Carbon 4.7K
R7	2-89	Resistor Carbon 4.7K
R8	2-97	Resistor Carbon 10K
T1	54-2	Transformer
U1	176-7805	I.C. +5V Reg. FSC 7805UC
U2	176-7805	I.C. +5V Reg. FSC 7805UC
U3	176-78M12	I.C. +12V Reg. FSC 78M12
U4	176-7912UC	I.C. -12V Reg. FSC 7912UC
U5	176-79L05	I.C. 79L05
U6	176-3130	I.C. RCA #CA3130

* Cap. Tant 22uf 15V, Part #32-45 may be used

Note: All resistors are 1/4W ± 5%



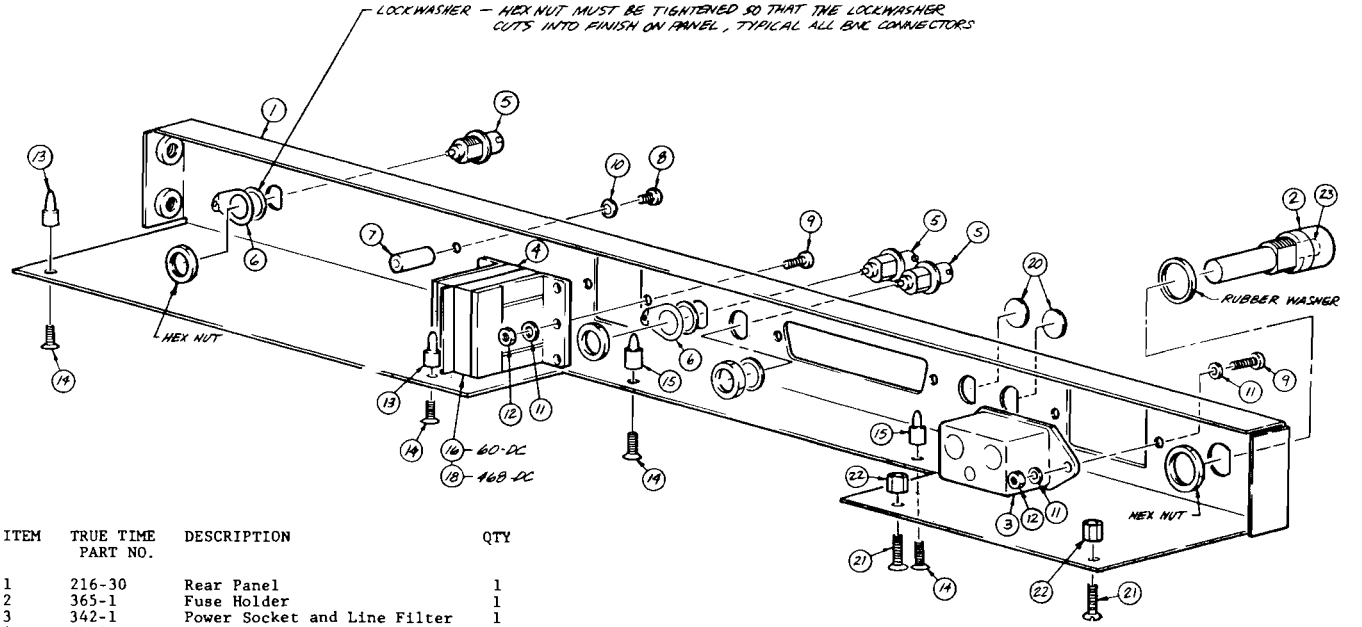
NOT USED:
D5

LAST USED:
D13
R8
C11
Q1
U6
T1
JPR-2
J2

NOTE: DIODES D1 THRU D4 = IN4005
DIODES D6 THRU D13 = IN4002

1. THIS SCHEMATIC IS TO BE USED WITH P.W. BOARD NO. 85-52 REVISION H AND SUBSEQUENT.
NOTE: UNLESS OTHERWISE SPECIFIED

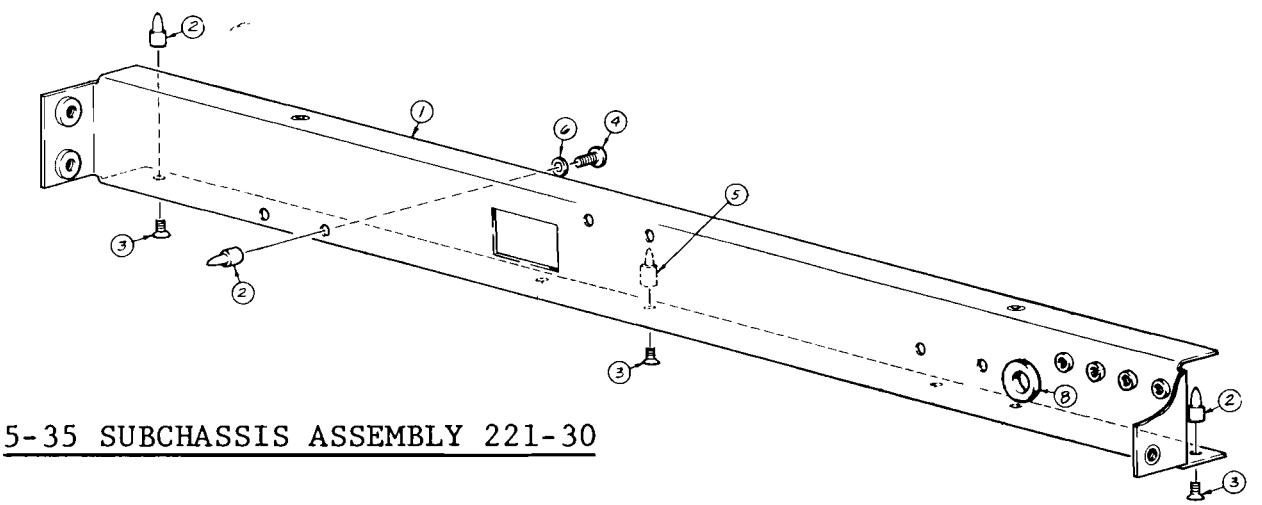
5-31 SCHEMATIC-ASSEMBLY 86-52



5-32 REAR PANEL ASSEMBLY 220-30

ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	216-30	Rear Panel	1
2	365-1	Fuse Holder	1
3	342-1	Power Socket and Line Filter	1
4	61-1	Thumb Wheel Switch	1
5	375-1	BNC Connector	3
6	256-.375	Solder Lug, .375" I.D.	2
7	255-4-4	Spacer, 4-40 x ¼" Threaded	1
8	240-4-2	Screw, 4-40 x ¼" Long PHMS	1
9	240-4-3	Screw, 4-40 x 3/8" Long PHMS	4
10	253-4	Washer #4 Flat	1
11	265-4	Lockwasher #4 Internal	6
12	252-4	Nut 4-40 Hex	4
13	277-2	Spacer, Circuit Board, ¼" Lg	2
14	241-6-2	Screw, 6-32 x ¼" Long PHMS	4
15	277-6	Spacer, Circuit Board 3/8" lg	2
16		NOT USED	
17		NOT USED	
18	61-2	Thumb Wheel (+ and -)	1
19	134-24	Wiring Harness (not shown)	1
20	274-1	Plug, Hole	A/R
21	241-6-5	Screw, 6-32 x 5/8" Long FHMS	2
22	255-6-2	Spacer, 6-32 x ½" Long Alum	2
23	363-.750	Fuse, 3 AG , 3/4A	1

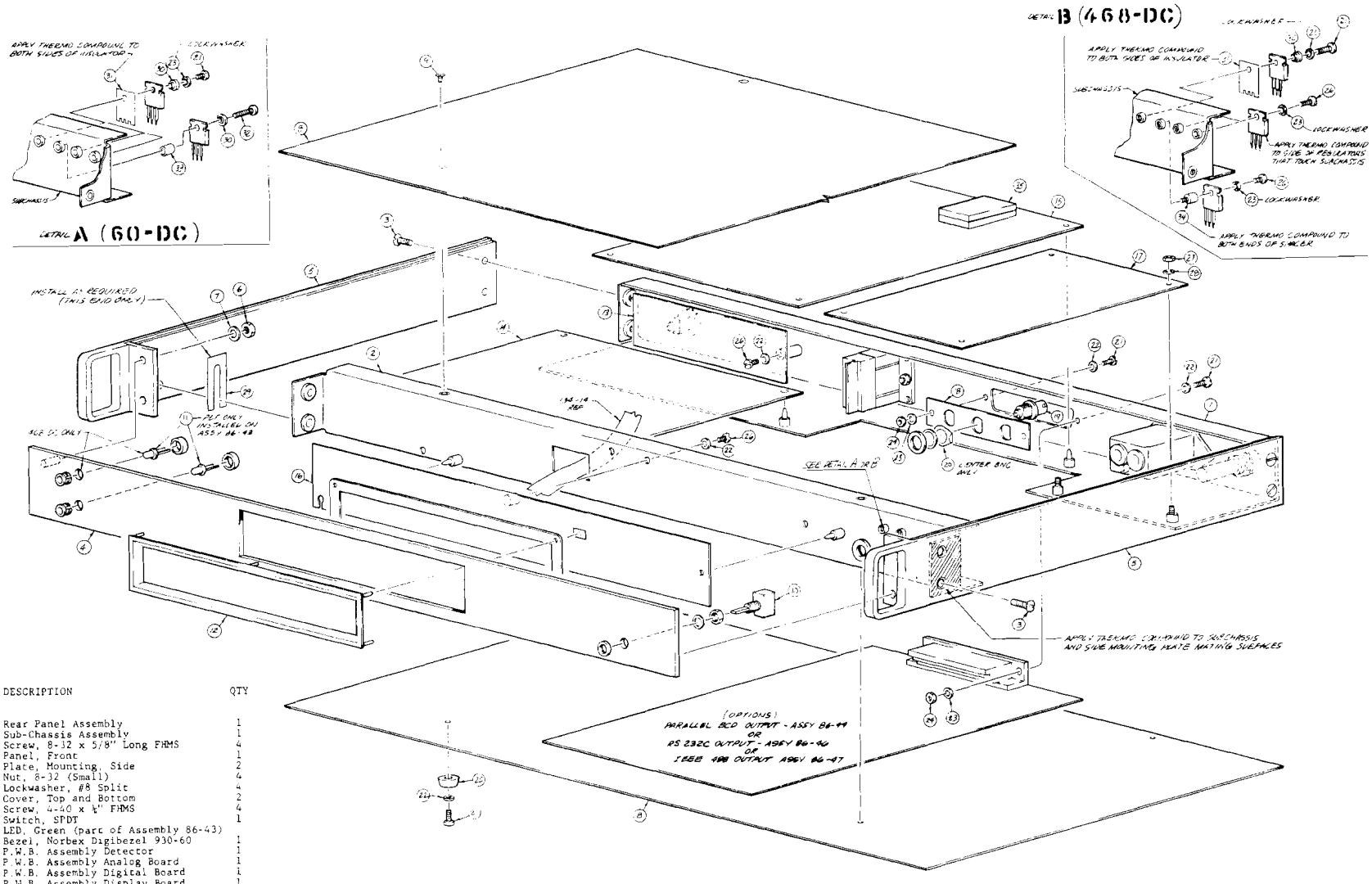
5-33 PARTS LIST 220-30



ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	215-30	Sub-Chassis	1
2	277-2	Spacer, P.W. Board ¼" Long	6
3	241-6-2	Screw, 6-32 x ¼" Long FHMS	6
4	240-6-2	Screw, 6-32 x ¼" Long PHMS	2
5	277-6	Spacer, P.W. Board, 3/8" Lg.	2
6	253-6	Washer, #6 Flat	2
7	282-1	Adhesive, Locktite	A/R
8	73-18	Grommet, Rubber	1

5-34 PARTS LIST 221-30

5-35 SUBCHASSIS ASSEMBLY 221-30

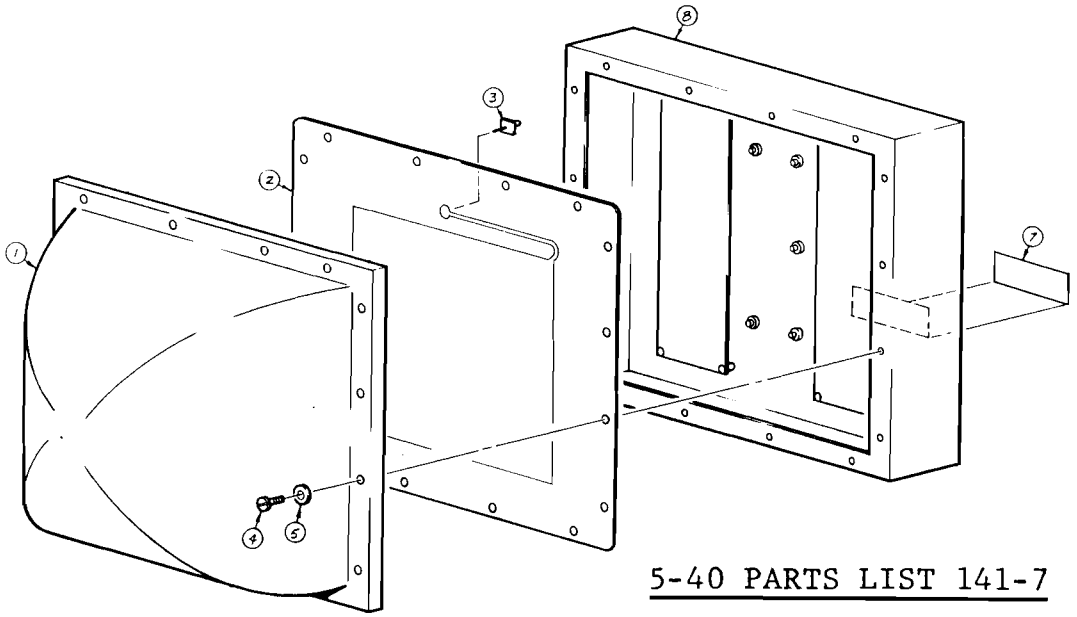


5-36 MODEL 468-DC FINAL ASSEMBLY 151-70

ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	220-30	Rear Panel Assembly	1
2	221-30	Sub-Chassis Assembly	1
3	241-8-5	Screw, 8-32 x 5/8" Long FHMS	4
4	100-70	Panel, Front	1
5	217-30	Plate, Mounting, Side	2
6	252-8	Nut, 8-32 (Small)	4
7	254-8	Lockwasher, #8 Split	4
8	203-6	Cover, Top and Bottom	2
9	249-1	Screw, 4-40 x ¼" FHMS	4
10	60-1	Switch, SPDT	1
11		LED, Green (part of Assembly 86-43)	
12	210-2	Bezel, Norbex Digibezel 930-60	1
13	86-73	P.W.B. Assembly Detector	1
14	86-74	P.W.B. Assembly Analog Board	1
15	86-42	P.W.B. Assembly Digital Board	1
16	86-43	P.W.B. Assembly Display Board	1
17	86-52	P.W.B. Assembly Power Supply	1
18	206-30	Plate, BNC Mounting	1
19	375-1	BNC Connector	3
20	256-.375	Solder Lug, .375" I.D.	1
21	240-4-3	Screw, 4-40 x 3/8" Long PHMS	7
22	253-4	Washer, #4 Flat	8
23	265-4	Lockwasher, #4 Internal	6
24	252-4	Nut, 4-40 Hex	2
25	261-1	Feet, Rubber	4
26	240-4-2	Screw, 4-40 x ¼" Long PHMS	5
27	252-6	Nut, 6-32 Hex	2
28	265-6	Lockwasher, #6 Internal	2
29	263-1	Shim, Chassis	A/R
30	271-4	Washer, Shoulder	1
31	272-1	Insulator, MICA	1
32		NOT USED	
33		NOT USED	
34	255-100	Spacer, 4-40 X ¼"Long	1
35	176-2716	I.C. Intel #2716	1
36	249-1	Screw, 4-40 x ¼" FHSC	4
37	332-2	Cord, Power (not shown)	1
38	206-1	Bracket, Rack Mounting	2
39	400-1	Nameplate, Product I.D.	1

5-37 PARTS LIST 151-70

5-38 MODEL A-468MS FINAL ASSEMBLY 142-70



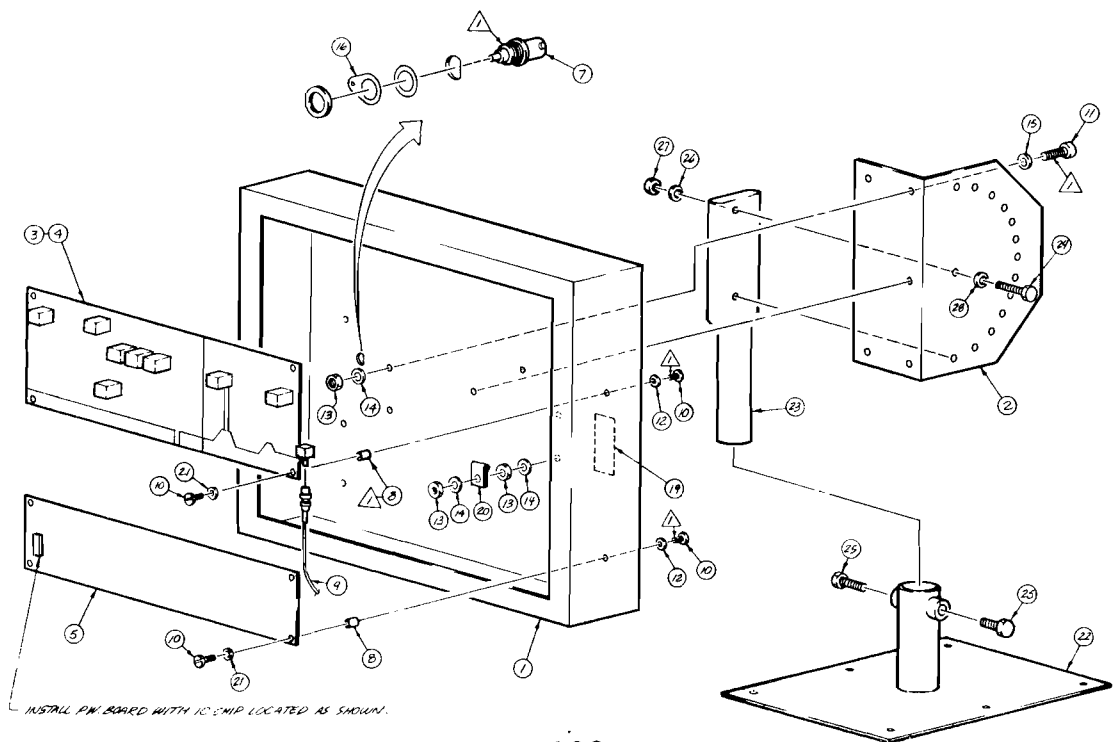
5-39 PARTS LIST 142-70

ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	227-8	Cover, Plastic Bubble	1
2	85-12	Antenna, Flat Plate	1
3	381-1	Receptacle, Jack	1
4	240-8-4	Screw, #8 x ¼" Lg. PHST	17
5	266-8	Washer, Seal	17
6	285-1	Sealant, Silicone	A/R
7	400-1	Label, Product I.D.	1
8	141-7	Subassembly, Antenna	1

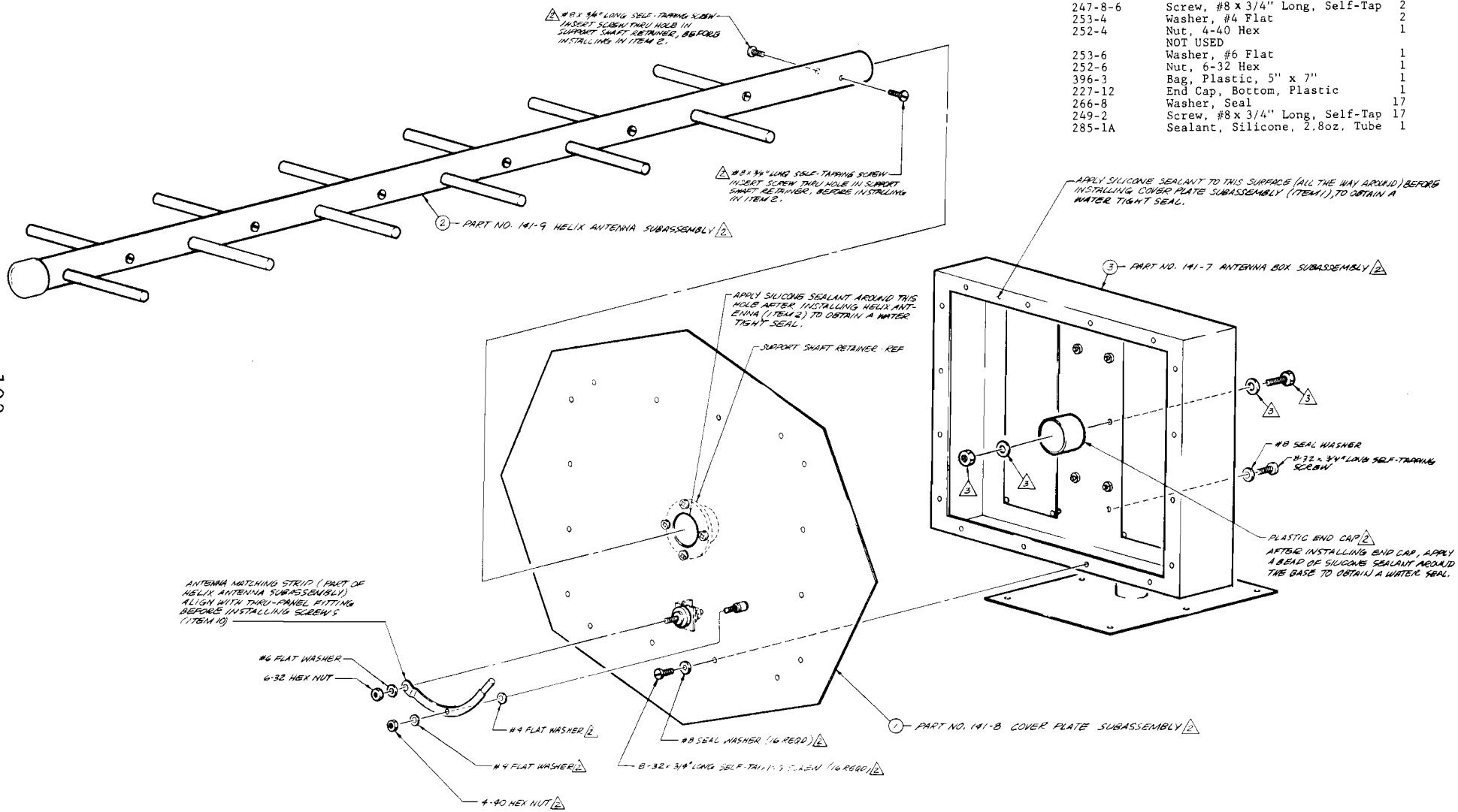
5-40 PARTS LIST 141-7

ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	138-3	Box, Antenna Housing	1
2	138-16	Pivot Bracket, Ant. Mounting	1
3	86-70	Printed Wiring Board, RF	1
4	86-71	Printed Wiring Board, RF	1
5	86-72	Printed Wiring Board, IF	1
6	134-20	Wiring Harness (not shown)	1
7	375-1	BNC Connector	1
8	255-4-3	Spacer, 4-40 x 3/8" Long, Alum.	1
9	339-12	Cable Assembly, Coax, 12" long	1
10	240-4-2	Screw, 4-40 x ¼" Long, PHMS	20
11	248-10-5	Screw, 10-32 x 1" Long, Hex Hd.	5
12	253-4	Washer, #4 Flat	10
13	252-10	Nut, 10-32 Hex	6
14	254-10	Lockwasher, #10, Split	5
15	253-10	Washer, #10 Flat	6
16	256-.375	Solder Lug .375" I.D.	1
17	285-1	Sealant, Silicone (not shown)	A/R
18	282-1	Adhesive, Locktite(not shown)	A/R
19	400-1	Label, Product I.D.	1
20	230-.,	Clamp, 1/8" Cable, Nylon	1
21	265-4	Lockwasher, #4 Internal	10
22	138-14	Base, Antenna Mounting	1
23	138-15	Pedestal, Antenna Mounting	1
24	231-.250-10	Bolt, ¼-20 x 1¼" Long, Hex Head	2
25	231-.250-5	Bolt, ¼-20 x 5/8" Long, Hex Head	2
26	254-.250	Lockwasher, .25 I.D. Split	2
27	252-.250	Nut, ¼-20 Hex	2
28	253-.250	Washer, Flat .250 I.D.	2
29	138-11	Antenna Mounting Hardware Kit (not shown)	1

5-41 A-468 SUBASSEMBLY 141-7



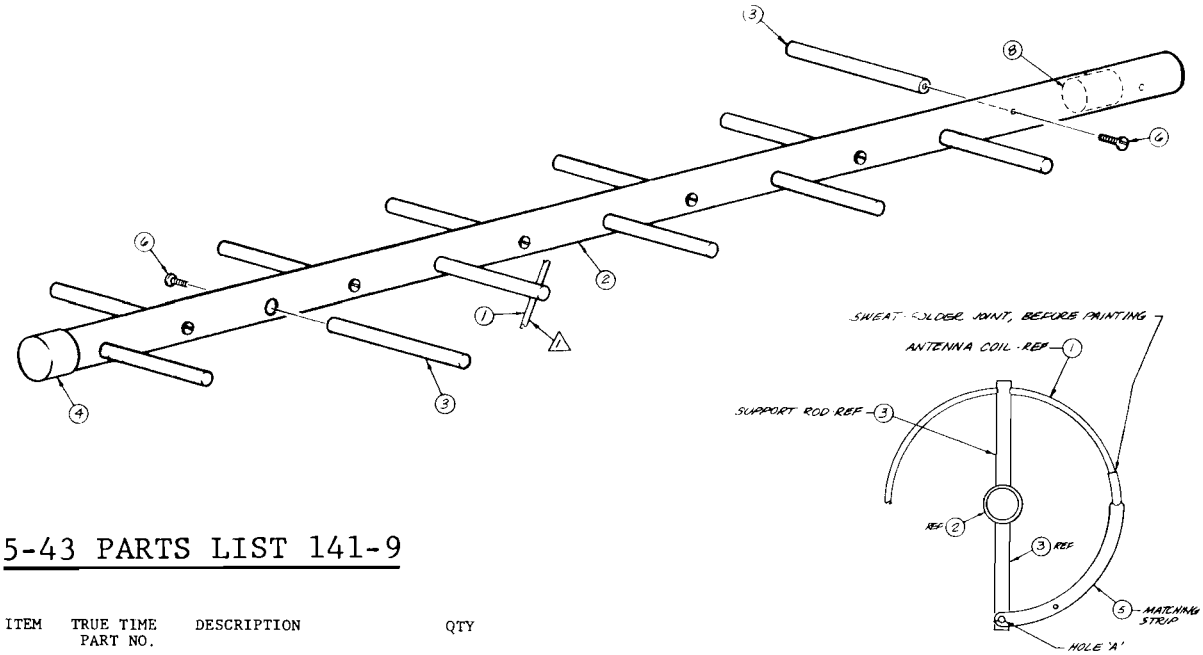
5-47 MODEL A-468HX FINAL ASSEMBLY 142-71



5-46 PARTS LIST 142-71

ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	141-8	Subassembly, Cover Plate	1
2	141-9	Subassembly, Helix Antenna	1
3	141-7	Subassembly, Antenna Box	1
	247-8-6	Screw, #8 x 3/4" Long, Self-Tap	2
	253-4	Washer, #4 Flat	2
	252-4	Nut, 4-40 Hex	1
		NOT USED	
	253-6	Washer, #6 Flat	1
	252-6	Nut, 6-32 Hex	1
	396-3	Bag, Plastic, 5" x 7"	1
	227-12	End Cap, Bottom, Plastic	1
	266-8	Washer, Seal	17
	249-2	Screw, #8 x 3/4" Long, Self-Tap	17
	285-1A	Sealant, Silicone, 2.8oz. Tube	1

5-42 HELIX ANTENNA COIL ASSEMBLY 141-9



5-43 PARTS LIST 141-9

ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	138-8	Coil, Helix Antenna	1
2	138-6	Support Shaft, Aluminum	1
3	227-11	Support Rod, Plastic	12
4	227-13	End Cap, Top, Plastic	1
5	138-17	Strip, Antenna Matching	1
6	247-8-6	Screw, #8 x 3/4" Lg. PHST	12

5-44 PARTS LIST 141-8

ITEM	TRUE TIME PART NO.	DESCRIPTION	QTY
1	138-4	Cover, Antenna Box	1
2	227-10	Retainer, Support Shaft, Plastic	1
3	206-27	Bracket, Receptacle Mounting	1
4	381-1	Receptacle, Flange Mounted	1
5	276-1	Bushing, Thru Panel	1
6	270-4-8	Spacer, #4 x ½" Long, Nylon	1
7	240-2-2	Screw, 2-56 x ¼" Long PHMS	2
8	240-4-7	Screw, 4-40 x 7/8" Long PHMS	1
9	240-8-6	Screw, 8-32 x 3/4" Long PHMS	4
10	265-2	Lockwasher, #2 Internal	2
11	266-8	Washer, Seal	4
12	265-8	Lockwasher, #8 Internal	4
13	271-4	Washer, #4 Shoulder, Nylon	2
14	252-2	Nut, 2-56 Hex	2
15	252-4	Nut, 4-40 Hex	1
16	252-8	Nut, 8-32 Hex	4
17	256-6	Solder Lug, #6	1
18	282-1	Locktite Adhesive (Not Shown)	A/R
19	285-1	Sealant, Silicone (Not Shown)	A/R

5-45 MODEL A-468HX SUBASSEMBLY 141-8