SEMICONDUCTOR DIODES AND TRANSISTORS

PROGRAMED INSTRUCTION

MANUFACTURERS OF CATHODE-RAY OSCILLOSCOPES

VOLUME 7
REFERENCE FOR VOLS. 4-5

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SEMICONDUCTOR DIODES AND TRANSISTORS

VOLUME 7

REFERENCE FOR VOLUMES 4 AND 5

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SEMICONDUCTOR DIODES AND TRANSISTORS

VOLUME 7

REFERENCE TO VOLUMES 4 and 5

This volume is about some approaches to circuit analysis of transistorized amplifier and switching configurations. It is designed as a reference volume for Volumes 4 and 5 of the Semiconductor Diodes and Transistors Programed Instruction Series. It covers the application of basic analysis approaches to transistor configurations and circuits. It deals with the substitution of equivalent circuits for semiconductor devices in order to solve for gains, impedance levels, and the prediction of the operation of the transistors when placed in a specific configuration. It also covers some useful and time-saving approximations that allow prediction of the approximate characteristics of semiconductor devices in amplifier and switching configurations when exactness is not a prerequisite.

PREREQUISITES:

This volume assumes the reader's completion of Semiconductor Diodes and Transistors, Volume 6, or Volumes 1, 2, and 3, or their equivalent. It further assumes the learner's knowledge and ability to apply to the solution of problems: basic voltage and current divider theory, Kirchhoff's voltage and current laws, Thevenin's Theorem, Norton's Theorem, Millman's Theorem, and an equivalent circuit approach to circuit analysis. If the reader does not have this background, some outside study is indicated before starting this volume.

OBJECTIVES:

Since specific educational objectives are difficult to specify and measure with a text-type publication, specific educational objectives will be neglected for this volume. Specific measurable objectives are possible with programed instruction, and Volumes 4 and 5 of this series have specific objectives listed. Volumes 4 and 5 contain much the same information as this text in a programed instruction approach. This volume is primarily designed as a reference and supplement for Volumes 4 and 5 of the programed instruction series.

The broad objective of this program is to provide the learner with convenient reference material for Volumes 4 and 5 of the programed instruction series. This book is complete in itself, however, and can be used without Volumes 4 and 5. Therefore, they are not listed as prerequisites.

SECTION ONE

The preceding volumes have more or less concentrated on the diode and transistor as a device. This volume deals with the diode and the transistor as a circuit component. This volume deals with the analysis of circuit configurations which contain diodes and transistors. Approaches are covered for the prediction of gains, impedances, and quiescent d-c levels of semiconductors in circuit configurations.

Some circuit analysis has already been discussed. The sections in previous volumes that dealt with load lines on the characteristic curves of a transistor were dealing with circuit analysis. Graphical circuit analysis is one approach to solving a transistor or diode circuit configuration. There are many other approaches which will be discussed in this volume, along with the continuance of the graphical analysis. Signal or a-c load lines will be discussed along with the insertion of a model or equivalent circuit to represent the semiconductor device in a configuration.

Table 8 in Volume 6 is an example of representing the transistor with a model. In Table 8 in Volume 6, the model was an attempt to relate the physical attributes of the device to electrical characteristics.

The symbol used for the transistor is one form of model. The lines and so forth in the symbol for the transistor indicate the emitter, base, and collector of the transistor and also indicate the type of transistor. This simple model in most cases does not give sufficient information on the transistor to make predictions as to its operation in the circuit. It does indicate the type (NPN, PNP) of transistor and its orientation in the circuit.

This simple model must be replaced with a more complex model if this will facilitate the analysis of the transistor configuration. The more complex models should give information that will allow the use of the basic electrical laws and theorems

in the solution of the semiconductor configuration. If the basic laws and theorems are limited to linear (current and voltage have a direct relationship) configurations, the non-linear transistor or diode configuration may require that incremental measurements are made to obtain parameters for the model. This will keep the measurements as linear as possible so that the basic laws and theorems can be used.

One of the most important factors when approaching the analysis of semiconductor circuit configurations is to remember that the basic theorems and laws can still be used. Persons first approaching semiconductor configurations for analysis are sometimes overwhelmed by the fact that semiconductors are in the circuit and forget that all of the basic laws have not been repealed. Ohm's Law, Kirchhoff's Law, Thevenin's Theorem, Norton's Theorem, Millman's Theorem may all be applied to the semiconductor configuration as well as to the vacuum tube circuit and the circuit configuration that does not contain active components. If this is kept in mind, analysis of a semiconductor configuration is greatly simplified.

SEMICONDUCTOR MODELS:

It is often convenient for analysis to substitute a model or equivalent circuit for the transistor or semiconductor device. One should not let the multitude of models or equivalent circuits put forth by authors on semiconductor circuits overwhelm him. The model should simplify or facilitate the analysis of a semiconductor configuration and, if it does not, should be avoided. A person attempting to use an equivalent circuit or a model for the transistor should thoroughly understand what the model is representing and not allow the model to be a confusion factor. On first investigating the analysis of semiconductor configurations, one might encounter the hybrid equivalent circuit, the T equivalent circuit, the lumped diffusion model, and Ebers-Moll models, and become thoroughly confused and overwhelmed by the multitude of information they feel they must absorb. It is the opinion of this writer that if the model does not simplify or facilitate the analysis of the semiconductor configuration, it should not be used. One should select the model or equivalent circuit that simplifies the analysis approach for the individual. In many cases, substituting a model for the semiconductor device will not be necessary once the analysis approach is understood. Approximate approaches to

analysis will be sufficient for the particular analysis encountered. Many technicians find that once the exact approaches to analysis are understood, they can accept the approximate approaches and use them to facilitate their work with semiconductor configurations.

This volume will deal with many approaches to analysis of semiconductor amplifier and switching configurations. It will then deal with approximate approaches that may be used when exactness is not a prerequisite. It should be remembered that these are not given as the way to approach a semiconductor circuit, but simply a way to approach the circuit. Several approaches will be covered to give the reader a selection of approaches from which he can select that approach which to him seems to facilitate the analysis of the configuration. This volume will also stress the use of the basic theorems and laws and applying them to transistor and diode configurations.

As an example to illustrate the use of the basic laws and theorems with semiconductor circuits, consider the configurations in Figure 1. Figure 1 is circuitry in a power supply in a Tektronix oscilloscope. Notice the use of silicon rectifiers in a bridge-type configuration (D642 and D612 A, B, C, D) and of transistors being used in essentially a single-ended power amplifier configuration for regulation purposes. Without any information on the parameters or characteristics of the transistors, we will attempt to find out a few things about the circuitry. Our only model will be the transistor symbol as shown in the schematic diagram in Figure 1.

First of all, the a-c input voltage applied to the primary of the transformer is stepped to the desired secondary level and applied to the bridge rectifier circuits made up of D642 and D612 A, B, C, and D. At the output points of the bridge rectifiers, there is pulsating d-c and the pulsations are partially filtered by C642 and C612. The output voltage is regulated by the transistor configuration. The upper diagram in Figure 1 is a -15v supply, and the lower diagram is a -75v supply. To gain some insight on the circuit in Figure 1, we might find any convenient starting point. Knowing nothing about the transistors, let's first look at the upper diagram and note that the emitter of Q667 is at ground potential. You may recall from the earlier volumes that the voltage across the emitter base of the transistor (assuming the transistor is on) is only a few tenths of a volt; therefore, the base of Q667 must be very near ground. This means the emitter of Q663 is also very near

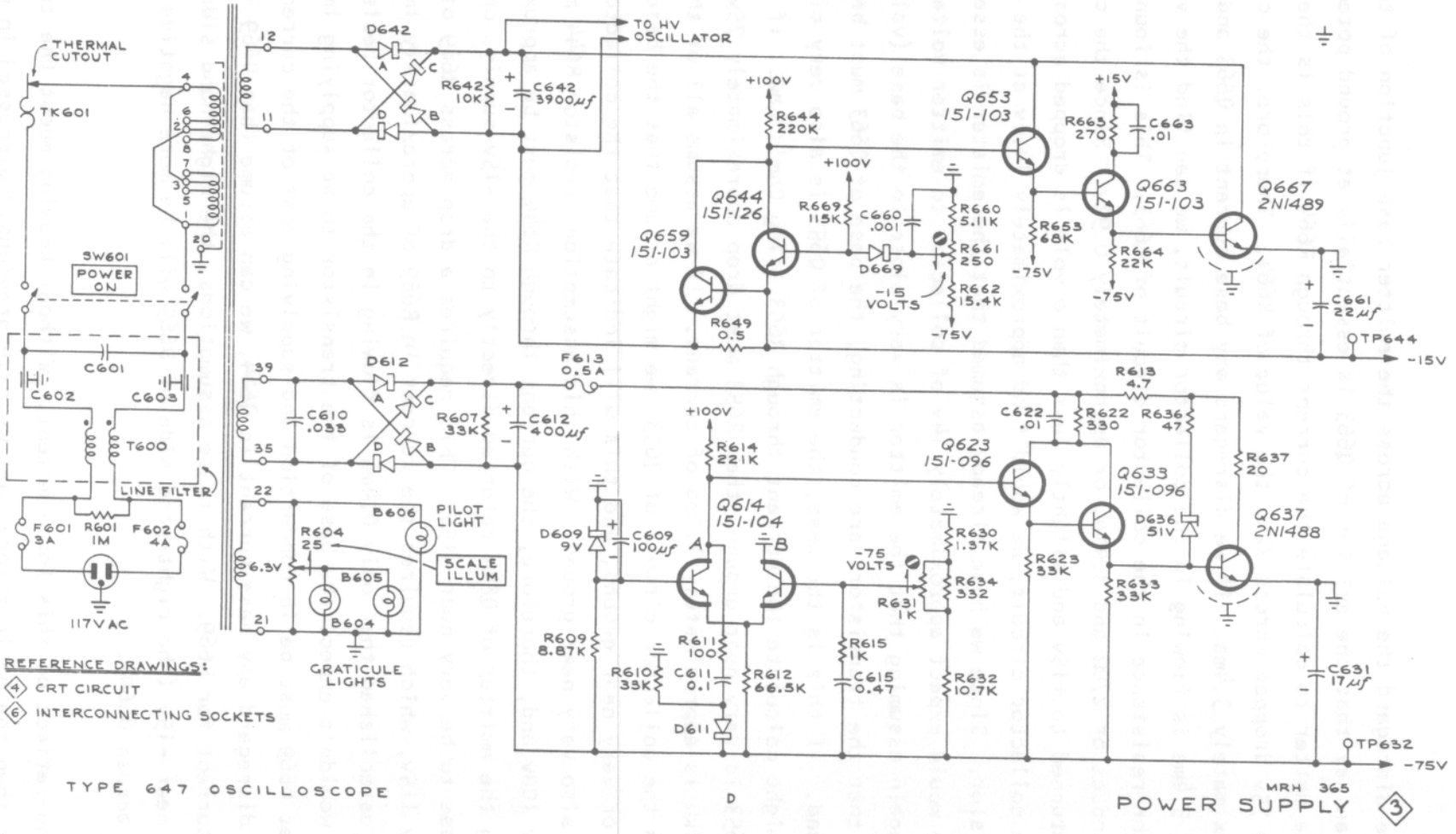

THERMAL CUTOUT
TK601
SW601 POWER ON
C601
C602
C603
T600
LINE FILTER
F601 3A
R601 1M
F602 4A
117VAC
D642
R642 10K
C642 3900µf
TO HV OSCILLATOR
+100V
R644 220K
Q653 151-103
+15V
R665 270
C663 .01
Q644 151-126
Q659 151-103
R669 115K
C660 .001
D669
R660 5.11K
R661 250
R662 15.4K
-15 VOLTS
R649 0.5
R653 68K
-75V
Q663 151-103
R664 22K
Q667 2N1489
C661 22µf
TP644
-15V
D612
C610 .033
R607 33K
C612 400µf
F613 0.5A
R613 4.7
C622 .01
R622 330
R636 47
R614 221K
Q623 151-096
Q633 151-096
R637 20
Q614 151-104
D609 9V
C609 100µf
R630 1.37K
R623 33K
D636 51V
Q637 2NI488
R634 332
R631 1K
R633 33K
R609 8.87K
R611 100
R610 33K
C611 0.1
R612 66.5K
R615 1K
C615 0.47
R632 10.7K
C631 17µf
D611
TP632
-75V
B606 PILOT LIGHT
R604 25
SCALE ILLUM
B605
B604
6.3V
GRATICULE LIGHTS
REFERENCE DRAWINGS:
4 CRT CIRCUIT
6 INTERCONNECTING SOCKETS
TYPE 647 OSCILLOSCOPE
D
MRH 365
POWER SUPPLY 3

FIGURE 1

ground. If we disregard the voltage across the emitter base junction of the transistors, we can say that the emitter of Q663 is essentially at ground potential. It is a simple matter to calculate the current through R664 if this is the case. There will be 75v dropped across 22k, the value of R664. Therefore, the current will be approximately 3.4ma. If we disregard any base current in Q663 and assume that the full 3.4ma is flowing in the collector circuit, we can find the voltage drop across the resistance in the collector circuit of Q663. This is found by taking the product of 270Ω and 3.4ma, or approximately 0.92v. Since the collector of Q663 is returned to +15v and slightly less than a volt is dropped across the resistor in the collector circuit, we would find approximately 14.1v at the collector of the transistor. Since we have already assumed that the emitter is essentially at ground, we would expect approximately 14v of collector to emitter voltage on Q663. Once again assuming that the emitter is very close to the base (voltage-wise) and assuming that the transistors are conducting, the base of Q663 must be very close to ground. If this is the case, the emitter of Q653 is also very close to ground. We might calculate the current through R653 using Ohm's Law. If the emitter of Q653 is very near ground, then R653 must drop approximately 75v. 75v divided by 68kΩ is approximately 1.1ma of current. If we assume all of this current is flowing in the collector circuit of Q653, we might assume that the base of Q653 is at ground or very near ground, and this will indicate that the collector of Q644 and Q659 are also very near ground. With this assumption, resistor R644 must drop approximately 100v and, therefore, the current through R644 must be approximately 0.45ma. With the emitter of Q644 returned directly to the -15v supply, one might expect the base to be very near -15v. This requires a drop across R669 of approximately 115v, which requires the current in R669 of approximately 1ma. We have already established that only 0.4ma is flowing in the collector resistor, so we certainly wouldn't expect the base of the transistor to be supplying 1ma. This indicates that D669 must be in conduction and supplying most of the current for R669. If we disregard any base current in Q644, we can assume that D669 is supplying all the current for R669. With these assumptions, the right-hand side D669 must be very near -15v (the right-hand side of D669 will be more negative by the voltage drop across D669).

Let's stop and reflect on this for a moment. Without knowing about the transistors at all, other than the basic theory that we have previously discussed in other volumes, we are able to make an approximate analysis of the circuit configuration

in the top diagram in Figure 1. Notice that we use nothing more than basic laws and theorems that we should be familiar with and the assumptions that the emitter follows the base of the transistor when it is in conduction. From this very approximate analysis, we might make voltage and/or resistance measurements in the semiconductor configuration in the top diagram in Figure 1 and expect to isolate a faulty component or transistor. If we had available the characteristics of the transistors in the configuration in Figure 1, we might do a quantitative analysis using Thevenin's Theorem and the characteristics of the transistors.

Note: If our desired results do not require a quantitative analysis, it seems ridiculous to go to the trouble of making a quantitative analysis. If we simply approximate voltage levels so that we know when we have an abnormal meter reading when making measurements, a qualitative analysis should be sufficient. If, for instance, we were not able to adjust the negative 15v supply with the variable resistor, R661, we might anticipate a faulty component in the configuration. If this were the case, we would want to be able to make measurements and know when the measurements were valid. We should try and keep the approach as simple as possible while gaining the required information.

Before going on, stop and do your own simple analysis of the lower diagram in Figure 1. Try and establish some of the current and the voltage levels throughout the circuit. Pick a convenient starting point where you know the voltage level or current level and work from there. Do your own analysis before reading the following:

Starting with the emitter of Q637 in the lower diagram in Figure 1, we see that it is returned to ground potential. Assuming very little drop across the emitter-base junction, the base of Q637 and therefore, the emitter of Q633, the base of Q633, the emitter of Q623, the base of Q623, and finally the collector of Q614A should all be very close to ground potential. (We have assumed very little drop across the emitter-base junctions of the transistors.) Even assuming a drop of a volt across the other three transistors, this would still leave nearly 100v to be dropped across R614 in the collector of Q614A. This requires Q614A to conduct about 0.45ma of current, neglecting any base current from Q623. Notice that the base of Q614A is returned to ground through a 9v Zener diode. Recalling zener diode theory, electron current flows with the arrow in the zener diode symbol and

the voltage across the zener diode is more negative at the end connected to the base of Q614A. This means that the base of Q614A is approximately negative 9v with respect to ground. This -9v is established by the drop across the zener diode. Since we have assumed that Q614 must supply the current for R614, it is also safe to assume that Q614 is in conduction and therefore, its emitter should be very close to -9v. Since the emitter of Q614 is returned through R612 to a negative 75v, this requires that R612 drop approximately 66v. This means that R612 is conducting slightly less than 1ma of current and Q614A only requires approximately 0.45ma of current. Therefore, Q614B must be carrying the remainder of the 1ma. The base of Q614B is returned to a variable resistor which must establish the base very near -9v (the emitter is returned to -9v established by the zener diode in Q614A, therefore, the base of Q614B must also be returned to very near -9v). Varying the voltage on the base of Q614B will vary the current carried by Q614B and, as a consequence, Q614A, and vary the reference voltage that established the negative 75v output. Notice once again in dealing with the lower diagram in Figure 1, knowing very little about the transistors other than the basic theory and the theory associated with zener diodes, we have been able to establish approximate levels throughout the transistor configuration and could very possibly isolate a faulty component if the supply were not functioning properly.

Let's briefly cover the theory of operation of the supply in the lower diagram in Figure 1. Q614A and B operate as a d-c comparator type configuration. The base of Q614A is established at -9v with respect to ground by the zener diode. The right-hand base is adjusted to vary the current in Q614A and, therefore, the voltage at the collector of Q614A. The voltage at the collector of Q614A establishes the voltage at the base of Q623, which establishes the voltage at the base of Q633, which establishes the level at the base of Q637, which of course establishes the current in Q637 and the resistance of Q637. The voltage drop across Q637 and any other series resistance in the circuit configuration must of necessity be 75v less than the total applied voltage. Q637 is the series regulator in the configuration. A change in the negative 75v supply is applied to the base of Q614, which is an error signal applied to the amplifier loop. Assume that the negative 75v tried to become more negative. This results in the base of Q614B becoming more negative and this reduces the forward bias on Q614B. This requires Q614A to conduct more current, which results in the collector of Q614A moving farther from the positive 100v supply, or in the negative direction. A negative change applied to the base of Q623 results in a negative

going change at its emitter. This change is applied to the base of Q633, which results in a negative going change at its emitter. This negative going change is applied to the base of Q637, reducing the forward bias on Q637, increasing its resistance. Increasing the resistance of Q637 results in more voltage across Q637, which brings the negative 75v supply down to its normal level. Just the opposite, of course, occurs when the negative 75v tries to change in the opposite polarity direction.

The foregoing example had two objectives: (1) To bring out the point that the basic laws and theorems still apply to a semiconductor type configuration, and (2) To introduce the reader to approximate analysis approaches to semiconductor amplifier configurations.

Let's continue approximating some d-c levels with the circuit configuration in Figure 2. This type of circuitry is referred to as hybrid circuitry, since it uses both vacuum tubes and transistors. The input circuitry is a cathode follower and the grid is returned to ground through two 1 meg resistors. Assuming that the input cathode follower V113A is in conduction, we would expect to find the cathode very near ground (positive by the bias on the tube). This requires that V113A conduct approximately 3ma of current (V113A is handling the current through R116, which must drop approximately 12v). Dividing the 12v by 3.9KΩ gives an approximate current of 3ma. The 3ma flowing through R114 in the plate circuit of the cathode follower would only drop about 0.6v and, therefore, the plate voltage is very near 125v. Assuming the cathode of V113A is near ground potential, the base of Q134 is near d-c ground potential. Carrying this a bit further, the emitter of Q134 will be very near ground. With two diodes back to back in the base of Q134, we can make an assumption that the signal applied to Q134 is going to be small in magnitude. It will require that the signal be smaller than the turn-on voltage of these two diodes, or the signal will be clipped. Disregarding the circuitry connecting the emitters of Q134 and Q144 together, notice that Q134 has its emitter returned through R135 and R136 to a +125v supply. If we assume that Q134 and Q144 in Figure 2 are both in conduction and their emitters are very near ground, we can determine the current carried by the two transistors. Each transistor will be assumed to carry half the current in R136. If this is the case, we will essentially have the two currents flowing through 5KΩ, which is parallel resistance of R135 and R145. In other words, we can take the parallel resistance of R135 and R145 in

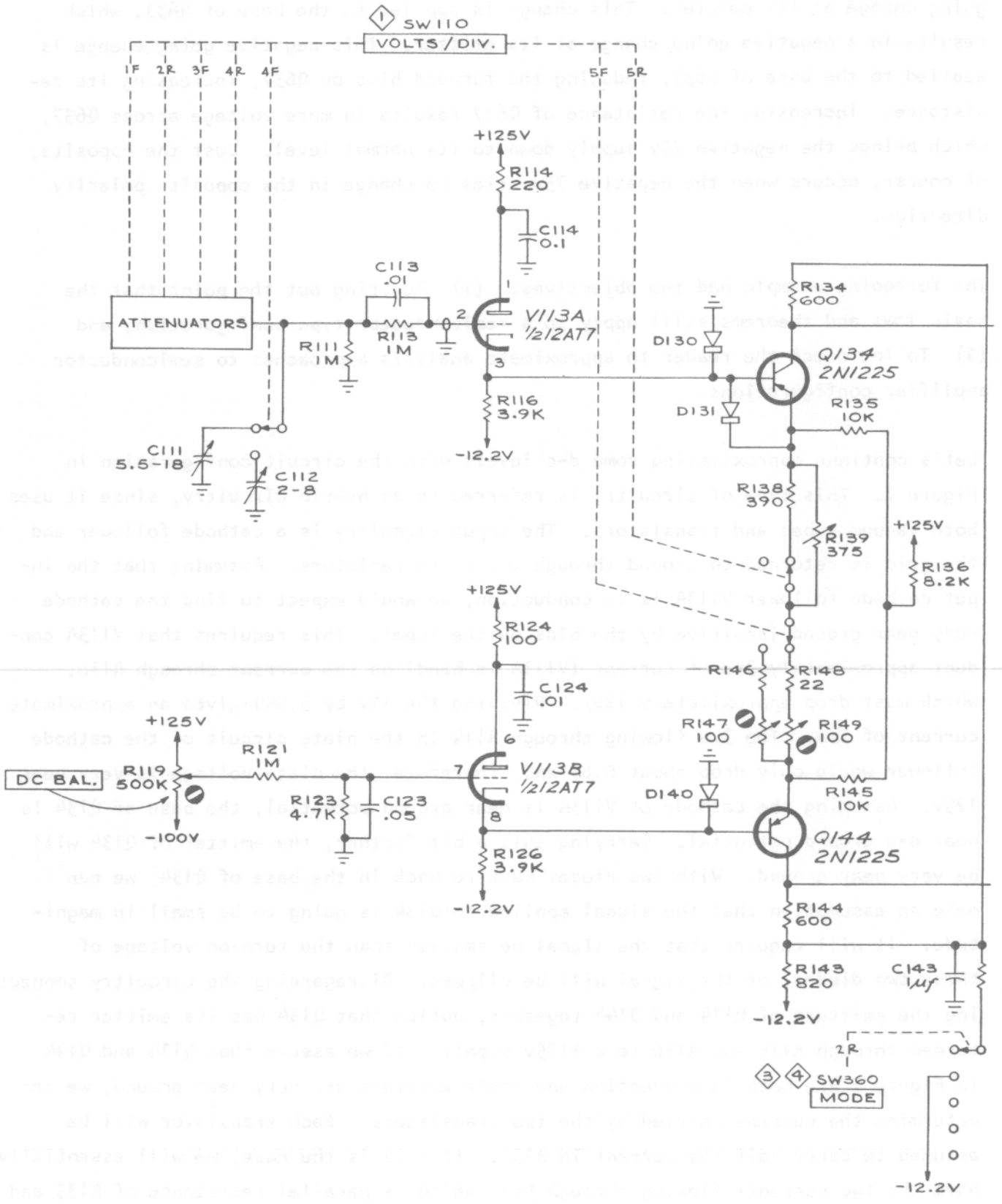

1 SW110
VOLTS/DIV.
1F 2R 3F 4R 4F
5F 5R
+125V
R114 220
C114 0.1
C113 .01
ATTENUATORS
R111 1M
R113 1M
V113A 1/2 12AT7
R116 3.9K
-12.2V
C111 5.5-18
C112 2-8
R134 600
D130
Q134 2N1225
D131
R135 10K
R138 390
R139 375
R136 8.2K
R124 100
C124 .01
DC BAL.
R119 500K
-100V
R121 1M
R123 4.7K
C123 .05
V113B 1/2 12AT7
R146
R148 22
R147 100
R149 100
D140
R145 10K
Q144 2N1225
R126 3.9K
R144 600
R143 820
C143 1uf
3 4 SW360
MODE

FIGURE 2

series with the resistance of R136 and determine the current carried by the two transistors. This is assuming both emitters are near ground d-c potential. This requires that approximately 125v is dropped across a series resistance of 13.2kΩ (the parallel resistance of R135 and R145 in series with R136), or slightly less than 10ma of current. Each transistor then is essentially conducting slightly less than 5ma of current.

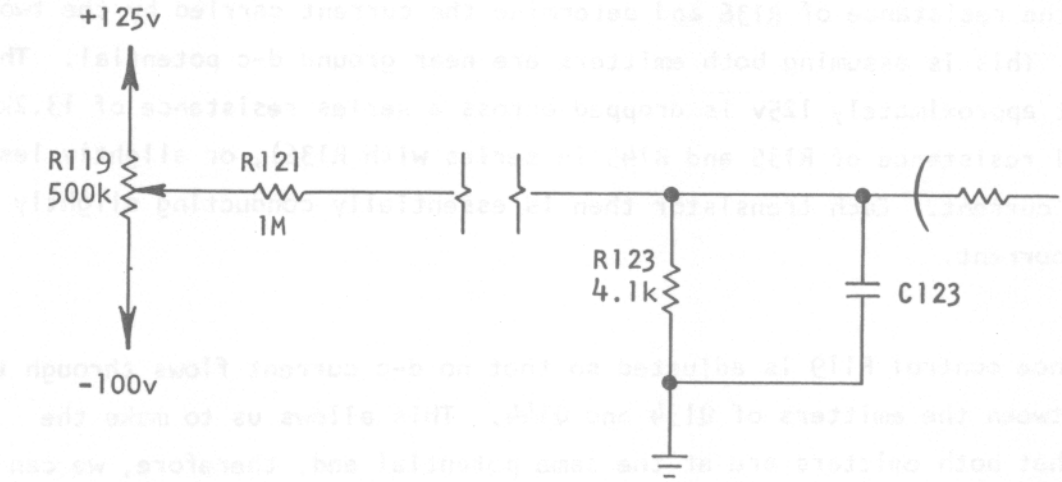
The d-c balance control R119 is adjusted so that no d-c current flows through the resistors between the emitters of Q134 and Q144. This allows us to make the assumption that both emitters are at the same potential and, therefore, we can parallel R135 and R145 to estimate the current carried by the transistors. If we assume that all this current flows in the collectors of the transistors (disregard base current), we would find 10ma flowing through R143. The product of 10ma and 820Ω gives a voltage drop across R143 of 8.2v. Subtracting this from the supply voltage of 12.2v, we find essentially a 4v supply for the two transistors.

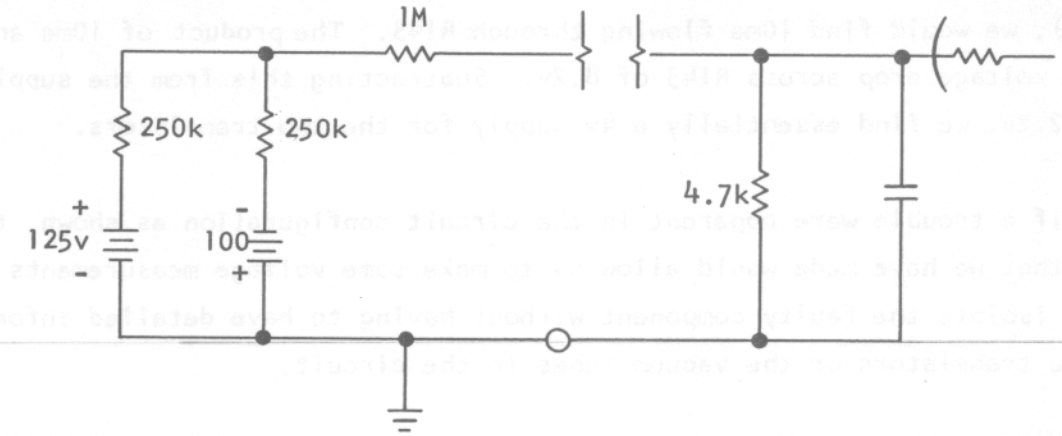
Notice that if a trouble were apparent in the circuit configuration as shown, the assumptions that we have made would allow us to make some voltage measurements and possibly isolate the faulty component without having to have detailed information on the transistors or the vacuum tubes in the circuit.

Let's apply Thevenin's Theorem to the grid circuit of V113B in Figure 2. Break the circuit between R121 and R123 and solve for the Thevenin equivalent circuit to the left of and including R121. This is illustrated in Figure 3. Assuming R119 to be at design center (250kΩ between the moveable arm and either end of the potentiometer), we essentially have the second circuit as shown in Figure 3. Applying Thevenin's Theorem in solving for an equivalent, we find we have a 12.5v d-c source with an internal resistance of 1.125megΩ supplying the 4.7k resistor in the grid circuit of V113B. Applying basic voltage divider theory, we might solve for the voltage at the grid of V113B with potentiometer R119 at design center by simply saying:

$$\frac{4.7k}{4.7k + 1.125meg} \times 12.5v = \text{the voltage at the grid of V113B.}$$

This slips out to be about +.00415mv; therefore, at the design center of potentiometer R119 we can expect to find the grid of V113B very near ground potential. This should be the case, since the grid of V113A is very near ground potential and R119 should allow small differences in the two sides of this amplifier con-


+125v
R119
500k
R121
1M
R123
4.1k
C123
-100v


1M
250k
250k
4.7k
+
125v
-
-
100
+

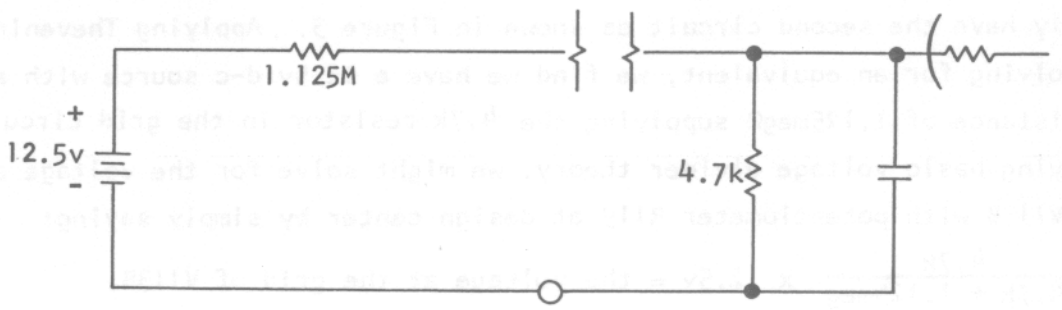

1.125M
+
12.5v
-
4.7k

FIGURE 3

figuration to be adjusted out. If this is not the case, varying components between the emitters of Q134 and Q144 will result in changes in the d-c levels in the amplifier. This is undesirable and will be discussed later; however, it does give us a rationale for the d-c balance control. We will also discuss some other purposes of the diodes D130, D131, and D140 later in this volume.

Once again, the foregoing examples have been included to review the use of the basic laws and theorems when semiconductors are in the circuit configuration. The Q134 and Q144 circuitry in Figure 2 is an emitter coupled paraphase amplifier and an analogy can be drawn between this circuitry and the cathode coupled paraphase amplifier as outlined in Typical Oscilloscope Circuitry. Emitter-coupled paraphase amplifiers will be discussed later in this volume. Approaches to calculating the gains and impedance levels of the transistors will also be discussed.

TRANSISTOR AMPLIFIER MODELS:

Basic circuit analysis approaches are limited to linear networks; however, the transistor's input circuit has a non-linear relationship between current and voltage. To use the basic laws and theorems in an a-c analysis of a transistor configuration, the parameters must be derived from incremental measurements so that the network can be considered essentially linear in the area of interest. These parameters are limited to use with small signals once they are measured; small signal being that magnitude of signal that does not result in a significant change in the parameters over the full swing of the signal. Since the current is not at all times proportional to the voltage in the input circuit of a transistor, it is termed non-linear. Figure 4 shows the plot of emitter base voltage versus emitter-base current.

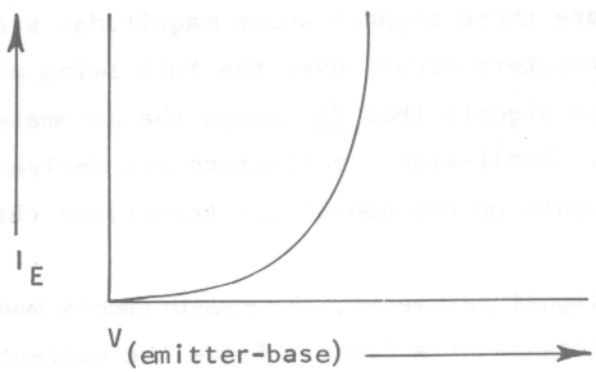


FIGURE 4

Since the current in a diode is related exponentially to the applied voltage, a plot of current versus voltage shows an exponential curve.

If a small segment of the transistor's input EI characteristic is selected, it will approach linearity. The current will be nearly proportional to the voltage in a small selected segment of the curve in Figure 4. When a small portion of the transistor's input characteristic is selected and measurements made that are approximately linear, parameters can be formulated and the basic theorems used in analysis. It should be clear, however, that any signals dealt with using these parameters must be small in magnitude. When incremental measurements are made to derive parameters, the parameters will be referred to as small signal parameters. Any model in which small signal parameters are used will be referred to as a small signal model or equivalent circuit.

When small signal parameters are derived by making incremental measurements, the parameters can be considered essentially linear and the basic theorems can be used in analysis. We might formulate small signal to mean such a magnitude of signal that will not result in the parameters of the transistor changing significantly over the swing of the input signal.

A signal of sufficient magnitude to result in the parameters changing at different points in the cycle is termed large signal. Of course, it is very difficult to obtain linear parameters when dealing with large signals. The parameters will change at different points in the input cycle when large signals are applied. Small signals, however, do not cause significant change in the parameters over the full swing of the signal.

In review, small signals are those signals whose magnitudes are such that no significant change in the parameters occurs over the full swing of the input signal, and large signals are those signals that do change the parameters over the full swing of the input signal. Small-signal parameters are derived by making incremental or very small measurements on the non-linear transistor characteristics.

As an example of a small signal parameter, the measurements made in Figure 5 will give the small signal resistance of a diode. Since the current is related exponentially to the applied voltage, making incremental measurements at different points

on the curve in Figure 5 will give different values of small signal resistance. The small signal resistance of a diode is that dynamic resistance that the diode exhibits at one particular point of its characteristics.

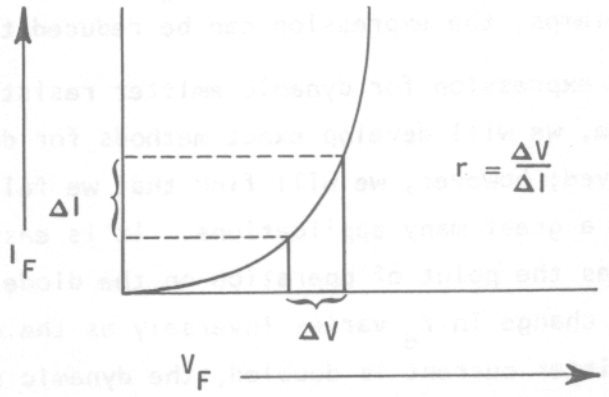


FIGURE 5

An ideal germanium diode has an EI curve that follows an exponential from the saturation current of the diode to infinity (this is in Volume 6). The small signal resistance of a diode can be found from the approximate expression

$$r_{(\text{small signal})} \approx \frac{KT}{qI}$$

where K = Boltzman's constant, T = Temperature, q = charge on an electron, and I = diode d-c current. $\frac{KT}{q}$ at 27°C is approximately 26mv for an ideal germanium diode. In this case, if the d-c diode current is 1ma, the small signal resistance is $\frac{26mv}{1ma} \approx 26\Omega$ at room temperature. If the diode's d-c current is 5ma, the diode's dynamic resistance at 27°C is about 5.2Ω.

The expression $\frac{KT}{qI}$ is valid for most germanium diodes and silicon diodes. Since it is an approximation, we can assume that it will be valid for all types of diodes. We should now recall that the input circuit of a transistor is a diode. The doping levels have been varied for transistor action, but the emitter-base junction is still a diode. The dynamic resistance of the emitter-base junction, as seen from the emitter, can be found by the approximate expression, $r_e \approx \frac{KT}{qI_E}$

where K = Boltzman's constant, T = Temperature, q = charge of an electron, I_E = d-c emitter current. Recalling that $\frac{KT}{q}$ at 27° is about 26mv, we can derive the approximate expression $\frac{26mv}{I_E}$. This will give the value of the dynamic resistance of the emitter-base junction as seen from the emitter at 27°C. This dynamic re-

sistance is given the symbol r_e. With this in mind, any transistor, whether it is germanium or silicon, can have its dynamic emitter-base junction resistance as seen from the emitter found from the simple expression $\frac{26mv}{I_E}$. Since emitter currents are usually expressed in milliamps, the expression can be reduced to $r_e \approx \frac{26}{I_{E(ma)}}$. This gives an approximate expression for dynamic emitter resistance of any transistor. Later in this volume, we will develop exact methods for determining the dynamic resistances involved; however, we will find that we fall back to the approximate expression in a great many applications. It is easy to see, however, that r_e certainly varies as the point of operation on the diode characteristic changes. Notice that the change in r_e varies inversely as the emitter current. In other words, if the emitter current is doubled, the dynamic resistance of the diode is approximately halved. It should be noted at this time that we used I_E, the emitter current, in the approximate formulation. Therefore, r_e is the small-signal or dynamic resistance that we would see at the emitter terminal of the transistor.

The current in the base lead is a small portion of that current flowing in the emitter lead. The current in the emitter lead is approximately the product of $(\beta + 1)$ and the current in the base lead. Therefore, we would expect to see a higher dynamic resistance at the base lead than at the emitter lead. The current in the base lead is magnified by a factor of $\beta + 1$ at the emitter terminal. The dynamic resistance seen at the base terminal of the transistor is magnified by approximately $\beta + 1$ times the impedance seen at the emitter terminal. Approximating the resistance seen at the base terminal of a transistor (base to emitter), we can simply take the product $r_e \times (\beta + 1)$. We now have two approximate expressions for determining the dynamic resistance seen at the terminals of the transistor. At the base terminal, $r_e \times (\beta + 1)$; at the emitter terminal, $r_e = \frac{KT}{qI_E} = \frac{26mv}{I_E} = \frac{26}{I_{E(ma)}}$. There is also some added base bulk resistance which will be discussed later.

If the value of r_e is stated for a transistor, the temperature and the emitter current at which r_e was measured must be stated. These discussion points should have indicated that the background we have gained in basic diodes can now be applied to our study of transistors and transistor amplifier configurations.

MODELS:

Early in this volume, it was stated that the simplest model would be used that will facilitate the particular job that it is desired to do. Figure 6 shows some typical models that we use quite often in electronics work -- the resistor, capacitor, and the inductor.

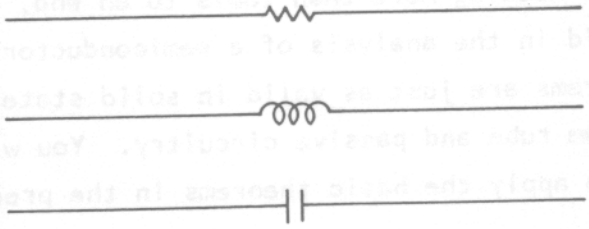


FIGURE 6

We tend to accept these models at face value at times, forgetting that there are times and instances when this simple model becomes useless and a more complex model is required. Take the resistor as an example. At d-c, representing a simple resistance might be valid. Let's take another extreme, however, and suppose that the resistor was being used at 2 gigacycles. Attempting to use a resistor at 2 gigacycles would force taking into account the end to end capacity, the radial capacity, the body to the chassis capacity, etc. The model of our resistor might look more like the model shown in Figure 7.

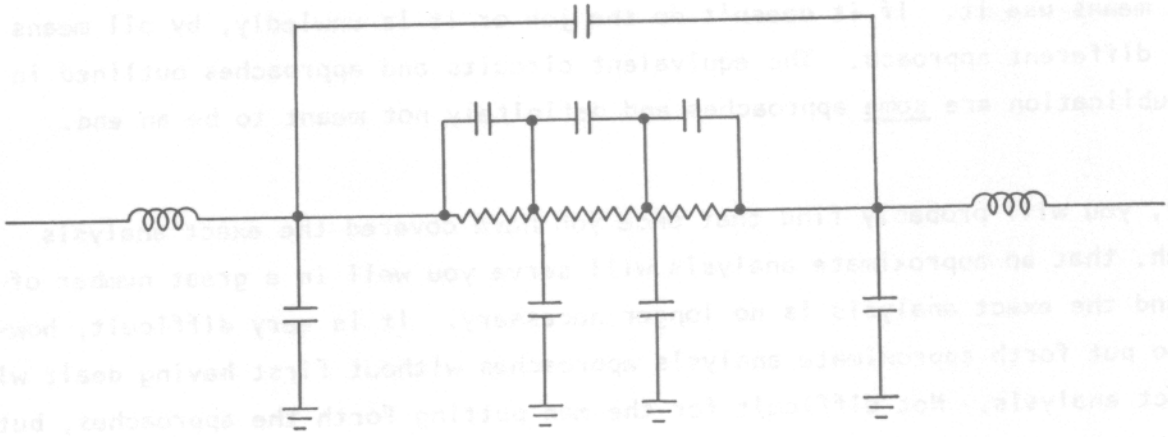


FIGURE 7

The same, of course, can be said of the other models in Figure 6. Each component for which the schematic synbol is shown in Figure 6 exhibits all of the characteristics of the other two as well. In other words, the resistor has inductance and

capacitance; the capacitor has resistance and inductance; and the inductor has resistance and capacitance. At certain frequencies, the simple model in Figure 6 is no longer applicable and a more complicated model must be constructed for analysis purposes.

When dealing with semiconductor devices, it is best to keep in mind that complicated parameters and models are nothing more than tools to an end. They are nothing more than a kit of tools to aid in the analysis of a semiconductor circuit. The basic electrical laws and theorems are just as valid in solid state circuitry as they are in the familiar vacuum tube and passive circuitry. You will note that we called for the ability to apply the basic theorems in the prerequisites for this volume.

The particular model selected for use in analysis of a transistor configuration will vary for a number of reasons. The particular application of the amplifier, the frequency of operation, the point of operation, whether small signals or large signals are applied, and even the personal preference of the man doing the analysis or design. All of the models, equivalent circuits, etc., that we will discuss in this volume are valid and applicable. They can be used for the particular purpose for which they are designed. Which one you use is up to you. If it will do the job at the particular point of operation and frequency of interest, by all means use it. If it doesn't do the job or it is unwiedly, by all means seek a different approach. The equivalent circuits and approaches outlined in this publication are <u>some</u> approaches and definitely not meant to be an end.

Further, you will probably find that once you have covered the exact analysis approach, that an approximate analysis will serve you well in a great number of cases and the exact analysis is no longer necessary. It is very difficult, however, to put forth approximate analysis approaches without first having dealt with the exact analysis. Not difficult for the man putting forth the approaches, but for acceptance by the learner.

In summary then, the parameters and equivalent circuits with which we will be dealing in analysis of the configurations in this volume are nothing more than tools to allow us to analyze and make predictions in transistor circuitry. We will

deal with several types of models and several approaches; however, they are all a means to the same end. They are all valid for the particular purpose they were intended and personal preference might play a big role in which of the approaches is used. It is suggested that particular attention be paid to the approximate approaches.

THE T EQUIVALENT CIRCUIT:

One of the first models that was formulated for analysis of a transistor configuration was the T equivalent circuit. The parameter r_e, which was discussed earlier, is used in the T equivalent circuit. The model of the T equivalent circuit is one that closely resembles the physical transistor. We should keep in mind that the particular parameters and the equivalent circuits that we are going to use will be governed by the applications to which the transistor is being put. For instance, for analysis of a low level audio amplifier, a low frequency small signal T equivalent circuit and parameters might be used. For d-c considerations, of course, we would want to use d-c parameters.

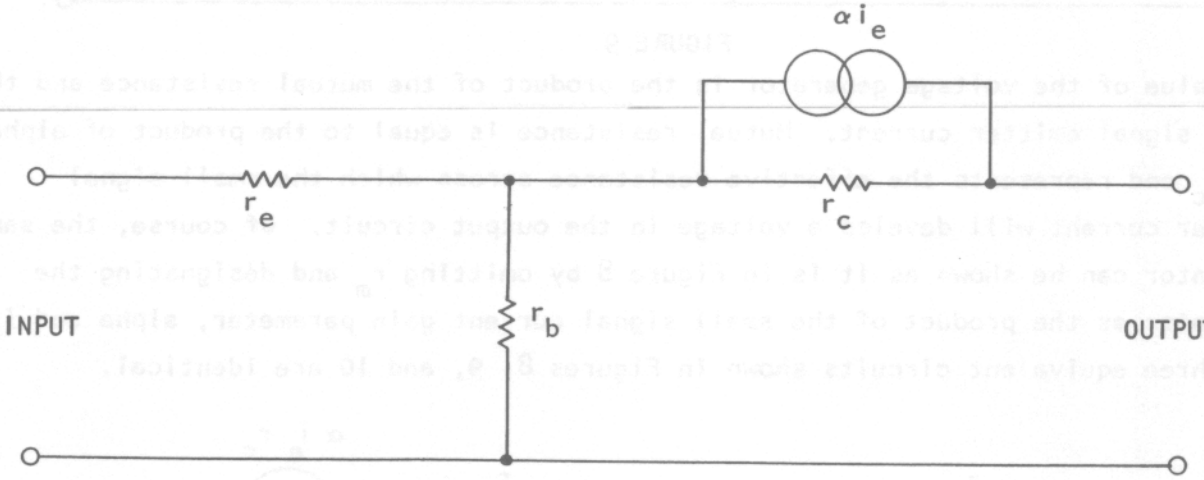


FIGURE 8

Figure 8 shows a diagram of the T equivalent circuit for a common-base-oriented transistor. The parameters are designated with lower case letters to indicate that they are small signal a-c parameters. We are already at least a little bit familiar with r_e, which is the internal small signal resistance at the emitter. Since the emitter is heavily doped, the emitter has a low bulk resistance. r_e is primarily the small signal dynamic resistance at the emitter. r_b in Figure 8 is primarily representing the bulk resistance in the base between the active areas and the base terminal. The base has a fairly high bulk resistance, because it is

lightly doped in comparison with the emitter. Since the collector is also heavily doped, it has a low bulk resistance; however, the junction is reversed biased and, if it were in an ideal diode, would have infinite resistance. r_c in the diagram in Figure 8 represents the small signal resistance of the collector, since the collector diode is not ideal.

The transistor in Figure 8 is an amplifier, and an internal generator is used to represent the amplifier action. An internal voltage generator can be used as shown in Figure 9.

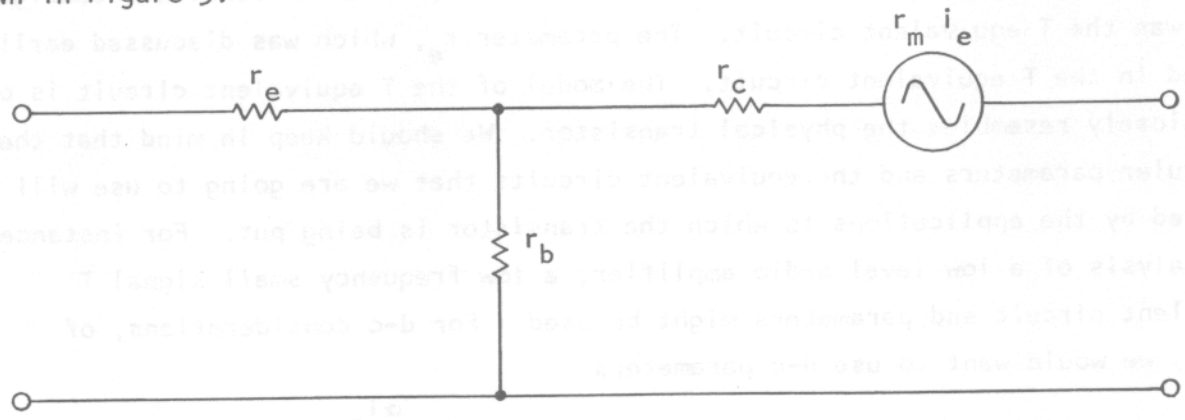


FIGURE 9

The value of the voltage generator is the product of the mutual resistance and the small signal emitter current. Mutual resistance is equal to the product of alpha and r_c and represents the effective resistance across which the small signal emitter current will develop a voltage in the output circuit. Of course, the same generator can be shown as it is in Figure 8 by omitting r_m and designating the generator as the product of the small signal current gain parameter, alpha and i_e. The three equivalent circuits shown in Figures 8, 9, and 10 are identical.

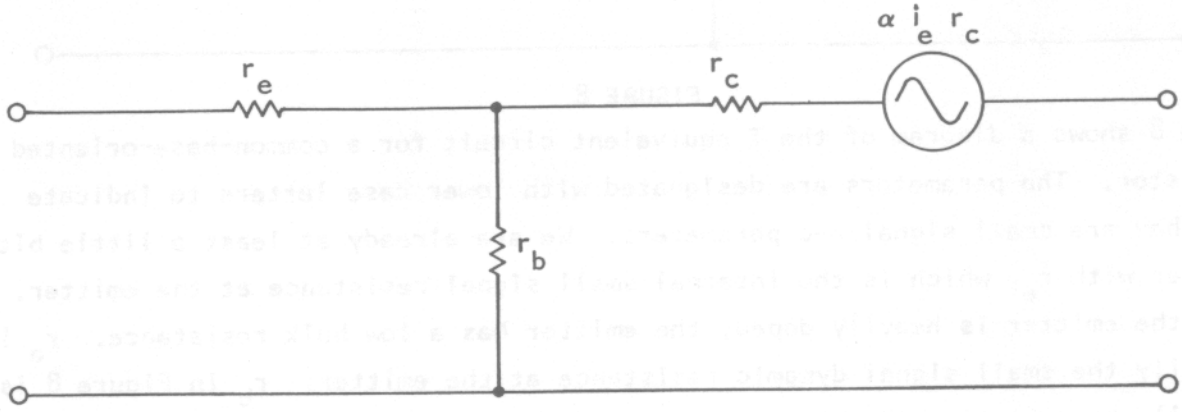


FIGURE 10

Of course, when the current generator is used, it is shunted by the resistance r_c, as shown in Figure 8. The value of the generator is that portion of the small signal emitter current that is in the collector, and in terms of alpha, the generator current equals αi_e. If the current generator αi_e in Figure 8 were a perfect current generator, resistance r_c would be infinite. Since r_c has a finite value, it represents the imperfections of the current generator. The most common internal generator used in the T equivalent circuit is the internal generator as a constant current source of αi_e (for common base configuration), as shown in Figure 8.

Since the parameters used in the T equivalent circuit are essentially linear, the basic theorems can be used in analysis. The basic theorems can be used to solve for input resistance, output resistance, current gain, and voltage gain in terms of the T parameters and any external components in the circuit. This can be done by writing equations for the currents and voltages involved. The equivalent circuit in Figures 8, 9, and 10 was designated a low frequency, small signal T equivalent circuit and, therefore, neglects reactances and those characteristics that effect the higher frequencies. A different equivalent circuit would have to be constructed for dealing with higher frequencies.

We should also keep in mind that the small signal equivalent circuit is not valid if the input signal is large enough to cause a significant change in the parameters. A signal of this magnitude, of course, is considered a large signal. This equivalent circuit is valid for the particular point of operation, temperature, and signal considerations under which the parameters are either measured or specified.

Let's stop and review for a moment. The T equivalent circuit is nothing more than a model to represent the transistor and allow the basic theorems and laws to be applied to the analysis and design of transistor circuits. The T equivalent circuit is not the only model; it is simply the first model that we are discussing. The particular equivalent circuit that we use will be governed by the point of operation, type of signal, and frequency considerations that were made when the parameters were measured. If the T equivalent circuit is a small signal, low frequency equivalent circuit, this indicates that the parameters or tools were measured at a low frequency, typically around 1kc, and that the parameters are only valid if the applied signal does not cause the parameters to vary significantly over its entire swing.

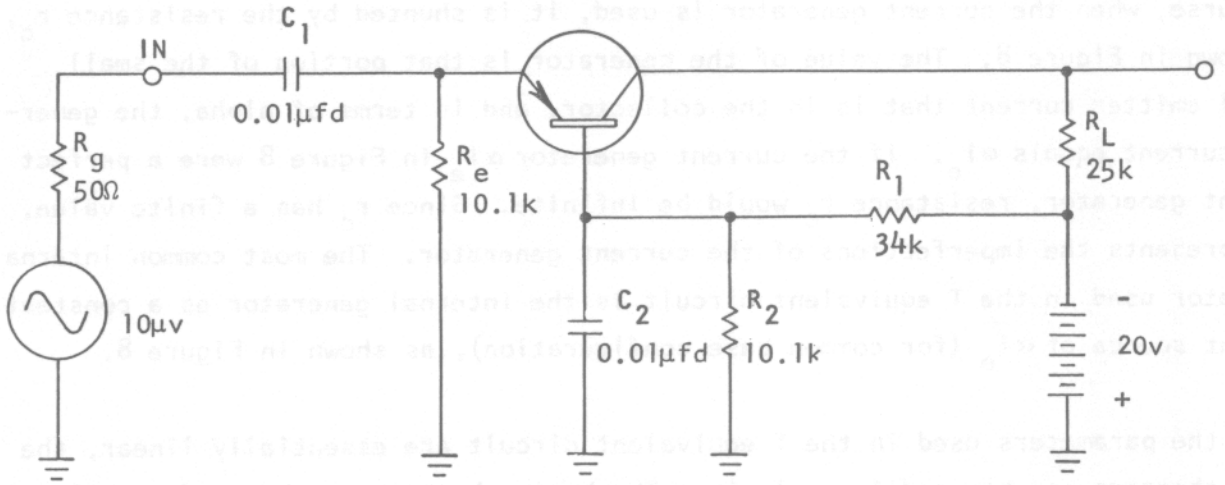


FIGURE 11

Figure 11 shows a transistor configuration with biasing applied and signal considerations. The transistor is in a common base configuration, and is being driven by a 10μv signal. The output is taken off the collector. You will recall that the T equivalent circuit that we have discussed was for the transistor only and did not take into account the external component. In order to accomplish an analysis of the transistorized configuration, we might want to construct an equivalent circuit for the entire amplifier, and then approach an analysis procedure. If the amplifier in Figure 11 is a low frequency (perhaps an audio) amplifier, the low frequency parameters will be valid. If it is a low level or small signal amplifier, small signal parameters are valid. Before analysis is approached, the circuit configuration can be redrawn and an equivalent circuit substituted for the transistor and the entire amplifier configuration.

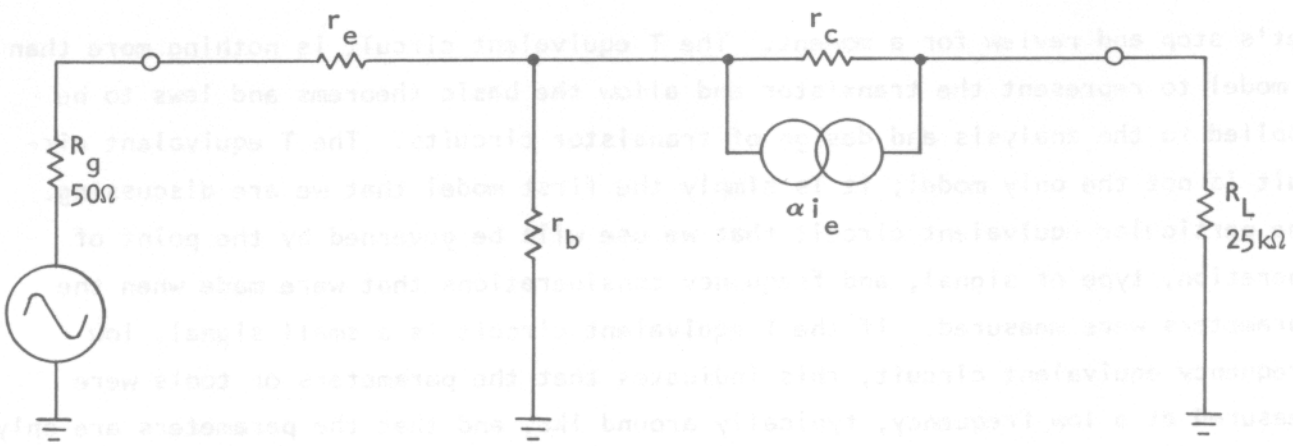


FIGURE 12

Figure 12 is an equivalent circuit for the amplifier in Figure 11 for low frequency, small signals. Notice in Figure 12 that the biasing components and any components that are not applicable for low frequency small signals have been neglected. R_1 and R_2 are simply biasing resistors, and C_2 places the base at signal ground. The biasing resistors, R_1 and R_2, have no effect on the signal. If we assume that the biasing battery is a perfect battery, then it has zero internal impedance and the bottom of R_L is at signal ground. If we assume that the capacitors, C_1 and C_2, have been properly selected so as to have low impedance to the signal frequencies, we can assume them to be short circuits, and they are disregarded in Figure 12. Since the internal impedance of the driving generator is only 50Ω, the resistance R_e has been neglected. In reality, in the equivalent circuit, R_g should be shown as the parallel resistance of R_g and R_e; however, 10.1k in parallel with 50Ω is rather insignificant and it has been neglected in the diagram.

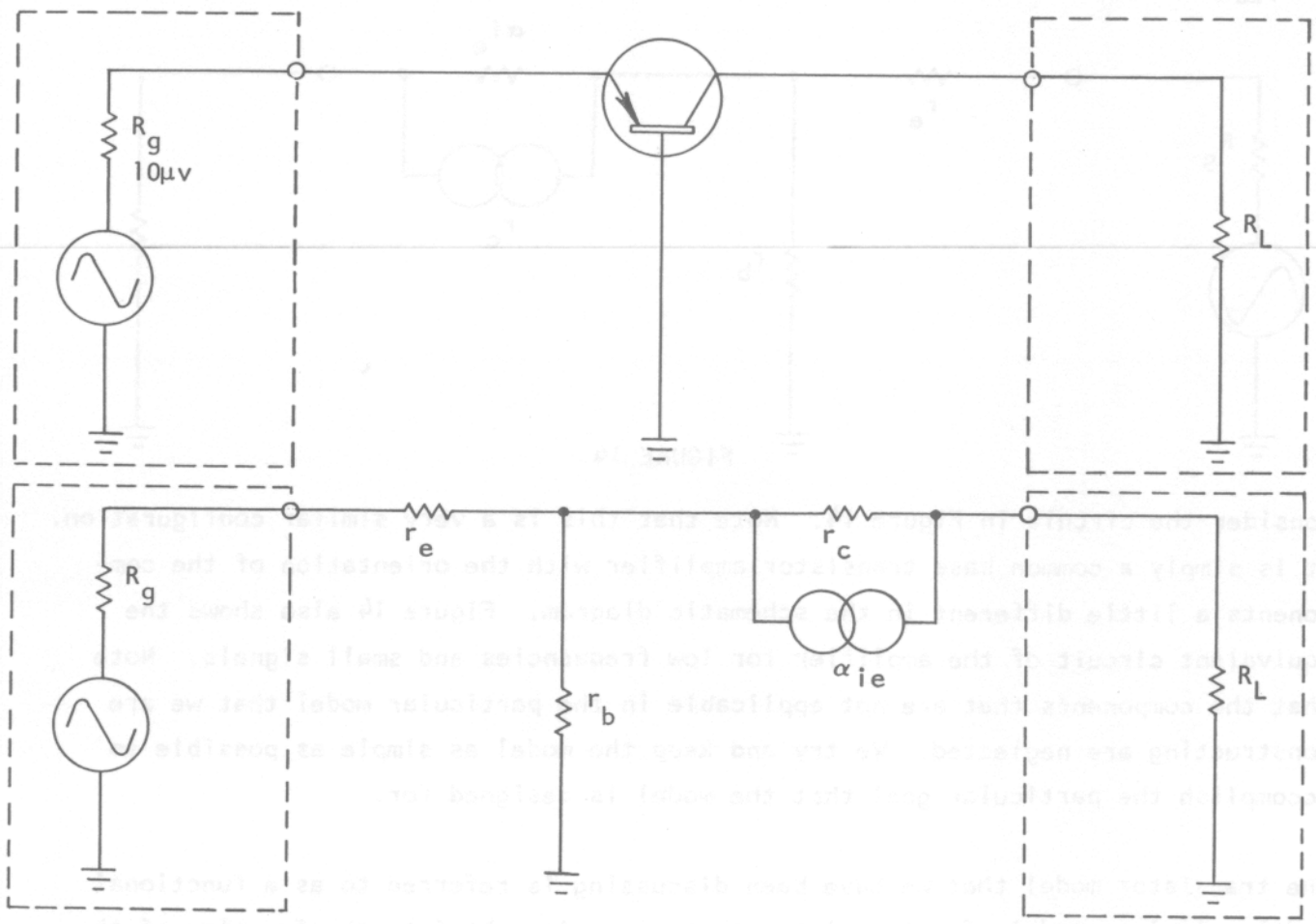


FIGURE 13

Figure 13 shows the equivalent circuits for the external signal components isolated from the transistor, and then the T equivalent circuit inserted for the transistor. We now have an equivalent circuit for which we could develop formulas and solve the circuit using the basic theorems if we had the values for the components in the T equivalent circuit for the transistor.

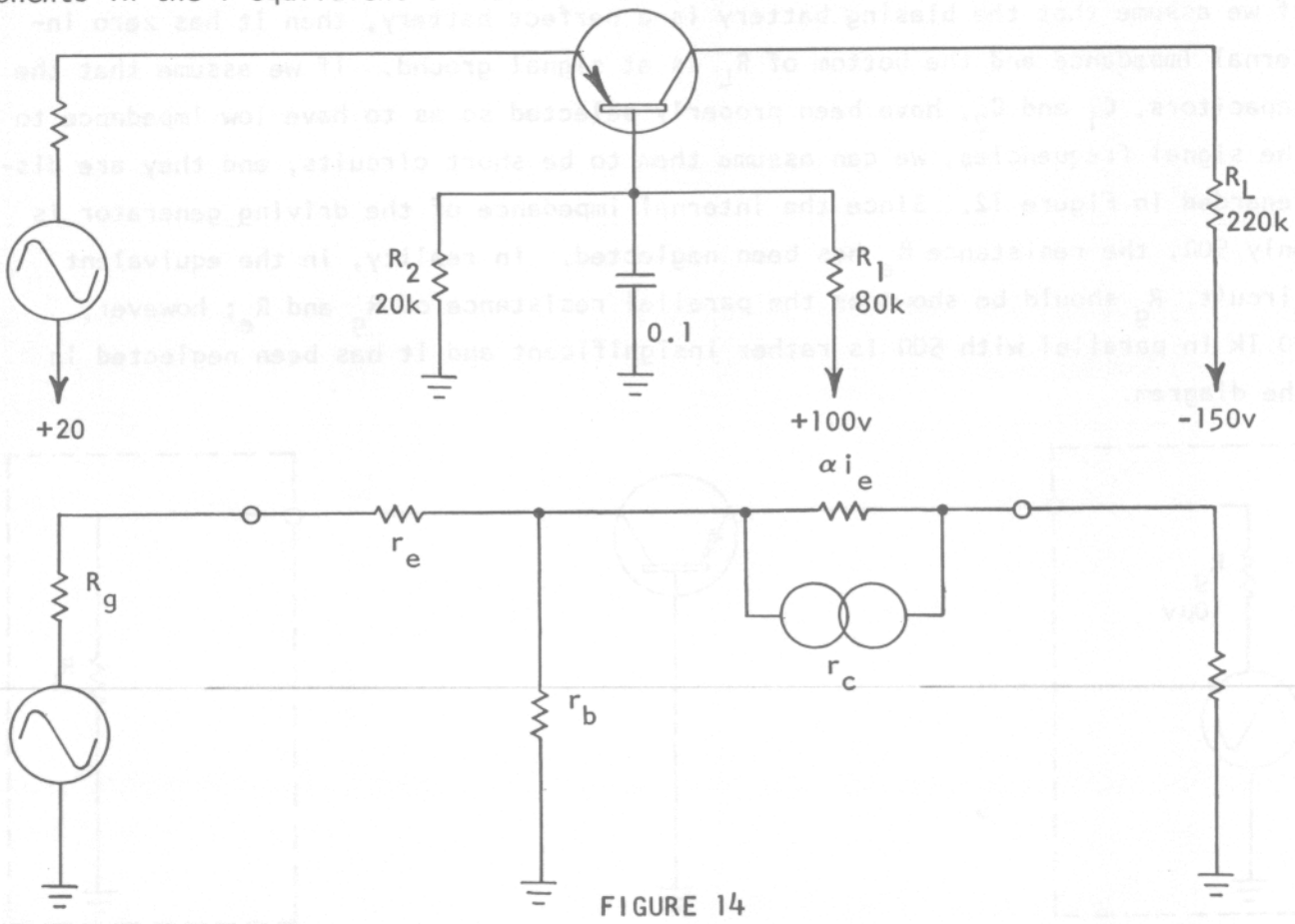


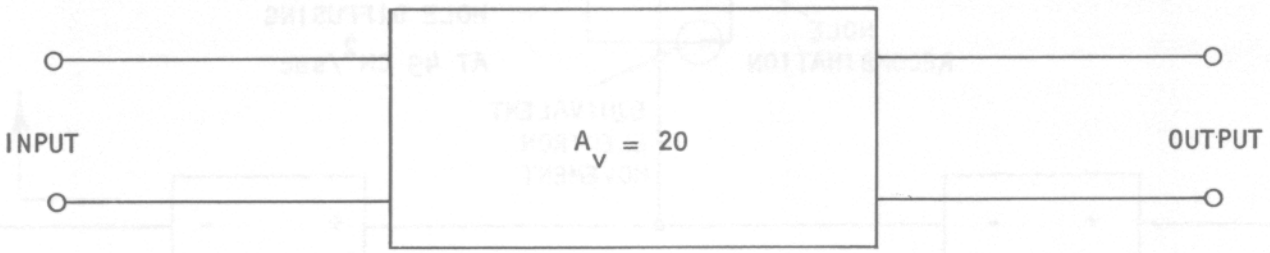
FIGURE 14

Consider the circuit in Figure 14. Note that this is a very similar configuration. It is simply a common base transistor amplifier with the orientation of the components a little different in the schematic diagram. Figure 14 also shows the equivalent circuit of the amplifier for low frequencies and small signals. Note that the components that are not applicable in the particular model that we are constructing are neglected. We try and keep the model as simple as possible to accomplish the particular goal that the model is designed for.

The transistor model that we have been discussing is referred to as a functional model. It is a model of a transistor that gives insight into the function of the transistor, electrically in a circuit, but does not give complete insight as to

the physical action of the transistor when it is operating in the circuit. We have started with the T equivalent circuit because it is the functional model that most closely approaches a physical model. The parameters associated with the T equivalent circuit are to a great degree related to the physical action of the transistor. The parameters are, however, related to measurements taken on a transistor external to the device. These measurements are then applied to constructing a model and allowing the analysis and prediction of the operation of the transistor in the circuit configuration.

If we were only interested in what voltage gains the transistor would offer under a given set of conditions, we might represent the transistor and its circuitry by the functional model such as shown in Figure 15.



A_v = voltage gain

FIGURE 15

Note in Figure 15 that the transistor is simply represented by a box, and the box is designated as having a voltage gain of 20. If we knew the considerations that apply to this functional model, we could expect to put in a certain level of signal voltage on the input terminals and find this signal voltage amplified 20 times at the output. We would not be concerned with what is happening inside the box. This is an extreme example of a functional model, but it does bring out that it is not as concerned with what is going on inside the device. A functional model is concerned with what happens external of the model. We might consider that Figure 16 is at the opposite extreme in that it is a physical model of the transistor action. Note that the physical model, as shown in Figure 16, might give more insight into the internal workings of a transistor and yet offer difficulties when trying to analyze the electrical action of the device in circuitry.

The T equivalent circuit is one attempt to bring together the functional and physical model. The parameters and arrangement of the components in the model try to give insight into the device and yet give parameters that can be used

functionally to allow analysis of the transistor in a configuration.

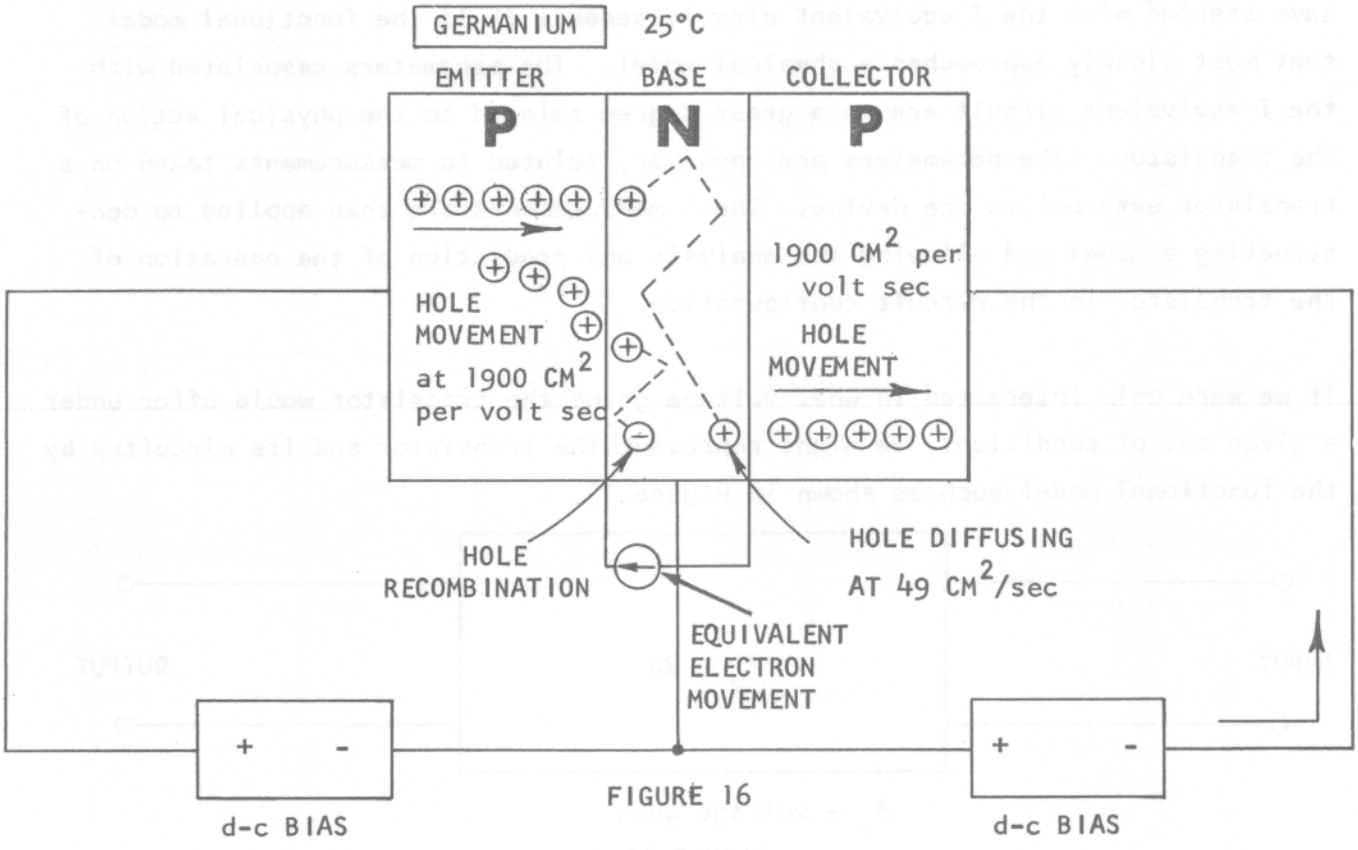


FIGURE 16

The functional model will be limited in that it will be valid only under the conditions that the parameters were measured. If the parameters are used under a different set of conditions, they will have to be modified to fit that particular application. We cannot neglect the direct current characteristic of the transistor and its configuration, and its effect on the small signal considerations. Since the direct current or static operating conditions of the transistor will govern to a great extent the parameters for a small signal configuration, these must definitely be taken into account. Consider the circuit in Figure 17. In earlier studies, we have established that for amplifier operation, the transistor should have the collector reverse biased and the emitter base junction forward biased, if linear amplification is to be accomplished. The transistor in Figure 17 must of necessity have its emitter base junction forward biased and its collector junction reverse biased. A negative 20 volts is applied through the collector load resistor to the collector of the transistor. The emitter is returned to ground through a 10.1kΩ resistor, and the base level is established by a

voltage divider circuit from the negative 20 volt supply to ground.

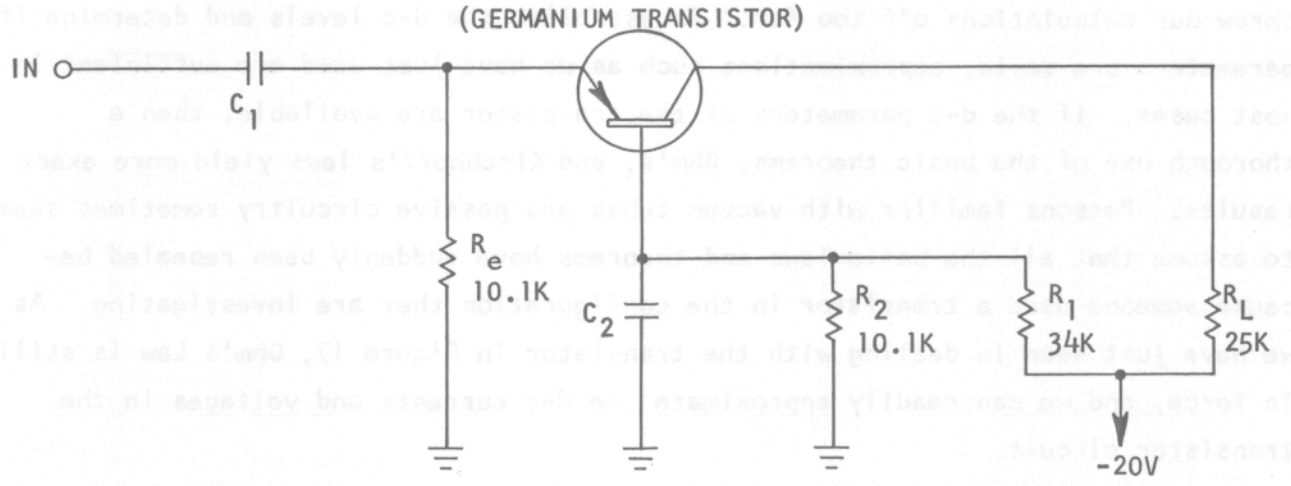


FIGURE 17

The level at the base can be approximated by using Thevenin's Theorem or basic voltage divider theory. The voltage across the 10.1k, if we disregard the base current (using Thevenin's Theorem we could break the lead going to the base of the transistor and solve for the open circuit voltage at the top of the 10.1k resistor), we can say that the voltage at the top of the 10.1k resistor at the base is equal to $\left(\frac{10.1k}{10.1k + 34k}\right)(-20v)$. This gives an open circuit voltage at the base of the transistor of approximately 4.57v. Since the emitter base junction is forward biased, we can expect only a few tenths of a volt from emitter to base. The emitter is very close to 4.57v. Since the 10.1k in the emitter in Figure 17 is returned to ground, the 10.1k resistor must drop approximately 4.5v. It then becomes a simple Ohm's Law problem to determine the current through it. $\frac{4.5v}{10.1k}$ is a little less than 0.45ma. We might carry this further and assume that approximately the same amount of current flows in the collector that flows in the emitter, and the collector current is approximately 0.45ma. Since the collector load resistance is 25k, the product of 25k and 0.45ma will give the drop across the collector load resistance. The drop is approximately 11.2v. Subtracting this from 20v, we have a voltage at the collector of approximately 8.8v. Since the emitter is at approximately 4.5v, the collector to emitter voltage is approximately 4.3v.

You might think that we have neglected some important factors in our approximation; however, assuming the base current to be 0 is justified in this case, since the emitter current is only 4.5ma. Even assuming a low d-c beta of perhaps 20 or 30,

the base current is only 1/20th or 1/30th of the emitter current, and does not throw our calculations off too far. To establish the d-c levels and determine if parameters are valid, approximations such as we have just used are sufficient in most cases. If the d-c parameters of the transistor are available, then a thorough use of the basic theorems, Ohm's, and Kirchhoff's laws yield more exact results. Persons familiar with vacuum tubes and passive circuitry sometimes seem to assume that all the basic laws and theorems have suddenly been repealed because someone used a transistor in the configuration they are investigating. As we have just seen in dealing with the transistor in Figure 17, Ohm's Law is still in force, and we can readily approximate the d-c currents and voltages in the transistor circuit.

OTHER FUNCTIONAL MODELS:

As previously discussed, the functional model of the transistor simply provides a kit of tools to allow analysis of the transistor in a specific configuration. The T equivalent circuit that was previously discussed is a functional model and provided parameters for dealing with the transistor in an amplifier configuration. Ohm's and Kirchhoff's laws and applied to the equivalent circuit to obtain formulas for solving for gains and impedance levels.

Most functional models are not concerned with the internal workings of the transistor or the particular device being represented. They are concerned with how the device reacts when placed in a configuration. Most equivalent circuits are formulated by making measurements on a configuration such as shown in Figure 18.

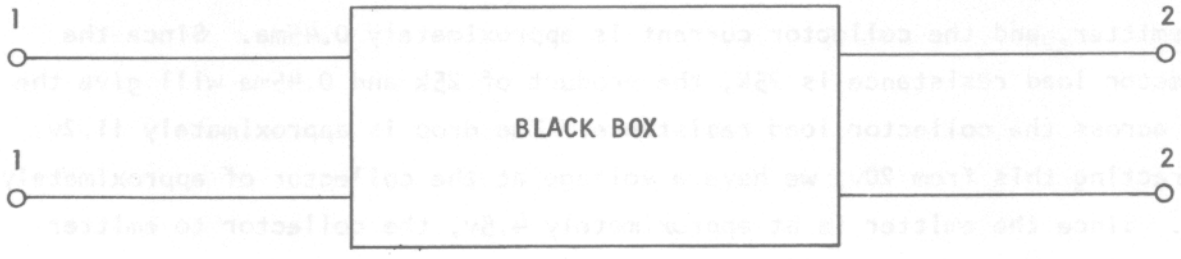


FIGURE 18

The device for which a representative model or equivalent circuit is desired is assumed to be in a black box with two input terminals and two output terminals. The input terminals are designated with the number 1; the output terminals are designated with the number 2. This approach is referred to in several ways. The black box approach, two-part formulations, etc. An equivalent circuit obtained by making measurements on the black box as shown in Figure 18 will vary with the type of measurements made and the values obtained. Since we have already discussed that the voltage versus current characteristics of a transistor are non-linear, we might wish to obtain a small signal, low frequency equivalent circuit for the transistor. By assuming it is in a black box, we could make incremental measurements on its terminals and obtain parameters which are essentially linear and can be inserted in an equivalent circuit. The T equivalent circuit already discussed is a form of functional model and similar measurements must be made in order to obtain parameters for the T equivalent circuit.

We will discuss a number of functional models or equivalent circuits based on the measurements made on the black box as shown in Figure 18. The important point to remember at this time is that all of the functional models we will be discussing are based on measurements made on a configuration such as shown in Figure 18. If incremental measurements are made, the results will be essentially linear and we can consider the black box to be a linear four-terminal network. This is assuming we are trying to obtain a low frequency, small signal equivalent circuit.

Let's assume that we want to obtain a low frequency, small signal equivalent circuit for a transistor for use in analyzing or predicting circuit impedances and gains when a transistor is used in a configuration. Since the transistor has three terminals - the emitter, base, and collector - one of the terminals can be made common, and the configuration such as shown in Figure 19 can be used to make measurements on the device. In the measurements configuration in Figure 19-a, the input voltage is being varied incrementally, and the input voltage and current are monitored by meters. So that the output voltage will have no effect on the measurements, the output has been a-c short-circuited by a large capacitor. The transistor itself is shown as nothing but a black box since the functional equivalent circuit is not interested in what the device <u>is</u>, but rather what it will do when placed in circuitry. Once the measurements in Figure 19-a are made, it is a simple matter to use Ohm's Law to determine the small signal resistance between the pins numbered 1

in the diagram.

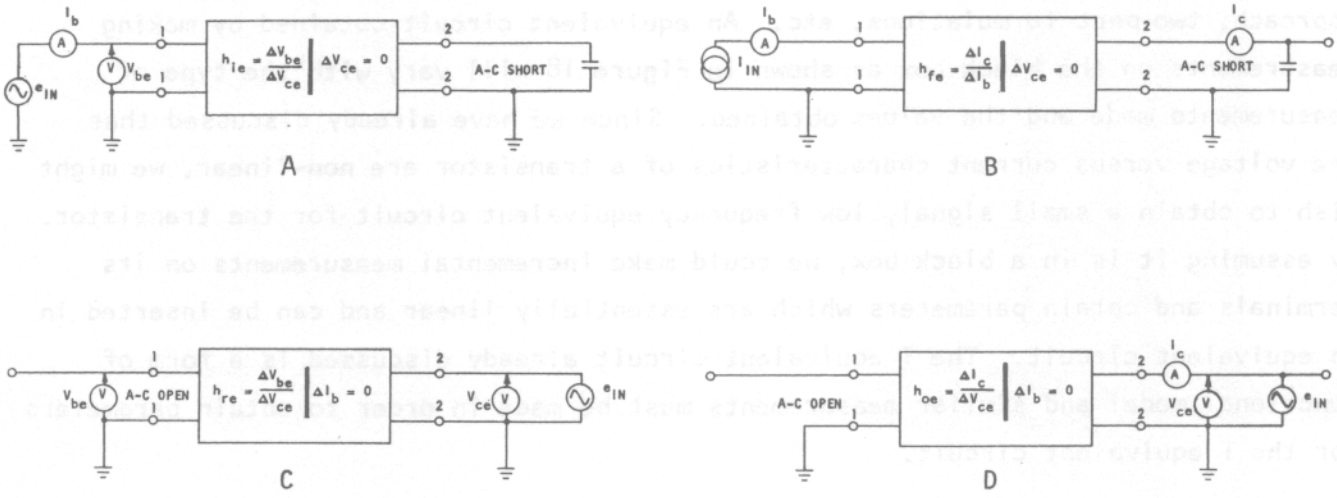


FIGURE 19

The resistance, let's call it h_{11}, is equal to the incremental change in the voltage between pins 1 and 1 divided by the incremental change in current that occurs. Of course, this is assuming that the output voltage has been held constant as a result of the large capacitor shorting the pins numbered 2 together.

Figure 19-b shows the measurement set-up for determining the effect of an incremental input current change on the current in the output circuit (the current gain of the device in the black box). Once again, in Figure 19-b, the output points have been essentially shorted together with a large capacitor so that the output voltage will not have an effect on the measurement. The measurement is made by applying an incremental change in input current and noting the change in the output current. It is a simple matter then to determine the current gain by dividing the measured change in the output current by the applied input current change. This measurement is also made with the output voltage held constant.

Figure 19-c shows the measurement set-up for determining the effect of the output voltage on the input voltage. An incremental change in output voltage is applied and the input voltage is monitored by a meter. The input current is held constant

by essentially keeping the input circuit a-c open circuited. This might involve a large reactance such as a large inductance to maintain a constant input current. The effect of the output voltage on the input voltage can be obtained by dividing the measured change in input voltage by the applied change in output voltage.

Figure 19-d shows the measurement set-up for determining the effect of changes in output voltage on the output current. The input circuit is essentially a-c open circuited so that the output current will not be effected by variations in the input current. An incremental change in output voltage is applied and the output current monitored. It is once again a simple matter to determine the resistance between the two pins numbered 2 by dividing the incremental change in the applied voltage by the incremental change in the current. For the particular model for which these parameters are to be used, the output conductance is desired. The values gained from the measurements in Figure 19 are measured for what is termed a hybrid equivalent circuit for a transistor. You will note in Figure 19 that two separate types of measurements were made. Measurements that could be referred to as short circuit measurements, since the output was essentially a-c short circuited to hold the output voltage constant, and measurements were made in which the input was essentially held a-c open circuited so that the input current would remain constant. Since the particular equivalent circuit that we are going to discuss involves two separate types of measurements, it is referred to as a hybrid equivalent circuit. The parameters associated with this equivalent circuit are also referred to as hybrid parameters. These parameters are designated with an "h" to indicate that they are hybrid parameters.

We should keep in mind that the other functional equivalent circuits that are discussed later in this volume are arrived at by making similar measurements on a black box. In this particular case, the black box contained a transistor. It might, of course, be a transistor, a resitive network, or any electronic device that we would like to represent with an equivalent circuit or model to simplify the analysis and design. Another thing that should be kept in mind is that, due to the inherent nonlinearity in the transistor circuit, the parameters will be different at different quiescent or d-c points of operation. Therefore, when these parameters are stated, the point of quiescent operation should also be stated.

The functional equivalent circuit is limited in that it must be used only under a

given set of conditions. The particular equivalent circuit that we gain parameters for in Figure 19 is only valid at low frequencies under small signal conditions at the particular point of operation at which the parameters were measured. Along with this, the parameters are effected by the configuration that the transistor is in within the black box when the measurements are made. In other words, the parameters will be different for the common emitter, common base, or common collector configuration.

We will first investigate the hybrid equivalent circuit and then show the relationship between the hybrid and other equivalent circuits and their parameters. Since they are all based on the measurements outlined in Figure 19, it is very easy to transpose from one functional equivalent circuit and set of parameters to another. The particular type of equivalent circuit that is used depends on a number of things. It might be the ease of measurement of the parameters; it might be the parameters that are most commonly stated by the manufacturer, and even personal preference enters into the consideration of which equivalent circuit is to be used. Some equivalent circuits will not lend themselves well to dealing with the higher frequencies, while others offer other limitations.

It should be remembered that, under the conditions the parameters were measured, any of the equivalent circuits is as valid as the next, and the particular one that is used as a functional model will probably boil down to personal preference of the user. Since they are all functional models and are valid, we will not try to indicate that one is better than the next.

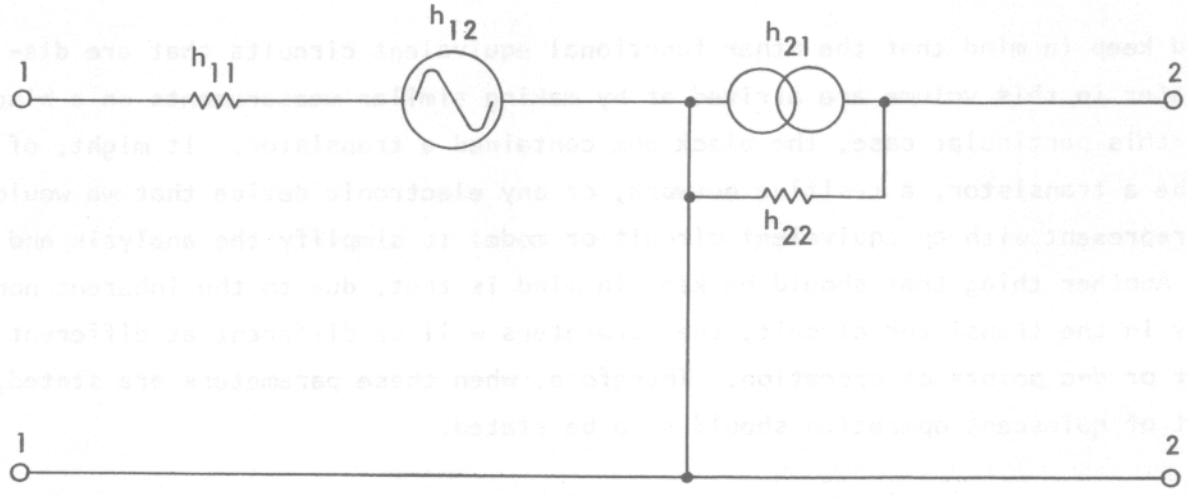


FIGURE 20

Figure 20 shows the hybrid equivalent circuit of a transistor for low frequency, small signal operation. The h in the symbols indicates that they are hybrid parameters. h_{11} indicates the dynamic or small signal resistance that is seen between the two input terminals designated with the 1. h_{12} is a voltage generator that indicates the effect of the output voltage on the input voltage. Notice that the input is a closed loop between the 1 terminals that were shown on the original black box. h_{11} indicates the resistance that is seen between the two input terminals, and h_{12} indicates the effect of the output voltage on the input voltage, allowing a closed input loop to be drawn. The transistor will exhibit a certain current gain between the input and the output terminals, and this is illustrated by the current generator symbol designated h_{21}. h_{22} represents the imperfections of the current generator. Since it is impossible for h_{21} to be a perfect current generator, the conductance that shunts the current generator is shown and designated h_{22}. In other words, this is the dynamic conductance that is seen between the output terminals designated 2.

It is well to stop and note at this point that the equivalent circuit shown in Figure 20 and obtained from the measurements made in Figure 19 does not indicate the internal physical workings of the device, but simply electrical symbols and parameters that show the electrical functioning of the device when placed in a circuit. Also, and this might sound repetitive, the parameters gained for insertion in the equivalent circuit in Figure 20 are only valid under the conditions set by the measurement environment. In other words, the d-c or static operating point, the frequency and signal considerations. If the parameters were measured under a low frequency situation, a new equivalent circuit would have to be constructed, and the parameters modified to do an analysis at the higher frequencies.

h_{11} in Figure 20 can be found using Ohm's Law and the formula $h_{11} = \frac{v_{11}}{i_{11}}$, assuming v_2 is held constant. This is illustrated in Figure 19. When dealing with h_{11}, both the dependent and the independent variables are measured at the input. The applied input voltage is measured between the input pins designated 1, and the change in current is measured at the input and, as a result, the parameter is designated h_{11}. There is only one parameter in this equivalent circuit for which values are gained by the measurement of both the dependent and independent variable at the input terminals. This is the dynamic input resistance.

The parameter h_{12}, however, has the dependent variable measured at the input, and the independent variable measured at the output. An applied voltage is inserted between the terminals marked 2 in the output and the change in the input voltage is measured to gain values for calculating h_{12}. The first number in the parameter designation indicates the point at which the dependent variable was measured, and the second number indicates the point at which the independent variable was measured. In the case of h_{12}, the dependent variable is measured at the input or terminals marked 1, and the independent variable was measured into the output terminals or the terminals marked 2. Therefore, it is designated h_{12}. h_{12} is the voltage generator indicating the effect of the output voltage variations on the input voltage. h_{21} is the current gain parameter of the device. It indicates the effect of the input current on the output current. Since the dependent variable is measured at the output (terminals marked 2) and the independent variable is measured at the input (terminals marked 1), it is designated h_{21}.

h_{22} is the dynamic output conductance of the transistor and it is found by dividing the incremental change in the output current by the incremental change in the output voltage. Both the dependent and independent variables are measured at the output or terminals marked 2, and designated h_{22}. This is the only parameter in this equivalent circuit that can have this designation.

We have four parameters in the hybrid equivalent circuit that may be used to represent the transistor in a configuration. The particular parameters that were gained for the equivalent circuit in Figure 19 were measured at low frequencies with small signals applied and with a given quiescent or d-c operating point. The parameters are not valid if these conditions are not met. Therefore, if these parameters were stated as the parameters for the particular device (in this case a transistor), the conditions under which the parameters were measured must also be stated. This, of course, is one disadvantage of this type of a functional model when dealing with a non-linear device, such as a transistor. A linear four-terminal network is only valid for linear devices. So that the transistor can be assumed to be a linear device, incremental measurements must be made for signal considerations. Since these incremental measurements will yield different parameters at different static points of operation, they are only valid at the particular point of operation at which they were measured. There are methods which will be discussed later by which the parameters may be adjusted for different operating points and for different con-

figurations, even though they were measured under one set of conditions and for a given configuration.

If the parameters are measured for a specific configuration, such as the common emitter, common base, or common collector, a letter following the parameter symbol will designate the common element in that configuration. If the parameters in Figure 20 were measured for a common base configuration, the parameter h_{11} becomes h_{11b}. A number of transistor manufacturers and persons generating text books assume that the common base is the reference configuration and, if the configuration is not designated, one must make the assumption that it is a common base configuration. Since a configuration is not specified, Figure 20 would be assumed to be an equivalent circuit for a common base configuration. If a parameter is followed by the subscript e, it indicates that it is for a common emitter configuration, and if a parameter is followed by the subscript c, it indicates that it is for a common collector configuration. Simply listing the configurations without a subscript requires that a person assume that it is a common base configuration. This leads to confusion, and my personal preference is to always designate which configuration is referred to by the parameter. Therefore, in this publication, the parameters will always have the configuration designated with a subscript letter.

The exact same parameters as shown in Figure 20 can be designated as shown in Figure 21.

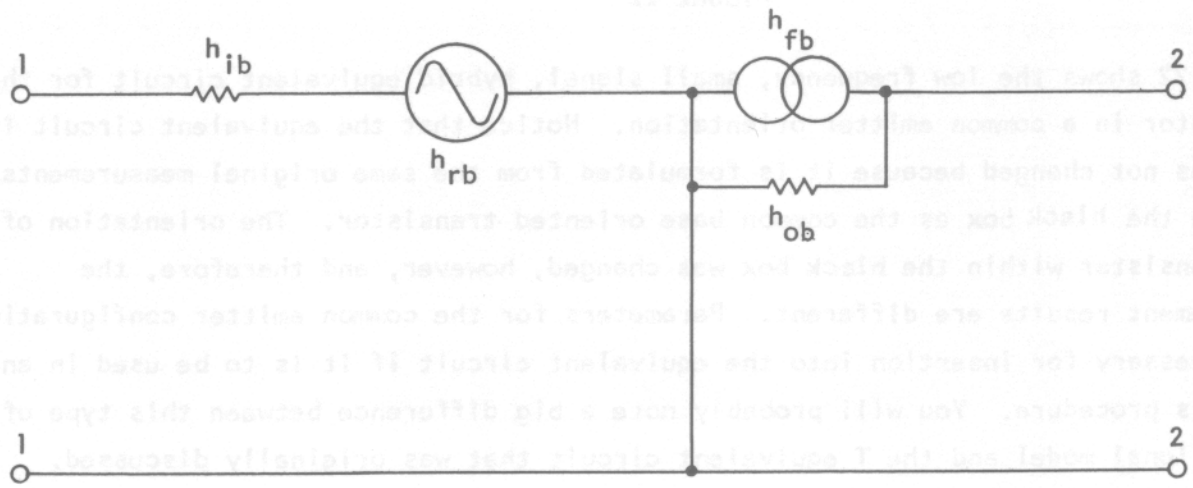


FIGURE 21

h_{11b} in Figure 20 is h_{ib} in Figure 21. The h indicates it is a hybrid parameter, the i indicates input resistance, and the b indicates that it is a common base configuration. Therefore, h_{ib} is the same as h_{11b}, using letter designations rather

than the numbers. The third letter indicates which configuration is being referred to. h_{rb} is the reverse voltage amplification factor, or the generator which indicates what effect the output voltage has on the input voltage, and is the same as h_{12b}. h_{fb} is the forward current gain of the transistor; the h indicating hybrid, the small f indicating forward current transfer or gain, and the b indicating a common base configuration. h_{fb} is also referred to as small signal alpha, or simply alpha. h_{fb} is the same as h_{21} in Figure 20. h_{ob} is the small signal output conductance of the transistor. The h indicates hybrid, the o indicates output conductance, and the b indicates a common base configuration. The use of lower case letters for the parameter designation indicates that they are small signal parameters.

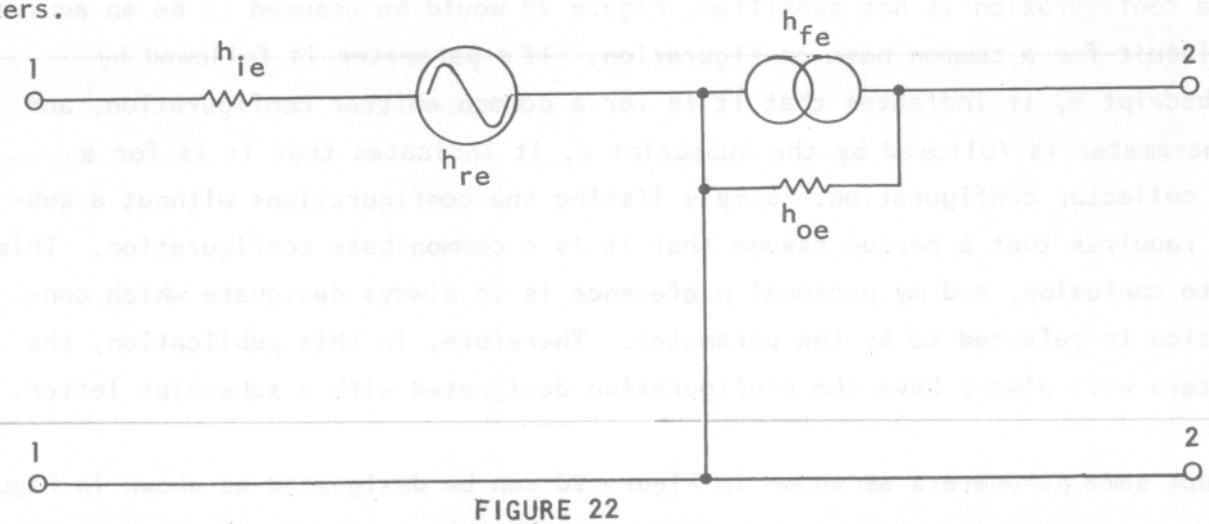


FIGURE 22

Figure 22 shows the low frequency, small signal, hybrid equivalent circuit for the transistor in a common emitter orientation. Notice that the equivalent circuit itself has not changed because it is formulated from the same original measurements made on the black box as the common base oriented transistor. The orientation of the transistor within the black box was changed, however, and therefore, the measurement results are different. Parameters for the common emitter configuration are necessary for insertion into the equivalent circuit if it is to be used in an analysis procedure. You will probably note a big difference between this type of a functional model and the T equivalent circuit that was originally discussed. When the configuration changed, the T equivalent circuit is changed, and the parameters remained constant. With the hybrid equivalent circuit, the equivalent circuit or model remains the same no matter what the orientation of the transistor, and the parameters are different for each configuration. Since a functional model is concerned with results, and much the same results will be obtained if either the

T or hybrid approach is used in analysis, the differences involved are not of consequence.

Figure 22 has the input resistance designated as h_{ie}; the h indicates hybrid, the i indicates input resistance, and the e indicates that the transistor is in a common emitter orientation. The rest of the parameters are similar. h_{fe} is what is normally referred to as the small signal beta, or simply the beta of the transistor.

COMMON BASE: $h_{fb} = h_{21} = h_{21b}$ = alpha
$h_{ib} = h_{11} = h_{11b}$
$h_{ob} = h_{22} = h_{22b}$
$h_{rb} = h_{12} = h_{12b} = \mu_{rb}$

COMMON EMITTER: $h_{fe} = h_{21e}$ = beta
$h_{ie} = h_{11e}$
$h_{oe} = h_{22e}$
$h_{re} = h_{12e} = \mu_{re}$

COMMON COLLECTOR: $h_{fc} = h_{21c}$
$h_{ic} = h_{11c}$
$h_{oc} = h_{12c}$
$h_{rc} = h_{12c} = \mu_{rc}$

FIGURE 23

Figure 23 lists the parameter designations commonly used for the hybrid equivalent circuit for the three configurations. Remember that these parameters are for the low frequency, small signal operation and must be given at a specified static operating point. The parameters will be different at different static operating points.

h_{ob} = COM. BASE - SMALL SIGNAL OUTPUT CONDUCTANCE, INPUT a-c OPEN CIRCUITED
h_{ib} = COM. BASE - SMALL SIGNAL INPUT RESISTANCE, OUTPUT a-c SHORT CIRCUITED
h_{rb} = COM. BASE - SMALL SIGNAL REVERSE VOLTAGE TRANSFER RATIO, INPUT a-c OPEN-CIRCUITED
h_{fb} = COM. BASE
h_{fe} = COM. EMITTER } SMALL SIGNAL FORWARD CURRENT TRANSFER RATIO, OUTPUT a-c SHORT-CIRCUITED
h_{fc} = COM. COL.

OTHER PARAMETERS CORRESPOND WITH THE SUBSCRIPT b REPLACED TO INDICATE CONFIGURATION USED.

FIGURE 24

Figure 24 lists the common parameters associated with the hybrid equivalent circuit and their definitions. Tables 1, 2, and 3 are specification sheets that have been reprinted with the permission of the particular manufacturer involved, and illustrate

how small signal parameters might be designated for the transistor.

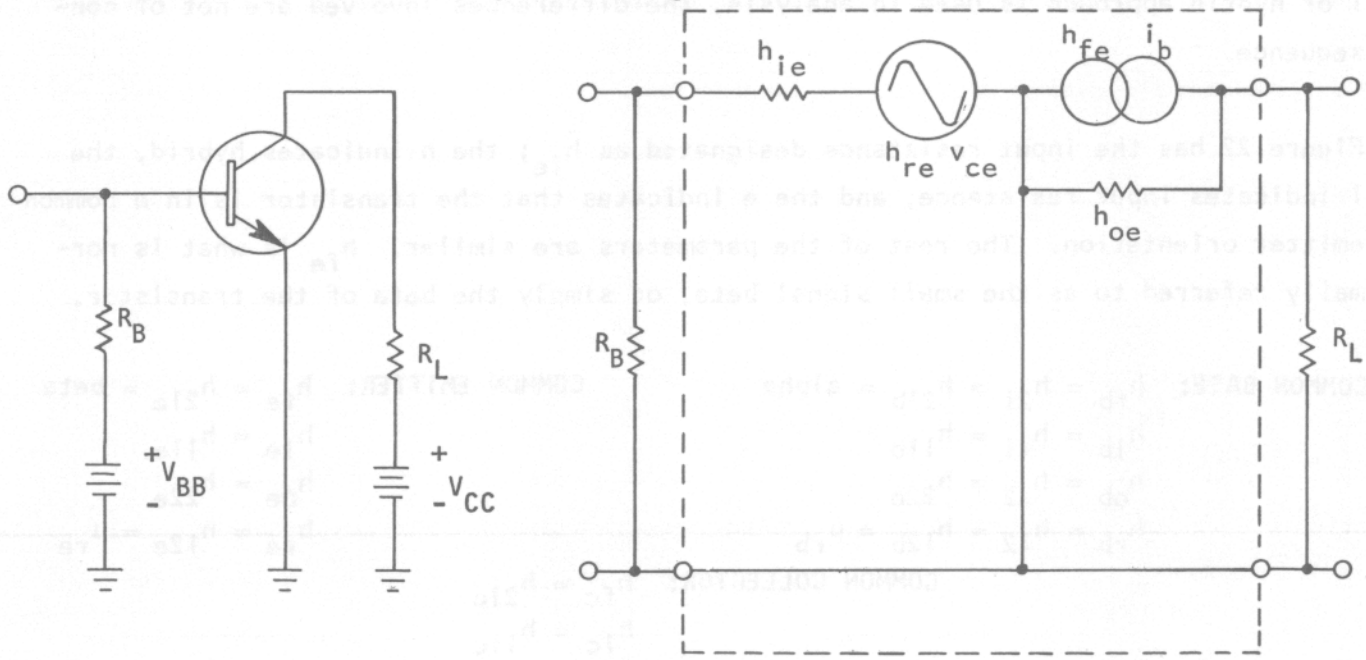


FIGURE 25

Figure 25 shows the schematic diagram of a simple transistor amplifier. The transistor in this particular application happens to be in a common emitter configuration. Shown beside the schematic is the equivalent circuit with the hybrid equivalent circuit substituted for the transistor. Like the examples used when substituting the T equivalent circuit for the transistor, only those components which have an effect on the signal at the frequency of interest are inserted in the equivalent circuit. In the small signal equivalent circuit, the biasing batteries are assumed to be perfect batteries and, therefore, having zero resistance, are disregarded. Any reactive components that are not effective at the particular frequency of interest are disregarded and the equivalent circuit is as shown in Figure 26. The transistor has been replaced by its hybrid equivalent circuit, made up of h_{ie}, h_{re}, h_{fe}, and h_{oe}. The actual values of the voltage and current generators in the equivalent circuit are determined as shown in Figure 26. The voltage generator is the product of h_r and the output voltage variations. The current generator is the product of h_f and the input current variations. Figure 26 shows the equivalent circuit without configuration designation such as common base, common emitter, and common collector configuration. Figure 26 will be used in deriving some transistor gain and impedance formulas. Since the equivalent circuit is the same for all three configurations, the gain and impedance formulas derived will be valid for all three configurations if the parameters for that configuration

to be analyzed are inserted.

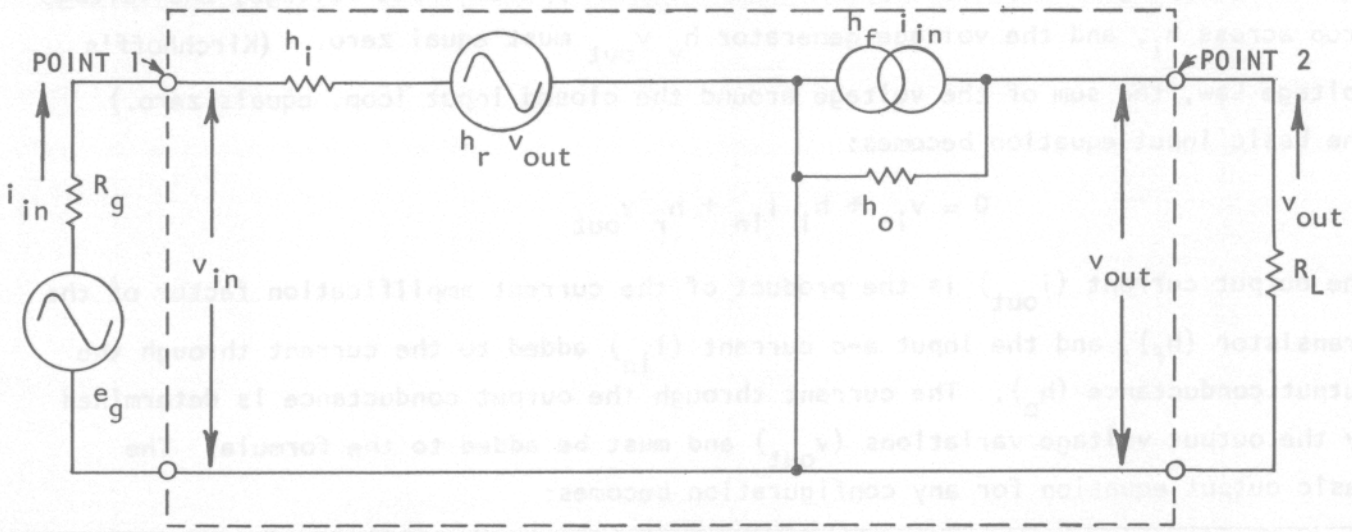


FIGURE 26

DERIVATION OF TRANSISTOR A-C FORMULAS:

When an a-c equivalent circuit of the transistor and its configuration is drawn, the transistor is replaced by its hybrid equivalent circuit and only those components seen by the a-c signal, governed by the considerations under which the parameters were measured, are placed in the equivalent circuit. Under a different set of conditions, a new equivalent circuit must be used. For instance, a high frequency analysis would require high frequency parameters, as the parameters measured at the low frequencies cannot be used.

To gain useable formulas, in terms of the parameters, for dealing with analysis of a transistor configuration, Kirchhoff's equations are written for both closed loops in the equivalent circuit, and these solved for the a-c transistor formulas. It should be made clear at this point that the exact formulas that we will formulate are not too often used in day to day approaches to circuitry. Approximate approaches will be formulated later that are based on these exact approaches. The approximate approaches will probably find the most use.

The initial Kirchhoff equations are in terms of circuit components, parameters, currents, and voltages. The final equations will be in terms of only the parameters and circuit components. The formulas will apply with any applied currents and voltages as long as they meet the conditions under which the parameters were measured.

Referring to Figure 26, the algebraic sum of the applied input voltage, the voltage drop across h_i, and the voltage generator $h_v v_{out}$ must equal zero. (Kirchhoff's Voltage Law, the sum of the voltage around the closed input loop, equals zero.) The basic input equation becomes:

$$0 = v_{in} + h_i\, i_{in} + h_r\, v_{out}$$

The output current (i_{out}) is the product of the current amplification factor of the transistor (h_f), and the input a-c current (i_{in}) added to the current through the output conductance (h_o). The current through the output conductance is determined by the output voltage variations (v_{out}) and must be added to the formula. The basic output equation for any configuration becomes:

$$0 = i_{out} + h_f\, i_{in} + h_o\, v_{out}$$

(Kirchhoff's Current Law writing a nodal equation for point 2 in Figure 26.)

A set of equations can be derived by using the basic input and output equations just written for the closed loops in the equivalent circuit. The parameters and circuit components can then be substituted for the currents and voltages involved.

CIRCUIT CURRENT GAIN:

The basic equation for the current gain of the equivalent circuit in Figure 26 is:

$$A_i = \frac{i_{out}}{i_{in}}$$

Starting with the basic output equation:

$$0 = h_f\, i_{in} + h_o\, v_{out} + i_{out}$$

and by Ohm's Law, $v_{out} = R_L\, i_{out}$, and substituting this into the basic output equation:

$$0 = h_f\, i_{in} + h_o\, R_L\, i_{out} + i_{out}$$

Factoring out i_{out}:

$$0 = h_f\, i_{in} + (h_o\, R_L + 1)\, i_{out}$$

In solving for $\frac{i_{out}}{i_{in}}$, which is A_i:

$$A_i = \frac{i_{out}}{-i_{in}} = \frac{-h_f}{1 + h_o\, R_L}$$

The equation for current gain in terms of parameters and circuit components becomes:

$$A_i = \frac{h_f}{1 + h_o R_L}$$

This formula, as well as others that will follow in this example, may be used to determine the current gain of any of the three configurations if the proper parameters and circuit components are inserted. This, of course, is because the equivalent circuit is based on the measurements made on the black box or linear four-terminal network, and the orientation of the transistor does not enter into it. Only the measurement results which give the parameters for insertion into the equivalent circuit will be governed by the orientation of transistor. A major difference between the hybrid equivalent circuit and the T equivalent circuit is that the hybrid equivalent circuit and the gain and impedance equations are the same regardless of the orientation of the transistor, whereas the T equivalent circuit has different equations and equivalent circuits for each of the three configurations.

CIRCUIT VOLTAGE GAIN:

The basic equation for voltage gain is:

$$A_v = \frac{v_{out}}{v_{in}}$$

To formulate an equation for the voltage gain in Figure 26, the Kirchhoff equations can once again be used:

$$0 = h_f i_{in} + h_o v_{out} + i_{out}$$

By Ohm's Law:

$$i_{out} = \frac{v_{out}}{R_L}$$

Substituting for i_{out}:

$$0 = h_f i_{in} + h_o v_{out} + \frac{v_{out}}{R_L}$$

To gain an expression for i_{in}, transpose:

$$0 = v_{in} + h_i i_{in} + h_r v_{out}$$

to read:

$$i_{in} = \frac{-v_{in}}{h_i} - \frac{h_r\, v_{out}}{h_i}$$

and substituting for i_{in}:

$$0 = h_f\left(\frac{-v_{in}}{h_i} - \frac{h_r\, v_{out}}{h_i}\right) + h_o\, v_{out} + \frac{v_{out}}{R_L}$$

Factoring v_{out} and rearranging:

$$\left(h_o + \frac{1}{R_L} - \frac{h_f\, h_r}{h_i}\right) v_{out} = \frac{h_f\,(-v_{in})}{h_i}$$

Multiply both sides by the expressions:

$$\frac{1}{-v_{in}} \text{ and } \frac{1}{h_o + \frac{1}{R_L} - \frac{h_f\, h_r}{h_i}}$$

to get:

$$\frac{v_{out}}{-v_{in}} = \frac{-h_f}{h_i\left[h_o + \frac{1}{R_L} - \frac{h_f\, h_r}{h_i}\right]} = A_v$$

Expanding the denominator and multiplying by R_L:

$$A_v = \frac{-h_f\, R_L}{(h_i\, h_o - h_f\, h_r)\, R_L + h_i}$$

and the equation for circuit voltage gain is:

$$A_v = \frac{-h_f\, R_L}{\Delta^h\, R_L + h_i}$$

where:

$$\Delta^h = h_i\, h_o - h_f\, h_r$$

INPUT RESISTANCE:

The equation for a-c resistance as seen at the input terminals of the transistor circuit can be formulated using the basic equation:

$$0 = v_{in} + h_i\ i_{in} + h_r\ v_{out}$$

The basic equation for input resistance is:

$$r_i = \frac{v_{in}}{i_{in}}$$

For the configuration in Figure 26:

$$0 = v_{in} + h_i\ i_{in} + h_r\ v_{out}$$

Transposing:

$$\frac{-v_{in}}{-i_{in}} = h_i + h_r \frac{v_{out}}{i_{in}}$$

To find an expression for $\frac{v_{out}}{i_{in}}$, the basic output equation is rewritten:

$$0 = h_f\ i_{in} + \left(h_o + \frac{1}{R_L}\right) v_{out}$$

and solving for $\frac{v_{out}}{i_{in}}$:

$$\frac{v_{out}}{i_{in}} = \frac{-h_f}{h_o + \frac{1}{R_L}}$$

Substituting for $\frac{v_{out}}{i_{in}}$ in the equation:

$$r_i = \frac{-v_{in}}{-i_{in}} = h_i + h_r \frac{v_{out}}{i_{in}}$$

It becomes:

$$r_i = h_i + h_r \frac{-h_f}{h_o + \frac{1}{R_L}}$$

Rearranging:

$$r_i = \frac{h_i + (h_i\, h_o - h_f\, h_r)\, R_L}{1 + h_o\, R_L}$$

and the equation for input resistance is:

$$r_i = \frac{h_i + \Delta^h\, R_L}{1 + h_o\, R_L}$$

where:

$$\Delta^h = h_i\, h_o - h_f\, h_r$$

OUTPUT RESISTANCE:

To formulate an equation for the a-c output resistance of the circuit, the current generator in Figure 26, along with its shunt conductance, is replaced by a voltage generator and its series resistance. Dividing the value of the current generator by its shunt conductance gives the value of the voltage generator. The series resistance is the reciprocal of the output conductance.

Since the desired information is the resistance as seen looking in the output terminals, the driving generator is moved to the output as illustrated in Figure 27. The driving source resistance (R_g) will effect the output resistance; therefore, it is left in the input of the equivalent circuit.

The input current and voltage relationship can be written:

$$h_r\, v_{out} = h_i\, i_{in} + R_g\, i_{in}$$

and the output current and voltage relationship can be written:

$$v_g = R_L\, i_{out} + \frac{i_{out}}{h_o} + \frac{h_f\, i_{in}}{h_o}$$

The driving source (v_g) in the right hand diagram in Figure 27 sees a series circuit of R_L and r_o, as shown in Figure 28.

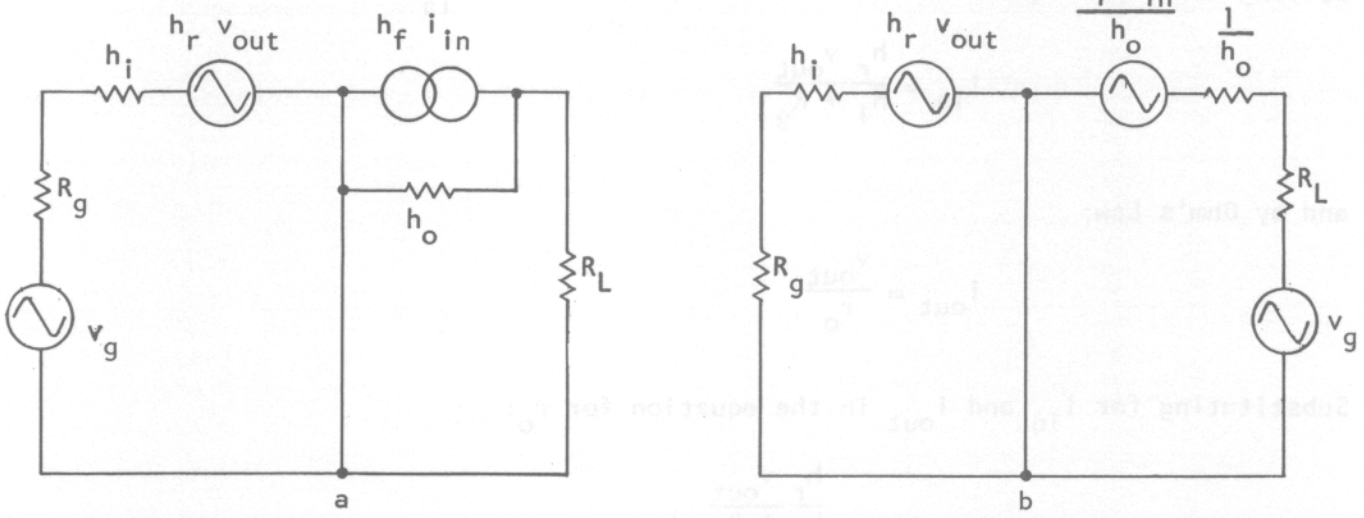


FIGURE 27

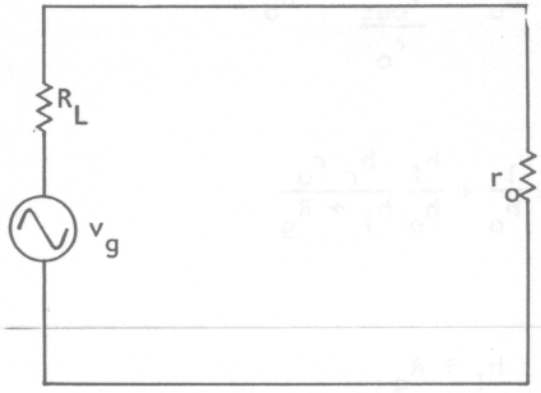


FIGURE 28

The equation for v_g can read:

$$v_g = R_L\ i_{out} + r_o\ i_{out}$$

Substituting for v_g in the output equation:

$$R_L\ i_{out} + r_o\ i_{out} = R_L\ i_{out} + \frac{i_{out}}{h_o} + \frac{h_f\ i_{in}}{h_o}$$

Subtracting $R_L\ i_{out}$ from both sides and dividing through by i_{out}:

$$r_o = \frac{1}{h_o} + \frac{h_f}{h_o}\frac{i_{in}}{i_{out}}$$

Solving the input equation to obtain an expression for i_{in}:

$$i_{in} = \frac{h_r \, v_{out}}{h_i + R_g}$$

and by Ohm's Law:

$$i_{out} = \frac{v_{out}}{r_o}$$

Substituting for i_{in} and i_{out} in the equation for r_o:

$$r_o = \frac{1}{h_o} + \frac{\dfrac{h_r \, v_{out}}{h_i + R_g}}{\dfrac{v_{out}}{r_o}} \frac{h_f}{h_o}$$

Simplified:

$$r_o = \frac{1}{h_o} + \frac{h_f}{h_o} \frac{h_r \, r_o}{h_i + R_g}$$

Rearranged:

$$r_o = \frac{h_i + R_g}{\Delta^h + h_o \, R_g}$$

Where:

$$\Delta^h = h_i \, h_o - h_f \, h_r$$

The parameters for the transistor are measured at a given d-c operating point and configuration. If other than the situation under which the parameters were measured exists, the parameters for the transistor must be adjusted for the configuration and operating point used before insertion into the equations.

These are a-c equations, and the components and parameters inserted in the equations must be a-c components and parameters. As an example, R_L in the equations must be the actual a-c or signal load resistance the transistor sees at the frequency of

interest. If the collector load is shunted by the input circuit of the following stage, this must be taken into account when calculating the a-c load resistance. These formulas are useable with any low frequency small signal configuration if the proper parameters for operating point and configuration are inserted. Figure 29 lists the equations for the hybrid equivalent circuit when dealing with small signals and low frequencies. Since the formulas remain the same regardless of the configuration, the configuration has not been specified in the equations in Figure 29. The parameters are different for each configuration.

Figure 29 also lists conversion formulas for transposing from common base to common emitter or common collector. Of course, the formulas listed in Figure 30 can also be transposed to solve for any unknown value.

To take external series shunt or feedback components into account, Figures 30 and 31 list formulas to allow the modification of the h parameters when there are external or feedback components involved. When external series, shunt or feedback components are involved, the original parameters can be adjusted for operating point, then inserted into the formulas in Figures 30 and 31.

The resultant parameters (given with an X in parenthesis to indicate they are modified parameters) may be inserted directly into the gain and resistance formulas for the hybrid circuit previously discussed. When this is done, there is no need to include the external components in the equivalent circuit because they are now part of the equivalent circuit and represented by the modified parameters. If the parameters are not modified using the equations in Figures 30 and 31, the basic theorems must be applied to solve for the effects of series, shunt, or feedback components. Either way is just as valid, and personal preference will play a part in selecting the approach. When more than one stage is involved, such as the transistor cascade in Figure 32, some initial considerations must be made.

TWO-STAGE A-C ANALYSIS PROCEDURE:

The parameters of the transistor must be known if the hybrid approach which we have just discussed is going to be used. Parameters are given in the manufacturers' reference under a given set of conditions (i.e., frequency, static emitter current, collector voltage, etc.).

These equations are for any configuration. Insert the parameters for the configuration to be analyzed.

Input resistance: $r_i = \dfrac{h_i + \Delta^h R_L}{1 + h_o R_L}$

Output resistance: $r_o = \dfrac{h_i + R_g}{\Delta^h + h_o R_g}$

Current gain: $A_i = \dfrac{h_f}{1 + h_o R_L}$

Voltage gain: $A_v = \dfrac{-h_f R_L}{\Delta^h R_L + h_i}$

Power gain: $A_p = \dfrac{h_f^2 R_L}{(1 + h_o R_L)(\Delta^h R_L + h_i)}$

WHERE: $\Delta^h = h_i h_o - h_f h_r$

R_L = a-c load resistance

R_g = input generator resistance

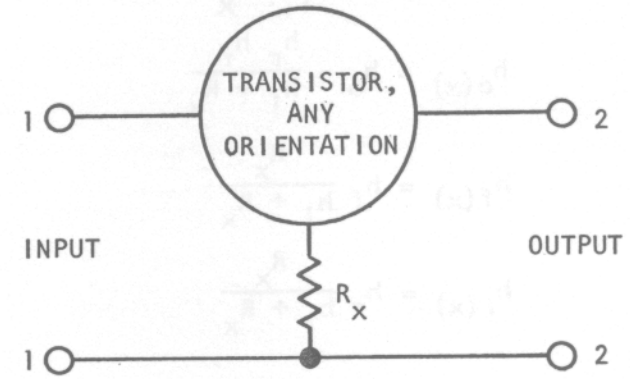
NOTE: h_{fb} is a negative quantity.

	COMMON BASE	COMMON EMITTER	COMMON COLLECTOR
	PARAMETER	CONVERSION FORMULA	CONVERSION FORMULA
1	h_{ib} or h_{11}	$h_{ie} = \dfrac{h_{ib}}{1 + h_{fb}}$	$h_{ic} = \dfrac{h_{ib}}{1 + h_{fb}}$
2	h_{rb} or h_{12}	$h_{re} = \dfrac{\Delta^h_b - h_{rb}}{1 + h_{rb}}$	$h_{rc} = 1$
3	h_{fb} or h_{21}	$h_{fe} = -\dfrac{h_{fb}}{1 + h_{fb}}$	$h_{fc} = -\dfrac{1}{1 + h_{fb}}$
4	h_{ob} or h_{22}	$h_{oe} = \dfrac{h_{ob}}{1 + h_{fb}}$	$h_{oc} = \dfrac{h_{ob}}{1 + h_{fb}}$

NOTE: $\Delta^h_b = h_{ib} h_{ob} - h_{rb} h_{fb}$.

FIGURE 29

MODIFIED h PARAMETERS TO INCLUDE EXTERNAL AND FEEDBACK RESISTANCES

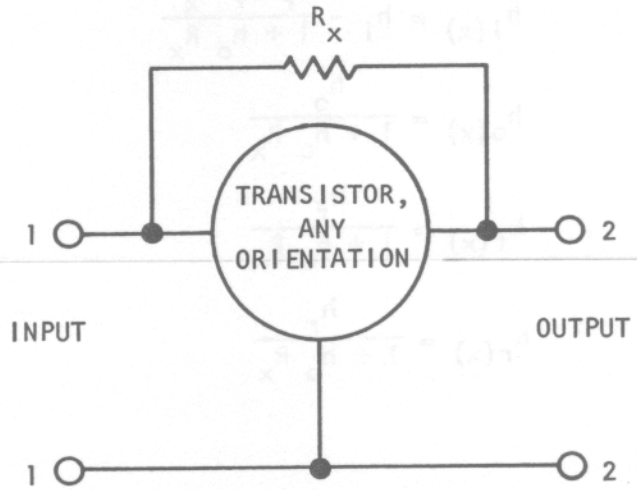


$$h_{i(x)} = h_i + \frac{(h_f + 1)\, R_x}{1 + h_o\, R_x}$$

$$h_{o(x)} = \frac{h_o}{1 + h_o\, R_x}$$

$$h_{f(x)} = \frac{h_f - h_o\, R_x}{1 + h_o\, R_x}$$

$$h_{r(x)} = \frac{h_r + h_o\, R_x}{1 + h_o\, R_x}$$

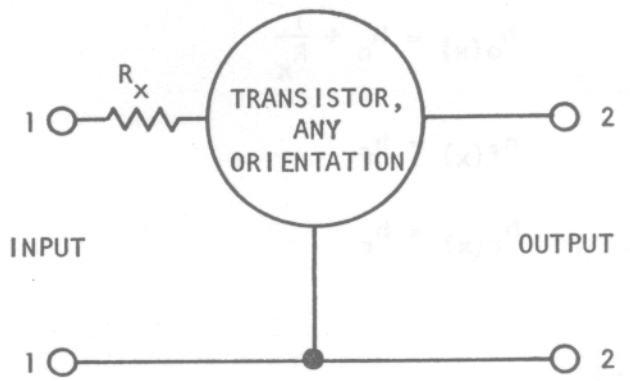


$$h_{i(x)} = \frac{h_i\, R_x}{h_i + R_x}$$

$$h_{o(x)} = h_o + \frac{(h_f + 1)\quad (1 - h_r)}{h_i + R_x}$$

$$h_{f(x)} = \frac{h_f\, R_x - h_i}{h_i + R_x}$$

$$h_{r(x)} = h_r + \frac{h_i\, (1 - h_r)}{h_i + R_x}$$



$$h_{i(x)} = h_i + R_x$$

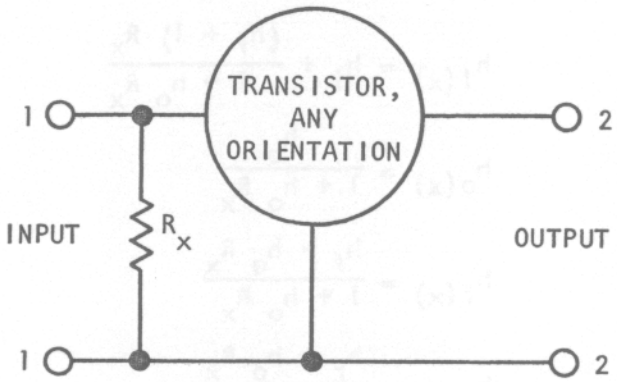
$$h_{o(x)} = h_o$$

$$h_{f(x)} = h_f$$

$$h_{r(x)} = h_r$$

FIGURE 30

MODIFIED h PARAMETERS TO INCLUDE EXTERNAL AND FEEDBACK RESISTANCES

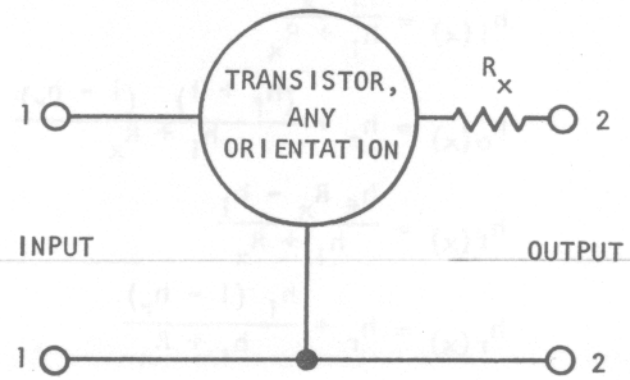


$$h_{i(x)} = h_i \frac{R_x}{h_i + R_x}$$

$$h_{o(x)} = h_o - \frac{h_r h_f}{h_i + R_x}$$

$$h_{f(x)} = h_f \frac{R_x}{h_i + R_x}$$

$$h_{r(x)} = h_r \frac{R_x}{h_i + R_x}$$

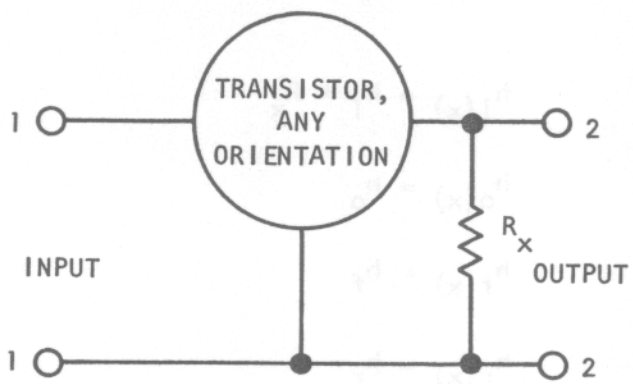


$$h_{i(x)} = h_i - \frac{h_r h_f R_x}{1 + h_o R_x}$$

$$h_{o(x)} = \frac{h_o}{1 + h_o R_x}$$

$$h_{f(x)} = \frac{h_f}{1 + h_o R_x}$$

$$h_{r(x)} = \frac{h_r}{1 + h_o R_x}$$



$$h_{i(x)} = h_i$$

$$h_{o(x)} = h_o + \frac{1}{R_x}$$

$$h_{f(x)} = h_f$$

$$h_{r(x)} = h_r$$

FIGURE 31

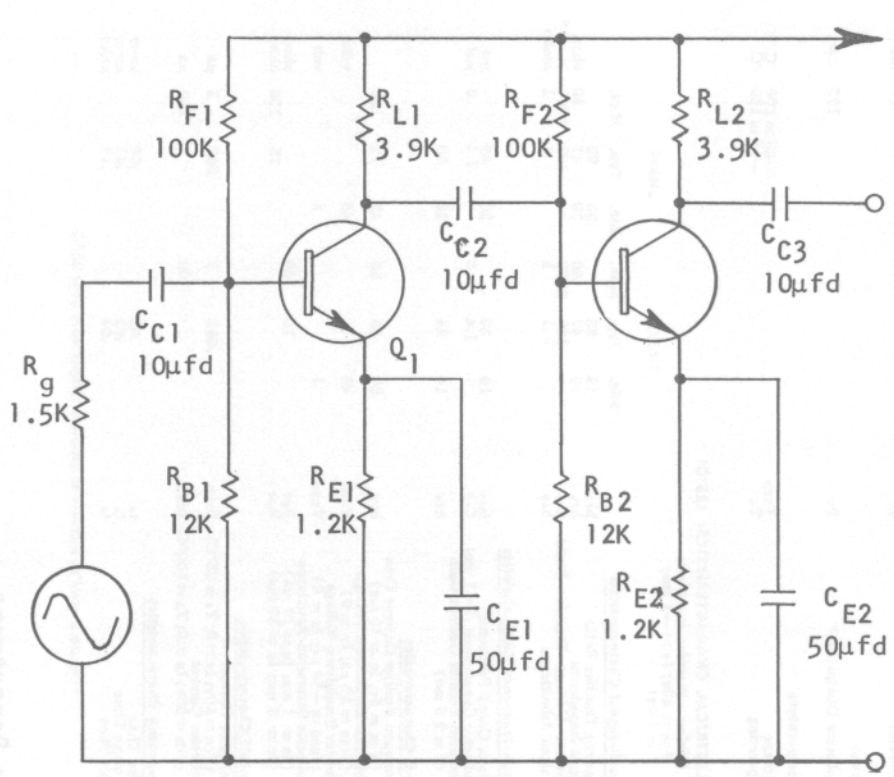


FIGURE 32

PARAMETERS

$h_{fe} = 44$

$h_{re} = 3.37 \times 10^{-4}$

$h_{ie} = 1400\Omega$

$h_{oe} = 27\mu mhos$

$\Delta h_e = 2.3 \times 10^{-2}$

Ohm's Law, Thevenin's Theorem, etc., can be used to determine the static emitter current and collector voltage for the circuits to be analyzed. The parameters, of necessity, must be adjusted to this set of conditions. Another method might be to measure the parameters of the transistor on the Tektronix Type 575 Transistor Curve Tracer at the operating point of the transistor in the circuit. If the parameters for the transistor are given in terms of common base, they must be converted to common emitter parameters for use with the configuration in Figure 32.

When two transistor amplifier stages are cascaded, the equivalent circuit will show the bias network and the input resistance to the second state as appearing in parallel with the load resistor of the first stage. Since the input resistance of the first stage is dependent on the input resistance of the second stage, we must solve for the input resistance of the second stage before dealing with the first stage. We might conclude from this that the second stage must be approached before the first stage.

The parameters might be obtained from a specification sheet, such as shown in Figure 33. The hybrid small signal parameters other than h_{fe} are given as common

20. TRANSISTOR SPECIFICATIONS

HOW TO READ A SPECIFICATION SHEET

Semiconductors are available in a large variety of different types, each with its own unique characteristics. At the present time there are over 2200 different types of diodes and rectifiers and over 750 different types of transistors being manufactured.

The Characteristics of each of these devices are usually presented in specification sheets similar to the ones represented on page 205 and page 306 respectively. These specifications, particularly the transistor specification on the next page, contain many terms and ratings that are probably new to you, so we have selected several of the more important ones and explained what they mean.

NOTES ON TRANSISTOR SPECIFICATION SHEET

① The lead paragraph is a general description of the device and usually contains three specific pieces of information — The kind of transistor, in this case a silicon NPN triode, — A few major application areas, amplifier and switch, — General sales features, electrical stability and a standard size hermetically sealed package.

② The **Absolute Maximum Ratings** are those ratings which should not be exceeded under any circumstances. Exceeding them may cause device failure.

③ The **Power Dissipation** of a transistor is limited by its junction temperature. Therefore, the higher the temperature of the air surrounding the transistor (ambient temperature), the less power the device can dissipate. A factor telling how much the transistor must be derated for each degree of increase in ambient temperature in degrees centigrade is usually given. Notice that this device can dissipate 125mw at 25°C. By applying the given derating factor of 1mw for each degree increase in ambient temperature, we find that the power dissipation has dropped to 0mw at 150°C, which is the maximum operating temperature of this device.

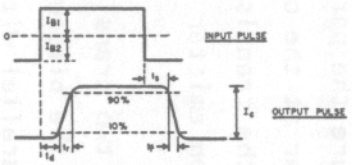
④ All of the remaining ratings define what the device is capable of under specified test conditions. These characteristics are needed by the design engineer to design matching networks and to calculate exact circuit performance.

⑤ **Current Transfer Ratio** is another name for beta. In this case we are talking about an a-c characteristic, so the symbol is h_{fe}. Many specification sheets also list the d-c beta using the symbol h_{FE}. Beta is partially dependent on frequency, so some specifications list beta for more than one frequency.

⑥ The **Frequency Cutoff** f_{hfb} of a transistor is defined as that frequency at which the grounded base current gain drops to .707 of the 1kc value. It gives a rough indication of the useful frequency range of the device.

⑦ The **Collector Cutoff Current** is the leakage current from collector to base when no emitter current is being applied. This leakage current varies with temperature changes and must be taken into account whenever any semiconductor device is designed into equipment used over a wide range of ambient temperature.

⑧ The **Switching Characteristics** given show how the device responds to an input pulse under the specified driving conditions. These response times are very dependent on the circuit used. The terms used are explained in the curves at right.



2N337, 2N338

Outline Drawing No. 4

① The General Electric Types 2N337 and 2N338 are high-frequency silicon NPN transistors intended for amplifier applications in the audio and radio frequency range and for high-speed switching circuits. They are grown junction devices with a diffused base and are manufactured in the Fixed-Bed Mounting design for extremely high mechanical reliability under severe conditions of shock, vibration, centrifugal force, and temperature. For electrical reliability and parameter stability, all transistors are subjected to a minimum 160 hour 200°C cycled aging operation included in the manufacturing process. These transistors are hermetically sealed in welded cases. The case dimensions and lead configuration conform to JEDEC standards and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

② **ABSOLUTE MAXIMUM RATINGS: (25°C)**

Voltage			
Collector to Base	V_{CBO}	45	volts
Emitter to Base	V_{EBO}	1	volt
Current			
Collector	I_C	20	ma
③ **Power**			
Collector Dissipation*	P_C	125	mw
Temperature			
Storage	T_{STG}	−65 to 200	°C
Operating	T_A	−65 to 150	°C

④ **ELECTRICAL CHARACTERISTICS: (25°C)**
(Unless otherwise specified; $V_{CB} = 20v$; $I_E = -1$ ma; f = 1 kc)

		2N337			2N338			
Small-Signal Characteristics		Min.	Typ.	Max.	Min.	Typ.	Max.	
⑤ Current Transfer Ratio	h_{fe}	19	55		39	99		
Input Impedance	h_{ib}	30	47	80	30	47	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}		180	2000		200	2000	$\times 10^{-6}$
Output Admittance	h_{ob}		.1	1		.1	1	μmho
High-Frequency Characteristics								
⑥ Alpha Cutoff Frequency	f_{hfb}	10	30		20	45		mc
Collector Capacitance (f = 1 mc)	C_{ob}		1.4	3		1.4	3	μμf
Common Emitter Current Gain (f = 2.5 mc)	h_{fe}	14	24		20	26		
D-C Characteristics								
Common Emitter Current Gain ($V_{CE} = 5v$; $I_C = 10$ ma)	h_{FE}	20	35	55	45	75	150	
Collector Breakdown Voltage ($I_{CBO} = 50$ μa; $I_E = 0$)	V_{CBO}	45			45			volts
Emitter Breakdown Voltage ($I_{EBO} = -50$ μa; $I_C = 0$)	V_{EBO}	1			1			volt
Collector Saturation Resistance ($I_B = 1$ ma; $I_C = 10$ ma)	R_{SC}		75	150				ohms
($I_B = .5$ ma; $I_C = 10$ ma)	R_{SC}					75	150	ohms
Cutoff Characteristics								
⑦ Collector Current ($V_{CB} = 20v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.002	1		.002	1	μa
Collector Current ($V_{CB} = 20v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			100			100	μa
Switching Characteristics								
⑧ Rise Time	t_r		.02			.06		μsecs
Storage Time	t_s		.02			.02		μsecs
Fall Time	t_f		.04			.14		μsecs

*Derate 1 mw/°C increase in ambient temperature over 25°C

Courtesy of General Electric Company, Semiconductor Products Department

FIGURE 33

base parameters in Figure 33. These must be changed to common emitter parameters for analysis of the configuration in figure 32. Figure 34 lists all equations needed to transpose hybrid parameters from one configuration to another. It also allows the T equivalent circuit parameters to be found when the hybrid parameters are given, or the hybrid parameters to be found if the T parameters are given.

The parameters are for a given d-c operating point. The operating point is 1ma of emitter current, and 20v of collector voltage for the transistor in Figure 33. If the operating point is other than that of which the parameters are given, the parameters must be modified for the new point of d-c operation. A chart such as shown in Figure 35 is sometimes supplied by the manufacturer and may be used to modify the parameters to the new operating point.

In analyzing a two-stage amplifier, such as shown in Figure 32, the first steps might be to find the gain and input resistance of the output stage. The equivalent load resistance of the first stage can then be found by paralleling the biasing resistors, r_{b2} and r_{f2}, with r_{i2} and R_{L1}. This equivalent value is the load resistance of the first stage. Voltage and current gain will be governed by this a-c value and not the d-c load resistance.

To determine the interstage gain, the equations in Figures 30 and 31 can be used to modify the parameters to take into account the series or shunting components, or the formula below can be used with the configuration in Figure 32. Current gain of the interstage network:

$$A_{i(\text{interstage})} = \frac{r_{eq}}{r_{eq} + r_{i2}}$$

Where r_{eq} is the parallel combination of R_{L1}, R_{B2}, and R_{F2}. Since all of the driving current will not enter the input of the transistor, this same approach can be used in the input circuit of the first stage.

$$A_{i\ (\text{pre-stage})} = \frac{r_{eq}}{r_{eq} + r_{i1}}$$

Where r_{eq} is the parallel resistance of R_{B1} and R_{F1}. The interstage voltage gain is unity as long as no impedance is placed in series with the signal.

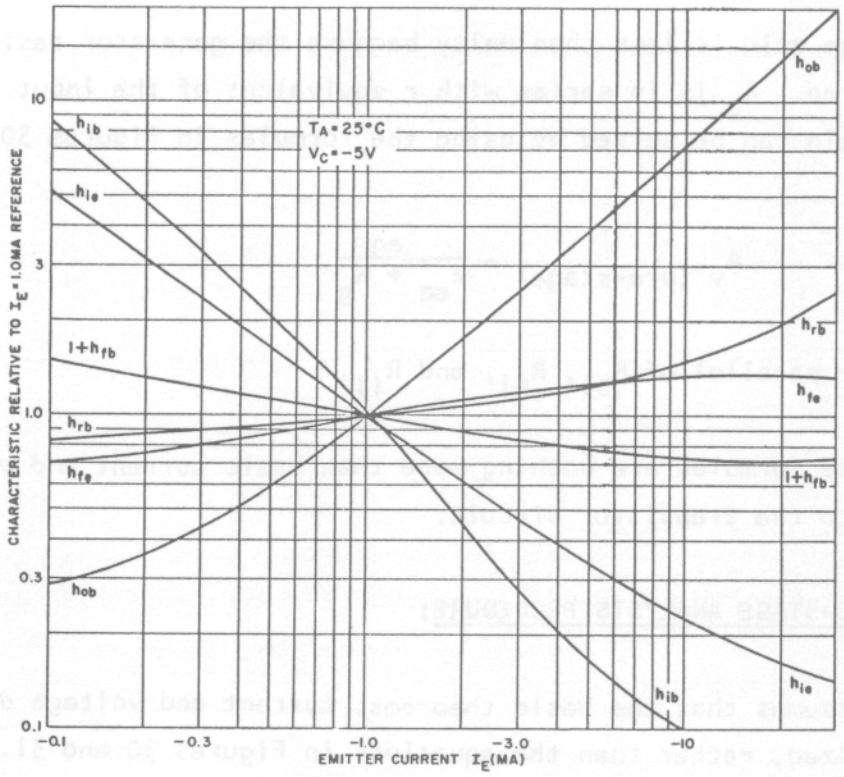
(NUMERICAL VALUES ARE TYPICAL FOR THE 2N525 AT 1MA, 5V)

SYMBOLS		COMMON EMITTER	COMMON BASE	COMMON COLLECTOR	T EQUIVALENT CIRCUIT (APPROXIMATE)
IRE	OTHER				
h_{ie}	h_{11e}, $\frac{1}{Y_{11e}}$	1400 OHMS	$\frac{h_{ib}}{1+h_{fb}}$	h_{ic}	$r_b+\frac{r_e}{1-\alpha}$
h_{re}	h_{12e}, μ_{bc}, μ_{re}	3.37×10^{-4}	$\frac{h_{ib}h_{ob}}{1+h_{fb}}-h_{rb}$	$1-h_{rc}$	$\frac{r_e}{(1-\alpha)r_c}$
h_{fe}	h_{21e}, β	44	$-\frac{h_{fb}}{1+h_{fb}}$	$-(1+h_{fc})$	$\frac{\alpha}{1-\alpha}$
h_{oe}	h_{22e}, $\frac{1}{Z_{22e}}$	27×10^{-6} MHOS	$\frac{h_{ob}}{1+h_{fb}}$	h_{oc}	$\frac{1}{(1-\alpha)r_c}$
h_{ib}	h_{11}, $\frac{1}{Y_{11}}$	$\frac{h_{ie}}{1+h_{fe}}$	31 OHMS	$-\frac{h_{ic}}{h_{fc}}$	$r_e+(1-\alpha)r_b$
h_{rb}	h_{12}, μ_{ec}, μ_{rb}	$\frac{h_{ie}h_{oe}}{1+h_{fe}}-h_{re}$	5×10^{-4}	$h_{rc}-1-\frac{h_{ic}h_{oc}}{h_{fc}}$	$\frac{r_b}{r_c}$
h_{fb}	h_{21}, α	$-\frac{h_{fe}}{1+h_{fe}}$	−0.978	$-\frac{1+h_{fc}}{h_{fc}}$	$-\alpha$
h_{ob}	h_{22}, $\frac{1}{Z_{22}}$	$\frac{h_{oe}}{1+h_{fe}}$	0.60×10^{-6} MHOS	$-\frac{h_{oc}}{h_{fc}}$	$\frac{1}{r_c}$
h_{ic}	h_{11c}, $\frac{1}{Y_{11c}}$	h_{ie}	$\frac{h_{ib}}{1+h_{fb}}$	1400 OHMS	$r_b+\frac{r_e}{1-\alpha}$
h_{rc}	h_{12c}, μ_{be}, μ_{rc}	$1-h_{re}$	1	1.00	$1-\frac{r_e}{(1-\alpha)r_c}$
h_{fc}	h_{21c}, α_{eb}	$-(1+h_{fe})$	$-\frac{1}{1+h_{fb}}$	−45	$-\frac{1}{1-\alpha}$
h_{oc}	h_{22c}, $\frac{1}{Z_{22c}}$	h_{oe}	$\frac{h_{ob}}{1+h_{fb}}$	27×10^{-6} MHOS	$\frac{1}{(1-\alpha)r_c}$
α		$\frac{h_{fe}}{1+h_{fe}}$	$-h_{fb}$	$\frac{1+h_{fc}}{h_{fc}}$	0.978
r_c		$\frac{1+h_{fe}}{h_{oe}}$	$\frac{1-h_{rb}}{h_{ob}}$	$-\frac{h_{fc}}{h_{oc}}$	1.67 MEG
r_e		$\frac{h_{re}}{h_{oe}}$	$h_{ib}-\frac{h_{rb}}{h_{ob}}(1+h_{fb})$	$\frac{1-h_{rc}}{h_{oc}}$	12.5 OHMS
r_b		$h_{ie}-\frac{h_{re}}{h_{oe}}(1+h_{fe})$	$\frac{h_{rb}}{h_{ob}}$	$h_{ic}+\frac{h_{fc}}{h_{oc}}(1-h_{rc})$	840 OHMS

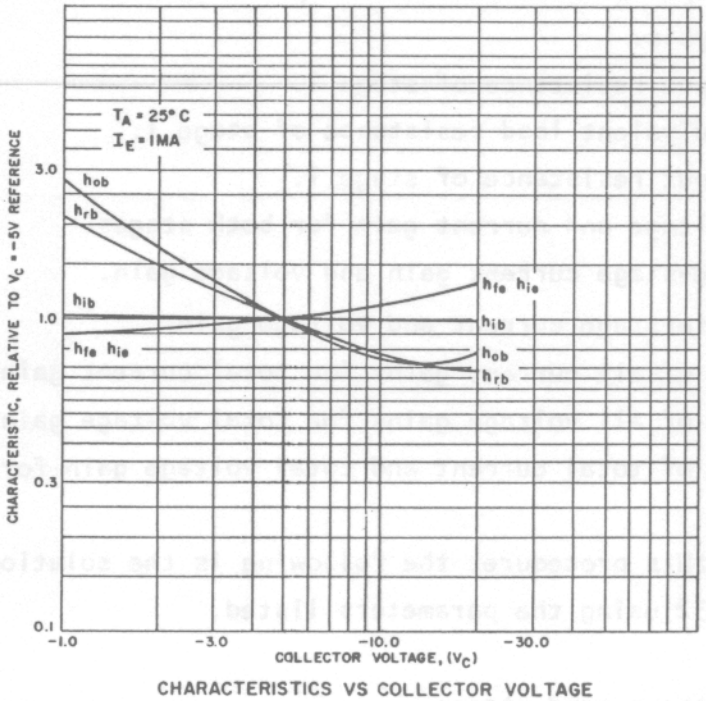
APPROXIMATE CONVERSION FORMULAE h-PARAMETERS AND T-EQUIVALENT CIRCUIT

Courtesy of General Electric Company, Semiconductor Products Department

FIGURE 34



CHARACTERISTICS VS EMITTER CURRENT



CHARACTERISTICS VS COLLECTOR VOLTAGE

VARIATION OF h-PARAMETERS WITH BIAS CONDITIONS

Courtesy of General Electric Company, Semiconductor Products Department

FIGURE 35

Pre-stage voltage gain is less than unity because the generator resistance, R_g, must be considered. R_g is in series with r equivalent of the input stage. Pre-stage voltage gain can be solved by using the formulas in Figures 30 and 31, or the formula:

$$A_v \text{ (pre-stage)} = \frac{r_{eq}}{r_{eq} + R_g}$$

Where R_{eq} is the parallel of R_{B1}, R_{F1}, and R_{i1}.

Notice that these formulas are nothing more than basic current and voltage divider theory applied to the transistor circuit.

STEP BY STEP TWO-STAGE ANALYSIS PROCEDURE:

The following assumes that the basic theorems, current and voltage divider theory theory are utilized, rather than the equations in Figures 30 and 31.

A. Determine the proper parameters for the operating point of the circuit configuration under analysis.
B. Calculate the input resistance of stage 2.
C. Calculate the equivalent load resistance of stage 1.
D. Calculate the input resistance of stage 1.
E. Calculate the voltage and current gain for both stages.
F. Calculate the pre-stage current gain and voltage gain.
G. Calculate the interstage current and voltage gain.
H. Take the product of all current gains for total current gain.
I. Take the product of all voltage gains for total voltage gain.
J. Take the product of total current and total voltage gain for total power gain.

As an example using this procedure, the following is the solution of the two-stage amplifier in Figure 32 using the parameters listed.

Input resistance of the second stage:

$$r_{i2} = \frac{h_{ie} + \Delta h_e R_L}{1 + h_{oe} R_L} = \frac{1.4 \times 10^3 + 2.3 \times 10^{-2}\ 3.9 \times 10^3}{1 + 27 \times 10^{-6}\ 3.9 \times 10^3} = 1.35k\Omega$$

The equivalent small signal load resistance of the first stage:

$$R_{L1(a\text{-}c)} = \frac{1}{\frac{1}{R_{L1}} + \frac{1}{R_{B2}} + \frac{1}{R_{F2}} + \frac{1}{r_{i2}}} = 917\Omega$$

The input resistance of the first stage:

$$r_{i1} = \frac{h_{ie} + \Delta^{h}e\ R_L}{1 + h_{oe}\ R_L} = \frac{1.4 \times 10^3 + 2.3 \times 10^{-2}\ 0.917 \times 10^3}{1 + 27 \times 10^{-6}\ 0.917 \times 10^3} = 1.39k\Omega$$

The voltage gain of the second stage:

$$A_{v2} = \frac{h_{fe}\ R_L}{\Delta^{h}e\ R_L + h_{ie}} = \frac{44\ \ 3.9 \times 10^3}{2.3 \times 10^{-2}\ 3.9 \times 10^3 + 1.4 \times 10^3} = 115$$

The current gain of the second stage:

$$A_{i2} = \frac{h_{fe}}{1 + h_{oe}\ R_L} = \frac{44}{1 + 27 \times 10^{-6}\ 3.9 \times 10^3} = 39.8$$

The voltage gain of the first stage:

$$A_{v1} = \frac{h_{fe}\ R_L}{\Delta^{h}e\ R_L + h_{ie}} = \frac{44\ \ 0.917 \times 10^3}{2.3 \times 10^{-2}\ 0.917 \times 10^3 + 1.4 \times 10^3} = 28.35$$

The current gain of the first stage:

$$A_{i1} = \frac{h_{fe}}{1 + h_{oe}\ R_L} = \frac{44}{1 + 27 \times 10^{-6}\ 0.917 \times 10^3} = 43$$

The interstage voltage gain is unity.

The interstage current gain:

$$A_{i(interstage)} = \frac{r_{eq}}{r_{eq} + r_{i2}} = \frac{2.86 \times 10^3}{4.21 \times 10^3} = 0.68$$

Where:

$$r_{eq} = \frac{1}{\frac{1}{R_{L1}} + \frac{1}{R_{B2}} + \frac{1}{R_{F2}}}$$

The pre-stage voltage gain:

$$A_{v(pre\text{-}stage)} = \frac{r_{eq}}{r_{eq} + R_g} = \frac{1.23 \times 10^3}{1.5 \times 10^3 + 1.23 \times 10^3} = 0.452$$

Where:

$$r_{eq} = \frac{1}{\frac{1}{R_{B1}} + \frac{1}{R_{F1}} + \frac{1}{r_{i1}}}$$

The pre-stage current gain:

$$A_{i(pre\text{-}stage)} = \frac{r_{eq}}{r_{eq} + r_{i1}} = \frac{10.71 \times 10^3}{10.71 \times 10^3 + 1.39 \times 10^3} = 0.886$$

Where:

$$r_{eq} = \frac{1}{\frac{1}{R_{B1}} + \frac{1}{R_{F1}}}$$

The product of all the current gains which is total current gain:

$$A_{i(total)} = (39.8)(43)(0.68)(0.886) = 1030$$

The product of all the voltage gains which is total voltage gain:

$$A_{v(total)} = (115)(28.35)(0.452) = 1474$$

The product of total current gain and total voltage gain which is total power gain:

$$A_{p(total)} = (1030)(1474) = 1,518,220$$

MODIFIED PARAMETERS FOR TRANSISTOR CASCADES:

You must have noted that the exact analysis procedure using the hybrid parameters is rather an involved process when more than one transistor is in a cascade. This is further complicated by the fact that the transistors can be connected in numerous ways, therefore, calling for the parameters to be adjusted for a different configuration. For instance, the two transistors in Figure 36. These two transistors can be connected in any of the following ways:

Common emitter to common emitter
Common emitter to common base
Common emitter to common collector
Common base to common emitter
Common base to common base
Common base to common collector
Common collector to common emitter
Common collector to common base
Common collector to common collector

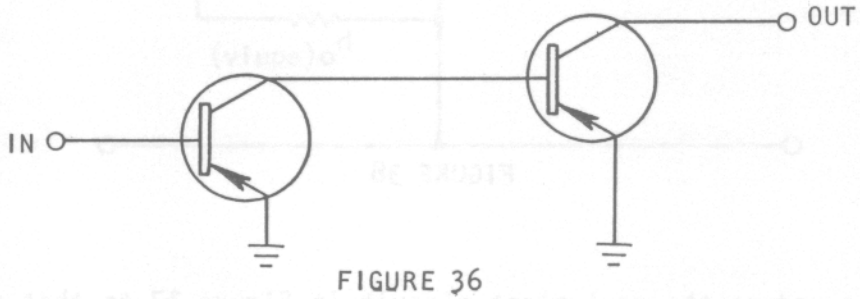


FIGURE 36

We have already established that if the hybrid equivalent circuit and parameters are used to represent the transistor, the equivalent circuit remains the same no matter what the configuration. Only the parameters are different when the configuration changes. Since this is the case, the equivalent circuit in Figure 37 is valid for any connection of the two transistors in Figure 36. This is assuming,

of course, that the parameters for the proper configuration are inserted in the equivalent circuit when the gains and impedance levels are solved.

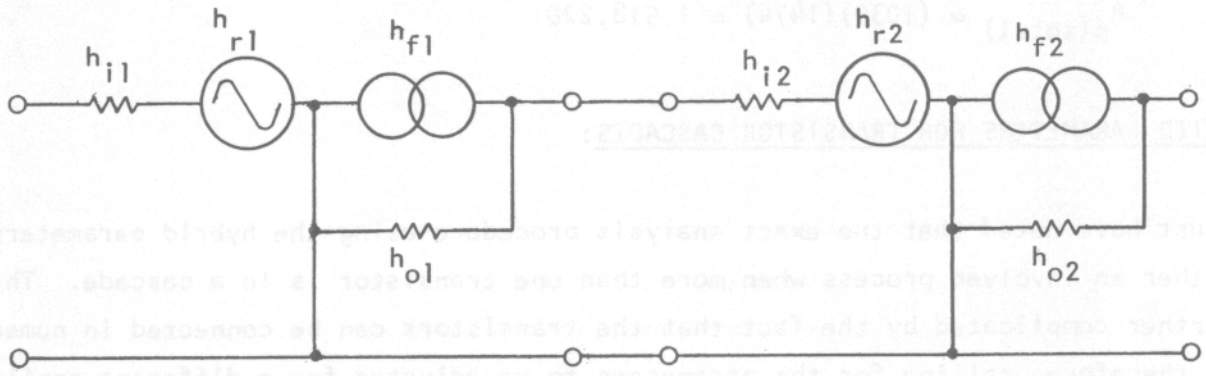


FIGURE 37

Since there are three possible configurations for each transistor, the transistor pairs as shown in Figure 36 have nine possible connections. This is the three possible configurations of the transistors, raised to the power of the number of transistors in the cascade. Therefore, three transistors in cascade have twenty-seven possible connections, etc.

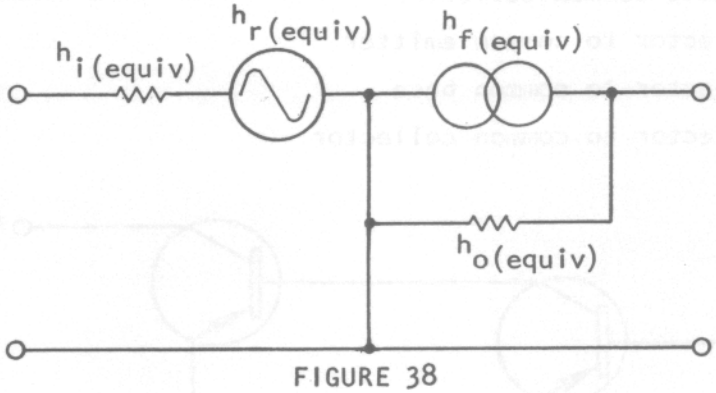


FIGURE 38

It is possible to reduce the equivalent circuit in Figure 37 to that shown in Figure 38. This is done by combining the parameters of the two transistor cascade into one equivalent circuit. The formulas listed in Figure 39 allow the parameters for the individual transistors in a transistor cascade to be modified so that one equivalent circuit can be used to represent both transistors. It should be evident that this should only be used when the total effect of the circuit on an input sig-

nal is the desired analysis result. If individual values within the circuit are of interest, reducing the transistors to one equivalent circuit is not advantageous. The parameters inserted into the formulas in Figure 39 must be for the configuration that the individual transistor is in. The subscript 1 indicates the parameters for the first stage, and the subscript 2 indicates the parameters for the second stage. The parameters should also, of course, be modified using the equations in Figures 30 and 31 if external or feedback components are present.

$$h_{i(equiv)} = h_{i_1} - \frac{h_{r_1} h_{f_1} h_{i_2}}{1 + h_{o_1} h_{i_2}}$$

$$h_{o(equiv)} = h_{o_2} - \frac{h_{r_2} h_{f_2} h_{o_1}}{1 + h_{o_1} h_{i_2}}$$

$$h_{f(equiv)} = \frac{-h_{f_1} h_{f_2}}{1 + h_{o_1} h_{i_2}}$$

$$h_{r(equiv)} = \frac{h_{r_1} h_{r_2}}{1 + h_{o_1} h_{i_2}}$$

FIGURE 39

The equivalent parameters can either be inserted directly into the hybrid formulas to solve for gain and impedance levels of the two transistor cascade, or if a third stage is present, can be lumped with the parameters of the third stage to further reduce the three-stage cascade to one equivalent circuit.

Let's review that a moment now. If there are more than one transistor in a cascade, the equivalent circuit can be reduced to one hybrid equivalent circuit by modifying the parameters by using the equations in Figure 39. When more than two transistors are in the cascade, two can be lumped into equivalent cparameters and the lumped parameters used in the equations in Figure 39 with the parameters of the third transistor. These parameters can also be modified to take into account external series shunt or feedback components using Figures 30 and 31, and inserted into the conventional hybrid equivalent circuit to solve for gain and impedance levels of the entire cascade.

TRANSDUCER GAIN:

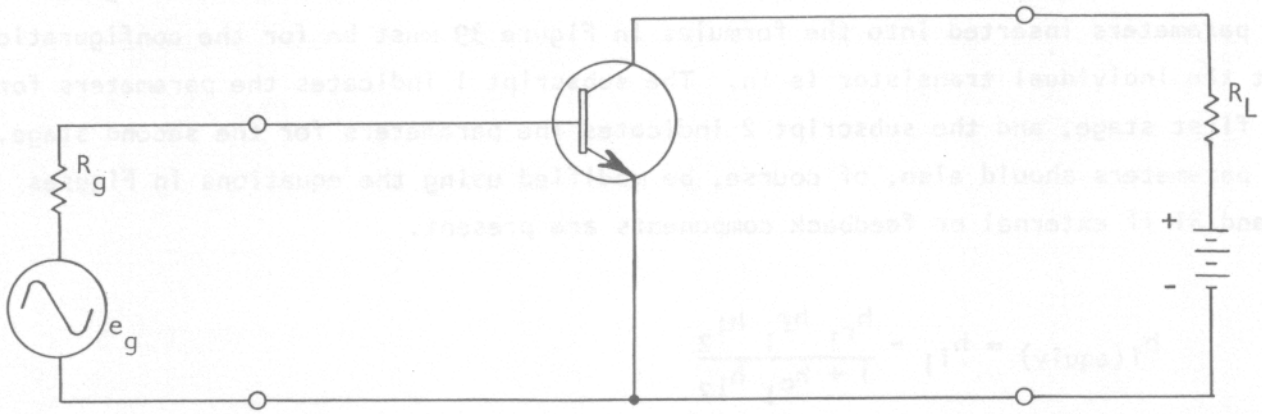


FIGURE 40

Consider the circuit configuration in Figure 40. As previously discussed, the following equations can be used to analyze this common emitter circuit:

$$\text{Current gain, } A_i = \frac{h_{fe}}{1 + h_{oe} R_L}$$

$$\text{Voltage gain, } A_v = \frac{h_{fe} R_L}{h_{ie} + \Delta h_e R_L}$$

$$\text{Input resistance, } r_i = \frac{h_{ie} + \Delta h_e R_L}{1 + h_{oe} R_L}$$

$$\text{Output resistance, } r_o = \frac{h_{ie} + R_g}{\Delta h_e + h_{oe} R_g}$$

When the transistor is considered as a transducer between the generator and a load, the gain is:

$$\text{Transducer gain} = \frac{\text{power out}}{\text{power available from generator}}$$

$$\text{Power available from the generator is} = \frac{e_g^2}{4R_g}$$

$$\text{Transducer gain (T.G.)} = \frac{\text{Power Out}}{\frac{e_g^2}{4R_g}}$$

$$T.G. = \frac{i_{out}^2 R_L}{\frac{e_g^2}{4R_g}}$$

$$T.G. = \frac{4\, i_{out}^2 R_L R_g}{e_g^2}$$

$$T.G. = \frac{4\, i_{out}^2 R_L R_g}{i_{in}^2 (R_g + r_i)^2}$$

$$\frac{i_{out}^2}{i_{in}^2} = A_i^2, \text{ so: } T.G. = \frac{4A_i^2 R_L R_g}{(R_g + r_i)^2}$$

and substituting in for A_i and r_i:

$$\text{Transducer gain (T.G.)} = \frac{4R_L R_g h_{fe}^2}{(R_g R_L h_{oe} + R_g + \Delta h_e R_L + h_{ie})^2}$$

INSERTION GAIN:

The insertion gain is the ratio of the gain with the transducer inserted to the gain without the transducer, or:

$$\text{Insertion gain} = \frac{\text{transducer gain}}{\text{gain without transducer}}$$

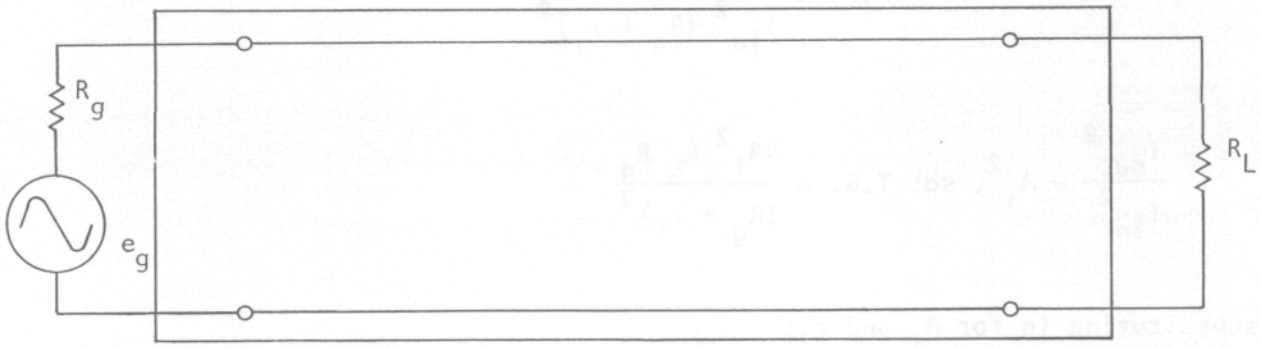
Output power without the transducer, as shown in Figure 41A, is:

$$P_{out} = \frac{e_{out}^2}{R_L} = \frac{\left(\frac{R_L e_g}{R_L + R_g}\right)^2}{R_L}$$

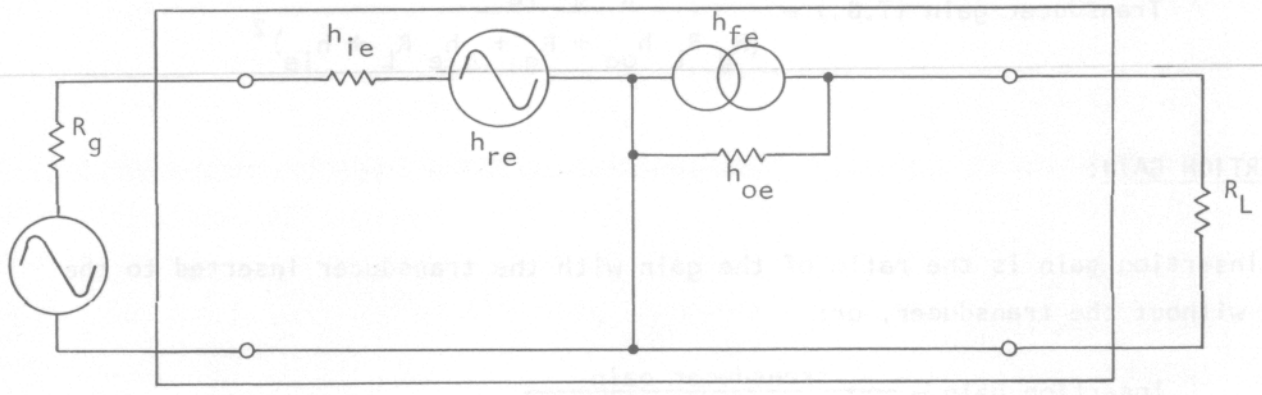
$$\text{Gain without transducer} = \frac{\text{power out}}{\text{power available from generator}} = \frac{\frac{\left(\frac{R_L e_g}{R_L + e_g}\right)^2}{R_L}}{\frac{e_g^2}{4R_g}} = \frac{4R_g \left(\frac{R_L e_g}{R_L + e_g}\right)^2}{R_L e_g^2}$$

$$\text{Insertion gain} = \frac{\text{transducer gain}}{\text{gain without transducer}}$$

$$\text{Insertion gain} = \frac{\dfrac{4R_L R_g h_{fe}^2}{(R_g R_L h_{oe} + R_g + \Delta h_e R_L + h_{ie})^2}}{\dfrac{4R_g \left(\dfrac{R_L e_g}{R_L + R_g}\right)}{R_L e_g^2}}$$



A



B

FIGURE 41

M. A. G. (Maximum Available Gain):

If a matched condition exists where the input generator resistance is equal to the transistor input resistance ($R_g = r_i$), and the load resistance is equal to the output resistance of the transistor ($R_L = r_o$), maximum power gain can be accomplished.

For M.A.G. to be accomplished, the following must be true:

$$R_g = r_i \qquad \text{and} \qquad R_L = r_o$$

Since r_i is effected by R_L, and r_o is effected by R_g, the simultaneous solution of R_L and R_g for a matched condition yields:

$$R_{L(matched)} = \sqrt{\frac{h_{ie}}{\Delta h_e \; h_{oe}}}$$

$$R_{g(matched)} = \sqrt{\frac{\Delta h_e \; h_{ie}}{h_{oe}}}$$

If these values are inserted, the maximum power gain will be accomplished and can be calculated in terms of the transistor parameters only, and becomes a figure of merit for the transistor:

$$\text{Maximum Available Gain (M.A.G.)} = \frac{h_{fe}^{\,2}}{\left[(h_{ie} \; h_{oe})^{1/2} + (\Delta h_e)^{1/2}\right]^2}$$

$$\text{M.A.G.} = \frac{h_{fe}^{\,2}}{\left(\sqrt{h_{ie} \; h_{oe}} + \sqrt{\Delta h_e}\right)^2}$$

Since the M.A.G. is in terms of the transistor parameters only, the M.A.G. of different transistors at a given operating point and frequency can be compared and used as an aid in selecting the right transistor for the right job. Operating frequency must be considered because M.A.G. will decrease as frequency increases. This will be discussed more thoroughly in the section on transistor high frequency characteristics and circuits. Equations will also be discussed that allow the calculation of M.A.G. at a given frequency.

APPROXIMATING INPUT RESISTANCE:

When the transistor is in a common base configuration, the input resistance is that signal resistance seen from the emitter to ground or the common point. Any external resistance in series with the signal will, of course, increase the input resistance, but the signal resistance offered by the transistor can be approximated by the formula:

$$r_{(input)} \approx \frac{26}{I_{E(ma)}} + \text{bulk resistance in the base}$$

The magnitude of bulk resistance in the base can vary from a few tenths of an ohm to as high as 30Ω when seen from the emitter. Typical bulk resistances are shown in Figure 42.

BASE BULK RESISTANCE AS SEEN FROM THE EMITTER

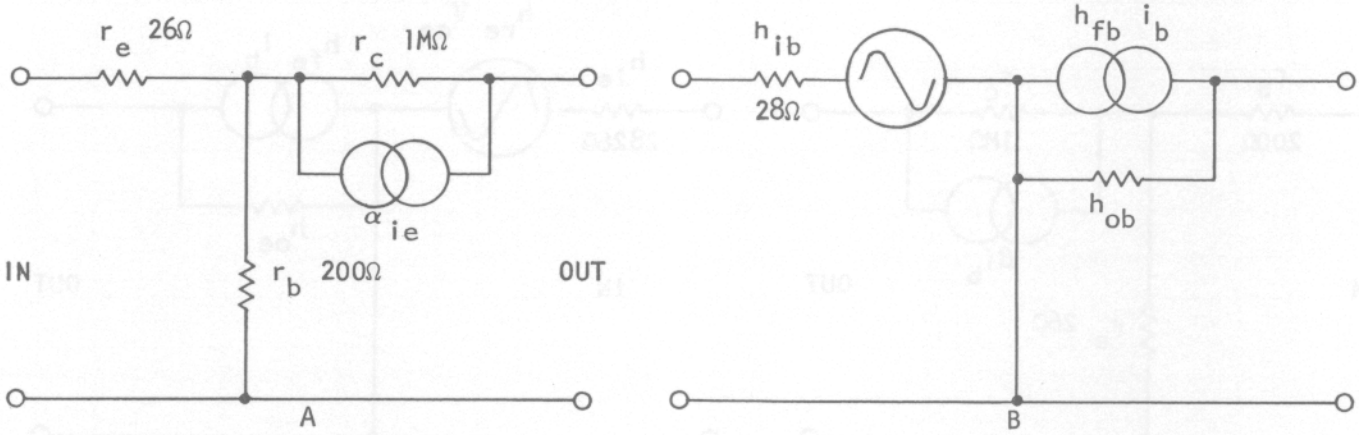
High Power Transistors	Typical High Performance Transistors
0.1Ω to 1Ω	1Ω to 5Ω

Some Special Purpose and Low Performance Types

5Ω to 30Ω

FIGURE 42

The T equivalent circuit represents the base bulk resistance with the parameter r_b as shown in Figure 43A. The base bulk resistance makes up part of h_{ib} in the hybrid equivalent circuit as shown in Figure 43B. The typical value of r_b shown in Figure 43A is 200Ω. It should be kept in mind that there is $(\beta + 1)$ more current flowing in the emitter as there is in r_b. Therefore, the effective portion of r_b as seen from the emitter is $\approx \frac{r_b}{(\beta + 1)}$ or, in the case of Figure 43A, with a β of 100, the effective r_b as seen from the emitter is 2Ω. This is a typical value for medium power, high performance transistors.



T equivalent of a common base amplifier

h equivalent of a common base amplifier

$\beta \doteq 100$

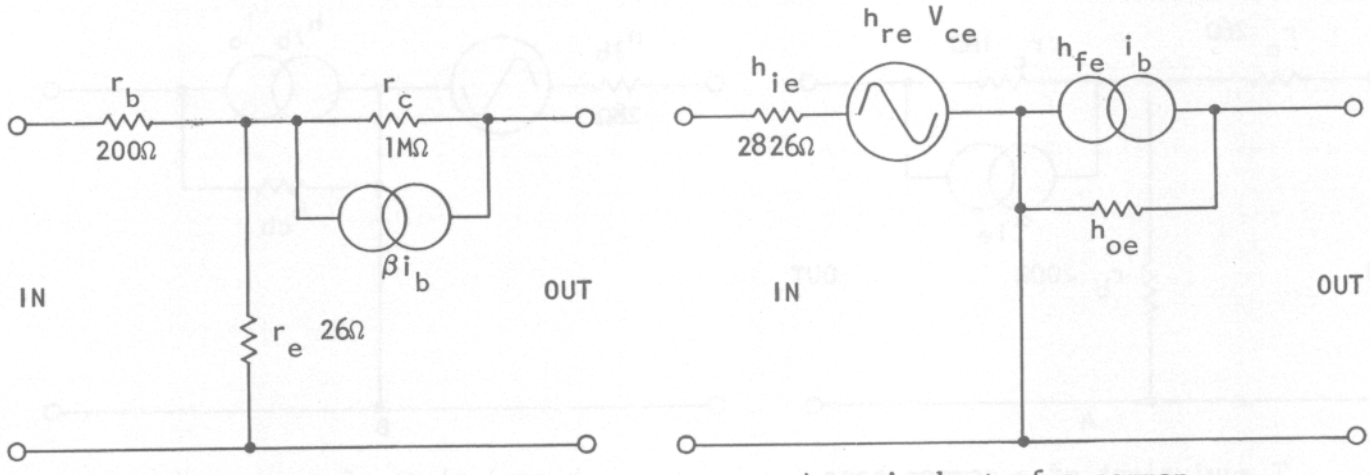
FIGURE 43

If we were to approximate the input resistance of the transistor in Figure 43, as $\approx r_e$, disregarding the bulk resistance would make little difference. Suppose, however, that the transistor were operating at a d-c emitter current of 5ma.

$$r_e \approx \frac{26}{I_{E(ma)}} \approx 5.2\Omega$$

Now, the bulk resistance is becoming a significant part of the input resistance and <u>cannot</u> be disregarded. This is especially so when we consider approximating the input resistance as seen from the base of the transistor.

Since there is approximately $(\beta + 1)$ times as much current flowing in the emitter as in the base lead of the transistor, any resistance in the emitter of the transistor is magnified by approximately $(\beta + 1)$ when seen from the base lead of the transistor. The input resistance can be approximated as $r_e (\beta + 1)$ plus any effective bulk resistance in the base. The base bulk resistance is shown by r_b in the T equivalent circuit of a common emitter amplifier as shown in Figure 44A. The value of r_e as seen from the base terminal is $\approx r_e (\beta + 1)$ or, in the case of the transistor in Figure 44A, 2626Ω. The input resistance is approximately 2626Ω plus the bulk resistance r_b of 200Ω, or 2826Ω. The bulk resistance is included in h_{ie} in the hybrid equivalent circuit.



T equivalent of a common emitter amplifier
$\beta = 100$

h equivalent of a common emitter amplifier

FIGURE 44

Notice that disregarding the bulk resistance, the input resistance in Figure 44A is only off by 200Ω in 2826Ω when the emitter d-c current is 1ma (i.e. $\frac{26}{1ma} = r_e = 26\Omega$); however, when the d-c emitter current is 5ma (i.e. $\frac{26}{5ma} = r_e = 5.2\Omega$), the product of r_e and $(\beta + 1)$ gives an approximate input resistance of 525Ω when the bulk resistance is disregarded, and an input resistance of 725Ω when the bulk resistance is included. In the latter case, the bulk resistance just cannot be disregarded when approximating the input resistance.

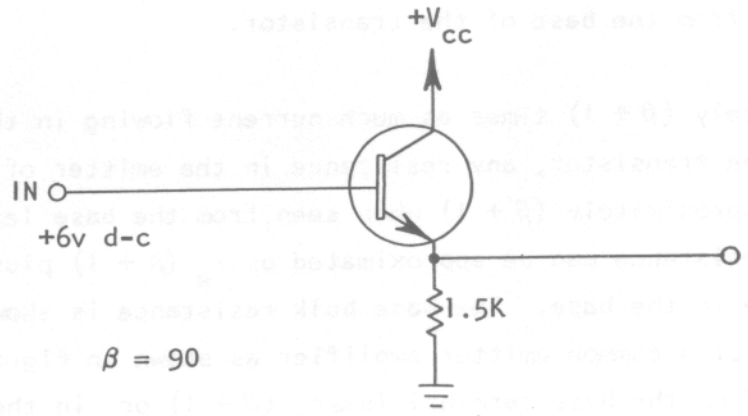


FIGURE 45

Let's approximate the input resistance of the common collector configuration in Figure 45. The base of the transistor is at +6v d-c with respect to ground. Disregarding any emitter-base drop on the transistor, we can say that the emitter is

approximately +6v d-c with respect to ground. The 6v must be dropped across the 1.5kΩ emitter resistor requiring approximately 4ma of d-c emitter current. Once we have established the approximate emitter current in Figure 45, we can approximate r_e.

$$r_e \approx \frac{26}{I_{E(ma)}} \approx \frac{26}{4ma} \approx 6.5\Omega$$

Assuming 2Ω of bulk resistance, the input resistance at the emitter is approximately 8.5Ω. This is increased by the factor $(\beta + 1)$ as seen at the base. Therefore, the transistor internal resistance as seen at the base is approximately:

$$(\beta + 1)\ 8.5\Omega \approx (91)\ (8.5\Omega) \approx 773.5\Omega$$

The 1.5k emitter resistor is also seen from the base and magnified by the factor $(\beta + 1)$. Therefore, the total input resistance is the sum of the internal and external effective resistances or:

$$773.5\Omega + (\beta + 1)\ 1.5k\Omega \approx 137.27k\Omega$$

If we had neglected the internal resistance of the transistor, the input resistance would have been approximated as:

$$(\beta + 1)\ 1.5k \approx 136.5k$$

From this, it can be seen that when the emitter circuit contains a resistor much greater than r_e, the input resistance can be approximated as the product of $(\beta + 1)$ and this external resistor in the emitter circuit.

To apply the approximate input resistance approach, consider the circuit in Figure 46. Let's approximate the input resistance of the common base transistors, Q1034, Q1044, Q1144, and Q1154. Notice the voltage readings at the base of Q1163, and at the collector of Q1144 indicate that 3.2v is being dropped across R1142. This requires a collector current in Q1144 of approximately 10ma. A little investigation will show that the same is true of Q1154.

$$r_e \approx \frac{26}{I_{E(ma)}} \approx \frac{26}{10ma} \approx 2.6\Omega \quad \text{for both Q1144 and Q1154}$$

The bases of these transistors are placed at small signal ground by capacitor C1153; therefore, the input resistance at the emitters is approximated by adding 2Ω to r_e.

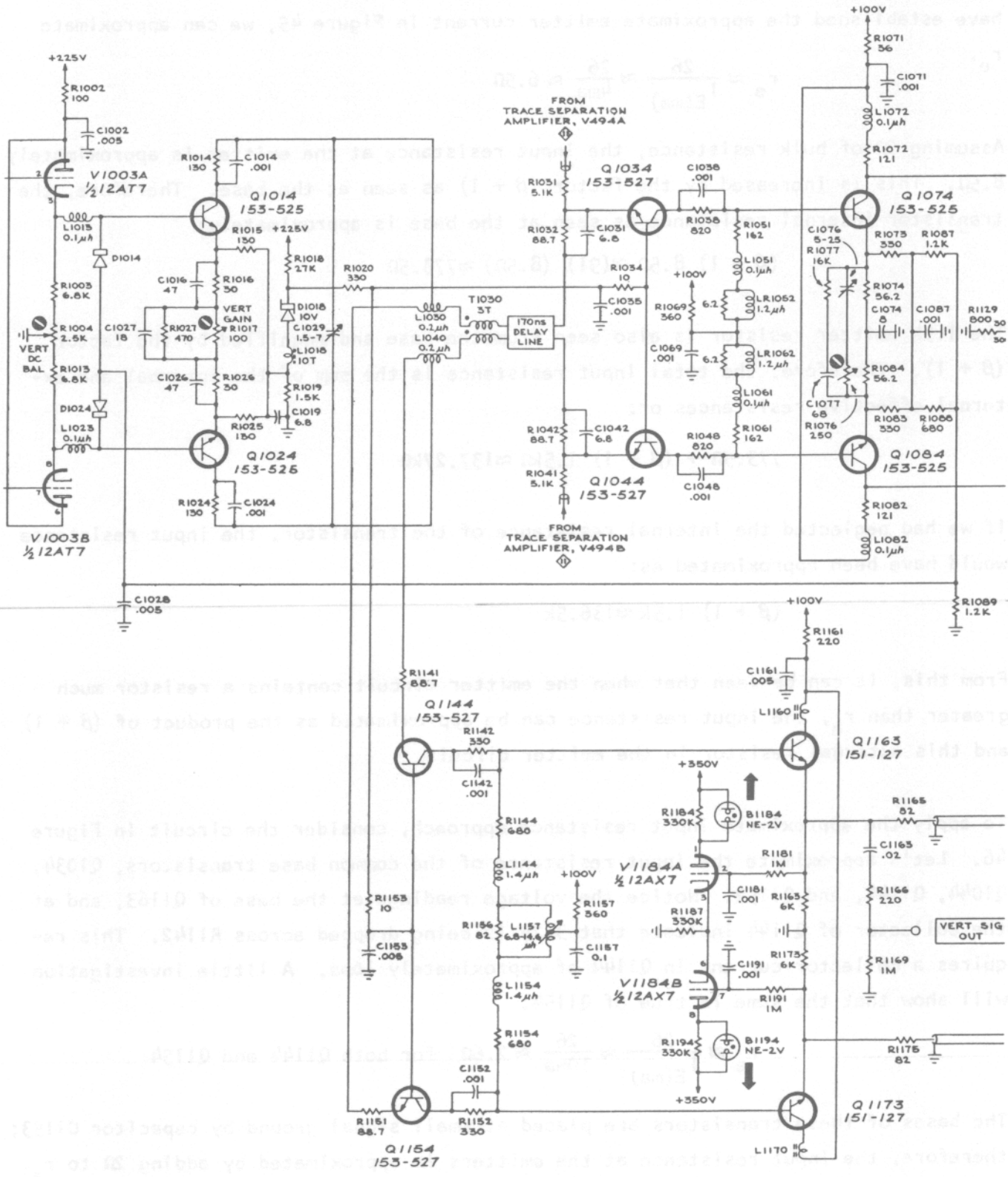

+225V
R1002 100
C1002 .005
V1003A ½12AT7
L1015 0.1μh
D1014
R1003 6.8K
R1004 2.5K
VERT DC BAL
R1013 6.8K
D1024
L1023 0.1μh
V10038 ½12AT7
C1028 .005
R1014 130
C1014 .001
Q1014 153-525
R1015 130
+225V
R1018 27K
R1016 30
C1016 47
VERT GAIN R1017 100
C1027 18
R1027 470
C1026 47
R1026 30
R1025 150
R1024 130
C1024 .001
Q1024 153-526
C1019 6.8
D1018 10V
C1029 1.5-7
L1018 10T
R1020 330
T1030 3T
L1030 0.2μh
L1040 0.2μh
170ns DELAY LINE
FROM TRACE SEPARATION AMPLIFIER, V494A
FROM TRACE SEPARATION AMPLIFIER, V494B
Q1034 153-527
R1031 5.1K
R1032 88.7
C1031 6.8
C1038 .001
R1038 820
R1034 10
C1035 .001
R1051 162
L1051 0.1μh
LR1052 1.2μh
R1069 360
6.2
C1069 .001
LR1062 1.2μh
L1061 0.1μh
R1061 162
Q1044 153-527
R1042 88.7
C1042 6.8
R1048 820
C1048 .001
R1041 5.1K
+100V
R1071 56
C1071 .001
L1072 0.1μh
R1072 121
Q1074 153-525
C1076 5-25
R1077 16K
R1073 330
R1087 1.2K
R1074 56.2
C1074 8
C1087 .001
R1129 800 30 30
R1084 56.2
C1077 68
R1076 250
R1083 330
R1088 680
Q1084 153-525
R1082 121
L1082 0.1μh
R1089 1.2K
R1161 220
C1161 .005
L1160
Q1163 151-127
R1141 88.7
Q1144 153-527
R1142 330
C1142 .001
+350V
R1184 330K
B1184 NE-2V
R1165 82
C1163 .02
R1144 680
L1144 1.4μh
V1184A ½12AX7
R1181 1M
C1181 .001
R1163 6K
R1166 220
VERT SIG OUT
R1153 10
C1153 .005
R1156 82
L1157 6.8-14.6 μh
R1157 560
C1157 0.1
R1187 330K
R1173 6K
R1169 1M
C1191 .001
V1184B ½12AX7
R1191 1M
L1154 1.4μh
R1154 680
R1194 330K
B1194 NE-2V
R1175 82
C1152 .001
R1151 88.7
R1152 330
Q1154 153-527
Q1173 151-127
L1170

FIGURE 46

The 2Ω is the assumed bulk resistance in the base of these high performance, medium power transistors. The input resistance as seen at the emitters of Q1144 and Q1154 is approximately 4.6Ω. Notice L1030 and L1040 see resistors R1141 and R1151 in series with the transistors input resistance. These coils see 88.7Ω in series with the approximated input resistance of 4.6Ω for a total of 93.3Ω. L1030 and L1040 are 186Ω coils, 93Ω per side. The series resistors R1141 and R1151 and the input resistances of the transistors must terminate the left end of the coils, while the 170nsec transmission line and its terminations terminate the right end of coils L1030 and L1040. (The 170nsec delay line is 93Ω per side.) The sum of 88.7Ω and our approximated input resistance of 4.6Ω is a total of 93.3Ω, which indicates that our approximations are very close.

Inspection of the voltage measurements on Q1034 and Q1044 will indicate that they too have emitter currents of approximately 10ma, which gives an input resistance of approximately 4.6Ω and in series with 88.7Ω, properly terminate the 170nsec delay line. We will investigate this circuit further later in this volume. It is a portion of the vertical amplifier in the Tektronix Type 547 oscilloscope.

Consider the circuit configuration in Figure 47. The resistor R_F is supplying both a-c and d-c feedback. A portion of the output voltage is fed back to the input. If we assume that the a-c feedback is 180° out of phase, it should increase the input resistance. If we assume that R_F is an open circuit and calculate the voltage gain with R_F open circuited, we can then approximate the input resistance with the equation:

$$r_{i(feedback)} \approx r_i \ (1 + K A_v)$$

Where:

$r_{i(feedback)}$ = dynamic input resistance with feedback

r_i = dynamic input resistance without feedback

K = feedback factor

A_v = absolute value of voltage gain without feedback

For the circuit configuration in Figure 47, R_F and R_B are a voltage divider, and the feedback factor can be found by:

$$K = \frac{R_B}{R_B + R_F}$$

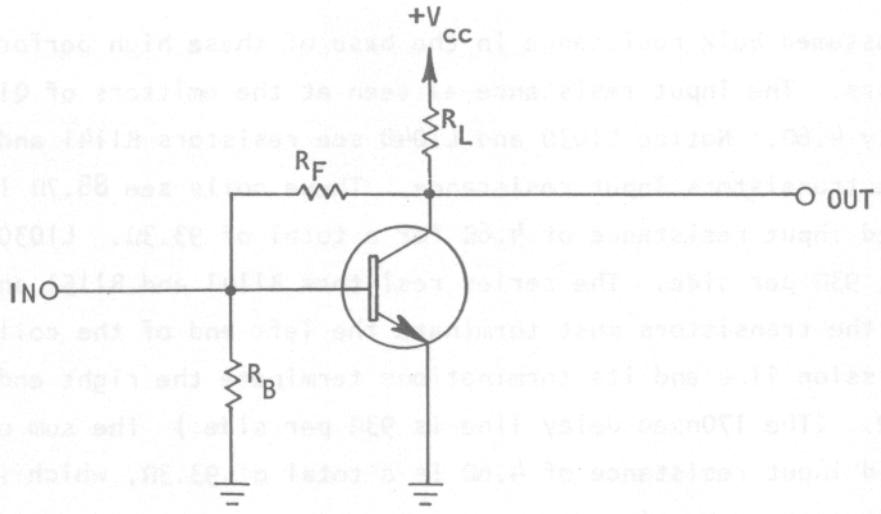


FIGURE 47

The formula:

$$r_{i(feedback)} \approx r_i \ (1 + K A_v)$$

is valid where the feedback is negative such as in Figure 47. When the feedback is positive, the input resistance is reduced and can be approximated by the expression:

$$r_{i(feedback)} \approx r_i \ (1 - K A_v)$$

and the symbols have the same meaning as before.

APPROXIMATING VOLTAGE GAIN:

If the assumption is made that collector and emitter current are nearly equal (assuming $\alpha = 1$, and $\beta = \infty$), then the same current is flowing through the collector load resistor as is flowing through any internal and external resistance in the emitter. Consider the transistor in Figure 48. With an emitter current of 9ma, the value of:

$$r_e \approx \frac{26}{I_{E(ma)}} \approx 2.9\Omega$$

Assuming the transistor is a medium power, high performance transistor, add $\approx 2\Omega$ for base bulk resistance, and the approximate emitter resistance is slightly less than 5Ω. Assuming the same signal current flows through this dynamic emitter resistance as flows through the collector load, the voltages will be proportional to the resistances involved. With no external resistance in the emitter signal path, the input voltage is distributed across the dynamic emitter resistance just approximated. Since we have assumed the same signal current through the dynamic emitter

resistor and the collector load resistance, the ratio of the collector load resistance to the dynamic emitter resistance is an approximation of the voltage gain of the amplifier. In the case of the transistor in Figure 48, the collector load is the parallel resistance of 1K R_L, and the 1K load circuit, or 500Ω. We approximated the dynamic resistance in the emitter as:

$$2.9\Omega\ (r_e) + 2\Omega\ \text{(base bulk resistance)} \approx 4.9\Omega$$

The approximate voltage gain is:

$$A_v \approx \frac{R_L\ (a\text{-}c)}{r_e + R_{bulk}} \approx \frac{500\Omega}{4.9\Omega} \approx 102$$

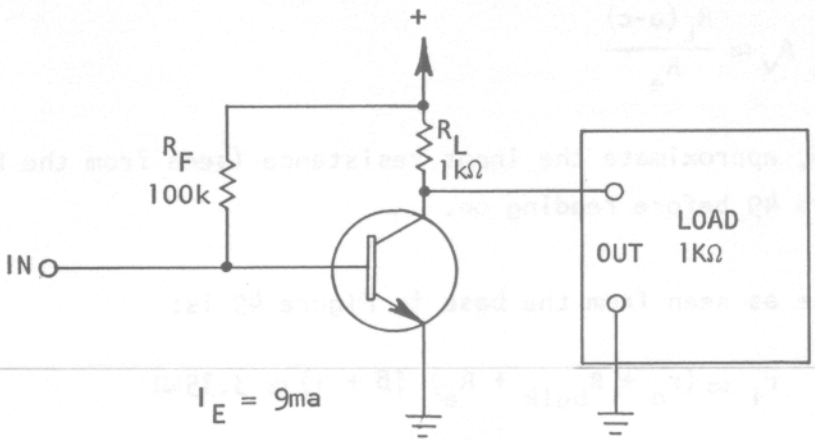


FIGURE 48

Now consider the circuit in Figure 49. With the same emitter current as the transistor in Figure 48, the dynamic internal resistor is the same. The external resistor R_e must also be taken into account, however, and the approximation for voltage gain becomes:

$$A_v \approx \frac{R_L\ (a\text{-}c)}{r_e + R_{bulk} + R_e}$$

and for the configuration in Figure 49:

$$A_v \approx \frac{500\Omega}{2.9\Omega + 2\Omega + 50\Omega} \approx 9.1$$

Completely neglecting the internal dynamic resistance, the voltage gain of the configuration in Figure 48 is:

$$A_v \approx \frac{R_L\ (a\text{-}c)}{R_e} \approx \frac{500}{50} \approx 10$$

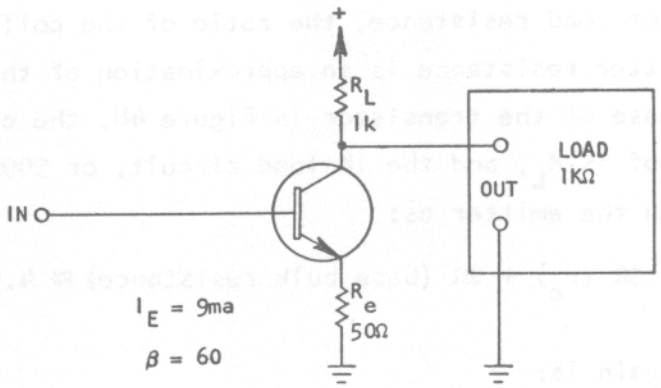


FIGURE 49

We might say that when R_e is much greater than r_e, the voltage gain can be approximated by:

$$A_v \approx \frac{R_L (a\text{-}c)}{R_e}$$

For a bit of review, approximate the input resistance (seen from the base) of the transistor in Figure 49 before reading on.

The input resistance as seen from the base in Figure 49 is:

$$r_i \approx (r_e + R_{bulk} + R_e)\ (\beta + 1) \approx 3.35k\Omega$$

Consider the configuration in Figure 47. Here negative feedback is also reducing the voltage gain of the amplifier, and the voltage gain with feedback can be approximated by first assuming that R_F is open circuited and determining the voltage gain without feedback and applying this to the equation:

$$A_{v(feedback)} \approx \frac{A_v}{1 + A_v K}$$

Where: $A_{v(feedback)}$ = voltage gain with feedback

A_v = absolute value of voltage gain without feedback

K = feedback factor

In Figure 47, the feedback factor can be found by solving the voltage divider of R_F and R_B:

$$K = \frac{R_B}{R_F + R_B}$$

If the feedback is positive, the voltage gain can be approximated by the equation:

$$A_{v(feedback)} \approx \frac{A_v}{1 - A_v K}$$

and the symbols have the same meaning as before:

EXAMPLE OF ESTIMATING INPUT RESISTANCE AND VOLTAGE GAIN:

Figure 50 is the A signal out amplifier in the Tektronix Type M, four-trace pre-amplifier. Among other things, it provides a triggering signal to allow a reference when viewing multiple trace displays on a Tektronix oscilloscope that accepts letter series plug-in pre-amplifiers.

We might start an approximate analysis by approximating the d-c emitter currents of the two transistors. Since voltage readings are given, we will use these to facilitage the analysis.

Q5344 has 0.9v dropped across its collector load resistor, R5351. If we disregard base current from Q5354, we can approximate the emitter current of Q5344 as:

$$\frac{0.9v}{1.5k} = 0.6ma$$

We will assume that the emitter current of Q5344 is approximately 0.6ma. The emitter resistor of Q5354 has 0.6v dropped across it, and we can approximate the emitter current by:

$$\frac{0.6v}{150\Omega} \approx 4ma$$

We will assume the emitter current of Q5354 is approximately 4ma. Knowing these values, we can approximate r_e for both transistors.

$$r_e(Q5344) \approx \frac{26}{I_{E(ma)}} \approx \frac{26}{0.6ma} \approx 43\Omega$$

$$r_e(Q5354) \approx \frac{26}{I_{E(ma)}} \approx \frac{26}{4ma} \approx 6.5\Omega$$

The effective external signal resistance in the emitter of Q5344 is the parallel resistance of R5352 and the series leg of R5355 and R5354. This is illustrated in Figure 51. The effective signal resistance in the emitter is 115Ω (R_e). This re-

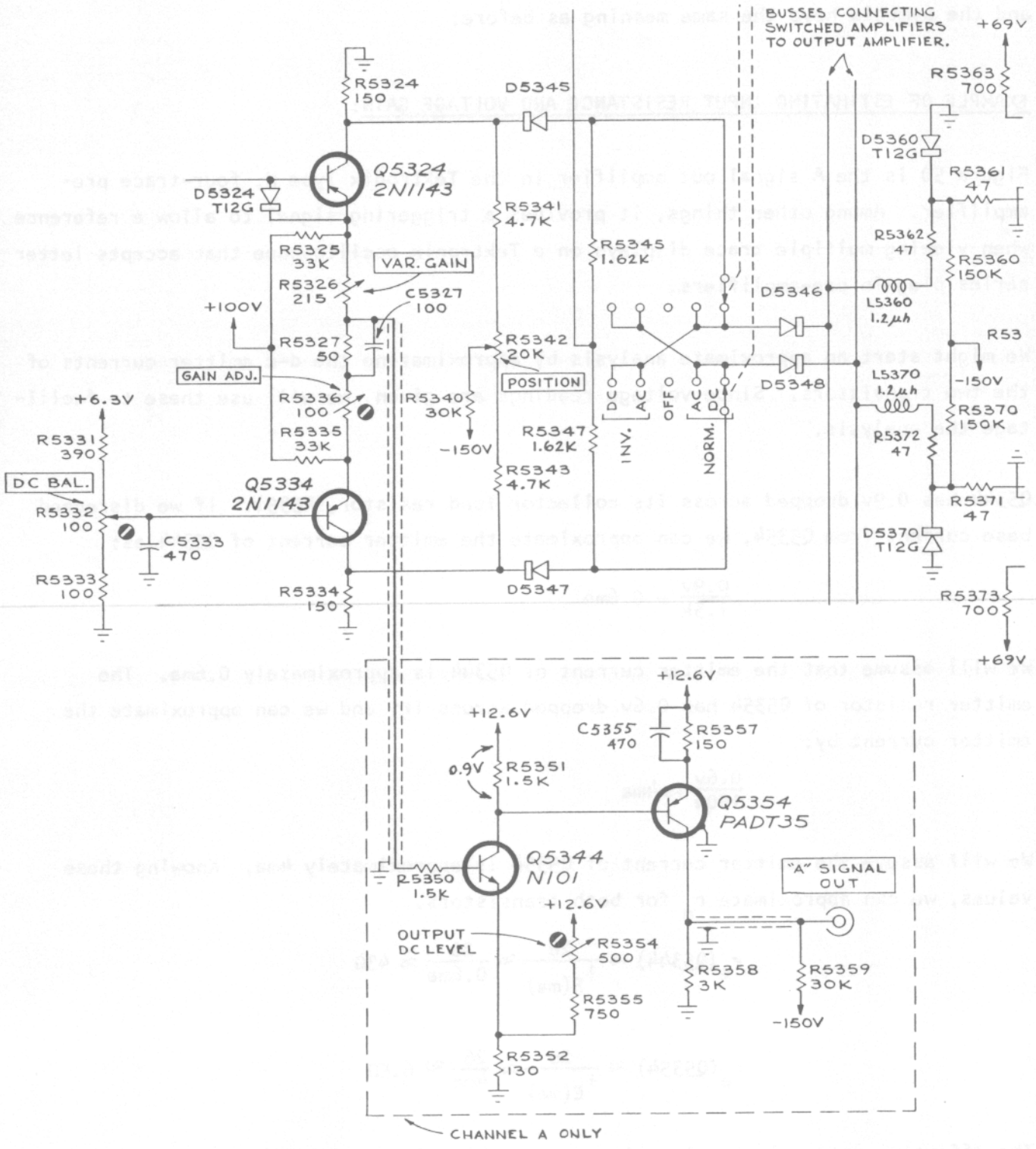

BUSSES CONNECTING SWITCHED AMPLIFIERS TO OUTPUT AMPLIFIER.
+69V
R5363 700
D5360 T12G
R5361 47
R5362 47
R5360 150K
D5346
L5360 1.2μh
R53
-150V
L5370 1.2μh
R5370 150K
R5372 47
R5371 47
D5370 T12G
R5373 700
+69V
R5324 150
D5345
Q5324 2N1143
D5324 T12G
R5341 4.7K
R5345 1.62K
R5325 33K
VAR. GAIN
R5326 215
C5327 100
+100V
R5327 50
R5342 20K
POSITION
GAIN ADJ.
R5336 100
R5340 30K
-150V
R5347 1.62K
R5343 4.7K
R5335 33K
+6.3V
R5331 390
DC BAL.
R5332 100
C5333 470
Q5334 2N1143
R5333 100
R5334 150
D5347
D5348
DC
AC
OFF
AC
DC
INV.
NORM.
+12.6V
C5355 470
R5357 150
+12.6V
0.9V
R5351 1.5K
Q5354 PADT35
Q5344 N101
R5350 1.5K
"A" SIGNAL OUT
+12.6V
OUTPUT DC LEVEL
R5354 500
R5355 750
R5352 130
R5358 3K
R5359 30K
-150V
CHANNEL A ONLY

FIGURE 50

sistor R5354 is assumed to be at design center (the middle of its range, 250Ω) and returned to ground (the +12.6v d-c supply is at a-c signal ground potential).

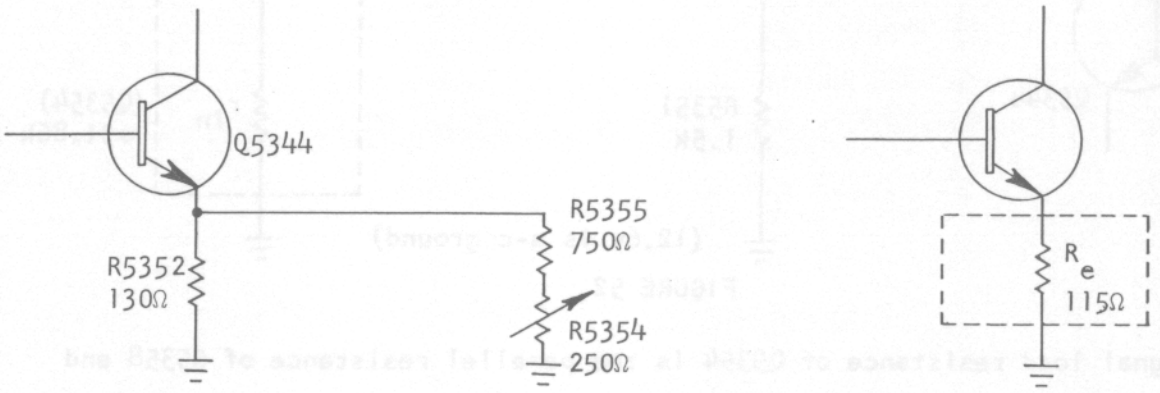


FIGURE 51

To approximate the input resistance at the base of Q5344, we can use:

$$r_{in} \approx (r_e + r_{bulk} + R_e)\ (\beta + 1)$$

Typical β of an N-101 at 0.6ma is 70, therefore:

$$r_{in}(Q5344) \approx (43\Omega + 2\Omega + 115\Omega)\ (70 + 1)$$

$$r_{in}(Q5344) \approx 11.36k\Omega$$

The same approximate expression can be used for Q5354. C5355 can be disregarded at the low frequencies; therefore, R_e is 150Ω. Typical β of a PADT-35 at 4ma is 200, therefore:

$$r_{in}(Q5354) \approx (6.5\Omega + 2\Omega + 150\Omega)\ (200 + 1)$$

$$r_{in}(Q5354) \approx 31.86k\Omega$$

The voltage gain of the two stages can be approximated with the expressions:

$$A_v \approx \frac{R_L(a\text{-}c)}{r_e + r_{bulk} + R_e}$$

The a-c load resistance of Q5344 is the parallel resistance of the resistor R5351, and the input resistance of Q5354, as shown in Figure 52. The parallel resistance is approximately 1.43k, therefore:

$$A_v(Q5344) \approx \frac{1.43k}{43\Omega + 2\Omega + 115\Omega} \approx 8.95$$

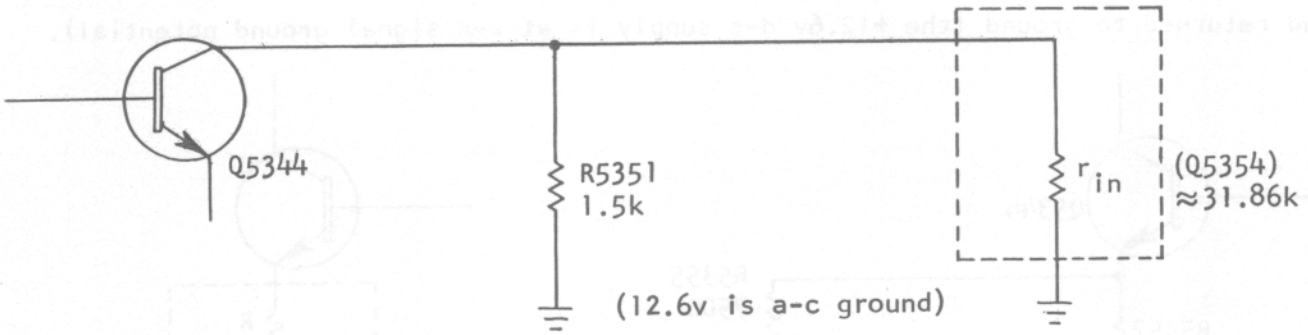


FIGURE 52

The a-c signal load resistance of Q5354 is the parallel resistance of R5358 and R5359, as shown in Figure 53; therefore:

$$A_v(Q5354) \approx \frac{2.73k}{6.5\Omega + 2\Omega + 150\Omega} \approx 17.2$$

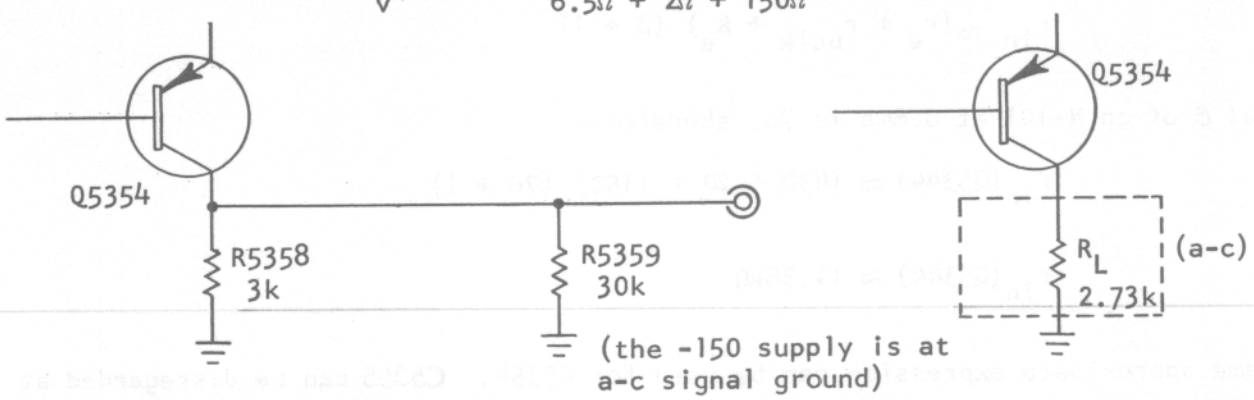


FIGURE 53

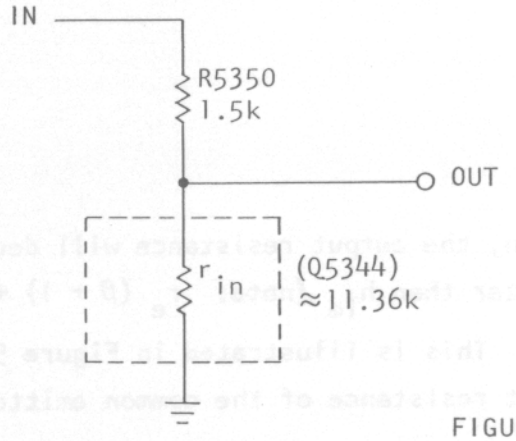
There is one more gain that cannot be neglected. Resistor R5350 drops some of the signal voltage before it reaches the input of Q5344. The input resistance Q5344 and the resistor R5350 can be treated as a simple voltage divider, as shown in Figure 54. Therefore, the pre-stage voltage gain is:

$$A_{v(pre\text{-}stage)} = \frac{r_{in}(Q5344)}{r_{in}(Q5344) + R5350} = \frac{11.36k}{12.86k} = 0.884$$

The product of these three gains is the total gain of the amplifier:

$$A_{v(total)} \approx A_{v(pre\text{-}stage)} \times A_v(Q5344) \times A_v(Q5354)$$

$$A_{v(total)} \approx (0.884)\ (8.95)\ (17.2) \approx 136$$



$$e_{out} = \frac{r_{in}\, e_{in}}{r_{in} + R5350}$$

$$\frac{e_{out}}{e_{in}} = A_v = \frac{r_{in}}{r_{in} + R5350}$$

FIGURE 54

Now, from the waveforms given in Figure 50, let's check our work. The waveform shown at the input to the amplifier shows a square wave 1.2 major divisions in amplitude with a measurement sensitivity of 0.05v/cm (major divisions). This is an input signal of 0.06v. The waveform at the output is a square wave of 1.6 major divisions in amplitude with a measurement sensitivity of 5v/cm (major division). This is an output voltage of 8v.

The voltage gain is:

$$A_{v(total)} = \frac{e_{out}}{e_{in}} = \frac{8v}{0.06v} = 133.3$$

Our approximations set the voltage gain at 136, plenty close enough to note abnormalties in the amplifier when making measurements.

APPROXIMATING OUTPUT RESISTANCE:

We have formulated an exact expression for output resistance of a transistor as:

$$r_o = \frac{h_i + R_g}{\Delta^h + h_o R_g}$$

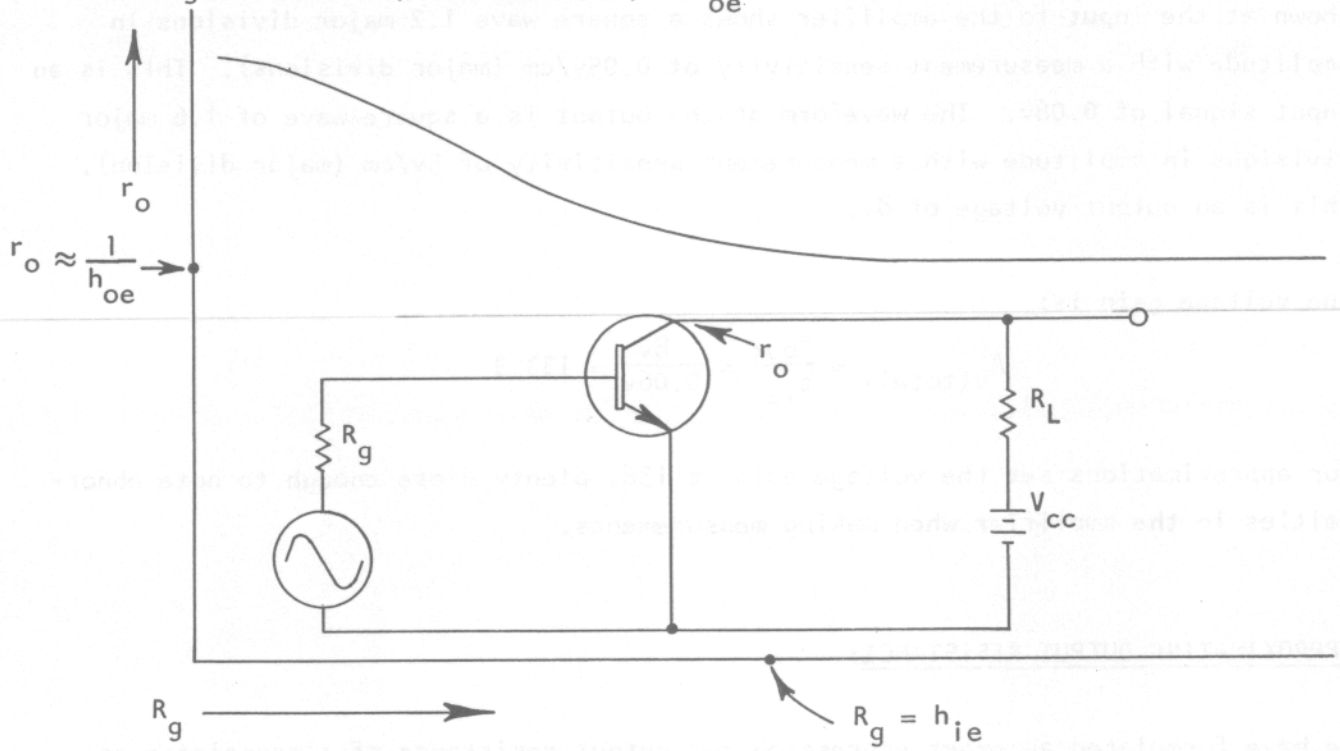
Where: $\Delta^h = h_i\, h_o - h_f\, h_r$, and R_g = resistance of the driving generator

This equation is valid for any configuration if the parameters for that configuration are inserted.

COMMON EMITTER:

Considering the common emitter configuration, the output resistance will decrease when R_g is varied from zero to a value greater than h_{ie} (note: $r_e (\beta + 1) + r_b$ when dealing with the T equivalent circuit) This is illustrated in Figure 55. When R_g becomes greater than h_{ie}, the output resistance of the common emitter stage can be approximated as:

$$R_g \gg h_{ie}: \quad r_{o(\text{common emitter})} \approx \frac{1}{h_{oe}} \text{ or } r_d \text{ or } r_c (1 - \alpha)$$



COMMON EMITTER STAGE

FIGURE 55

COMMON BASE:

Note in Figure 56 that the output resistance of the common base stage increases with an increase in R_g. Below $R_g = h_{ib}$, the output resistance can be below 100k.

When R_g is greater than $r_e + r_b$, the output resistance can be an order of magnitude

larger, perhaps a megohm. If R_g is greater than $r_e + r_b$, the output resistance can be approximated as:

$$R_g \gg r_b + r_e: \quad r_{o(\text{common base})} \approx \frac{1}{h_{ob}} \approx r_c$$

One might interpolate at the lower values of R_g if the desired answer need not be too close.

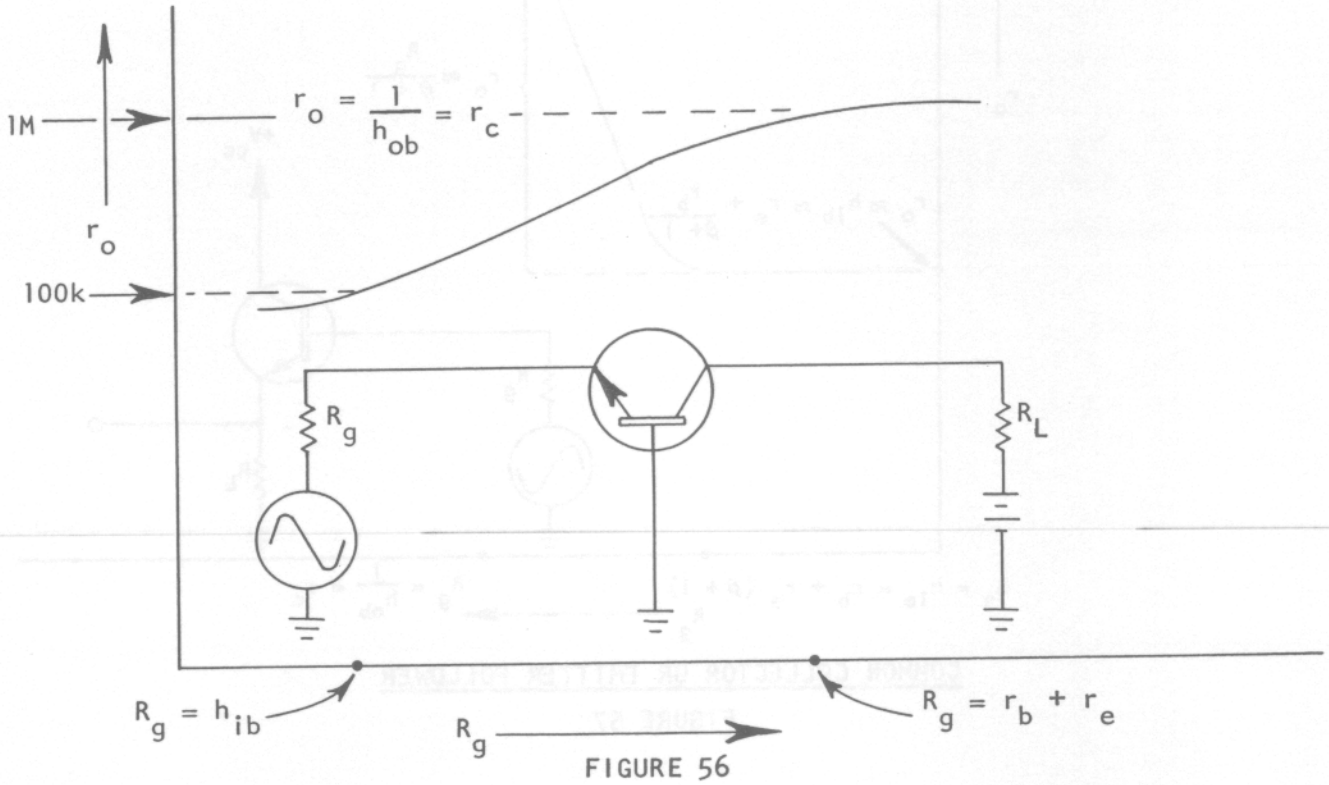


FIGURE 56

COMMON COLLECTOR OR EMITTER FOLLOWER:

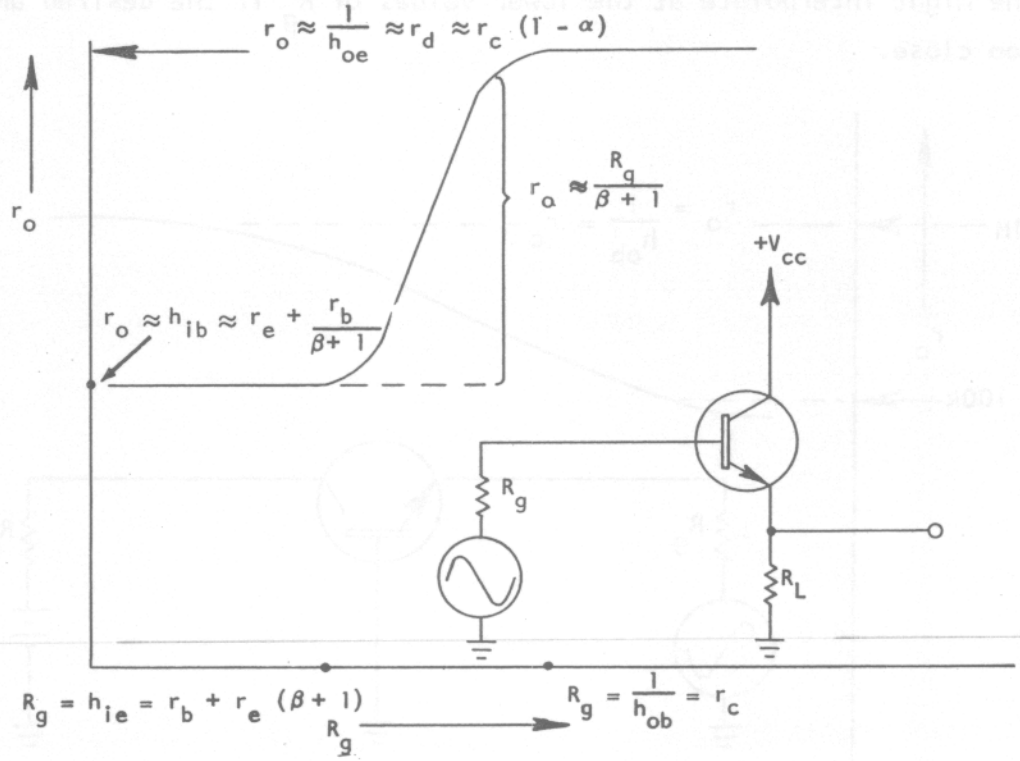
Since any resistance in the base lead of the transistor is seen from the emitter, modified by the factor $(1 - \alpha)$ (this is the same as dividing by $[\beta + 1]$), the value of R_g will have a large effect on the output resistance of the emitter follower. When the input generator resistance is less than h_{ie} (note: $r_b + r_e [\beta + 1]$ when using the T equivalent circuit), the output resistance is approximately equal to h_{ib} (note: $r_e + r_b [1 - \alpha]$ when using the T equivalent circuit). When R_g is greater than h_{ie}, the output resistance is:

$$R_g \gg h_{ie} \text{ but } < \frac{1}{h_{ob}}: \quad r_{o(\text{common collector})} \approx \frac{R_g}{\beta + 1}$$

When R_g becomes greater than $\frac{1}{h_{ob}}$ (note: r_c for T equivalent), the output resistance becomes:

$$R_g \gg \frac{1}{h_{ob}} \text{ or } \gg r_c: \quad r_{o(\text{common collector})} \quad \frac{1}{h_{oe}} \approx r_d \approx r_c (1 - \alpha)$$

This is illustrated in Figure 57.



COMMON COLLECTOR OR EMITTER FOLLOWER

FIGURE 57

APPROXIMATING OUTPUT RESISTANCE WHEN THERE IS FEEDBACK:

Consider the configuration in Figure 58. This is referred to as current feedback. This is because the signal current through R_{fb} is being sampled to develop a feedback voltage. When this is the case, the output resistance can be found by:

$$r_{o(\text{feedback})} = r_o + R_{fb} (1 + A_v)$$

Where: $r_{o(\text{feedback})}$ = output resistance with negative feedback

r_o = output resistance without feedback

R_{fb} = current sampling resistor across which the feedback is developed.

A_v = voltage gain without feedback

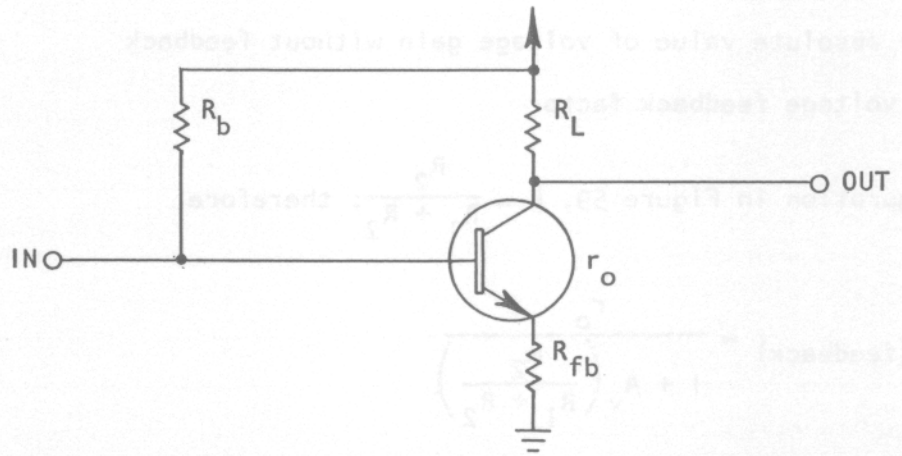


FIGURE 58

Of course, r_o and A_v without feedback can be approximated and inserted in these equations making them approximate expressions. When the output voltage is not directly sampled to obtain feedback, chances are the feedback is current feedback.

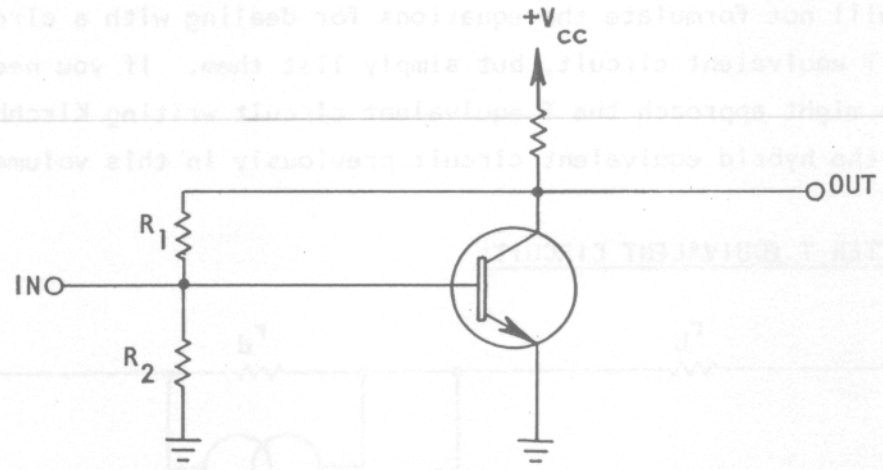


FIGURE 59

Now consider the configuration in Figure 59. The output voltage is directly sampled for feedback, and this is referred to as voltage feedback. An increase in the output impedance was evident with negative current feedback; however, we will find a decrease in output resistance with negative voltage feedback. With negative voltage feedback such as shown in Figure 59, the output resistance is:

$$r_{o(feedback)} = \frac{r_o}{1 + A_v K}$$

Where: $r_{o(feedback)}$ = output resistance with negative voltage feedback

r_o = output resistance without feedback

A_v = absolute value of voltage gain without feedback

K = voltage feedback factor

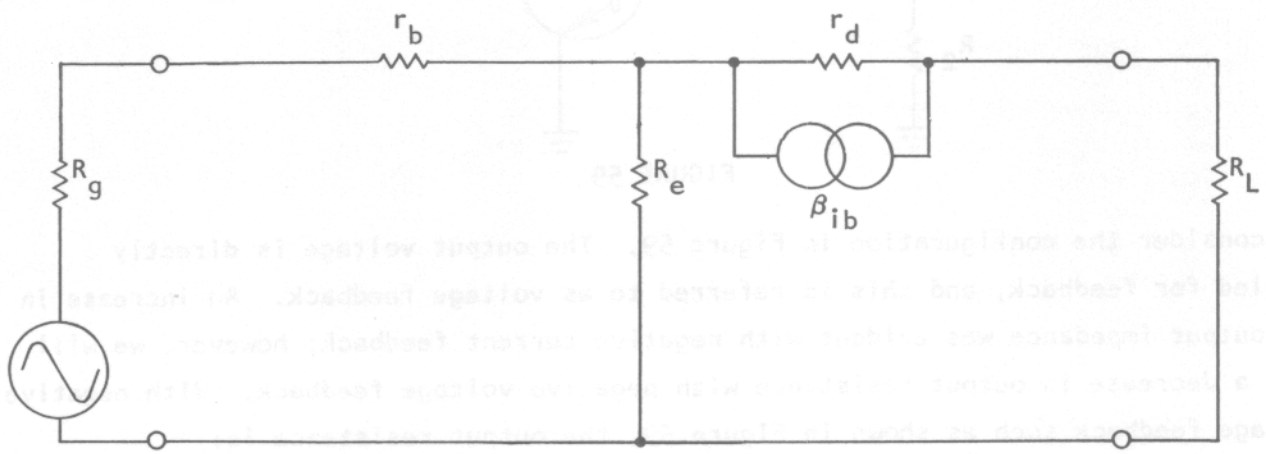
For the configuration in Figure 59, $K = \frac{R_2}{R_1 + R_2}$; therefore,

$$r_{o(feedback)} = \frac{r_o}{1 + A_v\left(\frac{R_2}{R_1 + R_2}\right)}$$

T EQUIVALENT CIRCUIT EQUATIONS:

We have formulated the gain and resistance equations for the hybrid equivalent circuit when it is used in place of the transistor for analysis and design purposes. Therefore, we will not formulate the equations for dealing with a circuit configuration with the T equivalent circuit, but simply list them. If you need further validation, you might approach the T equivalent circuit writing Kirchhoff equations as we did with the hybrid equivalent circuit previously in this volume.

THE COMMON EMITTER T EQUIVALENT CIRCUIT:



NOTE: $r_d = r_c\ (1 - \alpha)$

FIGURE 60

$$\text{Voltage gain } A_v = \frac{(\beta r_d - r_e)\, R_L}{r_e\,(r_b + \beta r_d) + (r_e + r_b)\,(r_d + R_L)}$$

$$\text{Current gain } A_i = \frac{\beta r_d - r_e}{r_e + r_d + R_L}$$

$$\text{Input resistance } r_i = \frac{r_e\,(r_b + \beta r_d) + (r_e + r_b)\,(r_d + R_L)}{r_e + r_d + R_L}$$

$$\text{Output resistance } r_o = \frac{r_d\,(R_g + r_b + r_e) + r_e\,(R_g + r_b + \beta r_d)}{R_g + r_b + r_e}$$

THE COMMON BASE T EQUIVALENT CIRCUIT:

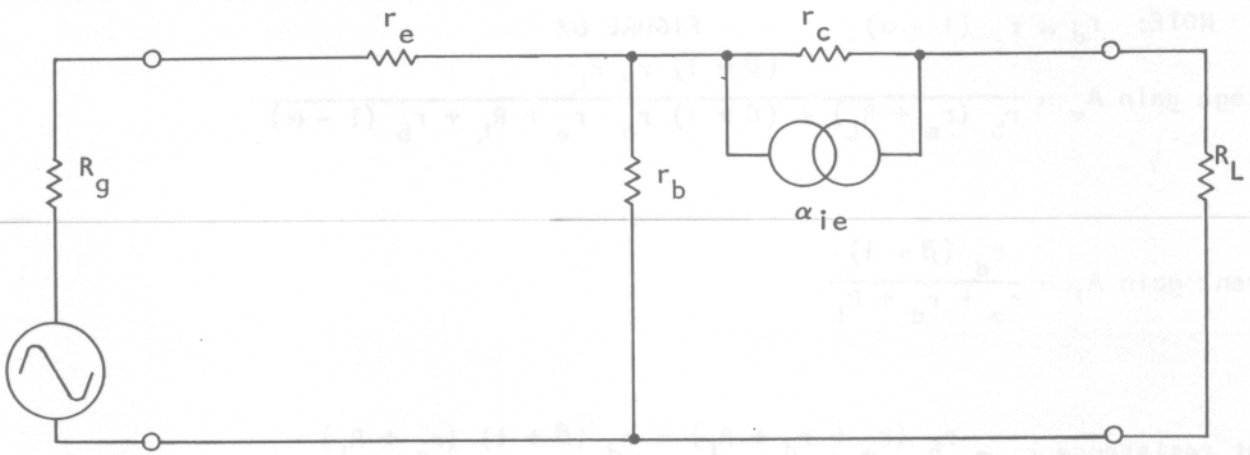


FIGURE 61

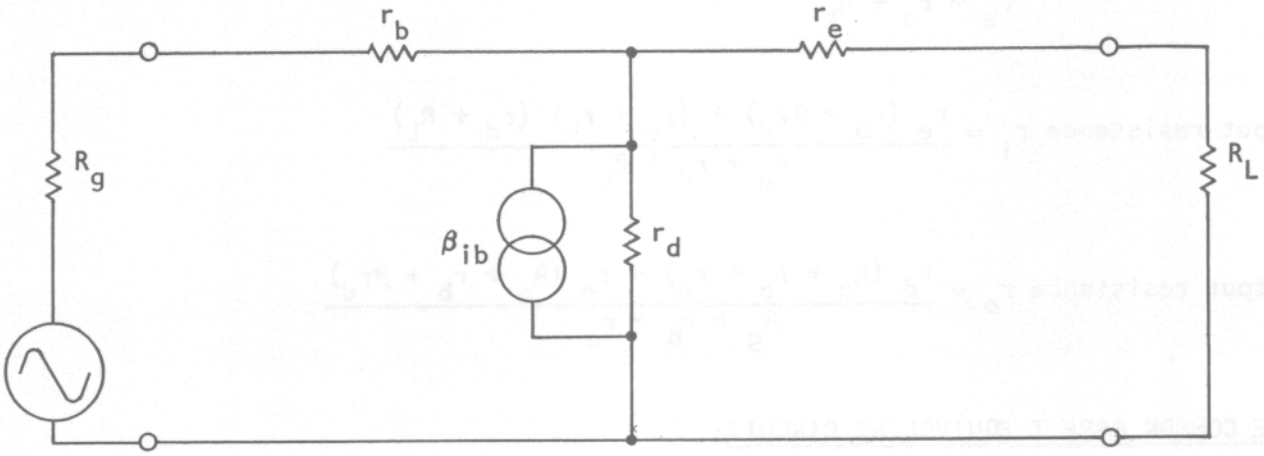
$$\text{Voltage gain } A_v = \frac{R_L\,(r_b + \alpha r_c)}{r_b\,[r_c\,(1 - \alpha) + R_L] + r_e\,(r_b + r_c + R_L)}$$

$$\text{Current gain } A_i = \frac{r_b + \alpha r_c}{r_b + r_c + R_L}$$

$$\text{Input resistance } r_i = \frac{r_b\,[r_c\,(1 - \alpha) + R_L] + r_e\,(r_b + r_c + R_L)}{r_b + r_c + R_L}$$

$$\text{Output resistance } r_o = \frac{r_b (R_g + r_e - \alpha r_c) + r_c (R_g + r_b + r_e)}{R_g + r_b + r_e}$$

THE COMMON COLLECTOR (EMITTER-FOLLOWER) T EQUIVALENT CIRCUIT:



NOTE: $r_d = r_c (1 - \alpha)$ FIGURE 62

$$\text{Voltage gain } A_v = \frac{(\beta + 1) r_d R_L}{r_b (r_e + R_L) + (\beta + 1) r_d r_e + R_L + r_b (1 - \alpha)}$$

$$\text{Current gain } A_i = \frac{r_d (\beta + 1)}{r_e + r_d + R_L}$$

$$\text{Input resistance } r_i = \frac{r_b (r_e + r_d + R_L) + r_d (\beta + 1) (r_e + R_L)}{r_e + r_d + R_L}$$

$$\text{Output resistance } r_o = \frac{r_e [R_g + r_b + r_d (\beta + 1)] + r_d (R_g + r_b)}{R_g + r_b + r_d (\beta + 1)}$$

INTERRELATIONSHIP BETWEEN THE MODELS AND PARAMETERS:

As previously discussed, most of the parameters and functional models presently in use for analysis of low frequency, small signal amplifiers are all based on the incremental measurements made on the black box, such as shown in Figure 63.

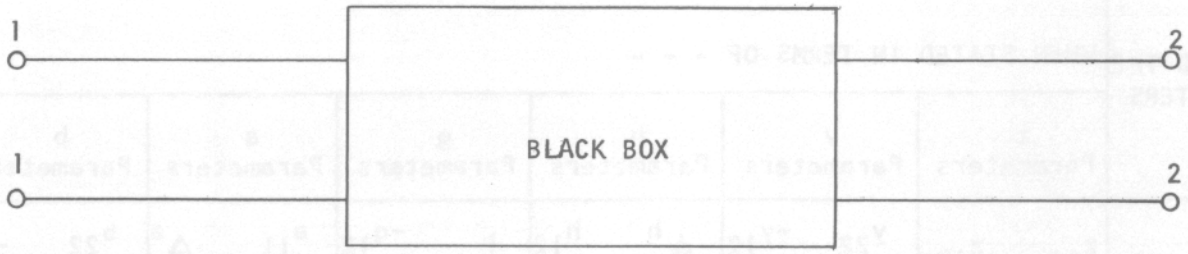


FIGURE 63

Figure 64 is a cross reference that allows any parameter that is based on measurements on the black box in Figure 63 to be found if the parameter is given in a different form than desired. For instance, suppose the manufacturer's specification sheets list the g parameters and the parameter h_{11} is needed. h_{11} is equal to $\frac{g_{22}}{\Delta^g}$ from the relationship shown in Figure 64. If the Z parameters are given and h_{21} is required, $h_{21} = \frac{-z_{21}}{z_{22}}$. Figure 64 allows a more flexible analysis when the parameters provided by several manufactueres must be relied on. To further enhance the conversion process, Figure 65 lists the determinants (Δ) in terms of the various parameters. As an example, suppose the y parameters are given and the determinant (Δ^h) of the hybrid (h) parameters is needed. $\Delta^h = \frac{y_{22}}{y_{11}}$

A-C ANALYSIS OF TWO-SIDED CIRCUITS:

Figure 66 shows a differential amplifier and its hybrid equivalent circuit. This equivalent circuit is for low frequency, small signal operation. The same hybrid equivalent circuit is used for the transistors as previously discussed, but the external emitter resistance, which is common to both, is placed common to both in the overall equivalent circuit. Kirchhoff's equations can be written to simplify the analysis. The equation for the transistor Q_1 input loop is:

$$e_1 = i_{b1} R_{g1} + i_{b1} h_{iel} + h_{rel} v_{cel} + i_x R_e$$

PARAMETER INTERRELATIONS

TO FIND THE PARAMETERS BELOW	WHEN STATED IN TERMS OF - - -											
	z Parameters		y Parameters		h Parameters		g Parameters		a Parameters		b Parameters	
z	z_{11}	z_{12}	$\frac{y_{22}}{\Delta^y}$	$\frac{-y_{12}}{\Delta^y}$	$\frac{\Delta^h}{h_{22}}$	$\frac{h_{12}}{h_{22}}$	$\frac{1}{g_{11}}$	$\frac{-g_{12}}{g_{11}}$	$\frac{a_{11}}{a_{21}}$	$\frac{\Delta^a}{a_{21}}$	$\frac{b_{22}}{b_{21}}$	$\frac{1}{b_{21}}$
	z_{21}	z_{22}	$\frac{-y_{21}}{\Delta^y}$	$\frac{y_{11}}{\Delta^y}$	$\frac{-h_{21}}{h_{22}}$	$\frac{1}{h_{22}}$	$\frac{g_{21}}{g_{11}}$	$\frac{\Delta^g}{g_{11}}$	$\frac{1}{a_{21}}$	$\frac{a_{22}}{a_{21}}$	$\frac{\Delta^b}{b_{21}}$	$\frac{b_{11}}{b_{22}}$
y	$\frac{z_{22}}{\Delta^z}$	$\frac{-z_{12}}{\Delta^z}$	y_{11}	y_{12}	$\frac{1}{h_{11}}$	$\frac{-h_{12}}{h_{11}}$	$\frac{\Delta^g}{g_{22}}$	$\frac{g_{12}}{g_{22}}$	$\frac{a_{22}}{a_{12}}$	$\frac{-\Delta^a}{a_{12}}$	$\frac{b_{11}}{b_{12}}$	$\frac{-1}{b_{12}}$
	$\frac{-z_{21}}{\Delta^z}$	$\frac{z_{11}}{\Delta^z}$	y_{21}	y_{22}	$\frac{h_{21}}{h_{11}}$	$\frac{\Delta^h}{h_{11}}$	$\frac{-g_{21}}{g_{22}}$	$\frac{1}{g_{22}}$	$\frac{-1}{a_{12}}$	$\frac{a_{11}}{a_{12}}$	$\frac{-\Delta^b}{b_{12}}$	$\frac{b_{22}}{b_{12}}$
h	$\frac{\Delta^z}{z_{22}}$	$\frac{z_{12}}{z_{22}}$	$\frac{1}{y_{11}}$	$\frac{-y_{12}}{y_{11}}$	h_{11}	h_{12}	$\frac{g_{22}}{\Delta^g}$	$\frac{-g_{12}}{\Delta^g}$	$\frac{a_{12}}{a_{22}}$	$\frac{\Delta^a}{a_{22}}$	$\frac{b_{12}}{b_{11}}$	$\frac{1}{b_{11}}$
	$\frac{-z_{21}}{z_{22}}$	$\frac{1}{z_{22}}$	$\frac{y_{21}}{y_{11}}$	$\frac{\Delta^y}{y_{11}}$	h_{21}	h_{22}	$\frac{-g_{21}}{\Delta^g}$	$\frac{g_{11}}{\Delta^g}$	$\frac{-1}{a_{22}}$	$\frac{a_{21}}{a_{22}}$	$\frac{-\Delta^b}{b_{11}}$	$\frac{b_{21}}{b_{11}}$
g	$\frac{1}{z_{11}}$	$\frac{-z_{12}}{z_{11}}$	$\frac{\Delta^y}{y_{22}}$	$\frac{y_{12}}{y_{22}}$	$\frac{h_{22}}{\Delta^h}$	$\frac{-h_{12}}{\Delta^h}$	g_{11}	g_{12}	$\frac{a_{21}}{a_{11}}$	$\frac{-\Delta^a}{a_{11}}$	$\frac{b_{21}}{b_{22}}$	$\frac{-1}{b_{22}}$
	$\frac{z_{21}}{z_{11}}$	$\frac{\Delta^z}{z_{11}}$	$\frac{-y_{21}}{y_{22}}$	$\frac{1}{y_{22}}$	$\frac{-h_{21}}{\Delta^h}$	$\frac{h_{11}}{\Delta^h}$	g_{21}	g_{22}	$\frac{1}{a_{11}}$	$\frac{a_{12}}{a_{11}}$	$\frac{\Delta^b}{b_{22}}$	$\frac{b_{12}}{b_{22}}$
a	$\frac{z_{11}}{z_{21}}$	$\frac{\Delta^z}{z_{21}}$	$\frac{-y_{22}}{y_{21}}$	$\frac{-1}{y_{21}}$	$\frac{-\Delta^h}{h_{21}}$	$\frac{-h_{11}}{h_{21}}$	$\frac{1}{g_{21}}$	$\frac{g_{22}}{g_{21}}$	a_{11}	a_{12}	$\frac{b_{22}}{\Delta^b}$	$\frac{b_{12}}{\Delta^b}$
	$\frac{1}{z_{21}}$	$\frac{z_{22}}{z_{21}}$	$\frac{-\Delta^y}{y_{21}}$	$\frac{-y_{11}}{y_{21}}$	$\frac{-h_{22}}{h_{21}}$	$\frac{-1}{h_{21}}$	$\frac{g_{11}}{g_{21}}$	$\frac{\Delta^g}{g_{21}}$	a_{21}	a_{22}	$\frac{b_{21}}{\Delta^b}$	$\frac{b_{11}}{\Delta^b}$
b	$\frac{z_{22}}{z_{12}}$	$\frac{\Delta^z}{z_{12}}$	$\frac{-y_{11}}{y_{12}}$	$\frac{-1}{y_{12}}$	$\frac{1}{h_{12}}$	$\frac{h_{11}}{h_{12}}$	$\frac{-\Delta^g}{g_{12}}$	$\frac{-g_{22}}{g_{12}}$	$\frac{a_{22}}{\Delta^a}$	$\frac{a_{12}}{\Delta^a}$	b_{11}	b_{12}
	$\frac{1}{z_{12}}$	$\frac{z_{11}}{z_{12}}$	$\frac{-\Delta^y}{y_{12}}$	$\frac{-y_{22}}{y_{12}}$	$\frac{h_{22}}{h_{12}}$	$\frac{\Delta^h}{h_{12}}$	$\frac{-g_{11}}{g_{12}}$	$\frac{-1}{g_{12}}$	$\frac{a_{21}}{\Delta^a}$	$\frac{a_{11}}{\Delta^a}$	b_{21}	b_{22}

NOTE: $\Delta^h = h_{11}\,h_{22} - h_{12}\,h_{21}$; $\Delta^z = z_{11}\,z_{22} - z_{12}\,z_{21}$; etc.

FIGURE 64

DETERMINANT INTERRELATIONS

Determinant	WHEN STATED IN TERMS OF - - -					
	z Parameters	y Parameters	h Parameters	g Parameters	a Parameters	b Parameters
Δ^z	Δ^z	$\frac{1}{\Delta^y}$	$\frac{h_{11}}{h_{12}}$	$\frac{g_{22}}{g_{11}}$	$\frac{a_{12}}{a_{21}}$	$\frac{b_{12}}{b_{21}}$
Δ^y	$\frac{1}{\Delta^z}$	Δ^y	$\frac{h_{22}}{h_{11}}$	$\frac{g_{11}}{g_{22}}$	$\frac{a_{21}}{a_{12}}$	$\frac{b_{21}}{b_{12}}$
Δ^h	$\frac{z_{11}}{z_{22}}$	$\frac{y_{22}}{y_{11}}$	Δ^h	$\frac{1}{\Delta^g}$	$\frac{a_{11}}{a_{22}}$	$\frac{b_{22}}{b_{11}}$
Δ^g	$\frac{z_{22}}{z_{11}}$	$\frac{y_{11}}{y_{22}}$	$\frac{1}{\Delta^h}$	Δ^g	$\frac{a_{22}}{a_{11}}$	$\frac{b_{11}}{b_{22}}$
Δ^a	$\frac{z_{12}}{z_{21}}$	$\frac{y_{12}}{y_{21}}$	$-\frac{h_{12}}{h_{21}}$	$-\frac{g_{12}}{g_{21}}$	Δ^a	$\frac{1}{\Delta^b}$
Δ^b	$\frac{z_{21}}{z_{12}}$	$\frac{y_{21}}{y_{12}}$	$-\frac{h_{21}}{h_{12}}$	$-\frac{g_{21}}{g_{12}}$	$\frac{1}{\Delta^a}$	Δ^b

NOTE: $\Delta^z = z_{11}\, z_{22} - z_{12}\, z_{21}$, etc.

FIGURE 65

The equation for the Q_2 input loop is:

$$e_2 = i_{b2}\, R_{g2} + i_{b2}\, h_{ie2} + h_{re2}\, v_{ce2} + i_x\, R_e$$

Where the current i_x is:

$$i_x = i_{e1} + i_{e2}$$

Where i_{e1} and i_{e2} are the a-c emitter currents of Q_1 and Q_2 and can be found by the equations:

$$i_{e1} = i_{b1}\, (h_{fe} + 1)$$

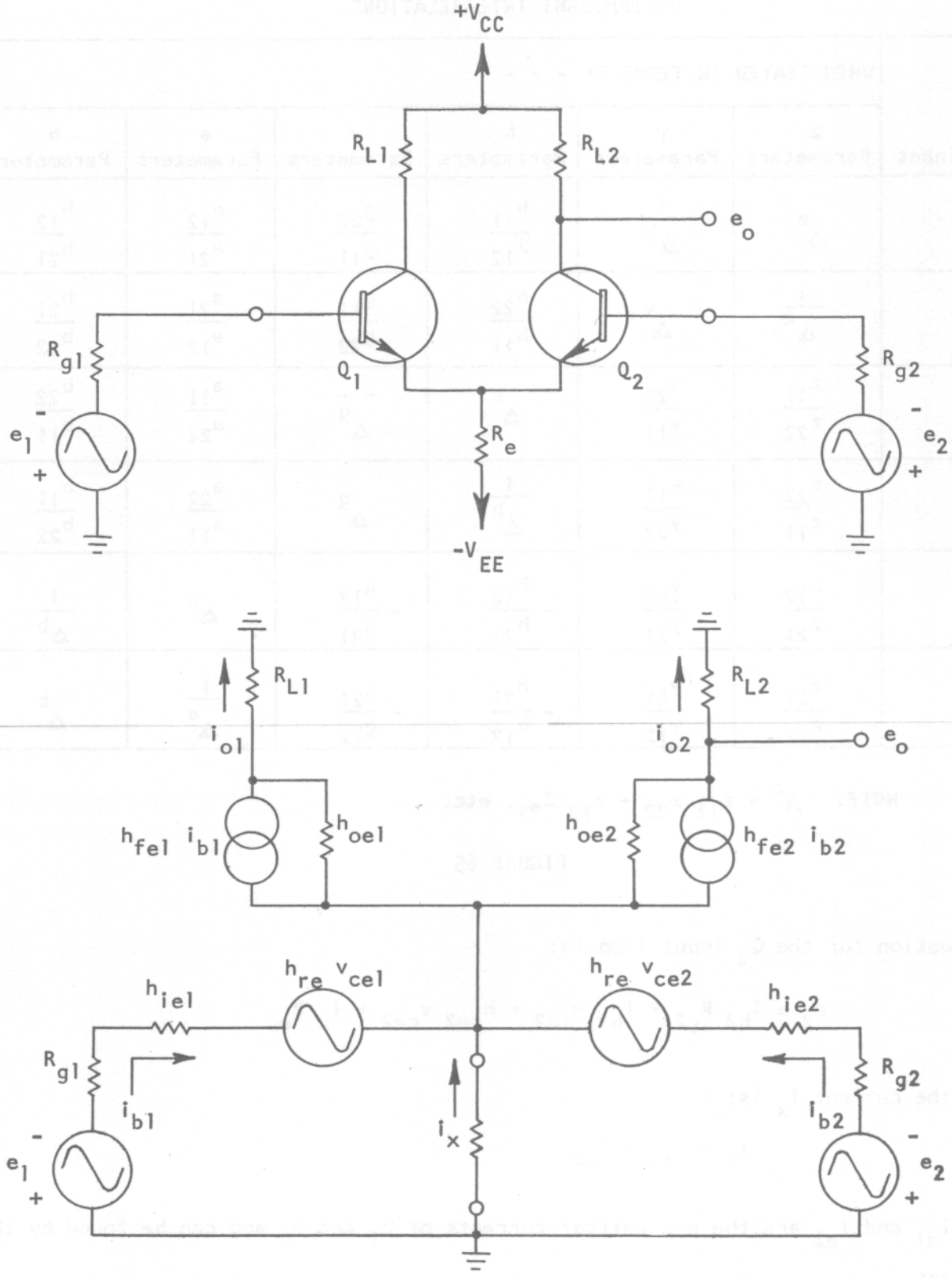

+V_CC
R_L1
R_L2
e_o
R_g1
Q_1
Q_2
R_g2
e_1
R_e
e_2
-V_EE
R_L1
R_L2
i_o1
i_o2
e_o
h_fe1 i_b1
h_oe1
h_oe2
h_fe2 i_b2
h_ie1
h_re v_ce1
h_re v_ce2
h_ie2
R_g1
R_g2
i_b1
i_x
i_b2
e_1
e_2

FIGURE 66

And: $$i_{e2} = i_{b2} (h_{fe} + 1)$$

Transposing the input loop equations to solve for i_{b1} and i_{b2}:

$$i_{b1} = \frac{e_1 - h_{re1} v_{ce1} - i_x R_e}{R_{g1} + h_{ie1}}$$

$$i_{b2} = \frac{e_2 - h_{re2} v_{ce2} - i_x R_e}{R_{g2} + h_{ie2}}$$

The circuit in most cases is long-tailed (synthesized constant current source) for stability and the external emitter resistance is much greater than the output resistance at the emitter, and $(h_{fe} + 1) R_e$ is much greater than $R_g + \frac{h_{re} v_{ce}}{i_b}$ (for either input loop), and the equations for i_b become:

$$i_{b1} = \frac{e_1 - e_2}{R_{g1} + R_{g2} + h_{ie1} + h_{ie2} + \frac{h_{re1} v_{ce1}}{i_{b1}} + \frac{h_{re2} v_{ce2}}{i_{b2}}}$$

$$i_{b2} = \frac{e_2 - e_1}{R_{g2} + R_{g1} + h_{ie2} + h_{ie1} + \frac{h_{re2} v_{ce2}}{i_{b2}} + \frac{h_{re1} v_{ce1}}{i_{b1}}}$$

Typically, the expression:

$$\frac{h_{re1} v_{ce1}}{i_{b1}} \ll R_{g1} + h_{ie1} \quad \text{and}$$

$$\frac{h_{re2} v_{ce2}}{i_{b2}} \ll R_{g2} + h_{ie2}$$

and the equations simplify to:

$$i_{b1} = \frac{e_1 - e_2}{R_{g1} + R_{g2} + h_{ie1} + h_{ie2}}$$

$$i_{b2} = \frac{e_2 - e_1}{R_{g2} + R_{g1} + h_{ie2} + h_{ie1}}$$

And for the balanced circuit with equal input generator resistances:

$$i_{b2} = \frac{e_2 - e_1}{2\,(R_g + h_{ie})}$$

The expression for current gain is:

$$A_i = \frac{h_{fe}}{1 + h_{oe}\,R_L}$$

Therefore, the expression for output current is:

$$i_{o2} = \frac{h_{fe}}{1 + h_{oe}\,R_L}\,(i_{b2})$$

Output voltage (e_o) is expressed as:

$$e_o = \frac{h_{fe}}{1 + h_{oe}\,R_L}\,(i_{b2})\,R_L$$

Therefore, substituting for i_{b2}:

$$e_o = \left(\frac{h_{fe}\,R_L}{1 + h_{oe}\,R_L}\right)\left(\frac{e_2 - e_1}{R_{g2} + R_{g1} + h_{ie2} + h_{ie1}}\right)$$

And with a balanced circuit with equal generator resistances:

$$e_o = \left(\frac{h_{fe}\,R_L}{1 + h_{oe}\,R_L}\right)\left(\frac{e_2 - e_1}{2\,(R_g + h_{ie})}\right)$$

Where the output is determined by the product of the amplifier gain and the differences in the input signals and is shown by:

$$e_2 - e_1 = \frac{2\,e_o\,(1 + h_{oe}\,R_L)\,(R_g + h_{ie})}{h_{fe}\,R_L}$$

INPUT RESISTANCE:

The input resistance for the configuration in Figure 66 can be found by dividing the input voltage by the input current. As an example, assuming a balanced circuit:

$$r_{i2} = \frac{e_2}{i_{b2}} = \left(\frac{e_2}{\frac{e_2 - e_1}{2\,(R_g + h_{ie})}}\right) = \frac{2\,e_2\,(R_g + h_{ie})}{e_2 - e_1}$$

You will note that we have been doing nothing but applying basic theorems, Ohm's Law, Kirchhoff's Law, and hybrid equivalent circuits to a two-sided configuration. Once the equivalent circuit has been established and the parameters inserted, Kirchhoff's equations can be written and the circuit solved as if we were solving a simple linear configuration. We should also keep in mind that most of the approximations that we have previously discussed can be applied to the two-sided configuration, once we have established the equivalent circuit. We can apply the exact approach that we have just been discussing or apply the approximate analysis approaches.

THE EMITTER COUPLED PARAPHASE AMPLIFIER:

Figure 67 shows the emitter coupled paraphase amplifier and its hybrid equivalent circuit for low frequency, small signals. Once again we can assume, for a practical circuit, that it is long-tailed (synthesized constant current source) and:

$$(h_{fe} + 1)\,R_e \gg h_{ie} + R_g \quad \text{and} \quad \frac{h_{re}\,v_{ce}}{i_b} \ll h_{ie} + R_g$$

Therefore:

$$i_{b1} \approx i_{b2} \approx \frac{e_1}{R_g + 2\,h_{ie}} \quad \text{(assuming a balanced circuit)}$$

and:

$$i_{o1} = \left(\frac{h_{fe}}{1 + h_{oe}\,R_L}\right)(i_{b1}) = \left(\frac{h_{fe}}{1 + h_{oe}\,R_L}\right)\left(\frac{e_1}{R_g + 2\,h_{ie}}\right)$$

$$i_{o1} = \frac{h_{fe}\,e_1}{(1 + h_{oe}\,R_L)\,(R_g + 2\,h_{ie})}$$

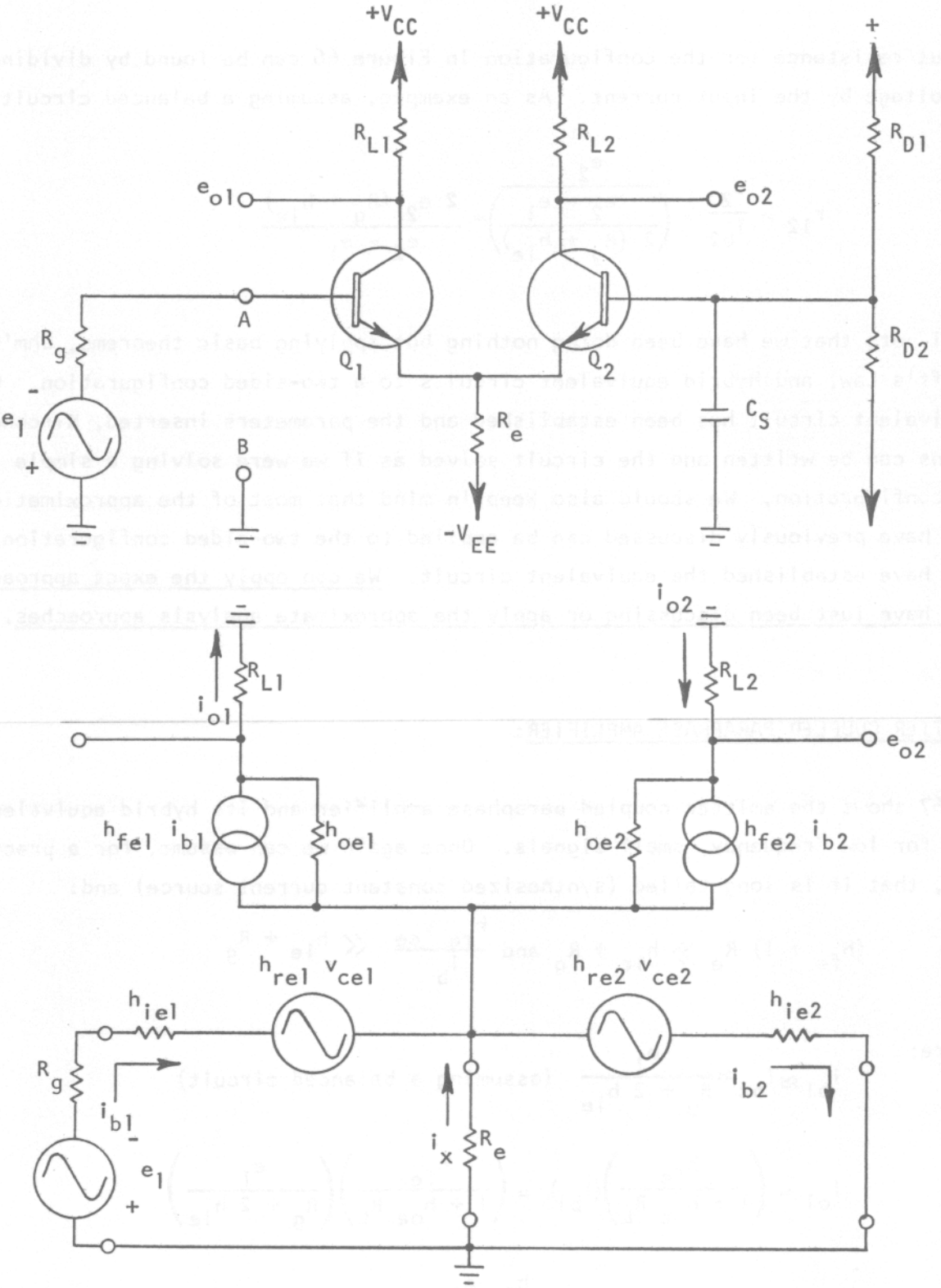

+V_CC
+V_CC
+
R_L1
R_L2
R_D1
e_o1
e_o2
A
R_g
Q_1
Q_2
R_D2
-
e_1
+
B
R_e
C_S
-V_EE
i_o2
i_o1
R_L1
R_L2
e_o2
h_fe1 i_b1
h_oe1
h_oe2
h_fe2 i_b2
h_re1 v_ce1
h_re2 v_ce2
h_ie1
h_ie2
R_g
i_b1
i_x
R_e
i_b2
e_1
+

FIGURE 67

Solving for the output voltage:

$$e_{o1} = \frac{h_{fe}\, e_1\, R_L}{(1 + h_{oe}\, R_L)\,(R_g + 2\, h_{ie})}$$

Note in Figure 67 (assuming a balanced circuit), the drive to transistor Q_2 is the same effective magnitude as that to Q_1, but that the two drives are 180° out of phase. A signal one-half the amplitude of that applied at the input terminal of Q_1 will appear across R_e, and the amount of emitter coupling is 0.5 with a long-tailed (synthesized constant current) circuit. The effective drives seen by each side is one-half the drive at the input (A-B) in Figure 67 and, assuming a balanced circuit, e_{o1} and e_{o2} will be equal in magnitude, but 180° out of phase.

Once the equivalent circuit of the emitter coupled paraphase is established, the basic laws and theorems can be applied to its solution. The approximate analysis approaches discussed earlier can also be applied to the emitter coupled paraphase amplifier.

Figure 68 shows the emitter coupled paraphase with two long-tail resistors in the emitters and a variable resistor, R_1 added as a gain control between the two. Figure 68 also shows the hybrid equivalent circuit of this configuration and illustrates how R_1 can serve as a gain control.

If R_1 is set at 0Ω, the same considerations are true as were true in Figure 67, and the same analysis approach would apply. When R_1 is not at 0Ω, the equivalent circuit in Figure 68 applies, and the equation for i_b becomes:

$$i_{b1} \approx i_{b2} \approx \frac{e_1}{R_g + 2\, h_{ie} + R_1\,(h_{fe} + 1)}$$

Therefore, the output current is:

$$i_{o1} = \left(\frac{h_{fe}}{1 + h_{oe}\, R_L}\right)(i_{b1}) = \left(\frac{h_{fe}}{1 + h_{oe}\, R_L}\right)\left(\frac{e_1}{R_g + 2\, h_{ie} + (h_{fe} + 1)\, R_1}\right)$$

And the output voltage is:

$$e_{o1} = \frac{h_{fe}\, e_1\, R_L}{(1 + h_{oe}\, R_L)\,(R_g + 2\, h_{ie} + (h_{fe} + 1)\, R_1)}$$

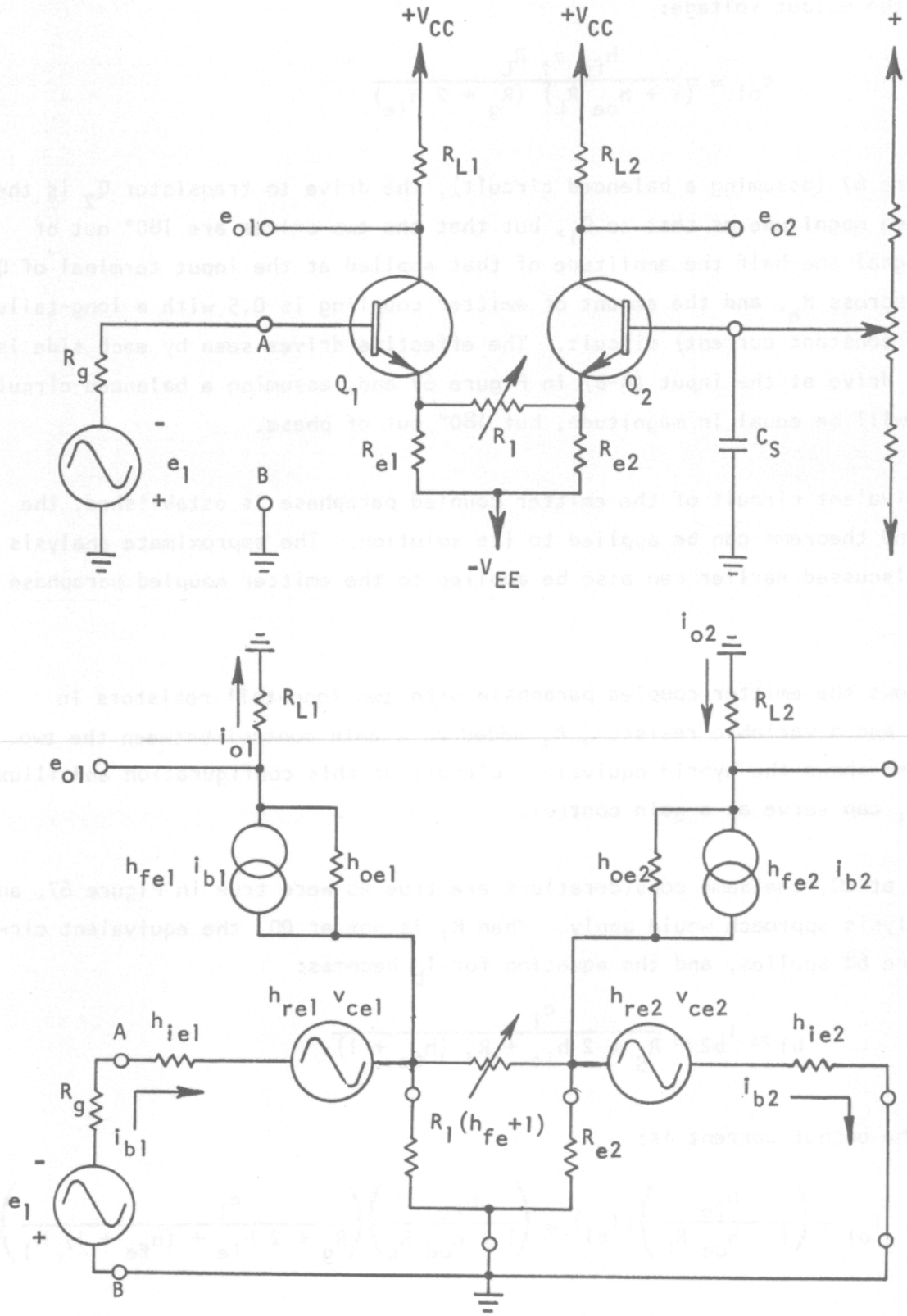

+V_CC
+V_CC
+
R_L1
R_L2
R_D1
e_o1
e_o2
R_2
A
R_g
Q_1
Q_2
-
e_1
+
B
R_e1
R_1
R_e2
C_S
R_D2
-V_EE
i_o2
i_o1
h_fe1 i_b1
h_oe1
h_oe2
h_fe2 i_b2
h_re1 v_ce1
h_re2 v_ce2
h_ie1
h_ie2
i_b2
i_b1
R_1 (h_fe+1)

FIGURE 68

Indicating that i_o and the output voltage will be inversely proportional to the resistance setting of R_1 (actually the value of R_1 is magnified by $h_{fe} + 1$). R_2 is the d-c balance control to insure that both sides of R_1 are at the same d-c level at any setting of R_1. If this is not so, d-c current will flow through R_1, and Rotating R_1 will present a d-c signal to the amplifier and result in a d-c shift of the level of the output of the amplifier. The equation for a mid-range value of R_1 for a desired value of output voltage when the input voltage e_1 is known, the preceding formulas can be transposed to read:

$$R_1 = \frac{h_{fe}\, R_L\, e_1}{(h_{fe} + 1)\,(1 + h_{oe}\, R_L)\, e_o} - \frac{R_g + 2\, h_{ie}}{h_{fe} + 1}$$

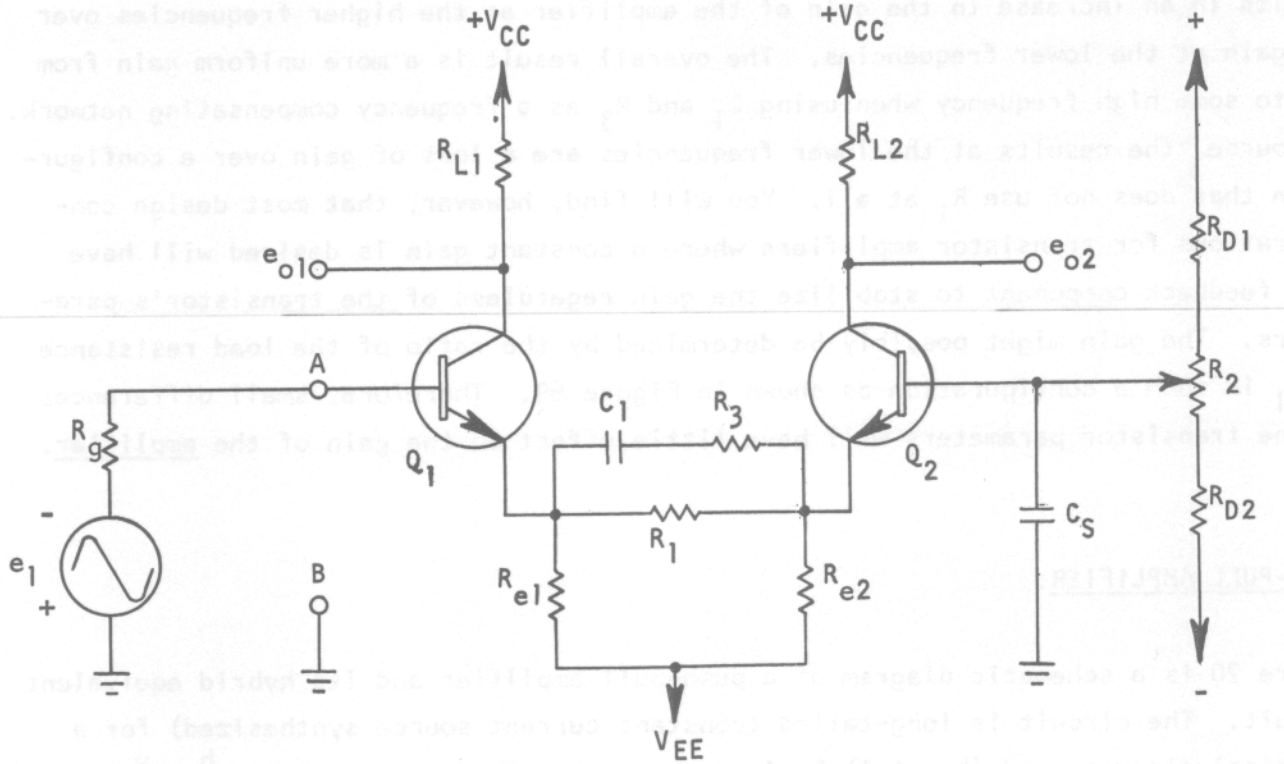


FIGURE 69

Figure 69 shows R_1 in conjunction with an RC network being used to frequency compensate the emitter coupled paraphase amplifier. This type of compensation can be used with any of the two-sided configurations; however, it is shown here as an example with the emitter coupled paraphase. We have already shown that R_1, when placed in the circuit, can be used to reduce the gain of the amplifier. If R_1 is in someway shunted at a different frequency (it's resistance effectively reduced), the gain at that frequency is increased (referring to the gain of the overall amplifier). At the higher frequencies, the reactance of C_1 is reduced, and the resistance of R_3 in series with the reactance of C_1 shunts R_1. At the lower frequencies, the reactance of C_1 is fairly high and most of R_1 is effectively in the circuit. We have already discussed that the transistor's gain at the higher frequencies is reduced when no compensation is added, and the reduction is similar to an RC roll-off of gain with frequency. The insertion of C_1 and R_3, shunting R_1, in Figure 69 results in an increase in the gain of the amplifier at the higher frequencies over its gain at the lower frequencies. The overall result is a more uniform gain from d-c to some high frequency when using C_1 and R_3 as a frequency compensating network. Of course, the results at the lower frequencies are a loss of gain over a configuration that does not use R_1 at all. You will find, however, that most design considerations for transistor amplifiers where a constant gain is desired will have some feedback component to stabilize the gain regardless of the transistor's parameters. The gain might possibly be determined by the ratio of the load resistance to R_1 in such a configuration as shown in Figure 69. Therefore, small differences in the transistor parameters will have little effect on the gain of the amplifier.

PUSH-PULL AMPLIFIER:

Figure 70 is a schematic diagram of a push-pull amplifier and its hybrid equivalent circuit. The circuit is long-tailed (constant current source synthesized) for a practical circuit, and $(h_{fe} + 1)\, R_e$ is much greater than $h_{ie} + R_g$; and $\frac{h_{re}\, v_{ce}}{i_b}$ is much less than $h_{ie} + R_g$.

Assuming a balanced circuit:

$$i_{b1} \approx i_{b2} \approx \frac{e_1 + e_2}{2\, R_g + 2\, h_{ie}}$$

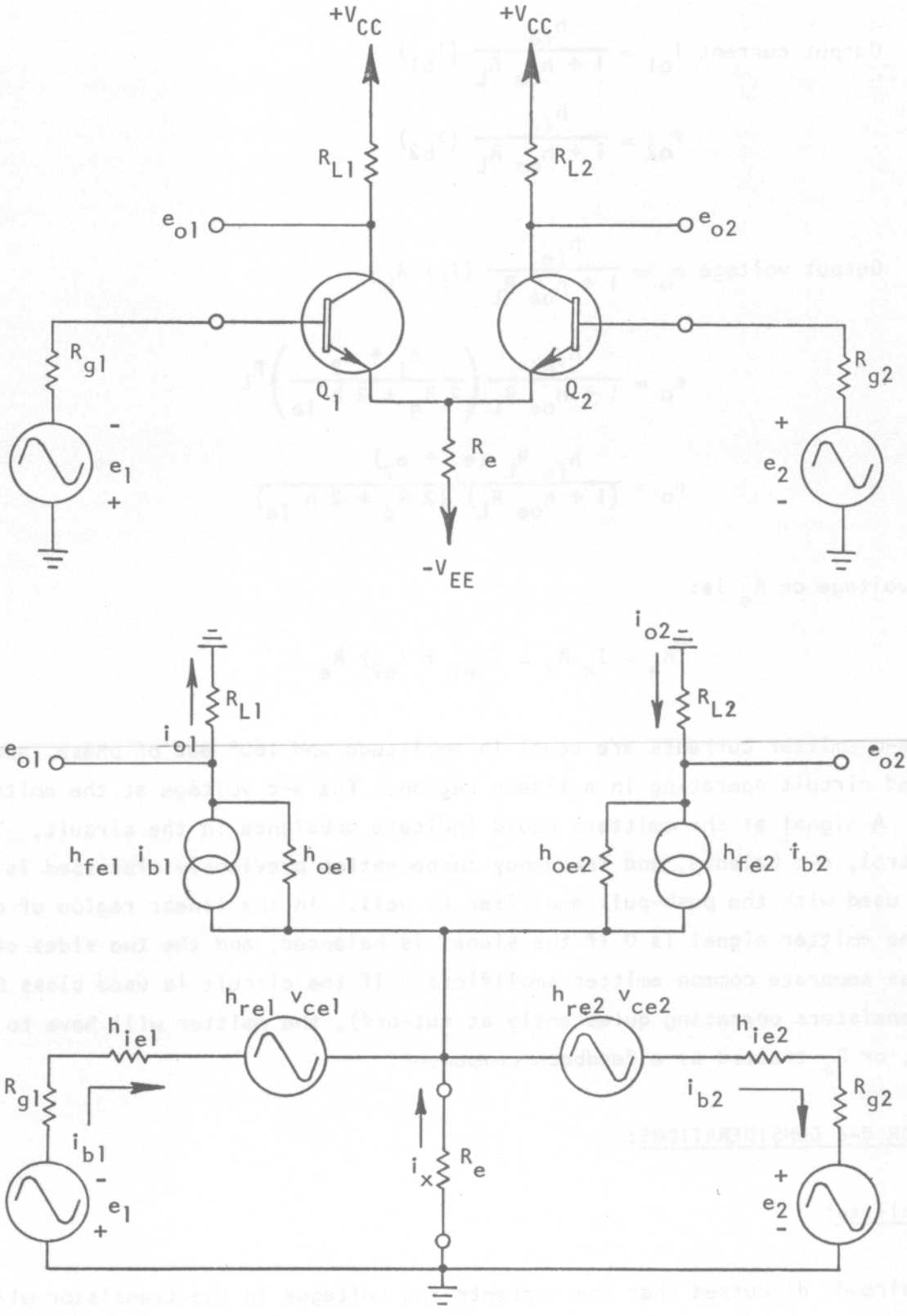

+V_CC
+V_CC
R_L1
R_L2
e_o1
e_o2
R_g1
R_g2
Q_1
Q_2
R_e
-V_EE
e_1
e_2
i_o2
i_o1
h_fe1 i_b1
h_oe1
h_oe2
h_fe2 i_b2
h_re1 v_ce1
h_re2 v_ce2
h_ie1
h_ie2
i_b1
i_b2
i_x

FIGURE 70

and:

$$\text{Output current } i_{o1} = \frac{h_{fe}}{1 + h_{oe} R_L} (i_{b1})$$

$$i_{o2} = \frac{h_{fe}}{1 + h_{oe} R_L} (i_{b2})$$

and:

$$\text{Output voltage } e_o = \frac{h_{fe}}{1 + h_{oe} R_L} (i_b) R_L$$

$$e_o = \frac{h_{fe}}{1 + h_{oe} R_L} \left(\frac{e_1 + e_2}{2 R_g + 2 h_{ie}} \right) R_L$$

$$e_o = \frac{h_{fe} R_L (e_1 + e_2)}{(1 + h_{oe} R_L)(2 R_g + 2 h_{ie})}$$

The a-c voltage on R_e is:

$$e_{R_e} = i_x R_e = (i_{e1} + i_{e2}) R_e$$

The two a-c emitter currents are equal in amplitude and 180° out of phase, assuming a balanced circuit operating in a linear region. The a-c voltage at the emitters is zero. A signal at the emitters would indicate unbalance in the circuit. The gain control, d-c balance, and frequency compensation previously discussed is commonly used with the push-pull amplifier as well. In the linear region of operation, the emitter signal is 0 if the signal is balanced, and the two sides can be treated as separate common emitter amplifiers. If the circuit is used class B (both transistors operating quiescently at cut-off), the emitter will have to be bypassed, or R_e treated as a feedback component.

TRANSISTOR d-c CONSIDERATIONS:

Bias Stability:

We have already discussed that the currents and voltages in the transistor will change as the surrounding temperature changes. The current is related exponentially to the temperature and the applied voltage. These changes within the transistor are

due primarily to the formation of more hole-electron pairs with an increase in temperature or the recombination of hole-electron pairs with a decrease in temperature. This, of course, increases and decreases the number of minority carriers available in all parts of the transistor.

These temperature changes can originate internal or external of the transistor. The change in the surrounding air temperature can result in a change of the number of hole-electron pairs in different parts of the transistor, or a change in the power being dissipated by the transistor can change the junction temperature. In normal amplifier action, the power dissipation and consequently the heat is generated at the collector junction. This is due to the product of collector voltage and collector current being generally much greater than the product of emitter current and emitter voltage. In a few cases, where considerable base current is flowing, the emitter junction heat must be taken into account.

The total change in temperature that the transistor can encounter can be calculated by determining the maximum ambient temperature that might be expected and adding this to the product of a transistor's thermal resistance, junction to ambient (θ_{JA}), and the collector power dissipation. Collector power dissipation can be the product of the average collector current and collector voltage, or when dealing with switching circuits and pulse amplifiers, the peak power dissipation is the product of the peak current and voltage. The thermal considerations and thermal to electrical analogy previously discussed, applies here as well.

Since the parameter considerations will vary with the change in the d-c operating point, it is essential in all amplifiers to hold the quiescent d-c operating point as stable as possible. Of course, thermal compensation in semiconductor d-c amplifier circuits is one of, if not the prime consideration, in design.

In general, the greatest problem with thermal instability is encountered in the common emitter configuration. A transistor in a common base configuration has the base at ground potential and the current, as a result of thermal generated minority carriers, is the current I_{CBO}. I_{CBO} is the current collector to base with the emitter d-c open circuited. In other words, this is simply the diode saturation current of the collector base junction at a given temperature. The current I_{CBO} is limited by the number of minority carriers adjacent to the reverse biased

collector junction. The current I_{CBO} is primarily limited by the number of minority carriers in the base since it is the more lightly doped of the two sides of the junction, and can be a relatively small value at room temperature.

If the base is d-c open circuited, and the emitter is not open circuited, the reverse voltage applied to the collector junction will also be applied to the emitter-base junction. The voltage applied to the collector junction will reverse bias the collector junction; however, this same voltage will forward bias the emitter-base junction. This is illustrated in Figure 71. We will find that the number of minority carriers in the base under these conditions will be increased by approximately the d-c beta of the transistor. In other words, we now have beta times the minority carriers available in the base as we did in the situation where the emitter was d-c open circuited, and the collector voltage was applied between collector and base. Since the current is related to the number of minority carriers adjacent to the junction, and the number of minority carriers in the base has been increased by approximately the d-c beta of the transistor, we might say that the current, collector to emitter, as a result of thermally generated carriers, is approximately beta times the current collector to base as a result of thermally generated carriers (this assumes the base is d-c open circuited so that all of the minority carrier current must take the path of the emitter-base junction). A deeper coverage of currents and voltages in a semiconductor junction can be found in the tables in Volume 6 of this series.

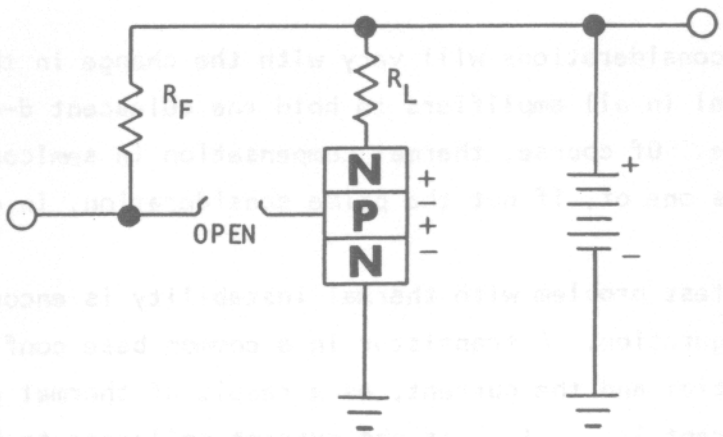


FIGURE 71

It can be seen that the transistor currents and voltages in a common base configuration will vary as the exponent containing temperature varies. In the common emitter configuration, however, if the base is a high resistance or near open circuit, the current and voltage changes can be magnified by approximately the beta of the transistor when the temperature changes. The common collector configuration, having its load resistance in the emitter lead, has sufficient d-c feedback to maintain control of the current with temperature variations. Transformer coupling, of course, would aid the problem of thermal instability by keeping a low d-c resistance in the base circuit of a common emitter configuration.

TEMPERATURE SENSITIVE DEVICE STABILITY:

Temperature sensitive components may be used to stabilize the operating point. Figure 72 shows a thermistor being used to stabilize the d-c operating point. A thermistor is a resistor with controlled negative temperature coefficient of resistance. That is, the resistance of the thermistor will decrease at a predetermined rate with an increase in temperature, and vice-versa.

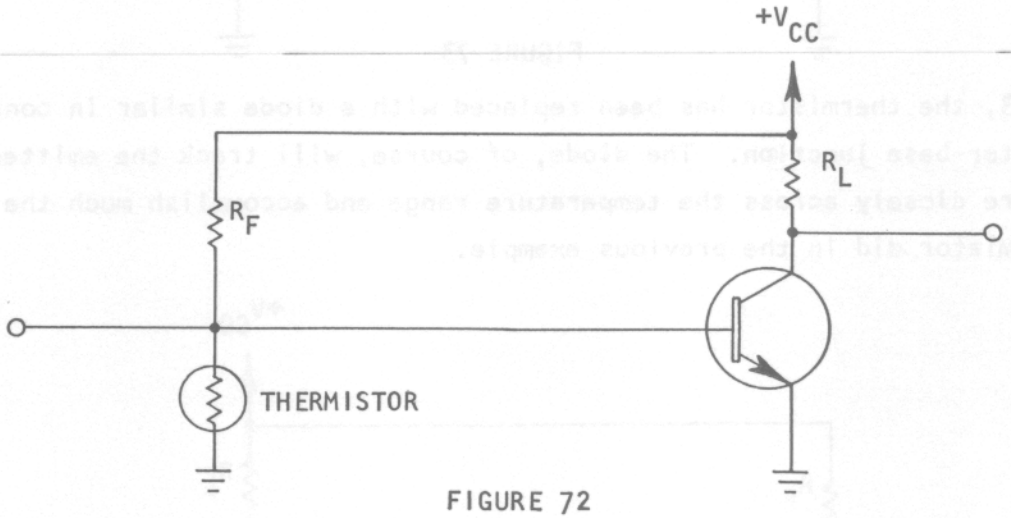


FIGURE 72

An increase in temperature, of course, increases the minority carrier current (thermally generated), increasing the collector current. With a high resistance in the base lead, the current is magnified by approximately the d-c beta of the transistor. This current can be considered to be approximately I_{CEO}. In the circuit in Figure 72, however, as the temperature increases, the resistance of a thermistor decreases, maintaining a near constant V_{BE} on the transistor, and holding

the collector current down. The disadvantage of the thermistor is that its resistance does not change exactly as the resistance of the emitter-base junction changes with temperature and, therefore, does not track exactly across temperature range. The thermistor typically loses control around 75°C, where large changes in minority carrier current occur in a germanium transistor. In a silicon transistor, the initial thermally generated minority carrier current is typically low, and the thermistor will track to a higher temperature. Figure 73 shows a temperature sensitive device that has much the same action as the thermistor, but will more closely track the emitter-base junction changes across the temperature range.

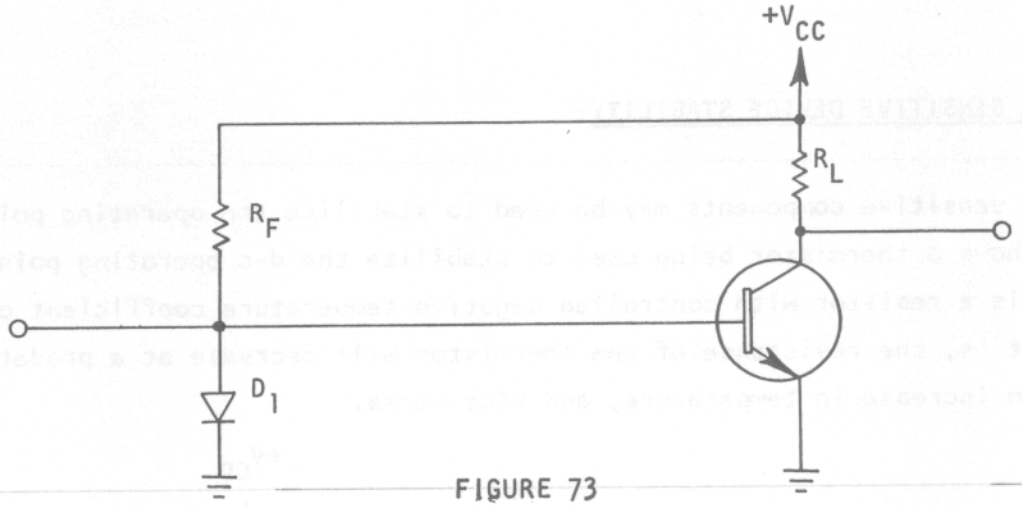


FIGURE 73

In Figure 73, the thermistor has been replaced with a diode similar in construction to the emitter-base junction. The diode, of course, will track the emitter-base junction more closely across the temperature range and accomplish much the same job as the thermistor did in the previous example.

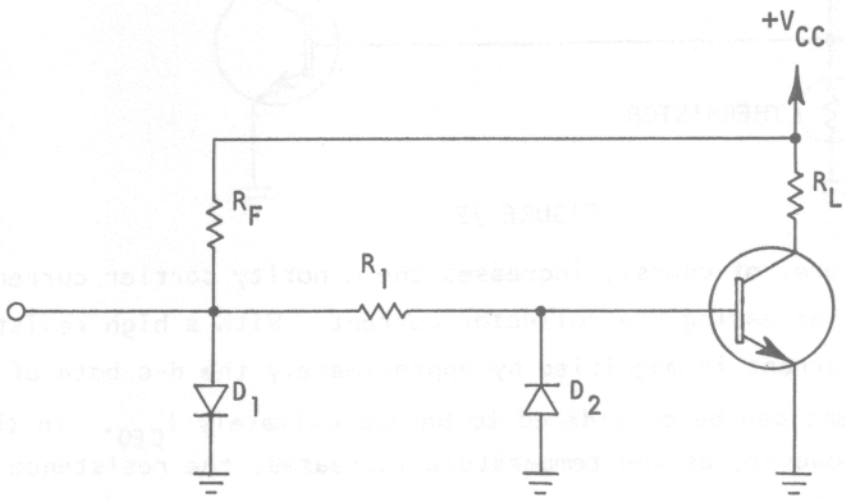
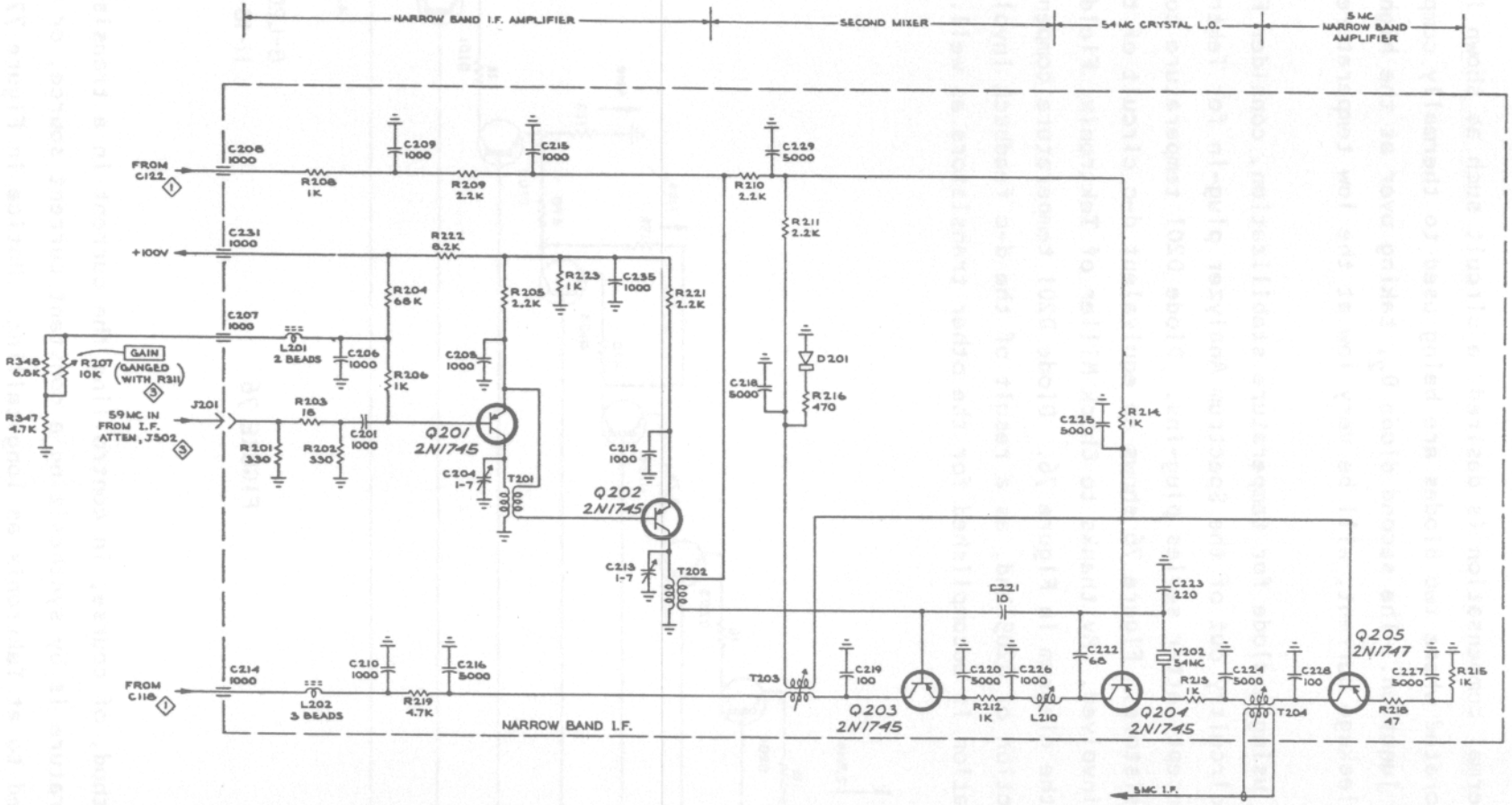


FIGURE 74

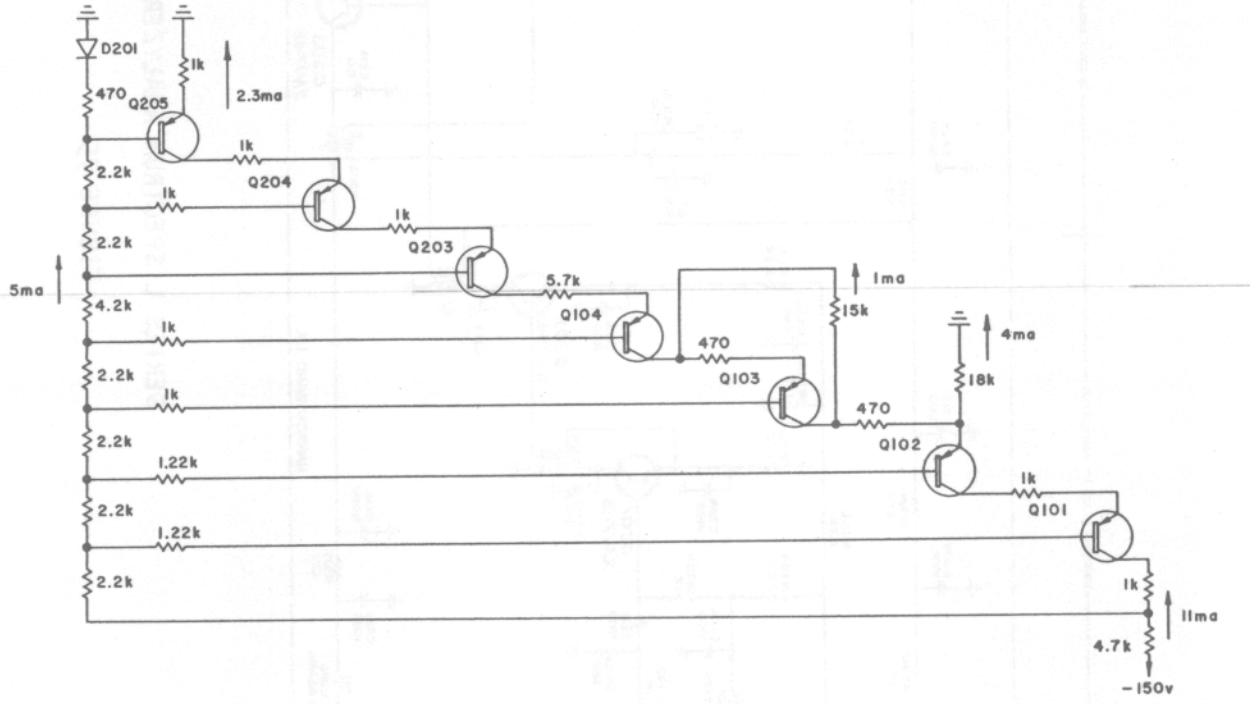


SERIES L SPECTRUM ANALYZER

FIGURE 75

If additional thermal compensation is desired, a circuit such as shown in Figure 74 can be incorporated where two diodes are being used to thermally compensate the emitter-base junction. The second diode D_2, taking over at the higher temperatures since its leakage current, will be very low at the low temperatures.

As an example of using a diode for temperature stabilization, consider Figure 75. Figure 75 shows circuitry out of the Spectrum Analyzer plug-in for Tektronix oscilloscopes, which accept letter series plug-ins. Diode D201 temperature compensates a string of transistors. Figure 76 shows an equivalent d-c circuit of the diode and transistors involved. My thanks to Chuck Miller of Tektronix, Field Training, by the way, for the diagram in Figure 76. Diode D201 temperature compensates the emitter-base junction of Q205 and, as a result of the d-c feedback involved, temperature compensation is accomplished for the other transistors as well.



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11-16-'64 dl

FIGURE 76

LONG-TAILING:

One very good method, of course, in controlling the current in a transistor with changes in temperature is by synthesizing a constant current source, or what is generally referred to at Tektronix as long-tailing. Notice in Figure 77 that, with the base of the transistor set at a given voltage, the emitter must follow if the

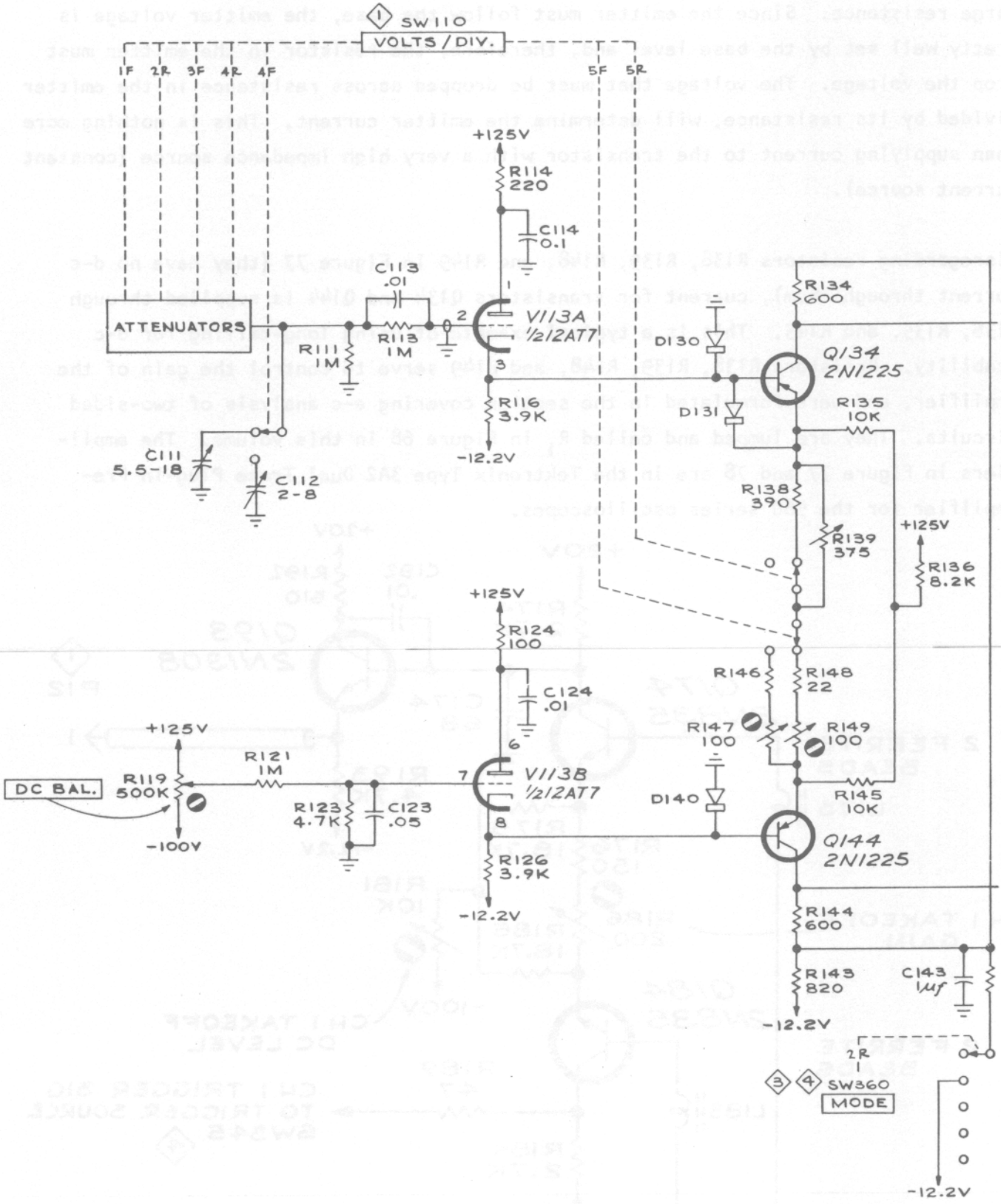

1 SW110
VOLTS / DIV.
1F 2R 3F 4R 4F
5F 5R
ATTENUATORS
+125V
R114 220
C114 0.1
C113 .01
R111 1M
R113 1M
V113A 1/2 12AT7
R116 3.9K
-12.2V
C111 5.5-18
C112 2-8
R134 600
D130
Q134 2N1225
D131
R135 10K
R138 390
R139 375
R136 8.2K
+125V
R124 100
C124 .01
R146
R148 22
R147 100
R149 100
+125V
DC BAL.
R119 500K
-100V
R121 1M
R123 4.7K
C123 .05
V113B 1/2 12AT7
D140
R145 10K
Q144 2N1225
R126 3.9K
-12.2V
R144 600
R143 820
C143 1μf
-12.2V
2R
3 4 SW360
MODE
-12.2V

FIGURE 77

transistor conducts. The emitter is returned to a fairly large voltage through a large resistance. Since the emitter must follow the base, the emitter voltage is pretty well set by the base level and, therefore, the resistor in the emitter must drop the voltage. The voltage that must be dropped across resistance in the emitter divided by its resistance, will determine the emitter current. This is nothing more than supplying current to the transistor with a very high impedance source (constant current source).

Disregarding resistors R138, R139, R148, and R149 in Figure 77 (they have no d-c current through them), current for transistors Q134 and Q144 is supplied through R136, R135, and R145. This is a typical example of using long-tailing for d-c stability. Resistors R138, R139, R148, and R149 serve to control the gain of the amplifier, and were formulated in the section covering a-c analysis of two-sided circuits. They are lumped and called R_1 in Figure 68 in this volume. The amplifiers in Figure 77 and 78 are in the Tektronix Type 3A2 Dual Trace Plug-In Preamplifier for the 560 series oscilloscopes.

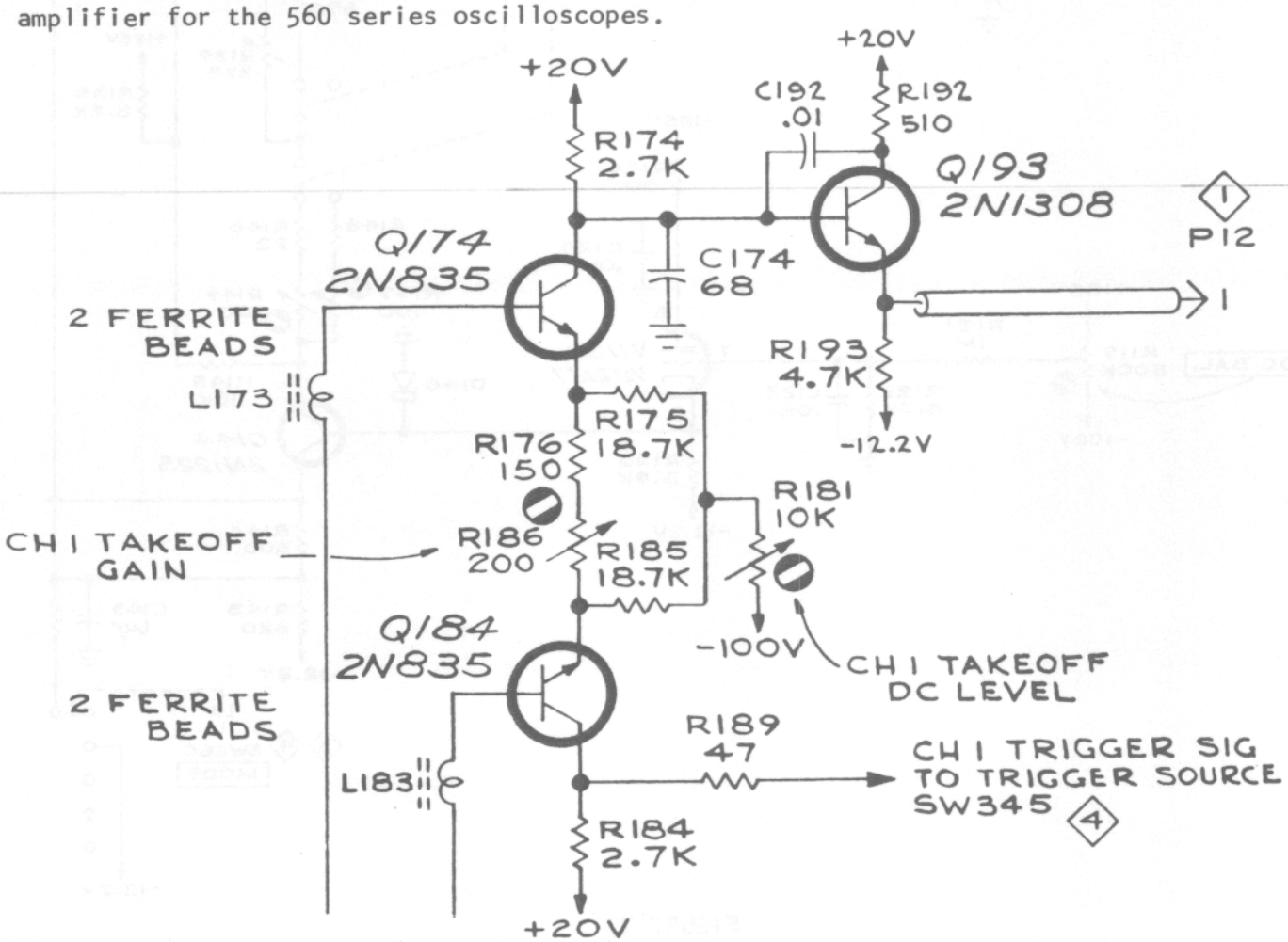


FIGURE 78

In Figure 78, a portion of the long-tail resistor is made variable. This allows the transistor currents to be adjusted. When the current is changed, the drop across the collector load resistor changes and the output voltage. The variable resistor R181 in Figure 78 allows the quiescent d-c operating point currents and voltages to be adjusted, while maintaining d-c stability with temperature changes.

When a second supply voltage is not available, a configuration such as shown in Figure 79 can be used, where a divider from the collector supply is used to establigh the base voltage at some level and then the long-tail or the emitter resistor is added to synthesize a constant current source. This is the most typical configuration that you will find in the less critical transistor circuitry.

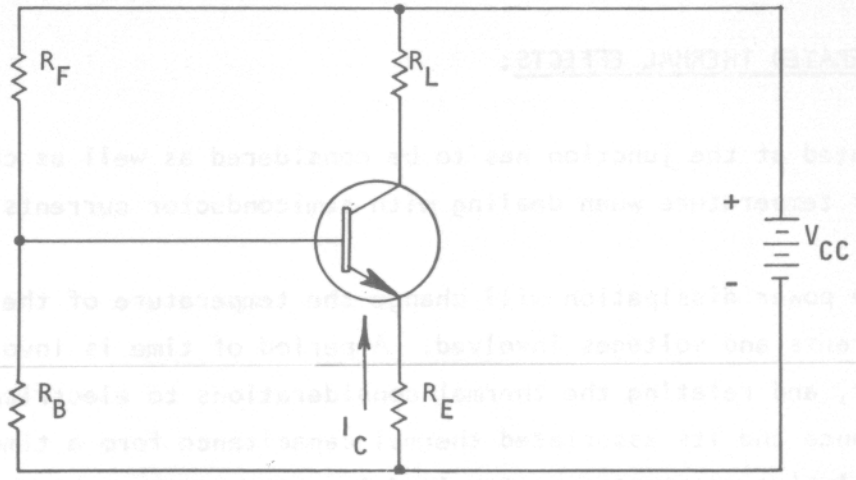


FIGURE 79

Figure 80 shows the further increase in the stability of the transistor configuration over that in Figure 79 by adding d-c feedback from the collector back to the base as well as utilizing the emitter resistor to effectively synthesize a constant current source.

It should be brought out at this point that if d-c gain is the consideration, these degenerative effects that we have added will reduce the d-c gain. In Figure 79, the long-tail resistor can be bypassed by a capacitor at the low frequencies and high frequencies, but at d-c this is not possible. This can be overcome by operating the circuitry two-sided in the linear region by using a push-pull amplifier or differential amplifier, such as shown in Figure 78. We can operate the transistors in the linear region and have any changes cancel across a common emitter resistance. We can, in this way, accomplish d-c stability, while accomplishing d-c amplification.

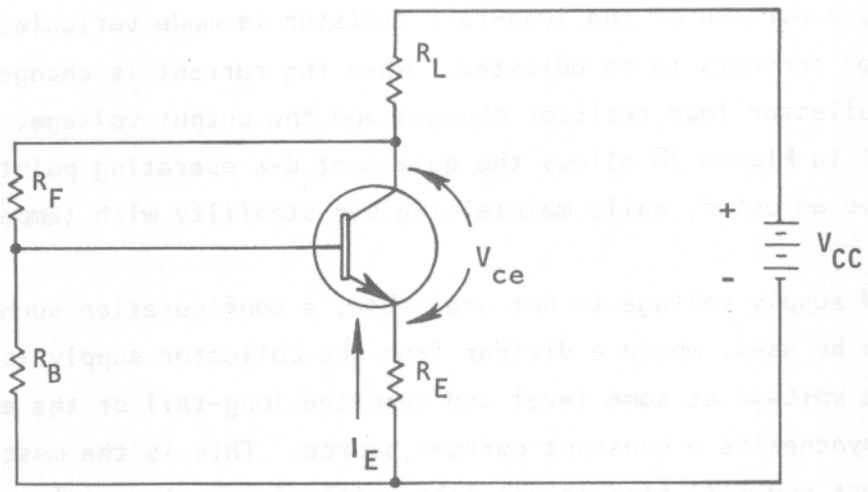


FIGURE 80

INTERNALLY GENERATED THERMAL EFFECTS:

The heat generated at the junction has to be considered as well as changes in surrounding air temperature when dealing with semiconductor currents and voltages.

A change in the power dissipation will change the temperature of the junction and change the currents and voltages involved. A period of time is involved for this change, however, and relating the thermal considerations to electrical terms, the thermal resistance and its associated thermal capacitance form a time constant, and five thermal time constants are involved in a temperature change. (This has previously been discussed in Volume 6.)

Synthesized constant current sources (long-tailing, etc.), negative feedback d-c, and temperature sensitive devices can be used to compensate the quiescent operating point of a semiconductor device to temperature changes. Once again, the temperature changes can be internal or external of the device. If a voltage is to be compensated, for instance the voltage across the thermals of a zener diode, a device with an opposite temperature coefficient of voltage can be inserted in series and the output taken across both devices. A zener diode operated in avalanche breakdown and a forward conducting diode are examples. The zener diode has a positive temperature coefficient of voltage when its breakdown voltage is above 6v, and the forward conducting diode has a negative temperature coefficient of voltage. The voltage across both devices can be made to stay relatively constant with temperature

changes when they are placed in series, and the output taken across both devices. (This was covered in Volumes 2 and 6.) Both of these devices can also be used to temperature compensate the transistor configuration.

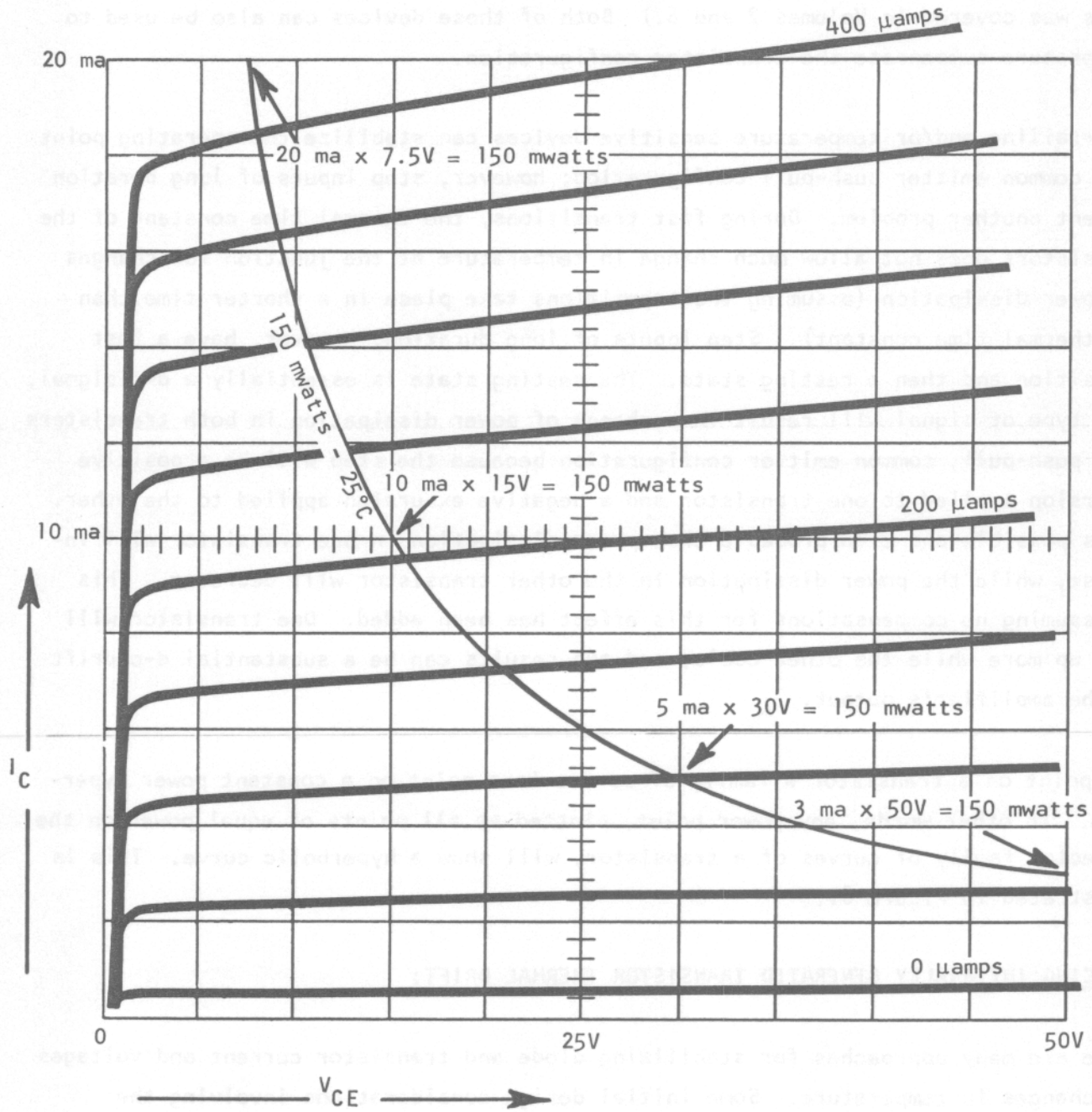
Long-tailing and/or temperature sensitive devices can stabilize the operating point of a common emitter push-pull configuration; however, step inputs of long duration present another problem. During fast transitions, the thermal time constant of the transistors does not allow much change in temperature at the junction for changes in power dissipation (assuming the transitions take place in a shorter time than one thermal time constant). Step inputs of long duration, however, have a fast transition and then a resting state. The resting state is essentially a d-c signal. This type of signal will result in a change of power dissipation in both transistors in a push-pull, common emitter configuration because the step will be a positive excursion applied to one transistor and a negative excursion applied to the other. It is possible and even probable that power dissipation in one transistor will increase, while the power dissipation in the other transistor will decrease. This is assuming no compensations for this effect has been added. One transistor will heat up more while the other cools, and the results can be a substantial d-c drift in the amplifier's output.

Any point on a transistor's family of curves is a point on a constant power hyperbole. In other words, any power point, plotted at all points of equal power on the collector family of curves of a transistor, will show a hyperbolic curve. This is illustrated in Figure 81.

REDUCING INTERNALLY GENERATED TRANSISTOR THERMAL DRIFT:

There are many approaches for stabilizing diode and transistor current and voltages for changes in temperature. Some initial design considerations involving the selection of the d-c load line and quiescent operating point can minimize the problems associated with internally generated heat as a result of changes in power dissipation when a signal is applied. The aim of this discussion is an approach to minimize the effects of applied signal change in the power dissipation which in turn results in a change in junction temperature.

Consider the linear plot of current versus voltage in Figure 82. A resistive load



COLLECTOR FAMILY OF CURVES WITH A MAXIMUM
POWER CURVE - 150 mwatts - 25°C

FIGURE 81

line is plotted in the left-hand diagram, and a constant power hyperbole in the right-hand diagram in Figure 82.

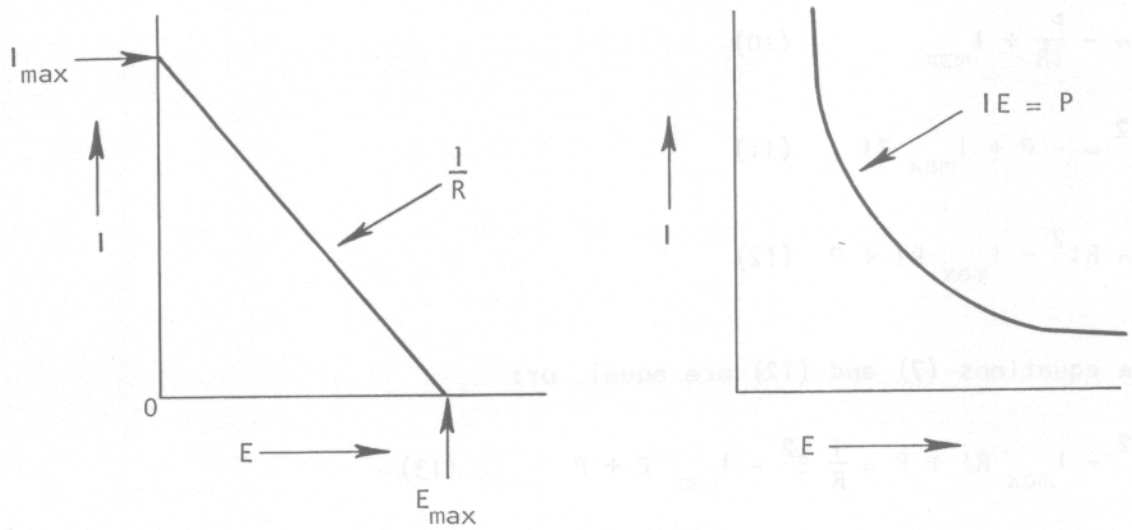


FIGURE 82

Writing equations for the load line and constant power hyperbole in Figure 1:

$$I = -\frac{1}{R}E + I_{max} \qquad (1)$$

$$P = IE \qquad (2)$$

$$E_{max} = R\, I_{max} \qquad (3)$$

The points of intersection of the load line and constant power hyperbole in Figure 82 (assuming they do intersect) can be found by the simultaneous solution of equations (1), (2), and (3).

$$I = -\frac{1}{R}E + I_{max} \qquad (4)$$

$$\frac{P}{E} = -\frac{1}{R}E + I_{max} \qquad (5)$$

$$P = -\frac{1}{R}E^2 + I_{max}E \qquad (6)$$

$$0 = \frac{1}{R}E^2 - I_{max}E + P \qquad (7)$$

$$I = -\frac{1}{R}E + I_{max} \qquad (8)$$

$$I = -\frac{1}{R}\frac{P}{I} + I_{max} \qquad (9)$$

$$I = -\frac{P}{IR} + I_{max} \qquad (10)$$

$$RI^2 = -P + I_{max}RI \qquad (11)$$

$$0 = RI^2 - I_{max}RI + P \qquad (12)$$

and therefore equations (7) and (12) are equal, or:

$$RI^2 - I_{max}RI + P = \frac{1}{R}E^2 - I_{max}E + P \qquad (13)$$

$$E = \frac{I_{max}R}{2} \pm \frac{R}{2}\sqrt{I_{max}^2 - \frac{4P}{R}} \qquad (14)$$

$$I = \frac{I_{max}}{2} \pm \frac{1}{2}\sqrt{I_{max}^2 - \frac{4P}{R}} \qquad (15)$$

If the load line and hyperbole intersect at only one point, the points of intersection found using equations (14) and (15) will be equal, and the load line is tangent to the constant power hyperbole and:

$$\frac{I_{max}R}{2} + \frac{R}{2}\sqrt{I_{max}^2 - \frac{4P}{R}} = \frac{I_{max}R}{2} - \frac{R}{2}\sqrt{I_{max}^2 - \frac{4P}{R}} \qquad (16)$$

$$0 = I_{max}^2 - \frac{4P}{R} \qquad (17)$$

then:
$$E = \frac{I_{max}R}{2} \qquad (18)$$

and since:
$$I_{max} = \frac{E_{max}}{R} \qquad (19)$$

E and I at the point of tangency are:

$$E = \frac{E_{max}}{2} \qquad (20)$$

$$I = \frac{I_{max}}{2} \qquad (21)$$

The point of tangency of a load line and a constant power hyperbole is at 1/2 maximum voltage and current for the load line.

Now, if the point of tangency is assumed to be the quiescent point, the product of $P = EI$ at points of $E \pm e_s$ can be found as illustrated in Figure 83.

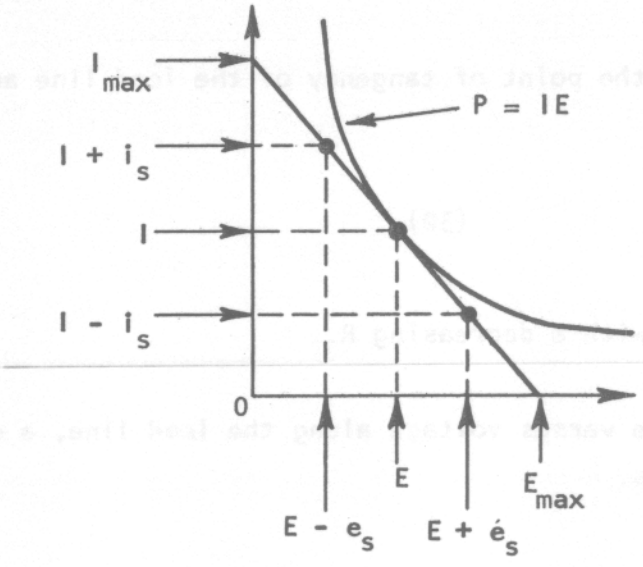


FIGURE 83

At the point of tangency, $P = EI$

At $E - e_s$: $P' = (E - e_s)(I + i_s)$ (22)

$$P' = IE + E\,i_s - e_s\,I - e_s i_s \qquad (23)$$

At $E = e_s$: $P'' = (E + e_s)(I - i_s)$ (24)

$$P'' = EI - E\,i_s + e_s\,I - e_s i_s \qquad (25)$$

The deviation of P' and P'' from the power at the point of tangency, P, can be found by:

$$\Delta P' = -E\, i_s + e_s\, I + e_s i_s \qquad (26)$$

$$\Delta P'' = E\, i_s - e_s i_s + e_s\, i_s \qquad (27)$$

and since $E = RI$ and $e_s = R\, i_s$:

$$\Delta P' = -RI\, i_s + R\, i_s\, I + R\, i_s^2 \qquad (28)$$

$$\Delta P'' = RI\, i_s - R\, i_s\, I + R\, i_s^2 \qquad (29)$$

and since the quiescent point is the point of tangency of the load line and the constant power hyperbole:

$$\Delta P' = \Delta P'' = R\, i_s^2 = \frac{e_s^2}{R} \qquad (30)$$

and for a given e_s, ΔP increases with a decreasing R.

Plotting power along the load line versus voltage along the load line, a curve such as shown in Figure 84 results.

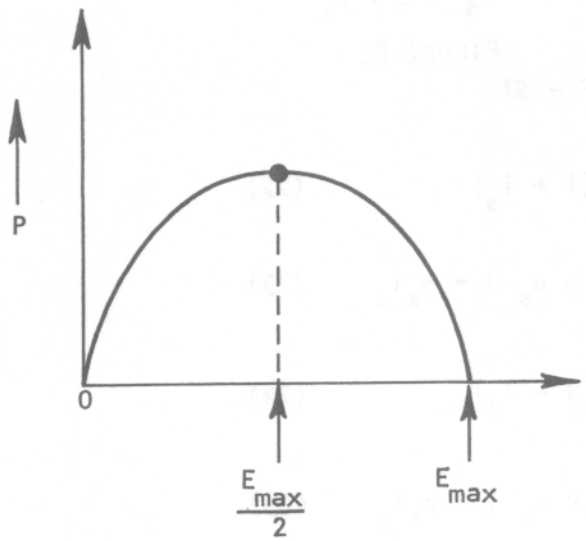


FIGURE 84

Note in Figure 84 that for a reasonable given value of e_s, the lowest ΔP will occur when the point of tangency is selected as the quiescent point.

Relating the foregoing discussion to a transistor collector family of curves, E_{max} is the total d-c supply voltage in series with the transistor. Minimum power change for a given e_s will occur when the quiescent operating point is selected at one-half the supply voltage for a given load line. This establishes the quiescent point at the point of tangency of the load line and a constant power hyperbole.

External compensation can be employed to maintain the quiescent operating point at the point of tangency with changes in surrounding air temperature. This can involve synthesized constant current sources, devices with opposing temperature coefficients of voltage or resistance, etc.

This discussion is aimed at internally generated temperature changes as a result of applied signal; therefore, most forms of external compensation will simply be accepted for now.

The opposition offered in the path of heat transfer from the junction to the surrounding air is related, analogically, to electrical resistance and is given in °C/watt (covered in Volumes 3 and 6). Power dissipation at the junction is related analogically to electrical current and temperature to electrical voltage. Therefore:

$$T_J = \Theta_{JA} P_D + T_A \qquad (31)$$

Where: T_J = junction temperature, °C

Θ_{JA} = total thermal resistance, °C/watt

P_D = junction power dissipation, watts

T_A = surrounding air or ambient temperature

Assuming that ΔP is a long term change, we might also state that:

$$T_J = P_D \Theta_{JA} \qquad (32)$$

or the change in junction temperature is directly proportional to the change in junction power dissipation. Since the relationship of current and voltage to temperature in a semiconductor is an exponential relationship, minimum change in power dissipation for a given signal voltage, e_s, is of prime concern.

When dealing with steady state power dissipation, the thermal to electrical analogy previously discussed is sufficient. When dealing with transients, pulses, etc., a thermal capacitance given in watt-sec/°C is assumed to be in parallel with total thermal resistance and any temperature change at the junction as a result of power dissipation occurs on an exponential (covered in Volume 6). The product of thermal capacitance (watt-sec/°C) and thermal resistance (°C/W) is time (τ in seconds). If a change in power dissipation occurs at t_o, the junction temperature at t_1 can be found by:

$$T_{J\ (t_1)} = T_{J\ (t_o)} + \Delta P_D\ \Theta_{JA}\ \epsilon^{-\frac{t_1 - t_o}{\tau}} \qquad (33)$$

where: $T_{J\ (t_1)}$ = the junction temperature at t_1

$T_{J\ (t_o)}$ = the junction temperature at t_o

ΔP_D = change in power dissipation

Θ_{JA} = total thermal resistance

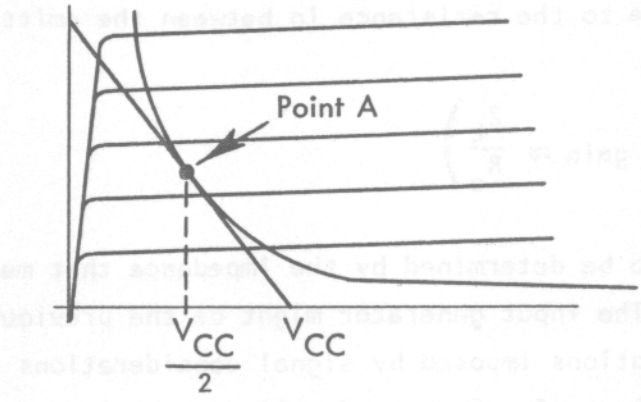
τ = the product of thermal capacity and thermal resistance

In transistorized d-c amplifiers, the effects of change in power dissipation with applied signal can be minimized by operating push-pull or differentially with both transistors quiescently at the point of tangency with a constant power hyperbole.

External compensation such as a synthesized constant current source supplying the transistors can be used to insure that the operating point is stable with changes in surrounding air temperature.

If the output is taken between the two transistors, internally generated temperature changes will tend to cancel. The reason is obvious because the transistors will

always have the same power dissipation (assuming identical transistors) as shown in Figure 85. Note that the transistor is dissipating maximum power for its load line when the quiescent operating point is selected as the point of tangency with a constant power hyperbole.



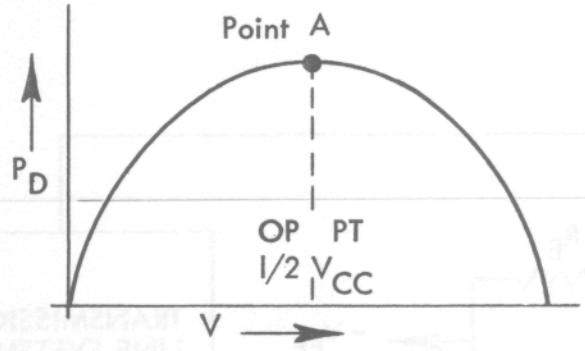


FIGURE 85

Input signals, either differential or push-pull, with equal magnitudes will result in both transistors stepping to a lower and identical point of power dissipation. If the transistors are perfectly matched and all conditions are ideal, the net change between the transistors is zero.

If two identical transistors are operated in a differential or push-pull configuration with a d-c load line and operating point shown in Figure 85, a step input of long duration will cause both transistors to step to a lower power dissipation and cool by the same amount giving no net d-c drift. The aim in design is evident. Two transistors in a push-pull or differential configuration, operating with their

d-c load line tangent to the same constant power hyperbole and dissipating maximum power for their load line at the static operating point.

This sounds simple at first, but consider the situation where a common emitter configuration has the maximum collector load impedance set by risetime requirements. The ratio of the load impedance to the resistance in between the emitters set by the gain requirements.

$$\left(\text{voltage gain} \approx \frac{Z_L}{R_e}\right)$$

The emitter resistance can also be determined by the impedance that must be shown the input driving generator. The input generator might be the previous stage, a transmission line, etc. Limitations imposed by signal considerations can make it almost impossible to select values of emitter and collector resistances that will satisfy the optimum thermal condition.

Consider the circuit in Figure 86.

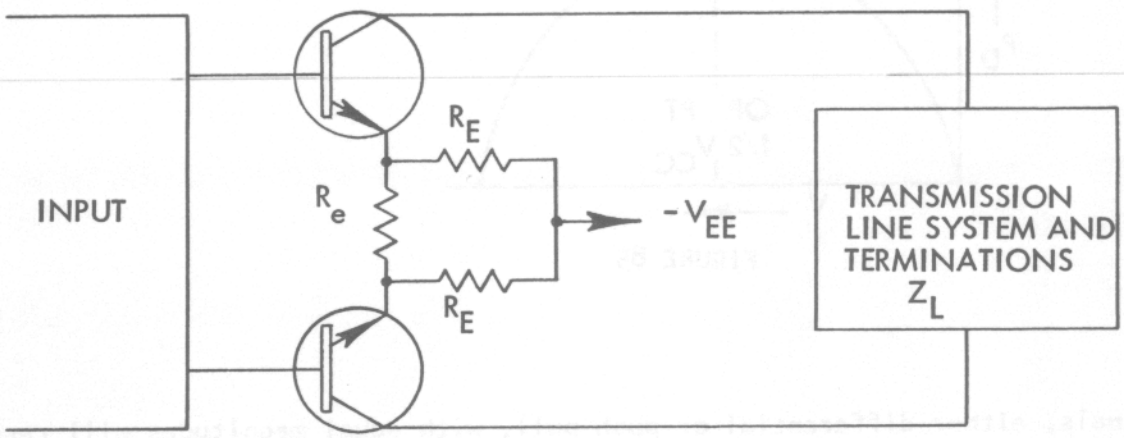


FIGURE 86

The transistors in Figure 86 must work into the transmission lines and amplify the signal with a flat response from d-c to some high frequency. The value of Z_L is set by the transmission lines and their terminations. The gain considerations are approximately set by the ratio of Z_L to the emitter resistance. The resistance in the emitter circuit determines the impedance shown the preceding stage or input generator and also the gain of the amplifier.

The approximate input resistance at the base can be determined by:

$$r_{in} \approx (r_e + R_e)\ (\beta + 1)$$

where r_{in} is the dynamic resistance seen at the base terminal, R_e is the external resistance in the emitter signal path, and r_e is the transistor's dynamic emitter resistance.

$$r_e \approx \frac{KT}{qI_E} \approx \frac{26mv}{I_E} \approx \frac{26}{I_{E(ma)}}$$ at 300°K or 27°C (discussed earlier in this volume)

The problem is establishing the d-c load line tangent to a constant power hyperbole with the operating point established for maximum power dissipation on the load line at the static operating point. The question generally is, if more series resistance is needed, where do we put it? If resistance is added to the collector circuit, the gain changes, risetime suffers, and the transmission system is no longer terminated. If the resistance is added to the emitter, the static current changes (assuming the base voltage is set by the input circuitry), and the input impedance changes.

The answer lies in adding a series resistance between the collector and the circuit it is driving. The added resistor simply becomes part of the output resistance of the transistor and has little effect on the gain-risetime considerations at the middle frequencies. This allows design for optimum thermal considerations while maintaining optimum signal considerations.

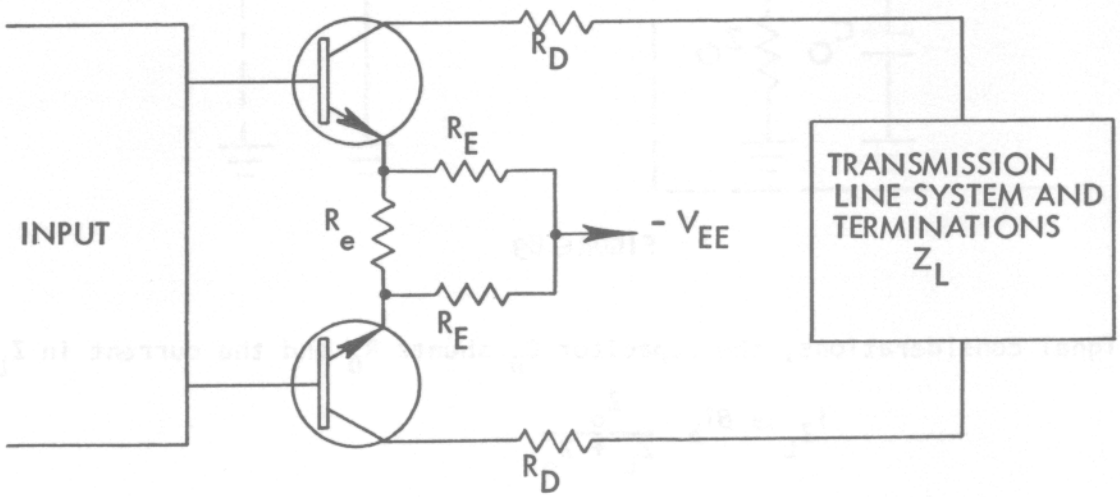


FIGURE 87

Figure 87 illustrates the addition of the resistance R_D to establish the d-c load line tangent to a constant power hyperbole. The output circuit of the transistor, with and without R_D, is shown in Figure 88.

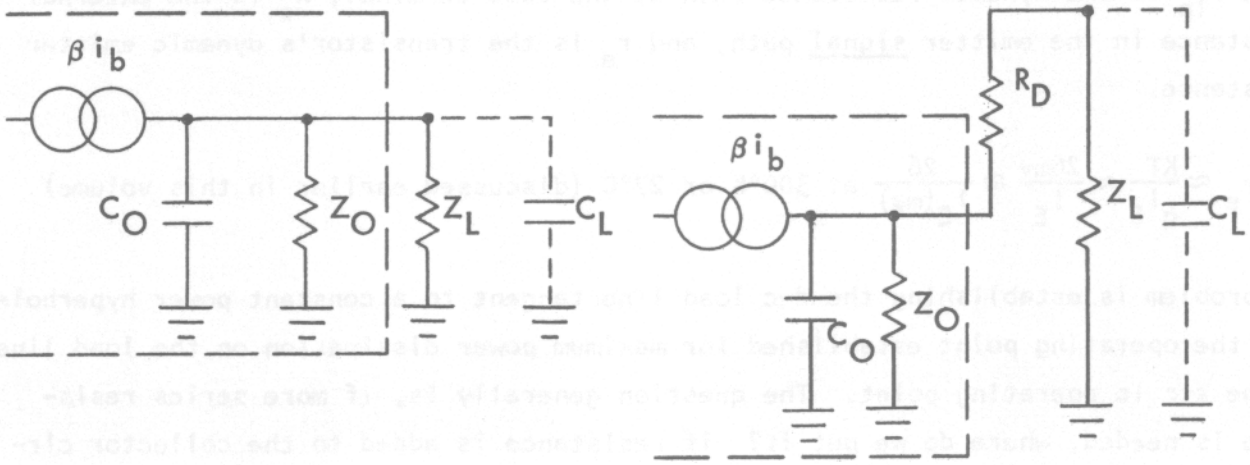


FIGURE 88

For high frequency considerations, a capacitor is placed in shunt with R_D to tie the output capacitance of the transistor to the load capacitance and the equivalent output circuit becomes:

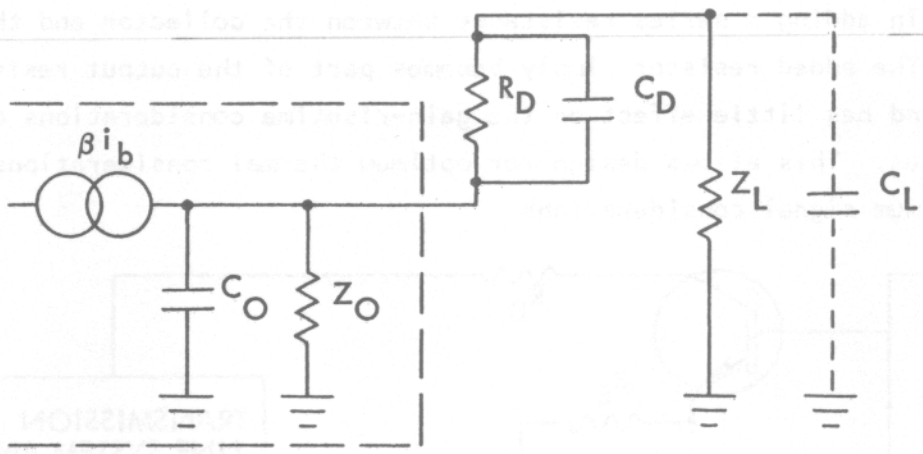


FIGURE 89

For a-c signal considerations, the capacitor C_D shunts R_D and the current in Z_L is:

$$i_{Z_L} \approx \beta i_b \frac{Z_o}{Z_L + Z_o}$$

At d-c, the generator βI_B sees a different configuration, since R_D is not by-passed

and the current in Z_L is:

$$I_{Z_L} \approx \beta I_B \frac{Z_o}{Z_o + Z_L + R_D}$$

If the Z_o of the transistors were infinite, there would be no problem. With a finite Z_o, the current in Z_L and hence the gain and output voltage will be different at d-c.

Since the gain is different at a-c and d-c, a step input of long duration results in a distorted output such as shown in Figure 90.

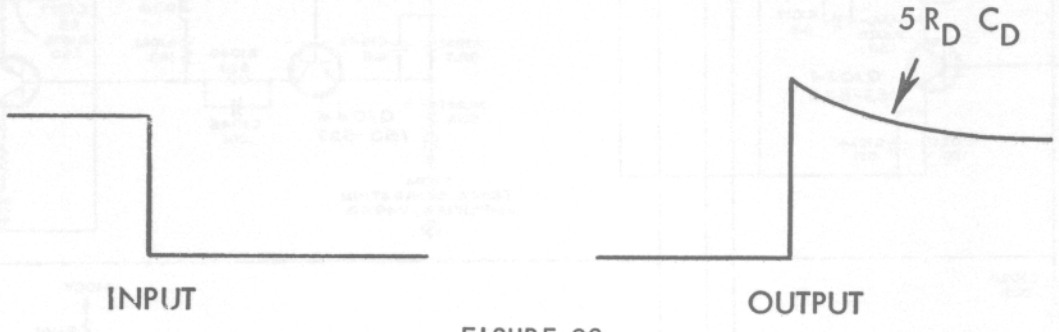


FIGURE 90

The output following the initial transition will decrease on a 5 RC exponential set by the $R_D C_D$ time constant. This is not too much of an obstacle because another time constant can be added in the circuit to compensate, and both signal and thermal considerations will be compensated.

Of course, the optimum situation occurs when $R_L + R_E = \frac{V_{CE}}{I_E}$ and no R_D is needed. If R_D is required, the formula $R_D \approx \left(\frac{V_{CC}}{2I_E}\right) - R_L - R_E$ can be used if β is assumed to be infinity. This simply says that one-half the static power is dissipated in the resistors for optimum thermal considerations, and I_E is assumed to be equal to I_C. If this is true, the static resistance of the transistor must equal the total series to I_C. If this is true, the static resistance of the transistor must equal the total series resistance, and there will be 1/2 V_{CC} across the transistor. The static resistance of the transistor is given by:

$$R_{T_{STATIC}} \approx \frac{V_{CE}}{I_E} \approx 1/2 \frac{V_{CC}}{I_E} \approx \frac{V_{CC}}{2I_E}$$

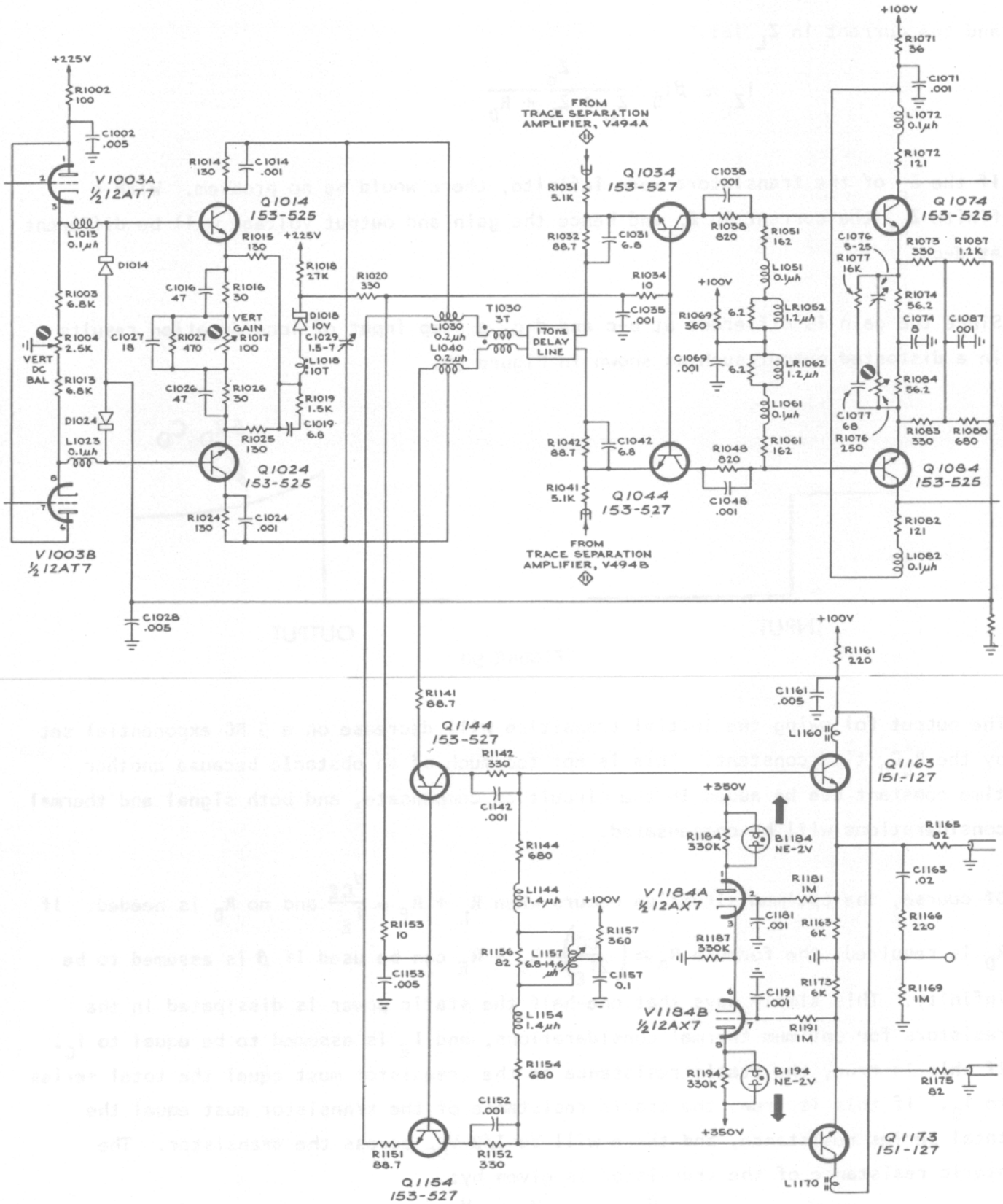

+225V
R1002 100
C1002 .005
V1003A ½12AT7
R1014 130
C1014 .001
Q1014 153-525
R1015 130
+225V
R1018 2.7K
D1018 10V
C1029 1.5-7
L1018 10T
R1020 330
C1016 47
R1016 30
VERT GAIN R1017 100
C1027 18
R1027 470
C1026 47
R1026 30
R1019 1.5K
C1019 6.8
R1025 130
L1015 0.1μh
D1014
R1003 6.8K
R1004 2.5K
VERT DC BAL
R1013 6.8K
D1024
L1023 0.1μh
Q1024 153-525
R1024 130
C1024 .001
V1003B ½12AT7
C1028 .005
L1030 0.2μh
L1040 0.2μh
T1030 3T
170ns DELAY LINE
FROM TRACE SEPARATION AMPLIFIER, V494A
FROM TRACE SEPARATION AMPLIFIER, V494B
R1051 5.1K
Q1034 153-527
C1038 .001
R1038 820
R1032 88.7
C1031 6.8
R1034 10
C1035 .001
R1042 88.7
C1042 6.8
R1041 5.1K
Q1044 153-527
R1048 820
C1048 .001
+100V
R1069 360
6.2
LR1052 1.2μh
C1069 .001
LR1062 1.2μh
L1061 0.1μh
R1051 162
L1051 0.1μh
R1061 162
+100V
R1071 36
C1071 .001
L1072 0.1μh
R1072 121
Q1074 153-525
C1076 5-25
R1077 16K
R1073 330
R1087 1.1K
R1074 56.2
C1074 8
C1087 .001
R1084 56.2
C1077 68
R1076 250
R1083 330
R1086 680
Q1084 153-525
R1082 121
L1082 0.1μh
+100V
R1161 220
C1161 .005
L1160
Q1163 151-127
R1141 88.7
Q1144 153-527
R1142 330
C1142 .001
+350V
R1184 330K
B1184 NE-2V
R1144 680
L1144 1.4μh
+100V
V1184A ½12AX7
R1181 1M
C1181 .001
R1163 6K
R1187 330K
R1157 360
R1156 82
L1157 6.8-14.6 μh
C1157 0.1
R1153 10
C1153 .005
C1191 .001
R1173 6K
V1184B ½12AX7
R1191 1M
L1154 1.4μh
R1154 680
R1194 330K
B1194 NE-2V
+350V
C1152 .001
R1151 88.7
R1152 330
Q1154 153-527
Q1173 151-127
L1170
R1165 82
C1163 .02
R1166 220
R1169 1M
R1175 82

FIGURE 91

$R_{T_{STATIC}}$ must equal R_{series} total where R_{series} total is:

$$R_{series} = R_D + R_L + R_E$$

and

$$R_{series} = R_{T_{STATIC}}$$

so

$$\frac{V_{CC}}{2I_E} = R_D + R_L + R_E$$

therefore

$$R_D = \left(\frac{V_{CC}}{2I_E}\right) - R_L - R_E$$

The time constant of R_D C_C changing the gain at the low frequencies can be compensated anywhere in the amplifier with an opposing time constant equal to R_D C_C. Normally, there are other compensations involved such as transmission line compensation, high frequency peaking, etc. These compensations can all be accomplished with variable resistive and reactive components, perhaps between the emitters of two of the transistors in the push-pull configuration. When the amplifier response is adjusted for optimum transient response with minimum overshoot and d-c drift with a good, fast rising square wave applied to the input, the system is said to have a Gaussian response. In this way, the time constant of R_D C_C and the other compensations can be made compatible. A typical circuit is shown in Figure 91.

The circuit just discussed is similar to the push-pull configuration of Q1014 and Q1024 in Figure 91. R1014 and R1024 are examples of the addition of R_D to optimize the thermal considerations. Capacitors C1014 and C1024 are the capacitors referred to as C_D in the preceding example.

Resistors R1038, R1048, R1142, and R1152 are a similar application with the added task of maintaining the transistor pair, Q1034 and Q1044, on the same constant power hyperbole as transistor pair, Q1144 and Q1154.

In the circuit configuration in Figure 91, the impedance of L1030 and L1040 is 186Ω (93Ω per side). Resistors R1032, R1042, R1141, and R1151 and the input resis-

tance of the common base transistors terminate the ends of L1030 and L1040. Rise-time considerations limit the collector loads and the R_D's place the proper load line tangent to the same constant power hyperbole for transistors Q1034, Q1044, Q1144, and Q1154.

Note the variable resistor and capacitor, R1076 and R1077. These allow the adjustment for optimum transient response. These, of course, work in conjunction with other resistive and reactive components in the amplifier. These circuit configurations are used in the vertical amplifier of the Tektronix Type 547 oscilloscope.

THE TRANSISTORIZED LONG-TAIL:

If extreme environmental conditions are going to be encountered, or if only very incremental changes can be allowed in the d-c levels on the transistor with changes in temperature or power dissipation, a very efficient synthesized constant current source must be used to maintain the d-c stability. A very high supply voltage returned through a very large long-tail resistor can be used to accomplish this. In many cases, this is not feasible; however, a circuit such as shown in Figure 92 can be used.

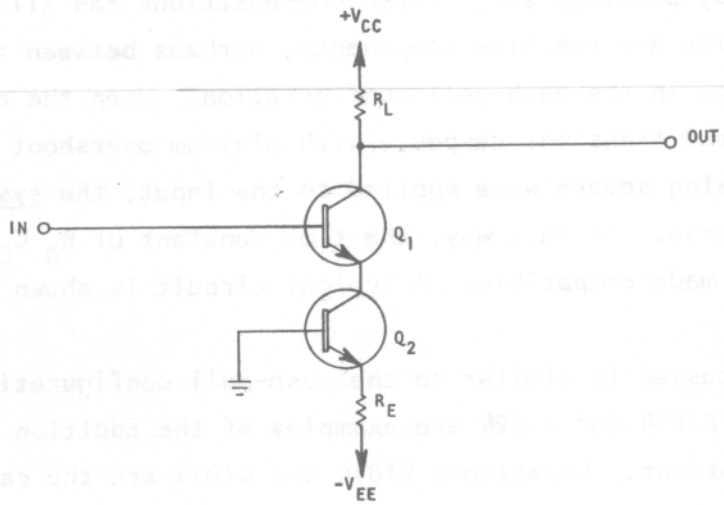


FIGURE 92

Figure 92 illustrates a transistor with a second transistor serving in the long-tailed circuit in its emitter. Notice the base of the long-tail transistor Q_2 is returned to ground. Therefore, its emitter is also going to be clamped near ground. The changes in the current in transistor Q_1 will have to be supplied by transistor Q_2. The voltage that the emitter of Q_2 is returned to and the size of

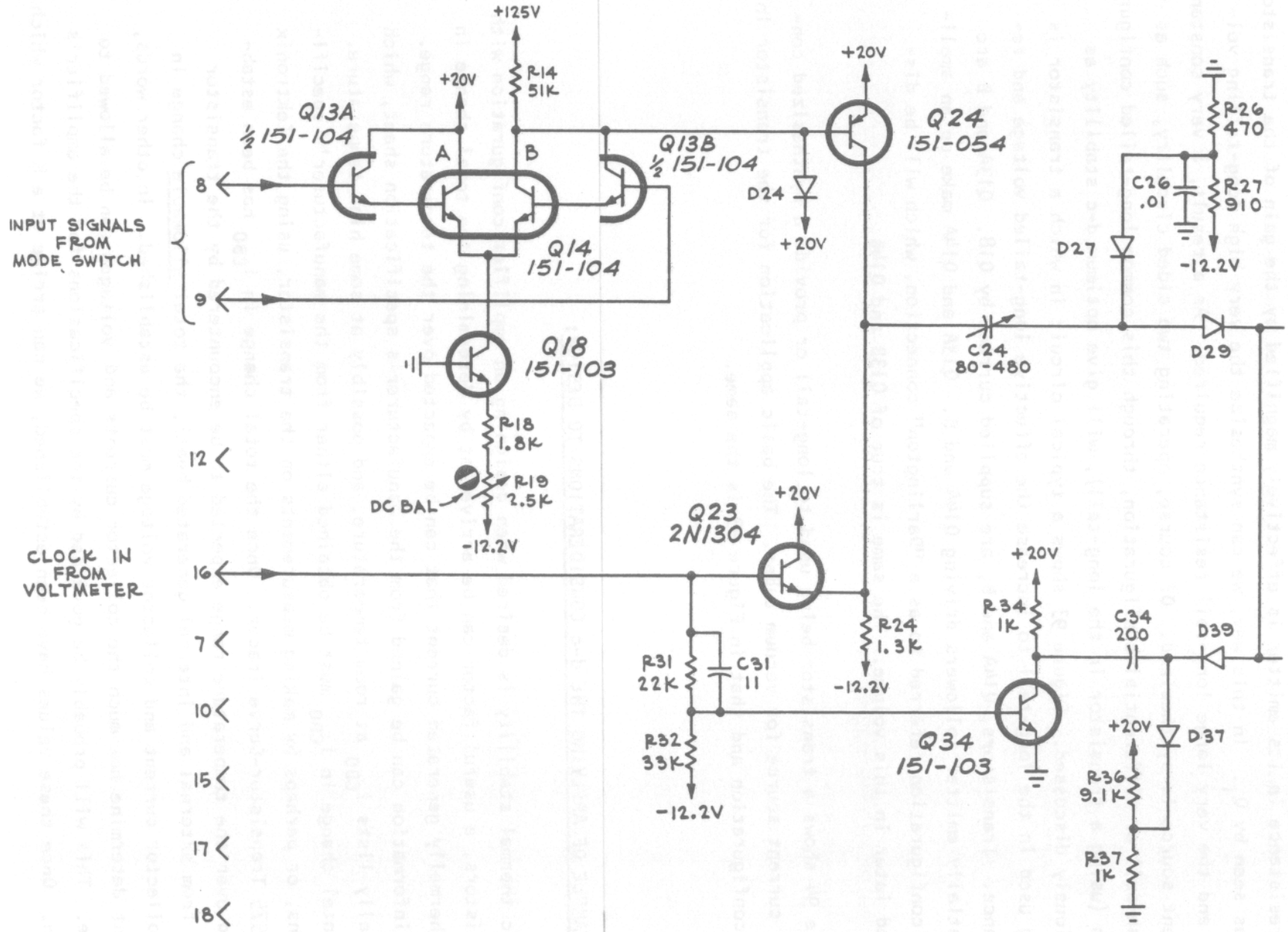

+125V
R14
51K
+20V
Q13A
½ 151-104
A
B
Q13B
½ 151-104
Q24
151-054
+20V
D24
+20V
R26
470
C26
.01
R27
910
D27
-12.2V
INPUT SIGNALS
FROM
MODE SWITCH
8
9
Q14
151-104
Q18
151-103
C24
80-480
D29
R18
1.8K
12
DC BAL
R19
2.5K
-12.2V
+20V
Q23
2N1304
CLOCK IN
FROM
VOLTMETER
16
7
10
15
17
18
R24
1.3K
-12.2V
+20V
R34
1K
C34
200
D39
R31
22K
C31
11
R32
33K
-12.2V
Q34
151-103
+20V
D37
R36
9.1K
R37
1K

FIGURE 93

the resistance in its emitter is effectively magnified by the gain of the transistor Q_2, as seen by Q_1. In this way, we can synthesize the very high long-tailing voltage and the very large long-tail resistance required. As a result, a very constant current source is synthesized. Of course, operating two sided circuitry, such as a push-pull or differential configuration, through this common long-tailed configuration (using a transistor in the long-tail), will give optimum d-c stability as previously discussed. Figure 93 shows a typical circuit in which a transistor is being used in the long-tail to increase the effective long-tailed voltage and resistance. Transistors, Q14A and B, are supplied current by Q18. Q13A and B are essentially emitter followers driving Q14A and B. Q13A and Q14A make up an amplifier configuration referred to as a "Darlington" connection, which will be discussed later in this volume. The same is true of Q13B and Q14B.

Figure 94 shows a transistor being used to long-tail or provide a synthesized constant current source for vacuum tubes. The basic application for the transistor in this configuration and that in Figure 93 is the same.

AN EXAMPLE OF APPLYING THE d-c CONSIDERATIONS TO DESIGN:

If d-c thermal stability is desired when designing an amplifier configuration with transistors, a useful factor can be arrived at by determining the total change in the thermally generated current that can be expected over the temperature range. This information can be gained from the manufacturer's specification sheet, which generally lists I_{CBO} at room temperature, and possibly at some high temperature. The total change in I_{CBO} must be obtained either from the manufacturer's specifications, or perhaps by making measurements on the transistor, using the Tektronix Type 575 Transistor-Curve Tracer. Once the total change in I_{CBO} has been established over the temperature range expected to be encountered by the transistor (both from external and internal generated heat), the total allowable change in the collector current and collector voltage must be established. In other words, we must determine how much the collector currents and voltages can be allowed to change. This will probably be governed by the specifications for the amplifier's design. Once these values have been established, we can arrive at a K factor which

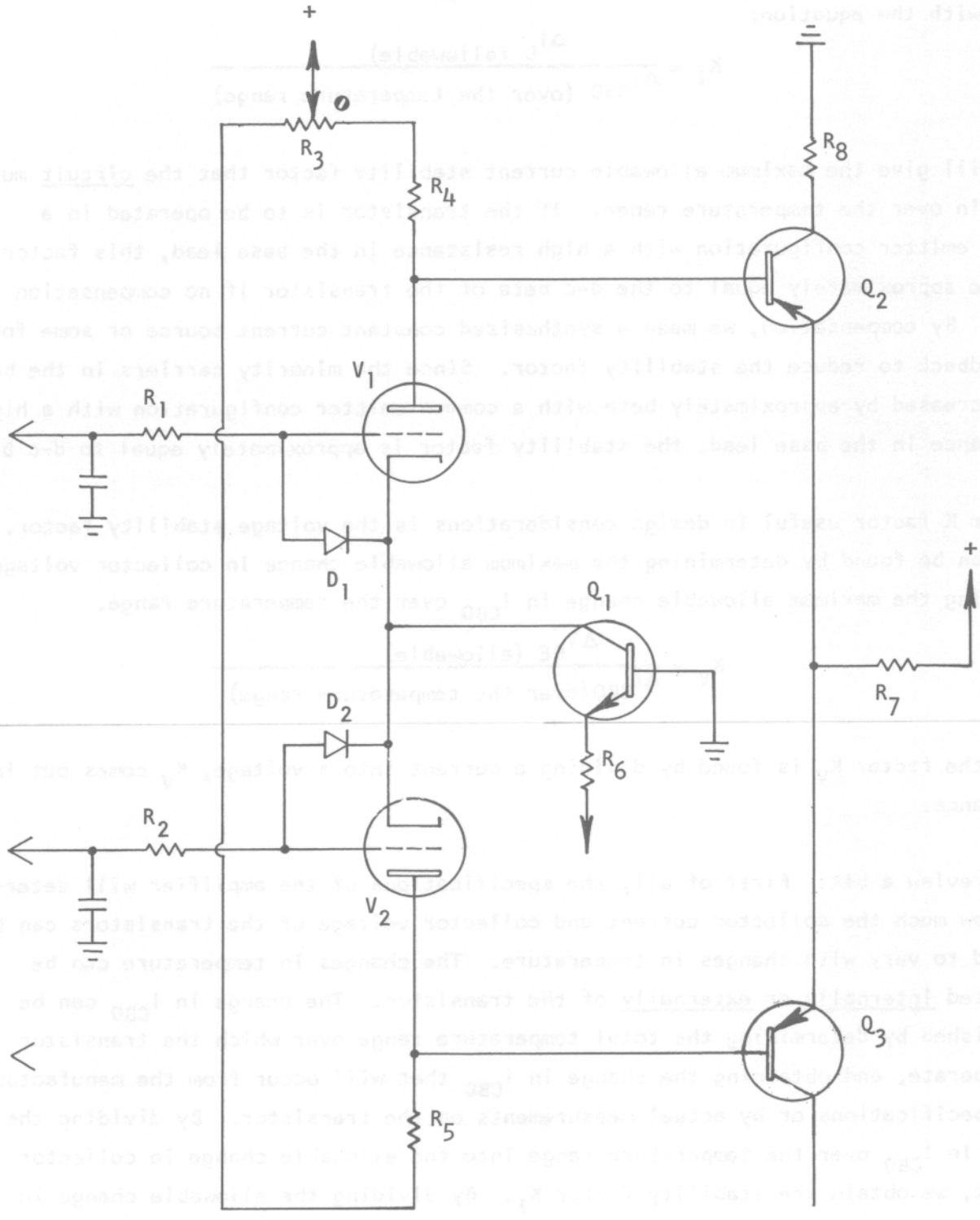


FIGURE 94

will be useful in the design. The K factor or stability factor for current can be found with the equation:

$$K_I = \frac{\Delta I_C \text{ (allowable)}}{\Delta I_{CBO} \text{ (over the temperature range)}}$$

This will give the maximum allowable current stability factor that the circuit must maintain over the temperature range. If the transistor is to be operated in a common emitter configuration with a high resistance in the base lead, this factor will be approximately equal to the d-c beta of the transistor if no compensation is added. By compensation, we mean a synthesized constant current source or some form of feedback to reduce the stability factor. Since the minority carriers in the base are increased by approximately beta with a common emitter configuration with a high resistance in the base lead, the stability factor is approximately equal to d-c beta.

Another K factor useful in design considerations is the voltage stability factor. This can be found by determining the maximum allowable change in collector voltage and using the maximum allowable change in I_{CBO} over the temperature range.

$$K_V = \frac{\Delta V_{CE} \text{ (allowable)}}{\Delta I_{CBO} \text{ (over the temperature range)}}$$

Since the factor K_V is found by dividing a current into a voltage, K_V comes out in resistance.

Let's review a bit. First of all, the specifications of the amplifier will determine how much the collector current and collector voltage of the transistors can be allowed to vary with changes in temperature. The changes in temperature can be generated internally or externally of the transistor. The change in I_{CBO} can be established by determining the total temperature range over which the transistor must operate, and obtaining the change in I_{CBO} that will occur from the manufacturer's specifications or by actual measurements on the transistor. By dividing the change in I_{CBO} over the temperature range into the allowable change in collector current, we obtain the stability factor K_I. By dividing the allowable change in collector voltage by the change in I_{CBO} over temperature range, we obtain the stability factor K_V. We might use these stability factors in an exact analysis or design of an amplifier configuration but more commonly, to insure that speci-

fications are met, the stability factors are reduced to allow a safety factor and approximate design approaches utilized in the design of the amplifier itself. To give an example of incorporating thermal stability in an amplifier design, we will use an example of an approximate design approach to a low frequency, audio amplifier. This does not indicate the way, but a simplified approximate design approach.

SELECTING A TRANSISTOR FOR THE AUDIO AMPLIFIER:

When selecting a transistor for design of an audio amplifier circuit, the following parameters should be well defined to insure good design:

h_{FE} (d-c current gain) - the variations in this parameter should be specified to aid in controlling the operating point. d-c feedback is sometimes used to minimize the effects of variations in this parameter.

h_{fe} (small signal, a-c current gain) - variations in this parameter should be specified for use in insuring the minimum variations in amplifier gain. a-c feedback is sometimes added to minimize the effects of variations in this parameter.

I_{CBO} (current, collector to base, with the emitter d-c open circuited) - the maximum value should be stated to aid in thermal stabilization. It is helpful when this current is given at room temperature and also at some high temperature. A chart is sometimes given to allow the calculation of I_{CBO} at different temperatures.

N_F (noise figure) - maximum value should be specified

$f_{h_{fe}}$ or f_e (frequency at which h_{fe} is reduced to 0.707 of its low frequency value - 3db down point) - minimum frequency should be specified to insure proper frequency response. This frequency should be high enough to prevent phase shift in any feedback circuit. For common emitter design considerations, the frequency parameter f_T is given by most manufacturers and gives information on the frequency characteristics of the transistor beyond $f_{h_{fe}}$ and f_e.

f_T (the frequency at which low frequency h_{fe} equals unity) - the minimum value should be specified to insure proper frequency response. f_T is the gain bandwidth product of the amplifier can be used to determine the gain at frequencies beyond the frequency $f_{h_{fe}}$.

B_{VCEO} (maximum collector d-c voltage) - the minimum value should be specified.

$V_{CE(sat)}$ (collector to emitter voltage at saturation for a given value of I_B and I_C) - the maximum value should be specified.

$P_{D(max)}$ (maximum collector power dissipation) - the minimum value should be specified. It is also useful if the value of maximum collector power dissipation at a higher ambient temperature is given. If it is not given, then the value of thermal resistance for the transistor should be given. The value of thermal resistance will be given for the transistor from junction to case or junction to ambient, depending on the application, and can be used to determine the maximum power dissipation at different temperatures.

For a safety margin in design, it is generally practiced to allow the following safety margins in the parameters given by the manufacturer. This assures that the variations of parameters in a batch or the aging of a transistor and component parts will be compensated for.

B_{VCEO} - Assume 75% of the value given by the manufacturer and limit peak audio swing below this point. If transformer coupling is to be used, limit the supply voltage to about 40% of the maximum value given by the manufacturer.

I_{CBO} - Assume twice the maximum specified by the manufacturer at the maximum temperature and voltage. (If this is not done, then a reduction in the K factors for current and voltage stability can be applied.)

h_{FE} and h_{fe} - Assume a variation between 50% of the minimum value specified and 200% of the maximum value specified for both parameters.

$P_{D(max)}$ - Assume approximately 75% of the specified maximum power rating at maximum expected operating temperature.

$f_{h_{fe}}$ or f_{α_e} - Assume 50% of the minimum frequency specified by the manufacturer.

f_T - Assume 75% of the minimum frequency specified by the manufacturer.

$V_{CE(sat)}$ - Assume 200% of the maximum value specified.

It should be brought out here that these safety margins do not apply to transistors being supplied by the manufacturer and guaranteed to meet certain specifications, etc. Once the specifications of the amplifier have been established, and after the transistor is selected, the initial design approximations can be made, and the proper operating point and load line selected. A high power amplifier, single ended, would probably have its load line selected so that voltage and current limiting occured at the same input level. For low distortion amplifiers, the a-c signal swing is limited to about one-half the supply voltage and the operating point selected for linear transfer characteristics (i.e., signal swing along the selected load line is linear).

Keeping the input drive as constant a current course as possible (high impedance drive) will reduce distortion due to the input resistance variations with larger input signals. Output load matching is best for signal power gain, but a low load is needed for maximum power output. The output load resistance must be selected for required power output with sufficient gain.

In push-pull amplifiers where temperature sensitive components are not used for thermal stability, it is sometimes necessary to use separate emitter resistances for proper feedback.

Temperature sensitive components, negative feedback or perhaps synthesizing a constant current source can be used for thermal stability, and a-c signal negative feedback can be used to reduce distortion. For transformer coupled loads, it is safe to assume only about 30% efficiency.

Transformer coupling gives a good thermal stability factor due to the low d-c resistance of the winding placed in the base circuit. This gives the thermally generated minority carriers a low resistance d-c path and reduces the magnification of the leakage current. If a transformer is used as a load resistance in the collector circuit, its d-c resistance does not cause large changes in the collector voltage for changes in collector current over the temperature range.

Let's assume that for this example we are going to design a low level audio amplifier.

Assume that we have available an input signal current of 0.5μa peak, and we require an output signal voltage of 1v peak. We want to limit ourselves to a single d-c supply voltage, and we will expect temperature variations from 10°C to 70°C. In order that we might hold the specifications for the amplifier that we have just determined, we would probably select a configuration, such as shown in Figure 95.

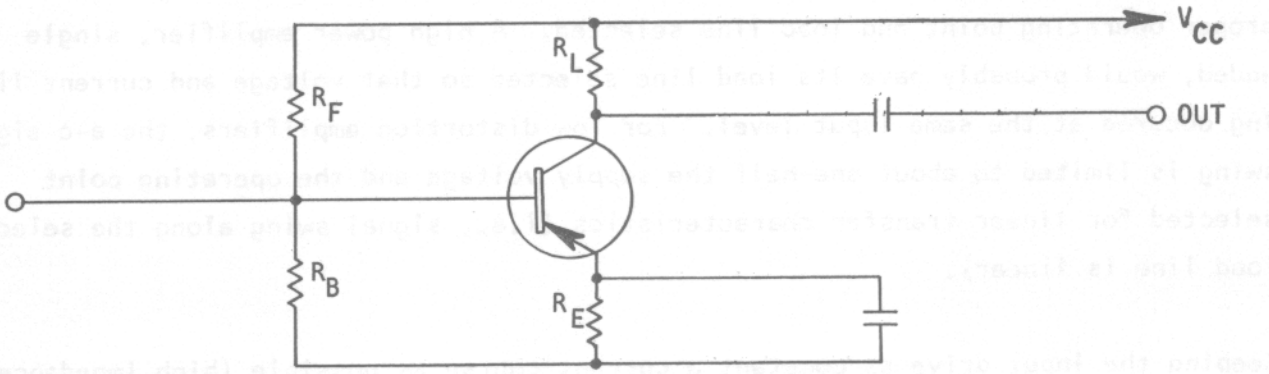


FIGURE 95

Let's assume we have selected a transistor with the following parameters at an emitter current of 1ma, and 25°C.

$h_{ie} = 2.1 \times 10^{3}\Omega$

$h_{re} = 1.8 \times 10^{-5}$

$h_{fe} = 50$

$h_{oe} = 4.8 \times 10^{-7}$mhos

$\Theta_{JA} = 0.5$°C/milliwatt

Once the transistor has been selected and the configuration decided upon, the design can be started with an estimate of the number of stages needed. Since the transistor must operate over a range of temperatures, the circuit must be stabilized for d-c operating point. The configuration we have selected will allow us to design in thermal stabilization as long as we take it into account in the initial design. The stabilization due to the circuit configuration we have selected will result in a loss of the signal at the input of the transistor. This can be easily seen be-

cause R_B and R_F in Figure 95 will certainly shunt some of the signal current. It is safe to assume about 50% loss in the estimations for determining the number of stages required. The signal entering the transistor is 0.25μa. h_{fe} = 50 and 0.25μa x 50 is approximately 12.5μa peak signal current in the collector circuit. An a-c signal of 1v is needed in the collector and, assuming an a-c collector current of 12.5μa (just approximated), Ohm's Law says that it would require an 80,000Ω collector load resistor to deliver a 1v peak signal in the output.

$$\left(\frac{1v}{12.5\mu a} = 80{,}000\Omega\right)$$

Using an 80,000Ω resistor in the collector circuit would require a large supply voltage and limit the frequency response. Adding another stage, and again assuming a 50% loss at the input of the second transistor, the input signal is 6.25μa peak to the second transistor. With h_{fe} = 50, 6.25μa x 50 is approximately equal to 312.5μa peak a-c collector current for the second stage. With a 1v signal swing required, the collector load resistance will have to be:

$$\frac{1v}{312.5 \times 10^{-6}} = 3.3k\Omega$$

This is a more reasonable value for both supply voltage and frequency considerations and two stages will probably do the job.

Let's review this for a moment. First of all, after selecting the transistor and determining the configuration, we started with a design approximation to determine the number of stages needed. We simply used the input signal and required output signal to determine what size components would be required. We continued to increase the number of stages until a reasonable value of collector load resistor for supply voltage and frequency considerations could be realized.

Since the first stage will be concerned primarily with current gain to drive the second stage, a small a-c load resistance can be tolerated. This is fortunate as the collector load of the first stage will be shunted by the input resistance of the second transistor and its biasing resistors.

Since there is only a small current change in the first stage, the d-c operating point (I_E) can be established at a fairly low value. Selecting the operating point

of the first stage to be a low value will help to reduce the noise level in the transistor (the noise level in a transistor will be less at the lower quiescent currents). This will also establish the input resistance of the first stage at a higher level, improving the signal to noise ratio in the amplifier.

The second stage will have a larger current swing (we estimated around 312μa), and its input will be shunted by its biasing resistors and the load resistor of the previous stage. Establishing the static emitter current of the second stage at a higher value than that of the first stage will allow a larger current change in the second stage and reduce the input resistance. This will allow more of the signal current to enter the second transistor.

At this point, we would probably examine the characteristic curves supplied by the manufacturer, or possibly measure the transistor characteristics on the Type 575 Transistor-Curve Tracer, and establish quiescent d-c operating points for collector voltage and emitter current. We would also assure that the d-c or a-c signal load lines do not cross the maximum power hyperbole and exceed the power handling characteristics of the transistor at any expected ambient or operating temperature. Figure 96 and 97 show the Tektronix Type 575 Transistor-Curve Tracer being used to measure the hybrid parameters for a transistor. We might also use the characteristic curves in Figures 96 and 97 to determine the quiescent operating point for the first and second transistor. Recall that we are going to set the first stage operating at a fairly low operating current to reduce the noise level, and the second stage a little bit higher current, since it has to have a higher current swing. Let's assume that curves, such as shown in Figures 96 and 97, let us decide to set the operating point emitter current of the first stage at 0.5ma, and the operating emitter current of the second stage at 2ma at the normal operating or design center temperature. Now, we might measure the hybrid parameters using the 575 as outlined in Figures 96 and 97, or we might use the parameters specified by the manufacturer at 1ma. If we use the parameters given by the manufacturer at 1ma, we will have to modify the parameters for use at the static operating point that we have selected. For the first stage, we selected 0.5ma and the second stage 2ma, and neither of these operating points will allow us to use the parameters that are given at 1ma. We can modify the parameters by using curves as supplied by the manufacturer to modify their parameters for different emitter currents.

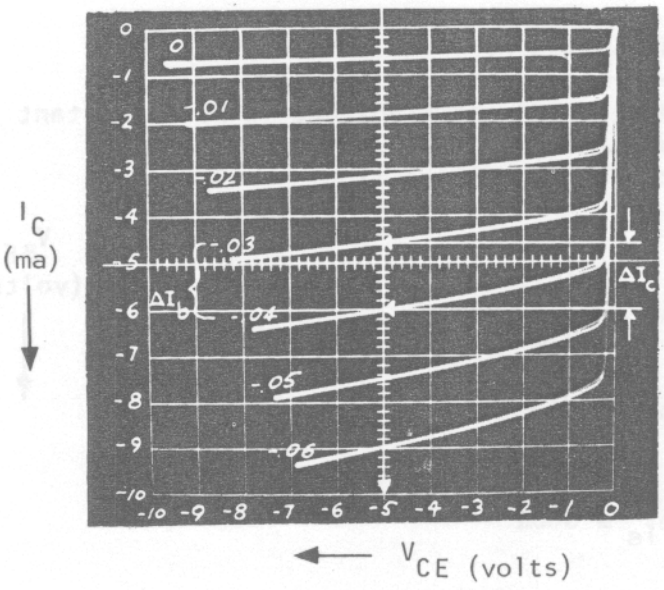
MEASURING h_{fe}:

Note: To hold collector voltage constant, the measurements are made along the 5V collector voltage line.

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}\Bigg|_{\Delta V_{CE} = 0}$$

$$h_{fe} = \frac{1.4\text{ma}}{10\mu\text{a}}$$

$$h_{fe} = 140$$



TEST SET-UP: TEKTRONIX TYPE 575 TRANSISTOR-CURVE TRACER
VERTICAL: COLLECTOR ma = 1ma/div
HORIZONTAL: COLLECTOR VOLTS = 1V/div
STEP SELECTOR: ma/step = 0.01ma/step
DISSIPATION LIMITING RESISTOR = 200Ω

MEASURING h_{oe}:

Note: To hold base current constant, the measurements are made along the 0.04ma base current curve.

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}\Bigg|_{\Delta I_B = 0}$$

$$h_{oe} = \frac{0.3\text{ma}}{2\text{V}}$$

$$h_{oe} = 0.00015\text{mhos}$$

$$h_{oe} = 150\mu\text{mhos}$$

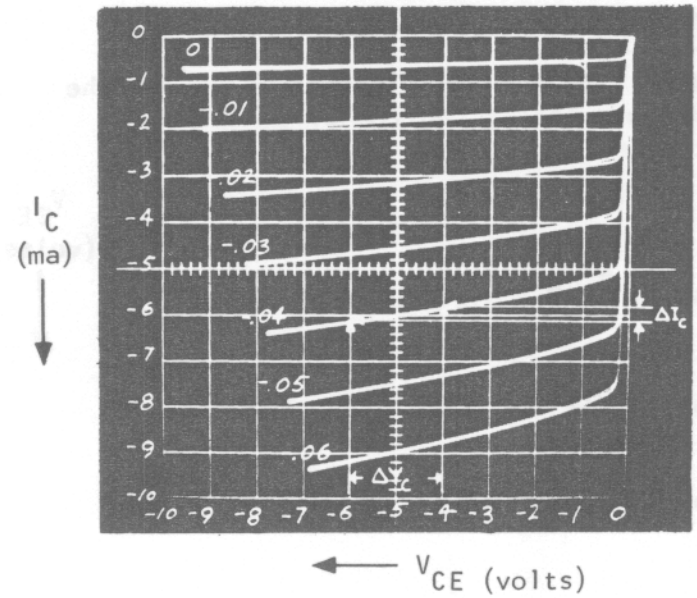


FIGURE 96

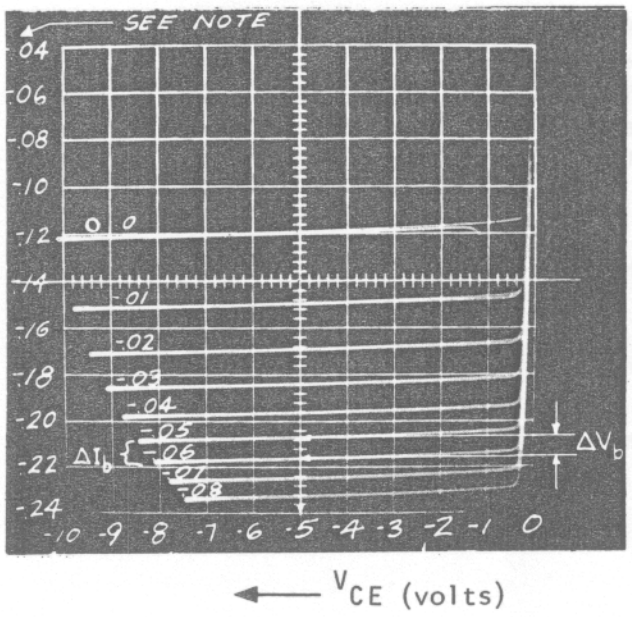
MEASURING h_{ie}:

Note: Collector voltage is held constant by making measurements along the 5V collector voltage line.

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \Bigg| \Delta V_{CE} = 0$$

$$h_{ie} = \frac{0.008V}{10\mu a}$$

$$h_{ie} = 800\Omega$$



TEST SET-UP: TEKTRONIX TYPE 575 TRANSISTOR-CURVE TRACER

VERTICAL: BASE VOLTS = 0.02V/div

HORIZONTAL: COLLECTOR VOLTS = 1V/div

STEP SELECTOR: BASE CURRENT = 0.01ma/step

DISSIPATING LIMITING RESISTOR = 200Ω

NOTE: VERTICAL POSITIONED UP TWO MAJOR DIVISIONS

MEASURING h_{re}:

Note: I_B is held constant by making the measurements along the 0.05ma base current curve.

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \Bigg| \Delta I_B = 0$$

$$h_{re} = \frac{0.002V}{4V}$$

$$h_{re} = 500 \times 10^{-6}$$

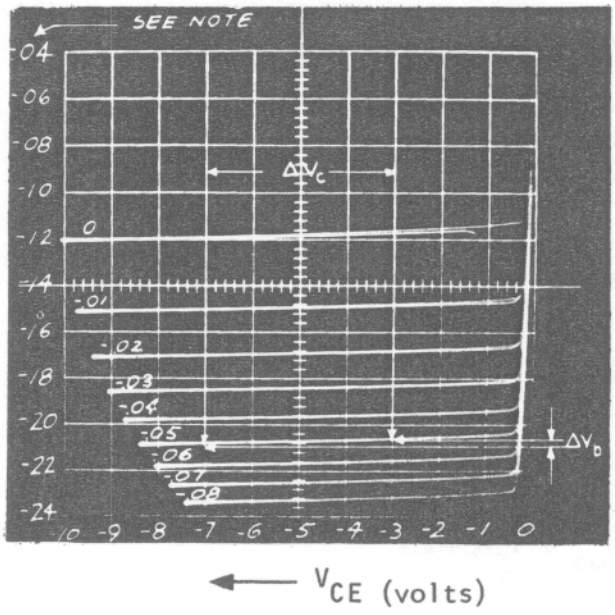


FIGURE 97

We might also use the following approximations which are fairly close. Assume that $\frac{1}{h_{ie}}$ and h_{oe} vary directly with the emitter current, and that the other parameters will remain fairly constant over this small range of emitter currents. h_{ie} of the first transistor will have to be modified by dividing 2100Ω (which is the h_{ie} given at 1ma) by the factor 0.5. This gives a value for h_{ie} of the first transistor of 4200Ω at an emitter current of 0.5ma. h_{ie} at 1ma is 2100Ω; operating point current is 0.5ma, or 0.5 times the current at which the parameter h_{ie} was given. Dividing h_{ie} by this factor gives h_{ie} at the new operating point current. The factor for the second stage is 2. I_E selected is twice the value of current at which the parameter was given. For the second stage, h_{ie} is approximately 2100Ω over 2, or 1050Ω. For initial design approximations, these parameters do not have to be exact and, therefore, we can use the approximations.

Keeping in mind that the input resistance of the second transistor will shunt the collector load of the first stage, we will have to assume an a-c load for the first stage of somewhat less than the input resistance of the second stage. This input resistance will also be shunted by the biasing resistors and by the load resistor for the first stage; therefore, we should assume a value below the input resistance of the second stage. Assuming 600Ω here will give an idea of the magnitude of the collector load and allow an approximate load line to be drawn on the collector family of curves for the transistor. This might be necessary to determine the maximum allowable change in collector current and collector voltage that can be allowed over the temperature range. These changes will have to be limited so that an applied signal will not cause the transistor to move into a non-linear region of its characteristics along the load line. Figure 98 shows a d-c load line and a signal load line constructed on a characteristic family of curves taken with the 575 Transistor-Curve Tracer. As temperature increases, the static operating point will move to a higher current point; therefore, the a-c load line will move to a different point of intersection with the d-c load line. It is possible with a significant increase in temperature for the a-c load line to move into an area of distortion. By an area of distortion, we mean an area where the applied signal will cause the transistor to give a non-linear result in the output circuit. Since we are designing a low level audio amplifier and we are going to use resistive-capacitive coupling, we won't be as concerned with the d-c levels as we might be if the amplifier were direct coupled. If the amplifier were direct coupled and it was necessary to amplify d-c signals, we would probably have to be a lot more

critical with the d-c operating point over the temperature range than when we are capacitive coupled. With direct coupling, any changes in the quiescent operating point represents a d-c signal to the following amplifier, and these changes are amplified. Any bias changes will appear as a signal to the following stage.

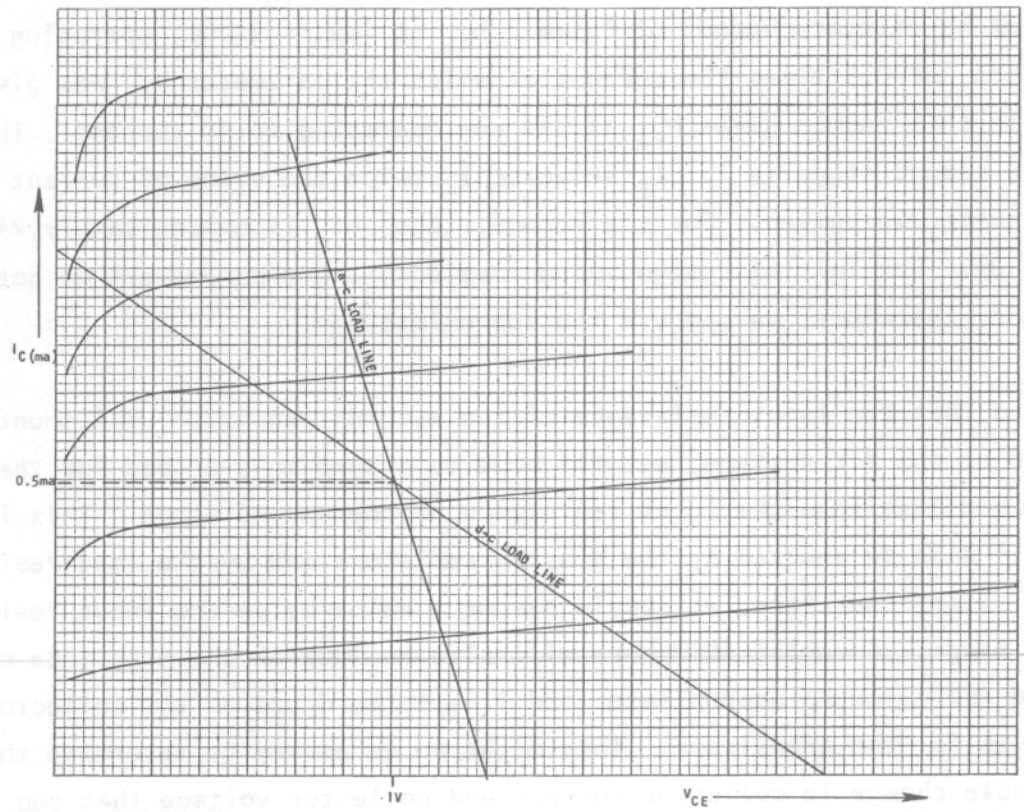


FIGURE 98

When we have an increase in temperature, the operating point moves up the d-c load line. The peak signal voltage and current changes will show how far it can move before distortion starts to occur. This will be the permissable shift in the operating point. From this, a maximum allowable change in collector current and collector voltage before distortion occurs can be determined. This allows calculation of the amount of d-c stability that must be incorporated in the circuit to compensate for changes in the thermally generated minority carrier current over the temperature range. The change in I_{CBO} over the temperature range can be calculated by determining the I_{CBO} at room temperature and at the maximum temperature that will be encountered. This can be done by taking the information from the manufacturer's specification sheets, or by measuring these changes using the 575 Transistor-Curve Tracer and a thermal probe. The maximum current stability factor can be found

by the formula:
$$K_{I(max)} = \frac{\Delta I_C \text{ (allowable)}}{\Delta I_{CBO} \text{ (over the temperature range)}}$$

And the maximum voltage stability factor can be found by the formula:
$$K_{V(max)} = \frac{\Delta V_{CE} \text{ (allowable)}}{\Delta I_{CBO} \text{ (over the temperature range)}}$$

The original specifications for the amplifier said that we would operate to 70°C ambient temperature. We must also take into account the heating effect at the junction due to power dissipation. Having selected the operating point for the first stage as emitter current = 0.5ma and V_{CE} = 1v (see Figure 98), the collector power dissipation can be found by taking the product of 1v and 0.5ma. The manufacturer's specifications list the thermal resistance, junction to ambient, of the transistor as 0.5°C/mw of collector dissipation. The first stage has only 0.5mw of power dissipation and, therefore, we can assume that the junction temperature will not rise much above ambient. The first stage has the temperature range of 10°C to 70°C.

If we start at room temperature and compensate for an increase in temperature, any decrease in temperature will be compensated for. Let's assume from the manufacturer's references that we find that I_{CBO} will have increased by 50µa when temperature increases from room temperature to 70°C. Change in I_{CBO} for the first transistor is 50µa over the temperature range.

From the curves of the transistor and the load line, we find that collector current can increase by 0.3ma before distortion occurs. Change in collector current allowable is 0.3ma. The current stability factor (K_I) can be found by the formula:
$$K_{I(max)} = \frac{\Delta I_C}{\Delta I_{CBO}} = \frac{0.3 \times 10^{-3}}{50 \times 10^{-6}} = 6$$

From the transistor characteristic curves, the collector voltage V_{CE} can change 850mv before distortion starts occuring. From the formula:
$$K_{V(max)} = \frac{\Delta V_{CE}}{\Delta I_{CBO}} = \frac{850 \times 10^{-3}}{50 \times 10^{-6}} = 17{,}000\Omega$$

Since these values are based somewhat on approximations and the finished circuits will be using available values of components with allowable tolerances, it is best to allow a safety factor. This will also take into account the changes in I_{CBO} over a batch of transistors, etc. This is done by taking the maximum allowable stability factors of the circuit (that we just calculated), and reducing them for insertion into any design formulas. In this case, let's reduce $K_{V(max)}$ to 14,000Ω and $K_{I(max)}$ to 4. We could do the same thing if we were to assume that I_{CBO} increased more than the manufacturer's specification listed. We would simply be doing the same thing by assuming a larger I_{CBO} in the first place; however, we would not want to do both.

We must keep in mind that when values of the stability factors are reduced, the maximum stability factor will be held to a tighter tolerance, but the circuit is made more critical and gain and impedance levels are sacrificed. Reducing the maximum K factor approximately 25% is a good starting point. If an approximate design approach is sufficient, the formulas in Figure 99 can be used to design the circuit. These are nothing more than Kirchhoff's equations with the K or stability factors added. These formulas assume that the base to emitter voltage can be neglected and that the collector current and the emitter current are nearly equal. They will give approximate values. Figures 100, 101, and 102 give the approximate Kirchhoff's equations using the stability factors for several other configurations. Figure 100 gives the approximate formulas for the synthesized constant current source type of stability, or what is generally referred to as long-tailing at Tektronix, Inc. Figure 101 gives the approximate Kirchhoff's equation using the stability factors for a circuit utilizing both the emitter resistor synthesizing a constant current source, and a feedback circuit from the collector back to the base to improve the stability. Figure 102 gives the approximate Kirchhoff's equations using the stability factors for a direct coupled cascade. The formulas, once again, are nothing more than Kirchhoff's equations with the stability factors used, and they are approximate, since they assume that the collector current and emitter current are equal, and there is very little voltage between the base and emitter on the transistor. Approximate formulas are generally good enough; however, since the circuit will then have RMA components added which have allowable tolerances and the design of the circuit will be checked with an analysis approach once the actual components have been substituted. If it does not meet specifications when an analysis approach is applied, steps will have to be taken to correct it;

however, the safety factors make this improbably.

Selection of a value for R_E in the equations can be governed by a number of factors. If R_E is not bypassed, it will greatly increase the input resistance seen at the base of the transistor and reduce the gain of the amplifier. We have discussed this earlier in this volume.

Optimum thermal considerations will occur when the operating point is selected as 1/2 V_{CC}. This is the point of tangency with a constant power hyperbole. This was also discussed earlier. The value of R_E will also limit the maximum current gain when using the formulas in Figure 99 to design a circuit, and this is covered in Figure 99. For our example, we will simply select a value of R_E considering current gain, because R_E will be bypassed with a capacitor.

Using the formulas in Figure 99, and selecting an emitter resistor of 1800Ω, the value of load resistor or R_{L1} is 1,360Ω, the base biasing resistor R_{B1} is 11,060Ω, the resistor R_{F1} is 20,650Ω, and the value of the supply voltage V_{CC} is 2.585v. These values were obtained by inserting the voltage stability factors 14,000Ω, the current stability factor of 4, the design center emitter current of 0.5ma, and the design center collector voltage of 1v into the equations in Figure 99.

The same formulas as used for the first stage in Figure 99 may be used for the second stage as well. The stability factors for the second stage, however, must take into account the change in I_{CBO} over the entire temperature range. The operating point emitter current of the second stage has been selected as 2ma, and a collector voltage of 10v. (We are assuming that we have selected these from the characteristic curves.) This gives a collector dissipation of 20mw. The thermal resistance, junction to ambient, of the transistor is 0.5°C/mw, and this will give a rise in junction temperature above ambient of 10°C. This means that the circuit will have to be stabilized, not to 70°C, but to 80°C to compensate for the heating effect at the collector junction. The collector power dissipation raises the junction temperature above ambient by 10°C. The specifications call for an ambient temperature of 70°C; therefore, the junction will have to be stabilized to 80°C.

Let's assume from the manufacturer's reference that I_{CBO} increases by 120μa at

80°C. The change in I_{CBO} for insertion into the K formulas is 120μa. Assume that from the curves for the transistor, it is found that the collector current can increase 1.08ma before distortion starts occuring, and V_{CE} can decrease by 6.72v before distortion occurs.

The maximum current stability factor can be calculated using the formula:

$$K_{I(max)} = \frac{\Delta I_C}{\Delta I_{CBO}} = \frac{1.08ma}{120\mu a} = 9$$

and the maximum voltage stability factor:

$$K_{V(max)} = \frac{\Delta V_{CE}}{\Delta I_{CBO}} = \frac{6.72v}{120\mu a} = 56,000\Omega$$

Since we did not reduce the value of the change in I_{CBO} over the temperature range, we must allow a safety factor. In this case, reduce $K_{I(max)}$ to 7, and $K_{V(max)}$ to 47,000Ω for use in the formulas in Figure 99.

The voltage change at the output is the prime consideration in this stage. The transistor is not working into another transistor, so the d-c collector load resistor can also constitute the a-c collector load resistor. In this case, R_E should be selected by considering the supply voltage available and the frequency response desired because R_E will effect the size of the load resistance. Thermal considerations should also be kept in mind.

As a starting point, select R_E = 1,200Ω. From the formulas in Figure 99:

$$R_{L2} = 4,830\Omega$$
$$R_{F2} = 77,000\Omega$$
$$R_{B2} = 9,430\Omega$$
$$V_{CC2} = 22.1v$$

A 22v supply is needed for the second stage. A divider network can be used to supply the first stage and allow the use of only one supply voltage source.

RMA components should now be inserted as close to the values calculated as tolerance

APPROXIMATE d-c DESIGN AND ANALYSIS EQUATIONS

In the equations on this page, the absolute value of quantities inserted into the equations must be used.

In general, the selection of R_E for this configuration governs to a great extent the maximum current gain that can be obtained. The nominal value of R_E for maximum current gain is $R_E = K_V/2K_I$.

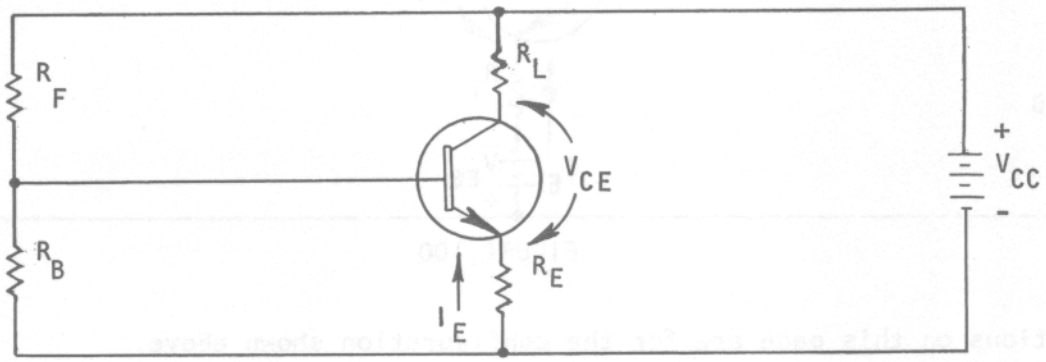


FIGURE 99

The equations on this page are for the configuration shown above. I_E and V_{CE} in the design formulas are the selected operating point emitter current and collector voltage. K_I and K_V are the calculated maximum allowable current and voltage stability factors that the circuit must meet. These are approximate formulas, but will generally give values within allowable tolerances, once RMA components are inserted.

DESIGN FORMULAS

1. Select R_E
2. $R_L \approx \dfrac{K_V - K_I R_E}{1 + K_I}$
3. $V_{CC} \approx \dfrac{K_I V_{CE} + I_E (K_V - R_L)}{K_I}$
4. $R_F \approx \dfrac{K_I V_{CC}}{I_E}$
5. $R_B \approx \dfrac{K_I R_E R_F}{R_F - K_I R_E}$

ANALYSIS FORMULAS

1. $K_I \approx \dfrac{R_B R_F}{R_E (R_B + R_F)}$
2. $K_V \approx K_I R_E + R_L (1 + K_I)$
3. $I_E \approx \dfrac{K_I V_{CC}}{R_F}$
4. $V_{CE} \approx V_{CC} - I_E (R_E + R_L)$

APPROXIMATE d-c DESIGN AND ANALYSIS EQUATIONS

In the equations on this page, absolute values of the quantities inserted into the equations must be used.

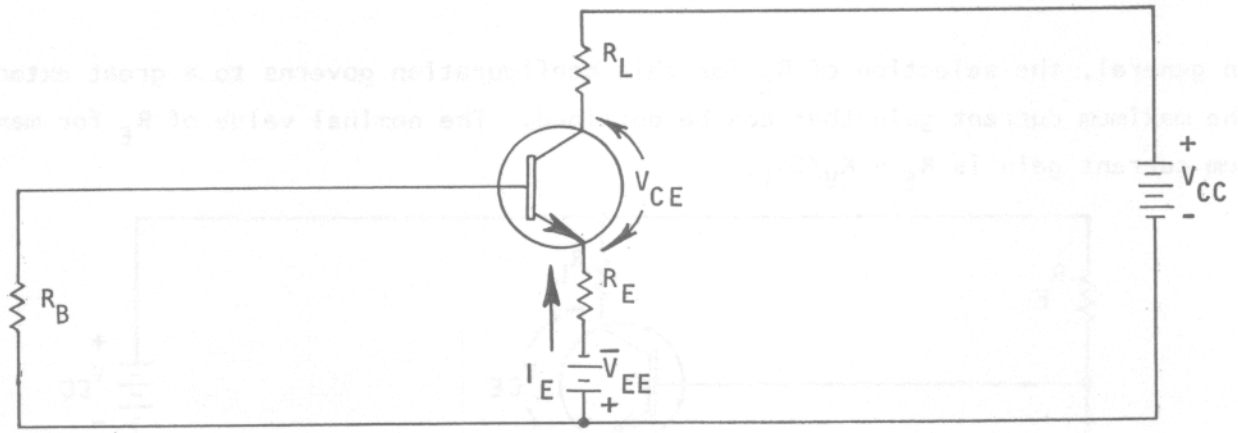


FIGURE 100

The equations on this page are for the configuration shown above.

NOTE: LONGTAIL

I_E and V_{CE} in the design formulas are the selected operating point emitter current and collector voltage. K_I and K_V are the calculated maximum allowable current and voltage stability factors that the circuit must meet. These are approximate formulas, but will generally give values within allowable tolerances, once RMA components are inserted.

DESIGN FORMULAS

1. Select R_E
2. $R_L \approx \dfrac{K_V - K_I R_E}{1 + K_I}$
3. $V_{EE} \approx R_E I_E$
4. $V_{CC} \approx \dfrac{K_I V_{CE} + K_V I_E - I_E R_L}{K_I - V_{EE}}$
5. $R_B \approx K_I R_E$

ANALYSIS FORMULAS

1. $K_I \approx \dfrac{R_B}{R_E}$
2. $K_V \approx K_I R_E + R_L (1 + K_I)$
3. $I_E \approx \dfrac{V_{EE}}{R_E}$
4. $V_{CE} \approx V_{CC} + V_{EE} - I_E (R_E + R_L)$

APPROXIMATE d-c DESIGN AND ANALYSIS EQUATIONS

In the equations on this page, absolute values of the quantities inserted in the equations must be used.

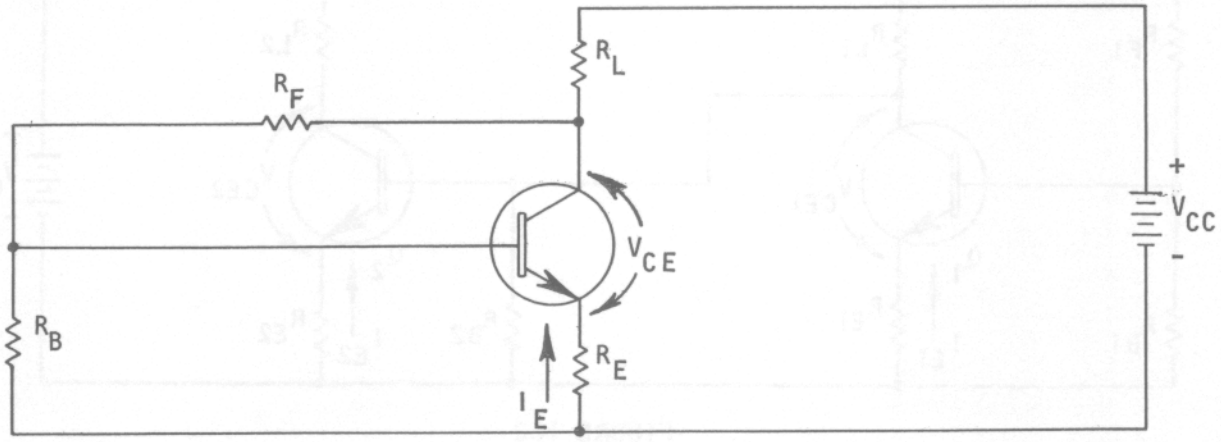


FIGURE 101

The equations on this page are for the configuration shown above.

NOTE: R_F returned to the collector for d-c feedback

I_E and V_{CE} in the design equations are the selected operating point emitter current and collector voltage. K_I and K_V are the calculated maximum allowable current and voltage stability factors that the circuit must meet. These are approximate formulas, but will generally give values within allowable tolerances, once RMA components are inserted.

DESIGN FORMULAS

1. Select R_E
2. $V_{CC} \approx \dfrac{K_I\ V_{CE} + K_V\ I_E}{K_I}$
3. $R_F \approx \dfrac{K_I\ V_{CC}}{I_E}$
4. $R_L \approx \dfrac{V_{CC}\ (K_V - K_I\ R_E)}{V_{CE}\ (1 + K_I) + K_V\ I_E}$
5. $R_B \approx \dfrac{K_I\ R_E\ V_{CC}}{V_{CE}}$

ANALYSIS FORMULAS

1. $K_I \approx \dfrac{R_B R_F}{R_E R_F + R_E R_B + R_L R_E + R_B R_L}$
2. $K_V \approx \dfrac{R_F\ I_E - K_I\ V_{CE}}{I_E}$
3. $I_E \approx \dfrac{K_I\ V_{CC}}{R_F}$
4. $V_{CE} \approx \dfrac{K_I\ V_{CC}\ R_E}{R_B}$

APPROXIMATE d-c DESIGN AND ANALYSIS EQUATIONS

In the equations on this page, absolute values of the quantities inserted in the equations must be used.

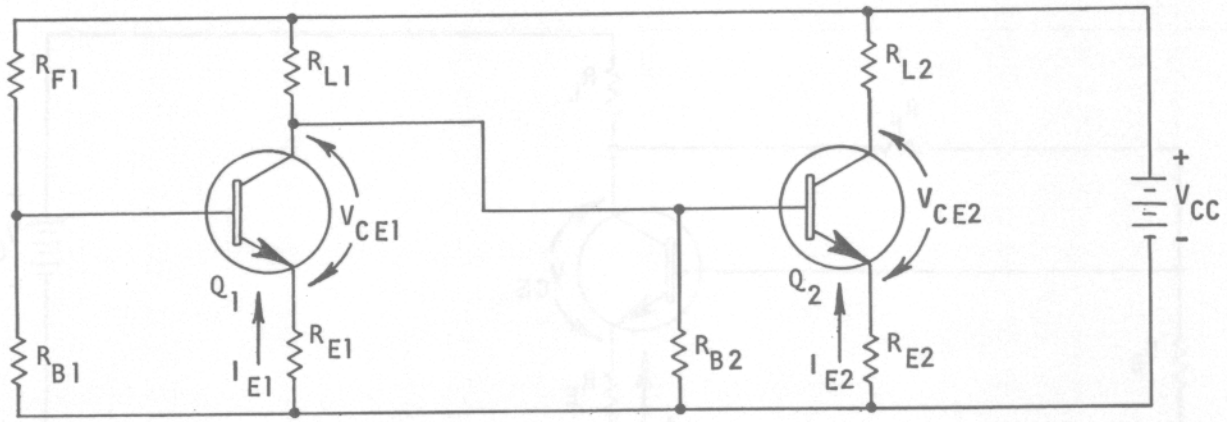


FIGURE 102

The equations on this page are for the configuration shown above.

NOTE: DIRECT COUPLING

I_E and V_{CE} in the design equations are the selected operating point emitter current and collector voltage. K_I and K_V are the calculated maximum allowable current and voltage stability factors that the circuit must meet. These are approximate formulas, but will generally give values within allowable tolerances, once the RMA components are inserted.

DESIGN FORMULAS

1. $R_{E1} \approx \dfrac{K_{V1}\, I_{E2} - K_{I2}\, V_{CE1}}{K_{I1}\, I_{E2} + K_{I2}\, I_{E1}}$

2. $R_{E2} \approx \dfrac{V_{CE1} + I_{E1}\, R_{E1}}{I_{E2}}$

3. $R_{L2} \approx \dfrac{K_{V2} - R_{E2}\, K_{I2}}{K_{I2} - 1}$

4. $V_{CC} \approx V_{CE2} + I_{E2}\,(R_{E2} + R_{L2})$

5. $R_{L1} \approx \dfrac{V_{CC}\, K_{I2}}{I_{E1}\, K_{I2} + I_{E2}\, K_{I1}}$

6. $R_{F1} \approx \dfrac{K_{I1}\, V_{CC}}{I_{E1}}$

7. $R_{B1} \approx \dfrac{R_{F1}\, R_{E1}\, K_{I1}}{R_{F1} - R_{E1}\, K_{I1}}$

8. $R_{B2} \approx \dfrac{R_{E2}\, R_{L1}\, K_{I2}}{R_{L1}\, K_{I1}\, R_{E2}\, K_{I2}}$

ANALYSIS FORMULAS

1. $K_{I1} \approx \dfrac{R_{B1}\, R_{F1}}{R_{E1}\,(R_{B1} + R_{F1})}$

2. $K_{I2} \approx \dfrac{K_{I1}\, R_{L1}}{R_{E2}\left(1 + \dfrac{R_{L1}}{R_{B2}}\right)}$

3. $K_{V1} \approx R_{E1}\, K_{I1} + R_{E2}\, K_{I2}$

4. $K_{V2} \approx K_{I2}\,(R_{E2} + R_{L2}) - R_{L2}$

5. $I_{E1} \approx \dfrac{K_{I1}\, V_{CC}}{R_{F1}}$

6. $I_{E2} \approx \dfrac{K_{I2}\,(V_{CC} - I_{E1}\, R_{L1})}{K_{I1}\, R_{L1}}$

7. $V_{CE1} \approx R_{E2}\, I_{E2} - R_{E1}\, I_{E1}$

8. $V_{CE2} \approx V_{CC} - I_{E2}\,(R_{E2} + R_{L2})$

permits, and the circuit checked using the approximate d-c analysis formulas in Figure 99. An a-c analysis approach can then be applied to insure that the specifications of the amplifier have been met. We can use the a-c analysis approaches that we have discussed earlier in this volume.

CALCULATING COUPLING CAPACITORS AND EMITTER BYPASS CAPACITORS:

The coupling capacitor and emitter bypass capacitor can be calculated from the formula:

The coupling capacitor:

$$C_C = \frac{1}{2\pi f_{3db}\left(R_L + \frac{r_{eq}\, r_i}{r_{eq} + r_i}\right)}$$

The emitter bypass capacitor:

$$C_E = \frac{h_{fe} + 1}{2\pi f_{3db}\left(r_i + \frac{R_L\, r_{eq}}{R_L + r_{eq}}\right)}$$

Where: f_{3db} = the lowest frequency it is desired to amplify

r_i = the a-c input resistance of the transistor

r_{eq} = any resistance shunting r_i

R_L = d-c load resistor of the previous stage.

The completed circuit with calculated values is shown in Figure 103. Figure 104 shows the completed circuit with RMA components substituted for the approximate components obtained in the design procedure.

The following is an approximate d-c analysis of the circuit in Figure 104 using the equations in Figure 99:

$$K_{I1} \approx \frac{R_{B1}\, R_{F1}}{R_{E1}\,(R_{B1} + R_{F1})} \approx 4.3$$

$$K_{V1} \approx K_{I1}\, R_{E1} + R_{L1}\,(1 + K_{I1}) \approx 15.7 \times 10^3$$

$$I_{E1} \approx \frac{K_{I1} V_{CC1}}{R_{F1}} \approx 0.508ma$$

$$V_{CE1} \approx V_{CC1} - I_{E1} (R_{E1} + R_{L1}) \approx 0.92v$$

$$K_{I2} \approx \frac{R_{B2} R_{F2}}{R_{E2} (R_{B2} + R_{F2})} \approx 7.45$$

$$K_{V2} \approx K_{I2} R_{E2} + R_{L2} (1 + K_{I2}) \approx 39.7K$$

$$I_{E2} \approx \frac{K_{I2} V_{CC2}}{R_{F2}} \approx 2ma$$

$$V_{CE2} \approx V_{CC2} - I_{E2} (R_{E2} + R_{L2}) \approx 10.2v$$

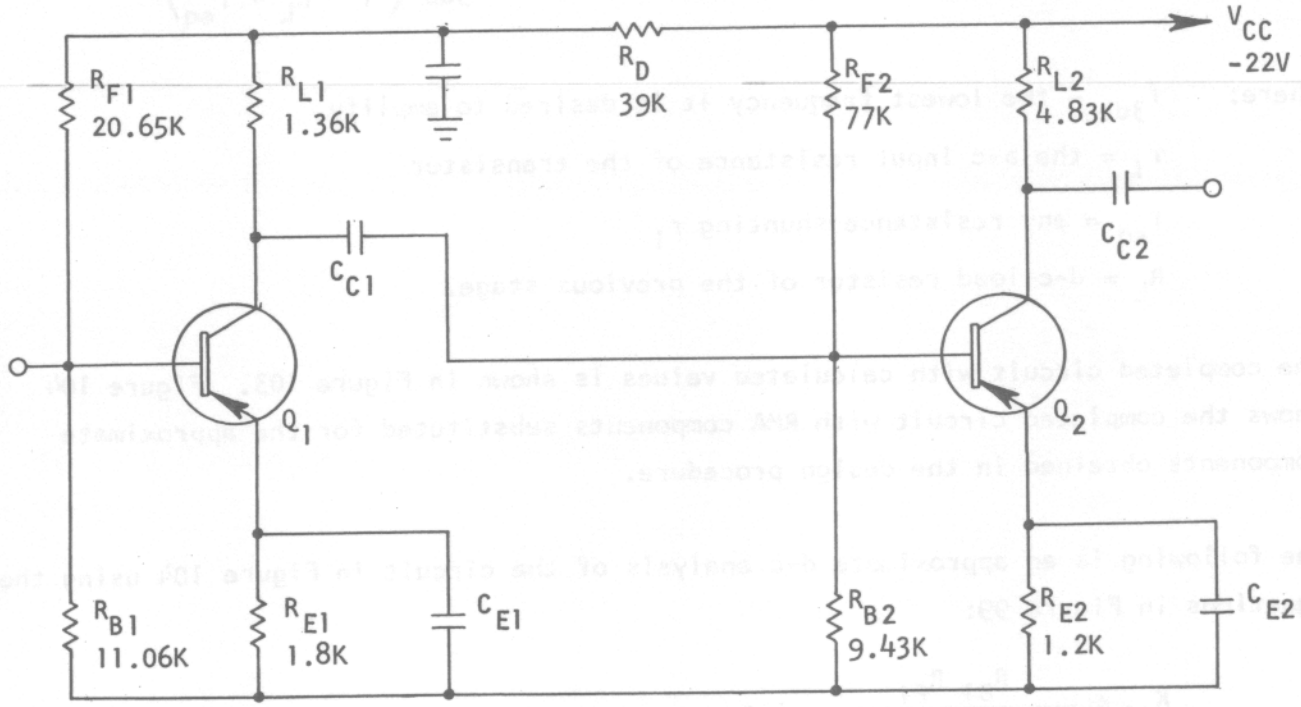


FIGURE 103

Notice that the stability factors are well below the maximum values calculated for the amplifiers using the specifications of the transistors. The transistor currents and voltages are very close to the design center values selected for both stages.

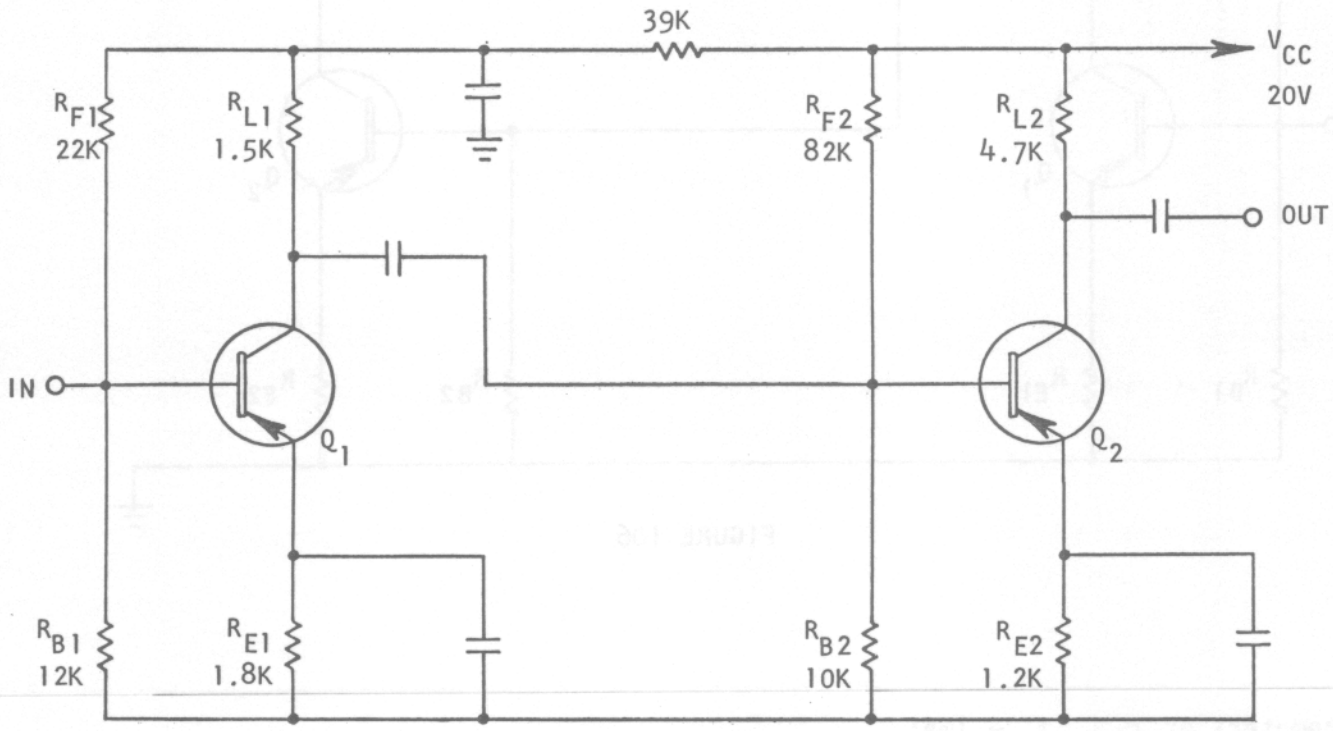


FIGURE 104

D-C COUPLED AMPLIFIER DESIGN:

To simplify an example of d-c coupled design, we will assume that the same stability factors and operating points will be applied as in the previous design situation. However, it is desired to have the amplifier amplify down to d-c and, therefore, direct coupling is a prerequisite. In order to design the amplifier for direct coupling, the approximate Kirchhoff equations in Figure 102 are used. Figure 106 shows the configuration that the amplifier will have, and the following parameters are given (they are the same as in the previous problem). $I_{E1} = 0.5ma$, $V_{CE1} = 1v$, $K_{I1} = 4$, $K_{V1} = 14K$, $I_{E2} = 2ma$, $V_{CE2} = 10v$, $K_{I2} = 7$, $K_{V2} = 47K$

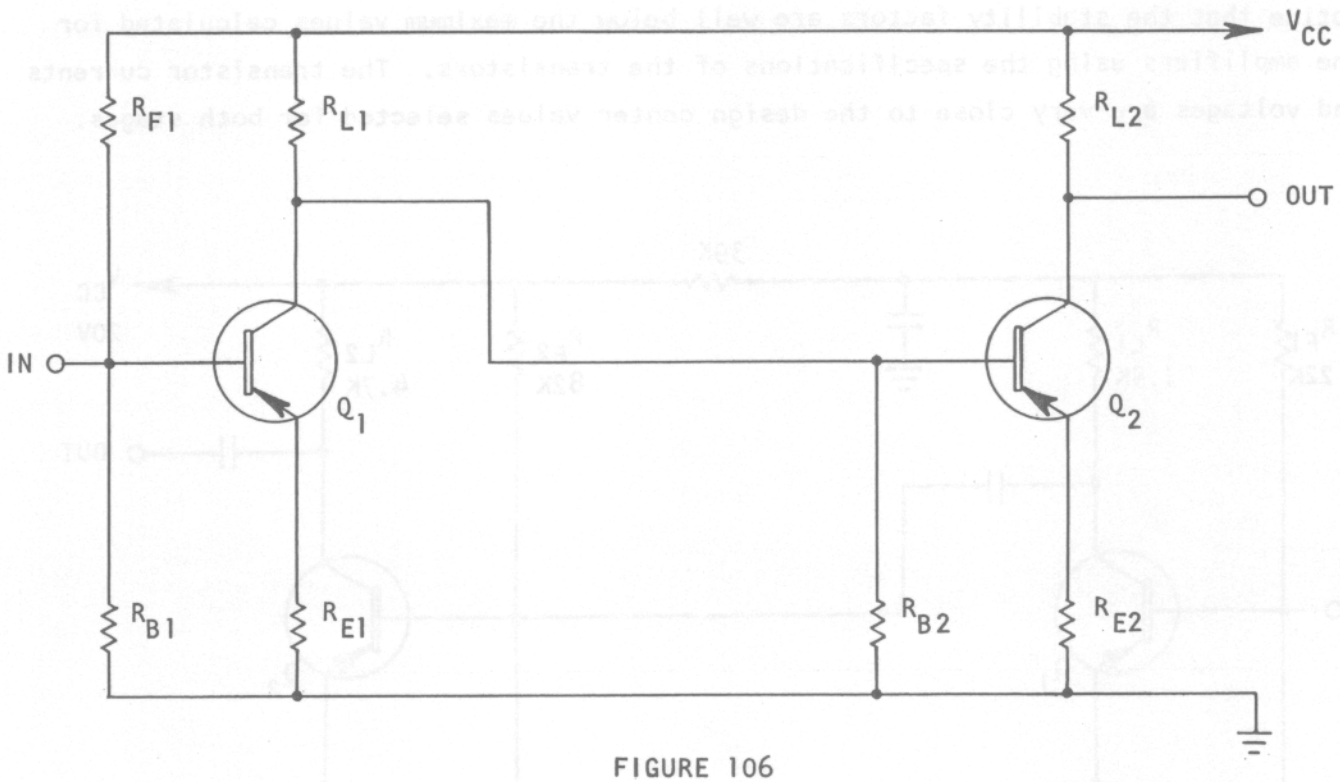


FIGURE 106

Parameters at 25°C, I_E = 1ma:

$h_{ie} = 2.1 \times 10^3$, $h_{re} = 1.8 \times 10^{-5}$, $h_{fe} = 50$, $h_{oe} = 4.8 \times 10^{-7}$, $\Theta_{JA} = 0.5°C/mw$

The underlined value is the selected RMA component value:

$$R_{E1} \approx \frac{K_{V1}\, I_{E2} - K_{I2}\, V_{CE2}}{K_{I1}\, I_{E2} + K_{I2}\, I_{E1}} \approx \frac{(14 \times 10^3)\ (2 \times 10^{-3}) - (7)\ (1)}{(4)\ (2 \times 10^{-3}) + (7)\ (0.5 \times 10^{-3})} \approx \underline{1.8K}$$

$$R_{E2} \approx \frac{V_{CE1} + I_{E1}\, R_{E1}}{I_{E2}} \approx \frac{1 + (0.5 \times 10^{-3})(1.8 \times 10^3)}{2 \times 10^{-3}} \approx \underline{1.5K}$$

$$R_{L2} \approx \frac{K_{V2} - R_{E2}\, K_{I2}}{K_{I2} - 1} \approx \frac{47 \times 10^3 - (1.5 \times 10^3)\ (7)}{7 - 1} \approx 6.08K \approx \underline{6.2K}$$

$$V_{CC} \approx V_{CE2} + I_{E2}\ (R_{E2} + R_{L2}) \approx 10 + (2 \times 10^{-3})\ (1.5 \times 10^3)\ (7) \approx \underline{25.4v}$$

$$R_{L1} \approx \frac{V_{CC}\, K_{12}}{I_{E2}\, K_{12} + I_{E2}\, K_{12}} \approx \frac{(25.4)\ (7)}{(0.5 \times 10^{-3})\ (7) + (2 \times 10^{-3})\ 4} \approx 15.45K \approx \underline{15K}$$

$$R_{F1} \approx \frac{K_{11}\, V_{CC}}{I_{E1}} \approx \frac{(4)\ (25.4)}{(0.5 \times 10^{-3})} \approx 208K \approx \underline{200K}$$

$$R_{B1} \approx \frac{R_{F1}\, R_{E1}\, K_{11}}{R_{F1} - R_{E1}\, K_{11}} \approx \frac{(200 \times 10^{3})\ (1.8 \times 10^{3})\ (4)}{(200 \times 10^{3}) - (1.8 \times 10^{3})\ (4)} \approx \underline{7.5K}$$

$$R_{B2} \approx \frac{R_{E2}\, R_{L1}\, K_{12}}{R_{L1}\, K_{11} - R_{E2}\, K_{12}} \approx \frac{(1.5 \times 10^{3})\ (15 \times 10^{3})\ (7)}{(15 \times 10^{3})\ (4) - (1.5 \times 10^{3})\ (7)} \approx 3.18K \approx \underline{3.3K}$$

Figure 107 shows the amplifier with component values.

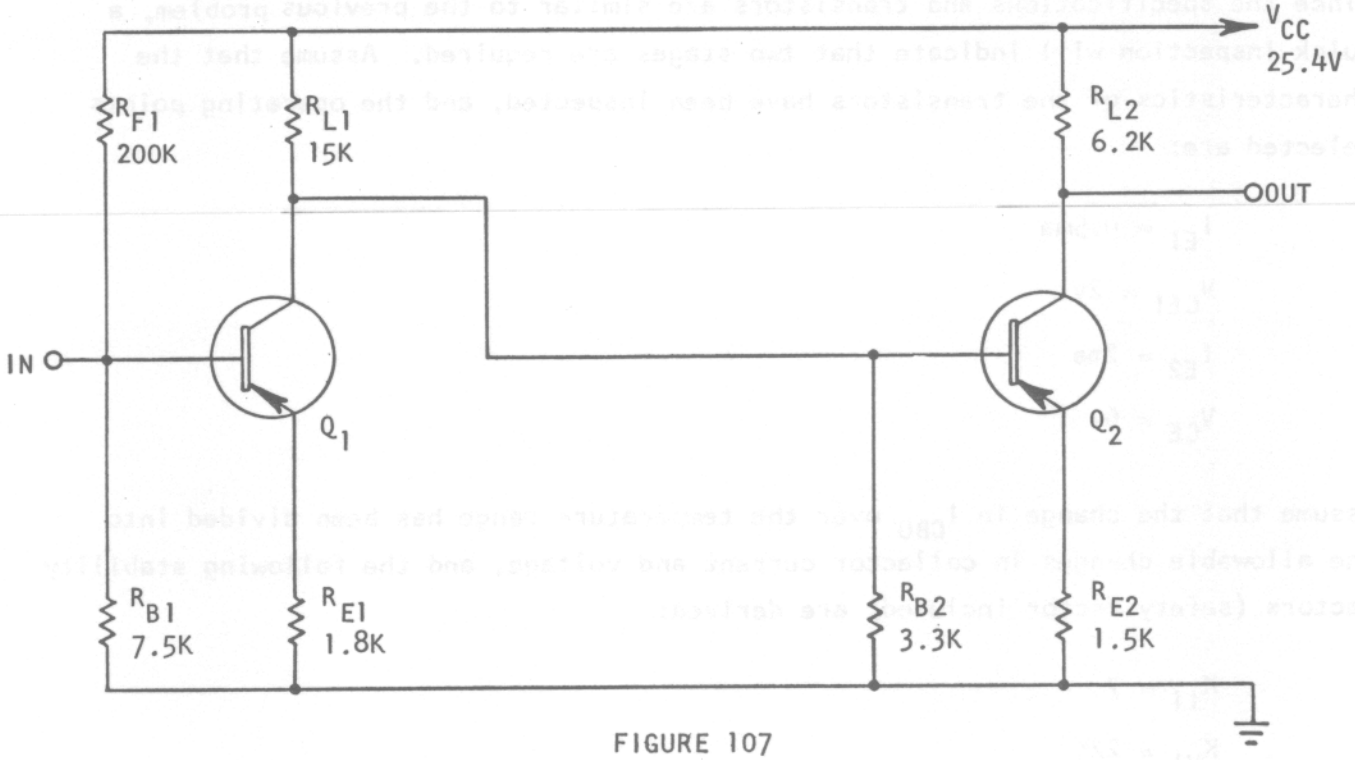


FIGURE 107

Let's apply the approximate design approach once more. Assume we are designing a low level, low frequency amplifier with the following specifications:

Input signal: 0.4μa peak
Required output signal: 1.2v peak
Single d-c supply operation
Design center temperature: 25°C
Stable to maximum ambient temperature of: 70°C
Supply voltage available: 20v

Assume a transistor has been selected, and the parameters at I_E = 1ma are:

$h_{ib} = 55\Omega$
$h_{fe} = 50$
$h_{ob} = 0.2\mu mhos$
$h_{rb} = 2 \times 10^{-4}$

Since the specifications and transistors are similar to the previous problem, a quick inspection will indicate that two stages are required. Assume that the characteristics of the transistors have been inspected, and the operating points selected are:

$I_{E1} = 0.5ma$
$V_{CE1} = 2v$
$I_{E2} = 2ma$
$V_{CE} = 6v$

Assume that the change in I_{CBO} over the temperature range has been divided into the allowable changes in collector current and voltage, and the following stability factors (safety factor included) are derived:

$K_{I1} = 7$
$K_{V1} = 22K$
$K_{I2} = 10$
$K_{V2} = 75K$

Since we will be limited to a single d-c power supply, we will use the configur-

ations in Figure 108.

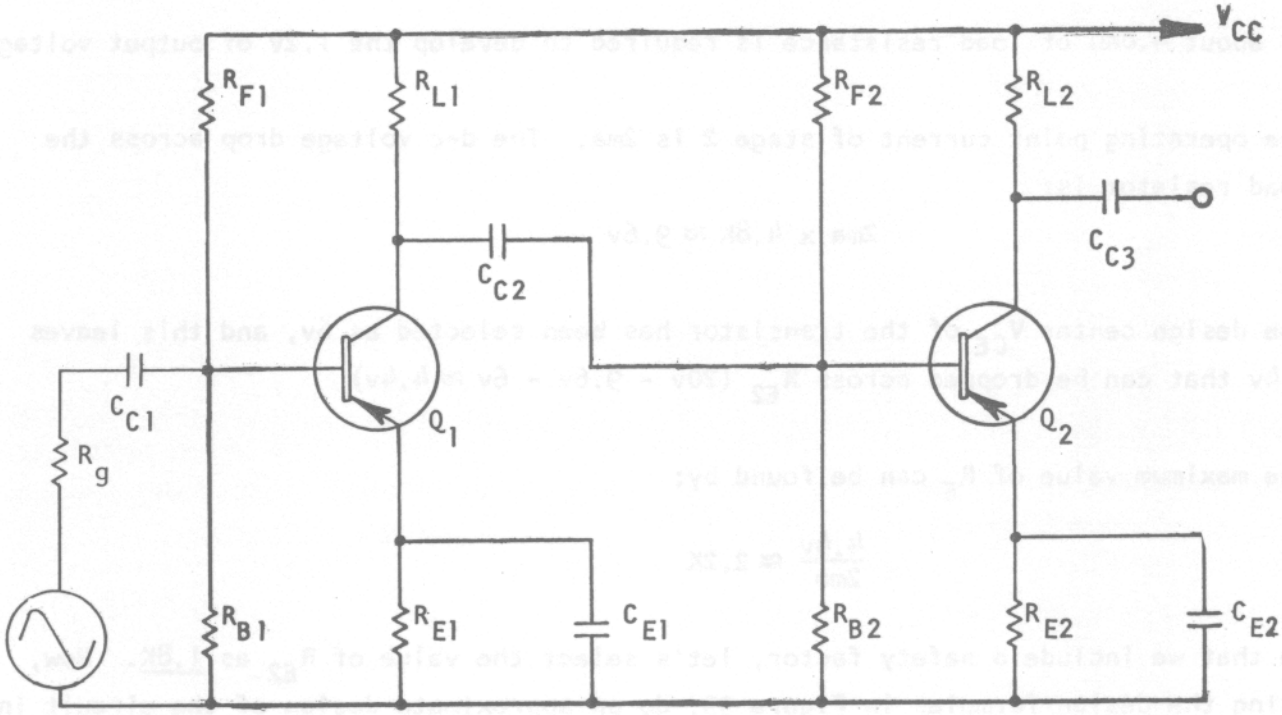


FIGURE 108

Stage 1 is essentially a current amplifier, and selection of R_E for optimum current gain is:

$$R_{E1} = \frac{K_{V1}}{2K_{I1}} = 1.571K$$

Let's select $R_{E1} = \underline{1.5K}$

Stage 2 is concerned with voltage swing at its output, and the supply voltage is limited to 20v. This must be considered when selecting R_{E2}. The selected transistors have an h_{fe} of 50. The input current to transistor 1 is 0.2μa peak, assuming a 50% loss in the input biasing network. Assuming the current gain of stage 1 is $\approx h_{fe}$; the output current of stage 1 is: 50 x 0.2μa $\approx$ 10μa peak
Once again, assuming a 50% loss in the biasing configuration at the input to stage 2, the input to stage 2 is $\approx$ 5μa peak. Assume the current gain of stage 2 is $\approx h_{fe}$, the output current of stage 2 is: 50 x 5μa peak $\approx$ 250μa peak

The required output voltage swing is 1.2v peak. By Ohm's Law:

$$\frac{1.2v}{250\mu a} \approx 4.8K\Omega$$

or about 4.8KΩ of load resistance is required to develop the 1.2v of output voltage.

The operating point current of stage 2 is 2ma. The d-c voltage drop across the load resistor is:

$$2ma \times 4.8K \approx 9.6v$$

The design center V_{CE} of the transistor has been selected as 6v, and this leaves 4.4v that can be dropped across R_{E2} (20v - 9.6v - 6v ≈ 4.4v)

The maximum value of R_E can be found by:

$$\frac{4.4v}{2ma} \approx 2.2K$$

So that we include a safety factor, let's select the value of R_{E2} as 1.8K. Now, using the design formulas in Figure 99, do an approximate design of the circuit in Figure 108 before reading on.

The following is the approximate d-c design of the circuit in Figure 108:

Stage 1:

R_{E1} = selected as 1.5K

$$R_{L1} \approx \frac{K_{V1} - K_{I1} R_{E1}}{1 + K_{I1}} \approx \frac{(22 \times 10^3) - (7)(1.5 \times 10^3)}{1 + 7} \approx 1.438K$$

$$V_{CC1} \approx \frac{K_{I1} V_{CE1} + I_{E1}(K_{V1} - R_{L1})}{K_{I1}} \approx \frac{(7)(2) + (0.5 \times 10^{-3})(22 \times 10^3 - 1.4 \times 10^3)}{7} \approx 3.47v$$

$$R_{F1} \approx \frac{K_{I1} V_{CC1}}{I_{E1}} \approx \frac{7 \times 3.47}{0.5 \times 10^{-3}} \approx 48.5K$$

$$R_{B1} \approx \frac{K_{I1} R_{E1} R_{F1}}{R_{F1} - K_{I1} R_{E1}} \approx \frac{(7)(1.5 \times 10^3)(48.5 \times 10^3)}{(48.5 \times 10^3) - (7)(1.5 \times 10^3)} \approx 13.38K$$

Stage 2:

R_{E2} = selected as 1.8K

$$R_{L2} \approx \frac{K_{V2} - K_{I2} R_{E2}}{1 + K_{I2}} \approx \frac{(75 \times 10^3) - (10)(1.8 \times 10^3)}{1 + 10} \approx 5.18K$$

$$V_{CC2} \approx \frac{K_{I2} V_{CE2} + I_{E2} (K_{V2} - R_{L2})}{K_{I2}} \approx \frac{(10)(6) + (2 \times 10^3)(75 \times 10^3 - 5.18 \times 10^3)}{10} \approx 20v$$

$$R_{F2} \approx \frac{K_{I2} V_{CC2}}{I_{E2}} \approx \frac{(10)(20)}{2 \times 10^{-3}} \approx 100K$$

$$R_{B2} \approx \frac{K_{I2} R_{E2} R_{F2}}{R_{F2} - K_{I2} R_{E2}} \approx \frac{(10)(1.8 \times 10^3)(100 \times 10^3)}{(100 \times 10^3) - (10)(1.8 \times 10^3)} \approx 21.95K$$

The completed circuit is shown in Figure 109. A 29K resistor drops the supply voltage down to approximately 3.5v for the first stage.

POWER TRANSISTORS:

All transistors are power amplifiers, but those transistors primarily designed for large signal amplification and for high power switching are referred to as power transistors.

The parameters and equations used in the section dealing with hybrid equivalent circuits and other functional models of small-signal, low frequency amplifiers are not valid for the power transistor. The small-signal parameters are obtained by making incremental measurements at a given operating point and set of conditions. The power transistor will generally swing over a large region of its operating range, making analysis and design difficult with the use of small-signal parameters.

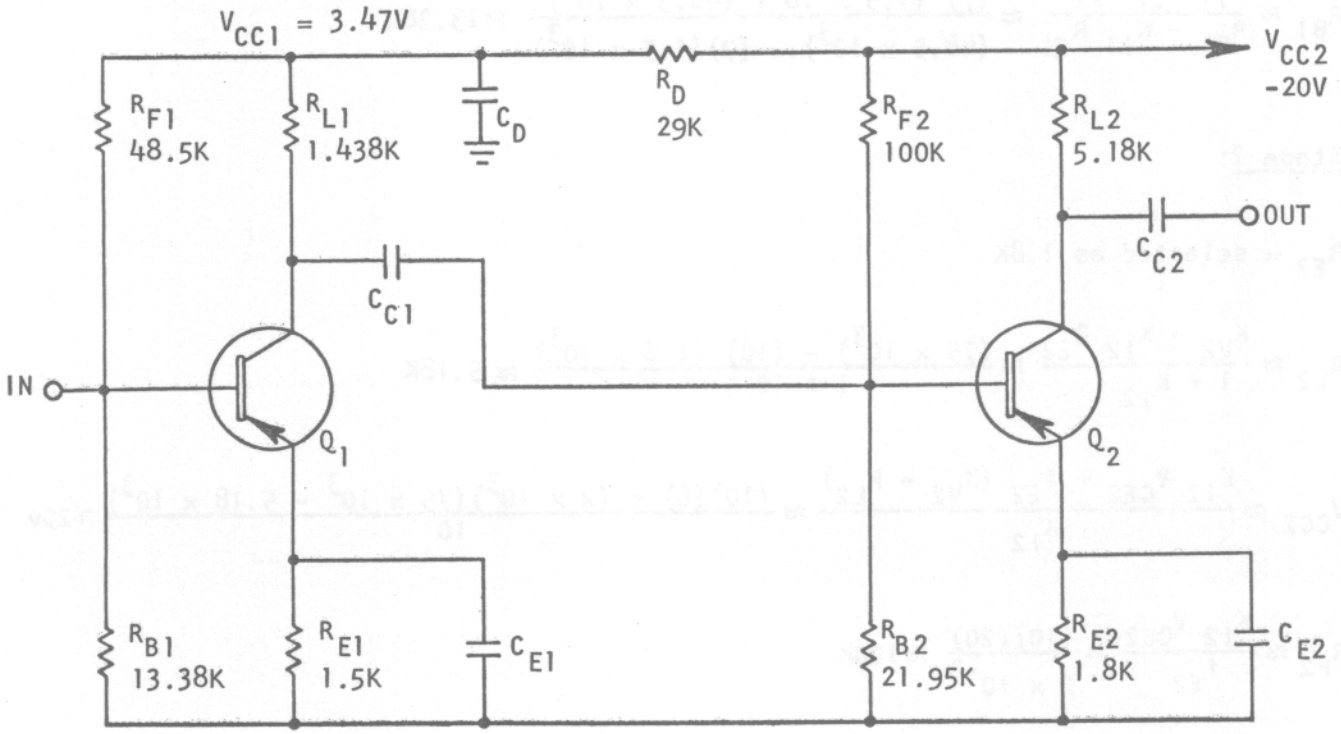


FIGURE 109

The use of curves and charts with power transistors is more common, although an approximation of the operation may be made using the equations for gain and impedance levels previously discussed. This is assuming that the parameters are given by the manufacturers, or measured on a device such as the Tektronix Type 575 Transistor-Curve Tracer, or other measurements devices for obtaining parameters. All the parameters for a power transistor are seldom given by a manufacturer. Those that are given are large signals, or d-c parameters, rather than small signal.

Two short circuit parameters are sometimes given because the power transistor will, in a great number of cases, be working into a transformer or a low impedance load. They are H_{FE}, the large signal, forward current gain, and H_{IE}, the large signal, input resistance. Open circuit parameters such as h_{oe} and h_{re} are seldom given because the input of the transistor is rarely open or near open circuited.

The small-signal parameters are measured using incremental changes in the currents or voltages. The large-signal parameter measurements are made using large variations.

The following is a list of parameters that you might encounter for a common emitter configuration:

Forward Current Gain:

Small signal: $$h_{fe} = \frac{\Delta I_C}{\Delta I_B} \Bigg|_{\Delta V_{CE} = 0}$$

Large signal: $$H_{FE} = \frac{\Delta I_C}{\Delta I_B} \Bigg|_{\Delta V_{CE} = 0}$$

d-c: $$h_{FE} = \frac{I_C - I_{CBO}}{I_B + I_{CBO}}$$

Input Resistance:

Small signal: $$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \Bigg|_{\Delta V_{CE} = 0}$$ note: Δ = incremental changes

Large signal: $$H_{IE} = \frac{\Delta V_{BE}}{\Delta I_B} \Bigg|_{\Delta V_{CE} = 0}$$ note: Δ = large changes

d-c: $$h_{IE} = \frac{V_{BE}}{I_B}$$

Transconductance:

$$g_{FE} = \frac{I_C}{V_{BE}} = \frac{h_{FE}}{h_{IE}}$$

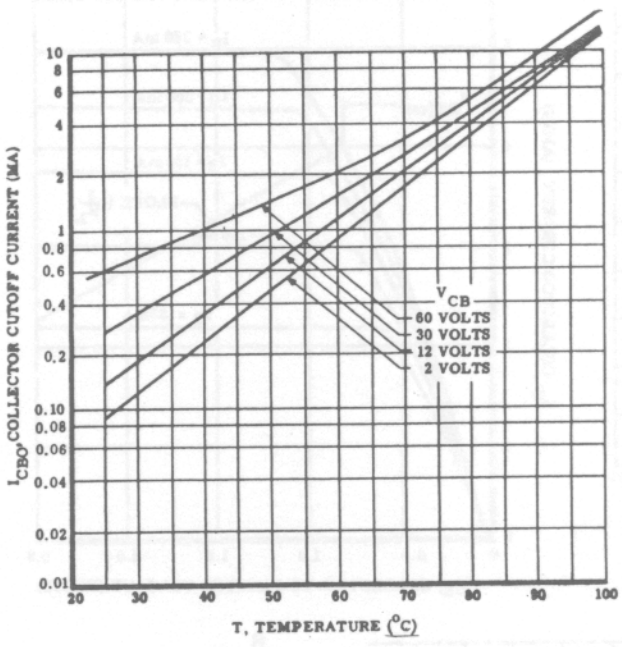
Transconductance is the transfer parameter for dealing with output current with respect to input voltage. Power amplifiers generally take on a common emitter configuration for maximum power gain. Curves, charts, and parameters are given by the manufacturer for the common emitter configuration typically for this reason. Common base, common collector, and special circuit configuration parameters are derived by converting these values.

Figures 110, 111, and 112 show a group of characteristic curves made available by a manufacturer of power transistors. These are reproduced here with the courtesy of Motorola Semiconductor Products, Inc., Phoenix, Arizona. Figure 110A is a plot of I_{CBO}, the collector cut-off current versus temperature for different voltages for this particular transistor. A typical application of this chart might be in finding the change in I_{CBO} over a range of temperatures for design stability considerations, or determining I_{CBO} at a given temperature.

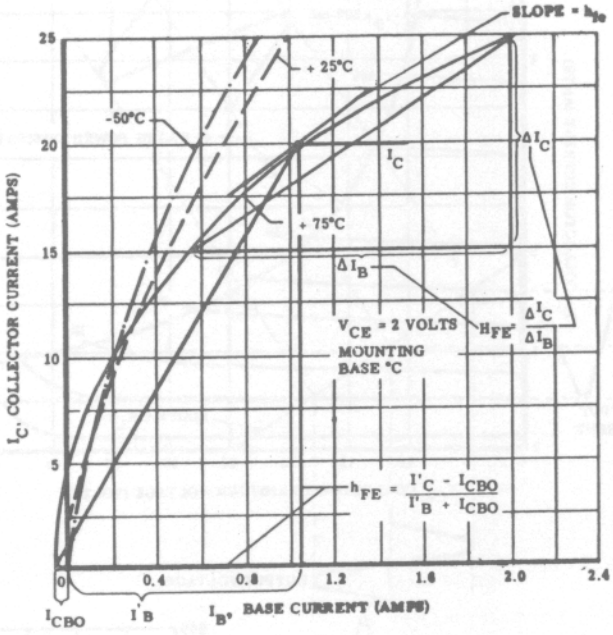
Figure 110B is a plot of collector current versus base current for several different temperatures, and gives a large signal graph of base current versus output current at these different temperatures. The slope of any curve in Figure 110B can be used to calculate the beta of the transistor at that temperature. Figure 110C plots collector current versus base to emitter voltage at several different temperatures. The slope of the line in this chart can be used to calculate the transconductance of the transistor. Figure 110D is a composite curve, showing base to emitter voltage versus base current and collector current. This is a combination of a graph of H_{IE} and a transfer characteristic. The effects of source impedance on output distortion is shown.

Figure 111A is a collector family of curves with the base current as the running parameter. A hyperbole indicating maximum power dissipation of the transistor has been superimposed, showing the safe limits of operation. A load line has been plotted and an input current applied, showing the results and variations in the output voltage and current, illustrating how they may be derived. Figure 111B is an expanded plot of collector voltage versus collector current with base current as a running parameter. This extends the area around saturation and allows $V_{CE(sat)}$ to be calculated, along with other transistor characteristics at or near saturation. Figure 111C is a plot of current gain (h_{FE}) versus collector current for determining h_{FE} at a given operating point. Figure 111C is a plot of h_{FE} versus temperature, allowing the variations in current gain with changes in temperature to be pre-determined. The vertical plot in Figure 111D is, in a percentage factor, the product of h_{FE} at the normalized temperature, and this factor will give h_{FE} at a different temperature. In the case where the change is desired, the difference in the two values of h_{FE} will give the change in h_{FE} with temperature.

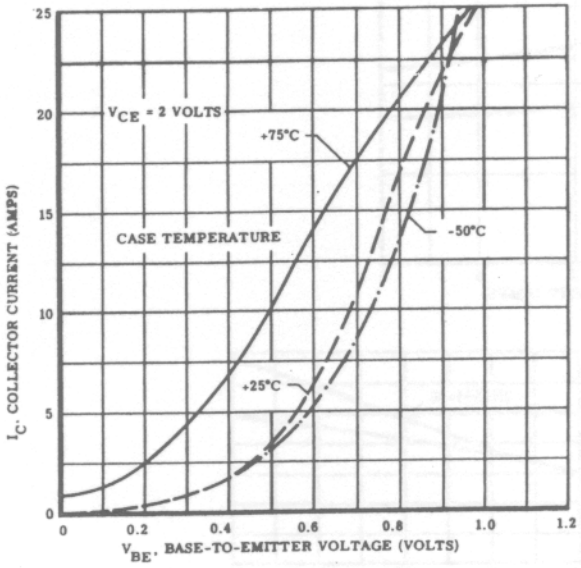
Figure 112A is the plot of temperature versus the percentage change of base to



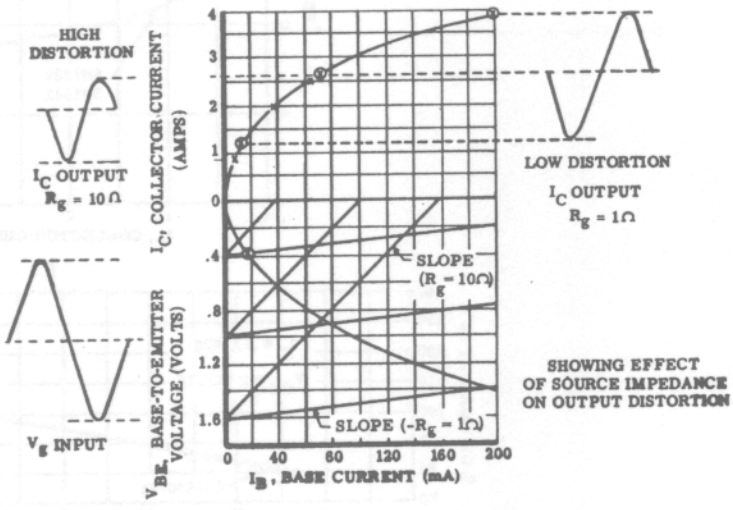
A



B



C



D

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FIGURE 110

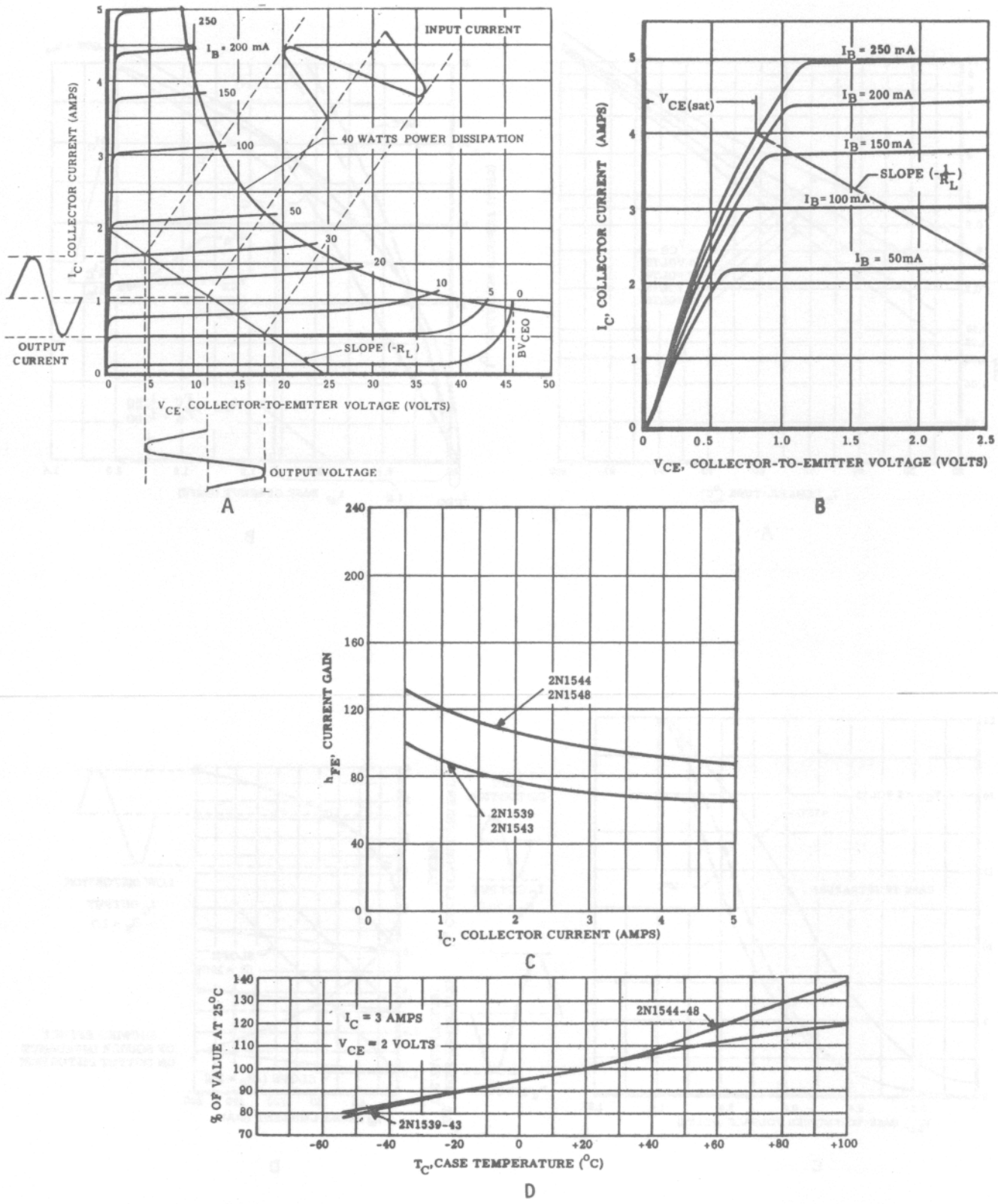

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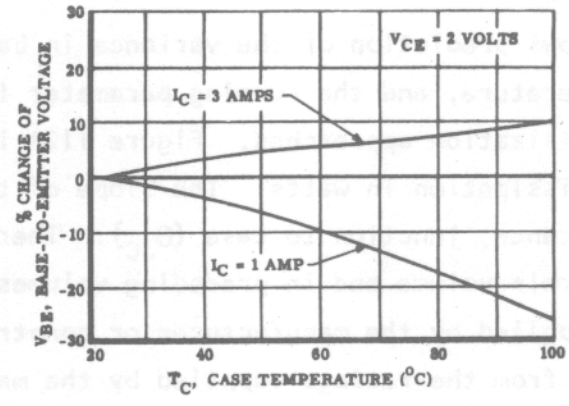
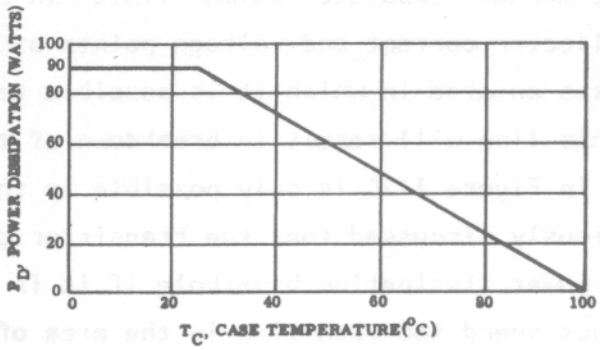
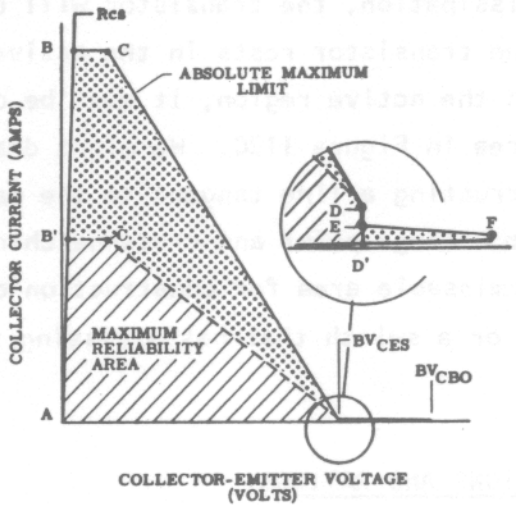
FIGURE 111



A



B



C

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FIGURE 112

emitter voltage. This allows prediction of the variance in base to emitter voltage for a given change in temperature, and the running parameter is collector current. This is useful in d-c stabilization approaches. Figure 112B is the plot of case temperature versus power dissipation in watts. The slope of the line can be used to calculate thermal resistance, junction to case (Θ_{JC}). Thermal resistance has been discussed earlier in this volume and in preceding volumes. Figure 111C is a chart that is sometimes supplied by the manufacturer or constructed from the collector family of curves from the ratings supplied by the manufacturer. Since the maximum power dissipation limits of the transistor can not be exceeded, it is obvious that both maximum current and voltage cannot be applied to the transistor simultaneously. The line marked "absolute maximum limit" in Figure 112C is constructed from maximum collector current and voltage points at given base current points. This line encloses an area in which it is possible to operate the transistor. Operation beyond this line will result in breakdown of the transistor. Operation in the dotted area in Figure 112C is only possible in the switching mode of the transistor. We previously discussed that the transistor can be operated beyond its maximum steady state power dissipation hyperbole if it is operated in the switching mode and does not spend too much time in the area of maximum power dissipation. Operating repetition rate in the dotted area in Figure 112C, however, is going to be limited by the thermal time constant of the transistor. If the repetition rate of switching is such that the transistor spends considerable time in the area of maximum power dissipation, the transistor will be harmed when operating in the dotted region. If the transistor rests in the active region, or has its quiescent operating point in the active region, it must be operated with its load line in the cross-hatched area in Figure 112C. We might draw the cross-hatched area in Figure 112C by constructing a line tangent to the maximum power hyperbole and extend it to the maximum voltage point and cross-hatching all the area below this. This would be the permissable area for construction of the load line for this transistor for an amplifier or a switch that has a resting state in the active region.

POWER TRANSISTOR SPECIFICATIONS AND RATINGS:

In addition to the curves and the parameter, the manufacturer generally specifies the following:

Frequency Cut-Off for Current Gain:

f_{α_e} or $f_{h_{FE}}$ - the frequency at which the forward current gain (h_{FE}) is reduced to 0.707 of its low frequency value (low frequency value to mean the standard frequency at which the current gain was measured). This represents a 3db reduction in current gain. $f_{h_{FB}}$ or f_{α_b} is the frequency at which the forward current gain of the transistor in the common base configuration is reduced to 0.707 of its low frequency value.

f_T:

f_T is the frequency at which the low frequency common emitter, forward current gain is reduced to unity. This is the gain bandwidth product of the transistor.

Switching Time:

Delay time, rise time, fall time, and storage time of the transistor are listed. These characteristics were covered in an earlier volume, and the earlier coverage is valid here as well.

Collector Cut-Off Current (I_{CBO}):

The collector reverse leakage current plus thermally generated minority carrier current, collector to base, with the emitter lead d-c open circuited.

Collector Saturation Voltage [$V_{CE(sat)}$]:

The minimum collector voltage necessary to sustain normal transistor action under specified collector current. At a voltage less than $V_{CE(sat)}$, the collector becomes forward biased, and the transistor is in saturation. The saturation resistance ($R_{CE[sat]}$) is sometimes given, and the product of $R_{CE(sat)}$ and the saturation collector current gives the value of $V_{CE(sat)}$.

MAXIMUM RATINGS:

Collector Breakdown Voltage:

The voltage across the collector junction at which the collector begins to avalanche. This is the maximum allowable collector to base d-c voltage. These voltages are also specified by configuration, as discussed in an earlier volume. For instance, BV_{CBO}, as shown in Figure 112C, is the breakdown voltage, collector to base, with the emitter d-c open circuited. In other words, this is the breakdown voltage of the collector-base diode, the voltage at which the collector base diode begins to avalanche. The breakdown voltages are determined by the temperature, which in turn determines the number of minority carriers in the base of the transistor. Since the injection of carriers from the emitter into the base increases the number of minority carriers available and allows the transistor to start avalanche at a lower reverse voltage, BV_{CEO} and BV_{CES} occur at a lower voltage than BV_{CBO}. This also is covered in an earlier volume.

Maximum Power:

The thermal considerations as applied to diodes and transistors that were discussed in the earlier volumes are valid when dealing with power transistors as well. The considerations for using a heat sink and determining the value of a heat sink and the maximum operating power of the transistor when thermal resistance is known may be used here in the same manner they were used in earlier volumes.

TYPICAL CIRCUIT:

Figure 113 shows a typical single-ended power amplifier, such as might be found in a Tektronix oscilloscope. It is being used as a power supply regulator in the Type 422, portable oscilloscope.

Transistors Q624 and Q634 make up what is termed an "emitter coupled comparator amplifier". This circuit can be compared to the vacuum tube "cathode coupled

comparator amplifier" adequately covered in the Tektronix publication, "Typical Oscilloscope Circuitry".

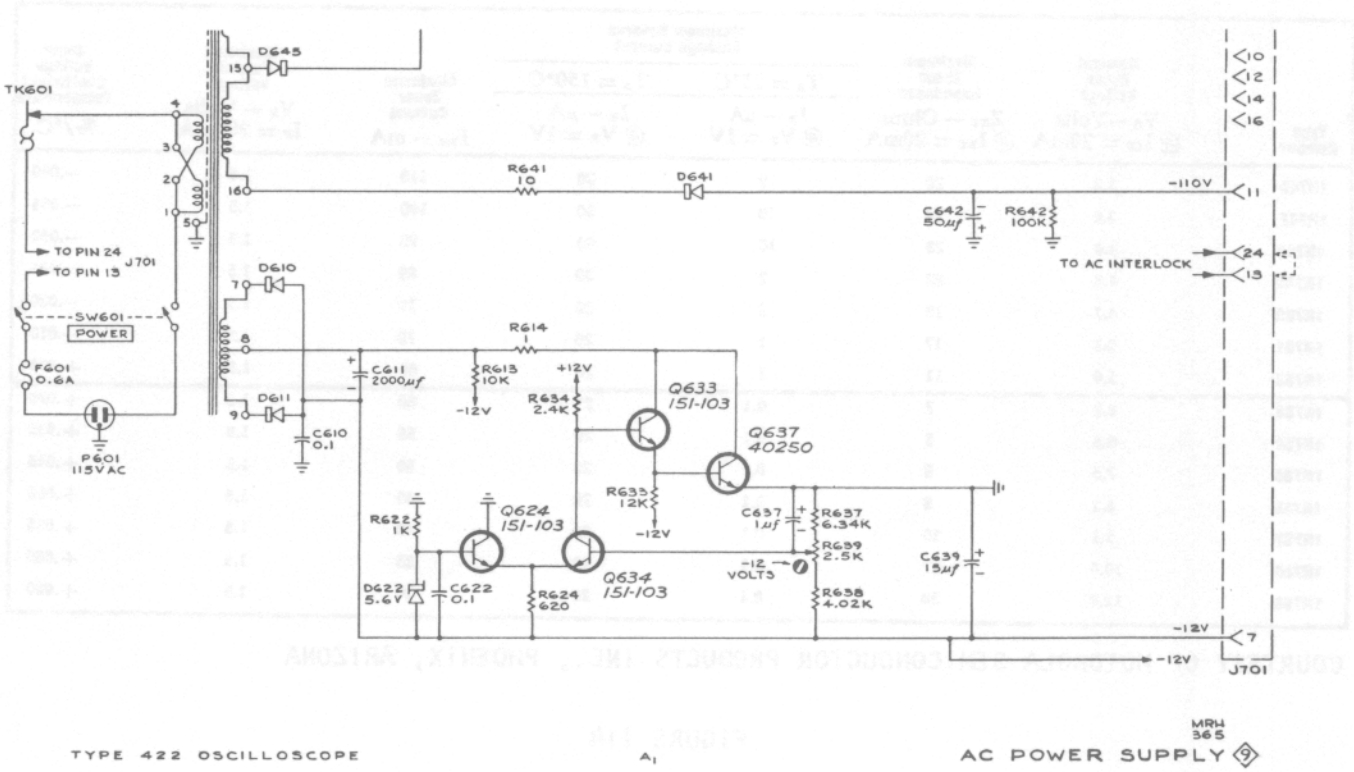

FIGURE 113

The circuit can be compared to the differential amplifier previously discussed. Any <u>difference</u> in the levels at the bases of the transistors results in an error signal delivered to Q633, and in turn to Q637. Zener diode D622 establishes the reference voltage on the base of Q624 with respect to the supply that the emitter resistor is returned to. The base of Q625 will always be 5.6v more positive than the bottom of R624. (Remember: electron current flows <u>with</u> the arrow in a zener diode symbol.) The zener diode is in a breakdown mode.

D622 is a 1N752, 400mwatt, 5.6v, 5% zener diode. Its characteristics are shown in Figure 114. Since D622 is in the breakdown area near the changeover point between avalanche and tunnel breakdown modes, it has a very low temperature coefficient of voltage. D622 has a temperature coefficient of voltage of +0.005%/°C. In other words, the voltage across the zener diode terminals will only change by 0.005% for each °C of temperature change. Therefore, the reference voltage at the base of Q624 will be very stable over a range of temperatures.

Type Number	Nominal Zener Voltage V_Z — Volts @ I_{ZT} = 20mA	Maximum Zener Impedance Z_{ZT} — Ohms @ I_{ZT} = 20mA	Maximum Reverse Leakage Current $T_A = 25°C$ I_R — μA @ V_R = 1V	Maximum Reverse Leakage Current $T_A = 150°C$ I_R — μA @ V_R = 1V	Maximum Zener Current I_{ZM} — mA	Maximum Forward Voltage V_F — Volts I_F = 200mA	Zener Voltage Coefficient Temperature %/°C
1N746	3.3	28	10	30	110	1.5	−.060
1N747	3.6	24	10	30	100	1.5	−.055
1N748	3.9	23	10	30	95	1.5	−.050
1N749	4.3	22	2	30	85	1.5	−.035
1N750	4.7	19	2	30	75	1.5	−.020
1N751	5.1	17	1	20	70	1.5	−.010
1N752	5.6	11	1	20	65	1.5	+.005
1N753	6.2	7	0.1	20	60	1.5	+.020
1N754	6.8	5	0.1	20	55	1.5	+.035
1N755	7.5	6	0.1	20	50	1.5	+.045
1N756	8.2	8	0.1	20	45	1.5	+.050
1N757	9.1	10	0.1	20	40	1.5	+.055
1N758	10.0	17	0.1	20	35	1.5	+.060
1N759	12.0	30	0.1	20	30	1.5	+.060

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FIGURE 114

Let's assume that the -12v supply in Figure 113 tried to become more negative or go beyond -12v. Since the drop across D622 is constant, the base of Q624 will become more negative, and its emitter will follow. The voltage drop between the base of Q634 and the bottom of R624 is not constant, however, and 0634 sees an error signal that requires a reduction in current. The reduction in current in Q634 allows the collector to become more positive. Q633 is an emitter follower, therefore, the positive excursion is applied to the base of Q637. This reduces the forward bias on Q637, increasing its resistance to drop the added voltage. The -12v supply returns to normal. The variable resistor R639 is adjusted in the initial calibration procedure to provide a voltage at the base of Q634 that results in the -12v supply being exactly -12v. Any changes in line voltage or load current (within the specifications of the circuit) are compensated for by the amplifier. Q637 is a silicon NPN, high power transistor. Its thermal resistance, junction to case (θ_{JC}) is 6°C/watt. It is mounted on a heat sink which has a dissipating area of approximately 5 square inches and is 1/32 of an inch think. From table 10 in Volume 6 of this series, this represents a heat sink thermal resistance (θ_{SA}) of

12°C/watt. The transistor is mounted using a dry mica insulating washer, which gives a thermal resistance, case to heat sink (Θ_{CS}), of 0.8°C/watts. Total thermal resistance (Θ_{JA}) is the sum of all the thermal resistances, or:

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$$

$$\Theta_{JA} = 6°C/w + 0.8°C/w + 12°C/w = 18.8°C/w$$

The maximum operating junction temperature (T_{Jmax}) of a 40250 transistor is 175°C.

$$\text{Maximum power dissipation } (P_{Dmax}) = \frac{T_{Jmax} - T_A}{\Theta_{JA}}$$

where: T_A = ambient or surrounding air temperature

T_{Jmax} = maximum junction operating temperature

For Q637 in Figure 113, at 25°C ambient temperature, the maximum power dissipation is:

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\Theta_{JA}} = \frac{175°C - 25°C}{18.8°C/w}$$

$$P_{Dmax} = 7.98w$$

Before reading on, if we measured 5.3v from collector to emitter of Q637 in Figure 113, how much current can it handle at 25°C?

The current capability can be found by dividing the maximum power by the voltage:

$$I_{max} = \frac{P_{Dmax}}{E} = \frac{7.98w}{5.3v} \approx 1.5A$$

We have applied some of the basics that were previously discussed to the foregoing example. The particular power supply that we were discussing provides a reference voltage for other supplies in the a-c power supply of the Tektronix Type 422 portable oscilloscope. The zener diode used has a low temperature coefficient of voltage and silicon, NPN transistors are used in the amplifier.

DARLINGTON OR COMPOUND CONFIGURATION:

When high input resistance and high β are required, a configuration such as shown in Figure 115 can be used. An extremely high β and input resistance can be accomplished with this type of connection.

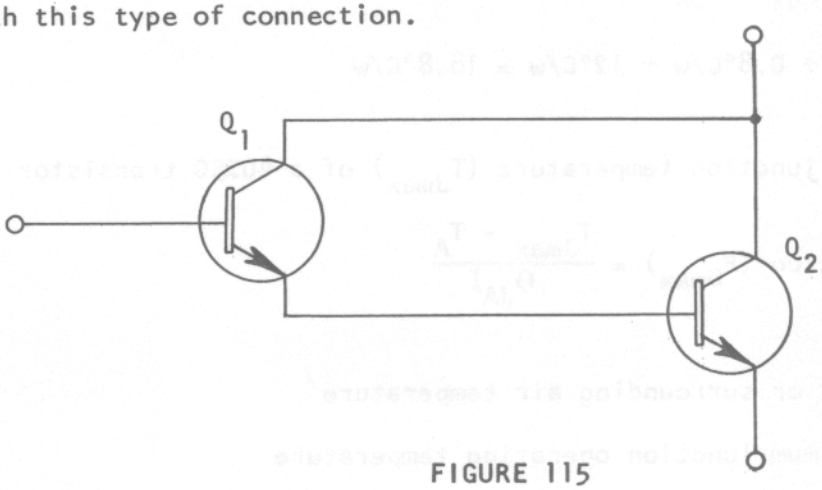

FIGURE 115

This configuration is referred to in a number of ways. Compound connection and darlington circuit are two. Notice in Figure 115 that the emitter current of Q_1 is supplied by the base of Q_2. The collectors are connected together, and we have a three-terminal device again. Some manufacturers are supplying a darlington connection in one encapsulation.

To see how the darlington circuit can offer such a high input resistance and equivalent β, consider the currents and values of α and β in Figure 116.

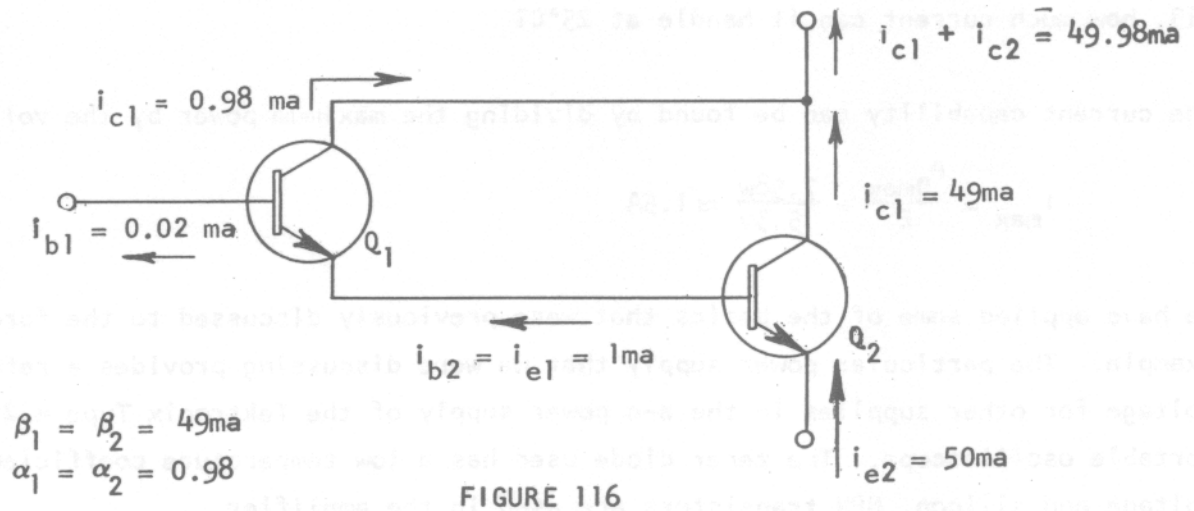

FIGURE 116

If the configuration in Figure 116 were placed in a black box, such as shown in Figure 117, and measurements made to obtain parameters, the results would not indicate the number of transistors.

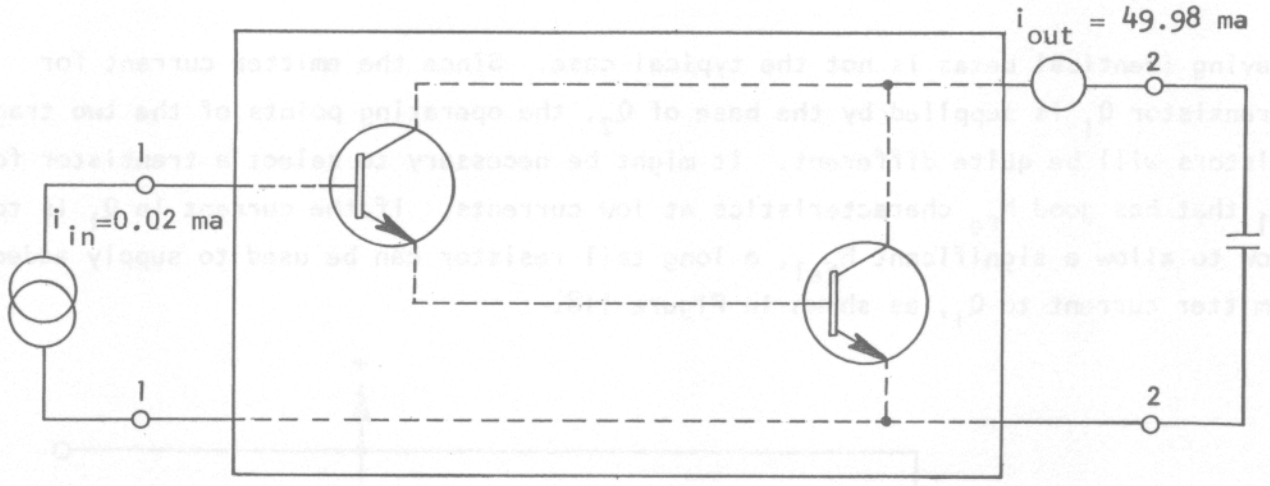

FIGURE 117

If a measurement is made to obtain β or h_{fe}, as shown in Figure 117, the equation is:

$$h_{fe} = \frac{\Delta i_{out}}{\Delta i_{in}} = \frac{\Delta i_c}{\Delta i_b} = \frac{49.98 \times 10^{-3}}{0.02 \times 10^{-3}} = 2499$$

Therefore, a measurement of h_{fe} on the configuration in Figure 116 gives an equivalent beta of nerely 2500. Equivalent collector current is $i_{c1} + i_{c2}$, and:

$$i_{c1} = h_{fe1}\, i_{b1}$$

$$i_{b2} = h_{fe2}\, i_{b2}$$

$$i_{b2} = i_{e1}$$

$$i_{b2} = (h_{fe1} + 1)\, i_{b1}$$

$$i_{c2} = (h_{fe1} + 1)\, i_{b1}\, h_{fe2}$$

$$i_{c(eq)} = i_{c1} + i_{c2} = i_{b1}\, h_{fe1} + i_{b1}\, (h_{fe1} + 1)\, h_{fe2}$$

$$i_{c(eq)} = i_{b1}\, [h_{fe1} + (h_{fe1} + 1)\, h_{fe2}]$$

and:

$$h_{fe(eq)} = h_{fe1} + (h_{fe1} + 1)\, h_{fe2}$$

Since we have assumed equal betas in the configuration in Figure 116:

$$h_{fe(eq)} = 49 + (50)\ 49 = 2499$$

Having identical betas is not the typical case. Since the emitter current for transistor Q_1 is supplied by the base of Q_2, the operating points of the two transistors will be quite different. It might be necessary to select a transistor for Q_1 that has good h_{fe} characteristics at low currents. If the current in Q_1 is too low to allow a significant h_{fe1}, a long tail resistor can be used to supply added emitter current to Q_1, as shown in Figure 118.

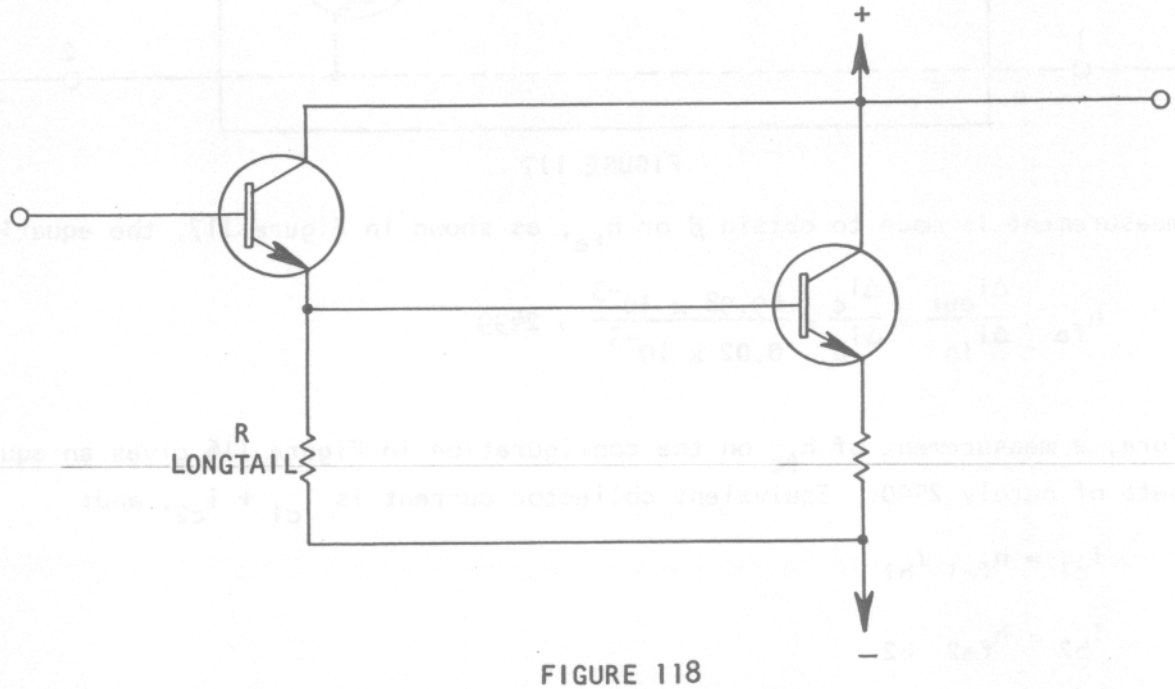

FIGURE 118

Some of the signal current will be lost in the added resistor, but the increase in the h_{fe} of transistor Q_1 will probably more than compensate for this.

A quick approximation of the equivalent h_{fe} of the darlington circuit is simply:

$$h_{fe(eq)} \approx h_{fe1}\ h_{fe2}$$

and if the betas are near equal:

$$h_{fe(eq)} \approx h_{fe}^{2}$$

DARLINGTON INPUT RESISTANCE:

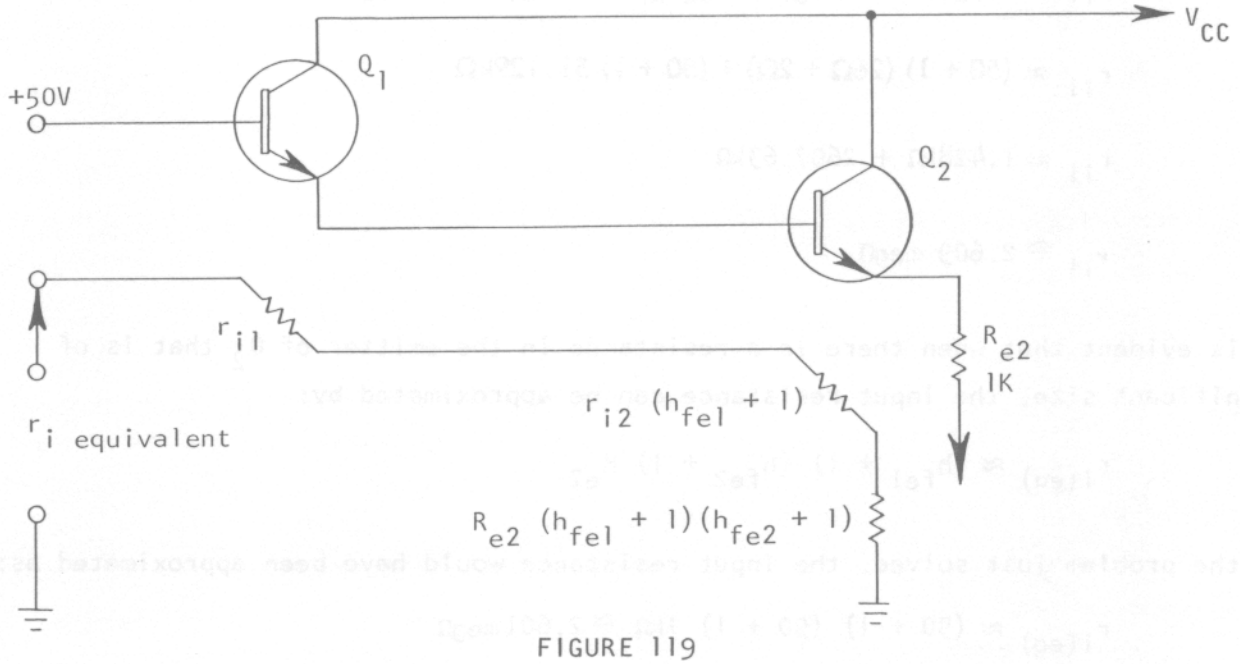

FIGURE 119

tor Q_1 and ground. The input resistance of Q_1 is increased by the input resistance of Q_2, which is increased by the resistor R_e in the emitter. To simplify the problem, let's assume that transistors Q_1 and Q_2 in Figure 119 both have a d-c and a-c beta of 50 at their respective operating points. This is not very likely, but in a hypothetical problem, we can assume it. Just don't expect it to be the rule.

The base of Q_1 is at +50v. If we neglect the base-emitter drops of the two transistors, we can say that the emitter of Q_1 and, therefore, the emitter of Q_2 is near +50v. This requires R_{e2} to drop approximately 50v.

$$I_{E2} \approx \frac{50v}{1k} \approx 50ma$$

$$r_{e2} \approx \frac{26}{50ma} \approx 0.52\Omega$$

$$r_{i2} \approx (h_{fe2} + 1)\ (r_{e2} + r_{bulk2}) + (h_{fe2} + 1)\ R_{e2}$$

$$r_{i2} \approx (50 + 1)\ (0.52\Omega + 2\Omega) + (50 + 1)\ 1k\Omega \approx 51.129k\Omega$$

The emitter current of Q_1 is the base current of Q_2, or approximately 1ma; therefore:

$$I_{E1} \approx 1ma$$

$$r_{e1} \approx \frac{26}{1ma} = 26\Omega$$

$$r_{il} \approx (h_{fe1} + 1)\ (r_{e1} + r_{bulk}) + (h_{fe1} + 1)\ r_{i2}$$

$$r_{il} \approx (50 + 1)\ (26\Omega + 2\Omega) + (50 + 1)\ 51.129k\Omega$$

$$r_{il} \approx 1.428k\Omega + 2607.63k\Omega$$

$$r_{il} \approx 2.609\ meg\Omega$$

It is evident that when there is a resistance in the emitter of Q_2 that is of significant size, the input resistance can be approximated by:

$$r_{i(eq)} \approx (h_{fe1} + 1)\ (h_{fe2} + 1)\ R_{e2}$$

In the problem just solved, the input resistance would have been approximated as:

$$r_{i(eq)} \approx (50 + 1)\ (50 + 1)\ 1k\Omega \approx 2.601\ meg\Omega$$

TYPICAL DARLINGTON CIRCUIT:

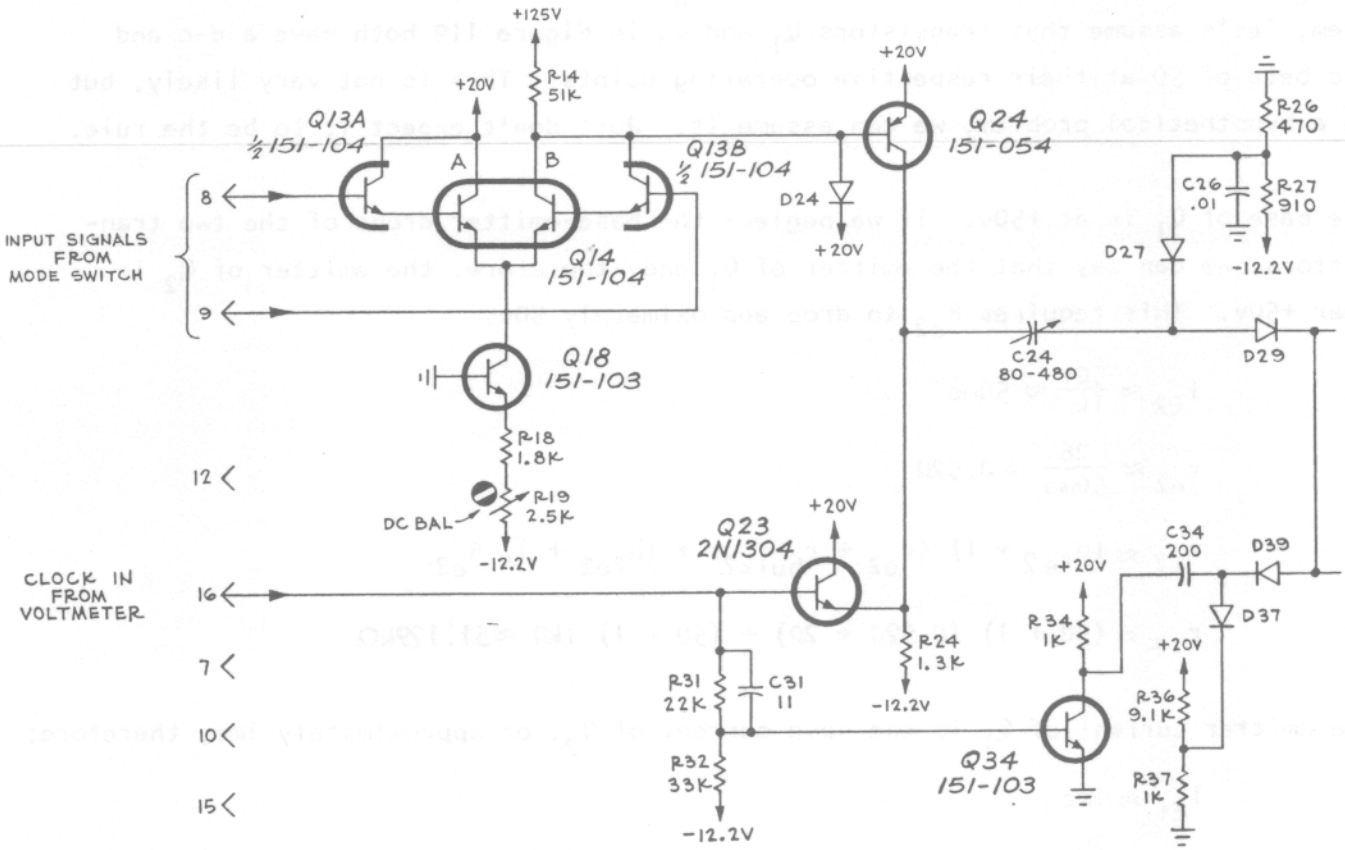

FIGURE 120

Figure 120 shows two darlington connections being used as the two sides of a signal comparator or difference amplifier. This is a circuit that we observed earlier in this volume when discussing the use of a long tailing transistor. The circuit is in the Signal Comparator in the Tektronix Type 6R1A Digital Unit. It includes several of the approaches that we have been discussing in this volume.

HIGH FREQUENCY CONSIDERATIONS:

Miller Effect:

Miller effect in transistors can be compared to Miller effect in vacuum tube amplifiers, discussed in the book, "Typical Oscilloscope Circuitry". We will discuss Miller effect first because it deals primarily with capacitive effects, external of the transistor itself. It does play a part in limiting the high frequency performance of the transistor.

Consider the transistor in Figure 121. Note that the stray and interelectrode capacitance between base and emitter and base and collector will shunt the input of the transistor.

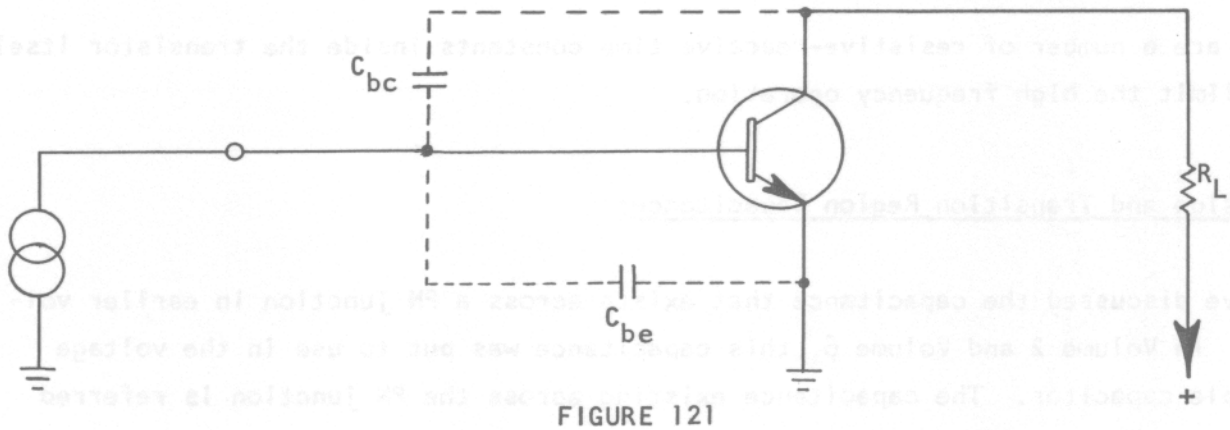

FIGURE 121

The input generator must supply current to charge both capacitances. With the common emitter configuration, however, the collector voltage is 180° out of phase with respect to the base voltage (normal phase inversion), assuming no other phase shift. Assuming a voltage gain of 10 in the configuration in Figure 121, a negative

going 1mv change at the base will be accompanied by a positive going 10mv at the collector. Since the base side of C_{bc} has moved negative by 1mv and the collector side of C_{bc} has moved positive by 10mv, the input generator must supply enough current to change the voltage on C_{bc} by 11mv. To the input generator, this simply looks like a larger capacitance. The effective C_{bc} can be calculated by:

$$C_{bc(Miller)} = C_{bc} (1 - A_v)$$

When A_v is negative, as it is with the common emitter configuration, $(1 - A_v)$ becomes $1 - (-A_v) = 1 + A_v)$. This effective magnification of the collector-base capacitance is referred to as Miller effect. Miller effect is very much a problem in vacuum tube triode configurations, with their reverse biased, high resistance inputs. Of course, the Tetrode and Pentode vacuum tubes place another isolating grid between the control grid and plate.

The transistor with its forward biased, low resistance input has the input capacitance shunting a much lower input resistance than its vacuum tube counterpart in the majority of applications.

High Frequency Models:

There are a number of resistive-reactive time constants inside the transistor itself that limit the high frequency operation.

Diffusion and Transition Region Capacitance:

We have discussed the capacitance that exists across a PN junction in earlier volumes. In Volume 2 and Volume 6, this capacitance was put to use in the voltage variable capacitor. The capacitance existing across the PN junction is referred to in a number of ways. Transition capacitance, carrier capacitance, and junction capacitance are some. We will refer to it as transition capacitance.

The transition capacitance is a result of the electric field existing across the transition region and is, therefore, voltage controlled. (Remember, the diode was referred to as a "voltage variable capacitor".)

The capacitance referred to as "diffusion capacitance" is a result of the effective stored charge of diffusing carriers. Therefore, diffusion capacitance is essentially current controlled. Table 8 in Volume 6 represented the transition capacitance at the emitter and collector junctions with variable capacitor symbols across the junctions, and the charge in the diffusion capacitance was represented while the diffusion capacitance was part of the parameter "Storance". The physical or charge control model used in Table 8 of Volume 6 is one method of representing the electrical characteristics of the transistor so that they closely relate to the physical transistor. We will use a different model for this discussion to give one more approach to transistor analysis.

Suppose we start with the low frequency T equivalent circuit, such as shown in Figure 122.

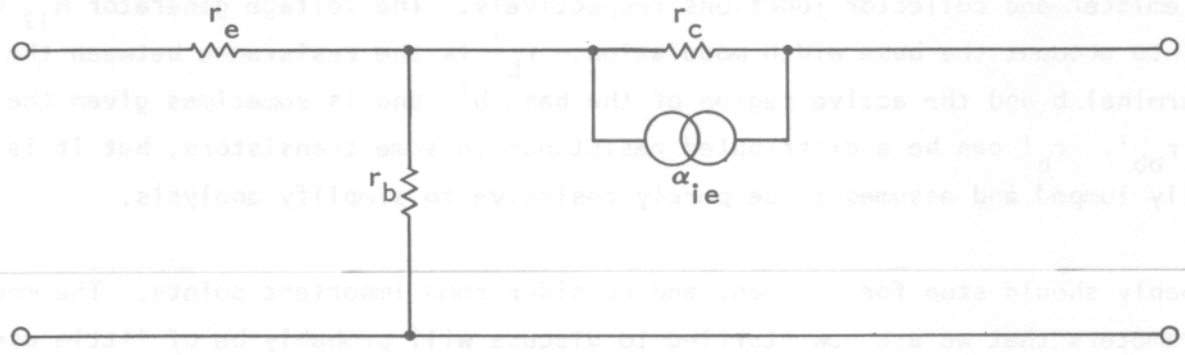

FIGURE 122

This model is valid at the standard frequency at which the parameters were measured (generally 1KC), and probably up through the audio frequencies. At the medium frequencies, transition capacitance starts to play a limiting role along with internal base modulation. To understand internal base modulation, you may want to review Table 9 in Volume 6. The active base width was shown as a determining factor in emitter current in Table 9. When the collector voltage varies, the width of the collector transition region varies and, therefore, the width of the active region of the base. Modulation of the emitter current is the result, and this feedback can be represented by a voltage generator in the emitter circuit allowing r_e to remain the same. This is illustrated in Figure 123.

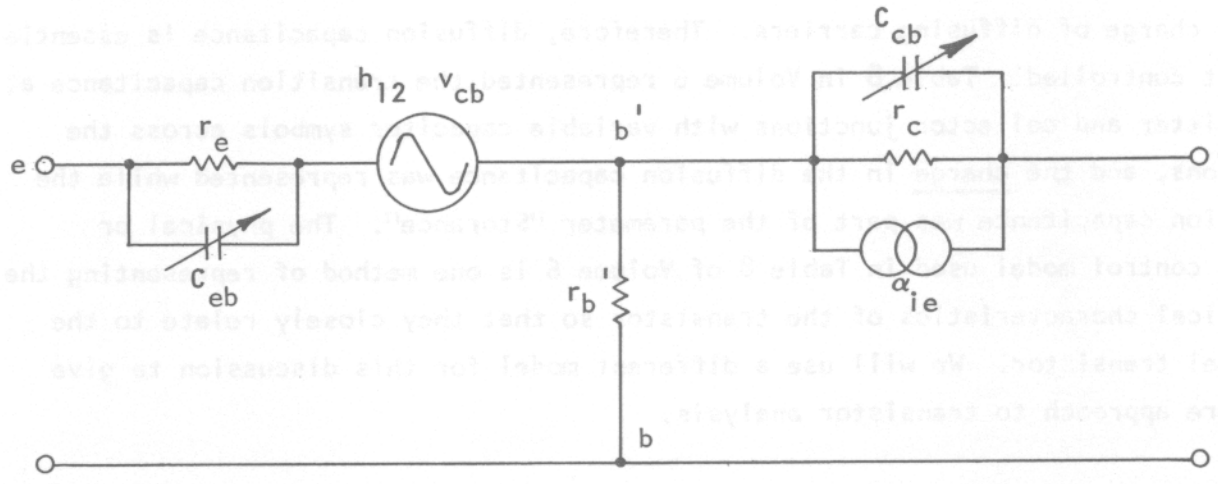

FIGURE 123

The capacitors C_{eb} and C_{cb} represent the voltage variable transition capacitances at the emitter and collector junctions respectively. The voltage generator $h_{12} v_{cb}$ takes into account the base width modulation. r_b' is the resistance between the base terminal b and the active region of the base b', and is sometimes given the symbol r_{bb}'. r_b' can be a distributed resistance in some transistors, but it is typically lumped and assumed to be purely resistive to simplify analysis.

We probably should stop for a moment and consider some important points. The models and parameters that we are now starting to discuss will probably be of little use to the analysis and design of transistor <u>circuits</u>. The parameters are difficult to measure and unweidly for design and analysis. The models and approaches will point out the important limiting parameters given by the manufacturer, and allow the formulation of less demanding approaches to the selection of high frequency transistors and design and analysis of high frequency circuits.

Consider the model in Figure 124. The resistance r_b' is shown as a distributed resistance in Figure 124. The collector capacitance is shown as being essentially transition capacitance (C_{tc}). The collector junction is reverse biased, involving high electric fields, and as long as there is not significant collector storage (see Table 8, Volume 6), the capacitance is primarily transition capacitance. The emitter capacitance is shown as being essentially diffusion capacitance. The emitter-base junction is a forward biased junction (typically), and the diffusing carrier density, adjacent to the junction, is high.

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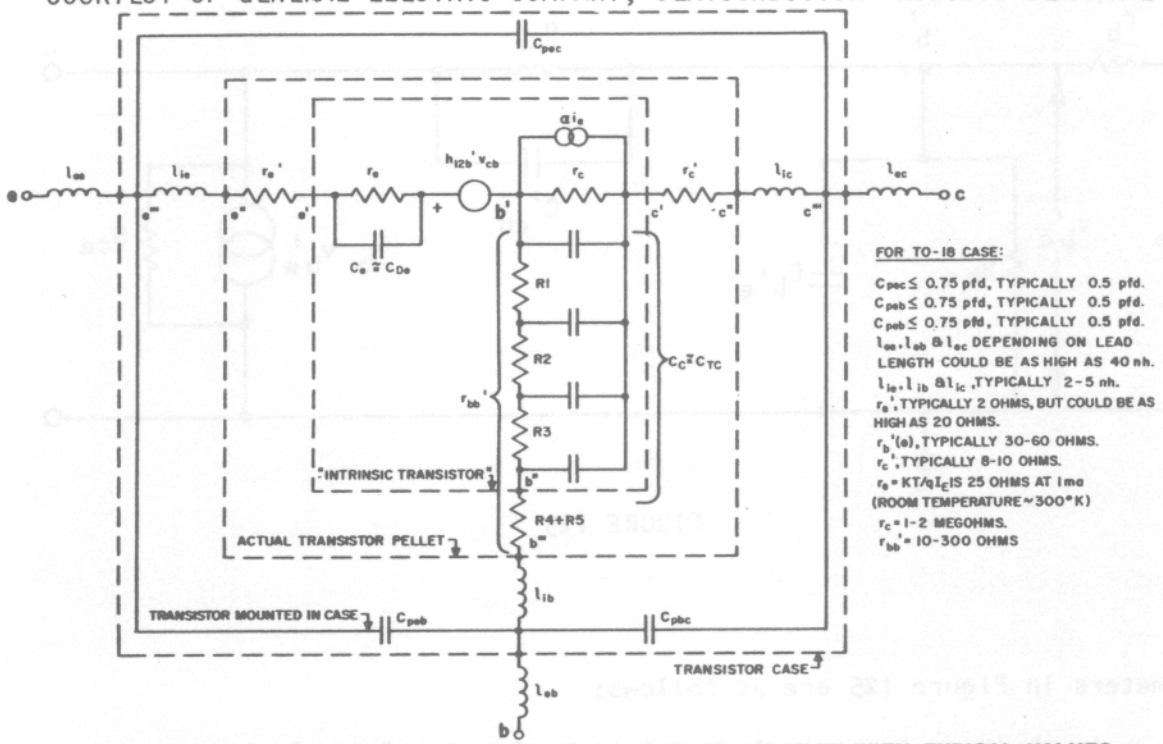


MODEL OF REASONABLY COMPLETE HIGH FREQUENCY TRANSISTOR WITH TYPICAL VALUES
(IN HF T-EQUIVALENT CIRCUIT)

FIGURE 124

Resistors r_e', r_b', and r_c' in Figure 124 are a combination of the bulk resistance and contact resistance between the active regions and the transistor terminals. l_{ie}, l_{ib}, and l_{ic} are the lead inductances inside the encapsulation, and l_{ee}, l_{eb}, and l_{ec} are the inductances of the leads, external of the encapsulation. C_{pec}, C_{pbc}, and C_{peb} are the capacitances associated with the encapsulation.

It should be evident from Figure 124 that such a model would be very difficult to work with for general analysis and design. A simplified model and approach is called for.

The lumped diffusion model in Table 8 of Volume 6 was one simplification. It dealt with the charge control approach to analyzing the transistor's characteristics, along with its high frequency and switching speed limitations. We will use the hybrid π approach here to give another example of a model and analysis approach.

Figure 125 is the hybrid π model for medium frequencies. As we discuss it, you will probably be able to relate it to the lumped diffusion model.

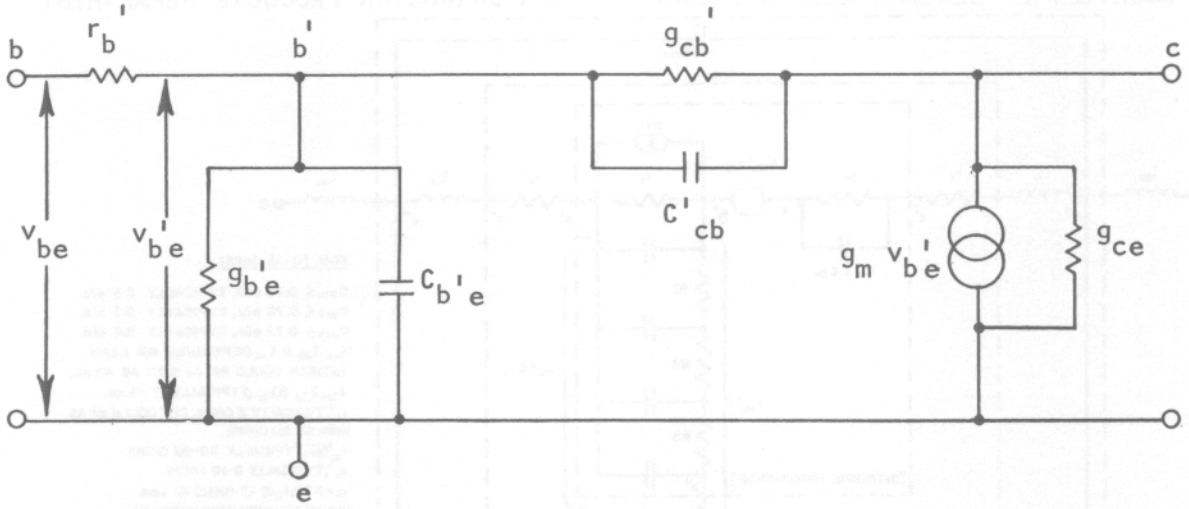


FIGURE 125

The parameters in Figure 125 are as follows:

r_b' = bulk resistance plus contact resistance from the base terminal to the active base region (b to b')

$g_{b'e}$ = the emitter diffusion conductance as seen from the base $(\frac{1}{\beta r_e})$

C_{be}' = essentially the emitter diffusion capacitance. The time constant

$$\frac{g_{b'e}}{C_{b'e}} \approx r_e \beta C_{b'e} \approx \frac{1}{2\pi f_t}$$

This, by the way, is the time constant $\tau_{\beta f}$ in the lumped diffusion model, Table 8, Volume 6.

$C_{c'b}$ = essentially the collector transition capacitance

$g_{c'b}$ = essentially the conductance from the collector to the active region of the base $\approx (\frac{1}{r_c}$ or $h_{ob})$

$g_m v_{b'e}$ = g_m is essentially the reciprocal of r_e. $v_{b'e}$ is the signal voltage from the active region of the base to the emitter terminal. The product of the two is the current in the output circuit as a result of $v_{b'e}$.

$$g_m = \frac{\alpha_{ie}}{v_{be}'} = \frac{\alpha}{r_e} \approx \frac{1}{r_e}$$

$$\left(\frac{1}{r_e} = \frac{i_e}{v_b'_e}\right)$$

g_{ce} = the feedback conductance. If $v_b'_e$ is assumed constant, and a voltage change (of appropriate frequency) is applied, collector to emitter, the conductance:

$$g_{ce} \approx \frac{i_c}{v_{ce}}$$

$$i_c \approx \frac{v_{ce}\, h_r'_e}{r_e}$$

(where $h_r'_e\, v_{ce}$ is the feedback generator)

therefore:

$$g_{ce} \approx \frac{h_r'_e}{r_e}$$

Any external emitter resistance or inductance (to include r_e') will reduce g_m. The value of g_m after external resistance and inductance in the emitter has been taken into account can be found by:

$$g_m' = \frac{g_m}{1 + g_m\sqrt{r_{e(external)}^2 + X_L^2}}$$

where: $R_{e(external)}$ is the sum of all series external resistance in the emitter lead

X_L is the inductive reactance in the emitter lead

The cut-off frequency for g_m, where g_m has been reduced to 0.707 of its low frequency value as a result of the shunting by $C_b'_e$, is given by:

$$f_{gm(3db)} = \frac{\frac{1}{g_b'_e} + r_b'}{2\pi C_b'_e\, r'_b \frac{1}{g_b'_e}}$$

It can be seen from the hybrid π model, that the factors discussed in Table 8 in Volume 6 are evident here too. Low values of C_{be}' and r_b' are prerequisites for

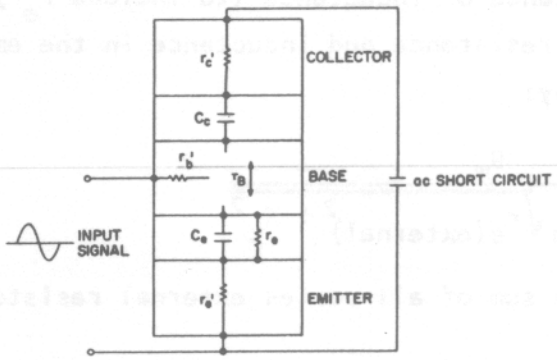
high frequency operation. Adding gold (gold diffused base) in the base to reduce r_b' and the frequency limiting time constant was discussed. Low values of collector capacitance is also indicated due to its providing feedback from the collector to the base. Manufacturers have specified f_{hfb} or $f\alpha_b$, and f_{hfe} or $f\alpha_e$ for high frequency transistors for sometime. These cut-off frequencies along with f_T were discussed in Volumes 3 and 6. They are given as:

$f_{hfb} = f\alpha_b$ = frequency at which h_{fb} (or α) is 0.707 of its low frequency (usually 1kc) value

$f_{hfe} = f\alpha_e$ = frequency at which h_{fe} (or β) is 0.707 of its low frequency (usually 1kc) value

f_T = frequency at which h_{fe} (or β) is equal to one or unity

There is another frequency, f_{MAX}, which is the maximum frequency of oscillations, and f_{MAX} is the frequency at which maximum available gain (M.A.G.) is reduced to unity.



VARIOUS TIME-CONSTANTS LIMITING THE GAIN-BANDWITH PRODUCT OF THE TRANSISTOR

COURTESY OF GENERAL ELECTRIC COMPANY, SEMICONDUCTOR PRODUCTS DEPARTMENT

FIGURE 126

Figure 126 shows the frequency limiting time-constants illustrated with resistors and capacitors, rather than the physical parameters, storance, combinance, and diffusance used in Table 8 in Volume 6.

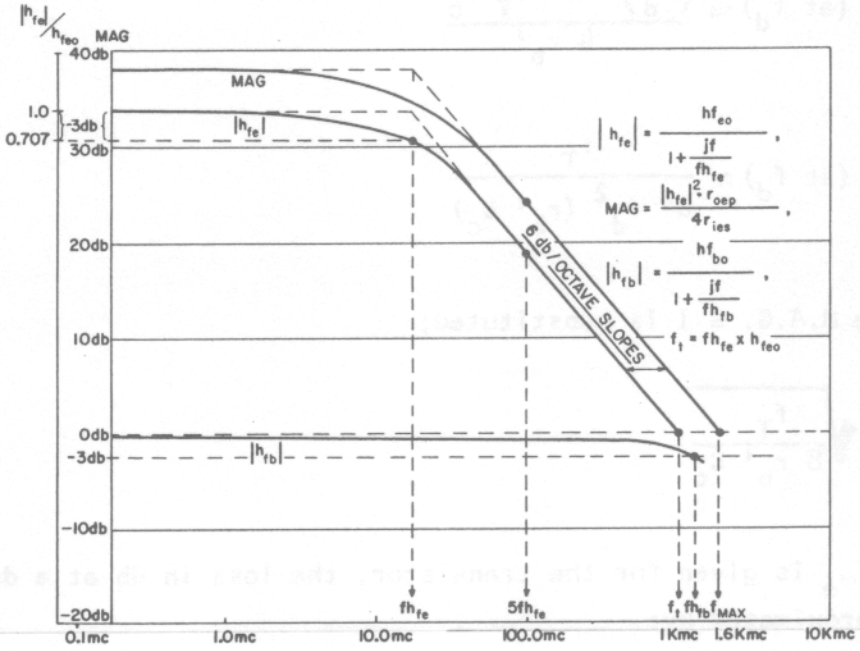
For the model in Table 8 of Volume 6, the frequency f_T could be found by:

$$f_T \quad \frac{1}{2\pi \tau_{\beta f}}$$

For the model in Figure 126, f_T is:

$$f_T = \frac{1}{[2\pi \tau_B + r_e (C_e + C_c)]}$$

In addition, if r_c', the collector bulk resistance, is a significant value, the time constant of r_c' and the collector transition capacitance must also be added.



MAG, $|h_{re}|$, $|h_{rb}|$ VS. FREQUENCY OF TYPICAL UHF TRANSISTOR

COURTESY OF GENERAL ELECTRIC COMPANY
SEMICONDUCTOR PRODUCTS DEPARTMENT

FIGURE 127

Figure 127 plots the frequency limitation parameters of a typical high frequency transistor.

From the curves in Figure 127, if one stays on the 6db/octave slope;

$$h_{fe(at\ f_d)} = \frac{f_T}{f_d}$$

Therefore, h_{fe} at any desired frequency (f_d) along the 6db/octave slope can be found when f_T is known. h_{fe} at any frequency down to f_{hfe} can be found with reduced accuracy.

$$\text{M.A.G. (at } f_d) = \frac{h_{fe(\text{at } f_d)}^2 \; \frac{1}{2\pi f_T C_c}}{4 r_b'}$$

$$h_{fe(\text{at } f_d)}^2 = \left(\frac{f_T}{f_d}\right)^2$$

therefore:

$$\text{M.A.G. (at } f_d) \approx \frac{\left(\frac{f_T}{f_d}\right)^2 \; \frac{1}{2\pi f_T C_c}}{4 r_b'}$$

$$\text{M.A.G. (at } f_d) \approx \frac{f_T}{8\pi f_d^2 (r_b' C_c)}$$

and if f_{MAX} where M.A.G. = 1 is substituted;

$$f_{MAX} \approx \sqrt{\frac{f_T}{8 r_b' C_c}}$$

If only f_{hfe} or f_{α_e} is given for the transistor, the loss in db at a desired frequency can be approximated by:

$$\Delta db \approx 10 \log \left[\frac{1}{1 + \left(\frac{f_d}{f_{hfe}}\right)^2}\right]$$

Interstage losses between high frequency transistors can be calculated in the same manner by:

$$\Delta db \approx 10 \log \left[\frac{1}{1 + \left(\frac{f_d}{f_{co}}\right)^2}\right]$$

where:

$$f_{co} = \frac{1}{2\pi C_T r_T}$$

C_T = total shunting capacitance in the interstage network to include input and output capacitances of the transistors

r_T = total equivalent resistance of the interstage network to include the input and output resistances of the transistors

SECTION TWO

SWITCHING CIRCUITS:

The transistor as a switch, its advantages, limiting factors, and methods of measuring switching parameters were discussed in Volumes 3 and 6. The section in Volume 6 dealing with pulse and switching thermal limitations on power for diodes is applicable to switching transistors. The approaches outlined can be directly applied to the transistor as a switch. We will concentrate on the transistor switch as a circuit element in this portion of Volume 7.

SIMPLE TRANSISTOR SWITCH:

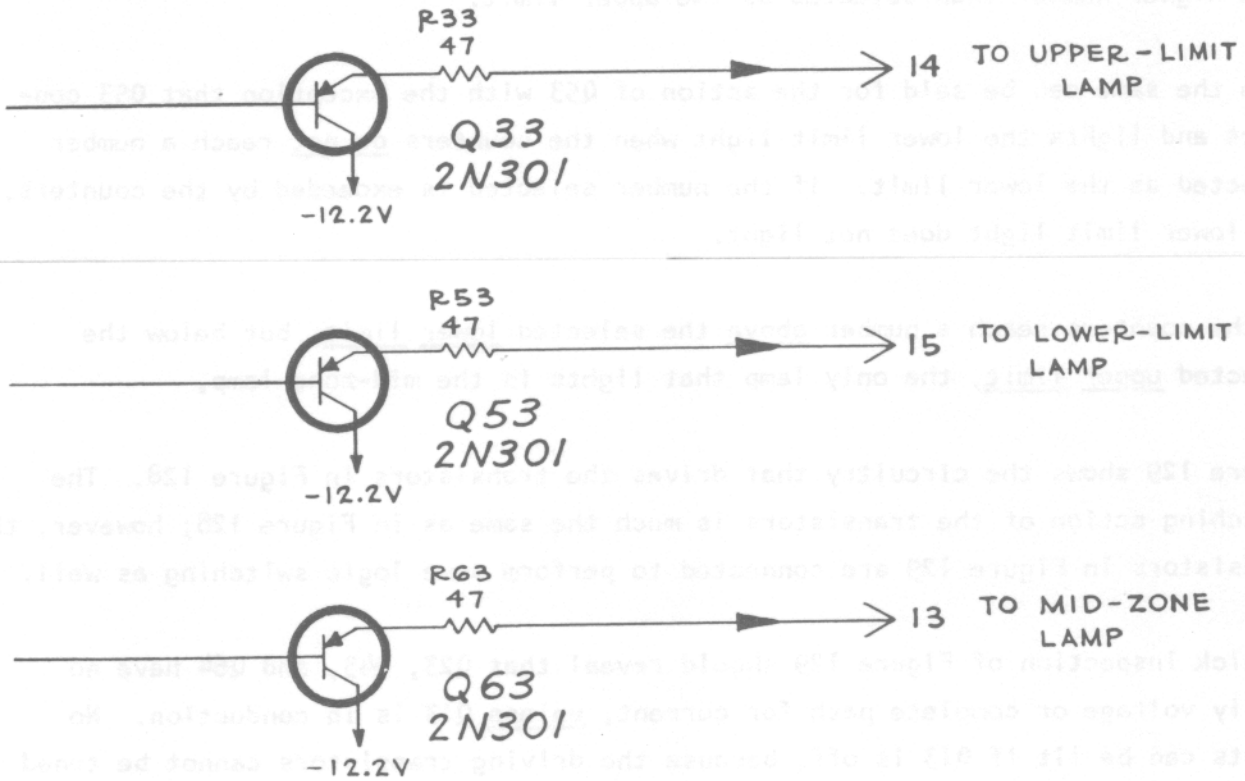


FIGURE 128

Figure 128 shows transistors being used in the 6R1A Digital Unit in a very simple switching arrangement.

The emitters of the transistors are returned to ground through a 47Ω resistor and a lamp. When the transistor conducts sufficient current, the lamp lights. When the transistor is not conducting, the lamp is out. The transistors in Figure 128 are simply acting as a switch that can handle sufficient power to illuminate the lamps, while requiring much less power from the circuit driving the transistors.

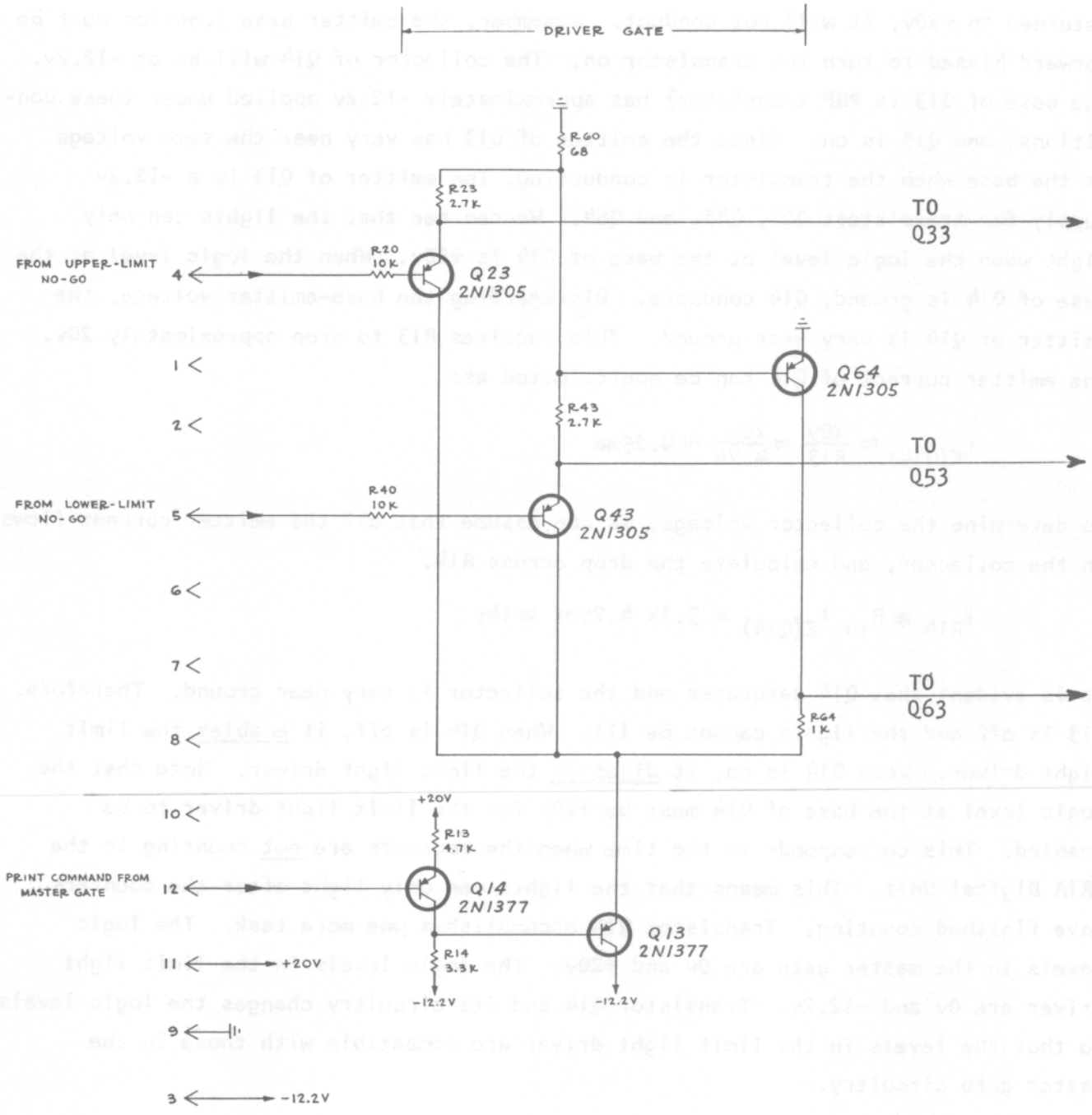
The transistors in Figure 128 are used to convey a message visually. In either of the two states, ON or OFF, the lights can indicate an occurance within the unit. As an example. Q33 lights the upper limit lamp when it conducts. There are counters in the 6R1A Digital Unit. It is possible to program the unit so that a count greater than a selected number will light the upper limit light. Knowing this, the light when on conveys one message, and a different message when off. When the upper limit light is on, the counters have counted to a number greater than the one selected as the upper limit. When the light is off, the counters have not counted to a higher number than selected as the upper limit.

Much the same can be said for the action of Q53 with the exception that Q53 conducts and lights the lower limit light when the counters do not reach a number selected as the lower limit. If the number selected is exceeded by the counters, the lower limit light does not light.

If the counters reach a number above the selected lower limit, but below the selected upper limit, the only lamp that lights is the mid-zone lamp.

Figure 129 shows the circuitry that drives the transistors in Figure 128. The switching action of the transistors is much the same as in Figure 128; however, the transistors in Figure 129 are connected to perform some logic switching as well.

A quick inspection of Figure 129 should reveal that Q23, Q43, and Q64 have no supply voltage or complete path for current, unless Q13 is in conduction. No lights can be lit if Q13 is off, because the driving transistors cannot be tuned on. Q13 has its emitter returned to ground through Q23, Q43, Q64, and their associated circuitry. In order to turn on Q13, we must drive its base negative with respect to its emitter. The logic levels (print command from master gate) at the base of Q14 are 0v and +20v. In other words, the base of Q14 will either be at +20v or ground potential. When the base of Q14 is at +20v with its emitter



TYPE GR1A

FIGURE 129

returned to +20v, it will not conduct. Remember, the emitter base junction must be forward biased to turn the transistor on. The collector of Q14 will be at -12.2v. The base of Q13 (a PNP transistor) has approximately -12.2v applied under these conditions, and Q13 is on. Since the emitter of Q13 has very near the same voltage as the base when the transistor is conducting, the emitter of Q13 is a -12.2v supply for transistors Q23, Q43, and Q64. We can see that the lights can only light when the logic level at the base of Q14 is +20v. When the logic level at the base of Q14 is ground, Q14 conducts. Disregarding the base-emitter voltage, the emitter of Q14 is very near ground. This requires R13 to drop approximately 20v. The emitter current of Q14 can be approximated as:

$$I_{E(Q14)} \approx \frac{20v}{R13} \approx \frac{20v}{4.7k} \approx 4.25ma$$

To determine the collector voltage, we can assume that all the emitter current flows in the collector, and calculate the drop across R14.

$$E_{R14} \approx R_{14}\ I_{E(Q14)} \approx 3.3k\ 4.25ma \approx 14v$$

It is evident that Q14 saturates and the collector is very near ground. Therefore, Q13 is off and the lights cannot be lit. When Q14 is off, it <u>enables</u> the limit light driver. When Q14 is on, it <u>disables</u> the limit light driver. Note that the logic level at the base of Q14 must be +20v for the limit light driver to be enabled. This corresponds to the time when the counters are <u>not</u> counting in the 6R1A Digital Unit. This means that the lights can only light after the counters have finished counting. Transistor Q14 accomplishes one more task. The logic levels in the master gate are 0v and +20v. The logic levels in the limit light driver are 0v and -12.2v. Transistor Q14 and its circuitry changes the logic levels so that the levels in the limit light driver are compatible with those in the master gate circuitry.

Let's look at the driver transistors, Q23, Q43, and Q64, in Figure 129. The logic levels at the bases of Q23 and Q43 are 0v and -12.2v. Their emitters are returned to ground through resistors. It should be evident that Q23 or Q43 will only conduct when the logic level at their base is -12.2v. When the counters count beyond the selected limits, the logic level at the base of the appropriate driver transistor becomes -12.2v. If the limits are not exceeded, the level at the base of transistors Q23 and Q43 is 0v, and they are non-conducting. If this is the case, there is

no forward bias applied to Q64, and it is non-conducting as well. When this condition exists, Q33 and Q53 remain off (base and emitter both essentially returned to ground). Q63, however, has its base returned to -12.2v when Q13 conducts, and the mid-zone lamp is lit. Therefore, when the circuit is enabled by a print command, if the selected limits have not been exceeded, the mid-zone lamp automatically lights.

If the logic level is -12.2v at the base of either Q23 or Q43 indicating that a selected limit has been exceeded, that transistor will conduct lighting the appropriate limit lamp. Either Q23 or Q43 conducting provides enough forward bias to turn on Q64, which makes it impossible to light the mid-zone lamp. This example indicates how the transistor operated as a simple switch can accomplish logic when arranged properly in appropriate circuitry.

MULTIVIBRATORS:

The vacuum tube versions of the multivibrators discussed here are covered in Chapter 10 of the Tektronix book, "Typical Oscilloscope Circuitry".

ASTABLE:

The astable free running multivibrator is a regenerative switching circuit that does not have a stable state. Consider the circuit in Figure 130. The configuration in Figure 130 is an astable multivibrator. The bases of the transistors are returned to the supply voltage through the base resistors, and any collector changes are coupled to the opposite base through the coupling capacitors. When power is applied, the voltage applied to the bases will start to draw biasing current, and the transistors will try and conduct. We must assume some unbalance in the circuit so that one transistor will conduct a bit more than the other, initially. Let's assume the collector voltage of Q_1 falls a bit more rapidly than the collector of Q_2. This change coupled back to the base of Q_2 will tend to reduce the Q_2 current. The collector voltage of Q_2 will rise, and this change is coupled back to the base of Q_1, further increasing the current in Q_1. This continues until Q_1 saturates, and Q_2 is off. The total voltage change that occurs at the collector of Q_1 is approximately equal to the supply voltage V_{CC}, neglecting any voltage across the

transistor [$V_{CE(sat)}$]. The base of Q_2 is driven negative by the total change at the collector of Q_1 (which in this case is approximately equal to V_{CC}), because C_C cannot change its charge instantaneously.

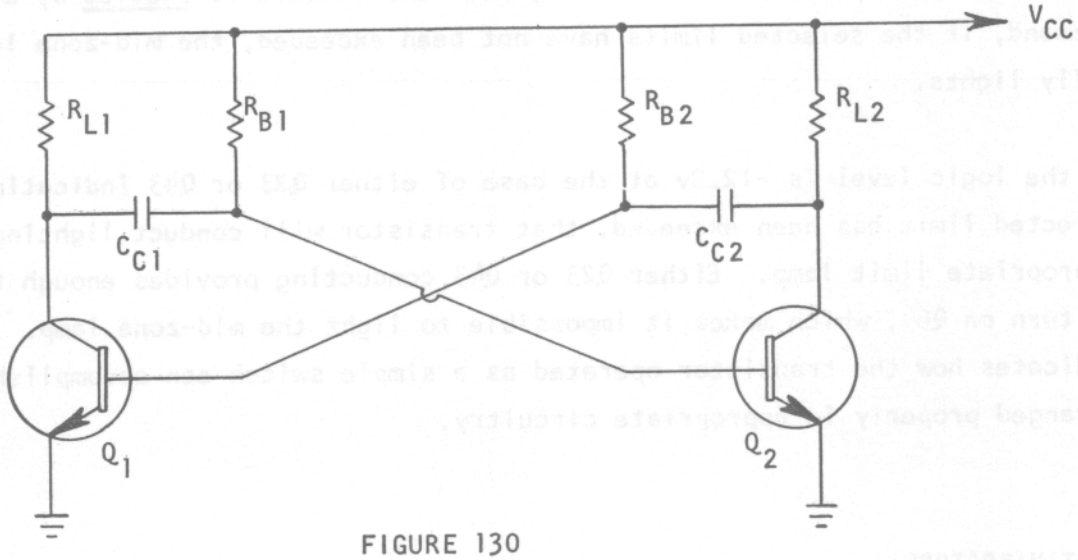


FIGURE 130

At the instant Q_1 becomes saturated, the condition exists as shown in Figure 131.

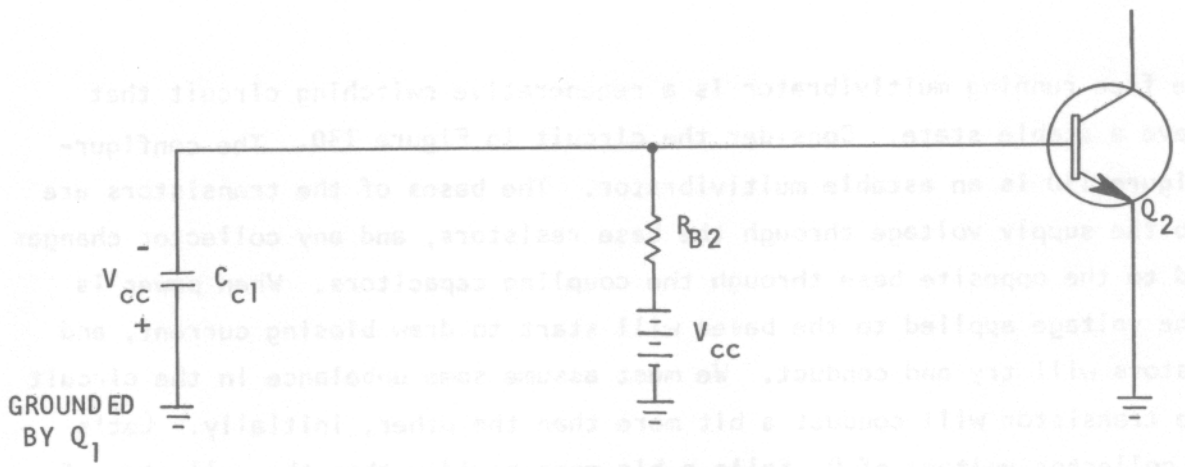


FIGURE 131

As shown in Figure 131, C_{C1} is charged with its plate that is connected to the base of Q_2, charged to approximately $-V_{CC}$ with respect to ground. R_{B1} is returned to the supply voltage $+V_{CC}$. C_{C1} starts to charge toward $+V_{CC}$. The total voltage

excursion that C_{C1} can charge through is $-V_{CC}$ to $+V_{CC}$, or a total excursion of $2V_{CC}$. Figure 132 illustrates the RC exponential charge curve involved.

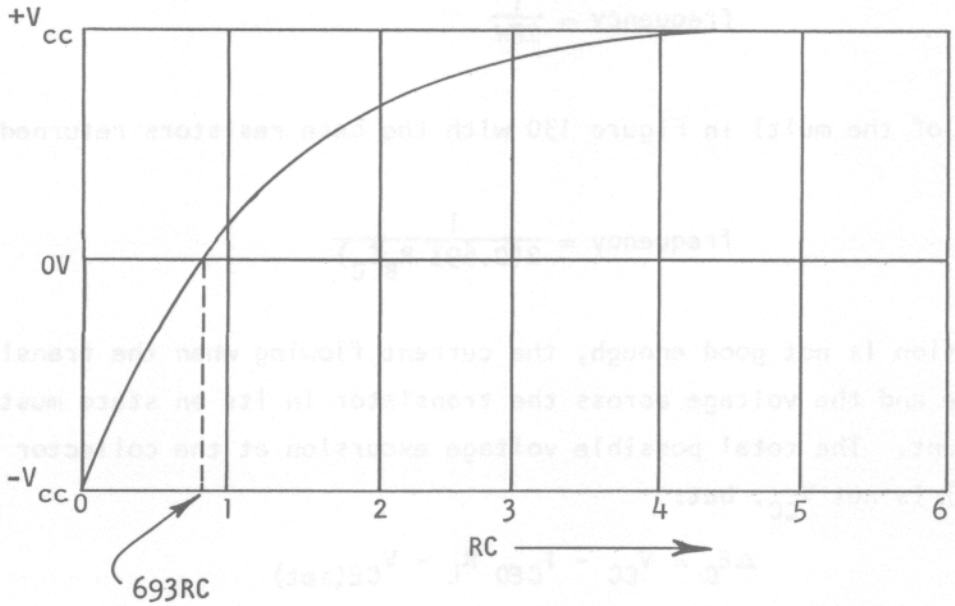


FIGURE 132

If we assume that the transistors will start switching when the base of Q_2 reaches 0V, the capacitor C_{C1} will only have to charge over 50% of its total possible voltage excursion before switching occurs. After the base of Q_2 reaches 0V, the voltage starts to forward bias Q_2. Once Q_2 starts into conduction, the change at its collector is coupled to the base of Q_1, which starts to bring it out of saturation. The regeneration continues, and Q_1 switches off and Q_2 saturates. This action continues, and the amount of time that the transistors spend in one state or the other is determined by the time constant of the base resistor and coupling capacitor, along with the total voltage excursion over which the capacitor can charge.

When the base resistors are returned to the collector supply voltage, such as in the circuit in Figure 130, the time in one state is approximately 0.693 $R_B C_C$ time constants, as shown in Figure 132. One pulse width of the square wave output of the multivibrator in Figure 130 can be calculated by: $P_W = 0.693\ R_B C_C$

The frequency of an astable multivibrator is:

$$\text{frequency} = \frac{1}{PW_1 + PW_2}$$

If the multivibrator is symetrical ($PW_1 = PW_2$), the frequency is:

$$\text{frequency} = \frac{1}{2PW}$$

and in the case of the multi in Figure 130 with the base resistors returned to the supply voltage:

$$\text{frequency} = \frac{1}{2(0.693\ R_B C_C)}$$

If an approximation is not good enough, the current flowing when the transistor is in its off state and the voltage across the transistor in its on state must be taken into account. The total possible voltage excursion at the collector of the transistor (ΔE_C) is not V_{CC}, but:

$$\Delta E_C = V_{CC} - I_{CEO}\ R_L - V_{CE(sat)}$$

The total voltage excursion over which C_C can charge (ΔE_T) is:

$$\Delta E_T = V_{CC} + \Delta E_C$$

One pulse width can be found by:

$$PW = R_B C_C \log_\epsilon \left(\frac{\Delta E_T}{E_{RB}}\right)$$

where: R_B and C_C are the timing components

ΔE_T is the total voltage excursion over which C_C could charge

E_{RB} is the voltage left across the resistor R_B at the time of switching

For the configuration in Figure 130:

$$P_W = R_B C_C \log_\epsilon \left(\frac{V_{CC} + \Delta E_C}{V_{CC}}\right)$$

Since the total voltage excursion over which C_C could charge is $V_{CC} + \Delta E_C$, and the voltage left to go or left across the resistor R_B is V_{CC} at the time of switching.

Frequency can be found by:

$$\text{frequency} = R_{B1}\, C_{C1}\, \log_{\epsilon}\left(\frac{V_{CC} + \Delta E_{C2}}{V_{CC}}\right) + R_{B2}\, C_{C1}\, \log_{\epsilon}\left(\frac{V_{CC} + \Delta E_{C1}}{V_{CC}}\right)$$

and if the multivibrator is symetrical:

$$\text{frequency} = \frac{1}{2\, R_B\, C_C\, \log_{\epsilon}\left(\frac{V_{CC} + \Delta E_C}{V_{CC}}\right)}$$

FREQUENCY CONTROL:

A circuit, such as shown in Figure 133, can be used to vary the frequency of the multivibrator without affecting the symmetry.

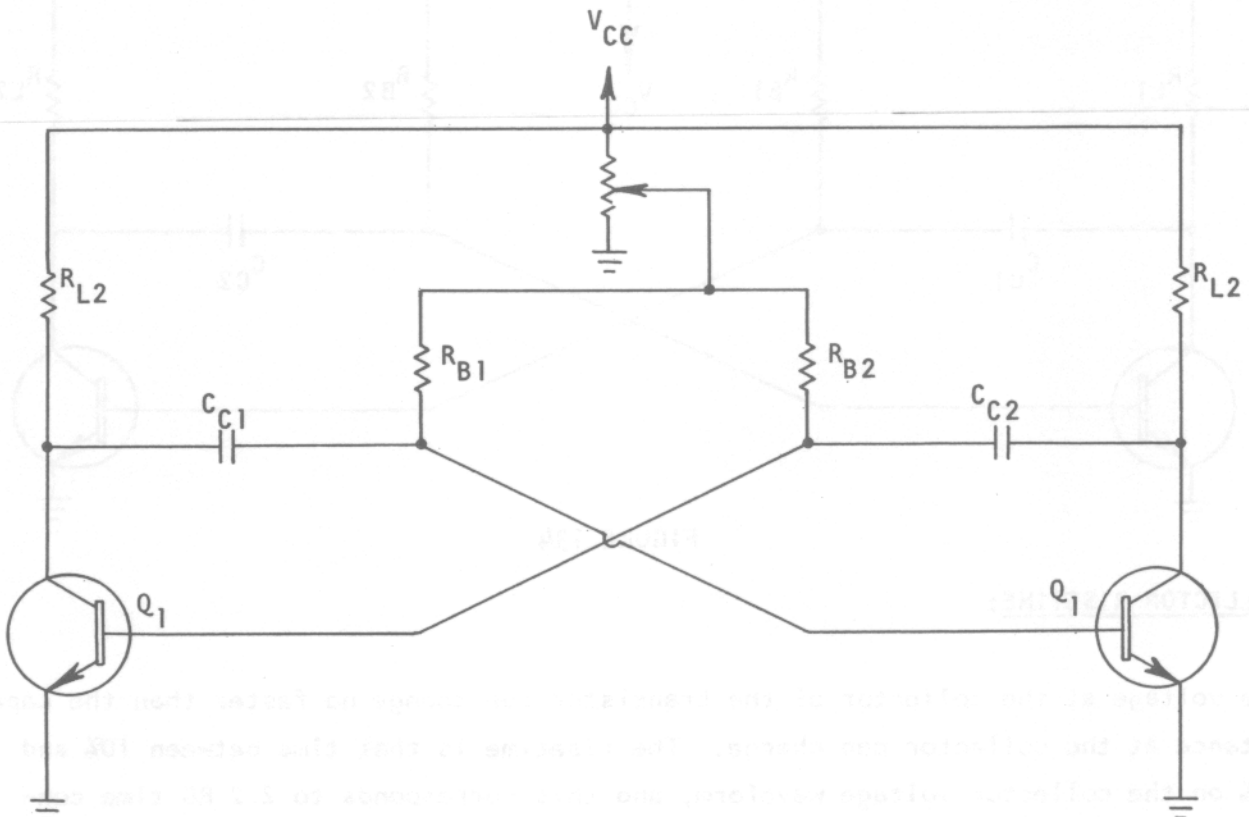


FIGURE 133

This is essentially varying the supply to which the base resistors are returned, which varies the total voltage excursion through which C_C can charge while the collector change remains the same. Reducing the voltage to which the base resistors are returned, increases the pulse width and reduces the frequency of the multivibrator.

SYMMETRY CONTROL:

Figure 134 illustrates a means by which the symmetry of the multivibrator can be adjusted. Adjusting R_1 effectively changes the size of R_{L1} and R_{L2} and the value of supply voltage to which they are returned. In other words, if we did a Thevenin analysis at different settings of R_1, we would find the collector returned to different equivalent supply voltages through different load resistors. Properly selected, R_1 will allow adjustment for desired waveform symmetry.

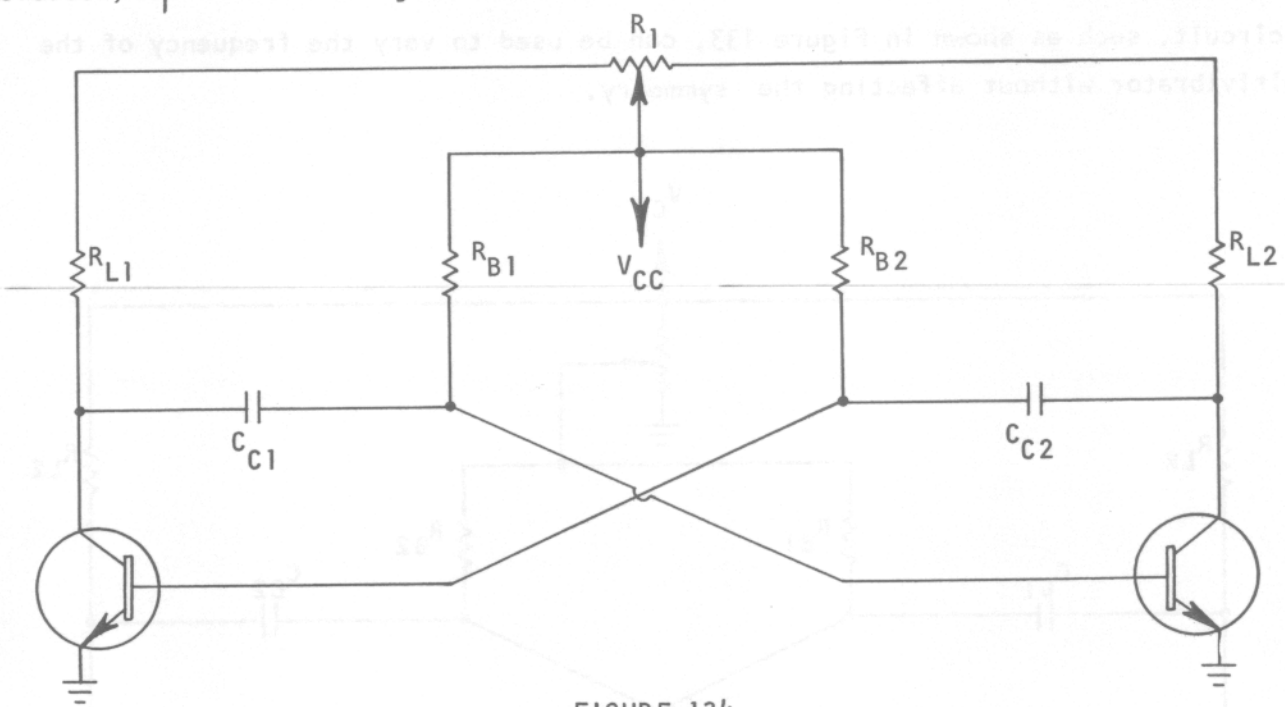


FIGURE 134

COLLECTOR RISETIME:

The voltage at the collector of the transistor can change no faster than the capacitance at the collector can charge. The risetime is that time between 10% and 90% on the collector voltage waveform, and this corresponds to 2.2 RC time constants. The collector capacitance of the transistor itself is only a few pico-

farads and, unless the timing capacitor C_C is very small, will not play the limiting role. Figure 135 illustrates the charge path of the timing capacitor for risetime considerations.

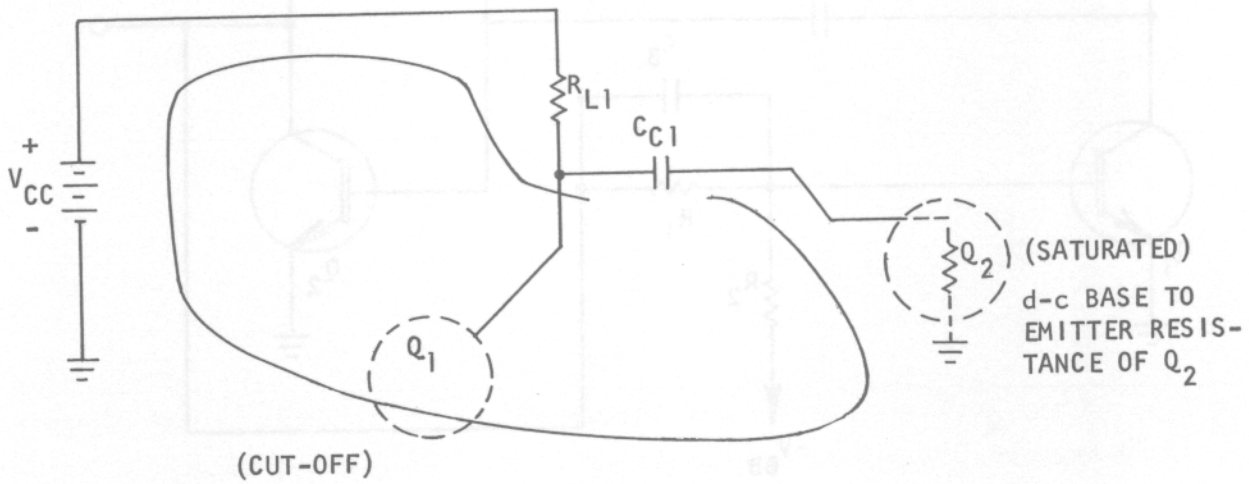


FIGURE 135

If R_L is large compared to the Q_2 resistance, the risetime of the Q_1 collector is:

$$\text{risetime } (t_r) = 2.2\ R_{L1}\ C_{C1}$$

MONOSTABLE MULTIVIBRATOR:

One of the timing networks in the astable multivibrator can be replaced with a d-c divider returned to a source of voltage, giving the multivibrator one stable state. This is illustrated in Figure 136.

The voltage divider R_1 and R_2 establish a reverse bias on Q_1, maintaining it in cut-off, while Q_2 is in saturation. When the multi is first turned on, the base of Q_2 returned to the supply voltage V_{CC} insures that Q_2 comes into conduction, and the reverse bias is established on Q_1. The multivibrator now has a stable state, and external energy must be applied to cause it to change states.

TRIGGERING THE MONO-STABLE:

Quiescently, the multi in Figure 136 is its stable state of Q_1 off and Q_2 in

saturation. An applied trigger initiates switching by bringing Q_2 out of saturation enough for regeneration to occur.

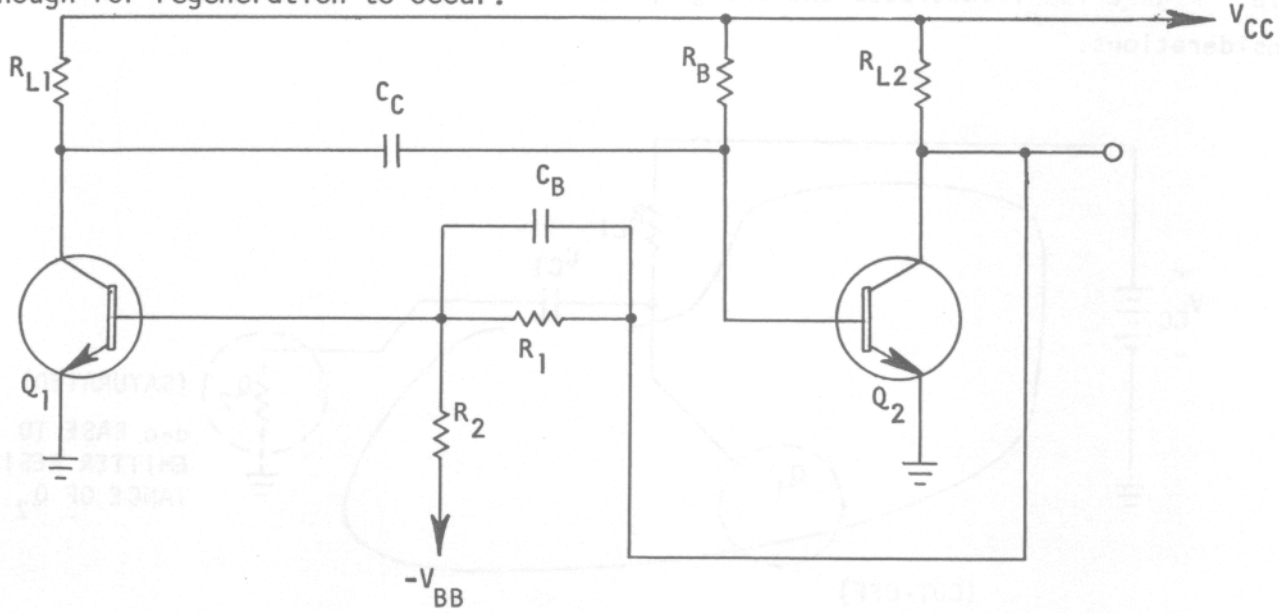


FIGURE 136

The trigger could also turn on Q_2 enough for regeneration to occur. The collector voltage of Q_2 changes from approximately ground potential to approximately V_{CC} once switching is completed. This change at the collector of Q_2 raises the voltage level at the base of Q_1 high enough for Q_1 to turn on and remain in conduction.

The opposite polarity voltage change at the collector of Q_1 is applied to the base of Q_2, because the capacitor cannot change its charge instantaneously. C_C and R_B serve the same timing task as they did in the astable. The base of Q_2 is driven down to a voltage approximately equal to $-V_{CC}$, and the timing network and calculations previously discussed for the astable multivibrator apply here as well.

When the capacitor charges to a point where the base of Q_2 reaches approximately 0V again, Q_2 starts back into conduction, the regeneration occurs, and the multi is once again in its stable state. The divider of R_1 and R_2 returned to a negative supply will hold Q_1 in cut-off until another trigger is applied and switching is initiated again.

When Q_2 returns to conduction, capacitor C_C should be allowed to charge before another trigger is applied, or else the pulse width will vary. The time constant involved is R_{L1} and C_C. At least 4 R_{L1} C_C time constants should be allowed after switching before another trigger is applied to assure a constant pulse width.

The pulse width when triggered is determined by the R_B C_C time constant and the voltages involved, and can be calculated just as it was for the astable. The repetition rate, of course, will be governed by the repetition rate of the applied triggering signal.

With the multi in its quiescent state of Q_2 in saturation in Figure 136, most combinations of R_1 and R_2 returned to a negative supply will maintain Q_1 in cut-off. The determining factors in the selection of R_1 and R_2 are:

1. Emitter-base reverse breakdown of Q_1
2. Magnitude of I_{CBO}
3. Triggering requirements

The reverse voltage applied to Q_1 by the divider must not exceed the emitter base breakdown of Q_1.

The greater the reverse bias applied to Q_1, the greater the required magnitude of triggering signal.

I_{CBO} of Q_1 flows through the parallel combination of R_1 and R_2 in Figure 136. An increase in temperature will increase I_{CBO}, all other factors held constant. If R_1 and R_2 are too large, the I_{CBO} drop can bring Q_1 out of cut-off by overcoming the negative supply. R_1 and R_2 should be selected with these limitations in mind. Even if R_1 and R_2 are selected properly, it should be brought out that an increase in temperature will reduce the required magnitude of a triggering signal. This is due to I_{CBO} reducing the reverse bias on Q_1.

R_1 and R_2 must also allow enough base current when the circuit is switched to saturate Q_1.

Note in Figure 136 that a capacitor has been placed in shunt with R_1. This is the speed-up capacitor discussed in Volumes 3 and 6, and optimum value is when the charge on C_B in Figure 136 is equal to the stored charge in Q_1 when the transistor is saturated.

TRIGGERING:

Referring to the multi in Figure 136 again, a trigger can be applied to the base of Q_1 to bring Q_1 into conduction. (The trigger could be applied to the collector of Q_2 and coupled through C_B to the base of Q_1.) A trigger can also be applied to the base of Q_2 to turn Q_2 off. (This trigger could be applied to the collector of Q_1 and coupled through C_C to the base of Q_2.)

If the trigger is applied to the base of Q_1, it must be sufficient magnitude to turn on Q_1 and get regeneration started. If the trigger is applied to the base of Q_2, the trigger is amplified as Q_2 comes out of saturation. A high amplification factor is involved, because Q_2 is at a high current, high gain point as it comes out of saturation.

EMITTER-BASE BREAKDOWN:

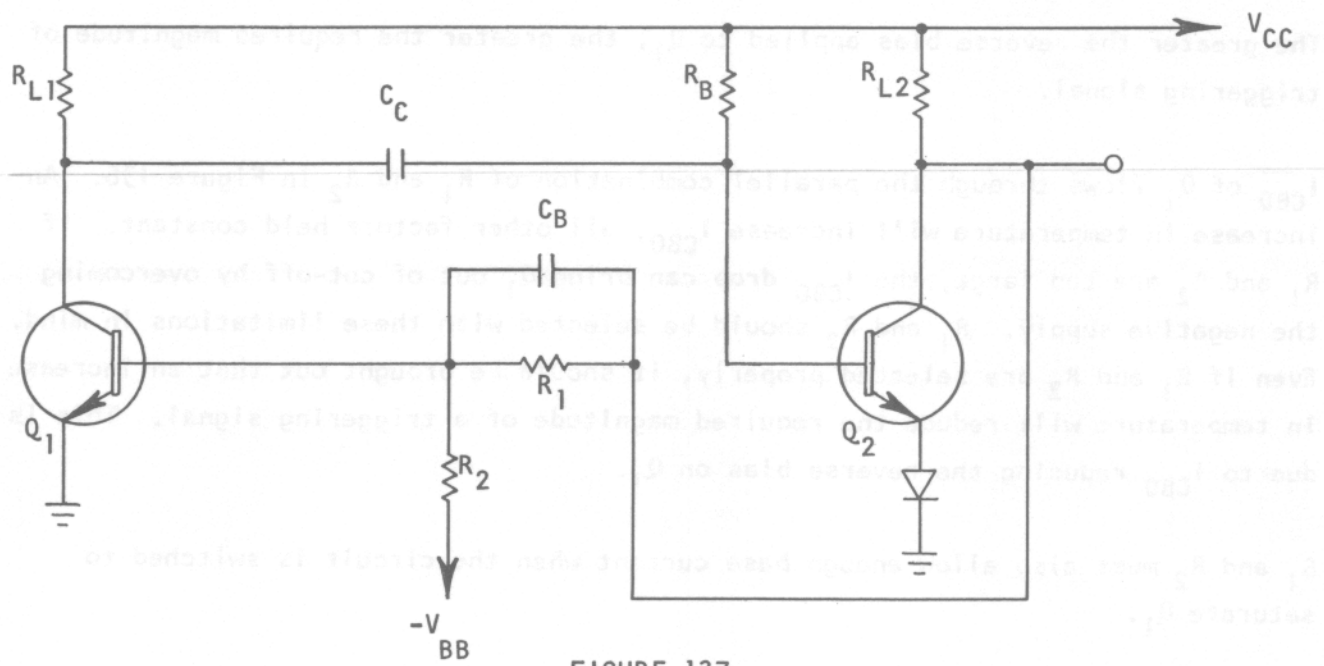


FIGURE 137

In all of the multivibrators discussed here, there is the possibility of a reverse voltage as high as V_{CC} being applied to the emitter-base junction of the transistor. If the reverse voltage applied exceeds the emitter-base breakdown voltage of the

transistor and breakdown occurs, the timing calculations are not valid. To prevent emitter-base breakdown from occuring, another diode can be placed in series with emitter-base junctions. The reverse voltage will distribute across the added diode and the emitter-base junction, and the breakdown rating of both must be exceeding before breakdown can occur. This is illustrated in Figure 137.

The diode could also be inserted in series in the base lead. This is a low current point, however, and the resistance of the diode is high and enters into the timing calculations. When the diode is placed in the emitter lead, emitter current of the transistor flows through it, and its resistance can be fairly low. The voltage across the diode becomes part of the collector to ground voltage of Q_2 when it is in its on state. When Q_2 is on, the diode in its emitter simply becomes forward biased, and conducts the emitter current of Q_2.

BLOCKING OSCILLATORS:

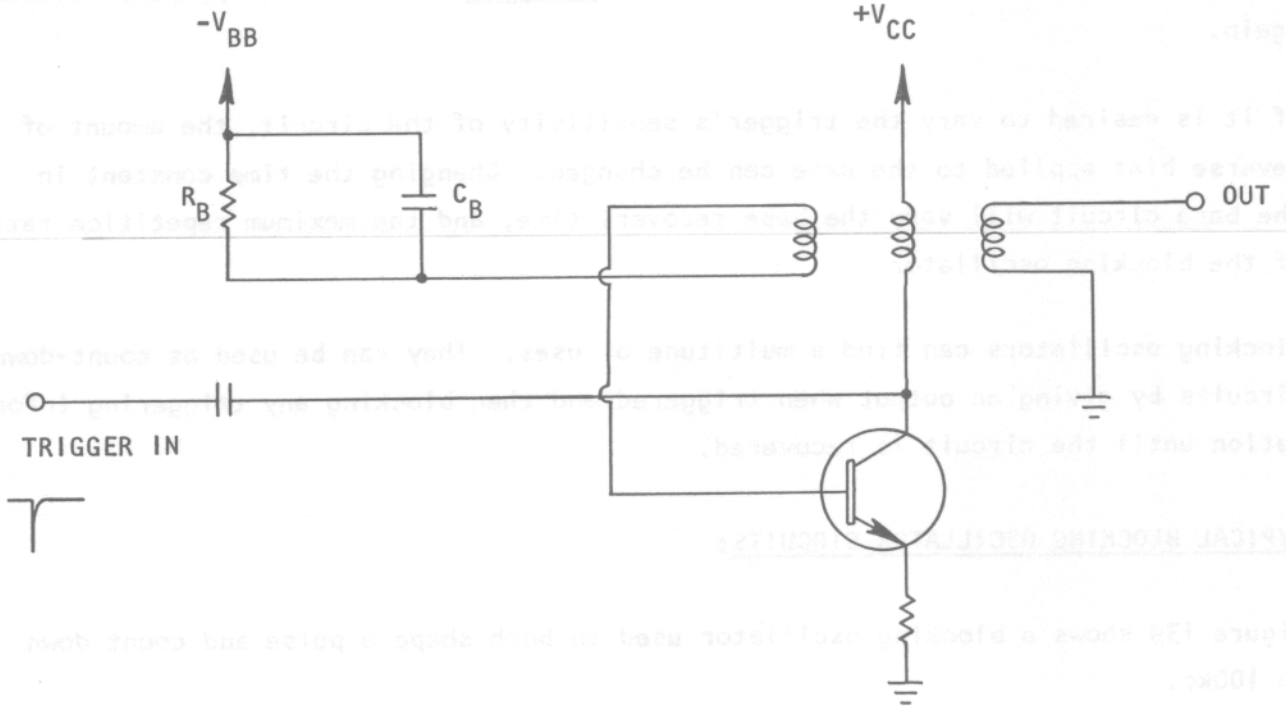


FIGURE 138

Consider the configuration in Figure 138. The transistor is off quiescently and, therefore, has one stable state. The transformer is arranged to provide regenerative feedback from collector to base. If a negative going trigger of sufficient magnitude is applied at the input, a positive going change is coupled back to the

base. This starts to turn on the transistor and the regeneration continues until one of two things occurs.

1. The transformer core saturates, or
2. The transistor saturates

Let's consider what happens if the transformer core saturates (much the same action occurs when the transistor saturates). The current in the transistor and, as a result, the current in the transformer primary increases until the core saturates. When the core saturates, there is no longer regenerative feedback to the base, and the base starts seeking its reverse bias supply once again. Once the transformer can recover, regeneration occurs in the opposite direction and the transistor turns off again. The width of the output pulse depends on the recovery time of the circuit. Once switching is instigated by an input trigger, and until the base of the transistor has completely recovered to the point that it will trigger on the magnitude of input trigger applied, the triggering information can be said to be blocked. No triggering can occur until the blocking oscillator completely recovers again.

If it is desired to vary the trigger's sensitivity of the circuit, the amount of reverse bias applied to the base can be changed. Changing the time constant in the base circuit will vary the base recovery time, and the maximum repetition rate of the blocking oscillator.

Blocking oscillators can find a multitude of uses. They can be used as count-down circuits by giving an output when triggered and then blocking any triggering information until the circuit is recovered.

TYPICAL BLOCKING OSCILLATOR CIRCUITS:

Figure 139 shows a blocking oscillator used to both shape a pulse and count down to 100kc.

The components in the blocking oscillator in Figure 139 are selected so that the blocking oscillator gives an output square pulse, 200 nanosec wide. R33 allows the reverse voltage applied to the base to be varied, which varies the triggering amplitude requirement. The time constant in the base is selected so that the maximum repetition rate of the blocking oscillator is 100kc. The blocking oscillator

in Figure 139 is in the Tektronix Type 111 Pretrigger Pulse Generator.

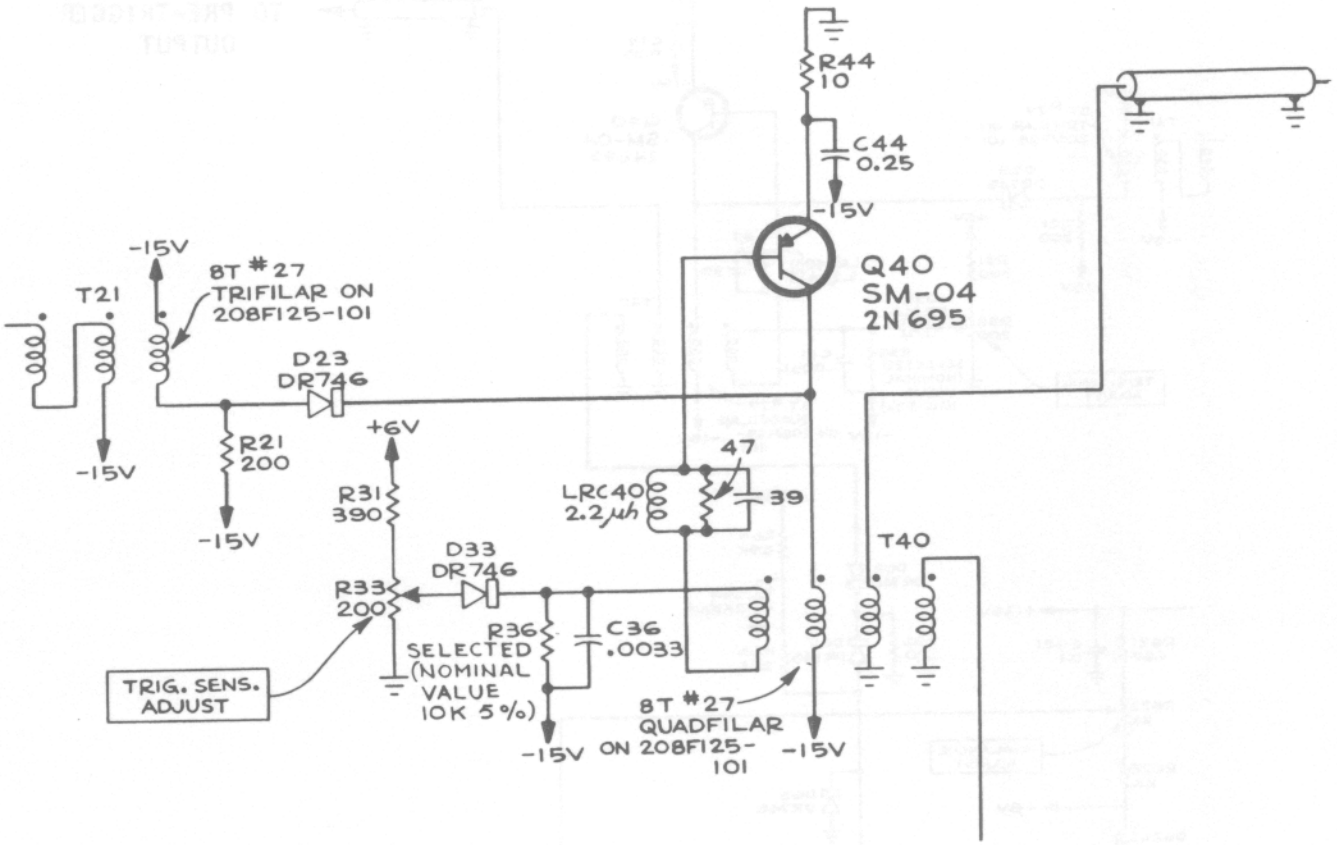
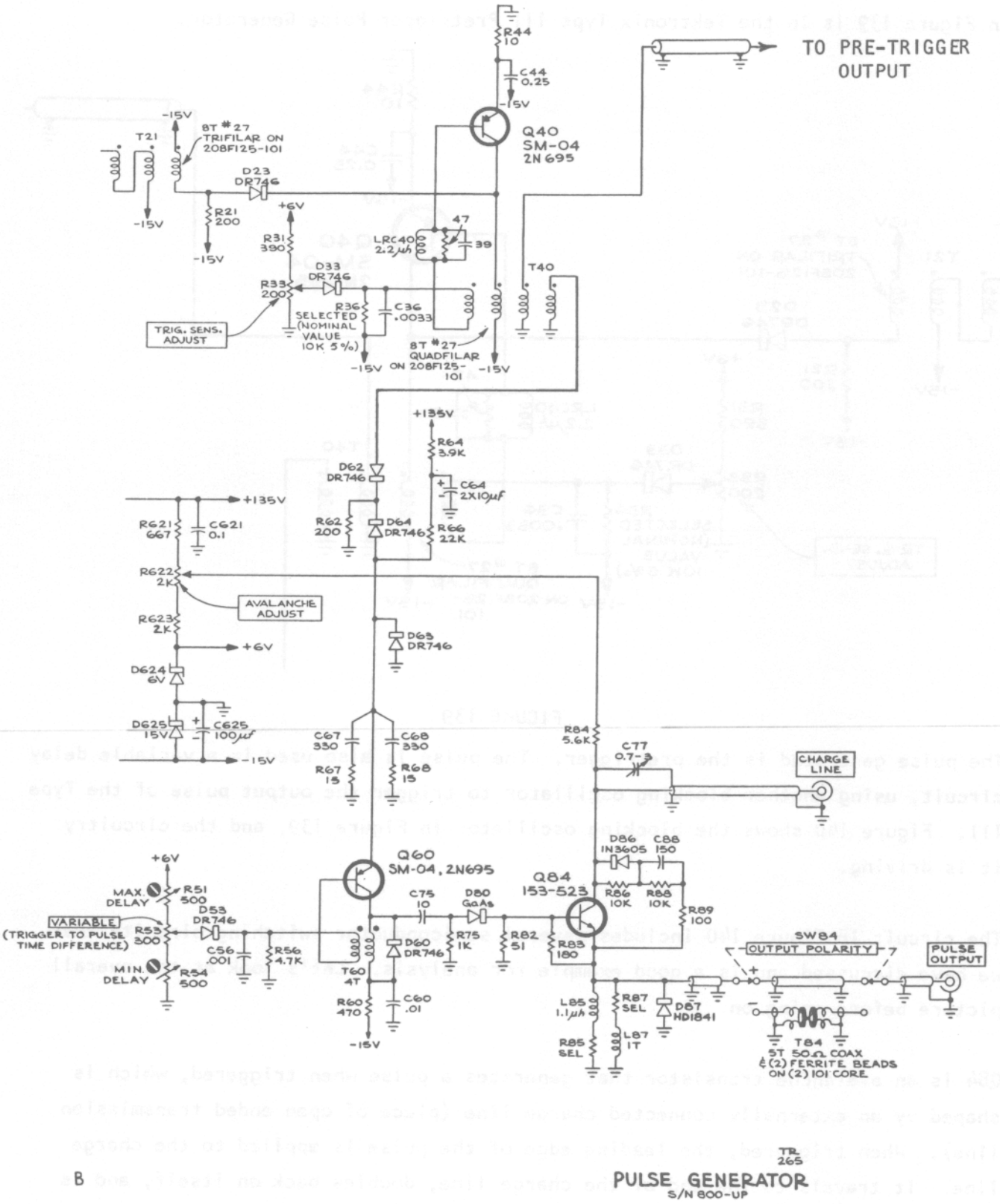


FIGURE 139

The pulse generated is the pretrigger. The pulse is also used in a variable delay circuit, using another blocking oscillator to trigger the output pulse of the Type 111. Figure 140 shows the blocking oscillator in Figure 139, and the circuitry it is driving.

The circuit in Figure 140 includes several semiconductor switching circuits that we have discussed and is a good example for analysis. Let's look at the overall picture before going on.

Q84 is an avalanche transistor that generates a pulse when triggered, which is shaped by an externally connected charge line (piece of open ended transmission line). When triggered, the leading edge of the pulse is applied to the charge line. It travels to the end of the charge line, doubles back on itself, and is reflected back up the line. When the reflected wave reaches the input of the charge line, the input signal and the reflected signal (which are 180° out of



B

TR. 265

PULSE GENERATOR
S/N 800-UP

FIGURE 140

phase) cancel, and the pulse is terminated. The pulse will only be present while the leading edge is moving down and back up the charge line; therefore, the pulse width is approximately twice the electrical length of the charge line. In other words, if it takes a pulse 10 nanoseconds to travel down the charge line and 10 nanoseconds to travel back up the charge line, the pulse will be 20 nanoseconds wide. Most texts and references on transmission lines and systems cover this in more detail. "Nanosecond Pulse Measurements", C. N. Winningstad, IRE WESCON Record, 1960, and "Pulse Reflection Measurement of Transmission Line Impedance and Discontinueties", Gordon D. Long, Tektronix, Inc., 1962 are good sources.

The avalanche transistor is base triggered by a signal from the blocking oscillator using Q60, coupled through a fast switching diode D80. D80 is a Tektronix Gallium Arsenide diode for switching speed.

The blocking oscillator of Q60 is very similar to the blocking oscillator in Figure 139 with the exception that the transistor saturates before the transformer core; however, the regeneration ceases and the action is very similar. Once positive excursions in the output are required to trigger the avalanche transistor, and D60 serves to clip any negative going excursions. The blocking oscillator is triggered in the emitter, and R53 in the base allows the adjustment of the required triggering level.

The blocking oscillator is triggered in the emitter circuit by a ramp waveform. The ramp is actually generated in the emitter circuit, and this will be discussed shortly. The circuit serves the dual role of a comparator that allows a variable delay between the time of generation of the pretrigger and the time of triggering the avalanche transistor and generating the leading edge of the output pulse. The Q60 blocking oscillator allows much the same results as the "Delay Time Multiplier" circuitry in the 530/540 series Tektronix oscilloscopes.

With no signal from the Q40 blocking oscillator, D62 is cut-off and D64 is in conduction. The current path is from ground through R62, D64, R66, and R64 to the +135V supply.

When Q40 in Figure 140 is triggered, a 10V positive going pulse is applied to the anode of D62, turning D62 on. The pulse generated by the Q40 blocking oscillator

is 200 nanoseconds wide; therefore, D62 will remain on for 200 nanoseconds. This pulls the cathode of D64 positive and D64 cuts off. We could do a Thevenin analysis, but it is not necessary here. With D64 off and Q60 off, capacitors C67 and C68 start charging toward 135V. It can be seen that only a very small portion of this exponential change will occur before the emitter of Q60 is raised high enough to turn on Q60. (The base is only returned to a portion of the 6V supply.) When Q60 turns on, the B.O. regenerates and the avalanche transistor is triggered. Capacitors C67 and C68 discharge through Q60, and the circuit cannot be triggered again until the blocking oscillator recovers.

The ability to adjust the level at the base of Q60 allows selection of that point on the ramp generated in the emitter, at which it is desired to have the blocking oscillator triggered. Since it takes different times for the ramp to reach different selected levels, the adjustment of the base reverse voltage becomes a variable time delay control. Resistors R51 and R54 allow the range of delay times to be varied, and are similar in operation to the delay start and stop adjustments in the 530/540 series Delay Time Multiplier circuit.

Figure 141 shows a blocking oscillator in another configuration in which the blocking oscillator is providing a triggering signal and an output pulse.

The blocking oscillator is made up of Q2010 and its circuitry. The reverse bias on the base is fixed in this case and set by the drop across D2013. Therefore, the required trigger amplitude is constant. A 2V positive trigger is coupled in through C2018 and D2018 to the collector of Q2010. Regeneration starts and the B.O. switches. Q2024, the memory gate driver, is a good example of taking advantage of transistor stored charge in a switching application. Q2024 is normally biased off by the small positive voltage drop across R2021 and D2022. When the B.O. (Q2010) switches, the negative going pulse coupled through D2022 drives Q2024 into saturation. When Q2010 recovers, Q2024 must lose its stored base charge before it can come out of saturation. The only path for removal of the stored charge is through R1022 and R1023. R1023 is variable to allow adjustment of the time involved in the removal of the stored charge, and as a result the width of the memory gate.

D2004 is a snap-off diode. Snap-off diodes were discussed in Volumes 2 and 6 of

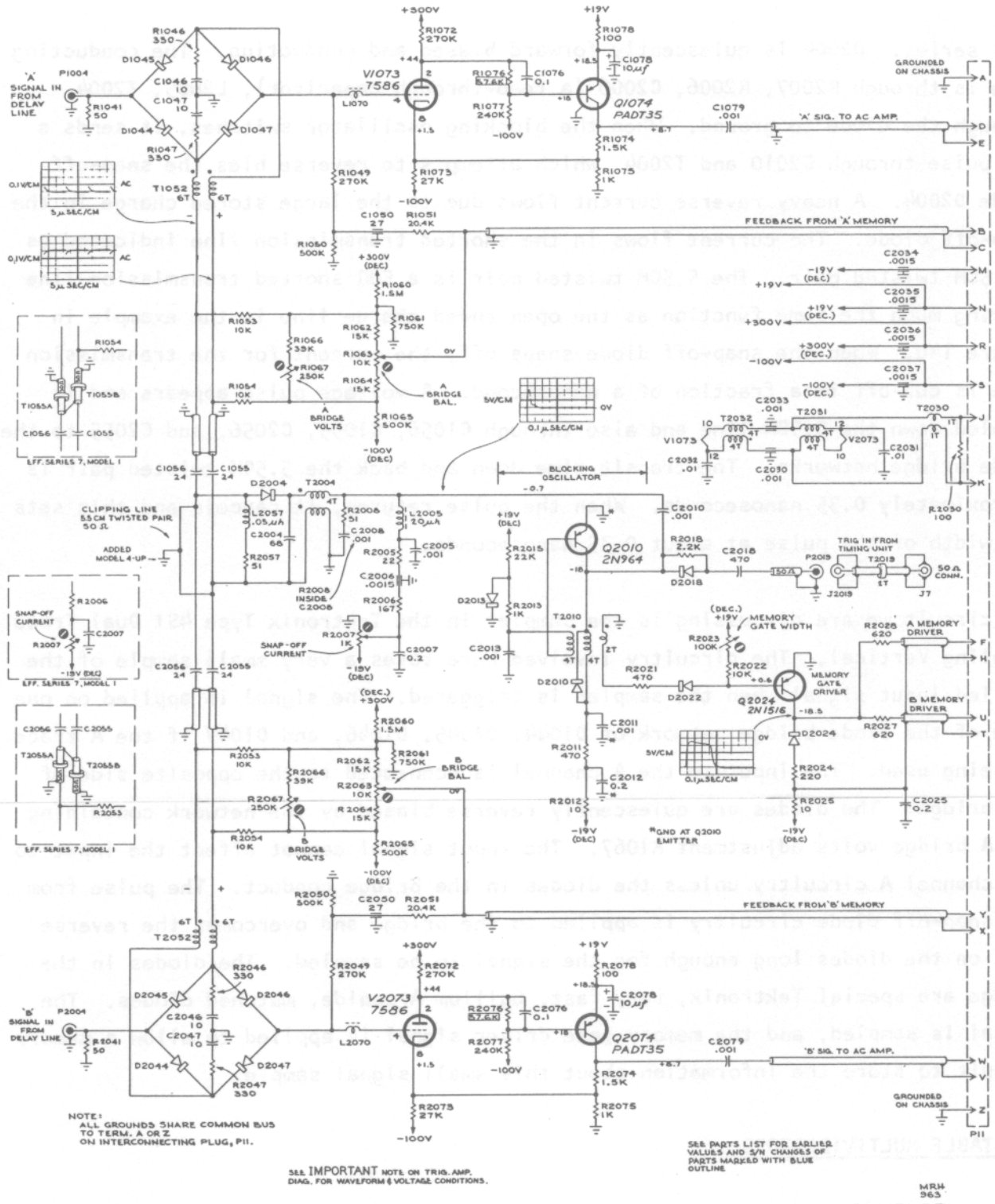

'A' SIGNAL IN FROM DELAY LINE
P1004
R1041 50
R1046 350
R1047 350
D1045
D1046
D1044
D1047
C1046 10
C1047 10
T1052
6T
0.1V/CM AC
5μ SEC/CM
0.1V/CM AC
5μ SEC/CM
+300V
R1072 270K
V1073 7586
L1070
+44
+1.5
R1076 57.6K
C1076 0.1
R1077 240K
-100V
+19V
R1078 100
C1078 10μf
+18.5
Q1074 PADT35
+8.7
R1074 1.5K
R1075 1K
C1079 .001
'A' SIG. TO AC AMP.
GROUNDED ON CHASSIS
A
D
E
R1049 270K
R1073 27K
-100V
C1050 27
R1051 20.4K
FEEDBACK FROM 'A' MEMORY
B
C
R1050 500K
+300V (DEC.)
R1060 1.5M
R1053 10K
R1061 750K
R1062 15K
R1066 35K
R1067 250K
R1063 10K
R1064 15K
R1054 10K
R1065 500K
-100V (DEC.)
A BRIDGE BAL.
A BRIDGE VOLTS
0V
5V/CM
0.1μ SEC/CM
BLOCKING OSCILLATOR
-0.7
C2034 .0015
-19V (DEC.)
+19V
M
C2035 .0015
+19V (DEC.)
N
+300V
C2036 .0015
+300V (DEC.)
R
-100V
C2037 .0015
-100V (DEC.)
S
C2033 .001
T2032
T2031
T2030
J
V1073
C2032 .01
V2073
C2030 .001
C2031 .01
K
R2030 100
T1055A
T1055B
C1056
C1055
EFF. SERIES 7, MODEL 1
C1056 24
C1055 24
D2004
T2004
CLIPPING LINE 55 CM TWISTED PAIR 50 Ω
ADDED MODEL 4-UP
L2057 .05μh
C2004 68
R2057 51
R2008 51
L2005 20μh
C2008 .001
R2008 INSIDE C2008
C2005 .001
C2006 .0015
R2005 22
R2006 167
R2007 1K
SNAP-OFF CURRENT
C2007 0.2
-15V (DEC)
C2056 24
C2055 24
Q2010 2N964
-18
R2015 22K
D2013
R2013 1K
C2013 .001
T2010
R2018 2.2K
C2018 470
D2018
TRIG IN FROM TIMING UNIT
P2019
T2018
J2019
50Ω CONN.
J7
(DEC.) +19V
MEMORY GATE WIDTH
R2023 100K
R2022 10K
+0.6
MEMORY GATE DRIVER
Q2024 2N1516
-18.5
D2010
D2022
R2021 470
A MEMORY DRIVER
R2028 620
F
H
B MEMORY DRIVER
R2027 620
U
T
D2024
R2024 220
R2025 10
C2025 0.2
C2011 .001
R2011 470
C2012 0.2
R2012 10
-19V (DEC)
*GND AT Q2010 EMITTER
5V/CM
0.1μ SEC/CM
0V
R2060 1.5M
R2053 10K
R2061 750K
R2062 15K
R2066 35K
R2063 10K
R2067 250K
R2064 15K
R2054 10K
R2065 500K
B BRIDGE BAL.
B BRIDGE VOLTS
R2050 500K
C2050 27
R2051 20.4K
FEEDBACK FROM 'B' MEMORY
Y
X
T2052
6T
R2046 330
R2049 270K
R2072 270K
V2073 7586
L2070
R2076 57.6K
C2076 0.1
R2077 240K
Q2074 PADT35
C2078 10μf
R2078 100
C2079 .001
'B' SIG. TO AC AMP.
W
V
R2074 1.5K
R2075 1K
R2073 27K
'B' SIGNAL IN FROM DELAY LINE
P2004
R2041 50
D2045
D2046
D2044
D2047
C2046 10
C2047 10
R2047 330
GROUNDED ON CHASSIS
Z
P11
NOTE: ALL GROUNDS SHARE COMMON BUS TO TERM. A OR Z ON INTERCONNECTING PLUG, P11.
SEE IMPORTANT NOTE ON TRIG. AMP. DIAG. FOR WAVEFORM & VOLTAGE CONDITIONS.
SEE PARTS LIST FOR EARLIER VALUES AND S/N CHANGES OF PARTS MARKED WITH BLUE OUTLINE
MRH 963
TYPE 451
SAMPLER
SERIES 7 MODELS 1,2,3,4

FIGURE 141

this series. D2004 is quiescently forward biased and conducting. The conducting path is through R2007, R2006, C2006 (a feed-through capacitor), L2005, T2004, through the diode to ground. When the blocking oscillator switches, it sends a 10V pulse through C2010 and T2004, which attempts to reverse bias the snap-off diode D2004. A heavy reverse current flows due to the large stored charge in the snap-off diode. The current flows in the shorted transmission line indicated as a 5.5CM twisted pair. The 5.5CM twisted pair is a 50Ω shorted transmission line serving much the same function as the open ended charge line in the example in Figure 140. When the snap-off diode snaps off, the current for the transmission line is cut-off in a fraction of a nanosecond. A voltage pulse appears and is coupled down the 5.5CM line and also through C1056, C1055, C2056, and C2055 to the diode bridge networks. The transit time down and back the 5.5CM twisted pair is approximately 0.35 nanoseconds. When the pulse returns, it cancels and this sets the width of the pulse at about 0.35 nanoseconds.

The circuit we are discussing is the sampler in the Tektronix Type 4S1 Dual Trace Sampling Vertical. The circuitry involved here takes a very small sample of the applied input signal when the sampler is triggered. The signal is applied on one side of the diode bridge network of D1044, D1045, D1046, and D1047 if the A trace is being used. The input to the A channel is connected to the opposite side of the bridge. The diodes are quiescently reverse biased by the network containing the A bridge volts adjustment R1067. The input signal cannot affect the input to the channel A circuitry unless the diodes in the bridge conduct. The pulse from the snap-off diode circuitry is applied to the bridge and overcomes the reverse bias on the diodes long enough for the signal to be sampled. The diodes in the bridge are special Tektronix, very fast, Gallium Arsenide, matched diodes. The signal is sampled, and the memory gate driver signal is applied to allow a memory circuit to store the information about this small signal sample.

BI-STABLE MULTIVIBRATORS:

To change from the simple astable to a monostable multivibrator, we changed one of the RC timing networks to a d-c divider. To make the circuit bi-stable, we can replace the remaining RC timing network with a d-c divider and give the circuit two stable states. The circuit is typically like that in Figure 142.

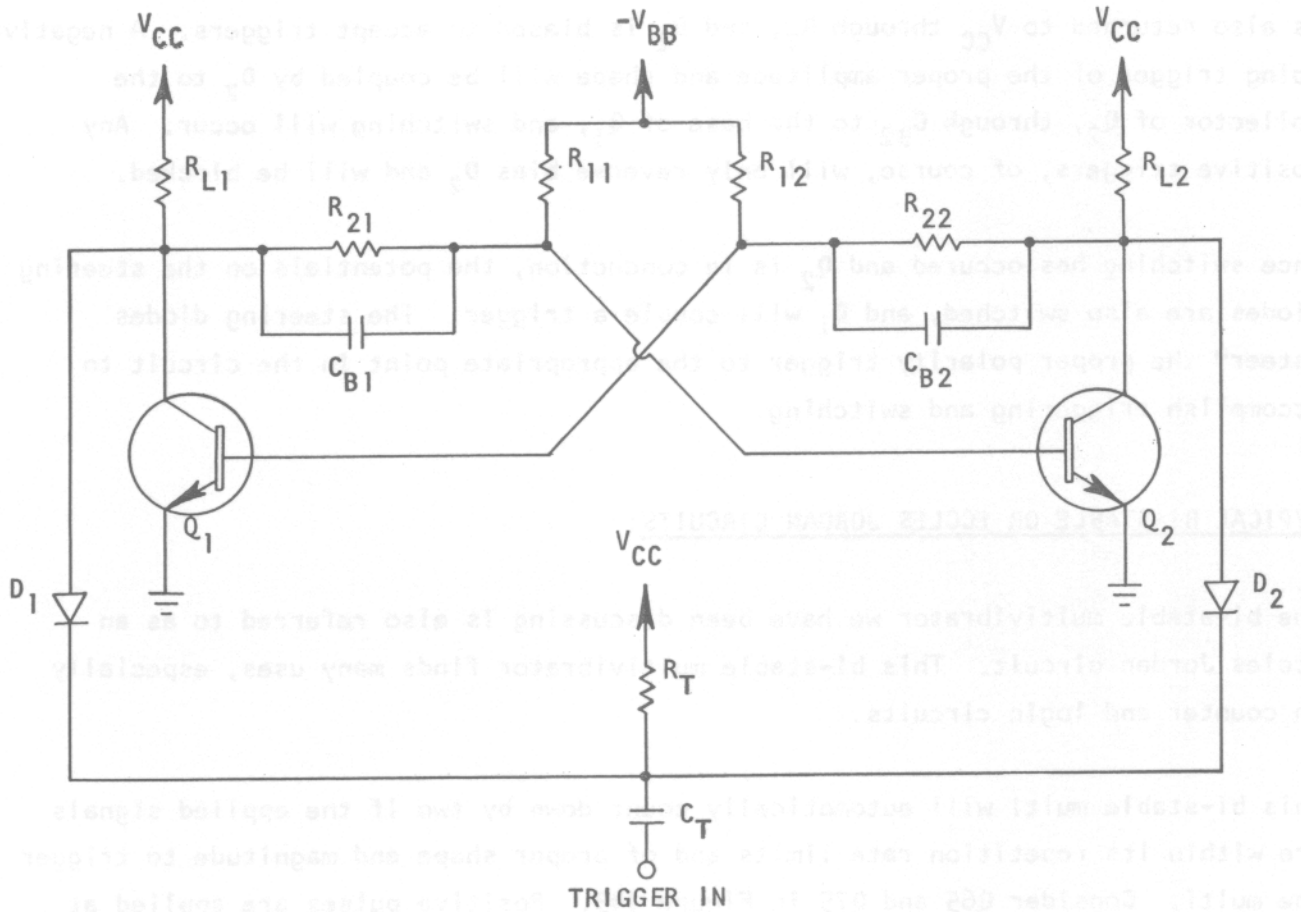


FIGURE 142

The circuit can rest in either of its stable states when first turned on. Therefore, if it is desired to have its starting point in a given state, some form of reset circuit will have to be used.

STEERING DIODES:

The triggering applied to the bi-stable multivibrator is typically accomplished as shown in Figure 142 by D_1, D_2, R_T, and C_C. D_1 and D_2 are often referred to as steering diodes. They "steer" the trigger to its proper point of application.

When Q_1 is conducting and Q_2 is cut-off, the anode of D_1 is essentially grounded by Q_1, and the anode of D_1 is returned to V_{CC}. D_1 is reverse biased by approximately V_{CC}, and any applied triggers must be greater in magnitude than V_{CC} to be coupled through D_1. The cathode of D_2 under these same conditions, however, is returned to the collector voltage of Q_2, which is very near V_{CC}. The anode of D_2

is also returned to V_{CC} through R_T, and D_2 is biased to accept triggers. A negative going trigger of the proper amplitude and shape will be coupled by D_2 to the collector of Q_2, through C_{B2} to the base of Q_1, and switching will occur. Any positive triggers, of course, will only reverse bias D_2 and will be blocked.

Once switching has occured and Q_2 is in conduction, the potentials on the steering diodes are also switched, and D_1 will couple a trigger. The steering diodes "steer" the proper polarity trigger to the appropriate point in the circuit to accomplish triggering and switching.

TYPICAL BI-STABLE OR ECCLES JORDAN CIRCUITS:

The bi-stable multivibrator we have been discussing is also referred to as an Eccles Jordan circuit. This bi-stable multivibrator finds many uses, especially in counter and logic circuits.

This bi-stable multi will automatically count down by two if the applied signals are within its repetition rate limits and of proper shape and magnitude to trigger the multi. Consider Q65 and Q75 in Figure 143. Positive pulses are applied at appropriate times to pin 7. These pulses are coupled through C62 and steering diodes D62 and D72 steer the trigger to the proper triggering point in the circuit. R67 and R77 are the base resistors, and R77 is returned to +125V through a reset circuit. The reset pulse in a positive going pulse superimposed on +125V. It sets the multi in its starting or quiescent state. Since Q65 and Q75 are PNP transistors, the reset pulse will insure that Q75 is off and Q65 is on initially. The positive reset pulse applied to the base of Q75 reverse biases Q75 to insure that it is off. Let's do an approximate analysis of the multi made up of Q65 and Q75 in its quiescent state. With Q65 in conduction, its base and emitter will be at very near the same voltage. Since the emitter is returned directly to +20V, the base of Q65 in Figure 143 is at approximately +20V with respect to ground. If we assume Q65 is saturated, its collector is also very near +20V.

The signal coming in on pin 7 in Figure 143 is applied to three points, through C_2 to the series of three Eccles Jordan multivibrators through C62 to the multi we are presently discussing, and directly to the transistor amplifier Q84. Either

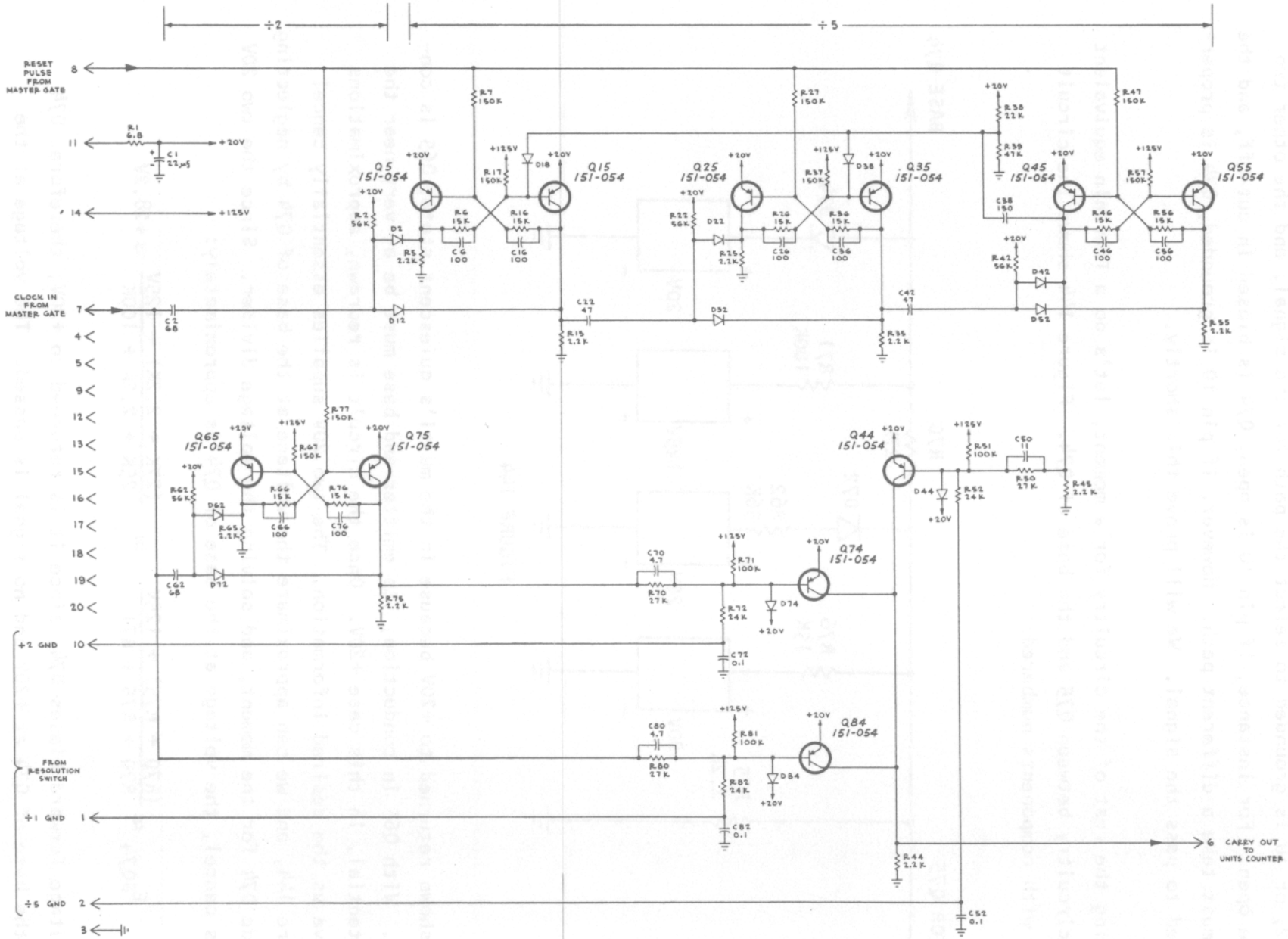

÷2
÷5
RESET PULSE FROM MASTER GATE
8
11
14
CLOCK IN FROM MASTER GATE
7
4
5
9
12
13
15
16
17
18
19
20
+2 GND
10
FROM RESOLUTION SWITCH
÷1 GND
1
÷5 GND
2
3
+20V
+12.5V
R1 6.8
C1 22µf
Q5 151-054
Q15 151-054
Q25 151-054
Q35 151-054
Q45 151-054
Q55 151-054
Q65 151-054
Q75 151-054
Q44 151-054
Q74 151-054
Q84 151-054
R7 150K
R17 150K
R27 150K
R37 150K
R47 150K
R57 150K
R67 150K
R77 150K
R38 22K
R39 47K
R42 56K
R62 56K
R72 14K
R82 14K
R52 14K
R71 100K
R81 100K
R51 100K
R2 56K
R22 56K
R5 2.2K
R25 2.2K
R65 2.2K
R15 2.2K
R35 2.2K
R55 2.2K
R75 2.2K
R45 2.2K
R44 2.2K
R6 15K
R16 15K
R26 15K
R36 15K
R46 15K
R56 15K
R66 15K
R76 15K
C6 100
C16 100
C26 100
C36 100
C46 100
C56 100
C66 100
C76 100
C38 150
C2 68
C62 68
C22 47
C42 47
C50 11
R50 27K
C70 4.7
R70 27K
C80 4.7
R80 27K
C72 0.1
C82 0.1
C52 0.1
D2
D12
D18
D22
D32
D38
D42
D52
D62
D72
D74
D84
D44
G CARRY OUT TO UNITS COUNTER
SERIES B-MODEL ÷1,2,5
364
TYPE 6R1A
A

FIGURE 143

pin 1, 2, or 10 is grounded to select the path for the signal, and the other two pins are open. For instance, if pin 10 is open, Q74 is biased in cut-off, and the pulses must take a different path. However, if pin 10 is grounded, Q74 is properly biased to pass the signal. We will prove this shortly.

Neglecting the rest of the circuitry for a moment, let's do a Thevenin equivalent of the circuitry between Q75 and the base of Q74. Figure 144 shows the circuit redrawn with components numbered.

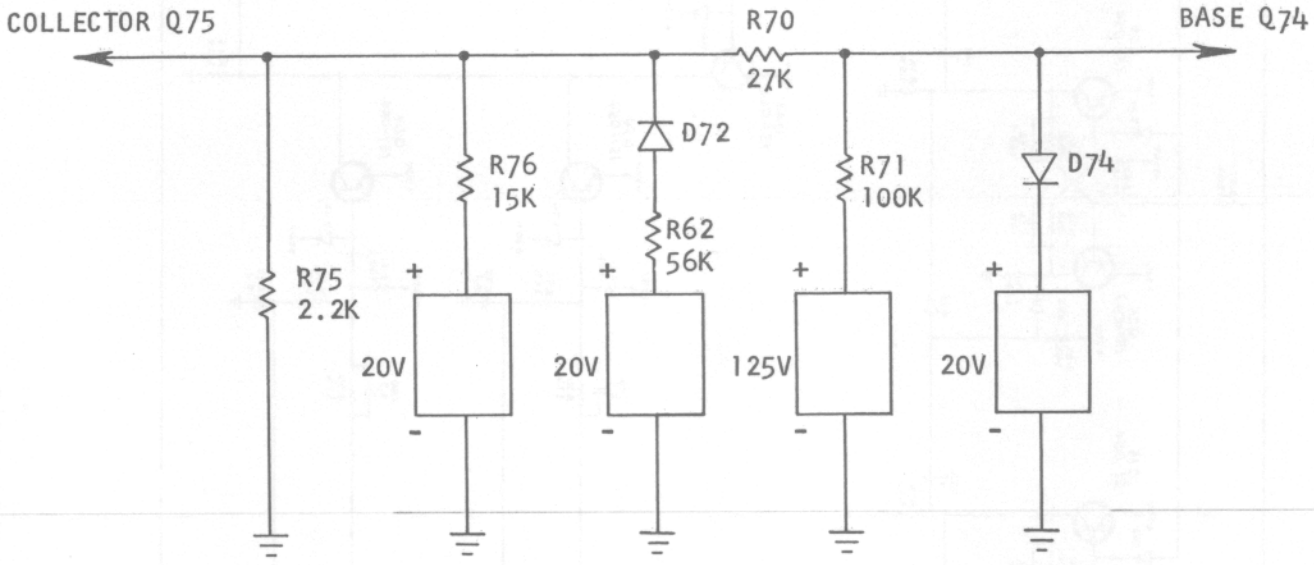


FIGURE 144

R76 is shown returned to +20V because in the multi's quiescent state, Q65 is conducting. With Q65 in conduction, its emitter and base must be at very near the same potential, in this case +20V. Once the circuit is redrawn, approximations will give us the desired information. The two 20V supplies essentially cancel in Figure 144, and we can approximate the voltage at the base of Q74 by neglecting the diode D74 for the moment, and solving the voltage divider. Since the two 20V supplies cancel, the voltage at the base of Q74 is approximately:

$$E_{BQ74} \approx \frac{(R70 + R75) + 125V}{R70 + R75 + R71} \approx \frac{(27K + 2.2K) + 125V}{25K + 2.2K + 100K} \approx +28.2V$$

This voltage forward biases D74, since it is returned to +20V; therefore, D74 clamps the base of Q74 at +20V and no signal is passed. The voltage at the

collector of Q75 can be approximated by solving the voltage divider:

$$E_{CQ75} \approx \frac{R75\ (125V)}{R75 + R70 + R71} \approx \frac{2.2K\ (125V)}{2.2K + 27K + 100K} \approx +1.93V$$

It is easy to see now that grounding pin 10 places R72 in shunt with R70 and R75 from the base of Q74 to ground. The voltage divider is now this equivalent resistance of approximately 13.1K and R71. The voltage at the base of Q74 is now approximately:

$$E_{BQ74} \approx \frac{13.1K}{113.1K}\ (125V) \approx +14.5V$$

D74 is cut-off and Q74 is biased for amplifier action.

The units counter that the circuit in Figure 143 drives will only respond to positive pulses. The first positive pulse applied to the Q65, Q75 multi will switch the multi, and the collector of Q75 will swing positive to near +20V. Q74 is a common emitter configuration and inverts the signal. The second positive pulse applied at pin 7 in Figure 143 switches the multi again, and the collector of Q75 swings less positive (in the negative direction) to its resting state level. This negative going pulse is inverted by Q74 and gives a positive output pulse. It is evident that it requires two positive input pulses to get one positive output pulse. The signal is divided by two.

In the divide by five operation, pin 2 is grounded and pins 1 and 10 are open. Q74 and Q84 are cut-off, and the signal is coupled through Q44. The three stages of bi-stable multivibrators are arranged so that it requires five input pulses before one positive output pulse from Q44 is obtained. The fifth input pulse gives an output and also feeds back a signal through diodes D18 and D38 to reset the multis to divide by five again.

In the divide by one, or straight-through operation, the input pulses are differentiated by C80 and R80, and applied directly to Q84, giving an output pulse for each input pulse.

Bi-stable or Eccles Jordan multivibrators find use in many applications in Tektronix

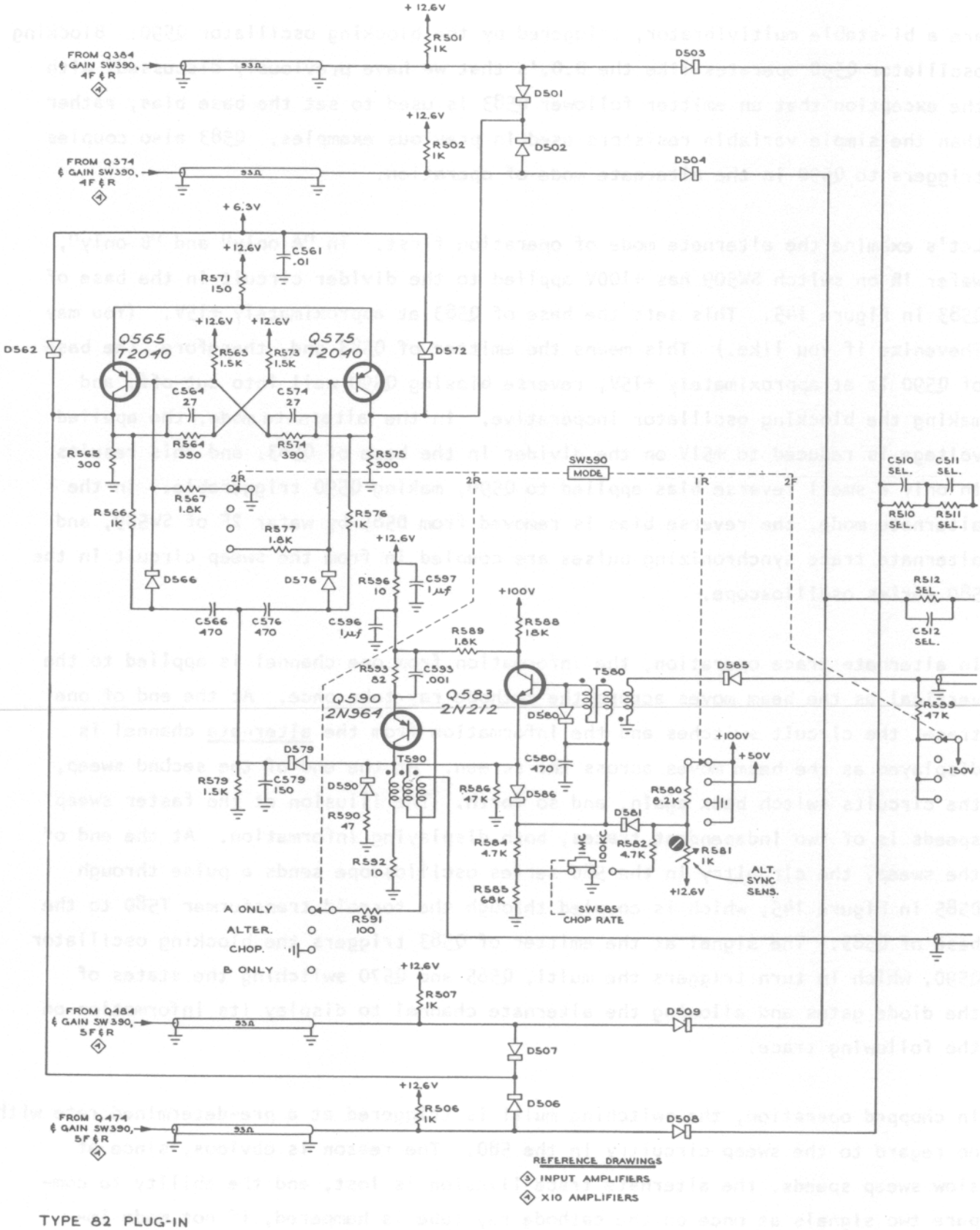
circuitry. The circuit we were just discussing is the ÷1, 2, 5 circuitry in the 6R1A Digital Unit. The counters, the heart of the 6R1A unit, are made up of this same type of multi.

Figure 145 shows the Eccles Jordan circuit in a little different application. It shows the switching circuit for the output amplifier in the Tektronix Type 82 vertical plug-in for the 580 series oscilloscopes. This is a dual trace plug-in, and the circuits in Figure 145 are used to switch the information from the two input amplifiers to the output amplifier at the appropriate time. In the alternate and chopped settings of switch SW590, transistors Q565 and Q575 serve as an Eccles Jordan circuit, or bi-stable triggered multivibrator. In the "A only" position, R567 is grounded, becoming part of the divider network for the base of Q565. This insures that Q565 has the most positive base and remains in cut-off. You can do a Thevenin equivalent if you like. Diode gating circuits are used to couple the signals from the input amplifier to the common output amplifier. They are D501 through D504 for one channel, and D506 through D509 for the other channel. The voltage levels at the collectors of Q565 and Q575 are approximately +8V when non-conducting, and approximately +6V when conducting. (You may Thevenize if you like). D503, D504, D508, and D509 are returned to ground through approximately 1.3K of resistance. If we disregard the drops across the diodes a moment, we can approximate the voltage at the anode of D501. It is approximately:

$$\frac{(+12.6V)\ 1.3K\Omega}{1.3K\Omega + R501} \approx \frac{1.3K\ (+12.6V)}{2.3} \approx 7.13V$$

The voltage is approximately the same at the anodes of D501., D502, D506, and D507 as well. We can see that the cathodes of D501 and D502 are returned to the collector of Q575. When A575 is on, its collector is at +8V, and D501 and D502 are reverse biased and cut-off. When Q575 is off, its collector is at approximately +6V, and D501 and D502 are forward biased. This, of course, shunts any signal while reverse biasing D503 and D504. When Q575 is on, signals are coupled through diode gates D501 through D504, and diode gate D506 through D509 blocks any signal. D501, etc., couples the A channel; therefore, when R567 is grounded in Figure 145, only A channel gets coupled to the output amplifier. Of course, in the "B only" setting of switch SW590, just the opposite is true.

When SW590 is in the alternate or chopped setting in Figure 145, Q565 and Q575



TYPE 82 PLUG-IN

FIGURE 145

C

are a bi-stable multivibrator, triggered by the blocking oscillator Q590. Blocking oscillator Q590 operates like the B.O.'s that we have previously discussed, with the exception that an emitter follower Q583 is used to set the base bias, rather than the simple variable resistors used in previous examples. Q583 also couples triggers to Q590 in the alternate mode of operation.

Let's examine the alternate mode of operation first. In "A only" and "B only", wafer 1R on switch SW509 has +100V applied to the divider circuit in the base of Q583 in Figure 145. This sets the base of Q583 at approximately +15V. (You may Thevenize if you like.) This means the emitter of Q583 and, therefore, the base of Q590 is at approximately +15V, reverse biasing Q590 well into cut-off, and making the blocking oscillator inoperative. In the alternate mode, the applied voltage is reduced to +51V on the divider in the base of Q583, and this results in only a small reverse bias applied to Q590, making Q590 triggerable. In the alternate mode, the reverse bias is removed from D585 by wafer 2F of SW509, and alternate trace synchronizing pulses are coupled in from the sweep circuit in the 580 series oscilloscope.

In alternate trace operation, the information from one channel is applied to the vertical as the beam moves across the cathode ray tube once. At the end of one trace, the circuit switches and the information from the alternate channel is displayed as the beam moves across the screen. At the end of the second sweep, the circuits switch back again, and so forth. The illusion at the faster sweep speeds is of two independent traces, both displaying information. At the end of the sweep, the circuitry in the 580 series oscilloscope sends a pulse through D585 in Figure 145, which is coupled through the torroid transformer T580 to the base of Q583. The signal at the emitter of Q583 triggers the blocking oscillator Q590, which in turn triggers the multi, Q565 and Q570 switching the states of the diode gates and allowing the alternate channel to display its information on the following trace.

In chopped operation, the switching multi is triggered at a pre-determined rate with no regard to the sweep circuitry in the 580. The reason is obvious, since at slow sweep speeds, the alternate trace illusion is lost, and the ability to compare two signals at once on the cathode ray tube is hampered, if not made impossible in the alternate mode. In the chopped mode, the circuit is switched at

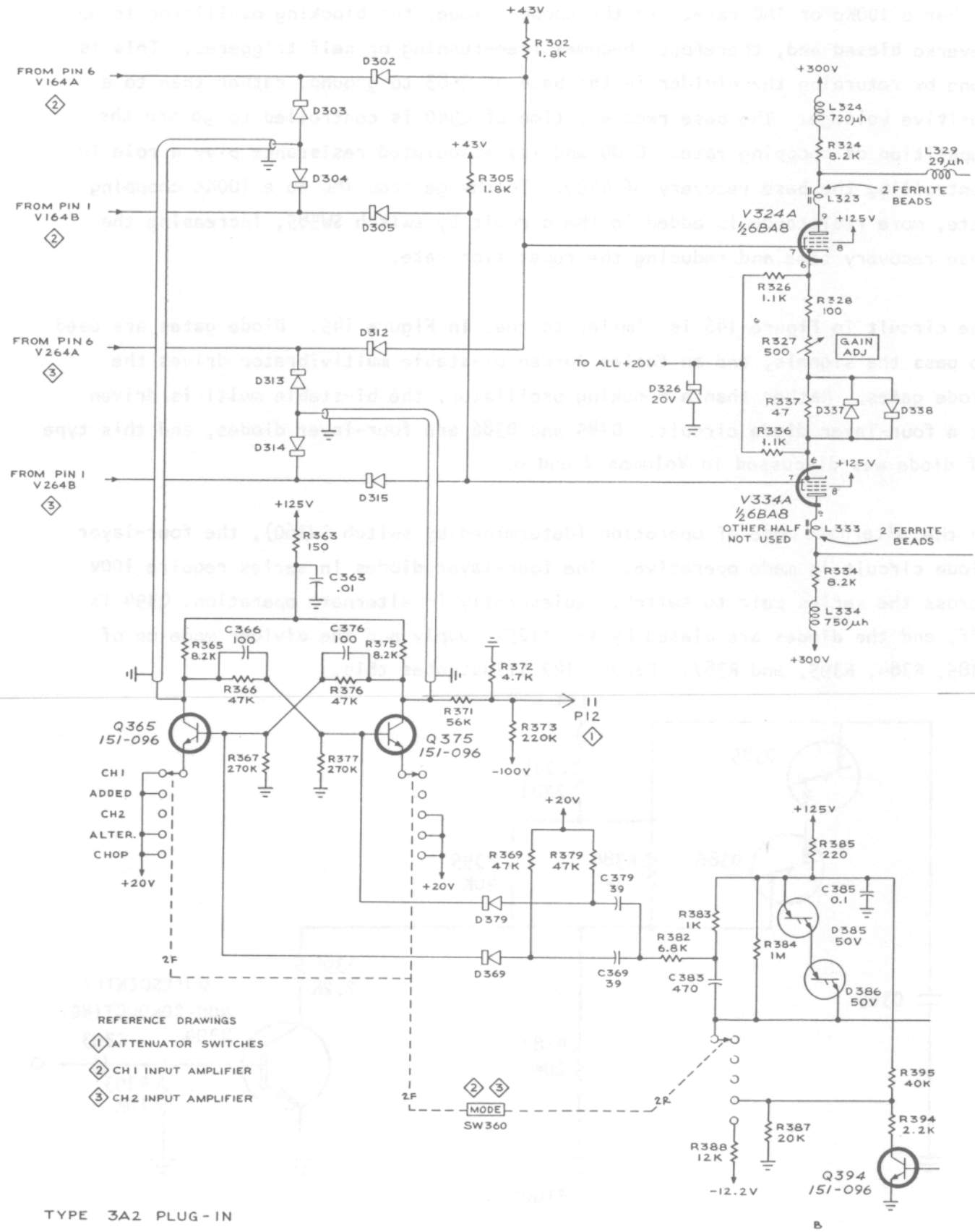

+43V
R302 1.8K
D302
FROM PIN 6 V164A
2
D303
D304
+43V
R305 1.8K
FROM PIN 1 V164B
2
D305
+300V
L324 720µh
R324 8.2K
L329 29µh
2 FERRITE BEADS
L323
V324A ½6BA8
+125V
R326 1.1K
R328 100
R327 500
GAIN ADJ
TO ALL +20V
D326 20V
R337 47
D337
D338
R336 1.1K
FROM PIN 6 V264A
3
D312
D313
D314
FROM PIN 1 V264B
3
D315
+125V
V334A ½6BA8
OTHER HALF NOT USED
L333
2 FERRITE BEADS
R334 8.2K
L334 750µh
+300V
+125V
R363 150
C363 .01
C366 100
C376 100
R365 8.2K
R375 8.2K
R366 47K
R376 47K
R372 4.7K
R371 56K
R373 220K
-100V
11
P12
1
Q365 151-096
Q375 151-096
R367 270K
R377 270K
CH1
ADDED
CH2
ALTER.
CHOP
+20V
+20V
+20V
R369 47K
R379 47K
C379 39
D379
D369
C369 39
2F
2F
2R
R382 6.8K
R383 1K
C383 470
R384 1M
+125V
R385 220
C385 0.1
D385 50V
D386 50V
R395 40K
R394 2.2K
R387 20K
R388 12K
-12.2V
Q394 151-096
2
3
MODE
SW360
REFERENCE DRAWINGS
1 ATTENUATOR SWITCHES
2 CH 1 INPUT AMPLIFIER
3 CH 2 INPUT AMPLIFIER
TYPE 3A2 PLUG-IN
8

FIGURE 146

either a 100Kc or 1MC rate. In the chopped mode, the blocking oscillator is not reverse biased and, therefore, becomes free-running or self triggered. This is done by returning the divider in the base of Q583 to ground, rather than to a positive voltage. The base recovery time of Q540 is controlled to govern the repetition or chopping rate. C580 and its associated resistance play a role in controlling the base recovery of Q590. To change from 1MC to a 100Kc chopping rate, more resistance is added in the circuit by switch SW585, increasing the base recovery time and reducing the repetition rate.

The circuit in Figure 146 is similar to that in Figure 145. Diode gates are used to pass the signals, and an Eccles Jordan bi-stable multivibrator drives the diode gates. Rather than a blocking oscillator, the bi-stable multi is driven by a four-layer diode circuit. D385 and D386 are four-layer diodes, and this type of diode was discussed in Volumes 2 and 6.

In the alternate mode of operation (determined by switch SW360), the four-layer diode circuit is made operative. The four-layer diodes in series require 100V across the series pair to switch. Quiescently in alternate operation, Q394 is off, and the diodes are biased by the +125V supply and the divider made up of R385, R384, R395, and R387. Figure 147 illustrates this.

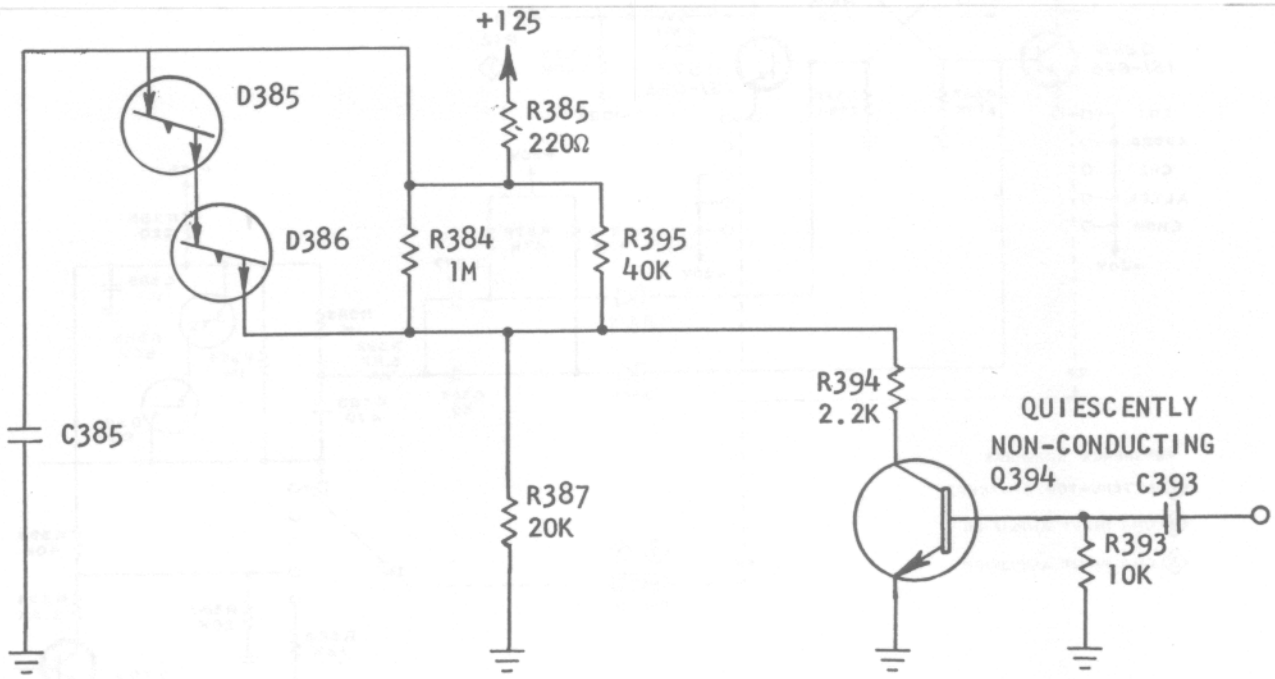


FIGURE 147

The initial voltage across the diodes can be found by solving the voltage divider. The voltage at the top of R387 is (note: Q394 non-conducting) approximately:

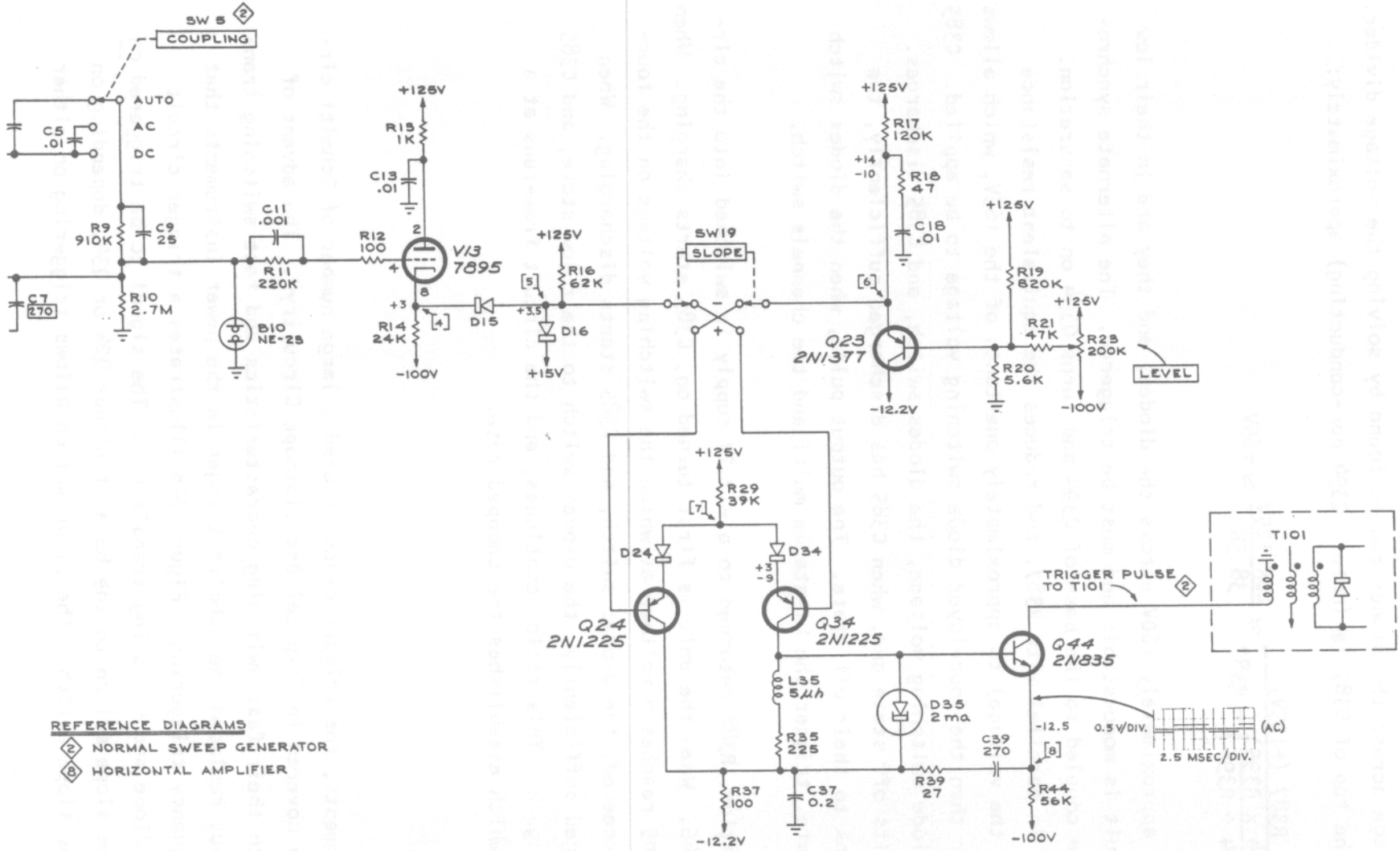
$$\frac{R387\ (+125V)}{\left(\frac{R384 \times R395}{R384 + R395}\right) + R387} \approx \frac{20K\ 125V}{38.5K} \approx +65V$$

This only leaves approximately +60V across the diodes, and they are in their low state. The circuit is mono-stable and must be triggered. The alternate synchronizing pulses are coupled to the base of Q394 and turns Q394 on to saturation. This places R394 in parallel with R387, and reduces the equivalent resistance (and as a result the voltage) to approximately one-tenth of the +65V, which allows a voltage greater than the four-layer diode switching voltage to be applied. C385 charges to the diode switching voltage, the diodes switch, and C385 discharges. Q394 returns to its off state and, when C385 has discharged sufficiently, the diodes switch back to their off state. The output pulse, when the diodes switch to their high state, trigger the bi-stable multi and the channels switch.

For chopped operation, R388 returned to a -12.2V supply is switched into the circuit in Figure 146. When the unit is first turned on, C385 starts charging. When the charge on C385 reaches a voltage at which the switching voltage on the four-layer diode is exceeded, the diodes switch, and C385 starts discharging. When C385 has discharged sufficiently, the diodes switch to their low state, and C385 starts charging again. This action continues, and the circuit free-runs at a 30 - 50kc rate, which establishes the chopped rate.

TRIGGER CIRCUITS:

In earlier instruments, the trigger circuits used a large number of Schmitt circuits. These are covered in "Typical Oscilloscope Circuitry". The advent of tunnel diodes with their fast switching characteristics and fast switching transistors has all but replaced the schmitt trigger in the newer instruments that require high frequency triggering. Figure 148 illustrates a trigger circuit using the tunnel diode and switching transistors. The signal to be triggered on is fed through the slope switch to the base of either Q24 or Q34, depending on the setting of the slope switch. The slope switch allows triggering on either



TYPE 3B3

NORMAL SWEEP TRIGGER

FIGURE 148

the positive or negative going portion of the triggering waveform.

The sweep trigger must be able to generate a shaped waveform when the input reaches a selected level. The shaped waveform must be capable of triggering the sweep generator circuitry. Q24 and Q34 in Figure 148 are a comparator type configuration. The triggering level is established on the base of the transistor other than the one receiving the triggering information, by the emitter follower Q23. When the triggering signal overcomes the level set on the opposite transistors base, the increase in conduction in Q34 increases the tunnel diode D35 current enough that D35 switches to its high state. The resulting pulse is amplified by Q44 and coupled through T101 to the sweep generator. This pulse is used to trigger the sweep generator and start the beam across the face of the cathode ray tube.

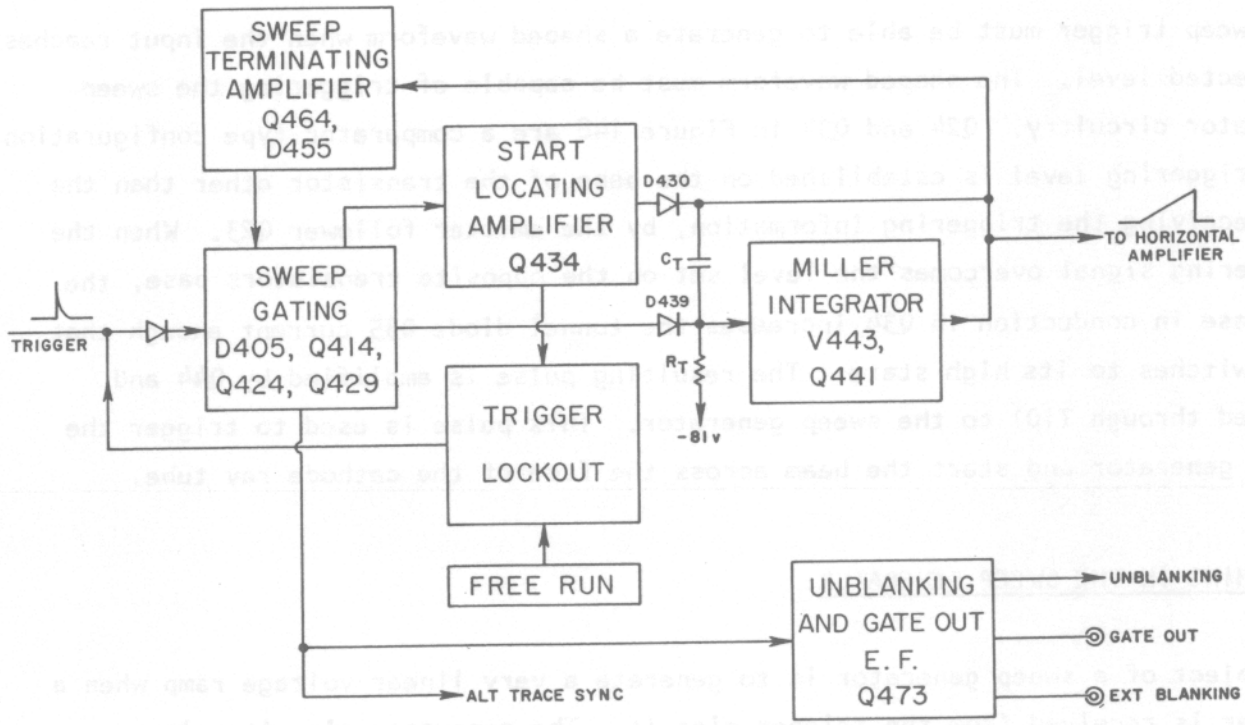
SWITCHING IN THE SWEEP GENERATOR:

The object of a sweep generator is to generate a very linear voltage ramp when a trigger is received from the trigger circuit. The generator circuits also typically generate signals to unblank the cathode ray tube and block triggering information until the sweep voltage has been generated and the circuit is completely recovered and ready to generate another ramp. Figure 150 is the sweep generator in the Tektronix Type 422 portable oscilloscope. Figure 149 is a block diagram of the circuitry in Figure 150. You will find Figure 150 as a pull-out schematic at the back of this book.

A switch provides for changing the values of C_T and R_T, the timing components in Figure 149, which changes the slope of the voltage ramp and, as a result, the time per centimeter of the instrument.

Referring to the block diagram in Figure 149, the overall operation will be considered first and then the switching investigated. The input to the sweep generator is a 15 nanosecond wide, 2 to 3ma current pulse generated by the sweep trigger circuits. The outputs are a 32V, positive going voltage ramp that runs from +3V to +35V, a negative going 600mv gate out waveform with a width as long as the duration of the sweep, and a negative going 5ma current waveform. Before a sweep is started, the sweep output is clamped at +3V by the start locating circuit

of D430 and Q434.



TYPE 422 SWEEP GENERATOR BLOCK DIAGRAM

B-422-0028
2-15-'65 ms

FIGURE 149

In the sweep gating block D405, a tunnel diode is in its low state. A trigger input switches the tunnel diode to its high state, and the positive step voltage generated by the tunnel diode is amplified, inverted, and applied as a negative going step to the anode of D439. D439 is referred to as a disconnect diode. Initially, D439 conducts, but the negative step cuts off or disconnects D439, and the Miller Integrator starts to generate a sweep. (Miller Integrators are covered in "Typical Oscilloscope Circuitry".)

The sweep output is fed on to the horizontal amplifier in the oscilloscope, and also fed to the sweep terminating amplifier. When the sweep reaches +35V, the sweep terminating amplifier takes part of the tunnel diode (D405) current, and the tunnel diode switches back to its low state. During the entire sweep and retrace plus an additional 5µsec, a lockout pulse is fed back to the sweep gating circuit to prevent the arrival of triggers. A new sweep cannot start until 5µsec after the end of the fall of the sweep ramp.

The block marked free run indicates that there are provisions to allow the sweep to re-occur without a trigger. When the trigger level control in the sweep trigger of the Type 422 is turned fully clockwise, triggers re-occur and the circuit free runs.

Let's examine Figure 150. Figure 150 pulls out and is at the back of the book. We have already stated that the sweep gating circuits develop a negative going step that disconnects the diode D439, and allows the sweep to start. We will deal with a qualitative analysis, stating values, and you may apply your analysis skills in justifying these.

Prior to a sweep, D405, a 2.2ma peak current tunnel diode, is conducting 1.3ma through the sweep terminating amplifier and about 0.4ma through diode D401. This establishes the tunnel diode current at about 0.5ma below its peak point current, and Q414 (a silicon transistor) is cut off. Q424 is conducting with its collector near ground. D439 is conducting; Q434 and D430 are conducting holding the output at about +3V. Q434 collector voltage is held at about 0.5V by diodes D435 and D436. The trigger lockout circuit D401 anode is at about 500mv (through T401 secondary).

The incoming trigger current pulse is formed in T401 and pulls the tunnel diode above its peak current. D405 anode voltage increases to about 500mv, and Q414 saturates. The quiescent current of 1.3ma in the sweep terminating circuit holds the tunnel diode in its high state. When Q414 saturates, its collector drops from about 4V to ground. This negative going step is coupled through D418, and disconnects D439 and the sweep starts to run up. The negative step also cuts off Q424, and its collector starts toward -12V, but D438 (a silicon diode) clamps the collector at about -1.6V. D439 having been cut-off by the initial negative step, is now held cut-off with its anode at -1.6V.

Q424 emitter drops to about 3V and its base is set solidly at 3.5V by the voltage regulator transistor Q429.

The emitter of Q434 also drops to 3V, and both Q434 and D430 cut-off. The collector of Q434, which was at about 0.5V, starts toward -12V, and D435 and D436 cut-off. This drop cuts off D401, and triggers cannot pass. This is the trigger lock-out

function.

The Miller Integrator ramp runs up, and the output is fed back to the sweep terminating amplifier. The Miller Integrator is made up of a nuvistor, a transistor, and two diodes, and is similar to the Miller Integrator discussed in "Typical Oscilloscope Circuitry", except that the Miller amplifier is a transistor rather than a vacuum tube. The nuvistor V443 is used to keep leakage current from the transistor out of the timing network. The nuvistor has a leakage current of only about 2-3 nanoamps. The disconnect diode D439 is a low leakage diode that has about 5 nanoamps leakage at 1V. C440 and R440 are the timing components, and are switched in to provide sixteen timing ranges.

Before a sweep starts, the grid of V443 is at -800mv, established by the regulator transistor Q429 in the sweep gating circuit, through D439. The same transistor sets the output point (collector of Q441) at 3V through D430.

The current path for D439 before the start of a sweep is from -80V through R440, R442, D439, and through Q424.

The current path for D430 before the start of a sweep is from ground, through Q441, D430, and R433 and Q434.

When the sweep gating circuit drops the anode of D439 to -1.6V, D439 disconnects or cuts off. Current through R440, the timing resistor that was flowing through D439, is now diverted to the timing capacitor C440, and the timing capacitor starts to charge. The grid of V443 starts to move toward -81V, and its cathode follows, driving the base of Q441. The voltage change applied to the base of Q441 is amplified and inverted at the collector. Q441 offers a gain of approximately 500 to 1000; therefore, the base need only move from 50 to 100mv for the collector to move through its entire voltage excursion.

The amplified and inverted (positive going ramp) is applied to the top of the timing capacitor, which opposes the change at the grid of V443. Since the voltage across the timing resistor R440 remains virtually constant, the current through the timing resistor and, therefore, the current into the timing capacitor, remains virtually constant. A constant charging current, of course, results in a linear

ramp voltage.

Prior to the sweep and during the sweep, R464 returned to +12V has been supplying about 1.3ma of current for the sweep gating tunnel diode D405. Transistor Q464 is off, and tunnel diode D455 is in its low state. As the sweep reaches its maximum desired level, D455 is pulled up until it switches to its high state, saturating Q464. Q464 shunts D405, pulls the bottom of R464 near ground, and D405 switches back to its low state. Q414 cuts off and D439 conducts, establishing the grid of V433 back at -800mv. Q441 conducts heavily, pulling its collector back down to 3V as rapidly as C440 can discharge. The discharge path for C441 is through R442, D439, Q424 (which is back on) to the 12V supply, to ground, and up through Q441. This is the retrace period.

As retrace starts, less and less current is pulled through D455 until, at the end of retrace, D455 switches back to its low state. Q464 turns off, and 1.3ma is once again supplied to D405. This makes D405 triggerable again, and it waits for a trigger. D401 is still cut-off, however, and triggers cannot reach D405. When retrace has dropped D430 cathode to about 3V, D430 conducts and once again establishes the sweep starting point at 3V. As D430 conducts, Q434 turns on. The collector of Q434 can only rise as fast as C401 can charge. It takes C401 about 5µsec to charge and bring D401 back into conduction; therefore, there will be about a 5µsec delay after retrace before triggers can reach D405 again. This is part of the hold-off time. When the collector of Q434 reaches about 500mv, D435 and D436 conduct and clamp the hold-off bus at this level.

The cathode ray tube has the electron beam turned off when there is no sweep. The sweep generator also puts out a waveform that turns on or unblanks the cathode ray tube. When there is no sweep, the collector of Q414 is about +4V with respect to ground. When a sweep is triggered, the collector of Q414 drops to near ground. At the end of the sweep, the collector of Q414 returns to near 4V. The positive going excursion at the end of the sweep is the alternate sweep or synchronizing pulse that we used to trigger multivibrators with earlier in this volume.

The levels at the collector of Q414 are applied to emitter follower Q473 and, when the collector of Q414 is at +4V, the cathode ray tube is blanked. When it is near ground, the cathode ray tube is unblanked.

My thanks to Chuck Miller for use of some of his Type 422 notes.

We have discussed some methods of approaching the analysis and perhaps the design of semiconductor amplifier and switching configurations. The individual should, and generally does, develop his own methods and approaches.

Any comments and constructive feedback on this series will be appreciated.

Jerry F. Foster

20. TRANSISTOR SPECIFICATIONS

HOW TO READ A SPECIFICATION SHEET

Semiconductors are available in a large variety of different types, each with its own unique characteristics. At the present time there are over 2200 different types of diodes and rectifiers and over 750 different types of transistors being manufactured.

The Characteristics of each of these devices are usually presented in specification sheets similar to the ones represented on page 205 and page 306 respectively. These specifications, particularly the transistor specification on the next page, contain many terms and ratings that are probably new to you, so we have selected several of the more important ones and explained what they mean.

NOTES ON TRANSISTOR SPECIFICATION SHEET

① The lead paragraph is a general description of the device and usually contains three specific pieces of information — The kind of transistor, in this case a silicon NPN triode, — A few major application areas, amplifier and switch, — General sales features, electrical stability and a standard size hermetically sealed package.

② The **Absolute Maximum Ratings** are those ratings which should not be exceeded under any circumstances. Exceeding them may cause device failure.

③ The **Power Dissipation** of a transistor is limited by its junction temperature. Therefore, the higher the temperature of the air surrounding the transistor (ambient temperature), the less power the device can dissipate. A factor telling how much the transistor must be derated for each degree of increase in ambient temperature in degrees centigrade is usually given. Notice that this device can dissipate 125mw at 25°C. By applying the given derating factor of 1mw for each degree increase in ambient temperature, we find that the power dissipation has dropped to 0mw at 150°C, which is the maximum operating temperature of this device.

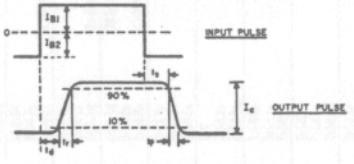
④ All of the remaining ratings define what the device is capable of under specified test conditions. These characteristics are needed by the design engineer to design matching networks and to calculate exact circuit performance.

⑤ **Current Transfer Ratio** is another name for beta. In this case we are talking about an a-c characteristic, so the symbol is h_{fe}. Many specification sheets also list the d-c beta using the symbol h_{FE}. Beta is partially dependent on frequency, so some specifications list beta for more than one frequency.

⑥ The **Frequency Cutoff** f_{hfb} of a transistor is defined as that frequency at which the grounded base current gain drops to .707 of the 1kc value. It gives a rough indication of the useful frequency range of the device.

⑦ The **Collector Cutoff Current** is the leakage current from collector to base when no emitter current is being applied. This leakage current varies with temperature changes and must be taken into account whenever any semiconductor device is designed into equipment used over a wide range of ambient temperature.

⑧ The **Switching Characteristics** given show how the device responds to an input pulse under the specified driving conditions. These response times are very dependent on the circuit used. The terms used are explained in the curves at right.



Courtesy of General Electric Company, Semiconductor Products Department

TABLE 1

2N337, 2N338

Outline Drawing No. 4

① The General Electric Types 2N337 and 2N338 are high-frequency silicon NPN transistors intended for amplifier applications in the audio and radio frequency range and for high-speed switching circuits. They are grown junction devices with a diffused base and are manufactured in the Fixed-Bed Mounting design for extremely high mechanical reliability under severe conditions of shock, vibration, centrifugal force, and temperature. For electrical reliability and parameter stability, all transistors are subjected to a minimum 160 hour 200°C cycled aging operation included in the manufacturing process. These transistors are hermetically sealed in welded cases. The case dimensions and lead configuration conform to JEDEC standards and are suitable for insertion in printed boards by automatic assembly equipment.

SPECIFICATIONS

② **ABSOLUTE MAXIMUM RATINGS: (25°C)**

Voltage			
Collector to Base	V_{CBO}	45	volts
Emitter to Base	V_{EBO}	1	volt
Current			
Collector	I_C	20	ma
③ **Power**			
Collector Dissipation*	P_C	125	mw
Temperature			
Storage	T_{STG}	−65 to 200	°C
Operating	T_A	−65 to 150	°C

④ **ELECTRICAL CHARACTERISTICS: (25°C)**
(Unless otherwise specified; $V_{CB} = 20v$; $I_E = -1$ ma; f = 1 kc)

		2N337			2N338			
⑤ **Small-Signal Characteristics**		**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	
Current Transfer Ratio	h_{fe}	19	55		39	99		
Input Impedance	h_{ib}	30	47	80	30	47	80	ohms
Reverse Voltage Transfer Ratio	h_{rb}		180	2000		200	2000	$\times 10^{-6}$
Output Admittance	h_{ob}		.1	1		.1	1	μmho
⑥ **High-Frequency Characteristics**								
Alpha Cutoff Frequency	f_{hfb}	10	30		20	45		mc
Collector Capacitance (f = 1 mc)	C_{ob}		1.4	3		1.4	3	μμf
Common Emitter Current Gain (f = 2.5 mc)	h_{fe}	14	24		20	26		
D-C Characteristics								
Common Emitter Current Gain ($V_{CE} = 5v$; $I_C = 10$ ma)	h_{FE}	20	35	55	45	75	150	
Collector Breakdown Voltage ($I_{CBO} = 50$ μa; $I_E = 0$)	V_{CBO}	45			45			volts
Emitter Breakdown Voltage ($I_{EBO} = -50$ μa; $I_C = 0$)	V_{EBO}	1			1			volt
Collector Saturation Resistance ($I_B = 1$ ma; $I_C = 10$ ma)	R_{SC}		75	150				ohms
($I_B = .5$ ma; $I_C = 10$ ma)	R_{SC}					75	150	ohms
⑦ **Cutoff Characteristics**								
Collector Current ($V_{CB} = 20v$; $I_E = 0$; $T_A = 25°C$)	I_{CBO}		.002	1		.002	1	μa
Collector Current ($V_{CB} = 20v$; $I_E = 0$; $T_A = 150°C$)	I_{CBO}			100			100	μa
⑧ **Switching Characteristics**								
Rise Time	t_r		.02			.06		μsecs
Storage Time	t_s		.02			.02		μsecs
Fall Time	t_f		.04			.14		μsecs

*Derate 1 mw/°C increase in ambient temperature over 25°C

REGISTERED JEDEC TRANSISTOR TYPES

For Explanation of Abbreviations, See Page 642.

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVco BVcb*	Ic ma	Tj°C	ELECTRICAL PARAMETERS MIN. hfe-hfe*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N22	Pt		120	−100	−20	55	1.9α							
2N23	Pt		80	−50	−40	55	1.9α							
2N24	Pt		120	−30	−25	50	2.2α							
2N25	Pt		200	−50	−30	60	2.5α							
2N26	Pt		90	−30	−40	55								
2N27	NPN		50	35*	100	85	100		1					
2N28	NPN		50	30*	100	85	100		.5					
2N29	NPN		50	35*	30	85	100		1		15	30		
2N30	Pt	Obsolete	100	30	7	40	2.2α		2T	17T				
2N31	Pt	Obsolete	100	30	7	40	2.2α		2T		150	25		
2N32	Pt	Obsolete	50	−40	−8	40	2.2α		2.7	21T				
2N32A	Pt	Obsolete	50	−40	−8	40	2.2α		2.7	21T				
2N33	Pt	Obsolete	30	−8.5	−7	40								
2N34	PNP	Obsolete	50	−25	−8	50	40		.6	40T			2N190	23
2N34A	PNP	Obsolete	50	−25	−8	50	40		.6	40T			2N190	23
2N35	NPN		50	25	8	50	40		.8	40T			2N169	22
2N36	PNP		50	−20	−8	50	45T			40T			2N191	23
2N37	PNP		50	−20	−8	50	30T			36T			2N190	23
2N38	PNP		50	−20	−8	50	15T			32T			2N189	23
2N38A	PNP		50	−20	−8	50	18T			34	−12	−3	2N189	23
2N41	PNP		50	−25	−15	50	40T			40T	−10	−12	2N190	23
2N43	PNP	AF	240	−30	−300	100	30	1	.5		−16	−45	2N43, 2N525	23, 24
2N43A	PNP	AF	240	−30	−300	100	30	1	.15		−16	−45	2N43A, 2N525	23, 24
2N44	PNP	AF	240	−30	−300	100	25T	1	.5		−16	−45	2N44, 2N524	23, 24
2N45	PNP	Obsolete	155	−25	−10	100	25T		.5	34	−16	−45	2N44	23
2N46	PNP		50	−25	−15	50	40T			4T	−10	−12	2N1414	24
2N47	PNP		50	−35*	−20	65	.975α				−5	−12	2N1414	24
2N48	PNP		50	−35*	−20	65	.970α				−5	−12	2N1414	24
2N49	PNP		50	−35*	−20	65	.975				−5	−12	2N1414	24
2N50	Pt		50	−15	−1	50	2α		3T					
2N51	Pt		100	−50	−8	50	2.2α				−350	−7		
2N52	Pt		120	−50	−8	50								
2N53	Pt			−50	−8									
2N54	PNP		200	−45	−10	60	.95α			40T			2N1098 16V	24
2N55	PNP		200	−45	−10	60	.92α			39T			2N1097 16V	24
2N56	PNP		200	−45	−10	60	.90α			38T			2N320	3
2N59	PNP		180	−25*	−200	85	90T*	−100		35T	−15	−20	2N1415	24
2N59A	PNP		180	−40*	−200	85	90T*	−100		35T	−15	−20	2N1415	24
2N59B	PNP		180	−50*	−200	85	90T*	−100		35T	−15	−20		

JEDEC No.	Type	Use	MAXIMUM RATINGS Pc mw @ 25°C	BVce BVcb*	Ic ma	Tj°C	ELECTRICAL PARAMETERS MIN. hfe-hfe*	@ Ic ma	MIN. fhfb mc	MIN. Ge db	MAX. Ico (μa)	@ Vcb	Closest GE	Dwg. No.
2N59C	PNP		180	−60*	−200	85	90T*	−100		35T	−15	−20		
2N60	PNP		180	−25*	−200	85	65T*	−100		35T	−15	−20	2N1415	24
2N60A	PNP		180	−40*	−200	85	65T*	−100		35T	−15	−20	2N1415	24
2N60B	PNP		180	−50*	−200	85	65T*	−100		35T	−15	−20	2N1925	24
2N60C	PNP		180	−60*	−200	85	65T*	100		35T	−15	−20	2N1926	24
2N61	PNP		180	−25*	−200	85	45T*	100		35T	−15	−20	2N1415	24
2N61A	PNP		180	−40*	−200	85	45T*	100		35T	−15	−20	2N1415	24
2N61B	PNP		180	−50*	−200	85	45T*	100		35T	−15	−20	2N1924	24
2N61C	PNP		180	−60*	−200	85	45T*	100		35T	−15	−20	2N1924	24
2N62	PNP		50	−35*	−20		.975αT							
2N63	PNP		100	−22	−10	85	22T	1		39T	−6	−6	2N1924	24
2N64	PNP		100	−15	−10	85	45T	1		41T	−6	−6	2N1415	24
2N65	PNP		100	−12	−10	85	90T	1		92T	−6	−6	2N324	3
2N66	PNP		1W	−40	.8A	80			.2		−300	−40		
2N67	PNP		2W	−25*	−1.5A	70				23T				
2N68	PNP		2W	−25*	−1.5A					23	−150 ma			
2N71	PNP		1W	−50	−250	60			.25	20				
2N72	Pt		50	−40	−20	55			2.5					
2N73	PNP		200	−50									2N1614	23
2N74	PNP		200	−50									2N1614	23
2N75	PNP		200	−20									2N1614	23
2N76	PNP	Obsolete	50	−20*	−10	60	.90α		1.0	34	−10	−20	2N322	3
2N77	PNP			−25*	−15	85	55		.70	44T	−10	−12	2N324	3
2N78	NPN	RF/IF	65	15	20	85	45*	1	5	27	3	15	2N78	22
2N78A	NPN	RF/IF	65	20	20	85	45*	1	5	29	3	15	2N78A	22
2N79	PNP		35	−30	−50		46		.7	44			2N321, 2N323	3, 3
2N80	PNP		50	−25	−8	100	80T				−30	−10	2N508, 2N1175	24, 24
2N81	PNP	Obsolete	50	−20	−15	100	20	1			−16	−30	2N1098	24
2N82	PNP		35 at 71° C	−20	−15	100	20	1			−16	−30	2N1098	24
2N94	NPN		30	20	5	75	40T	.5	3T	25T	3	10	2N169A	22
2N94A	NPN		30	20	5	75	40T	.5	6T	25T	3	10	2N169A	22
2N95	NPN		2.5W	25*	1.5	70	40		.4T	23T				
2N96	PNP		50	−30	−20	55	35		.5				2N1414	24
2N97	NPN		50	30	10	75	.85α		.5	38T	10	4.5	2N169 15V	22
2N97A	NPN		50	40	10	85	.85α		.5	38T	5	30	2N169A 25V	22
2N98	NPN		50	40	10	75	.95α		.8	47T	10	4.5	2N169A 25V	22
2N98A	NPN		50	40	10	85	.96α		.8	47T	10	4.5	2N169A 25V	22
2N99	NPN		50	40	10	75	.95α		2.0	47T	10	4.5	2N169A 25V	22
2N100	NPN		25	25	5	50	.99α		2.5	53T	10	4.5	2N170 6V	22
2N101	PNP		1W	−25*	−1.5	70				23T				
2N102	NPN		1W	25*	1.5	70				23T				
2N103	NPN		50	35	10	75	.60α		.75T	33T	50	35		

Courtesy of General Electric Company, Semiconductor Products Department

TABLE 2

Junction Transistor

GERMANIUM P-N-P ALLOY TYPE

For Medium-Speed Switching Service in Commercial and Military Data-Processing Systems

GENERAL DATA

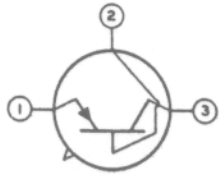
Mechanical:

Operating Position	Any
Maximum Length (Excluding flexible leads)	0.260"
Maximum Diameter	0.370"
Dimensional Outline	JEDEC No. TO-5
Case	Welded, Metal
Seals	Hermetic
Leads, Flexible	3
Minimum length	1.5"
Orientation and diameter	See *Dimensional Outline*

Terminal Diagram: BOTTOM VIEW

Lead 1 - Emitter

Lead 2 - Base



Lead 3 - Collector

SWITCHING SERVICE

Maximum and Minimum Ratings, *Absolute-Maximum Values:*

COLLECTOR-TO-BASE VOLTAGE	-30 max.	volts
EMITTER-TO-BASE VOLTAGE	-20 max.	volts
COLLECTOR-TO-EMITTER VOLTAGE:		
Base-to-emitter volts = 1	-20 max.	volts
Base open	-15 max.	volts
PEAK COLLECTOR CURRENT	-400 max.	ma
DC COLLECTOR CURRENT	-200 max.	ma
TRANSISTOR DISSIPATION:[a]		
At ambient temperature of 25° C	150 max.	mw
At ambient temperature of 55° C	75 max.	mw
AMBIENT-TEMPERATURE RANGE:		
Operating and storage	-65 to +85	°C
LEAD TEMPERATURE:		
For immersion in molten solder for 10 seconds maximum	240 max.	°C

[a] See accompanying *Rating Chart.*

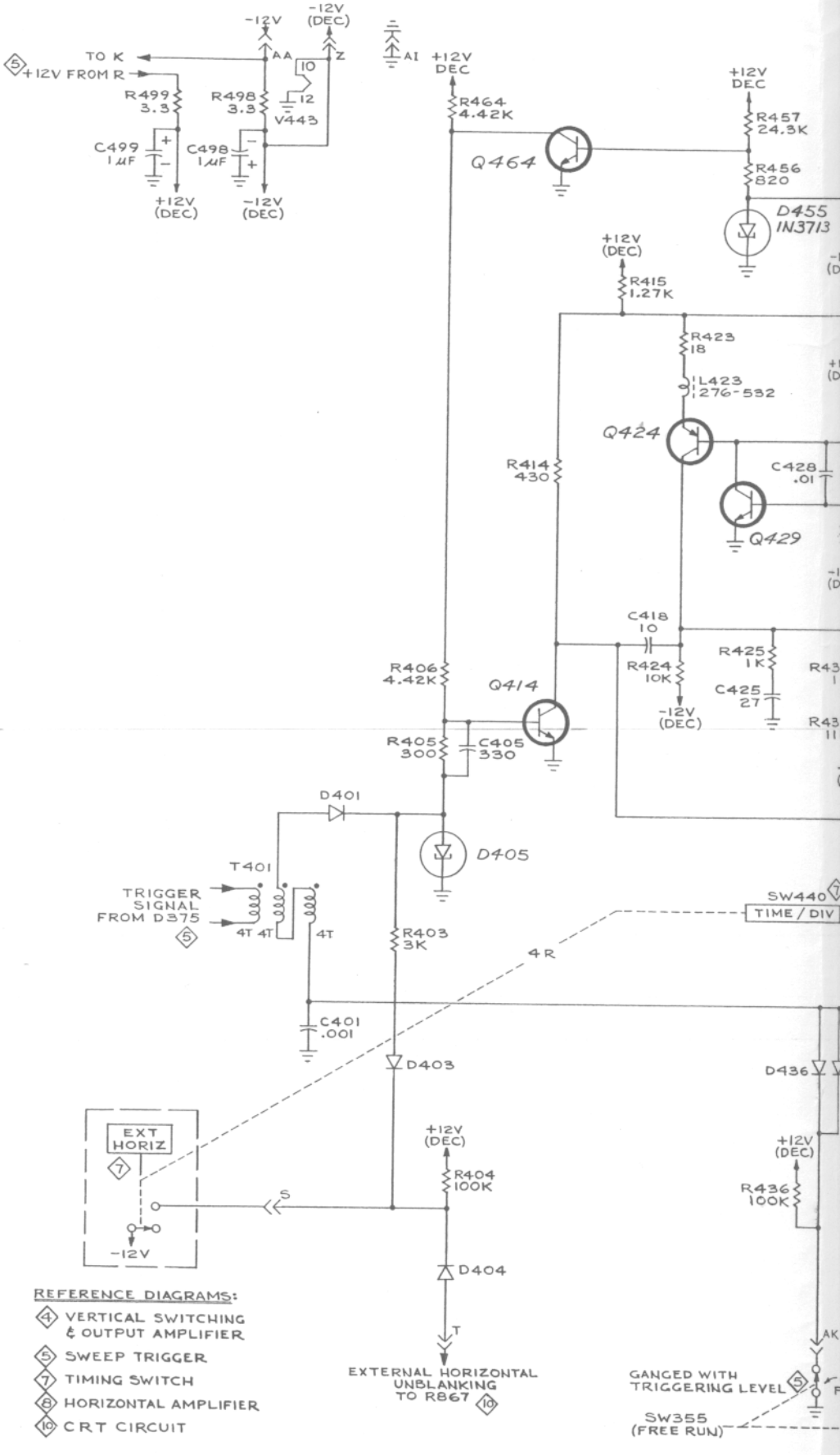
ELECTRICAL CHARACTERISTICS

Voltage values are given with respect to the base unless otherwise specified. Ambient temperature of 25° C.

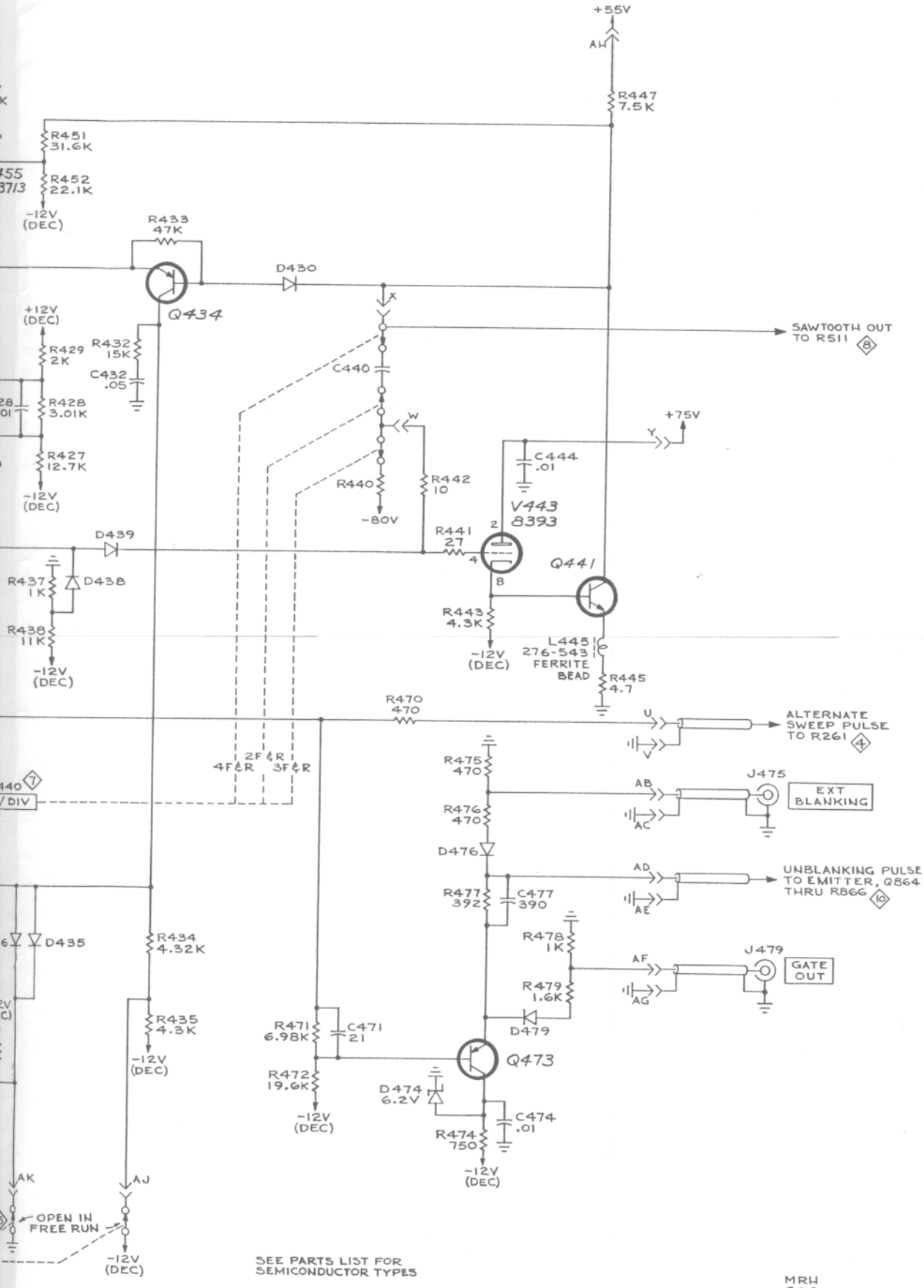
		Min.	Typical	Max.	
DC Collector-Cutoff Current for dc collector volts = -12, emitter open	I_{CBO}	-	-2	-5	μa
DC Emitter-Cutoff Current for dc emitter volts = -12, collector open	I_{EBO}	-	-2	-5	μa
Small-Signal Current Transfer Ratio for dc collector-to-emitter volts = -6, dc emitter ma. = 1, frequency of 1 kc.	h_{fe}	-	80	-	
Small-Signal Open-Circuit Reverse-Voltage Transfer Ratio for dc collector volts = -6, dc emitter ma. = 1, frequency of 1 kc.	h_{rb}	-	0.5×10^{-3}	-	
Alpha-Cutoff Frequency for dc collector volts = -6, dc emitter ma. = 1.	$f_{\alpha b}$	-	8	-	Mc
Small-Signal Short-Circuit Input Impedance for dc collector volts = -6, dc emitter ma. = 1, frequency of 1 kc.	h_{ib}	-	30	-	ohms
Extrinsic Base Resistance for dc collector-to-emitter volts = -6, dc emitter ma. = 1, frequency of 6 Mc.	$r_{bb'}$	-	120	-	ohms
Collector-to-Base Capacitance for dc collector volts = -6, dc emitter ma. = 1	C_{ob}	-	11	-	μμf
Power Gain for dc collector-to-emitter volts = -6, dc emitter ma. = 1, frequency of 1.5 Mc.	PG	-	16	-	db
Noise Factor for dc collector-to-emitter voltage = -6, dc emitter ma. = 1, frequency of 1.5 Mc	NF	-	6	-	db

Courtesy of Radio Corporation of America, Semiconductor and Material Department

TABLE 3



TYPE 422 OSCILLOSCOPE



SEE PARTS LIST FOR SEMICONDUCTOR TYPES

B1

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SWEEP GENERATOR 6