# SEMICONDUCTOR DIODES AND TRANSISTORS

## PROGRAMED INSTRUCTION



MANUFACTURERS OF CATHODE-RAY OSCILLOSCOPES

### VOLUME 3 TRANSISTORS

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### SEMICONDUCTOR DIODES AND TRANSISTORS

### VOLUME 3

### TRANSISTORS

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Mask covering second frame and response from first frame.

First Position:

Read the frame. Write in your response.

#### Second Position:

Move the mask down. Check your response with the one printed in the box in the lower left hand corner of newly exposed frame. Read the newly exposed frame and write in your response. Slide the mask down again, and repeat this step.



#### VOLUME 3 - TRANSISTORS

This volume is about the theory of operation of transistors, their characteristics, parameters and limiting factors. It discusses the operation of the transistor as an amplifier and as a switch. It further discusses methods of measuring the transistors characteristics and parameters and the effects of external energy and environment on the transistor.

#### PREREQUISITES:

This volume assumes the reader's successful completion of Semiconductor Diodes and Transistors - Volume 1 - Basic Semiconductors and Diodes, and Volume 2 - Diode Devices or their equivalent.

#### BROAD OBJECTIVES:

On <u>successful</u> completion of this volume, the reader will have gained knowledge of the theory and operation of junction transistors as amplifiers and switches and their characteristics, while preparing himself by meeting some of the prerequisites for volume 4 of this programed instruction series (Circuit Analysis 1 - Amplifiers).

#### SPECIFIC OBJECTIVES:

When the reader has <u>successfully</u> completed this volume, he will be able to do the following:

- Recall that a forward biased PN junction has majority carriers crossing the junction and becoming minority carriers. Some carriers move well beyond the junction before recombining. The average time the carriers exist as minority carriers is termed "minority carrier lifetime".
- 2. Recall that a different degree of doping in the two sides of a PN junction results in some carriers diffusing through the opposite side without recombining.
- 3. Recall that doping one side of a PN junction lightly and making it very narrow results in much of the current being transported by diffusion.

- 4. Recall that the N or the P side of the junction can be doped lighter and made narrow to enhance current by diffusion.
- Recall that two junctions can be formed in a single piece of semiconductor and the same action will take place at both junctions as when the basic diode is formed.
- 6. Recall that junction transistors are constructed by doping two junctions in a single piece of semiconductor, and that the center is doped much lighter than the ends to enhance diffusion current in the center.
- 7. Recall that the center portion of the transistor is made very narrow to enhance diffusion current in the center.
- 8. Name the three parts of the transistor and the paths of current carriers through the parts.
- Recall that forward bias is applied to the emitter-base junction which results in the emitter injecting carriers into the base.
- 10. Recall that the collector junction is normally reversed biased and depends on minority carriers in the base for current.
- 11. Recall the current distribution in the transistor when conducting.
- 12. Recognize the symbol for common base d-c current gain. Recall the definition of common base d-c current gain and be able to apply it to the solution of a problem dealing with transistor d-c currents.
- 13. Recognize the symbol for common emitter d-c current gain. Recall the definition of common emitter d-c current gain and be able to apply it to the solution of a problem dealing with transistor d-c currents.
- 14. Recall the proper polarities for biasing both junctions of the transistor. Recall the effects of a varying emitter or base current on the collector current and for a given change, while will result in the larger change in collector current.
- 15. Recall that without injected carriers from the emitter there will be some collector current carried by thermally generated carriers. Recognize its

symbol as  $I_{CBO}$  and recall that its magnitude will vary with temperature changes.

- 16. Define  $I_{CEO}$  and recall its relative magnitude with respect to  $I_{CBO}$ .
- 17. Recognize the symbols for both an NPN and a PNP transistor, and be able to label the parts.
- Recognize the common emitter configuration and recall its current gain capabilities with respect to unity.
- 19. Recall that both voltage gain and current gain are possible with a transistor in a common emitter configuration which makes possible a high power gain.
- 20. Recall the definition of the symbol  $h_{fe}$ , and recall that it does not take into account the circuit effects.
- 21. Recall the definition of the symbol  $h_{fb}$ , and recall that it does not take into account circuit effects.
- 22. Recall that voltage gain is possible with a transistor in a common base configuration and a corresponding power gain.
- 23. Recognize the common collector configuration and recall the magnitude of possible current and voltage gains with respect to unity.
- 24. Recall that the common collector configuration is also termed an "emitter follower".
- 25. Recall the definition of the symbol  $h_{fc}$  and its relative magnitude with respect to  $h_{fe}$ .
- 26. Recall the typical magnitude of input and output resistance of the common collector configuration.
- Recall that the emitter follower finds use in situations requiring high output currents to drive capacitance.
- 28. Recognize the collector family of curves for a transistor, and recall how it is plotted. Recall that it allows a cross reference of the transistors voltage and currents.

- 29. Recall that  $h_{fe}$  may be calculated from data gained from the collector family of curves or plotted directly on the 575 Transistor-Curve Tracer, and be able to apply this in making a measurement of  $h_{fe}$  when given the curves and the point of measurement.
- 30. Construct a load line on the collector family of curves by recalling what determines the slope of the load line and how to construct it when given appropriate values.
- 31. Construct a load line on a collector family of curves and determine the quiescent operating point when given a circuit with component values and a collector family of curves.
- 32. Recall the definition of transistor saturation,  $V_{CE}(sat)$ ,  $h_{FE}(sat)$ , and the bias condition at the collector junction at saturation.
- 33. Recall the bias conditions of the two junctions at saturation and that entering saturation increases the stored charge in the base of the transistor.
- 34. Given a circuit and collector family of curves, construct a load line, determine the static operating point base current, collector current, collector voltage and, given an applied signal current, determine <u>circuit</u> current gain.
- 35. Recognize avalanche breakdown on a collector family of curves, and recall that it relates to avalanche breakdown in the basic diode.
- 36. Recall the definitions and circuitry involved for B<sub>VCEO</sub>, B<sub>VCBO</sub>, and B<sub>VCER</sub>, and that they are all temperature sensitive. Recall the curves on which each is measured when using a collector family of curves.
- 37. Recall the factors limiting the maximum power handling capability of a transistor and the terminology involved.
- 38. Recognize the symbols used and recall their meaning when using a thermal to electrical analogy to gain parameters for dealing with thermal problems in transistors.
- 39. Recognize the change in the thermal to electrical analogy that takes place when a heat sink and silicone lubricant are used to increase the power

dissipation capabilities of a transistor.

- 40. Solve a problem determining maximum steady state power dissipation when given  $\Theta_{SA}$ ,  $\Theta_{LC}$ ,  $\Theta_{CS}$ ,  $T_A$  and  $T_{L}$  max.
- 41. Construct a maximum power curve on the collector family of curves of a transistor and recall the position of a load line for maximum output current swing.
- 42. Position a load line on the collector family of curves of a transistor for maximum output voltage swing.
- 43. Recall that very little power is dissipated by the transistor at cut-off or saturation, but that substantial power is dissipated in the area between these two limits which is termed the "active" or "transient" region.
- 44. Recall that when the transistor is acting as a switch, with its resting states at cut-off and saturation, it is possible for its load line to cross the maximum power hyperbola which allows greater power dissipation during switching than when a resting state occurs in the active region.
- 45. Recall that operating a transistor in the cut-off to saturated switching mode has the advantage of low resting state power dissipation, but the disadvantage of a larger stored charge which limits maximum repetition rate.
- 46. Recognize the symbols for the transistor switching parameters, and be able to define them. Recall what limits t<sub>on</sub> and t<sub>off</sub> of the transistor in the switching mode and a method of measuring the switching parameters.
- 47. Recall that the Tektronix Type 290 Transistor Switching Time Tester, or the Type 292 Semiconductor Tester in conjunction with a sampling system, may be used to check a transistor's switching times.
- 48. Recall the action of a speed-up capacitor when used to speed up a transistor switch, and be able to calculate the optimum value of speed-up capacitor given the voltage across the speed-up capacitor and the stored charge of the transistor.
- 49. Recall the meaning of current mode switching and that this mode reduces storage time which increases maximum possible repetition rate while sacri-

ficing maximum power dissipation with respect to the off to saturated mode.

- 50. Recall that current mode switching offers high speed, low noise, less critical transistor requirements, but more complicated design problems when compared to the off to saturated mode.
- 51. Recall that an avalanche switching transistor operates between cut-off and a point in the avalanche breakdown region and that the switching time can be on the order of fractional nanoseconds.
- 52. Recall that the main high frequency limiting factors of a transistor are junction capacitance transit time and the spreading out of carriers in the base.
- 53. Recognize the symbol for the cut-off frequency of a transistor in a common base configuration, and recall that it indicates the frequency at which low frequency  $h_{fb}$  has decreased to 0.707 of its low frequency value.
- 54. Recognize the symbol for cut-off frequency of the transistor in a common emitter configuration, and recall that it indicates the frequency at which  $h_{f_{e}}$  has decreased to 0.707 of its low frequency value.
- 55. Recognize the symbols for output capacitance of the transistor in a common emitter and a common base configuration, and recall that they are related by the formula  $C_{ob} = C_{oe} (1 + h_{fb})$ .
- 56. Recall that high frequency construction calls for a thin, uniform width base and that the narrower the base, the less the transit time and spreading out of the carriers.
- 57. Define  $f_t$  as the frequency at which low frequency  $h_{fe}$  has decreased to unity, and recall that  $f_t$  gives information on the transistor beyond  $f_{hfe}$ .
- 58. Recognize the construction of the rate-grown and alloy type transistors, and recall their high frequency limitations.
- 59. Recognize the construction of the micro alloy and micro alloy diffused transistors and recall their frequency limitations. Recall that the micro alloy diffused is sometimes termed a drift field transistor.

- 60. Recognize the construction of the mesa and the epitaxial mesa, and recall the advantages gained from the epitaxial layer.
- 61. Recognize the construction of the planar transistor, and recall the definitions of the terms "surface passivated" and "double diffused".

The reader will know when he has met these objectives by correctly answering 90% of the questions in the self-test at the back of this program.

#### INSTRUCTIONS

The material in this program is presented in a series of numbered statements. Each numbered statement is termed a "frame" and each group of frames bearing the same number (3, 3.1, 3.2, etc.) is termed a "set". The answer to each frame is in a small box in the lower left hand corner of the <u>following</u> frame.

The material is presented in three types of frames within a set; the "gating frame", the "teaching frame", and the "criterion frame".

The first frame in each set is the gating frame. Cover the following frame which contains the answers with the mask provided. Read the frame carefully, studying any diagrams that are provided and fill in the blanks. <u>Do not</u> look at the answer until you fill in the blanks.

You must know something about the material to fill in the blanks in the gating frames as there is no clue given to the answer. If you can answer the gating frame and you are sure of the material, skip to the next gating frame and continue. The gating frames are designed to give the student that is familiar with the subject an indication of the information contained in the set and allow him to skip the set if he feels he knows the information covered.

If you <u>cannot</u> answer the gating frame, continue with the teaching frames in that set, covering the answers and filling in the blanks. You <u>will</u> find <u>clues</u> to the answers in the teaching frames or their diagrams. The last frame in each set will have 2 (\*\*) asterisks following the number. This is the criterion frame and once again, no clue is given to the answers. The preceding teaching frames should have provided the information needed to work the criterion frame. If your answer is wrong, go back and review the material in the teaching frames.

You may progress through the program at any speed you select. Don't miss an opportunity to review the material in a set if you <u>can</u> answer the gating frame but are a little hazy on the subject.

This is <u>not</u> a <u>test</u>. You are not being graded and you are not expected to be able to answer the gating frames unless you have the knowledge to let you skip a set. If you answer the teaching frames or the criterion frames incorrectly, don't be concerned, but go back and review the previous frame or frames as needed. Answer from the information presented and, if your answer does not match, review the material before going on.

If you would like to measure your progress, go to the back of the volume and do the self test without grading it before proceeding with the programed material. After completing the programed material, do the self test again and grade both attempts. This will give you an indication of the gains that you have made with this volume.

Do each set of the programed material in sequence, starting with Set 1.

If you are ready to proceed with the programed material, turn to the first gating frame - - - -

A generator with a very high internal resistance with respect to the external circuit can be considered to be a constant \_\_\_\_\_\_ generator, and a generator with a very low internal resistance with respect to the external circuit can be considered to be a constant \_\_\_\_\_\_ generator.

1.1

1

The generator shown has zero internal resistance. Changes in the size of  $R_1$  have no effect on the voltage across  $R_1$ .



#### current voltage

1.2

The generator shown has a finite internal resistance represented by  $R_{\rm g}.$  The generator voltage will be distributed between \_\_\_\_\_ and



no answer needed

A generator can also be shown as a current generator shunted by a resistance. The current supplied by the generator shown divides between \_\_\_\_\_ and \_\_\_\_\_.



If  $R_{d}$  in the diagram has a value approaching infinity, most of the generator current is in \_\_\_\_\_.



1.5

If  $R_q$  in the diagram is not approaching infinity, but is very large with respect to  $\rm R_{L},$  most of the supplied current will flow in  $\rm R_{L}.$ 



1.3

1.4

R,

RL Rg

RL

1.6 A generator with an internal resistance very large with respect to the external circuit can be considered a <u>constant</u> current generator (referring to magnitude).

no answer needed

1.7 A generator with an internal resistance or impedance very large with respect to the circuit it is supplying can be considered a constant \_\_\_\_\_\_ generator, since the \_\_\_\_\_\_ will change very little with changes in the load resistance or impedance.

no answer needed

1.8 A constant current generator has a very \_\_\_\_\_ internal impedance with respect to the circuit it is supplying.

current current

1.9 A generator with a very low internal impedance with respect to the circuit it is supplying will have very little change in the output voltage with changes in the load.

1.10 A generator with a very low internal impedance with respect to the circuit it is supplying will supply a near constant\* \_\_\_\_\_ with changes in the load. (\* referring to magnitude)

no answer needed

1.11

A low impedance generator can be considered a \_\_\_\_\_\_\* voltage generator if it is driving a circuit with a much higher impedance. (\* referring to magnitude)

#### voltage

1.12\*\* A low impedance generator will supply a near constant \_\_\_\_\_\_ magnitude if driving a high impedance circuit and a high impedance generator will supply a near constant \_\_\_\_\_\_ magnitude if driving a low impedance circuit.

constant

1.13 END OF SET

voltage current

#### GATING FRAME - 2

A circuit or device can be said to be essentially current or voltage driven or biased depending on the \_\_\_\_\_\_ of the driving generator with respect to the \_\_\_\_\_\_ of the circuit being driven.

2.1

In the circuit shown, the resistance of R<sub>L</sub> must increase greatly to cause a significant change in the current in the circuit.



impedance impedance

2.2 The generator shown can be considered to be a constant amplitude generator.



no answer needed

2

Varying R will change the <u>current</u> in R<sub>L</sub>. R<sub>L</sub> is essentially current driven. (The current is changed which results in a voltage change.)



#### current

2.4 If the circuit or device to be driven changes its impedance when driven with voltage, it may be desirable to use a \_\_\_\_\_\_ impedance generator and essentially drive with current.

no answer needed

2.5 A d-c supply with a very high internal resistance with respect to its load is essentially a d-c \_\_\_\_\_\_ supply rather than a \_\_\_\_\_\_ supply.

high

2.3

For maximum transfer of power, the impedance of the generator or supply (is, is not) the case when should be equal to the load impedance. This it is desired to drive with current or voltage.

#### current voltage

2.7

The generator shown can be considered a constant\* generator. (\* referring to magnitude)



is not

2.8

d-c biasing can be accomplished with a \_\_\_\_\_\_ supply as well as a voltage supply.

If the resistance of the biasing supply is very high with respect to the device to be biased, the device can be said to be biased with \_\_\_\_\_\_.

current

2.10 Using a much higher than needed voltage and adding a high value of series resistance results in a near constant \_\_\_\_\_\_ biasing supply. (NOTE: At Tektronix, this approach is typically referred to as long tailing.)

current

2.11 By using a large value of resistance in series with a high voltage to bias a device results in the series resistor having control of the \_\_\_\_\_\_\_ in the circuit.

#### current

current

2.9

impedances

#### GATING FRAME - 3

Forward biasing a junction results in some carriers traveling well beyond the junction before recombining. The average time they exist after crossing the junction is termed minority carrier \_\_\_\_\_.

3.1

Forward bias reduces the potential difference across a PN junction and results in majority carriers crossing the junction. Electrons in the N side and holes in the P side cross the junction when forward bias is applied. Once across the junction, these carriers are existing as \_\_\_\_\_\_ carriers.

#### lifetime

#### minority

3.3 After crossing the junction and before recombination occurs, the carriers are existing as \_.

imperfections

3

The longer the carriers exist as minority carriers, the more opportunity they will have to spread out in the opposite side before recombining. With few imperfections near the junction, the carriers will \_\_\_\_\_\_ out in the opposite side.

minority carriers

3.5

The average time that the carriers exist as minority carriers before recombining is termed minority carrier lifetime. The fewer the imper-fections near the junction, the longer the \_\_\_\_\_

spread

3.6

If the minority carrier lifetime is long, some of the carriers will spread out through the entire opposite side of the junction without

minority carrier lifetime

3.7\*\*

Forward bias results in majority carriers crossing the junction. After crossing the junction, they exist as \_\_\_\_\_\_. The average time they exist after crossing the junction is termed \_\_\_\_\_\_.

recombining

minority carriers minority carrier lifetime

#### GATING FRAME - 4

Applying forward bias to a PN junction with the P side doped much lighter than the N side results in some of the electrons recombining with holes in the P side, but some of the electrons will \_\_\_\_\_\_ through the P side without \_\_\_\_\_\_.

4.1 Electrons crossing the junction as a result of applied forward bias must find imperfections before they can recombine. If the electrons do not find imperfections, they will not \_\_\_\_\_\_.

#### diffuse recombining

Electrons injected into the P side as a result of applied forward bias, but unable to find \_\_\_\_\_\_, spread out or "diffuse" in the P side and no not recombine.



4.2

4

Doping the P side much lighter than the N side results in many electrons injected into the P side by forward bias that cannot find imperfections to recombine. These electrons will \_\_\_\_\_\_ or spread out in the P side. \_\_\_\_\_\_ SOME ELECTRONS



4.4 Doping the P side with less impurities than the N side, results in forward bias injecting electrons into the P side that cannot readily recombine. These electrons are existing as \_\_\_\_\_ carriers while in the P side.

#### diffuse

4.5

Electrons crossing the junction (as a result of forward bias) that do not find imperfections, diffuse through the P side without recombining. Doping the P side with fewer imperfections than the N side results in some electrons through the P side without .



4.3

Some electrons diffusing through the P side are attracted to the positive side of the bias source. Doping the P side much lighter than the N side results in some of the current in the external circuit being the result of \_\_\_\_\_ current in the diode.



diffusing recombining

Current transported by both recombination and \_\_\_\_\_\_ will re-4.7 sult when electrons are injected into the P side and find insufficient imperfections to recombine.

#### diffusion

4.8\*\*

Doping the P side much lighter than the N side results in injected electrons that \_\_\_\_\_\_ through the P side without \_\_\_\_\_

diffusion

4.6

diffuse recombining Doping the P side much \_\_\_\_\_\_ than the N side and making the \_\_\_\_\_\_ (heavier, lighter) P side very \_\_\_\_\_\_ results in most of the injected electrons \_\_\_\_\_\_ (wide, narrow) diffusing through the P side without recombining.

Only a few of the electrons forced across the junction by applied forward bias find imperfections and \_\_\_\_\_\_ when the P side is doped much lighter than the N side.



5.2

5.1

The electrons forced across the junction by forward bias diffuse in the lightly doped P side. If the P side is made very narrow, most of the diffusing \_\_\_\_\_\_ pass through the P side without \_\_\_\_\_



5

Electron current in the external circuit results when electrons diffuse through the P side. The greater the number of diffusing electrons that cross the P material, the greater the external

#### electrons recombining

5.4

Electrons forced across the junction by forward bias and diffusing through the P side are existing as minority carriers. Forward bias current is made up primarily of \_\_\_\_\_\_



5.5\*\*

minority carriers or diffusion current diffusing minority

#### GATING FRAME - 6

Doping the N side of the junction much lighter than the P side and making the N side very narrow results in \_\_\_\_\_ diffusing through the \_\_\_\_\_ side when forward bias is applied.

6.1

Doping the N side much lighter than the P side of the junction results in more holes being injected into the N side than there are imperfections for recombination. If the holes do not find \_\_\_\_\_\_, they will not \_\_\_\_\_\_.

holes N

6.2 Holes injected into the N side that do not find imperfections,

6



6.4 Doping the N side much lighter than the P side and making the N side very narrow results in current by \_\_\_\_\_\_ of holes.



6.5 Applying forward bias to a junction with a lightly doped, narrow N side, injects \_\_\_\_\_\_ into the N side that \_\_\_\_\_\_ through without

diffusion

6.3

6.6\*\* The application of forward bias to a junction with a narrow and lightly doped N side results in current made up primarily of \_\_\_\_\_\_ that \_\_\_\_\_\_ through the N side.

> holes diffuse recombining

6.7 END OF SET

holes diffuse

#### GATING FRAME - 7

Two junctions can be formed in a single piece of semiconductor material in either a \_\_\_\_\_\_ or \_\_\_\_\_ arrangement. Forming two junctions in the same semiconductor results in holes and electrons at each junction, \_\_\_\_\_\_ until a state of \_\_\_\_\_\_ exists at both junctions.

7.1 If a piece of semiconductor has the two ends dopes with N type impurities and the center with P type impurities, there will be two distinct \_\_\_\_\_\_\_ in the material.



PNP or NPN recombining equilibrium or balance



junctions

7

With two junctions formed in the same semiconductor, recombination occurs at both junctions until the fermi levels line up. The alignment of the fermi levels indicates a state of \_\_\_\_\_\_.



7.4 With no external energy applied to a semiconductor containing two junctions, a potential difference exists across both junctions. The must be overcome to have current.



7.5 When two junctions are formed in one piece of semiconductor, the same action occurs at <u>both</u> junctions as when a single \_\_\_\_\_\_ is formed.

potential difference

7.3
7.6\*\* When two junctions are formed in a single piece of semiconductor, \_\_\_\_\_\_\_ occurs at both junctions until a state of \_\_\_\_\_\_ exists across both junctions.

junction

7.7 END OF SET

recombination equilibrium or balance Junction transistors are manufactured by forming two junctions in a single semiconductor, The center is doped much \_\_\_\_\_\_\_ than the ends (heavier, lighter) to enhance \_\_\_\_\_\_ current in the center.

8.1 A junction transistor functions by one end injecting carriers into the center portion and these carriers traveling as minority carriers through the center portion. Current in junction transistors relies on \_\_\_\_\_\_ current in the center portion.



8.2 Diffusion results when majority carriers are forced across the junction and are not able to find imperfections to recombine. Carriers forced across a junction that cannot imperfections, cannot \_\_\_\_\_\_ and, therefore, exist as \_\_\_\_\_\_ carriers.

diffusion (minority carrier)

8

8.3 Diffusing carriers are majority carriers that have been forced across a junction and are existing as minority carriers in the opposite side. Diffusing carriers unable to find \_\_\_\_\_\_ are existing as \_\_\_\_\_\_ carriers.

#### recombine minority

8.4 The center of the junction transistor is doped much lighter than the ends to enhance diffusion of carriers in the center portion. Carriers forced into the center portion will exist as \_\_\_\_\_ carriers and will \_\_\_\_\_ through the center portion.

# imperfections minority

minority

diffuse

8.5

With the center portion doped much lighter than the ends, some carriers will recombine in the center portion, but most of the carriers will through the center.





8.6\*\* Junction transistors are constructed by forming \_\_\_\_\_(#) junctions in the one piece of semiconductor. The center is doped much lighter than the ends to enhance \_\_\_\_\_\_ in the center.

diffuse

8.7 END OF SET

2 diffusion Junction transistors are manufactured by forming two junctions in a single piece of semiconductor. The width of the center portion between the two junctions is made very \_\_\_\_\_\_ to further enhance \_\_\_\_\_ by reducing

9.1 Junction transistors are made by doping the two ends of a semiconductor different than the center and forming two distinct \_\_\_\_\_.



Р	N	Ρ
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narrow, thin, etc. diffusion recombination

9.2 The center of the semiconductor is doped much lighter than the ends to enhance diffusion in the center. The wider the center portion, the more carriers will recombine and the less will \_\_\_\_\_\_.

junctions

9

The aim in junction transistors is to cause many of the carriers injected into the center portion to diffuse across the center region. The the center portion for given doping levels, the more (wider, narrower) carriers will diffuse across.

diffuse

Doping the center lightly results in a long minority carrier lifetime and enhances \_\_\_\_\_\_ of carriers.

#### narrower

9.5

The transistor utilizes diffusion of carriers through the center portion of the device. The center portion is made very \_\_\_\_\_\_ to reduce recombination and increase \_\_\_\_\_\_.



#### diffusion

9.3

9.4

9.6 The center of the transistor is doped much lighter than the ends to enhance diffusion in the center. The center is made very narrow to enhance carrier \_\_\_\_\_\_ and to reduce recombination.

> narrow, thin, etc. diffusion

9.7 Light doping in the center results in a long minority carrier lifetime and less carrier \_\_\_\_\_.

diffusion

9.8\*\* The center portion of a junction transistor is made very \_\_\_\_\_\_ to enhance carrier \_\_\_\_\_\_ and reduce carrier \_\_\_\_\_.

recombination

9.9 END OF SET

narrow, thin, etc. diffusion recombination That part of the transistor considered the source of current carriers is termed the \_\_\_\_\_\_ and the center part, the \_\_\_\_\_\_. The remaining part is termed the \_\_\_\_\_\_. The current carriers move through the parts of the transistor in \_\_\_\_\_\_ order as/than just stated.

10.1 The transistor works on the principle of one end of the device injecting or emitting carriers into the center portion. Once injected, the carriers either recombine or \_\_\_\_\_\_ through the center portion.



10.2 Since one end injects or emits carriers into the center portion, it is called the \_\_\_\_\_\_ and is considered the source of current carriers in the transistor.



diffuse

10

The center portion of the transistor is termed the base. The emitter injects carriers into the \_\_\_\_\_.



## emitter

10.4 The emitter injects carriers into the base. Some of the carriers recombine but, due to the base being made very thin, most of them \_\_\_\_ through the base.

## base

10.5 The carriers that diffuse through the base are collected by the remaining end of the transistor. The three parts of the transistor are the emitter, base and the \_\_\_\_\_.



diffuse

10.3

10.6 The emitter injects carriers into the base; the injected carriers diffuse through the base, and those that do not recombine are collected by the

## collector

10.7 Those carriers that recombine in the base become <u>base lead</u> or simply base current. Base lead current is <u>(recombination, diffusion)</u> current.

# collector

10.8\*\* Carriers are injected by the emitter into the \_\_\_\_\_ and diffuse to the \_\_\_\_\_. Those carriers that recombine in the base become \_\_\_\_\_ lead current.

recombination

10.9 END OF SET

base collector base

GATING FRAME - 11

11.1 The emitter-base junction must be forward biased to have current. To accomplish this, the current through the junction or the voltage across the junction can be controlled for biasing purposes.

> current voltage

11.2 A high resistance d-c source (with respect to the emitter-base junction) will essentially control the junction \_\_\_\_\_\_ for biasing purposes.

no answer needed

11.3 A low resistance d-c source (with respect to the emitter-base junction) will essentially control the junction \_\_\_\_\_\_ for biasing purposes.

current

11

11.4 A vacuum tube has the controlling circuit reversed biased\* and uses a d-c voltage source normally for biasing purposes \*(grid made negative with respect to the cathode).

#### voltage

11.5 A transistor has the emitter-base junction (its controlling circuit) forward biased in most cases and the junction resistance varies with voltage changes.

no answer needed

11.6 It is common to find a high resistance d-c source used to bias a
transistor's emitter-base junction since it is a
biased junction.
(forward, reverse)

no answer needed

11.7 Controlling the \_\_\_\_\_\_ in the emitter-base junction of a transistor for biasing purposes is common, since the emitter-base junction is normally \_\_\_\_\_\_ biased.

#### forward

Forward biasing a junction with current requires that the current source force majority carriers to cross the junction to recombine.

> current forward

11.9 When a biasing source is shown or referred to in this program, it can be either a voltage or current source, depending on its internal

no answer needed

11.10 Forward biasing the emitter base junction can refer to forcing current with a current source or voltage with a voltage source. In either case, the junction potential difference must be

(increased, reduced)

# resistance (impedance)

Forward bias applied to the emitter-base junction can be essentially a 11.11\*\* current or voltage source depending on its internal with respect to the emitter-base d-c resistance. A high resistance source will be essentially a \_\_\_\_\_\_ biasing source.

reduced

11.8

# 11.12 END OF SET

resistance current The potential difference at the emitter-base junction must be reduced for the emitter to inject carriers into the base. This is done by applying \_\_\_\_\_\_ bias to the emitter-base junction. Those injected carriers that \_\_\_\_\_\_ recombine, diffuse through the base. Those carriers that do recombine make up what is termed \_\_\_\_\_\_ current.

12.1

Recombination occurs at both junctions until the fermi levels line up after two junctions are formed in a single piece of semiconductor. The fermi levels line up indicating a state of \_\_\_\_\_\_.



12.2

Both junctions are at equilibrium with no external energy applied. The emitter \_\_\_\_\_\_\_ injecting carriers into the base without external energy applied.





12



FIGURE 12

Forward bias applied reduces the potential difference between emitter and 12.3 base, allowing majority carriers to move across the junction. Majority carriers become minority carriers, and those that do not recombine through the base as shown in figure 12.

is not

12.4 Forward bias injects many carriers into the base that cannot find imperfections and recombine. This is a result of the base being doped much lighter than the \_\_\_\_\_.

diffuse

12.5 Figure 12 shows both a PNP and an NPN transistor with forward bias applied, emitter to base. For both PNP and NPN transistors, the emitterbase junction is \_\_\_\_\_\_ biased to inject carriers into the base.

emitter

12.6 The carriers that do recombine make up base lead current. This current is generally referred to simply as \_\_\_\_\_ current.

forward

12.7 The term base current refers to the current in the base lead as a result of carrier \_\_\_\_\_\_ in the base.

12.8

Carriers injected into the base that do not recombine exist as minority carriers and \_\_\_\_\_\_\_\_\_\_ through the base.

#### recombination

base

12.9\*\*

Injection of majority carriers from the emitter into the base is accomplished by application of \_\_\_\_\_\_ to the emitterbase junction. Injected carriers that do not recombine, \_\_\_\_\_\_ through the base as \_\_\_\_\_\_ carriers. Carriers that recombine in the base result in a current in the base connecting lead that is termed current.

diffuse

12.10

END OF SET

forward bias diffuse minority base



FIGURE 13

- 13 The collector to base junction of a transistor is \_\_\_\_\_\_ biased and its current depends on minority carriers present due to thermal energy or carriers that are injected into the base from the \_\_\_\_\_\_ that do not recombine.
- 13.1 The carriers injected into the base that do not recombine are existing as minority carriers. In order to collect them, the collector-base junction is \_\_\_\_\_\_ biased, as shown in figure 13.

#### reverse emitter

13.2 Figure 13 shows both a NPN and a PNP transistor with biasing. Reverse biasing the collector-base junction causes this junction's current to be dependent on the number of minority carriers available in the \_\_\_\_\_

## reverse

13.3 Collector current is dependent on minority carriers in the base. Varying the number of injected minority carriers will vary the \_\_\_\_\_ in the collector junction.

base

13.4 The magnitude of the current in the reverse biased collector junction is dependent on the number of \_\_\_\_\_\_ carriers available in the base.

#### current

13.5 Reverse bias to the majority carriers will accelerate minority carriers across the junction if they enter the transition region.

#### minority

13.6 Without injected carriers from the emitter, the collector current is limited by the number of minority carriers in the base as a result of \_\_\_\_\_\_ energy.

no answer needed

13.7 The carriers injected from the emitter into the base that do not recombine are existing as \_\_\_\_\_\_ carriers in the base.

13.8 The diffusing carriers in the base, injected by the emitter, provide a supply of minority current carriers for the \_\_\_\_\_\_ junction.

#### minority

13.9\*\* The collector-base junction is \_\_\_\_\_ biased; its current magnitude is governed by the \_\_\_\_\_ carriers in the base as a result of heat energy or injection from the \_\_\_\_\_.

collector

13.10 END OF SET

reverse minority emitter

Base current is the result of \_\_\_\_\_\_ in the base and collector current is made up of carriers that \_\_\_\_\_\_ through the base. The emitter current in a transistor is the sum of \_\_\_\_\_\_ and \_\_\_\_\_ current.

14.1 Forward biasing the emitter-base junction injects carriers into the base. Some carriers recombine and the rest \_\_\_\_\_\_ through the base.



#### 14.2

Those injected carriers that do not recombine in the base and become base lead current diffuse through the base to the \_\_\_\_\_\_.





14.3 The carriers injected into the base from the emitter either recombine and become base lead current or \_\_\_\_\_\_ to the collector and become collector current.



14.4 Base current is defined as the current in the base lead as a result of carrier \_\_\_\_\_.

diffuse

14.5

Collector current is the current in the collector lead that has \_\_\_\_\_\_ across the base.

recombination





14.6 The sum of the carriers diffusing to the collector and the carriers that recombine in the base is equal to the \_\_\_\_\_ current.



## diffused

14.7 Figure 14 shows both a NPN and a PNP transistor indicating currents.  $I_E$  (d-c emitter current) is equal to the sum of  $I_C$  (d-c collector current) and  $I_B$  (d-c base current).  $I_C = 20$  ma,  $I_B = 1$  ma,  $I_E =$ \_\_\_\_\_.

#### emitter

 $I_{E} = 50 \text{ ma}, I_{B} = 2 \text{ ma}, \text{ therefore } I_{C} = \_$  I refers to the current in the base lead as a result of carrier \_\_\_\_\_ in the base.

21 ma

# 14.9 END OF SET

48 ma recombination 15

The d-c current in the collector  $(I_{C})$  can be calculated by taking the product of d-c emitter current  $(I_{E})$  and the d-c current gain factor, emitter to collector. This factor is referred to as \_\_\_\_\_ or

15.1

The d-c current in the collector  $(I_{C})$  is a percentage of the current in the emitter. In the diagram, collector current is \_\_\_\_\_% of emitter current.



15.2

2 If the current in the emitter (I<sub>E</sub>) in the diagram is 10 milliamperes, the current in the collector (I<sub>C</sub>) is \_\_\_\_\_ milliamperes.



alpha h<sub>FB</sub> 15.3 The product of emitter current and the percentage of the emitter current that flows in the collector will give the value of \_\_\_\_\_\_ current.

9.6

15.4 If 92% of the emitter current flows in the collector, and the emitter current is 5 milliamps, the collector current is \_\_\_\_\_ milliamps.

#### collector

15.5 The d-c current gain from <u>emitter</u> to <u>collector</u> will be less than unity and the collector current will be \_\_\_\_\_\_ than the emitter current. (more, less)

4.6

15.6 The fraction of emitter current that flows in the collector is called d-c alpha. The d-c current gain factor, emitter to collector, is termed d-c \_\_\_\_\_.

less

15.7 The symbol that indicates d-c alpha is h<sub>FB</sub> and this is the current gain from \_\_\_\_\_\_ to collector.

alpha

15.8

The h in the symbol for d-c current gain stands for "hybrid" and simply indicates that it is a hybrid parameter.

emitter

15.9 The term "hybrid" indicates an approach to analyzing transistor circuits and the h indicates that the particular parameter so designated can be used with the \_\_\_\_\_\_ approach.

no answer needed

15.10 The "F" in the d-c current gain symbol indicates "forward d-c current gain" and the "B" indicates the common point for measurement.

hybrid

15.11 The symbol "h<sub>FB</sub>" indicates hybrid forward current gain from emitter to collector since the B indicates that the \_\_\_\_\_\_ is the common point.

no answer needed

15.12 The product of "d-c alpha" or "h<sub>FB</sub>" and the emitter current will give the value of collector current. If alpha is 0.97 and emitter current is 2 milliamps, collector current is \_\_\_\_\_ milliamps.

#### base

15.13 The symbol h<sub>FB</sub> represents the d-c current gain factor of a transistor, from emitter to collector. h<sub>FB</sub> will always be less than \_\_\_\_\_

# 1.94

15.14\*\* The symbol for d-c current gain <u>emitter</u> to <u>collector</u> is \_\_\_\_\_\_\_ and the product of d-c current gain and emitter current is equal to

one, unity, etc.

# 15.15 END OF SET

h<sub>FB</sub> collector current (Ι<sub>C</sub>) The product of the d-c base current (I<sub>B</sub>) and the d-c current gain factor from base to collector will give the value of \_\_\_\_\_\_ current. This current transfer factor is given the symbol \_\_\_\_\_\_ and called "d-c \_\_\_\_\_".

16.1 The collector current in the diagram is 98% of emitter current. The base current is 2% of emitter current. This means the collector current is



16.2 The d-c current gain, base to collector, of the transistor in the diagram is 49. This means that the d-c collector currents is 49 times greater than the d-c \_\_\_\_\_\_ current.



16

49

3 If the base current in the diagram is 10 milliamps, the collector current is \_\_\_\_\_\_ milliamps.



16.4 The symbol given the d-c current gain factor is  $h_{FE}$  and is termed "d-c beta".  $I_B \times h_{FE} =$ \_\_\_\_\_.

490

I<sub>C</sub>

base

16.5 "h<sub>FE</sub>" indicates hybrid forward d-c current gain, base to collector, since the E indicates that the \_\_\_\_\_\_ is the common point.

16.3

16.6 If a transistor has an h<sub>FE</sub> or d-c "beta" of 60 and a d-c base current of 15 milliamps, the collector d-c current will be \_\_\_\_\_ milliamps.

emitter

16.7

 $h_{FE}$  or d-c beta can be found by dividing the d-c collector current by the d-c base current. (symbol) =  $\frac{I_C}{I_R}$ 

900

16.8\*\* The d-c current gain factor, base to collector, is given the symbol
\_\_\_\_\_\_. The product of \_\_\_\_\_\_\_ and d-c base current will
give the value of d-c collector current.

h<sub>FE</sub>

16.9 END OF SET

The emitter base junction of a transistor is the controlling circuit and changes in emitter-base current or voltage will be accompanied by a change in the \_\_\_\_\_ current. A change in the base-emitter will have the more linear effect.

17.1

17

The emitter-base junction of a transistor has a voltage versus current curve resembling that of a conventional diode.



Once the potential difference of the emitter-base junction has been 17.2 reduced, majority carriers cross the junction.

no answer needed

current
17.3 Due to the difference in the doping levels in the emitter and the base, only a few of the carriers from the emitter find imperfections and accomplish \_\_\_\_\_\_.

no answer needed

17.4

Those carriers that do not recombine, \_\_\_\_\_\_ to the collector and become collector current.

recombination

17.5 A change in the emitter-base junction voltage will change the number of carriers injected from the emitter and thus change the number diffusing to the \_\_\_\_\_\_.

diffuse

17.6

The emitter-base junction El curve shows that the current <u>does</u> not change linearly with changes in applied forward voltage.



collector

When the applied forward voltage on the emitter-base junction is varied to 17.7 change the current, the resultant change is non-\_\_\_



no answer needed

Since driving the emitter-base junction with voltage results in a non-17.8 linear result, it is common to find transistors driven with \_\_\_\_ sources.

linear

Driving the transistors emitter-base junction with a high impedance 17.9 drive. source is essentially (current, voltage)

current

17.10 Current driving the emitter base junction allows linear changes to be accomplished. This requires a \_\_\_\_\_\_ impedance input generator. (high, low)

current

17.11\*\* The emitter base junction is typically driven to give (voltage, current) the most linear change in the transistor currents.

high

17.12 END OF SET

current

Carriers are injected from the emitter into the base when the emitterbase junction is forward biased. The collector junction is \_\_\_\_\_\_ biased and depends on the injected carriers in the base for current. A change in emitter or base current will be accompanied by a change in collector current. For a given change in emitter and base current, varying \_\_\_\_\_\_ current will have the largest effect on collector current.

18.1 The emitter-base junction is normally forward biased. Since the base is doped much lighter than the emitter, only a few of the injected carriers find imperfections and recombine. The remaining carriers diffuse in the base as \_\_\_\_\_\_ carriers.

reverse base

18.2 The collector junction is reverse biased and depends on minority carriers for current. There are a few minority carriers present in the base at room temperature due to heat energy, but most minority carriers in the base have been injected from the \_\_\_\_\_\_.

minority

18.3 The number of minority carriers present in the base can be changed by varying either emitter or base current. Varying the number of \_\_\_\_\_\_\_ carriers in the base will vary collector current.

emitter

18.4 Consider that the base is doped with only one tenth as many imperfections as the emitter. Ten units of current flowing in the emitter will inject ten units of current into the base; one unit recombines in the base and the remaining nine units will \_\_\_\_\_\_ to the collector.

## minority

18.5 With the base doped one tenth as much as the emitter, increasing the emitter current by ten units of current will increase the base current by one unit and the collector current by \_\_\_\_\_ units.

diffuse

18.6 If a ten unit change in the emitter current results in a nine unit change in collector current, the a-c signal current gain, emitter to collector, is less than \_\_\_\_\_\_.

nine

18.7 Increasing the base current (of the same transistor as frame 18.6) by one unit of current causes an increase of ten units to be injected into the base from the emitter. One unit recombines in the base while the other nine add to \_\_\_\_\_\_ current.

one, unity

18.8 The a-c signal current gain, base to collector, of the transistor in frame 18.7 is \_\_\_\_\_\_.

## collector

#### nine

18.10\*\* A change in \_\_\_\_\_\_ or \_\_\_\_\_ current will be accompanied by a change in collector current. For the <u>same amount</u> of variance, a change in \_\_\_\_\_\_ current will be accompanied by the largest change in collector current.

less greater

18.11 END OF SET

emitter base base

- 19.1 At room temperature, there are some holes in the N material and some free electrons in the P material as a result of heat energy forming holeelectron pairs. These are \_\_\_\_\_\_ carriers.

minority carriers temperature

19.2 The emitter-base junction is forward biased (in the majority of applications) to the majority carriers and this opposes the movement of \_\_\_\_\_\_\_ carriers across the emitter-base junction.

minority

19.3 The collector-base junction is reversed biased (in most applications) to the majority carriers and enhances the movement of carriers across the collector junction.

19

There will be some current in the collector circuit when it is reverse biased (even if the emitter is open), because of the minority carriers present due to \_\_\_\_



The current in the diagram is temperature dependent as a change in 19.5 temperature changes the number of \_\_\_\_\_ carriers available.



19.6

The current in the diagram is given the symbol  $I_{CBO}$  indicating d-c current between collector and base with the emitter open.  $I_{CBO}$  is the result of "hole - \_\_\_\_\_".



In the symbol I CBO, the capital I indicates d-c current, the subscripts CB indicate that the current is between collector and base, and the subscript 0 indicates that the remaining element, the \_\_\_\_\_ is open circuited.

electron pairs

19.8

ICBO is the current at the collector junction carried by \_\_\_\_\_ carriers present as a result of thermal energy.  $I_{CBO}$  will flow with the emitter lead \_\_\_\_\_\_ circuited.

# emitter

19.9\*\* There is current in the collector junction when it is reverse biased, even if the \_\_\_\_\_ lead is open circuited. This current is given the symbol \_\_\_\_\_\_. A change in temperature will change the magnitude of \_\_\_\_\_

> minority open

END OF SET 19.10

> emitter CBO СВО

19.7





With bias voltages applied, there is some collector current with the base lead open circuited. This current is made up of minority carriers and is given the symbol \_\_\_\_\_\_. It is approximately equal to \_\_\_\_\_\_ x I<sub>CBO</sub>.

20.1



20.2

Opening the base lead as shown in figure 20 results in minority carriers crossing both junctions. With the base doped much lighter than the emitter, many minority carriers are injected into the base from the emitter with the condition in figure 20.

#### minority

20.3

I<sub>CBO</sub> is limited by the carriers present due to heat energy. With the condition in figure 20, the number of minority carriers in the base is increased by approximately d-c beta or \_\_\_\_\_ (symbol).

no answer needed





20.4 The minority carriers in the base are increased by approximately the d-c current gain of the transistor when the condition in figure 20 exists. There will be more \_\_\_\_\_ carriers available in the base than for the I<sub>CBO</sub> condition.

h<sub>FE</sub>

minority

20.6 The current termed  $I_{CB0}$  is magnified by  $\approx h_{FE}$  with the conditions in figure 20.  $I_{CB0} \times h_{FE} \approx$ \_\_\_\_\_.

larger

20.7\*\* I<sub>CEO</sub> indicates d-c current between \_\_\_\_\_ and \_\_\_\_\_ with the base lead open circuited. It is approximately equal to the product of I<sub>CBO</sub> and \_\_\_\_\_.

C EO

20.8 END OF SET

collector emitter h<sub>fe</sub>



21.1

The solid vertical line in the transistor symbol indicates the base. The line (without the arrow head) intersecting the base at an angle indicates





21.2 The line containing an arrow head that intersects the base at an angle indicates the \_\_\_\_\_\_.



collector

21

21.3 In an NPN transistor, the carriers are electrons injected from the emitter into the base. In the diode symbol, electrons flow \_\_\_\_\_\_ the symbol arrow point as shown in the diagram.



#### emitter

21.4 The emitter-base of a transistor is a PN junction and in the symbol electrons will flow \_\_\_\_\_\_ the tip of the arrow. (into, out of)



# into

21.5

The symbol shown has electrons flowing into the tip of the arrow. The arrow indicates that electrons are flowing from the emitter into the



into

21.6 An NPN transistor has the emitter injecting electrons into the base. The symbol shown must be a/an \_\_\_\_\_\_ transistor.



#### base

21.7 The emitter of a PNP transistor injects holes into the base. Holes move in the direction that the arrow is pointing in a diode symbol. The transistor shown must be a/an \_\_\_\_\_\_ transistor.



# NPN

21.8

PNP transistors have the emitter arrow pointing \_\_\_\_\_\_\_\_ the (toward, away from) base and NPN transistors have their emitter arrow pointing \_\_\_\_\_\_\_ (toward, away from) the base.





PNP

21.9\*\* The symbol shown is a/an \_\_\_\_\_ transistor. If the emitter arrow were pointing the other way, it would be the symbol for a/an \_\_\_\_\_ transistor. The part of the symbol containing the arrowhead indicates the \_\_\_\_\_.



toward away from

21.10 END OF SET

PNP NPN emitter

The transistor in the diagram is a/an \_\_\_\_\_ type and is in a common \_\_\_\_\_\_ configuration. A transistor in this configuration will give current gain \_\_\_\_\_ than unity. (less, greater) than unity. O OUT

22.1 The transistor in the diagram has the arrow indicating the emitter pointing away from the base. Electrons flow \_\_\_\_\_\_\_ the arrow in the symbol.



- NPN emitter greater
- 22.2 Electrons are injected into the base from the emitter in an NPN transistor. The diagram shown is a/an \_\_\_\_\_\_ transistor.



against

22

22.3 Grounding the emitter makes it <u>common</u> to both the input and output circuits. The transistor in the diagram has its emitter \_\_\_\_\_\_ to both the input and output circuits.



PNP

22.4 The grounded or common emitter circuit has the transistors' \_\_\_\_\_\_\_as its input point, and the transistors' \_\_\_\_\_\_as its output point.



#### common

22.5

A small change in input (base) current in the common emitter circuit will be accompanied by a \_\_\_\_\_\_ change in output (collector) current. (larger, smaller)

base collector 22.6 It is possible for the common emitter configuration to give a current gain greater than unity. The output (collector) current change can be larger than the change in the \_\_\_\_\_\_ current.

## larger

22.7\*\* The transistor in the diagram is an NPN type. The emitter injects \_\_\_\_\_\_ into the base. The current gain of this common \_\_\_\_\_\_ configuration can be greater than unity.



input (base)

22.8 END OF SET

electrons emitter Voltage gain along with current gain can be accomplished with the common \_\_\_\_\_\_ configuration making possible a high power gain.

23.1 The common emitter configuration allows a current gain greater than unity. The signal current in the output can be \_\_\_\_\_\_ than the signal current in the input.

## emitter

23.2 The emitter junction is forward biased while the collector junction is \_\_\_\_\_\_ biased in most amplifier configurations.



greater, larger, etc.

Forward bias is necessary at the emitter junction for carrier injection into the base. The emitter junction has a low impedance because it is biased.



#### reverse

23.4 The collector junction offers a higher impedance than the emitter junction because the collector junction is \_\_\_\_\_ biased.



#### forward

By ohms law, a current through a high impedance will develop a larger 23.5 voltage than the same current through a low impedance. There is a higher impedance at the \_\_\_\_\_\_ junction than at the \_\_\_\_\_\_ junction.



#### reverse

23.6 Voltage gain is possible with the common emitter configuration. Since the \_\_\_\_\_\_\_ is a higher impedance circuit, the current in the collector circuit develops a larger voltage than at the base.

# collector emitter

23.7 A small voltage change applied to the base to emitter circuit of a common emitter configuration can cause a larger voltage change at the

## collector

23.8 The common emitter configuration offers a high power gain because both current and \_\_\_\_\_\_ gain are possible.

### collector

23.9\*\* The common emitter configuration offers both \_\_\_\_\_ and \_\_\_\_\_ gain, making possible a large power gain.

#### voltage

# 23.10 END OF SET

current voltage The <u>small signal</u>, a-c current gain of the transistor in a common emitter configuration is given the symbol \_\_\_\_\_\_. This parameter \_\_\_\_\_\_\_\_. Include circuit effects on current gain.

24.1 Small signal indicates that the transistor will operate only over a small portion of its possible operating range. Forcing a transistor to operate to the extremes of its operating range of currents and voltages considered small signal.
(is, is not)

> h<sub>fe</sub> does not

24.2 Small signal characteristics are expressed by small or incremental changes. The small signal current gain indicates the amount that a/an \_\_\_\_\_\_ current change will be amplified.

is not

24.3 The common emitter configuration has the \_\_\_\_\_\_ as its input and the collector as its output with the \_\_\_\_\_\_ common to both.

small, incremental

24

24.4 A change in the base current of a common emitter configuration will be accompanied by a larger current change in the \_\_\_\_\_\_ circuit.

# base emitter

24.5 Varying the voltage on the collector junction will also cause a change in collector current. The effect of a collector voltage change on collector current will be much smaller than the effect of a/an current change on collector current.

collector

24.6 In order to gain an accurate measurement of the control of input current on the output current, the output \_\_\_\_\_ must be held constant.

input (base)

24.7 The current gain of the transistor in a common emitter configuration can be measured by varying the input current, noting the change in output current while holding output \_\_\_\_\_ constant.

### voltage

24.9

The transistor current gain parameter,  $\mathbf{h}_{fe}$  is referred to as small signal "beta". The small signal current gain from base to collector is called

#### emitter

24.10

h<sub>fe</sub> may be calculated by dividing the change in collector current by the applied change in base current while holding collector voltage constant.

$$h_{fe} = \frac{\Delta I_c}{\Delta I_b} \Delta V_{ce} = 0$$

 $\Delta$  = Incremental change  $I_{c} = Collector current$  $I_{\rm b}$  = Base current V<sub>ce</sub> = Voltage \_\_\_\_\_ to emitter

beta

24.11 h<sub>fe</sub> is the current gain of the <u>transistor</u> <u>only</u> when placed in a common emitter configuration. The effects of the \_\_\_\_\_ will also have to be taken into account when calculating total <u>circuit</u> current gain.

collector

24.12

$$h_{fe} = \frac{\Delta I_c}{\Delta I_b} \qquad \Delta V_{ce} = 0$$

The current gain parameter  $h_{fe}$  take into account losses (does, does not) take into account losses

circuit

24.13\*\* The symbol h<sub>fe</sub> indicates a transistor current gain parameter. It

be used with a transistor in a common base configuration. (would, would not) It \_\_\_\_\_\_\_\_\_take into account the effects of the circuit on current (does, does not) gain.

does not

24.14 END OF SET

would not does not A transistor in a common base configuration will give a current gain \_\_\_\_\_\_. The small signal, a-c current gain of the transistor in a common base configuration is given the symbol \_\_\_\_\_. This parameter take into account (does, does not) the effects of the circuit on current gain.

The common base configuration has the emitter as the input, the collector 25.1 as the output, and the \_\_\_\_\_ common to both.



Comparing the common base to the common emitter, the emitter junction is 25.2 biased in both and the collector junction is \_\_\_\_\_ biased in both. Only the configuration or orientation of the transistor is different.



25

base

25.3 A change in the emitter (input) current in the circuit in the diagram will result in a \_\_\_\_\_\_ change in the collector (output) circuit.



forward reverse

25.4 The output current will always be smaller than the input current in a common \_\_\_\_\_\_ configuration.

# smaller

25.5 The current gain of the common base configuration can be said to be less than one (unity), since the output current will be \_\_\_\_\_\_ than the input current.

base

A change in the emitter current will be accompanied by a change in the 25.6 collector current. A change in the voltage on the collector junction will also result in a change in \_\_\_\_\_ current.

less, smaller, etc.

To make an accurate measurement of the relation of a varying emitter 25.7 current to collector current, the collector \_\_\_\_\_ must be held constant.

## collector

The small signal, a-c current gain of the transistor in a common base con-25.8 figuration is referred to as small signal "alpha" and given the symbol (does, does not) take into account the effects of h<sub>fb</sub>. This parameter \_\_\_\_ the circuit on current gain.

## voltage

25.9

while holding the output \_\_\_\_\_ constant.

 $h_{fb} = \frac{\Delta I_c}{\Delta I_c} \Delta V_{cb} = 0$  $\Delta =$  Incremental change C = Collector current (output) l e = Emitter current (input)  $V_{cb} = Voltage collector to base (output)$ 

h<sub>fb</sub> can be calculated by dividing the output current by the input current

does not

25.10\*\*\* The small signal current gain of the transistor in a common base configuration is given the symbol \_\_\_\_\_\_. This current gain parameter be used for a transistor in a common emitter configur-(would, would not) ation. The effects of the circuit \_\_\_\_\_\_ taken into account by this parameter.

voltage

25.11 END OF SET

h<sub>fb</sub> would not are not

- Since the collector junction is a \_\_\_\_\_\_ impedance circuit and the emitter junction is a \_\_\_\_\_\_ impedance circuit, voltage gain can be accomplished with the common base configuration and a corresponding \_\_\_\_\_\_ gain.
- 26.1 Common base current gain is less than unity. The current in the collector (output) circuit will be \_\_\_\_\_\_ than the current in the emitter (input) circuit.

high low power

26.2 Reverse biasing the collector results in a high impedance collector circuit with respect to the low impedance, \_\_\_\_\_\_ biased emitter circuit.

less

26.3 The product of collector impedance and collector current can be greater than the product of emitter current and emitter impedance. This indicates that voltage gain is possible.

26

26.4 Although current gain is less than unity in the common base configuration, voltage gain greater than unity is possible and a corresponding \_\_\_\_\_\_ gain may be realized.

no answer needed

26.5 The product of current gain (less than unity) and voltage gain (greater than unity) will give the \_\_\_\_\_ gain.

power

26.6\*\* Power gain is possible with the common base configuration although the current gain is \_\_\_\_\_\_ \_\_\_\_ \_\_\_\_ since there is the possibility of \_\_\_\_\_\_ gain.

power

26.7 END OF SET

less than unity voltage

The transistor shown is in a common \_\_\_\_\_\_ configuration. gain is possible with this configuration with a (Current, Voltage) corresponding power gain. IN FORWARD HAS HAS TREVERSE BIAS

27.1 The \_\_\_\_\_\_ serves as the input, the \_\_\_\_\_\_ serves as the output, and the \_\_\_\_\_\_ is common to both in this configuration.



27.2 The input signal voltage is applied at the base and will be distributed across the emitter-base junction and the resistance in the emitter circuit.



TOTAL DISTRIBUTION OF INPUT VOLTAGE

base emitter collector

27
27.3 If the emitter resistor has a high resistance with respect to the resistance of the emitter-base junction, most of the input voltage will be across the



27.4 Since the voltage across the emitter resistor is only part of the input voltage, the voltage across the emitter resistor will always be less than the input voltage.

emitter resistor

27.5 Signal voltage at the emitter can never be equal to or larger than the applied signal voltage at the \_\_\_\_\_\_ terminal of a transistor in the common collector configuration.

27.6 The emitter is the output point and the base is the input point. Since the emitter signal voltage can never equal the base signal voltage, the voltage gain is less than \_\_\_\_\_\_.

base

27.7 The emitter current is the sum of base and collector current. The handles the greatest amount of current in the transistor.

one, unity

27.8 The current gain of a transistor in a common collector configuration is greater than unity. The current in the emitter is greater than the current in the

emitter

27.9 The voltage gain of a common collector configuration is less than unity. Power gain is possible, however, as this configuration yields \_\_\_\_\_\_ gain.

base (input)

Since the emitter current is equal to collector current plus base current of the transistor in the diagram, its current gain can be greater than



The common collector configuration has the largest potential current 27.11 gain of the three transistor configurations, since the input is at the lowest current point on the transistor while the output is taken from the \_\_\_\_\_ current point.

## one, unity

The common collector configuration can yield power gain even though its 27.12\*\* voltage gain is less than unity, since \_\_\_\_\_ gain is possible.

highest, largest, etc.

27.10

### current

\_\_\_\_\_

28.1 An increase in base current will be accompanied by an increase in collector and emitter currents. In the transistor shown, an increase in input current will be accompanied by an \_\_\_\_\_ in the output current.



28.2

A positive voltage change on the base will be accompanied by an increase in base current and an increase in collector and \_\_\_\_\_\_ current.



28

A positive voltage change on the base will cause an increase in emitter 28.3 current and a positive \_\_\_\_\_ change at the emitter.



The voltage and current changes at the emitter will follow the changes 28.4 at the base. The \_\_\_\_\_ follows the \_\_\_\_\_.

## voltage

The voltage changes at the emitter of an emitter follower configuration 28.5 can never be larger than the voltage changes at the base. The current changes at the emitter, however, can be much larger than the current changes at the \_\_\_\_\_

> emitter base

28.6\*\* The emitter changes follow the base changes in the common collector configuration. This configuration is commonly referred to as an \_\_\_\_\_

base (input)

28.7 END OF SET

emitter follower

The small signal, low frequency current gain parameter for the <u>transistor</u> in a common collector configuration is given the symbol \_\_\_\_\_\_. It is equal to h<sub>fe</sub> + \_\_\_\_\_\_.

29.1 A change in base current in an emitter follower will give a collector current change equal to  $h_{fe} \times \Delta I_B$ . The change in emitter current is equal to the sum of the collector current change and the \_\_\_\_\_ current change.

29

$$\Delta I_{E} = \Delta I_{C} + \Delta I_{B}$$
$$\Delta I_{C} = h_{fe} \Delta I_{B}$$
$$\Delta I_{E} = h_{fe} \Delta I_{B} + \Delta I_{B}$$
$$\Delta I_{E} = (h_{fe} + 1)' \Delta I_{B}$$
$$\Delta I_{E} = h_{fc} \Delta I_{B}$$

h<sub>fc</sub> is the same as \_\_\_\_\_

base

h<sub>fc</sub> 1 29.3 Since  $h_{fc}$  is the same as  $h_{fe}$  + 1, the potential current gain is greatest for the common \_\_\_\_\_\_ configuration.

h<sub>fe</sub> + 1

29.4\*\* Emitter follower small signal current gain parameter is given the symbol \_\_\_\_\_\_. It has the same value as \_\_\_\_\_\_.

collector

29.5 END OF SET

The common collector configuration offers a high \_\_\_\_\_\_ resistance and a low \_\_\_\_\_\_ resistance.

30.1 The output from the common collector (emitter follower) configuration is taken at the emitter. The emitter is a \_\_\_\_\_\_ current point with (high, low) respect to the other transistor terminals.

## input output

30

high

30.3 Since the emitter follows the base, some of the input voltage change is, in effect, cancelled due to the emitter moving in a/the polarity direction as/than the base. 30.4 In comparing the common collector to the common emitter configuration, it will take a greater voltage change at the base to cause the same current change in the common collector configuration.

same

The requirement of a larger voltage change to cause the same current 30.5 in the change indicates the input resistance is (greater, smaller) emitter follower than in the common emitter configuration.

no answer needed

The output point of the emitter follower has nearly the same voltage 30.6 change as at the input, but a much larger current change. This indicates resistance at the output than the input. a much (higher, lower)

### greater

The emitter follower offers a high \_\_\_\_\_\_ resistance and a low 30.7\*\* resistance.

lower

# 30.8 END OF SET

input output

31 The emitter follower configuration with its high input resistance and low output resistance finds use in applications requiring high output to drive capacitance.

31.1 The emitter follower input resistance is made large by the negative feedback (emitter following the base) from the emitter. The base is a high resistance, \_\_\_\_\_ current point. \_\_\_\_\_ (high, low)

### current

31.2 The emitter has a low resistance and is a \_\_\_\_\_\_ current point. (high, low) Taking the output at the emitter allows high output currents, with respect to other points in the emitter follower circuit.

low

31.3 The emitter follower finds much use as an impedance matching circuit that also offers \_\_\_\_\_\_ gain greater than unity. (current, voltage)

high

31.4 Since the emitter follower offers a high output current, it is often used to drive circuits with high input capacitance. The emitter follower can provide current to charge \_\_\_\_\_\_ that would load down the output of other configurations.

# current

31.5

#### capacitance

31.6\*\* The \_\_\_\_\_\_ configuration is noted for high input resistance and low output resistance and its ability to drive capacitance because it can supply a high output \_\_\_\_\_.

capacitance

31.7 END OF SET

common collector (emitter follower) current



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FIGURE 32

GATING FRAME - 32

32 A chart such as the one in figure 32 shows the transistor's characteristics over a range of currents and voltages. The "collector \_\_\_\_\_\_\_ of curves" shown is for the common \_\_\_\_\_\_\_ configuration. Each curve represents a value of \_\_\_\_\_\_ current and allows a cross reference of the transistor's currents and voltages.

32.1 The horizontal scale in figure 32 is in units of collector to emitter voltage. \_\_\_\_\_\_ current is plotted vertically.

family emitter base

32.2 Each individual curve on the chart in figure 32 is for a given value of base current. Another way of stating this is to say that current is the running parameter.

# Collector

32.3

The chart in figure 32 is called a collector family of curves. The voltages and currents in the collector circuit are shown at several values of \_\_\_\_\_\_ current resulting in a group or family of curves.

base



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FIGURE 32

A given point on a base current curve gives a cross reference of collector current and collector \_\_\_\_

base

The base current in the collector family of curves in figure 32 varies 32.5 between zero and 100  $\mu\text{amps}$  . The base current curve near the bottom of the chart indicates \_\_\_\_\_ base current.

## voltage

According to the chart in figure 32, for a given value of  $V_{CF}$ , an 32.6 increase in base current results in a/an \_\_\_\_\_ in \_\_\_\_\_ (increase, decrease) collector current.

### zero

Each curve in the chart in figure 32 indicates a given value of base 32.7 current. The slope of the base current curve indicates the effect of voltage on collector current.

increase

32.4



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FIGURE 32

32.8 An increase in collector voltage causes a/an \_\_\_\_\_\_ in collector current for a given value of base current as shown by the curves in figure 32.

## collector

32.9 Each curve in the collector family of curves in figure 32 represents a value of base current. When base current ( $I_B$ ) is 60 µamps and collector voltage ( $V_{CE}$ ) is 5 volts, collector current ( $I_C$ ) is \_\_\_\_\_ma.

### increase

32.10 Any point along a base current curve gives a cross reference of collector current and voltage. The 30 μamp base current curve crosses the 1.6ma collector current point at \_\_\_\_\_\_ volts of collector voltage.

3

5

32.11 From the collector family of curves in figure 32, with a collector voltage of 7 volts and a collector current of 3.5ma, there is \_\_\_\_\_ μamps of base current.

32.12\*\* The collector family of curves for a common emitter configuration is a plot of \_\_\_\_\_\_ voltage versus \_\_\_\_\_\_ current for different values of \_\_\_\_\_\_ current, allowing a cross reference of the transistor's voltages and currents.



## 32.13 END OF SET

collector collector base



FIGURE 33

h<sub>fe</sub> may be calculated from data gained from the collector family of curves of the transistor. It may also be calculated from data gained by plotting collector current versus \_\_\_\_\_\_ current directly on the 575 Transistor-Curve Tracer.

33.1 h<sub>fe</sub> can be calculated from data gained by varying base current while holding collector voltage constant and noting the change in collector current.

base

33.2 To hold collector voltage constant on a collector family of curves, the measurements are made along only one vertical line indicating collector voltage.

no answer needed

33.3

The measurements made on the collector family of curves in figure 33 are made along the vertical line indicating \_\_\_\_\_ volts of  $V_{CF}$ .

no answer needed

33



The assumed change in base current in figure 33 is \_\_\_\_\_  $\mu$ amps. This is accompanied by a change in collector current (along the 5 volt  $V_{CE}$  line) of \_\_\_\_\_ ma.

33.5

$$n_{fe} = \frac{\Delta I_{C}}{\Delta I_{B}} \qquad \Delta V_{CE} = 0$$

At the point selected for measurement on the collector family of curves in figure 33,  $h_{fe} =$ \_\_\_\_\_\_.

20 1

5

33.6

In the second display in figure 33, base current is plotted directly against collector current and the slope of the line indicates  $h_{fe}$ . Each step represents \_\_\_\_\_  $\mu$ amps of base current.

$$\frac{\Delta I_{C}}{\Delta I_{B}} = \frac{\Delta I_{M}}{\Delta 20 \ \mu a} = 50$$

33.7

Photo B in figure 33 is a direct plot of base current versus collector current. The horizontal scale is not given a dimension because each step in the display corresponds to a given value of base current.

10



no answer needed

33.9 The measurement used to determine h<sub>fe</sub> from the collector family of curves in figure 33 was made between a base current of <u>10</u> and <u>30</u> μamps. To gain the same results from photo B in figure 33, the measurements should be made between \_\_\_\_\_\_ and \_\_\_\_\_ μamps of base current.

base current

33.10

Making these same measurements at a different point on the curves in figure 33 will result in a different value of \_\_\_\_\_.

10 30

h<sub>fe</sub>

33.11 h<sub>fe</sub> will change with the selected point of operation of the transistor. The slope of the line indicating h<sub>fe</sub> in photo B of figure 33 is not straight because \_\_\_\_\_ has different values at different points of operation.



FIGURE 33

33.12 Make a few measurements of  $h_{fe}$  at different points on the curves in figure 33.

h<sub>fe</sub>

33.13 To have the transistor whose curves are shown in figure 33 operate with a collector current of 2.5 ma and a collector voltage of 4 volts, there must be \_\_\_\_\_\_ μa of base current.

no answer needed

33.14\*\* h<sub>fe</sub> may be found from the collector \_\_\_\_\_\_ of curves. When base current is plotted directly against collector current on the 575, the slope of the line indicates \_\_\_\_\_.

50

33.15 END OF SET



To gain information on the operation of the transistor in a circuit, a load line may be drawn on the collector family of curves. The slope of the d-c load line is determined by the \_\_\_\_\_\_ in series with the transistor.

34.1 With supply voltages applied to the transistor and the transistor nonconducting, the full collector supply voltage appears across the transistor. One limit of the transistor's operation is the collector

#### resistance

34.2

Considering that the transistor is short circuited, the amount of current flowing is governed by the value of collector supply voltage and the total series resistance. One limit of the transistor's operation may be found by dividing the collector supply voltage by the total

### supply voltage

34.3 Figure 34 shows a transistor with a resistance in series to the collector supply. The slope of the line on the collector family of curves is determined by the \_\_\_\_\_.

series resistance

34



FIGURE 34

34.4 The load line in figure 34 intersects the base line at 10 volts on the collector family of curves. If the transistor is non-conducting, there will be \_\_\_\_\_\_ volts, collector to emitter.

#### resistor

34.5

Considering that the transistor is a short circuit, current is limited by the series resistance in the circuit; in the case in figure 34, K ohms.

10

34.6

With the transistor shorted, the full supply voltage is across the series resistance. With the transistor in figure 34 shorted, there are \_\_\_\_\_\_\_volts across 2.2K ohms.

2.2

34.7

With the transistor shorted, the current flow is calculated by dividing the voltage across the series resistance by the resistance. With the transistor in figure 34 shorted, the current is \_\_\_\_\_m amps.

$$I = \frac{V_R}{R} = \frac{10V}{2.2K} = \frac{?}{?}$$

10



34.8 The load line is constructed between the two extremes calculated in the previous frames and shown in figure 34. The extremes are \_\_\_\_\_ m amps and \_\_\_\_\_ volts.

4.54

34.9 Construct a load line on the collector family of curves in figure 34 for the same circuit if the collector supply were 5 volts instead of 10.

> 4.54 10

34.10 The load line constructed in frame 34.9 parallel to the (is, is not) load line for a supply voltage of 10 volts.

THE LOAD LINE SHOULD EXTEND BETWEEN 2.27ma on the vertical scale and 5 volts on the horizontal scale.

34.11 The slope of the load line does not change when a different supply voltage is used, since the slope is determined by the value of \_\_\_\_\_.

is

34.12\*\* The d-c load line is constructed between the two extremes of d-c operation. These two extremes are found by considering the transistor is first

> \_\_\_\_\_\_ then \_\_\_\_\_. The slope of the d-c load line is determined by the series \_\_\_\_\_\_.

resistance

34.13 END OF SET

open, shorted (any order) resistance




## TEST SETUP

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 $R_{L} = COLLECTOR LOAD RESISTOR$ 

 $R_{F} = BASE BIASING RESISTOR$ 

 $V_{CC} = COLLECTOR SUPPLY VOLTAGE$ 

FIGURE 35

Construct a d-c load line for the circuit in figure 35.  $\rm R_{F}$  sets the operating point base current at a value of \_\_\_\_\_ µamps.

Consider that the transistor in figure 35 is open circuited. The voltage 35.1 across the transistor will be the collector supply voltage or \_\_\_\_\_ volts.

> load line on following page 20

One extreme of the transistor's operation is the supply voltage. To find 35.2 the other extreme, consider that the transistor is \_\_\_\_\_\_ circuited.

35.3 With the transistor in figure 35 short circuited, the current is limited by  $\rm R_{L}$  . The full supply voltage will be dropped across  $\rm R_{L}$  and the current will be \_\_\_\_\_ ma.

short



FIGURE 35-A

35.4 The two extremes for the transistor in figure 35A are: (1) 10 volts V<sub>CE</sub> with zero collector current and, (2) \_\_\_\_\_ma I<sub>C</sub> with zero collector volts. A line connecting these points is the d-c load line.

$$\frac{10V}{5K} = 2 \text{ ma}$$

2

35.5

Since the voltage, base to emitter, is a very small value (a few tenths of a volt), consider that the full supply voltage is across  $R_F$ . The current through  $R_F$  is then \_\_\_\_\_.

$$\frac{V_{RF}}{R_{F}} = \frac{10V}{500K} = -?$$

35.6

The current through  $R_F$  is  $I_B$  of the transistor.  $I_B$  is \_\_\_\_\_\_ for the transistor in figure 35-A.

10V = 20  $\mu$ amps 500K

35.7 The static (no applied signal) operating point of the transistor in figure 35-A is indicated by the point at which the 20 μamp base current curve intersects the load line. The collector current at this point is

about

20 µamps



FIGURE 35-A

35.8 Figure 35-A shows the load line and operating point for the circuit in figure 35. The collector voltage at the operating point is about \_\_\_\_\_ volts.

1.15ma

35.9

The static or no input signal conditions of the transistor in figure 35-A are:  $I_B =$ \_\_\_\_\_,  $I_C =$ \_\_\_\_\_, and  $V_{CE} =$ \_\_\_\_\_.

## 4.2V

1.15 ma

35.10

Since  ${\rm I}_{\rm F}$  is the sum of collector and base current, the emitter current at the static operating point in figure 35-A is \_\_\_\_\_ma.



Turn to figure 35C for answer





 $R_L = COLLECTOR LOAD RESISTOR$  $R_F = BASE BIASING RESISTOR$  $V_{CC} = COLLECTOR SUPPLY VOLTAGE$ 

FIGURE 35-B

A transistor is termed in \_\_\_\_\_ when the collector junction becomes forward biased. The collector to emitter voltage at which this occurs is given the symbol \_\_\_\_\_. The current gain at saturation is given the symbol \_\_\_\_\_.

36.1

In most small signal amplifier applications, the transistor remains in the most linear portion of its operating characteristics. This falls somewhere between the non-conducting or cut-off state, and the condition where the collector junction becomes forward biased which is termed saturation.

saturation V<sub>CE</sub> (sat) h<sub>FE</sub> (sat)

36.2

In the cut-off state, the only current flowing is the result of holeelectron pairs and perhaps some surface leakage current. The transistor offers a very high resistance (near open circuit) and the voltage across the transistor approaches the collector supply voltage.

#### no answer needed

36.3

As the base current is increased, collector current increases and added voltage is dropped across the series resistance in the circuit. As base current increases, the voltage across the transistor

(increases, decreases)

no answer needed



Changes in collector voltage have only a small effect on collector current as long as the collector junction is reverse biased. When the collector junction becomes forward biased, the transistor is said to be in \_\_\_\_\_

#### decreases

36.5

When the collector junction becomes forward biased, collector current is reduced as shown in figure 36. The sharp change occurs at approximately \_ volts,  $V_{CE}$ , when  $I_B = 100 \ \mu \text{amps.}$ 

# saturation

The transistor in the common emitter configuration starts to enter 36.6 saturation when the voltage collector to emitter ( $V_{CE}$ ) is equal to the voltage, base to emitter ( $V_{B\,F}$ ). On the 100  $\mu$ amp base current curve in figure 36,  $V_{BE} = V_{CE} =$ \_\_\_\_\_\_ volts when the transistor enters saturation.

0.3

36.7

The collector to emitter voltage at the point the transistor enters saturation is given the symbol V<sub>CE</sub> (sat). \_\_\_\_\_ is given at a specified value of  $I_{\rm B}$  and  $I_{\rm C}$  in manufacturers specifications.

0.3



Figure 36

36.8 In figure 36,  $V_{CE}$  (sat)  $\approx$  0.3 volts at  $I_B = 100 \ \mu \text{amps}$  and  $I_C = 4 \ \text{ma.}$  When  $I_B = 90 \ \mu \text{amps}$  and  $I_C = 3.5 \ \text{ma.}$ ,  $V_{CE}$  (sat)  $\approx$  \_\_\_\_\_.

V<sub>CE</sub> (sat)

36.9

 $h_{FE}$  (sat) is the current gain of the transistor at saturation.  $h_{FE}$  (sat) =  $\frac{l_{C}$  (sat)}{l\_{B}}. On the 100 µamp base current curve in figure 36,  $h_{FE}$  (sat) = \_\_\_\_\_.

## 0.25V

36.10\*\* The current gain at saturation is given the symbol  $h_{FE}$  (sat). When the collector junction is reverse biased, the transistor in saturation and  $V_{CE}$  is  $\frac{1}{(less, greater)}$  than  $V_{CE}(sat)$ .

40

36.11 END OF SET

is not greater



Figure 36

A transistor in saturation has both the emitter and collector junctions \_\_\_\_\_\_\_biased. The injection of minority carriers into the base from the collector when the transistor enters saturation increases the \_\_\_\_\_\_\_ in the base. This must be removed in order to turn \_\_\_\_\_\_ the transistor.

37.1 Carriers injected into the base recombine or diffuse to the collector. Once injected and until they recombine in the base or move into the collector circuit, they are existing as \_\_\_\_\_\_ carriers in the base.

> forward stored charge off

37.2 Carriers injected into the base from the emitter represent a charge in the base during their diffusion to the collector.

#### minority

37.3 To turn on a transistor, the charge of minority carriers must be established in the base. To turn off a conducting transistor, this stored \_\_\_\_\_ must be removed.

no answer needed

37

37.4 A period of time is required to turn on a non-conducting transistor to establish the \_\_\_\_\_\_ of minority carriers in the \_\_\_\_\_\_ before collector current can reach its final value.

#### charge

37.5 Once the transistor is in full conduction, removal of the stored charge of minority carriers in the base is required to turn it off.

#### charge base

37.6 It takes a period of time to remove the stored charge when turning off a conducting transistor. The greater the magnitude of stored charge, the more \_\_\_\_\_\_ is required to remove it.

no answer needed

37.7 When the transistor is driven into saturation, the collector injects carriers into the base as a result of becoming forward biased. The number of minority carriers in the base is increased and the collector current is decreased.

time

37.8 Until the carriers in the base recombine or move into the collector, they are existing as a stored charge in the base. The extra injected carriers forced into the base in saturation represent an increase in the \_\_\_\_\_\_ in the base.

no answer needed

37.9 A transistor driven into saturation has a larger stored charge in its base than when in an un-saturated condition. The deeper the transistor is driven into \_\_\_\_\_\_, the greater the stored charge.

stored charge

37.10 Since the stored charge represents a supply of minority carriers, the stored charge must be removed before the transistor can be turned

#### saturation

37.11\*\* The collector becoming forward biased as the transistor enters saturation results in an increase in the \_\_\_\_\_\_ in the base of the transistor which must be removed to turn the transistor

off

stored charge off



38

Construct a load line; determine the operating point base current, collector voltage and collector current for the circuit in figure 38. With an applied signal current of 10 µamps peak to peak, what signal current is flowing in the output circuit and what is <u>circuit</u> current gain?

38.1

One extreme of the transistor's operating range is the supply voltage. The load line will intersect the zero collector current line at \_\_\_\_\_\_ volts of collector voltage in figure 38.

### answers on following page

38.2

The second extreme of the transistor's operation is determined by the series resistance in the paths of emitter and collector current. The load line intersects the zero collector voltage line at \_\_\_\_\_ma of collector current in figure 38.

38.3 Operating or quiescent point base current is determined by the base biasing resistor, R<sub>F</sub>. The operating point base current in figure 38 is \_\_\_\_\_\_µamps.

1.8

<sup>9</sup> 



38.4 The operating point base current curve intersects the load line at the operating point. In figure 38-A, operating point collector current is and collector voltage is \_\_\_\_\_\_.

<u>9 Volts</u> = 15 µamps 600K

38.5

h<sub>fe</sub> gives the current gain of the transistor, but disregards the circuit. Making a current gain measurement along the load line gives the current gain of the \_\_\_\_\_\_.

0.74ma 5.4 Volts

38.6 With an input signal current of 10 μamps peak to peak, the base current will vary 5 μamps above and below the operating point. In figure 38-A it varies between \_\_\_\_\_\_ μamps and \_\_\_\_\_\_ μamps of base current.

#### circuit

38.7 If the applied change in base current is assumed to take place <u>along the</u> <u>load line</u>, the change in circuit collector current can be found. In figure 38-A, the change in collector current for an input change of 10 μamps base current is \_\_\_\_\_ ma.

> 10 20



38.8 Dividing the change in collector current by the applied change in base current along the load line gives the circuit current gain . In figure 38-A, circuit current gain is \_\_\_\_\_\_.

0.48 ma

38.9\*\*

Construct a load line; determine the operating point base current, collector current, and collector voltage for the circuit in figure 38-B.

 $\frac{0.48 \text{ ma}}{10 \text{ } \mu \text{ amps}} = 48$ 

38.10 END OF SET

answer on following page



39.1 At room temperature, there are minority carriers present in all parts of the transistor. \_\_\_\_\_\_ bias on the collector junction results in any minority carriers that enter the transition region, crossing the junction.

#### avalanche breakdown acceleration or multiplication

39.2 A high value of reverse bias accelerates the carriers to great speeds. The <u>accelerated</u> carriers strike other atoms in the structure, freeing more carriers which are also \_\_\_\_\_\_ by the high reverse bias.

reverse

39.3 The multiplication of carriers at high values of reverse bias causes the collector to go into a reverse breakdown condition.

#### accelerated



39.4 The multiplication of carriers in the reverse breakdown mode is termed avalanche. Avalanche breakdown occurs at high values of collector voltage.

no answer needed

39.5 Figure 39 shows a collector family of curves in the top photo. The second photo is a collector family of curves for the same transistor, but includes the area around collector \_\_\_\_\_\_

reverse

20

39.6 When the breakdown voltage is reached, collector current increases greatly. For zero  $I_B$  in figure 39, avalanche breakdown occurs at approximately \_\_\_\_\_\_\_\_\_volts of  $V_{CF}$ .

#### avalanche breakdown

39.7 When the breakdown voltage of the collector junction is exceeded, the collector enters a condition termed \_\_\_\_\_\_ or reverse break-down. This is a result of the multiplication of carriers on impact of accelerated carriers.

39.8 Avalanche breakdown in the collector of a transistor is the same as discussed for the basic diode. The orientation of the transistor can effect the voltage point at which breakdown occurs, however, due to the influence of transistor gains.

#### avalanche

39.9 A transistor in avalanche breakdown has \_\_\_\_\_\_\_\_ action (the same, a different) occuring at the collector junction as the basic diode when in avalanche breakdown.

no answer needed

39.10\*\* When the transistor enters \_\_\_\_\_\_ breakdown, the current increases greatly. This is a result of the \_\_\_\_\_\_ of carriers by accelerated carriers striking atoms in the structure.

the same

39.11 END OF SET

avalanche multiplication, etc. 40 The symbol \_\_\_\_\_\_ indicates breakdown voltage, collector to emitter, with the base lead open; the symbol \_\_\_\_\_\_ indicates breakdown voltage, collector to base, with the emitter lead open; and the symbol \_\_\_\_\_\_ indicates breakdown voltage, collector to emitter, with a specified resistance from base to emitter. They are all given at a specified temperature.

40.1 The configuration affects the voltage point at which the transistor starts to break down. The manufacturer lists several breakdown voltages for several \_\_\_\_\_.

<sup>B V</sup>C EO <sup>B V</sup>C BO <sup>B V</sup>C ER

#### configurations

40.3 Without injected carriers from the emitter and the reverse voltage applied directly between collector and base, the breakdown voltage is determined by the characteristics of the collector base junction (and the temperature).

temperature

40.4 The common base configuration finds the situation in frame 40.3, if the emitter lead is open circuited. The breakdown voltage is determined by the point at which the collector diode starts to avalanche.

no answer needed

40.5

The common emitter configuration has the collector supply voltage applied across <u>both</u> junctions when the base lead is open circuited. Although this reverse biases the collector junction, it \_\_\_\_\_\_ biases the emitter junction.



no answer needed

40.6

Voltage applied from collector to emitter with the base lead open circuited will reverse bias one junction and forward bias the other. This will \_\_\_\_\_\_\_\_ the number of minority carriers in the base. (increase, decrease)

forward



# <sup>B V</sup>C EO

BREAKDOWN VOLTAGE, COLLECTOR TO EMITTER, WITH THE BASE LEAD OPEN  $(I_b = 0)$ 



<sup>в V</sup>сво

BREAKDOWN VOLTAGE, COLLECTOR TO BASE, WITH THE EMITTER LEAD OPEN  $(1_e = 0)$ 



FIGURE 40-A

<sup>B∀</sup>CER

BREAKDOWN VOLTAGE, COLLECTOR TO EMITTER, WITH A SPECIFIED VALUE OF RESISTOR BE-TWEEN BASE AND EMITTER 40.7 The action of the emitter junction when the voltage is applied, collector to <u>emitter</u> rather than collector to base, reduces the voltage required to cause the transistor to enter a breakdown condition.

increase

40.8 A transistor in a common base configuration will break down at collector voltage as/than a transistor in a common (a different, the same)

(a different, the same) emitter configuration.

no answer needed

40.9 Figure 40-A shows three possible configurations and the breakdown voltage symbols. BV<sub>CEO</sub> indicates that the breakdown voltage was measured with the \_\_\_\_\_\_ lead open circuited.

a different

40.10 Biasing the transistor to allow zero base lead current, allows the measurement of the breakdown voltage whose symbol is \_\_\_\_\_

base





BREAKDOWN VOLTAGE, COLLECTOR TO EMITTER, WITH THE BASE LEAD OPEN  $(I_b = 0)$ 



в V сво

BREAKDOWN VOLTAGE, COLLECTOR TO BASE, WITH THE EMITTER LEAD OPEN  $(I_e = 0)$ 



<sup>B V</sup> C ER

BREAKDOWN VOLTAGE, COLLECTOR TO EMITTER, WITH A SPECIFIED VALUE OF RESISTOR BE-TWEEN BASE AND EMITTER

FIGURE 40-A

40.11 BV<sub>CBO</sub> is measured with the \_\_\_\_\_\_ lead open. BV<sub>CBO</sub> breakdown occurs between collector and \_\_\_\_\_, as shown in figure 40-A.

# <sup>BV</sup>CE0

40.12

 $^{\rm BV}{
m CEO}$  is aided by the gain of the transistor and occurs at a (lower, higher) voltage than  $^{\rm BV}{
m CBO}$  for the same transistor.

#### emitter base

40.13

BV<sub>CER</sub> is an attempt to specify a breakdown voltage that will be closer to the conditions encountered in an actual circuit. BV<sub>CER</sub> is given with a specified value of resistance between \_\_\_\_\_\_ and \_\_\_\_\_ and \_\_\_\_\_ as shown in figure 40-A.

#### lower

40.14

On a common emitter collector family of curves, the open base lead condition is represented by the \_\_\_\_\_ base current curve.

base emitter



FIGURE 40-B

40.15 On a common emitter collector family of curves, reverse biasing the emitter base junction sufficiently to reduce emitter current to zero is the same as opening the \_\_\_\_\_ lead.

zero

40.16 In figure 40-B (photo 2), the line marked  $I_E = 0$  indicates that sufficient reverse base current is applied to reduce the emitter current to zero. This is the same as opening the \_\_\_\_\_ lead.

#### emitter

40.17 Figure 40-B (photo 1) is a collector family of curves for a common emitter configuration. The sharp increase in current at high values of V<sub>CE</sub> indicates \_\_\_\_\_\_ breakdown is occuring.

emitter

40.18

In figure 40-B (photo 2), reverse biasing current is being applied to reduce emitter current. BV<sub>CBO</sub> is measured on the \_\_\_\_\_\_ emitter current curve.

avalanche


FIGURE 40-B

40.19 In figure 40-B (photo 2), BV<sub>CBO</sub> is measured on the base current curve that is marked I<sub>E</sub> = 0. This curve indicates that sufficient reverse base current has been applied to oppose any minority or leakage current and simulates an open \_\_\_\_\_\_ circuit.

# zero

40.20**	The symbol BV <sub>CEO</sub> indicates	°,
	the symbol BV <sub>CBO</sub> indicates	°,
	the symbol BV <sub>CER</sub> indicates	•
	(Note: Define the symbols above.)	

emitter

40.21 END OF SET

breakdown voltage collector to emitter with the base lead open breakdown voltage collector to base with the emitter lead open breakdown voltage collector to emitter with a specified resistor from base to emitter temperature

- 41 Maximum power handling capabilities of the transistor are limited by the maximum temperature that the junctions can reach without harm, the surrounding air temperature and the total \_\_\_\_\_\_ from junction to surrounding air.
- 41.1 As with the basic diode, the transport of carriers results in carriers changing energy bands and giving off energy in the form of \_\_\_\_\_\_\_\_.

thermal resistance

41.2

The majority of the energy given off at the transistor's junctions is in the form of heat. The more power dissipated at the junction, the more is given off.

heat light

41.3 The power (I x E) dissipated by a junction results in the generation of heat and raises the junction \_\_\_\_\_\_ above that of its surroundings.

heat (energy)

41.4 The junction can reach an operating temperature at which it is harmed if too much power is dissipated. Moving some of the generated heat away from the junction allows \_\_\_\_\_\_ power to be dissipated. (more, less)

temperature

41.5 The collector junction dissipates the greater amount of power of the two junctions in most cases. The <u>smaller</u> amount of heat will be generated at the \_\_\_\_\_\_ junction.

more

41.6 The transistor is normally mounted in a case and this offers opposition to the transfer of \_\_\_\_\_\_ from the junction to the surrounding air.

#### emitter

41.7 The greater the amount of heat that can be moved from the junction to the surrounding air, the more power can be dissipated for the same surrounding air (ambient) temperature. The lower the surrounding air (ambient) temperature, the \_\_\_\_\_\_ power a given transistor can dissipate.

heat

41.8 The difference between the ambient (surrounding air) temperature and the maximum temperature at which the junction can operate, is the allowable rise in junction temperature due to dissipating power.

more

41.9

The opposition offered in the path of heat transfer from the junction to the surrounding air is termed "thermal resistance". The higher the thermal resistance, the  $\frac{1}{(more, less)}$  heat will be transferred.

no answer needed

41.10 The maximum allowable junction temperature (T<sub>JMAX</sub>), the ambient temperature (T<sub>A</sub>), and the opposition offered in the path of heat transfer from the junction to surrounding air which is termed \_\_\_\_\_\_, limits the maximum power dissipation.

less

#### thermal resistance

4

41.12**	Thermal resis	tance,	maximum	 			(T	(), and
				(T <sub>A</sub> )	limit	the	amount of	power
	the transisto	r can d	dissipate					

total

41.13 END OF SET

junction temperature ambient (surrounding air) temperature



THERMAL TO ELECTRICAL ANALOGY FIGURE 42

GATING FRAME - 42

The symbol for total thermal resistance, junction to ambient, is \_\_\_\_\_\_\_. When dealing with a transistor that is not connected thermally to an external heat sink, \_\_\_\_\_\_\_(#) thermal resistances add to give the total and their symbols are \_\_\_\_\_\_ and \_\_\_\_\_. Thermal resistance is expressed in \_\_\_\_\_\_.

42.1 Thermal resistance is given the symbol  $\Theta$ . The subscripts indicate between what two points the opposition to heat transfer exists.  $\Theta_{JA}$  indicates thermal resistance, \_\_\_\_\_\_\_ to ambient (surrounding air).

> $\Theta_{JA}$ two  $\Theta_{JC}$  $\Theta_{CA}$ degrees centigrade per watt (°C/W)

42.2 When the transistor is in a case and depends on radiation of heat to the surrounding air from the case, two thermal resistances add to give total thermal resistance. Thermal resistance, junction to case  $(\Theta_{JC})$ , and thermal resistance, case to ambient  $(\Theta_{CA})$ , add to give \_\_\_\_\_.

#### junction

42.3 Figure 42 shows the transistor and the thermal considerations in electrical terms. Thermal resistance is analogically compared with electrical resistance, power dissipation at the junction with electrical current, and ambient temperature with electrical

total thermal resistance  $(\Theta_{\mathsf{JA}})$ 

42



THERMAL TO ELECTRICAL ANALOGY FIGURE 42 42.4  $\theta_{JC}$  indicates thermal resistance, junction to \_\_\_\_\_, and  $\theta_{CA}$  indicates thermal resistance, case to \_\_\_\_\_.

#### voltage

42.5 The product of thermal resistance total and the power dissipation will give a temperature (voltage in the analogy) that will add to temperature which is also analogically compared to a voltage and this sum gives junction temperature.

> case ambient

42.6 Thermal resistance is expressed in degrees centigrade per watt (°C/W). This indicates the rise in junction temperature with power dissipation at the junction in degrees centigrade per \_\_\_\_\_.

#### ambient

42.7 Connecting the transistor thermally to an external heat sink (such as the chassis) is termed "heat sinking" the transistor. Heat sinking will

(raise, lower) total thermal resistance.

watt

Total thermal resistance (°C/W) times the power dissipation ( $P_d$  in watts) gives the rise in junction temperature ( $\Delta T_J$ ). The rise in junction temperature added to the ambient temperature ( $T_A$ ) gives the operating temperature of the junction ( $T_J$ ).  $P_d = \Theta_{JA} + T_A =$ \_\_\_\_\_\_

#### lower

42.9\*\*

42.8

operating temperature of the junction  $(T_{1})$ 

42.10 END OF SET

junction to case case to ambient junction to ambient watt



INSULATING WASHER	GHER TYPICAL THERMAL RESISTANCE, (Θ <sub>CS</sub> ) IN °C/W	
	DRY	W/SILICON LUBRICANT
NONE	0.2	0.1
TEFLON	1.45	.8
MICA	0.8	0.4
ANODIZED ALUMINUM	0.4	0.35

THERMAL TO ELECTRICAL ANALOGY WHEN USING A SEPARATE HEAT SINK

FIGURE 43

When a heat sink is used to increase power dissipating capabilities, \_\_\_\_\_(#) thermal resistances add to give  $\theta_{JA}$ . Their symbols are \_\_\_\_\_, and \_\_\_\_\_, and \_\_\_\_\_ lubricant will reduce  $\theta_{JA}$ .

43.1

Using a separate heat sink replaces the rather large thermal resistance, case to ambient  $(\Theta_{CA})$ , with two thermal resistances whose sum is much less than  $\Theta_{CA}$ .  $\Theta_{CA}$  has a \_\_\_\_\_\_\_\_\_ value than the thermal resistances that replace it when a heat sink is used.

3 θJC θCS θSA silicone

43.2

Higher power handling transistors generally have the collector connected directly to the case to aid in heat transfer. This, in most cases, requires that the case be insulated electrically from the heat sink. The electrical insulator used should have good \_\_\_\_\_\_ conductivity.

#### larger

43.3 Figure 43 shows a power transistor with an external heat sink and the equivalent thermal considerations in an electrical analogy. Once again power dissipation ( $P_d$ ) is expressed analogically as electrical

heat (thermal)

43



INSULATING WASHER	TYPICAL TH	ermal resistance, (θ <sub>cs</sub> ) in °c/W
	DRY	W/SILICON LUBRICANT
NONE	0.2	0.1
TEFLON	1.45	.8
MICA	0.8	0.4
ANODIZED ALUMINUM	0.4	0.35

THERMAL TO ELECTRICAL ANALOGY WHEN USING A SEPARATE HEAT SINK

FIGURE 43

There is opposition to the transfer of heat from the case to the heat sink. 43.4 This thermal resistance is given the symbol \_\_\_\_\_\_ as shown in figure 43.

current

θ<sub>CS</sub>

43.5

 $\theta_{\rm CS}$  is the thermal resistance, case to heat sink.  $\theta_{\rm SA}$  is thermal resistance, \_\_\_\_\_ to ambient.  $\theta_{JC} + \theta_{CS} + \theta_{SA} = -$ 

43.6

The sum of the three thermal resistances is total thermal resistance when an external heat sink is used. The product of total thermal resistance and the power dissipation gives the rise in junction temperature \_\_\_\_(T<sub>A</sub>). (Each individual thermal resistance above contributing to the temperature rise)

heat sink θ

 $\theta_{CS}$  and  $\theta_{SA}$  replace  $\theta_{CA}$  when an external heat sink is used. Coating the 43.7 insulating washer (between the case and the heat sink) with silicone lubricant will (increase, decrease)  $\Theta_{CS}$  as shown in figure 43.

ambient temperature



INSULATING WASHER	TYPICAL THE	RMAL RESISTANCE, (⊖ <sub>CS</sub> ) IN °C/W
	DRY	W/SILICON LUBRICANT
NONE	0.2	0.1
TEFLON	1.45	.8
MICA	0.8	0.4
ANODIZED ALUMINUM	0.4	0.35

THERMAL TO ELECTRICAL ANALOGY WHEN USING A SEPARATE HEAT SINK

FIGURE 43

43.8 As shown in figure 43, silicone lubricant will reduce  $\Theta_{CS}$  even if no insulating washer is used. Reducing  $\Theta_{CS}$  also reduces \_\_\_\_\_

#### decrease

43.9\*\* The sum of  $\theta_{\rm JC}$ , \_\_\_\_\_\_ and \_\_\_\_\_, is the total thermal resistance when an external heat sink is used. \_\_\_\_\_\_ lubricant reduces the total thermal resistance.

θ

43.10 END OF SET

 $\overline{\Theta}_{CS}$  $\Theta_{SA}$ silicone

GIVEN:

44

 $\begin{array}{l} \Theta_{SA} = 3.2^{\circ}\text{C/watt} \\ \Theta_{JC} = 1.2^{\circ}\text{C/watt} \\ \Theta_{CS} = 0.6^{\circ}\text{C/watt} \\ T_{A} = 50^{\circ}\text{C} \\ T_{J}\text{max} = 150^{\circ}\text{C} \end{array}$ 

The maximum steady state power the transistor can dissipate is \_\_\_\_\_

44.1 The sum of the individual thermal resistances is the total thermal resistance.  $\theta_{JC} + \theta_{CS} + \theta_{SA} = \theta_{JA} = \_$  °C/watt with the values given in frame 44.

## 20 watts

44.2 Given an ambient temperature  $(T_A)$  of 50°C, and a maximum allowable junction temperature  $(T_J max)$  of 150°C, the allowable change in junction temperature due to power dissipation is found by subtracting  $T_A$  from  $T_J max$ .  $T_J max - T_A =$  allowable  $\Delta T_J = \_\_\_°C$ .

5

44.3

The product of power dissipation and total thermal resistance must not exceed the maximum allowable change in junction temperature. Rearranging formula:  $P_d$ max  $\Theta_{JA} = T_J$ max -  $T_A$ 

P<sub>d</sub>(max) = \_\_\_\_?

100

44.4

Since 
$$P_d^{max} = \frac{T_{Jmax} - T_A}{\Theta_{JA}}$$

 $P_d(max)$  for the problem in frame  $44 = \frac{150°C - 50°C}{5°C/watt} = ___?$ 

$$\frac{T_{J} \max - T_{A}}{\Theta_{JA}}$$

44.5

To find the maximum allowable power dissipation for a given ambient temperature, divide the allowable change in junction temperature by the total thermal resistance.  $P_d(max) =$ \_\_\_\_\_

#### 20 watts

END OF SET

44.6\*\*

$$\Theta_{JC} = 2.1 \text{ C/wall}$$

$$\Theta_{CS} = 0.8 \text{ °C/wall}$$

$$\Theta_{SA} = 5.1 \text{ °C/wall}$$

$$T_{A} = 70 \text{ °C}$$

$$T_{J}\text{max} = 150 \text{ °C}$$

$$P_{d}(\text{max}) = \underline{?}$$

$$\frac{T_{J}\text{max} - T_{A}}{\Theta_{JA}}$$

44.7

$$P_{d}(max) = \frac{T_{J}max - T_{A}}{\theta_{JA}} = \frac{150°C - 70°C}{2.1°C/watt + 0.8°C/watt + 5.1°C/watt} = 10 watts$$



COLLECTOR FAMILY OF CURVES WITH A MAXIMUM POWER CURVE - 150 mwatts - 25°C

FIGURE 45

The maximum power curve is constructed by connecting all points of \_\_\_\_\_\_ on the collector family of curves. For maximum safe output power, the load line should be \_\_\_\_\_\_ to the maximum power curve on the collector family of curves. For maximum current and power, the load line also intersects the maximum \_\_\_\_\_\_ point. \_\_\_\_\_ (T\_A) must be specified.

45.1

When maximum power dissipation is given by the manufacturer or calculated using thermal resistance, it can be plotted on the collector family of curves as shown in figure 45. The curve that results connects all points of maximum power dissipation at a given \_\_\_\_\_.

maximum power tangent current temperature

45.2

The maximum power dissipation of the transistor in figure 45 is 150 mwatts at a temperature of 25°C. At a higher temperature, the maximum power dissipation is \_\_\_\_\_\_\_ than this value.

#### temperature

45.3

In figure 45, the area below and to the left of the maximum power curve is the safe operating area at 25°C. The area above and to the right of the maximum power curve is the un-\_\_\_\_\_ area.

less

45



COLLECTOR FAMILY OF CURVES WITH MAXIMUM POWER CURVE AND LOAD LINE FOR MAXIMUM LINEAR POWER

FIGURE 45-A

45.4 A load line that is tangent to the maximum power curve and passes through the <u>linear</u> region of the curves will handle maximum \_\_\_\_\_\_ power.

# safe

45.5

Figure 45-A shows a load line constructed tangent to the maximum power curve for maximum linear power. This load line \_\_\_\_\_\_ allow \_\_\_\_\_\_ (will, will not) maximum possible current swing.

## linear

45.6

To allow maximum current swing along with maximum power, the load line should intersect the maximum rated forward \_\_\_\_\_\_ point and be tangent to the maximum \_\_\_\_\_\_ curve.

will not



COLLECTOR FAMILY OF CURVES WITH MAXIMUM POWER CURVE AND LOAD LINE FOR MAXIMUM POWER WITH MAXIMUM POSSIBLE CURRENT SWING

FIGURE 45-B

> current power

45.8

The load line for maximum current should be constructed from the maximum current point to a point \_\_\_\_\_\_ to the maximum power curve.

## current

tangent

45.10 END OF SET

power maximum current tangent



COLLECTOR FAMILY OF CURVES WITH A MAXIMUM POWER CURVE AND A LOAD LINE FOR MAXIMUM POWER WITH MAXIMUM POSSIBLE VOLTAGE SWING

FIGURE 46

The load line, to insure maximum power and maximum possible voltage swing, should be \_\_\_\_\_\_ to the maximum power curve and intersect the maximum \_\_\_\_\_\_ point on the collector family of curves.

46.1 To insure maximum power, the load line should be tangent to the maximum power curve. To insure maximum possible voltage swing, the load line should also intersect the maximum \_\_\_\_\_ point.

# tangent voltage

46.2 The maximum power curve is constructed by joining together all points on the collector family of curves equal to maximum power. The area to the left and below the maximum power curve is the \_\_\_\_\_ area.

# voltage

46.3 In figure 46, the load line is tangent to the maximum power curve. The maximum voltage of this transistor is 50 volts. The load line is constructed for maximum power and maximum voltage swing.

safe

46

46.4 The load line must not cross the maximum power dissipation curve. It is, therefore, placed \_\_\_\_\_\_ to the maximum power dissipation curve.

voltage

46.5 To insure maximum possible <u>voltage</u> swing, the load line should also intersect the maximum \_\_\_\_\_\_ point.

#### tangent

46.6\*\* The load line for maximum power and voltage swing should be \_\_\_\_\_\_ to the maximum power curve and intersect the maximum \_\_\_\_\_\_ point.

voltage

46.7 END OF SET

tangent voltage

- 47 Only a small amount of power is dissipated when the transistor is at the extremes of its operation. The extremes of the transistor's operation are termed \_\_\_\_\_\_ and \_\_\_\_\_. The most power is dissipated in the ''\_\_\_\_\_'' region between these two points (also known as the transient region).
- 47.1 A transistor in saturation has very little voltage across it, but a relatively large current flowing which results in a <u>small</u> power dissipation.

saturation cut-off active

no answer needed

47.3 At the two extremes of its operation, the transistor dissipates very little power. The power is dissipated between \_\_\_\_\_\_ and \_\_\_\_\_.

power

47.4 The area between saturation and cut-off is termed the active region. The majority of the power is dissipated in the \_\_\_\_\_\_ region.

#### saturation cut-off

47.5 The active region is also termed the transient region. The transistor dissipates the greatest amount of power in the \_\_\_\_\_\_ or \_\_\_\_\_ region.

#### active

47.6\*\* Very little power is dissipated at the extremes of the transistor's operation. The power is dissipated mainly in the \_\_\_\_\_ or \_\_\_\_ region.

active transient

47.7 END OF SET

active transient The transistor, acting as a switch, (may, may not) have its load line cross over the maximum power curve if it has its resting states at the extremes of the transistor's operation (saturation and cut-off) and not in the active region. This will allow the switching of (less, more)

power than if the transistor rests in the active region.

48.1

48

With the transistor operating as a switch in either the on or off condition, it may have its resting states at saturation and cut-off. Very little power is dissipated at \_\_\_\_\_\_ and \_\_\_\_\_.

# may <u>more</u>

48.2

When the transistor is <u>switched</u> from saturation to cut-off or vice-versa, it will make an excursion through the \_\_\_\_\_\_ region.

# saturation cut-off

48.3

Power will be dissipated during the excursion through the active region. The greater the amount of time spent in the active region, the

\_\_\_\_ power will be dissipated.

(more, less)

active or transient



at 25°C  $\begin{cases}
B_{VCE0} = 50V \text{ (maximum voltage)} \\
I_{C}(max) = 20ma \text{ (maximum forward current)}
\end{cases}$ 

TOTAL POSSIBLE POWER SWING = 1,000 mwatts  $I_{C}(max) \times V_{CE}(max) = 20ma \times 50V = 1,000$  mwatts

FIGURE 48

If the transistor does not spend too much time in the active region during its excursion and does not enter the active region too many times per second, the load line can be constructed between the maximum and \_\_\_\_\_ points as shown in figure 48.

more

48.5 Operating the transistor as a switch between saturation and cut-off transistor power dissipation (during the transition) allows (greater, less) than when the transistor has a resting state in the active region.

# current voltage

48.6 Figure 48 shows the construction of a load line for a transistor switch operating between cut-off and . This allows output power than when the transistor rests in the active (greater, less) region.

#### greater

The total possible power excursion in figure 48 is 1,000 mwatts since the 48.7 transistor can make a transition from approximately 50V to 20ma and viceversa. The maximum transistor power dissipation when the transistor rests in the active region is 150 mwatts.

> saturation greater

48.4



at 25°C  $\begin{cases}
B_{VCE0} = 50V \text{ (maximum voltage)} \\
I_{C}(\text{max}) = 20\text{ma (maximum forward current)}
\end{cases}$ 

TOTAL POSSIBLE POWER SWING = 1,000 mwatts  $I_{C}(max) \times V_{CE}(max) = 20ma \times 50V = 1,000 mwatts$ 

FIGURE 48

48.8 If the transistor in figure 48 had a resting state in the active region, the load line \_\_\_\_\_\_ cross over the 150 mwatt curve. (could, could not)

no answer needed

48.9

Operating in the cut-off to saturated switching mode allows greater power dissipation (and as a result, greater output power), as long as the transistor does not spend too much time in the \_\_\_\_\_\_ region.

#### could not

48.10\*\* Operating the transistor as a switch with one of its resting states in the active region \_\_\_\_\_\_\_ allow the load line to cross the (does, does not) maximum steady state power curve. This allows \_\_\_\_\_\_ power dissi-(more, less) pation and output power than the cut-off to saturated mode of operation for the same switching rate.

active or transient

48.11 END OF SET

does not less Operating a transistor in the cut-off to saturated switching mode has the advantage of low resting state power dissipation, but has the disadvantage of limiting \_\_\_\_\_\_ rate because of the larger \_\_\_\_\_\_ \_\_\_\_ in the base as a result of driving the transistor into saturation.

#### repetition stored charge

49.2 The collector becomes forward biased when the transistor enters saturation. The collector injects carriers into the base when it enters \_\_\_\_\_\_ and becomes \_\_\_\_\_\_ biased.

#### forward

49.3 The collector, becoming forward biased and injecting carriers into the base, results in an increase in the number of carriers stored in the base of the transistor. This increase in base stored charge is a result of the transistor entering \_\_\_\_\_\_.

saturation forward

49
49.4 On entering saturation, the stored charge in the base of the transistor is increased. The deeper the transistor is driven into saturation, the greater the \_\_\_\_\_\_ in the base.

#### saturation

49.5 As with the basic diode, the stored charge must be removed before the transistor may be turned off. It takes a period of time to remove the

stored charge

49.6 Since it takes a period of time to remove the stored charge, the total switching time of the transistor is \_\_\_\_\_\_\_ when the \_\_\_\_\_\_\_ (increased, decreased) transistor rests in saturation rather than the active region.

### stored charge

49.7 An increase in total switching time of the transistor will the maximum number of times the transistor can switch (increase, decrease) between its resting states per second.

increased

49.8 The maximum repetition rate of the transistor is the maximum number of times per second that it can switch from one resting state to the other and back again. Maximum repetition rate is reduced when the transistor is driven into \_\_\_\_\_\_.

decrease

49.9 The deeper the transistor is driven into saturation, the lower the maximum \_\_\_\_\_\_.

#### saturation

49.10\*\* The disadvantage of operating in the cut-off to saturated switching mode, is the increase in the \_\_\_\_\_\_ in the base which limits maximum \_\_\_\_\_\_.

repetition rate

49.11 END OF SET

stored charge repetition rate In dealing with a transistor switch, the turn on time (t<sub>on</sub>) is equal to the sum of \_\_\_\_\_\_ and \_\_\_\_\_ and the turn off time (t<sub>off</sub>) is equal to the sum of \_\_\_\_\_\_ and \_\_\_\_\_. There is some current flow in the off state and some voltage across the transistor in the \_\_\_\_\_\_ state.

50.1

50

delay time  $(t_d)$ rise time  $(t_{f})$ storage time  $(t_{s})$ fall time  $(t_{f})$ on

50.2

When the transistor is off, there is some current, due mostly to hole-electron pairs as formed by heat energy. The transistor in its off state will offer a high, but not a/an \_\_\_\_\_ resistance.

none

50.3

When the transistor is on and saturated, there will still be some voltage across the transistor which is given the symbol  $V_{CE(sat)}$ . In the on condition, the transistor will not be a/an \_\_\_\_\_\_ circuit.

## infinite



FIGURE 50

50.4 When the transistor is turned on, it will take a period of time for the stored charge to be established and for the recombination and diffusion to reach an equilibrium rate. In other words, it will take a period of time for the injected carriers to move across the base to the collector. When a change is instigated at the emitter junction, there is some \_\_\_\_\_ before the change occurs in the collector.

zero resistance (short)

50.5

Figure 50 shows a transistor in a circuit to check its switching characteristics. The time between the instigation of the input change and the point that collector current has changed, 10% of its total excursion, is termed \_\_\_\_\_ time (t<sub>d</sub>).

time (delay)

Delay time  $(t_d)$  is the time it takes to move carriers into the \_ 50.6 to establish the stored charge of \_\_\_\_\_\_ carriers.

# delay

In figure 50, the time between the points on the leading edge of the 50.7 waveform where collector current has changed from 10% to 90% of its total excursion is termed \_\_\_\_\_\_time.

> base minority





FIGURE 50

50.8 Rise time is determined by the charge control time constant in the base, governed by minority carrier lifetime. The sum of delay time  $(t_d)$  and rise time  $(t_r)$  is the transistor's \_\_\_\_\_\_ time  $(t_{on})$ .

rise

50.9

In figure 50, the time between the fall of the input pulse and the point that collector current falls to 90% of its maximum value is termed time  $(t_s)$ .

turn on

50.10 Storage time is increased when the forward biased collector injects carriers into the base when the transistor enters \_\_\_\_\_\_.

storage

50.11 Holding the transistor out of saturation will reduce \_\_\_\_\_\_ time.

saturation



FIGURE 50

50.12 The time between 90% and 10% on the falling portion of the collector current waveform in figure 50 is termed \_\_\_\_\_\_ time  $(t_f)$ .

storage (switching)

50.13 The sum of storage time  $(t_s)$  and fall time  $(t_f)$  gives the transistors \_\_\_\_\_\_ time  $(t_{off})$ .

fall

50.14 Turn off time  $(t_{off}) = storage time (t_s) + fall time (t_f) and turn on time <math>(t_{on}) = delay time (t_d) + rise time (t_r)$ .

turn off

50.15\*\*

 $t_s + t_f =$  and  $t_d + t_r =$ 

The transistor is less than an ideal switch as there is some \_\_\_\_\_\_ in the off state and some \_\_\_\_\_\_ across the transistor in the on state.

storage time  $(t_s)$ 

50.16 END OF SET

turn off time (t<sub>off</sub>) turn on time (t<sub>on</sub>) current voltage

51 The switching times of fast transistors may be checked using the Tektronix Type 290 Transistor Switching Time Tester or the Type 292 Semiconductor Tester in conjunction with a sampling system. The \_\_\_\_\_\_ checks the transistor in a specific configuration while the \_\_\_\_\_\_ allows the circuit to be inserted with the transistor.

51.1 The manual switch used in the previous set is not fast enough to give accurate readings of switching times. In practice, electrically driven switches are used.

290 sampling 567

51.2 The 290 Switching Time Tester provides a circuit, bias voltages, and input and output jacks along with facilities to drive the input of the transistor. The output is monitored with a sampling oscilloscope. Both the input driving signal and the transistor's output may be monitored.

no answer needed

51.3 The input pulse and the transistor's output can be monitored and measurements taken of switching times exactly as in set 50 when the 290 and a sampling system are used. These measurements are similar to the diode switching time measurements made in volume 2 of this series.



FIGURE 51

51.4 Figure 51 shows the 290 being used with the Tektronix Type 661 sampling oscilloscope. It should be remembered that the risetime considerations, when making measurements as discussed in volume 2, are valid for these measurements as well.

no answer needed

51.5

The dual trace ability allows the observance of the input and output pulse, simultaneously. The risetime measurement in figure 51 is approximately nsec.

no answer needed

51.6 The storage time in figure 51 is approximately \_\_\_\_\_\_ nsec.

11

51.7

The 290 Transistor Switching Time Tester can be used in conjunction with a sampling system and a pulse generator to make the measurements described in set 50. This allows measurement of fractional nanosecond switching times.



TEKTRONIX TYPE 292 SEMICONDUCTOR TESTER AND ACCESSORIES



FIGURE 51-A

51.8 The Type 292 Semiconductor Tester (shown in figure 51-A) allows the circuit for the transistor to be selected and built while maintaining the transistor in an optimum measurement environment.

no answer needed

51.9 The Type 292 does not limit the measurements to a specified circuit, but allows the measurement circuit to be fabricated on special test fixtures provided.

no answer needed

51.10 The Type 292 does not limit the switching time measurements to a specified

no answer needed

51.11 The Type 292 (shown in figure 51-A) can be used for diode measurements as well as \_\_\_\_\_\_ measurements.

circuit



TEKTRONIX TYPE S-3401 SYSTEM

FIGURE 51-B

51.12 For transistor manufacturers, the system of measurement becomes more complex. A great number of measurements must be made in a short period of time. Figure 51-B shows a programmed measurement system for transistors (and other semiconductor devices).

#### transistor

51.13 The system in figure 51-B is the Tektronix S-3401 system. This is a programable, computer type system that can be used for rapid, sequential measurements of fast transistors. (Also, other semiconductor devices and integrated circuits.)

no answer needed

51.14\*\* The Type \_\_\_\_\_ Transistor Switching Time Tester or the Type \_\_\_\_\_ Semiconductor Tester may be used in conjunction with a pulse generator and sampling system to check fast transistor switching times.

no answer needed

51.15 END OF SET

290 292

- A \_\_\_\_\_\_ capacitor will reduce the time involved in establishing the base charge when turning on a transistor and removing the base charge when turning off a conducting transistor. The optimum value of speed-up capacitor may be found by dividing the transistor's stored charge by the value of \_\_\_\_\_\_ on the speed-up capacitor.

## speed-up voltage

52.2 A capacitor connected across the resistance in the input circuit of a transistor will <u>speed up</u> the establishment of the base charge when turning the transistor on and <u>speed up</u> the removal of the stored charge when turning the conducting transistor off.

stored charge base charge

52.3 The output resistance of the driving source must be low for best effect of the added capacitor. Since the capacitor <u>speeds</u> up the switching time, it is referred to as a \_\_\_\_\_\_ capacitor.

no answer needed

52





FIGURE 52

52.4 Figure 52 shows the added speed-up capacitor and its effect on the output waveform. The optimum value of speed-up capacitor to accomplish this will have a charge equal to the transistor's \_\_\_\_\_\_ charge.

### speed-up

52.5 The charge on the speed-up capacitor speeds up the establishment and removal of the stored charge when the speed-up capacitor is of optimum value. While observing the transistor's switching characteristics on the 290 Switching Time Tester or the 292 Semiconductor Tester, the speed-up capacitor can be adjusted for minimum switching \_\_\_\_\_.

stored or base

52.6 Letting  $Q_s$  indicate total transistor stored charge, and  $Q_c$  indicate the charge on the speed-up capacitor,  $Q_c$  should be approximately equal to \_\_\_\_\_\_ for optimum speed-up action.

times

Q<sub>s</sub>

52.7

 $Q_c \cong Q_s$  for optimum speed-up operation.

 $\rm Q_{c}$  = CE where C is the capacity of the speed-up capacitor and E is the voltage across the capacitor.  $\rm Q_{c}$  =  $\rm Q_{s}$  = CE

$$\frac{Q_s}{F} = -$$

52.8 The optimum value of speed-up capacitor is found by dividing the transistor's stored charge by the voltage on the speed-up capacitor. When this value of capacitor is used, the charge on the capacitor will equal the transistor's \_\_\_\_\_\_\_.

C (value of speed-up capacitors)

52.9\*\* A speed-up capacitor across the input driving resistance will reduce times. The optimum value of speed-up capacitor is equal to the transistor's \_\_\_\_\_\_ divided by the voltage on the speed-up capacitor.

stored charge

52.10 END OF SET

switching stored charge  $(Q_s)$ 

An obvious method of reducing saturated mode storage time is to keep the transistor out of saturation. This is termed \_\_\_\_\_\_\_ switching and the transistor operates between cut-off and the \_\_\_\_\_\_ region. Current mode switching allows \_\_\_\_\_\_ transistor power dissipation (more, less) than saturated mode switching.

53.1

Not allowing the collector to become forward biased will prevent the collector from injecting carriers into the base. The collector voltage must be held  $\frac{1}{(less, greater)}$  than  $V_{CE}(sat)$  to accomplish this.

current mode active less

53.2 Zener or avalanche diodes are sometimes used to catch the collector voltage and hold it above  $V_{CE}(sat)$ . This prevents the transistor from entering

greater

53.3

When the transistor is held out of saturation, it switches from cut-off to a high <u>current</u> point and this is termed \_\_\_\_\_\_ mode switching.

saturation

53



CURRENT MODE SWITCHING CUT-OFF TO ACTIVE REGION

FIGURE 53

53.4 Current mode switching has the transistor switching between cut-off and the \_\_\_\_\_\_ region. This switching mode allows \_\_\_\_\_\_ tran-(less, more) sistor power dissipation during switching than the off to saturated switching mode.

current

53.5

Figure 53 shows the load line for current mode switching. The collector voltage is caught in the active region and not allowed to go below

active less

53.6

In figure 53, the <u>on</u> resting state is held below the maximum power curve. A disadvantage of current mode switching is the reduction in \_\_\_\_\_\_ dissipation capabilities with reference to the cut-off to \_\_\_\_\_\_ switching mode.

V<sub>CE</sub> (sat)

53.7\*\* Transistor storage time can be reduced by holding the transistor out of \_\_\_\_\_\_. This switching mode is termed \_\_\_\_\_\_ mode switching. This mode can allow the transistor to dissipate \_\_\_\_\_\_ power during switching than the saturated mode.

> power saturated

# 53.8 END OF SET

saturation current less Current mode switching offers \_\_\_\_\_\_\_ speed, \_\_\_\_\_\_ noise, (higher, lower) (higher, lower) critical transistor requirements and \_\_\_\_\_\_\_ complicated (more, less) d-c design problems than the saturated switching mode.

54.1 Current mode switching reduces the storage time which reduces total switching time over the saturated switching mode. Current mode switching offers a \_\_\_\_\_\_ maximum repetition rate than the saturated mode. (higher, lower)

> high low less more

54

54.2 When the transistor enters saturation, both the emitter and collector inject carriers into the base resulting in an increase in the noise level. The current mode switch does not enter saturation and generates

(more, less) noise than the saturated mode.

## higher

54.3 V<sub>CE</sub>(sat), h<sub>FE</sub>(sat), breakdown voltage from emitter to base, thermal and leakage currents are less critical with the current mode, since the transistor does not enter \_\_\_\_\_.

less

54.4 The transistor must remain out of saturation under worst case conditions, using the current switching mode. This increases the complexity of the d-c design considerations over the \_\_\_\_\_ mode.

#### saturation

54.5

Since the current mode switch has a resting state in the \_\_\_\_\_\_ region, care must be taken that maximum power is not exceeded.

#### saturated

54.6\*\*

The advantages of current mode switching over saturated mode switching are switching speed, \_\_\_\_\_\_ critical transistor para-(faster, slower) (less, more) meters. The disadvantages are \_\_\_\_\_\_ resting state power dissipation and \_\_\_\_\_\_ complicated d-c design considerations than the off (less, more) to saturated mode.

active

54.7

END OF SET

faster less less higher more



- The avalanche switching mode has the transistor switching between cut-off and a point in the \_\_\_\_\_\_ region. The switching time can be on the order of fractional \_\_\_\_\_\_\_ seconds. Avalanche switching can be triggered in the base or \_\_\_\_\_ circuit.
- One resting state of an avalanche switching transistor is just out of 55.1 avalanche breakdown and the other is in the \_\_\_\_\_\_ breakdown region.

avalanche breakdown nano collector

55.2

The action of causing the transistor to switch states is termed triggering and the applied energy to cause switching is termed a \_\_\_\_\_.

## avalanche

Figure 55 shows transistors biased for avalanche switching. V is very 55.3 near the \_\_\_\_\_\_ voltage point.

#### trigger

55



55.4 The transistors in figure 55 must operate on the load line. The transistor can operate only at points A, B and C with the load line and value of shown.

avalanche breakdown

55.5 Consider the transistor in circuit X in figure 55 as operating at point A on the curve. Forcing more current with  $V_{CC}$  constant will cause the operating point to shift to B and then to \_\_\_\_\_\_.

V<sub>CC</sub>

55.6

С

55.7 A trigger is needed to return the transistor to point A. The avalanche switching mode shown in figure 55 is bi-stable, meaning the transistor has (#) stable states.



55.8 The circuit Y in figure 55 has the trigger applied to the collector. The trigger will increase or decrease the collector voltage depending on its polarity.

two

55.9 With circuit Y operating at point A in figure 55, a positive going trigger will increase the applied collector voltage and the <u>load line</u> will move to point D. At that instant, the only point on the load line that the transistor can exist is at point \_\_\_\_\_.

no answer needed

55.10 Once triggered to point E in figure 55, the transistor in circuit Y will rest at point \_\_\_\_\_\_ when the trigger is no longer present.

Е

С

55.11 In order to move back to point A from point C, the collector must be triggered in the opposite polarity. Circuit Y in figure 55 is \_\_\_\_\_\_\_ stable and switches between resting points \_\_\_\_\_\_ and \_\_\_\_\_. 55.12 Avalanche mode switching can be accomplished in fractional nanoseconds, allowing very fast rising outputs. The collector supply voltage is near the \_\_\_\_\_\_ voltage.

> bi A C

55.13\*\* The two resting states of an avalanche switching transistor are just below the \_\_\_\_\_\_ point and in the \_\_\_\_\_\_ \_\_\_\_ region. Fractional \_\_\_\_\_\_second risetimes are possible with this switching mode.

avalanche breakdown

55.14 END OF SET

avalanche breakdown avalanche breakdown nano The main high frequency limiting factors in the transistor are collector and emitter junction \_\_\_\_\_\_, base \_\_\_\_\_\_ time, and the spreading out of the carriers in the \_\_\_\_\_\_.

56.1 Carriers injected from the emitter into the base are existing as minority carriers in the base. They must diffuse the entire \_\_\_\_\_\_ thickness to reach the collector.

capacitance transit base

56.2 As the applied frequency is increased, a frequency will be reached where the time involved in the <u>transit</u> of the carriers across the base causes phase shift and loss of gain. The greater the <u>transit</u> time, the

(lower, higher) the frequency at which phase shift and loss of gain occur.

base

56.3 There is capacitance across the collector and emitter junctions. This capacitance will change with the amount of current and the voltage across the junction. This capacitance shunts the junction and, as frequency is increased, will have \_\_\_\_\_\_\_ effect.

lower

56

56.4 The collector junction is reverse biased and the emitter junction is forward biased in amplifier configurations. The \_\_\_\_\_\_ junction will have the highest resistance.

a greater

56.5 The effects of collector junction capacitance will occur at a lower frequency than the effects of emitter junction capacitance as collector junction capacitance is shunting a \_\_\_\_\_\_ resistance.

collector

higher

56.7 The diagram shows a typical path a current carrier might take in its transit through the base. Several carriers entering the base at the same time could well arrive at the collector at \_\_\_\_\_\_ times.


56.8 The wider the base, the \_\_\_\_\_ opportunity the carriers will have (more, less) to spread out and arrive at the collector at \_\_\_\_\_\_ times.

different

56.9\*\* High frequency operation in transistors is limited mainly by the \_\_\_\_\_\_ at the collector and emitter junctions, the time of \_\_\_\_\_\_ in the base, and the \_\_\_\_\_ out of the carriers in the base.

> more different

56.10 END OF SET

capacity transit spreading

is the symbol for the cut-off frequency of the transistor in a common base configuration. This indicates the frequency at which has fallen to 0.707 of its low frequency value.

57.1 h<sub>fb</sub> is the small signal, a.c. current gain of the transistor in a common base configuration. Due to factors already discussed, h<sub>fb</sub> will decrease with an increase in frequency.

f<sub>hfb or f<sub>a</sub> h<sub>fb</sub>(alpha)</sub>

57.2 A frequency will be reached at which  $h_{fb}$  has decreased to 0.707 of its low frequency value. The <u>frequency</u> at which this occurs is given the symbol  $f_{hfb}$  or  $f_{\alpha_b}$ . This is usable with the common \_\_\_\_\_\_ configuration. In the diagram,  $h_{fb}$  is plotted vertically and frequency is plotted on the base line. f is given the symbol \_\_\_\_

and indicates the common base cut-off frequency of the transistor.



 $f_{hfb}$  or  $f_{lpha_b}$  indicates the \_\_\_\_\_ at which  $h_{fb}$  falls to \_\_\_\_ 57.4\*\* of its low frequency value. This is the cut-off frequency of the transistor in a common \_\_\_\_\_ configuration.

> horizontally f<sub>hfb</sub> or  $f_{\alpha}_{b}$

END OF SET 57.5

> frequency 0.707 base

is the symbol for the cut-off frequency of the transistor in a common emitter configuration. This indicates the frequency at which has diminished to 0.707 of its low frequency value. For a given transistor, this frequency will be much \_\_\_\_\_\_ than f hfb.

58.1 h<sub>fe</sub>, the small signal, a-c current gain of the transistor in a common emitter configuration will decrease at the higher frequencies. The cutoff point is considered to be the point at which h<sub>fe</sub> has decreased to \_\_\_\_\_\_ of its low frequency value.

> f<sub>hfe</sub> or f<sub>αe</sub> h<sub>fe</sub> lower

58.2 The frequency at which  $h_{fe}$  has decreased to 0.707 of its low frequency value is given the symbol  $f_{hfe}$  or  $f_{\alpha}e$ . This frequency is usable with the common \_\_\_\_\_\_ configuration.

58

0.707

In the diagram, h is plotted vertically and frequency is plotted horizontally. f<sub>1</sub> is given the symbol \_\_\_\_\_\_ and indicates the common emitter cut-off frequency of the transistor.



emitter

The relationship of  $f_{hfe}$  and  $f_{hfb}$  is expressed as  $f_{hfe} = f_{hfb} (1 + h_{fb})$ . 58.4 Consider a transistor with an  $h_{fb}$  = -0.98 and an  $h_{fe}$  of 49. If the transistor has an  $f_{hfb}$  of 10 megacycles,  $h_{fe}$  will fall to 0.707 of its low frequency value at \_\_\_\_\_ cycles.

> $f_{hfe} = f_{hfb} (1 + hfb)$ (NOTE: hfb is <u>always</u> a <u>negative</u> quantity)

 $f_{hfe}$  or  $f_{\alpha}_{e}$ 

58.5

 $f_{\rm hfe}$  will occur at a much lower frequency than  $f_{\rm hfb}$  . For a given transistor, the common emitter configuration will have its gain reduced to 0.707 of its low frequency value at a \_\_\_\_\_\_ frequency than the \_\_\_\_\_\_ (higher, lower) common base configuration.

 $f_{hfe} = f_{hfb} (1 + h_{fb}) = 10^7 1 + (-0.98) = 10^7 \times 0.02 = 200K$ 

58.3

58.6 Consider a transistor with an  $h_{fb} = -0.96$  and an  $f_{hfe} = 500$ K cycles.

f<sub>hfb</sub> = \_\_\_\_\_

(NOTE: h<sub>fb</sub> is <u>always</u> a negative quantity)

lower

58.7\*\* f<sub>hfe</sub> is the symbol for the transistor's cut-off frequency in a common \_\_\_\_\_\_\_ configuration. This is the frequency at which \_\_\_\_\_\_\_ has fallen to \_\_\_\_\_\_ of its low frequency value. For given transistor, f<sub>hfb</sub> will be a \_\_\_\_\_\_ frequency than f<sub>hfe</sub>.

$$f_{hfb} = \frac{f_{hfe}}{1+h_{fb}} = \frac{500 \times 10^3}{0.04} = 12.5 \text{ megacycles}$$

58.8 END OF SET

emitter <sup>h</sup>fe 0.707 higher  $C_{ob}$  is the symbol given the output capacitance of a transistor in a common orientation and  $C_{oe}$  is the symbol given the output capacitance of a transistor in a common \_\_\_\_\_\_ orientation. They are related as shown by the formula  $C_{ob} =$ \_\_\_\_\_.

59.1 In the symbol C<sub>ob</sub>, the C indicates capacitance, the o indicates output, and the \_\_\_\_\_\_ indicates common base.

base emitter C (l+h<sub>fb</sub>)

b

59.2 In the symbol C , the C indicates capacitance, the o indicates output, and the e indicates common \_\_\_\_\_\_.

59

The relationship between  $C_{ob}$  and  $C_{oe}$  is expressed by the formula 59.3  $C_{ob} = C_{oe} (1+h_{fb})$ . If  $h_{fb} = -0.98$  and  $C_{oe} = 200$  picofarads, C<sub>ob</sub> = \_\_\_\_ (Note: h<sub>fb</sub> is always a <u>negative</u> quantity.)

#### emitter

C will be much larger than C for a given transistor and set of 59.4 conditions. It has already been shown that the common \_\_\_\_ configuration current gain will fall off to 0.707 of its low frequency value at a lower frequency than the common \_\_\_\_\_\_ configuration.

 $C_{ob} = 200 \text{pf} (1-0.98) = 200 \text{pf} \times 0.02 = 4 \text{pf}$ 

 $C_{ob} = C_{oe} (1+h_{fb})$ 59.5  $C_{ob} = 9pf$ (Note: h<sub>fb</sub> is always a <u>negative</u> quantity.)  $h_{fb} = -0.97$ C\_\_\_\_\_

> emitter base

The output capacitance of the common emitter configuration has the symbol 59.6\*\* \_\_\_\_\_ and, the output capacitance of the common base configuration has the symbol \_\_\_\_\_\_. Their relationship is expressed by the formula C<sub>ob</sub> = \_\_\_\_\_

 $C_{oe} = \frac{C_{ob}}{1 + h_{fb}} = \frac{9pf}{0.03} = 300pf$ 

59.7 END OF SET

C<sub>oe</sub> C<sub>ob</sub> C<sub>oe</sub> (l+h<sub>fb</sub>)

High frequency construction calls for a \_\_\_\_\_ but uniform base width. The narrower the base, the less the \_\_\_\_\_ time and the less time the carriers have to \_\_\_\_\_ out in the base.

60.1 The narrower the base thickness between the emitter and the collector, the less the transit time for a given minority carrier lifetime. Making the base very narrow increases the frequency at which \_\_\_\_\_\_ shift becomes a problem.

# narrow transit spread

60

60.2 The thin base should also have a uniform thickness. The transistor in the diagram has high frequency problems built in, since it takes some of the carriers longer than others to move through the base.



phase

60.3 Making the base narrow reduces the time the carriers spend in the base. The carriers will spread out less in a \_\_\_\_\_ base with a short transit time.

no answer needed

narrow, thin, etc.

60.5 High frequency transistors will have a different structure than low frequency or general purpose types. The desired characteristics will govern the \_\_\_\_\_\_ of the transistor.

#### frequency

60.6\*\* High frequency operation dictates a narrow \_\_\_\_\_ with uniform width. This reduces \_\_\_\_\_ time and the spreading out of the carriers in the \_\_\_\_\_.

structure, construction, etc.

60.7 END OF SET

base transit base

4

\_

1

A narrow, uniform width base is the aim in construction of high frequency transistors. The rate grown transistor has limited high frequency characteristics. The alloy type transistor gives a/an (increase, decrease) in f<sub>hfb</sub> over the rate grown. Typical f<sub>hfb</sub> for the alloy transistor is \_\_\_\_\_\_ megacycles.

## increase 1 to 10

62.2 Changing the rate at which the crystal is grown is one method of forming the N and P type regions. Different amounts of dopent impurities enter the crystal when the growing \_\_\_\_\_\_ is changed.

grown

62.3 The rate grown crystal is cut up and makes a number of transistors. Changing the \_\_\_\_\_\_ of growing forms the N and P regions as shown in the cross section in figure 62.

62

62.4 The base could be made thinner in the rate grown process, but the problem is both in getting a uniform width and attaching a wire to the base. The base should be thinner than the \_\_\_\_\_\_ that must be attached.

rate

62.5 The alloy transistor is constructed by alloying two dots of material to the sides of a very thin crystal wafer. The dots should give an impurity concentration \_\_\_\_\_\_ the thin wafer. (opposite of, same as)

wire, lead, etc.

62.6 Figure 62 shows a cross section of the alloy transistor. The dots become the emitter and collector contacts and the crystal wafer becomes the

opposite of

62.7 The alloying process makes possible a much thinner base between the emitter and collector with the ability to connect a wire to the crystal wafer for an electrical connection to the \_\_\_\_\_\_.

base

# FIGURE 62





RATE GROWN



62.8 It is difficult to gain uniformity if the base is made too thin in the alloy transistor. Typical  $f_{hfb}$  for the alloy transistor is from 1 to 10 megacycles. This is an increase in  $f_{hfb}$  over the \_\_\_\_\_ \_\_\_\_\_ transistor.

base

62.9\*\*

The rate grown transistor is rugged and useful at the (lower, higher)frequencies. The alloy type gives a/an (lower, higher) in f<sub>hfb</sub> with (increase, decrease) in f<sub>hfb</sub> with respect to the rate grown type. Typical f<sub>hfb</sub> for the alloy type is to \_\_\_\_\_\_ to \_\_\_\_\_ megacycles.

rate grown

62.10 END OF SET

lower increase l 10

# FIGURE 62





RATE GROWN



The micro-alloy is a variation of the \_\_\_\_\_\_ type transistor. To obtain a very thin, uniform base, the center of the wafer is etched very thin before the dots are applied and \_\_\_\_\_\_. This gives the characteristics of a/an \_\_\_\_\_\_ transistor with a thinner base. An increase of  $f_{hfb}$  to \_\_\_\_\_\_ megacycles is typical. A further improvement in  $f_{hfb}$  to \_\_\_\_\_\_ megacycles can be obtained with the micro-alloy diffused. This transistor gives the effect of a built-in electric \_\_\_\_\_\_ in the base. The micro-alloy diffused is also called a drift \_\_\_\_\_\_ transistor.

63.1 In order to get a thinner base and yet not make the device too fragile, the center of the wafer is etched very thin. Etching is the process of concentrating a stream of acid on the two sides and removing some of the material. The outer edges, not being etched, gives the device \_\_\_\_\_

> alloy alloyed alloy 40 200 field field

63.2

The dots are applied to the thin portion of the wafer and when alloyed, give a very thin base. The dots should give an impurity concentration as/to the etched wafer as shown in figure 63. (the same, opposite)

strength, rigidity, etc.

63.3 The micro-alloy gives the characteristics of an alloy transistor with a much thinner \_\_\_\_\_\_. An increase in f<sub>hfb</sub> to 40 megacycles is typical. This is \_\_\_\_\_\_ than the alloy transistor. (higher, lower)

### opposite

63.4

A further variation of the alloy is the micro-alloy diffused or drift field transistor. In this type, the dopents are diffused into the wafer. Diffusion doping is the process of heating the wafer while surrounding it with the impurities in the form of a gas. The impurities \_\_\_\_\_\_\_ into the wafer during the process.

### base higher

63.5 The diffused wafer is then etched, predominately on the collector side. This places the heavier doped portion of the base nearest the emitter when the dots are applied and alloyed. The doping will appear to be graduated heavy to light from \_\_\_\_\_\_ to \_\_\_\_\_.

## diffuse, spread, etc.

63.6 The graduated doping in the base gives the effect of an electric accelerating field in the base. The diffusing carriers will be accelerated reducing both \_\_\_\_\_\_ time and the amount that the carriers \_\_\_\_\_\_ out in the base.

> emitter collector



MICRO-ALLOY



MICRO-ALLOY DIFFUSED

FIGURE 63

63.7 The effective electric field in the micro-alloy diffused base increases the frequency limits. An extension of f<sub>hfb</sub> to 200 megacycles can be obtained with this construction. Another name commonly used for the microalloy diffused is "drift field" transistor.

## transit spread

63.8 The micro-alloy diffused or \_\_\_\_\_\_ transistor has an effective accelerating electric \_\_\_\_\_ built into the base.

no answer needed

63.9 Figure 63 shows the cross section of the drift field transistor. Base doping is heaviest near the \_\_\_\_\_.

# drift field field

63.10\*\* The wafer is etched very thin before the dots are placed and alloyed to form a \_\_\_\_\_\_ transistor. This gives the characteristics of an alloy transistor with an extension of f<sub>hfb</sub> to \_\_\_\_\_ megacycles. The micro-alloy diffused gives an extension of f<sub>hfb</sub> to \_\_\_\_\_ megacycles by graduated doping in the base. It is also called a \_\_\_\_\_\_ transistor.

#### emitter



MICRO-ALLOY



MICRO-ALLOY DIFFUSED

FIGURE 63

micro-alloy 40 200 drift field



MICRO-ALLOY



MICRO-ALLOY DIFFUSED

FIGURE 63

The aim in construction of the mesa transistor is a very narrow base, low collector junction \_\_\_\_\_\_, while maintaining the collector large to dissipate \_\_\_\_\_\_. The epitaxial mesa has an epitaxial layer that makes up the flat topped peak. The epitaxial layer allows high \_\_\_\_\_\_, while the collector is a low resistance material for a low \_\_\_\_\_\_.

64.1

64

The mesa construction starts with a thin layer of dopent being diffused into a basic wafer. The diffusing dopent is opposite to the dopent in the basic wafer. The thin diffused layer and the basic wafer will form

capacitance heat, (power) <sup>B</sup>VCBO V<sub>CE</sub>(sat)

а\_\_\_\_

64.2 The thin diffused layer becomes the base. A non-rectifying contact is connected to the layer for electrical connection. The basic pellet should be doped \_\_\_\_\_\_ than the diffused layer.

The emitter is alloyed into the base (or an aluminum stripe is used) to form the emitter. The alloyed emitter (or the aluminum stripe) and the diffused layer will form the second \_\_\_\_\_

## heavier

64.4

The top of the wafer is etched away except that portion containing the base lead and the emitter. This leaves a flat topped peak or \_\_\_\_ as shown in figure 64.

## junction

The area around the collector junction is etched away to reduce collector 64.5 junction capacitance, while leaving the rest of the wafer to dissipate the generated by power dissipation. Etching away part of the junction effectively reduces the area of the plates of the \_\_\_\_\_ at the junctions.

mesa

The mesa has an increase in  $\mathsf{f}_{\mathsf{hfb}}$  into the hundreds of megacycles. The 64.6 low resistance of the collector allows a low value of  ${\rm V}_{\rm C\,E}({\rm sat})$  . The low resistance collector results in a low value of collector to base breakdown voltage, \_\_\_\_(symbol).

capacitance

64.3



MESA

BASE CONTACT EM I TT ER EPITAXIAL LAYER (HIGH RESISTIVITY) DIFFUSED BASE COLLECTOR (ORIGINAL PELLET, LOW

RESISTIVITY MATERIAL)

EPITAXIAL MESA

FIGURE 64

64.7

An epitaxial layer refers to the process of passing a gas over a structure until the gas has deposited a layer of solidified material on top of the original structure. The epitaxial mesa utilizes an \_\_\_\_\_ layer.

# <sup>в V</sup>сво

64.8

The epitaxial mesa has the same characteristics as the mesa with the added advantage of a higher value of BV<sub>CBO</sub>. The \_\_\_\_\_ layer makes possible the higher breakdown voltage capability.

# epitaxial

64.9

The epitaxial mesa is constructed by first depositing a high resistivity epitaxial layer on a basic low resistant crystal pellet. The base is diffused into the epitaxial layer and the rest of the construction is the same as the \_\_\_\_\_\_\_.

# epitaxial

64.10 The diffused collector ju heat. The <u>b</u>

The diffused base and the remainder of the epitaxial layer form the collector junction. The rest of the pellet or wafer serves to dissipate heat. The <u>high</u> resistance epitaxial layer at the collection junction allows a higher value of collector breakdown voltage.

mesa



MESA

BASE CONTACT EM I TT ER EPITAXIAL LAYER (HIGH RESISTIVITY) DIFFUSED BASE -COLLECTOR (ORIGINAL PELLET, LOW RESISTIVITY MATERIAL)

EPITAXIAL MESA

FIGURE 64

The planar transistor does not need the flat topped peak of the mesa, as \_\_\_\_\_\_ is used to mask the basic pellet and allow controlled diffusion. Selected portions for the emitter and base are cut through the protection to allow \_\_\_\_\_\_. The junctions are protected immediately on being formed and are said to be surface \_\_\_\_\_\_.

65.1 The planar transistor is made by diffusing both the emitter and base into the basic crystal wafer. The planar is a double \_\_\_\_\_\_ transistor.

silicon dioxide diffusion passivated

65.2 A layer of silicon dioxide is grown on the surface of the basic crystal wafer. Diffusion cannot occur through the \_\_\_\_\_\_

## diffused

65.3 Holes can be cut through the silicon dioxide and allow well controlled diffusion of the emitter and base as shown in figure 65. The original pellet becomes the \_\_\_\_\_.

silicon dioxide

65



MESA



EPITAXIAL MESA

FIGURE 64

65.4 The silicon dioxide masks the remainder of the collector area and keeps the junction confined to the selected area. This maintains low junction capacitance and the mesa is not necessary. The \_\_\_\_\_\_ mask does much the same job as etching the mesa.

#### collector

65.5 Since the silicon dioxide is replaced immediately over the junction after it is formed, the junction is protected from the surrounding environment and is said to be surface passivated. The \_\_\_\_\_\_ transistor is double-diffused and surface \_\_\_\_\_.

## silicon dioxide

65.6 The emitter and base contacts in figure 65 are termed ohmic contacts. This indicates that they are passive or non-rectifying contacts. The junctions are active internally, but are surface \_\_\_\_\_\_.

planar passivated

65.7\*\* The mesa or flat topped peak is not needed in the planar because \_\_\_\_\_\_\_\_ is used to mask the device and allow controlled diffusion. Holes are cut through the surface protection for selected \_\_\_\_\_\_\_ of a given area for the emitter and base. The junctions are surface \_\_\_\_\_\_.

#### passivated

65.8 END OF SET

silicon dioxide diffusion passivated



PLANAR

FIGURE 65

#### SELF TEST

Read each question carefully, studying any diagrams provided and select the <u>most</u> <u>correct</u> answer.

- Forward biasing a PN junction results in majority carriers crossing the junction and becoming minority carriers. The average time the carriers exist after crossing the junction and before recombining is termed
  - a. half life of the material
  - b. minority carrier lifetime
  - c. transit time
  - d. recombination time
- 2. Applying forward bias to a PN junction with one side dopes much lighter than the other, results in some carriers failing to recombine and diffusing through the lightly doped side as carriers.
  - a. heat b. bias
  - c. majority
  - d. minority
- 3. Doping one side of a PN junction much lighter and making it very narrow results in much of the forward bias current in the external circuit being the result of

\_\_\_\_ current in the diode.

- a. diffusion
- b. majority carrier
- c. photon
- d. phonon
- 4. Forward bias current transported by diffusion of carriers results when the

\_ side of the junction is doped much lighter than the opposite side.

- a. N
- b. P
- c. either N or P
- d. none of the above

5. When two junctions are formed in a single piece of semiconductor, recombination occurs at both junctions until a state of \_\_\_\_\_\_ exists at both junctions and carrier movement across the junctions \_\_\_\_\_\_.

- a. pandimonium, starts
- b. balance, stops
- c. equilibrium, starts
- d. reverse bias, reverses

- Junction transistors are constructed by doping two junctions in a single piece of semiconductor with the two ends \_\_\_\_\_\_ doped and the center \_\_\_\_\_\_ doped.
  - a. lightly, heavilyb. heavily, heavilyc. heavily, lightly
  - d. lightly, lightly
- 7. The center portion of a junction transistor is made narrow to enhance the transport of carriers by \_\_\_\_\_\_ in the center portion.
  - a. photon
  - b. majority carrier
  - c. only electron
  - d. diffusion
- The center portion in the diagram is termed the \_\_\_\_\_ and the right hand portion the \_\_\_\_\_\_.



- a. base, collector
- b. collector, base
- c. gate, collector
- d. gate, anode
- Injection of carriers from the emitter into the base is accomplished by application of \_\_\_\_\_\_ to the emitter-base junction.
  - a. thermal energy
  - b. reverse bias
  - c. forward bias
  - d. series resistance

10. The collector junction is normally \_\_\_\_\_\_ biased and depends on \_\_\_\_\_\_
carriers in the base for current.

- a. reverse, minority
- b. forward, majority
- c. forward, minority
- d. reverse, majority

11	The en	nitte	er current is the sum of and current in the		
	THE CI				
		b. c. d. e.	recombination, diffusion, base collector, diffusion, base base, collector, transistor either a or c base, recombination, collector either b or e		
12.	h <sub>FB</sub> is		e symbol for current gain from the to the		
			of the transistor.		
		b. c.	<pre>small signal, emitter. collector d-c, base, collector small signal, base, collector d-c, emitter, collector</pre>		
13.	The p	rodu	ct of d-c current gain,(symbol), and the d-c base current		
			the value of current.		
			h <sub>FE</sub> , collector h <sub>FB</sub> , collector h <sub>FE</sub> , emitter h <sub>FB</sub> , emitter		
14.	A vai	riat	ion in base or emitter current will be accompanied by a change in		
	colle	ecto	r current. For a given change in base or emitter current, a change		
	in _		current will result in the greatest change in collector		
	curre	ent.			
			base emitter		
15.	I CBO	indi	cates current between and, with the		
	000		uited.		
		a. b. c.	emitter, collector, base collector, emitter, base collector, base, emitter emitter, base, collector		
16.	CBO is made up of carriers present as a result of and will vary				
	with a change in				
		b. c. d.	thermal energy, forward bias reverse bias, thermal resistance forward bias, temperature thermal energy, temperature reverse bias, capacitance		

17. I CEO is the current between \_\_\_\_\_ and \_\_\_\_\_ with the \_\_ open circuited. a. collector, emitter, base b. collector, base, emitter .c. emitter, base, collector d. collector, emitter, emitter 18. I<sub>CE0</sub>≈\_\_\_\_\_× I<sub>CB0</sub>. a, h b. h'E c. ambient temperature d. thermal resistance 19. 2Clead.

2CSYMBOL A SYMBOL B

Symbol B is a/an \_\_\_\_\_\_ transistor and point 2 indicates the \_\_\_\_\_

a. NPN, base b. PNP, base c. PNP, emitter d. NPN, emitter

20. A transistor in a common emitter configuration has a greater possible current gain than \_\_\_\_\_

- a. a transistor in a common base configuration
- b. a transistor in a common collector configuration
- c. unity
- d. any of the above
- e. either a or c

- 21. A transistor in a common \_\_\_\_\_\_ configuration can yield the highest possible power gain of the three configurations.
  - a. emitter
  - b. base
  - c. collector

22. A transistor in a common \_\_\_\_\_\_ configuration <u>cannot</u> offer a current gain greater than unity.

- a. collector
- b. emitter
- c. base

23. A transistor in a common \_\_\_\_\_\_ configuration <u>cannot</u> offer a voltage gain greater than unity.

- a. collector
- b. emitter
- c. base

24. h<sub>fe</sub> is the \_\_\_\_\_\_, a-c current gain of the transistor in a common configuration.

- a. direct current, base
- b. small signal, emitter
- c. direct current, emitter
- d. small signal, base

25. The small signal, a-c, current gain of the transistor in a common base configuration is given the symbol \_\_\_\_\_ and \_\_\_\_\_ include circuit effects.

a. h<sub>fb</sub>, does not
b. h<sub>fc</sub>, does not
c. h<sub>fb</sub>, does
d. h<sub>fe</sub>, does
e. h<sub>fc</sub>, does not

26. Power gain is possible with the common base configuration, although

gain is less than unity, since \_\_\_\_\_ gain greater than unity is possible. a. voltage, current b. current, voltage

<pre>configuration. a. emitter b. collector c. base h<sub>fc</sub> is the small signal, low frequency current gain of the transistor in a common configuration and is approximately equal to a. base, h<sub>fb</sub> + 1 b. emitter, h<sub>fe</sub> + 1 c. collector, h<sub>fb</sub> + 1 d. collector, h<sub>fe</sub> + 1 The emitter follower offers a input resistance and a output resistance. a. low, low b. high, high c. high, low d. low, high A transistor in a common configuration has a very low output resistance is able to supply large output a. collector, currents b. emitter, voltages c. base, voltages d. base, currents d. base, currents</pre>	is possible.
<pre>configuration. a. emitter b. collector c. base h<sub>fc</sub> is the small signal, low frequency current gain of the transistor in a common configuration and is approximately equal to a. base, h<sub>fb</sub> + 1 b. emitter, h<sub>fe</sub> + 1 c. collector, h<sub>fb</sub> + 1 d. collector, h<sub>fb</sub> + 1 d. collector, h<sub>fe</sub> + 1 The emitter follower offers a input resistance and a output resistance. a. low, low b. high, high c. high, low d. low, high A transistor in a common configuration has a very low output resistance is able to supply large output a. collector, currents b. emitter, voltages c. base, voltages d. base, currents The slope of a d-c load line constructed on a collector family of curves if</pre>	
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<pre>b. collector c. base h<sub>fc</sub> is the small signal, low frequency current gain of the transistor in a common configuration and is approximately equal to a. base, h<sub>fb</sub> + 1 b. emitter, h<sub>fe</sub> + 1 c. collector, h<sub>fe</sub> + 1 d. collector, h<sub>fe</sub> + 1 The emitter follower offers a input resistance and a output resistance. a. low, low b. high, high c. high, low d. low, high A transistor in a common configuration has a very low output resistance is able to supply large output a. collector, currents b. emitter, voltages c. base, voltages d. base, currents The slope of a d-c load line constructed on a collector family of curves is</pre>	configuration.
<pre>common configuration and is approximately equal to a. base, h<sub>fb</sub> + 1 b. emitter, h<sub>fe</sub> + 1 c. collector, h<sub>fb</sub> + 1 d. collector, h<sub>fe</sub> + 1 The emitter follower offers a input resistance and a output resistance. a. low, low b. high, high c. high, low d. low, high A transistor in a common configuration has a very low output resistance is able to supply large output a. collector, currents b. emitter, voltages c. base, voltages d. base, currents The slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family defined account of the slope of a d-c load line constructed on a collector family defined account of the slope of a d-c load line constructed on a collector family defined account defined accou</pre>	b. collector
<ul> <li>a. base, h<sub>fb</sub> + 1</li> <li>b. emitter, h<sub>fe</sub> + 1</li> <li>c. collector, h<sub>fb</sub> + 1</li> <li>d. collector, h<sub>fe</sub> + 1</li> </ul> The emitter follower offers a input resistance and a output resistance. <ul> <li>a. low, low</li> <li>b. high, high</li> <li>c. high, low</li> <li>d. low, high</li> </ul> A transistor in a common configuration has a very low output resistance is able to supply large output <ul> <li>a. collector, currents</li> <li>b. emitter, voltages</li> <li>c. base, voltages</li> <li>d. base, currents</li> </ul> The slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c l	$^{ m h}_{ m fc}$ is the small signal, low frequency current gain of the transistor in a
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<pre>d. collector, h<sub>fe</sub> + 1 The emitter follower offers a input resistance and a output resistance.     a. low, low     b. high, high     c. high, low     d. low, high A transistor in a common configuration has a very low output resistance is able to supply large output     a. collector, currents     b. emitter, voltages     c. base, voltages     d. base, currents The slope of a d-c load line constructed on a collector family of curves in </pre>	b. emitter, h <sub>fe</sub> + 1
The emitter follower offers a input resistance and a output resistance. a. low, low b. high, high c. high, low d. low, high A transistor in a common configuration has a very low output resistance is able to supply large output a. collector, currents b. emitter, voltages c. base, voltages d. base, currents The slope of a d-c load line constructed on a collector family of curves in	c. collector, h <sub>fb</sub> + 1
<pre>output resistance.     a. low, low     b. high, high     c. high, low     d. low, high A transistor in a common configuration has a very low output resistance is able to supply large output     a. collector, currents     b. emitter, voltages     c. base, voltages     d. base, currents The slope of a d-c load line constructed on a collector family of curves i </pre>	d. collector, h <sub>fe</sub> + 1
<ul> <li>a. low, low</li> <li>b. high, high</li> <li>c. high, low</li> <li>d. low, high</li> </ul> A transistor in a common configuration has a very low output resistance is able to supply large output <ul> <li>a. collector, currents</li> <li>b. emitter, voltages</li> <li>c. base, voltages</li> <li>d. base, currents</li> </ul> The slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of the slope of a d-c load line constructed on the slope o	The emitter follower offers a input resistance and a
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<ul> <li>a. collector, currents</li> <li>b. emitter, voltages</li> <li>c. base, voltages</li> <li>d. base, currents</li> </ul> The slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed line constructed on the slope of a d-c load line constructed line con	A transistor in a common configuration has a very low output
<ul> <li>b. emitter, voltages</li> <li>c. base, voltages</li> <li>d. base, currents</li> </ul> The slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on a collector family of curves in the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed on the slope of a d-c load line constructed d-c load line con	resistance is able to supply large output
<pre>c. base, voltages d. base, currents The slope of a d-c load line constructed on a collector family of curves i</pre>	
The slope of a d-c load line constructed on a collector family of curves i	
	d. base, currents
determined by the in the transistor.	The slope of a d-c load line constructed on a collector family of curves is
	determined by the in the transistor.
a. reactance, series with b. resistance, series with	
c. current, the base of	

	The d-c load line is constructed between the maximum point and				
	the maximum point on the collector family of curves set by the				
	series resistance and the total supply				
	a. voltage, current, current b. voltage, current, voltage c. voltage, current, resistance d. resistance, current, voltage				
ŀ.	The transistor is termed in saturation when the collector becomes				
	. The collector voltage at this point is given the symbol				
	a. cut-off, V <sub>CC</sub>				
	b. forward biased, <sup>BV</sup> CBO				
	c. reversed biased, V <sub>CE(sat)</sub>				
	d. forward biased, V <sub>CE(sat)</sub>				
	e. fully saturated, BV CBO(sat)				
- ) .	Saturation in a transistor results in an increase in the				
	in the base as a result of the collector junction becoming biase				
	a. stored charge, reverse b. depletion region, forward c. depletion region, reverse d. stored charge, forward				
, ).	Avalanche breakdown occurs at high collector voltages due to t				
	of carriers at the collector junction.				
	a. forward, acceleration b. reverse, recombination				
	<ul><li>c. reverse, multiplication</li><li>d. forward, multiplication</li></ul>				
7.	Changing the transistor's configuration will change the collector voltage poir				
	at which avalanche breakdown occurs. ${}^{ m BV}{}_{ m CB0}$ indicates the breakdown voltage,				
	to with the d-c open circuited.				
	a, collector, base, emitter b. collector, emitter base c. emitter base, collector d. collector, ground, emitter				

38.	BV CEO inc	dicates the breakdown voltage, to	with the			
		d-c open circuited.				
	b. c.	base, emitter, collector collector, emitter, base collector, base, emitter collector, ground, emitter				
39.	BV <sub>CER</sub> is	the breakdown voltage, to	with a			
	specified	d value of resistance between and	. ·			
	b. c.	collector, emitter, collector, base collector, base, base, emitter collector, emitter, base, emitter collector, emitter, collector, emitter				
40.	Maximum s	steady state power dissipation in a transistor is limited b	y the maximum			
	allowable	e junction, surrounding air, an	d the total			
		, junction to ambient.				
	b.	temperature, temperature, thermal resistance current, temperature, temperature gradient voltage, temperature, thermal resistance temperature, temperature, temperature gradient				
41.	$\theta_{IA}$ is the	ne symbol for thermal resistance, to	and is			
	011	in				
	b. c.	<pre>jacket, ambient, °C/watt junction, area, watts/°C junction, ambient, watts/°C junction, ambient, °C/watt</pre>				
42.	$\Theta_{\rm JC} + \Theta_{\rm CS}$	+ = $\Theta_{JA}$ when a separate sink is us	ed with a			
	transisto	pr.				
		$\Theta_{sc}$ , heat $\Theta_{cA}$ , conductance $\Theta_{cA}$ , heat $\Theta_{sA}$ , heat				
43.		lubricant reduces thermal resistance, case to	and			
	as a resu	as a result, reduces total thermal resistance.				
	a. b. c.	Germanium, heat sink				

5		
		$ \Theta_{JC} = 1.8^{\circ}C/watt $ $ \Theta_{SA} = 3.6^{\circ}C/watt $ $ \Theta_{CS} = 0.6^{\circ}C/watt $ $ T_{A} = 60^{\circ}C $ $ T_{Jmax} = 150^{\circ}C $ $ P_{max} = \frac{T_{J(max)} - T_{A}}{\Theta_{JA}} $
		JIIAX
		The maximum steady state power the transistor can dissipate with the thermal characteristics listed above is
		a. l.5 watts b. 30 watts c. l5 watts d. 3 watts
J	45.	For maximum linear power operating in the active region, the load line should be
		placed a. tangent to the maximum power curve in the most linear region of curves. b. from $BV_{CB0}$ to a point tangent to the maximum power curve c. from $I_{C}(max)$ to a point tangent to the maximum power curve d. $I_{C}(max)$ to $V_{CE}(max)$
	46.	Answer d in question 45 will allow for a given transistor. a. maximum linear power b. maximum power with maximum current swing in the linear region c. maximum power for low repetition rate switching d. maximum power for high repetition rate switching
	47.	Little power is dissipated at cut-off and while most of the power
		<pre>is dissipated in the region of the transistor's character- istics. a. transient, active b. depletion, transient c. saturation, active d. saturation, depletion</pre>
	48.	power can be dissipated during switching with the tran-
		<pre>sistor is operated as a cut-off to saturated, low rep-rate switch and the load line can the maximum power curve on a collector family of curves. a. less, not cross over b. more, be tangent to c. more, be in the safe area below d. more, cross over</pre>

49.	The off t	o saturated switching mode offers resting state power,				
		ed repetition rate due to increased				
	a. b. c.	low, storage time high, storage time maximum, transit time low, transit time				
50.	A transis	tor switch turn on time (t <sub>on</sub> ) is equal to the sum of				
	and	, and the transistors turn off time is equal to the sum of				
		and when using the switching parameters.				
	b. c.	rise time, transit timefall time, response timerise time, transit timestorage time, fall timerise time, delay timestorage time, fall timerise time, interface timestorage time, recovery time				
51.	A capacit	or used to reduce switching time in a transistor switching configur-				
	ation, by	aiding in the establishment and removal of the stored charge is re-				
	ferred to	as a capacitor.				
	b. c.	switching filter speed up charge chopper time chopper				
52.	The charg	e on the capacitor mentioned in question 51 should be the				
	transisto	rs stored charge for an effective increase in switching time.				
	b. c.	equal to less than ten times one tenth of				
53.						
	saturated	mode, but sacrifices				
	b. c.	cut-off, flexibility current mode, less critical transistor specification voltage mode, power current mode, power capabilities				
54.		switching transistor has the transistor switching in the				
	collector breakdown region and can offer rise times in the fractional					
		avalanche, nano				
	b. c. d.	avalanche, micro current mode, nano current mode, micro avalanche, milli				

55. The three main high frequency limiting factors in transistors are

a. doping ratio, junction capacity, storage time

- b. junction capacity, base transit time, thermal resistance
- c. base transit time, spreading of carriers in the base, junction capacity
- d. emitter transit time, spreading of carriers in the base, junction capacity

> a.  $f_{hfe}$ ,  $h_{fe}$ b.  $f_t$ ,  $h_{fb}$ c.  $f_{hfb}$ ,  $h_{fb}$ d.  $f_{\alpha_b}$ ,  $h_{fe}$

, and \_\_\_\_\_

57. C<sub>ob</sub> is the symbol for the output capacitance of a transistor in a common \_\_\_\_\_\_\_ orientation. C<sub>oe</sub> is the symbol for the output capacitance of a transistor in a common \_\_\_\_\_\_ orientation. a. base, emitter

b. emitter, base

58. A \_\_\_\_\_\_ base and \_\_\_\_\_\_ junction capacity is the aim in high frequency transistors.

a. heavily doped, lowb. lightly doped, diffusedc. narrow, low

d. narrow, variable

59. f<sub>t</sub> is the symbol for the frequency at which \_\_\_\_\_\_ falls to \_\_\_\_\_.
a. h<sub>fe</sub>, unity
b. h<sub>fb</sub>, 0.707 of low frequency value

c.  $h_{fe}$ , 0.707 of low frequency value

d. h<sub>fb</sub>, unity

60. f<sub>hfe</sub> indicates the cut-off (\_\_\_\_\_) of the transistor in a common \_\_\_\_\_\_ configuration.

a. h<sub>fe</sub> = unity, emitter

b. low frequency  $h_{fe} \times 0.707$ , base

c.  $h_{fe} = unity$ , base

d. low frequency  $h_{fe} \times 0.707$ , emitter

29. d 30. c

59. a 60. d

# ANSWERS TO SELF TEST

1.	b	31.	а
2.	d	32.	b
3.	a	33.	b
4.	d	34.	d
5.	b	35.	d
6.	с	36.	С
7.	d	37.	а
8.	a	38.	b
9.	с	39.	С
10.	а	40.	а
11.	d	41.	d
12.	d	42.	d
13.	а	43.	b
14.	а	44.	С
15.	с	45.	а
16.	d	46.	С
17.	a	47.	С
18.	b	48.	d
19.	b	49.	а
20.	e	50.	С
21.	a	51.	b
22.	с	52.	а
23.	a	53.	d
24.	b	54.	а
25.	a	55.	С
26.	b	56.	С
27.	b	57.	а
28.	b	58.	С
29.	d	59.	а
30.	с	60.	d