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WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

468
DIGITAL STORAGE OSCILLOSCOPE

SERVICE

VOLUME I

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

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Product Group 40

Serial Number _____

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates either a personal injury hazard not immediately accessible as one reads the marking or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols as Marked on Equipment


DANGER – High voltage.


Protective ground (earth) terminal.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and connectors, see Figure 2-2.

Use the Proper Fuse

To avoid fire hazard, use only a fuse of the correct type, voltage rating, and current rating as specified in the parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

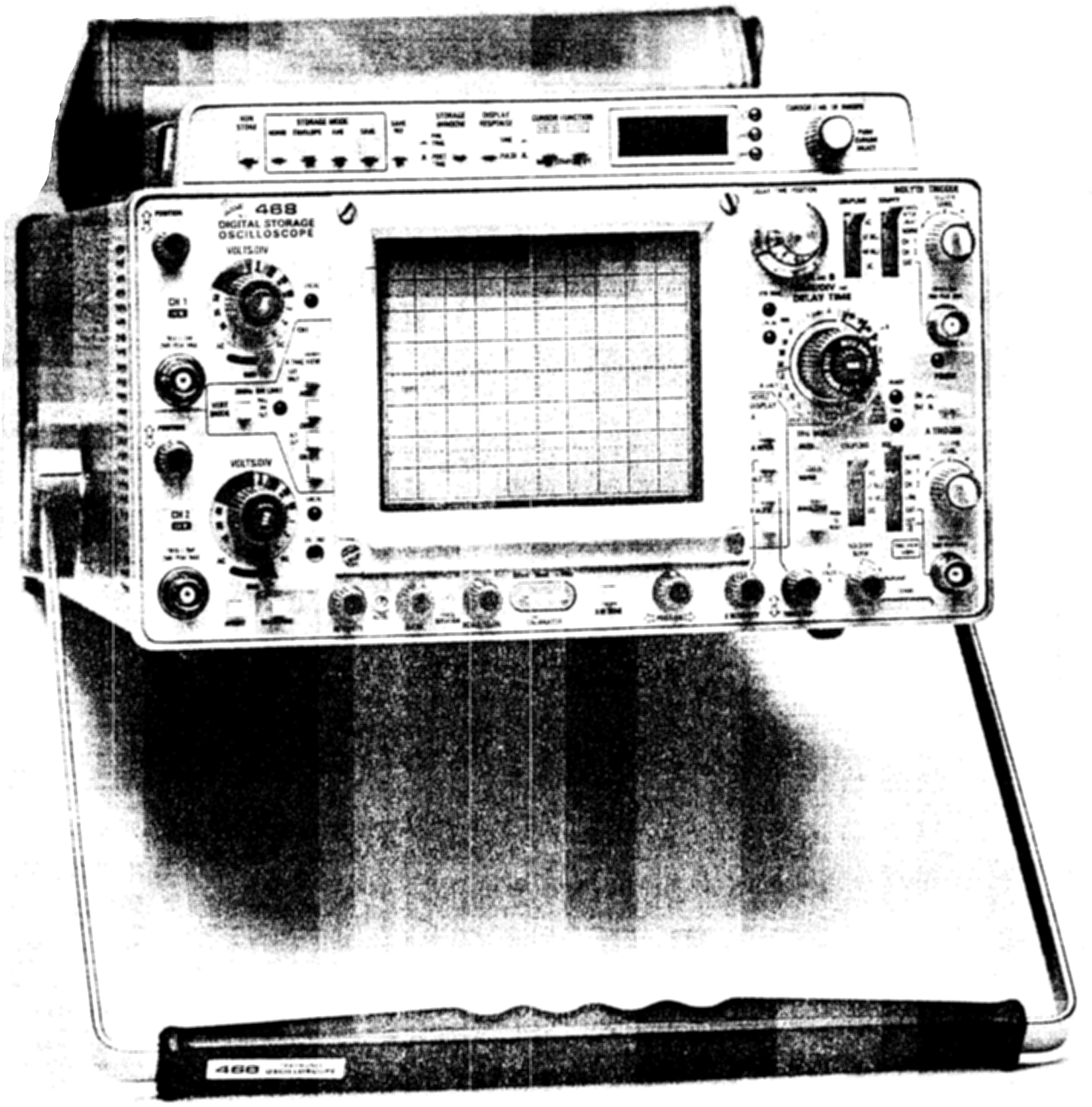
Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



The 468 Digital Storage Oscilloscope.

3515-01

SPECIFICATION

INTRODUCTION

The TEKTRONIX 468 Oscilloscope is a portable digital storage oscilloscope with a four-trace, dc-to-100 MHz, vertical deflection system. The 468 combines an easy-to-use storage function with cursor measurement of time and voltage. Measurement values are indicated on a four-digit, seven-segment LED display.

NON STORE MODE

In the NON STORE mode, the 468 operates as a conventional oscilloscope that can display CH 1, CH 2, ADD, and A TRIG VIEW (external trigger only) simultaneously. The vertical deflection system has calibrated deflection factors ranging from 5 mV to 5 V per division. The horizontal deflection system has calibrated A Sweep rates from 0.5 s to 0.02 μs per division and is capable of operating in the following sweep modes: A, A intensified by B, A alternated with delayed B, and B delayed. The calibrated B Sweep rates are from 50 ms to 0.02 μs per division.

The horizontal magnifier circuit feature increases each sweep rate by a factor of 10. This provides a maximum sweep rate of 2 ns per division when the TIME/DIV switch is in the 0.02 μs per division position.

STORAGE MODE

The 468 digital storage circuitry has a 10 MHz Useful Storage Bandwidth for the acquisition of signals, and will display the acquired waveform with a bright, flicker-free trace. With the digital storage feature, low-frequency signal analysis and waveform measurements—previously difficult or impossible to make—are easily performed. A choice of two standard and one optional signal acquisition modes are available: NORM and ENVELOPE (standard) and AVG (optional). Two storage functions are available to hold a display indefinitely for measurement and comparison: SAVE Storage Mode (stops acquisition) and SAVE REF (holds a reference display and continues acquisition in the selected Storage Mode). Using the PRE TRIG or POST TRIG Storage Window, waveform data may be acquired prior to or after the trigger. Time and voltage measurements on the acquired waveform are easily made using the VOLTS and TIME Cursor Functions, and the measurement values are indicated on a four-digit, seven-segment light-emitting diode (LED) display.

Digital storage adds three TIME/DIV switch positions, increasing the storage time base to 5 s per division (a total sweep time of 50 s). The waveshape of signals acquired at these low frequencies would be impossible to view on a conventional oscilloscope. Digital storage circuitry, however, constantly refreshes an acquired waveform to produce a directly viewable display for ease of analysis and measurement. Three added VOLTS/DIV switch positions increase the digital storage vertical deflection sensitivity up to 0.5 mV per division. Small-amplitude signals are acquired at 5 mV per division and are amplified to produce the added sensitivity.

The digital storage signal acquisition modes are NORM and ENVELOPE Storage Modes and an optional AVG Storage Mode. Selecting NORM Storage Mode causes acquisition and display of a new waveform with each trigger. The display in this mode most resembles conventional oscilloscope displays, and waveforms acquired will react to the oscilloscope front-panel controls with each trigger.

When ENVELOPE Storage Mode is chosen, the maximum and minimum waveform values for a selected number of sweeps are acquired, and the resultant waveform envelope is displayed. This mode is useful for detecting noise and spurious or erratic signals.

Choosing the optional AVG Storage Mode allows waveforms to be acquired for a selected number of sweeps and causes the averaged value of the acquired signals to be displayed. In this mode, signal-to-noise ratio is improved in direct proportion to the square root of the number of sweeps acquired, and noise accompanying the signal is either averaged out or reduced to a small level. The signal acquired in the AVG Storage Mode is processed to increase the vertical resolution of the displayed signal. This feature is very useful for displaying small-amplitude signals acquired in the 0.5, 1, and 2 mV per division positions of the VOLTS/DIV switch.

Once the desired signal is obtained in storage, the signal acquisition may be halted and the display frozen by selecting the SAVE Storage Mode. The waveform will remain displayed indefinitely for analysis and measurement purposes. In the SAVE mode, the next six faster positions of the TIME/DIV switch (if available) horizontally expand the display (up to 100 times). Additionally, signals acquired at sweep rates of 1 μs per division or faster may be reduced back to the 2 μs per division acquisition rate.

The SAVE display may also be expanded vertically (up to 10 times) with the next three higher deflection sensitivity positions of the VOLTS/DIV switch (if available) for the channel used to obtain the SAVE display. Signals obtained in the NORM or ENVELOPE Storage Mode at VOLTS/DIV switch settings 0.5, 1 or 2 mV per division may be reduced back to the 5 mV per division deflection sensitivity if desired. The SAVE display of a waveform acquired in the AVG Storage Mode may be expanded, but it may not be reduced below the deflection sensitivity at which the signal was acquired.

When the SAVE REF push button is pressed in, the waveform being displayed at that time will be stored and held on the display while the digital storage continues to acquire data. The SAVE REF display is then available for comparison with signals obtained from other circuits, or it can be used as a before-and-after check on circuit operation when changes or adjustments are made to the circuit under test. A new reference waveform is obtained each time the button is released and then pressed in again. Displaying the reference signal reduces the number of vertical mode possibilities that the 468 is capable of displaying simultaneously.

The time window used to obtain a stored waveform may be set to acquire either aproximately 8.75 horizontal divisions of waveform data occurring before the triggering signal (in PRE TRIG Storage Window) or the same amount of waveform data occurring after the triggering signal (in POST TRIG Storage Window). The PRE TRIG feature is useful for analyzing events that might cause an error to occur. If the oscilloscope is set to trigger on the error, data immediately prior to the error is stored for analysis. POST TRIG Storage Window most resembles conventional triggering; but while conventional oscilloscope triggering usually starts the sweep, POST TRIG Storage Window triggering does not occur until approximately 1.25 horizontal divisions of waveform data are acquired.

Voltage and time measurements are made directly on the displayed waveform. Pressing in the VOLTS Cursor Function push button causes two horizontal lines (VOLTS Cursors) to be presented on the display. Only one cursor at a time is positionable using the CURSOR control knob. The active cursor is displayed as a dashed line, while the fixed cursor is a solid line. Voltage difference (as represented by the cursor positions) is directly read on the seven-segment LED display, and the appropriate measurement scale factor is shown on the three dual-color (red and green) LED indicators to the right of the seven-segment LED display. Time measurements are made using two bright, positionable dots that appear on the trace when the TIME Cursor Function button is pressed in. The TIME cursor dots are positioned to the desired measurement points, and the time difference between the dots is directly read on the LED display.

A COUPLED V/T measurement mode is made available by pressing in both the VOLTS and TIME Cursor Function push buttons. In this mode, the TIME dots attach to the VOLTS cursors, and the VOLTS cursors will never be displayed beyond the limits of the waveform. The COUPLED V/T mode is useful for slope, peak-to-peak amplitude, and time duration measurements. While the cursors are coupled, the LED readout will display the voltage difference between the cursors.

In instruments factory equipped or converted to firmware version 2.0 or higher, the COUPLED V/T mode is also useful for making asolute dc-voltage measurements with respect to ground.

AVAILABLE OPTIONS

Option 02 is the General Purpose Interface Bus (GPIB), used to transmit the waveform data stored in the display memory. The waveform data transmitted will conform to the Waveform Transmission Standard as specified in the Tektronix Interface Standard—General Purpose Interface Bus (GPIB), Codes and Formats.

Option 12 is the AVE Storage Mode. This option will acquire data for a selected number of sweeps (from 2 to 256 in a binary sequence) and display the average waveform accumulated.

NOTE

The AVE Storage Mode is part of the standard instrument above SN B032430.

Option 04 (EMC provides additional reduction of electromagnetic interference.

Option 05 provides the instrument with front-panel selection of additional trigger-signal processing capabilities to facilitate observation and measurement of composite video and related television waveforms.

Option 11 enables the 468 to convert the digital data stored in memory into analog X and Y outputs for driving an X-Y Plotter.

SPECIFICATION TABLES

The following electrical characteristics (Table 1-1) are valid only if the instrument has been calibrated at an ambient temperature between +20°C and +30°C, the instrument is operating at an ambient temperature between −15°C and +55°C (unless otherwise noted), and the instrument has had a warmup period of about 20 minutes.

Environmental characteristics are given in Table 1-2. The 468 meets the requirements of MIL-T-28800B, Class 3, Style D equipment. Physical characteristics are listed in Table 1-3, and option electical characteristics are presented in Table 1-4.

Table 1-1

Electrical Characteristics

Characteristics	Performance Requirements	Supplemental Information
VERTICAL SYSTEM		
Deflection Factor (Nonstorage Mode)		
Range		5 mV per division to 5 V per division in a 1-2-5 sequence of 10 steps.
DC Accuracy	Graticule indication is within 3% of true input voltage up to ±12 divisions, referenced to instrument ground, for all calibrated VOLTS/DIV switch settings.	Gain set with VOLTS/DIV switch set to 5 mV per division.
Uncalibrated (VAR) Range (Nonstorage Mode)	Continuously variable between settings of VOLTS/DIV switch. Extends deflection factor to at least 12.5 V per division.	
Low-Frequency Linearity		0.1 division or less compression or expansion of a 2-division signal at center screen with waveform positioned to upper and lower extremes of graticule area.
Frequency Response		5-division reference signal from a 25-Ω source; centered vertically, with VAR VOLTS/DIV control in calibrated detent.
Bandwidth (Channel 1 and Channel 2 Nonstorage Mode)		
−15°C to +40°C	Dc to at least 100 MHz.	
+40°C to +55°C	Dc to at least 85 MHz.[a]	
AC Coupled Lower −3 dB Point		
1X Probe	10 Hz or less.	
10X Probe	1 Hz or less.	

[a]Performance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
VERTICAL SYSTEM (cont)		
Step Response (Non-Storage Mode)		5-division reference signal, dc coupled at all deflection factors, from a 25-Ω source; vertically centered with VAR VOLTS/DIV control in calibrated detent.
Rise Time		
0°C to +40°C	3.5 ns or less (calculated).[a]	Rise Time = $\frac{0.35}{\text{BW (in MHz)}}$
Positive-Going Step (Excluding ADD Mode)		
Aberrations		
0°C to +40°C		+4%, −4%, 4% p-p or less. +6%, −6%, 6% p-p or less (5 V setting only).
Position Effect		
0°C to +40°C		Total aberrations less than +6%, −6%, 6% p-p; checked at 5 mV per division.
Negative-Going Step		Add 2% to all positive-going specifications; checked at 5 mV per division.
ADD Mode Operation		Add 5% to all aberration specifications; checked at 5 mV per division.
Common Mode Rejection Ratio (ADD Mode With Channel 2 Inverted)		At least 10:1 at 20 MHz for common mode signals of 6 divisions or less with GAIN adjusted for best CMRR at 50 kHz. (10:1 at 10 MHz for storage mode.)
Trace Shift as VAR VOLTS/DIV Control Is Rotated		1 division or less. Digital Storage scale-factor LED will indicate voltage measurements are in divisions in a storage mode with the VAR control out of calibrated detent.
INVERT Trace Shift		Less than 2 divisions when switching from non-inverted to inverted.
Input Gate Current		
+20°C to +30°C		0.5 nA or less (0.1 division or less trace shift when switching input coupling between DC and GND with VOLTS/DIV switch set to 5 mV per division).
−15°C to +55°C		4 nA or less (0.8 division or less trace shift when switching input coupling between DC and GND with VOLTS/DIV switch set to 5 mV per division).

[a]Performance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
VERTICAL SYSTEM (cont)		
Channel Isolation		At least 100:1 at 25 MHz (10 MHz in storage).
Vertical POSITION Range		At least +12 and −12 divisions from graticule center.
Chopped Mode Repetition Rate (Nonstorage Mode)	Approximately 500 kHz.	Within 20%.
Input R and C		
Resistance	1 MΩ, within 2%.[a]	
Capacitance	Approximately 20 pF.[a]	
R and C Product (+20°C to +30°C)		Aberrations 2% or less using a P6105 probe.
Maximum Input Voltage		
DC Coupled	250 V (dc + peak ac).[a] 500 V (p-p ac at 1 kHz or less).[a]	
AC Coupled	250 V (dc + peak ac).[a] 500 V (p-p ac at 1 kHz or less).[a]	
Cascaded Operation		CH 1 VERT OUT SIGNAL OUT coupled into CH 2 input; ac coupled, using 50-Ω, 42-inch RG-58 C/U cable, terminated in 50 Ω at the CH 2 input connector.
Bandwidth (Nonstorage)	Dc to at least 50 MHz.	
Cascaded Sensitivity	At least 1 mV per division; terminated in 50 Ω at the CH 2 input connector.	
DIGITAL STORAGE VERTICAL ACQUISITION		
Resolution		8 bits, 25 levels per division. 10.24 divisions dynamic range.
DC Accuracy	Scaled binary value of stored digital word is within 3% of true input voltage up to ±12 divisions, referenced to instrument ground, for all calibrated VOLTS/DIV switch settings.	Gain set with VOLTS/DIV set to 5 mV per division.
Range		0.5 mV to 5 V per division in a 1-2-5 sequence of 13 steps.
Digital Sample Rate		10 Hz to 25 MHz as determined by the TIME/DIV switch setting.

[a]Performance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements		Supplemental Information
DIGITAL STORAGE VERTICAL ACQUISITION (cont)			
Digital Chop Rate			5 Hz to 12.5 MHz (1/2 of the non-chopped sample rate at all TIME/DIV switch settings).
Analog Step Response	3% or less acquired overshoot on a 5-division pulse with Display Response set to PULSE.		Checked on a saved waveform display using horizontal expansion (X10 MAG off).
Analog Bandwidth	Dc to 10 MHz, within ±1 dB, measured in ENVELOPE Storage Mode with the TIME/DIV switch set to 1 ms.		At exactly 10 MHz input signal frequency, it is possible for aliasing to occur and produce an envelope with variable amplitude. If aliasing occurs, shift the test frequency slightly to obtain an envelope with flat amplitude.
Useful Storage Bandwidth			
NORM Storage Mode	**Single Trace or Alt**	**CHOP**	
SINE Display Response	Dc to 10 MHz, within +1, −3 dB, measured p-p over any single cycle, with TIME/DIV switch set to 0.2 μs (X10 MAG off).	Dc to 5 MHz, within +0.5, −1.5 db, measured p-p over any single cycle, with TIME/DIV switch set to 0.2 μs (X10 MAG off).	For SINE Display Response, useful storage bandwidth is limited to that frequency where there are 2.5 samples per input cycle period at the maximum sampling rate (max sampling rate is 25 MHz in Single Trace or ALT and 12.5 MHz in CHOP). Accuracy at useful storage bandwidth limit is measured with respect to a 6 division, 50 kHz reference sine wave.
PULSE Display Response	Dc to 3.5 MHz, within +0.5, −1.5 dB, measured p-p over any single cycle, with TIME/DIV switch set to 0.2 μs (X10 MAG off).	Dc to 1.75 MHz, within +0.5, −1.5 db, measured p-p over any single cycle, with TIME/DIV switch set to 0.2 μs (X10 MAG off).	For PULSE Display Response, useful storage bandwidth is limited to that frequency where there are 7 samples per input cycle period at the maximum sampling rate (max sampling rate is 25 MHz in Single Trace or ALT and 12.5 MHz in CHOP). Accuracy at useful storage bandwidth limit is measured with respect to a 6-division, 50-kHz reference sine wave.
Useful Storage Rise Time			Useful storage rise time is defined as 1.6 times the minimum sampling interval (40 ns in Single Trace or ALT and 80 ns in CHOP).
NORM Storage Mode			
PULSE Display Response	64 ns.	128 ns.	

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
TRIGGERING		
Sensitivity		In EXT/10, multiply requirements by 10.
AC Coupled Signal	0.3 division internal or 50 mV external from 30 Hz to 10 MHz; increasing to 1.5 divisions internal or 150 mV external up to 100 MHz.	
LF REJ Coupled Signal	0.5 division internal or 100 mV external from 50 kHz to 10 MHz; increasing to 1.5 divisions internal or 300 mV external up to 100 MHz.	Attenuates signals below approximately 50 kHz.
HF REJ Coupled Signal	0.5 division internal or 100 mV external from 30 Hz to 50 kHz.	Attenuates signals above approximately 50 kHz.
DC Coupled Signal	0.3 division internal or 50 mV external from dc to 10 MHz; increasing to 1.5 divisions internal or 150 mV external up to 100 MHz.	
Trigger Jitter		
Nonstorage Mode	0.5 ns or less at 100 MHz at 2 ns per division (X10 MAG on).	
Storage Mode	±1 sample period for data transmitted on the GPIB. See Jitter Correction Performance Requirement.[a]	Inherent ±1 sample jitter between sample clock and asynchronous trigger is partially compensated for by the jitter correction circuitry.
External Trigger Inputs		
Maximum Input Voltage	250 V (dc + peak ac).[a] 250 V (p-p ac at 1 kHz or less).[a]	
Input Resistance	1 MΩ within 10%.[a]	
Input Capacitance		Approximately 20 pF, within 30%.
LEVEL Control Range		
EXT	At least + and −2 V, 4 V p-p.	
EXT/10	At least + and −20 V, 40 V p-p.	
A External Trigger View (Nonstorage Mode Only)		
Deflection Factor		Dc trigger coupling only; checked with a 1 kHz signal.
EXT	100 mV per division ±5%.	
EXT/10	1 V per division ±5%.	

[a]Performance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
TRIGGERING (cont)		
A External Trigger View (Nonstorage Mode Only) (cont)		
Rise Time	5 ns or less.[a]	BW Limit at full (button out).
Delay Difference	⩽±0.20 division (⩽±400 ps at 2 ns per division).	5-div signal with 5 ns rise time or less from a 25-Ω source; centered vertically with equal 50-Ω cable length from signal source to vertical channel and external trigger input connectors; terminated in 50-Ω at each input.
Centering of Triggering Point		Within 1 division of center screen.
Flatness and Aberrations		+10%, −10%, 10% p-p.
HORIZONTAL DEFLECTION SYSTEM		
Sweep Rate (Nonstorage Mode)		
Calibrated Range		
A Sweep		0.5 s/div to 0.02 μs/div in 23 steps in a 1-2-5 sequence. X10 MAG extends maximum sweep rate to 2 ns/div.
B Sweep		50 ms/div to 0.02 μs/div in 20 steps in a 1-2-5 sequence. X10 MAG extends maximum sweep rate to 2 ns/div.
Accuracy	Within the given percentages of the indicated value.	Accuracy specification applies over the full 10 div of the unmagnified sweep.
	Unmagnified / **Magnified**	In X10 MAG, at TIME/DIV switch setting of .02 μs, .1 μs, and .2 μs, exclude the first and last 50 ns of the sweep; and at a TIME/DIV switch setting of .5 μs, exclude the first 100 ns of the sweep.
+20°C to +30°C	Within 2% / Within 3%	
−15°C to +55°C	Within 3%[a] / Within 4%[a]	
Two-Division Linearity Check		±5% over any two-division portion (or less) of the full 10 div. When in X10 MAG exclude first and last magnified div when checking 2 ns,5 ns, and 10 ns/div rates.
Alternate Sweep Trace Separation (Nonstorage Mode Only)		⩾±4 divisions.
Variable Range (A Only) (Nonstorage Mode)	Continuously variable between calibrated settings of the A TIME/DIV switch. Extends slowest A sweep rate to at least 1.25 s/div.	At least 2.5:1.

[a]Performance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements		Supplemental Information
HORIZONTAL DEFLECTION SYSTEM (cont)			
A Sweep Length (Nonstorage Mode)			10.5 to 11.5 divisions.
A Trigger HOLDOFF (Variable)			Increases A sweep holdoff time by at least a factor of 10 (Nonstorage Mode). Storage holdoff time is a function of microprocessor operation.
Magnifier Registration			Within 0.2 division from graticule center (X10 MAG on to X10 MAG off).
POSITION Range (Horizontal)			Start of sweep must position to right of graticule center. End of sweep must position to left of graticule center.
Differential Time Measurement Accuracy (Nonstorage Mode)	**Measurements of 1 or more major dial divisions**	**Measurements of less than 1 major dial division**	With the A TIME/DIV switch at 0.5 μs per division, or 0.2 μs per division, the differential time measurement accuracy limit is valid only for DELAY TIME POSITION dial settings between 1.50 and 8.50.
+15°C to +35°C	Within 1% of indicated value.	±0.01 major dial division.	
−15°C to +55°C	Within 2.5% of indicated value.[a]	±0.03 major dial division.[a]	
Delay Time Jitter (Nonstorage Mode)	One part or less in 50,000 (0.002% of 10 times the A TIME/DIV switch setting) when operating on an ac-power-source frequency above 50 Hz. One part or less in 20,000 (0.005% of A TIME/DIV switch setting) when operating on a 50-Hz or lower ac-power source frequency.[a]		
Calibrated Delay Time (VAR Control in Calibrated Detent)	Continuous from 0.2 μs to at least 5 s after the delaying (A) sweep.		
X-Y Operation (Nonstorage Mode Only)			
X-Axis Deflection Factor	Same as vertical system, with X10 MAG off.		
Variable Range	Same as vertical system.		
X-Axis Bandwidth	Dc to at least 4 MHz.		10-division reference signal.
Input Resistance	Same as vertical system.[a]		
Input Capacitance	Same as vertical system.[a]		

[a]**Performance requirement not checked in manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
HORIZONTAL DEFLECTION SYSTEM (cont)		
X-Y Operation (Nonstorage Mode Only) (cont)		
Maximum Usable Input Voltage	Same as vertical system.[a]	
Phase Difference Between X and Y Amplifiers		Within 3° from dc to 50 kHz.
Deflection Accuracy	Graticule indication is within 4% of true input voltage.	
DIGITAL STORAGE HORIZONTAL ACQUISITION		
Horizontal Resolution		
Single Waveform Acquisition		9 bit. 512 data points (50 data points per division across the graticule area).
Chopped Acquisition (NORM Storage Mode Only)		8 bit. 256 data points per division (25 data points per division across the graticule area).
Range		5 s per division to 20 ns per division in a 1-2-5 sequence. At TIME/DIV switch settings of 5 s to 2 µs, waveform sampling rate is determined by the switch setting. From 1 µs to 0.02 µs per division, sampling rate is at the 2 µs per division rate. Interpolation and analog gain are used to expand the signal to the correct horizontal scale.
Accuracy (Sample Period)		Sample clock is within 0.01% of selected sample period, ±50 ps ADC aperture uncertainty. Crystal oscillator: 0°C to +70°C V_{cc} = +5 V ±0.5 V.
Dynamic Range	10.24 divisions.	
STORAGE DISPLAY		
Vertical		
Resolution		1 part in 1024 (10 bit). Calibrated for 100 points per division.
Differential Accuracy	Graticule indication of voltage cursor difference is within 2% of LED readout value, measured over center six divisions.	

[a]**Performance requirement not checked in manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
STORAGE DISPLAY (cont)		
Vertical (cont) POSITION Range		Any portion of a stored waveform vertically magnified X10 can be positioned to the top and to the bottom of the graticule area.
Position Registration NON STORE to NORM		Within ±0.5 division at graticule center at VOLTS/DIV settings from 5 mV to 5 V per division.
NORM, ENVELOPE, or AVG to SAVE		Within ±0.2 divisions at VOLTS/DIV settings from 5 mV to 5 V per division.
SAVE Mode Gain Range (Vertical)		Up to X10 as determined by the setting of the VOLTS/DIV switch.
ENVELOPE Fill		90% or more of a six division ENVELOPE display.
Rise Time		≤ 0.3 horizontal graticule division for a five-division step, with horizontal X10 MAG on. Checked with no samples on the rising edge of the waveform.
Aberrations		+6%, −6%, 6% p-p or less on a five-division step (fast rise) input.
Horizontal Resolution		1 part in 1024 (10 bit). Calibrated for 100 points per division.
Differential Accuracy	Graticule indication of time cursor difference is within 2% of LED readout value, measured over center eight divisions.	
SAVE Mode Gain Range (Horizontal)		Up to X100 as determined by the setting of the TIME/DIV switch.
Position Registration		Sweep start between NON STORE and Storage within ±0.2 division at TIME/DIV switch setting of 1 ms.
Display Response (Selectable) SINE		Microprocessor performs an interpolation between data points that is optimized to produce the best response for input signals that have no frequency components above Fs/2, when Fs is the sampling rate.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
STORAGE DISPLAY (cont)		
Display Response (Selectable) (cont) SINE (cont)		For a 6-division, sinusoidal input, digitized at 2.5 samples per input cycle and expanded 10X with the TIME/DIV switch, SINE Display Response envelope distortion produces a maximum amplitude error at any peak which is less than 5% of the ideally reconstructed reference p-p amplitude, assuming no distortion in the acquired input signal.
PULSE		Microprocessor performs linear interpolation between data points to optimize the display response for fast-rise and fast-fall waveforms (rise and fall times faster than 3 times the sampling interval). For a 6-division, sinusoidal input at seven samples per input cycle period, PULSE Display Response envelope distortion produces a maximum amplitude error at any peak which is less than 5% of the ideally reconstructed reference p-p amplitude.
Jitter Correction Gain		Reduces effect of sample clock-to-trigger jitter. 0.4 division, ±10%; X10 MAG on.
Resolution		±0.1 sample period for TIME/DIV switch settings of 20 μs to 5 s per division. ±3 ns for switch settings of 0.02 μs to 10 μs per division. **NOTE** *Due to inherent uncertainty involved in the jitter correction, the resolution will occasionally, an random intervals, exceed the limits given above.*
READOUT DISPLAY		
Display Type VOLTS Readout		Four-digit, seven-segment LED indicators. Displays calculated voltage difference between horizontal cursors in VOLTS measurement mode. Scale factor is determined by VOLTS/DIV switch setting.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
READOUT DISPLAY (cont)		
Display Type (cont) VOLTS Readout (cont) Resolution		1 part in 1024 (10 bit).
TIME Readout		Displays calculated time difference between cursor dots in TIME measurement mode. Scale factor determined by setting of the appropriate TIME/DIV switch (A or B).
Resolution		1 part in 1024 (10 bit). **NOTE** *Scale-factor LED indicates measurement is in DIV in the VOLTS measurement mode when vertical UNCAL LED is illuminated, or when different deflection factors are used in a dual-channel mode.*
CRT DISPLAY		
Display Area		8 X 10 cm.
Geometry		0.1 division or less of tilt or bowing.
Trace Rotation Range		Adequate to align trace with horizontal graticule lines. At least ±3°.
Standard Phosphor		P31 (green).
Nominal Accelerating Potential		18.5 kV.
Electrode Voltages to Ground Heater Voltage Between CRT Pins 1 and 14		6.3 Vrms, ±3 V; elevated to −2450 V.
Cathode (Pin 2)		−2450 V, ±2%.
Grid No. 1 (Pin 3)		≈ −2455 V to −2555 V.
Focus (Pin 4)		≈ −1780 V to −2000 V.
Astigmatism (Pin 5)		0 V to ≈ +95 V.
Isolation Shield (Pin 7)		+35 V, ±5 V.
First Anode (Pin 8)		≈ +55 V.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
CRT DISPLAY (cont)		
Electrode Voltages to Ground (cont)		
Geometry (Pin 10)		0 to ≈ +95 V.
Mesh (Pin 12)		≈ −150 V.
CALIBRATOR		
Output Voltage		
0°C to +40°C	0.3 V, within 1.0%	Within 0.5% at 25°C, ±5°C.
−15°C to +55°C		0.3 V, within 1.5%.
Repetition Rate	Approximately 1 kHz.	Within 25%.
Output Resistance		Approximately 10.3 Ω.
Output Current		
+20°C to +30°C	30 mA, within 2%.[a]	
−15°C to +55°C		30 mA, within 2.5%.
Z-AXIS INPUT		
Sensitivity	5 V p-p signal causes noticeable modulation at normal intensity.	Positive-going signal decreases intensity.
Usable Frequency Range	Dc to 50 MHz.[a]	
Input Resistance		25 kΩ, within 10%. Decreases to approximately 200 Ω at 2 MHz and above.
Maximum Input Voltage		25 V (dc + peak ac).
SIGNAL OUTPUTS		
CH 1 VERT SIGNAL OUT		
Output Voltage	At least 50 mV per division of displayed signal into 1 MΩ. At least 25 mV per division of displayed signal into 50 Ω.	
Output Resistance		Approximately 50 Ω.
Bandwidth	Dc to at least 50 MHz into 50 Ω.	
DC Level	Approximately 0 V.	Within 100 mV.

[a]Performance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements	Supplemental Information
SIGNAL OUTPUTS (cont)		
A and B + GATES		
Output Voltage	Approximately 5.5 V, positive-going rectangular pulse.	Starts at 0 V, within 500 mV.
Output Resistance		Approximately 500 Ω.
POWER SOURCE		
AC-Source Voltage Ranges		
115 V		
(High)	108 V to 132 V.[a]	
(Low)	90 V to 110 V.[a]	
230 V		
(High)	216 V to 250 V.[a]	
(Low)	198 V to 242 V.[a]	
AC-Source Frequency	48 Hz to 440 Hz.[a]	
Power Consumption		
Typical	115 watts (140 VA).[a]	
Maximum	150 watts (190 VA).[a]	48 Hz, 110 Vac, low regulating range.

Characteristics	Supplemental Information			
INTERNAL POWER SUPPLIES				
	Initial Setting	Any 500-Hour Period After First 200 Hours	Maximum p-p Ripple	Accuracy From −15°C to 55°C
Main Supply Accuracy (+20°C to +30° C)				
−8 V	±0.9%	±1.7%	2 mV	Within 0.5% of 25°C value
+5 V	±0.9%	±1.7%	2 mV	Within 0.5% of 25°C value
+15 V	±0.9%	±1.7%	2 mV	Within 0.5% of 25°C value
+55 V	±0.3%	±0.7%	4 mV	Within 0.5% of 25°C value
−2450 V	±1.2%	±2.2%		
+110 V	±3%		100 mV	

[a]Performance requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Supplemental Information			
INTERNAL POWER SUPPLIES (cont)				
Digital Storage Power Supplies (Not Adjustable)				
Voltage	−6 V	−12 V	+5 V	+12 V
Tolerance	±4%	±5%	±4%	±5%
Maximum p-p Ripple			150 mV	

Table 1-2

Environmental Characteristics

Characteristics	Description
	NOTE *All of the environmental tests performed meet the requirements of MIL-T-28800B,Class 3, Style D equipment.*
Temperature	
Nonoperating (Storage)	−62°C to +85°C.
Operating	−15°C to +55°C.
Altitude	
Nonoperating (Storage)	To 50,000 ft.
Operating	To 15,000 ft.
Humidity (Operating and Nonoperating)	5 cycles (120 hrs) referenced to MIL-T-28800B, Par. 3.9.2.2. Class 3, 95% to 97% relative humidity.
Vibration (Operating)	15 minutes along each of 3 major axes at a total displacement of 0.025 inch p-p (4 g's at 55 Hz), with frequency varied from 10 Hz to 55 Hz to 10 Hz in 1-minute sweeps. Hold 10 minutes at each major resonance, or if no major resonance present, hold 10 minutes at 55 Hz.
Shock (Operating and Nonoperating)	30 g's, half-sine, 11-ms duration, 3 shocks per axis in each direction, for a total of 18 shocks.
EMI	
Option 04 Only	*Meets TEKTRONIX Standard 062-2866-00 with exception of RE-02 specification being relaxed by 20 dB.*

Table 1-3

Physical Characteristics

Characteristics	Description
Weight	
With Panel Cover, Accessories, and Accessory Pouch	33 pounds (15 kg).
Without Panel Cover, Accessories, and Accessory Pouch	30 pounds (13.6 kg).
Domestic Shipping Weight	47 pounds (21.4 kg).
Height	
With Feet and Pouch	7.5 inches (19.0 cm).
Without Pouch	7.2 inches (18.3 cm).
Width	
With Handle	12.9 inches (32.8 cm).
Without Handle	11.5 inches (29.2 cm).
Depth	
Including Panel Cover	21.7 inches (55.1 cm).
Handle Extended	23.7 inches (60.2 cm).

Table 1-4

Option Electrical Characteristics

Characteristics	Performance Requirement	Supplemental Information
GENERAL PURPOSE INTERFACE BUS (GPIB) OPTION 02		
Interface Function[a]	SH1 Source Handshake. AH1 Acceptor Handshake. T1 Basic talker, talk only mode, serial poll. L0 No Listener. SR1 Service Request. RL0 No Remote/Local. PP0 No Parallel Poll. DC2 Device Clear. DT0 No Device Trigger. C0 No Controller.	
Waveform Data Transmitted[a]	Conforms to Tektronix Interface Standard, GPIB Codes and Formats (Rev. C).	When no waveform has been acquired, only the ID portion of the waveform message will be transmitted.
SIGNAL AVERAGING OPTION 12		
Averaging Range	Two to 256 waveforms in a 2-4-8 binary sequence. Number of sweeps to be averaged set with CURSOR/NO. OF SWEEPS control knob when NO. OF SWEEPS push button (on side panel) is pressed in.	Uncorrelated noise, signal-to-noise ratio is improved by the square root of the number of waveforms averaged.

[a]Performance requirement not checked in manual.

OPERATING INSTRUCTIONS

This section of the manual provides information on instrument installation and power requirements. The functions of controls, connectors, and indicators are described, and procedures intended to familiarize the operator with obtaining basic oscilloscope displays are included. For more complete operating information, refer to the 468 Operators Manual.

INSTALLATION

The 468 is shipped in its carton with its standard accessories (listed on the "Accessories" tab page at the end of Volume II of this manual). At installation time, save the shipping carton and packaging materials for repackaging. Refer to the "Maintenance" section of this manual for repackaging information.

PREPARATION FOR USE

NOTE

For instruments with Option 02 (GPIB), a firmware bug exists in both version 1.0 and version 2.0 ROM. This causes an incorrect transmission of the Y-multiplier and the Y-units of a waveform whenever the acquired waveform is vertically uncalibrated or when an ADD display is obtained with unequal VOLTS/DIV switch settings. To avoid this bug, rotate the VAR VOLTS/DIV controls into the detent position and use the same VOLTS/DIV switch setting on both channels for ADD displays when acquiring the data for transmission.

Safety Considerations

CAUTION

This instrument may be damaged if operated with either the Line Voltage Selector switch or the Regulating Range Selector switch set for the wrong applied ac-power input source voltage or if the wrong line fuse is installed.

Refer to the Safety Summary at the front of this manual for power source, grounding, and other safety considerations pertaining to the use of this instrument. Before applying power, verify that the Line Voltage Selector switch and the Regulating Range Selector switch are both set for the ac-power input voltage source available and that the proper line fuse is installed.

Line Voltage Selection

This instrument operates from either a 115-V or a 230-V nominal ac-power source with a line frequency from 48 Hz to 440 Hz. To convert the instrument for operation from one ac source to the other, disconnect the power cord from the power input source, and move the Line Voltage Selector (230/115) switch to the position indicating the available nominal voltage (see Figure 2-1). The detachable power cord may have to be changed to match the ac-power-source outlet. (See the "Power Cord" discussion in this manual for optional power cords.) Verify that the proper line fuse is installed (see Table 2-1).

Regulating Range Selection

The Regulating Range Selector (HIGH/LOW) switch is located on the right side panel near the Line Voltage Selector switch (Figure 2-1). Verify that the selector switch

Table 2-1

Fuse Selection

Line Voltage Selector Switch Position	Fuse Size
115 V Nominal	1.5 A, 3AG, Slow-blow
230 V Nominal	0.7 A, 3AG, Slow-blow

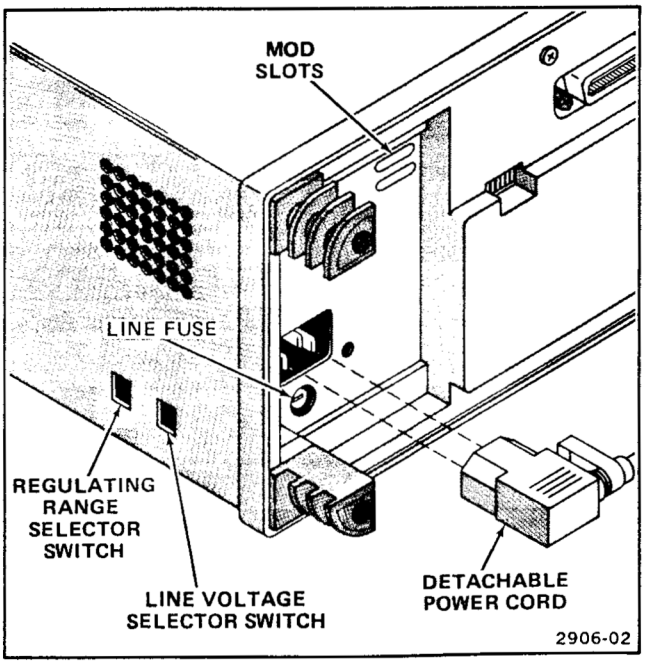


Figure 2-1. Ac-power-source switches, line fuse, and power cord.

is set for the average line voltage being used. See Table 2-2 for a listing of the regulating ranges.

To change the regulating range:

1. Disconnect the instrument from the ac-power source.

2. Select a range from Table 2-2 that corresponds to the average ac-power-source voltage available and set the selector switch to the required position.

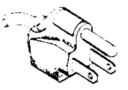
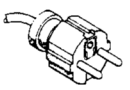
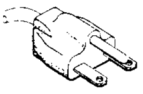
Table 2-2
Regulating Ranges

Regulating Range Selector Switch Position	Regulating Range	
	115 V Nominal	230 V Nominal
HIGH	108 V to 132 V	216 V to 250 V
LOW	90 V to 110 V	198 V to 242 V

Power Cord

This instrument has a detachable, three-wire power cord with a three-contact plug for connection to the power source and to protective ground. The plug protective ground contact connects (through the power cord protective grounding conductor) to the accessible metal parts of the equipment. For electrical-shock protection, insert this plug into a power source outlet that has a securely grounded protective-ground contact.

For the non-U.S. customer, the appropriate power cord used is supplied by an option specified when the instrument is ordered. The optional power cords available are illustrated in Figure 2-2. For part numbers, refer to "Replaceable Mechanical Parts" at the end of Volume II of this manual, or contact your Tektronix representative or local Tektronix Field Office.

Plug Configuration	Usage	Nominal Line-Voltage (AC)	Reference Standards	Option #
	North American 120V/ 15A	120V	ANSI C73.11[a] NEMA 5-15-P[b] IEC 83[c]	Standard
	Universal Euro 240V/ 10-16A	240V	CEE (7), II, IV, VII[d] IEC 83[c]	A1
	UK 240V/ 13A	240V	BS 1363[e] IEC 83[c]	A2
	Australian 240V/ 10A	240V	AS C112[f]	A3
	North American 240V/ 15A	240V	ANSI C73.20[a] NEMA 6-15-P[b] IEC 83[c]	A4

[a]ANSI—American National Standards Institute
[b]NEMA—National Electrical Manufacturer's Association
[c]IEC—International Electrotechnical Commission
[d]CEE—International Commission on Rules for the Approval of Electrical Equipment
[e]BS—British Standards Institution
[f]AS—Standards Association of Australia

2931-05

Figure 2-2. Optional power cords for the 468.

Power On Self-Verification

A limited self-test is performed by the digital storage circuitry whenever power is applied to the instrument. If all the self-tests are passed, the oscilloscope will operate. If the system, random-access memory (RAM) or read-only memory (ROM) fails the test, the instrument halts and will not operate.

As an aid to servicing, a failure code is displayed in the seven-segment, light-emitting diode (LED) indicators to help a service technician locate the area of failure. This error code will remain displayed in either the storage or nonstorage mode, and power may be applied with either mode selected.

NOTE

If power is applied while a storage mode is selected and while one of the measurement cursors (VOLTS or TIME) is also selected, a normal display may appear in the LED indicators (after the self-test is completed). To avoid possibly confusing a normal display with an error display, either release the CURSOR FUNCTION push buttons or select the NON STORE mode before applying power to the instrument.

Should an error indication appear in the display, ensure that the NON STORE push button is pressed, then restart the self test by cycling the POWER switch off, then on again. If the error display appears a second time, refer the instrument to qualified service personnel.

Instrument Cooling

To maintain adequate instrument cooling, the ventilation holes in the equipment cabinet must remain open, and the air filter must be clean. The air filter should be visually checked every few weeks and cleaned or replaced if dirty. More frequent inspections are required under severe operating conditions.

CONTROLS, CONNECTORS AND INDICATORS

VERTICAL

Refer to Figure 2-3 for location of items 1 through 11.

(1) **VOLTS/DIV Switches**—Select the vertical deflection factor from 5 mV per division to 5 V per division in 10 steps for Channel 1 and Channel 2 in a 1-2-5 sequence. Three additional switch positions (0.5 mV, 1 mV, and 2 mV) are used in storage modes to vertically expand the waveform acquired at 5 mV per division (up to 10 times). VAR control must be in the calibrated detent to obtain a calibrated deflection factor. These switches also set the scale factor of the digital storage VOLTS measurement LED readout.

When a stored waveform is displayed in the SAVE Storage mode, the VOLTS/DIV switch vertically expands the appropriate channel display up to 10 times in a 1-2-5 sequence. Waveforms acquired in NORM and ENVELOPE Storage modes at VOLTS/DIV settings of 2, 1, or 0.5 mV per division, may be reduced back to 5 mV per division deflection if desired.

NOTE

In firmware version 1.0, SAVE Storage Mode waveforms acquired at VOLTS/DIV attenuator settings of 5 mV per division, and higher, cannot be reduced below the deflection sensitivity at which they were acquired. An attempt to do so will cause an invalid VOLTS readout on the LED indicators.

In instruments factory equipped or converted to firmware version 2.0 or higher, attempting to reduce the display below the limits at which it was acquired will cause the display to cease reducing and the VOLTS readout to change to DIV scale factor. Attempting to expand the display beyond the instruments limits causes the display and the VOLTS readout scale factor to cease changing.

(2) **VOLTS/DIV Readouts**—Consist of two light-emitting diodes (LED) for each channel, located beneath the skirt of each VOLTS/DIV knob. Either one LED or the other will light to indicate the correct deflection factor (if the channel is active). The 10X LED is illuminated only when a 10X probe with a scale-factor-coding-ring contact is connected to the input of the oscilloscope; otherwise, the 1X LED is illuminated. In the 0.5-, 1-, and 2-mV positions of the VOLTS/DIV switch, the LED will not be illuminated for the NON STORE mode.

(3) **VAR Control**—Provides variable uncalibrated deflection factors between the calibrated settings of the VOLTS/DIV switches when storage is off. In a storage mode, if the VAR control is out of the calibrated detent, digitial storage circuitry will continue to acquire data; but the storage scale-factor LED will indicate that VOLTS function measurements are in divisions (DIV).

(4) **UNCAL Indicator**—A LED that is illuminated when the VAR VOLTS/DIV control is out of the calibrated detent. It indicates that the vertical deflection factor is uncalibrated.

(5) **POSITION Controls**—Control the vertical position of the channel displays on the crt both in storage and nonstorage modes. In the X-Y mode, the Channel 2 POSITION control adjusts the vertical positioning of the display.

(6) **CH 1 OR X and CH 2 OR Y Input Connectors**—Provide for application of external signals to the input of the vertical amplifiers. In the X-Y mode (A TIME/DIV switch set to X-Y), the signal applied to the CH 1 OR X connector provides horizontal deflection (X-axis), and the signal applied to the CH 2 OR Y connector provides vertical deflection (Y-axis).

These connectors each include a coding ring that activates the scale-factor-switching circuitry whenever a 10X scale-factor-switching probe is connected.

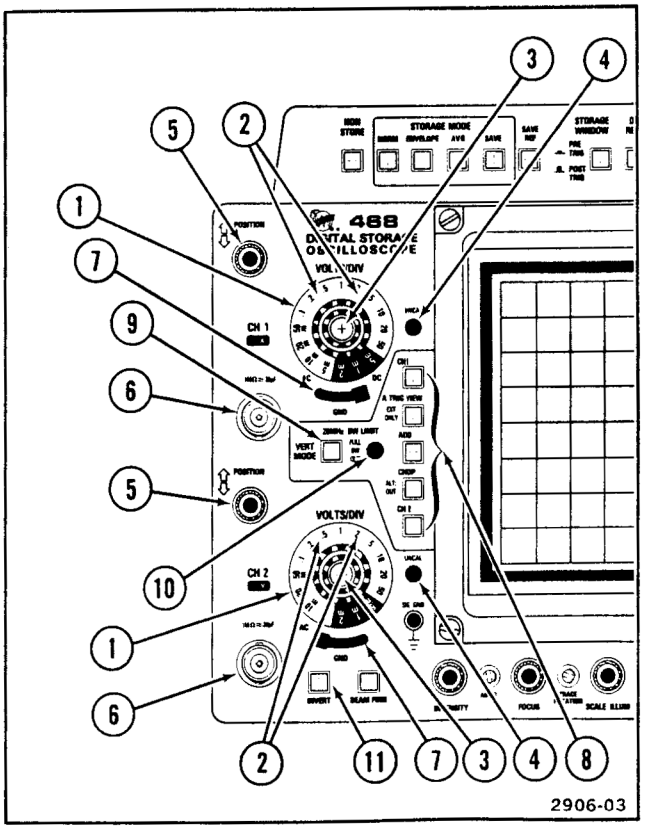


Figure 2-3. Vertical controls, connectors, and indicators.

(7) **Input Coupling Switches (AC-GND-DC)**—Select the method of coupling the input signal to the vertical deflection system.

AC position—Signals are capacitively coupled to the vertical deflection system. The dc component of the input signal is blocked.

DC position—All frequency components of the input signal are passed to the vertical input amplifier.

GND position—The input of the vertical amplifier is grounded to provide a ground reference and to allow the input coupling capacitor to be precharged to the input signal dc level through a high resistance connected to ground.

When operating in the NORM, ENVELOPE, or AVG Storage Mode, the ground reference is stored in the GND position and displayed as an intensified dot at the left edge of the graticule when the input coupling is switched to AC or DC. In ADD vertical mode, both CH 1 and CH 2 Input Coupling switches must be set to GND to store a ground reference.

In instruments equipped with firmware version 1.0, at the end of the power-on routine a random ground dot may be displayed. Switching the input coupling switch to GND will place the dot at a valid ground reference.

NOTE

If the Vertical POSITION control is adjusted after the ground reference is stored, the dot position is no longer a valid ground reference. Additionally, in firmware version 1.0, vertically expanding either waveform of a dual-channel storage display using the 2 mV, 1 mV, or 0.5 mV VOLTS/DIV switch position will cause an invalid ground dot display. A single-channel display ground dot remains valid during expansion.

In instruments factory equipped or converted to firmware version 2.0 or higher, the ground dot position remains valid as display vertical expansion occurs in a dual-channel display.

(8) **VERT MODE Switches**—Five push-push switches, used to select the vertical mode of operation in both storage and nonstorage modes. The oscilloscope can display any combination of CH 1, CH 2, ADD, and A TRIG VIEW (external trigger only) in either Chopped (CHOP) or Alternate (ALT) mode, when NON STORE is selected. The A TRIG VIEW mode is not functional in storage modes. If A TRIG VIEW is the only vertical mode selected or no vertical mode is selected when a storage mode push button is pressed in, the digital storage will continue to acquire and display the Channel 1 input signal, but all the probe coding LED (X1 and X10) are extinguished. The NON STORE display, with no vertical mode selected, will be a single, unpositionable baseline trace with no vertical deflection.

CH 1—Selects Channel 1 input signal for display or storage when push button is pressed in. To end the NON STORE display of the Channel 1 input signal, push CH 1 VERT MODE button to release it (Channel 1 remains selected in a storage mode if ADD or CH 2 vertical mode is not selected).

A TRIG VIEW—Displays the signal applied to the A External Trigger input connector when push button is pressed in, if the A TRIGGER SOURCE switch is set to either EXT or EXT/10. Remove the A External Trigger View trace from the display by pressing the A TRIG VIEW VERT MODE button to release it. The A TRIG VIEW display cannot be selected in any storage mode.

CH 2—Selects the Channel 2 input signal for display or storage when push button is pressed in. To end the display of the Channel 2 input signal, push CH 2 VERT MODE button to release it.

ADD—Selects the algebraic sum of Channel 1 and Channel 2 input signals to be displayed or stored when push button is pressed in. To end the display of the ADD signal, push the ADD VERT MODE button to release it.

CHOP-ALT:OUT (Nonstorage Mode)—When CHOP is selected (switch pressed in), the oscilloscope Vertical Switching circuitry is switched between two or more of the selected vertical modes at approximately a 500-kHz rate.

When ALT is selected (switch released out), the oscilloscope Vertical Switching circuitry is alternately switched between two or more of the selected vertical modes at the end of each sweep.

CHOP-ALT:OUT (Storage Mode)—When pressed in (CHOP) with the NORM Storage mode selected, the digital storage circuitry interleaves the Channel 1 and Channel 2 input signals into memory. Each channel is chopped to obtain 256 samples of each input signal. The storage chop rate is one half of the sampling rate of the selected sweep speed.

NOTE

For firmware versions 1.0 and 2.0, a horizontal displacement of the displayed signal occurs between ALT and CHOP dual-channel acquisition. The displacement increases from approximately 0.1 division to approximately 1 division as the TIME/DIV switch setting is changed from 1 μs to 0.02 μs per division.

When either the ENVELOPE or AVG Storage mode is selected, the position of the CHOP-ALT: OUT switch has no effect on the storage; and Channel 1 and Channel 2 are alternately sampled to obtain 512 samples of each input signal.

When released out (ALT) with the NORM Storage mode selected, Channel 1 and Channel 2 are alternately sampled to obtain 512 samples of each input signal. However, if ADD Vertical mode is also selected, the ADD waveform is sampled 512 times alternately and Channel 1 and Channel 2 are chopped (256 samples each).

NOTE

CHOP and ALT functions are disabled if only one VERT MODE push button—CH 1, CH 2, ADD, or A TRIG VIEW (nonstorage only) is selected—or if X-Y mode is selected.

(9) **20 MHz BW LIMIT (FULL BANDWIDTH OUT) Switch**—Limits the bandwidth of the vertical preamplifier to approximately 20 MHz when pressed in. Push button must be pressed a second time to release it and regain full 100-MHz bandwidth operation. This control has no affect on the digital storage signal acquisition even though the BW LIMIT LED may be illuminated.

(10) **20 MHz BW LIMIT Indicator**—A LED that is illuminated to indicate that the bandwidth is limited to 20 MHz whenever the 20 MHz BW LIMIT push button is pressed in.

(11) **INVERT**—Inverts Channel 2 display when push button is pressed in. Push button must be pressed a second time to release the button and return to a noninverted display of Channel 2.

DISPLAY AND CALIBRATOR

Refer to Figure 2-4 for location of items 12 through 19.

(12) **Internal Graticule**—Eliminates parallax. Rise time amplitude measurement points are indicated at the left edge of the graticule.

(13) **BEAM FIND Switch**—When held in, the display is compressed to within the graticule area and a visible viewing intensity is provided to aid in locating off-screen displays.

(14) **INTENSITY Control**—Determines the brightness of the crt display (has no effect when BEAM FIND switch is pressed in).

(15) **FOCUS Control**—Adjusts for optimum display definition.

(16) **CALIBRATOR Loop**—A combination 30-mA current loop and 0.3-V square-wave voltage output (at approximately 1 kHz) that permits the operator to compensate voltage and current probes and to check oscilloscope vertical operation. It is not intended to verify precise time-base calibration.

(17) **SCALE ILLUM Control**—Adjusts graticule illumination.

(18) **ASTIG Control**—Screwdriver control used in conjunction with the FOCUS control to obtain a well-defined display. It does not require readjustment during normal use of the instrument.

(19) **TRACE ROTATION Control**—Screwdriver control used to align a baseline trace with the horizontal graticule lines.

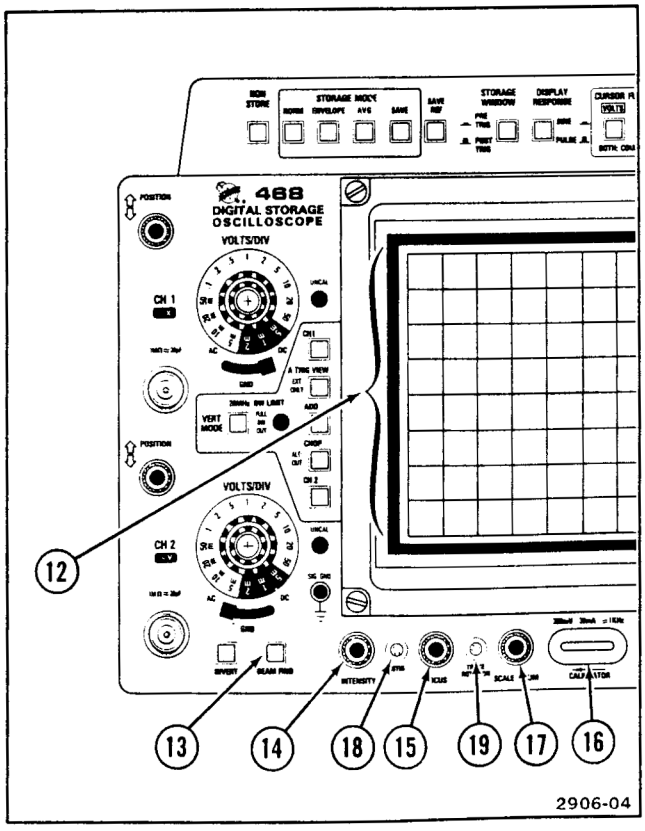


Figure 2-4. Display controls and CALIBRATOR.

TRIGGERING
(both A and B if applicable)

Refer to Figure 2-5 for location of items 20 through 28.

(20) **TRIG MODE Switches**—Three push-button switches that determine the mode of trigger operation for the instrument.

AUTO—Permits triggering on waveforms with a repetition rate of about 20 Hz or greater. Sweep free runs and provides a bright baseline when either an adequate trigger signal is absent, or if the repetition rate of the trigger signal is below 20 Hz. In a storage mode, the digital storage circuitry will acquire data from the selected time window and display the acquired data.

NORM—Sweep is initiated, or storage acquires data when an adequate trigger signal is applied. NORM Trigger Mode may be used to obtain stored waveforms to ensure that the time window the waveform is acquired from is synchronized with the triggering signal.

SINGL SWP—Sweep is initiated one time (or one time window of data is stored) when an adequate trigger signal is applied. Sweep cannot be initiated again (or a new time window of data cannot be stored) until the sweep logic is reset by pressing the SINGL SWP push button. Stored data from the single time window will remain displayed on the crt.

Any front-panel control change that affects the data acquisition (VOLTS/DIV, VERT MODE, SEC/DIV, HORIZ MODE, etc.,) requires that the SINGL SWP push button be pressed again to obtain a valid display that agrees with the control setting. When storing displays that require two time windows to acquire, the SINGL-SWP push button must be pressed twice to obtain a valid display. If a valid display is not completed after a change affecting the acquisition timing, the TIME dot readout may switch between two different numbers at various settings of the SEC/DIV switch.

NOTE

Applying power to the instrument with either NORM or SINGL SWP Trigger Mode selected without a trigger signal present to acquire a waveform, will cause a dashed line to be displayed in any storage mode. The dashed line will be replaced by an acquired waveform when the instruments is adequately triggered.

In firmware version 1.0 instruments, the first SINGL SWP trigger received after Power on or after a control change that affects the data being acquired is not considered valid. In either case, the SINGL SWP must be reset and a second trigger received before a waveform is stored and displayed. For instruments equipped with firmware version 2.0 and higher, the first SINGL SWP trigger received is valid and a waveform will be stored and displayed.

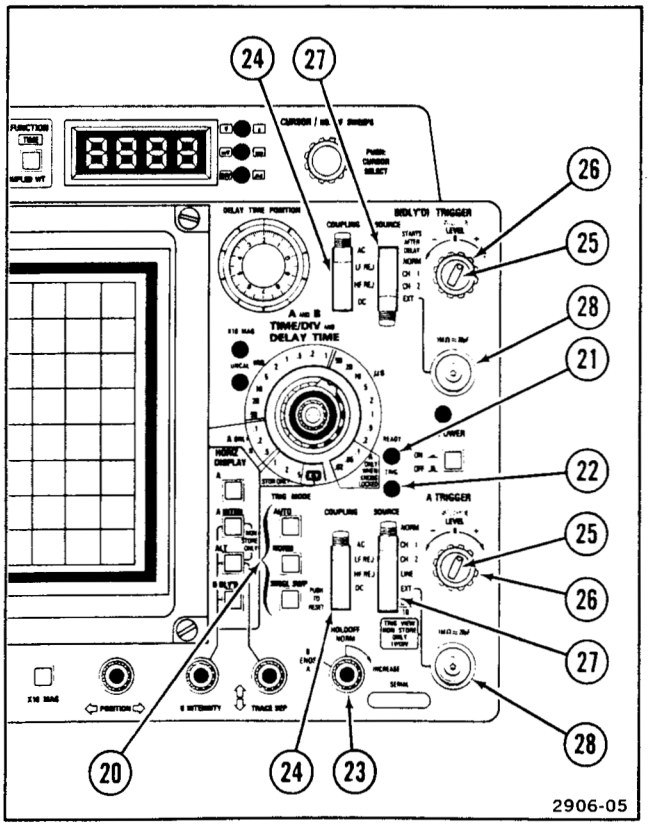


Figure 2-5. Trigger controls, connectors, and indicators.

(21) **READY Indicator LED**—Illuminates in the single-sweep mode to indicate that the sweep circuitry is armed and ready to initiate the sweep when a trigger signal occurs.

(22) **TRIG Indicator LED**—Illuminates to indicate the A Sweep is triggered.

(23) **A TRIG HOLDOFF Control**—Provides continuous control of holdoff time between sweeps. Allows triggering on aperiodic signals (such as complex digital words). In the fully clockwise position (B ENDS A), the A Sweep is automatically terminated at the end of the B Sweep to provide the fastest possible sweep repetition rate for delayed-sweep presentations and low-repetition-rate signals. In the NON STORE mode, holdoff time is variable to approximately ten times NORM holdoff time. Use the A trigger controls to obtain as stable a display as possible before setting the A TRIG HOLDOFF control to a position other than NORM.

The variable holdoff capability is reduced in the storage modes due to the added digital holdoff time required for signal acquisition by the microprocessor.

(24) **COUPLING Switch**—Determines method used to couple a signal to the input of the trigger generator circuit.

AC—Signals are capacitively coupled to the input of the trigger circuit. The dc component is rejected, and signals below approximately 30 Hz are attenuated. Triggering is allowed only on the ac portion of the vertical signal.

LF REJ—Signals are capacitively coupled to the input of the trigger circuits. The dc component is rejected, and signals below approximately 50 kHz are attenuated. This position is useful for providing a stable display of the high-frequency components of a complex waveform.

HF REJ—Signals are capacitively coupled to the input of the trigger circuit. The dc component is rejected, and signals below approximately 30 Hz and above approximately 50 kHz are attenuated. This position is useful for providing a stable display of the low-frequency components of a complex waveform.

DC—All frequency components of a trigger signal are coupled to the input of the trigger circuit. This position is useful for providing a stable display of low-frequency or low-repetition-rate signals.

(25) **SLOPE Switch**—Selects the slope of the signal that triggers the sweep.

+ (plus)—Sweep can be triggered from the positive-going portion of a trigger signal.

– (minus)—Sweep can be triggered from the negative-going portion of a trigger signal.

(26) **LEVEL Control**—Selects the amplitude point on the trigger signal at which the sweep is triggered. This control is usually adjusted for the desired display after the Trigger SOURCE, COUPLING, and SLOPE have been selected.

(27) **SOURCE Switch**—Selects the source of the trigger signal coupled to the input of the trigger circuit.

NORM—The waveform displayed on the crt is the source of a composite trigger signal. Stable triggering of non-time-related signals usually can be obtained by setting VERT MODE to ALT, SOURCE to NORM, COUPLING to LF REJ (high-frequency signals only), and adjusting the Trigger LEVEL control for a stable display. Time relationship between the Channel 1 signal and the Channel 2 signal is not indicated by the display.

CH 1—The signal applied to the CH 1 input connector is the source of the trigger signal. Channel 2 signal display is unstable if it is not time related to the Channel 1 signal.

CH 2—The signal applied to the CH 2 input connector is the source of the trigger signal. The Channel 1 signal display is unstable if it is not time related to the Channel 2 signal.

LINE (in the A Sweep Trigger circuity only)—The ac-power-source waveform is the source of the trigger signal. This position is useful when the input signal is time related (multiple or sub-multiple) to the frequency of the ac-power source or when it is desirable to provide a stable display of a power-source frequency component in a complex waveform.

EXT—The signal connected to the External Trigger Input connector is used for triggering. External signals must be time related to the displayed signal for a stable display. This position is useful when the internal signal is either too small or contains undesired components that cause unstable triggering. The external trigger signal may be viewed by pushing the A TRIG VIEW button in only when the 468 is operating in the NON STORE mode. The A TRIG VIEW display is not selectable in any storage mode.

EXT/10 (in the A Sweep Trigger circuit only)—External trigger signal is attenuated by a factor of 10.

STARTS AFTER DELAY (in the B Sweep Trigger circuit only)—B Sweep starts immediately after the delay time selected by the DELAY TIME POSITION control. In this position, the B Sweep is independent of the B trigger signal. When making differential time measurements with the 468 in the NON STORE Mode, this position of B Trigger SOURCE switch must be selected for valid measurements.

(28) **External Trigger Input Connectors**—Provide for application of external triggering signals to the A TRIGGER and B (DLY'D) TRIGGER circuits, when either EXT or EXT/10 (A Trigger only) SOURCE is selected.

HORIZONTAL AND POWER

Refer to Figure 2-6 for location of items 29 through 35.

(29) **A and B TIME/DIV Switches**—Select the calibrated sweep rates in the nonstorage mode and the time window for the storage modes.

Nonstorage Mode—The A TIME/DIV switch selects 23 calibrated sweep rates and delay times from 0.5 s to 0.02 μs per division in a 1-2-5 sequence. Extreme counterclockwise position of the switch selects the X-Y horizontal display.

The B TIME/DIV switch selects calibrated sweep rates from 50 ms to 0.02 μs per division in a 1-2-5 sequence.

Storage Mode—The A or B TIME/DIV switch selects the time window to be acquired (10 divisions multiplied by the TIME/DIV switch setting) for TIME/DIV switch settings between 0.02 μs and 5 s per division. Sampling of the analog input signal is done 512 times during one full sweep time (50 in 1 division). Rate of sampling is calculated by dividing the number of samples in 1 division by the sweep time for 1 division:

$$\text{Sample rate} = \frac{\text{50 samples}}{\text{TIME/DIV}}$$

For TIME/DIV switch settings from 1 μs per division to 0.02 μs per division, a waveform is sampled at the 2 μs per division rate and expanded horizontally, using a combination of digital interpolation and analog gain, to the correct horizontal scale.

The A TIME/DIV switch selects the time for A and A INTEN Horizontal Displays, and the B TIME/DIV switch selects the time for ALT and B DLY'D Horizontal Displays. The 1, 2, and 5 s per division positions of the A TIME/DIV switch are used in the storage modes only. The X-Y position of the A TIME/DIV switch is not used in any storage mode.

The SAVE display of a stored waveform acquired at 2 μs per division and slower may be expanded up to 100 times using the next six faster positions of the TIME/DIV switch associated with the selected Horizontal Display Mode. Waveforms acquired at 1 μs per division and faster are expanded by each of the remaining faster positions of the TIME/DIV switch. Additionally, waveforms acquired at 1 μs per division and faster may be reduced back to the 2 μs per division sweep rate in the steps of the TIME/DIV switch.

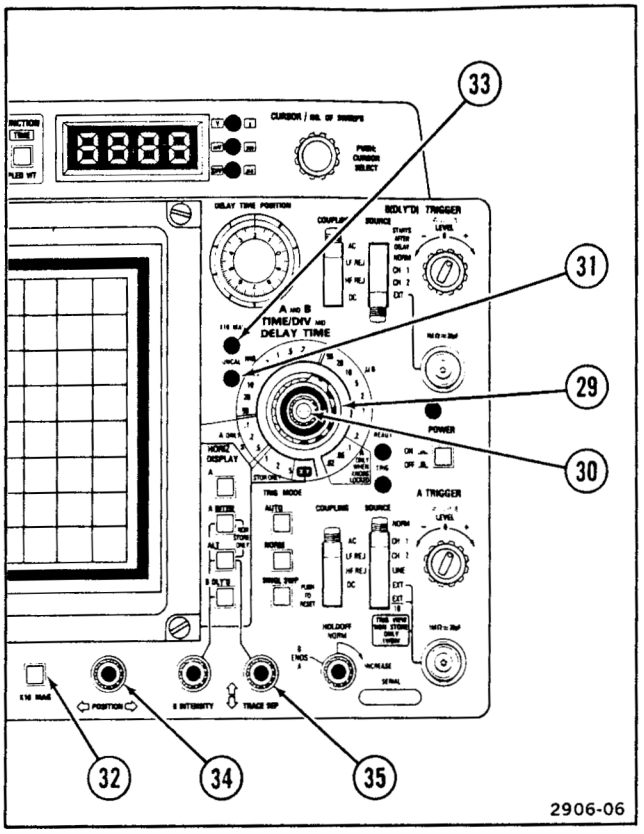


Figure 2-6. Sweep rate and position controls and indicators.

(30) **A Sweep VAR Control**—Provides continuously variable uncalibrated A Sweep rates to at least 2.5 times the calibrated setting (extends slowest NON STORE sweep rate to at least 1.25 s per division). This control is effective only in the NON STORE mode.

(31) **UNCAL Indicator LED**—Illuminates to indicate that the A time base sweep rate is uncalibrated (VAR control is out of calibrated detent).

In the storage modes the VAR control is ignored, and the UNCAL LED is not illuminated when the VAR control is out of calibrated detent. The storage time base is obtained from the setting of the TIME/DIV switch associated with the selected Horizontal Display mode.

(32) **X10 MAG Switch**—When pressed in, increases the displayed sweep rate by a factor of 10. Extends the fastest sweep rate to 2 ns per division. The magnified sweep expands the center division of the unmagnified display (0.5 division either side of the center vertical graticule line).

(33) **X10 MAG Indicator LED**—Illuminates when the X10 MAG push button is in to indicate that the horizontal display is magnified.

(34) **POSITION Control**—Positions the display horizontally for both nonstorage and storage modes. Provides both coarse and fine control action. Reverse the direction of rotation to actuate fine positioning action.

(35) **TRACE SEP Control**—Positions the B Sweep vertically when the ALT horizontal display mode is selected. TRACE SEP has no effect on the stored display.

Refer to Figure 2-7 for location of items 36 through 40.

(36) **B INTENSITY Control**—Controls the intensity of the B trace and interacts with INTENSITY control. The B INTENSITY control has no effect when a storage mode is selected.

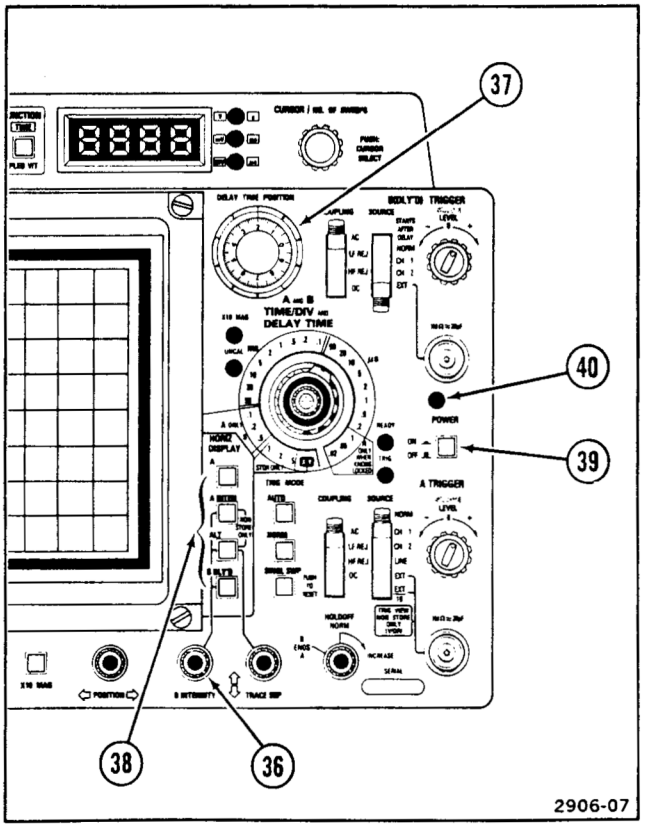


Figure 2-7. Horizontal display, B INTENSITY, DELAY TIME POSITION, and power controls and indicator.

(37) **DELAY TIME POSITION Control**—Selects the amount of delay time between the start of the A Sweep and start of the B Sweep. Delay time is variable to at least 10 times the A TIME/DIV switch setting. This control is used in conjunction with the STARTS AFTER DELAY position of the B TRIGGER SOURCE switch.

(38) **HORIZ DISPLAY Switches**—Select the mode of operation for the horizontal deflection system.

A—Displays only the A Sweep. The digital storage time base and the horizontal deflection rate are determined by the setting of the A TIME/DIV switch.

A INTEN—Displays the A Sweep at a rate determined by the setting of the A TIME/DIV switch. An intensified portion corresponding to the length and position of the B Sweep will appear on the trace when the B Sweep is properly triggered. The INTENSITY and B INTENSITY controls should be adjusted to obtain the proper brightness for viewing. The intensified zone is used to position the B Sweep (delayed) to the desired location within the A Sweep interval to obtain an expanded view of a waveform for examination.

The digital storage time base is determined by the setting of the A TIME/DIV switch in the A INTEN Horizontal Display mode.

ALT—Alternates the display between the A INTEN and B DLY'D sweeps. The TRACE SEP control will position the B display vertically. In the nonstorage mode, the B INTENSITY control will adjust the intensity of the B Sweep whenever it is displayed. The digital storage circuitry time base is determined by the setting of the B TIME/DIV switch.

B DLY'D—Displays only the B Sweep. The B Sweep rate is determined by the setting of the B TIME/DIV switch, and the delay time is determined by both the A TIME/DIV switch and the DELAY TIME POSITION control. The digital storage circuitry time base is determined by the setting of the B TIME/DIV switch.

(39) **POWER Switch**—A push-push switch used to turn instrument power on and off. It must be pushed in to apply power to the instrument and pushed in again to release the switch and remove power from the instrument.

(40) **Power On Indicator LED**—Illuminates when power is applied to the instrument and POWER switch is set to the "on" (in) position.

DIGITAL STORAGE

Refer to Figure 2-8 for location of items 41 through 49.

(41) **NON STORE Switch**—Selects operation as a conventional oscilloscope. Any data stored in the 468 digital storage memory remains unchanged while NON STORE is selected. The last acquired waveform data may be transmitted via the optional IEEE-488 GPIB interface during NON STORE. While transmitting, the 468 switches to the SAVE Storage Mode to display the waveform being transmitted. At the completion of a transmission the oscilloscope returns to the selected operation. The AVG waveform data cannot be transmitted from the NON STORE Mode unless a completed waveform was saved prior to selecting NON STORE. Switching directly from AVG to NON STORE will abort the AVG acquisition cycle in progress, and an attempt to transmit will result in sending only the instrument ID.

(41A) **STORAGE MODE Switches**—Select storage mode operation. Selection of a switch cancels the remaining switches.

NORM (Normal)—In this mode, the 468 digitizes, stores, and displays data from Channel 1 and Channel 2 at the vertical gain and horizontal sweep speed determined by the oscilloscope front-panel Vertical and Horizontal controls. If the oscilloscope TRIG MODE is SINGL SWP, data will be acquired for that sweep and displayed. If the TRIG MODE is AUTO or NORM, data will be repetitively acquired and displayed.

ENVELOPE—The ENVELOPE mode is a repetitive mode that acquires a selected number of sweeps and displays the resultant waveform envelope. Each data point of the input waveform is compared to the maximum and minimum values of the same data point accumulated from previous sweeps. If the data point is greater than the previous maximum or less than the previous minimum for that data point, the previous data point is replaced by the new data point. If the data point does not meet one of the conditions mentioned, it is discarded.

The ENVELOPE accumulation cycle is restarted whenever any of the following events occurs: the ENVELOPE push button is pressed in, the selected number of sweeps to be accumulated is changed, or any of the front-panel controls affecting the data being acquired is changed (VERT MODE, VOLTS/DIV, STORAGE WINDOW, TIME/DIV, HORIZ DISPLAY, or VAR in and out of detent). A new cycle is also started upon completion of the current cycle.

At TIME/DIV switch settings slower than 20 μs per division, the analog input will be sampled every 200 ns. Only the maximum and minimum values over every data point time interval (4% of the TIME/DIV switch setting) are stored in the digital storage memory.

The number of waveforms to be accumulated to develop the display is selectable in a binary sequence of (1, 2, 4, ...) up to 256 sweeps. Press in the NO. OF SWEEPS push button and use the CURSOR/NO. OF SWEEPS control to obtain a new number of sweeps to be accumulated (number is displayed on the LED indicators). An unlimited number of sweeps may also be selected (LED display is 9999), and the digital storage memory will repetitively acquire data until either a new "number of sweeps" selection is made or a control setting is changed to restart the accumulation of data. The NO. OF SWEEPS push button must be pressed again to release it and return the readout to cursor control. During the first ENVELOPE cycle, the readout will count down

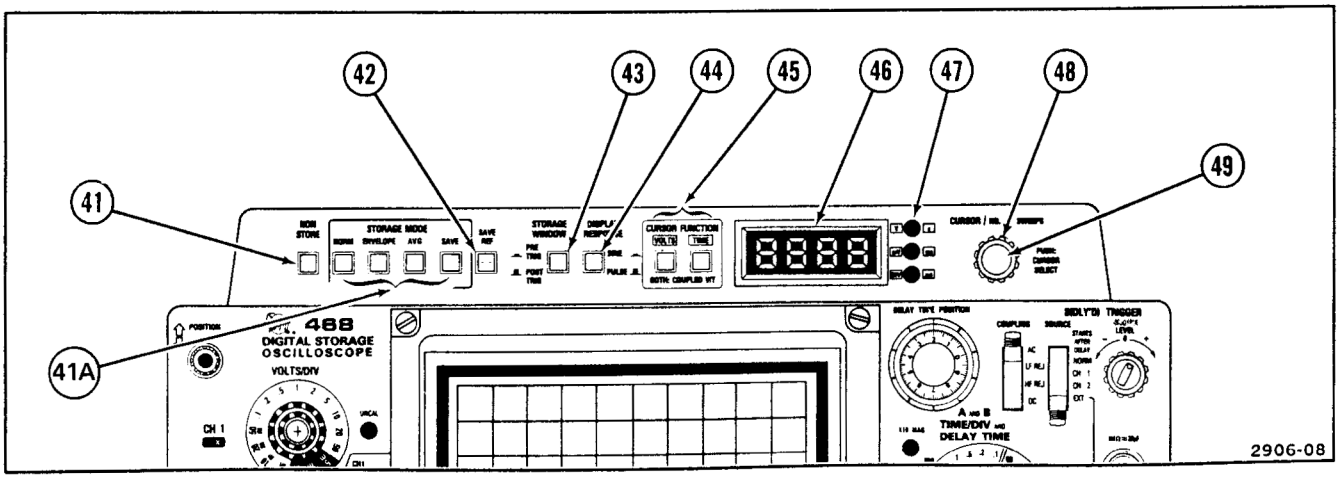


Figure 2-8. Digital storage controls and indicators.

the sweeps as they are being acquired. Thereafter, the readout returns to cursor control. The readout will not count down when an unlimited number of sweeps is selected.

At power on, the number of sweeps to be accumulated is automatically set to 32.

AVG (Average) (Option SN B032429 & Below) —When equipped with this option, the 468 will average the input signal for a selected number of sweeps and display the accumulated waveform. The number of sweeps to be averaged may be altered (from the power on number of 32) by pressing the NO. OF SWEEPS push button to display the number and adjusting the CURSOR/NO. OF SWEEPS control to obtain a new number from 2 to 256 in a binary sequence. The NO. OF SWEEPS push button must be pressed again to release it and return the readout to cursor control. Upon releasing the NO. OF SWEEPS push button, the readout will count down the sweeps as they are being acquired during the first average cycle only. Thereafter, the readout returns to cursor control.

The AVG accumulation cycle is restarted whenever the AVG push button is pressed in, whenever the selected number of sweeps is changed, or if any of the front-panel controls affecting the data being acquired is changed (VERT MODE, VOLT/DIV, TIME/DIV, STORAGE WINDOW, HORIZ DISPLAY, or VOLTS/DIV VAR in and out of detent).

After a control setting change, and before an AVG acquisition is completed that reflects the new control setting, a dashed line will be displayed. The dashed line will be replaced by the AVG waveform upon completion of the current cycle, and a new acquisition cycle will begin. A SAVE REF waveform will remain displayed as acquired during any control setting changes.

SAVE—Pressing the SAVE push button in when NORM Storage Mode is selected will stop acquisition of data, and the displayed waveform will be saved. When either ENVELOPE or AVG Storage Mode is selected, the acquisition cycle in progress will be completed, and the new waveform will be saved. A cycle is defined as the selected number of sweeps in the ENVELOPE and AVG Storage Modes. In the ENVELOPE Storage Mode, if the number of sweeps selected is set to 9999, pressing the SAVE push button will switch the digital storage to the SAVE Storage Mode at the end of the current sweep.

If a dual-trace display is in use, the action that occurs before entering the SAVE Storage Mode after the SAVE button is pressed differs for ENVELOPE and AVG Storage Modes. Since the ENVELOPE display is updated with each sweep alternately, both waveforms will complete the selected number of sweep acquisitions before the SAVE Storage Mode is entered. The AVG display must complete the cycle, acquiring all the sweeps selected for a trace, before that trace is updated. Therefore, for the AVG display, only the waveform being acquired at the time the SAVE button is pressed in will be completed before entering the SAVE Storage Mode.

NOTE

In the event that the storage modes are selected in the following order; AVG, NON STORE, then back to SAVE: the SAVE display will not be valid and a dashed line will be displayed. Switching from NON STORE to SAVE will display the last waveform acquired in either NORM or ENVELOPE Storage Mode.

Additionally, in firmware version 1.0, changing the number of sweeps to be averaged in a dual-channel storage display and then switching to SAVE Storage Mode before the waveform has been acquired at least one time at the new NO. OF SWEEPS setting will prevent a valid expansion (both vertical and horizontal) of one of the waveforms. Instruments equipped with firmware version 2.0 or higher will display the valid acquired waveform only, and the display can be expanded normally.

(42) **SAVE REF**—Pressing in the SAVE REF push button will save one waveform for the purpose of comparing it with waveforms stored later. If more than one VERT MODE is selected, the waveform stored as a reference is in the following priority: ADD, CH 1, then CH 2. If a chopped display of CH 1 and CH 2 is selected, then both traces will be saved as a reference; but if ADD Vertical mode is selected as well, the ADD display will be saved as a reference. See Table 2-3 in "Digital Storage Displays" for a complete listing of references saved and displays available with various selections of Vertical and Storage modes. The number of VERT MODE selections that may be simultaneously displayed is reduced while the SAVE REF display is selected.

NOTE

If power is applied in a storage mode with the SAVE REF push button pressed in, a residual waveform from the power-on self test will remain displayed. Remove the residual waveform by pressing the SAVE REF push button to release it.

Additionally, in firmware version 1.0 when powering on with the TIME/DIV switch set slower than 2 μs per division, a TIME cursors readout will oscillate. Again, release the SAVE REF push button to eliminate the condition.

Selecting SAVE REF when a chopped dual-channel acquisition is being made, causes the Channel 2, X1 and X10 probe coding LED to be extinguished. The SAVE REF push button must be released to reilluminate them.

In instruments equipped with firmware version 2.0 or higher, both the TIME cursor readout oscillation and the Channel 2 probe-coding LED operation anomalies do not exist.

(43) **STORAGE WINDOW (PRE TRIG or POST TRIG)**—Selects pretrigger or post-trigger storage of data. When pressed in (pretrigger), approximately 8.75 divisions of the waveform are stored before the trigger event. When out (post-trigger), approximately 1.25 divisions of the waveform are stored before the trigger event.

(44) **DISPLAY RESPONSE (SINE or PULSE)**—Controls the interpolation applied to the displayed data at TIME/DIV switch settings from 1 μs per division to 0.02 μs per division only. When pressed in (SINE), interpolation is applied that optimizes the display accuracy for waveforms containing no frequency components above half of the sampling rate. When out (PULSE), linear interpolation is applied to optimize the display accuracy for fast-rise and fast-fall waveforms (rise time or fall time faster than three times the sampling interval) and to eliminate overshoot. The SINE and PULSE Display Response will affect the SAVE Storage mode display. Switching from one to the other will change the interpolation method applied to the displayed waveform.

(45) **CURSOR FUNCTION**—Two push-push switches used to select the cursors (VOLTS or TIME) to be displayed on the crt. Cursors are used to select measurement points on the displayed waveform. Voltage and time differences between the cursors are displayed on the four-digit, seven-segment LED indicators.

VOLTS—When pressed in, cursors displayed consist of two horizontal lines that may be positioned vertically to any location on the crt. The cursor selected to be active is dashed. LED indicators display the voltage difference (represented by the cursor positions) based on the VOLTS/DIV setting of the channel used to obtain the stored waveform. If the VAR control is out of the calibrated detent during acquisition of the signal, the scale factor LED will indicate that the measurement is in divisions rather than voltage units. Press the push button again to release it and remove the VOLTS cursors from the display.

TIME—When pressed in, the displayed cursors are two bright dots on the trace that may be positioned anywhere on the displayed waveform. The seven-segment LED indicators display the time difference between the dots as determined by the TIME/DIV switch setting for the selected time base. In the SAVE Storage Mode, time dots will appear on all the traces simultaneously, with the exception of the SAVE REF waveform. Press the push button again to release it and remove the time dots from the display.

NOTE

In instruments with firmware versions 1.0 and 2.0, the TIME cursor dots can be positioned off the left end of the traces in a SAVE display of the combined CH 1, CH 2, and ADD traces. The TIME dots will remain visible on the ADD trace unless the display is expanded horizontally.

BOTH: COUPLED V/T—Pressing the VOLTS and TIME push buttons in together causes the voltage cursors to couple to the time dots. The coupled cursors may be positioned to any location on the displayed waveform. If more than one VERT MODE is selected, the coupled cursors may be used with only one waveform, determined by the following priority: ADD, CH 1, then CH 2.

In instruments containing firmware version 2.0 or higher, rotating the cursor knob fully counterclockwise into the end-stop spring and holding it, will cause the dashed VOLTS cursor to attach to a previously acquired ground dot. Rotating the control clockwise will detach the VOLTS cursor from the ground dot and reattach it to the time dot on the displayed waveform. In certain instances, the VOLTS cursor may not attach to the ground dot. If this occurs, reacquire a valid ground dot. The VOLTS cursor will then attach to the ground dot as previously described.

While in the COUPLED V/T mode, the seven-segment LED indicators will display the voltage difference between the VOLTS cursors.

Pressing the VOLTS push button to release the 468 from the COUPLED V/T measurement mode will switch the 468 to the TIME measurement mode, and the seven-segment LED indicators will display the time period between the time cursor dots. Time cursors will remain as set in COUPLED V/T.

Pressing the TIME push button to release the 468 from the COUPLED V/T measurement mode will switch the 468 to the VOLTS measurement mode, and the voltage cursors will return to the position they were in before the COUPLED V/T selection was made.

(46) **LED INDICATORS**—Four-digit, seven-segment LED indicators used to display the measurements made on the stored waveform. The LED indicators also display error messages that are generated in the event that an error is detected during the self-test that is performed when power is first applied to the 468. In the NON STORE mode, the LED indicators will not be illuminated after the self-test is completed unless an error message is being displayed.

(47) **Scale-Factor Indicators**—Three dual-color LEDs (red and green under a single lens) used to indicate the scale (V, mV, and DIV; or s, ms, and μs) and the function (red illuminates for V, mV, and DIV measurements; green illuminates for s, ms, and μs measurements).

The DIV scale-factor LED will be illuminated when either both CH 1 and CH 2 are selected or the ADD mode is selected, and the CH 1 and CH 2 VOLTS/DIV switches are set differently. If either VOLTS/DIV VAR control is out of calibrated detent, the DIV LED will illuminate when the VOLTS cursors are selected.

(48) **CURSOR/NO. OF SWEEPS Control**—Combined slow and fast cursor positioning control used to change the position of the selected cursor on the displayed trace. The midrange rotation of the control moves the selected cursor linearly at the slow rate. When the control is rotated into the end-point stop spring, the cursor rate of travel increases to quickly move the cursor to the point of interest.

When the instrument is equipped with the AVG Storage Mode option, this control is used to select the number of sweeps to be averaged. In the ENVELOPE Storage mode, the control is used to set the number of sweeps to be accumulated in the envelope display. While the NO. OF SWEEPS push button is pressed in, rotating the control to the clockwise stop will increase the number of sweeps, and rotating the control to the counterclockwise stop will decrease the number of sweeps. Releasing the NO. OF SWEEPS push button returns the control to its CURSOR positioning function.

(49) **PUSH: CURSOR SELECT**—A momentary contact switch (concentric within the CURSOR/NO. OF SWEEPS control knob) used to alternately select the cursor that will be positioned by the CURSOR control knob. In the VOLTS measurement mode, the cursor selected to be positioned (active cursor) will be displayed as a dashed horizontal line.

Refer to Figure 2-9 for location of items 50 through 52.

(50) **NO. OF SWEEPS (AVG Option and ENVELOPE)**—When pressed in, the number of waveforms (sweeps) selected to be either averaged in the AVG Storage mode or accumulated in the ENVELOPE Storage mode is displayed on the seven-segment LED indicators. This number, for the AVG mode, may be changed in a binary sequence of 2, 4, 8, 16, 32, 64, 126, or 256 by rotating the CURSOR/NO. OF SWEEPS control knob to the end-stop positions. For ENVELOPE Storage mode, the number may also be set to acquire either one waveform or an unlimited number of waveforms (LED indication is 9999). If set for an unlimited number of waveforms, the digital storage circuitry will continually acquire data to be accumulated in the display until a new selection is made.

When the instrument is turned on, the number of sweeps or accumulations is automatically set to 32, and it will remain at this number until a different selection is made by the operator. Switching between any of the modes will not change the number selected for either ENVELOPE or AVG Storage mode.

(51) **TRANSMIT (GPIB Option)**—A momentary contact push-button switch that, when pressed, causes the 468 to go into the SAVE Storage mode to freeze the waveform at the end of the storage cycle in progress.

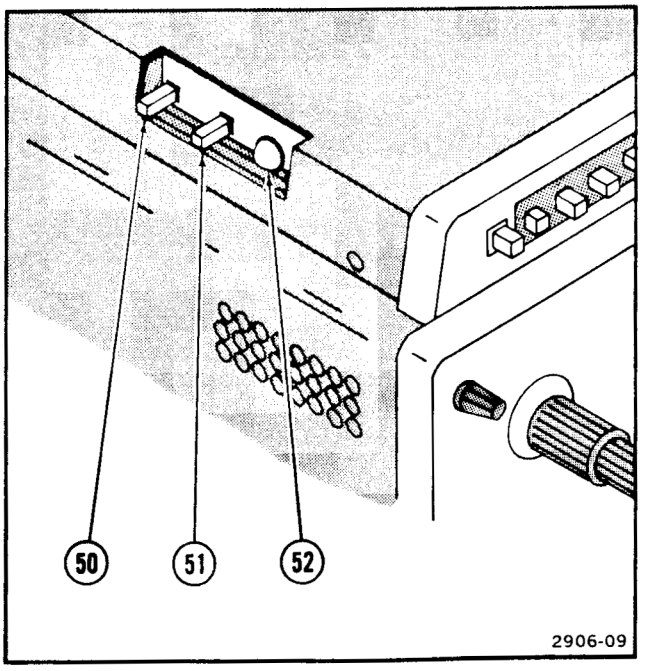


Figure 2-9. Digital storage left side panel controls and indicator.

The current contents of the digital storage memory are transmitted to the GPIB (General Purpose Interface Bus). During transmission time, cursor functions may be used, but controls that can affect the stored data will not be effective until completion of the data transmission. The oscilloscope will return to the selected operation mode upon completion of the transmission.

NOTE

The waveform data will be transmitted as acquired (no interpolation or expansion) with the exception of the AVG waveform acquired in the 0.5, 1, and 2 mV per division positions of the VOLTS/DIV switch. The AVG data is processed to produce added resolution in these VOLTS/DIV settings, and the processed AVG waveform is sent.

Two ways of entering the TRANSMIT mode are possible as determined by the position (on or off) of the TALK ONLY switch on the 468 rear panel. When the TALK ONLY switch is on, the 468 is always a talker, and the waveform will be transmitted when the TRANSMIT button is pressed if the bus is active.

If the TALK ONLY switch is off, pressing the TRANSMIT button will cause the 468 GPIB option to transmit a service request (SRQ). The bus controller does a serial poll in response to the SRQ, and the 468 status byte indicates that a waveform is available. At the end of the poll, the controller arranges for listeners, if required, then sends the 468 talk address (MTA). Upon receiving MTA, the 468 GPIB interface transmits the waveform to the listener(s) on the bus. If device clear (DCL) is received by the 468 during transmission of a waveform, the GPIB interface will go to a state equivalent to having completed the transmission.

The data presented to the GPIB will conform to the Waveform Transmission Standard as specified by Tektronix Interface Standard—General Purpose Interface Bus (GPIB), Codes and Formats.

NOTE

Pressing the TRANSMIT button with no controller or listener on the bus will put the 468 into SAVE, and it will not return to normal operation. The only way to exit this condition is by cycling the POWER switch off, then on again.

To disable the circuit action of TRANSMIT switch (S612) when the 468 is not connected to a GPIB system, set section 8 of the internal Service/Options switch (S707) to the "OPEN" position. The Service/Options switch is located on the A16 STORAGE DISPLAY board, and is shown in Figure 5-6 in the Maintenance section of this manual.

(52) **GPIB Status Indicator ($\overline{\text{TIDS}}$/SRQ) (Option)**—A dual red/green LED indicator that illuminates to indicate GPIB status.

Red—Indicates that a service request (SRQ) has been issued by the 468. Power-on self-test will issue an SRQ, and the red LED will remain on if there is no device on the GPIB to respond to the SRQ.

Green—Indicates that the GPIB interface has been addressed to talk ($\overline{\text{TIDS}}$), either by a bus controller or by setting the TALK ONLY switch on and pressing the TRANSMIT push button.

In normal operation (with controller on the bus) the red LED will flash on (SRQ issued) when the TRANSMIT push button is pressed, and the green LED will be on ($\overline{\text{TIDS}}$, addressed to talk) during the actual transmission of data.

REAR PANEL

Refer to Figure 2-10 for location of items 53 through 58.

(53) **A +GATE OUT**—Bnc connector providing an approximately 5 V, positive-going square wave coincident with the A Sweep time.

(54) **B +GATE OUT**—Bnc connector providing an approximately 5 V, positive-going square wave coincident with the B Sweep time.

(55) **CH 1 VERT OUT SIGNAL OUT**—Bnc connector providing an output signal with an amplitude of approximately 50 mV per each division of displayed Channel 1 signal into 1 MΩ or 25 mV per each division of displayed Channel 1 signal into 50 Ω.

(56) **EXT Z-AXIS INPUT**—Bnc connector used to apply external signals to the Z-axis Amplifier to intensity modulate the crt display. Intensity modulation does not affect the displayed waveshape. Signals with fast rise and fall time provide the most abrupt intensity change. Positive-going signals decrease the intensity, and a 5 V p-p signal will produce noticeable modulation. Z-axis signals must be time related to the display to obtain a stable intensity modulation pattern on the crt. External Z-axis modulation is useful for the NON STORE mode only.

(57) **GPIB Connector (Option)**—Standard GPIB connector allows interconnection with other devices on a GPIB. Conforms to IEEE-488 Standard of 1978.

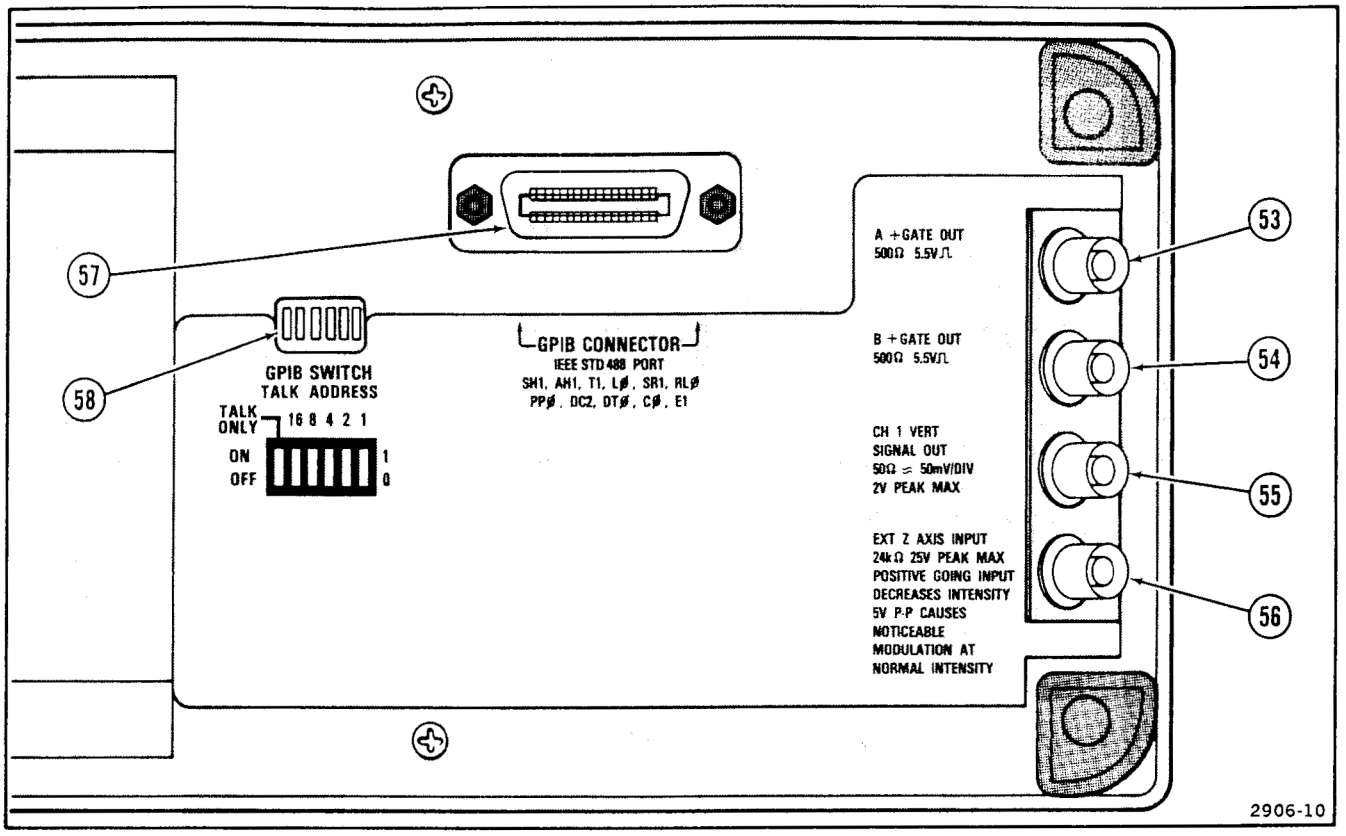


Figure 2-10. Rear panel controls and connectors.

(58) **GPIB Switch (Option)**—The first section of this six-section, two-position switch controls the TALK ONLY local message. In the ON position, the 468 is permanently addressed as a talker. In the OFF position, the 468 must be addressed to talk by a bus controller. The remaining five sections of the switch set the binary talk address of the 468.

Refer to Figure 2-11 for location of items 59 through 64.

(59) **Line Fuse Holder**—Contains the line fuse. See Table 2-1 for fuse change information.

(60) **Detachable Line Cord**—Makes the connection between the oscilloscope and the power source. The cord may be conveniently stored by wrapping it around the feet on the rear panel.

(61) **Power Cord Jack**—Receptacle for detachable line cord.

(62) **Mod Slots**—A number in either slot indicates the instrument contains an option or other modification.

RIGHT SIDE PANEL

(63) **Regulating Range Selector Switch**—Selects the regulating range of the 468 power supplies to match the available ac-power-source voltage. See Table 2-2 for switch change information.

(64) **Line Voltage Selector Switch**—Selects either 115-V or 230-V nominal ac-power-source voltage. Refer to Table 2-2 for switch change information. The line fuse must be changed to match the ac-power-source voltage range selected (see Table 2-1).

LEFT SIDE PANEL

Refer to Figure 2-12 for location of items 65 and 66.

(65) **Vertical Gain Controls (accessible through left side panel)**—Screwdriver adjustments to set the gain of each vertical channel.

(66) **Variable Balance Controls (accessible through left side panel)**—Screwdriver adjustments to set balance of each vertical channel.

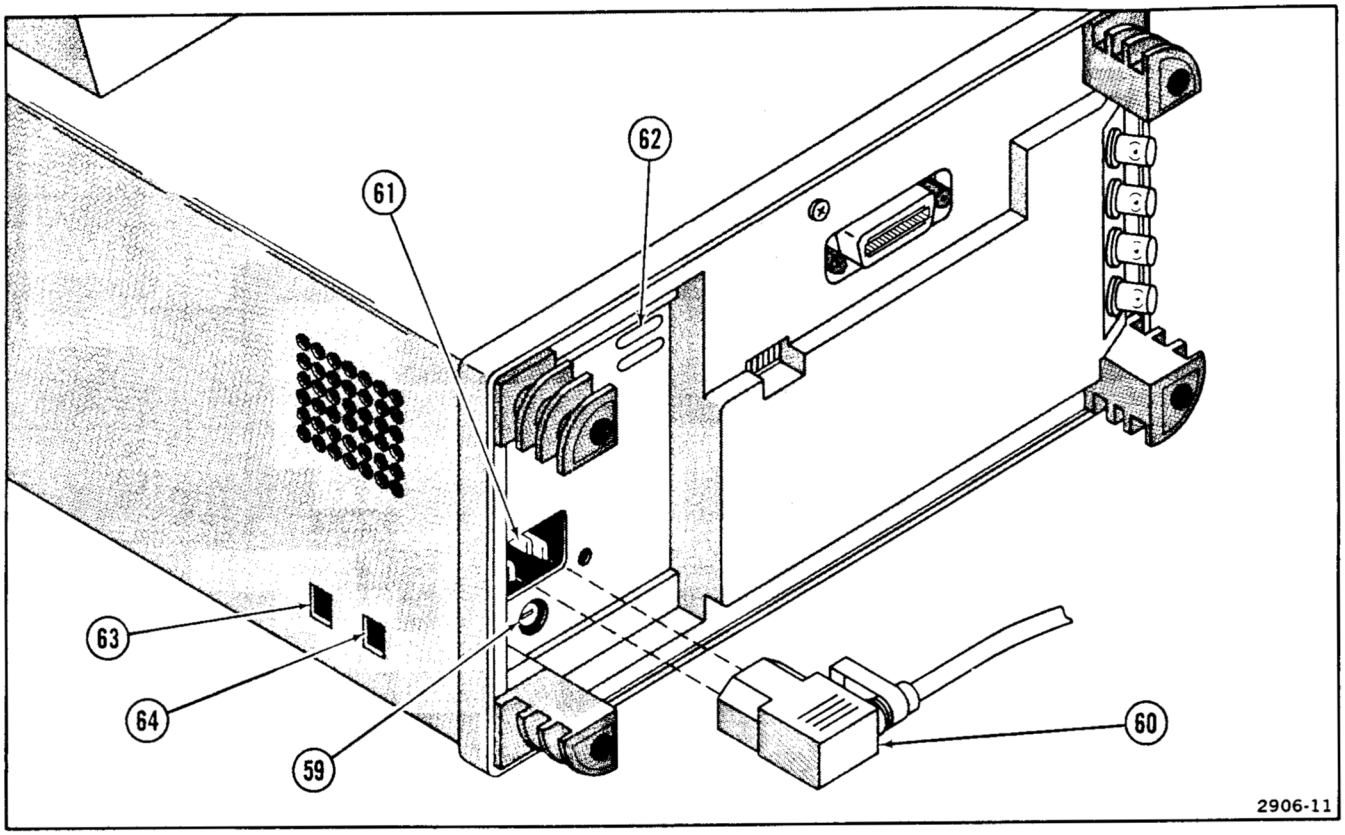


Figure 2-11. Rear panel and right side panel power controls, connectors, and indicators.

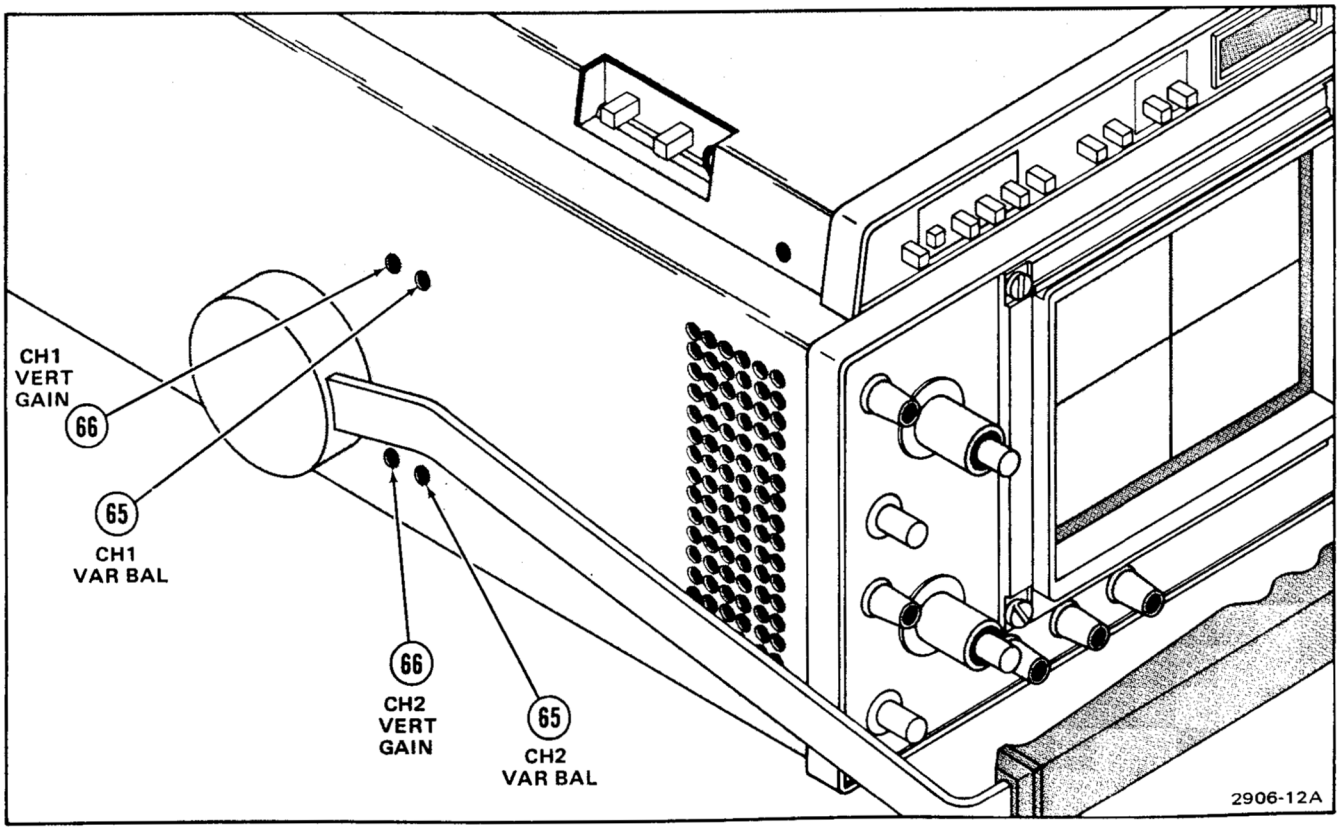


Figure 2-12. Left side panel controls.

OSCILLOSCOPE DISPLAYS

The procedures in this section will allow you to set up and operate your instrument to obtain the most commonly used oscilloscope displays. Before proceeding with these instructions, verify that both the Line Voltage Selector switch and the Regulating Range Selector switch are placed in the proper positions and that the correct line fuse is installed for the ac-power-input voltage being used. Refer to the "Preparation for Use" instructions in this manual for the information and procedures relating to ac-power-input-source voltage, regulating range, and fuse selection. Verify that the POWER switch is OFF (push button out), then plug the power cord into the ac-power-input-source outlet.

NON STORE DISPLAYS

The following procedures are used to obtain the most commonly used conventional oscilloscope displays.

NORMAL SWEEP DISPLAY

1. Preset the instrument controls as follows:

Vertical

VERT MODE	CH 1
VOLTS/DIV	Proper setting determined by amplitude of signal to be applied
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC (Input Coupling)	AC
POSITION	Midrange
20 MH BW LIMIT	Not limited (push button out)
INVERT	Off (push button out)

Display

INTENSITY	Fully counterclockwise
FOCUS	Midrange
SCALE ILLUMINATION	Midrange

Horizontal

TIME/DIV (A and B)	Locked together at 0.1 ms
A TIME/DIV VAR	Calibrated detent
HORIZ DISPLAY	A
X10 MAG	Off (push button out)
POSITION	Midrange

Trigger (both A and B if applicable)

SLOPE	+ (plus)
LEVEL	0 (midrange)
SOURCE	NORM
COUPLING	AC
TRIG MODE (A only)	AUTO
A TRIG HOLDOFF	NORM (fully ccw)

Digital Storage

NON STORE	Push button in

2. Push the POWER push button in (ON) and allow the instrument time to warm up. Using the supplied 10X probe or a properly terminated coaxial cable, apply a signal to the CH 1 input connector. The signal source output impedance determines the termination required when using a coaxial cable to interconnect test equipment.

NOTE

Instrument warmup time required to meet all specification accuracies is 20 minutes.

3. Advance the INTENSITY control until the display is visible. If the display is not visible with the INTENSITY control at midrange, press the BEAM FIND push button and hold it in while adjusting the Channel 1 VOLTS/DIV switch to reduce the vertical display size. Center the compressed display using the Vertical and Horizontal POSITION controls. Release the BEAM FIND push button.

4. Set the Channel 1 VOLTS/DIV switch and the Vertical and Horizontal POSITION controls to locate the display within the graticule area.

5. Adjust the A Trigger LEVEL control for a stable, triggered display.

6. Set the A TIME/DIV switch for the desired number of cycles of displayed signal. Then adjust the FOCUS control (and ASTIG, if necessary) for the best defined display.

MAGNIFIED SWEEP DISPLAY

1. Obtain a Normal Sweep Display.

2. Adjust the Horizontal POSITION control to move the area to be magnified to within the center crt graticule division (0.5 division on each side of the center vertical graticule line). Change the TIME/DIV switch setting as required.

3. Press the X10 MAG push-button switch in (on) and adjust the Horizontal POSITION control for precise positioning of the magnified display.

4. To calculate the magnified sweep rate, divide the TIME/DIV switch setting by 10.

B DELAYED SWEEP DISPLAY

1. Obtain a Normal Sweep Display.

2. Set the HORIZ DISPLAY switch to A INTEN and the B Trigger SOURCE switch to STARTS AFTER DELAY.

3. Pull out the B TIME/DIV knob to unlock it from the A TIME/DIV knob and turn it clockwise from the counterclockwise stop until the intensified zone is the desired length. Adjust the INTENSITY and B INTENSITY controls as required to make the intensified zone distinguishable from the remainder of the display.

4. Adjust the DELAY TIME POSITION control to move the intensified zone to cover that portion of the A trace that is desired to be displayed on the B trace.

5. Set the HORIZ DISPLAY switch to B DLY'D. The intensified zone adjusted in steps 3 and 4 is now displayed as the B trace at the sweep rate indicated by the white stripe on the B TIME/DIV knob.

6. A more stable display with less jitter may be obtained by setting the B Trigger SOURCE switch to match the position of the A Trigger SOURCE switch and adjusting the B Trigger LEVEL control for a stable display.

NOTE

The DELAY TIME POSITION control will not provide continuously variable delay when the B Trigger SOURCE is set to a position other than STARTS AFTER DELAY. Also, differential time measurements are invalid when the B Trigger SOURCE switch is not set to STARTS AFTER DELAY.

ALTERNATE HORIZONTAL SWEEP DISPLAY

1. Obtain a Normal Sweep Display.

2. Set the HORIZ DISPLAY switch to ALT and the B Trigger SOURCE to STARTS AFTER DELAY.

NOTE

Two traces will be visible: the A trace with an intensified zone, and the B DLY'D trace.

3. Adjust the Channel 1 POSITION control and TRACE SEP control as required to display the A trace above the B trace.

4. Pull out the B TIME/DIV knob to unlock it from the A TIME/DIV knob, and turn it clockwise to the desired B Sweep rate. (The B Sweep rate is indicated by the white stripe on the B TIME/DIV knob.)

5. Adjust the INTENSITY and B INTENSITY controls as required to make the intensified zone distinguishable on the A trace and to set the B trace intensity to the desired brightness.

6. Adjust the DELAY TIME POSITION control to move the intensified zone to cover the portion of the A trace that is to be displayed on the B trace.

X-Y DISPLAY

1. Obtain a Normal Sweep Display. Rotate the INTENSITY control fully counterclockwise and disconnect the CH 1 input signal.

2. Use equal length coaxial cables, or the two supplied 10X probes, and apply the vertical signal (Y-axis) to the CH 2 OR Y input connector and the horizontal signal (X-axis) to the CH 1 OR X input connector.

3. Set the A TIME/DIV switch fully counterclockwise to the X-Y position.

NOTE

For instruments with firmware version 1.0, both the CH 1 and CH 2 VERT MODE push buttons must be pressed in to illuminate the scale-factor LED only. It is not necessary to select any VERT MODE to obtain the X-Y display.

4. Advance the INTENSITY control until the display is visible. If the display is not visible with the INTENSITY control at midrange, press and hold in the BEAM FIND push button while adjusting the Channel 1 and Channel 2 VOLTS/DIV switches until the display is reduced in size, both vertically and horizontally. Center the compressed display with the POSITION controls (Channel 2 POSITION control for vertical movement; Horizontal POSITION control for horizontal movement). Release the BEAM FIND push button. Adjust the FOCUS control for a well-defined display.

NOTE

The display obtained when sinusoidal signals are applied to the X- and Y-axis is called a Lissajous Figure. This display is commonly used to compare the frequency and phase relationship of the two input signals. The frequency relationship of the two input signals determines the pattern seen. The pattern will be stable only if a common divisor exists between the two frequencies.

5. Disconnect the input signals from the channel input connectors and rotate the A TIME/DIV knob to 1 ms per division.

SINGLE SWEEP DISPLAY

1. Obtain a Normal Sweep Display. For random signals, set the A Trigger LEVEL control to trigger the sweep on a signal that is approximately the same amplitude as the random signal.

2. Press the SINGL SWP push button. The next trigger pulse will initiate the sweep, and a single trace will be displayed. If no trigger signal is present, the READY indicator LED should illuminate to indicate that the A Sweep Generator circuit is set to initiate a sweep when a trigger signal is received.

3. When the single sweep has been triggered, and the sweep is completed, the sweep logic circuitry is locked out. Another sweep cannot be generated until the SINGL SWP push button is pressed to set the Sweep Generator to the READY condition.

DIGITAL STORAGE DISPLAYS

The following procedures explain how to set up and use the digital storage capabilities of the 468. Front panel controls set the conditions under which a waveform is acquired for display. Display amplitude is controlled by the VOLTS/DIV switches, and the storage window is controlled by the A or B TIME/DIV switch. Certain conditions of Vertical Mode selection and Storage Mode selection will store waveforms under a priority plan. See Table 2-3 for a complete chart describing the waveform stored for both display and reference with different combinations of Vertical Mode and Storage Mode selections.

NORM STORAGE MODE DISPLAY

1. Obtain a Normal Sweep Display of the waveform to be stored.

2. If the signal is obtained at sweep speeds of 1 μs per division or faster, select either the SINE Display Response for sinusoidal signals or PULSE Display Response for pulse-type signals.

3. Select PRE TRIG or POST TRIG Storage Window. PRE TRIG will cause 7/8 of a waveform to be stored before the trigger event; POST TRIG will cause only 1/8 of a waveform to be stored before the trigger event. In both cases, the remaining portion of the waveform is stored after the trigger event occurs.

4. Press the NORM Storage Mode push button in.

Table 2-3

Priority Storage Plan

Selected Vertical Mode(s)	Selected Storage Mode	CHOP/ALT	Display With SAVE REF Off	Ref Saved	Display With SAVE REF On
CH 1	a	b	CH 1 Only	CH 1	CH 1 and Ref
CH 2	a	b	CH 2 Only	CH 2	CH 2 and Ref
ADD	a	b	ADD Only	ADD	ADD and Ref
CH 1, CH 2	a	ALT	CH 1 and CH 2	CH 1	CH 1 and Ref
CH 1, ADD	a	b	CH 1 and ADD	ADD	ADD and Ref
CH 2, ADD	a	b	CH 2 and ADD	ADD	ADD and Ref
CH 1, CH 2	NORM	CHOP	CHOP of CH 1/CH 2	CH 1/CH 2	CH 1/CH 2 and Ref
CH 1, CH 2, ADD	NORM	b	CHOP of CH 1/CH 2 and ALT ADD	ADD	ADD and Ref
CH 1, CH 2	ENV or AVG	b	CH 1 and CH 2	CH 1	CH 1 and Ref
CH 1, CH 2, ADD	ENV or AVG	b	CH 1 and ADD	ADD	ADD and Ref

[a]NORM ENV, or AVG Storage Mode selected.

[b]Either CHOP or ALT Vertical Mode selected.

5. In this mode, the display responds to front-panel control changes with each sweep trigger, and the results of changes may be viewed each sweep. Waveforms acquired and displayed at low sweep rates require an increasing time to change as the sweep rate decreases (e.g., a waveform acquired at a sweep rate of 1 s per division requires approximately 10 seconds for the sweep time, and the triggering signal must be received after the sweep in progress is completed). Therefore, at the slower sweep speeds a longer delay is required before the display responds after changing a front-panel control.

NOTE

A signal displayed at 2, 1, and 0.5 mV per division is acquired at 5 mV per division and expanded vertically 2.5, 5, or 10 times in the steps of the VOLTS/DIV switch.

ENVELOPE STORAGE MODE DISPLAY

1. Obtain a Normal Sweep Display of the waveform to be stored.

2. Set TRIG MODE to NORM and adjust the A Trigger LEVEL control to obtain a stable display of the waveform to be stored. (This ensures that the trigger and the waveform to be stored are synchronized, especially on low-repetition-rate waveforms.)

3. Select either PRE TRIG Storage Window to acquire 7/8 of the waveform before the trigger event or POST TRIG Storage Window to acquire 7/8 of the waveform that occurs after the trigger.

4. Press the ENVELOPE Storage Mode push button in.

5. Change the number of sweeps to be accumulated in the waveform envelope display using the following procedure, if necessary. (The number is automatically set to 32 at power on.)

   a. Press the NO. OF SWEEPS push button in. The seven-segment LED indicators will now display the number of sweeps to be accumulated.

   b. Rotate the CURSOR/NO. OF SWEEPS control knob either clockwise to increase the displayed number or counterclockwise to decrease the number.

   c. Press the NO. OF SWEEPS push button again to release it. The number on the display will count down as the sweeps are being acquired for the first storage cycle after the NO. OF SWEEPS push button is released. However, countdown begins as soon as a new selection is made, and the push button must be released immediately if it is desired to view the countdown. After the first ENVELOPE storage cycle countdown is com-

pleted, the LED display will be under the control of the CURSOR FUNCTION mode in use. The displayed number will not count down if the number of sweeps is set to 9999.

NOTE

The number of sweeps to be accumulated in the display is selectable from 1 to 256 in a binary sequence. The digital storage circuitry will display the resultant waveform with each sweep as the selected number of sweeps are acquired, then remove the resultant waveform and start the accumulations again in a repetitive cycle. An unlimited number of sweeps may also be selected (LED indicator display is 9999). In that case, the digital storage circuitry will continue to accumulate sweeps until the operator either makes a new number-of-sweeps selection or starts the accumulation cycle again by changing any oscilloscope front-panel control that will affect the data being acquired.

AVG STORAGE MODE DISPLAY (OPTION) (STANDARD SN B032430 & UP)

1. Obtain a Normal Sweep Display of the waveform to be stored.

2. Set oscilloscope TRIG MODE to NORM, and adjust the A Trigger LEVEL control to obtain a stable display of the waveform to be stored. (This ensures that the trigger and the waveform to be stored are synchronized, especially on low-repetition-rate waveforms.)

3. If waveforms are acquired at a TIME/DIV switch setting of 1 μs per division or faster, select either SINE Display Response for sinusoidal signals or PULSE Display Response for pulse-type signals.

4. Select either PRE TRIG Storage Window to acquire 7/8 of a waveform prior to the trigger or POST TRIG Storage Window to acquire 7/8 of a waveform occurring after the trigger.

5. Press the AVG Storage Mode push button in.

6. Change the number of sweeps to be accumulated in the display using the following procedure, if required. (The number is automatically set to 32 at power on.)

   a. Press NO. OF SWEEPS push button in. The seven-segment LED indicators will now display the number of sweeps to be averaged.

   b. Rotate the CURSOR/NO. OF SWEEPS control knob either clockwise to increase the displayed number or counterclockwise to decrease the number.

   c. Press the NO. OF SWEEPS push button again to release it. The number on the display will count down as the sweeps are being acquired for the first storage cycle after the NO. OF SWEEPS push button is released. Averaging begins as soon as a new selection is made, so the push button must be released immediately if it is desired to view the countdown. After the first AVG storage cycle is completed, the LED display will be under the control of the CURSOR FUNCTION mode in use.

NOTE

The number of sweeps to be accumulated in the averaged waveform is selectable from 2 to 256 in a binary sequence. The digital storage circuitry will acquire the selected number of sweeps to be averaged, then display the averaged waveform while the required sweeps are being accumulated for the next averaged waveform. This cycle continues in a repetitive manner until a new mode is selected. Changing a front-panel control that affects the data being acquired will start the accumulation process over, to obtain the selected number of sweeps at the new control setting.

SAVE STORAGE MODE DISPLAY

1. Acquire a waveform in either NORM, ENVELOPE, or AVG (option) Storage Mode.

2. Press the SAVE Storage Mode push button in.

NOTE

For early serial number instruments, with firmware version 1.0 installed, a minor firmware bug can occur when making voltage cursor measurements in the SAVE STORAGE MODE. The bug occurs when the voltage cursors are positioned at or within 0.05 division of the following spacings: together (one cursor superimposed over the other), 2.5 divisions apart, 5 divisions apart, and 7.5 divisions apart. Under these conditions, an incorrect voltage readout can appear in the seven-segment LED display. (If a 10X scale-factor-switching probe is used to acquire the displayed signal, the incorrect readout can occur over a range of up to 0.6 graticule divisions at each of the preceding voltage cursor spacings.)

Occurence of the bug can be recognized by a decimal point shift in the seven-segment LED display. The digits displayed usually change, but not in every instance.

NOTE (cont.)

The following methods enable the user to compensate for this problem:

a. *Use the COUPLED V/T CURSOR FUNCTION. The voltage readout appearing in the seven-segment LED display will be correct.*

b. *If an off-waveform voltage measurement must be made, use NORMAL STORAGE MODE. SAVE STORAGE MODE is the only function affected by the bug.*

c. *Check the readout (appearing in the seven-segment LED display) against the graticule and VOLTS/DIV switch setting when making measurements over the small ranges affected when the voltage cursors are spaced at 2.5-graticule-division multiples while operating in SAVE STORAGE MODE.*

NOTE

NORM or continuous ENVELOPE acquisition stops immediately, and the displayed waveform is saved. Acquisition of data will stop at the end of a set ENVELOPE or AVG cycle in progress, and the new waveform will be saved. If a front-panel contol setting is changed after the SAVE push button is pressed in but before an ENVELOPE or AVG cycle in progress is completed, the storage cycle will restart to obtain waveforms at the new control setting.

The SAVE display of a waveform acquired in the NORM or AVG (option) Storage Mode with the TIME/DIV switch set to 1 μs per division or faster, will be affected by the setting of the SINE or PULSE Display Response switch, If the ENVELOPE Storage Mode is selected and the number of sweeps to be accumulated is set to 9999, pressing the SAVE push button will immediately switch the 468 to the SAVE Storage Mode.

3. The SAVE Storage Mode display may be expanded up to 100 times depending on the setting of the TIME/DIV switch that controls the horizontal mode in operation when the waveform was acquired. Waveform data is expanded, using digitial interpolation and analog gain. The display is expanded horizontally in both directions from the POST TRIG trigger point (data point 64) and is correctly scaled for the TIME/DIV switch setting (Data point 64 is approximately 1.3 horizontal graticule divisions from the beginning of the trace). When a chopped waveform acquisition is used, the POST TRIG trigger point is data point 32.

4. The SAVE Storage Mode display may be expanded vertically up to 10 times depending on the setting of the VOLTS/DIV switch of the channel used for the data acquisition.

SAVE REF DISPLAY

1. Acquire a waveform in either NORM, ENVELOPE, or AVG (option) Storage Mode to be used as a reference waveform. Refer to Table 3 for a chart of the waveform stored as a reference with various combinations of Vertical Mode and Storage Mode selection.

2. Press the SAVE REF push button in. The reference waveform will be displayed in the vertical position at which it was acquired. It will not be further affected by any control knob or switch setting change on the oscilloscope front panel except the Horizontal POSITION control.

3. Press the SAVE REF push button again to release it and remove the reference waveform from the display. A new reference waveform will be saved each time the SAVE REF push button is pressed in.

THEORY OF OPERATION

INTRODUCTION

SECTION ORGANIZATION

This section contains a functional description of the 468 Digital Storage Oscilloscope circuity. The discussion begins with a general summary of instrument functions broken down into conventional and digital storage operation. Following the General Description, each major circuit is explained in detail, using functional block diagrams and schematic diagrams to show the interconnections between parts of the circuitry, to indicate circuit components, and to identify interrelationships with the front-panel controls. Circuit diagrams and the larger block diagrams are located in the tabbed "Diagrams" section found in Volume II of this manual. The circuit diagram associated with each description is identified in the text and indicated on the tab of the appropriate foldout page by a numbered diamond symbol. For best understanding of the circuit being described, refer to both the appropriate circuit diagram and functional block diagram.

INTEGRATED CIRCUIT DESCRIPTIONS

Digital Logic Conventions

Digital logic circuits perform many functions within this instrument. Function and operation of the logic circuits are represented by logic symbology and terminology. Most logic functions are described using the positive logic convention. Positive logic is a system of notation whereby the more positive of two levels is the TRUE, or 1 state; the more negative level is the FALSE or 0 state. In this logic description the TRUE state is referred to as HI, and the FALSE state is referred to as LO. The specific voltages which constitute a HI or a LO state vary between specific devices.

In the discussion of the General Purpose Interface Bus (GPIB) option, signals are described as asserted (TRUE) or unasserted (FALSE) rather than HI or LO. The GPIB uses negative logic signals for bus operation. Circuitry in the 468 GPIB interface convert the negative-logic GPIB signals to positive logic signals for use within the 468.

Linear Devices

The functioning of individual linear integrated circuit devices is described in this section using waveforms or other techniques to illustrate their operation.

GENERAL DESCRIPTION

In the following overall functional description of the 468 Digital Storage Oscilloscope, refer to basic block diagrams Figures 3-1 and 3-2 and to the detailed block diagrams located in the "Diagrams" section of this manual. Each major block in the diagrams represents a major circuit within the instrument. In Figure 3-1, the numbered diamond symbol in each block refers to the appropriate schematic diagram number.

CONVENTIONAL OPERATION

Signals to be displayed on the crt are applied to the CH 1 OR X input connector or the CH 2 OR Y input connector. These input signals are then amplified by the Preamplifier circuitry. Each channel includes separate vertical deflection factor, input coupling, balance, gain, and variable attenuation switches or controls. A trigger pickoff

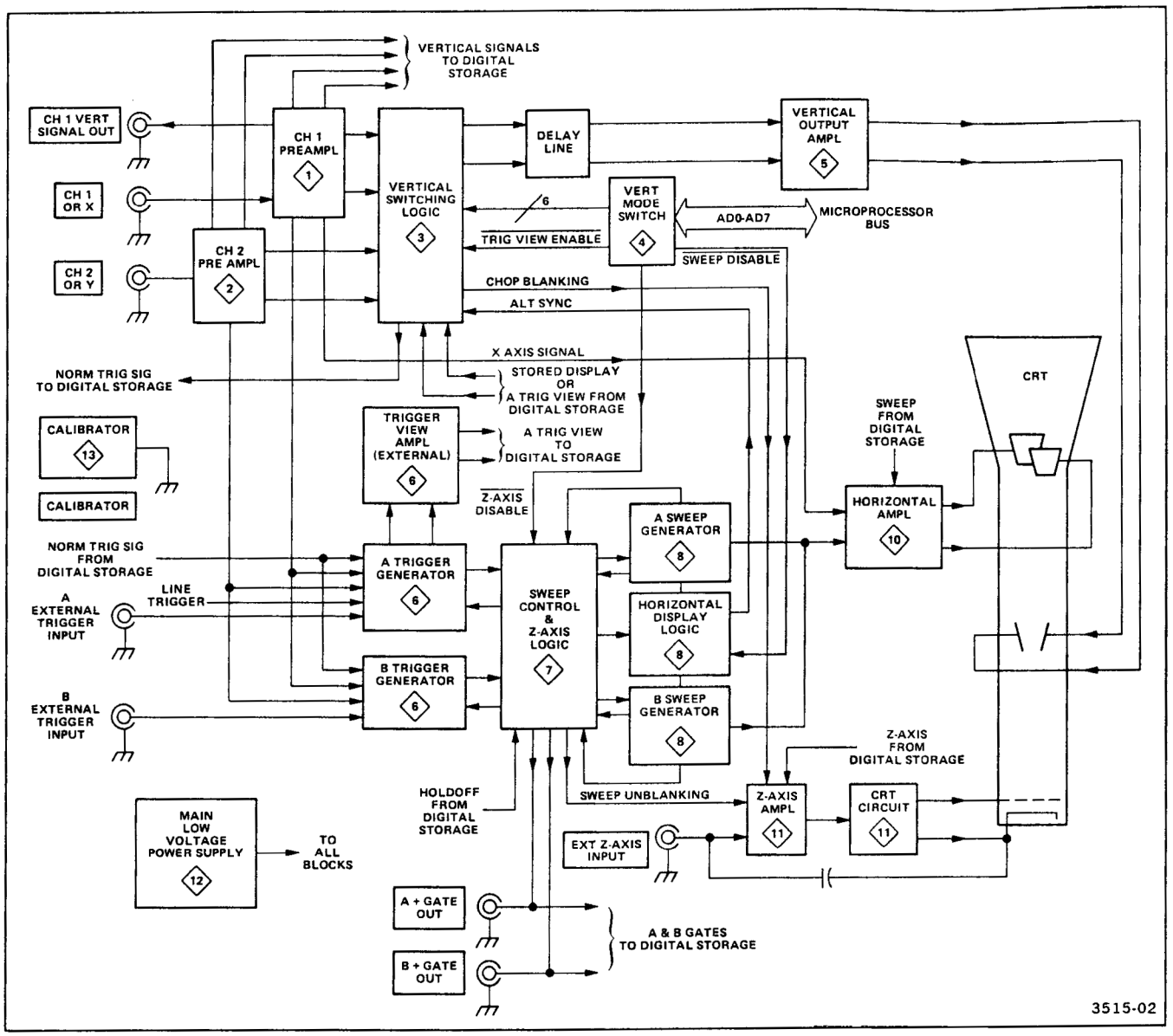


Figure 3-1. Basic block diagram of the 468 Oscilloscope, conventional operating portion.

stage in each vertical Preamplifier supplies a trigger signal from that channel to the Trigger Generator circuits. Another pickoff amplifier supplies the Channel 1 signal to the CH 1 VERT SIGNAL OUT connector on the instrument rear panel. Additional pickoff amplifiers in each Preamplifier supply the Channel 1 and Channel 2 vertical signals to the digital storage input circuitry.

In the X-Y mode of operation, the Channel 1 signal is connected to the input of the Horizontal Amplifier circuit to provide the X-Axis deflection. The Channel 2 signal is amplified by the Vertical Output Amplifier circuit to provide the Y-Axis deflection. The Channel 2 Vertical Preamplifier circuit contains an invert feature to allow the operator to invert the Channel 2 signal displayed on the crt.

The outputs of both vertical Preamplifier circuits, along with the output of the A Trigger View Amplifier via the digital storage circuitry, are connected to the Vertical Switching Logic circuitry. The Vertical Mode Switch circuitry supplies the VERT MODE selection information to the Microprocessor. The Microprocessor then sets the Vertical Switching Logic circuit to the chosen vertical mode of operation. The Vertical Switching Logic circuit selects the input(s) to be displayed on the crt at the appropriate time.

The Chopped Blanking signal (produced in the Vertical Switching circuit and fed to the Z-Axis Amplifier circuit) blanks the switching transients between channels when the chopped mode of operation is selected. A Normal Trigger

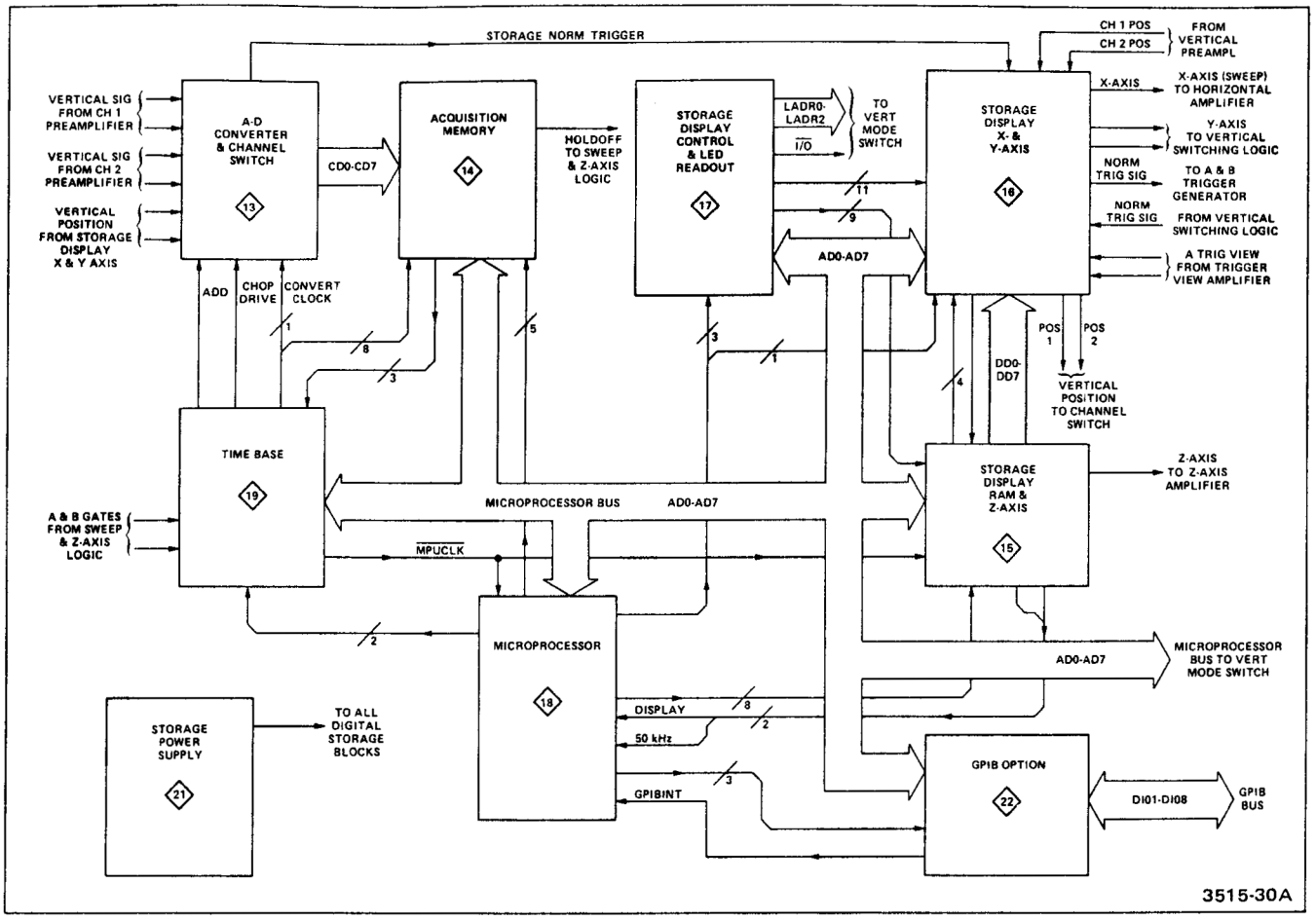


Figure 3-2. Basic block diagram of the 468 digital storage circuitry.

pickoff stage at the output of the Vertical Switching circuit provides a composite trigger (made up of the signal(s) displayed on the crt) to the Trigger Generator circuits via digital storage circuitry.

The Vertical Switching circuit output is connected to the Vertical Output Amplifier through the Delay Line. The Vertical Output Amplifier amplifies the signal and applies it to the crt vertical deflection plates. The vertical portion of the BEAM FIND switch circuitry is included in the Vertical Output Amplifier circuit. When activated, the action of the circuit limits vertical deflection to within the graticule area to aid in locating off-screen or overscanned displays.

The A and B Trigger Generator circuits each create an output pulse that initiates the sweep produced by either the A or B Sweep Generator circuits. Input signals to the A and B Trigger Generator circuits can be individually selected from any of the following sources: Channel 1 signal, Channel 2 signal, signal(s) displayed on the crt (NORM), signal(s) connected to the External Trigger input connectors, or a signal derived from the ac-power source (A Trigger only). Each trigger circuit contains level, slope, coupling, and source controls or switches. The A External Trigger input is also fed to the A Trigger View Amplifier where it is amplified and made available to the Vertical Switching circuitry for viewing on the crt during nonstorage (conventional) oscilloscope operation. The A Trigger View input to the Vertical Switching circuitry is also used to apply the Storage Display signal to the Vertical Switching circuitry during storage operation.

When activated by the A Trigger Generator circuit, the A Sweep Generator circuit produces a linear sawtooth output signal, the slope of which is controlled by the A TIME/DIV switch. The TRIG MODE switches control the operating mode of the A Trigger Generator circuit. When AUTO is selected, absence of an adequate trigger signal for about 100 ms after the end of holdoff causes an A Sweep start gate to be generated. When NORM Trigger Mode is selected, a horizontal sweep is generated only when triggered by an adequate trigger signal. Pushing the SINGL SWP push button sets the Sweep Logic to initiate only one sweep after a trigger pulse is received.

The Z-Axis Logic circuit produces a gate signal to unblank the crt so that the display can be presented. This gate signal is coincident with the sawtooth sweep signal produced by the A Sweep Generator circuit. The A Gate (another signal also coincident with the sawtooth) is fed to the digital storage circuitry to be used as the trigger for ending the acquisition of a signal during storage-mode operation of the oscilloscope. From the digital storage circuitry, the A Gate is made available to the A + GATE output connector on the instrument rear panel.

The Sweep Control Logic circuit produces the Horizontal Alternate Sync pulse that is fed to the Horizontal Display Logic circuit to switch the display between A Intensified and B Delayed sweeps when ALT Horizontal Display mode is selected.

The B Sweep Generator circuit is basically the same as the A Sweep Generator circuit. However, this circuit only produces a sawtooth output signal either when a delay time period (determined by the DELAY TIME POSITION control) has lapsed, or when a trigger pulse is received from the B Trigger Generator circuit. If the B Trigger SOURCE switch is set to the STARTS AFTER DELAY position, the B Sweep Generator produces the sweep immediately following the selected delay time. If the SOURCE switch is set to one of the other available positions, the B Sweep Generator circuit does not produce a sweep until it receives a trigger pulse from the B Trigger Generator circuit. The B Gate signal, produced in the Sweep and Z-Axis Logic circuit coincident with the B Sweep, is fed to the digital storage circuitry for ending the acquisition of a signal at the B Sweep rate for Horizontal Display selections of ALT and B D'LYD. From the digital storage circuitry, the B Gate is made available to the B + GATE output connector on the instrument rear panel.

Sweep signals from either the A or B Sweep Generator are amplified by the Horizontal Amplifier circuit to produce horizontal deflection for the crt except when either the X-Y display mode or storage operation is selected. The Horizontal Amplifier circuit contains a 10X magnifier circuit that may be selected to increase the displayed sweep rate 10 times for any A or B TIME/DIV switch position. External signals may be used for horizontal deflection by using the X-Y position of the A TIME/DIV switch. In the X-Y mode of operation, signals connected to the CH 1 OR X input connector supply the horizontal deflection signal (X-Axis). When operating in a storage mode, the horizontal deflection signal is supplied to the Horizontal Amplifier from the digital storage circuitry.

The Z-Axis Amplifier circuit determines crt intensity and blanking. Input current from the INTENSITY control, the Vertical Switching circuit (chopped blanking), the Z-Axis Logic circuit (unblanking), and the EXT Z-AXIS Input connector are summed in the Z-Axis Amplifier circuit to control the crt trace intensity.

The CRT circuit contains the HV oscillator, the HV multiplier, DC restorer, and HV regulator circuitry. The regulator controls the drive to the oscillator to maintain the correct voltage drive to the HV multiplier. Alternating current from the oscillator is fed to a transformer that is used to supply the HV multiplier drive voltage, the DC restorer drive, and the crt cathode voltage, as well as the focus voltage levels.

The HV multiplier converts the ac input voltage to the high dc accelerating voltage applied to the crt. The sealed multiplier circuitry output is supplied directly to the crt via a HV insulated lead.

DC restoration raises the output level of the Z-Axis amplifier to allow it to be coupled to the crt. Direct coupling is not possible due to the large voltage levels applied to the crt elements.

During storage operation, both the conventional A and B Sweep signals to the Horizontal Amplifier and the Z-Axis signal to the Z-Axis amplifier are disabled, and the horizontal deflection and intensity modulation signals are provided by the digital storage circuitry.

The Main Power Supply circuit provides the low-voltage power for the conventional portion of the 468. Power is distributed as necessary throughout the instrument.

A Calibrator circuit produces a square-wave output (with both accurate voltage and current amplitudes) that is useful for both checking the calibration of the instrument and compensating voltage probes. The CALIBRATOR current loop provides an accurate current source for calibration of current-measuring probe systems.

DIGITAL STORAGE OPERATION

Channel 1 and Channel 2 input signals supplied from the Preamplifier circuits are applied to the digital storage Channel Switch and A-D Converter circuitry. The Channel Switch, under control of the Microprocessor via the Time Base, selects the appropriate channel signal or signals to be digitized by the A-D Converter and supplied to the Acquisition Memory as parallel, eight-bit data byes to be stored.

The CH 1 and CH 2 vertical position signals (POS1 and POS2), applied to the Channel switch set the dc operating level of the circuit.

A composite storage NORM trigger output signal is provided for application to the A and B Trigger Generator for NORM Trigger Mode storage operation.

The Acquisition Memory is a dual-purpose, random-access memory (RAM). It may be used to either store the waveform data during acquisition of an input signal or as additional system RAM by the Microprocessor during nonacquisition periods. ENVELOPE Storage Mode Min/Max is data determined by four amplitude comparators that locate the minimum and maximum data values at each data point for storage into the Acquisition RAM.

Additional circuitry produces the digital storage holdoff signals to the oscilloscope Sweep and Z-Axis Logic circuit. The digital holdoff prevents another trigger from being generated until the Acquisition Memory has acquired enough data to fill the Pretrigger portion of the input waveform.

Selection of the digital storage sample rate is accomplished in the Time Base circuitry. A 50-MHz Master Clock is divided to produce 25-MHz, 10-MHz and 5-MHz clocks, and the 5-MHz clock is further divided to produce a variable sampling interval under control of the Microprocessor. The selected output clock provides the timing required for signal acquisition.

The Microprocessor sets the Time Base to start acquisition of an input waveform, and the acquisition cycle begins. When either the A Gate or B Gate is received from the oscilloscope Sweep and Z-Axis Logic circuit, the cycle in progress is completed to obtain 512 waveform data points before the acquisition is halted for that cycle.

Each sample clock is counted, and when the required record length is reached, the acquisition cycle is stopped. Additional circuitry in the Time Base measures the time interval between the arrival of the A or B Gate trigger and the occurrence of the next sample clock. The Microprocessor uses the measured time interval data to generate a jitter-correction signal that compensates for signal jitter due to uncorrelated sampling of the input waveform.

Microprocessor clock $\overline{\text{MPUCLK}}$ is provided by buffering the 5-MHz clock frequency through an inverter.

Instrument operation is controlled by the Microprocessor. Devices to perform required circuit operations are addressed by the Microprocessor via address decoding circuitry, and commands are issued to cause the devices under control of the Microprocessor to perform the selected operation. Operating instructions for each routine are stored in the Microprocessor read-only memory (ROM). Instructions are fetched from the ROM, and the Microprocessor determines the required operation to be performed.

At regular intervals, the Microprocessor reads the Status and Switch-position registers that contain the instrument's operating mode. Based on the data obtained from reading these registers, the Microprocessor determines the required sequence of operations necessary to respond to the current conditions.

The operating memory used by the Microprocessor is composed of two random-access memories (Scratch RAM and System RAM). Data being processed by the Microprocessor and the intermediate results of an operation are stored in the two RAM arrays. As stated previously, the Acquisition Memory may also be used by the Microprocessor as additional System RAM between waveform acquisition cycles.

Several interrupting lines are applied to the Microprocessor. The lines allow a routine in progress to be interrupted by another device that either requires service or is signaling the end of an operation.

Processed waveform data is transferred from the Microprocessor memory to the Storage Display RAM and further processed for application to the oscilloscope display circuitry.

The digital storage front-panel controls are read by the Microprocessor from registers located in the Storage Display Control and LED Readout circuitry. Also read is the Service Switch register used for selecting the available service routines when operating the instrument in the service mode.

Under control of the Microprocessor, strobes are generated to control both the display circuitry and the seven-segment LED indicators. The indicators display the VOLTS and TIME cursor differences when waveform measurements are being made. During the power-on routine, the progress of the power-on test is displayed on the seven-segment LED indicators. If an error occurs during the power-on test, an error code will be displayed for use by the service personnel.

In the X- and Y-Axis circuitry, the digital contents of the Display RAM are converted to an analog signal, amplified, then converted into a balanced differential output signal. The signal is applied to the oscilloscope vertical circuitry.

Separate vertical position signals are generated to control the vertical displacement of a channel input signal; one as it is being acquired and the other during a SAVE Storage Mode display of that signal.

The storage display horizontal deflection signal is produced in a ramp generator circuit that starts the ramp on command from the Microprocessor. Correction signals from the Microprocessor are applied to the ramp to reduce the timing jitter that results from the difference in time between the oscilloscope trigger signal and the sampling clock.

Additional circuitry is provided to switch the Normal trigger between the conventional normal trigger signal and the storage display normal trigger signal. Also, switching circuitry selects either the Stored Display or the A Trigger View signal to be applied to the oscilloscope Vertical Output Amplifier circuitry.

The optional General Purpose Interface Bus (GPIB) circuitry provides for transfer of stored digital waveform data to external devices on the bus.

When the GPIB interface is required to function, a GPIBINT signal is generated to interrupt the operation of the Microprocessor and direct it to the section of the ROM containing the GPIB service routine. At the end of interruption and the resulting routine, the Microprocessor returns to the operation that was in progress prior to the interrupt.

The Storage Power Supply produces regulated +5 V, −6 V, +12 V, and −12 V for operation of the digital storage circuitry.

DETAILED CIRCUIT DESCRIPTION

CHANNEL 1 PREAMP

The Channel 1 Preamplifier circuit (Figure 3-3 and diagram 1) provides control of input coupling, vertical deflection factor, gain, and dc balance. Input signals for crt vertical deflection are connected to the CH 1 OR X input connector. When the TIME/DIV switch is set to the X-Y mode, the input signal applied to the CH 1 OR X connector provides the horizontal (X-Axis) deflection.

Input Coupling

Signals applied to the input connector can be either ac-coupled or dc-coupled, or they can be internally disconnected from the input to the Vertical Input Amplifier stages. When Input Coupling switch S30A is set for dc coupling, the input signal is coupled directly to the Input Attenuator stage. When ac coupled, the input signal passes through capacitor C13012, which prevents the dc component of the input signal from passing to the amplifier. In the GND position of S30A, the direct signal path is opened and the input of the amplifier is connected to ground through R3015. This provides a ground reference without the need to disconnect the applied signal from the input connector. Resistor R3014 is a high resistance connected across switch S30A to allow precharging of C13012 when the switch is set to GND. Therefore, the trace remains within the viewing area of the crt when the switch is placed in the AC position.

Input Attenuator

The effective overall deflection factor of each vertical channel of the 468 is determined by the setting of the Channel VOLTS/DIV switch. The basic deflection factor of the vertical deflection system is 5 mV/division of crt deflection.

For VOLTS/DIV switch positions above 5 mV, frequency-compensated voltage dividers (precision attenuators) are switched into the circuit to produce the vertical deflection factors indicated on the front panel. Each channel has a 2X, 4X, 10X, and 100X attenuator which may be selected in various combinations. The selected combination provides constant attenuation at all frequencies within the bandwidth range of the instrument. The Input Attenuators maintain the same input characteristics (1 MΩ and approximately 20 pF) for each setting of the VOLTS/DIV switch. Each attenuator contains an adjustable series capacitor to provide correct attenuation at high frequencies and an adjustable shunt capacitor to provide correct input capacitance.

NOTE

Each attenuator is a hybrid encapsulated plug-in assembly; therefore, replacement of individual components within the attenuator is not possible. Should defects occur, the attenuator must be replaced as a unit.

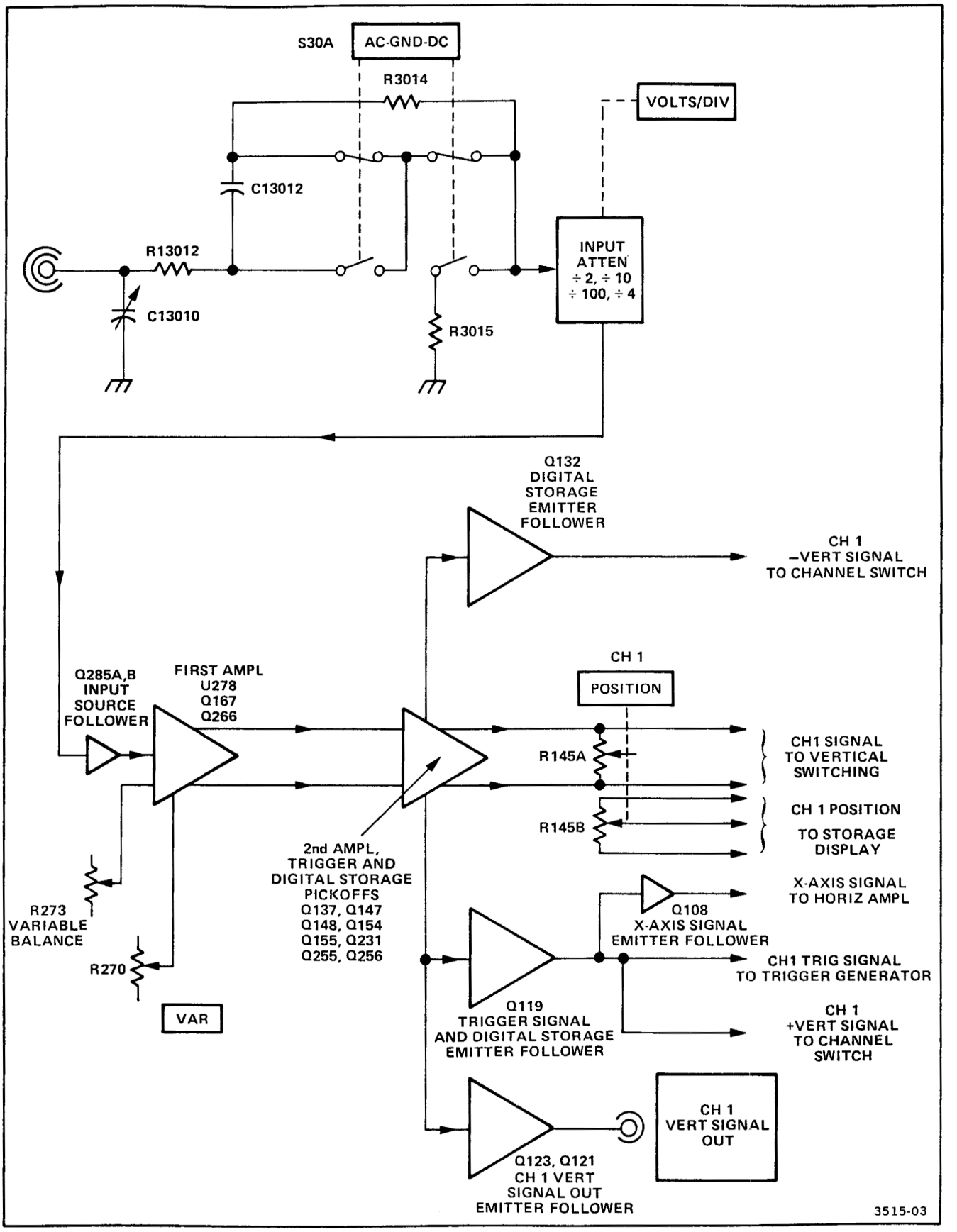


Figure 3-3. Detailed block diagram of the Channel 1 Preamplifier circuit.

Source Follower

The Channel 1 signal from the Input Attenuator is connected to Source Follower Q285A through R3042, C3042, and R3045. Resistor R3039 provides the input resistance and resistor R3045 functions as a damping resistor. A constant current source for Q285A is provided by JFET Q285B. Together, Q285A and B provide a high input impedance for the attenuators and supply the current drive needed for the First Amplifier stage.

In the event that excessively high-amplitude signals are applied to Source Follower Q285A, CR288 and the gate-source junction of Q285A limit the signal amplitude to a safe level for the following circuitry. If the negative signal amplitude causes CR288 to become forward biased, the Q285A gate will be clamped to approximately −8.7 V. Excessive positive-signal amplitude will forward bias the gate-source junction of Q285A. As soon as gate current flows in Q285A, the gate voltage will cease increasing. Gate current is limited to a safe value by the high resistance of R3042.

First Amplifier

The First Amplifier stage (U278) is an integrated-circuit, emitter-coupled, push-pull, cascode amplifier. The single-ended input signal on pins 13 and 16 is converted to a push-pull signal by a paraphase amplifier and then fed to the common-base output stage to produce the current drive to Q167 and Q266. The CH 1 VAR VOLTS/DIV control, from pin 11 of U278, connects into the cascode amplifier stage. The control provides variable vertical deflection for each position of the VOLTS/DIV switch. With the VAR control in its calibrated detent (wiper at ground), the A and D output transistors of U278 are conducting; and the B and C output transistors are biased off. Thus, the signal current available to the following amplifier stage (Q167 and Q266) is the collector current flowing in output transistors A and D.

When the VAR control is rotated out of its calibrated detent, the B and C output transistors of U278 begin to conduct by an amount determined by the position of the VAR control. This causes two events to occur:

1. The signal current flowing in the A and D output transistors is reduced by the amount of signal current flowing in the B and C output transistors; and

2. Output transistors A and C and output transistors B and D conduct current of opposite polarity. The output of transistor C is added to the output of transistor A to reduce the signal current available at pins 5 and 6, and the output current of transistor B is added to the output current of transitor D to reduce the signal current available at pins 8 and 9.

The selected component values provide a variable attenuation ratio of approximately 2.5 to 1.

Channel 1 Variable Balance adjustment R273 is adjusted so that no trace shift occurs in the display when rotating the VAR control. When the Channel 1 VAR control is out of its calibrated detent, the Channel 1 UNCAL LED is illuminated. The components connected between pins 2 and 3 of U278 provide high-frequency compensation for the stage.

Q167 and Q266 are common-base amplifiers that convert the output current signals from U278 into voltage signals to be amplified in the Second Amplifier stage. Gain adjust R269 sets the overall gain of the Channel 1 Vertical Preamplifier by adjusting the signal voltage to the bases of Q255 and Q256.

Second Amplifier

Transistors Q255 and Q256, in conjunction with Q247 and Q248 in the Vertical Switching circuit (diagram 3), form a push-pull, cascode amplifier. High-frequency temperature compensation of the amplifier stage is provided by CR258, CR259, and RT362 to ensure constant gain in the presence of varying ambient temperature. As temperature increases, the resistance value of RT362 decreases, and the reverse bias on both CR258 and CR259 decreases. As the reverse bias decreases, the capacitance value of CR258 and CR259 (voltage-variable capacitors) increases. The increase in capacity at higher temperatures provides additional high-frequency peaking to counteract the effects of increased temperature on the amplifier's gain.

The push-pull signal at the emitters of Q255 and Q256 are converted to a single-ended signal by Q154, Q155, Q147, and Q148. The current signal from Q148 is converted to a voltage signal by common-base amplifier stage Q231 and applied to the bases of Q119 and Q123. Emitter followers Q123 and Q121 provide the output signal to the CH 1 VERT SIGNAL OUT connector located on the instrument rear panel. Diodes CR114, CR119, CR118, and CR112, connected from the CH 1 VERT SIGNAL OUT bus to ground, protect the emitter circuit of Q121 in the event that damaging signal levels are accidentally connected to the output connector.

The output signal at the emitter of Q119 is used both as the trigger source in the CH 1 positions of the A and B Trigger SOURCE switches and as the signal source for the + vertical signal to the digital storage Input Channel Switch (diagram 13). When in the X-Y mode, emitter follower Q108 provides the X-axis signal to the Horizontal Amplifier (diagram 10).

CH 1 TRIG DC BAL potentiometer R122 adjusts the dc level of the CH 1 trigger source signal. In the nonstorage mode, R145A is the Channel 1 Vertical POSITION control. When the potentiometer is set to its mid-position, the constant current supplied by Q151 flows equally through each side of R145A into the collectors of Q255 and Q256. As the POSITION control is rotated from its midpoint, one side of the amplifier receives more current while the other side of the amplifier receives less current. The proportional change in the amount of current flowing into the Delay Line Drivers causes the trace position to move vertically on the crt. The midrange operating point of the POSITION control is set by adjusting R238.

A common-base amplifier stage (Q137) in the collector circuit of Q147 and emitter follower Q132 together form a circuit used to provide the vertical signal to the digital storage Input Channel Switch.

CHANNEL 2 PREAMP

The Channel 2 Preamplifier circuit (diagram 2) is similar to the Channel 1 Preamplifier circuit. Only the differences between the two circuits are described in this part. Input signals for vertical deflection on the crt are connected to the CH 2 OR Y input connector. When the TIME/DIV switch is set to the X-Y mode, the Channel 2 input signal provides the vertical (Y-axis) deflection.

First Amplifier

Basically, the First Amplifier stage in Channel 2 operates in the same manner as the First Amplifier stage in Channel 1. However, the Channel 2 circuit also contains the INVERT switching function to allow the Channel 2 crt display to be inverted. When pushed in, the INVERT switch changes the biasing on the output transistors of U479 so that the normally inactive transistors (B and C) now carry the signal. Since their outputs are cross-coupled from side to side, the output signal is of opposite polarity from the signal available when the INVERT switch is in the normal (button out) position. Channel 2 Invert Balance potentiometer R566 allows the dc balance of the stage to be adjusted to eliminate baseline shift in the display when switching from a normal to an inverted display.

VERTICAL SWITCHING LOGIC

The Vertical Switching Logic (Figure 3-4 and diagram 3) selects the input signal or combination of input signals to be connected to the Vertical Output Amplifier. Input signal combinations to be displayed are selected by a ROM integrated circuit that is controlled by the Microprocessor via the Vertical Mode Switch (diagram 4).

Diode Gates

Channel 1, Channel 2, and Trig View or Stored Display Diode Gates, consisting of four diodes each, act as switches that are controlled by the Vertical Switching Logic circuit. Outputs Q_0, Q_1, and Q_2 of U409 control the switching transistors that switch the Diode Gates on or off. These output signals also are fed into the A_0, A_1 and A_2 inputs of ROM U408 (pins 5, 6, and 7 respectively) to indicate the state of the switches. (Refer to Table 3-1 for a logic table of the ROM switching functions.) A LO indicates that a particular switch is on, and a HI indicates it is off. The ROM uses the state indicators from U409 and the U408 inputs A3 through A7 (pins 4, 3, 2, 1, and 15) from the VERT MODE Switch to turn on the Diode Gates needed to obtain the desired display.

Nonstorage Display

CHANNEL 1 DISPLAY ONLY. When the CH 1 VERT MODE push button is pressed in, the Microprocessor applies a HI to the A_3 input of U408. The A_4, A_5, and A_6 inputs will be LO, and the A_7 input ($\overline{XY}$ select) will be HI. This combination of inputs is used to switch transistor Q418 on, thereby switching on the Channel 1 Diode Gate. The O_1 output of U408 will be LO, while the O_2 and O_3 outputs will be HI. The O_4 output, which controls the CHOP Clock Oscillator, will also be LO. A LO on O_4 disables the CHOP clock and U409 will remain in a state that allows the diode gates to pass only the Channel 1 input signal to the Delay Line Driver.

With only Channel 1 selected, the Q_0 output of U409 will be LO. The LO turns on transistor Q418, and the junction of CR338 and CR334 in the CH 1 Diode Gate is returned to the +5-V supply through R422 and Q418, thus raising the junction voltage to reverse bias CR338 and CR334. Then CR332 and CR336 are forward biased to pass the Channel 1 input signal on to the Delay Line Driver.

The Trig View or Stored Display Diode Gate diodes, CR325 and CR326, and the CH 2 Diode Gate diodes, CR339 and CR335, remain forward biased through pull-down resistors, R421 and R424, to the −8-V power supply. The A Trigger View signals and the Channel 2 input signals are shunted to the −8-V supply and are blocked from the Delay Line Driver because diodes CR331 and CR330 (in the Trig View or Stored Display Diode Gate) and CR337 and CR333 (in the CH 2 Diode Gate) are reverse biased.

CHANNEL 2 DISPLAY ONLY. When CH 2 VERT MODE is selected, Q419 turns on; Q418 and Q318 remain off. The center diodes of the CH 1 Diode Gate and the center diodes of the Trig View or Stored Display Diode Gate are forward biased, while the center diodes of the

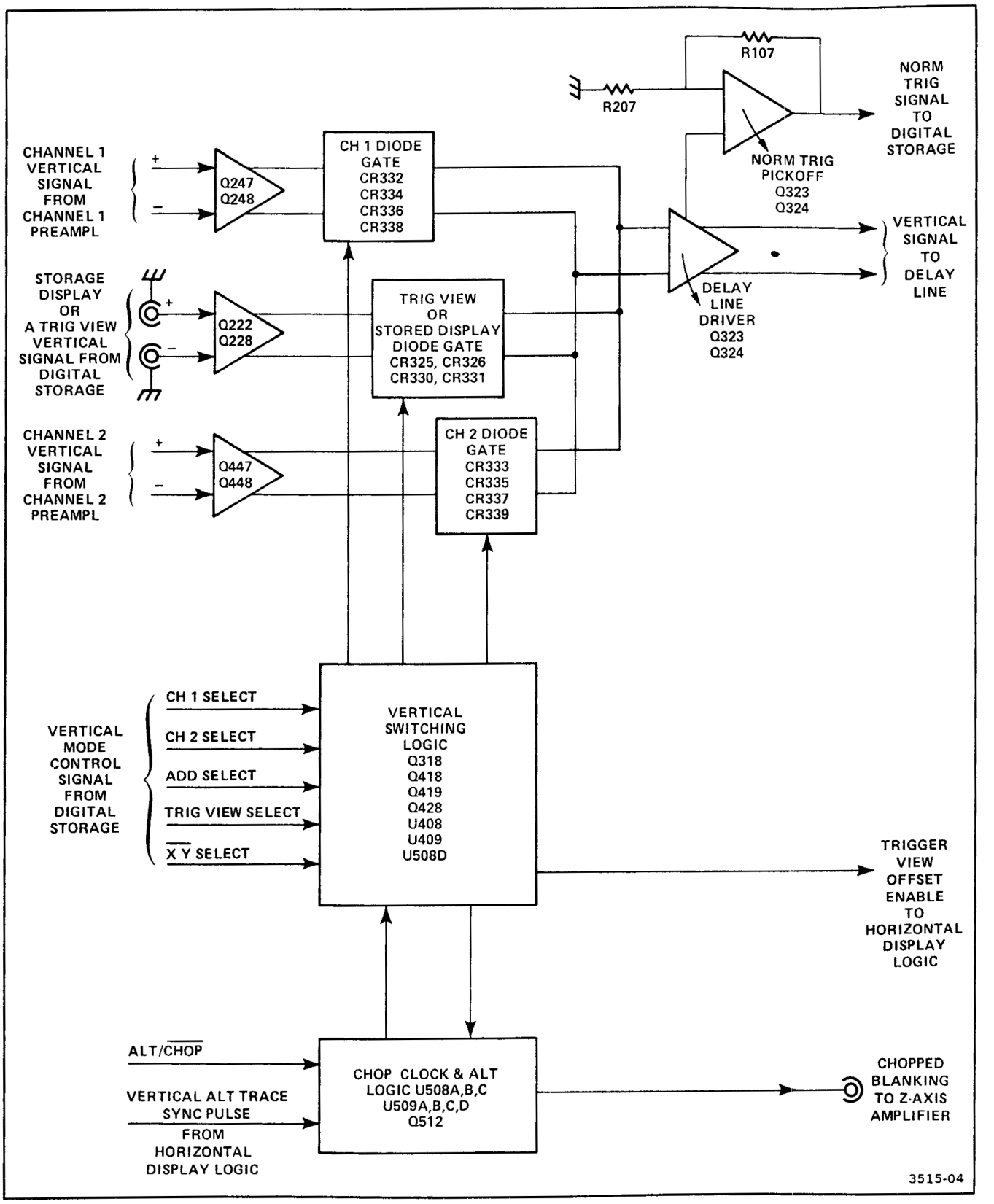


Figure 3-4. Detailed block diagram of the Vertical Switching Logic circuit.

Table 3-1

Read-Only Memory U408 Logic

VERT MODE PRESENT DATA AT U408					UNDEFINED			TRIG VIEW	ADD	CH 2	CH 1	IDLE
$\overline{XY}$	TRIG VIEW	ADD	CH 2	CH 1	$\overline{000}$	$\overline{001}$	$\overline{010}$	$\overline{011}$	$\overline{100}$	$\overline{101}$	$\overline{110}$	$\overline{111}$
1	0	0	0	0	1111	1111	1111	1111	1111	1111	1111	0111
1	0	0	0	1	1110	1110	1110	1110	1110	1110	0110	1110
1	0	0	1	0	1101	1101	1101	1101	1101	0101	1101	1101
1	0	0	1	1	1110	1110	1110	1110	1110	1110	1101	1110
1	0	1	0	0	1100	1100	1100	1100	0100	1100	1100	1100
1	0	1	0	1	1110	1110	1110	1110	1110	1110	1100	1110
1	0	1	1	0	1101	1101	1101	1101	1101	1100	1101	1101
1	0	1	1	1	1110	1110	1110	1110	1110	1100	1101	1110
1	1	0	0	0	1011	1011	1011	0011	1011	1011	1011	1011
1	1	0	0	1	1110	1110	1110	1110	1110	1110	1011	1110
1	1	0	1	0	1101	1101	1101	1101	1101	1011	1101	1101
1	1	0	1	1	1110	1110	1110	1110	1110	1011	1101	1110
1	1	1	0	0	1100	1100	1100	1100	1011	1100	1100	1100
1	1	1	0	1	1110	1110	1110	1110	1011	1110	1100	1110
1	1	1	1	0	1101	1101	1101	1101	1011	1100	1101	1101
1	1	1	1	1	1110	1110	1110	1110	1011	1100	1101	1110
0	0	0	0	0	1101	1101	1101	1101	1101	0101	1101	1101
0	0	0	0	1	1101	1101	1101	1101	1101	0101	1101	1101
0	0	0	1	0	1101	1101	1101	1101	1101	0101	1101	1101
0	0	0	1	1	1101	1101	1101	1101	1101	0101	1101	1101
0	0	1	0	0	1101	1101	1101	1101	1101	0101	1101	1101
0	0	1	0	1	1101	1101	1101	1101	1101	0101	1101	1101
0	0	1	1	0	1101	1101	1101	1101	1101	0101	1101	1101
0	0	1	1	1	1101	1101	1101	1101	1101	0101	1101	1101
0	1	0	0	0	1101	1101	1101	1101	1101	0101	1101	1101
0	1	0	0	1	1101	1101	1101	1101	1101	0101	1101	1101
0	1	0	1	0	1101	1101	1101	1101	1101	0101	1101	1101
0	1	0	1	1	1101	1101	1101	1101	1101	0101	1101	1101
0	1	1	0	0	1101	1101	1101	1101	1101	0101	1101	1101
0	1	1	0	1	1101	1101	1101	1101	1101	0101	1101	1101
0	1	1	1	0	1101	1101	1101	1101	1101	0101	1101	1101
0	1	1	1	1	1101	1101	1101	1101	1101	0101	1101	1101

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CH 2 Diode Gate are reverse biased. Trigger view and Channel 1 signals are blocked from the Delay Line Driver, and the Channel 2 input signal is allowed to pass through its diode gate to the Delay Line Driver.

A TRIGGER VIEW (EXT ONLY). When A TRIG VIEW is selected, the CH 1 and CH 2 Diode Gates are biased off, and the Trig View or Stored Display Diode Gate is biased on to allow either the Stored Display (Storage Mode Operation) or the External Trigger signal to be connected to the Delay Line Driver.

The $\overline{\text{Trigger View Enable}}$ signal is applied to the Trigger View Amplifier to turn it on. The amplifier is disabled when not in use to prevent crosstalk that may occur through the diode gate when large-amplitude trigger signals are applied to the A External Trigger input connector.

In all single-input selections (CH 1 only, CH 2 only, or A TRIG VIEW only) and for a stored waveform display, the switching clock to U409 pin 9 is disabled, and U409 remains in a state to select only the single input chosen for display.

ADD VERTICAL MODE. In ADD, U408 is programmed to turn on both Q419 (CH 1) and Q418 (CH 2). The logic from U409 will also turn on Q428 (ADD) at the same time. It is not necessary to select CH 1 or CH 2 Vertical Modes to obtain the ADD display. With ADD selected, the Q_0 and Q_1 outputs of U409 will be LO, and the $\overline{Q_0}$ and $\overline{Q_1}$ outputs are HI. This switching combination turns both Channel 1 and Channel 2 Diode Gates on. With $\overline{Q_0}$ and $\overline{Q_1}$ HI, AND-gate U508D will be enabled to turn on Q428. The junction of R328 and R330 in the Delay Line Driver input will have −8-V applied to provide sufficient additional current to keep both CH 1 and CH 2 Diode Gates turned on without altering the dc levels associated with the Delay Line Driver circuitry. By selecting additional VERT MODE switches, it is possible to view the Channel 1 signal, the Channel 2 signal, the A External Trigger, and the ADD signal (CH 1 + CH 2) on four separate traces during one display cycle.

X-Y FUNCTION. When the A TIME/DIV switch is set fully counterclockwise to the X-Y position, a LO is applied to ROM U408 pin 15 via the Vertical Mode Switch (diagram 4). This ROM is programmed to produce outputs that turn on Channel 2 switching transistor Q419 and disable the Chop Clock. This action connects the Channel 2 input signal to the Delay Line Driver for use as the Y-axis signal. It is not necessary to select CH 2 Vertical Mode, since the ROM will do all the switching automatically when X-Y function is selected.

ROM Switching

Input signals to ROM U408 are as follows:

1. Input lines A_0 through A_2—The logic levels from the Q_0, Q_1, and Q_2 outputs of U409 are used to indicate the present state of the switching. Q_0, Q_1, and Q_2 outputs are active when LO.

2. Input lines A_3 through A_6—Logic levels applied from the Microprocessor as determined by the VERT MODE switch selection (CH 1, CH 2, ADD, and A TRIG VIEW). A HI logic level is present for the selected Vertical Mode.

3. Input line A_7—This logic level is determined by the X-Y position of the A TIME/DIV switch. A LO logic level is present when X-Y function is selected.

After U409 is clocked, ROM U408 uses the present data on its input lines (A_0 through A_7) to select the next output switching state to be presented to U409 for decoding. On the four output lines of U408, lines O_1 through O_3 carry the future data, and line O_4 is the Chop Clock Oscillator enabling logic (HI enables).

In the partial table shown in Figure 3-5, no Vertical Modes are selected, and the present data from U409 is an undefined column (i.e., 000 is not a Vertical Mode selection). In the example given, the Chop Clock Oscillator will be enabled, and the next clock pulse to U409 will switch U409 output to 111. Table 3-1 shows that column

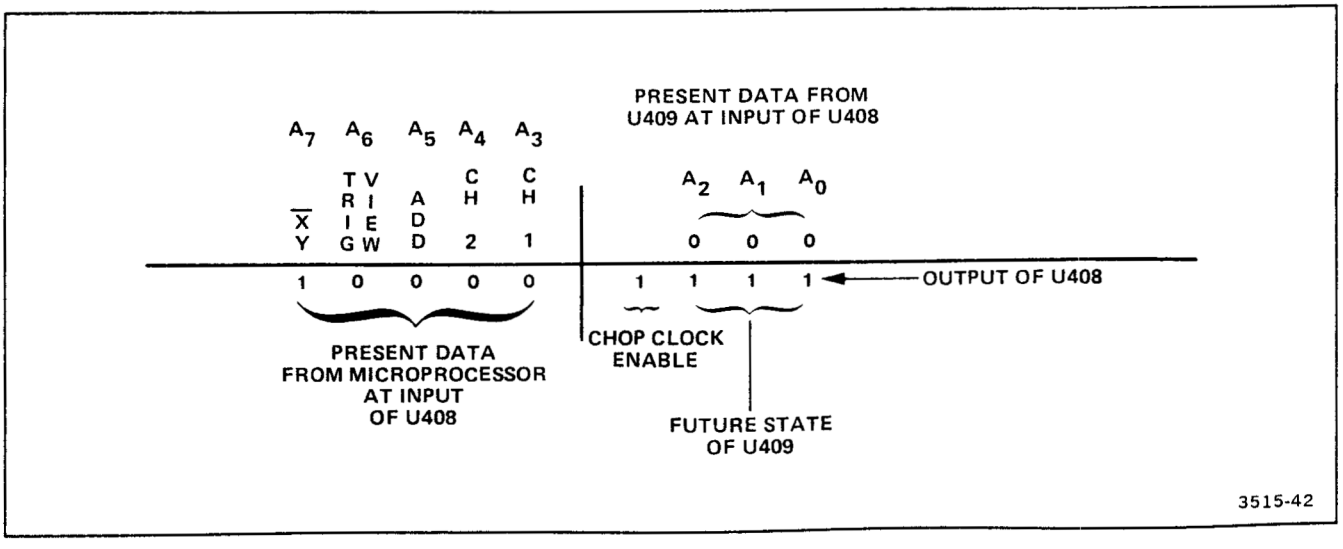

Figure 3-5. Partial Table 3-1.

111 is the idle state of U408 (the state switched to when no Vertical Mode has been selected).

NOTE

In an acquisition storage mode, CH 1 is selected automatically if no Vertical Mode is selected; however, the probe-coding LED will not be illuminated.

In the Idle column of Table 3-1, it is seen that the future state of U409 will remain 111, and the Chop Clock Oscillator will not be enabled. Each row across the table indicates the possible future states of U409, while the column headings indicate the possible present states. The order of priority in switching (when multiple Vertical Modes are selected) is CH 1, CH 2, ADD, and then A TRIG VIEW.

When any Storage Mode is selected, U408 is held in the TRIG VIEW mode. The Stored Display signal is fed to the Delay Line Drivers via the same diode gate that is used for the A Trig View signal.

USING THE LOGIC TABLE. To use the table, determine the Vertical Mode(s) selected. Follow that row across the table. If the output of U409 is at the present state indicated by a column heading, the data given in that column is the future state of U409.

Example 1. Assume CH 1 and CH 2 Vertical Modes are selected. The present data from the Microprocessor is 10011. Move across that row to the 000 column. The data given indicates that if the present state of U409 is 000, the future state will be 110 (CH 1) and that the Chop Clock Oscillator will be enabled. Following across the row, each column, except 110 (CH 1), gives the same future state. If the present state is CH 1, the future state will be 101 (CH 2). From there, it will switch back to CH 1 for the chopped display of the Channel 1 and Channel 2 input signals.

Example 2. Assume that X-Y function is selected. Go to any Vertical Mode selection in the bottom half of the table. All the columns indicate that regardless of the state of U409 output, the future state will be 101 (CH 2). When the output of U409 goes to 101, the Chop Clock Oscillator will be turned off, and the Chop Clock to U409 will cease.

Example 3. Assume ADD Vertical Mode is selected. In the first five columns find 10100. Move across that row (adjacent to 10100) to the 000 column, and note that the future state of U408 is 1100. The output state required to switch to the ADD display is 100. Note that Trig View is not selected, but both CH 1 and CH 2 are selected (LO logic level selects). The Chop Clock Oscillator will be enabled to clock U409. After clocking, the $\overline{Q_0}$ and $\overline{Q_1}$ outputs of U409 (pins 3 and 6 respectively) will be HI to gate U508D thus turning on transistor Q428. This transistor supplies the extra current required to keep both CH 1 and CH 2 Diode Gates forward biased. In the case of the 000 state, it indicates that CH 1, CH 2, and A TRIG VIEW are selected for viewing simultaneously. While this output state exists, the diode gates will not be forward biased during this time and the three signals will not be displayed.

Whenever a Vertical Mode switch is changed, the Microprocessor enables the Chop Clock Oscillator for a specified amount of time to switch U408 to the selected state.

Stored Signal Display

When stored waveforms are displayed, all waveforms (CH 1, CH 2, and ADD) are applied to the Delay Line Driver through the Trig View or Stored Display Diode Gate. The digital storage input Channel Switch (diagram 13) does all the data selection for placing the input signal(s) into the digital storage Acquisition Memory. Input signals are acquired (either chopped or alternately) under control of the Microprocessor. A switching circuit (diagram 16) selects either the stored waveform or the A External Trigger signal for application to the oscilloscope Vertical Output Amplifier.

Chop Clock and Alternate Logic

The Chop Clock Oscillator stage is composed of U509B, U508A, R504, R503, and C504. It supplies the Chop Clock to U409 pin 9 (CLK) for a chopped display of two or more input signals.

When the Q_4 output of U408 is HI and the CHOP VERT MODE is selected, a HI is present on U509B pin 5. A HI, and then a LO will be placed alternately on U509B pin 4 by U508A. For example, assume an initial LO on pin 4 of NAND-gate U509B. The output of this gate will be HI. Capacitor C504 charges forward a HI, and as soon as its charge reaches the threshold level of U508A, U508A will switch to a HI output. The HI output of U508A will assert a HI on U509B pin 4. This HI is NANDed with the HI already present on U509B pin 5 to produce a LO at U509B pin 6. Now C504 must discharge toward a LO. As soon as the charge on C504 reaches the LO threshold of U508B, U508B will switch to a LO output, and the cycle repeats. The Chop Clock Oscillator frequency is approximately 1 MHz and depends on the RC time constant of R503 and C504, as well as the threshold level of U508A (see Figure 3-6).

If CHOP is selected, U509A pin 2 will be LO. Pin 3 of U509A will be HI to enable U508C to pass the Chop Clock

Oscillator frequency to U409 pin 9. Every positive transition of the Chop Clock will cause U409 to change state, thus performing a divide-by-two of the input frequency. Therefore, the chopping frequency is approximately 500 kHz. The Chop Clock Oscillator will not be enabled unless more than one input is selected. As stated previously, a single-input VERT MODE selection will cause U409 to remain in a state that allows only the selected input to be passed on to the Delay Line Driver.

When multiple inputs are selected for chopped display, U409 is clocked to select the appropriate inputs programmed for display. Transistors Q419, Q418, Q318, and Q428 (if ADD is selected) are switched between the input signals at the CHOP frequency. As the displays are incremented, the Q_0, Q_1, and Q_2 outputs of U409 are used as state indicators to the A_0, A_1, and A_2 inputs of ROM U408 to indicate the next input to be selected for display. The order of priority of the switching is: CH 1, CH 2, ADD, then TRIG VIEW.

ALTERNATE TRACE SYNC. With ALT Vertical Mode selected, a HI is present at U509D pin 12. If more than a single-input display is also selected, a HI will be present at pin 13. The CHOP clock is then disabled, and the Alternate Trace Sync pulse is enabled through U508C to the clock input of U409 pin 9. The alternate switching rate between the selected inputs of U409 occurs at a rate determined by the TIME/DIV switch setting.

If a single input is selected for display in the Alternate Vertical Mode, U508B pin 5 will be LO and the Chop Clock Oscillator remains disabled. The Alternate Trace Sync pulse will be present at U409 pin 9, but with only one input selected, U409 will not change state. Therefore, the switching transistor for the selected input to be displayed remains on.

When ALT Horizontal Display is chosen, the Alternate Trace Sync input becomes a square wave with a period equal to twice the time between Alternate Trace Sync pulses. This timing allows the display of both the A Sweep and the B Sweep before switching to the next vertical input signal to be displayed (see Figure 3-7).

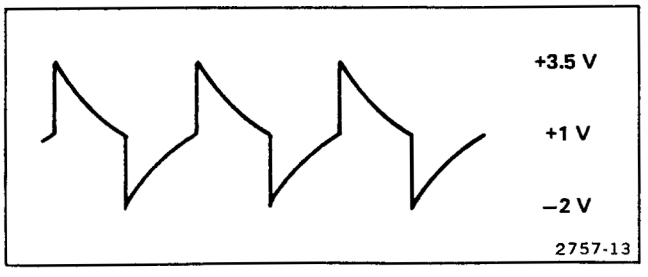

Figure 3-6. Switching waveform at the junction of R503 and R504.

Chopped Blanking Amplifier

When CHOP Vertical Mode is selected, a LO on U509D pin 12 holds U509A pin 11 HI. This HI enables U509C to pass the Chop pulse to C512 and R515. Here it is differentiated to produce positive and negative spikes having sufficiently fast rise times to develop the Chopped Blanking pulse. The positive spike is limited by CR516, and the base current of Q512 is limited by R514. Transistor Q512 is reverse biased by the positive portion of the differentiated waveshape, but when the transition from positive to negative level occurs, Q512 is driven rapidly into conduction. The blanking time is determined by the charging time of C512 through R515. The positive-going output pulse from Q512, which is coincident with trace switching, is applied to the Z-Axis Amplifier in the CRT circuitry (diagram 11) through R513.

Delay Line Driver

The output from each of the diode gates is applied to the Delay Line Driver amplifier composed of Q323, Q324, and associated components. Transistors Q324 and Q323 are connected as a feedback amplifier, with R220 and R319 providing feedback from the collector to the base of its respective transistor. A sample of the composite signal in the collector circuit of Q323 is picked off for triggering the oscilloscope in the NORM Trigger Mode.

Bandwidth Limit switch S310 connects a pi filter (composed of C316, C306, L213, and L310) between the output signal lines of the Delay Line Driver to reduce the upper −3 dB bandwidth of the Vertical Amplifier system

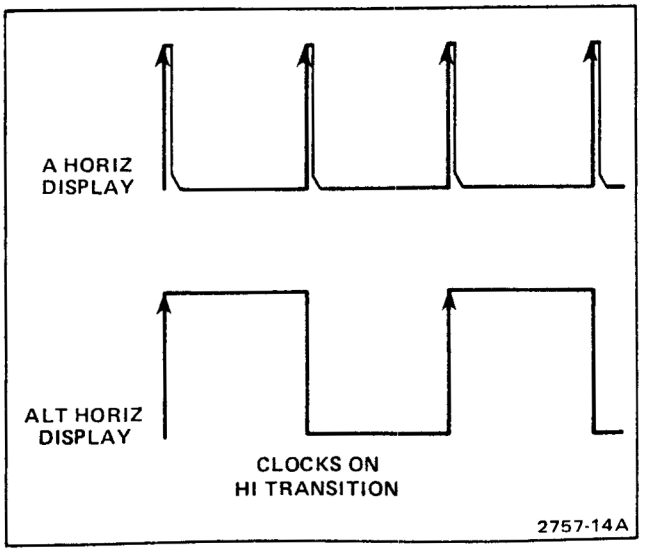

Figure 3-7. Vertical Alt Sync pulse at U409 pin 9.

to approximately 20 MHz. Storage bandwidth is not affected by the bandwidth limiting provided by this filter circuit.

Reverse termination of the delay line is provided by resistors R214 and R311.

Normal Trigger Pickoff Amplifier

The composite trigger signal for nonstorage NORM Trigger Mode operation is obtained from the collector circuit of Q323. Normal Trigger DC Balance Adjustment R205 is used to set the dc level of the Normal trigger output signal so that the sweep is triggered at the zero level of the displayed signal whenever the trigger LEVEL control is set to zero. A feedback amplifier is formed by Q214 and Q114, with the signal applied to the base of Q214. The feedback path is between the Q114 collector and the emitter of Q214 through R107.

The nonstorage Normal trigger signal is fed to a trigger selection circuit in the digital storage Display X- and Y-Axis circuitry (diagram 16). Here either the nonstorage Normal trigger or storage Normal trigger is selected for application to the oscilloscope A and B Trigger Generator circuitry (diagram 6).

VERTICAL MODE SWITCH

The Vertical Mode Switch circuitry (diagram 4) contains the oscilloscope front-panel buffers through which the Microprocessor reads the control positions. A functional block diagram of the Vertical Mode Switch circuitry is located in the "Diagram" section of Volume II of this manual. The front-panel controls are read at regular intervals by the Microprocessor through the use of enabling strobes to each buffer. The Channel VOLTS/DIV switches, Input Coupling switches (AC-GND-DC), UNCAL (VAR) switches, A and B TIME/DIV switches, HORIZ MODE switches (A, A INTEN, ALT, and B DLY'D), and A Trigger SOURCE switch (EXT and EXT/10) directly control the designated oscilloscope functions, but their positions are sensed by the Microprocessor to set the display scale factors and program the correct sampling rate.

The probe-coding light-emitting diodes (X1 and X10 LED) and the vertical mode switching are under control of the Microprocessor via two write-only control registers. Probe coding is controlled so that the probe scale-factor LED may be disabled to indicate either invalid vertical mode selections or that a selected channel is not being displayed. Vertical mode switching must be under the control of the Microprocessor to ensure that data is acquired in the proper sequence and with the correct timing.

Vertical Mode Strobe Control

Address decoder U358 is used by the Microprocessor to generate the strobes required for either reading from the buffers or writing into the Vertical Mode Switch control registers. Table 3-5 in the discusssion of Microprocessor circuitry contains a listing of the addresses assigned to the front-panel controls. Strobes from U358 are generated when address bus ADRB is HI and the I/O strobe is generated LO. Both conditions must be met to enable the selection of a 1-of-8 output line. The U358 output line that is enabled depends on the latched address on input lines LADR0 through LADR1 (pins 1, 2, and 3 respectively). See Table 3-2.

Table 3-2

Front Panel Strobe Generation

U358 Inputs			Output Selected
LADR2 (C)	LADR1 (B)	LADRO (A)	
0	0	0	Y0 ($\overline{\text{CH 1}}$)
0	0	1	Y1 ($\overline{\text{CH 2}}$)
0	1	0	Y2 ($\overline{\text{ATIME}}$)
0	1	1	Y3 ($\overline{\text{BTIME}}$)
1	0	0	Y4 ($\overline{\text{MODE}}$)
1	0	1	Y5 ($\overline{\text{LIGHTS}}$)
1	1	0	Y6 ($\overline{\text{VSM}}$)
1	1	1	Not Selected

CH 1 and CH 2 Selection Buffers

Two identical buffer circuits, composed of U336 and U346 (tristate octal buffers), transfer the positions of the Channel VOLTS/DIV switches, the Input Coupling switches (AC-GND-DC), the probe coding (X1 or X10), and the VAR control (UNCAL condition) to the Microprocessor bus. At the input to the Channel Selection Buffers, transistors Q1308 (CH 1) and Q1309 (CH 2) act as buffer-inverters for the probe coding signals; they also convert the signals to the TTL (transistor-transistor logic) levels required for proper circuit operation. An UNCAL condition is indicated when the VAR control is out of the calibrated detent and S270 is closed. This allows the UNCAL LED to be illuminated and grounds U336 pin 16 (A7).

The remaining input pins (A1 through A6) are either grounded through contacts on the VOLTS/DIV and Input

Coupling switches or raised to a HI through pullup resistors when the switch contacts are open.

During the interval in which the Microprocessor reads the register, U336 is read when the $\overline{CH1}$ strobe is generated, and U346 is read using the $\overline{CH2}$ strobe. Transferred data is placed on the Microprocessor bus lines AD0 through AD7. When the registers are not enabled, the output pins are raised to a high impedance level to isolate the bus.

A TIME/DIV and B TIME/DIV Buffers

Two identical buffers (U326 and U320) are used to place the A and B TIME/DIV switch position information on the Microprocessor bus. The A TIME/DIV buffer places five parallel bits of A TIME/DIV data on the bus, while the B TIME/DIV buffer also places an A or B Time Selection bit (U320 pin 18) on the bus in addition to the B TIME/DIV switch data bits.

The $\overline{ATIME}$ strobe allows U326 to be read, and the $\overline{BTIME}$ strobe allows U320 to be read. Again, when these buffers are not enabled, their output impedance is high to isolate the devices from the bus.

Probe-Coding LED Control Register

The probe-coding LED, located behind the knob skirt of each Channel VOLTS/DIV switch, are controlled by the Microprocessor via commands placed on Probe-Coding LED Control Register U458. Register U458 is composed of four, D-type flip-flops that transfer the bus data placed on inputs D1 through D4 (pins 4, 5, 12, and 13) to outputs Q1 through Q4 on the rising edge of the $\overline{LIGHTS}$ strobe. The rising edge of $\overline{LIGHTS}$ occurs after the data placed on the bus has settled. Data on the output pins remains constant between clocks to provide for constant illumination of the selected probe-coding LED. When an invalid vertical operating mode is selected (i.e., no vertical mode selection or only TRIG VIEW in a storage mode), none of the probe-coding LED will be illuminated. If CH 1 and CH 2 are both selected when a SAVE REF display is also selected, the Microprocessor disables the probe-coding LED of CH 2 to indicate that the CH 2 signal is not being displayed. During the power-on self-test performed by the Microprocessor, all of the probe-coding LED will be illuminated to provide a visual check of their operation.

Vertical Mode Buffer and Control Register

When buffer U466 is strobed by $\overline{MODE}$, the Microprocessor reads the vertical mode selected, the A Trigger SOURCE switch for EXT or EXT/10, and the XY enabling signal. The $\overline{TRIG\ VIEW\ ENABLE}$ signal is buffered and inverted by Q369. Transistor Q369 also converts the signal to the correct level for use in TTL circuitry. Whenever the A Trigger SOURCE switch is set to EXT or EXT/10, the A TRIG VIEW vertical mode is enabled in NON STORE mode. When the A TIME/DIV switch is set to the X-Y position, the X-Y function is enabled. Transistor Q366 performs a similar function for the XY line as transistor Q369 does for the $\overline{TRIG\ VIEW\ ENABLE}$ input line.

Once the Microprocessor has read the Vertical Mode Selection Buffer U466, the data is used at the appropriate time to supply the commands to the Vertical Mode Control Register U310. See Table 3-5 in the Microprocessor discussion to determine the appropriate data bit for each output selection of U310.

The U310 Q_1 output (pin 2) is the SWEEP DISABLE line. When a storage mode is selected, the SWEEP DISABLE line is HI and the signal at P130 pin 7 is fed to the TIME/DIV UNCAL LED to prevent it from being illuminated. The TIME/DIV VAR control does not affect the storage sweep time because the sample rate is derived from a crystal-controlled oscillator in the Time Base circuitry.

Two additional disabling strobe outputs are obtained from buffer-inverter Q115. The $\overline{Z\text{-}AXIS\ DISABLE}$ signal prevents the conventional oscilloscope Z-axis signal from reaching the crt, thus allowing the Stored Display Z-axis signal to provide intensity modulation of the display. The $\overline{SWEEP\ DISABLE}$ signal is fed to CR374 and CR471 in the Horizontal Display Logic circuitry (diagram 8) to prevent the A and B Sweep ramps from reaching the Horizontal Output Amplifier. A horizontal deflection signal is supplied by the Storage Display circuitry when a storage mode is selected. Output Q_2 of U310 is HI when the A TRIG VIEW Vertical Mode is selected in the NON STORE mode provided the A Trigger SOURCE switch is set to either EXT or EXT/10. A HI from U310 pin 5 turns transistor Q203 off to allow the collector to float, and transistor Q209 is biased off. With Q209 off, the $\overline{TRIG\ VIEW\ ENABLE}$ line is LO, and the A TRIG VIEW signal is allowed to reach the Stored Display or Trigger View Diode Gate (diagram 3). When U310 pin 5 is LO, Q208 turns on and Q209 saturates to apply +15 V to the $\overline{TRIG\ VIEW\ ENABLE}$ output line. If TRIG VIEW is selected without being enabled, the +15 V turns off the A Trig View Amplifier and supplies a common-mode current to hold the Delay Line Driver transistors (Q323 and Q324) within their linear operating range.

Vertical Mode selection outputs from U310 (Q4 through Q8) are applied to the Vertical Mode Switching Logic circuitry (diagram 3, circuit operation previously discussed) to select the appropriate diode gate to pass the vertical deflection signal on to the Vertical Output Amplifier.

VERTICAL OUTPUT AMPLIFIER

The Vertical Output Amplifier circuit (Figure 3-8 and diagram 5) provides the final amplification for the vertical deflection signal. The circuit includes the Delay Line, part of the Beam Finder circuitry, and part of the Trace Separation circuitry. Pushing the BEAM FIND button compresses an overscanned display to within the graticule viewing area. The Trace Separation circuit provides vertical positioning of the B trace when the ALT Horizontal Display mode is selected.

Delay Line

Delay Line DL208 (diagram 3) provides approximately 120 ns delay of the vertical signal to allow the Sweep Generator circuits sufficient time to initiate a sweep before the vertical signal reaches the deflection plates of the crt. When using internal triggering, the instrument is allowed to display the leading edge of the signal that originates the trigger pulse. Resistors R211 and R210 provide the correct termination impedance for the Delay Line.

Input Amplifier

Input Amplifier U218 is an integrated-circuit cascode amplifier. Differential vertical signals from the Delay Line are applied to pins 14 and 16 (the bases of the common-emitter input transistors). The output transistors of U218 are arranged as common-base amplifiers with cross connections between the two sides to maintain equal amplitude differential signals from both outputs. Gain of the Input Amplifier is adjusted with R117 by changing the base bias voltage on one of the pair of output transistors on each side.

Emitter current for the input transistors is provided from a network connected between pins 2 and 3. The network circuitry contains the compensation components. the vertical portion of the Beam Finder circuit, and a portion of the Trace Separation circuit.

Beam Finder

The dynamic range of the input transistors is reduced when BEAM FIND push button S175 is pressed in. During normal (noncompressed) operation, either Q108 or Q101 will be conducting to supply emitter current to the input transistors. When S175 opens, the direct −8 V supplied to the emitter circuits of Q103 and Q202 is removed, and emitter voltage is supplied through resistor R349 to reduce the emitter current available to the Input Amplifier. The vertical gain is then reduced to compress an overscanned or off-screen display.

Trace Separation

During display of the B trace, when ALT Horizontal Display mode is selected, a circuit composed of Q108, Q205, Q206, and U105 permits adjustment of the separation between the A and B traces. When the ALT mode is not in use, Q108 is biased off by a LO on its base, and Q202 is conducting to supply equal emitter currents to both sides of the Input Amplifier via R201 and R202.

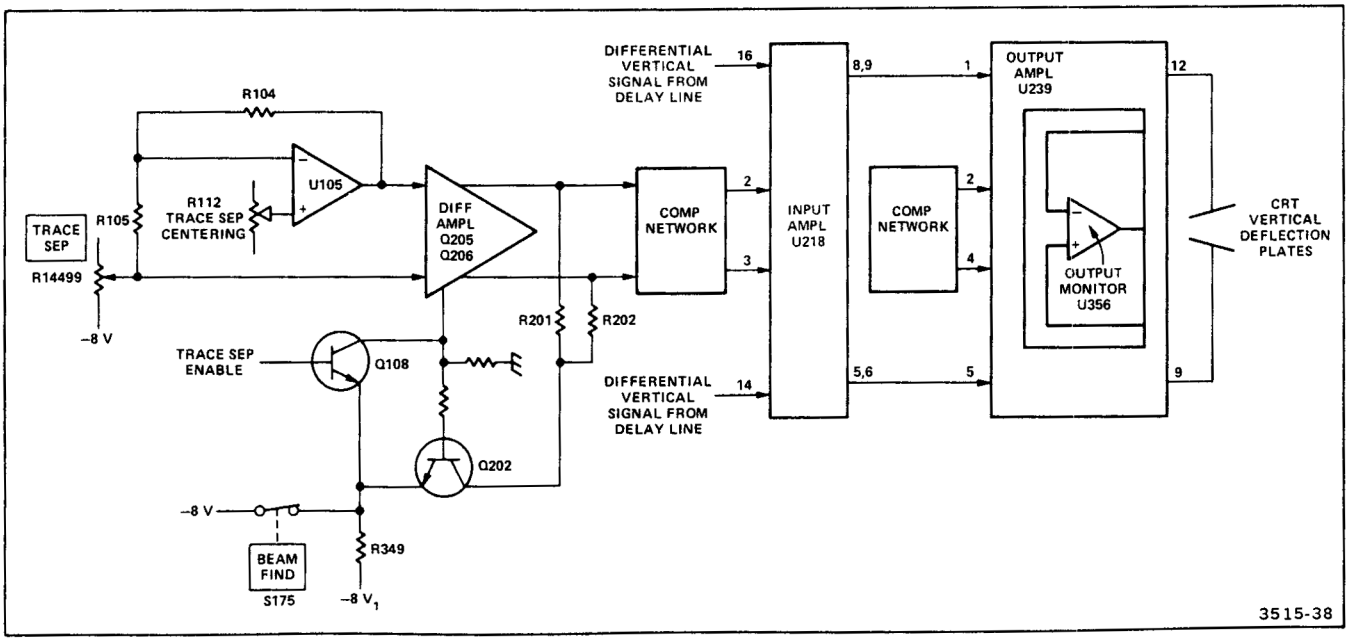

Figure 3-8. Simplified diagram of the Vertical Output Amplifier circuit.

When the Trace Separation circuit is enabled during an ALT Horizontal Display B trace, a HI is applied to the base of Q108 to forward bias it. Transistor Q202 is biased off, and the Differential Amplifier, composed of Q205 and Q206, is supplied a constant-current source from the collector current of Q108. Emitter current to both sides of the Input Amplifier is then supplied from Q205 and Q206.

The TRACE SEP front-panel control supplies a position signal to the base of Q206 and (through a unity-gain, inverting amplifier U105) to the base of Q205. By changing the balance between Q205 and Q206, an offset current is supplied to the emitters of the Input Amplifier to change the vertical position of the B trace. The operating range of the TRACE SEP control is centered with Trace Sep Centering adjustment R112.

Output Amplifier

Integrated circuit U239 is a multi-stage, cascode amplifier that provides final amplification for the vertical signal. The differential input signal is applied to pins 1 and 5, and the output signal to the crt vertical deflection plates is taken from pins 12 and 9. Output Control amplifier U356 monitors the emitter currents of the output transistors and automatically sets the dc level of the output stage to obtain the maximum, undistorted gain from U239. Compensating adjustment components for the Output Amplifier are connected between pins 2 and 4.

A AND B TRIGGER GENERATORS

The Trigger Generator circuits (diagram 6) produce trigger pulses to start the Sweep Generator circuits. These trigger pulses are derived either from the internal trigger signal (sampled from the vertical deflection system), from an external signal connected to the external trigger connectors, or from a sample of the line voltage applied to the instrument. Controls are provided in each circuit to select trigger level, slope, coupling, and source.

An A Trigger View Amplifier circuit amplifies the external A Trigger signal for application to the Trigger View Diode Gate, where the trigger signal may be selected for viewing. The trigger view display provides a method of making a quick and convenient check of the external trigger signal being used to trigger the A Sweep Generator. The external trigger input signal may be continually monitored, when in the NON STORE mode, by selecting the A TRIG VIEW Vertical Mode. The external trigger signal is not viewable in any storage mode.

Since the A and B Trigger Generator circuits are similar, only the A Trigger Generator circuit action and the differences between the A and B Trigger Generator circuits are described.

Trigger Source

Trigger SOURCE switch S320A selects the source of the trigger signal. The sources available to the A Trigger Generator circuit are: the signal(s) being displayed (NORM), Channel 1 (CH 1), Channel 2 (CH 2), LINE, and EXT. The EXT/10 switch position (for the A Trigger circuit only) attenuates the external trigger signal by a factor of 10. The B Trigger SOURCE switch does not have a LINE or an EXT/10 position, but it does have a STARTS AFTER DELAY position.

The STARTS AFTER DELAY position of the B Trigger SOURCE switch is used in conjunction with the DELAY TIME POSITION control. When STARTS AFTER DELAY is selected as a trigger source for the B Sweep, +5 V is applied to the Free Run input of U240, causing the B sweep to start immediately after the delay time (selected by the DELAY TIME POSITION control) has elapsed.

In the LINE mode of triggering, a sample of the power line frequency is obtained from the secondary of power transformer T14500 located in the Low Voltage Power Supply circuit. To prevent unwanted attenuation of the trigger signal by the LF REJ circuit, the A Trigger COUPLING switch should not be set to LF REJ when using line voltage as a trigger source.

Trigger Coupling

The Trigger COUPLING switches offer a means of accepting or rejecting certain components of the trigger signal. In the AC, LF REJ, and HF REJ modes of trigger coupling, the dc component of the trigger signal is blocked by coupling capacitors C423 or C327. Frequency components below 60 Hz are attenuated when using AC coupling, and components below about 50 kHz are attenuated when using LF REJ coupling. The higher frequency components of the trigger signal are passed without attenuation. In the HF REJ mode of trigger coupling, the high-frequency components of the trigger signal (above about 50 kHz) and low-frequency components (below 60 Hz) are attenuated, while the remaining frequency components are passed with minimal attenuation. The DC mode of trigger coupling passes all signals from dc to at least 100 MHz without attenuation.

Input Source Follower

Field-effect transistor (FET) Q430A is a source follower. It provides both a high input impedance for the trigger signal and isolation between the Trigger Generator circuit and the trigger signal source. Diode CR330 provides input protection for Q430A if an excessively high amplitude negative-going input signal is present. If a high-amplitude positive signal is applied, the source-gate junction of Q430A becomes forward biased and clamps the voltage at that level. The second FET of the matched pair, Q430B, is a high-impedance, constant-current source for Q430A. Since both FET are matched and mounted in the same heat sink, both will display equal temperature effects, and Q430B will provide temperature compensation for Q430A.

Trigger Generator

Monolithic integrated circuit U445 generates a stable Trigger Gate output to the A Sweep Start Comparator composed of Q360 and Q316. Trigger Level Centering adjustment R330 sets the level at U445 pin 9 so the display is correctly triggered when the LEVEL control is centered. LEVEL control R17305 varies the level at U445 pin 9 to select the point on a trigger signal where triggering occurs.

The slope of the input signal that triggers the Sweep Generator circuit is determined by the setting of SLOPE switch S17305. When the SLOPE switch is set to the + position, the output signal at U445 pin 14 switches HI only on a positive slope of the input signal at pin 7. When the SLOPE switch is set to the — position, the output signal at pin 14 switches HI only on a negative slope of the input signal at pin 7. The A Slope Center adjustment, R349, balances U445 so that triggering occurs at the same level on both the positive and negative slopes. The A Trigger Sensitivity adjustment, R351, adjusts the built-in hysteresis in U445 to a level that will not allow triggering to occur on low-level noise at the input.

At the end of the sweep time and during holdoff, a HI level is applied to U445 pin 17, resetting the IC and causing the output at pin 14 to go LO. The HI reset level remains on pin 17 during holdoff time to ensure that a sweep-gating signal will not be generated at pin 14 until the sweep circuit has returned to its quiescent state.

Trigger View Amplifier

Transistors Q433 and Q432 make up half of a cascode, push-pull amplifier. In the Vertical Switching Logic circuit, Q222 and Q228 form the rest of the Trigger View Amplifier. The Trigger View Amplifier requires that the A Trigger SOURCE switch be set to EXT or EXT/10, the A TRIG VIEW Vertical Mode be selected, and the NON STORE mode be selected before the amplifier is enabled to pass the external trigger signal to the diode gate and on to the Vertical Output Amplifier. If the trigger view display is selected, the Vertical Switching Logic circuit will turn on the Trigger View Diode Gate during the proper time to pass the signal on to the Delay Line Driver.

A sample of the push-pull external trigger signal is taken from U445 pins 7 and 9 and amplified by Q433 and Q432. Trigger View Centering control R534 is used to vertically position the trigger view display. Potentiometer R443 is adjusted to set the Gain of the Trigger View Amplifier; C438, L532, C538, and R435 provide HF compensation. Diodes VR526, CR530, and CR541 are used to clamp the collectors of Q433 and Q432 to approximately +5.7 V whenever the Trigger View feature is disabled. Transistors Q222 and Q228 will be reverse biased during this time.

SWEEP AND Z-AXIS LOGIC

The Sweep and Z-Axis Logic circuit (Figure 3-9 and diagram 7) develops the logic levels necessary to control the sequence of events associated with sweep generation and crt unblanking. The A + Gate and B + Gate signals are also generated in this circuit.

A Sweep Gate

The A Sweep Gate circuit includes Q360 and Q361. They form an emitter-coupled stage where only one transistor can be conducting at any time. The input signal to the stage is the positive-going trigger signal from the A Trigger Generator circuit (diagram 6). The signal at the collector of Q360 is connected to the A Sweep Z-Axis Gate circuit to control the crt unblanking and to generate the A + Gate signal. The signal at the collector of Q361 is connected to the emitter of Sweep Disconnect Amplifier Q890 in the A Sweep Generator circuit (diagram 8) to initiate A Sweep generation.

B Sweep Gate

The B Sweep Gate circuit includes Q160 and Q161. These transistors also form an emitter-coupled stage where only one transistor can be conducting at any time. The input signal to the stage is the positive-going trigger signal from the B Trigger Generator circuit. The signal at the collector of Q160 is connected to the B Sweep Z-Axis Gate circuit (Q1007 and Q1006) for control of crt unblanking, and to Q1005 for generating the B + Gate signal. The signal at the collector Q161 is connected to the emitter of Sweep Disconnect Amplifier Q864 in the B Sweep Generator circuit to initiate B Sweep generation.

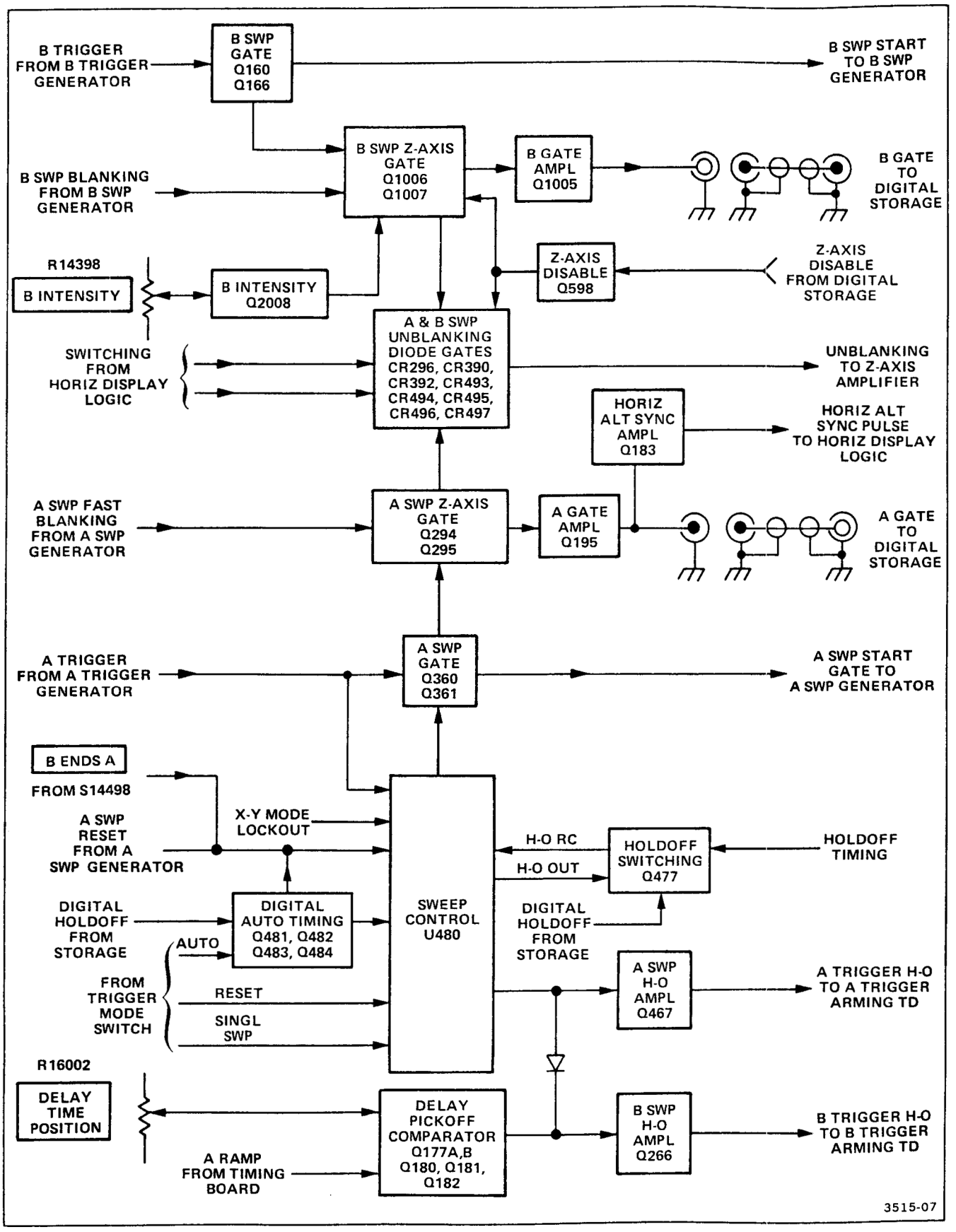

Figure 3-9. Detailed block diagram of the NON STORE Sweep and Z-Axis Logic circuit.

Sweep Control Integrated Circuit

The Sweep Control integrated circuit is U480. Several functions are performed in this stage, depending on the mode of operation of the instrument sweep generators. The following is a brief explanation of the function associated with each pin of the IC.

Pin 1 is the positive Auto Sense input. The signal connected here comes from the A Trigger Generator.

Pin 2 is a reference input to the Auto Sense circuit. A fixed dc level established by R383 and R382 is connected here.

Pin 3 is the + auto gate terminal. In the AUTO mode of operation, if no trigger signals are applied to pin 1 of U480 during the approximately 100 ms following the end of holdoff, the gate level at pin 3 steps LO to turn Q361 on, thus initiating a sweep.

Pin 4 is the auto gate terminal and is not used in this application. The pin is held at a positive level.

Pin 5 is the input terminal for the negative voltage supply. Zener diode VR383 provides some regulation of the negative supply at pin 5.

Pin 6 is the auto gate timing terminal. R380 and C380 determine the amount of time between the end of holdoff and the generation of the auto gate when no triggering signal is received. A feedback capacitor, C381, provides positive feedback to pin 6 from pin 4 to speed up the edge of the auto gate output at pin 3.

Pin 7 output illuminates the TRIG LED when a triggered gate has occurred.

Pin 8 is the holdoff timing terminal. An RC network connected to this terminal and selected by the A TIME/DIV switch (see diagram 9) determines the length of holdoff time. The digital holdoff signal, BHOF, holds this pin LO to disable the trigger until the digital holdoff time is completed.

Pin 9 is the ground terminal.

Pin 10 is the holdoff output terminal. The gate level present here is LO during sweep holdoff time and HI otherwise.

Pin 11 output illuminates the READY LED when operating in the single-sweep mode.

Pin 12 is the single-sweep mode terminal. When +5 V is applied to this terminal, the sweep operates in the single-sweep mode; when the terminal is left open or grounded, the sweep operates in the repetitive mode.

Pin 13 is not used in this application. The pin is grounded.

Pins 14 and 15 are the single-sweep reset terminals. Pushing the SINGLE SWP button prepares the single sweep circuitry to respond to the next triggering event and causes the READY LED to illuminate.

Pin 16 is the holdoff start input terminal. The HI sweep reset gate pulse from the sweep generators is applied here to initiate sweep holdoff. The digital holdoff signal is applied here to reset the sweep and Trigger Generator ICs.

Pin 17 is the sweep disable output terminal. The gate level at this terminal is HI during holdoff and LO otherwise. A HI gate level at pin 17 holds a reset level on the A and B Trigger Generator ICs (diagram 6) until holdoff time has elapsed. The gate goes LO at the end of holdoff to allow the Trigger Generators to respond to an input triggering signal.

Pin 18 is the sweep lockout input. When +5 V is applied to this terminal in the X-Y display mode, all sweep action is disabled.

Pin 19 is the auto mode terminal. Grounding this terminal enables auto sweep operation.

Pin 20 is the input terminal for positive supply voltage.

NON STORE Holdoff Timing

A resistor and capacitor network located in the A and B Timing Switch circuit (diagram 9) connects to U480 pin 8 via J550 pin 8. Various resistor and capacitor combinations switch into the circuit, depending on the setting of the A TIME/DIV switch. At sweep end, pin 16 of U480 receives a reset pulse, releasing pin 8. Now the timing capaciators in the holdoff timing network start to charge. A LO from U480 pin 10 biases Q477 off during the sweep holdoff time to allow the voltage at pin 8 to rise as the timing capacitors charge. When the charge on the capacitors rises to approximately +4 V at pin 8, pin 10 goes HI to turn

on Q477. The holdoff timing capacitors discharge rapidly through Q477, and pin 8 goes LO. At this time, the sweep disable output pin 17 also goes LO to remove the reset level from the A and B Trigger Generator ICs.

In the A and B Timing Switch circuit, C435, C437, C429, R431, and R432 are switch-selectable holdoff timing components that set the various timing holdoff ranges selected by the TIME/DIV switch. The A Trigger HOLDOFF control, R14498 (diagram 9), is a variable resistor that allows lengthening of the time constant to increase holdoff time for each holdoff range.

Digital Holdoff

When the storage feature of the instrument is in use, timing of the operation requires that the Storage Time Base circuitry has control of the sweep circuitry. A digital holdoff signal (BHOF) is applied to the Sweep Control IC to disable the Trigger and Sweep circuits until the necessary processing time has elapsed.

The rising edge of BHOF is coupled through C480 to forward bias CR488. A positive pulse is applied through CR488 to U480 pin 16 to reset the Sweep Control IC. The duration of the pulse is determined by the RC time constant of C480 charging through R487.

A HI BHOF signal also forward biases CR478 to supply base current to Q477 and saturate it. With Q477 on, U480 pin 8 is held LO to keep the sweep disabled until BHOF goes LO. When the digital holdoff time passes, Q477 is turned off and the holdoff RC network in the A and B Timing Switch circuitry can begin charging.

The circuit composed of Q481, Q482, Q483, and Q484 functions as a digital auto timer for the AUTO trigger mode of operation. During digital holdoff time, BHOF is HI and CR480 is forward biased. Saturation current flows in both Q483 and Q484, and C593 charges up to approximately +5 V. As C593 charges, the base voltage of Q482 rises until the transistor becomes saturated and Q481 is cut off. With Q481 off, pin 19 of the Sweep Control Logic IC, U480, will float HI to place the IC in its NORM trigger operating mode.

When BHOF goes LO, CR480 becomes reverse biased and both Q483 and Q484 turn off. Now C593 will discharge through R482 and R481 to reduce the forward bias on Q482 and eventually turn off the transistor. With Q482 off, Q481 becomes forward biased to place a LO on U480 pin 19, and the Sweep Control Logic IC goes into the AUTO trigger mode. The time interval between the end of the BHOF signal and the point that Q481 turns on permits a triggering signal to occur before an AUTO trigger is generated.

If either the NORM or SINGL SWP trigger mode of operation is selected, the base of Q483 is ungrounded. With the base of Q483 held forward biased through R591, the BHOF signal cannot switch Q483 off when it goes LO, and the Sweep Control IC will not generate an AUTO trigger.

A Sweep Holdoff Amplifier

The A Sweep Holdoff Amplifier is Q467. The holdoff gate waveform from U480 pin 17 is applied to the emitter of Q467 through CR470. When Q467 is turned off (during holdoff time), its collector is HI, thus placing a HI on the A Trigger Generator reset input (diagram 6). When U480 pin 17 goes LO at the end of holdoff time, Q467 is biased on, and its collector voltage goes LO to remove the reset level from the A Trigger Generator IC, U280. Once the reset level has been removed, the IC is allowed to respond to the next adequate triggering signal.

B Sweep Holdoff Amplifier

The B Sweep Holdoff Amplifier is Q266. Its circuit action is controlled both by the holdoff gate from U480 pin 17 (through CR471) and the collector current of Q182 in the Delay Pickoff Comparator. Both control sources must be in their LO state for the B Trigger Generator reset level to be removed. Either source in its HI state will keep Q266 biased off to hold a HI on the reset input of B Trigger Generator U445.

Delay Pickoff Comparator

A circuit composed of Q177, Q180, Q181, and Q182 is used to compare the A Sweep ramp voltage with the level set by the DELAY TIME POSITION potentiometer, R16002.

When B Sweep is enabled, Q181 is biased to supply a constant current to Q177. At the start of an A Sweep, the right half of Q177 is biased on, and the left half, with the level from the DTP control, is off. At the point that the A Sweep ramp runs down to meet the level from the DELAY TIME POSITION control, the left half of Q177 becomes forward biased and the right half turns off. Transistor Q182, in the collector circuit of the right side of Q177, will turn off and allow the emitter of Q266 to go LO. The reset level is removed from the B Trigger Generator when Q266 conducts, and the B Sweep either will start immediately if the STARTS AFTER DELAY B Trigger SOURCE is selected or will start when the next triggering signal occurs when any other B Trigger SOURCE is selected.

A Sweep Z-Axis Gate

The A Sweep Z-Axis Gate is an emitter-coupled bistable stage composed of Q294 and Q295. Only one of these transistors can be conducting. The controlling signals consist of inputs from: the collector of Q360 in the A Sweep Gate, the A Sweep Fast Blanking signal from Q986 in the A Sweep Generator circuit (via J550 pin 2), and Q791 in the Horizontal Display Logic circuit. The unblanking signal for use in the Z-Axis Amplifier is taken from the collector of Q295 through CR495. The collector signal of Q294 is applied to the A + Gate Emitter Follower, Q195.

The Horizontal Display Logic circuit controls the bias voltage on CR296. When the diode is reverse biased, as it is for all horizontal modes except B DLY'D, −8 V is connected to the anode of CR296 through Q791 (diagram 8). The gate signal at the collector of Q295 is allowed to pass through CR495 to create the unblanking signal to the Z-Axis Amplifier. In the B DLY'D mode, Q791 is turned off and CR296 is forward biased through R294 to the +5-V supply level. Now CR495 will be reverse biased, and the A unblanking signal is blocked from reaching the Z-Axis Amplifier. In the ALT Horizontal Display mode, CR296 will be reverse biased during the A sweep and forward biased during the B sweep.

B Sweep Z-Axis Gate

The B Sweep Z-Axis Gate is composed of transistors Q1006 and Q1007. These transistors form an emitter-coupled stage where only one transistor can be conducting at a time, as in the A Sweep Z-Axis Gate circuit. The controlling signals come from the collector of Q160 (B Sweep Gate), and the blanking signal from the collector of Q956 in the B Sweep Generator. The emitter current in the gate transistors is supplied partly by Q2008, which is controlled by B INTENSITY control R14398. The B INTENSITY control sets the level of the B Sweep unblanking signal to control the B Sweep intensity separately from the overall display intensity. The collector of Q1007 supplies the unblanking signal to the Z-Axis Amplifier, and the collector of Q1006 supplies the signal to the B + Gate Emitter Follower (Q1005).

When the A Horizontal display is selected, −8 V from Q790 in the Horizontal Display Logic circuit is applied to the cathode of CR390. This reverse biases CR392 and allows the collector of Q1007 to be pulled positive, through CR493 and R390, to the +5-V supply level. Diode CR494 will be reverse biased, and the B Sweep Z-Axis Gate (Q1006 and Q1007) will not affect crt unblanking. When either A INTEN, ALT, or B DLY'D Horizontal Display is selected, −8 V is supplied from S469 to the anode of CR493, reverse biasing it and allowing the Horizontal Display Logic circuit to control the B Sweep Z-Axis Gate.

In the A Intensified Horizontal Display mode, CR390 becomes reverse biased and CR392 becomes forward biased. Diode CR494 is still reverse biased, but when B Sweep starts, the collector of Q1007 steps negative enough to forward bias CR494, adding a slight amount of unblanking to the A Sweep unblanking already present. This provides further intensification for the B Sweep portion of an A Intensified display.

In the ALT Horizontal Display mode, the Horizontal Display Logic circuit controls the A Sweep Z-Axis Gate (Q294 and Q295) and the B Sweep Z-Axis Gate (Q1006 and Q1007). The B Sweep unblanking signal is added to the A Sweep unblanking signal during the A Intensified display. The A Sweep unblanking signal is blocked during the B DLY'D Sweep display. In B DLY'D Horizontal Display, the A Sweep Z-Axis Gate output diode CR494 is held reverse biased, and the only unblanking signal presented to the Z-Axis Amplifier input is the B Sweep unblanking signal.

A + Gate and B + Gate Emitter Followers

Emitter followers Q195 and Q1005 provide the A + Gate and B + Gate signals to trigger the Digital Storage Time Base. The positive-going gate signals are also made available from connectors on the instrument rear panel. The amplitude of the rectangular gate signals is set at the collectors of Q294 and Q1006 at approximately +5.5 V. When Q294 is conducting, the base of Q195 can go no more negative than approximately −0.7 V (limited by CR189). When Q294 is not conducting, the base of Q195 rises to the +5-V power supply level through R295. Diodes CR1000, CR1001, CR1100, and CR1101 protect Q195 and Q1005 from accidental application of damaging voltage levels to the A + Gate and B + Gate output connectors.

Horiz Alt Sync Pulse Amplifier

The pickoff amplifier for the Horiz Alt Sync pulse is Q183. Biased into saturation, its quiescent output voltage is approximately zero. A sample from the A + Gate is coupled to the base of Q183 by C284 where the positive-going gate is integrated by the action of C284 and R280. The positive-going portion of the integrated signal cannot increase the collector current of Q183 beyond its saturation level, so no signal output is obtained. When the A + Gate negative-going edge occurs, C284 cannot change its charge instantaneously and the entire negative transistion is impressed on the base of Q183 across R280. The negative peak of the signal is enough to cut off Q183, and the collector voltage rises in response to the base voltage decrease. The base voltage rapidly returns to a positive level, the transistor again saturates, and ends the Horiz Alt Sync Pulse.

A AND B SWEEP GENERATORS

The A and B Sweep Generators (diagram 8) produce sawtooth voltages which are amplified by the Horizontal Amplifier circuit to provide horizontal deflection on the crt for the nonstorage displays. These sawtooth voltages are produced on command (Sweep Start gate) from the Sweep Logic circuits. The Sweep Generator circuits also produce gate waveforms that are used by the Z-Axis Logic circuit to unblank the crt during sweep time and by the Sweep Logic circuit to terminate sweep generation. Figure 3-10 shows a detailed block diagram of the A Sweep Generator circuit that is described in the following paragraphs. Since the B Sweep Generator circuit is very similar to the A Sweep Generator, discussion of the B Sweep Generator is about the differences in operation between the two.

Disconnect Amplifier

After holdoff, but before the next sweep, Disconnect Amplifier Q890 is biased on and conducts through R888 and R_t back to $+V_t$. This sets the charge on C_t in preparation for the beginning of the next A Sweep and prevents current from the Miller Integrator circuit from changing the charge on C_t. When the positive-going A Sweep Start Gate is applied to the emitter of Q890, CR889 becomes forward biased and turns off Q890. Now the A Sweep starts, and the Miller Integrator circuit begins to change the charge on C_t. Disconnect Amplifier Q890 remains biased off until retrace is initiated and the A Start Sweep Gate is removed. Then Q890 will become forward biased again, and C_t will rapidly charge to its quiescent value for the start of the next A Sweep.

Sawtooth Generator

The Miller Integrator circuit is made up of Q891 and Q998. It works on the principle that if the charging current to a capacitor can be held constant, then the charging curve will be linear rather than exponential. The action starts when Disconnect Amplifier Q890 is turned off by the A Sweep Start Gate. The selected capacitor for the chosen setting of the TIME/DIV switch (C_t) begins to charge through the R_t. This causes the junction of C_t and R_t to start positive in the direction of $+V_t$, thereby causing the gate of Q891 to start positive. The Q891 source then starts in a positive direction and increases the forward bias on

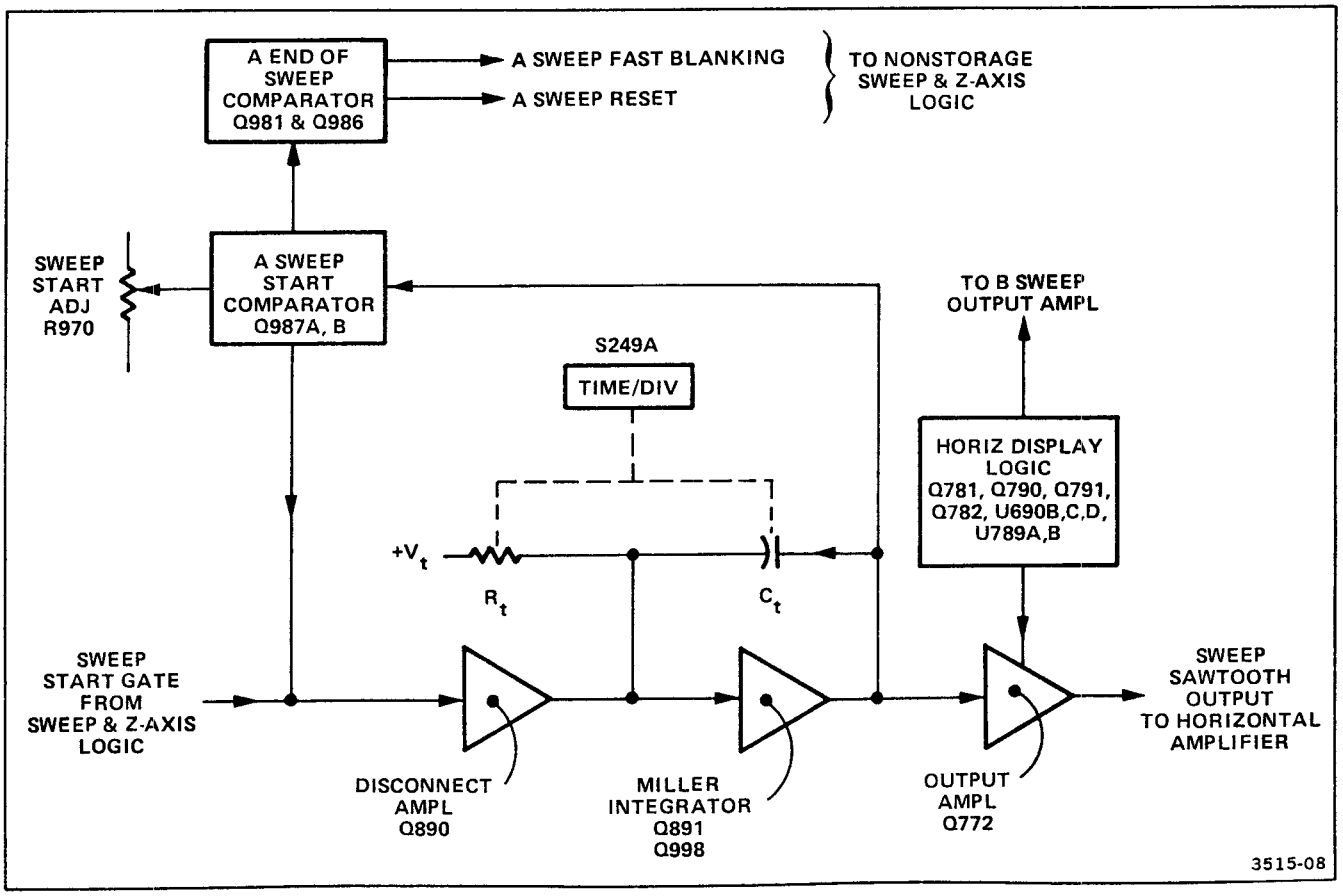

Figure 3-10. Detailed block diagram of the A Sweep Generator circuit.

Q998; causing the collector voltage to move in a negative direction (less positive). This couples back through C_t and opposes the positive change at the gate of Q891. Capacitor C_t is attempting to charge toward $+V_t$, but the action of both the Q891 gate being held virtually constant and the collector of Q998 going more negative results in reduction of the charge on C_t (it discharges). The gate of Q891 rises positive about 10 mV over the entire sweep generation time. Since the voltage at the gate of Q891 remains relatively constant, both the voltage across R_t and the current through R_t (current discharging from C_t) remain constant. The linear rate of discharge of C_t results in a linear ramp across it. The resultant output at the collector of Q998 appears as a negative-going ramp, dropping from approximately +13 V to approximately +2 V.

When the ramp reaches +2 V, Q981 sends a pulse to U480 to initiate retrace. Transistor Q890 turns on, and its collector goes more negative. The gate of Q891 moves in the negative direction, causing the voltage on the base of Q998 to go more negative and its collector voltage to go more positive. Now C_t charges rapidly through Q890 to its quiescent state in preparation for the next A Sweep start gate.

Output Amplifier

Output Amplifier Q772 is a common-base amplifier with the signal current-driven into the emitter. It provides the output sawtooth current signal to the Horizontal Amplifier and a measure of isolation between the Sawtooth Generator and the Horizontal Amplifier. The Horizontal Display Switching circuit connects to this stage and controls the A sawtooth output in the various horizontal modes of operation. In the A and A INTEN modes of operation, the A sweep signal passes through Q772 to the Horizontal Amplifier. In the ALT mode, Q772 is enabled for the A sweep and turned off for the B sweep by the Horizontal Display Logic circuit. In the B DLY'D mode, Q772 is held off, and Q760 in the B Sweep Generator is held on, passing the B sweep sawtooth to the Horizontal Amplifier.

For stored waveform displays, both the A and B sawtooth outputs are not allowed to pass to the Horizontal Amplifier, and the horizontal deflection signal is supplied by the digital storage X-Axis circuitry (diagram 16).

A Sweep Start Comparator

Just before the sweep starts to run down, the levels at the bases of Q987A and Q987B are approximately equal. When the sweep starts to run down, the base of Q987B goes negative, following the collector of Q998. The forward bias on CR984 increases, which in turn decreases the forward bias on CR980. Very shortly after start of the sweep, CR980 becomes reverse biased and interrupts the current through Q987A. The circuit remains in this condition until after the sweep retrace is complete. When the circuit returns to quiescence, Q987A again begins to conduct through R888, thereby setting the current available to Disconnect Amplifier Q890 and establishing the starting point of the sweep. Sweep Start adjustment R970 is used to set the base voltage of Q987A. The sweep start level is also applied to the base of Q958 in the B Sweep Start Comparator to ensure that the B sweep starts at the same level as the A sweep.

A Sweep End of Sweep Comparator

The A Sweep End-of-Sweep Comparator is a switching circuit composed of Q981 and Q986. At quiescence, Q986 is conducting and Q981 is biased off. When the sweep starts to run, the negative-going ramp at the collector of Q998 is coupled through the base of Q987B and through CR984 to the cathode of CR975. When the collector of Q998 reaches about +2 V, the cathode of CR975 reaches about +4 V. At this point, CR975 begins conducting to turn on Q981, which then turns off Q986. The resulting positive step at the collector of Q981 is fed to U480 pin 16 where it is used to initiate retrace and holdoff. The negative-going pulse at the collector of Q986 is applied to the A Sweep Z-Axis Logic Gate to blank the crt as soon as a sweep-end command is generated.

B Sweep Generator Differences

The B Sweep Generator differs from the A Sweep Generator in two respects. The first is that Q946 is used as a constant-current source in the B Sweep Start Comparator circuit. The second is that one of the outputs of the B Sweep Generator is controlled by the B ENDS A switch associated with the A Trigger HOLDOFF control. In the B ENDS A position, the end of the B sweep resets the Sweep Control IC (diagram 8) to also end the A Display on the crt.

Horizontal Display Logic

The Horizontal Display Logic circuit produces the signals that switch both the A and B Sweep Generator outputs and the A Sweep and B Sweep Z-Axis Gates. The circuit also provides a Vertical Alt Sync pulse to the Vertical Switching circuitry. In addition, an enabling voltage is produced via VR695 to allow the Trace Separation circuitry to function for ALT Horizontal Displays.

VERT ALT SYNC PULSE. A gating circuit is formed by U690B and U690D to control the Vertical Alt Sync pulse. The pulse is used in the Vertical Switching circuit for clocking U409 whenever the ALT Vertical Mode is selected. In all Horizontal Display modes except ALT, a HI at U690B pin 6 will put a LO at U690D pin 3. The positive-going Horiz Alt Sync pulse is applied to U690D pin 2. The

pulse is inverted through U690D and fed to the Vertical Switching circuit at U509A, pin 1 (diagram 3). In ALT Horizontal Display mode, pin 6 of U690B will be LO, and the signal at pin 5 will control the output at pin 4. The signal present at U789A pin 6, which changes state with every Horiz Alt Sync pulse, now controls U690D, and the Vert Alt Sync pulse becomes a rectangular pulse having a period equal to twice the time between Horiz Alt Sync pulses.

TRACE SEPARATION. During the B Sweep time the TRACE SEP potentiometer is used to supply an offset signal to Q205 and Q206 (in the Vertical Output Amplifier circuitry) for controlling the vertical separation between the A trace and the B trace. During B Sweep, in ALT Horizontal Display mode, a HI will be present on pin 4 of U690B. The HI forward biases Q108 (diagram 5) on and enables the Trace Separation circuitry. See the "Vertical Output Amplifier" circuit description for a discussion of the Trace Separation circuitry.

A AND B SWEEP SWITCHING. Flip-flop U789A controls Horizontal Display Switching transistors Q782 and Q781 in the A and B Sweep Generators. HORIZ DISPLAY switch S469 sets the flip-flop to perform one of the following actions:

1. Turn off Q781 and turn on Q782, allowing the A Sweep signal to go to the Horizontal Amplifier;

2. Turn off Q782 and turn on Q781, allowing the B Sweep signal to go to the Horizontal Amplifier; or

3. Alternately turn the two transistors off and on to display both sweeps in Alt Horizontal Display mode.

During a stored waveform display, a Sweep Disable signal is applied to both the set and reset input of U789A through CR471 and CR374. The Q and $\overline{Q}$ outputs of U789A go HI, and both sweep switching transistors will be biased on to shunt the A and B Sweep current to ground.

Flip-flop U789A is clocked by the Horiz Alt Sync pulse when the Horizontal Display is set to ALT. When the Horizontal Display is set to A, A INTEN, or B DLY'D, the state of the outputs of U789A is determined by the logic levels present at pins 1 and 4. The HORIZ DISPLAY switches set these logic levels.

Flip-flop U789B controls the A and B Sweep Z-Axis Gate switching transistors Q791 and Q790. These transistors switch the bias on CR390 and CR296 in the A and B Sweep Z-Axis Gates to either allow the unblanking gates to pass to the Z-Axis Amplifier or block them. U789B is controlled by both the signal on U789A pin 5 and the A position of the HORIZ DISPLAY switch.

A AND B TIMING SWITCH

The components shown in diagram 9 include the cam activated switch contacts that select the timing components for the A and B Sweep Generator circuits. Added switch contacts on cam segments 21 through 25 of the A TIME/DIV switch and contacts 16 through 20 of the B TIME/DIV switch supply a binary input signal to A and B TIME/DIV Registers in the Vertical Mode Switch circuitry (diagram 4). The registers are read at regular intervals by the Microprocessor to determine if a timing change is required for the stored waveform display.

Many of the adjustments for both the A and B Sweep timing calibration are located in the A and B Timing Switch circuitry.

HORIZONTAL AMPLIFIER

The Horizontal Amplifier circuitry (Figure 3-11 and diagram 10) provides the output signals that drive the horizontal deflection plates of the crt. The source of the signal applied to the input of the Horizontal Amplifier is determined by the TIME/DIV switch, the HORIZ DISPLAY switch, and the digital STORAGE MODE switches. The deflection signal can come from either of the sweep generators within the instrument, from the CH 1 OR X input connector (X-Y mode), or from the digital storage horizontal display system (if operating the instrument in a storage mode).

Horizontal positioning controls, X10 magnifier circuitry, and the horizontal portion of the beam finder circuitry are also contained in the Horizontal Amplifier.

X-Axis Amplifier

The sawtooth horizontal deflection signals to U564A and U564B come from either the A or B Sweep Generator (nonstorage mode) or the Storage Display X-Axis output (when operating the instrument in a storage mode). However, in the nonstorage mode, when the X-Y position of the A TIME/DIV switch is selected, the signal applied to U564A and U564B comes from the Channel 1 Preamplifier via the X-Axis Amplifier. The X-Axis Amplifier is composed of Q582, Q583, and associated components.

Transistor Q582 is connected as a feedback amplifier, with R486 as the feedback element. The input resistance of the amplifier is made up of R679 and the gain-setting adjustment of R681. When not operating in the X-Y mode, the base of Q582 rises toward the +15-V supply, but the base is clamped at approximately +5.7 V by CR587 and R587. The base-emitter junction of Q582 is reverse biased.

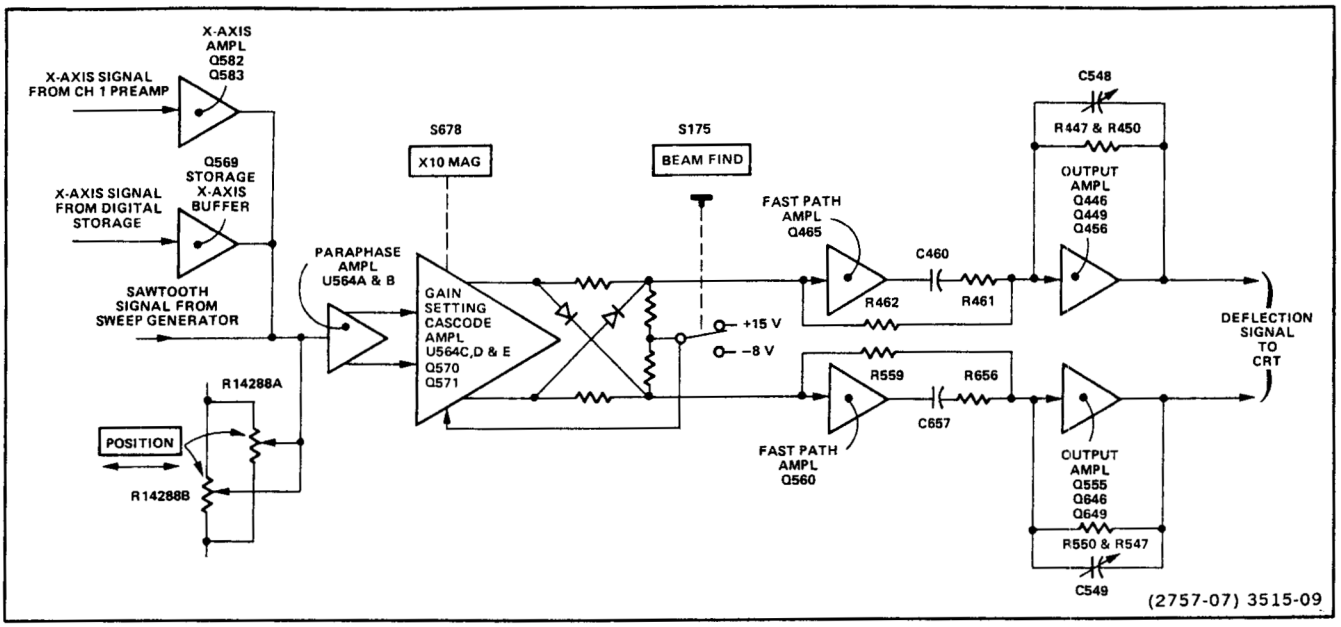

Figure 3-11. Detailed block diagram of the Horizontal Amplifier circuit.

The base of Q583 also rises to approximately +5.7 V and is biased off.

When the A TIME/DIV switch is set to X-Y (fully counterclockwise), −8 V is applied to the junction of R682 and R683. In addition, +5 V is applied to the emitter circuit of Q583, through CR486, to bias the X-Axis Amplifier into conduction. Diode CR679 is now forward biased to allow the X-Axis signal to pass to the base of Q582. The +5 V is also applied via P970 pin 4 and J550 pin 4 to U480 pin 18 in the Sweep and Z-Axis Logic circuit, disabling sweep generation during the X-Y function display.

Input Paraphase Amplifier

The Input Paraphase Amplifier is composed of U564A and U564B (part of a transistor array). The transistors form an emitter-coupled amplifier stage that converts the single-ended input signal to a differential output signal. The signal at the collector of U564A is opposite in phase to the input signal, while the signal at the collector of U564B is in phase with the input signal. Temperature compensation for U564A and U564B is provided by RT672 which varies in resistance value with changes in ambient temperature.

Horizontal POSITION potentiometers R14288A (coarse) and R14288B (fine) are mounted on the same shaft in a mechanical arrangement that allows R14288B to rotate about one-eighth turn in either direction before R14288A moves. The fine potentiometer has approximately one-tenth the positioning range of the coarse potentiometer.

Gain Setting Cascode Amplifier

A cascode, push-pull amplifier stage composed of Q570, Q571, U564C, U564D, and associated circuitry provides the current drive to the output stage and sets the overall gain of the Horizontal Amplifier circuit. The gain of the Cascode Amplifier is controlled by adjusting the resistance connected between the emitters of Q570 and Q571. The X1 Gain adjustment, R572, is used to adjust the unmagnified horizontal gain, and the X10 Gain adjustment, R571, is used to adjust the magnified horizontal gain. Magnifier Registration adjustment R578 is used to balance the quiescent dc current in Q570 and Q571 so that a center screen display does not change position horizontally when switching between magnified and unmagnified display.

The horizontal portion of the Beam Finder circuitry is activated when the BEAM FIND push button is pressed in. The +15 V is disconnected from the junction of R464 and R655, and −8 V is applied at that junction through R273. This causes the following circuit actions to occur:

1. The base voltage of U564C and U564D is lowered, thus decreasing the current through the two transistors. The reduced current flow decreases the voltage drop across R463 and R558, and the diode clamps (CR560 and CR561) clamp at a much lower voltage to limit the horizontal deflection on the crt; and

2. Less current flows through R464 and R655 to compensate for the decreased current flowing through U564C and U564D. This maintains the output stage in a linear operating region.

Output Amplifier

The differential signal from the Gain Setting Cascode Amplifier is directly connected to the bases of Q465 and Q560. It is also applied to the bases of Q456 and Q455 through R462 and R559. At lower sweep frequencies, the signal path is through R462 and R559 to the bases of Q456 and Q555. These transistors are arranged as inverting amplifiers whose collector signals drive the emitters of complementary amplifiers Q446-Q449 and Q646-Q649, respectively.

Capacitor C555 provides emitter peaking for fast ac signals. Capacitors C450 and C644 transfer part of the high-frequency signal to the emitters of Q446 and Q646 to maintain the gain of the output stage at high sweep speeds. Resistors R447-R450 and R547-R550 are the feedback elements, with C548 and C549 providing high-frequency compensation.

As the frequency of the sweep signal increases, the reactance of C548 and C549 decreases and feedback current increases. To compensate for the increase in drive required to maintain the gain of the output stage, Q465 and Q560 (fast-path amplifiers) increase signal current to the bases of Q456 and Q555. High-frequency signal current is shunted around R462 by C460 and R461, while C657 and R656 shunt high-frequency signal current around R559.

The Output Amplifiers are limited from being overdriven by CR560 and CR561. If the output signal from U564C and U564D becomes too large, the diodes become forward biased and prevent further increase in the signal level. These diodes operate mainly to clamp the signal whenever the X10 Magnification function is in use. The signal level is limited to the forward drop across the diodes plus the drop across R463 and R558.

CRT CIRCUIT

The CRT circuit (Figure 3-12 and diagram 11) provides the voltage levels and control circuitry necessary for operation of the cathode-ray tube.

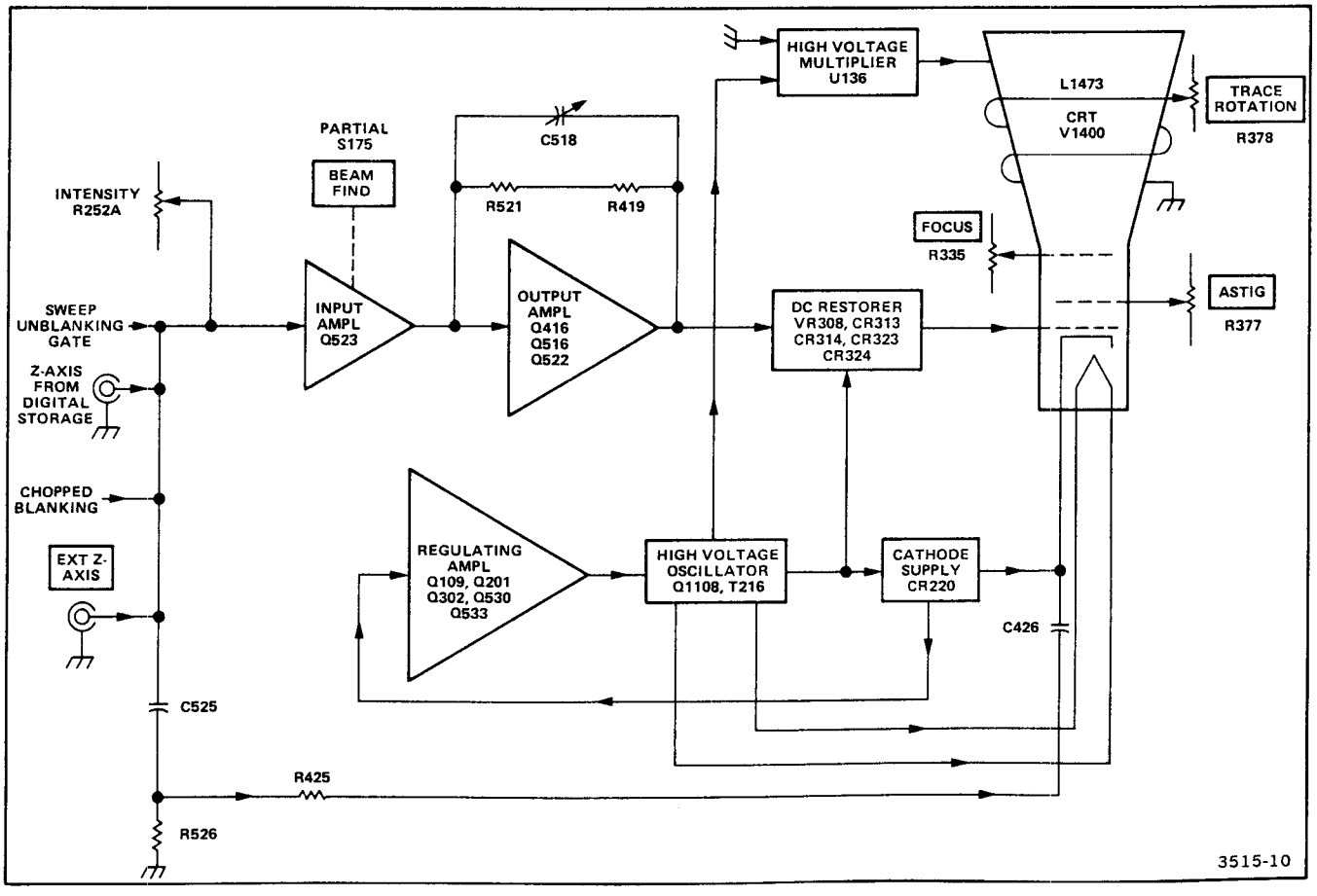

Figure 3-12. Detailed block diagram of the CRT and Z-Axis Amplifier circuits.

High-Voltage Oscillator

The high-voltage oscillator includes Q1108 and associated circuitry. It produces the drive for high-voltage transformer T216. When the instrument is turned on, transistor Q109 is forward biased and conducts through the base circuit of Q1108 to forward bias Q1108. The increasing collector current of Q1108 through the primary winding of T216 induces a voltage across the positive feedback winding, pins 6 and 7. The positive feedback to the base of Q1108 causes the collector current to rapidly increase toward saturation. Soon the rate of increase slows to a point where the voltage induced in the positive feedback winding starts to decrease. Then the current through Q1108 decreases, further decreasing the feedback voltage. The circuit action continues until Q1108 turns off, and the magnetic field around the primary winding of T216 starts to collapse. Transistor Q1108 is held off until the field has collapsed sufficiently to allow the base of Q1108 to become biased into conduction again, and the cycle is repeated as the circuit oscillates.

The voltage waveform at the collector of Q1108 is a sinusoidal wave at the resonant frequency of T216. The amplitude of sustained oscillations depends on the average current delivered to the base of Q1108. Frequency of oscillation is approximately 50 kHz. Fuse F809 protects the unregulated +15-V supply in the event the High-Voltage Oscillator stage becomes shorted. The stage is decoupled from the unregulated +15-V supply by C108 and L107 to prevent current changes (in the High-Voltage Oscillator stage) from affecting the +15-V supply.

High-Voltage Regulator

After the instrument is turned on and the output voltage from the High-Voltage Oscillator has reached its stable level, regulation occurs as follows. A sample of the −2450-V crt cathode voltage supply is applied to the base of Q530 through R429D which, with the voltage supplied by the bias network (R633, R429C, C629, and CR631), sets the forward bias on Q530. Any change in the −2450 V changes the conduction level of Q530 to produce a proportional dc change on its collector current.

Assume that the −2450-V supply starts to go positive (less negative). The positive-going change is applied to the base of Q530 to cause the collector current to increase, which in turn causes Q533 and Q109 to conduct harder. A resulting greater bias current is applied to the base of Q1108 through the feedback winding of T216. Now Q1108 is biased closer to its conduction level, and it will start conducting sooner in the oscillation cycle of T216, increasing the average current delivered to the primary of T216. The increase in the amplitude of oscillation induces a larger voltage into the high-voltage secondary of T216 to correct the original positive-going change. By sampling the output of the crt cathode supply in this manner, the total output of the High-Voltage Supply is held relatively constant.

Overvoltage protection is provided by Q201, Q302, and associated circuitry. Normally Q201 and Q302 are biased off, but if the crt cathode supply voltage approaches approximately −3000 V, the voltage level at the emitter of Q109 will be approximately −6 V. At this point Q201 will be biased into conduction, which in turn biases Q302 into conduction to reduce the forward bias on Q109. Thus, the base drive to Q1108 is reduced, limiting the amplitude of oscillations in T216, and the crt cathode supply is prevented from going more negative than approximately −3000 V.

High-Voltage Rectifiers and Output

High-voltage transformer T216 has two secondary windings. One winding provides heater voltage for the cathode-ray tube. The heater voltage is supplied from the High-Voltage Supply, since the cathode-ray tube has a very low heater current drain. This allows the cathode and heater of the crt to be connected together to prevent cathode-to-heater breakdown. The high-voltage secondary winding is the source for both the negative crt cathode potential and High-Voltage Multiplier U136.

A sample of the signal in the high-voltage winding is applied to a dc restorer circuit. The sample level and dc levels supplied by both the Z-Axis Amplifier and the crt negative cathode potential set the crt grid bias voltage.

The positive accelerating potential is supplied by High-Voltage Multiplier U136. Regulated output voltage is approximately +15,500 V. The negative cathode potential of −2450 V is supplied by half-wave rectifier CR220.

CRT Control Circuits

Focus of the crt display is controlled by FOCUS control, R335. ASTIG adjustment R377, which is used in conjunction with the FOCUS control to provide a well-defined display, varies the positive level on the astigmatism grid. Geometry adjustment R267 varies the positive level on the horizontal deflection plate shields to control the overall geometry of the display.

Two adjustments control the trace alignment by varying the magnetic field around the crt. The Y-Axis adjustment, R270, controls current through L14175 to affect the crt beam after vertical deflection but before horizontal deflection. Therefore, it affects only the vertical (Y) components of the display. The TRACE ROTATION adjustment, R378, controls current flow through L14176 and affects both vertical and horizontal alignment of the trace.

Z-Axis Amplifier

The Z-Axis Amplifier circuit controls the crt intensity level via several input signal sources. The effect of these input signals is to either increase or decrease the trace intensity or to completely blank portions of the display. Input transistor Q523 is a current-driven, low-input-impedance amplifier. It provides proper termination for the input signals and isolates the input signals from the following stages. Current signals from the various control sources are connected to the emitter of Q523, and the algebraic sum of these signals determines the collector conduction level.

Transistors Q522, Q516, and Q416 are configured in a feedback amplifier arrangement, with R419 and R521 as feedback elements. The high-frequency compensation for the circuit is provided by C518. Emitter follower Q522 provides the drive to complementary amplifier Q516-Q416. Diodes CR622, CR517, and CR414 provide protection to the circuitry feeding the Z-Axis Amplifier in the event of high-voltage arcing.

The Z-axis portion of the Beam Find circuit acts on the input to the Z-Axis Amplifier. When the BEAM FIND push button is pressed, two events occur: First, +15 V is applied to the anode of CR437 which lifts the emitter of Q523 sufficiently positive to ensure cutoff of the transistor. Second, R621 connects to −8 V through R619 to establish a fixed and predetermined unblanking level at the output of the amplifier. Thus the INTENSITY control and all of the input unblanking signals have no control over the intensity level of the crt display whenever the BEAM FIND push button is pressed, and a bright trace will be displayed.

DC Restorer

The DC Restorer circuit provides crt control grid bias and couples both dc and low-frequency components of the Z-Axis Amplifier unblanking signal to the crt control grid. This circuit allows the Z-Axis Amplifier output to control the intensity of the crt display. The potential difference between the Z-Axis Amplifier output and the control grid (about 2465 V) prevents direct signal coupling.

The DC Restorer circuit's ac drive is taken from the center tap of T216. Voltage on the center tap is approximately 300 V p-p to 50 kHz. A sample of this sinusoidal voltage is fed through C210 and R313 to the junction of CR313, CR314, and R312. CRT Bias Adjust R409 sets the voltage level on the cathode of CR313 to approximately +100 V. When the ac sample voltage rises to +100 V, CR313 becomes forward biased and clamps the junction of CR313 and CR314 to approximately +100 V.

The Z-Axis Amplifier output voltage level is applied via R316 to the anode of CR314. This voltage level varies between +15 V and +95 V, depending on the setting of the INTENSITY control. The sample voltage will hold CR314 reverse biased until the voltage falls below the Z-Axis Amplifier output level. At that point CR314 becomes forward biased and clamps the junction of CR313 and CR314 to the Z-Axis Amplifier output level (Figure 3-13). Clamping the sample between +100 V and the positive voltage level set by the INTENSITY control produces an approximate square-wave signal with a positive dc offset level.

The DC Restorer circuit is referenced from the −2450 V, crt cathode voltage, through R327 and CR324 to the junction of C318 and CR323. Initially C318 will charge to a level determined by the difference between the Z-Axis Amplifier output level and the −2450-V reference voltage. The charging path is from the −2450-V line, through R327, CR324, C318, R312, CR314, and R316 to the Z-Axis output.

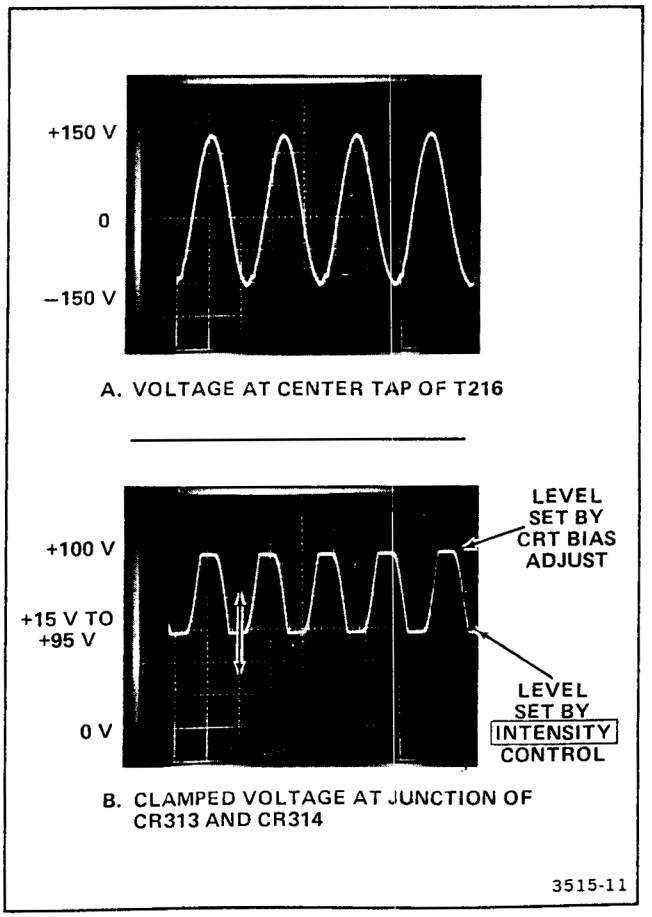

Figure 3-13. DC Restorer ac drive signal.

Initially, C319 will also be charged to approximately the same voltage as C318, through R327, CR324, and CR323 to the Z-Axis output.

When the sinusoidal sample voltage starts its positive transition from the lower clamped level (+15 V to +95 V) toward the higher clamped level (+100 V), the charge on C318 increases due to the rising voltage at the anode of CR313. The additional charge acquired by C318 is proportional to the amplitude of the positive transition of the clamped sample voltage.

When the sample voltage starts its negative transition from its upper clamped level toward its lower clamped level, the negative transition is coupled through C318 to reverse bias CR324 and forward bias CR323. When CR323 becomes forward biased, the charge on C318 is transferred to C319 as C318 attempts to discharge to the Z-Axis output. The amount of charge that is transferred depends on the setting of the INTENSITY control because the INTENSITY control sets the lower clamping level of the sample voltage from T216 (Figure 3-14).

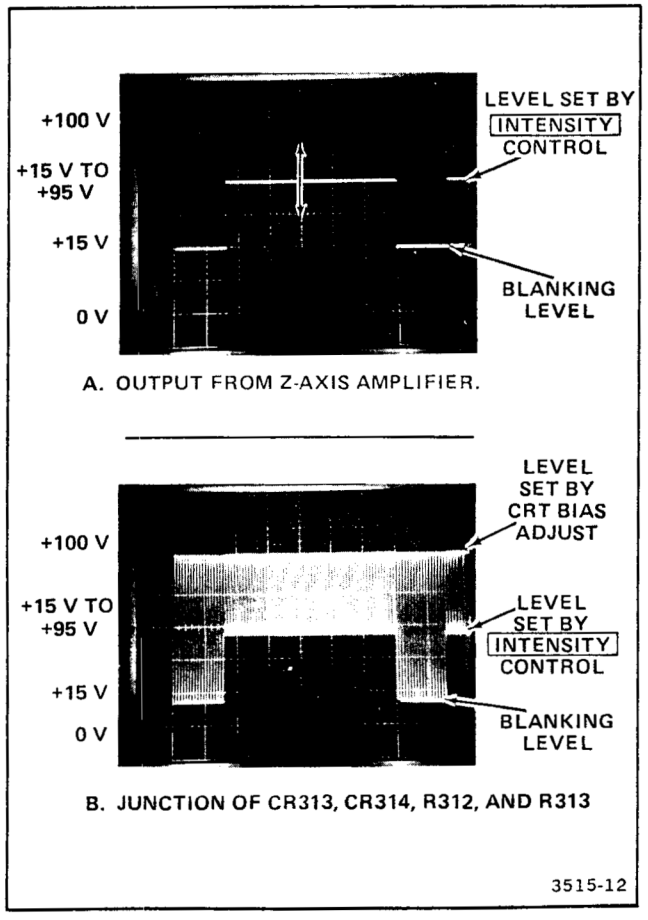

Figure 3-14. Effect of Z-Axis output on the DC Restorer signal.

If the INTENSITY control is set so the lower level of the sample voltage is clamped at +15 V, a voltage change of approximately 75 V is coupled through CR323. The 75-V negative excursion is added to the charge already present on C319. This causes the control grid to be sufficiently negative with respect to the crt cathode to keep the crt blanked. When the INTENSITY control is set to increase the display intensity, the lower clamping level of the sample voltage is moved toward the +100-V upper clamping level. This action reduces the swing of the negative transitions, therefore less charge will be added to C319. The voltage on the crt control grid becomes less negative with respect to the cathode and allows more beam current to flow in the crt. A more positive lower clamping level causes a brighter trace on the crt.

During periods that C318 is charging, the voltage on the control grid is held constant by the filter action of C319 as it discharges through R325 back to the −2450-V line. The resistance value of R325 is very high, so the RC time constant of C319 and R325 is long with respect to the frequency of the sample voltage from T216. Whatever charge is leaked off of C319 during the positive transitions of the sample voltage will be replaced by C318 when the sample voltage makes its negative transitions.

The fast rise and fall of the unblanking pulses from the Z-Axis Amplifier are coupled by C314 to the control grid to start the crt beam current change. The DC Restorer output level then follows the Z-Axis output level to set the new bias level on the control grid.

In the event of a failure that causes a loss of potential on either the control grid or the cathode, protection against internal arcing in the crt is provided by DS323 and DS324.

CALIBRATOR

The Calibrator circuit (Figure 3-15 and diagram 12) produces a square-wave output signal with accurate voltage and current amplitudes. The output signal is available as both a voltage and a current at the CALIBRATOR current loop on the instrument front panel.

Multivibrator

Transistors Q380 and Q396 and associated circuitry are configured as an astable multivibrator. The basic frequency of the multivibrator is approximately 1 kHz and is primarily determined by the resistance and capacitance of C486, R387, R391, R385, and R386. Transistors Q380 and Q396 alternately conduct, producing a square-wave output signal taken from the collector circuit of Q396.

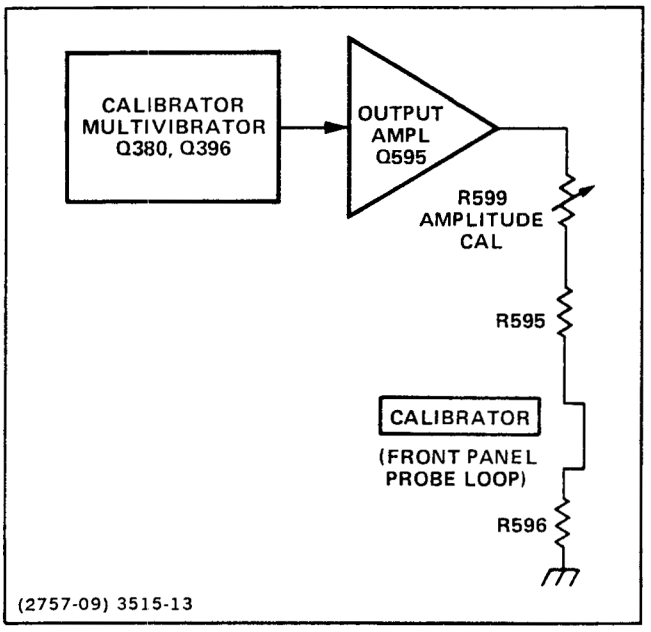

Figure 3-15. Detailed block diagram of the Calibrator circuit.

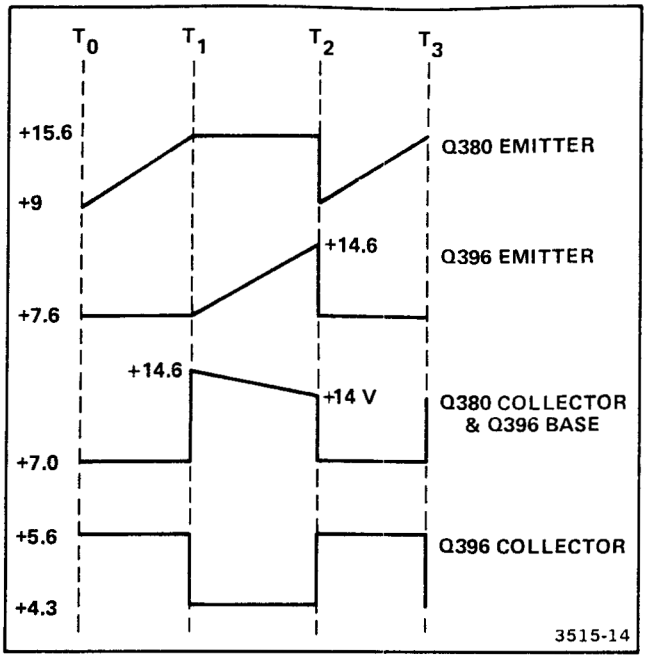

Figure 3-16. Calibrator circuit waveform diagram.

Refer to Figure 3-16 for the following discussion. At T_0 assume that the circuit has reached its normal operating conditions. Also assume Q380 is off and Q396 is on. At T_0 the emitter of Q380 is at approximately +9 V, and the emitter of Q396 is at +7.5 V, with its base at approximately +7.0 V. From T_0 to T_1, C486 charges toward the +55-V supply through R387. When the emitter of Q380 reaches +15.6 V, Q380 becomes forward biased. At T_1 the collector of Q380 rises to approximately +14.6 V, and since the base of Q396 is directly connected to the collector of Q380, Q396 is cut off.

Now C486 charges in the opposite direction. At T_1, as C486 starts charging through R391 and Q380, the emitter of Q396 rises from +7.6 V to approximately +14.6 V. When +14.6 V is reached at T_2, Q396 begins to conduct. This action reduces both the charging current through C486 and the collector current of Q380. At T_2 the collector voltage of Q380 drops in a negative direction, and Q396 conduction increases. The emitter of Q396 drops from +14.6 V to +7.6 V. This negative voltage transition is coupled through C486 to the emitter of Q380 to cut Q380 off, and the cycle just described is repeated.

Output Amplifier

The output signal from the Multivibrator drives Output Amplifier Q595 to produce a square wave at the output. When the base of Q595 goes positive, the transistor is cut off, and the collector voltage drops to zero. When the base goes negative, Q595 is biased into saturation, and the collector voltage rises in a positive direction to about +5 V. Amplitude calibration adjustment R599 is used to control the amount of resistance between the collector of Q595 and ground to control the amount of current allowed to flow. This in turn determines the voltage developed across R596. When the output voltage at the CALIBRATOR current loop on the instrument front panel is adjusted to 300 mV ±1 percent, the output current is 30 mA ±2 percent.

A/D CONVERTER AND CHANNEL SWITCH

The acquisition channel(s) used to obtain the waveform data is selected by Channel Switch U328 (diagram 13), and converted from a balanced signal to a single-ended signal before being digitized. Digitization occurs in A/D Converter U456 to produce a parallel, eight-bit digital output. A functional block diagram of the A/D Converter and Channel Switch circuitry is located in the "Diagrams" section of Volume II of this manual.

Channel Switch

A circuit composed of U328, Q336, Q333, Q327, and Q326 performs the channel switching, gain, and position functions for the vertical input signals. Channel Switch U328 is controlled by the ADD and $\overline{\text{CHAN1}}$ signals from the Time Base (diagram 19). See Table 3-3 for a listing of the switching logic and output functions.

Table 3-3

Channel Switch Control Logic

ADD	$\overline{\text{CHAN1}}$	OUTPUT SIGNAL
0	0	CH 1
0	1	CH 2
1	0	ADD (CH 1 + CH 2)
1	1	Not Selected

The Channel Switch provides high impedance differential inputs (pins 2 and 15 for CH 1; pins 8 and 9 for CH 2) for the vertical input signals. Proper 50-ohm termination of the signal lines from the Vertical Preamplifiers (diagrams 1 and 2) is provided by R331 and R332 for Channel 1 and by R326 and R327 for Channel 2. A differential output signal current is obtained from U328 at pins 12 and 13.

Adjustable current sources, composed of Q336 and Q333 for CH 1 and of Q327 and Q326 for CH 2, set the dc quiescent current for the Channel Switch. The sum of the differential output currents at U328 pins 12 and 13 is equal to the sum of the CH 1 and CH 2 position differential input currents at pins 1, 8, 9, and 16; the dc bias current to the A/D Converter Driver Amplier remains constant regardless of the channel selection.

Vertical positioning of the CH 1 input signal is accomplished by varying the differential output current of Q333 and Q336. The front-panel Vertical POSITION control output voltage is applied to a unity-gain buffer on the Storage Display board (diagram 16) to generate a vertical positioning signal (POS1). When varied, the single-ended POS1 signal applied to the base of Q336 produces a changing differential output current applied to U328 at pins 1 and 16. The differential position current is added to the CH 1 vertical signal current to change the CH 1 + and CH 1 – output dc levels, thus positioning the CH 1 signal.

Vertical positioning of the CH 2 signal is accomplished in an identical manner by Q326 and Q327 in the CH 2 Position circuit using the POS2 signal.

Channel gain of the CH 1 input is adjustable with potentiometer R335 which is in series with fixed resistance R333. The CH 2 gain adjust potentiometer is R420.

Switching between the CH 1 and CH 2 input signals is controlled by the $\overline{\text{CHAN1}}$ signal from Time Base Chop Drive flip-flop U150B (diagram 19). When CHOP Vertical Mode is selected, U328 output is switched between CH 1 and CH 2 at one-half the SAVE clock rate determined by the Time Base circuitry. Otherwise, the Chop Drive flip-flop is controlled by the Microprocessor via the Acquisition Mode Register (diagram 19) to select the appropriate channel signal for acquisition.

Selecting ADD Vertical Mode for acquisition of waveform data produces the ADD control signal from Time Base Acquisition Mode Register U236 pin 12. When ADD is HI, the differential output of U328 is the algebraic sum of the CH 1 and CH 2 vertical input signals.

A/D Converter Driver Amplifier

An amplifier stage composed of Q221, Q224, Q225, Q324, Q210, and Q115 converts the differential output current from U328 into a single-ended voltage used to drive the A/D Converter. Input transistors Q221 and Q224 form a common-base differential amplifier that presents a low-impedance load for the output current of Channel Switch U328.

Output current from the collector of Q221 is applied to the base of Q225, a shunt-feedback inverting amplifier. The inverted output signal voltage from Q225 is developed across R219 in the collector circuit, with L219 providing high-frequency peaking. The output signal of Q224 is developed across R220 in series with the signal developed across R219. The two signals add at the collector of Q224 to produce a single-ended replica of the differential input signal.

Components R315 and C315, in parallel with R220, provide step-response thermal compensation for the amplifier. Constant bias current is supplied to the Driver Amplifier by a circuit comprised of Q324 and associated components.

The single-ended vertical signal from the collector of Q224 is applied to the base of emitter-follower Q210. The emitter follower supplies the current drive to A/D Converter U456. A constant-current load for Q210 is provided by Q115 and associated components. Diode CR315, between the collector of Q221 and the collector of Q224, limits the peak voltage applied to the base of Q210. Compensation of the vertical signal line to the A/D Converter analog input is provided by potentiometer R271.

The storage NORM trigger signal is obtained from the collector circuit of Q224 via emitter-follower Q236. Potentiometer R126 is used to adjust the Storage NORM trigger dc level.

A/D Converter

The A/D Converter is an eight-bit parallel-output device, capable of digitizing an analog input signal with a sampling rate ranging from 10 Hz to 25 MHz. The rising edge of the CONVERT signal from the Time Base Sample Rate Timing Generator enables the internal comparators to make a 225-level comparison of the input signal. A 255-to-8 encoder produces an eight-bit parallel output on the falling edge of the CONVERT signal, and on the next rising edge of the CONVERT signal the eight data bits are transferred into the internal output latch circuit of the A/D Converter.

Since the output of the internal encoding circuit does not start changing to new data immediately, a new sample may be obtained on the same CONVERT rising edge that transfers the previous conversion data into the output latch. An additional delay is encountered before the digital output responds to input changes. The overall result is that the digital output data is read two sample times later than the input analog signal is sampled.

The output digitized waveform is applied to an input latch in the Acquisition Memory (diagram 14) to be processed for storage.

Reference Voltage

A −2.0-V reference voltage required for operation of the internal A/D comparators is developed by a circuit composed of U274, U264, Q260, and associated components.

The +2.5-V reference output from U274 is applied to the inverting input of U264. The output voltage from U264 is held to −2 V by the negative feedback current through R266. Additional current-handling capability is provided by emitter-follower Q260 at the output of U264. Reference voltage is applied to U456 pin 22 at the bottom of a resistive voltage divider within the A/D Converter. The resistive divider provides 255 different reference levels for comparison with the input analog signal.

The top of the reference divider string is grounded at U456 pin 11, and bypass capacitor C266 shunts hf noise away from the reference input to ground.

ACQUISITION MEMORY

The Acquisition Memory (diagram 14) is a dual-function circuit. One of its functions is the storage of converted waveform data during the acquisition cycle. When not being used to store acquired waveform data, it may be used by the Microprocessor for additional system random-access memory. A functional block diagram of the Acquisition Memory circuitry is located in the "Diagrams" section of Volume II of this manual.

When acquiring a signal, the memory functions as a write-only, circular memory. Configured in a 256-by-16 bit array, it requires an 80-ns write cycle. The output of A/D Converter U456 (diagram 13) is parallel eight-bit data bytes, at a maximum rate of 40 ns per byte. To fulfill the maximum limit requirement of the memory write cycle, a double-buffer storage system converts the data to 16-bit byte pairs at a maximum rate of 80 ns.

During a waveform acquisition cycle, data storage in the memory is directed by a modulo-256 address counter. The counter allows only the last 512 converted waveform samples to be stored at any one time (record length is 512 bytes).

During nonacquisition periods, the Microprocessor can either write into or read from the Acquisition Memory. The waveform acquisition signal path is not enabled during Microprocessor read or write periods.

Acquisition Control

Waveform acquisition is controlled by the Time Base circuit (diagram 19) using the RSTACQ, STORON, and ENVL control lines and the SAVE and CONVERT clock signals. The Acquisition Control circuitry produces buffer control clocks and enabling signals. The buffer control clocks direct the storage of data into the odd and even halves of the memory, while the enabling signals start and end an acquisition cycle.

When STORON is HI at U332A pin 4, a LO RSTACQ (restart acquisition) pulse clears the Acquire flip-flop. A LO is placed on pin 5 ($\overline{\text{ACQUIRE}}$) and a HI on pin 6 (ACQUIRE). The ACQUIRE signal is applied to the Sample Rate Timing Generator in the Time Base (diagram 19) to enable the SAVE and CONVERT clocks. It is also applied to Time Base Status Register U240 to be read by the Microprocessor.

In a NORM Storage Mode acquisition (ENVL = 0), the CONVERT clock drives First Buffer U248 through pin 11, but it has no effect on the Envelope Control circuitry at U326 pin 11 or U340B pin 5. The SAVE clock is applied to U440A pin 3, where it is divided-by-two to produce $\overline{\text{SAVE0}}$ at the Q output (pin 5) and SAVE0 at the $\overline{\text{Q}}$ output (pin 6). SAVE0 is used to develop the Write Enable signals to the Acquisition Memory and clock the buffers to transfer data into the Acquisition Memory. The SAVE0 signal is also applied to Chop Drive flip-flop U150B in the Time Base to supply the drive to the Input Channel Switch.

Therefore, each time a chopped sample of the waveform is acquired, it will be stored in the same half of the memory as other samples of that waveform.

At the end of an acquisition, the Record Counter in the Time Base generates and transfers the DONE signal to U340D pin 12. Going HI, the DONE signal clocks U332B to record the level of SAVE0 (HI or LO). The A0M signal produced at U332B pin 9 is applied to Time Base Status Register U240. Here it is read by the Microprocessor to determine whether a trigger occurred in an odd or even memory address. The A0M signal is used by the Microprocessor to determine the most significant bit of the jitter-correction signal that is applied to the horizontal ramp in the Display X- and Y-Axis circuitry (diagram 16).

On the next rising edge of SAVE0 (from U440A pin 6), Acquire flip-flop U332A will clock a HI to pin 5 and a LO to pin 6, causing the acquisition cycle to stop. When the Microprocessor reads the Time Base Status Register and finds ACQUIRE HI, the stored waveform data can be read from the Acquisition Memory.

BUFFER CLOCK SELECTION. Clocks to buffers U448 and U548 are selected by dual four-line-to-one-line data selector U540. In a normal acquisition cycle, ENVL is LO at AND gate U340B pin 5, and both sections of the dual data selector will be enabled (U540 pins 1 and 15). This LO is also applied to the BSEL input of U540 (pin 2). The logic level present at the ASEL input (pin 14) is obtained from a circuit composed of U326A and U326B.

Flip-flops U326A and U326B are arranged into a circuit that initializes and controls buffers U448 and U548 during the ENVELOPE Storage Mode. When ENVELOPE is not selected, U326A pin 4 is held LO to preset the flip-flop output HI at pin 5. On the rising edge of the CONVERT clock (U326B pin 11), the HI from U326A pin 5 is clocked through to place a HI on U326B pin 9 and a LO on U326B pin 8. The LO from pin 8 is then applied to U326A pin 1. At this point, both pin 4 and pin 1 of U326A are LO, and the output at pin 5 is held HI. Each CONVERT clock to U326B pin 11 will continue to hold a HI on U326B pin 9. Therefore, during a NORM Storage Mode acquisition, U540 pin 14 (ASEL) will be held HI. See Figure 3-17 for a simplified switching illustration of U540. When BSEL is LO and ASEL is HI, the inputs at $1C_1$ and $2C_1$ are transferred to the outputs of U540 ($1C_1$ to 1Y and $2C_1$ to 2Y). In a NORM Storage Mode acquisition, U448 is clocked by the rising edge of $\overline{\text{AWE0}}$ (derived from SAVE0), and U548 is clocked by the rising edge of $\overline{\text{SAVE0}}$ (Figure 3-18).

Data Acquisition (NORM Storage Mode)

Eight-bit waveform data from the A/D Converter is clocked into First Buffer U248 on the rising edge of a CONVERT clock. From U248 the data is alternately

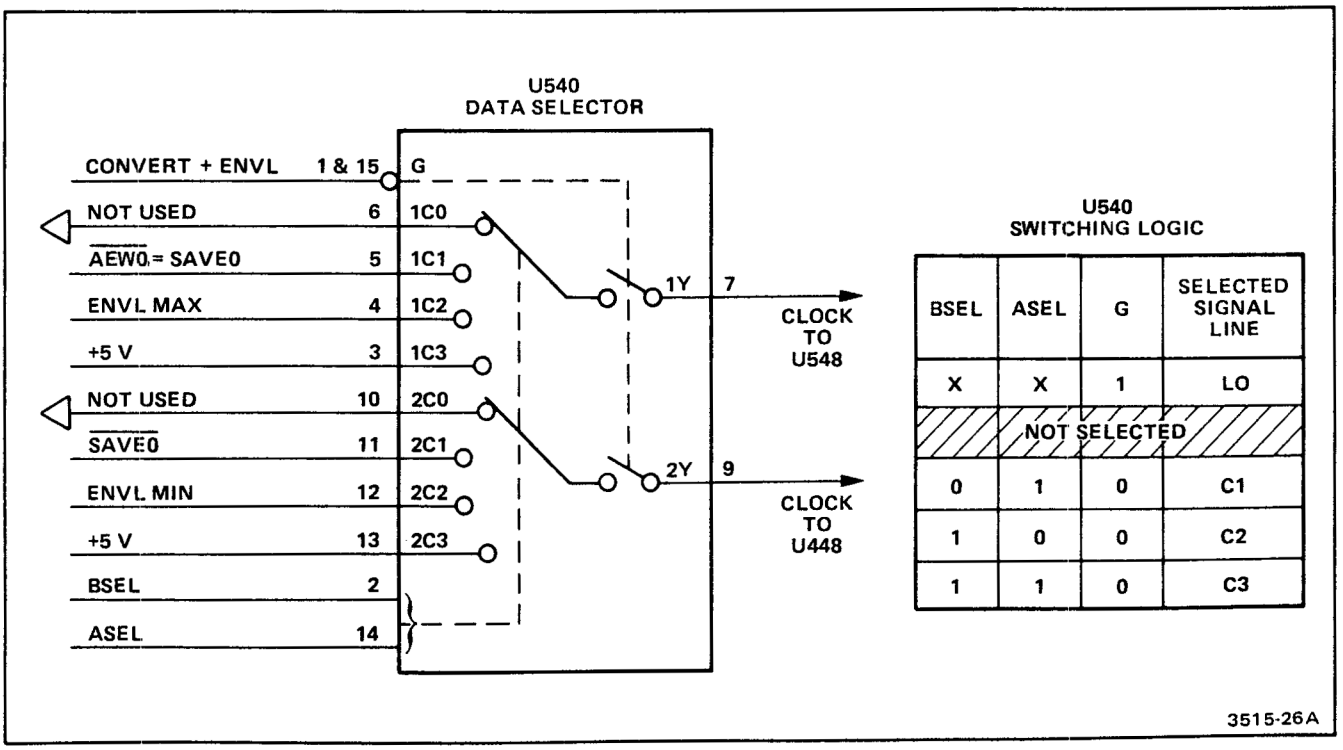

Figure 3-17. Simplified illustration of Data Selector U540 switching operation.

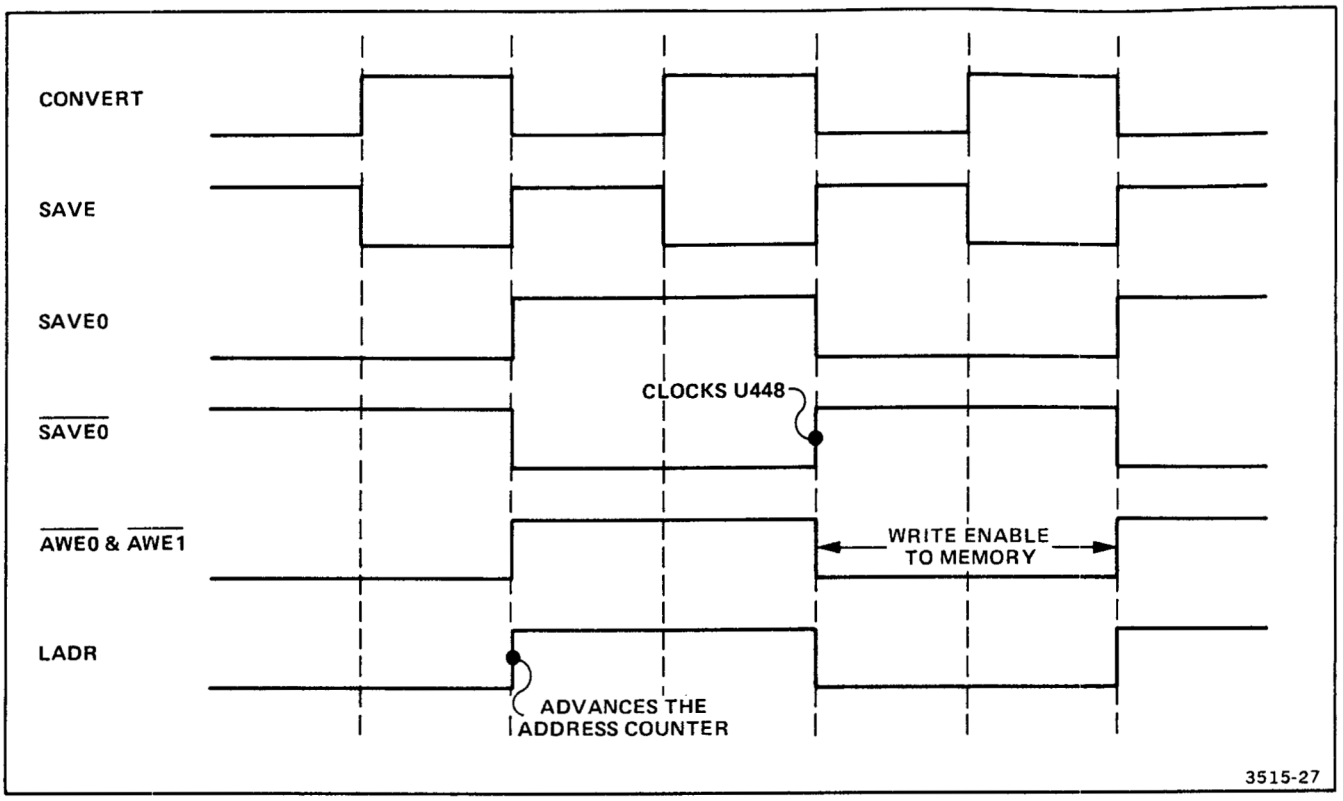

Figure 3-18. NORM Storage Mode Acquisition timing diagram.

transferred to Even Buffer U548 and Odd Buffer U448 by $\overline{\text{AWE0}}$ and $\overline{\text{SAVE0}}$. Data from U548 and U448 is transferred into Acquisition Data Buffers U520 and U320 by the rising edge of the Acquisition Memory write-enabling signals $\overline{\text{AWE0}}$ and $\overline{\text{AWE1}}$ (both are SAVE0 during acquistion). However, due to a propagation delay of the $\overline{\text{AWE0}}$ clock through U540, the data from buffer U548 is clocked into buffer U520 before the new data byte is clocked into U548. As the data byte is being clocked into U520 from U548, the data byte in U448 is concurrently clocked into Memory Input Buffer U320 by the rising edge of $\overline{\text{AWE1}}$.

When $\overline{\text{AWE0}}$ and $\overline{\text{AWE1}}$ go LO to enable the memory write inputs, the two eight-bit data bytes present in Acquisition Data Input Buffers U520 and U320 are written into the memory as a full 16-bit data byte.

Address Counters U210 and U206 are incremented by the LADR signal from U216 (Figure 3-19). In normal acquisition, the counters are incremented on the rising edge of SAVE0. Each time the memory is written into, the address is retained in Memory Address Register U112. At the end of an acquisition cycle, the Microprocessor reads register U112 (using the $\overline{\text{RDMAR}}$ strobe) to determine the address of the last data byte stored. The next address in the Acquisition Memory is the location of the first data point of the acquired waveform.

Envelope Acquisition

In the ENVELOPE Storage Mode, data bytes are written into the memory in a manner similar to that for NORM Storage Mode acquisition. The difference is that the CONVERT clock is much faster than the SAVE clock for ENVELOPE acquisition, and only selected data bytes are stored at each data point. The method used to select the data byte for storage at each memory location involves the use of Amplitude Comparators U432, U436, U532, and U526 for determining the maximum and minimum values of the waveform occurring at each data point.

At the beginning of each sample interval, buffers U448 and U548 are initialized by a pulse developed by AND gate U340B and flip-flops U326A and U326B. When ENVL (Figure 3-20) is HI (ENVELOPE Storage Mode selected), U326A pin 4 is HI and does not affect the state of U326A. When SAVE0 occurs, its rising edge clocks the fixed HI on U326A pin 2 onto pin 5 (the U326A Q output). The next rising edge of the CONVERT clock at U326B pin 11 clocks the HI at pin 12 onto the Q output (pin 9) to the U540 ASEL input pin 14. The $\overline{\text{Q}}$ output of U326B (pin 8) goes LO, placing a LO on U326A pin 1 and resetting the U326A Q output (pin 5) LO.

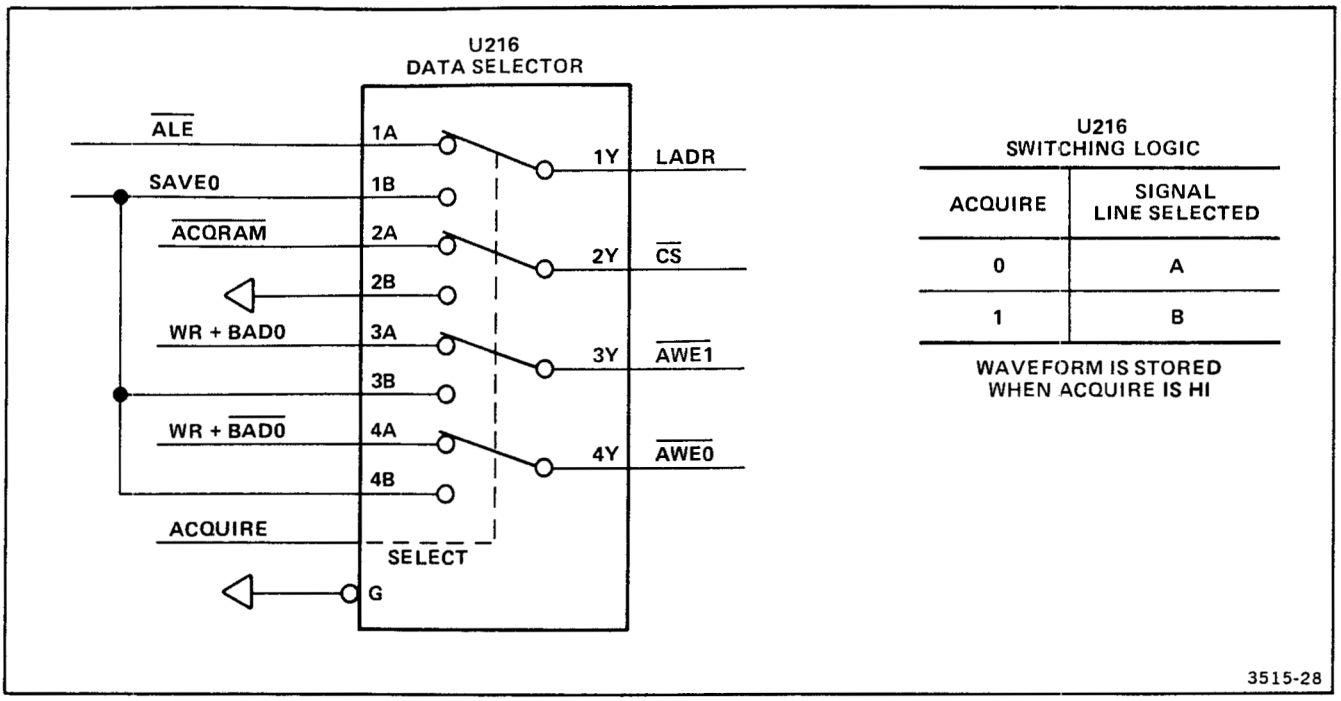

Figure 3-19. Simplified illustration of Data Selector U216 switching operation.

With both ASEL and BSEL of U540 HI, the $1C_3$ and $2C_3$ inputs of U540 are switched to the output pins; but while CONVERT and ENVL are HI, both halves of U540 are disabled, and its outputs are LO (Figure 3-20). On the falling edge of the CONVERT clock, the output of AND gate U340B goes LO to enable U540 for the duration of the CONVERT clock pulse. The HI pulses from the outputs of U540 are applied to both U448 and U548 to clock in the first data point value, thus initializing the ENVELOPE acquisition cycle.

The next CONVERT clock rising edge clocks the LO previously placed on U326A pin 5 onto the U326B Q output (pin 9) and U540 ASEL input goes LO. The $\overline{Q}$ output of U326B goes HI, and U326A is no longer affected.

Now U540 BSEL is HI and ASEL is LO. During the CONVERT clock LOs, the C_2 inputs are selected for transfer to the output. The envelope MAX signal is applied to the $1C_2$ input, and the envelope MIN signal is applied to $2C_2$ (from the Amplitude Comparators). When new maximum or minimum data point values occur, they are transferred either into U448 by the envelope MIN signal or into U548 by the envelope MAX signal. During the CONVERT clock HIs, both of the U540 outputs will be LO.

Envelope Comparators

A circuit composed of four, four-bit comparators performs the task of finding the minimum and maximum signal magnitudes for each data point during an envelope acquisition cycle. Waveform data transferred into buffers U548 and U448 during each $\overline{SAVE0}$ initializing pulse is compared with new data clocked into First Buffer U248 on each CONVERT clock rising edge. The four-bit magnitude comparators are cascaded to compare the full eight bits of each data byte.

For minimum data comparison, the four least significant bits of the waveform data in buffer U448 are applied to comparator U432 at the A inputs; the four most significant bits are applied to the A inputs of U426. New data being transferred into U248 with each CONVERT clock is applied to the B inputs of U432 and U426 in the same order as the data on the A inputs. If a comparator pair receives an amplitude value less than the previous value, U426 A>B output at pin 5 goes HI. This HI is applied to U448 (via U540) to clock the new data minimum value into U448. The comparison continues in this manner until a rising edge of SAVE0 occurs, and the data present in U448 at that time is transferred into the Acquisition Data Input Buffer U320 (Figure 3-20).

In the same way, waveform data maximum value comparison is performed by U532 and U526 producing a MAX clock when a larger maximum value is found. A MAX signal applied to buffer U548 (via U540) clocks in the new

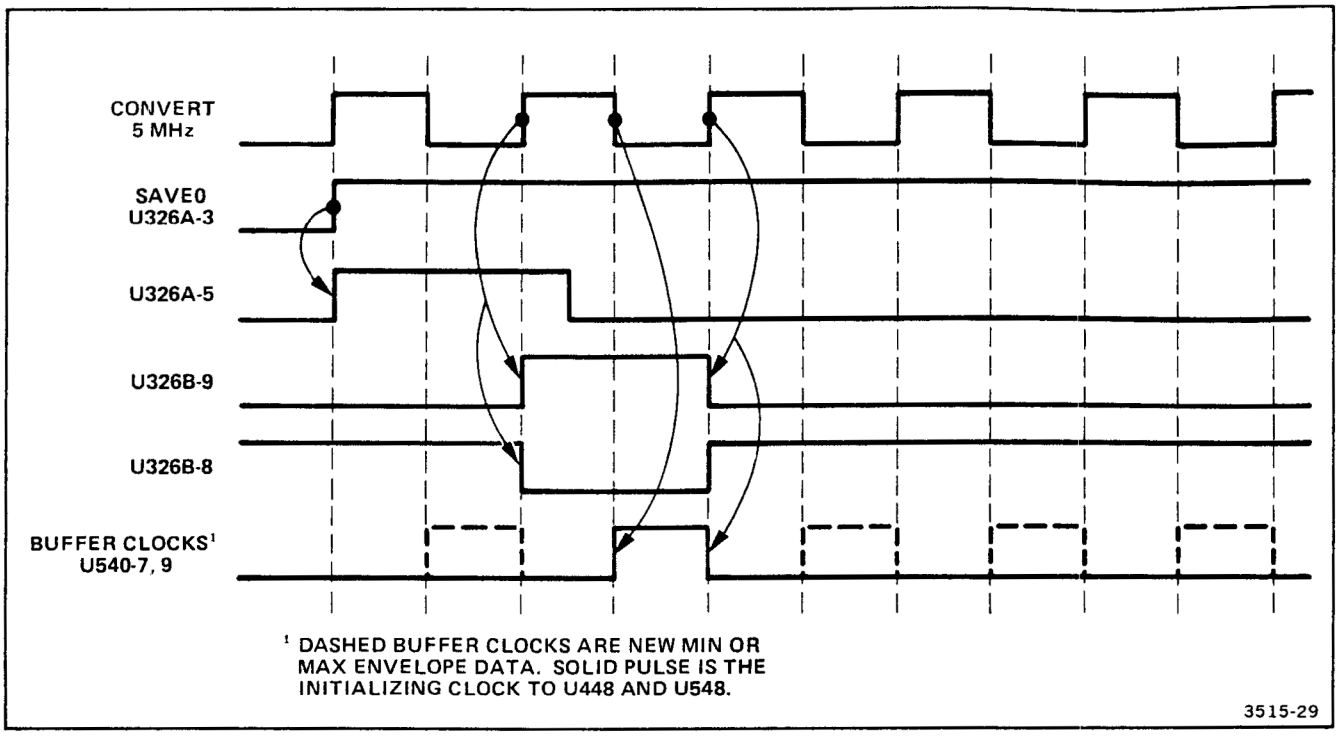

Figure 3-20. ENVELOPE Storage Mode Acquisition timing diagram.

maximum data. When the SAVE0 rising edge occurs, data present in U538 and U448 is simultaneously transferred into both Acquisition Data Input Buffers U320 and U520 (Figure 3-20).

Memory Control

Data selector U216, in the Memory Control circuit, selects the control signal presented to the Acquisition Memory and Address Counters. During a waveform acquisition, ACQUIRE on U216 pin 1 is HI, and the memory write enables ($\overline{AWE0}$ and $\overline{AWE1}$) and the address counter incrementing signal (LADR) are all derived from the SAVE0 clock (see Figure 3-19). The memory chip selects are held enabled by the LO on U216 pin 6 (the B_2 input).

Acquired waveform data is read from the Acquisition Memory while ACQUIRE is LO. The Microprocessor reads from any location in the memory by addressing that location through the buffered address lines (BAD0 through BAD7) from Memory Address or Data Buffer U240. The address is loaded into Address Counters U206 and U210 by LADR from U216. The RD (read) and $\overline{ACQRAM}$ (acquisition memory select) signals are then produced from the Microprocessor. The RD signal is applied to NAND gate U220B pin 5 and $\overline{ACQRAM}$ (inverted by U220A) is applied to U220B pin 4 to produce an enabling LO to Memory Output Buffer U108.

The BAD0 bit is latched into flip-flop U120B to select which half (odd or even) of the memory is to be read. When BAD0 is LO, the even half of memory (U512 and U508) is enabled for reading. When BAD0 is HI, the $\overline{Q}$ output of U120B (pin 8) will be LO, enabling U312 and U306 (the odd half of memory) to be read.

The Microprocessor writes into the Acquisition Memory by performing a memory-write cycle to the address in the Acquisition Memory. Addressing is done in the same manner as a memory read, but the WR signal is used (along with the BAD0 bit) to enable the data into the selected memory half. During a write cycle, RD is LO so the Memory Output Buffer is not enabled.

Data to be written into the Acquisition Memory passes from the BAD0 through BAD7 lines via Microprocessor Data Input Buffers U226 and U232. It is written into the selected memory address by either the $\overline{AWE0}$ or $\overline{AWE1}$ memory write enabling signal.

Digital Holdoff

When an input trigger occurs, the Acquisition Memory acquires the remaining data point samples necessary to fill a 512-byte record length. The memory is continually

acquiring waveform samples before a trigger occurs. To ensure that enough samples are obtained prior to a trigger for the PRETRIGGER data to be acquired, a holdoff signal is produced which prevents a trigger from being generated until Address Counters U210 and U206 overflow.

At the beginning of an acquisition cycle, the Address Counters are loaded with either a PRETRIGGER or a POST-TRIGGER Display Window count. For a single-trace, PRETRIGGER acquisition, the counters will be loaded with 448_{10}; for POST-TRIGGER, the counters will be loaded with 64_{10}. When the Address Counters reach a count of 512, the ripple carry output of U206 pin 15 goes HI and Digital Holdoff flip-flop U120A is clocked to place a LO on U120A pin 5. The LO is ANDed with the STORON HI, and the holdoff signal (BHOF) to the Oscilloscope Sweep and Z-Axis Logic circuitry (diagram 7) goes LO, releasing the holdoff.

The first incoming trigger is now accepted to generate the A and B gate triggers to the digital storage Time Base (diagram 19). When a trigger occurs, pin 4 of U120A (TRIG) goes LO and sets U120A pin 5 to a HI. This asserts the BHOF signal and prevents triggering until the next acquisition cycle.

When the trigger is accepted, the Record Counter in the Time Base begins counting the SAVE clocks. When enough SAVE clocks have been counted to complete the POST TRIGGER portion of the waveform, the DONE signal is generated and is applied to Acquire flip-flop U332A in the Acquisition Control circuitry to end the acquisition cycle.

In the NON STORE mode, the BHOF signal is prevented from being applied to the digital holdoff circuitry in the Sweep and Z-Axis Logic circuit while STORON is LO at U340A pin 1 to disable the AND gate.

MICROPROCESSOR

The Microprocessor (diagram 18) contains the necessary circuitry to control the operation of the oscilloscope. A functional block diagram of the Microprocessor circuitry is located in the "Diagrams" section of Volume II of this manual. In addition to the 8-bit Microprocessor IC, this circuit contains: 16 k bytes of read-only memory, 2 k bytes of random-access memory (1 k for system RAM and 1 k for scratch RAM), address decoding circuitry to select appropriate components for performing an operation, and necessary timing and gating circuits that enable the Microprocessor to control the circuit functions.

Power-On Sequence

A power-on restart circuit comprised of CR172, C174, R172, and R173 provides the proper timing for resetting the digital circuitry (initialize) each time power is applied to the instrument. When power is applied, the charge on C174 is zero, and the $\overline{\text{RESET IN}}$ signal on pin 36 of Microprocessor (U364) is initially held LO. While $\overline{\text{RESET IN}}$ is LO, U364 pin 3 (RESET OUT) is held HI, causing the initializing signal ($\overline{\text{INIT}}$) from inverter U272G to be LO.

The $\overline{\text{INIT}}$ signal remains LO until the voltage on capacitor C174 (charging through R173) reaches the HI input threshold of an internal Schmitt trigger circuit at the $\overline{\text{RESET IN}}$ input of U364. At that time, RESET OUT goes LO and $\overline{\text{INIT}}$ goes HI, ending the reset period. The time constant of C174 and R173 is such that the reset period is greater than 10 ms.

When power is removed from the instrument, the charge on C174 forward biases diode CR172, and C174 discharges quickly to allow rapid on-off power cycling. This is necessary to ensure initialization each time the power is applied to the instrument.

Jumper plug P182 provides a means for service personnel to manually reset the digital circuitry without cycling the power off-and-on. When the jumper is used to connect R172 to ground, $\overline{\text{RESET IN}}$ is forced LO to reset the digital circuitry. Removing the jumper then starts the charging cycle of C174 to end the reset period. A measure of protection from static discharge damage to Microprocessor U364 is provided by R172.

Processor Operation

The Microprocessor is clocked from an external 5-MHz clock signal ($\overline{\text{MPUCLK}}$). This signal is buffered by U272D, and a pull-up resistor R263 is used to bring the HI clock level up to the required voltage at the X_1 clock input (pin 1). The processor clock is divided-by-two internally and can be tested at U364 pin 37 (CLK OUT).

ADDRESS AND DATA DEMULTIPLEXING. Signals generated by the Microprocessor are used to address peripheral devices which perform the different operations required to control the 468. These signals also determine whether the information on the bus is either an address or data. Through selection of proper address and control signals, information is transferred either into or out of the Microprocessor. Low-order addresses (A0 through A7) are multiplexed with data on the bus lines. To obtain address information, it is therefore necessary to demultiplex the AD0 through AD7 bus lines.

Timing of the demultiplexing and data transfer is based on clock periods (Figure 3-21). On the MPU Board, demultiplexing is performed by Address Latch U550. When an address appears on the AD0 through AD7 lines during clock period T_1, the address latch enable signal (ALE) at U364 pin 30 goes HI, enabling the Address Latch U550. Also, the ALE signal is inverted by U272C and resets flip-flop U255A. The Q output of U255A goes LO to enable Address or Data Buffer U452. Approximately 200 ns later ALE returns LO, and the address on AD0-AD7 is latched into U550. Address information latched into U550 is available only on the Microprocessor circuit board. Other address latch-circuits throughout the instrument must latch addresses from the bus (via U452) on the rising edge of $\overline{ALE}$ from P130 pin 30.

ADDRESS DECODING AND STROBE GENERATION. Selection of a particular device address is performed in the Address Decode and Strobe Generator circuitry (Figure 3-22). The high-order addresses from the Microprocessor are decoded to determine the desired peripheral(s) to be activated, and an enabling strobe is generated to turn on the selected device. High-order addresses (A8 through A15) appearing on Microprocessor pins 21 through 28 are not multiplexed, and they are presented to the decoder input during clock periods T_1 through T_3 (Figure 3-21).

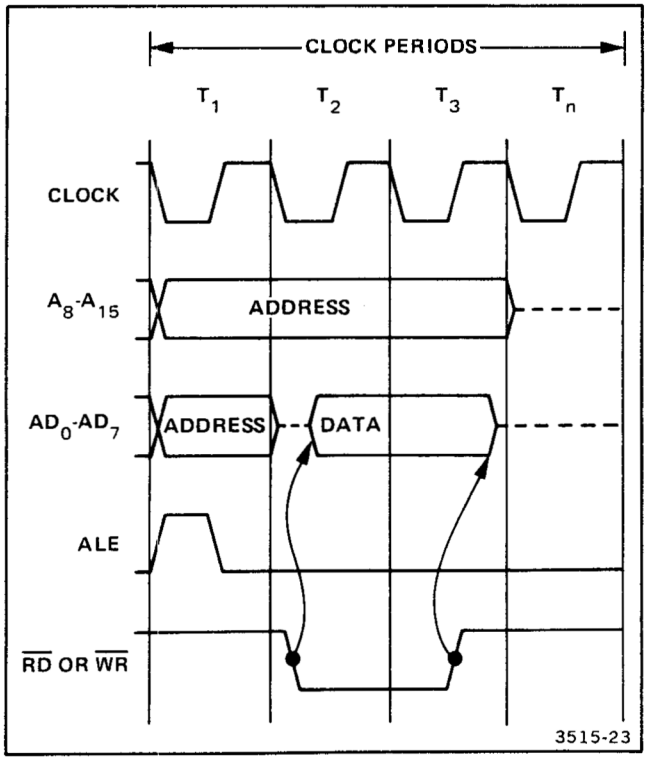

Figure 3-21. Address decoding timing diagram.

Decoder timing is controlled by the read or write signal $\overline{RD + WR}$ from U278B pin 4. The three highest address lines (A13 through A15) are applied to 1-in-8 decoder U478 where they are decoded to access eight address blocks, each containing 8k addresses. Six of the decoded blocks are assigned to certain areas of circuit operation, and two address blocks are unassigned. See Table 3-4 for a listing of address block assignments.

Table 3-4

Address Block Assignments

BLOCK ASSIGNMENT, SIZE, AND BOUNDARIES	
$\overline{ROML}$ (8 k) 000-13FF / SERVICE ROM (5 k) 000-13FF	ACQ RAM COPY (0.5 k) C200-C3FF
$\overline{ROMH}$ (8 k) 2000-3FFF	ACQ RAM COPY (0.5 k) C400-C5FF
ROM DEVELOPMENT (16 k) 4000-7FFF	ACQ RAM COPY (0.5 k) C600-C7FF
SYSTEM RAM (1 k) 8000-83FF	ACQ RAM COPY (0.5 k) C800-C9FF
SYSTEM RAM COPY (1 k) 8400-87FF	ACQ RAM COPY (0.5 k) CA00-CBFF
SCRATCH RAM (1 k) 8800-8BFF	ACQ RAM COPY (0.5 k) CC00-CDFF
SCRATCH RAM COPY (1 k) 8C00-8FFF	ACQ RAM COPY (0.5 k) CE00-CFFF
UNASSIGNED (4 k) 9000-9FFF	ACQ RAM COPY (0.5 k) D000-D1FF
DISPLAY RAM (2 k) A000-A7FF	ACQ RAM COPY (0.5 k) D200-D3FF
DISPLAY RAM COPY (2 k) A800-AFFF	ACQ RAM COPY (0.5 k) D400-D5FF
DOT RAM (1 k) B000-B3FF	ACQ RAM COPY (0.5 k) D600-D7FF
DOT RAM COPY (1 k) B400-B7FF	ACQ RAM COPY (0.5 k) D800-D9FF
DOT RAM COPY (1 k) B800-BBFF	ACQ RAM COPY (0.5 k) DA00-DBFF
DOT RAM COPY (1 k) BC00-BFFF	ACQ RAM COPY (0.5 k) DC00-DDFF
ACQ RAM (0.5 k) C000-C1FF	ACQ RAM COPY (0.5 k) DE00-DFFF
	I/O (8 k) E000-FFFF

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Blocks Y_0 and Y_1 are assigned to ROM U565 and U575 respectively. Therefore, these decoded address blocks are used directly as select strobes, $\overline{\text{ROML}}$ and $\overline{\text{ROMH}}$ (U478 pins 14 and 15 respectively), to choose either the high-order or low-order ROM. A section of the ROML addresses is assigned to the service ROM that is used when running service routines.

Blocks Y_2 and Y_3 are not assigned.

Address block Y_4 (U478 pin 11) is assigned to the Microprocessor RAM and produces the $\overline{\text{RAM}}$ strobe. This block of addresses is further decoded by U378 into two address blocks containing 2k addresses each. The $2Y_1$ block (U378 pin 12) is assigned to select the system RAM with the $\overline{\text{SYSRAM}}$ strobe, and the $2Y_0$ block (U378 pin 11) is assigned to select the scratch RAM, using the $\overline{\text{SCRRAM}}$ strobe. The RAM-select strobes go directly to the chip select inputs of the RAM ($\overline{\text{SYSRAM}}$ to U540 and U545 pin 8 and $\overline{\text{SCRRAM}}$ to U525 and U530 pin 8).

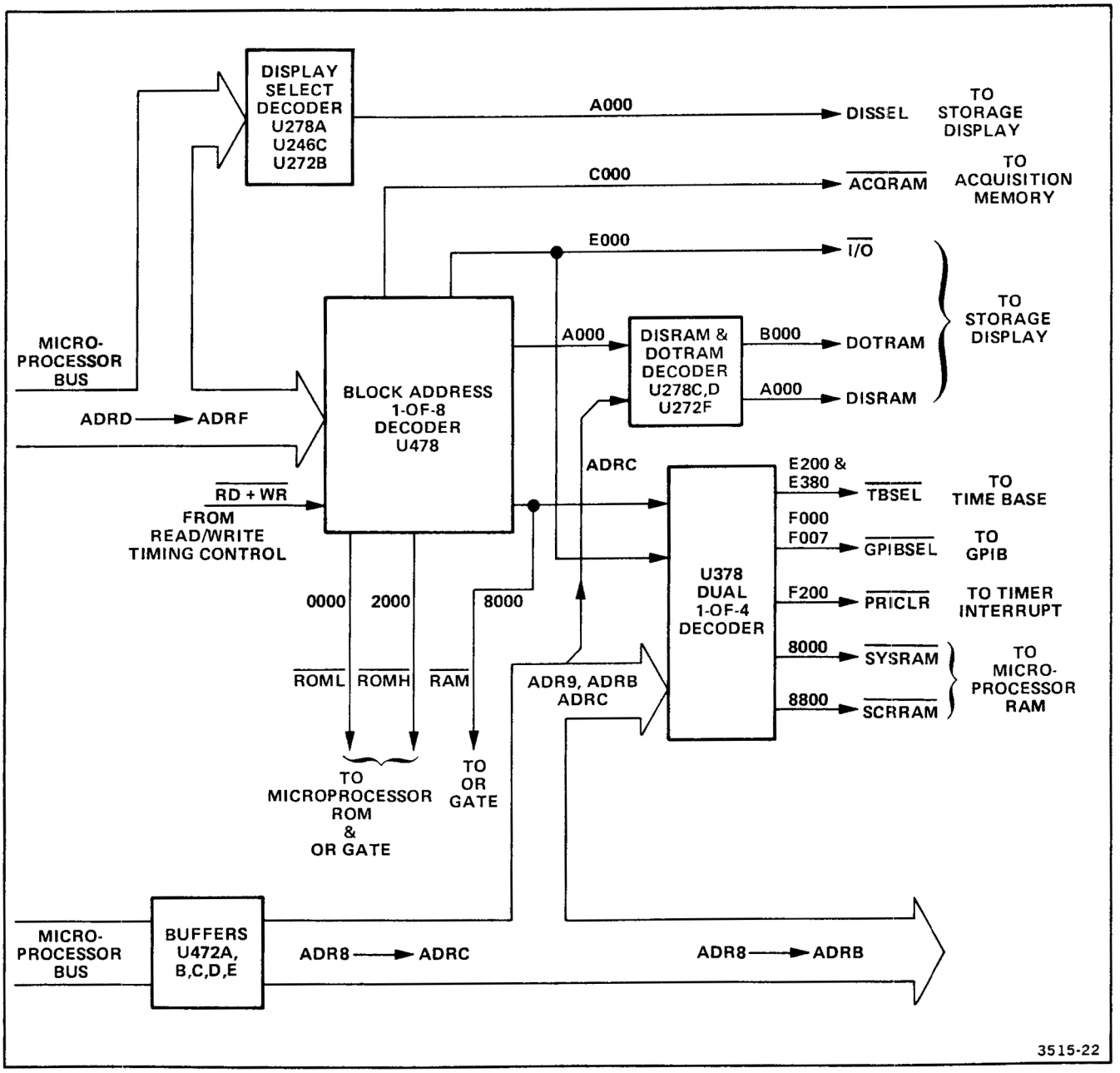

Figure 3-22. Detailed block diagram of the Address Decoding and Strobe Generation circuits.

Address block Y_5 is assigned to select either the Display RAM or the Dot RAM (both located on the Storage Display Board). The decoded block Y_5 addresses from U478 pin 10 are applied to a 1-of-2 decoder circuit composed of U278C, U278D, and U272F. Address line ADRC is also applied to this decoder circuit to control which strobe is produced at the output (DISRAM or DOTRAM). When ADRC is LO at U278 pin 9, block Y_5 will be gated through U278C to become the DISRAM strobe. When ADRC is HI, block Y_5 will be gated through U278D to become the DOTRAM strobe. The DOTRAM strobe selects a 1024 by 1-bit RAM which is used to produce the TIME cursor dots. A DISRAM strobe selects the 1024 by 8-bit Display Memory RAM. Timing of the block Y_5 DISRAM and DOTRAM strobes is controlled by processor $\overline{RD}$ or $\overline{WR}$ signals which occur during clock periods T_2 and T_3 (see Figure 3-21). A select signal is required in clock period T_1 for use on the Storage Display Board, therefore additional block Y_5 decoding is performed by a circuit consisting of U278A, U272B, and U246C. The A13 through A15 Microprocessor lines are applied to this decoding circuitry to produce a DISSEL strobe beginning in clock period T_1. The DISSEL strobe is produced when A13 and A15 are HI and A14 is LO.

Address block Y_6 (U478 pin 9) produces a strobe ($\overline{ACQRAM}$) that selects the acquisition RAM on the Memory Board (diagram 14). Additional discussion of the selection method is included in the "Acquisition Memory" circuit discussion.

An $\overline{ACQRAM}$ strobe is decoded from only the upper three addresses (A13 through A15). The next four lower addresses of the acquisition RAM are unselected ("don't care" to the Microprocessor). The remaining nine acquisition RAM addresses are produced by the Microprocessor and placed on the bus to select each storage address in a 512 byte segment of the acquisition RAM.

I/O REGISTER SELECTION. Address block Y_7 produces strobe I/O at U478 pin 7. This strobe is used when selecting the various registers that must be read from or written into by the Microprocessor. Additional decoding is performed on the Storage Display Board (diagram 17) to select both the register banks (Display 1, Display 2, or Front Panel) and the exact register in a bank. Three other register banks are selected by decoding circuits on the Microprocessor board. See Table 3-5 for the address bit assignments of the block Y_7 addresses.

When the Microprocessor restarts the acquisition of the input waveform, some of the restart signal address bits are used to determine the amount of pretrigger holdoff. This selection is performed by U378 decoding address bits ADRC (on pin 3) and ADR9 (on pin 2) in conjunction with the I/O strobe. When the combination of these two bits equals 01, in either of two address (E200 or E380), the $\overline{TBSEL}$ strobe is produced. This action provides a restart signal ($\overline{RSTACQ}$) for both the pretrigger and post-trigger operation of the Time Base.

Two remaining strobes are selected by different combinations of the ADRC and ADR9 bits. Access to the GPIB register bank is obtained when the combination equals 10. This produces the strobe, $\overline{GPIBSEL}$. When the combination of these bits equals 11, the CURSOR position rate potentiometer digitizing circuit strobe ($\overline{PRICLR}$) is produced at address F200.

When the block Y_7 addresses are not being decoded, $\overline{I/O}$ is HI. This HI is applied to U378 pin 1, and the U378 outputs at pins 5, 6, and 7 are all forced HI. This prevents a decoding of the ADRC and ADR9 address bits, except when the $\overline{I/O}$ strobe is activated.

DATA TRANSFER. At the beginning of clock period T_2 (Figure 3-21), the information on the AD0 through AD7 multiplexed lines becomes undefined, causing either the $\overline{RD}$ or the $\overline{WR}$ signal from U364 to become LO. At this time, the $\overline{RD + WR}$ signal, generated by U278B at pin 4, also goes LO at U478 pin 5 to activate the selected address that was set up in U478 during clock period T_1.

If a memory-read operation is required (RAM read, instruction fetch, or status register read), the selected device will place data on the bus. Address or Data Buffer U452 is gated by the RD signal going LO at its GAB input pin 1 (via buffer U472H) to transfer the data from the bus to the Microprocessor (B-to-A). Approximately 600 ns later, during the middle of clock period T_3, RD goes HI, and U364 latches the data from its AD0 through AD7 lines. The positive transition of RD clocks Address or Data Buffer control flip-flop U255A pin 3, forcing its Q output HI at pin 5. This HI, applied to U452 pin 19, disables the Address or Data Buffer to isolate the AD0 through AD7 lines from the U364. This prevents both the Microprocessor and any devices still driving the bus from conflicting with each other.

Further clock periods (T states) are needed by the Microprocessor to handle certain instructions obtained by a fetch cycle. During these added T states, the information present on lines A8 through A15 also becomes invalid, and the decoder U478 will have all of its outputs forced HI by the $\overline{RD + WR}$ signal going HI at U478 pin 5. Thus, invalid addresses are not decoded.

For memory-write cycles (RAM write and control register write) $\overline{RD}$ remains HI after the address is selected in clock period T_1. The GAB input of U452 pin 1 is HI, and during clock period T_2, data is gated from U364 onto the AD0 through AD7 bus lines via U452. When the $\overline{WR}$ signal goes HI in clock period T_3, it signals the selected device that data is valid. This data will remain valid for approximately 90 ns, during which time it must be either latched or written into the selected device.

The ROM and RAM are connected to the AD0 through AD7 bus lines via bidirectional Memory Buffer U558. The $\overline{RAM}$, $\overline{ROML}$, and $\overline{ROMH}$ strobes are combined in OR gate U264B to enable U558 whenever RAM or ROM is selected. Control of the direction of data transfer through U558 is accomplished by the RD signal at pin 1. During a read cycle, RD is HI and data is gated from A-to-B. In a write cycle, RD is LO and data is gated from B-to-A.

MICROPROCESSOR INTERRUPT OPERATION. There are five hardware interrupt inputs to U364. The Microprocessor will first respond to the highest priortiy interrupt before handling other, lower-priority interrupts. Interrupt functions and their priorities are shown in Table 3-6. The interrupts are divided into three types:

1. The INTR interrupt can be enabled or disabled by program instructions (maskable). It causes the Microprocessor to fetch a special instruction placed on the bus. Execution of this instruction calls a subroutine used to handle the interrupt from the ROM.

2. Interrupts RST 7.5, RST 6.5, and RST 5.5 are also maskable depending on the current conditions of U364 as well as the program instructions. The vector addresses for these interrupts are obtained internally from the Microprocessor (Table 3-6).

3. The TRAP interrupt is not maskable and is initiated manually by removing NORM plug P262. With this plug removed, the TRAP input is pulled HI to interrupt the Microprocessor.

Interrupts are used to divert the Microprocessor from the operation in progress so that some other circuit functions can be performed. Each interrupt will cause a different operating sequence to begin.

The TRAP interrupt is used to start a bus-test servicing routine. When P262 is disconnected, the Microprocessor vectors to address 0024, which contains the instruction INX HL. This command increments the contents of the Microprocessor's internal H and L register pair. Continuing, the Microprocessor then reads the contents of address location 0025, which contains the instruction MOV A,M. This command moves the contents of memory, whose address is indicated by the contents of the H and L register pair, into the Microprocessor A register. The content of the address location is not used, so it is only temporarily stored in the A register until it is replaced during the next read cycle of the bus test routine.

Next, U364 reads the contents of address location 0026 which contains the instruction JMP. The address of the jump location is contained in the next two address locations, 0027 and 0028. The entire command is JMP 24, which returns the routine back to address location 0024 to start the increment-move-jump sequence over again.

The routine continues to loop back to address 0024, and as the H and L register pair are incremented each time, a different memory location is read. This looping routine is useful for signature analysis testing of Microprocessor address sequences and of address generated strobes.

Interrupt RST 5.5 is connected through buffer U472F to the GPIBINT line. When the GPIBINT signal is generated, it is held HI until the Microprocessor receives the interrupt. Then U364 vectors to 002C to begin the GPIB routine. When the rountine is finished, the Microprocessor clears the interrupt from the GPIB interface.

Interrupt RST 6.5 is the DISPLAY interrupt connected through inverter U272A. This interrupt vectors the Microprocessor to address 0034. The DISPLAY line going LO signals the Microprocessor that a display cycle was completed. When a display cycle is restarted at the completion of the interrupt service routine, the DISPLAY signal is set HI again.

Interrupt RST 7.5 is an edge-triggered interrupt used to provide a time reference required by the firmware to perform various operations. The reference is derived from a 50-kHz signal generated on the Storage Display Board. Divider U440 receives the 50-kHz signal on pin 1 and divides it by 100 to produce a rectangular pulse 500 μs wide with a period of 2 ms. The rising edge of the pulse sets the internal RST 7.5 flip-flop. This flip-flop remains set until it is cleared by the Microprocessor with an internal reset signal.

When the RST 7.5 interrupt is acknowledged, the Microprocessor vectors to address 003C.

Table 3-5
Address Block Y7 Control Bit Assignments

Control Signal Address	Control Signal Name	Controlling Strobe	Control Signal Function	Bit Assignments							
				AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
E040	$\overline{FPC}$	$\overline{I/O}$	WRITE	$\overline{TIDS}$ LED	TRACK / $\overline{HOLD}$	CH1POS	CH2POS	RESET	LATCH	ADVAN	SRQLED
E041	$\overline{CONTRL}$	$\overline{I/O}$	WRITE	ACTIVEL	$\overline{ZAXON}$	—	$\overline{LINECUR}$	$\overline{TRIGVIEW}$	$\overline{STORDIS}$	BOTH	ODD
E042	$\overline{FP2}$	$\overline{I/O}$	READ	—	—	—	$\overline{XMIT}$	—	$\overline{NO.AVG}$	$\overline{TIME}$	$\overline{VOLTS}$
E043	$\overline{FP1}$	$\overline{I/O}$	READ	PULSE / $\overline{SINE}$	POST-TRIG / $\overline{PRETRIG}$	$\overline{SAVEREF}$	$\overline{SAVE}$	$\overline{AVG}$	$\overline{ENV}$	$\overline{NORM}$	$\overline{OFF}$
E044	$\overline{LEDRO}$	$\overline{I/O}$	WRITE	← $\overline{SCALE\ LED}$ →			DEC.PT	← LSD DIGIT STROBE →			MSD
E045	$\overline{SVNSEG}$	$\overline{I/O}$	WRITE	—	—	—	—	← BCD SEGMENT →			
E200	$\overline{RSTACQ}$	$\overline{TBSEL}$	STROBE	← START ACQUISITION →							
E201	WRSR1	$\overline{TBSEL}$	WRITE	LT2	STORON	ENVL	PRETRG	AGTSEL	ADD	CH1	CH2
E202	WRSR2	$\overline{TBSEL}$	WRITE	← MSB SAMPLE RATE WORD TO DIVIDE CHAIN SEE TABLE 3-7 →							LSB
E203	MTRIG	$\overline{TBSEL}$	STROBE	← MANUAL TIME BASE TRIGGER →							
E204	$\overline{RDSTAT}$	$\overline{TBSEL}$	READ	—	—	—	—	—	—	AOM	$\overline{ACQUIRE}$
E205	$\overline{RDMAR}$	$\overline{TBSEL}$	READ	← A8 ADDRESS OF LAST ACQUIRED WAVEFORM DATA POINT →							A1
E206	$\overline{RDJC8}$	$\overline{TBSEL}$	READ	← MSB 8-BIT JITTER CORRECTION SIGNAL →							LSB
E207	$\overline{RDJC4}$	$\overline{TBSEL}$	READ	← MSB 4-BIT JITTER CORRECTION SIGNAL → LSB				—	—	—	—
E400	$\overline{DIPSW}$	$\overline{I/O}$	READ	← OPTION SERVICE AND OPTION SWITCH →							
E401	$\overline{LINER}$	$\overline{I/O}$	WRITE	← 8 MSB OF 10-BIT LINE CURSOR →							
E402	$\overline{DISREG}$	$\overline{I/O}$	WRITE	CSEL	STOP512	STOP256	STOP128	VERT10X	START	V2SB ← LINE CURSOR BITS →	VLSB
E403	$\overline{CURSOR}$	$\overline{I/O}$	READ	—	RATE / $\overline{POS}$	SELECT	PRDONE	← MSB POSITION RATE COUNT →			LSB
E404	$\overline{JITTER}$	$\overline{I/O}$	WRITE	← MSB JITTER CORRECTION →							LSB

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Table 3-5 (cont)

Control Signal Address	Control Signal Name	Controlling Strobe	Control Signal Function	Bit Assignments							
				AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
E405	$\overline{\text{VGAIN}}$	$\overline{\text{I/O}}$	WRITE	← VERTICAL GAIN WORD →							
E406	$\overline{\text{HGAIN}}$	$\overline{\text{I/O}}$	WRITE	← HORIZONTAL GAIN WORD →							
E407	$\overline{\text{STOPDIS}}$	$\overline{\text{I/O}}$	STROBE	← STOPS DISPLAY →							
E800	CH1	$\overline{\text{I/O}}$	READ	CH1 PROBE CODING	CH1 UNCAL	← CH1 INPUT COUPLING →		← CH1 VOLTS/DIV →			
E801	CH2	$\overline{\text{I/O}}$	READ	CH2 PROBE CODING	CH2 UNCAL	← CH2 INPUT COUPLING →		← CH2 VOLTS/DIV →			
E802	ATIME	$\overline{\text{I/O}}$	READ	—	—	—	← A TIME/DIV →				
E803	BTIME	$\overline{\text{I/O}}$	READ	A / $\overline{\text{B}}$	—	—	← B TIME/DIV →				
E804	MODE	$\overline{\text{I/O}}$	READ	$\overline{\text{CH1}}$	$\overline{\text{TRIG VIEW}}$	$\overline{\text{ADD}}$	$\overline{\text{CHOP}}$	$\overline{\text{CH2}}$	$\overline{\text{XY}}$	EXT TRIG	—
E805	LIGHTS	$\overline{\text{I/O}}$	WRITE	—	—	—	—	$\overline{\text{CH1X10}}$	$\overline{\text{CH1X1}}$	$\overline{\text{CH2X10}}$	$\overline{\text{CH2X1}}$
E806	VSM	$\overline{\text{I/O}}$	WRITE	SWEEP DISABLE	TRIGVIEW ENABLE	ALT / $\overline{\text{CHOP}}$	CH1	$\overline{\text{XY}}$	CH2	ADD	TRIG VIEW
F000	$\overline{\text{TALKREG}}$	GPIBSEL	READ	TALK ONLY	—	—	← TALK ADDRESS → 16	8	4	2	1
F001	$\overline{\text{SNTACK}}$	GPIBSEL	STROBE	← SENT ACKNOWLEDGED →							
F002	$\overline{\text{DATACC}}$	GPIBSEL	STROBE	← DATA ACCEPTED →							
F003	$\overline{\text{ATNFLS}}$	GPIBSEL	STROBE	← ATTENTION FLAG SET →							
F004	$\overline{\text{WIFDO}}$	GPIBSEL	WRITE	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
F005	$\overline{\text{RIFDI}}$	GPIBSEL	READ	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
F006	$\overline{\text{WIFCTL}}$	GPIBSEL	WRITE	TP335	TP333	LAT.IFC	—	TEOI	TSRQ	nba	TADS
F007	$\overline{\text{RIFSTAT}}$	GPIBSEL	READ	SENT	TADS	RRFD	NDAC	ATNDAV	ATTEN	RATN	$\overline{\text{IFCL}}$
F200	PRICLR	$\overline{\text{I/O}}$	STROBE	← CLEAR POSITION RATE INTERRUPT F-F →							

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Table 3-6

Microprocessor Interrupts

Function	Name	Trigger Required	Priority	Vector Address
Bus Looping Routine	TRAP	Rising edge AND remain HI until sampled.	1	0024
Firmware Timing	RST 7.5	Rising edge (latched).	2	003C
Display	RST 6.5	HI until sampled.	3	0034
GPIB	RST 5.5	HI until sampled.	4	002C
Position Rate Pot	INTR (RST 7)	HI until sampled.	5	0038

An additional divide-by-five is performed by U446 to reduce the 2-ms signal to a pulse (PRDONE) that is HI for 2 ms and LO for 8 ms. During the 8-ms LO time, a counter (on the Storage Display Board) is accumulating counts from a voltage-to-frequency converter that is used to digitize the output of the CURSOR position-rate potentiometer. When PRDONE goes HI, the rising edge clocks PRDONE latch U255B, and its Q output at pin 9 goes HI.

This HI interrupts the Microprocessor, and it responds by performing an instruction fetch to obtain a vector address from the bus. However, the $\overline{RD}$ signal at U364 pin 32, which is present during a normal instruction fetch, is not activated, and Address or Data Buffer U452 is not gated. Therefore, the Microprocessor is not connected to the bus lines. Instead, its AD0 through AD7 lines are all HI due to pull-up resistor pack R450. Thus the instruction obtained from the AD lines is FF (the RST 7 instruction), and the Microprocessor is vectored to address 0038.

Firmware response to this interrupt includes reading and resetting the CURSOR position-rate counter and generating the $\overline{PRICLR}$ strobe used to clear PRDONE latch U255B. The $\overline{PRICLR}$ strobe is generated in the address decoder circuitry when address F200 is accessed by the Microprocessor.

SERVICING OUTPUTS. For servicing, the Microprocessor serial out data (SOD) pin 4 is used with the service ROM to provide the Start/Stop pulse used with signature analysis testing.

Certain system error conditions will cause the Microprocessor to halt. A halt condition can be detected by checking the logic level at pins 29 and 33 (S_0 and S_1). If both pins are LO, the Microprocessor is halted.

Microprocessor clock signal $\overline{MPUCLK}$ is divided-by-two internally and is available for testing at the CLK OUT pin 37.

TIME BASE

A functional block diagram of the Time Base circuitry is located in the "Diagrams" section of Volume II of this manual. The Time Base circuitry (diagram 19), under control of the Microprocessor, controls the sample rate and acquisition mode of the oscilloscope's digital storage circuitry. Continual signal sampling occurs during the time interval between triggers. When a trigger signal occurs, the Record Counter circuit begins counting the samples as they are acquired. After the remaining samples required to obtain 512 samples for either pretrigger or post-trigger operation are obtained, the Record Counter generates the DONE signal. This signal indicates that the acquisition cycle has ended and that a display cycle may be entered.

The time difference between the fixed-rate sample clock and the oscilloscope trigger causes display jitter. This effect is reduced by measuring the time between the occurrence of a trigger signal and the next sample clock (measured by the Time Interval circuit) and then offsetting the display with a jitter-correction signal to compensate for the measured difference in timing.

Strobe Control

The Strobe Control circuit, composed of address latch U140 and 1-of-8 decoder U146, generates the timed strobes used by the Microprocessor to control the Time Base circuitry. Addresses from the Microprocessor AD0 through AD2 bus lines are latched into U140 on the rising edge address latch enable signal $\overline{ALE}$. When the Time Base is selected by the Microprocessor, the TBSEL strobe enables U146 to decode the address and to generate the appropriate strobe to the selected device in the Time Base (Table 3-5).

Two strobes generated by U146 are directed to the Memory Board: $\overline{\text{RSTACQ}}$ starts a new acquisition, and $\overline{\text{RDMAR}}$ strobes the Memory Address Register to allow the Microprocessor to obtain the address of the last waveform sample acquired at the end of an acquisition cycle.

Also generated by U146 are two write strobes: $\overline{\text{WRSR1}}$ strobes register U236 to load the acquisition mode data, and $\overline{\text{WRSR2}}$ strobes register U436 to load the sample-period data.

Two read strobes are directed to the Time Interval Meter. $\overline{\text{RDJC8}}$ strobes register U440 to allow the Microprocessor to read the 8-bit jitter-correction time-interval measurement between the sample clock and the trigger for sweep rates from 10 μs to 20 ns per division. $\overline{\text{RDJC4}}$ strobes register U240 to allow the Microprocessor to read the 4-bit jitter-correction data for sweep speeds from 5 s to 20 μs per division.

Another read strobe, $\overline{\text{RDSTAT}}$, enables a section of register U240 (containing the acquisition status) to be read by the Microprocessor.

The final strobe generated, $\overline{\text{MTRIG}}$, is used to supply a trigger to Trigger flip-flop U110A. Whenever a front-panel control is changed that affects the data being acquired, the Microprocessor supplies a manual reset to Trigger flip-flop U110A. This reset signal starts the Record Counter, and the sample timing is switched to fast sampling so the count is finished rapidly. This feature eliminates a long time delay in beginning a new acquisition when very low sweep speeds are in use. Thus, the next trigger signal received will begin a data acquisition at the new control setting, with no wait to complete a full record count with slow triggers.

Time Base Control Registers

Two write-only registers, Sample Rate register U436 and Acquisition Mode register U236, receive commands from the Microprocessor that control the sample rate and acquisition mode of the instrument. Sampling rate is determined by setting the Sample Period Divide Chain to produce different divide ratios of the 5-MHz clock (C5M). The sampling-period commands are loaded into register U436 as it is strobed with $\overline{\text{WRSR2}}$ from Strobe Control U146.

Acquisition Mode register U236 is loaded with commands that control the instrument operating mode. These commands are loaded in register U236 when the $\overline{\text{WRSR1}}$ strobe from U146 is applied, and they remain unchanged at the register outputs until new commands are clocked in by the next enabling strobe.

Trigger Control

The trigger select circuit (composed of U100A, U100B, U100D, and U434A) forms a gating circuit that allows either the A + Gate or the B + Gate signal to clock Trigger flip-flop U110A. At the beginning of the acquisition cycle, U110A is reset by the $\overline{\text{RSTACQ}}$ strobe. The AGTSEL signal from Acquisition Mode register U236 is applied directly to NAND gate U100A pin 2; this signal is also inverted by U434A and applied to NAND gate U100D. When AGTSEL is HI, the A + Gate causes U100A pin 3 to to go LO. This LO, along with the HI from U100D pin 11, causes U100B pin 6 to go HI for the duration of the A + Gate. The rising edge of the A + Gate sets Trigger flip-flop U100A, indicating that a trigger has been received.

When AGTSEL is LO (A + Gate not selected), NAND gate U100D is enabled to pass the B + Gate for use in clocking the Trigger flip-flop.

Both the A + Gate and the B + Gate continue on to the external A + GATE and B + GATE bnc connectors on the rear panel of the oscilloscope.

50-MHz Master Clock

A 50-MHz, crystal-controlled oscillator-and-dividing circuit composed of Y134, U230B, U230A, U220B, U128B, and U128A provides the clock frequencies that control circuit timing. The 50-MHz frequency is reduced to 25 MHz (C25M) by divide-by-two flip-flop U128A. A divide-by-five circuit composed of U230B, U230A, and U128B produces the 10-MHz clock (C10M), which is further reduced by divide-by-two flip-flop U220B to produce the 5-MHz clock (C5M). The 5-MHz clock is buffered by inverting amplifier U434B to produce the Microprocessor clock signal $\overline{\text{MPUCLK}}$.

Sample Rate Divide Chain

A divide chain comprised of U430, U424, U418, U510, U518, and U218C and D, provides the variable clock rates used to clock the Sample Rate Timing Generator. The Microprocessor, in response to TIME/DIV switch settings, programs the divide ratio of the chain. Sweep rates for A and A INTEN HORIZ DISPLAY are controlled by the A TIME/DIV switch, while ALT and B DLY'D HORIZ DISPLAY are controlled by the B TIME/DIV switch.

The programmed divide ratio reduces the 5-MHz clock (C5M) to the required clock frequency. Each counter in the divide chain is clocked on the rising edge of the clock pulse. Also clocked at the same time is U220A, a flip-flop used to synchronize the divide chain output with the rising edge of the 5-MHz clock.

Table 3-7 is a listing of the divide ratios and their respective final output clock frequencies from the divide chain, as produced by commands from the Microprocessor.

The data at the input of U436 is gated into the register when the Microprocessor activates the $\overline{\text{WRSR2}}$ strobe.

Located at the beginning of the divide chain is prescaling divider U430. It is programmed by the Microprocessor to divide by 2, 5, or 10 as determined by the data preset into the A, B, C, and D counter inputs. For example, a divide-by-two is accomplished in the following manner. In Table 3-7, the command for the chain to divide by two is FE_{16}. In binary notation, FE_{16} is 11111110, with AD7 being the most significant address bit.

Enabling inputs T (SRA) and P (SRB), arriving at U430 pin 10 and pin 7, will both be HI (address lines AD7 and AD6). Inputs T and P must be HI in order for the divide chain to function. Other logic combinations of the SRA and SRB bits are used in succeeding circuitry to select clock frequencies different from those produced by the divide chain.

The A and C inputs of U430 (pins 3 and 5) are connected together, while the B input (pin 4) is permanently LO and the D input (pin 6) is independently selectable. In the case of a divide-by-two, the inputs to U430 will be as follows: A, B, and C are LO, while D is HI. In binary notation, this corresponds to 1000, or decimal 8. Although the input is preset, the 8 count will not be placed in the counter until it is loaded by a LO on U430 pin 9 (the LOAD input).

When the Prescaler count reaches 9, the CARRY OUT output pin 15 is activated HI. This HI is applied to NAND gate U218D pin 12 along with the fixed HI on pin 13, causing the LOAD input at U430 pin 9 to go LO. The next rising edge of the clock will gate the preset 8 into the counter, and CARRY OUT will go LO. At the next clock rising edge, the counter will go to 9, which will again preset 8 into the counter. The count sequence then continues as 8,9,8,9,8,9,8,..., with each 9 count producing a CARRY OUT output.

To preset the divide chain, all the counters must initially reach a full count to produce a LOAD signal at the output. The counting cycle just prior to a loaded preset count occurs in the following sequence. Each counter in the chain is enabled by the CARRY OUT output from its preceding counter. Thus, each time the CARRY OUT of U430 goes HI, the T and P inputs of U424 are enabled, and U424 will count once. When the count of U424 reaches 9, its CARRY OUT is enabled, and U418 will begin to count. This cascaded operation continues until all the counters reach a full count of 9. At that point, the CARRY OUT of the last counter, U518, is activated HI. This HI is applied to NAND gate U218C pin 10 which, along with the HI from U430's CARRY OUT, is applied to U218C pin 9, causing U218C pin 8 to go LO. This LO is applied to each decade counter's LOAD input (pin 9), and the preset 9 placed on each of the counter's inputs (from register U436) is loaded into the counters.

From this point, in a divide-by-two routine, all the counters except U430 are preset to 9; and each time U430 counts from 8 to 9, the CARRY OUT is generated synchronously through the entire divider chain. This means that Prescaler U430 is performing the divide-by-two, while the rest of the divide chain is merely propagating the CARRY OUT, and the output clock frequency is 2.5 MHz.

The LO CARRY OUT from the last counter, U518, is also applied to synchronizing flip-flop U220A pin 2, and on the next rising edge of the C5M clock, the $\overline{\text{Q}}$ output of U220A is clocked HI. The CARRY OUT output from U430 to U218C pin 9 also starts LO on the same clock rising edge that clocked U220A pin 6 HI. The propagation delay involved in loading the preset input into U430 allows U220A pin 6 to complete its transition before the CARRY OUT output goes LO. This LO from U430 disables NAND gate U218C, and pin 2 of U220A goes HI.

Table 3-7

Sample Rate Divide Chain

Input to Sample Rate Register U436	Divide Ratio of Prescaler U430 (÷)	Four Stage Divide Chain (÷)	Output Clock Frequency (Sample Rate)
FE	2	1	2.5 MHz
FD	5	1	1.0 MHz
FC	10	1	500 kHz
FA	2	10	250 kHz
F9	5	10	100 kHz
F8	10	10	50 kHz
F2	2	100	25 kHz
F1	5	100	10 kHz
F0	10	100	5 kHz
E2	2	1,000	2.5 kHz
E1	5	1,000	1 kHz
E0	10	1,000	500 Hz
C2	2	10,000	250 Hz
C1	5	10,000	100 Hz

The next clock rising edge causes U430 to count from 8 to 9. However, before U430 CARRY OUT becomes HI again, the LO on U220A pin 2 is clocked through to become a HI on U220A pin 6. The pulse thus generated is 200 ns wide and is initiated with each LOAD input pulse.

By using different presets to both the Prescaler and the Divide Chain counters, other divide ratios are similarly set up to obtain the desired output sample clock frequency.

For servicing, jumper P420 in the divider chain LOAD line is removed to break the feedback loop, and the four-stage divider will only perform a divide-by-10,000.

Timing Signal Selector

The source of the sample rate clock is selected by multiplexer U120. A choice of 25 MHz (C25M), 10 MHz (C10M), 5 MHz (C5M), or the output of the Sample Rate Divide Chain, is available at the input pins of the multiplexer. The logic combinations of the SRA and SRB bits (AD7 and AD6) on U120 pins 2 and 14 control the switching function to select the clock frequency that was applied to the Sample Rate Timing Generator U436. See Table 3-8 for a listing of the selection combinations.

Table 3-8

Timing Signal Selection at U120

SRB	SRA	Timing Signal
0	0	25 MHz (C25M)
0	1	10 MHz (C10M)
1	0	5 MHz (C5M)
1	1	2.5 MHz to 100 Hz (From Divide Chain Output)

Sample Rate Timing Generator

Multiplexer U118 is switched by two output signals (LT2 and ENVL) from Acquisition Mode Register U236. These two signals select the clock frequencies to be used for the CONVERT and SAVE clocks that control the acquisition of data into the Acquisition Memory (Figure 3-23).

The rising edge of the CONVERT clock starts both data conversion by the A/D Converter and data storage into the Acquisition Memory. The SAVE clock signals the storage of a data byte and also clocks the Record Counter, the Time Interval Meter, and Chop Drive flip-flop U150B.

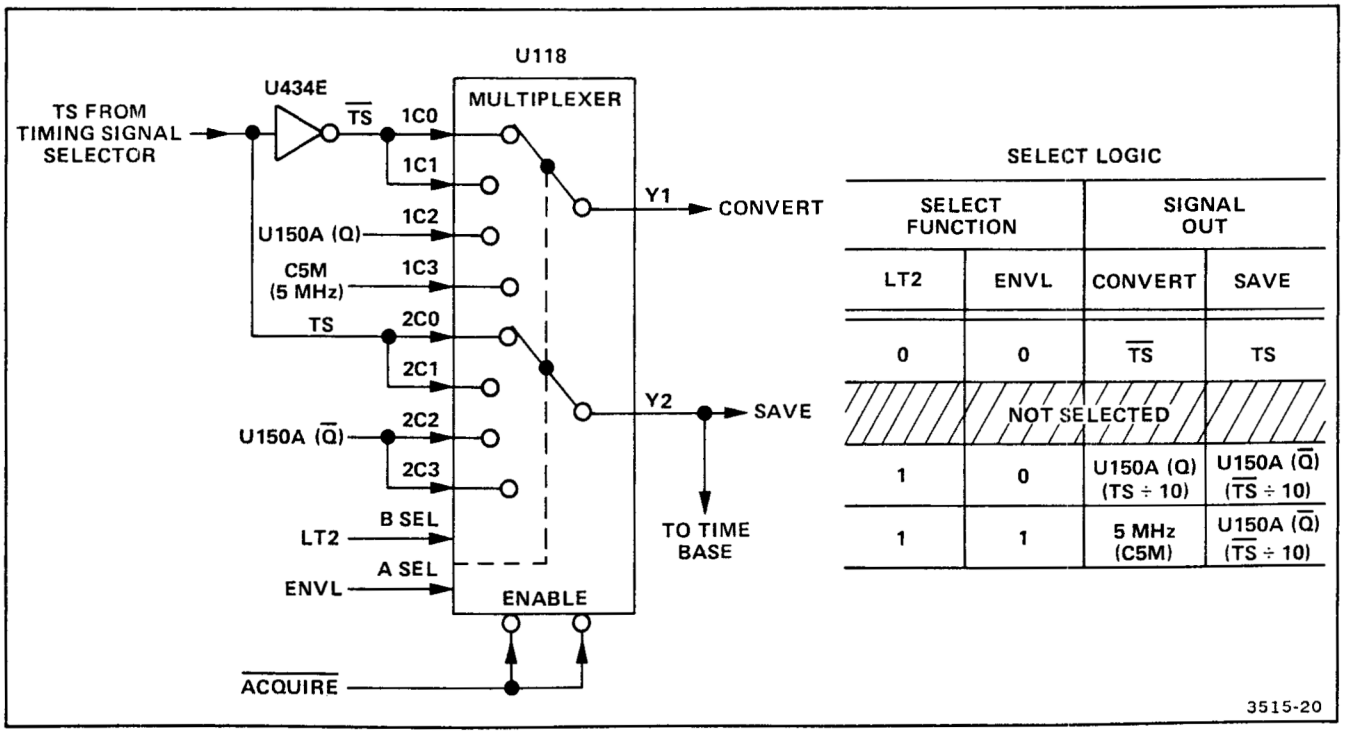


Figure 3-23. Simplified illustration of Multiplexer U118 switching operation.

For sample periods of 40 ns, 100 ns, and 200 ns, the CONVERT clock is the logical complement of the SAVE clock. Selection of TS and $\overline{TS}$ for the timing occurs when LT2 is LO. The inverted timing signal (inverted by U434E to $\overline{TS}$) is applied to the U118 $1C_0$ and $1C_1$ inputs at pins 6 and 5, while the noninverted timing signal is applied to the $2C_0$ and $2C_1$ inputs at pins 10 and 11. Multiplexer U118 gates the $\overline{TS}$ signal to output Y_1 (pin 7 CONVERT), and the TS signal is gated to the Y_2 output (pin 9 SAVE). See Figure 3-23 for a logic table of the multiplexer switching.

At sample periods slower than 200 ns and when in the NORM and AVG Storage Modes, the CONVERT clock is the Q output of flip-flop U150A, and the SAVE clock is the $\overline{Q}$ output. When ENVELOPE Storage Mode is selected, ENVL will be HI at U118 pin 14. Thus the CONVERT clock will be 5 MHz, while the SAVE clock frequency remains one-tenth of the timing signal TS.

The divide-by-10 circuit composed of U210, U150, and U218B is used to divide the timing signal by 10. The result is a square-wave output having a period equal to one-tenth of the timing signal (TS). The divided signal is synchronized with the rising edge of the 5-MHz clock pulse.

This square wave has a 50 percent duty cycle (symmetrical) rather than a rectangular pulse (Figure 3-24). To establish this condition, U210 is preset to 3 on each load. The A and B inputs (pins 3 and 4) are held HI and the C and D inputs are held LO for a fixed 3 at the four preset inputs. At a TS count of 8, the U210 Q_D line (pin 11) goes HI. This HI is applied to the D input (pin 2) of synchronizing flip-flop U150A. The next 5-MHz clock (C5M) rising edge clocks the HI on pin 2 to the Q output of U150A at pin 5.

When U210 reaches a count of 12, its Q_C and Q_D outputs are both HI. These HIs are NANDed by U218B to place a LO on the U210 LOAD input at pin 9. With LOAD enabled, the next TS clock rising edge at U210 pin 2 clocks the preset 3 into the counter, and Q_C and Q_D both go LO, thus removing the LOAD signal from U210. On the next 5-MHz clock rising edge at U150A pin 3, the LO from U210's Q_D output at pin 11 is clocked to the U150A Q output while the U150A $\overline{Q}$ output goes HI. Thus, the TS timing signal is divided by 10, and the transitions are synchronized to the rising edge of the 5-MHz clock.

The Q and $\overline{Q}$ outputs of U150A are applied to the selecting inputs of multiplexer U118 for use at sample periods longer than 200 ns. For sample periods of 40 ns, 100 ns, and 200 ns, the divide-by-10 counter is not used. For these sample periods, the 50-MHz Master Clock circuit produces the required clock frequencies of 25 MHz, 10 MHz, and 5 MHz.

The TS timing signal is also used to clock the low-speed Time Interval Meter at U100C pin 9 when TS/10 is selected for SAVE.

The $\overline{ACQUIRE}$ signal on U118 enabling inputs pins 1 and 15 is used to turn off the CONVERT and SAVE clocks when a waveform acquisition is not in progress.

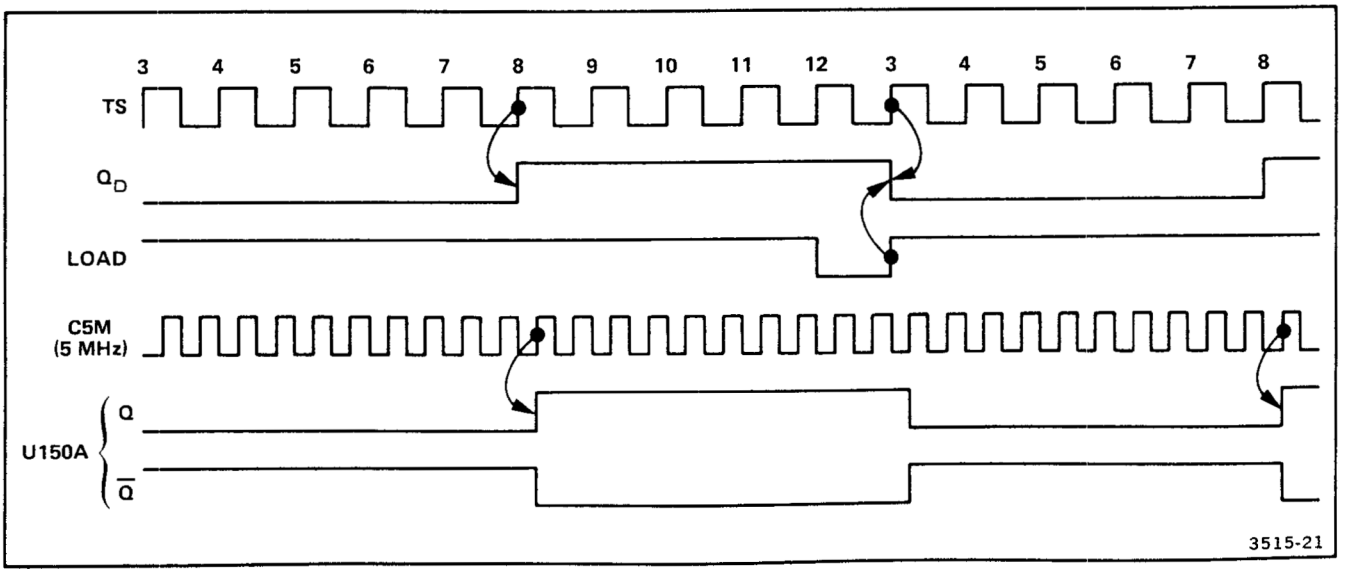


Figure 3-24. Sample Rate Timing Generator divide-by-ten timing diagram.

Record Counter

A circuit composed of U536, U540, U530A, U530B, U530C, and U524 records the number of samples obtained during an acquisition cycle. This circuit is used to determine the correct number of samples required to complete the cycle in progress after the oscilloscope trigger occurs. Post-trigger Storage Display requires 448 samples after the trigger, while Pretrigger operation requires 64 samples after the trigger occurs to complete the full 512-sample record length.

To accomplish the required count, the counter is preset either with 040_{16} (64_{10}) for post-trigger mode or $1C0_{16}$ (448_{10}) for pretrigger mode. The preset is loaded each time an acquisition is finished and when the STOP signal is set LO (before the acquisition is restarted). When STOP is LO, the enabling inputs to U540 pins P and T are also LO, and the counter is disabled.

Upon receiving a trigger signal, Trigger flip-flop U110A is set, and on the first rising edge of the SAVE clock, the STOP signal from flip-flop U110B is set HI. At that point, the counter begins to count up to 512, starting from the preset count previously loaded. Upon completing the count of 512_{10} (200_{16}), the Q_B output of U524 pin 13 is set HI to signal DONE to the Acquisition Memory.

The AND gates U530A, U530B, and U530C are used to produce an enabling signal to U524, the final counter in the chain. Each time U540 and U536 reach a full count (FF_{16}), both the P and T inputs of U524 will be HI to allow U524 to count once. In pretrigger operation, U524 only counts once to produce an output; in post-trigger operation it must count twice. The AND gates generate a faster CARRY OUT from U536 and U540 to U524 than the internal CARRY OUT circuits of the counters can provide.

Chop Drive

Flip-flop U150B is used to drive the digital storage Input Channel Switch U328 (diagram 13). Acquisition Register U236 provides the set and reset signals to the flip-flop (CH 1 and CH 2). Table 3-9 lists the switch logic of the flip-flop for selecting the input signal.

When chopping CH 1 and CH 2, the Acquisition Mode Control provides the SAVE0 signal from U440A pin 6 (diagram 14). The SAVE0 signal, applied to U150B pin 12, ensures that the data acquired from CH 1 and the data acquired from CH 2 will each be directed to the same part of the Acquisition Memory during each acquisition.

Table 3-9

Chop Drive Switching Logic

CH 1	CH 2	$\overline{\text{CHAN1}}$	Function
0	0	1	Not used
1	0	0	Selects CH 1
0	1	1	Selects CH 2
1	1	SAVE0	Chops Between CH 1 and CH 2

Flip-flop U150B is clocked by the SAVE clock (inverted by U434F). Since the SAVE clock is a square-wave signal, it provides symmetrical timing for CH 1 and CH 2 signal acquisition when chopping between the two inputs. When ALT Vertical Mode is selected, the Microprocessor alternately selects CH 1 and CH 2 for application to the Chop flip-flop to produce the switching signal to the Input Channel Switch (diagram 13).

Time Base Status Register

Part of register U240 in the Time Interval Meter circuitry is used as an Acquisition Status register. Status register strobe $\overline{\text{RDSTAT}}$ is provided by the Microprocessor at the end of each acquisition cycle. The Microprocessor polls the $\overline{\text{ACQUIRE}}$ signal, applied to U240 pin 14, to determine when the data acquisition is completed. $\overline{\text{ACQUIRE}}$ is generated in the Acquisition Mode Control circuitry (diagram 14) from U332A pin 5, and it tells the Microprocessor that the new acquired data can be read from the Acquisition Memory.

A second signal read is the A0M bit, also from the Acquisition Mode Control (U332B pin 9). This signal records the location of the trigger with respect to the current address (odd or even) being written into. The location of the trigger with respect to the current address is used to generate the most significant bit of the jitter correction data.

Time Interval Meter

Jitter correction signals are generated in a circuit that measures the time interval between the trigger point and the next rising edge of a SAVE clock. Due to the wide range of sample clocks used for acquiring data, two separate Time Interval Meter circuits are used. One of the two circuits is used for clock frequencies of 2.5 MHz or less and the other for 25 MHz, 10 MHz, and 5 MHz SAVE clocks.

The low sample rate counter is composed of counter U246 and NAND gate U100C. A clock frequency equal to 10 times the SAVE clock is used to produce a counting sequence from 0 to 9 by U246 during the time interval between trigger occurrence and the next rising edge of the SAVE clock. The actual count reached by the counter is a measure of the time interval between the two points.

When a trigger is received, flip-flop U110A pin 5 goes HI and the counter clear input (U246 pin 13) is released to begin counting from 0. This HI is also applied to U110B pin 13 to release the Reset input of the Stop flip-flop. The $\overline{Q}$ output (pin 8) of the Stop flip-flop is HI, and timing signal TS is gated through NAND gate U100C. Counter U246 counts the TS clocks until the next SAVE clock rising edge clocks U110B to make U110B pin 8 go LO, shutting off the timing signal clocks to U246 through U100C. The count stored in the counter is read by the Microprocessor from register U240 and is scaled to produce the jitter-correction data for the stored display.

The high-sample-rate (25 MHz, 10 MHz, and 5 MHz) Time Interval Meter circuit is composed of U446, U218A, U546, Q552, Q554, Q546, Q547, and Q544. These components, along with associated circuit components, form a counter that uses a dual-slope integrating technique to measure time intervals. The dual-slope technique is required because the TTL logic of the counter cannot handle clocking frequencies of 10 times the SAVE clock frequency for the high sample rates.

Transistor pair Q546 and Q547 forms a switchable 10-mA current source, and transistor pair Q554 and Q552 forms a 100-μA current source, either of which is used to supply a charging current to capacitor C538 during the counting intervals. Between counting intervals, the charge on C538 is held to zero by Q544 conducting the charging current to ground. The transistor pair supplying the capacitor charging current is selected by the state of STOP flip-flop U110B.

Initially, before a trigger is received, $\overline{\text{TRIG'D}}$ from U110A pin 6 is HI and TRIG'D on pin 5 is LO. When $\overline{\text{TRIG'D}}$ is HI, Q544 is conducting the charging current to ground. With TRIG'D LO, STOP flip-flop U110B is reset, and STOP at pin 9 is LO, while $\overline{\text{STOP}}$ at pin 8 is HI. STOP being LO turns on Q552, causing the 100-μA current source Q554 to be shunted to ground. Simultaneously, $\overline{\text{STOP}}$ is HI and Q546 is biased off, and the 10-mA current from Q547 is shunted through Q544.

When a trigger is received, $\overline{\text{TRIG'D}}$ goes LO and Q544 turns off, allowing the 10-mA current from Q547 to flow into C538. The current into C538 causes the voltage across C538 to ramp up.

On the first rising edge of the SAVE clock, after the trigger is received, Stop flip-flop U110B changes state and Q546 conducts, shunting the 10-mA charging current to ground. At the same time, Q552 is turned off, allowing a 100-μA charging current from Q554 to continue charging C538 at a rate reduced by a factor of 100 from the previous charging rate.

Counting begins when the charging rate is switched by simultaneously releasing the U446 clear inputs (pins 2 and 12). Counter U446 begins counting the 10-MHz clock (C10M) being applied through NAND gate U218A.

When the 100-μA charging current causes the voltage across C538 to reach 2 V, comparator U546 output at pin 7 goes LO to stop the 10-MHz clock, through U218A, to the counter.

The 100-μA charging current is capable of charging C538 from 0 to 2 V during the time required for the counter, counting the 10-MHz clock, to reach a count of 200. However, the 10-mA charging current is capable of charging C538 100 times faster. Thus, the actual count reached by the counter measures the time during which the 10-mA current was charging C538. Since the ratio of the 100-μA current to the 10-mA current is 100:1, each count is equal to 1/100 of the 10-MHz clock period, or 1 ns. Therefore, the high-sample-rate Time Interval Meter measures the time between the trigger and the next SAVE clock rising edge to within 1 ns.

Data from the Time Interval Meter is read from either register U440 or register U240, using the appropriate strobe. The Microprocessor then generates a horizontal offset that removes the displayed signal jitter caused by the one-sample-period uncertainty between the oscilloscope trigger and the sample clock.

A Typical Acquisition Sequence in the Time Base

The typical acquisition sequence begins with the Microprocessor loading the selected sample rate and acquisition mode into registers U436 and U236. Then the Microprocessor generates the $\overline{\text{RSTACQ}}$ strobe from U146 to arm Trigger flip-flop U110A and to reset Stop flip-flop U110B. The $\overline{\text{RSTACQ}}$ strobe also sets Acquire flip-flop U332A (diagram 14). The correct sample clock is selected by Timing Signal Selector U120, and CONVERT and SAVE clocks are sent to both the A/D Converter and the Acquisition Memory from Sample Rate Timing Generator U118.

If CH 1 and CH 2 are both selected in the CHOP Vertical Mode, the SAVE0 signal at pin 12 of Chop Drive flip-flop U150B will be clocked through on each falling edge of the SAVE clock and will drive the digital storage Input Channel Switch U328 (diagram 13). Using the SAVE0 signal to drive the Input Channel Switch ensures that the CHOP data for each waveform will be placed into the correct half of the Acquisition Memory (diagram 14).

When ALT Vertical Mode is selected, the Microprocessor controls CHOP Drive flip-flop U150 by alternately selecting CH 1 and CH 2.

When a trigger occurs, Trigger flip-flop U110A is set, and the Time Interval Meter measures the time between the trigger and the SAVE clock rising edge.

The trigger also starts the Record Counter to count from the preset value. When a count of 512_{10} is reached, the DONE signal is sent to the Acquisition Memory to set Acquire flip-flop U332A, thus stopping the CONVERT and SAVE clocks from Sample Rate Timing Generator U118.

When Microprocessor polls Acquisition Status Register U240, the $\overline{\text{ACQUIRE}}$ signal on U240 pin 4 will be HI, and at that time the acquired waveform data is transferred from the Acquisition Memory to the Display Memory. Then the Microprocessor reads the Time Interval Meter and processes it to produce a jitter-correction offset. Now the Microprocessor is free to start another waveform acquisition.

STORAGE DISPLAY CONTROL AND LED READOUT

The Storage Display Control circuitry (diagram 17) is located on the A16 Storage Display circuit board. A functional block diagram of the Storage Display Control and LED Readout circuitry is located in the "Diagrams" section in Volume II of this manual.

In the Storage Display Control circuitry, control strobes are generated that select the Microprocessor-controlled display functions. The digital storage front-panel switch positions are stored in registers located on the Storage Display board. These are scanned at regular intervals by the Microprocessor to check for switch position changes that will alter the present operating state of the oscilloscope. At power-on, the Service Test Switch Register is also read to determine whether the Power-On RAM test switch and the GPIB Option switch are set.

Strobe Control

The low byte of addresses (AD0-AD7) being accessed by the Microprocessor is latched into Display Strobe Control Register U207 on the rising edge of the Address Latch Enable pulse (ALE). From U207 outputs Q_1, Q_8, and Q_2, the latched addresses (LADR0-LADR2) are applied to two 3-to-8 decoders, U213 and U218.

Decoding of the latched addresses occurs as follows. The $\overline{\text{I/O}}$ strobe, produced by decoding the high-order addresses (diagram 18), is applied to pin 5 of both U213 and U218. When the I/O strobe is LO, decoding of the latched addresses occurs. Another enabling strobe determines which of the decoders will produce an output strobe. If address line A (ADRA) is HI on pin 6 of U213 while $\overline{\text{I/O}}$ is LO, U213 will produce a strobe. If latched address line 6 (LADR6) at pin 6 of U218 is HI while $\overline{\text{I/O}}$ is LO, U218 will produce an output strobe. The strobes generated are identified in the description of the circuitry with which they are used.

The LADR0-LADR2 addresses are also fed to the Vertical Mode switch (diagram 4), along with the $\overline{\text{I/O}}$ strobe, for generating the strobes needed in that circuitry.

Display Control Registers

Control data to the Storage Display Board is latched into the Display Control Registers, U223 and U228, from the AD0-AD7 Microprocessor Bus lines. The latching strobes are supplied by Latched Address Decoder, U218. The $\overline{\text{CONTRL}}$ strobe from U218 pin 14 latches control bits into U223, while the $\overline{\text{FPC}}$ strobe from U218 pin 15 latches control bits into U228. See Table 3-5 in the "Microprocessor" part of this section for a listing of the control bit assignments.

Storage Front-Panel Switches

The Microprocessor scans the front-panel switches at 100-ms intervals to determine if a change in a switch position has occurred. Switch positions are buffered by U743 (for VOLTS, TIME, NO. OF AVE, and XMIT) and U717 (for NON STORE, NORM, ENVELOPE, AVG, SAVE, SAVE REF, PRE TRIG/POST TRIG, and SINE/PULSE switches). The Microprocessor reads U717 when $\overline{\text{FP1}}$ is decoded by U218, and U743 is read when $\overline{\text{FP2}}$ is decoded.

A third switch register (Service Test Switch Register U713) is read when the $\overline{\text{DIPSW}}$ strobe is decoded by U213. The Service Test Switch Register is read at power-on to

determine whether the Option Present Switch (switch 8) is set on and whether the Power-On RAM Test Disable Switch (switch 7) is set for a normal power-on sequence. If the instrument is set up for servicing, the register will contain the binary number of the test routine to be performed by the Microprocessor.

Seven-Segment LED Indicators

The display seen on the four, seven-segment LED indicators is controlled by the Microprocessor using timing strobes to latch data from the Microprocessor bus into both U759 and U748. The segments of the indicators are controlled by U759, a binary-coded-decimal (BCD) to seven-segment decoder driver.

Segment control bits to be written into U759 from the Microprocessor are placed on the AD0 through AD3 bus lines. After the data has settled, the Microprocessor sends the $\overline{\text{SVNSEG}}$ strobe, from U218 pin 10, to latch the data into U759. These control bits are decoded by U759 to select the indicator segments that will be illuminated (Figure 3-25).

Each digit to be displayed is selected by the Microprocessor in a time-multiplexed sequence. Data placed on the AD0 through AD7 bus lines by the Microprocessor is latched into U748 when the $\overline{\text{LEDRO}}$ strobe, from U218 pin 11, is applied to U748 pin 11. The data written into U748 includes the scale-factor LED to be illuminated and the appropriate decimal-point-select bit.

Display multiplexing is done in the following manner. When U748 receives the $\overline{\text{LEDRO}}$ strobe, data present at the input pins of U748 is latched in. The data selects the appropriate scale-factor LED and controls the decimal point. However, at this time all the digits are disabled to blank the display while the seven-segment data is being changed in U759. During this blanking time, BCD information for the next digit to be displayed is latched into U759 by the $\overline{\text{SVNSEG}}$ strobe.

After the digit code is written into U759, new data containing the digit to be enabled is written into U748 (along with the repeated scale-factor information). If the decimal point is to be illuminated for the digit selected, that information is also written into U748 at the same time. See Figure 3-26 for the bit controlling plan for both U759 and U748. At this time, the selected digit will be enabled, and the segments of that digit will be illuminated as determined by the output of U759. A new digit is displayed approximately every 4 ms.

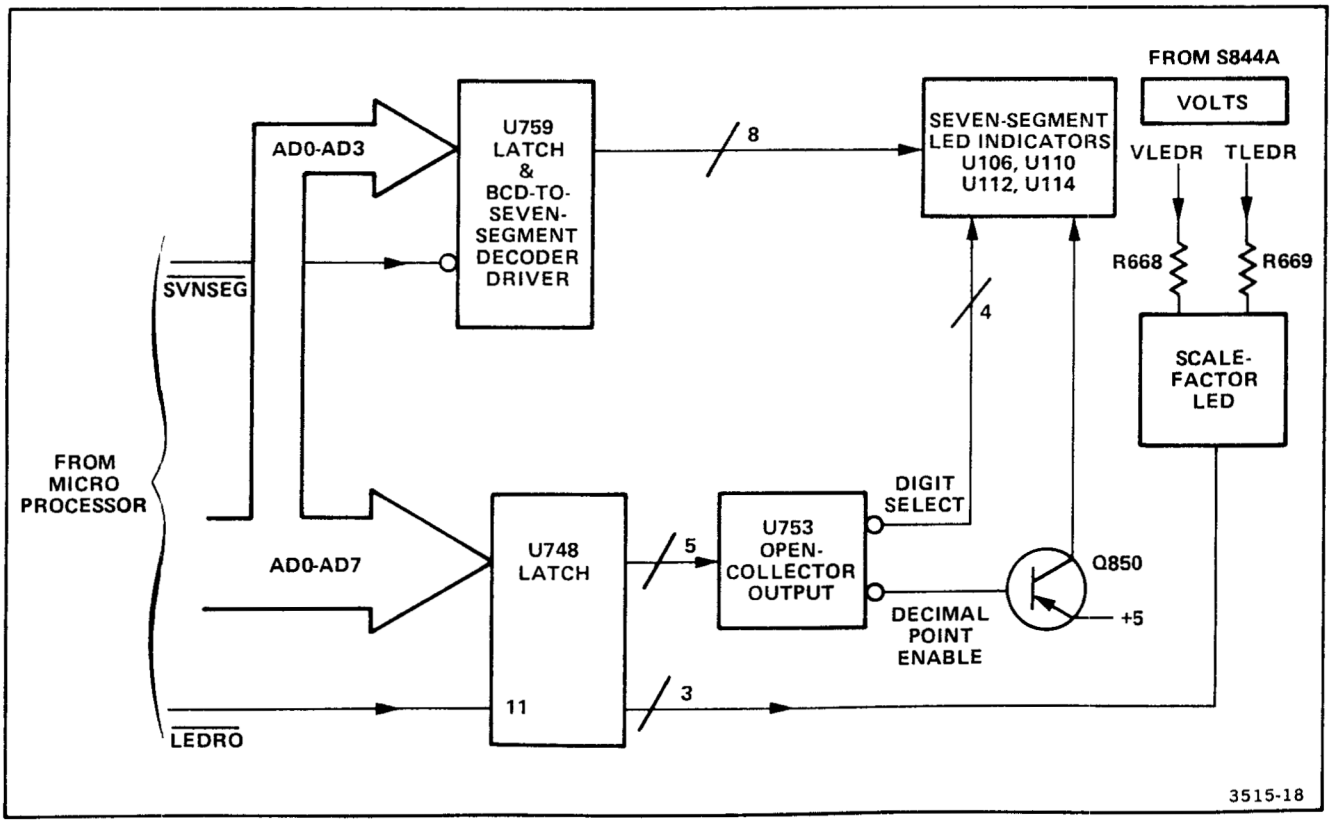


Figure 3-25. Simplified block diagram of the LED Display circuit.

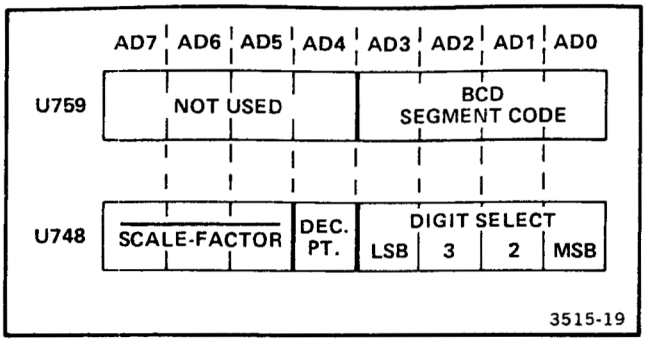


Figure 3-26. Bit controlling plan for U759 and U748.

The path for the driving current from U759 to the seven-segment LED indicators is via U753, which converts the TTL level outputs of U748 into open-collector outputs. Whenever a decimal point bit is written into U748 by the Microprocessor, the current path for the decimal point is provided by Q850.

The selected color of the bicolor, scale-factor LED (either red or green) is determined by the position of S844A, the VOLTS Cursor Function switch. When the switch is pushed in, R668 is connected to the +5-V supply, and the appropriate red LED will be illuminated by the output of U748. The green LED will be connected to the +5-V supply through R669 whenever the VOLTS push-button switch is out; a green LED selected by U748 will be illuminated to indicate the scale factor when a time measurement is being made.

STORAGE DISPLAY RAM AND Z-AXIS

The portion of the A16 Storage Display Board shown on diagram 15 performs several different functions. On this board a signal is produced to provide the drive to the Z-Axis circuitry of the oscilloscope for the display of cursors and stored waveforms. Other circuitry included is the Display Memory (a RAM) which stores the vertical data used to construct the displayed waveform. Additional circuitry produces the clocking and control signals required to time the operation of the display circuitry. A functional block diagram of the Storage Display RAM and Z-Axis circuitry is located in the "Diagrams" section of Volume II of this manual.

Display Control Register

Control bits are latched into U723 from the Microprocessor bus when the $\overline{\text{DISREG}}$ strobe is decoded from Latched Address Decoder U213 (diagram 17). Outputs from U723 are fed to U623 in the Display Control Logic circuitry to control starting and stopping the display. Other outputs are fed to the Storage Display X- and Y-Axis circuitry. The purpose of the output signals is discussed in the descriptions of the circuitry with which they are used.

Display Control Logic

Logic gating contained in the Display Control Logic circuitry combines signals to produce the select and write signals for the Display and Dot Memories. In addition, control bits latched into Display Control Register U723 are used to produce the display-on (DISPLAY) and display-done (DISDN) signals that indicate whether the display is either on or off.

The circuit composed of U623 and U618B provides the gating and output logic for starting and stopping the display. The START level (U723 pin 5) is ANDed with the DISDN signal coming from the $\overline{Q}$ output of U618B pin 8 and a 250-kHz frequency from U245 pin 3. This frequency is derived from the 5-MHz Microprocessor clock frequency ($\overline{\text{MPUCLK}}$) to clock flip-flop U618B.

When the display is off, DISDN from U618B pin 8 is HI. On the first falling edge of the 250-kHz pulse (after the START signal from U723 goes HI), U618B is clocked by the rising edge of the logic pulse from U623 pin 6. With START also applied to the D input of U618B pin 12, a HI is placed on U618B pin 9 to start the display (see Figure 3-27). Then DISDN will go LO, and both the 250-kHz clock frequency and the START level are no longer enabled through the logic gating.

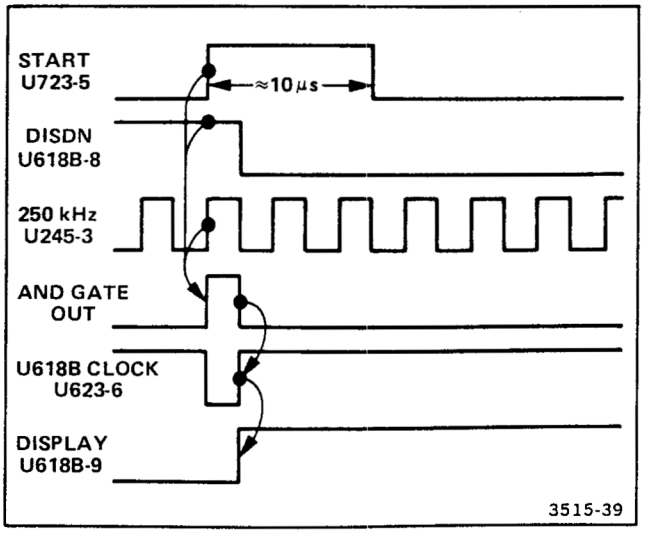


Figure 3-27. Display-start timing diagram.

The display is stopped by control bits from U723 and address outputs Q_7, Q_8, or Q_9 from Display Address Counters U413 and U418. A choice of 128 counts, 256 counts, or 512 counts is programmable by the Microprocessor. Setting HI any of the STOP control bits from U723 will enable one of the input gates of U623. When the Display Address count bit applied to the enabled gate also goes HI and then LO, the rising edge of the output from U623 pin 6 clocks U618B. The START signal on U618B pin 12 is LO, so U618B pin 9 (DISPLAY) goes LO to stop the display.

The Microprocessor can stop the display at any time by applying the $\overline{\text{STOPDIS}}$ signal (from U213 pin 7, diagram 17) to the reset input of U618B pin 13.

Clock Divider and Display Clock Multiplexer

In this circuitry the Microprocessor 5-MHz clock is divided in U245, a dual-decade counter, to produce 500-kHz, 250-kHz, and 50-kHz clocking signals (Figure 3-28). The 250-kHz clock is used to advance the Display Address Counters for all display except the ENVELOPE display.

For the ENVELOPE display, the minimum and maximum data point values are stored alternately in the Display Memory. The display is swept between the maximum and minimum values to produce the envelope fill, and then a 256-point minimum envelope and 256-point maximum envelope are displayed to complete the ENVELOPE display. Each address advance for the 256-point displays is done at a 500-kHz rate to obtain the same overall display rate for all the displays at the vertical signal output filter (diagram 16).

Both the 500-kHz and the 250-kHz clock signals are fed to one half of U528, a 4-line-to-1-line multiplexer used to select the Display Address Counter clock frequency. The 50-kHz frequency is fed to the Microprocessor circuitry (diagram 18) to be further divided and to provide one of the Microprocessor interrupt signals.

The other half of Multiplexer U528 is used to select the least significant address bit of the Display Memory. This bit comes from either the output of Address Counter U407 at pin 13 (Q_1) or the ODD signal from U223 pin 2 (diagram 17). The ODD signal selects either the odd or even Display Memory addresses during an ENVELOPE display.

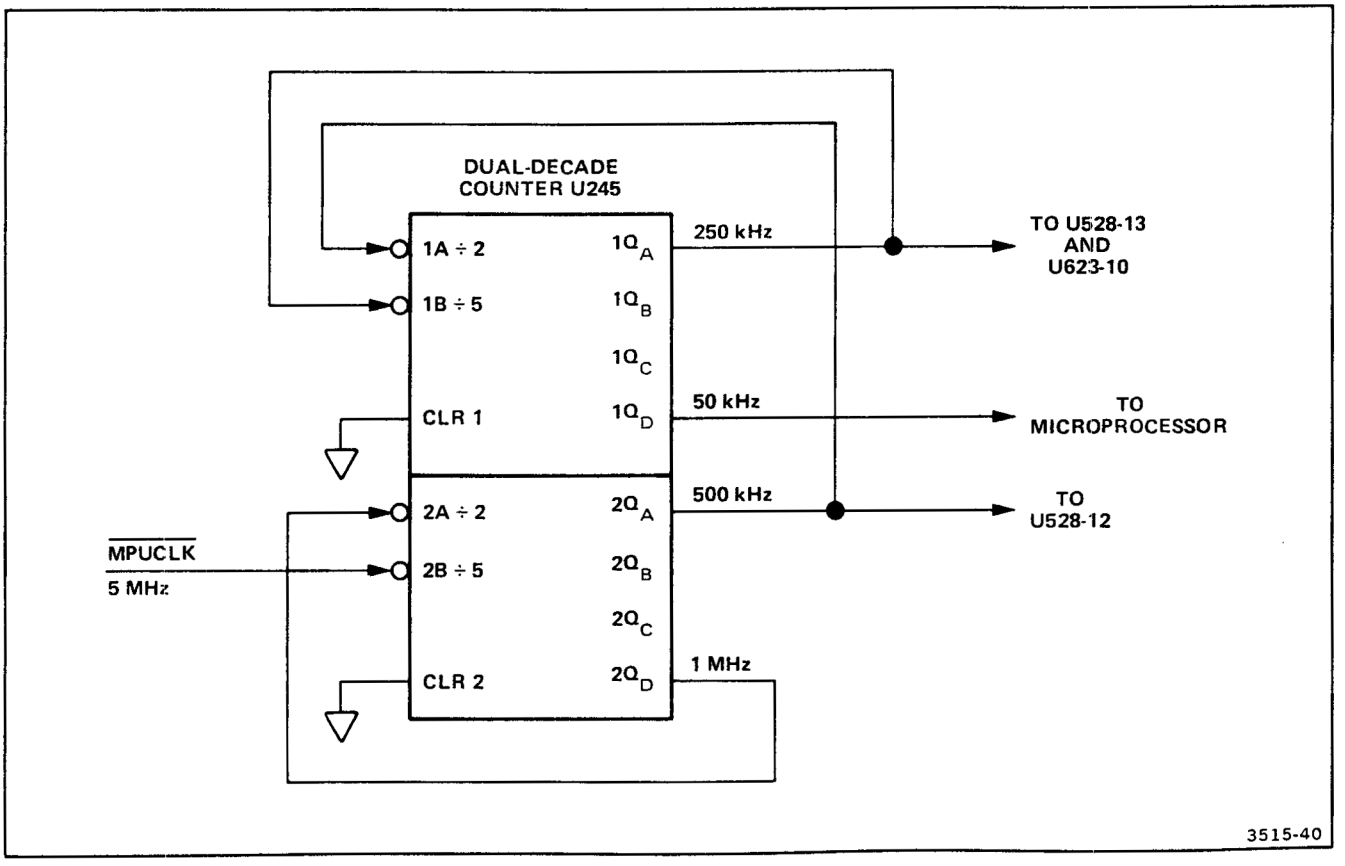


Figure 3-28. Simplified illustration of Clock Divider U245.

The Q_1 counter output controls the least significant bit of the Display Memory during a Microprocessor read or write cycle, and it controls all displays except ENVELOPE. During a read or write cycle, the Q_1 output of U407 follows the Microprocessor AD1 address or data bus line.

Switching of Display Clock Multiplexer U528 is done by the DISPLAY signal from U618B pin 9 and the BOTH signal (set by the Microprocessor from U223 pin 19, diagram 17). Table 3-10 provides a logic table for the Multiplexer switching operation.

Table 3-10

U528 Switching Logic Table

Display (B)	Both (A)	Memory LSB	Counter Clock	Function
0	0	ODD	$\overline{ALE}$	Microprocessor Read/Write
0	1	Q_1	$\overline{ALE}$	Microprocessor Read/Write
1	0	ODD	500 kHz	ENVELOPE Display
1	1	Q_1	250 kHz	All other storage displays

Display Address Counters

The Address Counter circuit, composed of U407, U413, and U418, performs a dual function. During a Microprocessor read or write of Display Memory, these counters latch the address to be accessed by the Microprocessor. Early in the address portion of the Microprocessor AD bus, DISSEL (from the Microprocessor Address Decoder, diagram 18) is gated through U643D to place each counter in the Load mode. Since the DISPLAY signal is LO, address latch enable signal $\overline{ALE}$ is selected by U528 to clock the address levels on bus lines AD0 through ADRA into the counters.

During the display of a stored waveform, the starting address of the display in memory is loaded into the counters by accessing the first data point address. The Q_0 level from U407 pin 14 is a HI (from the AD0 bus line) that is fed to the Track/Hold circuit in the Storage Display vertical circuitry (diagram 16) to place that circuitry in the Track mode.

The START signal from U723 pin 5 is set HI to prevent $\overline{ALE}$ from being selected by U528 to clock the Address Counters. With the DISPLAY signal HI, Display Clock Multiplexer U528 selects either the 500-kHz clocking signal (for ENVELOPE display) or the 250-kHz clocking signal (for all other displays) to increment the Address Counters. A HI DISPLAY signal enables U407, U413, and U418 as counters, and the count begins from the address of the first data point (access by the Microprocessor to set the starting point address). Counting continues until one of the STOP numbers set in U723 (STOP 128, STOP 256, or STOP 512) is reached to produce a DISDN signal from U618B.

Display and Dot Memories

The Display Memory RAM (U328 and U334) is selected by the inverted DISRAM signal from U238D pin 13, and the Display Memory Buffer is enabled (through U238A) to gate data either to or from the Display Memory. For a memory write, DISSEL is gated with WR through U643A to gate data through U731 from B to A into the Display Memory. When the memory is read, WR is LO, and data is gated from A to B in U731.

In a Microprocessor read from or write into Display Memory operation, U328 and U334 behave in the same manner as the Microprocessor System Memory.

Access to Dot Memory U234 is obtained in the same manner as just described for the Display Memory. However, in selecting the write only Dot Memory, the select signal (DOTRAM) is gated through U238C; while the Display Memory select signal (DISRAM) is not present. Thus neither Display Memory Buffer U731 nor the Display Memory is enabled.

To display a waveform, the Microprocessor loads the waveform's Y-Axis data point values into the Display Memory. If TIME Cursor dots are to be displayed, zeros are written into the Dot Memory at the two addresses of the data points to be intensified. The CSEL and $\overline{LINCUR}$ signals both are set to HI, placing a HI enabling level on U238D pin 11 and U238C pin 9. This allows both the Display Memory and the Dot Memory to be selected during the stored waveform display.

The START signal is sent, and the display is started as discussed previously. The Address Counters start counting at a 250-kHz rate, and vertical data is fed from the Display Memory to the Vertical digital-to-analog converter (DAC) in the Storage Display X- and Y-Axis circuitry (diagram16). Data continues out of the Display Memory until one of the STOP levels is reached by the Address Counters.

The Display Memory does not follow the Q_0 output of the Address Counter, so a data word goes to the vertical

DAC every 8 μs (125-kHz rate). However, the Dot Memory, which drives the Z-Axis output, does follow the Q_0 address line. This allows a dot to be placed between two vertical data points of the displayed waveform.

Line Cursors

When a VOLTS cursor is displayed, the value of the cursor's vertical position is latched into Line Cursors Register U737 by the $\overline{\text{LINER}}$ strobe. Then the $\overline{\text{LINCUR}}$ signal is set LO to enable the register output onto the display data bus, DD0-DD7. The $\overline{\text{LINCUR}}$ strobe going LO also prevents the CSEL signal at U523B pin 4 from enabling the Display and Dot Memories.

The Microprocessor then starts a display cycle with the STOP 128 level set (from U723 pin 6), and the cursor level is fed to the Vertical DAC to display a horizontal line.

Overrange/Underrange

A logic gating circuit composed of U631, U637, and U648 provides signals to force the Z-Axis to blank if the Y-Axis value is beyond the range of the digital display system (255-to-0). An all HI output on the vertical data bus is detected by U631, and an all LO output is detected by U637. If either of these conditions becomes true, a LO is gated to the output of U648. This LO is then applied to the D input (pin 2) of flip-flop U618A in the Z-Axis Control circuitry.

Another gating path through U648 is used to generate the dashed cursor display seen before a valid waveform has been stored in the Acquisition Memory. The ACTIVEL signal is generated by the Microprocessor, via U223 (diagram 17), and is then ANDed with the Q_2 output of the Address Counters to produce a square-wave output used to toggle flip-flop U618A.

Z-Axis Control

Control of the Z-Axis signal for the stored waveform display is accomplished by flip-flop U618A. If DASH (Q output, pin 5) is HI, the Z-Axis output will be on; and if LO, the Z-Axis will be off. During a ground reference dot display, the Z-Axis is forced on by setting $\overline{\text{ZAXON}}$ LO on the set input (pin 5) of U618A. If $\overline{\text{ZAXON}}$ is HI while DISPLAY (pin 1) is LO (display not running), the Z-Axis will be held off.

When the display is running, the logic output from U648 is clocked into U618A by the Q_0 bit (LSB) from U407. The Q_0 bit rising edge turns on the Z-Axis output after the new vertical data word has settled on the display data bus.

Z-Axis signal current is controlled by current-switching transistor pairs in five-transistor array U378. When the display is to be on, signal current is supplied to the oscilloscope Z-Axis circuitry (diagram 11) via J486.

When DASH from U618A is HI, the base of U378A becomes biased into conduction, and U378B switches off. If DASH is LO, U378B conducts to shunt the Z-Axis signal current to ground.

A dot is supplied similarly by the $\overline{\text{DOT}}$ signal from Dot Memory U234 controlling the conduction of the U378D and U378E transistor pair. When $\overline{\text{DOT}}$ is LO, Z-Axis signal current is supplied by U378E. No dot appears when $\overline{\text{DOT}}$ is HI.

Cursor Positioning

Positioning of both the VOLTS cursors and the TIME dots is performed by the circuit composed of U788, U776, and U770 in conjunction with the CURSOR control knob and CURSOR SELECT push-button switch. Two cursors are displayed (in either VOLTS or TIME Cursor mode), but only one cursor at a time is controlled by CURSOR control potentiometer R881. The CURSOR SELECT push-button switch S881B is a momentary contact switch. When S881B is closed, the A_6 input of Cursor Register U770 is pulled LO. It is pulled HI again as the switch is released. The pulse produced is the clock input to a control firmware toggle flip-flop that switches the active cursor. The stationary cursor will remain displayed at the position set by the CURSOR control knob.

The CURSOR control knob is an assembly made up of potentiometer R881 and switch pair S881A. While both contacts of S881A are closed, the linear voltage changes, produced at the wiper of R881, produce a linear change in the position of the active cursor. Near either end of the potentiometer rotation, one of the contacts of S881A will open, and the A_4 input of the Cursor Register will be pulled HI. With A_4 HI, the position of the active cursor will change more rapidly at a rate proportional to how far the knob is rotated.

The R881 wiper-arm voltage is applied to U788, a voltage-to-frequency converter. A digital logic output, with a frequency proportional to the voltage input level, is applied to the clock input (pin 12) of U776, a three-digit, BCD counter. At regular intervals, the Microprocessor reads the counter output through Buffer U770. The CURSOR strobe, generated from U213 (diagram 17), enables the counter output onto the Microprocessor bus to be read.

Timing of the Microprocessor read operation of U770 is as follows:

1. The PRDONE signal has a 10-ms period that is HI for 2 ms and LO for 8 ms. A rising edge of the PRDONE signal interrupts the Microprocessor (discussed in the "Microprocessor" circuit description) and stops the counter so the Microprocessor can read the current count.

2. The LATCH signal (U776 pin 10) is sent by the Microprocessor to latch the BCD digits.

3. The $\overline{\text{CURSOR}}$ strobe is sent to U770 to enable the first digit onto the Microprocessor bus.

4. The second digit is addressed by sending the ADVAN signal to the counter at pin 4.

5. The second digit is read.

6. Steps 4 and 5 are repeated to read the third BCD digit from the counter.

7. The RESET signal is applied to U776 pin 13 to set up the counter for the next counting sequence.

8. The PRDONE signal goes LO and again the counter starts counting the output frequency from U788.

The cursor position on the display moves in proportion to the count change derived from the CURSOR control knob rotation. If the count remains the same each time, the cursor position does not change. Increasing the count causes the active cursor to slew in one direction, and decreasing the count causes the active cursor to slew in the opposite direction from its current position. The linear displacement region of R881 moves the cursor position approximately one division before one of the contacts of S881A opens, causing the cursor position slew rate to increase.

STORAGE DISPLAY X- AND Y-AXIS

The circuitry shown on diagram 16 produces the X-axis and Y-axis signals to the oscilloscope horizontal and vertical amplifiers when a stored waveform is displayed. In addition, the normal trigger to the A and B Trigger Generator is selected from either the digital storage Input Channel Switch or the oscilloscope Vertical Switching Logic circuit. Channel 1 and Channel 2 vertical positioning signals are generated for use in waveform acquisition and during a SAVE Storage Mode display. A functional block diagram of the Storage Display X- and Y-Axis circuitry is located in the "Diagrams" section in Volume II of this manual.

Vertical Signal Path

Digital words representing either the eight-bit stored waveform or the 10-bit voltage cursors are applied to Vertical Signal DAC U435 and are converted to an analog current signal. The +7.5-V reference voltage applied to U435 pin 15 sets the reference current for digital-to-analog conversions.

The least significant bit and second least significant bit inputs (VLSB and V2SB) at pins 13 and 12 are used only during the voltage cursor display. For a stored waveform display, VLSB and V2SB are set LO.

Output current from DAC U435 is converted to a voltage by feedback amplifier U545. A feedback resistor for U545 is provided internally in U435 to allow simple connection of the amplifier. Since U545 is connected as an inverting amplifier, the voltage output ranges from zero, for all LO digital inputs to the DAC, to −7.5 V for all HI digital inputs.

Stabilization of the U435-U545 circuit is provided by C448, and diode CR342 protects the pin 1 output of U435 from reverse biasing that may occur during power-up. High-frequency bypassing of the supply voltages is supplied by capacitors throughout the circuit.

The vertical signal voltage, ranging from 0 to −7.5 V, is changed to signal current by R567 and applied to U571B pin 6, the inverting input of the operational amplifier. An offset current is added to the signal by R569 (from +VREF) to center the vertical signal around ground, and this signal is amplified with unity gain through U571B. The combination of feedback resistor R565 and input resistor R567 sets the gain, and R568 supplies a compensating bias current at pin 5 to balance out any leakage current. High-frequency compensation of the feedback circuit is provided by capacitor C570.

Vertical positioning current for a SAVE Storage Mode display waveform is added to the vertical signal at U571B pin 6. This signal comes from either U466B (the CH 1 Position switch) or U466A (the CH 2 Position switch). The method used to generate the vertical positioning signals is discussed later in this circuit description.

The output voltage from U571B is applied to pin 16 of Vertical Gain DAC U766 where it is converted to a current signal. The DAC is programmable by the Microprocessor to control the vertical expansion of the stored waveform display. Vertical gain data is latched into U766 from the Microprocessor bus by the $\overline{\text{VGAIN}}$ strobe from the Display Control circuitry (diagram 17). The vertical gain digital data is used to control the gain of U571A.

Feedback from the output of U571A pin 1 is applied to the V_{ref} input of U766 at pin 15. Gain of U571A is controlled by changing the amount of attenuation of the negative feedback signal introduced by U766 through programming from the Microprocessor. Increasing the attenuation decreases negative feedback and increases the amplifier gain. Conversely, decreasing the attenuation of the negative feedback signal decreases the gain of U571A. The signal current is added to the feedback current at U766 pin 1 and applied to the inverting input of U571A pin 2.

Voltage excursions from U571A are limited to the range of ±5 V by the network composed of CR664, CR665, CR666, CR667, and R670. The network is shunted by C571, a stabilizing capacitor for U571A. Additional stabilization for analog gains of less than 10X is provided by the circuit composed of Q570 (a p-channel, junction field-effect transistor) and R563.

When the VERTX10 signal is LO, Q570 is biased on, allowing R563 to act as a low impedance on the input pin of U571A, dampening its response. The low impedance of R563 is removed from the input circuit of U571A when Q570 is switched off by VERTX10 going HI. This allows the frequency response to increase for a X10 gain setting. The Vertical Gain DAC is never programmed for gains higher than 10.

From the output of U571A pin 1, the vertical signal is applied to pins 4 and 5 of analog switch U466C via R566. The combination of U466C, U523D, and C348 performs a sample-and-hold function. Large switching transients from the Vertical Signal DAC are rejected by allowing the vertical signal to be applied to U352 only after the signal has settled. New waveform data is being applied to the DAC inputs at a 125-kHz rate.

A 250-kHz signal is applied to AND gate U523D pin 12, and a 125-kHz signal is applied to pin 13. The AND gate is enabled when both input signals are HI, thus allowing U466C to pass the vertical signal to the input of amplifier U352 and charge the hold capacitor C348.

In the short time period that U466C is enabled, hold capacitor C348 must be charged to the new signal level. The RC combination of R566 and C465 aids the output of U541A in supplying the current required to rapidly charge C348. The hold capacitor retains the signal voltage level between each data level change.

Amplifier U352 is a unity-gain, operational amplifier with a high input impedance. The amplifier buffers the hold capacitor voltage level and supplies the signal current to an active filter network composed of U558 and associated components. The filter network has a third-order, low-pass response that approximates an ideal signal averaging filter for the vertical signal. The response of the filter is such that a step input produces a nearly linear vector from initial to final value at the output.

The filter circuit includes the Storage Vertical Centering adjustment (R345) that is used to supply an offset voltage through R348 that centers the stored display on the crt graticule. Output signals from U558 are applied directly to Storage Vertical Gain control R571. This gain control is used to set the attenuation of the signal path composed of R571, R580, R581, and C676 to the base of Q578. Transistors Q578 and Q580 are configured into a differential amplifier that converts the single-ended vertical signal into a balanced, differential output signal.

A diode switching circuit at the output of the differential amplifier selects either the stored signal or the A External Trigger View signal to be passed on to the oscilloscope Vertical Switching circuitry (diagram 3). During NON STORE mode operation, $\overline{\text{STORDIS}}$ at the base of U378C is HI, biasing it on and forward biasing CR584 and CR586. The stored display vertical signal current is shunted to ground through U378C; CR587 and CR585 are reverse biased to prevent any signal current from passing on to the oscilloscope Vertical Switching circuit. During a storage mode display, $\overline{\text{STORDIS}}$ is LO, U378C is biased off, and the stored signal is allowed to pass through CR587 and CR585 to be displayed.

In all modes (Storage and NON STORE), Q680 is biased on except when TRIG VIEW vertical mode is selected in NON STORE. When TRIG VIEW is selected in NON STORE, Q680 is biased off, and the A External Trigger View signal is allowed to pass through CR686 and CR684 to the Vertical Switching circuit to be selected for display.

Vertical Positioning

Both Channel 1 and Channel 2 positioning is accomplished by identical circuits. Channel 1 vertical positioning is discussed for the purpose of describing the circuit operation.

POSITIONING DURING ACQUISITION. Position voltage from the CH 1 POSITION potentiometer is buffered by unity-gain operational amplifier U374C and is then directly applied to the Acquisition Input Channel Switch (diagram 13) via P138 to offset the dc level of the waveform being acquired.

POSITIONING OF A SAVE STORAGE MODE DISPLAY. After a waveform is acquired and the SAVE mode entered, a positioning signal is produced to offset the dc level of the waveform display. The output voltage of CH 1 Vertical POSITION control buffer U374C is applied to a Track-and-Hold circuit composed of U373B, U377, U385, and U374D. The circuit is arranged as a successive-approximation A/D converter with a digital hold feature. The circuit uses closed-loop feedback to produce a voltage that tracks the output from the POSITION control.

Feedback voltage from U374D and position voltage from U374C are summed at the input of analog voltage comparator U373B pin 5. Output from U373B is applied to successive-approximation register U377 at pin 6.

The digital output of U377 is applied to DAC U385 where it is changed to an analog output current. Output current applied to the inverting input of feedback amplifier U374D is converted to a voltage level and applied to pin 5 of U373B, through R470, to form the complete closed-feedback loop.

At the start of each successive approximation conversion, the Q_0 output of U377 is HI, while all the other outputs are LO. The gain of U374D is set, via the feedback input of U385, to produce an output voltage equal to one-half of the POS REF voltage at U385 pin 15, but of the opposite polarity. The output of U374D is compared to the incoming vertical position voltage by U373B. If the output of U374D is higher than the vertical signal voltage, the output of U373B will go LO, and on the next rising edge of PRDONE, U377 will set its Q_0 output LO and its Q_1 output will go HI. The gain of U374D, as set by U385, will be reduced to lower its output to one-quarter of the POS REF voltage.

The new output voltage level is then compared to the vertical position voltage, and if the output is still higher, U377's Q_1 output will go LO and its Q_2 output will go HI to again lower the gain of U374D. However, if the output of U374D is now lower in magnitude than the vertical position voltage, U373B output will go HI when the comparison is made. On the next rising edge of PRDONE, Q_1 of U377 will remain HI and Q_2 will also switch HI. The gain of U374D is raised to produce an output voltage equal to 0.375 times the POS REF voltage.

With each clock, the output bits of U377 are set and tested until all eight bits have been checked. At the end of nine PRDONE cycles, the output of U377 is an eight-bit digital representation of the vertical position voltage, and the gain of U374D is set to produce a voltage level equal in magnitude but of opposite polarity to the vertical position voltage.

Upon entering the SAVE Storage Mode, TRACK/$\overline{\text{HOLD}}$ at U377 pin 9 goes LO, and the circuit enters the HOLD state. The current conversion in progress by U377 is completed, and then the output ceases to change state. The voltage output of U374D remains equal in magnitude, but of opposite polarity, to the vertical position voltage level that was present when the HOLD state was entered.

After SAVE Storage Mode is entered, and prior to any further vertical positioning, the position voltage at pin 15 of U466B is zero due to the summation of voltages from U374C and U374D through R472 and R473. Adjusting the Vertical POSITION control causes the voltage at U466B pin 15 to vary in proportion to the amount of rotation.

If a Channel 1 waveform has been stored, CH 1 POS at U466B pin 10 goes HI when SAVE Storage Mode is entered. Also the input voltage at pin 15 is connected to the vertical signal path at pin 6 of U571B. Any POSITION control voltage change is applied to the vertical signal dc level to effect positioning of the displayed signal.

Channel 2 SAVE positioning is accomplished in an identical manner by the circuit composed of U374A, U373A, U374B, U365, U359, and U466A.

If more than one channel is displayed, the position voltages are applied to the input of U571B in a time-shared manner to effect positioning of the appropriate trace. When ADD vertical mode is displayed, both U466A and U466B will close to allow both CH 1 and CH 2 POSITION controls to affect the vertical position of the ADD trace.

Horizontal Signal Path (X-Axis)

The voltage ramp that produces the horizontal deflection for the stored display originates in the Ramp Generator, composed of Q441, Q442, and U444. Just before the start of the sweep, DISDN at the gate of Q442 is HI, and Q442 is biased on to hold the collector of Q441 at a fixed level near ground potential. The actual voltage on the collector is determined by the JITTER signal (attenuated by R640 and R439) applied at the source of Q442.

The JITTER signal is produced by DAC U659 under control of the Microprocessor. This signal adds a horizontal offset to the ramp to compensate for the sample-clock-to-trigger jitter encountered in the Time Base (diagram 19). Output level of operational amplifier U553A is controlled by the data latched into U659 from the Microprocessor in the same manner as discussed previously in the "Vertical Signal Path" description. A new JITTER offset voltage is generated for each waveform display produced.

When DISDN (from U618B-8, diagram 15) goes LO, a 70-mV step occurs at the collector of Q441 as Q442 turns off. The step occurs as charging current (that had been flowing through Q442) starts flowing through C437 and R438. After the step, the collector voltage of Q441 continues to rise, but now with a constant slope, as C437 charges from the constant current supplied by Q441. The voltage reaches approximately 6 V in 4 ms, when DISDN goes HI again to reset the Ramp Generator at sweep end. The ramp voltage is buffered by U444, a unity-gain, high-impedance buffer amplifier.

The output ramp from U444 is applied to Horizontal Gain DAC U653, which with operational amplifier U553B, forms a programmable gain amplifier circuit similar in operation to the Vertical Gain DAC and amplifier, U766 and U571A, discussed previously. Under control of the Microprocessor, the stored display is expanded horizontally to the correct scale as determined by the TIME/DIV switch.

Refer to Figure 3-29 during the following circuit description. The ramp from U553 pin 7 is fed to Q569 in the Horizontal Amplifier (diagram 10). Transistor Q569 is a common-base amplifier that provides a low-impedance termination for the ramp output from U553B and a high-impedance output to the Horizontal Amplifier. Ramp current to Q569 is controlled primarily by R350 in series with Storage Horizontal Gain potentiometer R550. Horizontal offset current is added through R351 and the Storage Horizontal Centering potentiometer R346 to center the display horizontally.

High-frequency noise suppression for the horizontal ramp is provided by C570 and R567 (diagram 10). The time constant of C570 and R567 is long enough that, if an ideal ramp were applied, a significant amount of distortion in the ramp start would occur. However, the time constant of C570 and R567 is identical to the time constant of C437 and R438 in the collector circuit of Q441. The ramp has an initial step as a result of the action of C437 and R438 when the Ramp Generator started, and the step is canceled by C570 and R567. The resultant current signal to Q569 is close to an ideal ramp with very little noise present.

When the storage display is not in use, $\overline{\text{STORDIS}}$ at the base of Q345 goes HI to forward bias Q345. The storage horizontal ramp current is then shunted to ground to prevent it from reaching the Horizontal Amplifier.

Reference Voltages

The +7.5-V and −7.5-V reference voltages used by the Storage Display circuitry are generated in a circuit composed of U783, U559A, and U559B. A stable +2.5 V is output from pin 2 of U783, a reference voltage IC. Operational amplifier U559B multiplies the +2.5 V three times to produce a low-impedance +7.5-V source for $+V_{REF}$. The output of U559B is inverted with unity gain by U559A to produce $-V_{REF}$. Pull-up current to aid U559B in driving all of the required loads on the $+V_{REF}$ line is supplied through R287.

MAIN POWER SUPPLY

The Main Power Supply circuit (diagram 20) provides the operating power for this instrument from five regulated supplies. Regulation provides stable, low-ripple output voltages. Three unregulated output voltages are supplied for use in special circuit applications. Figure 3-30 shows a detailed block diagram of the Power Supply circuit.

Power Input

Power is applied to the primary of transformer T14500 through Line Fuse F14500, POWER switch S108, Thermal Cutout S14520, Line Voltage Selector switch S226, and Regulating Range Selector switch R216. Line Voltage Selector switch S226 connects the split primaries of T14500 either in parallel (for 115-V nominal operation) or in series (for 230-V nominal operation). Line Fuse F14500 value is selected to provide the required protection for each nominal line voltage. Refer to "Replaceable Electrical Parts" list in Volume II of this manual for correct fuse values.

Secondary Circuit

The −8-V, +5-V, +15-V, +55-V, and +110-V power supplies are series-regulated supplies. Amplifiers U712A, U712B, U506A, and U506B are two-channel, high-gain cells with differential inputs. These amplifiers monitor variations in the output voltages and supply correction information to the series-regulating transistors (except for the +110-V supply). The +55-V supply is the reference voltage source for the remaining supplies, and its output must be correct to enable the other supplies to operate within their regulating limits.

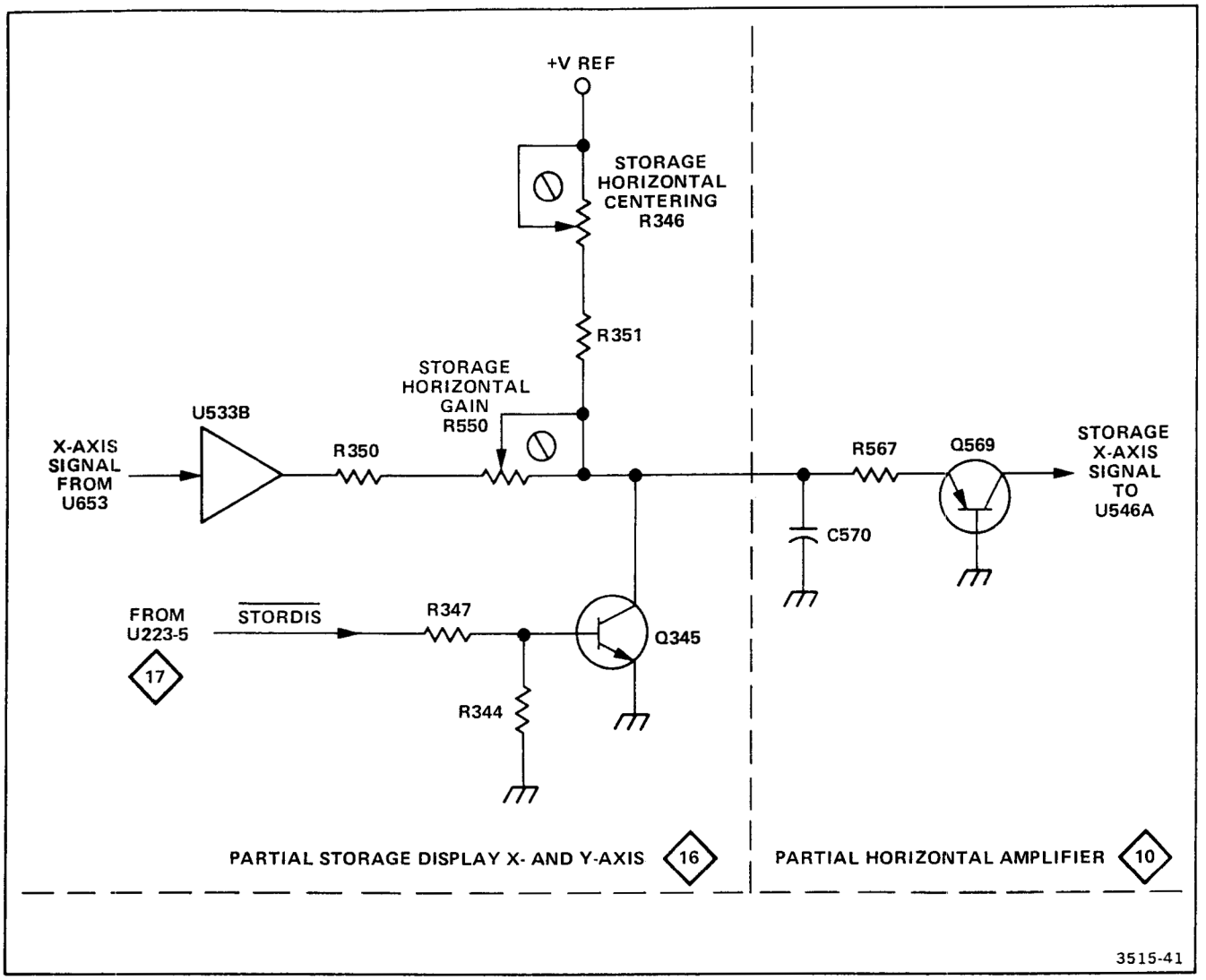


Figure 3-29. Partial circuit diagram of the Storage Display X-Axis signal path.

Current-limiting circuits provide short-circuit protection for each of the regulated supplies. The following description applies only to the +55-V current-limiting circuit; the other current-limiting circuits operate in a similar manner.

In the +55-V supply, Q606 is normally biased off. Under normal conditions, the base voltage of Q606 is about +55 V. Under conditions of power supply loading, when the supply current increases, the voltage drop across R602 (in the emitter circuit of Q501) increases. The increasing emitter voltage level is coupled through the base of Q501 to a voltage divider (composed of R508 and R507) thereby causing the base of Q606 to go more positive. If the +55-V supply is loaded down sufficiently, Q606 will turn on. The collector of Q606 then moves in the negative direction, and Q503 and Q501 begin turning off to limit the output current. Even though the supply is limited, transistor Q501 will continue to conduct current in order to produce enough voltage drop across R602 to keep Q606 biased on. The limited supply output voltage can be any value between its regulated value and zero, depending on the extra load it is trying to supply (Figure 3-31). The limiting transistors for the other supplies are:

+15 V	Q704
+5 V	Q617
−8 V	Q406
+110 V	Q740

Figure 3-31 also shows the action of the current limiting (foldover) circuit. At point A, Q606 begins conducting. At point B the supply is directly shorted to ground through a current meter.

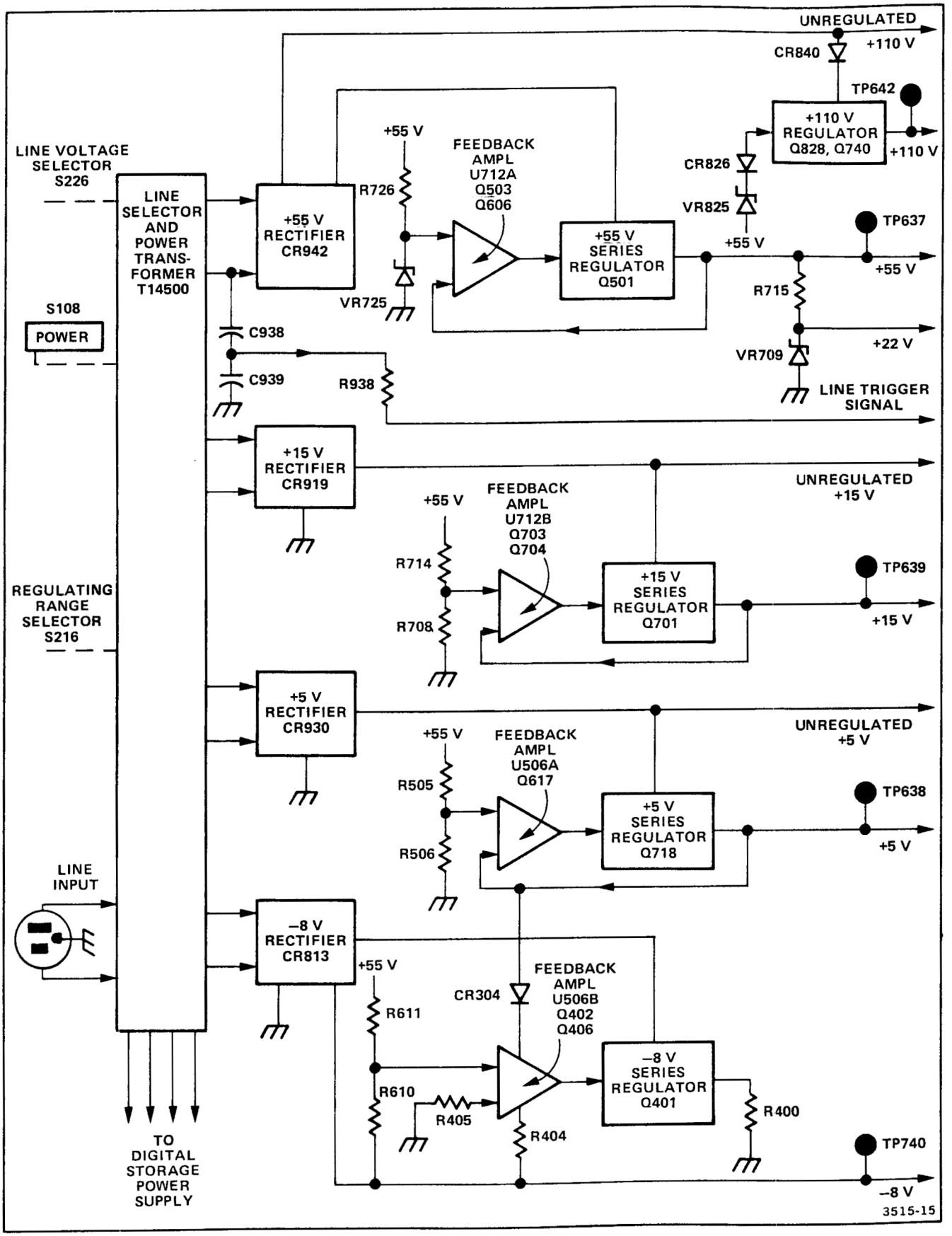


Figure 3-30. Detailed block diagram of the Main Low-Voltage Power Supply circuit.

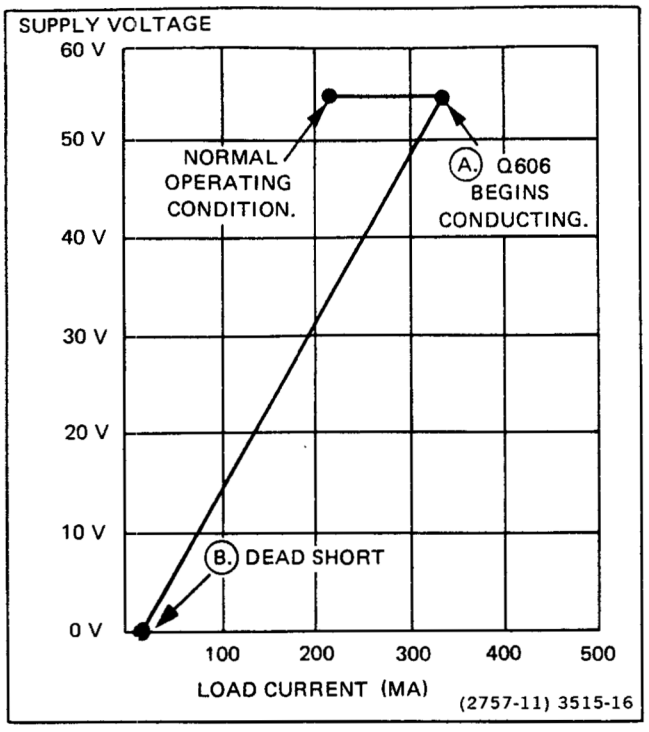


Figure 3-31. Foldover circuit action.

Two of the unregulated output voltages, +110 V and +15 V, supply the HV Oscillator circuitry of the CRT circuit (diagram 11). The third unregulated output, +5 V, supplies power to the Scale Illumination lamps.

A sample of the ac voltage (present in the secondary of T14500) is shaped by the circuit composed of C938, C939, and R932 and applied to the trigger circuitry for use in the LINE position of the A Trigger SOURCE switch.

STORAGE POWER SUPPLY

The Storage Power Supply (diagram 21) produces the low-voltage power required for the digital storage portion of the oscilloscope. A high-efficiency switching converter supplies the +5-VS high-current logic supply. Three-terminal regulators and associated circuitry provide the other stable, low-ripple output voltages. An unregulated source provides the fan supply voltage.

Power Input

Power is obtained from two fused secondaries of main power transformer T14500. The secondary voltage from the tapped secondary is applied to CR190, a full-wave bridge rectifier whose output is applied across filter capacitors C292 and C350. Noise-suppression capacitors C197 and C188 are placed across the secondary windings to reduce conducted interference back into the power source.

Prefiltering for both the +12-VS and +5-VS supplies is provided by C292, and C350 provides filtering for the −12-VS power supply.

Three-terminal regulators U190 (+12 V) and U560 (−12 V) provide all the regulation required for the + and −12-VS supplies. Additional bypassing to increase regulator stability is provided by C190 (from U190 pin 3 to ground) on the +12-VS output and by C558 and C560 on the −12-VS regulator.

In the −12-VS output, CR567 protects both U560 and the components in the output load from damage in the event of a short to a positive supply.

+5-V Switching Regulator

A high-efficiency regulator circuit composed of U470, U566A, Q380, Q280, Q259, and Q269 provides the +5-VS regulated output voltage. Three-terminal reference U470 produces a highly stable +2.5-V reference voltage used for the +5-VS supply and for the −6-VS supply. The reference is multiplied by two in U566A, a high-input-impedance operational amplifier, to supply a +5-V reference from a low-impedance source.

An RC filter composed of R471, R470, and C571 decouples the output of U566A to prevent switching transients at the base of Q380 from affecting the output of U566A.

The reference voltage is applied to the base of Q380, which is one-half of a voltage comparator used to turn switching transistors Q259 and Q269 on and off.

ASTABLE SWITCHING CIRCUIT. An astable switching circuit composed of Q380, Q280, Q259, and Q269 dynamically maintains the dc voltage present at the base of Q280 at the same level as the +5-V reference applied to the base of Q380. Steady-state circuit operation is described in the following discussion.

As an initial starting point, assume that Q259 and Q269 are beginning to conduct. Current through T160 produces a positive voltage step that is coupled through R278 and C279 to the base of Q380. The positive step turns Q380 fully on to drive to saturation Q259 and Q269, functioning as a Darlington pair. Supplying the collector current of Q259 from a tap on T160 allows Q269 to approach full saturation, thus obtaining more efficient switching.

In the steady-state operation of the circuit, the dc voltage at C162 is approximately +5 V. During the conduction time of Q269 and Q259, the voltage across C162 rises slowly as the current through T160 increases. At the same time, the voltage step at the base of Q380, applied when Q269 turned on, is decreasing rapidly as C279 discharges. When the base voltage of Q380 meets the base voltage of Q280, circuit operation begins to switch, and Q259 and Q269 begin to turn off. As they turn off, the induction of T160 forces a rapid negative step at the collectors of Q259 and Q269 that is coupled to the base of Q380 through R278 and C279. The negative step reinforces the turn-off sequence, which is in progress, to rapidly complete the switching. With Q259 and Q269 off, the current from T160 flows through clamp diode CR169, a Schottky power diode.

As the output load continues to draw current, the voltage across C162 slowly falls, while the base voltage of Q380 rapidly rises as C279 discharges the negative step applied at turn off. Again, when the base voltage of Q380 meets the base voltage of Q280, both Q259 and Q269 will begin to turn on to repeat the switching cycle.

When the circuit is operating at nominal input voltage, the switching frequency is set by the time constant of R278, C279, and R470 to approximately 30 kHz. As the input voltage and output loading vary, the operating frequency of the switching circuit varies to maintain regulation of the output voltage.

TURN-OFF SWITCHING. A circuit composed of C171, CR170, and R170 provides protection to Q269 during the transistor's turn off. When the collector voltage of Q269 starts to fall, CR170 becomes forward biased to allow current from T160 to flow through C171 until CR169 becomes forward biased and turns on. Therefore, Q269 does not have to handle the full current while the full supply voltage is present at turn off.

While Q269 is turning on, CR170 is back biased and C171 is charged up slowly through R170 to the output voltage. With C171 charged to the output voltage, CR170 becomes forward biased to allow current flow as soon as the voltage across T160 reverses in polarity. The current supplied by Q269 at turn on is limited to that current required by T160, and the current to charge C171 is supplied over a longer time period due to the time constant of R170 and C171.

OVERVOLTAGE PROTECTION. Overvoltage protection for the IC components supplied from the +5-VS power source is provided by a "crowbar" circuit composed of Q157, VR258, and associated components. Zener diode VR258 begins conducting if the +5-VS output exceeds about +5.6 V. When the current through VR258 is high enough to cause the voltage drop across R254 to reach the firing point of Q157, Q157 switches on and drops the output voltage to near ground potential, causing secondary supply fuses F4007 and F4009 to open. The current will continue to flow in Q157 until the flow drops below the maintaining current level.

Service jumper W158 may be removed to isolate the load from the power supply in the event it becomes necessary to perform troubleshooting of the +5-VS supply.

–6-VS Regulator

A separate secondary winding provides the source for the –6-VS supply. Secondary voltage is applied to diode bridge rectifier CR471, and the rectified output voltage from the bridge is filtered by C456. An unregulated output from this point is applied to the oscilloscope ventilation fan.

The input to U570, a three-terminal regulator, is bypassed by C572 to prevent the fan load from affecting the regulator input and to stabilize the regulator.

The –6-VS regulator circuit is composed of three-terminal regulator U570 (nominal –5.2-V output), operational amplifier U566B, and associated components. Pin 1 of U570 is not directly grounded but is held below ground potential by the output of U566B. The additional voltage to ground sets the output voltage level from U570 at –6 V. Operational amplifier U566B is a high-input-impedance device that sums the +2.5-V reference input and the –6-VS output from U570. Any rise in the –6 V toward ground will cause the output of U556B to go more negative, and U570 will pass more current to regulate the –6 VS output. Conversely, if the output of U570 should attempt to go more negative, the output of U566B would move in a positive direction to decrease the current output of U570.

Diodes CR472 and CR473 limit the negative output of U566B to less than approximately –1.4 V, protecting U570 and preventing large negative voltage swings when power is initially applied.

Overvoltage protection for the components supplied by the –6-VS output is provided by a "crowbar" circuit composed of Q577, VR479, and associated components.

GENERAL PURPOSE INTERFACE BUS (GPIB)

The GPIB Option (diagram 23) provides a digital output port for stored waveforms acquired by the 468. The GPIB is composed of an eight-bit bidirectional TTL bus for data transfer, acceptor and source handshake circuitry, one register for control of the interface logic, a buffer to report the current status of the interface to the Microprocessor, and a strobe generator under control of the Microprocessor. A functional block diagram of the GPIB circuitry is located in the "Diagrams" section of Volume II of this manual.

NOTE

Section 8 of the internal Service/Options switch must be set to the closed position to enable the GPIB option. Refer to Figure 5-6 in the Maintenance section of this manual for the switch location.

Strobe Generation

Timing of the interface read and write cycles is controlled by the Microprocessor via strobes generated by U450 and U460. Data present on the AD0 through AD2 Microprocessor bus lines is stored in U450 on the rising edge of the $\overline{ALE}$ signal (from the Microprocessor). When the GPIB is selected by the Microprocessor, the $\overline{GPIBSEL}$ signal is sent to U460 to enable it, and the control bits present on the U460 input pins are decoded to generate the appropriate control strobe.

The $\overline{GPIBSEL}$ signal is a decoded combination of the Microprocessor high address bits plus additional timing to ensure that the read and write cycles occur during a data portion of the Microprocessor cycle. At power-on, register U450 is cleared by the initializing signal ($\overline{INIT}$).

Status Buffer

Status Buffer U330 has the current interface status signals present at its input pins. When the $\overline{RIFSTAT}$ strobe is generated, the interface status is placed on the Microprocessor bus. These status signals are read by the Microprocessor to determine the next operation to be performed.

Control Register

Controlling signals from the Microprocessor are sent to the interface via Control Register U340. Data present on the Microprocessor bus is transferred to the U340 output pins on the rising edge of the $\overline{WIFCTL}$ strobe. The controlling signals remain at the output pins until the next $\overline{WIFCTL}$ strobe is received. The initializing power-on pulse ($\overline{INIT}$) clears Control Register U340.

Bidirectional Data Buffer

The Data I/O Buffer and Latch is composed of U350, U342, U168, and U152. These components send data to and receive data from the GPIB data lines. Message bytes to be placed on the bus from the Microprocessor are latched in eight-bit bytes, into U350 when the $\overline{WIFDO}$ strobe is applied to U350 pin 11. When the Source Handshake circuitry generates the $\overline{SHEN}$ signal, Bidirectional Buffers U168 and U152 place the data byte (present at the U350 output pins) onto the bus data lines.

When the $\overline{RIFDI}$ strobe is applied to U342 during the acceptor handshake, data from the GPIB is read by the Microprocessor, via U168 and U152.

Interrupt

The GPIBINT signal is generated by U310E, U442A and B, and U434C when a bus controller asserts the IFC or ATN signal. The interrupt signal is applied to the Microprocessor RST 5.5 pin to cause an interrupt of the routine in progress. Then the Microprocessor switches to the GPIB service routine.

When the LAT.IFC line from Control Register U340 is set HI (talker or serial poll condition), RIFC is latched into U442B. The latched IFC signal ($\overline{IFCL}$) output is supplied to Status Buffer U330 to be read by the Microprocessor. It is also applied to U434C at pin 11. It is inverted through U434C to become the Microprocessor unterrupt. When the interrupt is received, the Microprocessor reads the Status Buffer to determine the cause of the interrupt ($\overline{IFCL}$ or ATTEN). The LAT.IFC line from the Control Register is then cleared by the Microprocessor. At this time, if the IFC signal is unasserted, the interrupt is removed from the Microprocessor.

The Microprocessor will also be interrupted when the ATN signal is asserted by the bus controller. When the $\overline{RATN}$ signal is generated by the Acceptor Handshake circuitry, it is applied to U430A pin 4 (in the Source Handshake circuitry) and latched. The outputs of U430A are the ATTEN signal (applied to Status Buffer U330 at pin 4) and the $\overline{ATTEN}$ signal (applied to U434C at pins 9 and 10). The $\overline{ATTEN}$ signal is inverted by U434C and applied to the Microprocessor as the GPIBINT signal, and the GPIB service routine is started.

When the Microprocessor reads Status Buffer U330, the ATTEN signal indicates that a controller caused the interrupt by asserting the ATN signal. The Microprocessor clears U430A using the $\overline{ATNFLS}$ strobe after the ATN signal becomes unasserted. The $\overline{INIT}$ signal (applied at power-on to the U430A reset input at pin 1) also clears U430A.

TALK ONLY and Talk Address Switches

The 468 talk address is operator selected by setting switch S210. When the $\overline{\text{TALKREG}}$ strobe is applied to register U320, the Microprocessor reads the address switch setting information (from switch numbers two through six) on the AD0 through AD4 data bus lines. The TALK ONLY switch (number one) setting information is obtained from the AD7 data bus line.

Acceptor Handshake

The Acceptor Handshake circuitry controls the reception of data bytes from the GPIB. It is active when the ATN signal is asserted on the bus control lines. The negative logic ATN signal is received by U110 and is inverted to produce the RATN signal. This signal is again inverted by U310D to produce the $\overline{\text{RATN}}$ signal that is applied to U110 at pin 12. The $\overline{\text{RATN}}$ signal gates the TNDAC signal (from U410B pin 8) and the TNRFD signal (from U421A pin 12) onto the GPIB handshake lines.

Initially, TNDAC is HI and TNRFD is LO. When these levels are gated onto the bus handshake lines, the controller will put a new data byte on the bus and assert DAV, signaling that the new data is valid.

The DAV signal is received by U121 (in the Source Handshake circuitry), inverted to RDAV and applied to U421A pin 2, U410A pin 3, and U410B pin 13. When RDAV is HI, ATNDAV and TNRFD are both HI. During handshake, the Microprocessor polls Status Buffer U330. When the ATNDAV signal goes HI, the Microprocessor reads the data byte from the GPIB.

After the byte has been read, the Microprocessor sends the $\overline{\text{DATACC}}$ strobe to U410A pin 1 and U410B pin 11. Flip-flop U410A is cleared on the falling edge of $\overline{\text{DATACC}}$ thus removing ATNDAV from pin 5, and TNDAC goes LO on the rising edge. This signals the controller that the data byte has been accepted. When all the devices on the bus have signaled that the data byte is accepted, the DAV signal may be unasserted. The RDAV signal goes LO on U421A pin 2 and U410B pin 13, thus causing TNDAC to go HI and TNRFD to go LO. The interface is now ready for the next data byte to be placed on the bus.

Source Handshake

Placing data bytes to be transmitted onto the bus is controlled by the Source Handshake circuitry. This circuitry is active when the interface has been addressed as a talker and a bus controller is not sending IFC or ATN. Under these conditions, the TADS signal (at U434B pin 3 and U421C pin 10), $\overline{\text{ATTEN}}$ (at U434B pin 5 and U421C pin 9), and $\overline{\text{IFCL}}$ (at U442B pin 4) are all HI. The $\overline{\text{SHEN}}$ signal from U434B pin 6 becomes LO and is applied to Bidirectional Buffers U168 and U152 to gate the data latched into U350 onto the GPIB.

The TDAV signal is gated onto the bus handshake lines, and RNDAC and RRFD are inputs from the listeners on the line. Initially RNDAC is HI, RRFD is LO, nba is LO, SENT is LO, and TDAV is LO. When all the devices on the bus are ready for data, RRFD will become HI, and the Microprocessor will see a HI on the RRFD line (U330 pin 14) as it polls Status Buffer U330. The Microprocessor will then put a data byte on the bus and set nba HI (U434A pin 1). The TDAV signal becomes HI when SENT is LO and RRFD and nba are HI, and the GPIB listeners may read the data.

As the listeners on the bus read the data, they set their RNDAC signal lines LO. When all the listeners have accepted the data byte, the RNDAC control line will go LO, TDAV will go LO, and SENT (U440A pin 5) will go HI. This HI level is read from Status Buffer U330 by the Microprocessor and nba is set LO. The $\overline{\text{SNTACK}}$ strobe from U460 pin 14 is applied to U440A pin 1 to reset SENT LO. At this time, the data byte has been sent, and the Microprocessor starts looking for a HI on the Status Buffer RRFD line (pin 14) in preparation for sending the next data byte.

CALIBRATION

This section is in two parts. It contains a Performance Check and an Adjustment Procedure. The Performance Check is used to verify that the instrument meets the Performance Requirements listed in the Specification, while the Adjustment Procedure is used to restore the instrument to its original Performance Requirements.

The test equipment listed in Table 4-1, or an equivalent piece of test equipment, is required to accomplish a complete Performance Check and Adjustment Procedure. In Table 4-1, the specifications given for the equipment are the minimum necessary to provide accurate results. Therefore, the equipment used must meet or exceed the listed specifications. Detailed operating instructions for the test equipment are not provided in these procedures. Refer to the appropriate test equipment instruction manual if more operating information is required.

Table 4-1

Test Equipment Required

Description	Minimum Specification	Purpose	Examples of Suitable Test Equipment
1. Variable Autotransformer	Capable of supplying 1.5 A over a range of 108 to 132 V.	Power Supply Regulation check.	General Radio W8WT3VM Variac Autotransformer.
2. Digital Voltmeter	Range, 0 to 140 V; dc voltage accuracy, ±0.15%; 4 1/2 digit display.	Low-Voltage Power Supply checks and adjustments. CRT Grid Bias adjustment. Vertical and Horizontal Centering adjustments. Calibrator Output adjustment.	a. TEKTRONIX DM501A Digital Multimeter.[a] b. TEKTRONIX DM44 Digital Multimeter. c. Any digital multimeter that meets minimum specification.
3. DC Voltmeter	Range, 0 to 2500 V, calibrated to 1% accuracy at −2450 V.	High-Voltage Power Supply check.	a. Triplett Model 630-NA. b. Simpson Model 262.
4. Test Oscilloscope with 10X probe and 1X probe (1X probe is optional accessory)	Bandwidth, dc to 100 MHz; minimum deflection factor, 5 mV/div; accuracy, ±3%, dual trace. Probe, 10X scale-factor switching.	Power Supply Ripple check. CRT Z-Axis compensation. Vertical Gain adjustment. A Trigger Holdoff check. A and B + Gate Output Signal check.	a. TEKTRONIX 465B Oscilloscope with 2 (included) 10X probes. b. TEKTRONIX 475 Oscilloscope with 2 (included) 10X probes. c. TEKTRONIX P6101 Probe (1X). Part Number 010-6101-03.

[a] Requires a TM500-Series Power Module.

Table 4-1 (cont)

Description	Minimum Specification	Purpose	Examples of Suitable Test Equipment
5. Calibration Generator	Standard-amplitude accuracy, ±0.25%; signal amplitude, 2 mV to 50 V; output signal, 1 kHz square wave; fast-rise repetition rate, 1 to 100 kHz; rise time, 1 ns or less; signal amplitude, 100 mV to 1 V; aberrations, ±2%; high-amplitude output, 60-V pulse supplying at least 10 mA.	Vertical checks and adjustments. Trigger View checks and adjustments. X-Gain adjustment. Z-Axis check.	a. TEKTRONIX PG 506 Calibration Generator.[a] b. TEKTRONIX 067-0502-01 Standard-Amplitude Calibrator (amplitude calibrator only). c. TEKTRONIX Type 106 Square-Wave Generator (fast-rise and high-amplitude only).
6. Sine-Wave Generator	Frequency, 350 kHz to above 100 MHz; output amplitude variable from 0.5 to 5.5 V p-p; output impedance, 50 Ω; reference frequency, 50 to 350 kHz; amplitude accuracy, constant within 3% of reference frequency as output frequency changes.	Vertical Centering checks and adjustments. Bandwidth and Isolation checks. Trigger checks and adjustments. X-Y Phase Difference check. X Bandwidth check.	a. TEKTRONIX SG 503 Leveled Sine-Wave Generator.[a] b. TEKTRONIX Type 191 Constant-Amplitude Signal Generator.
7. Time-Mark Generator	Marker outputs, 2 ns to 0.5 s; marker accuracy, ±0.1%; trigger output, 1 ms to 0.1 μs, time-coincident with markers.	CRT Y-Axis and Geometry adjustments. Auto Trigger check. Horizontal Timing checks and adjustments.	TEKTRONIX TG 501 Time-Mark Generator.[a]
8. Low-Frequency Generator	Frequency, 60 Hz to 100 kHz; output amplitude, variable from 30 mV to 4 V p-p; positive square-wave output amplitude, 5 V.	Low-Frequency Trigger checks. Vertical compensation.	TEKTRONIX SG 502 Oscillator.[a]
9. Function Generator	Frequency response, less than 1 Hz to 1 kHz; sinusoidal output amplitude, variable up to greater than 5 V p-p.	AC-Coupled Lower −3 dB Point check.	TEKTRONIX FG 501 Function Generator.[a]
10. HV Probe	1 kV to 40 kV dc; input resistance, 1000 MΩ; accuracy, ±1% to 25 kV dc.	HV measurement using DMM in lieu of DC Voltmeter.	TEKTRONIX HV Probe. Part Number 010-0277-00.
11. 50-Ω Signal Pickoff	Frequency response, 50 kHz to 100 MHz; 50-Ω impedance for signal input, signal output, and trigger output.	Trigger checks and adjustments.	TEKTRONIX CT-3 Signal Pickoff. Part Number 017-0061-00.
12. Cable (2 required)	Impedance, 50 Ω; length, 42 in; connectors, bnc.	Signal interconnection.	Tektronix Part Number 012-0057-01.

[a] Requires a TM500-Series Power Module.

Table 4-1 (cont)

Description	Minimum Specification	Purpose	Examples of Suitable Test Equipment
13. Cable (2 required)	Impedance, 50 Ω; length, 18 in; connectors, bnc.	Signal interconnection.	Tektronix Part Number 012-0076-00.
14. Adapter	Connectors, GR874-to-bnc female.	Signal interconnection.	Tektronix Part Number 017-0063-00.
15. Adapter	Connectors, GR874-to-bnc male.	Signal interconnection.	Tektronix Part Number 017-0064-00.
16. Adapter	Connectors, bnc female-to-bnc female.	Signal interconnection.	Tektronix Part Number 103-0028-00.
17. Adapter	Connectors, bnc female-to-coaxial cable connector.	Signal interconnection.	Tektronix Part Number 131-1315-01.
18. Adapter	Connectors, bnc male-to-miniature probe tip.	Signal interconnection.	Tektronix Part Number 013-0084-01.
19. Dual-Input Coupler (2 required)	Connectors, bnc female-to-dual-bnc male.	Vertical checks. Trigger checks and adjustments. X-Y Phase check.	Tektronix Part Number 067-0525-01.
20. T-Connector	Connectors, bnc.	Signal interconnection.	Tektronix Part Number 103-0030-00.
21. 10X Attenuator (2 required)	Ratio, 10X; impedance, 50 Ω; connectors, bnc.	Vertical compensation. Vertical Bandwidth check. Trigger adjustments.	Tektronix Part Number 011-0059-02.
22. 5X Attenuator	Ratio, 5X; impedance, 50 Ω; connectors, bnc.	Vertical System compensation. Trigger adjustments.	Tektronix Part Number 011-0060-02.
23. 2X Attenuator	Ratio, 2X; impedance, 50 Ω; connectors, bnc.	Vertical System compensation. Trigger adjustments.	Tektronix Part Number 011-0069-02.
24. Termination (2 required)	Impedance, 50 Ω; connectors, bnc.	Signal termination.	Tektronix Part Number 011-0049-01.
25. Screwdriver	Length, 3-in shaft; bit size, 3/32 in.	Adjust variable resistors.	Xcelite R-3323.
26. Low-Capacitance Alignment Tool	Length, 1-in shaft; bit size, 3/32 in.	Adjust all variable capacitors.	J.F.D. Electronics Corp. Adjustment Tool Number 5284.
27. Shorting Strap		Calibrator adjustment.	

[a]Requires a TM500-Series Power Module.

PERFORMANCE CHECK

PURPOSE

The Performance Check is used to verify the Performance Requirements as listed in the Specification (section 1) and to determine the need for recalibration (adjustment) of the product. Removing the instrument's dust cover is not necessary to perform this procedure. All checks are made using the operator-accessible controls and connectors.

LIMITS AND TOLERANCES

The limits and tolerances given in this procedure are valid only if the instrument has been calibrated at an ambient termperature between +20°C and +30°C, the instrument is operating at an ambient temperature between −15°C and +55°C (unless otherwise noted), and the instrument has had a warmup period of about 20 minutes.

TEST EQUIPMENT REQUIRED

The following equipment is required to perform a complete Performance Check. The numbers preceding equipment types correspond to the items listed in Table 4-1.

4. 10X Scale-factor-switching Probe (supplied with 468)

5. Calibration Generator
   a. Square-Wave Generator
   b. Amplitude Calibrator

6. Leveled Sine-Wave Generator

7. Time-mark Generator

8. Low-Frequency Sine-Wave Generator

9. Function Generator

11. 50-Ω Signal Pickoff Unit (Type CT-3)

12. 42-in, 50-Ω Bnc Cable (2 required)

15. GR-to-bnc-male Adapter

16. GR-to-bnc-female Adapter

18. Bnc-to-miniature-probe-tip Adapter

19. Dual-Input Coupler (2 required)

20. Bnc T-Connector

21. 10X Bnc Attenuator

22. 5X Bnc Attenuator

23. 2X Bnc Attenuator

24. 50-Ω Bnc Termination (2 required).

At the beginning of each subsection there is also a list showing only the test equipment necessary for performing the steps in that subsection. In this list, the number that precedes each piece of equipment corresponds to the item number listed in Table 4-1.

SPECIAL FIXTURES

Special fixtures are used only where they simplify the test setup and procedure. These fixtures are available from Tektronix, Inc. Order by part number through your local Tektronix Field Office or representative.

TEST EQUIPMENT ALTERNATIVES

When equipment other than that recommended is used, control settings or the test setup may need to be altered. If the exact item of equipment given as an example in the Test Equipment list (Table 4-1) is not available, first check the Minimum Specification column carefully to see if any other equipment might suffice. Then check the Purpose column to verify use of this item. If it is used for a check that is of little or no importance to your measurement requirements, the item and corresponding steps may be deleted.

PREPARATION

Before performing this procedure, ensure that the Regulating Range Selector and Line Voltage Selector switches are set for the line voltage being used (see "Preparation for Use" in the "Operating Instructions" section of this manual). Connect the test equipment and the instrument to be checked to an appropriate ac-power-input source.

Power-On Self-Test

When power is applied to the 468, the instrument's Microprocessor performs a self-test to check the operational capability of the digital circuitry. Should an error be detected during the self-test, the seven-segment LED indicators will display an error code to aid in locating specific circuitry that is malfunctioning.

To check the power-on self-test, either select the NON STORE function (push button in) or ensure that both the VOLTS and TIME Cursor Function push buttons are released before applying power to the instrument. When the POWER switch is set to ON (button pressed in), self-test commences immediately. All the segments and decimal points of the display and all of the LED indicators read by the Microprocessor are illuminated (the seven-segment display is 8.8.8.8). Then a series of zeros will begin appearing on the display as checks of the random-access and read-only memories are made. The zeros flash rapidly and continue until all four digits indicate zero (0000). At that point, if the test is passed, the 468 will power up in an operating mode, and the seven-segment indicators will go blank.

Any seven-segment LED display that remains upon completion of the self-test is an error message. Should an error display be generated, cycle the POWER switch off, then on again to restart the self-test. If the error indication remains after the second power-on attempt, refer the instrument to qualified service personnel.

After checking the self-test, turn the INTENSITY control fully counterclockwise and allow a 20-minute warmup period of the 468 and all the test equipment before commencing the Performance Check.

INDEX TO PERFORMANCE CHECK PROCEDURE

VERTICAL

Equipment Required (see Table 4-1):

4. 10X Scale-factor-switching Probe
5. Calibration Generator
6. Leveled Sine-Wave Generator
8. Low-Frequency Sine-Wave Generator
9. Function Generator
12. 42-in, 50-Ω Bnc Cable (2 required)
18. Bnc-to-probe-tip Adapter
19. Dual-Input Coupler
20. Bnc T-Connector
21. 10X Bnc Attenuator
22. 5X Bnc Attenuator
23. 2X Bnc Attenuator
24. 50-Ω Bnc Termination (2 required)

468 CONTROL SETTINGS

POWER	ON (button in)

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2 if applicable)

VERT MODE	CH 1
POSITION	Midrange
VOLTS/DIV	5 mV
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC	GND
INVERT	Normal (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Trigger (A and B if applicable)

COUPLING	AC
LEVEL	Midrange
SLOPE	+
SOURCE	NORM
TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep (A and B if applicable)

HORIZ DISPLAY	A
TIME/DIV	1 ms
TIME/DIV VAR	Calibrated detent
DELAY TIME POSITION	Fully counterclockwise
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

NON STORE	On (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check TRACE ROTATION

a. Position trace to the center horizontal graticule line.

b. CHECK—Trace is parallel with the center horizontal graticule line. Readjust TRACE ROTATION (front-panel screwdriver adjustment) if necessary.

2. Check ALT Mode

NOTE

The VERT MODE switches are push-push types that must be pressed to select a particular VERT MODE and pressed again to remove the trace from the crt display. For example, selecting CH 1 VERT MODE does not release any VERT MODE switch previously selected. The CH 1 VERT MODE switch must be pressed again to remove the CH 1 trace from the display.

a. Set:

VERT MODE	CH 1, CH 2, A TRIG VIEW, ADD, and ALT
A TRIGGER SOURCE	EXT

b. Use the CH 1 and CH 2 Vertical POSITION controls to space the CH 1, CH 2, and ADD traces approximately

2 divisions apart. Use the A TRIGGER LEVEL control to position the A TRIG VIEW trace below the vertical channel traces.

c. CHECK—Sweep alternates in all settings of the A TIME/DIV switch except STOR ONLY (1, 2, and 5 s per division) and X-Y. The order of alternate traces is as follows: CH 1, CH 2, ADD, and A TRIG VIEW.

NOTE

At sweep speeds of 2 ms per division and faster, the trace alternations occur rapidly and cannot be seen.

d. Release ADD and A TRIG VIEW VERT MODE push buttons to remove their traces from the crt display.

3. Check CHOP Mode

a. Set:

A TIME/DIV	1 μs
A TRIGGER SOURCE	NORM
VERT MODE	CH 1, CH 2, and CHOP

b. Use the Channel 1 and Channel 2 Vertical POSITION controls to position the two traces about 4 divisions apart.

c. Adjust the A TRIGGER LEVEL control for a stable display of the CHOP frequency.

d. CHECK—Period of one cycle is approximately 2 μs (2 horizontal divisions).

e. Press in the ADD and A TRIG VIEW VERT MODE switches.

f. CHECK—Chopped mode display has four levels.

g. CHECK—Display for blanking of switching transients.

h. Press ADD, A TRIG VIEW, and CH 2 push buttons to remove their traces from the display.

4. Check CH 1 and CH 2 Balance

a. Set:

VERT MODE	CH 1

b. Position trace to the center horizontal graticule line.

c. CHECK—Trace shift is 1.0 division or less as the CH 1 VAR control is rotated from one extreme of its range to the other. (CH 1 UNCAL LED is illuminated when the VAR control is out of the detent position.)

d. Return CH 1 VAR control to its calibrated detent.

e. Release the CH 1 VERT MODE push button and press in the CH 2 VERT MODE push button.

f. Repeat parts b through c for the CH 2 VAR control.

g. Return the CH 2 VAR control to its calibrated detent.

5. Check CH 2 INVERT Trace Shift

a. Press the CH 2 INVERT push button.

b. CHECK—Trace shift is 2 divisions or less when switching between normal and INVERT.

c. Return the INVERT push button to normal (button out).

6. Check Vertical POSITION Range and Centering

a. Set:

CH 1 VOLTS/DIV	20 mV
CH 2 VOLTS/DIV	0.1 V
AC-GND-DC (both)	DC
A TRIGGER LEVEL	Fully clockwise

b. Connect the leveled sine-wave generator output to the CH 2 or Y input via a 50-Ω bnc cable and a 50-Ω bnc termination. Set the generator frequency to 50 kHz and adjust the output for a vertical display of 4.8 divisions.

c. Set CH 2 VOLTS/DIV to 20 mV.

d. CHECK—Top of display can be positioned down to the center horizontal graticule line, and bottom of display can be positioned up to the center horizontal graticule line.

e. Move the signal from the CH 2 OR Y input to the CH 1 OR X input connector.

f. Set VERT MODE switches for a CH 1 display.

g. CHECK—Repeat step 6, part d, for CH 1.

7. Check BEAM FIND Operation

a. Push in and hold the BEAM FIND push button.

b. CHECK—A compressed display is visible regardless of the setting of the following controls:

CH 1 POSITION

INTENSITY control

Horizontal POSITION control

c. Return both the Horizontal POSITION control and the INTENSITY controls to midrange.

d. Set CH 1 AC-GND-DC switch to GND.

e. While still holding in the BEAM FIND button, vertically position the trace to the center horizontal graticule line.

f. Release the BEAM FIND button.

g. CHECK—Trace remains within the graticule area.

h. Return the CH 1 AC-GND-DC switch to DC and disconnect the test equipment.

8. Check CH 1 and CH 2 DC Accuracy

a. Connect a 20 mV standard-amplitude signal to the CH 1 input connector via a 50-Ω bnc cable. Do not use a termination.

b. CHECK—CH 1 dc accuracy is within the limits given in Table 4-2.

c. Set:

VERT MODE	CH 2
CH 2 VOLTS/DIV	5 V

d. Move the signal from the CH 1 OR X input to the CH 2 OR Y input connector.

e. CHECK—CH 2 dc accuracy is within the limits given in Table 4-2. Reverse the order of checks (from bottom to top) for ease in making the checks.

Table 4-2

DC Accuracy Limits

VOLTS/DIV Switch Setting	Standard Amplitude Signal	Vertical Deflection (Divisions)	3% Tolerance (Divisions)
5 mV	20 mV	4	3.88 to 4.12
10 mV	50 mV	5	4.85 to 5.15
20 mV	0.1 V	5	4.85 to 5.15
50 mV	0.2 V	4	3.88 to 4.12
0.1 V	0.5 V	5	4.85 to 5.15
0.2 V	1.0 V	5	4.85 to 5.15
0.5 V	2.0 V	4	3.88 to 4.12
1.0 V	5.0 V	5	4.85 to 5.15
2.0 V	10.0 V	5	4.85 to 5.15
5.0 V	20.0 V	4	3.88 to 4.12

9. Check CH 1 and CH 2 Storage DC Accuracy

a. Set:

VOLTS/DIV (both)	5 mV
STORAGE MODE	NORM
CURSOR FUNCTION	VOLTS

b. Change the generator to 20 mV.

c. CHECK—CH 2 NORM Storage dc accuracy. The acquired waveform must be 4 divisions, within 3% (3.88 divisions to 4.12 divisions).

d. Move the signal from the CH 2 OR Y input to the CH 1 OR X input connector and set VERT MODE switches to display CH 1.

e. CHECK—Repeat step 9, part c, for CH 1.

10. Check VOLTS CURSOR Readout Accuracy

a. Set:

VOLTS/DIV (both)	0.5 mV
AC-GND-DC (both)	GND

b. Use VOLTS CURSOR controls to obtain an exact 6-vertical-division difference between the VOLTS cursors.

c. CHECK—VOLTS Readout accuracy is within the limits given in Table 4-3 for each VOLTS/DIV switch setting.

d. Rotate the CH 1 VOLTS/DIV VAR control out of the calibrated detent.

e. CHECK—Readout is 5.88 to 6.12 divisions.

f. Return the VAR control to its calibrated detent.

g. Set VERT MODE switches to display CH 2.

h. CHECK—VOLTS readout changes for each VOLTS/DIV switch setting.

i. CHECK—Repeat step 10, parts d, e, and f using the CH 2 VAR control.

Table 4-3

VOLTS Cursor Readout Accuracy

VOLTS/DIV Switch Setting	2% Readout Tolerance
0.5 mV	2.940 to 3.060 mV
1 mV	5.88 to 6.12 mV
2 mV	11.76 to 12.24 mV
5 mV	29.40 to 30.60 mV
10 mV	58.8 to 61.2 mV
20 mV	117.6 to 122.4 mV
50 mV	294.0 to 306.0 mV
0.1 V	0.588 to 0.612 V
0.2 V	1.176 to 1.224 V
0.5 V	2.940 to 3.060 V
1 V	5.88 to 6.12 V
2 V	11.76 to 12.24 V
5 V	29.40 to 30.60 V

11. Check CH 1 and CH 2 VAR VOLTS/DIV Range

a. Set:

VOLTS/DIV (both)	20 mV
NON STORE	On (button in)
AC-GND-DC	DC

b. Change the generator output to 0.1 V.

c. CHECK—Display reduces to less than 2 divisions when the CH 2 VAR control is rotated to its extreme counterclockwise rotation.

d. Move the signal to the CH 1 OR X input connector and set VERT MODE switches to display CH 1.

e. CHECK—Repeat step 11, part c, using the CH 1 VAR control.

f. Return both VAR controls to their calibrated detent positions and disconnect the signal from the CH 1 input connector.

12. Check ADD Mode

a. Set:

VOLTS/DIV (both)	5 mV
VERT MODE	ADD

b. Connect a 10-mV standard-amplitude signal to both the CH 1 and CH 2 input connectors via a 50-Ω bnc cable and a dual-input coupler.

c. CHECK—Displayed signal is approximately 4 divisions in amplitude.

d. Set:

STORAGE MODE	NORM

e. CHECK—Repeat step 12, part c, for the Stored Display.

f. Press in the NON STORE push button.

13. Check CH 1 and CH 2 Gain Balance

a. Press in CH 2 INVERT push button.

b. CHECK—Displayed vertical amplitude is approximately zero division.

c. Return the CH 2 INVERT push button to normal (button out) and disconnect the test equipment.

14. Check Vertical Low-Frequency Compensation

a. Set:

VERT MODE	CH 1
TIME/DIV (both)	0.2 ms
VOLTS/DIV (both)	5 mV

b. Connect a 1-kHz fast-rise + square-wave signal to the CH 1 input connector via a 50-Ω bnc cable, 10X bnc attenuator, and a 50-Ω bnc termination.

c. Adjust generator output to obtain a 5-division display. Adjust the A TRIGGER LEVEL control for a stable display.

d. CHECK—Rounding or overshoot is within 3% (±0.15 division) at the frequencies listed in Table 4-4.

e. Disconnect the fast-rise + signal from the CH 1 input connector.

Table 4-4

Low-Frequency Compensation Setup

Calibration Generator Frequency	TIME/DIV Switch Setting
1 kHz	0.2 ms
10 kHz	20 μs
100 kHz	2 μs

15. Check CH 1 and CH 2 VOLTS/DIV Compensation

a. Set:

TIME/DIV (both)	0.2 ms

b. Connect a 10X probe with scale-factor switching connector to the CH 1 input (note that the VOLTS/DIV scale-factor switching LED now indicates 50 mV).

c. Connect a 1-kHz high-amplitude square-wave signal through a 2X, 5X, or 10X bnc attenuator (depending on generator output amplitude) to a 50-Ω bnc termination that is connected to a bnc-to-probe-tip adapter. Insert the 10X probe tip into the probe-tip adapter.

d. Adjust the generator output and select attenuators as necessary to obtain a 5-division display.

e. Adjust probe compensation for the best flat-top waveform. Do not readjust the probe compensation during the remainder of this step.

f. CHECK—Rounding or overshoot on the waveform is within 3% (±0.15 division) at all settings of the VOLTS/DIV switch between 50 mV and 5 V. Add or remove attenuators and/or termination as required and adjust generator output amplitude as necessary to maintain a 5-division display at each VOLTS/DIV switch setting.

g. Move the test setup to CH 2 input connector and set the VERT MODE switches to display CH 2.

h. Repeat step 15, part f, for CH 2.

i. Disconnect the test setup.

16. Check CH 1 and CH 2 Transient Response

a. Set:

TIME/DIV (both)	0.05 μs
VOLTS/DIV (both)	5 mV
A TRIGGER SLOPE	+ (plus)

b. Connect a 100-kHz fast-rise + square-wave signal to the CH 2 input connector via a 50-Ω bnc cable, 10X attenuator, and a 50-Ω bnc termination. Set the generator output for a vertical display of 5 divisions at 100 kHz.

c. CHECK—Flat-top waveform is within 4% (5 divisions ± 0.2 division).

d. Move the test setup to the CH 1 input connector and set the VERT MODE switches to display CH 1.

e. CHECK—Repeat step 16, part c, for CH 1.

17. Check Storage Acquisition Step Response

a. Set:

TIME/DIV (both)	0.1 μs
STORAGE MODE	NORM
DISPLAY RESPONSE	PULSE
STORAGE WINDOW	POST TRIG

b. Adjust the A TRIGGER LEVEL control as necessary to obtain a triggered acquisition of the 5-division fast-rise + waveform.

c. Press in the ENVELOPE Storage Mode push button, then press in the SAVE Storage Mode push button.

d. Allow the ENVELOPE acquisition cycle to complete and enter the SAVE Storage Mode.

e. CHECK—Overshoot on leading edge of the waveform is 3% or less (0.15 division or less).

f. Disconnect the fast-rise + signal from the CH 1 input connector.

18. Check CH 1 and CH 2 Bandwidth

a. Set:

A TIME/DIV	0.2 ms
A TRIGGER LEVEL	Fully clockwise

b. Connect a 50-kHz leveled sine-wave signal to the CH 1 input connector via a 50-Ω bnc cable, 10X bnc attenuator, and 50-Ω bnc termination.

c. Set the generator output for a vertical display of 5 divisions, then change the generator output frequency to 100 MHz.

d. CHECK—Display amplitude is 3.5 divisions or greater.

e. Repeat step 18, parts c and d for all CH 1 VOLTS/DIV switch settings from 5 mV to 0.5 V. Adjust the generator output amplitude and either add or remove attenuators as necessary to maintain a 5-division, 50-kHz reference signal display.

f. Move the sine-wave generator output signal from the CH 1 input to the CH 2 input connector and set VERT MODE switches to display CH 2.

g. Repeat step 18, parts c and d, for all CH 2 VOLTS/DIV switch settings from 5 mV to 0.5 V. Adjust the generator output amplitude and add or remove attenuators as needed to maintain a 5-division, 50-kHz reference signal display.

NOTE

Attempting to check VOLTS/DIV settings beyond 0.5 V will exceed the power-handling capability of the 50-Ω terminations and output power of standard calibration equipment.

19. Check Useful Storage Bandwidth

a. Set:

VOLTS/DIV (both)	5 mV
STORAGE MODE	NORM
A TIME/DIV	10 μs
CURSOR FUNCTION	VOLTS

b. Remove any attenuators between the leveled sine-wave generator and the CH 2 input connector and reconnect the cable, with a 50-Ω bnc termination, to the CH 2 input connector.

c. Set the generator to obtain a 50-kHz, 6-division display. Adjust the A TRIGGER LEVEL control as necessary to obtain a triggered acquisition of the 50-kHz reference signal.

d. Change the A TIME/DIV switch to 0.2 μs and change the sine-wave generator output frequency to 10 MHz.

e. Press in the SAVE Storage Mode push button to hold a stable display for measurement.

f. CHECK—Any single-cycle p-p signal amplitude is not greater than 33.65 mV or less than 21.20 mV. Use the VOLTS cursors to make the measurements.

g. Set the VERT MODE switches for a CHOP display of CH 1 and CH 2 and change the sine-wave generator output frequency to 5 MHz.

h. Press in the NORM Storage Mode push button. Then, after a new display has been acquired, press in the SAVE Storage Mode push button.

i. CHECK—Any single cycle p-p signal amplitude is not greater than 31.80 mV or less than 25.25 mV. Again, use the VOLTS cursors to make the measurements.

20. Check Storage Analog Bandwidth

a. Set:

STORAGE MODE	ENVELOPE
A TIME/DIV	1 ms

b. Set the sine-wave generator output frequency to 50 kHz and verify that a 6-division vertical signal display is being acquired.

c. Change the sine-wave generator output frequency to 10 MHz.

NOTE

At exactly 10 MHz input signal frequency, it is possible for an alias display to be seen. If an ENVELOPE display with variable amplitude appears, shift the test frequency slightly off 10 MHz to obtain an envelope with flat amplitude.

d. Press in the SAVE Storage Mode push button. The 468 will enter the SAVE Storage Mode at the end of the ENVELOPE acquisition cycle.

e. CHECK—The ENVELOPE display signal amplitude is 30 mV p-p within ±3.65 mV (33.65 mV to 26.35 mV). Use the VOLTS cursors to make the measurement.

f. Disconnect the test setup.

21. Check Cascaded Gain and Bandwidth

a. Set:

VERT MODE	CH 2
A TIME/DIV	2 ms
NON STORE	On (button in)

b. Connect the CH 1 VERT SIGNAL OUT connector (on the 468 rear panel) to the CH 2 input connector via a 50-Ω cable and a 50-Ω bnc termination.

c. Connect a 5-mV standard-amplitude signal to the CH 1 input connector via a 50-Ω bnc cable.

d. CHECK—Display vertical amplitude is 5 divisions or greater.

e. Remove the standard-amplitude signal from the CH 1 input connector.

f. Connect a 50-MHz, leveled sine-wave signal to the CH 1 input connector via a 50-Ω bnc cable, a 10X bnc attenuator, and a 50-Ω bnc termination. Adjust the generator output to obtain a 5-division signal display.

g. Adjust the generator output frequency to 50 MHz.

h. CHECK—Displayed signal amplitude is now 3.5 divisions or greater.

i. Disconnect the test setup.

22. Check Trigger View Gain

a. Set:

VERT MODE	A TRIG VIEW
A TIME/DIV	0.2 ms
A TRIGGER COUPLING	DC
A TRIGGER SOURCE	EXT
A TRIGGER LEVEL	Midrange

b. Connect a 0.5-V standard-amplitude signal to the EXT A TRIGGER input connector via a 50-Ω bnc cable. Use no termination.

c. Use the A TRIGGER LEVEL control to vertically center the signal display.

d. CHECK—Display signal amplitude is 5 divisions ±5% (4.75 divisions to 5.25 divisions).

e. Set the A TRIGGER SOURCE to EXT/10 and change the output of the calibration generator to 5 V. Use

the A TRIGGER LEVEL control to vertically center the display.

f. CHECK—Display signal amplitude is 5 divisions ±5% (4.75 divisions to 5.25 divisions).

g. Disconnect the test signal from the EXT A TRIGGER input connector.

23. Check Trigger View Centering

a. Set:

A TRIGGER SOURCE	EXT

b. Connect a 1-kHz, sine-wave signal to the EXT A TRIGGER input connector via a 50-Ω bnc cable. Use no termination.

c. Set the generator to obtain a 5-division signal display.

d. CHECK—Sweep symmetrically triggers within ±1 graticule division of the center horizontal graticule line when the A TRIGGER SLOPE is switched between + (plus) and – (minus).

e. Disconnect the sine-wave generator from the EXT A TRIGGER input connector.

24. Check Trigger View Low-Frequency Compensation

a. Set:

A TIME/DIV	0.1 ms
A TRIGGER SLOPE	+ (plus)

b. Connect a 1-kHz, high-amplitude square-wave signal to the EXT A TRIGGER input connector via a 50-Ω bnc cable and a 50-Ω bnc termination. Set the generator output for a 5-division signal display.

c. Use the A TRIGGER LEVEL control to vertically center the display.

d. CHECK—Square-wave leading edge has less than 10% overshoot or rounding (±0.5 division).

e. Set the A TRIGGER SOURCE to EXT/10 and adjust the generator output for a signal display of 5 vertical divisions. Use the A TRIGGER LEVEL control to vertically center the displayed signal.

f. CHECK—Square-wave leading edge has less than 10% overshoot or rounding (±0.5 division).

g. Disconnect the generator output from the EXT A TRIGGER input connector.

25. Check Trigger View High-Frequency Compensation

a. Set:

A TRIGGER SOURCE	EXT
A TIME/DIV	0.2 μs

b. Connect a 100-kHz fast-rise + square-wave signal to the EXT A TRIGGER input connector via a 50-Ω bnc cable and a 50-Ω bnc termination.

c. Adjust the generator output amplitude for a signal display of 5 vertical divisions. Use the A TRIGGER LEVEL control to vertically center the display.

d. CHECK—Square-wave front-corner aberration is less than ±10% (±0.5 division).

e. Disconnect the test setup.

26. Check A and B Zero Trigger View Delay

a. Set:

VERT MODE	CH 1 and A TRIG VIEW
A TIME/DIV	0.02 μs
X10 MAG	On (button in)
A TRIGGER COUPLING	AC
CH 1 VOLTS/DIV	0.1 V

b. Connect a 40-MHz leveled sine-wave signal via a bnc T-connector, two 42-inch (equal length) 50-Ω bnc cables, and two 50-Ω bnc terminations; one leading to the CH 1 input connector, and the other to the EXT A TRIGGER input connector. Set the sine-wave generator output amplitude for a 6-vertical-division display of the A TRIG VIEW signal.

c. Adjust CH 1 VAR and VOLTS/DIV controls to match the amplitude of the CH 1 displayed signal to the amplitude of the A TRIG VIEW signal. Use the A TRIGGER LEVEL control to vertically center the A TRIG VIEW display and use the CH 1 Vertical POSITION control to vertically center the CH 1 display.

d. CHECK—Time difference between the CH 1 and A TRIG VIEW signals (with displays superimposed) is 0.2 horizontal graticule division or less.

e. Set:

HORIZ DISPLAY	B DLY'D
A TIME/DIV	0.2 μs
B TIME/DIV	0.02 μs

f. Repeat step 26, part c.

g. CHECK—Time difference between the CH 1 and A TRIG VIEW signals with displays superimposed is 0.2 horizontal graticule division or less.

h. Disconnect test setup.

27. Check AC-Coupled Lower −3 dB Point

a. Set:

A TIME/DIV	0.5 ms
VERT MODE	CH 1
CH 1 VOLTS/DIV	1 V
A TRIGGER SOURCE	CH 1
AC-GND-DC	AC

b. Connect a 1-kHz sine-wave signal from the function generator via a 50-Ω bnc cable and a 50-Ω bnc termination, to the CH 1 input connector.

c. Set the generator amplitude for a 5-vertical-division signal display.

d. Set the A TRIG MODE to NORM and adjust the A TRIGGER LEVEL control for a stable, triggered display.

e. Press in the NORM Storage Mode push button.

f. Use the Channel 1 Vertical POSITION control to vertically center the display.

g. Press in the VOLTS Cursor Function push button. Use the VOLTS cursors in conjunction with the generator amplitude control to obtain a 5-V p-p reference signal display.

h. Set the generator output frequency to 10 Hz. Do not change the generator output amplitude control.

i. Set the A TIME/DIV switch to 50 ms and adjust the A TRIGGER LEVEL control as necessary for a stable, triggered siplay.

j. Use the VOLTS cursors to measure the p-p amplitude of the display.

k. CHECK—Display p-p amplitude is 3.54 V or greater.

l. Disconnect the bnc cable and termination from the CH 1 input connector.

m. Connect a 10X probe (preferably one supplied with the instrument) to the CH 1 input connector. Use a bnc-to-probe-tip adapter at the output of the function generator and apply the generator sine-wave output to the CH 1 input connector via the 10X probe tip.

n. Press in the NON STORE push button and repeat step 27, parts c through g.

o. Set the generator output frequency to 1 Hz. Do not adjust the generator output amplitude.

p. Set the A TIME/DIV switch to 0.5 s and adjust the A TRIGGER LEVEL control as necessary for a stable, triggered display.

q. Use the VOLTS cursors to measure the p-p amplitude of the 1-Hz signal.

r. CHECK—Display amplitude is 3.54 V or greater.

s. Disconnect the test setup.

TRIGGERING

Equipment Required (see Table 4-1):

5. Calibration Generator
6. Leveled Sine-Wave Generator
11. 50-Ω Signal Pickoff Unit (Type CT-3)
12. 42-in, 50-Ω Bnc Cable (2 required)
14. GR-to-bnc-female Adapter
15. GR-to-bnc-male Adapter
19. Dual-Input Coupler (2 required)
21. 10X Bnc Attenuator
23. 2X Bnc Attenuator
24. 50-Ω Bnc Termination (2 required)

468 CONTROL SETTINGS

POWER	ON (button in)

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2)

VERT MODE	CH 1
POSITION	Midrange
VOLTS/DIV	5 mV
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC	DC
INVERT	Normal (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Triggers (A and B)

COUPLING	AC
LEVEL	Midrange
SLOPE	+
SOURCE	NORM
TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep (A and B)

HORIZ DISPLAY	A
TIME/DIV	5 μs
TIME/DIV VAR	Calibrated detent
DELAY TIME POSITION	Fully counterclockwise
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

NON STORE	On (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check A and B Internal Triggering

a. Connect the test equipment to the 468 as illustrated in Figure 4-1.

b. Adjust the leveled sine-wave generator for a 3-division, 50-kHz signal display and set both VOLTS/DIV switches to 50 mV (0.3-division vertical display) for AC and DC TRIGGER COUPLING.

c. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control in the following A TRIGGER COUPLING and A TRIGGER SOURCE switch positions:

TRIGGER COUPLING	TRIGGER SOURCE	Display Amplitude
AC	NORM	0.3 div
	CH 1	0.3 div
	CH 2	0.3 div
DC	NORM	0.3 div
	CH 1	0.3 div
	CH 2	0.3 div

d. Set CH 1 VOLTS/DIV switch to 5 mV and adjust the sine-wave generator output for a 5-division vertical signal display. Then, set the CH 1 VOLTS/DIV switch to 50 mV to obtain a 0.5-division vertical display.

e. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control in the following A TRIGGER COUPLING and A TRIGGER SOURCE switch positions:

TRIGGER COUPLING	TRIGGER SOURCE	Display Amplitude
LF REJ	NORM	0.5 div
	CH 1	0.5 div
	CH 2	0.5 div
HF REJ	NORM	0.5 div
	CH 1	0.5 div
	CH 2	0.5 div

f. Set:

HORIZ DISPLAY	B DLY'D
A TRIGGER LEVEL	Fully clockwise
CH 1 VOLTS/DIV	5 mV

g. CHECK—Repeat step 1, parts b through e, using the B TRIGGER COUPLING and B TRIGGER SOURCE switch positions and adjusting the B TRIGGER LEVEL control.

2. Check A and B External Triggering

a. Set:

CH 1 VOLTS/DIV	20 mV
TRIGGER SOURCE (both)	Ext
TRIGGER COUPLING (both)	AC

b. Adjust the leveled sine-wave generator output for a display amplitude of 5 vertical divisions.

c. CHECK—Stable display can be obtained by adjusting the B TRIGGER LEVEL control with B TRIGGER COUPLING in the following switch positions:

AC and DC

d. Remove the 2X bnc attenuator from the test setup.

e. CHECK—Stable display can be obtained by adjusting the B TRIGGER LEVEL control with B TRIGGER COUPLING in the following switch positions:

LF REJ and HF REJ

f. Set:

HORIZ DISPLAY

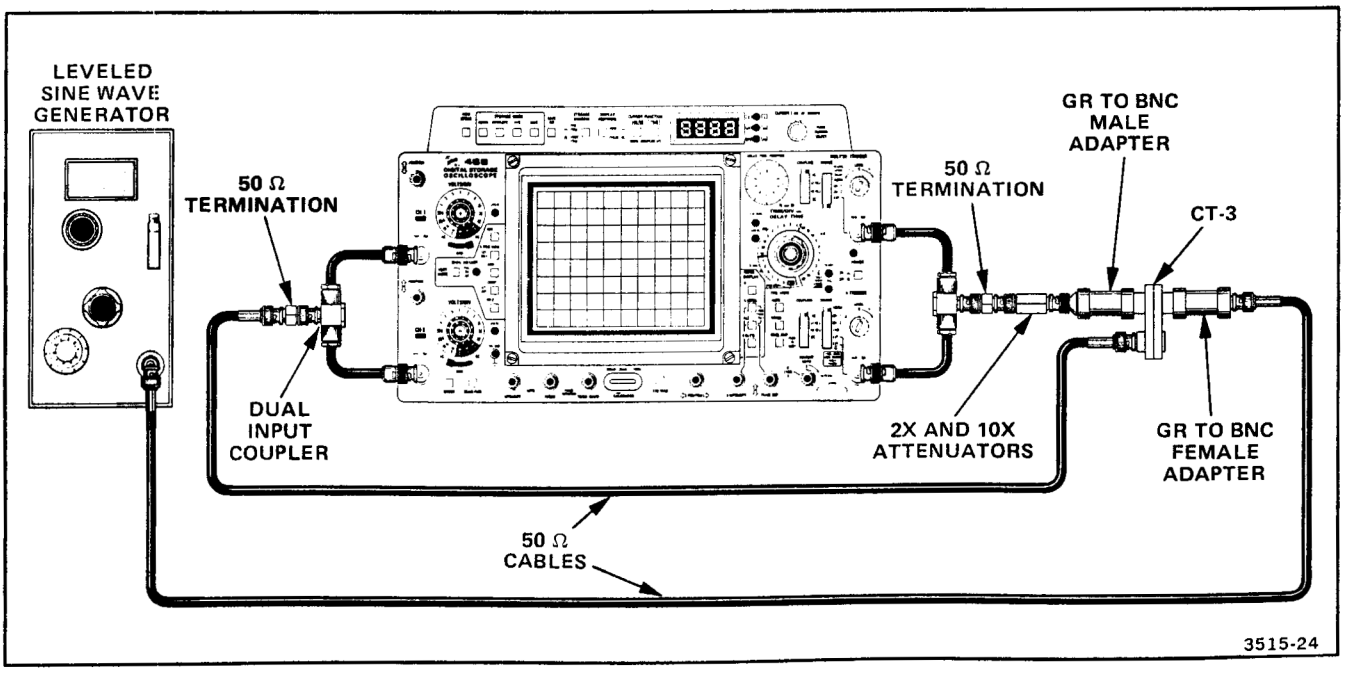


Figure 4-1. Test setup for A and B triggering checks.

g. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control with A TRIGGER COUPLING in the following switch positions:

LF REJ and HF REJ

h. Reinstall the 2X attenuator in series with the 10X attenuator.

i. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control with the A TRIGGER COUPLING in the following switch positions:

AC and DC

j. Remove the 10X attenuator from the test setup and set A TRIGGER SOURCE to EXT/10.

k. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control with the A TRIGGER COUPLING in the following switch positions:

AC and DC

l. Remove the 2X attenuator from the test setup.

m. CHECK—Stable display can be obtained by adjusting the A TRIGGER LEVEL control with the A TRIGGER COUPLING in the following switch positions:

LF REJ and HF REJ

3. Check NORM TRIG Mode

a. Set:

A TRIGGER COUPLING	A
A TRIGGER SOURCE	NORM

b. Adjust the A TRIGGER LEVEL control for a stable display.

c. Set TRIG MODE to NORM.

d. CHECK—Stable display is visible.

e. Set CH 1 AC-GND-DC switch to GND.

f. CHECK—No visible display in the absence of an adequate trigger signal.

g. Press in the NORM Storage Mode push button and return the CH 1 AC-GND-DC switch to AC.

h. Repeat step 3, parts b through e, for the Storage NORM trigger operation.

i. CHECK—TRIG LED is extinguished in the absence of an adequate trigger signal.

4. Check SINGL SWP Mode

a. Set:

NON STORE	On (button in)
CH 1 AC-GND-DC	DC

b. Adjust the A TRIGGER LEVEL control until display just triggers.

c. Set CH 1 AC-GND-DC switch to GND.

d. Press SINGL SWP push button (READY LED should illuminate and remain on).

e. Set CH 1 AC-GND-DC switch to DC.

f. CHECK—READY LED goes out and a single sweep occurs.

NOTE

The INTENSITY control may require adjustment to observe the single-sweep trace.

g. Press in SINGL SWP push button several times.

h. CHECK—Single sweep occurs every time SINGL SWP push button is pressed in.

i. Disconnect test setup.

HORIZONTAL

Equipment Required (see Table 4-1):

5. Calibration Generator
6. Leveled Sine-Wave Generator
7. Time-Mark Generator
12. 42-in, 50-Ω Bnc Cable
24. 50-Ω Bnc Termination

468 CONTROL SETTINGS

POWER	ON

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2)

VERT MODE	CH 1
POSITION	Midrange
VOLTS/DIV	0.5 V
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC	DC
INVERT	Normal (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Trigger (A and B)

COUPLING	AC
LEVEL	Midrange
SLOPE	+
SOURCE (both)	NORM
TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep (A and B)

HORIZ DISPLAY	A
TIME/DIV	1 ms
TIME/DIV VAR	Calibrated detent
DELAY TIME POSITION	Fully counterclockwise
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

NON STORE	On (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check A and B Timing Accuracy

a. Connect 1-ms time markers to the CH 1 input connector via a 50-Ω bnc cable and a 50-Ω bnc termination.

b. Use the CH 1 Vertical POSITION control to center the trace vertically and adjust the A TRIGGER LEVEL control for a stable, triggered display.

c. Switch the A TIME/DIV switch to 0.02 μs and select the 20-ns time markers. Use the Horizontal POSITION control to align the first time marker with the first vertical graticule line (extreme left edge of the graticule area).

d. CHECK—The A timing accuracy. Timing must be accurate within 2% (0.2 division at the 11th time marker).

e. Using the TIME/DIV switch and time-mark generator settings given in Table 4-5, check timing accuracy for the remaining A TIME/DIV switch settings. Readjust the A TRIGGER LEVEL control and Horizontal POSITION control as necessary.

NOTE

For the A TIME/DIV switch settings from 50 ms to 0.5 s per division, watch the time-marker tips only at the 1st and 11th graticule lines while adjusting the horizontal position and checking the timing accuracy.

f. Press in the X10 MAG push button.

g. CHECK—The A Magnified timing accuracy using the TIME/DIV switch and time-mark generator settings given in Table 4-5 under the X10 MAG column. Timing must be accurate within 3% (0.3 division at the 11th time marker).

Table 4-5

A and B Timing Accuracy

A and B TIME/DIV Switch Setting	Time-Mark Generator Output	
	NORM	X10 MAG
0.02 μs	20 ns	Not checked
0.05 μs	50 ns	5 ns
0.1 μs	0.1 μs	10 ns
0.2 μs	0.2 μs	20 ns
0.5 μs	0.5 μs	50 ns
1 μs	1 μs	0.1 μs
2 μs	2 μs	0.2 μs
5 μs	5 μs	0.5 μs
10 μs	10 μs	1 μs
20 μs	20 μs	2 μs
50 μs	50 μs	5 μs
0.1 ms	0.1 ms	10 μs
0.2 ms	0.2 ms	20 μs
0.5 ms	0.5 ms	50 μs
1 ms	1 ms	0.1 ms
2 ms	2 ms	0.2 ms
5 ms	5 ms	0.5 ms
10 ms[a]	10 ms	1 ms
20 ms[a]	20 ms	2 ms
50 ms[a]	50 ms	5 ms
A Sweep Only		
0.1 s[a]	0.1 s	10 ms
0.2 s[a]	0.2 s	20 ms
0.5 s[a]	0.5 s	50 ms

[a]For A TIME/DIV switch settings slower than 5 ms/division, set TRIG MODE to NORM.

h. Set:

HORIZ DISPLAY	B DLY'D
B TIME/DIV	0.02 μs
A TIME/DIV	0.05 μs
A TRIGGER LEVEL	Triggered A Sweep
B TRIGGER LEVEL	Stable display
X10 MAG	Off (button out)

i. Set the time-mark generator to 20 ns.

j. CHECK—Repeat the accuracy checks of step 1, parts c and d, for the B Sweep using the TIME/DIV switch and time-mark generator settings given in Table 4-5.

k. Press in the X10 MAG push button.

l. CHECK—Repeat step 1, part g, for the B Magnified timing-accuracy check.

2. Check Storage Timing Accuracy

a. Set:

HORIZ DISPLAY	A
STORAGE MODE	NORM
STORAGE WINDOW	POST TRIG (button out)
A TRIGGER MODE	AUTO
A TRIGGER LEVEL	Triggered display
A TIME/DIV	2 μs
CURSOR FUNCTION	TIME

b. Set the time-mark generator to obtain 2-μs time markers. Obtain a NORM Storage Mode time-marker display. For POST TRIG Storage Window, only 10 time markers will be displayed. Use the CH 1 Vertical POSITION control to center the display vertically.

NOTE

Amplitude variations occurring in the time markers as they are being acquired is due to the sample clock and time marker frequency difference. Sampling of the narrow time markers does not always occur either at peak amplitude of the markers or at the same amplitude point on the markers between sampling intervals.

c. Use the Horizontal POSITION control to align the 2nd time marker rising edge with the 2nd vertical graticule line.

NOTE

If display amplitude variation becomes a problem, pressing in the SAVE Storage Mode push button when an acquisition is completed will hold the waveform display stable for making the accuracy check. The SAVE Storage Mode display may also be positioned vertically, if required, to move any portion of the waveform to the graticule markings on the center horizontal graticule line.

d. Set the CH 1 AC-GND-DC switch to GND and adjust the INTENSITY control for a visible display of the trace and the TIME dots.

e. Use the CURSOR control knob to set the active TIME cursor to the second vertical graticule line. Press the CURSOR SELECT push button to activate the 2nd TIME cursor. Position the cursor to the 10th vertical graticule line (8-division spacing between TIME cursors).

f. CHECK—LED readout accuracy is within 2% (16.00 μs ± 0.32 μs).

g. Set the CH 1 AC-GND-DC switch to DC and adjust the INTENSITY control as necessary for viewing the time markers.

h. CHECK—Readout accuracy and A timing using the TIME/DIV settings, time-mark generator outputs, and LED readouts given in Table 4-6. Timing must be accurate within 2% (±0.16 division) over the center 8 divisions (between the 2nd and 10th time markers). Use the Horizontal POSITION control as necessary to maintain cursor alignment of the 2nd time marker on the graticule as the TIME/DIV switch setting is changed.

NOTE

To obtain a valid display on the first trigger accepted at a new TIME/DIV switch setting, change the time-mark generator output to the next required time markers before changing the 468 TIME/DIV switch setting. This procedure is especially useful for TIME/DIV switch settings from 0.1 s to 5 s per division. Watch for a display update (display flickers and TIME LED readout changes to the scale of the newly acquired waveform) prior to making the accuracy check at the new TIME/DIV switch setting. As TIME/DIV switch setting increases, the time required for the update to occur increases. At 5 s per division, it takes at least 50 s to acquire a complete waveform.

i. Set:

A TRIG MODE	AUTO
HORIZ DISPLAY	B DLY'D
TIME/DIV (both)	2 μs
B TRIGGER LEVEL	Triggered display

j. Set the time-mark generator for 2-μs markers.

k. CHECK—Repeat step 2, part h, to check the B timing.

Table 4-6

Storage Timing Accuracy

A and B TIME/DIV Switch Setting	Time-Mark Generator Output	LED Readout Accuracy Over Center 8 Divisions
2 μs	2 μs	15.68 μs to 16.32 μs
5 μs	5 μs	39.20 μs to 40.80 μs
10 μs	10 μs	78.40 μs to 81.60 μs
20 μs	20 μs	157.8 μs to 163.2 μs
50 μs	50 μs	392.0 μs to 408.0 μs
0.1 ms	0.1 ms	0.784 ms to 0.816 ms
0.2 ms	0.2 ms	1.568 ms to 1.632 ms
0.5 ms	0.5 ms	3.920 ms to 4.080 ms
1.0 ms	1.0 ms	7.84 ms to 8.16 ms
2.0 ms	2.0 ms	15.68 ms to 16.32 ms
5.0 ms	5.0 ms	39.20 ms to 40.80 ms
10.0 ms	10.0 ms	78.40 ms to 81.60 ms
20.0 ms	20.0 ms	156.8 ms to 163.2 ms
50.0 ms	50.0 ms	392.0 ms to 408.0 ms
0.1 s[a]	0.1 s	0.784 s to 0.816 s
0.2 s[a]	0.2 s	1.568 s to 1.632 s
0.5 s[a]	0.5 s	3.920 s to 4.080 s
1.0 s[a]	1.0 s	7.84 s to 8.16 s
2.0 s[a]	2.0 s	15.68 s to 16.32 s
5.0 s[a]	5.0 s	39.20 s to 40.80 s

[a]For TIME/DIV switch settings slower than 50 ms/division, set TRIG MODE to NORM.

3. Check Storage 0.02-μs to 2.0-μs Timing Accuracy

a. Set:

A TRIGGER MODE	AUTO
HORIZ DISPLAY	A
TIME/DIV (both)	0.02 μs
CH 1 AC-GND-DC	GND
DISPLAY RESPONSE	PULSE (button out)
B TRIGGER SOURCE	STARTS AFTER DELAY

b. Obtain a NORM Storage display of the baseline trace. Then press in the SAVE Storage Mode push button.

c. Adjust the INTENSITY control for a visible display of the trace and TIME cursor dots. Use the CH 1 Vertical POSITION control to center the trace vertically.

d. Use the CURSOR control knob to set the active time cursor on the 2nd vertical graticule line. Press in the CURSOR SELECT push button to activate the 2nd TIME cursor. Use the CURSOR control knob to adjust the 2nd TIME cursor to the 10th vertical graticule line (8 divisions between the dots).

e. CHECK—LED Readout accuracy using the TIME/DIV switch settings and LED readouts given in Table 4-7. Accuracy must be within 2%.

f. Set HORIZ DISPLAY to B DLY'D.

g. CHECK—Repeat step 3, parts b through e, to check the B-timing LED readout accuracy.

Table 4-7

0.02 μs to 2.0 μs Timing Accuracy

TIME/DIV Switch Setting	LED Readout Accuracy
0.02 μs	0.157 μs to 0.163 μs
0.05 μs	0.392 μs to 0.408 μs
0.1 μs	0.784 μs to 0.816 μs
0.2 μs	1.568 μs to 1.632 μs
0.5 μs	3.920 μs to 4.080 μs
1.0 μs	7.84 μs to 8.16 μs
2.0 μs	15.68 μs to 16.32 μs

4. Check A TIME/DIV VAR Range

a. Set:

HORIZ DISPLAY	A
TIME/DIV	2 ms
NON STORE	On (button in)
CH 1 AC-GND-DC	DC

b. Select the 5-ms time markers from the time-mark generator.

c. Adjust the INTENSITY control for best viewing level. Use Horizontal POSITION control to align the first time marker with the left edge of the graticule area.

d. CHECK—One time marker per division can be displayed by rotating the TIME/DIV VAR control.

e. Return the TIME/DIV VAR control to its calibrated detent.

5. Check Delay or Differential Time Linearity

a. Set:

A TIME/DIV	1 ms
B TIME/DIV	5 μs
HORIZ DISPLAY	B DLY'D
B TRIGGER SOURCE	STARTS AFTER DELAY
DELAY TIME POSITION	1.00

b. Select 1-ms time markers from the time-mark generator.

c. Rotate the DELAY TIME POSITION dial to set the rising edge of the time marker that appears nearest to the center of the trace on the center graticule line. Note the dial setting.

d. Rotate the DELAY TIME POSITION dial to 2.00 and then set the time marker that appears nearest to the center of the trace on the center graticule line. Note the dial setting.

e. CHECK—Difference in setting between part c and part d is 1.00 ±0.01 division (0.99 to 1.01 division difference), with ambient temperature within the range of +15°C to +35°C. If the ambient temperature is outside this range, but between −15°C and +55°C, the difference should not exceed 1.00 ±0.03 division (0.97 to 1.03 division difference).

6. Check Delay or Differential Time Accuracy

a. Set:

A TIME/DIV	0.2 μs
B TIME/DIV	0.02 μs

b. Select the 0.1-μs time markers from the time-mark generator.

c. Set the DELAY TIME POSITION dial to 1.00. Adjust the Horizontal POSITION control so that the top of one displayed time marker crosses the center vertical graticule line. (If the top of the time marker at the beginning of the sweep isn't visible, then use the second time marker.)

d. Without changing the Horizontal POSITION control setting, set the DELAY TIME POSITION dial to 9.00. Slightly readjust the DELAY TIME POSITION dial to align the top of the displayed time marker with the center vertical graticule line.

e. CHECK—The DELAY TIME POSITION dial setting is 9.00 ±0.08 (8.92 to 9.08).

f. CHECK—Repeat step 6, parts c through e, for each setting listed in Table 4-8.

Table 4-8

Delay or Differential Time Accuracy

A TIME/DIV Switch Setting	B TIME/DIV Switch Setting	Time-Mark Generator Output
0.2 μs	0.02 μs	0.1 μs
0.2 μs	0.05 μs	0.1 μs
0.5 μs	0.05 μs	0.5 μs
1 μs	0.1 μs	1 μs
2 μs	0.1 μs	1 μs
5 μs	0.5 μs	5 μs
10 μs	1 μs	10 μs
20 μs	1 μs	10 μs
50 μs	5 μs	50 μs
0.1 ms	10 μs	0.1 ms
0.2 ms	10 μs	0.1 ms
0.5 ms	50 μs	0.5 ms
1 ms	0.1 ms	1 ms
2 ms	0.1 ms	1 ms
5 ms	0.5 ms	5 ms
10 ms[a]	1 ms	10 ms
20 ms[a]	1 ms	10 ms
50 ms[a]	5 ms	50 ms
0.1 s[a]	10 ms	0.1 s
0.2 s[a]	10 ms	0.1 s
0.5 s[a]	50 ms	0.5 s

[a]**For sweep times greater than 5 ms/division set TRIG MODE to NORM.**

7. Check Delay or Differential Jitter

a. Set:

DELAY TIME POSITION Dial	9.00
A TIME/DIV	1 ms
B TIME/DIV	0.2 μs

b. Select the 1-ms time markers from the time-mark generator.

c. Verify that the A TRIGGER SLOPE is set to + (plus). Slightly readjust the DELAY TIME POSITION dial to position a time marker within the graticule area.

d. CHECK—Jitter on the leading edge of the time marker does not exceed 1 division (2.5 divisions if operating from a 50 Hz or less ac power source). Disregard slow drift.

e. Set the DELAY TIME POSITION dial to 1.00.

f. CHECK—Repeat step 7, parts c and d.

g. Disconnect the time-mark generator from the 468.

8. Check ALT HORIZ DISPLAY Trace Separation

a. Set:

A TRIG MODE	AUTO
HORIZ DISPLAY	A INTEN
A TIME/DIV	1 ms
B TIME/DIV	0.1 ms
B INTENSITY	As required for visible display

b. Use the CH 1 Vertical POSITION control to align the trace with the center horizontal graticule line.

c. Select ALT HORIZ DISPLAY.

d. CHECK—TRACE SEP control will move the B trace at least ±4 vertical divisions from the center graticule line, with the A trace centered.

9. Check A INTEN and B ENDS A Operation

a. Set:

DELAY TIME	
POSITION Dial	5.00
HORIZ DISPLAY	A INTEN

b. CHECK—B portion of trace is intensified (approximately 1 division).

c. Rotate the A TRIGGER HOLDOFF control clockwise to the B ENDS A position (detent position).

d. CHECK—Trace ends at the end of the intensified portion.

e. Rotate the A TRIGGER HOLDOFF control counterclockwise to the NORM position.

10. Check X Gain

a. Set:

TIME/DIV (both)	X-Y
VOLTS/DIV (both)	5 mV
CH 1 AC-GND-DC	AC
CH 2 AC-GND-DC	GND
HORIZ DISPLAY	A

NOTE

For instruments with firmware version 1.0 installed, both the CH 1 and CH 2 VERT MODE buttons must be pushed in to illuminate the scale-factor probe-coding LED. It is not necessary to select any VERT MODE push buttons to obtain the X-Y function display.

b. Connect a 20-mV standard-amplitude signal from the calibration generator to the CH 1 input via a 50-Ω bnc cable.

c. CHECK—Display shows a difference of 4 divisions ±0.16 division between the two dots (3.84 to 4.16 divisions).

d. Disconnect the test setup from the 468.

11. Check X Bandwidth

a. Connect a 50-kHz leveled sine-wave signal to the CH 1 input via a 50-Ω bnc cable and a 50-Ω termination.

b. Set the generator to obtain a 10-division horizontal display.

c. Without changing the generator amplitude, adjust generator output frequency to 4 MHz.

d. CHECK—Display is at least 7 divisions in length.

e. Disconnect the test equipment from the 468.

GATE OUTPUTS, EXTERNAL Z-AXIS, AND CALIBRATOR

Equipment Required (see Table 4-1):

4. 10X Probe (supplied with 468)
5. Calibration Generator
12. 42-in, 50-Ω Bnc Cable (2 required)
24. 50-Ω Bnc Termination

468 CONTROL SETTINGS

POWER	ON

Crt

INTENSITY	Midrange
FOCUS	Best defined display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2)

VERT MODE	CH 1
POSITION	Midrange
VOLTS/DIV	2 V
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC	DC
INVERT	Normal (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Trigger (A and B)

COUPLING	AC
LEVEL	Fully clockwise
SLOPE	+ (plus)
A TRIGGER SOURCE	NORM
B TRIGGER SOURCE	STARTS AFTER DELAY
TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep (A and B)

TIME/DIV (both)	10 μs
TIME/DIV VAR	Calibrated detent
DELAY TIME POSITION	Fully counterclockwise
HORIZ DISPLAY	A INTEN
X10 MAG	Normal (button out)
POSITION (Horizontal)	Midrange

Digital Storage

NON STORE	On (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check A and B + GATE Outputs

a. Connect the A + GATE output (connector on the 468 rear panel) to the CH 1 input of the test oscilloscope via a 42-inch, 50-Ω bnc cable.

b. CHECK—For a positive pulse display (amplitude of 5.5 V, starting within approximately 500 mV of 0 V).

c. Move the bnc cable from the A + GATE connector to the B + GATE connector.

d. CHECK—Repeat part b for the B + GATE signal.

e. Disconnect the test setup from the 468.

2. Check EXT Z-AXIS Operation

a. Set:

HORIZ DISPLAY	A
TIME/DIV	0.5 ms

b. Connect a 5-V, standard-amplitude square-wave signal to the EXT Z-AXIS connector (located on the 468 rear panel) via a 50-Ω bnc cable.

c. CHECK—For noticeable intensity modulation of the trace when the INTENSITY control is set for normal viewing brightness. Adjust the TIME/DIV VAR control,

if necessary, to observe the modulation. Return the VAR control to the calibrated detent.

d. Disconnect the test setup from the 468.

3. Check CALIBRATOR Operation

a. Set:

CH 1 VOLTS/DIV	10 mV
TIME/DIV	1 ms

b. Connect the CALIBRATOR current-loop signal to the CH 1 input via a 10X scale-factor switching probe (preferably one supplied with the oscilloscope).

c. CHECK—For a 3-division vertical display of the CALIBRATOR square-wave signal (square-wave period is typically 1 ms, within 20%).

d. Disconnect all test equipment.

ADJUSTMENT PROCEDURE

IMPORTANT—PLEASE READ BEFORE USING THIS PROCEDURE

PURPOSE

The Adjustment Procedure is used to return the instrument to conformation with its Performance Requirements as listed in the "Specification" (Section 1).

LIMITS AND TOLERANCES

The limits and tolerances listed in this Adjustment Procedure are instrument specifications only if they are listed in the "Performance Requirements" column of the "Specification" (Section 1). Tolerances given are for the instrument undergoing calibration and do not include test equipment error. Calibration (adjustment) of the instrument must be accomplished at an ambient temperature between +20°C and +30°C, and the instrument must have had a warmup period of at least 20 minutes.

TEST EQUIPMENT REQUIRED

Table 4-1 at the beginning of this section describes the test equipment required to accomplish the entire Adjustment Procedure. The Adjustment Procedure is based on using the first item of equipment listed in the "Examples of Suitable Test Equipment" column of Table 4-1. When other equipment is substituted, the control settings or calibration setups might need to be altered. If the exact equipment listed is not available, check the "Minimum Specification" column carefully to see if any other equipment might suffice. Then check the "Purpose" column to see where this equipment is used. If it is used for a check or adjustment that is of little or no importance to your requirement(s), the item and corresponding step(s) may be omitted.

At the beginning of each subsection there is also a list showing only the test equipment necessary for performing the steps in that subsection. In this list, the number that precedes each piece of equipment corresponds to the item number listed in Table 4-1.

ADJUSTMENT SEQUENCE

The Adjustment Procedure is written such that complete calibration of the conventional oscilloscope portion of the 468 is accomplished prior to performing Digital Storage Circuit adjustments. This ensures that the level of the signals applied to the Digital Storage circuitry for processing is correct and that the Vertical Output and Horizontal Output Amplifiers are correctly adjusted, since they affect Digital Storage calibration.

PARTIAL PROCEDURES

This procedure is structured in subsections to permit adjustment of individual sections of the instrument (except the Power Supply) whenever a complete recalibration is not required. For example, if only the Vertical section fails to meet Performance Requirements (or has had repairs made and components replaced), it can be readjusted with little or no effect on other sections of the instrument. However, if the Power Supply section has undergone repairs or adjustments that change the absolute value of any of the supply voltages, a complete recalibration of the instrument will usually be required. In this case the entire Adjustment Procedure must be accomplished.

At the beginning of each subsection is a list of all the front-panel control settings required to prepare the instrument for performing Step 1 in that subsection. Each succeeding step within a subsection should then be performed both in sequence and in its entirety to ensure that control-setting changes will be correct for ensuing steps.

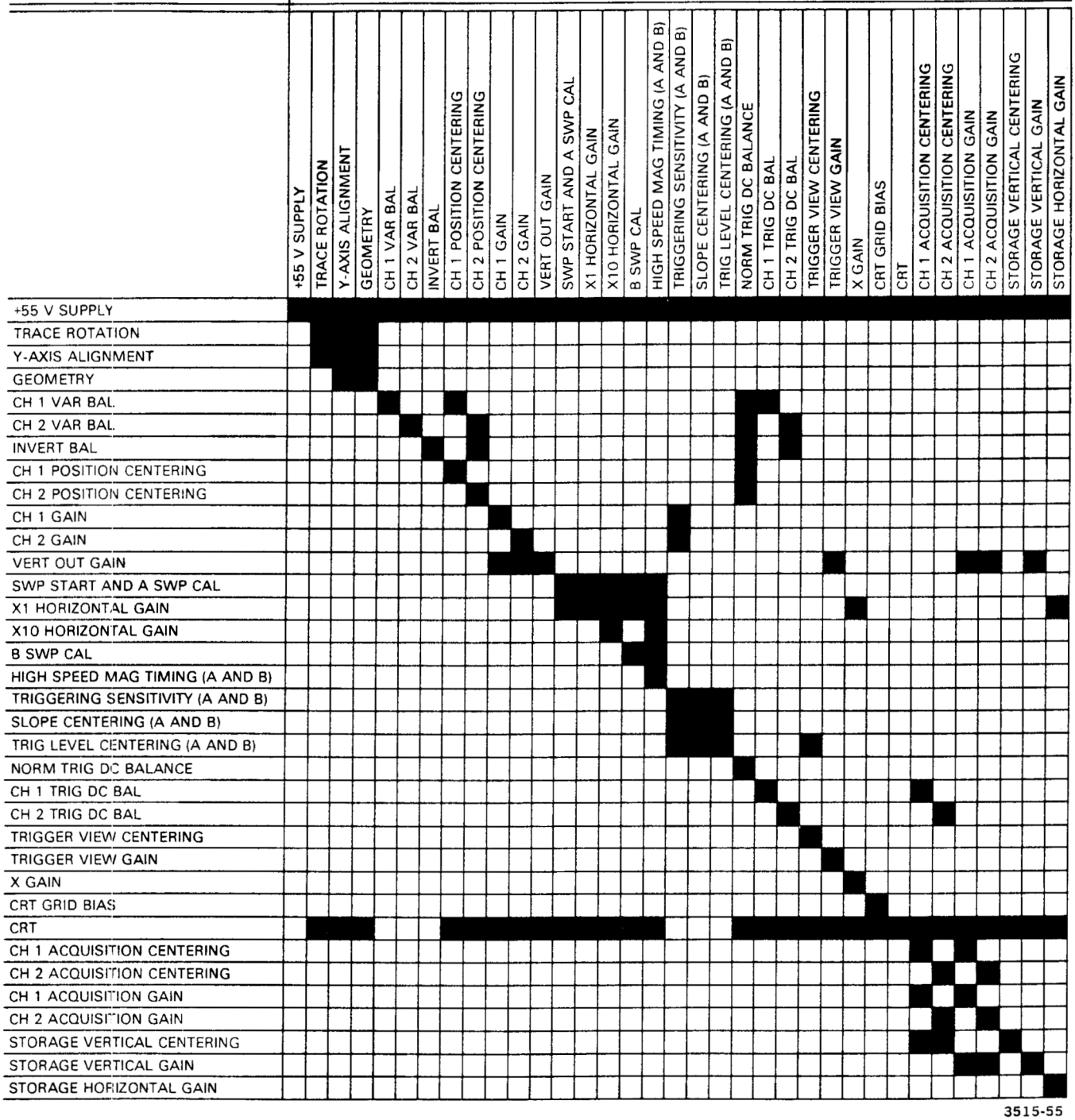
INTERNAL ADJUSTMENTS AND ADJUSTMENT INTERACTION

Do not preset any internal controls or change the +55-V power supply adjustment, since this will typically necessitate a complete recalibration of the instrument when only a partial recalibration might otherwise be required. To avoid unnecessary recalibration, change an internal control setting only when a Performance Characteristic is not met with the original setting. When it is necessary to change the setting of any internal control, always check Table 4-9 for any possible interacting adjustments that might require recalibration.

The use of Table 4-9 is particularly important if only a partial procedure is performed or if a circuit requires

Table 4-9
Adjustment Interactions

Adjustments Made	Interacting Adjustments
	+55 V SUPPLY
+55 V SUPPLY	
TRACE ROTATION	
Y-AXIS ALIGNMENT	
GEOMETRY	
CH 1 VAR BAL	
CH 2 VAR BAL	
INVERT BAL	
CH 1 POSITION CENTERING	
CH 2 POSITION CENTERING	
CH 1 GAIN	
CH 2 GAIN	
VERT OUT GAIN	
SWP START AND A SWP CAL	
X1 HORIZONTAL GAIN	
X10 HORIZONTAL GAIN	
B SWP CAL	
HIGH SPEED MAG TIMING (A AND B)	
TRIGGERING SENSITIVITY (A AND B)	
SLOPE CENTERING (A AND B)	
TRIG LEVEL CENTERING (A AND B)	
NORM TRIG DC BALANCE	
CH 1 TRIG DC BAL	
CH 2 TRIG DC BAL	
TRIGGER VIEW CENTERING	
TRIGGER VIEW GAIN	
X GAIN	
CRT GRID BIAS	
CRT	
CH 1 ACQUISITION CENTERING	
CH 2 ACQUISITION CENTERING	
CH 1 ACQUISITION GAIN	
CH 2 ACQUISITION GAIN	
STORAGE VERTICAL CENTERING	
STORAGE VERTICAL GAIN	
STORAGE HORIZONTAL GAIN	



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recalibration due to a component replacement. To use this table, first find, in the leftmost column, the adjustment that was made. Then move to the right, across that row, until you come to a darkened square. From the darkened square, move up the column and check the accuracy of the adjustment found at the heading of that column. Readjust if necessary.

Certain interactions are called out in the Adjustment steps to indicate that the adjustments affected must be repeated until no further improvement is noted.

DISPLAY

The most accurate display adjustments are made with a stable, well-focused, low-intensity display. Unless otherwise noted, adjust the INTENSITY, ASTIG, FOCUS, and TRIGGER LEVEL controls as needed.

STEP TITLES

Where possible, instrument performance is checked before an adjustment is made. Steps containing checks and adjustments are titled "Check/Adjust." Those steps with checks only are titled "Check."

SPECIAL CALIBRATION FIXTURES

Special calibration fixtures are used only where they facilitate instrument adjustment. These fixtures are available from Tektronix Inc. Order by part number through your local Tektronix Field Office or representative.

PREPARATION FOR ADJUSTMENT

It is necessary to remove the equipment cabinet to perform the Adjustment Procedure. See the "Cabinet Removal" instructions located in the Maintenance section of this Volume. Connect the test equipment to be used to an appropriate power source. Connect the 468 to an autotransformer set for 115 V ac. Apply power and allow a 20-minute warmup period before commencing the Adjustment Procedure. This procedure is written for the instrument to be operated from a 115-V power source. Operating from other power-source voltages will require setting the Line Voltage Selector and Regulating Range Selector to the appropriate settings for the available power source.

INDEX TO ADJUSTMENT PROCEDURE

Triggering Page

Horizontal

Gates, Calibrator, and Ext Z-Axis Page

Storage Power Supply

Storage Vertical

Storage Triggering

Storage Horizontal

MAIN POWER SUPPLY

Equipment Required (see Table 4-1)

1. Autotransformer
2. Digital Voltmeter
3. DC Voltmeter
4. Test Oscilloscope
25. 3-in. Flat-Bit Screwdriver

See ADJUSTMENT LOCATIONS 1 *in this Volume for test point and adjustment locations.*

NOTE

Prior to applying power to the 468, make the initial control settings. Connect the 468 to an appropriate power source through a variable autotransformer. Set the autotransformer to 115 V, apply power to the instrument and test equipment, and allow a 20-minute warmup period before commencing the adjustments and checks.

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER	See preceding NOTE

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2)

VERT MODE	CH 1
POSITION	Midrange
VOLTS/DIV	5 mV
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC	GND
INVERT	Normal (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Trigger (A and B)

COUPLING	AC
SLOPE	+
LEVEL	As needed for a stable display
SOURCE	NORM
TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep (A and B if applicable)

HORIZ DISPLAY	A
TIME/DIV	1 ms
TIME/DIV VAR	Calibrated detent
DELAY TIME POSITION	Fully counterclockwise
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

NON STORE	On (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check/Adjust Power Supply DC Levels, Regulation, and Ripple (R614)

NOTE

Review the information at the beginning of the Adjustment Procedure before starting this step.

a. Connect the digital voltmeter low lead to chassis ground and connect the volts lead to the first test point listed in Table 4-10.

b. CHECK—Voltage level is within the range given in Table 4-10.

c. Repeat parts a and b for each test point in Table 4-10.

d. If voltages are within tolerance, skip to part g. If not, continue with part e.

NOTE

Adjustment of the +55-V power supply will make it necessary to perform a complete recalibration of the instrument. Do not adjust the +55-V level if it is within tolerance unless a complete Adjustment Procedure is being performed.

e. Connect the digital voltmeter low lead to chassis ground and connect the volts lead to TP637.

f. ADJUST—+55-V supply (R614) for +55 V. Recheck all power supply dc levels according to Table 4-10.

g. Connect the test oscilloscope to the first test point indicated in Table 4-11.

h. CHECK—Ripple amplitude of the dc supply while varying the source voltage between 108 V and 132 V. To obtain the necessary vertical resolution for measuring ripple amplitude, use a 1X probe and cascaded gain on the test oscilloscope. Ripple amplitude should be within the typical value given in Table 4-11.

i. Repeat parts g and h for each test point in Table 4-11.

j. Return the source voltage to 115 V.

Table 4-10

Main Power Supply Limits

Power Supply	Test Point (+ Lead)	Reading	Tolerance
+55 V	TP637	+54.62 to +55.39	±0.7%
+15 V	TP639	+14.75 to +15.26	±1.7%
+5 V	PT638	+4.92 to +5.09	±1.7%
−8 V	TP740	−7.86 to −8.14	±1.7%
+110 V	TP642	+106.7 to +113.3	±3.0%

Table 4-11

Typical Main Power Supply Ripple

Power Supply	Test Point	Typical p-p Ripple
+55 V	TP637	4 mV
+15 V	TP639	2 mV
+5 V	TP638	2 mV
−8 V	TP740	2 mV
+110 V	TP642	20 mV

2. Check High Voltage Supply

a. Connect the low lead of a dc voltmeter capable of measuring at least 3000 V dc to chassis ground and the volts lead to TP328 on the Interface board. (TP328 is accessible through a hole in the high-voltage power-supply shield.)

NOTE

The digital voltmeter with HV probe may be used in lieu of the dc voltmeter to perform this check.

b. CHECK—High Voltage Supply dc level is −2450 V ±54 V (−2396 V to −2504 V).

c. Disconnect the dc voltmeter.

DISPLAY AND Z-AXIS

Equipment Required (see Table 4-1)

3. DC Voltmeter
4. Test Oscilloscope
4. 10X Probe
7. Time-Mark Generator
12. 50-Ω Bnc Cable
24. 50-Ω Bnc Termination
25. 3-in., Flat-Bit Screwdriver
26. Low-Capacitance Alignment Tool

See ADJUSTMENT LOCATIONS *in this Volume for test point and adjustment locations.*

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER Switch	ON (button in)

Crt

INTENSITY	Fully counterclockwise
FOCUS	Best focused display
SCALE ILLUMINATION	Fully counterclockwise

Vertical (CH 1 and CH 2)

VERT MODE	CH 1
VOLTS/DIV	5 mV
VOLTS/DIV VAR	Calibrated detent
POSITION	Midrange
AC-GND-DC	GND
INVERT	Normal (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Triggering (A and B if applicable)

TRIG MODE	AUTO
SOURCE	NORM
COUPLING	AC
SLOPE	+
LEVEL	As needed for a stable display
A TRIGGER HOLDOFF	NORM

Sweep (A and B if applicable)

HORIZ DISPLAY	A
A TIME/DIV	X-Y
TIME/DIV VAR	Calibrated detent
DELAY TIME POSITION	Fully counterclockwise
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

NON STORE	On (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check/Adjust CRT Grid Bias (R409)

a. Connect the digital voltmeter low lead to chassis ground and the volts lead to TP418 on the Interface circuit board. (TP418 is accessible through a hole in the high-voltage power-supply shield.

b. Set the INTENSITY control for a digital voltmeter reading of +20 V.

c. CHECK–Display for a well-defined, low-intensity dot. Use FOCUS and ASTIG controls as needed.

d. ADJUST–CRT Grid Bias (R409) for a visible dot, then back off the control until the dot is just visible.

e. Disconnect the voltmeter from the 468.

2. Check/Adjust Trace Alignment (TRACE ROTATION)

a. Set:

A TIME/DIV	0.5 ms
INTENSITY	As desired
SCALE ILLUM	As desired

b. Position the trace to the center horizontal graticule line.

c. CHECK—Trace is parallel with the center horizontal graticule line.

d. ADJUST—TRACE ROTATION control (front-panel screwdriver adjustment) to align the trace parallel with the center horizontal graticule line.

3. Check/Adjust Y-Axis Alignment (R270)

a. Set:

CH 1 AC-GND-DC	DC
CH 1 VOLTS/DIV	0.1 V
CH 1 POSITION	Fully counterclockwise

b. Connect 0.2-ms time markers from the time-mark generator to the CH 1 input via a 50-Ω bnc cable and 50-Ω bnc termination. (Time markers should fill the graticule area vertically. If not, reduce the VOLTS/DIV switch setting until they do.)

c. CHECK—Display for 0.1 division of tilt or less, when compared to the center vertical graticule line.

d. ADJUST—Y-Axis Alignment (R270) to align a time marker parallel with the center vertical graticule line.

e. CHECK—TRACE ROTATION adjustment. Repeat steps 2 and 3 for best display alignment.

4. Check/Adjust Geometry (R267)

a. CHECK—Display for 0.1 division or less of bowing of the time markers across the graticule area from top to bottom.

b. ADJUST—Geometry (R267) for minimum bowing of the time markers across the graticule area (especially at the left and right graticule edges).

c. CHECK—Y-Axis Alignment adjustment (step 3, part c).

d. Disconnect the test setup and vertically center the trace.

5. Check/Adjust Z-Axis Compensation (C518)

a. Set:

A TIME/DIV	0.05 μs
A TRIGGER LEVEL	Fully clockwise

b. Set test oscilloscope controls as follows:

VOLTS/DIV	5 V (with 10X probe)
TIME/DIV	0.1 μs
AC-GND-DC	DC
Trigger controls	As required for a stable display

c. Connect the 10X probe from the test oscilloscope to TP418 (accessible through hole in high-voltage shield, Z-Axis TP).

d. Adjust the 468 INTENSITY control for a 15-V (3-division) unblanking-gate-signal display on the test oscilloscope.

e. ADJUST—Z-Axis Compensation (C518), using a low-capacitance alignment tool, for the best square corner on the unblanking pulse displayed on the test oscilloscope.

f. Disconnect the test setup.

g. CHECK—Display for uniform trace intensity in the first two divisions of the trace.

h. READJUST—Z-Axis Compensation (C518), if necessary, for a trace of uniform intensity. (Compromise best square corner for uniform intensity.)

VERTICAL

Equipment Required (see Table 4-1)

4. Test Oscilloscope (only if gain requires complete recalibration)
4. Two 10X Probes (one should have scale-factor switching, however an 11-kΩ resistor may be substituted in step 1, part a)
5. Calibration Generator
   a. Standard Amplitude Calibrator
   b. Square-Wave Generator
6. Leveled Sine-Wave Generator
8. Low-Frequency Sine-Wave Generator
12. 50-Ω Bnc Cable (2 required)
17. Bnc-female-to-coaxial-cable-connector Adapter
18. Bnc-to-probe-tip Adapter
19. Dual-Input Coupler
21. 10X Bnc Attenuator (2 required)
23. 2X or 5X Bnc Attenuator
24. 50-Ω Bnc Termination (2 required)
25. 3-in., Flat-Bit Screwdriver
26. Low-Capacitance Alignment Tool

See ADJUSTMENT LOCATIONS 2 *and* ADJUSTMENT LOCATIONS 3 *in this Volume for test point and adjustment locations.*

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER Switch	ON (button in)

Vertical (CH 1 and CH 2)

VERT MODE	CH 1
VOLTS/DIV	5 mV
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC	DC
POSITION	Midrange
INVERT	Normal (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Triggering (A and B if applicable)

A TRIGGER SOURCE	NORM
B TRIGGER SOURCE	STARTS AFTER DELAY
TRIG MODE	AUTO
COUPLING	AC
SLOPE	+
LEVEL	For a stable display
A TRIGGER HOLDOFF	NORM

Sweep (A and B)

HORIZ DISPLAY	A
TIME/DIV (both)	1 ms
TIME/DIV VAR	Calibrated detent
DELAY TIME POSITION	Fully counterclockwise
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

NON STORE	ON (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check Probe Coding Indicator LED

a. Connect a 10X probe with a scale-factor switching connector to the CH 1 input (if no scale-factor switching probe is available, an 11-kΩ resistor may be used. Connect the resistor between ground and the metal coding ring on the input connector).

b. CHECK— 5 mV LED is extinguished and 50 mV LED is illuminated.

c. Set VERT MODE switches to display CH 2 and move the probe to the CH 2 input connector.

d. CHECK— 5 mV LED is extinguished and 50 mV LED is illuminated.

e. Remove 10X probe from the 468.

2. Check Input Coupling (AC-GND-DC) Switches

a. Connect a 20-mV, standard-amplitude square-wave signal to the CH 2 input via a 50-Ω cable.

b. Position the bottom of the display to the center horizontal graticule line and set CH 2 AC-GND-DC switch to GND.

c. CHECK—Trace is at center horizontal graticule line with no vertical deflection.

d. Set CH 2 AC-GND-DC switch to AC.

e. CHECK—Display is centered about the center horizontal graticule line.

f. Set VERT MODE switches to display CH 1 and move test signal to CH 1 input connector.

g. Position bottom of the display to the center horizontal graticule line.

h. Set CH 1 AC-GND-DC switch to GND.

i. CHECK—Trace is at center horizontal graticule line with no vertical deflection.

j. Set CH 1 AC-GND-DC switch to AC.

k. CHECK—Display is centered about the center horizontal graticule line.

l. Disconnect test equipment from the 468.

3. Check ALT Mode

a. Set:

VERT MODE	CH 1 (in), CH 2 (in), and ALT (button out)
A TRIGGER LEVEL	Fully clockwise

b. Position CH 1 and CH 2 traces about 2 divisions apart.

c. CHECK—Sweeps alternate for all A TIME/DIV settings except STOR ONLY and X-Y.

4. Check CHOP Mode

a. Set:

A TIME/DIV	0.5 μs
VERT MODE	CH 1, CH 2, and CHOP (all buttons in)
AC-GND-DC (both)	GND
A TRIGGER COUPLING	HF REJ

b. Position the CH 1 and CH 2 traces about 4 divisions apart and adjust the A TRIGGER LEVEL control for a stable display.

c. CHECK—Vertical switching transients are completely blanked between horizontal chopped segments for normal viewing intensity.

d. CHECK—Duration of each cycle is approximately 4 divisions.

5. Check BEAM FIND

a. Push in BEAM FIND push button and hold.

b. CHECK—Display remains entirely within the graticule area regardless of setting of Vertical or Horizontal POSITION controls.

c. CHECK—Trace intensity remains constant and visible regardless of setting of INTENSITY control.

d. Set VERT MODE to CH 1 and center the CH 1 trace both vertically and horizontally while holding the BEAM FIND button in.

e. Release BEAM FIND button.

f. CHECK—Trace remains within the graticule area.

6. Check/Adjust CH 1 VOLTS/DIV VAR Balance (R273) and CH 1 UNCAL LED

a. Position trace to the center horizontal graticule line.

b. Rotate CH 1 VOLTS/DIV VAR control counterclockwise out of calibrated detent.

c. CHECK—CH 1 UNCAL LED is illuminated.

d. CHECK—Trace shift of 1 division or less when rotating VAR control from fully counterclockwise to fully clockwise.

e. ADJUST—CH 1 Var Bal (R273) for minimum trace shift while rotating the CH 1 VAR control from one extreme to the other.

f. Return CH 1 VAR control to the detent position (fully clockwise).

7. Check/Adjust CH 1 Position Centering (R238)

a. Set:

CH 1 VOLTS/DIV	0.2 V
CH 1 AC-GND-DC	AC
A TIME/DIV	1 ms
A TRIGGER LEVEL	Fully clockwise

b. Connect a 50-kHz, leveled sine-wave signal to the CH 1 input via a 50-Ω bnc cable and a 50-Ω termination. Set the generator for a 2.4-division signal display.

c. Set CH 1 VOLTS/DIV switch to 20 mV.

d. CHECK—Top of display positions down to (or below) the center horizontal graticule line, and bottom of display positions up to center (or above) horizontal graticule line.

e. ADJUST—CH 1 Position Center (R238) so that display positions the same distance above and below the center horizontal graticule line.

f. Disconnect the test signal from the 468.

8. Check/Adjust CH 2 VOLTS/DIV VAR Balance (R573) and CH 2 UNCAL LED

a. Set:

VERT MODE	CH 2

b. Position trace to the center horizontal graticule line.

c. Rotate CH 2 VOLTS/DIV VAR control out of calibrated detent.

d. CHECK—CH 2 UNCAL LED is illuminated.

e. CHECK—Trace shift of 1 division or less when rotating VAR control from fully counterclockwise to fully clockwise.

f. ADJUST—CH 2 Var Bal (R573) for minimum trace shift while rotating the CH 2 VAR control from one extreme to the other.

g. Return CH 2 VAR control to the detent position (fully clockwise).

9. Check/Adjust CH 2 INVERT Balance (R566)

a. Set:

CH 2 AC-GND-DC	GND

b. Position trace to the center horizontal graticule line and push in the INVERT button.

c. CHECK—Trace shift is 2 divisions or less when switching from normal to inverted.

d. ADJUST—Invert Bal (R566) for minimum trace shift when switching between normal and inverted.

10. Check/Adjust CH 2 Position Centering (R434)

a. Set:

INVERT	Normal (button out)
CH 2 VOLTS/DIV	0.2 V
CH 2 AC-GND-DC	AC
A TRIGGER LEVEL	Fully clockwise

b. Connect a 50-kHz, leveled sine-wave signal to the CH 2 input via a 50-Ω bnc cable and a 50-Ω termination. Set the generator for a 2.4-division signal display.

c. Set CH 2 VOLTS/DIV switch to 20 mV without changing the VAR control.

d. CHECK—Top of display positions down to the center horizontal graticule line or below, and bottom of display positions up to center horizontal graticule or above.

e. ADJUST—CH 2 Position Center (R434) so that display positions the same distance above and below the center horizontal graticule line.

f. Disconnect test signal from the 468.

11. Check CH 1 and CH 2 Input FET Gate Current

a. Set:

AC-GND-DC (both)	GND
VOLTS/DIV (both)	5 mV

b. Position the CH 2 trace to graticule center and set the CH 2 AC-GND-DC switch to DC.

c. CHECK—Trace shift is 0.1 division or less when switching between GND and DC.

d. Set VERT MODE switches to display CH 1. Position the CH 1 trace to graticule center and change the CH 1 AC-GND-DC switch to DC.

e. CHECK—Trace shift is 0.1 division or less when switching between GND and DC.

f. Set both AC-GND-DC switches to DC.

12. Check/Adjust Gain (R269, R117, and R569)

NOTE

It is not always necessary to perform a complete readjustment to meet instrument gain specifications. Use the following procedure to determine adjustments required.

a. Set:

VERT MODE	CH 2
CH 2 VOLTS/DIV	5 mV
CH 2 AC-GND-DC	DC

b. Connect a 20-mV, standard-amplitude square-wave signal to CH 2 input connector via a 50-Ω bnc cable.

c. CHECK—Display amplitude is 4 divisions within 3% (4 divisions ±0.12 division).

d. Change CH 2 VOLTS/DIV switch settings and standard-amplitude signals as shown in Table 4-12 and CHECK that dc accuracies are within the display limits listed in the table.

e. Set VERT MODE switches to display CH 1 and set the CH 1 AC-GND-DC switch to DC.

f. Move the input signal from the CH 2 input connector to the CH 1 input.

g. CHECK—Display amplitude is 4 divisions within 3% (4 divisions ±0.12 division).

h. Change CH 1 VOLTS/DIV switch settings and standard-amplitude signals as shown in Table 4-12 and CHECK that deflection accuracies are within the display limits listed in the table.

i. If all checks for both channels are within 3%, no further vertical gain calibration is required; skip to step 13. If any single check falls outside the 3% accuracy limits, a complete gain recalibration is required. Continue with part j of this step.

j. Set CH 1 VOLTS/DIV switch to 5 mV and set the standard-amplitude signal output to 20 mV.

Table 4-12

Vertical DC Accuracy

VOLTS/DIV Switch Setting	Standard Amplitude Signal	Deflection for 3% Accuracy		Display Limits (divisions)
		Divisions	Accuracy	
10 mV	50 mV	5	±0.15 div	4.85 to 5.15
20 mV	0.1 V	5	±0.15 div	4.85 to 5.15
50 mV	0.2 V	4	±0.12 div	3.88 to 4.12
.1 V	0.5 V	5	±0.15 div	4.85 to 5.15
.2 V	1 V	5	±0.15 div	4.85 to 5.15
.5 V	2 V	4	±0.12 div	3.88 to 4.12
1 V	5 V	5	±0.15 div	4.85 to 5.15
2 V	10 V	5	±0.15 div	4.85 to 5.15
5 V	20 V	4	±0.12 div	3.88 to 4.12

k. Set test oscilloscope controls as follows:

Vertical Mode	Add
Invert	On
Volts/Div (both)	0.1 V (with 10X probe)
Triggering	Auto (free-running sweep)
A Trigger Source	Ext (with no triggering signal applied)

l. Connect two 10X probes from the test oscilloscope; one to TP217 and the other to TP314 on the 468 Vertical Preamplifier board. Connect the probe ground leads to chassis ground.

m. CHECK—Signal between TP217 and TP314 is 400 mV p-p (4 divisions).

n. ADJUST—CH 1 Gain Adjust (R269) for 400 mV p-p.

NOTE

This is a nominal value for this adjustment. Readjustment may be required to obtain correct CH 1 overall gain.

o. Disconnect the probes from the 468 test points.

p. CHECK—Display is 4 divisions within 3% (4 divisions ±0.12 division).

q. ADJUST—Output Gain Adjust (R117) on the Vertical Output Amplifier board for a 4-division display.

r. Set CH 2 VOLTS/DIV switch to 5 mV and move the input signal from the CH 1 input to the CH 2 input. Set VERT MODE switches to display CH 2 only.

s. CHECK—Display is 4 divisions within 3% (4 divisions ±0.12 division).

t. ADJUST—CH 2 Gain Adjust (R569) for a 4-division display.

u. Repeat parts e through i of this step to recheck Vertical DC Accuracy for correct overall gain.

13. Check CH 1 and CH 2 VOLTS/DIV VAR Range

a. Set:

VERT MODE	CH 2
VOLTS/DIV (both)	10 mV

b. Connect a 50-mV, standard-amplitude square-wave signal to CH 2 input.

c. Rotate CH 2 VOLTS/DIV VAR control fully counterclockwise.

d. CHECK—Display reduces to 2 divisions or less in amplitude.

e. Move the test signal to CH 1 input and set the VERT MODE switches to display CH 1 input.

f. Rotate CH 1 VOLTS/DIV VAR control fully counterclockwise.

g. CHECK—Display reduces to 2 divisions or less in amplitude.

h. Return both VAR controls to their calibrated detent.

14. Check ADD Mode

a. Set:

VOLTS/DIV (both)	5 mV
VERT MODE	ADD
INVERT	Normal (button out)

b. Connect a 10-mV, standard-amplitude square-wave signal to both CH 1 and CH 2 inputs via a 50-Ω cable and dual-input coupler.

c. CHECK—Display amplitude is 4 divisions within 3% (4 divisions ±0.12 division).

15. Check Compression and Expansion

a. Set:

CH 2 AC-GND-DC	GND
VERT MODE	CH 1 only

b. Adjust CH 1 VAR control for an exact 2-division display, centered about the center horizontal graticule line.

c. Position top of display to top graticule line.

d. CHECK—For typical display compression or expansion of 0.1 division or less.

e. Position bottom of display to bottom graticule line.

f. CHECK—For typical display compression or expansion of 0.1 division or less.

g. Set CH 1 VAR control to the calibrated detent.

h. Disconnect the test equipment from the 468.

16. Check/Adjust TRACE SEP Centering (R112)

a. Set:

A TIME/DIV	2 μs
HORIZ DISPLAY	ALT
B TIME/DIV	0.2 μs

b. Use the CH 1 Vertical POSITION control to center the A trace and use the TRACE SEP control to superimpose the B trace at the center horizontal graticule line.

c. CHECK—TRACE SEP control will separate the B trace from the A trace equally (at least 4 divisions) in both the upward and downward direction as the control is rotated between fully clockwise and fully counterclockwise.

d. ADJUST—Trace Sep Centering (R112) for a vertically centered trace separation range when rotating the TRACE SEP control between the fully clockwise and fully counterclockwise positions.

17. Check/Adjust Low-Frequency Compensation

a. Set:

A TIME/DIV	0.2 ms
VERT MODE	CH 1
AC-GND-DC (both)	DC
VOLTS/DIV (both)	5 mV
A TRIGGER LEVEL	For a stable display
HORIZ DISPLAY	A

b. Connect the square-wave generator fast-rise + output through a 50-Ω bnc cable, a 10X attenuator, and a 50-Ω bnc termination to the CH 1 input.

c. Adjust the generator as necessary to maintain a 5-division display throughout the step.

d. CHECK—Display overshoot or rounding is within 3% (4.85 to 5.15 division) for each A TIME/DIV switch setting and generator setting given in Table 4-13.

Table 4-13

Maximum Overshoot or Rounding

Fast-Rise + Frequency	A TIME/DIV Switch Setting	Rounding or Overshoot Tolerance (divisions)
1 kHz	0.2 ms	4.85 to 5.15
10 kHz	20 μs	4.85 to 5.15
100 kHz	2 μs	4.85 to 5.15

e. If all checks are within tolerance, skip to step 18. If not, continue with part f of this step.

f. Set:

A TIME/DIV	0.2 ms
VERT MODE	CH 1, CH 2, and ALT
A TRIGGER SLOPE	– (minus)
A TRIGGER LEVEL	For a stable display

g. Unplug the cable connector from J686 (Vert Alt Sync output from the Interface board) and insert the P686 plug into a bnc-female-to-coaxial-cable-connector adapter. Connect the square-wave output of the low-frequency sine-wave generator to the bnc-to-cable-connector adapter via a 50-Ω bnc cable. Set the generator output frequency to 1 kHz and adjust CH 1 and CH 2 Vertical POSITION controls for a 6-division display. Adjust the A TRIGGER LEVEL control for a stable display. Presentation will be a square wave when the CH 1 and CH 2 traces alternate at the generator frequency.

NOTE

As an alternate signal source, use the fast-rise – (minus) output of the calibration generator. Do not terminate the cable and adjust the output amplitude to maximum. Any other signal source used must be TTL compatible to supply the proper logic voltage levels to drive the Vertical Switching Logic circuit.

h. ADJUST—Vertical Output LF Compensation for the best flat top on the display, using the settings and adjustments given in Table 4-14. Rounding or overshoot must be 3% or less.

i. INTERACTION—Repeat 1-kHz, 10-kHz, and 100-kHz adjustments until no further improvement is obtained.

Table 4-14

Vertical Output Low-Frequency Compensation

Square-Wave Frequency	TIME/DIV Switch Setting	Adjustment Circuit Number
1 kHz	0.2 ms	R335
10 kHz	20 μs	R329, R325
100 kHz	2 μs	R321, R319

j. Unplug the P686 cable connector from the bnc-to-cable-connector adapter and plug the connector back into J686.

k. Set:

A TIME/DIV	0.2 ms
VERT MODE	CH 1
A TRIGGER SLOPE	+ (plus)

l. Connect a 1-kHz, fast-rise + signal to the CH 1 input connector via a 50-Ω bnc cable, a 10X attenuator, and a 50-Ω bnc termination. Set the generator for a 6-division display and adjust the A TRIGGER LEVEL control for a stable display.

m. ADJUST—CH 1 LF Compensation for the best flat top on the display, using the settings and adjustments given in Table 4-15. Rounding or overshoot must be 3% or less.

Table 4-15

CH 1 Low-Frequency Compensation

Square-Wave Frequency	TIME/DIV Switch Setting	Adjustment Circuit Number
1 kHz	0.2 ms	R165
10 kHz	20 μs	R172
100 kHz	2 μs	R321 and R319 on the Vertical Output board if needed (see Table 4-16).

n. Move the test signal from the CH 1 input to the CH 2 input and set the VERT MODE switches to display CH 2 only.

Table 4-16

CH 2 Low-Frequency Compensation

Square-Wave Frequency	TIME/DIV Switch Setting	Adjustment Circuit Number
1 kHz	0.2 ms	R371
10 kHz	20 μs	R373
100 kHz	2 μs	R321 and R319 for best compromise between CH 1 and CH 2.

o. ADJUST—CH 2 LF Compensation for the best flat top on the display, using the settings and adjustments given in Table 4-16. Rounding or overshoot must be 3% or less.

p. Disconnect the fast-rise + signal from the 468.

NOTE

In steps 18 and 19, all VOLTS/DIV Checks and Adjustments require the use of a 10X probe with scale-factor switching (preferably the probe supplied with the oscilloscope being calibrated).

18. Check/Adjust CH 1 VOLTS/DIV Compensation

NOTE

Input capacitor C13010, in the CH 1 Attenuator, is set at the factory to give C13010 in the CH 2 Attenuator enough range to match CH 2 input capacitance with CH 1 input capacitance. Unless there is a circuit malfunction, the CH 1 C13010 should not require readjustment.

Make any adjustments required in the attenuator and preamplifier using a low-capacitance screwdriver only. If the screwdriver has a metal bit, the adjustment may be affected. Check adjustment after the screwdriver is removed from the adjustment screw, and readjust if necessary.

a. Set:

VOLTS/DIV (both)	5 mV (see NOTE preceeding step 18)
VERT MODE	CH 1
A TIME/DIV	0.2 ms (see NOTE after part h)
20 MHz BW LIMIT	Limited bandwidth (button in)

b. Connect a 10X probe to the CH 1 input (note that the VOLTS/DIV Scale-Factor LED now indicates 50 mV).

NOTE

If the oscilloscope is to be used primarily with a 50-Ω signal source, more accurate reproduction of the waveform front corner may be achieved by calibrating with a 50-Ω system. To accomplish this, substitute a properly terminated 50-Ω bnc cable for the 10X probe while making the front-corner adjustments listed in Table 4-17.

c. Connect the square-wave high-amplitude test signal to the tip of the 10X probe via a 2X, 5X, or 10X attenuator (depending on the generator output signal amplitude) and bnc-to-probe-tip adapter. Check generator output impedance to determine if a 50-Ω termination is required.

d. Set the generator for a 1-kHz, 5-division display. During the remainder of procedure steps 18 and 19, add or remove attenuators and/or termination as needed to maintain a 5-division display of the test signal.

e. Adjust the probe compensation for the best flat top on the displayed waveform. Do not readjust the probe compensation during the remainder of this step.

f. Set CH 1 VOLTS/DIV switch to 0.1 V (with 10X probe).

g. CHECK—Compensation for all VOLTS/DIV settings listed in Table 4-17 is adjusted to produce a displayed waveform that has 2% or less overshoot or rounding and has a flat top within 2% (4.9 to 5.1 divisions). If compensation is within 2%, skip part h. If not, perform part h.

h. ADJUST—Any adjustment pair (as given in Table 4-17) required to compensate all settings of the VOLTS/DIV switch to within 2%.

NOTE

When adjusting compensation, one adjustment will affect the waveform front corner and another will affect the flat top. Ignore the front corner when making the flat-top adjustment and vice versa. The A TIME/DIV switch should be set to 1 ms for the flat-top and to 0.2 ms for front-corner checks and adjustments.

Table 4-17

VOLTS/DIV Compensation

VOLTS/DIV Setting (10X Scale-Factor)	Adjust	
	TIME/DIV Set to 1 ms FLAT	TIME/DIV Set to 0.2 ms CORNER
0.1 V	C37	C36
0.2 V	C35	C34
0.5 V	C33	C32
1.0 V	Check	Check
2.0 V	Check	Check
5.0 V	C31	C30

19. Adjust CH 2 VOLTS/DIV Compensation

a. Set:

VERT MODE CH 2

b. Move the 10X probe connector from the CH 1 input to the CH 2 input. Do not readjust probe compensation.

c. Adjust the generator for a 1-kHz, 5-division display. Add or remove attenuators and/or termination as needed to maintain a 5-division signal display throughout the remainder of this step.

d. CHECK—Display for a flat-top waveform, within 2% (±0.1 division).

e. ADJUST—C13010 in the CH 2 Preamplifier input for best flat-top waveform, using a low-capacitance alignment tool.

f. Set:

CH 2 VOLTS/DIV 0.1 V

g. Repeat step 18, parts g and h, for CH 2.

h. Disconnect the test setup from the 468.

NOTE

Adjustments contained in steps 20 through 26 interact. Before attempting to make any adjustment, first perform these seven steps in sequence and make all the checks. If all checks are within the given limits, proceed to step 27.

If any of the checks are not within the given limits, perform steps 20 through 26, making adjustments as required with a low-capacitance alignment tool.

If all checks are still not within the given limits after making adjustments, perform all of steps 6 through 26.

If calibration is being performed after repair or replacement of vertical system components, adjustments may be made as they occur in each step.

20. Check/Adjust CH 2 and Output High-Frequency Compensation

a. Set:

VOLTS/DIV (both) 5 mV
20 MHz BW LIMIT Full bandwidth (button out)

b. Connect a 100-kHz, fast-rise + (positive-going) square-wave signal via a 50-Ω bnc cable, a 10X attenuator, and a 50-Ω bnc termination to the CH 2 input.

c. Adjust the generator for a 5-division signal display.

d. Set:

A TIME/DIV 0.2 μs

e. CHECK—Flat-top display aberrations are within 4% (±0.2 division). See Figure 4-2 for a typical display.

f. ADJUST—R477, C480, R438, C444 (CH 2), and C213, R218, R229, and C234 (Vertical Output Amplifier) for best front corner.

g. Apply a fast-rise – (negative-going) signal to the CH 2 input. Maintain the 5-division signal amplitude.

h. Set A TRIGGER SLOPE switch to – (minus).

i. CHECK—Flat-bottom display aberrations are within 6% (±0.3 division).

21. Check CH 2 Position Effect

a. Use the CH 2 Vertical POSITION control to position the bottom of the display to the top graticule line.

b. CHECK—Display aberrations are within 8% (±0.4 division).

c. Set A TRIGGER SLOPE switch to + (plus).

d. Apply a fast-rise + signal (5 divisions in amplitude) to the CH 2 input.

e. Position the top of the display to the bottom graticule line.

f. CHECK—Display aberrations are within 6% (±0.3 division).

22. Check/Adjust CH 1 High-Frequency Compensation

a. Set VERT MODE switches to display CH 1 only.

b. Move the fast-rise + signal from the CH 2 input to the CH 1 input.

c. CHECK—Flat-top display aberrations are within 4% (±0.2 division). See Figure 4-2 for a typical display.

d. ADJUST—R176, C181, R240, and C244 (CH 1) for best flat-top display.

INTERACTION—It may be necessary to compromise the Vertical Output Amplifier adjustments and the CH 2 adjustments made in step 20, part f, to obtain the best high-frequency match between CH 1 and CH 2.

e. Apply the fast-rise – (negative-going) signal to the CH 1 input.

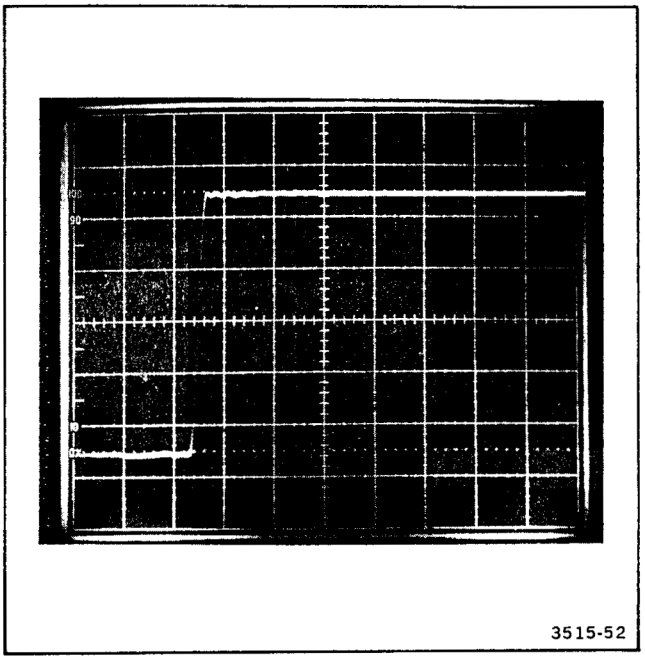

Figure 4-2. Typical display when high-frequency compensation is correctly adjusted.

f. Set A TRIGGER SLOPE switch to – (minus).

g. CHECK—Flat-bottom aberrations are within 6% (±0.3 division).

23. Check CH 1 Position Effect

a. Position bottom of the display to the top graticule line.

b. CHECK—Display aberrations are within 8% (±0.4 division).

c. Set A TRIGGER SLOPE switch to + (plus).

d. Apply the fast-rise + signal to the CH 1 input.

e. Position top of the display to the bottom graticule line.

f. CHECK—Display aberrations are within 6% (±0.3 division).

24. Check CH 1 Transient Response

a. Verify that A TRIGGER SLOPE switch is set to + and that the fast-rise + signal is connected to the CH 1 input via a 50-Ω bnc cable, a 10X attenuator, and a 50-Ω bnc termination.

b. Set the generator and add or remove attenuators as required to maintain a 5-division display throughout part c of this step.

c. CHECK—Display flat-top aberrations are within 4% (±0.2 division) for each of the following VOLTS/DIV switch settings: 5 mV, 10 mV, 20 mV, and 50 mV. (Maintain the 5-division display in each position checked.)

25. Check CH 2 Transient Response

a. Set VERT MODE switches to display CH 2 only.

b. Move the fast-rise + signal from the CH 1 input to the CH 2 input.

c. Adjust the generator and add or remove attenuators as required to maintain a 5-division display throughout part d of this step.

d. CHECK—Display flat-top aberrations are within 4% (±0.2 division) for each of the following VOLTS/DIV switch settings: 5 mV, 10 mV, 20 mV, and 50 mV. (Maintain the 5-division display in each position checked.)

e. Disconnect the test equipment from the 468.

26. Check Bandwidth

a. Set:

A TIME/DIV	0.2 ms
CH 2 VOLTS/DIV	5 mV

b. Connect the leveled sine-wave generator reference signal (reference signal frequency is typically 50 kHz) via a 50-Ω bnc cable, a 10X attenuator, and a 50-Ω bnc termination to the CH 2 input.

c. Adjust the generator for a 5-division reference-signal display.

d. Set the generator frequency to 100 MHz.

e. CHECK—Display amplitude is 3.5 divisions or more.

f. Repeat parts c, d, and e of this step for the 10-mV through 1-V positions of the CH 2 VOLTS/DIV switch.

g. Change VERT MODE switches to display CH 1 only and move the signal from the CH 2 input to the CH 1 input.

h. Repeat parts c, d, and e of this step for the 5-mV through 1-V positions of the CH 1 VOLTS/DIV switch.

i. Disconnect the test setup from the 468.

27. Check Cascaded Gain and Bandwidth

a. Set:

VOLTS/DIV (both)	5 mV
AC-GND-DC (both)	AC
VERT MODE	CH 2
A TIME/DIV	1 ms

b. Connect the CH 1 VERT SIGNAL OUT (located on the 468 rear panel) via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 2 input connector.

c. Connect a 5-mV, standard-amplitude square-wave signal to the CH 1 input via a 50-Ω bnc cable.

d. CHECK—Display amplitude is 5 divisions or more.

e. Remove the standard-amplitude signal from the CH 1 input.

f. Connect a leveled sine-wave reference signal via a 50-Ω bnc cable, a 10X attenuator, and a 50-Ω bnc termination to the CH 1 input.

g. Adjust generator for a reference signal display of 5 divisions. (Reference-signal frequency is typically 50 kHz.)

h. Change the generator output frequency to 50 MHz.

i. CHECK—Display amplitude is 3.5 divisions or more.

j. Disconnect the test signal from the 468.

28. Check Channel Isolation

a. Set:

CH 2 VOLTS/DIV	0.2 V
VERT MODE	CH 2
CH 1 AC-GND-DC	GND
CH 2 AC-GND-DC	DC

b. Connect a 25-MHz, leveled sine-wave signal via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 2 input.

c. Adjust the generator for a 2-division display.

d. Set:

VOLTS/DIV (both)	20 mV
VERT MODE	CH 1
A TRIGGER SOURCE	CH 2
A TRIGGER LEVEL	As needed for a stable display

e. CHECK—Display amplitude is 0.2 division or less.

f. Move the test signal from the CH 2 input to the CH 1 input.

g. Set:

CH 1 AC-GND-DC	DC
CH 2 AC-GND-DC	GND
VERT MODE	CH 2
A TRIGGER SOURCE	CH 1
A TRIGGER LEVEL	As needed for a stable display

h. CHECK—Display amplitude is 0.2 division or less.

i. Disconnect the test setup from the 468.

29. Check/Adjust Common-Mode Rejection Ratio (R569)

a. Set:

VOLTS/DIV (both)	20 mV
AC-GND-DC (both)	DC
A TRIGGER SOURCE	NORM
VERT MODE	CH 1
CH 2 INVERT	Inverted (button in)

b. Connect a 20-MHz, leveled sine-wave signal via a 50-Ω bnc cable, a 10X attenuator, a 50-Ω bnc termination, and a dual-input coupler to the CH 1 and CH 2 inputs.

c. Set the generator amplitude for a 6-division display.

d. Set VERT MODE switches to display ADD only (press CH 1 push button to release it, removing the CH 1 trace from the display).

e. CHECK—Display amplitude is 0.6 division or less. This indicates that the common-mode rejection ratio is at least 10:1 at 20 MHz.

f. If the check in part e meets the requirement, skip to part m. If it does not, continue with part g.

g. Set VERT MODE switches to display CH 1 only.

h. Change the generator frequency to 50 kHz and adjust the amplitude to obtain a 6-division display.

i. Set VERT MODE switches to display ADD only.

j. ADJUST—CH 2 Gain Adjust (R569) for minimum display amplitude (best CMRR).

k. Change the generator frequency to 20 MHz.

l. CHECK—Display amplitude is 0.6 division or less.

m. Press CH 2 INVERT push button to release it; disconnect the test setup.

30. Check Bandwidth Limit Operation

a. Set:

20 MHz BW LIMIT	Limited bandwidth (button in)
CH 1 AC-GND-DC	DC
VERT MODE	CH 1

b. Connect the leveled sine-wave reference frequency signal via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input.

c. Set the generator output amplitude to obtain a 6-division display.

d. Increase the generator frequency until the display amplitude is 4.2 divisions.

e. CHECK—Generator frequency is within the range of 16 MHz to 24 MHz.

f. Disconnect the test setup from the 468.

31. Check/Adjust Trigger View Centering and Gain (R534 and R443)

a. Set:

A TRIGGER COUPLING	AC
A TRIGGER SOURCE	EXT
A TRIGGER LEVEL	0
A TIME/DIV	0.2 ms
VERT MODE	A TRIG VIEW

b. Connect a 0.5-V, standard-amplitude square-wave signal to the EXT A TRIGGER input via a 50-Ω bnc cable.

c. CHECK—Display will trigger symmetrically within 1 division of the center horizontal graticule line when A TRIGGER SLOPE is switched between + and —.

d. ADJUST—Trig View Centering (R534) to center the display about the center horizontal graticule line (verify that the A TRIGGER LEVEL is set to 0).

e. CHECK—Display amplitude is 5 divisions ±5% (4.75 to 5.25 divisions).

f. ADJUST—Trig View Gain (R443) to obtain a 5-division display.

g. INTERACTION—Between Trig View Centering and Trig View Gain adjustments. Repeat parts d through f until no visible interaction is observed.

h. Disconnect the signal from the EXT A TRIGGER input.

32. Check/Adjust Trigger View Low-Frequency Compensation (C509 and C510)

a. Connect a 1-kHz high-amplitude square-wave signal to the EXT A TRIGGER input via a 50-Ω bnc cable (check generator used to determine if a 50-Ω bnc termination is required).

b. Set generator output amplitude to obtain a 5-division display.

c. CHECK—Square wave has 10% or less overshoot or rounding (±0.5 division).

d. ADJUST—C509 for the best flat top on the square-wave display.

e. Set A TRIGGER SOURCE switch to EXT/10 and adjust the generator to obtain a 5-division display.

f. ADJUST—C510 for the best flat top on the square-wave display.

g. Disconnect the bnc cable from the 468.

33. Check/Adjust Trigger View High-Frequency Compensation (C438, C538, and R435).

a. Set:

A TIME/DIV	0.2 μs
A TRIGGER SOURCE	EXT

b. Connect a 100-kHz, fast-rise + square-wave signal via a 50-Ω bnc cable and a 50-Ω bnc termination to the EXT A TRIGGER input.

c. Adjust the generator output amplitude to obtain a 5-division display.

d. CHECK—Square-wave front corner has less than 10% aberration (±0.5 division).

e. ADJUST—C438, C538, and R435 for the best front corner to obtain a square-wave rise time of 5 ns or less.

f. Disconnect test signal from the 468.

34. Check/Adjust Zero Trigger View Delay (R124 and R270)

a. Set:

VERT MODE	CH 1 and A TRIG VIEW
HORIZ DISPLAY	A
A TIME/DIV	0.02 μs
A TRIGGER SOURCE	EXT
A TRIGGER COUPLING	AC
CH 1 VOLTS/DIV	0.1 V

b. Connect a 40-MHz, leveled sine-wave signal via a bnc T-connector, two 42-inch (equal-length) 50-Ω bnc cables, and two 50-Ω bnc terminations; one connected to the CH 1 input and the other to the EXT A TRIGGER input. Set the generator output signal amplitude to obtain a 6-division A TRIG VIEW signal display.

c. Set the CH 1 VOLTS/DIV switch and VAR control to match the CH 1 display-signal amplitude to the A TRIG VIEW display-signal amplitude.

d. Use the CH 1 Vertical POSITION control and the A TRIGGER LEVEL control to superimpose the two displayed signals.

e. Set:

X10 MAG	On (button in)

f. CHECK—Phase difference between the CH 1 signal and the A TRIG VIEW signal is 0.2 horizontal graticule division or less.

NOTE

See Figure 4-3 for location of access holes through the Storage Display circuit board to reach adjustments located on the Timing circuit board.

g. ADJUST—R124 for zero phase difference between the CH 1 signal and the A TRIG VIEW signal.

h. Set:

HORIZ DISPLAY	B DLY'D
A TIME/DIV	0.2 μs
B TIME/DIV	0.02 μs
X10 MAG	Off (button out)

i. Repeat part c of this step to verify the two signals are superimposed.

j. Set:

X10 MAG	On (button in)

k. CHECK—Phase difference between the CH 1 signal and the A TRIG VIEW signal is 0.2 horizontal graticule division or less.

l. ADJUST—R270 for zero phase difference between the CH 1 signal and the A TRIG VIEW signal.

m. Disconnect the test setup from the 468.

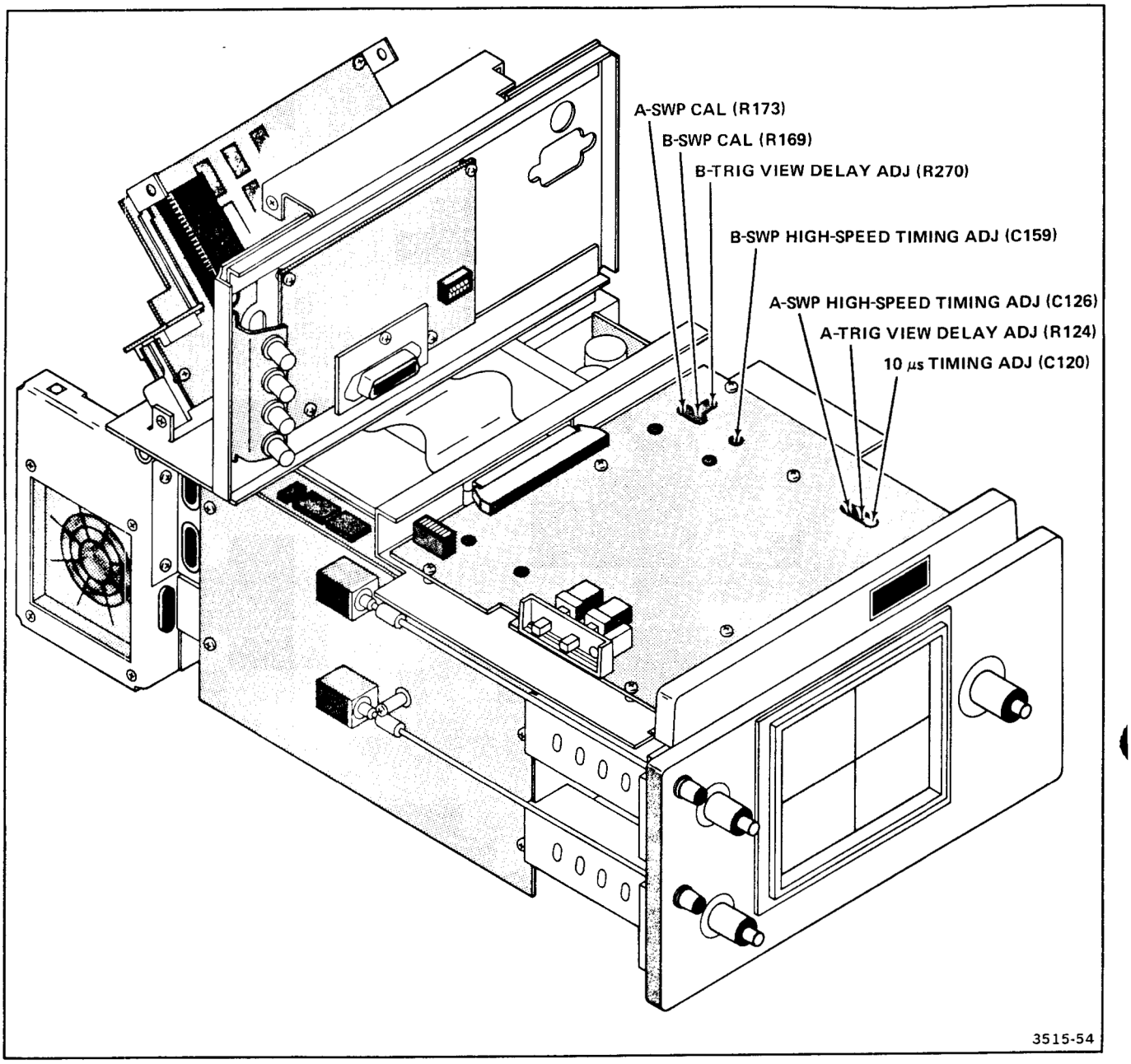

Figure 4-3. Location of timing adjustments accessed through the Storage Display circuit board.

TRIGGERING

Equipment Required (see Table 4-1)

4. 10X Probe (supplied with the 468)
6. Leveled Sine-Wave Generator
7. Time-Mark Generator
8. Low-Frequency Sine-Wave Generator
11. 50-Ω Signal Pickoff Unit (Type CT-3)
12. 42-in., 50-Ω Bnc Cable (2 required)
14. Gr-to-bnc-female Adapter
15. Gr-to-bnc-male Adapter
19. Dual-Input Coupler (2 required)
20. Bnc T-Connector
21. 10X Bnc Attenuator
24. 50-Ω Bnc Termination
25. 3-in., Flat-Bit Screwdriver

See ADJUSTMENT LOCATIONS 2 *and* ADJUSTMENT LOCATIONS 3 *in this Volume for test point and adjustment locations.*

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER	ON (button in)

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2)

VOLTS/DIV	10 mV
VOLTS/DIV VAR	Calibrated detent
VERT MODE	CH 1
POSITION	Midrange
AC-GND-DC	DC
INVERT	Off (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Triggering (A and B if applicable)

A TRIGGER SOURCE	NORM
A TRIG MODE	AUTO
SLOPE	+
COUPLING	AC
LEVEL	For a stable display
A TRIGGER HOLDOFF	NORM

Sweep (A and B)

HORIZ DISPLAY	A
DELAY TIME POSITION	Fully counterclockwise
TIME/DIV (both)	0.05 μs
TIME/DIV VAR	Calibrated detent
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

NON STORE	On (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check/Adjust A Trigger Sensitivity and TRIG LED (R351)

a. Connect a 10-MHz, leveled sine-wave signal to both the A and B EXT TRIGGER inputs and the CH 1 and CH 2 inputs as shown in Figure 4-4.

b. Adjust the generator output amplitude for a 3-division signal display.

c. Set the CH 1 VOLTS/DIV switch to 0.1 V (0.3 division display).

d. CHECK—Stable display can be obtained by rotating the A TRIGGER LEVEL control with SLOPE switch in both + and —.

e. CHECK—TRIG LED is illuminated when the display is stable.

f. Set:

CH 1 AC-GND-DC GND

g. CHECK—Stable display cannot be obtained for any position of the A TRIGGER LEVEL control with SLOPE switch in either + or — (TRIG LED does not remain illuminated). Return the A TRIGGER SLOPE to +.

h. If the checks in parts b through g meet the requirements, skip to step 2. If not, continue with the following parts.

i. Set:

CH 1 AC-GND-DC AC

j. ADJUST—A Trigger Sensitivity (R351) so display can just be triggered by rotating the A TRIGGER LEVEL control (A TRIGGER SLOPE in +).

k. Set:

CH 1 AC-GND-DC GND

l. CHECK—Stable baseline display cannot be obtained for any position of the A TRIGGER LEVEL with SLOPE in + (negative slope is generally slightly more sensitive).

m. If a stable display can be obtained, then the trigger sensitivity is too high. Adjust A Trigger Sensitivity (R351) slightly so display just fails to trigger for any position of the A TRIGGER LEVEL control (with the A TRIGGER SLOPE in + only).

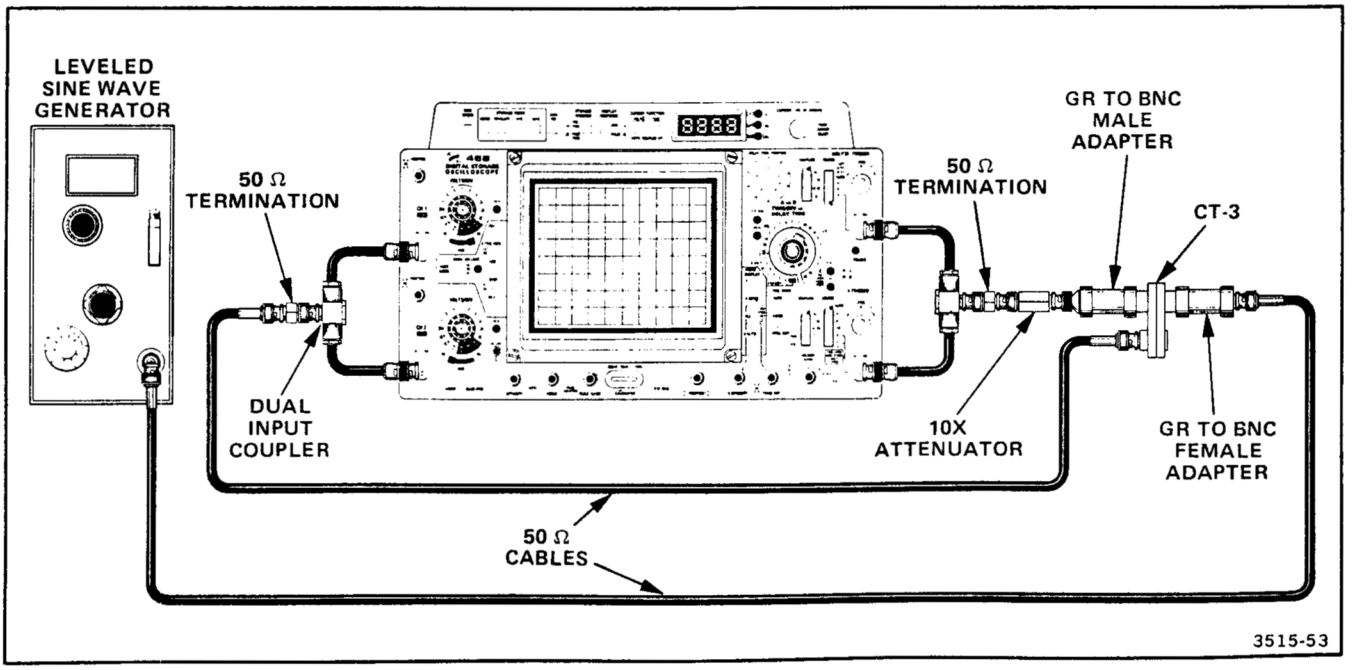

Figure 4-4. Test setup for A and B triggering checks and adjustments.

n. Repeat step 1, parts i through m, until a stable display can be obtained on a 0.3-division display, but not on a baseline trace (+ SLOPE only).

o. Repeat checks in step 1, parts b through g.

2. Check/Adjust B Trigger Sensitivity (R154)

a. Set:

HORIZ DISPLAY	B DLY'D
CH 1 VOLTS/DIV	10 mV
CH 1 AC-GND-DC	DC
A TRIGGER LEVEL	Fully clockwise
B TRIGGER LEVEL	For a stable display

b. Adjust the generator for a 3-division signal display.

c. Set:

CH 1 VOLTS/DIV	0.1 V (0.3-division display)

d. CHECK—Stable display can be obtained by rotating the B TRIGGER LEVEL control with the B TRIGGER SLOPE in either + or —.

e. Set:

CH 1 AC-GND-DC	GND

f. CHECK—Stable display cannot be obtained by rotating the B TRIGGER LEVEL control with the B TRIGGER SLOPE in either + or —.

g. If the checks in preceding parts b through f meet the requirements, skip to step 3. If they do not, continue with the following parts.

h. Set:

CH 1 AC-GND-DC	AC

i. ADJUST—B Trigger Sensitivity (R154) so display can just be triggered by rotating the B TRIGGER LEVEL control (B TRIGGER SLOPE in + only).

j. Set:

CH 1 AC-GND-DC	GND

k. CHECK—Stable display cannot be obtained by rotating the B TRIGGER LEVEL control (with B TRIGGER SLOPE in + only).

l. If a stable display can be obtained, then the trigger sensitivity is too high. Adjust B Trigger Sensitivity (R154) slightly so display will just fail to trigger in any position of the B TRIGGER LEVEL control (with SLOPE in + only).

m. Repeat step 2, parts h through l, until a stable display can be obtained on a 0.3-division display, but not on a baseline trace.

n. Repeat checks in parts c through f.

3. Check/Adjust B Trigger Slope Center and Level (R148 and R134)

a. Set:

B TRIGGER SOURCE	STARTS AFTER DELAY
TIME/DIV (both)	10 μs
B TRIGGER LEVEL	0
CH 1 VOLTS/DIV	10 mV
CH 1 AC-GND-DC	GND

NOTE

The B TRIGGER LEVEL control must remain set to 0 throughout this step.

b. Use the CH 1 Vertical POSITION control to align the trace with the center horizontal graticule line.

c. Set:

CH 1 AC-GND-DC	DC
B TRIGGER SOURCE	NORM

d. Adjust the generator for a 50-kHz, 4-vertical-division signal display.

e. CHECK—Display begins at about the same vertical point, within 1 division of graticule center, when B TRIGGER SLOPE is switched between + and —.

f. ADJUST—B Slope Center (R148) so that the display starts at the same vertical point on the sine wave with SLOPE switch in both + and — (not necessarily the center horizontal graticule line). Return the B TRIGGER SLOPE switch to +.

g. ADJUST—B Trig Level (R134) to move the starting point of the display to the center horizontal graticule line.

INTERACTION—B Trig Level (R134), B Slope Center (R148), and B Trigger Sensitivity (R154) will interact. Repeat parts f and g of this step and step 2, parts i through o, until no improvement is noted.

4. Check/Adjust A Trigger Slope Center and Level (R349 and R330)

a. Set:

HORIZ DISPLAY	A
A TRIGGER LEVEL	0

NOTE

The A TRIGGER LEVEL control must remain set to 0 throughout this step.

b. CHECK—Display begins at about the same vertical point (within 1 division of graticule center) when A TRIGGER SLOPE is switched between + and —.

c. ADJUST—A Slope Center (R349) so that the display starts at the same vertical point on the sine wave with the SLOPE in both + and — (not necessarily the center horizontal graticule line). Return the A TRIGGER SLOPE switch to +.

d. ADJUST—A Trig Level (R330) to move the starting point of the display to the center horizontal graticule line.

INTERACTION—A Trig Level (R330), A Trigger Sensitivity (R351), and A Slope Center (R349) will interact. Repeat parts c and d of this step and step 1, parts i through p, until no improvement is noted.

5. Check/Adjust A Trigger DC Levels (R205, R122, and R431)

a. Set:

A TRIGGER COUPLING	DC

NOTE

The A TRIGGER LEVEL control must remain set to 0 throughout this step.

b. CHECK—Vertical position of the start of the display is within 1 division of the center horizontal graticule line when A TRIGGER SLOPE is switched between + and —. Return the A TRIGGER SLOPE to +.

c. ADJUST—Norm Trig DC Balance (R205) to move the starting point of the display to the center horizontal graticule line.

INTERACTION—A and B Trig Level (R330 and R134) interact with Norm Trig DC Balance (R205). Repeat part c of this step, step 4 part d, and step 3 part g until no improvement is noted.

d. Set:

A TRIGGER SOURCE	CH 1

e. CHECK—Vertical position of the start of the display is within 1 division of the center horizontal graticule line when A TRIGGER SLOPE is switched between + and —. Return the A TRIGGER SLOPE to +.

f. ADJUST—CH 1 Trig DC Balance (R122) to move the starting point of the display to the center horizontal graticule line.

g. Set:

A TRIGGER SOURCE	CH 2

h. CHECK—Vertical position of the start of the display is within 1 division of the center horizontal graticule line when the A TRIGGER SLOPE is switched between + and —. Return the A TRIGGER SLOPE to +.

i. ADJUST—CH 2 Trig DC Balance (R431) to move the starting point of the displayed signal to the center horizontal graticule line.

6. Check B Trigger DC Levels

a. Set:

HORIZ DISPLAY	B DLY'D
A TRIGGER LEVEL	Fully clockwise
B TRIGGER LEVEL	0
B TRIGGER COUPLING	DC
B TRIGGER SOURCE	NORM

NOTE

The B TRIGGER LEVEL control must remain set to 0 throughout this step.

b. CHECK—Vertical position of start of the display is within 1 division of the center horizontal graticule line when B TRIGGER SOURCE is switched to the following positions: NORM, CH 1, and CH 2.

7. Check B Internal 10-MHz Triggering

a. Set:

TRIGGER COUPLING (both)	AC
CH 1 VOLTS/DIV	10 mV
CH 2 VOLTS/DIV	0.1 V
A TIME/DIV	0.2 μs
B TIME/DIV	0.05 μs
TRIGGER SOURCE (both)	NORM

b. Adjust the generator for a 10-MHz, 3-division signal display amplitude (30 mV).

c. Set the CH 1 VOLTS/DIV switch to 0.1 V (0.3-division display).

d. Adjust the B TRIGGER LEVEL control as needed for a stable display.

e. CHECK—For a stable display, with B TRIGGER SLOPE switched to both + and — in the following B TRIGGER switch settings:

B TRIGGER	
SOURCE	COUPLING
NORM	AC, DC
CH 1	DC, AC
CH 2	AC, DC

f. Set:

CH 1 VOLTS/DIV	10 mV
B TRIGGER COUPLING	LF REJ

g. Adjust the generator for a 10-MHz, 5-division signal display (50 mV).

h. Set the CH 1 VOLTS/DIV switch to 0.1 V (0.5-division display).

i. Adjust the B TRIGGER LEVEL control as needed to obtain a stable display.

j. CHECK—For a stable display, with B TRIGGER SLOPE switched to both + and — in each of the following B TRIGGER SOURCE switch positions: CH 2, CH 1, and NORM.

k. Set:

B TRIGGER COUPLING	HF REJ

l. CHECK—A stable display cannot be obtained in any of the following B TRIGGER SOURCE switch positions: NORM, CH 1, and CH 2.

8. Check A Internal 10-MHz Triggering

a. Set:

HORIZ DISPLAY	A
A TIME/DIV	0.05 μs
A TRIGGER LEVEL	For a stable display
CH 1 VOLTS/DIV	10 mV

b. Adjust the generator for a 10-MHz, 3-division signal display (30 mV).

c. Set the CH 1 VOLTS/DIV switch to 0.1 V (0.3-division display).

d. Adjust the A TRIGGER LEVEL control to obtain a stable display.

e. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and — for the following A TRIGGER switch settings:

A TRIGGER	
SOURCE	COUPLING
NORM	AC, DC
CH 1	DC, AC
CH 2	AC, DC

f. Set:

CH 1 VOLTS/DIV	10 mV
A TRIGGER COUPLING	LF REJ

g. Adjust the generator for a 10-MHz, 5-division signal display (50 mV).

h. Set the CH 1 VOLTS/DIV switch to 0.1 V (0.5-division display).

i. Adjust the A TRIGGER LEVEL control as needed to obtain a stable display.

j. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and — in each of the following A TRIGGER SOURCE switch positions: CH 2, CH 1, and NORM.

k. Set:

A TRIGGER COUPLING	HF REJ

l. CHECK—No stable display can be obtained in the following A TRIGGER SOURCE switch positions: NORM, CH 1, and CH 2.

9. Check A External 10-MHz Triggering

a. Set:

VOLTS/DIV (both)	10 mV
TRIGGER COUPLING (both)	AC
TRIGGER SOURCE (both)	EXT

b. Set the generator for a 10-MHz, 5-division signal display and adjust the A TRIGGER LEVEL control to obtain a stable display.

NOTE

The generator must be adjusted as necessary to maintain a 5-division signal display throughout this step.

c. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and — in each of the following A TRIGGER COUPLING switch positions: AC and DC.

d. Set:

CH 1 VOLTS/DIV	20 mV
A TRIGGER COUPLING	LF REJ

e. Adjust the generator for a 10-MHz, 5-division signal display (100 mV).

f. Adjust the A TRIGGER LEVEL control as needed to obtain a stable display.

g. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and —.

h. Set:

A TRIGGER COUPLING	HF REJ

i. CHECK—No stable display can be obtained.

j. Remove the 10X attenuator from the external trigger test setup and set the A TRIGGER SOURCE switch to EXT/10.

k. CHECK—No stable display can be obtained at any TRIGGER SLOPE or TRIGGER LEVEL setting.

l. Set:

A TRIGGER COUPLING	LF REJ

m. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and —.

n. Set:

CH 1 VOLTS/DIV	10 mV
A TRIGGER COUPLING	AC

o. Adjust the generator for a 10-MHz, 5-division signal display (50 mV display with 0.5 V at the EXT TRIGGER input connector).

p. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and — in each of the following A TRIGGER COUPLING switch positions: AC and DC.

10. Check B External 10-MHz Triggering

a. Set:

HORIZ DISPLAY	B DLY'D
A TIME/DIV	0.2 μs
B TIME/DIV	0.05 μs

b. Reconnect the 10X attenuator into the external trigger test setup.

NOTE

The generator must be adjusted as necessary to maintain a 5-division signal display throughout this step.

c. CHECK—For a stable display, with the B TRIGGER SLOPE switched to both + and — in each of the following B TRIGGER COUPLING switch positions: AC and DC.

d. Set the CH 1 VOLTS/DIV switch to 20 mV.

e. Adjust the generator for a 10-MHz, 5-division signal display (100 mV).

f. Set:

B TRIGGER COUPLING	LF REJ
B TRIGGER LEVEL	For a stable display

g. CHECK—For a stable display, with the B TRIGGER SLOPE switched to both + and —.

h. Set:

B TRIGGER COUPLING	HF REJ

i. CHECK—No stable display can be obtained.

11. Check B and A External 100-MHz Triggering

a. Set:

TRIGGER COUPLING (both)	AC
TRIGGER SOURCE (both)	EXT
CH 1 VOLTS/DIV	50 mV

b. Adjust the generator for a 10-MHz, 5-division signal display (150 mV); then change the generator frequency to 100 MHz. Do not readjust signal amplitude.

c. Press in the X10 MAG push button.

d. Adjust both the A and B TRIGGER LEVEL controls as needed in the remainder of this step to obtain a stable display.

e. CHECK—For a stable display, with 0.1 division or less jitter, when the B TRIGGER SLOPE is switched to both + and — in each of the following B TRIGGER COUPLING switch positions: AC and DC.

f. Adjust the generator for a 10-MHz, 6-division signal display (300 mV); then change the generator frequency to 100 MHz. Do not readjust the signal amplitude.

g. Set:

B TRIGGER COUPLING	LF REJ

h. CHECK—For a stable display, with 0.1 division or less jitter, when the B SLOPE is switched to both + and —.

i. Set:

B TRIGGER COUPLING	HF REJ

j. CHECK—No stable display can be obtained.

k. Set:

A TIME/DIV	A
A TRIGGER COUPLING	LF REJ
A TRIGGER LEVEL	For a stable display

l. CHECK—For a stable display, with 0.1 division or less jitter, when the A TRIGGER SLOPE is switched to both + and —.

m. Set:

A TRIGGER COUPLING HF REJ

n. CHECK—No stable display can be obtained at any TRIGGER SLOPE or TRIGGER LEVEL setting.

o. Set:

A TRIGGER COUPLING AC

p. Adjust the generator for a 10-MHz, 5-division signal display (150 mV); then change the generator frequency to 100 MHz. Do not readjust the signal amplitude.

q. Adjust the A TRIGGER LEVEL control as needed to obtain a stable display.

r. CHECK—For a stable display, with 0.1 division or less jitter, when the A TRIGGER SLOPE is switched to both + and — in each of the following A TRIGGER COUPLING switch positions: AC and DC.

s. Remove the 10X attenuator from the external trigger test setup and set the A TRIGGER SOURCE switch to EXT/10.

t. Adjust the A TRIGGER LEVEL control as needed to obtain a stable display.

u. CHECK—For a stable display, with 0.1 division or less jitter, when the A TRIGGER SLOPE is switched to both + and — in each of the following A TRIGGER COUPLING switch positions: DC and AC.

v. Adjust the generator for a 10-MHz, 6-division signal display (300 mV); then change the generator frequency to 100 MHz. Do not readjust the signal amplitude.

w. Set:

A TRIGGER COUPLING	LF REJ
A TRIGGER LEVEL	For a stable display

x. CHECK—For a stable display, with 0.1 division or less jitter, when the A TRIGGER SLOPE is switched to both + and —.

y. Set:

A TRIGGER COUPLING HF REJ

z. CHECK—No stable display can be obtained at any TRIGGER SLOPE or TRIGGER LEVEL setting.

12. Check A Internal 100-MHz Triggering

a. Set:

VOLTS/DIV (both)	50 mV
TRIGGER SOURCE (both)	NORM
TRIGGER COUPLING (both)	AC

b. Reconnect the 10X attenuator into the external trigger test setup. Adjust the generator for a 100-MHz, 1.5-division signal display.

c. CHECK—For a stable display, with 0.1 division or less jitter, when the A TRIGGER SLOPE is switched to both + and — for each of the following A TRIGGER switch settings.

	A TRIGGER
SOURCE	COUPLING
NORM	AC, LF REJ, DC
CH 1	DC, LF REJ, AC
CH 2	AC, LF REJ, DC

d. Set:

A TRIGGER COUPLING HF REJ

e. CHECK—No stable display can be obtained at any TRIGGER SLOPE or TRIGGER LEVEL setting.

13. Check B Internal 100-MHz Triggering

a. Set:

HORIZ DISPLAY	B DLY'D
A TIME/DIV	0.2 μs
B TIME/DIV	0.05 μs
A TRIGGER COUPLING	DC
A TRIGGER SOURCE	NORM

b. CHECK—For a stable display, with 0.1 division or less jitter, when the B TRIGGER SLOPE is switched to both + and — for each of the following B TRIGGER switch settings.

B TRIGGER SOURCE	B TRIGGER COUPLING
NORM	AC, LF REJ, DC
CH 1	DC, LF REJ, AC
CH 2	AC, LF REJ, DC

NOTE

It may be necessary to adjust both A and B TRIGGER LEVEL controls to obtain the most stable display at higher frequencies when B Sweep is displayed.

c. Set:

B TRIGGER COUPLING	HF REJ

d. CHECK—No stable display can be obtained at any TRIGGER LEVEL or TRIGGER SLOPE setting.

14. Check A and B HF REJ Triggering

a. Set:

HORIZ DISPLAY	A
TIME/DIV (both)	10 μs
X10 MAG	Off (button in)
TRIGGER COUPLING (both)	HF REJ
TRIGGER SOURCE (both)	NORM
CH 1 VOLTS/DIV	0.1 V
CH 2 VOLTS/DIV	10 mV
VERT MODE	CH 2

b. Adjust the generator for a 50-kHz, 5-division signal display (50 mV).

c. Set the CH 2 VOLTS/DIV switch to 0.1 V.

d. Adjust the A TRIGGER LEVEL control as needed to obtain a stable display.

e. Change the generator frequency to 1 MHz and press in the X10 MAG push button.

f. CHECK—A stable display cannot be obtained with the A TRIGGER SOURCE switch in any of the following positions: NORM, CH 1, and CH 2.

g. Set:

A TRIGGER LEVEL	Fully clockwise
HORIZ DISPLAY	B DLY'D

h. CHECK—A stable display cannot be obtained with the B TRIGGER SOURCE switch in any of the following positions: NORM, CH 1, and CH 2.

15. Check Single Sweep

a. Set:

HORIZ DISPLAY	A
CH 1 VOLTS/DIV	50 mV
VERT MODE	CH 1
X10 MAG	Off (button out)
A TRIGGER COUPLING	AC
A TRIGGER SOURCE	NORM
A TRIGGER SLOPE	+
A TRIGGER LEVEL	0

b. Adjust the generator for a 50-kHz, 1-division signal display.

c. Adjust the A TRIGGER LEVEL control so the display is just triggered.

d. Set:

TIME/DIV (both)	10 ms
CH 1 AC-GND-DC	GND
A TRIG MODE	SINGL SWP (push in)

e. CHECK—READY LED illuminates.

f. Set:

CH 1 AC-GND-DC	DC

g. CHECK—A single sweep occurs, and the READY LED goes out.

h. Press in the SINGL SWP push button.

i. CHECK—A single sweep occurs each time the SINGL SWP push button is pressed.

j. Disconnect the test setup from the 468.

16. Check 60-Hz Internal Triggering

a. Set:

TIME/DIV (both)	5 ms
A TRIG MODE	NORM
CH 1 VOLTS/DIV	10 mV

b. Connect a 60-Hz, low-frequency sine-wave signal via a 50-Ω bnc cable, a bnc T-connector, and a 50-Ω bnc termination to the CH 1 input. From the other output of the T-connector, connect a 50-Ω bnc cable and a 50-Ω bnc termination to the EXT B TRIGGER input.

c. Adjust the generator for a 3-division signal display (30 mV).

d. Set the CH 1 VOLTS/DIV switch to 0.1 V (0.3-division display).

e. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and − in each of the following A TRIGGER COUPLING switch positions: AC and DC.

f. Set:

CH 1 VOLTS/DIV	10 mV
A TRIGGER COUPLING	HF REJ

g. Adjust the generator for a 60-Hz, 5-division signal display (50 mV).

h. Set the CH 1 VOLTS/DIV switch to 0.1 V (0.5-division display).

i. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and −.

j. Set:

A TRIGGER COUPLING	LF REJ

k. CHECK—No stable display can be obtained at any TRIGGER SLOPE or TRIGGER LEVEL setting.

l. Set:

A TRIG MODE	AUTO
A TRIGGER LEVEL	Fully clockwise
A TIME/DIV	10 ms
B TIME/DIV	5 ms
B TRIGGER SOURCE	NORM
B TRIGGER COUPLING	HF REJ
HORIZ DISPLAY	B DLY'D
CH 1 VOLTS/DIV	0.1 V

m. CHECK—For a stable display, with the B TRIGGER SLOPE switched to both + and −.

n. Set:

B TRIGGER COUPLING	LF REJ

o. CHECK—No stable display can be obtained at any TRIGGER LEVEL or TRIGGER SLOPE setting.

p. Set:

CH 1 VOLTS/DIV	10 mV
B TRIGGER COUPLING	AC

q. Adjust the generator for a 60-Hz, 3-division signal display (30 mV).

r. Set the CH 1 VOLTS/DIV switch to 0.1 V.

s. Adjust the B TRIGGER LEVEL control as needed to obtain a stable display.

t. CHECK—For a stable display, with the B TRIGGER SLOPE switched to both + and − in each of the following B TRIGGER COUPLING switch positions: AC and DC.

17. Check 60-Hz External Triggering

a. Set:

B TRIGGER COUPLING	AC
CH 1 VOLTS/DIV	10 mV

b. Adjust the generator for a 60-Hz, 5-division signal display (50 mV).

c. Set:

B TRIGGER SOURCE	EXT

d. CHECK—For a stable display, with the B TRIGGER SLOPE switched to both + and – in each of the following B TRIGGER COUPLING switch positions: AC and DC.

e. Set:

CH 1 VOLTS/DIV	20 mV
B TRIGGER COUPLING	HF REJ

f. Adjust the generator for a 60-Hz, 5-division signal display (100 mV).

g. CHECK—For a stable display, with the B TRIGGER SLOPE switched to both + and –.

h. Set:

B TRIGGER COUPLING	LF REJ

i. CHECK—No stable display can be obtained at any TRIGGER LEVEL or TRIGGER SLOPE setting.

j. Move the test signal from the EXT B TRIGGER input to the EXT A TRIGGER input.

k. Set:

HORIZ DISPLAY	A
A TIME/DIV	5 ms
A TRIGGER COUPLING	HF REJ
A TRIG MODE	NORM
A TRIGGER SOURCE	EXT
A TRIGGER LEVEL	For a stable display

l. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and –.

m. Set:

A TRIGGER COUPLING	LF REJ

n. CHECK—No stable display can be obtained at any TRIGGER LEVEL or TRIGGER SLOPE setting.

o. Set:

A TRIGGER COUPLING	AC
CH 1 VOLTS/DIV	10 mV

p. Adjust the generator for a 60-Hz, 5-division signal display (50 mV).

q. CHECK—For a stable display, with the A TRIGGER SLOPE switched to both + and – in each of the following A TRIGGER COUPLING switch positions: AC and DC.

18. Check A and B External Trigger Level Ranges

a. Set:

TRIGGER COUPLING (both)	AC
TRIGGER SLOPE (both)	+
CH 1 VOLTS/DIV	1 V
HORIZ DISPLAY	A
A TRIG MODE	AUTO
A TIME/DIV	1 ms
TRIGGER SOURCE (both)	EXT

b. Remove the 50-Ω termination from the external trigger input cable and adjust the generator for a 1-kHz, 4-division signal display (4 V).

c. CHECK—Display is triggered along the positive slope of the waveform as the A TRIGGER LEVEL control is rotated.

d. CHECK—Display is not triggered (free runs) at either extreme of the A TRIGGER LEVEL control's rotation.

e. Set:

A TRIGGER SLOPE	– (minus)

f. CHECK—Display is triggered along the negative slope of the waveform as the A TRIGGER LEVEL control is rotated.

g. CHECK—Display is not triggered (free runs) at either extreme of the A TRIGGER LEVEL control's rotation.

h. Move the test signal from the EXT A TRIGGER input to the EXT B TRIGGER input.

i. Set:

A TRIGGER LEVEL	Fully counterclockwise
HORIZ DISPLAY	B DLY'D

j. CHECK—Display is triggered along the positive slope of the waveform as the B TRIGGER LEVEL control is rotated.

k. CHECK—Display is not triggered (not visible) at either extreme of the B TRIGGER LEVEL control's rotation.

l. Set:

B TRIGGER SLOPE	– (minus)

m. CHECK—Display is triggered along the negative slope of the waveform as the B TRIGGER LEVEL control is rotated.

n. CHECK—Display is not triggered (not visible) at either extreme of the B TRIGGER LEVEL control's rotation.

o. Disconnect the test setup from the 468.

p. Set:

HORIZ DISPLAY	A
A TRIGGER SOURCE	EXT/10
CH 1 VOLTS/DIV	5 V
CH 1 VAR	Fully counterclockwise
A TRIGGER COUPLING	AC

q. Connect a 50-V, standard-amplitude calibrator square-wave signal via a 50-Ω bnc cable and a bnc T-connector to the CH 1 input. Connect the other T-connector output via a 50-Ω bnc cable to the EXT A TRIGGER input.

NOTE

The range of the A TRIGGER LEVEL control, with the A TRIGGER SOURCE switch set to EXT/10, is ±20 V (40 V p-p) or greater. The applied test signal is 50 V p-p. Therefore, untriggered operation at either rotation extreme of the A TRIGGER LEVEL control is not required.

r. CHECK—Display is triggered along the negative slope of the waveform as the A TRIGGER LEVEL control is rotated.

s. Set:

A TRIGGER SLOPE	+ (plus)

t. CHECK—Display is triggered along the positive slope of the waveform as the A TRIGGER LEVEL control is rotated.

u. Disconnect the test setup from the 468.

19. Check Line Triggers

a. Set:

CH 1 VOLTS/DIV	50 mV (with 10X probe)
A TRIGGER SOURCE	LINE
A TRIGGER LEVEL	0

b. Connect a 10X probe to the CH 1 input connector.

c. Place the 10X probe tip next to the ac-power cord.

d. Adjust the spacing and/or orientation of the probe with respect to the ac-power cord to obtain approximately 4 to 5 divisions of display amplitude.

e. CHECK—For a stable display, starting on the positive peak of the waveform.

f. Set:

A TRIGGER SLOPE	– (minus)

g. CHECK—For a stable display, starting on the negative peak of the waveform. Return the A TRIGGER SLOPE to +.

h. Disconnect the 10X probe from the 468.

20. Check NORM A Triggering Mode

a. Set:

A TIME/DIV	1 ms
CH 1 VOLTS/DIV	0.5 V
CH 1 VOLTS/DIV VAR	Calibrated detent
A TRIGGER SOURCE	NORM

b. Connect 0.1-s time markers via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input.

c. CHECK—Display can be triggered by adjusting the A TRIGGER LEVEL control.

d. Set:

A TRIG MODE	NORM

e. CHECK—Display is triggered.

f. Set:

CH 1 AC-GND-DC	GND

g. CHECK—No display or trace is visible.

21. Check AUTO Recovery Time

a. Set:

CH 1 AC-GND-DC	DC
A TRIG MODE	AUTO

b. CHECK—Display is triggered.

c. Set the generator for 0.5-s time markers.

d. CHECK—Display cannot be triggered (free runs).

e. Disconnect the test equipment from the 468.

HORIZONTAL

Equipment Required (see Table 4-1)

4. Test Oscilloscope
5. Calibration Generator
   a. Stanrdard-Amplitude Calibrator
6. Leveled Sine-Wave Generator
7. Time-Mark Generator
12. 50-Ω Bnc Cable
19. Dual-Input Coupler
24. 50-Ω Bnc Termination
25. 3-in., Flat-Bit Screwdriver
26. Low-Capacitance Alignment Tool

See ADJUSTMENT LOCATIONS 1 *and* [redacted] *in this Volume for test point and adjustment locations.*

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER Switch	ON (button in)

CRT

INTENSITY	As desired
FOCUS	Best focused display
SCALE	As desired
B INTENSITY	Midrange

Vertical (CH 1 and CH 2)

VOLTS/DIV	0.5 V
VOLTS/DIV VAR	Calibrated detent
POSITION	Midrange
AC-GND-DC	DC
VERT MODE	CH 1
INVERT	Off (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Triggering (A and B if applicable)

A TRIG MODE	Auto
TRIGGER LEVEL	For a stable display
TRIGGER SLOPE	+ (plus)
TRIGGER COUPLING	AC
A TRIGGER SOURCE	EXT
B TRIGGER SOURCE	STARTS AFTER DELAY
A TRIGGER HOLDOFF	NORM

Sweep (A and B)

HORIZ DISPLAY	ALT
DELAY TIME POSITION	1.00
A TIME/DIV	1 ms
B TIME/DIV	5 μs
TIME/DIV VAR	Calibrated detent
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange
TRACE SEP	As needed for ALT HORIZ DISPLAY trace separation

Digital Storage

NON STORE	On (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check/Adjust Sweep Start and A-Sweep Calibration (R970 and R173)

a. Connect 1-ms time markers via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input. Connect the generator trigger output via a 50-Ω bnc cable and a 50-Ω bnc termination to the EXT A TRIGGER input.

b. CHECK—Intensified portion of the A sweep begins at the 2nd time marker. It may be necessary to readjust the INTENSITY and B INTENSITY controls so that the intensified portion of the sweep is visible.

c. ADJUST—Sweep Start (R970) so that intensified portion of the A sweep begins at the start of the 2nd time marker, and the pulse displayed on the B DLY'D sweep starts at the beginning of the sweep.

d. Set:

DELAY TIME POSITION 9.00

e. CHECK—Intensified portion of the sweep begins at the 10th time marker.

f. ADJUST—A SWP Cal (R173) so that intensified portion of the A sweep begins at the start of the 10th time marker, and the pulse displayed on the B DLY'D trace starts at the beginning of the sweep. See preceding Figure 4-3 for location of adjustment access holes through the Storage Display circuit board.

g. INTERACTION—Set the DELAY TIME POSITION dial to 1.00 and repeat parts c through f of this step until no further improvement is observed.

2. Check Delay or Differential Time Linearity

a. Set the DELAY TIME POSITION dial to position the B sweep display of the 10th time marker to the beginning of the sweep.

b. Note the reading on the DELAY TIME POSITION dial.

c. Adjust the DELAY TIME POSITION dial so that the B sweep display of the 9th time marker is positioned to the beginning of the sweep. Note the dial reading.

d. CHECK—DELAY TIME POSITION dial for a difference in reading of 1.00 ±0.01 (0.99 to 1.01), for ambient temperatures from +15°C to +35°C. For ambient temperatures outside the range of +15°C to +35°C, but within the range of −15°C to +55°C, the dial-reading difference must be within 1.00 ±0.03 (0.97 to 1.03).

NOTE

One division on the DELAY TIME POSITION dial is equal to one complete revolution of the inner knob. One minor division on the inner knob is equal to 0.01 division on the DELAY TIME POSITION dial.

e. Rotate the DELAY TIME POSITION dial to position each successive time marker to the beginning of the sweep. Note the dial reading at each marker.

f. CHECK—DELAY TIME POSITION dial for a difference in reading between each successive time marker of 1.00 ±0.01 (0.99 to 1.01), for ambient temperatures from +15°C to +35°C. For ambient temperatures outside the range of +15°C to +35°C, but within the range of −15°C to +55°C, the dial-reading difference must be within 1.00 ±0.03 (0.97 to 1.03).

3. Check/Adjust Horizontal Amplifier Gain (R571 and R572)

a. Set:

HORIZ DISPLAY	A
TIME/DIV (both)	1 ms
DELAY TIME POSITION	Fully counterclockwise

b. Set the generator for 1-ms time markers.

c. Align the 1st time marker with the 1st vertical graticule line.

d. CHECK—Display for 1 marker per division ±2% (±0.2 division at the 11th time marker).

e. ADJUST—X1 Gain (R572) for exactly 1 marker per division.

f. Set the generator for 0.1-ms time markers.

g. Press in the X10 MAG push button (X10 MAG LED should light).

h. Align a time marker with the 1st vertical graticule line.

i. CHECK–For 1 marker per division ±3% (±0.3 division at the 11th time marker).

j. ADJUST–X10 Gain (R571) for exactly 1 time marker per division.

4. Check Sweep Linearity

a. CHECK–Linearity over any 2 divisions of the magnified sweep is within ±0.1 division.

b. Release the X10 MAG push button.

c. Set the generator for 1-ms time markers.

d. CHECK–Linearity over any 2 divisions of the sweep is within ±0.1 division.

5. Check/Adjust Magnifier Centering and Registration (R551 and R578)

a. Press in the X10 MAG push button.

b. Press and hold in the BEAM FIND push button.

c. CHECK–Display is centered horizontally.

d. ADJUST–Horizontal DC Centering (R551) to horizontally center the display with the BEAM FIND push button held in.

e. Release the BEAM FIND push button.

f. Release the X10 MAG push button.

g. Set the generator for 5-ms time markers.

h. Position the middle time marker to the center vertical graticule line.

i. Press in the X10 MAG push button.

j. Position the displayed time marker to the center vertical graticule line.

k. Release the X10 MAG push button.

l. CHECK–Middle time marker is within 0.2 division of the center vertical graticule line.

m. ADJUST–Magnifier Registration (R578) to position the middle time marker to the center vertical graticule line.

n. Repeat parts i through m of this step until no horizontal shift is observed between X10 MAG on and X10 MAG off.

6. Check/Adjust B-Sweep Calibration (R169)

a. Set:

DELAY TIME POSITION	Fully counterclockwise
HORIZ DISPLAY	B DLY'D
A TIME/DIV	2 ms
B TIME/DIV	1 ms
X10 MAG	Off (button out)

b. Set the generator for 1-ms time markers.

c. CHECK–Display for 1 time marker per division ±2% (±0.2 division at the 11th time marker).

d. ADJUST–B SWP Cal (R169) for exactly 1 time marker per division. See preceding Figure 4-3 for location of adjustment access holes through the Storage Display circuit board.

7. Check A-Sweep Length

a. Set:

HORIZ DISPLAY	A
TIME/DIV (both)	1 ms

b. Set the generator for 5-ms time markers.

c. Position the 3rd time marker horizontally to the center vertical graticule line.

d. CHECK—Trace extends to the right of the center vertical graticule line by 1 division ±0.5 division.

8. Check Variable Time/Division

a. Set:

A TIME/DIV	2 ms

b. Set the generator for 5-ms time markers.

c. Rotate the TIME/DIV VAR control fully counterclockwise (UNCAL LED should light).

d. CHECK—Display for 1 or more time markers per division.

e. Return the VAR control to the calibrated detent.

9. Check Horizontal POSITION Range

a. Rotate the Horizontal POSITION control fully clockwise.

b. CHECK—Start of sweep is to the right of the center vertical graticule line.

c. Rotate the Horizontal POSITION control fully counterclockwise.

d. CHECK—End of sweep is to the left of the center vertical graticule line.

NOTE

Horizontal POSITION control is a combined Coarse and Fine position control mounted on the same shaft in a mechanical arrangement that allows the Fine position potentiometer to rotate approximately 1/4 turn (1/8 turn in either direction from midrange) before the Coarse position control potentiometer is engaged.

e. Return the Horizontal POSITION control to midrange.

f. Rotate the Horizontal POSITION control through its Fine range.

g. CHECK—Horizontal POSITION control Fine range will move the display position approximately 1 horizontal division.

10. Check/Adjust the A-Sweep 10-μs Timing (C120)

a. Set:

DELAY TIME POSITION	1.00
A TIME/DIV	10 μs
B TIME/DIV	1 μs

b. Set the generator for 10-μs time markers.

c. Align the 1st time marker with the 1st vertical graticule line.

d. CHECK—Display for 1 time marker per division ±2% (±0.2 division at the 11th time marker).

e. ADJUST—10-μs Timing (C120), with a low-capacitance alignment tool, for exactly 1 time marker per division. See preceding Figure 4-3 for location of adjustment access holes through the Storage Display circuit board.

f. Set:

HORIZ DISPLAY	B DLY'D
B TRIGGER SOURCE	STARTS AFTER DELAY

g. Horizontally position the displayed marker to align it with a vertical graticule line. The selected line is then used as a reference point in part i.

h. Set:

DELAY TIME POSITION	9.00

i. ADJUST—10-μs Timing (C120), with a low-capacitance alignment tool, to align the displayed marker with the same vertical graticule line selected in part g.

j. Set the DELAY TIME POSITION dial to 1.00 and repeat parts g through i until no error exists between a DELAY TIME POSITION dial setting of 1.00 and 9.00.

11. Check/Adjust A-Sweep High-Speed Timing (C126)

a. Set:

DELAY TIME POSITION	1.50
A TIME/DIV	0.5 μs
B TIME/DIV	0.05 μs
HORIZ DISPLAY	A

b. Set the generator for 0.5-μs time markers.

c. Align the 1st time marker with the 1st vertical graticule line.

d. CHECK—Display for 1 time marker per division ±2% (±0.2 division at the 11th time marker).

e. ADJUST—A-SWP High-Speed Timing (C126), with a low-capacitance alignment tool, for exactly 1 time marker per division. See preceding Figure 4-3 for adjustment access holes.

f. Set:

HORIZ DISPLAY	B DLY'D

g. Use the Horizontal POSITION control to align the displayed marker with the center vertical graticule line.

h. Set:

DELAY TIME POSITION	8.50

i. CHECK—Displayed time marker aligns with the center vertical graticule line.

j. ADJUST—The A-SWP High-Speed Timing (C126), with a low-capacitance alignment tool, to align the displayed marker with the center vertical graticule line.

k. INTERACTION—Readjust C126 as necessary to obtain the correct timing between the 1.50 and 8.50 settings of the DELAY TIME POSITION dial (within 2%). A compromise in the adjustment may be necessary. Set HORIZ DISPLAY to A and DELAY TIME POSITION to 1.50, then repeat parts c through j until no improvement in timing accuracy is obtained.

12. Check/Adjust B-Sweep High-Speed Timing (C159)

a. Set:

DELAY TIME POSITION	Fully counterclockwise
HORIZ DISPLAY	B DLY'D
B TRIGGER SOURCE	NORM
A TIME/DIV	1 μs
B TIME/DIV	0.5 μs

b. Adjust both the A and B TRIGGER LEVEL controls for a stable display.

c. Align the 1st time marker with the 1st vertical graticule line.

d. CHECK—Display for 1 time marker per division ±2% (±0.2 division at the 11th time marker).

e. ADJUST—B-SWP High-Speed Timing (C159), with a low-capacitance alignment tool, for exactly 1 time marker per division. See preceding Figure 4-3 for adjustment access holes.

13. Check A and B TIME/DIV Accuracy

a. CHECK—B-Sweep timing is within 0.2 division, over the full 10 divisions of the display, for each of the B TIME/DIV switch settings and time-mark generator settings listed in Table 4-18. Align the 1st time marker with the 1st vertical graticule line at each setting.

b. Set:

HORIZ DISPLAY	A
A TRIG MODE	Auto

c. CHECK—The A-Sweep timing is within 0.2 division over the full 10 divisions of the display, for each of the A TIME/DIV switch settings and time-mark generator settings listed in Table 4-18. Align the 1st time marker with the 1st vertical graticule line at each setting.

Table 4-18

A and B Timing Accuracy

A and B TIME/DIV Switch Setting	Time-Mark Generator Setting
0.02 μs	20 ns
0.05 μs	50 ns
0.1 μs	0.1 μs
0.2 μs	0.2 μs
0.5 μs	0.5 μs
1 μs	1 μs
2 μs	2 μs
5 μs	5 μs
10 μs	10 μs
20 μs	20 μs
50 μs	50 μs
0.1 ms	0.1 ms
0.2 ms	0.2 ms
0.5 ms	0.5 ms
1 ms	1 ms
2 ms	2 ms
5 ms	5 ms
10 ms[a]	10 ms
20 ms[a]	20 ms
50 ms[a]	50 ms
A Sweep Only	
0.1 s[a]	0.1 s
0.2 s[a]	0.1 s
0.5 s[a]	0.5 s

[a]Switch A TRIG MODE to NORM below 5 ms/division.

14. Check/Adjust High-Speed Magnified Timing (C548 and C549)

a. Set:

HORIZ DISPLAY	A
X10 MAG	On (button in)
Horizontal POSITION	Midrange (as required)
TIME/DIV (both)	0.05 μs
A TRIG MODE	AUTO

b. Set the generator for 5-ns time markers.

c. Set CH 1 VOLTS/DIV switch for at least a 4-division display amplitude.

d. Align the 1st time marker with the 1st vertical graticule line.

e. CHECK—Display for 1 time marker per division ±3% (±0.3 division at the 11th time marker).

f. ADJUST—C548 and C549 equally to obtain 1 time marker per division over the entire 10 divisions.

g. Set:

TIME/DIV (both) 0.02 μs

h. Press and hold in BEAM FIND push button.

i. CHECK—Display is centered horizontally.

j. ADJUST—Horizontal DC Centering (R551), if necessary, to horizontally center the compressed display. Release the BEAM FIND push button.

k. INTERACTION—If R551 is adjusted, recheck Magnifier Registration (step 5, parts g through n).

l. ADJUST—C548 for 2 time markers per 5 divisions over the entire 10 divisions. Adjust Horizontal POSITION control as necessary to align markers.

m. Set:

TIME/DIV (both) 0.05 μs

n. ADJUST—C549 for 1 time marker per division over the entire 10 divisions.

o. Repeat part g and parts l through n for best timing for both the 0.05-μs and the 0.02-μs TIME/DIV switch settings until no further improvement is noted.

15. Check A and B Magnified Timing Accuracy

a. CHECK—The A magnified sweep timing is within 0.3 division over the center 10 divisions of the magnified display for each A TIME/DIV switch setting and time-mark generator setting listed in Table 4-19. Note the portions of the total magnified sweep length to be excluded from the measurement.

Table 4-19

A and B Magnified Accuracy

A and B TIME/DIV Switch Setting	Time-Mark Generator Setting	Magnified Sweep Portions to Exclude
0.02 μs	2 ns	First and last 25 divisions
0.05 μs	5 ns	First and last 10 divisions
0.1 μs	10 ns	First and last 5 divisions
0.2 μs	20 ns	First and last 2.5 divisions
0.5 μs	50ns	First 2 divisions
1 μs 2 μs 5 μs	0.1 μs 0.2 μs 0.5 μs	
10 μs 20 μs 50 μs	1 μs 2 μs 5 μs	
0.1 ms 0.2 ms 0.5 ms	10 μs 20 μs 50 μs	
1 ms 2 ms 5 ms	0.1 ms 0.2 ms 0.5 ms	
10 ms[a] 20 ms[a] 50 ms[a]	1 ms 2 ms 5 ms	
A Sweep Only		
0.1 s[a] 0.2 s[a] 0.5 s[a]	10 ms 20 ms 50 ms	

[a]Switch TRIG MODE to NORM below 5 ms/division.

b. Set:

HORIZ DISPLAY	B DLY'D

c. CHECK—The B magnified sweep timing is within 0.3 division over the center 10 divisions of the magnified sweep for each B TIME/DIV switch setting and time-mark generator setting listed in Table 4-19. Note the portions of the total magnified sweep length to be excluded from the measurement.

d. Release the X10 MAG push button.

16. Check Delay or Differential Time Accuracy

a. Set:

B TRIGGER SOURCE	STARTS AFTER DELAY
A TRIG MODE	AUTO
TIME/DIV (both)	According to Table 4-20
HORIZ DISPLAY	ALT

b. CHECK—Differential time accuracy is within ±8 minor dial divisions of the DELAY TIME POSITION control for each A TIME/DIV switch setting, B TIME/DIV switch setting, and time-mark generator setting listed in Table 4-20. Use the following procedure to make this check.

Rotate the DELAY TIME POSITION dial to 1.00 and readjust it slightly until the sweep starts at the top of the 2nd time marker. Note the dial reading. Then, rotate the dial to 9.00 and readjust it slightly until the sweep starts at the top of the 10th time marker. The DELAY TIME POSITION dial setting must be 8.00 divisions ±0.08 division higher than the dial reading noted previously.

NOTE

Below 5 ms/division the ALT HORIZ DISPLAY traces switch too slowly to observe the display with ease; therefore, set HORIZ DISPLAY to B DLY'D. If in doubt as to the correct setting of the DELAY TIME POSITION dial, set the HORIZ DISPLAY switch to A INTEN and check which marker is intensified.

17. Check Delay or Differential Time Jitter

a. Set:

DELAY TIME POSITION	1.00
HORIZ DISPLAY	B DLY'D
A TIME/DIV	1 ms
B TIME/DIV	0.2 μs
A TRIG MODE	AUTO

b. Set the generator for 1-ms time markers.

Table 4-20

Differential Time Accuracy

A TIME/DIV Switch Setting	B TIME/DIV Switch Setting	Time-Mark Generator Setting
0.1 μs	0.02 μs	0.1 μs
0.2 μs	0.05 μs	0.2 μs
0.5 μs	0.05 μs	0.5 μs
1 μs	0.1 μs	1 μs
2 μs	0.2 μs	2 μs
5 μs	0.5 μs	5 μs
10 μs	1 μs	10 μs
20 μs	2 μs	20 μs
50 μs	5 μs	50 μs
0.1 ms	10 μs	0.1 ms
0.2 ms	20 μs	0.2 ms
0.5 ms	50 μs	0.5 ms
1 ms	0.1 ms	1 ms
2 ms	0.2 ms	2 ms
5 ms	0.5 ms	5 ms
10 ms[a]	1 ms	10 ms
20 ms[a]	2 ms	20 ms
50 ms[a]	5 ms	50 ms
0.1 s[a]	10 ms	0.1 s
0.2 s[a]	20 ms	0.2 s
0.5 s[a]	50 ms	0.5 s

[a]**Below 5 ms/division, set HORIZ DISPLAY to B DLY'D and A TRIG MODE to NORM.**

c. Position the time marker to a point near the center vertical graticule line, using the DELAY TIME POSITION dial.

d. CHECK—Jitter on the leading edge of the time marker should not exceed 1 division (2.5 divisions if the instrument is being operated on a 50-Hz or below line frequency). Disregard the slow drift.

e. Rotate the DELAY TIME POSITION dial to 9.00 and readjust it slightly so the time marker is displayed near the center vertical graticule line.

f. CHECK—Jitter on the leading edge of the time marker should not exceed 1 division (2.5 divisions if the instrument is being operated on a 50-Hz or below line frequency). Disregard the slow drift.

g. Disconnect test equipment from the 468.

18. Check/Adjust X-Gain (R681)

a. Set:

TIME/DIV (both)	X-Y
VOLTS/DIV (both)	5 mV
CH 1 AC-GND-DC	AC
CH 2 AC-GND-DC	GND
HORIZ DISPLAY	A
A TRIGGER SOURCE	NORM

NOTE

Setting the A TIME/DIV switch to X-Y disables all VERT MODE switch selections and automatically selects the CH 1 input for the X-Axis signal and the CH 2 input for the Y-Axis signal. However, for firmware version 1.0, the CH 1 and CH 2 VERT MODE push buttons must be pressed in to illuminate the scale-factor LED behind the VOLTS/DIV knob skirts.

b. Connect a 20-mV, standard-amplitude square-wave signal via a 50-Ω, unterminated bnc cable to the CH 1 input.

c. CHECK—Display for 4 divisions of horizontal deflection ±4% (3.84 to 4.16 divisions).

d. Set:

CH 1 AC-GND-DC	DC

e. CHECK—Display for 4 divisions of horizontal deflection ±4% (3.84 to 4.16 divisions).

f. Set:

CH 1 AC-GND-DC	AC

g. ADJUST—X-Gain (R681) for exactly 4 divisions of horizontal deflection.

h. Disconnect test equipment from the 468.

19. Check X-Y Phasing and Bandwidth

a. Connect a 50-kHz, leveled sine-wave signal via a 50-Ω bnc cable, a 50-Ω termination, and a dual-input coupler to the CH 1 and CH 2 inputs.

b. Adjust the generator to obtain an 8-division horizontal display.

c. Set:

CH 2 AC-GND-DC	AC

d. Center the display both vertically and horizontally using the Horizontal POSITION and CH 2 Vertical POSITION controls.

e. CHECK—Display for an X-Axis elipse dimension at the center horizontal graticule line of 0.4 division or less.

f. Set:

CH 2 AC-GND-DC	GND

g. Adjust the generator to obtain a 10-division horizontal display.

h. Increase the sine-wave frequency until the display reduces to 7 divisions.

i. CHECK—Output frequency of the leveled sine-wave generator is at least 4 MHz.

j. Disconnect test equipment from the 468.

20. Check B Ends A

a. Set:

HORIZ DISPLAY	A INTEN
A TIME/DIV	1 ms
B TIME/DIV	0.1 ms
A TRIGGER HOLDOFF	B ENDS A (in detent)

b. Adjust both the INTENSITY and B INTENSITY controls for a visible intensified portion of the trace.

c. Rotate the DELAY TIME POSITION dial through its entire range.

d. CHECK—The A sweep ends after the intensified portion at all settings of the DELAY TIME POSITION dial.

21. Check A Trigger Holdoff

a. Set:

HORIZ DISPLAY	A
A TRIGGER HOLDOFF	NORM
A TRIGGER LEVEL	Fully clockwise

b. Connect the A + GATE output signal (from the 468 rear panel) via a 50-Ω, unterminated bnc cable to the input of the test oscilloscope.

c. Set the test oscilloscope Time/Div switch and Var control so that the bottom portion of the waveform (holdoff time of the A + GATE is exactly 1 horizontal division.

d. Rotate the A TRIGGER HOLDOFF control clockwise.

e. CHECK—For at least a 10-times increase in the holdoff time of the A + GATE.

f. Disconnect test equipment from the 468.

GATES, CALIBRATOR, AND EXT Z-AXIS

Equipment Required (see Table 4-1)

2. Digital Voltmeter
4. Test Oscilloscope
5. Calibration Generator
   a. Standard-Amplitude Calibrator
12. 42-in., 50-Ω Bnc Cable (2 required)
20. Bnc T-Connector
24. 50-Ω Bnc Termination
25. 3-in., Flat-Bit Screwdriver
27. Shorting Strap

See ADJUSTMENT LOCATIONS 1 *in this Volume for test point and adjustment locations.*

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER Switch	ON (button in)

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired
B INTENSITY	As desired

Vertical (CH 1 and CH 2)

VOLTS/DIV	5 mV
VOLTS/DIV VAR	Calibrated detent
POSITION	Midrange
VERT MODE	CH 1
INVERT	Off (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Triggering (A and B if applicable)

TRIGGER LEVEL	Fully clockwise
TRIGGER SLOPE	+
TRIGGER COUPLING	AC
A TRIGGER SOURCE	NORM
B TRIGGER SOURCE	STARTS AFTER DELAY
A TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep (A and B)

HORIZ DISPLAY	B DLY'D
DELAY TIME POSITION	Fully counterclockwise
TIME/DIV (both)	50 μs
TIME/DIV VAR	Calibrated detent
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

NON STORE	On (button in)
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check A and B + GATES

a. Connect the B + GATE output (from the 468 rear panel) via a 50-Ω, unterminated bnc cable to the test oscilloscope input.

b. Set test oscilloscope controls:

Vert Mode	CH 1
Ch 1 Volts/Div	1 V
A Time/Div	50 μs
A Trigger Slope	– (minus)
Horiz Display	A
Ac-Gnd-Dc	Dc

c. CHECK—Test oscilloscope display for a positive-going square wave of approximately +5.5 V in amplitude (starting within 500 mV of 0 V).

d. Move the bnc cable from the B + GATE connector to the A + GATE connector.

e. CHECK—Test oscilloscope display for a positive-going square wave of approximately +5.5 V in amplitude (starting within 500 mV of 0 V).

f. Disconnect test equipment from the 468.

2. Check/Adjust Calibrator DC Level (R599)

a. Connect a shorting strap between TP474 and TP475 on the Interface circuit board (A15).

b. Connect the digital voltmeter Low lead to chassis ground and connect the Volts lead to the CALIBRATOR current loop.

c. CHECK—CALIBRATOR dc level is 300 mV ±1% (297 to 303 mV).

d. ADJUST—Amplitude Cal (R599) for a digital voltmeter reading of exactly 300 mV.

e. Remove the shorting strap and digital voltmeter connections.

f. Connect a 10X probe from the test oscilloscope to the CALIBRATOR current loop.

g. Set test oscilloscope controls:

Ch 1 Volts/Div	0.1 V
Time/Div	0.5 μs
A Trigger Slope	+ (plus)

h. CHECK—Test oscilloscope display for a 0.3-V, positive-going square-wave signal (typical square-wave period is approximately 1 ms).

i. Disconnect the test setup.

3. Check External Z-Axis

a. Set:

HORIZ DISPLAY	A
A TIME/DIV	0.2 ms
A TRIGGER SOURCE	EXT

b. Set the INTENSITY control for a normal viewing level.

c. Connect a 5-V, standard-amplitude calibration signal via a 50-Ω bnc cable and T-connector to the EXT A TRIGGER input. Connect the other output of the T-connector via a 50-Ω cable to the EXT Z-AXIS input (on the 468 rear panel).

d. Adjust the A TRIGGER LEVEL control to obtain a stable display (TRIG LED illuminated).

e. CHECK—Trace has noticeable intensity modulation.

f. Disconnect the amplitude calibration signal from the T-connector.

g. Set:

A TIME/DIV	0.02 μs

h. Connect a 5-V, 50-MHz leveled sine-wave signal via a 50-Ω bnc cable and a 50-Ω termination to the T-connector.

i. CHECK—Trace has noticeable intensity modulation.

j. Disconnect the test equipment from the 468.

STORAGE POWER SUPPLY

Equipment Required (see Table 4-1)

2. Digital Voltmeter

4. Test Oscilloscope

See ADJUSTMENT LOCATIONS *in this Volume for test point and adjustment locations.*

NOTE

If commencing the Adjustment Procedure at this point, prior to applying power to the 468 make the initial control settings. Then, connect the 468 to an appropriate ac-power source. Apply power to the instrument and test equipment and allow a 20-minute warmup period before commencing the adjustments and checks.

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER	See preceding NOTE

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2)

VOLTS/DIV	5 mV
VOLTS/DIV VAR	Calibrated detent
VERT MODE	CH 1
POSITION	Midrange
AC-GND-DC	GND
INVERT	Normal (button out)
20 MHz BW LIMIT	Full Bandwidth (button out)

Trigger (A and B)

COUPLING	AC
SLOPE	+
LEVEL	For a stable display
SOURCE	NORM
A TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep (A and B if applicable)

HORIZ DISPLAY	A
TIME/DIV	1 ms
TIME/DIV VAR	Calibrated detent
DELAY TIME POSITION	Fully counterclockwise
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

STORAGE MODE	NORM
SAVE REF	Off (button out)
CURSOR FUNCTION	Both off (buttons out)

1. Check Power Supply DC Level and Ripple

a. Connect the Low lead of the digital voltmeter to chassis ground and connect the Volts lead to the first test point listed in Table 4-21.

b. CHECK—Voltage level is within the range given in Table 4-21.

c. Repeat parts a and b for each test point in Table 4-21.

d. Disconnect the digital voltmeter Volts lead from the 468, then disconnect the Low lead from chassis ground.

e. Connect a test oscilloscope 10X probe ground lead to chassis ground and connect the probe tip to TP315.

f. Set the test oscilloscope controls as follows:

Vert Mode	Ch 1
Ch 1 Ac-Gnd-Dc	Ac
Volts/Div	50 mV (with 10X probe attached)

g. Obtain a stable display on the test oscilloscope.

h. CHECK—For a display of **3 divisions** or less of p-p amplitude.

i. Disconnect the probe tip from TP315, then disconnect the probe ground lead from the 468.

Table 4-21

Digital Storage Power Supply Limits

Power Supply	Test Point	Reading	Tolerance
+12 VS	TP148	+11.4 to +12.6 V	±5%
+5 VS	TP315	+4.8 to +5.2 V	±4%
−12 VS	TP520	−11.4 to −12.6 V	±5%
−6 VS	TP518	−5.76 to −6.24 V	±4%

STORAGE VERTICAL

Equipment Required (see Table 4-1)

5. Calibration Generator
   a. Standard-Amplitude Calibrator
   b. Fast-Rise Square-Wave Generator
6. Leveled Sine-Wave Generator
7. Time-Mark Generator
12. 42-in., 50-Ω Bnc Cable (2 required)
19. Dual-Input Coupler
23. 2X, 50-Ω Bnc Attenuator
24. 50-Ω Bnc Termination
25. 3-in., Flat-Bit Screwdriver
26. Low-Capacitance Alignment Tool

See ADJUSTMENT LOCATIONS 2, ADJUSTMENT LOCATIONS 6, ADJUSTMENT LOCATIONS 7, *and* ADJUSTMENT LOCATIONS 8 *in this Volume for test point and adjustment locations.*

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER	ON

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2)

VERT MODE	CH 1
VOLTS/DIV	5 mV
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC	GND
POSITION	Midrange
INVERT	Off (button out)

Trigger (A and B)

COUPLING	AC
SLOPE	+
LEVEL	For a stable, triggered display
SOURCE	NORM
A TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep (A and B if applicable)

HORIZ DISPLAY	A
TIME/DIV	5 μs
TIME/DIV VAR	Calibrated detent
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

STORAGE MODE	NORM
CURSOR FUNCTION	Both off (buttons out)
STORAGE WINDOW	POST TRIG (button out)
DISPLAY RESPONSE	SINE (button in)
SAVE REF	Off (button out)

1. Check VOLTS Cursor Operation

a. Set:

CURSOR FUNCTION	VOLTS

b. Use the CH 1 Vertical POSITION control to move the baseline trace out of the graticule area.

c. Press in the POWER push button to turn off the 468 then press it in again to reapply power. Power-on self-test will operate.

d. CHECK—Two horizontal VOLTS cursors appear within the graticule area. One is a solid line, and the other is a dashed line.

NOTE

The CURSOR control knob has two operating modes. In its linear region, the knob rotates freely about 1/4 turn. At either end of its free rotation range, spring-stop switches increase resistance to movement of the knob, and cursor displacement becomes a function of how long the spring stop is held open. As the control knob is rotated further into the rate region, cursor displacement rate within the graticule area increases.

e. CHECK—Rotating the CURSOR control knob through its linear region positions the dashed cursor vertically about 1 division.

f. Rotate the CURSOR control knob counterclockwise into the rate region (against the spring tension).

g. CHECK—Dashed cursor moves downward past the bottom of the graticule area.

h. Rotate the CURSOR control knob clockwise into its rate region.

i. CHECK—Dashed cursor moves upward past the top of the graticule area.

j. Rotate the CURSOR control knob counterclockwise into its rate region.

k. CHECK—Dashed cursor is positioned more rapidly as the CURSOR control knob is rotated further into the rate region. Position the dashed cursor near the solid cursor.

l. Press in the CURSOR SELECT push button.

m. CHECK—Previous solid cursor becomes the dashed cursor, and the dashed cursor becomes the solid cursor.

n. Use the CURSOR control knob and CURSOR SELECT push button to position the VOLTS cursors 6 divisions apart on the graticule.

2. Check COUPLED V/T Cursor Operation

a. Set:

CURSOR FUNCTION	TIME only
VERT MODE	CH 2
CH 2 AC-GND-DC	AC

b. Connect a 50-kHz, leveled sine wave via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 2 input.

c. Set the generator output for a 4-division display amplitude. Adjust the A TRIGGER LEVEL control as necessary for a stable display.

d. Set:

STORAGE MODE	SAVE

e. Adjust the INTENSITY control for a visible display of the TIME dots on the waveform.

f. Press in the VOLTS CURSOR FUNCTION push button (both VOLTS and TIME push buttons are in for the COUPLED V/T CURSOR FUNCTION).

g. CHECK—Dashed VOLTS cursor becomes coupled to the active TIME dot, and the solid cursor is coupled to the fixed TIME dot.

h. Rotate the CURSOR control knob to position the active TIME dot to both ends of the display.

i. CHECK—Dashed VOLTS cursor remains coupled to the active TIME dot as the TIME dot is positioned to both ends of the display.

j. Press in the CURSOR SELECT push button.

k. CHECK—Previously active coupled cursors become fixed, and fixed cursors become the active cursors.

l. Press in the TIME CURSOR FUNCTION push button to release the COUPLED V/T CURSOR FUNCTION.

m. CHECK—VOLTS cursors return to the positions to which they were set in part n of step 1 (6 divisions apart).

n. Disconnect the test equipment from the 468.

3. Check/Adjust Storage Vertical Centering (R345)

a. Set:

STORAGE MODE	SAVE
CURSOR FUNCTION	Both off (buttons out)

b. Press in POWER switch twice. Power-on self-test will run.

c. CHECK—Horizontal dashed line that appears is vertically centered within 0.2 division of the center horizontal graticule line.

d. ADJUST—Vertical Display Centering (R345, ADJUSTMENT LOCATIONS 6) to align the dashed line with the center horizontal graticule line.

4. Check/Adjust Storage Vertical Gain (R571)

a. Set:

VERT MODE	CH 1
VOLTS/DIV (both)	0.5 mV
CURSOR FUNCTION	VOLTS
STORAGE MODE	NORM
AC-GND-DC (both)	GND

b. Use the CURSOR control to position the active cursor (dashed line) 3 divisions below the center horizontal graticule line.

c. Press in the CURSOR SELECT push button and use the CURSOR control to position the 2nd cursor 3 divisions above the center horizontal graticule line for an exact 6-division difference between the two VOLTS cursors.

d. CHECK—Volts readout accuracy is within the limits listed in Table 4-22 for each VOLTS/DIV switch setting. The red scaling LED should be illuminated.

e. Rotate the VOLTS/DIV VAR control out of the calibrated detent. The seven-segment display readout should be within 5.88 to 6.12, and the DIV scaling LED should illuminate.

f. Return the VAR control to the calibrated detent.

Table 4-22

VOLTS Cursor Readout Accuracy

VOLTS/DIV Switch Setting	2% Readout Tolerance
0.5 mV	2.940 to 3.060 mV
1 mV	5.88 to 6.12 mV
2 mV	11.76 to 12.24 mV
5 mV	29.40 to 30.60 mV
10 mV	58.8 to 61.2 mV
20 mV	117.6 to 122.4 mV
50 mV	294.0 to 306.0 mV
0.1 V	0.588 to 0.612 V
0.2 V	1.176 to 1.224 V
0.5 V	2.940 to 3.060 V
1 V	5.88 to 6.12 V
2 V	11.76 to 12.24 V
5 V	29.40 to 30.60 V

g. Set:

VERT MODE	CH 2

h. Repeat parts d through f for CH 2. If checks are within tolerance, skip to step 5. If they are not, continue with parts i through m of this step.

i. Set:

VOLTS/DIV	5 mV
VERT MODE	CH 1 only

j. Verify that the bottom cursor is positioned exactly 3 divisions below the center horizontal graticule line.

k. Press in the CURSOR SELECT push button.

l. Set the active cursor for a seven-segment LED display readout of 30.00 mV.

m. ADJUST—Vertical Display Gain (R571, ADJUSTMENT LOCATIONS 6) for exactly 6 vertical divisions of spacing between the VOLTS cursors.

n. INTERACTION—Vertical Display Centering and Vertical Display Gain interact slightly. Adjust R345 to align the VOLTS cursors with the horizontal graticule lines as you adjust R571 to obtain a 6-division difference between the VOLTS cursors. Repeat steps 3 and 4 until no improvement is noted.

5. Check/Adjust CH 1 and CH 2 Acquisition Gain (R335 and R420)

a. Set:

VOLTS/DIV	5 mV
VERT MODE	CH 1 only
AC-GND-DC (both)	DC
TIME/DIV	1 ms
CURSOR FUNCTION	Both off (buttons out)

b. Connect a 20-mV, standard-amplitude square-wave signal via a 50-Ω bnc cable to the CH 1 input connector.

c. CHECK—DC accuracy is within 3% for each of the VOLTS/DIV switch settings and standard-amplitude generator settings listed in Table 4-23. If the CH 1 DC accuracy is within tolerance, skip to part f. If it is not, continue with part d of this step.

d. Set the generator output for 20 mV and switch the CH 1 VOLTS/DIV switch to 5 mV per division.

Table 4-23

Storage DC Accuracy

CH 1 and CH 2 VOLTS/DIV Switch Setting	Standard-Amplitude Generator Setting	Vertical Deflection (Divisions)
5 mV	20 mV	3.88 to 4.12
10 mV	50 mV	4.85 to 5.15
20 mV	0.1 V	4.85 to 5.15
50 mV	0.2 V	3.88 to 4.12
0.1 V	0.5 V	4.85 to 5.15
0.2 V	1 V	4.85 to 5.15
0.5 V	2 V	3.88 to 4.12
1 V	5 V	4.85 to 5.15
2 V	10 V	4.85 to 5.15
5 V	20 V	3.88 to 4.12

NOTE

CH 1 and CH 2 Acquisition Gain adjustments (R335 and R420) are accessible through the gap between the bottom of the rear frame assembly and the bottom of the main frame. Use an insulated-shaft screwdriver or alignment tool to make the adjustments.

e. ADJUST—CH 1 Acquisition Gain (R335, ADJUSTMENT LOCATIONS 8) for exactly 4 divisions of display amplitude.

f. Set the generator output for 20 mV (if skipping from part c) and move the signal from the CH 1 input connector to the CH 2 input connector.

g. Set:

VERT MODE	CH 2 only

h. CHECK—DC accuracy is within 3% for each of the VOLTS/DIV switch settings and standard-amplitude generator settings listed in Table 4-23. If the CH 2 DC accuracy is within tolerance, skip to step 6. If it is not, continue with parts i and j of this step.

i. Set the generator output for 20 mV and switch the CH 2 VOLTS/DIV switch to 5 mV per division.

j. ADJUST—CH 2 Acquisition Gain (R420, ADJUSTMENT LOCATIONS 8) for exactly 4 divisions of display amplitude.

6. Check/Adjust CH 1 and CH 2 Acquisition Centering (R232 and R436)

a. Set:

VERT MODE	CH 1 and CH 2
AC-GND-DC	GND
VOLTS/DIV (both)	5 mV
NON STORE	On (button in)

b. Use the Channel Vertical POSITION controls to vertically center both the CH 1 and CH 2 baseline traces to the center horizontal graticule line.

c. Set:

STORAGE MODE	NORM

d. CHECK—Both CH 1 and CH 2 traces are within 0.5 division of the center horizontal graticule line. If the traces are within tolerance, skip to step 7. If they are not within tolerance, continue with the remainder of this step.

NOTE

CH 1 and CH 2 Trig DC Balance controls (R122 and R431) must be correctly adjusted before attempting to adjust CH 1 and CH 2 Acquisition Centering. Refer to "TRIGGERING" adjustments, step 5, given previously in this section of the manual. If the complete Adjustment Procedure is being performed, R122 and R431 are correctly adjusted. If only the Digital Storage Adjustment Procedure is being performed, the Trig DC Balance Adjustments must be checked and adjusted if necessary.

e. ADJUST—CH 1 Acquisition Centering (R232, ADJUSTMENT LOCATIONS 2) to align the CH 1 baseline trace with the center horizontal graticule line.

f. ADJUST—CH 2 Acquisition Centering (R436, ADJUSTMENT LOCATIONS 2) to align the CH 2 trace with the center horizontal graticule line (superimpose the CH 1 and CH 2 traces).

g. INTERACTION—CH 1 and CH 2 Acquisition Centering adjustments interact slightly with the CH 1 and CH 2 Acquisition Gain adjustments. Switch both AC-GND-DC switches to DC and repeat steps 5 and 6 until no improvement is noted.

h. Disconnect the test equipment from the 468.

7. Check 0.5 mV to 2.0 mV VOLTS Readout Accuracy

a. Set:

CURSOR FUNCTION	VOLTS (button in)
VOLTS/DIV (both)	2 mV
STORAGE MODE	NORM
AC-GND-DC (both)	DC
VERT MODE	CH 1

b. Use the CURSOR/NO. of SWEEPS control to position the dashed VOLTS cursor 3 divisions above the center horizontal graticule line. Press in the CURSOR SELECT push button to activate the other VOLTS cursor and position it 3 divisions below the center horizontal graticule line (exact 6-division difference between the cursors).

c. CHECK—Readout accuracy is within 3% for each of the VOLTS/DIV switch settings listed in Table 4-24.

d. Set:

VERT MODE	CH 2

e. Repeat part c using the CH 2 VOLTS/DIV switch.

Table 4-24

0.5 to 2.0 mV VOLTS Readout Accuracy

CH 1 and CH 2 VOLTS/DIV Switch Setting	LED Readout Accuracy
2 mV	11.64 to 12.36 mV
1 mV	5.82 to 6.18 mV
0.5 mV	2.910 to 3.090 mV

8. Check ADD Mode

a. Set:

VERT MODE	ADD
VOLTS/DIV (both)	5 mV

b. Connect a 10-mV, standard-amplitude square-wave signal via a 50-Ω bnc cable and a dual-input coupler to both the CH 1 and CH 2 input connectors.

c. Adjust the A TRIGGER LEVEL control for a stable display.

d. CHECK—Display amplitude is 4 divisions ±0.12 division (3.88 to 4.12 divisions). If the VOLTS cursors are used to make the measurement, the seven-segment LED readout should be within 19.4 to 20.6 mV.

e. Disconnect the test equipment from the 468.

9. Check NORM to SAVE Registration

a. Set:

VERT MODE	CH 1 only
AC-GND-DC (both)	GND

b. Use the Vertical POSITION control to align the trace with the center horizontal graticule line.

c. Press in the SAVE Storage Mode push button.

d. CHECK—Trace remains within 0.2 division of the center horizontal graticule line.

e. Set:

VERT MODE	CH 2 only
STORAGE MODE	NORM

f. Repeat parts b through d for CH 2.

10. Check/Adjust A/D Converter Compensation (R271)

a. Set:

VERT MODE	CH 1, CH 2, and CHOP
AC-GND-DC (both)	DC
A TRIGGER SOURCE	CH 1
STORAGE MODE	NORM
DISPLAY RESPONSE	PULSE
TIME/DIV (both)	2 μs

b. Connect a 1-MHz, fast-rise + square-wave signal via a 50-Ω bnc cable, 2X attenuator, and a 50-Ω bnc termination to the CH 1 input connector.

c. Set the generator output for a 6-division display amplitude.

d. Use the Vertical POSITION controls to vertically center both the CH 2 baseline trace and the CH 1 square-wave display.

e. CHECK—No vertical deflection appears on the CH 2 trace and overshoot on the CH 1 square-wave display is 3% or less (0.2 division or less).

NOTE

R271 is accessible through the gap between the bottom of the rear frame assembly and the bottom of the main frame.

f. ADJUST—A/D Converter Compensation (R271, ADJUSTMENT LOCATIONS 7) for minimum vertical deflection of the CH 2 baseline trace (typically zero deflection) using the following procedure:

1. Using an insulated-shaft screwdriver, adjust R271 fully clockwise.

2. Slowly adjust R271 counterclockwise until the CH 2 baseline trace is flat (no square-wave deflection).

NOTE

Excessive counterclockwise rotation of the adjustment will cause the CH 1 square-wave display to overshoot on the leading edge.

g. CHECK—Overshoot on CH 1 square-wave leading edge is 3% or less (0.2 division or less). If the overshoot exceeds 3%, repeat parts f and g until no further improvement is noted.

11. Check Display Response

a. Set:

VERT MODE	CH 1 only
A TRIGGER SOURCE	NORM
TIME/DIV	1 ms
A TRIGGER LEVEL	For a stable display

b. Set the generator output for a 1-kHz, 5-vertical-division display.

c. Set:

STORAGE MODE	SAVE
X10 MAG	On (button in)

d. Use the Horizontal POSITION control to position a square-wave rising edge to the center vertical graticule line.

NOTE

A rise time of 0.3 division or less is obtainable only on a pulse leading edge with no samples. If a sample is obtained on a pulse leading edge, the rise time will be at least 1.5 sample periods. To make the rise time and aberration measurements, use the Horizontal POSITION control to position a pulse having no samples on the leading edge to the center vertical graticule line.

e. CHECK—Front corner aberrations are ±0.3 division or less.

f. Use the CH 1 Vertical POSITION control to align the top and bottom of the waveform with the 0% and 100% dotted graticule lines.

g. CHECK—Rise time between 10% and 90% on the waveform rising edge is 0.3 horizontal division or less.

12. Check Storage Acquisition Step Response

a. Set:

TIME/DIV (both)	0.1 μs
STORAGE MODE	NORM
DISPLAY RESPONSE	PULSE (button out)
X10 MAG	Off (button out)

b. Change the generator to 1 MHz and set the output for a 5-division display amplitude.

c. Adjust the A TRIGGER LEVEL control for a triggered acquisition of the signal.

d. Press in the ENVELOPE Storage Mode push button, then press in the SAVE Storage Mode push button.

e. Allow the ENVELOPE acquisition cycle to end (468 then enters the SAVE Storage Mode).

f. CHECK—Overshoot on leading edge of the waveform is 3% or less (0.15 division or less).

13. Check SAVE Storage Mode

a. Set:

VOLTS/DIV (both)	5 mV
TIME/DIV (both)	0.5 ms
STORAGE MODE	NORM

b. Change the generator frequency to 1 kHz and set the generator output to obtain a 5-division display amplitude.

c. Adjust the A TRIGGER LEVEL control for a stable display.

d. Set:

STORAGE MODE	SAVE

e. CHECK—Waveform acquisition stops (trace stops flickering), and the last acquired waveform remains displayed.

NOTE

Waveforms can be expanded up to 100 times horizontally in the steps of the TIME/DIV switch. They can be expanded up to 10 times vertically in the steps of the VOLTS/DIV switch of the channel used to acquire the display.

f. Set:

A TIME/DIV	0.2 ms

g. CHECK—Displayed square-wave period is approximately 5 horizontal divisions wide.

h. CHECK—Waveform continues to expand as the A TIME/DIV switch is stepped to each position clockwise up to and including 5 μs per division.

i. CHECK—Switching the A TIME/DIV switch clockwise past 5 μs per division has no further expansion effect on the waveform.

j. Set:

A TIME/DIV	0.5 ms

k. CHECK—Waveform display is the same as the original waveform saved (5 divisions of amplitude and 1 cycle per 2 divisions).

l. Set:

STORAGE MODE	NORM
CH 1 VOLTS/DIV	50 mV

m. Set:

STORAGE MODE	SAVE

n. CHECK—Display amplitude is approximately 0.5 division.

o. Set:

CH 1 VOLTS/DIV	20 mV

p. CHECK—Display amplitude is approximately 1.25 divisions.

q. CHECK—Waveform continues to expand vertically as the CH 1 VOLTS/DIV switch is stepped clockwise to the 10 mV and 5 mV switch positions. At the 5 mV per division switch position the display amplitude is approximately 5 divisions.

NOTE

When the waveform is fully expanded (10 times), noise present on the acquired signal will cause a least-significant-bit level change on either peak of the displayed waveform. This level change is approximately 0.4 division in amplitude.

r. CHECK—Switching the CH 1 VOLTS/DIV switch clockwise past 5 mV per division has no further expansion effect on the waveform.

s. Return the CH 1 VOLTS/DIV switch to 50 mV.

t. CHECK—Display amplitude is the same as the original waveform saved (approximately 0.5 division).

14. Check SAVE Position Range

a. Set:

STORAGE MODE	NORM
CH 1 VOLTS/DIV	5 mV

b. Set the generator output to obtain an 8-division display amplitude.

c. Set:

STORAGE MODE	SAVE

d. Set:

VOLTS/DIV (CH 1 or CH 2 as appropriate)	0.5 mV

e. CHECK—Top of waveform can be positioned past the bottom graticule line and bottom of waveform can be positioned past the top graticule line using the Vertical POSITION control.

f. Move the signal from the CH 1 input connector to the CH 2 input connector.

g. Set:

VERT MODE	CH 2 only
STORAGE MODE	NORM

h. Repeat parts b through e for CH 2.

i. Disconnect the test equipment from the 468.

15. Check NORM Storage Mode Position Range

a. Set:

STORAGE MODE	NORM
VERT MODE	CH 1
CH 1 VOLTS/DIV	0.1 V
CH 2 VOLTS/DIV	10 mV
AC-GND-DC (both)	DC
TIME/DIV	50 μs

b. Connect a 50-kHz, leveled sine-wave signal via a 50-Ω bnc cable, a 50-Ω bnc termination, and a dual-input coupler to both the CH 1 and CH 2 input connectors.

c. Set the generator output to obtain a 2.4-division display amplitude.

d. Set:

CH 1 VOLTS/DIV	10 mV

e. CHECK—Full counterclockwise rotation of the Vertical POSITION control positions the top of the waveform to at least the 2nd graticule division above the center horizontal graticule line, and full clockwise rotation of the

Vertical POSITION control positions the bottom of the waveform to at least the 2nd graticule division below the center horizontal graticule line.

f. Set:

VERT MODE	CH 2 only

g. Repeat part e using the CH 2 Vertical POSITION control.

h. Disconnect the test equipment from the 468.

16. Check SAVE REFERENCE Operation

a. Set:

VERT MODE	CH 1
TIME/DIV (both)	5 μs
VOLTS/DIV (both)	5 mV

b. Connect a 50-kHz, leveled sine-wave signal via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input connector.

c. Set the generator output to obtain a 5-division display amplitude. Adjust the A TRIGGER LEVEL control as necessary for a stable display.

d. Set:

SAVE REF	On (button in)

e. Rotate the CH 1 Vertical POSITION control to move the waveform about 1 division vertically.

f. CHECK—A reference waveform was acquired at the original position of the displayed waveform.

g. Change the setting of both the CH 1 VOLTS/DIV switch and the A TIME/DIV switch.

h. CHECK—Reference waveform remains unchanged.

i. Press the SAVE REF push button to release it (reference waveform will be removed from the display).

17. Check Useful Storage Bandwidth

a. Set:

DISPLAY RESPONSE	SINE
STORAGE MODE	NORM
VOLTS/DIV (both)	5 mV
A TIME/DIV	10 μs
CURSOR FUNCTION	VOLTS

b. Set the generator output to obtain a 6-division display amplitude.

c. Change the A TIME/DIV switch to 0.2 μs and change the generator output frequency to 10 MHz.

d. Press in the SAVE Storage Mode push button to hold a stable display for measurement.

e. CHECK—Amplitude of any two adjacent peaks is not greater than 33.65 mV nor less than 21.20 mV. Use the VOLTS cursors to make the required measurements.

f. Set:

VERT MODE	CH 1, CH 2, and CHOP

g. Change the generator output frequency to 5 MHz.

h. Press in the NORM Storage Mode push button. Then, after a new display has been acquired, press in the SAVE Storage Mode push button.

i. CHECK—Amplitude of any two adjacent peaks is not greater than 31.80 mV nor less than 25.25 mV. Again, use the VOLTS cursors to make the required measurements.

18. Check Storage Analog Bandwidth

a. Set:

CURSOR FUNCTION	Both off (buttons out)
STORAGE MODE	ENVELOPE
A TIME/DIV	1 ms
VERT MODE	CH 1

b. Change the generator output frequency to 50 kHz and verify that a 6-division vertical signal display is being acquired.

c. Change the generator output frequency to 10 MHz.

NOTE

At exactly 10 MHz input signal frequency, it is possible to produce a beat-signal display. If an ENVELOPE display with variable amplitude appears, shift the test frequency slightly off 10 MHz to obtain an envelope with flat amplitude.

d. Press in the SAVE Storage Mode push button. The 468 will enter the SAVE Storage Mode at the end of the ENVELOPE acquisition cycle.

e. CHECK—The ENVELOPE display signal amplitude is 30 mV peak-to-peak within ±3.65 mV (33.65 mV to 26.35 mV). (Press in the VOLTS CURSOR FUNCTION push button and use the VOLTS cursors to make the required measurement.)

f. Disconnect the test equipment from the 468.

19. Check Storage ALT/CHOP Function

a. Set:

STORAGE MODE	NORM
TIME/DIV (both)	1 ms
CURSOR FUNCTION	Both off (buttons out)
VOLTS/DIV (both)	0.1 V
VERT MODE	CH 1, CH 2, and ALT

b. Connect a 50-kHz, leveled sine-wave signal via a 50-Ω bnc cable, a 50-Ω bnc termination, and a dual-input coupler to both the CH 1 and CH 2 input connectors.

c. Set the generator output to obtain about a 1-division display amplitude of each waveform.

d. Vertically position the waveforms near the middle of the graticule area, about 1 division apart.

e. Set:

TIME/DIV	50 ms

NOTE

Waveforms are aliased and will not appear as a normal sine wave signal.

f. CHECK—Waveforms are acquired and updated alternately (first one and then the other).

g. Set:

VERT MODE	CH 1, CH 2, and CHOP

h. CHECK—Waveforms are acquired and updated simultaneously.

i. Disconnect the test equipment from the 468.

20. Check Channel Isolation

a. Set:

CH 2 VOLTS/DIV	0.2 V
CH 1 VOLTS/DIV	20 mV
VERT MODE	CH 2
AC-GND-DC (both)	DC
A TIME/DIV	0.1 μs
STORAGE MODE	ENVELOPE

b. Connect a 10-MHz, leveled sine-wave signal via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 2 input connector.

c. Set the generator output for a 2-division display amplitude.

d. Set:

VERT MODE	CH 1 only
CH 2 VOLTS/DIV	20 mV

e. CHECK—CH 1 baseline trace amplitude is 0.2 division or less.

f. Set:

VERT MODE	CH 2 only

g. Move the signal from the CH 2 input connector to the CH 1 input connector.

h. CHECK—CH 2 baseline trace amplitude is 0.2 division or less.

i. Disconnect the test equipment from the 468.

21. Check/Adjust Common-Mode Rejection Ratio (R420)

a. Set:

TIME/DIV	50 μs
INVERT	On (button in)
VOLTS/DIV (both)	5 mV
AC-GND-DC (both)	DC
VERT MODE	CH 1
STORAGE MODE	NORM

b. Connect a 50-kHz, leveled sine-wave signal via a 50-Ω bnc cable, a 50-Ω bnc termination, and a dual-input coupler to both the CH 1 and CH 2 input connectors.

c. Set the generator output for a 6-division display amplitude.

d. Set:

STORAGE MODE	ENVELOPE
VERT MODE	ADD only

e. Change the generator frequency to 10 MHz.

f. CHECK—Display amplitude is 0.6 division or less. If it is not, continue with the remainder of this step.

g. Change the generator frequency to 50 kHz.

NOTE

R420 is accessible through the gap between the bottom of the rear frame assembly and the bottom of the main frame. Use an insulated-shaft screwdriver or alignment tool to make the adjustment.

h. ADJUST—CH 2 Acquisition Gain (R420, ADJUSTMENT LOCATIONS 8) for minimum amplitude of the ADD display.

i. Disconnect the test equipment from the 468.

22. Check Ground Dot Display

a. Set:

STORAGE MODE	NORM
VERT MODE	CH 1
AC-GND-DC (both)	GND

b. Use the Vertical POSITION control to align the trace with the center horizontal graticule line. Use the Horizontal POSITION control to align the start of the trace with the left graticule edge.

c. Set:

CH 1 AC-GND-DC	DC

d. Use the Vertical POSITION control to position the trace to both the top and bottom of the graticule area.

e. CHECK—Bright ground dot remains displayed at the center horizontal graticule line as the trace is positioned.

f. Position the trace 2 divisions above the center horizontal graticule line.

g. Set the AC-GND-DC switch to GND momentarily; then, to AC.

h. Position the trace 2 divisions below the center horizontal graticule line.

i. CHECK—Ground dot remains displayed at 2 divisions above the center horizontal graticule line.

j. Set:

VERT MODE	CH 2

k. Repeat parts b through i for CH 2.

23. Check ENVELOPE Storage Mode

a. Set:

TIME/DIV (both)	5 μs
NON STORE	On (button in)
VERT MODE	CH 1
VOLTS/DIV (both)	5 mV

b. Connect a 50-kHz, leveled sine-wave signal via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input.

c. Set the generator for a 4-division display amplitude.

d. Set:

STORAGE MODE	ENVELOPE
NO. OF SWEEPS	On (button in)

e. The seven-segment LED readout should be 32 unless previously changed by the operator. This number is the default value (number automatically set at power-on) for the number of sweeps to be acquired in each envelope waveform. If necessary, use the CURSOR/NO. OF SWEEPS control knob to set the number to 32. Clockwise rotation increases the display number, while counterclockwise rotation of the control knob decreases the number.

f. Use the CH 1 Vertical POSITION control to move the display vertically about 2 divisions. A 2-trace envelope waveform should appear until the display is automatically reset at the end of 32 sweeps.

g. Rotate the CURSOR/NO. OF SWEEPS control knob to the counterclockwise stop. The seven-segment LED display should count down by powers of two to 1.

h. Use the CH 1 Vertical POSITION control to position the waveform vertically. Only a single waveform should appear (display reset with each sweep).

i. Rotate the CURSOR/NO. OF SWEEPS control knob to its clockwise end stop.

j. CHECK—The seven-segment LED display counts up to 256 by powers of two, then displays 9999.

k. Position the display vertically on the graticule.

l. CHECK—An envelope waveform is created, and it does not reset.

m. Rotate the CH 1 VOLTS/DIV VAR control momentarily out of, then back into, its calibrated detent position.

n. CHECK—Envelope display is reset both when the VAR contol is rotated out of its detent position and when it is returned to its detent position.

o. Set:

CH 1 AC-GND-DC	GND
TIME/DIV (both)	20 μs

p. Use the CH 1 Vertical POSITION control to create a 6-division envelope display amplitude. (Rotate the POSITION control clockwise until the maximum envelope amplitude is up 3 divisions from the center graticule line. Then, rotate the control counterclockwise until the minimum envelope amplitude is 3 divisions down from the center graticule line.)

q. CHECK—Space between the maximum and minimum envelope amplitudes is filled at least 90% (5.4 divisions or more).

r. Disconnect the test equipment from the 468.

24. Check Option 12, AVG Operation

a. Set:

VERT MODE	CH 1
VOLTS/DIV (both)	0.5 V
TIME/DIV (both)	5 μs
A TRIGGER SOURCE	CH 1
STORAGE MODE	NORM
AC-GND-DC (both)	DC

b. Connect a 50-kHz, leveled sine-wave signal via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input connector.

c. Set the generator output for about a 5-division display amplitude.

d. Adjust the A TRIGGER LEVEL control for a stable display.

e. Connect 5-μs time markers via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 2 input connector.

f. Set:

VERT MODE	ADD
STORAGE MODE	AVG

g. Press in the NO. OF SWEEPS push button (located on the left side panel). The number 32 should appear in the seven-segment LED display, unless previously changed by the operator. This number is the power-on default value and is automatically set when power is applied to the 468.

h. Note the approximate time marker amplitude seen on the ADD waveform.

i. Rotate the CURSOR/NO. OF SWEEPS control knob clockwise to increase the displayed number to 4, then 8, 16, 32, 64, 128, and finally 256. Allow the display to update at each of the NO. OF SWEEPS selections.

j. CHECK—Time marker amplitude on the sine wave decreases with each completed average cycle as the number of sweeps selected increases. At 256 sweeps, time markers are not visible on the ADD waveform.

k. Return the number of sweeps selected to 32 and press the NO. OF SWEEPS push button (on the left side panel) to release it.

l. Disconnect the test equipment from the 468.

25. Check Option 02, GPIB Operation

Refer to the 468 Digital Storage Oscilloscope Operators Manual for the driver program that enables a Tektronix 4050-series terminal to act as a bus controller for checking operation of the GPIB. Either that program or an operator-developed program must be used with a bus controller to handle the 468 service request that is issued when the 468 is powered on. The program listed in the Operators manual will handle the service request, copy the waveform message, and display the waveform (with graticule lines) and certain 468 control settings that affect the displayed waveform.

STORAGE TRIGGERING

Equipment Required (see Table 4-1)

6. Leveled Sine-Wave Generator
7. Time-Mark Generator
12. 42-in., 50-Ω Bnc Cable
24. 50-Ω, Bnc Termination
25. 3-in., Flat-Bit Screwdriver

See ADJUSTMENT LOCATIONS 8 *in this Volume for test point and adjustment locations.*

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER	ON (button in)

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2)

VOLTS/DIV	0.5 V
VOLTS/DIV VAR	Calibrated detent
VERT MODE	CH 1
POSITION	Midrange
AC-GND-DC	DC
INVERT	Off (button out)
20 MHz BW LIMIT	Full bandwidth (button out)

Trigger (A and B if applicable)

LEVEL	Midrange
SLOPE	+
COUPLING	AC
SOURCE (both)	NORM
A TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep (A and B)

HORIZ DISPLAY	A
TIME/DIV (both)	5 μs
TIME/DIV VAR	Calibrated detent
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

STORAGE MODE	NORM
STORAGE WINDOW	POST TRIG (button out)
CURSOR FUNCTION	Both off (buttons out)
SAVE REF	Off (button out)
DISPLAY RESPONSE	SINE (button in)

1. Check STORAGE WINDOW Operation

a. Connect 0.1 ms time markers via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input connector.

b. Use the CH 1 Vertical POSITION control to align the display's baseline with the center horizontal graticule line and use the Horizontal POSITION control to align the sweep start with the left graticule edge.

c. CHECK—Rising edge of the time marker occurs at approximately 1.3 divisions from the left graticule edge.

d. Set:

STORAGE WINDOW	PRE TRIG

e. CHECK—Rising edge of the time marker occurs at approximately 9 divisions from the left graticule edge.

2. Check A and B + GATES

a. Set:

NON STORE	On (button in)
A TIME/DIV	0.1 ms
B TIME/DIV	20 μs
TRIGGER LEVEL (both)	For a stable display

b. Note—Display has 1 time marker per division.

c. Set:

STORAGE MODE	NORM

d. CHECK—Display continues to have 1 time marker per division.

e. Set:

HORIZ DISPLAY	A INTEN

f. CHECK—Display remains unchanged.

g. Set:

NON STORE	On (button in)
HORIZ DISPLAY	B DLY'D

h. Note—Display has 1 time marker per 5 divisions.

i. Set:

STORAGE MODE	NORM

j. CHECK—Display continues to have 1 time marker per 5 divisions.

k. Set:

HORIZ DISPLAY	ALT

l. CHECK—Display remains unchanged.

m. Disconnect the test equipment from the 468.

3. Check/Adjust Storage NORM Trigger DC Balance (R126)

a. Set:

CH 1 VOLTS/DIV	5 mV
HORIZ DISPLAY	A

b. Connect a 50-kHz, leveled sine-wave signal via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input connector.

c. Set the generator output for a 6-division display amplitude.

d. Use the CH 1 Vertical POSITION control to center the display vertically.

e. Use the A TRIGGER LEVEL control to align the point where the sine wave's leading edge intersects the center horizontal graticule line with the 2nd vertical graticule line (1 division from the left graticule line).

f. Set:

A TRIGGER COUPLING	DC

g. CHECK—Intersection point of the sine wave and the center horizontal graticule line remains at the 2nd vertical graticule line within ±0.2 division.

h. ADJUST—Storage NORM DC TRIG Balance (R126) to align the intersection point of the sine wave's leading edge and the center horizontal graticule line with the 2nd vertical graticule line. The adjustment is accessible through a hole in the top of the rear frame assembly next to the 50-conductor ribbon cable connector.

i. Disconnect the test equipment from the 468.

STORAGE HORIZONTAL

Equipment Required (see Table 4-1)

6. Leveled Sine-Wave Generator
7. Time-Mark Generator
12. 42-in., 50-Ω Bnc Cable
24. 50-Ω Bnc Termination
25. 3-in., Flat-Bit Screwdriver

See ADJUSTMENT LOCATION *in this Volume for test point and adjustment locations.*

468 CONTROL SETTINGS

Power

Regulating Range Selector	High
Line Voltage Selector	115 V
POWER	ON

Crt

INTENSITY	As desired
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (CH 1 and CH 2)

VERT MODE	CH 1
VOLTS/DIV	0.5 V
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC	DC
POSITION	Midrange
INVERT	Off (button out)

Trigger (A and B)

COUPLING	AC
SLOPE	+
LEVEL	For a stable, triggered display
SOURCE	NORM
A TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM
B TRIGGER SOURCE	STARTS AFTER DELAY
DELAY TIME POSITION	Fully counterclockwise

Sweep (A and B if applicable)

HORIZ DISPLAY	A
TIME/DIV	1 ms
TIME/DIV VAR	Calibrated detent
X10 MAG	Off (button out)
POSITION (Horizontal)	Midrange

Digital Storage

STORAGE MODE	NORM
STORAGE WINDOW	POST TRIG (button out)
DISPLAY RESPONSE	PULSE (button out)
CURSOR FUNCTION	Both off (buttons out)
SAVE REF	Off (button out)

1. Check/Adjust Storage Horizontal Gain (R550) and Storage Horizontal Centering (R346)

a. Connect 1-ms time markers via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input connector.

b. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

c. CHECK—Timing at the 10th time marker is within ±0.16 division (2% over the center 8 divisions). If timing is within tolerance, skip to part j. If it is not, continue with the remainder of this procedure.

d. Set:

CURSOR FUNCTION	TIME
AC-GND-DC	GND

e. Use the Vertical POSITION control to center the trace vertically and use the Horizontal POSITION control to align the start of the trace with the left graticule edge. Trace must extend approximately 0.24 division beyond the right graticule edge.

f. Adjust the INTENSITY control so that only the TIME dots are visible.

g. Use the CURSOR control knob to position the active TIME dot to the 2nd vertical graticule line.

h. Press in the CURSOR SELECT push button to activate the 2nd TIME dot and position it to obtain a seven-segment LED readout of exactly 8.00 ms.

i. ADJUST—Horizontal Display Gain (R550) to obtain exactly 8 divisions between the two TIME dots. Use the Horizontal POSITION control to keep the 1st TIME dot aligned with the 2nd graticule line while adjusting R550.

j. Set:

VERT MODE	None (all buttons out)
NON STORE	On (button in)

k. Position the start of the trace to the left graticule edge.

l. Set:

STORAGE MODE	NORM
INTENSITY	For a visible trace

m. CHECK—Start of trace is at the left graticule edge within ±0.2 division.

n. ADJUST—Horizontal Display Centering (R346) to position the start of the trace at exactly the left graticule edge.

o. INTERACTION—Horizontal Display Centering slightly affects Horizontal Display Gain. Press in the CH 1 VERT MODE push button and repeat parts b and c to check the Horizontal Display Gain. If the gain is not within tolerance, repeat parts d through o of this step until no further improvement is noted.

2. Check Storage Timing Accuracy

a. Set:

VERT MODE	CH 1
STORAGE MODE	NORM
A TIME/DIV	2 μs
CH 1 AC-GND-DC	DC

b. Set the time-mark generator for 2-μs time markers. Obtain a NORM Storage Mode time-marker display. For POST TRIG Storage Window, only 10 time markers will be displayed. Use the CH 1 Vertical POSITION control to center the display vertically.

NOTE

Amplitude variations occurring in the time markers as they are being acquired is due to the sample-clock and time-marker frequency differences. Sampling of the narrow time markers does not always occur either at peak amplitude of the markers or at the same amplitude point on the markers between sampling intervals.

c. Use the Horizontal POSITION control to align the 2nd time marker rising edge with the 2nd vertical graticule line.

NOTE

If display amplitude variation becomes a problem, press in the SAVE Storage Mode push button (when an acquisition is completed) to hold the waveform display stable for making the accuracy check. The SAVE Storage Mode display may also be positioned vertically, if required, to move any portion of the waveform to the graticule markings on the center horizontal graticule line.

d. Set the CH 1 AC-GND-DC switch to GND and adjust the INTENSITY control for a visible display of the trace and the TIME dots.

e. Use the CURSOR/NO. OF SWEEPS control knob to set the active TIME dot to the 2nd vertical graticule line. Press the CURSOR SELECT push button to activate the other TIME dot. Position the TIME dot to the 10th vertical graticule line (8-division spacing between the TIME dots).

f. CHECK—LED readout accuracy is within 2% (16.00 μs ± 0.32μs).

g. Set the CH 1 AC-GND-DC switch to DC and adjust the INTENSITY control as necessary for viewing the time markers.

h. CHECK—Readout and timing accuracy at each TIME/DIV switch setting listed in Table 4-25. The time marker spacing must be accurate within 2% (8 divisions ± 0.16 division) over the center 8 divisions. The LED readout limits at each TIME/DIV switch setting are listed in Table 4-25. Use the Horizontal POSITION control as necessary to maintain alignment of the 2nd time marker on the 2nd vertical graticule line as the TIME/DIV switch setting is changed.

NOTE

To obtain a valid display on the 1st trigger accepted at a new TIME/DIV switch setting, change the time-mark generator output to the next required time markers before changing the 468 TIME/DIV switch setting. This procedure is especially useful for TIME/DIV switch settings from 0.1 s to 5 s per division. Watch for a display update (display flickers and TIME LED readout changes to the scale of the newly acquired waveform) prior to making the accuracy check at the new TIME/DIV switch setting. As TIME/DIV switch setting increases, the time required for the update to occur increases. At 5 s per division, it takes at least 50 s to acquire a complete waveform.

i. Set:

A TRIG MODE	AUTO
HORIZ DISPLAY	B DLY'D
TIME/DIV (both)	2 μs
A TRIGGER LEVEL	For a stable display

j. Set the time-mark generator for 2-μs markers.

k. CHECK—Repeat part h of this step to check the B timing accuracy.

l. Disconnect the test equipment from the 468.

3. Check Storage 0.02-μs to 1.0-μs Timing Accuracy

a. Set:

A TRIGGER MODE	AUTO
HORIZ DISPLAY	A
TIME/DIV (both)	0.02 μs
CH 1 AC-GND-DC	GND

Table 4-25

Storage Timing Accuracy

A and B TIME/DIV Switch Setting	Time-Mark Generator Output	LED Readout Accuracy Over Center 8 Divisions
2 μs	2 μs	15.68 μs to 16.32 μs
5 μs	5 μs	39.20 μs to 40.80 μs
10 μs	10 μs	78.40 μs to 81.60 μs
20 μs	20 μs	157.8 μs to 163.2 μs
50 μs	50 μs	392.0 μs to 408.0 μs
0.1 ms	0.1 ms	0.784 ms to 0.816 ms
0.2 ms	0.2 ms	1.568 ms to 1.632 ms
0.5 ms	0.5 ms	3.920 ms to 4.080 ms
1.0 ms	1.0 ms	7.84 ms to 8.16 ms
2.0 ms	2.0 ms	15.68 ms to 16.32 ms
5.0 ms	5.0 ms	39.20 ms to 40.80 ms
10.0 ms	10.0 ms	78.40 ms to 81.60 ms
20.0 ms	20.0 ms	156.8 ms to 163.2 ms
50.0 ms	50.0 ms	392.0 ms to 408.0 ms
0.1 s[a]	0.1 s	0.784 s to 0.816 s
0.2 s[a]	0.2 s	1.568 s to 1.632 s
0.5 s[a]	0.5 s	3.920 s to 4.080 s
1.0 s[a]	1.0 s	7.84 s to 8.16 s
2.0 s[a]	2.0 s	15.68 s to 16.32 s
5.0 s[a]	5.0 s	39.20 s to 40.80 s

[a]For TIME/DIV switch settings slower than 50 ms/division, set TRIG MODE to NORM.

b. Obtain a NORM Storage Mode display of the baseline trace. Then, press in the SAVE Storage Mode push button.

c. Adjust the INTENSITY control for a visible display of the trace and the TIME dots. Use the CH 1 Vertical POSITION control to center the trace vertically.

d. Use the CURSOR/NO. OF SWEEPS control knob to set the active TIME dot on the 2nd vertical graticule line. Press in the CURSOR SELECT push button to activate the other TIME dot. Use the CURSOR/NO. OF SWEEPS control knob to position the 2nd TIME dot to the 10th vertical graticule line (8 divisions between the TIME dots).

e. CHECK—LED readout accuracy at each TIME/DIV switch setting listed in Table 4-26. The seven-segment read-

out must be accurate within 2%. The green scaling LED should be illuminated for TIME measurements.

f. Set:

HORIZ DISPLAY	B DLY'D

g. CHECK—Repeat parts b through e of this step to check the B-timing LED readout accuracy.

h. Disconnect the test equipment from the 468.

Table 4-26

0.02-μs to 1.0-μs Timing Accuracy

TIME/DIV Switch Setting	LED Readout Accuracy
0.02 μs	0.157 μs to 0.163 μs
0.05 μs	0.392 μs to 0.408 μs
0.1 μs	0.784 μs to 0.816 μs
0.2 μs	1.568 μs to 1.632 μs
0.5 μs	3.920 μs to 4.080 μs
1.0 μs	7.84 μs to 8.16 μs

4. Check Jitter Correction

a. Set:

VERT MODE	CH 1
VOLTS/DIV	5 mV
HORIZ DISPLAY	A
TIME/DIV	0.02 μs
DISPLAY RESPONSE	SINE (button in)
STORAGE MODE	NORM
CURSOR FUNCTION	Both off (buttons out)

b. Connect a 10-MHz, leveled sine-wave signal via a 50-Ω bnc cable and a 50-Ω bnc termination to the CH 1 input connector.

c. Set the generator output for about a 5-division display amplitude.

d. Adjust the A TRIGGER LEVEL control for a stable display.

e. CHECK—Horizontal display jitter is 0.3 division or less.

NOTE

Due to an inherent uncertainty in jitter correction, the jitter will occasionally, at random intervals, exceed 0.3 division. Abnormal jitter correction circuit operation is indicated by a constant horizontal jitter in the display.

f. Set:

TIME/DIV (both)	20 μs
CH 1 VOLTS/DIV	2 mV
X10 MAG	On (button in)

g. Change the generator frequency to 50 kHz.

h. CHECK—Horizontal display jitter is 0.2 division or less.

i. Disconnect the test equipment from the 468.

MAINTENANCE

This section of the manual contains information for use in preventive maintenance, troubleshooting, and corrective maintenance. Signature tables for use in signature analysis testing of the digital storage circuitry are contained at the end of this section. These table are used in conjunction with the troubleshooting charts located at the back of this volume.

PREVENTIVE MAINTENANCE

INTRODUCTION

Preventive maintenance consists primarily of cleaning and visual inspection. When performed on a regular basis, it can enhance instrument reliability. A convenient time to perform preventive maintenance is just prior to recalibration of the instrument. Operating the 468 under severe environmental conditions will necessitate a more frequent preventive maintenance schedule.

CLEANING

The cabinet minimizes accumulation of dust inside the instrument and should normally be in place when operating the instrument. The front cover provides dust protection for the front panel and crt face and should be installed whenever the instrument is stored or is being transported.

Exterior

Loose dust accumulated on the outside of the oscilloscope can be removed with a soft cloth or small camel-hair brush. The paint brush is particularly useful for dislodging dirt on and around the front-panel controls. Dirt that remains can be removed with a soft cloth dampened in a mild detergent and water solution. Do not use abrasive cleaners.

Interior

Dust and dirt inside the instrument should be removed as often as operating conditions require. Accumulation of dirt can cause overheating and component breakdown. Dirt on components acts as an insulating blanket, preventing efficient heat dissipation. It also provides an electrical conducting path that can result in instrument failure, especially under high humidity conditions.

CAUTION

Avoid the use of chemical cleaning agents that might damage the plastics used in this instrument. Do not use chemicals that contain acetone, benzene, toluene, xylene, petroleum ether, white kerosene, carbon tetrachloride, methylene chloride, trichloroethane, trichlorotrifluoroethane (Freon 113, -tf, -ta, -te, -tmc) and trichlorethylene. Recommended cleaning agents are isopropyl alcohol, kelite (1 part kelite, 20 parts water), and a solution of 1% mild detergent and 99% water.

Before performing interior cleaning, refer to the "Cabinet Removal" instructions in the Corrective Maintenance part of this section. The best way to clean the interior is to blow out the accumulated dust with dry, low-pressure air (approximately 9 pounds per square inch). Remove any remaining dirt with a soft brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces or for cleaning ceramic terminal strips and circuit boards. Do not use an applicator on switch contacts since they tend to snag, possibly causing damage. Strands of cotton caught by the contacts can also cause intermittent electrical contact.

CAUTION

To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the instrument.

The high-voltage circuits should receive special attention. Excessive accumulations of dirt in these areas may cause high-voltage arcing that can result in circuit component damage.

Switch Contacts

Many of the switches in the 468 are circuit-board mounted, cam-activated contacts. Exercise care to preserve the high-frequency characteristics of these switches. Switch maintenance is seldom necessary, but if it is required, observe the following precautions:

1. Use only isopropyl alcohol as a cleaning solution, especially in the area of the vertical attenuator boards. Carbon-based solvents will damage the board material used for these boards.

2. Apply the alcohol with a small, camel-hair brush. Do not use cotton-tipped applicators on the contacts.

CAUTION

Most spray-type circuit coolants contain Freon 12 as a propellant. Because many Freons adversely affect switch contacts, check the contents and brand name before using a spray-type coolant. The following brand names are acceptable: Artic Freeze, Quik-Freeze, and Can-O-Gas. Do not use Zero Mist brand. The only recommended circuit coolant for the volts/division attenuators is either dry ice (CO_2) or isopropyl alcohol.

Crt

Two plastic light filters, one blue and one clear, are provided with the oscilloscope. Clean the light filters and the crt face with a soft lint-free cloth dampened with denatured alcohol or a mild detergent and water solution. The optional crt mesh filter can be cleaned in the following manner:

1. Hold the filter in a vertical position and brush lightly with a Number 7 soft watercolor brush to remove light coatings of dust and lint.

2. Greasy residues or dried-on dirt can be removed with a solution of warm water and a neutral-pH liquid detergent. Use the brush to lightly scrub the filter.

3. Rinse the filter thoroughly in clean water and allow to air dry.

4. If any lint or dirt remains, use clean low-pressure air (approximately 9 pounds per square inch) to remove it. Do not use tweezers or other hard cleaning tools on the filter, as the special finish may be damaged.

5. When not in use, store the mesh filter in a lint-free dust-proof container such as a plastic bag.

Air Filter

The air filter should be visually checked every few weeks and cleaned or replaced if dirty. More frequent inspections are required under severe operating conditions. The following procedure is suggested for cleaning the filter:

1. Remove the filter from the side panel. Be careful not to drop any accumulated dirt into the instrument.

2. Flush the loose dirt from the filter with a stream of hot water.

3. Place the filter in a solution of mild detergent and hot water and let it soak for several minutes.

4. Squeeze the filter to force out any remaining dirt.

5. Rinse the filter in clear water and allow it to dry.

6. Coat the dry filter with an air-filter adhesive (available from an air-conditioner supplier, or see Table 5-3 "Maintenance Aids" under "Corrective Maintenance").

7. Let the adhesive dry thoroughly.

8. Reinstall the filter in the side panel.

If the filter is to be replaced, order new air filters from your local Tektronix Field Office or representative. Refer to the Replaceable Mechanical Parts List in Volume II for ordering information.

VISUAL INSPECTION

The instrument should be inspected occasionally for such defects as broken connections, broken or damaged ceramic strips, improperly seated semiconductors, damaged or improperly installed circuit boards, and heat-damaged parts.

The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

LUBRICATION

The fan motor and most of the potentiometers used in the 468 are permanently sealed and generally do not require periodic lubrication. The switches used in the 468, both cam- and lever-type, are installed with proper lubrication applied where necessary and will rarely require any additional lubrication. A regular periodic lubrication program for the 468 is not recommended.

SEMICONDUCTOR CHECKS

Periodic checks of the transistors and other semiconductors in the oscilloscope are not recommended. The best check of semiconductor performance is actual operation in the instrument.

PERIODIC READJUSTMENT

To ensure accurate measurements, check the adjustment of this instrument after each 1000 hours of operation or, if used infrequently, every six months. In addition, replacement of components may necessitate readjustment of the affected circuits.

Complete adjustment instructions are given in the "Calibration" section. The adjustment procedure can also be helpful in localizing certain troubles in the instrument. In some cases, minor troubles may be revealed and/or corrected by readjustment. If only a partial adjustment is performed, see the interaction chart, Table 4-9 in the "Calibration" section, for possible interactions with circuits not adjusted.

TROUBLESHOOTING

The following information is provided to facilitate troubleshooting the 468. Information contained in other sections of this manual should be used along with the following information to aid in locating the defective component(s). An understanding of the circuit operation is helpful in locating troubles, particularly where integrated circuitry is used. See the "Theory of Operation," Section 3.

POWER-ON SELF-TEST

Each time the POWER push-button switch is pressed in to apply power to the instrument, a power-on self-test will be initiated by the 468. The various tests are performed in the sequence in which they are presented in the following discussion. The test sequence may be restarted by cycling the POWER switch OFF, then ON again.

ROM Checksum Test

A checksum will be calculated and checked for each ROM in the instrument. If an incorrect checksum is found, the Microprocessor will halt, and the oscilloscope will neither respond to the front-panel switches nor will it operate.

Front-panel indication of a ROM failure is that the Lamp test is never started. All LED displays may either be off or on in a random pattern. A definite indication of a ROM problem is failure to execute the RAM Verification test. A failure of an individual LED indicates that the LED or its controlling circuitry has become inoperative.

Lamp Test

All LED displays on the front panel that are under control of the Microprocessor, including all the segments and decimal points of the seven-segment display, will be illuminated at power-on. Failure of the LED to come on indicates occurrence of a problem that prevents the ROM program from reaching that particular point in the power-on sequence.

RAM Verification Test

NOTE

The RAM Verification portion of the power-on self-test can be internally disabled. To do so, set section 7 of the Service/Options switch to the "OPEN" position. Refer to Figure 5-6 in this section of the manual for the Service/Options switch location.

If the ROM Checksum test result is correct, the self-test will proceed to the RAM Verification test. When the RAM Verification test starts, the seven-segment display will first be blanked and then will start displaying the RAM Verification test error codes. The RAM are checked in the following order:

1. System RAM
2. Scratch RAM
3. Display RAM
4. Acquisition RAM

If all tests are passed, the seven-segment display will be blank, and then the oscilloscope will begin operating immediately. Total time required for completion of the power-on self-test is approximately six seconds. Any RAM failure will prevent oscilloscope operation. In addition, a failure in the System RAM will cause the self-test to halt, and a single error code will appear in the seven-segment display (see Figure 5-1 for the display location assigned to each RAM). Any other RAM failure will not stop self testing.

At the end of the RAM Verification test, the seven-segment display will indicate the results of the test.

RAM Verification Test Description

Two tests will be performed on each RAM section: MARCH and DIAPAT. Each RAM section will be tested separately by both tests. Error codes displayed on the seven-segment LED display indicate either that a RAM section has passed the test or that it has failed. A zero is displayed in each segment if all the tests are passed. Error codes appear in any segment assigned to a RAM section that fails a test. See Figure 5-1 for error code definition. In general, failure of a MARCH test indicates a problem in writing or reading data, while failure of a DIAPAT test indicates an addressing problem.

MARCH TEST. This test determines whether each RAM address can be accessed and written into with both a zero and a one. Testing sequence for each RAM section under test is as follows:

1. Writes a background pattern of all zeros into each address.

2. Reads, tests, and writes complements to all addresses.

3. Repeats step 2, reversing the address order.

4. Writes a background pattern of all ones and repeats steps 2 and 3.

DIAPAT TEST. This test is a shifting diagonal pattern used to detect internal multiple-address selection, destruction of stored data due to noise coupling, faulty sense amplifiers, and slow sense amplifier recovery. The testing sequence for each RAM section under test is as follows:

1. Writes a background pattern of all zeros into each address.

2. Starting with a pattern of 00000001 as the original data stored, the Microprocessor performs a left shift.

3. Stores the shifted data and shifts it left again.

SEVEN-SEGMENT LED DISPLAY

ACQUISITION RAM	DISPLAY RAM	SCRATCH RAM	SYSTEM RAM

ERROR CODE	MEANING
0	NO ERROR
1	MARCH TEST ERROR
2	DIAPAT TEST ERROR
3	BOTH TEST ERROR

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Figure 5-1. RAM error code display.

4. Repeats step 3 until all the address locations are filled.

5. Tests all locations and writes a zero at each location.

6. Shifts original pattern left one position and saves the shifted pattern.

7. Repeats steps 3 through 5.

8. Repeats step 6 until the pattern is back to 00000001.

9. Writes a background pattern of all ones.

10. With an original pattern of 11111110, the Microprocessor performs a left shift.

11. Repeats steps 3 through 6 until the pattern is back to 11111110.

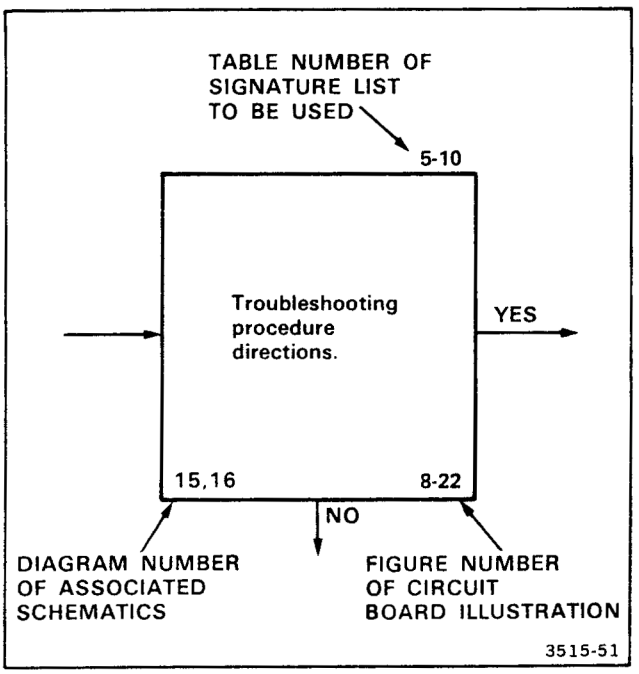


Figure 5-2. Explanation of troubleshooting chart procedure block notations.

TROUBLESHOOTING AIDS

Troubleshooting Charts

The troubleshooting charts, located on tabbed foldout pages at the back of this volume, are to be used as an aid in locating malfunctioning circuitry. They cover both conventional and digital-storage circuitry, with special emphasis placed on the digital-storage portion.

Begin troubleshooting with the Troubleshooting Index chart. The Index chart will help identify a particular problem area and will indicate which other chart can be used for further troubleshooting of that area.

Note that some troubleshooting-procedure boxes on each chart contain numbers in their bottom corners. These are the numbers of the applicable circuit diagram(s) and circuit board illustration(s) (see Figure 5-2). Numbers shown at the start of a troubleshooting path remain applicable to downstream procedure boxes in the path until the procedure specifies a different diagram and/or illustration.

Many of the procedures call for signature-analysis testing. The applicable signature table number is shown outside the upper right corner of the procedure box (see Figure 5-2). The table number is not repeated beyond the first box for which it is used in a troubleshooting path. Any change of the table to be used will be indicated at the box where the change occurs.

Signature tables are located at the end of this section to facilitate their use with the troubleshooting charts contained at the back of this volume. Schematic diagrams and circuit board illustrations are located in Volume II so that they may be referred to without disturbing the pages selected in Volume I.

General and specific notes called out in the troubleshooting-procedure boxes are located on the inner panels of the foldout pages. These notes are usually specific procedures, or amplifying information, to be used in performing the troubleshooting step called for in that box. General notes contain information that pertains to the overall troubleshooting procedure.

Some malfunctions, especially those involving multiple simultaneous failures, may require more elaborate approaches with frequent reference to circuit descriptions in the "Theory of Operation" section of this manual.

Signature Lists

Many of the troubleshooting procedures will refer you to one of the signature list tables at the end of this section. Identified at the top of each table are the circuit boards

on which signatures are to be taken or on which the signature analyzer setup points are to be connected. Signatures contained on a specific circuit board are preceded by the assembly number for that board. Before attempting to take signatures, connect the signature analyzer setup and perform the 468 setup as specified in the appropriate table; then verify the +5 V Check signature.

Service ROM and Test Counter IC

Many of the troubleshooting procedures also require the use of an optional servicing package that includes a Service ROM and a Test Counter IC. The ROM contains the service routines, and the Test Counter IC simulates operation of the vertical signal A/D Converter. Refer to "Maintenance Aids," Table 5-3 in this section of the manual, or contact your local Tektronix Field Office or representative for more information concerning procurement of these accessories.

Diagrams

Complete schematic diagrams are contained on tabbed foldout pages in the Diagrams section of Volume II. The portions of circuitry mounted on each circuit board are enclosed with a heavy black line. Also within the black line, near either the top or bottom edge, is the assembly number and name of the circuit board.

The component number and electrical value of each component in this instrument are shown on the diagrams. See the first page of the Diagrams section for definition of the reference designators and symbols used to identify components in this instrument. Important voltages and waveform numbers are also shown on the schematic diagrams. The physical location of each waveform test point is shown on the appropriate circuit board illustration, and the waveform illustrations are located adjacent to the respective schematic diagram.

Circuit Board Illustrations

A circuit board illustration is provided in conjunction with each schematic diagram. These illustrations are found on the back side of a pullout page which precedes the schematic diagram to which it relates. If more than one diagram is associated with a particular circuit board illustration, the board illustration is located just before its first appearance in a schematic diagram.

Each component shown on a diagram is identified on the circuit board illustration by its component number. In general, component numbers on the circuit boards increase from the left side of the circuit board to the right side and from the top to the bottom. The lowest component numbers will be at the top-left corner, and the highest at the bottom-right corner of the circuit board.

Waveform test points are identified by hexagonal outlined numbers that correspond to the points indicated on the schematic diagrams.

Adjustment Location Illustrations

To aid in locating test points and adjustable components, the ADJUSTMENT LOCATION foldout pages (normally used with the "Adjustment Procedure" are located at the back of this volume.

Grid Coordinate System

Each circuit diagram and circuit board illustration has a grid border. A table located adjacent to each schematic diagram lists the grid coordinates of each component shown on that diagram. The component grid location is shown for both the schematic diagram and the circuit board illustration to aid in cross referencing component location.

Adjacent to each board illustration are alpha-numeric listings of all components mounted on that board. The components are separated by the schematic diagram number in which each component can be found. These grid tables are especially useful when more than one diagram is associated with a particular circuit board.

Power Distribution Diagram

As an aid in troubleshooting power supply problems, Diagram 22 in the foldout pages of Volume II shows the distribution of each voltage from the Main Power Supply. The service jumpers used to remove power from the various circuit boards are also indicated. Excessive loading on the Main Power Supply by a circuit board can be rapidly isolated to the faulty board with the aid of these service jumpers. The power distribution diagram should be used in conjunction with the power supply isolation procedures adjacent to the power supply troubleshooting charts.

Circuit Board Interconnection Diagram

Circuit board interconnections are provided to aid in tracing a signal path or power source between boards. The entire oscilloscope is illustrated, with plug and jack numbers shown along with associated pin numbers. The off-board components are also shown, and the schematic diagram number on which the component is located is identified.

Block Diagrams

Detailed block diagrams of the conventional portion of the oscilloscope and of each major circuit in the digital storage portion of the oscilloscope are included to aid in understanding circuit function and interconnection. Circuit descriptions located in the "Theory of Operation" section

of this manual are based on both the schematic diagrams and the block diagrams.

Component Color Coding

Information regarding color codes and markings of resistors and capacitors is located in the color-coding illustration (Figure 8-1) at the beginning of the Diagrams section in Volume II.

DIODE COLOR CODE. The cathode end of each glass-encased diode is indicated by a stripe, a series of stripes, or a dot. For most silicon or germanium diodes marked with a series of stripes, the color combination of the stripes identifies the three significant digits of the Tektronix Part Number, using the resistor color-code system. For example, a diode having either pink or blue at the cathode end, then brown-gray-green, is Tektronix Part Number 152-0185-00. The cathode and anode ends of metal-encased diodes can be identified by the diode symbol stamped on the diode body.

Semiconductor Lead Configurations

Typical semiconductor lead configurations are illustrated at the beginning of the Diagrams section (Figure 8-2) in Volume II.

Multi-Connector Holders

Multi-connector holders are keyed with two index triangles: one on the holder and one on the circuit board. Slot numbers are usually stamped on the holder. When a connection is made perpendicular to a circuit board surface, ensure that the triangle on the holder and the triangle on the circuit board are aligned pointing toward each other (see Figure 5-3).

TROUBLESHOOTING EQUIPMENT

A list of suggested test equipment for servicing this instrument is contained in Table 5-1.

CAUTION

Before using any test equipment to make measurements on static-sensitive components or assemblies, be sure that any voltage or current supplied by the test equipment does not exceed the limits of the component to be tested.

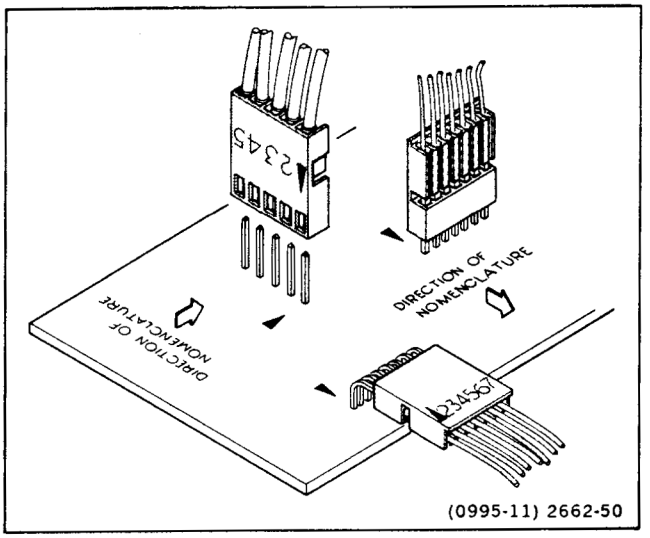


Figure 5-3. Multi-connector holder orientation.

TROUBLESHOOTING TECHNIQUES

This troubleshooting procedure is arranged in an order which checks the simple trouble possibilities before proceeding with extensive troubleshooting. The first few checks ensure proper connection, operation, and calibration. If the trouble is not located by these checks, the remaining steps will aid in locating the defective component. When the defective component is located, it should be replaced following the replacement procedure given under "Corrective Maintenance" in this section.

Check Control Settings

Incorrect control settings can give a false indication of an instrument malfunction. If there is any question about the correct function or operation of any control, refer to either the "Operating Information" section of this manual or the 468 Operators Manual.

Check Associated Equipment

Before proceeding with troubleshooting, check that the equipment used with this instrument is operating correctly. Check that the signal is properly connected and that the interconnecting cables are not defective. Also, check the power source for correct voltage.

Check Instrument Calibration

Check the calibration of either the entire instrument, or of the affected circuit, if the trouble exists in one circuit. The apparent trouble may only be a result of misadjustment and may be corrected by adjustment. Complete adjustment instructions are given in the "Calibration" section of this manual.

Table 5-1

Suggested Troubleshooting Equipment

Equipment	Minimum Specification	Usage	Examples
1. Signature Analyzer	Capable of analyzing signatures and displaying a four-digit standard signature.	Check signatures in troubleshooting procedures.	SONY/TEKTRONIX 308 Data Analyzer.
2. Test Oscilloscope with 10X Voltage Probe	Frequency response, dc to at least 100 MHz; deflection factor, 5 mV to 5 V/div; input impedance, 1 MΩ, 20 pf; sweep rate, 0.5 s to 0.02 μs/div.	Check operating waveforms.	TEKTRONIX 465B Oscilloscope with included 10X probe.
3. Semiconductor Tester	Dynamic type tester. Measure reverse breakdown voltages up to at least 400 V.	Test semiconductors.	a. TEKTRONIX 576 Curve Tracer. b. TEKTRONIX 577 (D1 or D2) Curve Tracer with 177 Test Fixture.
4. Multimeter	Digital multimeter. Voltmeter input impedance, 10 MΩ range 0 to 150 volts; voltage accuracy, within 0.15%, display 4 1/2 digits. Ohmmeter, 0 to 20 MΩ.	Check voltages and general troubleshooting.	a. TEKTRONIX DM 501A Digital Multimeter.[a] b. TEKTRONIX 465B44 Oscilloscope DMM.
5. Variable Autotransformer	Variable from 0 to 140 V, 1.2 A. Equipped with 3-wire power cord, plug, and receptacle.	Vary input line voltage when troubleshooting power supply.	General Radio W8MT3VM or W10MT3W Metered Variac Autotransformer.

[a]Requires a TM 500-Series power module.

Visual Check

Visually check the portion of the instrument in which the trouble is located. Many troubles can be located by visible indications such as unsoldered connections, broken wires, loose plugs, damaged circuit boards, and damaged components.

Isolate Trouble to a Circuit

To isolate trouble to a particular circuit, note the trouble symptom. The symptom often identifies the circuit in which the trouble is located. Use the troubleshooting charts found at the back of this volume as an aid in locating a faulty circuit.

When trouble symptoms appear in more than one circuit, first check the power supplies, then check the affected circuits. If the trouble has been isolated to a power supply, follow the troubleshooting chart for that supply. The Main Power Supply voltage levels are interdependent. All the Main low-voltage supplies depend on the +55-V supply for a reference. If more than one of the Main Power Supply voltages appears defective, repair them in the following order: +55 V, +110 V, +15 V, −8 V, +5 V, then −2450 V.

The Digital Storage Power Supply is independent of the Main Power Supply.

Check Circuit Board Interconnections

After the trouble has been isolated to a particular circuit, check for loose or broken connections, improperly seated transistors, and heat-damaged components.

Check Voltages and Waveforms

Often the defective component can be located by checking for the correct voltage or waveform in the circuit. Typical voltages are listed on the diagrams. Waveforms are shown adjacent to the circuit diagram, and waveform test points are indicated by a hexagonal outlined number.

NOTE

Voltages and waveforms given on the diagrams are not absolute and may vary slightly between instruments. To obtain operating conditions similar to those used to take these readings, see the voltage and waveform setup procedures at the beginning of the Diagrams section for the preliminary equipment setup. Note the recommended test equipment, front-panel control settings, voltage and waveform conditions, and test equipment cable connection instructions. The 468 Oscilloscope control settings required to obtain the given waveforms and voltages are located adjacent to the waveform diagrams. Changes to the control settings from the preliminary setup, other than those given, are usually not required.

Check Individual Components

The following procedures describe methods of checking individual components. Components that are soldered in place are most accurately checked by disconnecting one end. This isolates the measurement from the effects of surrounding circuitry.

WARNING

Turn off POWER switch and unplug the line cord from the ac-power source before removing or replacing components.

SEMICONDUCTORS. A good check of transistor operation is actual performance under operating conditions. A transistor can be most effectively checked by substituting a new component for it (or one which has been checked previously). However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic tester. Static-type testers are not recommended, since they do not check operation under simulated operating conditions.

When troubleshooting transistors in the circuit with a voltmeter, measure both the emitter-to-base and emitter-to-collector voltages to determine if the voltages are consistent with normal circuit voltage. Voltages across a transistor vary with the type of device and its circuit function. Some of these voltages are predictable. The emitter-to-base voltage of a conducting silicon transistor will normally be 0.6 to 0.8 V. The emitter-to-collector voltage of saturated transistors is approximately 0.2 V.

Because these values are small, the best way to check them is by connecting the voltmeter across the junction and using a sensitive voltmeter setting. This method is preferable to comparing two voltages taken with respect to ground (both leads of the voltmeter must be isolated from ground, if this method is used). If values less than those in the preceding paragraph are obtained, either the device is short-circuited or no current is flowing in the circuit. If values are in excess of the base-emitter voltages given, either the junction is back-biased or the device is defective. Values in excess of those given for emitter-collector voltages could indicate either a non-saturated device operating normally or a defective (open-circuited) transistor. If the device is conducting, voltage will be developed across resistors in series with it; if it is open, no voltage will be developed across resistors in series with it unless current is being supplied by a parallel path.

When troubleshooting a field-effect transistor, the voltage across its elements can be checked in the same manner as for a transistor. However, remember that in the normal depletion mode of operation, the gate-to-source junction is reverse biased; in the enhanced mode, the junction is forward biased.

Integrated circuits (IC) can be checked either with a voltmeter, test oscilloscope, or by direct substitution. A good understanding of circuit operation is essential to troubleshooting circuits having IC. Use care when checking voltages and waveforms around the IC so that adjacent leads are not shorted together. Typical semiconductor lead configurations are shown at the beginning of the Diagrams section in Volume II.

CAUTION

Do not use an ohmmeter scale that has a high internal current. High current may damage the diode. Do not measure tunnel diodes with an ohmmeter; use a dynamic tester (such as a TEKTRONIX Type 576 Transistor-Curve Tracer). Checks on diodes can be performed in much the same manner as on transistor emitter-to-base junctions. Silicon diodes should have 0.6 to 0.8 V across the junction when conducting. Higher readings indicate that they are either back biased or defective, depending on polarity.

DIODES. A diode can be checked for an open or a short circuit by measuring the resistance between terminals with an ohmmeter set to the R X 1k scale. The diode resistance should be very high in one direction and very low when the meter leads are reversed. Do not check tunnel diodes or back diodes with an ohmmeter.

RESISTORS. Check resistors with an ohmmeter. Refer to the Replaceable Electrical Parts List in Volume II for tolerance of resistors used in this instrument. Resistors normally do not require replacement unless the measured value varies widely from the specified value.

INDUCTORS. Check for open inductors by checking continuity with an ohmmeter. Shorted or partially shorted inductors can usually be found by checking the waveform response when high-frequency signals are passed through the circuit.

NOTE

Some coils are wound on high ohmic value resistors. If one of these coils is checked, an open is indicated by a high measured-resistance value.

CAPACITORS. A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter on the highest scale. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after initial charge of the capacitor. An open capacitor can be detected with a capacitance meter or by checking whether the capacitor passes ac signals.

ATTENUATORS. The thick film attenuators are best checked by substitution. If only one channel of the 468 is not operating properly and there is reason to believe an attenuator is defective, replace the suspected attenuator with the same attenuator from the other channel; then recheck instrument operation. If proper operation results, replace the defective attenuator.

Repair and Readjust the Circuit

If any defective parts are located, follow the replacement procedures given in this section. Be sure to check the performance of any circuit that was repaired or that had any electrical components replaced. Readjustment of the affected circuit may be necessary. Refer to Table 4-9 in the "Adjustment Procedure" of this manual for possible adjustment interaction.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and instrument repair. Special techniques required to replace components in this instrument are given here.

MAINTENANCE PRECAUTIONS

To reduce the possibility of personal injury or instrument damage, observe the following precautions.

1. Disconnect the instrument from the ac-power source before removing or installing components.

2. Use care not to interconnect instrument grounds which may be at different potentials (cross grounding).

3. Do not use excessive heat when soldering, since circuit boards and semiconductors can be damaged.

STATIC-SENSITIVE COMPONENTS

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 5-2 for various classes of semiconductors and relative susceptibilities to damage. Static voltages of 1 kV to 30 kV are common in unprotected environments.

Observe the following precautions to avoid damage.

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive assemblies or components.

3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by the body, never by the leads.

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground to resolder components.

10. Use only approved anti-static vacuum-type desoldering tools for component removal from multilayered boards.

Table 5-2

Relative Susceptibility to Static Discharge Damage

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFET	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a]**Voltage equivalent for levels:**

1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V (est)
2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
3 = 250 V 6 = 600 to 800 V 9 = 1200 V
(Voltage discharged from a 100-pF capacitor through a resistance of 100 ohms.)

OBTAINING REPLACEMENT PARTS

Standard Parts

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, you should be able to obtain many of the standard electronic components from a local commercial source in your area. Before you purchase or order a part from a source other than Tektronix, Inc., please check the Replaceable Electrical Parts List for the proper value, rating, tolerance, and description.

NOTE

Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special Parts

In addition to the standard electronic components, some special components are used in the 468. These components are manufactured or selected by Tektronix, Inc. to meet specific performance requirements, or are manufactured for Tektronix, Inc. in accordance with our specifications (see Cross Index—Manufacturers Code Number to Manufacturer in Replaceable Electrical Parts List for code numbers). Most of the mechanical parts used in this instrument have been manufactured by Tektronix, Inc. Order all special parts directly from your local Tektronix Field Office or representative.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., it is imperative that all of the following information be included in order to ensure receiving the proper parts.

1. Instrument type (include modification or option numbers).

2. Instrument serial number.

3. A description of the part (if electrical, include the circuit number).

4. Tektronix part number.

SOLDERING TECHNIQUES

WARNING

To avoid an electric-shock hazard, disconnect the instrument from the ac-power source before attempting to solder in the instrument.

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used to remove or replace parts.

Desoldering and removing parts from multilayer circuit boards is especially critical and should be done only with a vacuum-type solder extractor. Many of the integrated circuits are static sensitive and can be damaged by a static charge that may be generated by some types of solder extractors. Use only an anti-static type of solder extractor approved by a Tektronix, Inc. Service Center for work involving static-sensitive devices.

Use rosin-core wire solder containing 63% tin and 37% lead. Contact your local Tektronix, Inc. Field Office or representative to obtain the names of approved solder types.

Circuit boards in this instrument have as many as six conductive layers. Conductive paths between the top and bottom board layers may connect one or more of the inner layers. If any inner-layer conductive path becomes broken due to poor soldering practices, the board becomes unusable and must be replaced. Damage of this nature can void the instrument warranty.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum-type desoldering equipment, should attempt repair of any circuit board in this instrument. The following multilayer board assemblies are particularly susceptible to heat damage: A16, A17, A18, A19, and A21.

When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron can cause etched circuit conductors to separate from the board base material and melt the insulation on small wires. Always keep the soldering-iron tip properly tinned to ensure the best heat transfer from the iron tip to the solder joint. Apply only enough heat to make a good solder joint. To protect heat-sensitive components, either hold the component lead with a pair of long-nose pliers or place a heat block between the component body and the solder joint.

CAUTION

Attempts to unsolder, remove, and resolder leads from the component side of the circuit board may cause damage to the reverse side of the circuit board.

The following technique should be used to replace a component on any of the circuit boards:

1. Touch the vacuum desoldering tool to the lead at the solder connection. Never place the iron directly on the board; doing this may damage the board.

NOTE

Some components are difficult to remove from the circuit board due to a bend placed in each lead during machine insertion of the component. The purpose of the bent leads is to hold the component in position during a flow-solder manufacturing process that solders all the components at once. To make removal of machine-inserted components easier, straighten the component leads on the reverse side of the circuit board with a small screwdriver or pliers. It may be necessary to remove the circuit board to gain access to the component leads on the reverse side of the circuit boards. Circuit-board removal and reinstallation procedures are discussed later in this section.

2. When removing multipin components, especially IC, do not heat adjacent conductors consecutively. Apply heat to pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

CAUTION

Excessive heat can cause the etched circuit conductors to separate from the circuit board. Never allow the solder extractor tip to remain at one place on the board for more than three seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for desoldering multipin components) must not be used. Damage caused by poor soldering techniques can void the instrument warranty.

3. Bend the leads of replacement components to fit the holes in the circuit board. If the component is replaced while the board is installed in the instrument, cut the leads so they only just protrude through the reverse side of the circuit board. Excess lead length may cause shorting to other conductive parts.

4. Insert the leads into the holes of the board so that the replacement component is positioned the same as the original component. Most components should be firmly seated against the circuit board.

CAUTION

Do not allow solder or solder flux to flow beneath etched circuit board switches. The etched switch contacts on the circuit board are an integral part of the switch, and intermittent operation can occur if the contacts become contaminated.

5. Touch the soldering iron to the connection and apply enough solder to make a firm solder joint. Do not move the component while the solder hardens.

6. Cut off any excess leads protruding through the circuit board (if not clipped to size in step 3).

7. Clean the area around the solder connection with an approved flux-removing solvent. Be careful not to remove any of the printed information from the circuit board.

When soldering to the ceramic strips in the instrument, a slightly larger soldering iron can be used. It is recommended that a solder containing about 3% silver be used when soldering to these strips to avoid destroying the bond to the ceramic material. This bond can be broken by repeated use of ordinary tin-lead solder or by the application of too much heat; however, occasional use of ordinary solder will not break the bond, if excessive heat is not applied.

If it becomes necessary to solder in the general area of any of the high-frequency contacts in the instrument, clean the contacts immediately upon completion of the soldering. Refer to the "Switch Contacts" paragraph in the "Preventive Maintenance" part of this section for recommended cleaners and procedures.

REMOVAL AND REPLACEMENT INSTRUCTIONS

WARNING

To avoid electric shock, disconnect the instrument from the power input source before removing or replacing any component or assembly.

The exploded view drawing associated with the Replaceable Mechanical Parts list in Volume II may be helpful in the removal or disassembly of individual components or subassemblies. Component locations are shown in the Diagrams section. The maintenance aids listed in Table 5-3 include items required for some of the maintenance procedures in this instrument. Equivalent products may be substituted for the examples given, provided the characteristics are similar.

CABINET REMOVAL

The instrument cabinet can be removed and reinstalled in the following manner:

1. Disconnect the instrument from its ac-power-input source.

2. Install the front-panel cover, place the cabinet handle against the bottom of the cabinet, and set the instrument face down on a flat surface.

3. Unwrap the power cord from the instrument feet and detach it from the instrument.

4. Remove six screws (indicated in Figure 5-4) holding the rear cabinet frame and remove the frame with feet and screws from the instrument as an assembly.

5. Slide the cabinet up over the main chassis assembly until it is separated from the instrument.

WARNING

Dangerous potentials exist at several points throughout this instrument. If it is operated with the cabinet removed, do not touch exposed connections or components. Some transistors may have elevated cases. Disconnect the ac-power-input source from the instrument before cleaning the instrument or replacing parts.

Table 5-3

Maintenance Aids

Description	Specifications	Usage	Example
1. Soldering Iron	15 to 25 W.	General soldering.	Antex Precision Model C.
2. Screwdriver	Phillips #1 tip.	Assembly and disassembly.	Xcelite Model X108.
3. Screwdriver	Phillips #2 tip.	Assembly and disassembly.	Xcelite Model X102.
4. Screwdriver	Three-inch shaft; 3/32-inch flat bit.	Assembly and disassembly.	Xcelite Model R3323.
5. Service ROM and Test Counter IC	Servicing accessory package.	Signature analysis and troubleshooting.	Tektronix Part Number 067-0989-00.
6. Nutdrivers	1/4 inch, 5/16 inch, 3/8 inch, 7/16 inch.	Assembly and disassembly.	Xcelite #8, #10, #12, and #14.
7. Open-end Wrenches	1/4 inch, 5/16 inch, 9/16 inch.	Assembly and disassembly.	
8. Allen Wrenches	1/16 inch, 5/64 inch, 0.050 inch.	Assembly and disassembly.	
9. Vacuum Solder Extractor	No static charge retention.	Unsoldering static-sensitive devices and components on multilayer boards.	Pace Model PC 10.
10. Lubricant	Versilube.	Switch lubrication.	Tektronix Part Number 006-1353-00.
11. Spray Clearner	No Noise.	Switch pad cleaning.	Tektronix Part Number 006-0442-02.
12. Air Filter Adhesive		Coating air filter after cleaning.	Tektronix Part Number 006-0580-00.
13. IC-Removal Tool		Removing DIP IC packages.	Augat T114-1.
14. IC Test Clip	14/16-, 20-, 24-, and 40-lead testers.	Testing DIP IC packages.	Tektronix Part Number 015-0330-00; Pomona DIP Clip Adapter Models 4124-A, 4140; AP Products Model TC16.

CABINET INSTALLATION

The instrument cabinet can be reinstalled in the following manner:

1. Disconnect the instrument power cord from the ac-power-input source and detach the cord from the instrument.

2. If parts were removed or replaced, check all sections of the instrument for proper assembly. It may be helpful to refer to the exploded view in the "Replaceable Mechanical Parts" section of Volume II of this manual to aid in verifying the complete assembly of the instrument.

3. Install the front cover and set the instrument face down on a flat surface.

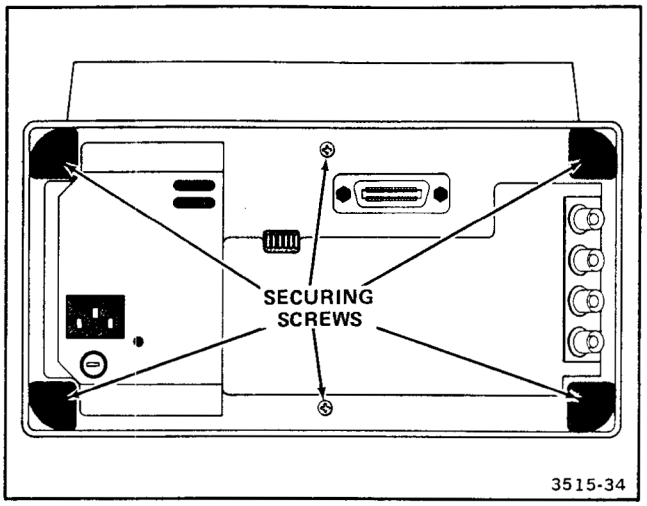


Figure 5-4. Removing the wrap-around cabinet.

4. Place the cabinet handle against the bottom of the cabinet.

5. Carefully slide the cabinet over the instrument. Avoid pinching cables or damaging components that protrude from the circuit boards.

6. Using both hands, press lightly on the top, bottom, and sides of the cabinet until the cabinet front edge is inserted into the groove around the front cabinet frame.

7. Set the feet and screws into place and with one hand exert a light downward pressure on the rear cabinet panel. Press lightly on the top and bottom of the cabinet with the other hand, while checking that the cabinet edge is properly seated in the gasket groove of both the front and rear frames. Continue to exert a downward pressure and tighten the six screws of the rear frame to a snug fit. Do not overtighten these screws.

8. Reattach the instrument power cord.

CIRCUIT BOARDS

Occasionally it may be necessary to gain access to the reverse side of a circuit board or to remove one circuit board to gain access to another. The following procedures outline the necessary steps to facilitate instrument disassembly and reassembly. Most of the connections to the circuit boards in the instrument are made with pin connectors. However, some connections are soldered to the board. Observe the soldering precautions given under "Soldering Techniques" in this section.

Storage Display Circuit Board, Assembly A16

The Storage Display circuit board can be removed and reinstalled as follows:

1. Disconnect nine miniature coaxial connectors from the Storage Display circuit board. Note the cable color codes and locations to aid in proper installation during reassembly. The cable color code numbers are printed on the circuit board adjacent to each connector. Verify the color and location from the following list:

a. J158, white with yellow and black stripes.

b. J172, white with an orange stripe.

c. J262, white with orange and black stripes.

d. J449, white with blue and black stripes.

e. J486, white with green and black stripes.

f. J583, white with orange and black stripes.

g. J586, white with yellow and black stripes.

h. J683, white with brown and black stripes.

i. J686, white with red and black stripes.

2. Disconnect P204 and P404 (connected to the Vertical Mode Switch and Attenuator circuit board).

3. Disconnect P262 (connected to CH 1 and CH 2 POSITION controls).

4. Disconnect the 50-conductor ribbon cable by pulling it straight out from connector P138. Note the location of the edge stripe for later reinstallation.

5. Remove four Phillips-head screws retaining the mounting bracket to the main frame and lift the Storage Display circuit board, with bracket, from the instrument.

Reinstall the Storage Display circuit board into the instrument using the following steps:

6. Align the holes for the four retaining screws and install the screws.

7. Reconnect the ribbon cable. Align the edge stripe, as noted in step 4, and insert it into connector P138.

8. Reconnect P204 and P404 (from the Vertical Mode Switch circuit board).

9. Reconnect nine miniature coaxial connectors (disconnected in step 1).

10. Reconnect P262 (from the CH 1 and CH 2 POSITION controls).

Vertical Preamplifier Circuit Board, Assembly A11

The Vertical Preamplifier circuit board must be removed to gain access to the High-Voltage Multiplier, the High-Voltage Transformer, and the High-Voltage Oscillator power transistor. Removal and reinstallation of the Vertical Preamplifier circuit board is accomplished as follows:

1. Use a 0.050-inch Allen wrenth to loosen the front set screws of the Vertical VOLTS/DIV VAR shaft coupler and slide the shafts out of the instrument.

2. Disconnect the INVERT and 20 MHz BW LIMIT push-button extension shafts from the switch shafts. Insert a scribe or a similar tool in the notch between the end of the white plastic shaft and the end of the black plastic extension shaft. Then, gently pry the shaft and extension apart.

3. Disconnect 14 miniature coaxial cables from the Preamplifier circuit board. Note the cable color codes and locations to aid in proper connection during reassembly. The cable color code number is printed on the circuit board next to each connector. Verify the wire color and cable number from the following list:

a. J103, white with a purple stripe.

b. J104, white with a brown stripe.

c. J105, white with yellow and black stripes.

d. J107, white with red and black stripes.

e. J123, white with orange and black stripes.

f. J133, white with green and black stripes.

g. J204, white with blue and black stripes.

h. J218, white with yellow and black stripes (located approximately two inches from the rear edge of the board).

i. J500, white with an orange stripe.

j. J501, white with a red stripe (located at the rear edge of the board near the bottom).

k. J502, white with a gray stripe.

l. J523, white with a red stripe (located near the bottom of the board approximately two inches from the rear).

m. J535, white with gray and black stripes.

n. J536, white with purple and black stripes.

4. Disconnect the following wires and connectors from the Preamplifier circuit board (note location of each for reassembly reference):

a. Unplug the delay line from the end of the Preamplifier circuit board (located toward the rear of the circuit board).

b. Unsolder the ground braid (located near the High-Voltage Power-Supply shield) connection between the Preamplifier circuit board and the Interface board. (Unsolder the end of the braid attached to the Preamplifier circuit board.)

c. P356, a three-wire connector near the middle of the Preamplifier circuit board (connected to the Interface circuit board).

d. P306, an eight-wire connector near the rear of the Preamplifier circuit board (from the Vertical Mode Switch circuit board).

e. P138 and P343, both three-wire connectors near the CH 1 and CH 2 POSITION potentiometers (connected to the Storage Display circuit board).

5. Unsolder two 30-Ω resistors (R3045) that connect the CH 1 and CH 2 Attenuator Assemblies to the Preamplifier circuit board.

6. Remove five circuit board securing screws from the circuit board (two at the rear, two closest to the middle at the front, and the first one back from the front on the top) and a standoff with grounding clip attached (near P356). (The remaining screws retain the shield on the reverse side of the circuit board).

7. Separate the board from the instrument by carefully pulling out on the rear of the board to clear the front. Then remove the circuit board from the instrument.

Reinstall the Vertical Preamplifier circuit board into the instrument using the following steps:

8. Place the circuit board into position and reinstall five Phillips-head screws and one standoff post, with grounding clip (removed in step 6).

9. Resolder the two resistors that connect the CH 1 and CH 2 Attenuator assemblies to the Preamplifier circuit board.

10. Reconnect the 14 miniature cables disconnected in step 3.

11. Reconnect the following wires and connectors:

a. The delay-line connector at the end of the Preamplifier circuit board.

b. Ground braid connecting the Preamplifier to the Interface circuit board.

c. P356, a three-wire connector near the middle of the Preamplifier circuit board.

d. P306, an eight-wire connector near the rear of the Preamplifier circuit board.

e. P138 and P343, both three-wire connectors near the CH 1 and CH 2 POSITION potentiometers (from the Storarage Display circuit board).

12. Align the extension shafts of both the INVERT and 20 MHz BW LIMIT switch shafts and gently press them together until they snap into position.

13. Insert the VOLTS/DIV VAR control shafts into the couplers and use a 0.050-inch Allen wrench to tighten the front set screws.

Vertical Mode Switch Circuit Board, Assembly A14

The Vertical Mode Switch circuit board and the Attenuator circuit boards can be removed and reinstalled using the following procedure:

1. Remove the Vertical Preamplifier circuit board using the previously described procedure in this section.

2. Use a 1/16-inch Allen wrench to loosen the set screws in both VOLTS/DIV switch knobs and remove the knobs. Note their positions for reinstallation reference.

3. Remove the AC-GND-DC lever switch knobs by grasping them and pulling straight out from the instrument.

4. Remove the 10 Phillips-head screws retaining the Attenuator covers (five in each) and remove the covers.

5. Unplug both input coupling capacitors from the board and gently bend the capacitors out of the way, leaving the lead soldered to the input connector attached.

6. Use a 1/4-inch nut driver to remove the four nuts securing the Attenuator chassis to the front casting of the instrument.

7. Disconnect the following wires and connectors from the Vertical Mode Switch circuit board:

a. P160 (from the Interface circuit board).

b. P196 (from the VOLTS/DIV VAR controls).

c. P1100 (from the CH 1 and CH 2 VOLTS/DIV UNCAL LED).

d. P307 (from the Preamplifier circuit board).

e. P1118 and P1440 (from the Probe Coding circuit boards).

f. P356 (from the Storage Display circuit board).

g. P142 (from the Storage Display circuit board).

h. P190 (from the 20 MHz BW LIMIT LED).

i. P111 (from the Trigger circuit board).

j. P120 and P130 (from the Timing circuit board).

8. Remove four Phillips-head screws and two 1/4-inch standoff posts securing the Vertical Mode Switch circuit board.

9. Lift the Vertical Mode Switch circuit board from the instrument.

Reinstall the Vertical Mode Switch circuit board into the instrument using the following steps:

10. Position the Vertical Mode Switch circuit into place.

11. Reinstall four Phillips-head screws and two 1/4-inch standoff posts (removed in step 8).

12. Reconnect the wires and connectors that were disconnected in step 7.

13. Reinstall four nuts used to secure the Attenuator chassis to the front casting (removed in step 6).

14. Plug in the input coupling capacitors (unplugged in step 5).

15. Replace the attenuator covers, ensuring that the edge-grounding fingers are correctly placed. Exercise care not to bend or break the fingers.

16. Reinstall 10 Phillips-head screws in the Attenuator covers (five in each, small one in front).

17. Reinstall the knobs on the AC-GND-DC lever switches by pushing the knobs onto the levers (removed in step 3).

18. Reinstall the knobs on the VOLTS/DIV controls at the position noted in step 2 and use a 1/16-inch Allen wrench to tighten the set screws.

19. Reinstall the Vertical Preamplifier circuit board using the previously described procedure in this section.

Vertical Output Amplifier Circuit Board, Assembly A23

Remove the Storage Display circuit board using the previously described procedure in this section. Then, the Vertical Output Amplifier circuit board can be removed and reinstalled using the following procedure:

1. Remove the two screws securing the Vertical Output Amplifier shield and lift the shield from the instrument.

2. Disconnect P2495 (near the front edge of the circuit board).

3. Disconnect delay line DL208 (located near the rear edge of the circuit board).

4. Disconnect the two Y-Axis (vertical) deflection lead connectors (close to resistors R156 and R256 near the front of the circuit board) using a pair of long-nose pliers. Pull straight out on these connectors to prevent strain on the metal-to-glass seal on the crt neck. Note the wire color and location for correct reinstallation.

5. Lay the instrument on its Trigger circuit board side and use a 1/4-inch open-end wrench to remove the nut and washer (located on the outside of the crt compartment) used to secure U239 to the main frame.

6. Lay the instrument down on its Interface board side again and remove the two Phillips-head screws securing the Vertical Output Amplifier circuit board to the main chassis.

7. Slide the U239 mounting stud out of the main chassis and lift the circuit board out of the instrument.

Reinstall the Vertical Output Amplifier circuit board into the instrument using the following steps:

8. Position the circuit board into the main chassis crt compartment (insert the U239 mounting stud through the mounting hole in the main chassis) and reinstall two Phillips-head screws (removed in step 6).

9. Lay the instrument on its Trigger board side and reinstall the nut and washer used to secure U239 to the main chassis (removed in step 5).

10. Reconnect the two Y-Axis lead connectors on the neck of the crt at the location noted in step 4.

11. Reconnect delay line DL208 (disconnected in step 3).

12. Lay the instrument back down on its Interface board side and reconnect P2495 (disconnected in step 2).

13. Reinstall the Vertical Output Amplifier shield using two Phillips-head self-tapping screws (removed in step 1).

14. Reinstall the Storage Display circuit board using the previously described procedure in this section.

Trigger Circuit Board, Assembly A12

The Trigger circuit board can be removed and reinstalled using the following procedure:

1. Insert a scribe, or similar tool, in the notch between the POWER-switch-extension shaft and the switch shaft and gently pry them apart. The shaft extension remains in place until the circuit board is separated from the instrument.

2. Disconnect the following connectors from the Trigger circuit board:

a. P110 (from the POWER LED).

b. P112 (from the B DLY'D TRIGGER SLOPE and LEVEL control).

c. P160 (from the main wiring harness).

d. P310 (from the READY and TRIG LED).

e. P410 (from the A TRIGGER SLOPE and LEVEL control).

f. P483 (from the Memory circuit board).

g. P493 (from the Vertical Mode Switch circuit board).

h. P3008 (from the power transformer secondary windings).

i. P4008 (from the Storage Power Supply).

3. Unsolder the wire from both the EXT A TRIGGER input connector and the EXT B TRIGGER input connector.

4. Disconnect eight miniature coaxial connectors. Note their circuit numbers and verify their wire colors and locations for correct reinstallation.

a. J183, white with a blue stripe.

b. J188, white with a yellow stripe.

c. J190, white with a green stripe.

d. J210, white with a brown stripe.

e. J219, white with a red stripe.

f. J227, white with an orange stripe.

g. J533, white with brown and black stripes.

h. J540, white with red and black stripes.

5. Set both SOURCE (A and B) and both COUPLING (A and B) switch levers to approximately midrange.

6. Remove four Phillips-head screws and one standoff post (near P160) that secure the Trigger circuit board to the main chassis.

7. Use a flat-bit screwdriver to gently pry the Trigger circuit board away from the Interface circuit board until the pins of J560 and J580 are disengaged from P944 and P970 on the Interface board.

8. Slide the Trigger circuit board toward the rear of the instrument until the SLOPE and COUPLING switch lever and the POWER-switch-extension shaft clear the front panel; then lift the board from the instrument.

Reinstall the Trigger circuit board into the instrument using the following steps:

9. Align the SOURCE and COUPLING switch levers and the POWER-switch-extension shaft with the corresponding holes in the front panel and position the circuit board in place.

10. Carefully mate the pins of J560 and J580 with the connectors on the Interface board and press them together until they are fully engaged.

11. Reinstall four Phillips-head retaining screws and one 1/4-inch standoff post (removed in step 6).

12. Reconnect the eight miniature coaxial connectors that were disconnected in step 4.

13. Resolder the wires to both the EXT A TRIGGER and the EXT B TRIGGER input connectors.

14. Reconnect the connectors that were disconnected in step 2.

15. Use a flat-bit screwdriver to fully hold in the POWER switch while aligning the POWER-switch-extension shaft with the switch shaft. Gently press them together until they snap into position.

Timing Circuit Board, Assembly A13

To access the Timing circuit board, both the Trigger circuit board and the Storage Display circuit board must first be removed using the previously described procedures in this section. Then remove and reinstall the Timing circuit board using the following procedure:

1. Disconnect the following connectors from the Timing circuit board:

a. P111 (from the X10 MAG and UNCAL LED).

b. P117 (from the DELAY TIME POSITION potentiometer).

c. P129 (from the main wiring harness).

d. P135 and P146 (from the Vertical Mode Switch circuit board).

2. Use a 1/16-inch Allen wrench to loosen the set screw of the TIME/DIV VAR knob and remove the knob.

3. Rotate the A and B TIME/DIV switch knobs until the shaft-coupling set screws are accessible (inside the instrument). Note the position of the A and B TIME/DIV control knobs for reinstallation reference (this is important to obtain the correct alignment during reinstallation).

4. Use a 1/16-inch Allen wrench to loosen the two set screws holding the A TIME/DIV knob and remove the knob from the shaft.

5. Use a 5/64-inch Allen wrench to loosen the two shaft-coupling set screws on the B TIME/DIV control shaft. Then use a flat-bit screwdriver between the coupling and switch housing to gently pry the control knob (clear plastic) from the instrument. Retain the black front-panel spacer for reinstallation.

6. Remove the Phillips-head screw located towards the front of the board.

7. Use a 3/16-inch nutdriver to remove the standoff post located near the rear of the board.

8. Gently lift the Timing circuit board up, separating the pins of P524 and P555 from J885 and J887 on the Interface board.

9. Pull the Timing circuit board to the rear until the push buttons of the HORIZ DISPLAY and TRIG MODE switches clear the front panel and lift the circuit board from the instrument.

Reinstall the Timing circuit board into the instrument using the following steps:

10. Insert the push buttons of the HORIZ DISPLAY and TRIG MODE switches through the corresponding holes in the front panel.

11. Carefully mate the pins of P524 and P555 with J885 and J887 on the Interface board and press them together until fully engaged.

12. Reinstall the 3/16-inch standoff post (removed in step 7).

13. Reinstall the Phillips-head screw (removed in step 6).

14. Reinstall the B TIME/DIV knob at the position noted in step 3 and use a 5/64-inch Allen wrench to tighten the set screws in the shaft coupling.

15. Reinstall the A TIME/DIV knob at the position noted in step 3 and use a 1/16-inch Allen wrench to tighten the set screws in the knob.

NOTE

Check the alignment of the knobs over their full rotation and reposition them slightly, if necessary, to obtain the correct alignment with the front-panel numbers.

16. Reinstall the TIME/DIV VAR knob and use a 1/16-inch Allen wrench to tighten the set screw.

17. Reconnect the connectors disconnected in step 1.

18. Reinstall the Trigger circuit board and the Storage circuit board using the previously described procedures in this section.

Microprocessor Circuit Board, Assembly A21

The Microprocessor circuit board may be removed and reinstalled using the following procedure:

1. Detach the power cord (if not previously removed) and remove two Phillips-head screws securing the rear panel of the instrument.

2. Disconnect the 50-conductor ribbon cable from P152 and P130 (located on the Memory circuit board and Microprocessor circuit board, respectively, in the rear frame assembly). Note the location of the edge stripe on the cable for correct reinstallation.

3. Remove four large Phillips, flat-head screws from the top of the rear chassis assembly.

4. Slide the rear chassis assembly to the rear until all of the components are clear of the main chassis.

5. Lift the rear chassis assembly and rotate it 180 degrees. Place it on top of the main chassis and align the two innermost mounting holes with the corresponding threaded inserts on the main chassis. Then reinstall two of the screws removed in step 3 into the threaded inserts to hold the rear chassis assembly in place.

6. Lift the Interconnect board straight up to disconnect it from P278 (on the Memory circuit board) and from P206 (on the Microprocessor circuit board).

7. Disconnect the following five miniature coaxial connectors located at the lower-right corner of the Microprocessor circuit board. Verify the cable color code and location of each cable for reinstallation reference.

a. J107, white with green and black stripes.

b. J110, white with blue and black stripes.

c. J112, white with purple and black stripes.

d. J118, white with gray and black stripes.

e. J120, white with orange and black stripes.

8. Remove five Phillips-head screws securing the Microprocessor circuit board and lift the board from the instrument.

Reinstall the Microprocessor circuit board into the instrument using the following steps:

9. Position the board in place and reinstall five Phillips-head securing screws (removed in step 8).

10. Reconnect five miniature coaxial cables (disconnected in step 7).

11. Reconnect the Interconnect board into the pins of P278 (located on the Memory circuit board) and P206 (located on the Microprocessor circuit board).

12. Remove two Phillips-head screws securing the rear chassis to the main chassis.

13. Lift the rear chassis assembly, rotate it 180 degrees downward, and slide it into the main chassis until the mounting-screw holes are aligned.

14. Reinstall four Phillips-head screws (removed in step 3) into the top of the rear chassis assembly.

15. Reconnect the 50-conductor ribbon cable to P130 (on the Microprocessor circuit board) and to P152 (on the Memory circuit board).

16. Reinstall two Phillips-head screws in the rear panel (removed in step 1).

Memory Circuit Board, Assembly A18

The Memory circuit board can be removed and reinstalled using the following procedure:

1. Detach the power cord (if not previously removed) and remove two Phillips-head screws securing the rear panel to the instrument.

2. Disconnect the 50-conductor ribbon cable from P152 (on the Microprocessor circuit board) and from P130 (on the Memory circuit board). Note the location of the edge stripe for reinstallation.

3. Remove four Phillips, flat-head screws from the top of the rear chassis assembly.

4. Slide the rear chassis assembly to the rear until all of the components are clear of the main chassis.

5. Lift the rear chassis assembly and rotate it 180 degrees. Place it on top of the main chassis and align the two innermost mounting holes with the corresponding threaded inserts on the main chassis. Then reinstall two of the screws removed in step 3 to hold the rear chassis assembly in place.

6. Lift the Interconnect board straight up to disconnect it from P278 (on the Memory circuit board) and from P206 (on the Microprocessor circuit board).

7. Remove two Phillips-head screws (one from each side) holding the hinged bracket in place and rotate the bracket down approximately 90 degrees.

8. Disconnect five 10-wire connectors located across the bottom of the circuit board. Exercise care to maintain the lead spacing and dress of the wiring and pins on the circuit board.

9. Disconnect P160, a two-wire connector at the bottom of the board.

10. Remove five Phillips-head securing screws and remove the Memory circuit board from the instrument.

Reinstall the Memory circuit board into the instrument using the following steps:

11. Position the circuit board into place and reinstall five securing screws (removed in step 10).

12. Reconnect P160, a two-wire connector (disconnected in step 9).

13. Reconnect the five 10-wire connectors (disconnected in step 8). Retain the original lead spacing and arrangement of the wiring harnesses and circuit-board pins.

14. Rotate the hinged bracket up approximately 90 degrees until the securing-screw holes are aligned and reinstall two Phillips-head screws (removed in step 7).

15. Reinstall the Interconnect circuit board into the pins of P278 (on the Memory circuit board) and P206 (on the Microprocessor circuit board).

16. Remove two Phillips-head screws holding the rear chassis to the main chassis.

17. Lift the rear chassis assembly, rotate it 180 degrees downward, and slide it into the main chassis until the mounting-screw holes are aligned.

18. Reinstall four Phillips-head screws into the rear chassis assembly mounting holes.

19. Reconnect the 50-conductor ribbon cable to P130 and P152, with the edge stripe positioned as noted in step 2.

20. Position the rear panel into place and reinstall two Phillips-head screws (removed in step 1).

Time Base/Power Supply Circuit Board, Assembly A19

The Time Base/Power Supply circuit board can be removed and reinstalled using the following procedure:

1. Detach the power cord (if not previously removed) and remove two Phillips-head screws securing the rear panel.

2. Disconnect the 50-conductor ribbon cable from P152 (on the Memory circuit board) and from P130 (on the Microprocessor circuit board). Note the location of the edge stripe for reinstallation reference.

3. Remove four Phillips-head screws from the top of the rear chassis assembly.

4. Slide the rear chassis assembly to the rear until all of the components are clear of the main chassis.

5. Lift the rear chassis assembly and rotate it upward 180 degrees. Place it on top of the main chassis and align the two innermost mounting holes with the corresponding threaded inserts on the main instrument chassis. Then reinstall two of the screws removed in step 3 to hold the rear chassis assembly in place.

6. Remove two Phillips-head screws (one on each side) holding the hinged bracket in position and rotate the bracket down approximately 90 degrees.

7. Disconnect the five 10-wire connectors located across the bottom of the Time Base/Power Supply circuit board. Exercise care to retain the original lead dress and spacing of the wiring harness and pin connectors.

8. Disconnect the following four miniature coaxial connectors located at the lower right side of the circuit board. Note the cable color code and location of each connector for reinstallation reference.

a. J101, white with a yellow stripe (from the main wiring harness).

b. J105, white with a green stripe (from the main wiring harness).

c. J110, white with a yellow stripe (from the A + GATE bnc connector on the rear chassis assembly).

d. J115, white with a green stripe (from the B + GATE bnc connector on the rear chassis assembly).

9. Disconnect P140 (a 16-wire connector from P265 of the GPIB Option circuit board, if installed).

10. Disconnect P380 (a two-wire connector from the Fan motor).

11. Disconnect P199 (a five-wire connector from the Trigger circuit board).

12. Use a 3/16-inch wrench and a Phillips-tip screwdriver to remove the nut and screw retaining the three-terminal regulator on each of the power supplies. U190 is located near the power-supply shield, and both U560 and U570 are mounted on the top of the rear chassis assembly (as viewed in the servicing position).

13. Pull straight out on the three-terminal regulators to remove them from their sockets. Note their type and location for reinstallation reference.

14. Remove 10 Phillips-head securing screws from the circuit board. The hinged bracket must be pushed into its fully up position to reach the bottom-middle securing screw (in the edge of the power-supply shield).

15. Slide the Time Base/Power Supply circuit board out of the right side of the rear chassis assembly (as viewed from the front of the instrument) to remove it.

Reinstall the Time Base/Power Supply circuit board in the instrument using the following steps:

16. Slide the circuit board into position and reinstall 10 Phillips-head screws (removed in step 14).

NOTE

When installing the three-terminal regulators (U190, U560, and U570), ensure that there is a mica insulator and silicone grease (or similar thermal-transfer compound) between the regulators and chassis ground.

WARNING

Handle silicone grease with care. Avoid getting silicone grease in the eyes. Wash hands thoroughly after use.

17. Insert the three-terminal regulators into their sockets at the locations noted in step 13 and reinstall the Phillips-head securing screws with the hex nuts (removed in step 12).

18. Reconnect P199 (five-wire connector from the Trigger circuit board).

19. Reconnect P380 (two-wire Fan lead connector).

20. Reconnect P140 (16-wire connector from the GPIB Option circuit board, if installed).

21. Reconnect four miniature coaxial connectors (removed in step 8).

22. Reconnect the five 10-wire connectors across the bottom of the Time Base/Power Supply circuit board. Retain the original lead spacing and arrangement of the wiring harness.

23. Push the hinged bracket into the fully up position to align the securing screw holes and reinstall two Phillips-head screws (one in each side).

24. Reinstall the Interconnect board into the pins of P278 (on the Memory circuit board) and P206 (on the Microprocessor circuit board).

25. Remove two Phillips-head screws holding the rear chassis to the main chassis.

26. Lift the rear chassis assembly and rotate it 180 degrees downward. Slide it into the main chassis until the securing-screw holes are aligned and reinstall four Phillips-head screws (removed in step 3).

27. Reconnect the 50-connector ribbon cable to P130 (on the Microprocessor circuit board) and to P152 (on the Memory circuit board), with the edge stripe positioned as noted in step 2.

28. Install two Phillips-head securing screws in the rear panel (removed in step 1).

GPIB Option Circuit Board, Assembly A17

The GPIB Option circuit board can be removed and reinstalled using the following procedure:

1. Disconnect P265, located near the right edge of the circuit board.

2. Remove four Phillips-head retaining screws and lift the board from the instrument.

Reinstall the GPIB Option circuit board in the instrument using the following steps:

3. Position the board and reinstall four Phillips-head securing screws (removed in step 2).

4. Reconnect P265.

Interface Circuit Board, Assembly A15

If repair of a circuit board run on the reverse side of the Interface circuit board is necessary, it is usually possible to gain access to that area of the board by removing one or two of the other circuit boards as previously described. Other than repairing a damaged run, there is no reason to remove the Interface circuit board except for exchange.

CAUTION

If the Interface circuit board becomes defective, it is recommended that your local Tektronix Field Office or representative be contacted to arrange for instrument repair at a Tektronix Service Center.

Removal and reinstallation of the Interface circuit board can be accomplished using the following procedure:

1. Remove the Trigger circuit board and Vertical Preamplifier circuit board using the previously described procedures in this section.

2. Position the instrument with the front panel to your right and the Interface circuit board facing you.

3. Remove four Phillips-head screws securing the High-Voltage Power-Supply shield and separate the shield from the Interface board. Note the location of the ground spring clip for reinstallation reference.

4. Disconnect the BEAM FIND, INVERT, and X10 MAG push-button extension shafts by inserting a scribe in the notch between the end of the white plastic shaft and the end of the black plastic extension shaft and gently pry them apart. Then, pull the extension shaft out of the front-panel holes toward the rear of the instrument.

5. Use a 0.050-inch Allen wrench to loosen the front set screws of the INTENSITY, FOCUS, SCALE ILLUM, ASTIG, and TRACE ROTATION control shafts. Note the position of each shaft for reinstallation reference and remove the shafts, with knobs attached, from the instrument.

6. Disconnect the following cables and connectors from the Interface circuit board:

a. P108, at the top left corner of the circuit board (from Q1180).

b. P137, near the top center of the circuit board (from the crt socket).

c. P151, near the INTENSITY potentiometer at the top center of the circuit board (from the Vertical Mode Switch circuit board).

d. P154, near the INTENSITY potentiometer at the top center of the board (from the Vertical Preamplifier circuit board).

e. P252, near the INTENSITY potentiometer at the top center of the board (from the Vertical Output Amplifier circuit board).

f. P288, near Q390 (from the graticule lights).

g. P359, near the front of the INTENSITY potentiometer at the top center of the board (from the crt Y-Axis deflection plates).

h. P473, near the TRACE ROTATION potentiometer (from the crt).

i. P799, at the front edge of the board (from the TRACE SEP and HOLDOFF potentiometers).

j. P699, at the front edge of the board (from the horizontal POSITION and B INTENSITY potentiometers).

k. P956, near the bottom center of the board (from the HOLDOFF control).

7. Unsolder the CALIBRATOR loop from the front edge of the Interface circuit board.

8. Unsolder six wires (listed below) from the Interface circuit board. Note each wire's color code and location for reinstallation reference.

a. Wire to the one-notch ceramic strip (white with a yellow stripe).

b. Wire to TP328, the −2450-V test point (white with a red stripe).

c. Wire to the center notch on the three-notch ceramic strip (white with an orange stripe).

d. Lower wire of a pair of wires between the large high-voltage capacitors (white with brown and yellow stripes).

e. Upper wire of a pair of wires between the large high-voltage capacitors (white with a brown stripe).

f. Small wire near VR207 (white with brown and red stripes).

9. Using a pair of long-nose pliers, gently disconnect the horizontal deflection plate lead connectors from the neck of the crt. Pull the connectors straight out from the pins to avoid placing a strain on the metal-to-glass seal. Note the wire's color code and location for reinstallation reference.

a. Right (lower lead) deflection plate lead (white with a green stripe).

b. Left (upper lead) deflection plate lead (white with a red stripe).

10. Disconnect seven miniature-coaxial connectors (listed below) from the Interface circuit board. Verify the cable color code and location of each cable for reinstallation reference.

a. J526, white with black and brown stripes, from the rear center of the circuit board.

b. J683, white with black and red stripes, from near the front of the circuit board.

c. J686, white with a red stripe, from near the front of the circuit board.

d. J687, white with a blue stripe, from near the front of the circuit board.

e. J873, white with an orange stripe, located between interboard connectors J857 and J885.

f. J773, white with black and blue stripes, located above interboard connectors J857 and J885.

g. J750, white with black and green stripes, above and to the left of interboard connectors J857 and J885.

11. Unsolder the center conductor of one miniature-coaxial cable (white with a gray stripe) near the left center of the board. Note the location on the board for reinstallation reference.

12. Remove the mounting screws that secure power transistors Q401, Q501, and Q701 to the main chassis (along the rear of the board).

13. Remove the mounting screw that secures transistor Q718 to the main chassis (near the left center of the board);

14. Remove the mounting screw that secures transistor Q390 to the main chassis (near the top right corner of the board).

15. Use a 3/16-inch nut driver to remove four hexagonal posts (standoffs for the High-Voltage Power-Supply shield).

16. Remove seven Phillips-head securing screws from the Interface circuit board.

17. Remove three Phillips-head screws securing the shield over the High-Voltage Transformer and the High-Voltage Multiplier and remove the shield from the instrument.

18. Unsolder the black wire (connecting the High-Voltage Multiplier to the Interface board).

19. Unsolder the diode and wire from the terminal post on the High-Voltage Multiplier.

20. Use a 3/8-inch wrench to remove two nylon nuts securing the High-Voltage Multiplier to the Interface circuit board.

21. Separate the Interface circuit board from the instrument chassis. Use a flat-bit screwdriver to gently pry the connectors of J857 and J885 away from the Timing circuit board. Exercise care to prevent damage to components and wiring. Carefully thread interconnecting cables through the board and chassis as necessary to avoid any strain on the power transformer leads that are still connected to the circuit board.

NOTE

The preceding steps allow access for repairs on the reverse side of the Interface circuit board. To remove the Interface circuit board, continue with this procedure.

22. Unsolder the power transformer wires from the Interface circuit board. Confirm the color code and location of each wire (see Figure 5-5) for reinstallation reference.

23. Separate the Interface circuit board from the instrument. Exercise care not to damage the cables that must pass through the holes in the circuit board. Note their color, size, and routing for reinstallation reference.

24. Remove any of the components from the old Interface board (such as power transistors and filter capacitors) that are not included on the replacement Interface board. Either install the removed components on the replacement Interface circuit board or install new components.

Install the replacement Interface circuit board using the following steps:

25. Resolder the power transformer wires (disconnected in step 22), referring to Figure 5-5 for their colors and locations.

26. Insert the High-Voltage Multiplier mounting studs into the corresponding holes in the Interface board.

27. Mate Interface board connectors J857 and J885 with the corresponding pins of P524 and P555 on the Timing circuit board and press them together until the pins are fully engaged.

28. Reinstall two nylon securing nuts on the High-Voltage Multiplier (removed in step 20).

29. Resolder the diode and wire to the High-Voltage Multiplier terminal post.

30. Resolder the black wire from the High-Voltage Multiplier to the Interface circuit board.

31. Replace the High-Voltage Multiplier shield and reinstall three Phillips-head screws (removed in step 17).

32. Reinstall seven Phillips-head securing screws (removed in step 16).

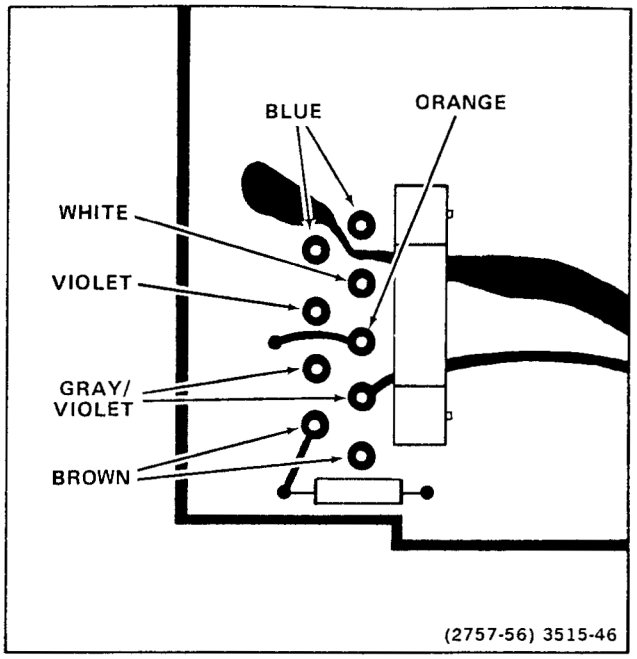


Figure 5-5. Location and color of the power transformer main power supply secondary leads.

33. Reinstall four standoff posts (removed in step 15). Use a 3/16-inch nutdriver to tighten the post.

NOTE

When reinstalling the chassis-mounted power transistors, ensure that there is a mica insulator and silicone grease (or similar thermal-transfer compound) between the transistors and the chassis.

WARNING

Handle silicone grease with care. Avoid getting grease in the eyes. Wash hands thoroughly after use.

34. Reinstall the mounting screw for transistor Q390 (located near the top right corner of the circuit board).

35. Reinstall the mounting screw for transistor Q718 (located near the left center of the board).

36. Reinstall the mounting screws for power transistors Q401, Q501, and Q701 (located along the rear edge of the board).

37. Resolder the center conductor of the miniature-coaxial cable (white with a gray stripe) at the location noted in step 11.

38. Reconnect the seven miniature-coaxial cables (disconnected in step 10).

39. Reconnect two horizontal deflection plate lead connectors (disconnected in step 9) at the locations noted. Push the connectors straight onto the crt pins (until the connectors are seated) to avoid strain on the metal-to-glass seal.

40. Resolder six wires to the Interface circuit board at locations noted in step 8.

41. Resolder the CALIBRATOR loop to the front edge of the Interface circuit board.

42. Reconnect the cables and connectors disconnected in step 6.

43. Reinstall the shafts of the INTENSITY, FOCUS, SCALE ILLUM, ASTIG, and TRACE ROTATION controls oriented as noted in step 5. Use a 0.050-inch Allen wrench to tighten the front set screws.

44. Insert the extension shafts of the BEAM FIND, INVERT, and X10 MAG switches (through the rear of the front panel) into the corresponding front-panel holes. Align the shaft extensions with the switch shafts and gently press them together until they snap into position.

45. Reinstall the High-Voltage Power-Supply shield with four securing screws (removed in step 3). Position the ground clip spring as noted in step 3.

46. Reinstall the Trigger Generator and Vertical Preamplifier circuit boards using the previously described procedures in this section.

CATHODE-RAY TUBE REMOVAL AND REINSTALLATION

The cathode-ray tube (crt) can be removed and reinstalled using the following procedure:

WARNING

Use care when handling a crt. Breakage of the crt may cause high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses should be worn. Avoid striking it on any object which may cause it to crack or implode. When storing a crt, place it in a protective carton or set it face down on a smooth surface in a protective location with a soft mat under the faceplate to protect it from scratches.

1. Remove four screws that secure the plastic bezel and light filter. Remove the bezel and light filter from the instrument.

2. Remove two Phillips-head screws from the rear cover.

3. Remove four Phillips-head screws from the top of the rear chassis assembly.

4. Slide the rear chassis assembly to the rear until all of the components are clear of the main chassis.

5. Lift the rear chassis assembly and rotate it upward 180 degrees. Place it on top of the main chassis and align the two innermost mounting holes with the corresponding threaded inserts on the main chassis. Then reinstall two of the screws removed in step 3 to hold the rear chassis assembly in place.

6. Remove two Phillips-head screws securing the bell-shaped crt socket shield and remove the shield to expose the crt socket.

7. Gently unplug the crt socket by pulling straight toward the rear until all pins are disengaged.

8. Use long-nose pliers to disconnect the two Y-Axis (vertical) deflection pin connectors from the neck of the crt. Pull straight out on these connectors to prevent strain on the metal-to-glass seal. Note the wire color and location for reinstallation reference.

9. Set the instrument on its left side (Vertical Preamplifier circuit board side down).

10. Use long-nose pliers to disconnect the two X-Axis (horizontal) deflection pin connectors from the neck of the crt. Pull straight out on these connectors to prevent strain on the metal-to-glass seal. Note the wire color and location for reinstallation reference.

11. Position the instrument so that the top is accessible.

WARNING

The crt anode and the output terminal of the High-Voltage Multiplier may retain a high-voltage charge after the instrument is turned off. To avoid electrical shock, ground both the output terminal of the multiplier and the crt high-voltage anode lead to the main instrument chassis when disconnecting the high-voltage lead.

12. Disconnect the anode lead connector (held in place by a metal retaining clip fastened to the chassis). Pull the top portion of the anode lead out of the connector (where the connector plugs together, just above the retaining clip) and discharge it to the chassis.

13. Hold the crt face with one hand and slowly push on the crt base with the other hand to remove the crt through the front of the instrument. Guide the anode lead through the front crt shield. If the plastic crt corner pads fall out, save them for reinstallation. (These pads hold the front corners of the crt in place.) Exercise care not to damage or move the Y-Axis coil that is mounted in the crt rear shield.

Reinstall the crt into the instrument using the following steps:

14. Insert the crt through the front of the instrument. While pushing gently on the crt face, guide the anode lead through the crt shield. Reinstall any plastic crt corner pads that may be out of place. Do not damage or move the Y-Axis coil mounted in the crt rear shield.

a. Ensure that the plastic corner pads are securely seated.

b. Ensure that the plastic spacer ring is firmly centered on the crt neck. Reposition the ring if necessary.

15. Reconnect the crt anode lead connector to the jack from the High-Voltage Multiplier.

16. Reinstall the X- and Y-Axis deflection pin connectors at the locations noted in steps 8 and 10. Gently push the connectors straight onto the crt neck pins to prevent strain on the metal-to-glass seal.

17. Align the index slot of the crt socket with the index guide on the crt base and press the socket in place.

18. Reinstall the bell-shaped crt socket shield using two screws (removed in step 6).

19. Remove two screws holding the rear chassis assembly, rotate it 180 degrees, and slide it into the main chassis until the mounting-screw holes are aligned.

20. Reinstall four Phillips-head screws (removed in step 3).

21. Reinstall the rear cover with two screws (removed in step 2).

22. Reinstall the plastic bezel and light filter on the front of the instrument with four screws (removed in step 1).

HIGH-VOLTAGE MULTIPLIER REMOVAL AND REINSTALLATION

The High-Voltage Multiplier can be removed and reinstalled using the following procedure:

WARNING

The crt anode and the output terminal of the High-Voltage Multiplier may retain a high-voltage charge after the instrument is turned off. To avoid electrical shock, ground both the output terminal of the multiplier and the crt high-voltage anode lead to chassis ground when disconnecting the high-voltage lead.

1. Remove the Vertical Preamplifier circuit board and the crt using the previously described procedures in this section.

2. Unplug P359 (Y-Axis) from the Interface circuit board and move the round part of the crt shield to the rear approximately two inches.

3. Place the instrument on its side with the Trigger circuit board down and the Interface circuit board facing toward you.

4. Remove four Phillips-head screws securing the High-Voltage Power-Supply shield and remove the shield. Note the location of the cabinet grounding clip for reinstallation reference.

5. Use a 3/16-inch nutdriver to remove the four shield standoff posts.

6. Remove the mounting screws that secure Q401, Q501, and Q701 to the main chassis (located along the rear edge of the Interface circuit board).

7. Remove the Phillips-head screw located approximately one inch to the right of P359.

8. Remove three Phillips-head screws securing the shield for the High-Voltage Transformer and High-Voltage Multiplier and remove the shield.

9. Unsolder the black wire (connected between the High-Voltage Multiplier and the Interface circuit board) from the Interface circuit board.

10. Unsolder the diode and wire from the terminal post on the High-Voltage Multiplier.

11. Use a 3/8-inch wrench to remove two nylon nuts securing the High-Voltage Multiplier to the Interface circuit board.

12. Gently pull the upper left corner of the Interface circuit board away from the instrument and remove the High-Voltage Multiplier by pulling it away from the Interface circuit board. Return the Interface circuit board to its original position. Feed the high-voltage lead through the space between the rear and front crt shields.

Reinstall the High-Voltage Multiplier into the instrument using the following steps:

13. Feed the Multiplier high-voltage lead into the crt compartment. Then, gently pull the upper left corner of the Interface circuit board away from the instrument approximately 1/2 inch. Insert the High-Voltage Multiplier threaded mounting studs through the mounting holes in the Interface circuit board and return the board to its original position.

14. Reinstall two 3/8-inch nylon nuts (removed in step 11) to secure the High-Voltage multiplier.

15. Resolder the diode and wire (unsoldered in step 10) to the terminal post on the High-Voltage Multiplier.

16. Resolder the black wire (unsoldered in step 9) from the High-Voltage Multiplier to the Interface circuit board.

17. Reinstall the shield (removed in step 8) over the High-Voltage Transformer using three Phillips-head screws.

18. Reinstall the Phillips-head screw (removed in step 7) in the screw hole located approximately one inch to the right of P359.

NOTE

When installing power transistors Q401, Q501, and Q701, ensure that there is a mica insulator and silicone grease (or similar thermal-transfer compound) between these transistors and the instrument chassis.

WARNING

Handle silicone grease with care. Avoid getting silicone grease in the eyes. Wash hands thoroughly after use.

19. Reinstall the mounting screws (removed in step 6) for power transistors Q401, Q501, and Q701 (located along the rear edge of the board).

20. Reinstall four 3/16-inch mounting standoff posts (removed in step 5).

21. Reinstall the High-Voltage Power-Supply shield using four screws (removed in step 4). The cabinet grounding clip should be at the position noted in step 4.

22. Place the instrument with the Interface circuit board down.

23. Move the round part of the crt shield forward approximately two inches. Then reconnect P359 (disconnected in step 2).

24. Reinstall the Vertical Preamplifier circuit board and the crt using the previously described procedures.

HIGH-VOLTAGE OSCILLATOR TRANSISTOR REMOVAL AND REINSTALLATION

The High-Voltage Oscillator Transistor (Q1108) can be removed and replaced using the following procedure:

1. Remove the Vertical Preamplifier circuit board using the previously described procedure in this section.

2. Place the instrument on its side with the Trigger circuit board down and the High-Voltage Power-Supply shield facing you.

3. Remove four Phillips-head screws securing the High-Voltage Power-Supply shield and remove the shield from the instrument.

4. Use a 1/4-inch wrench to remove two hex nuts securing the mounting bracket for Q1108.

5. Use long-nose pliers (or a similar tool) to remove Q1108 and its mounting bracket from the instrument. Disconnect P108 from the Interface circuit board.

6. Unsolder the wires connected to the emitter, base, and collector of Q1108. Note the color and location of each for reinstallation reference.

7. Use a 1/4-inch wrench to remove two hex nuts retaining Q1108 to the bracket and separate it from the bracket.

NOTE

When installing Power Transistor Q1108 ensure that there is a mica insulator and silicone grease (or similar thermal-transfer compound) between the transistor and its mounting surface.

WARNING

Handle silicone grease with care. Avoid getting silicone grease in the eyes. Wash hands thoroughly after use.

Replace Q1108 into the instrument using the following steps:

8. Install the replacement transistor in the mounting bracket and reinstall two 1/4-inch hex nuts (removed in step 7).

9. Resolder the appropriate wires to the emitter, base, and collector of Q1108 at the locations noted in step 6.

10. Reinstall Q1108 and the mounting bracket in the instrument using two 1/4-inch hex nuts (removed in step 4).

11. Reconnect P108 (disconnected in step 5).

12. Reinstall the High-Voltage Power-Supply shield on the Interface circuit board using four Phillips-head screws (removed in step 3).

13. Reinstall the Vertical Preamplifier circuit board using the previously described procedure in this section.

POWER TRANSFORMER REMOVAL AND REPLACEMENT

If the Power Transformer becomes defective, replace it only with a Tektronix direct-replacement part. After the transformer is replaced, check the performance of the entire instrument. The Power Transformer can be removed and installed using the following procedure:

1. Remove two Phillips-head screws from the rear panel of the instrument (one in each lower corner of the rear chassis assembly).

2. Remove four large Phillips-head screws from the top of the rear chassis assembly.

3. Disconnect P138, a 50-conductor ribbon cable from the Storage Display circuit board. Note the edge-stripe position for reinstallation reference.

4. Slide the rear chassis assembly to the rear until all the components are clear of the main chassis.

5. Disconnect P199, a five-wire connector located near the large filter capacitor on the Time Base/Power Supply circuit board.

6. Disconnect P380, a two-wire connector from the Fan to the Time Base/Power Supply circuit board.

7. Lift the rear chassis, rotate it upward 180 degrees, and set in on top of the main chassis.

8. Remove two Phillips-head securing screws from the hinged bracket assembly (one on each side) and rotate the bracket down approximately 90 degrees.

9. Disconnect P160, a two-wire connector located near the 50-conductor ribbon-cable connector (P162) on the Memory circuit board. Note the wire routing for reinstallation reference.

10. Disconnect four miniature coaxial-cable connectors (listed below). Note cable color, location, and routing for reinstallation reference.

a. J101, white with a yellow stripe.

b. J105, white with a green stripe.

c. J11103, white with a purple stripe (CH 1 VERT SIGNAL OUT bnc connector).

d. J11526, white with black and brown stripes (EXT Z-AXIS INPUT bnc connector).

11. Push the hinged bracket into the fully up position and disconnect five miniature coaxial-cable connectors (listed below) from the Microprocessor circuit board. Note wire color and connector location for reinstallation reference.

a. J107, white with green and black stripes.

b. J110, white with blue and black stripes.

c. J112, white with purple and black stripes.

d. J118, white with gray and black stripes.

e. J120, white with orange and black stripes.

12. Lift the rear chassis assembly away from the main chassis. Guide the disconnected wires through the holes in the circuit board to prevent excessive strain on the wiring. Set the rear chassis assembly in a secure location while removing the Power Transformer.

13. Lay the instrument on its Trigger circuit board side and remove the Phillips-head screw from the side cover of the Line-Selector-Switch Assembly. Remove the cover from the instrument by lifting the end from which the securing screw was removed.

14. Disconnect the single-wire connectors (listed below) from the Line-Selector-Switch Assembly circuit board. Note wire color and location for reinstallation reference.

a. P230, gray with brown and white stripes.

b. P222, gray with an orange stripe.

c. P206, gray with a red stripe.

d. P204, black with a gray stripe.

e. P224, gray with yellow and black stripes.

15. Remove two Phillips-head securing screws from the ac-power-source receptacle and slide the receptacle out of the chassis approximately one inch.

16. Use a 5/16-inch nutdriver to remove the hex nut securing the gray ground wire and lift the terminal lug from the mounting stud.

17. Use a 5/16-inch open-end wrench to remove the hex nut securing the Power Transformer to the chassis through the crt compartment side panel.

18. Lay the instrument on its Vertical Preamplifier circuit board side.

19. Disconnect P4008, a five-wire connector leading through a slot in the rear of the main chassis and remove the wiring harness from the instrument. Lay the harness near the rear chassis assembly.

20. Remove the Phillips-head screw securing the cable clamp at the rear of the Trigger circuit board and disconnect P3008, a five-wire connector from the Power Transformer secondary windings.

21. Remove the remaining Phillips-head screw securing the Power Transformer mounting bracket to the Trigger circuit board and remove one Phillips-head screw securing the bracket to the Interface circuit board.

22. Remove three 5/16-inch nuts securing the transformer mounting bracket to the main chassis frame (two from the top of the bracket and one from below the

transformer). A 5/16-inch nutdriver is required to reach the lower nut, and a 5/16-inch open-end wrench and a Phillips screwdriver are required to remove the other two nuts.

23. Disconnect the POWER-switch-extension shaft from the POWER switch by inserting a scribe (or similar tool) into the notch between the end of the extension shaft and the end of the switch shaft. Then gently pry them apart.

24. Lift up gently on the rear of the Trigger circuit board to separate the pins of P944 (on the Interface circuit board) from J580 (on the Trigger circuit board).

25. Hold the rear end of the Trigger circuit board up approximately 3/4 inch and lift the Power Transformer up enough to clear the mounting studs from the chassis. Then slide the transformer toward the top of the chassis approximately one inch. Release the end of the Trigger circuit board.

26. Remove the POWER-switch-extension shaft from the instrument by pulling it out of the front panel and shaft support, toward the rear of the instrument.

27. Unsolder the Power Transformer secondary wires from the Interface circuit board. Refer to Figure 5-5 to verify correct wire color and location for reinstallation reference. Remove all excess solder from the lead holes in the circuit board to facilitate installation of the replacement transformer.

28. Pull the wires from the Line-Selector-Switch Assembly through the slot in the main chassis one at a time. The connectors must be oriented in the same direction as the slot to pass through the slot.

29. Lift the rear of the Trigger circuit board again, lift the transformer enough to clear the main chassis, and slide the transformer from the top of the instrument.

30. Use a 1/4-inch wrench on the nut and a 5/16-inch wrench on the bolt head to remove the bolts securing the mounting bracket to the transformer.

Install a replacement transformer into the instrument using the following steps:

31. Attach the mounting bracket to the replacement transformer using four bolts and 1/4-inch hex nuts (removed in step 30).

32. Lift the rear of the Trigger circuit board and slide the transformer into place so that the transformer bracket mounting stud just clears the top of the main chassis.

33. Let the transformer rest at this position and release the end of the Trigger circuit board.

34. Feed the transformer primary leads (nearest the rear of the chassis) through the slot in the main chassis to the Line-Selector-Switch Assembly one at a time.

35. Solder the transformer secondary leads to the Interface circuit board (start with the ones farthest in and work out toward the edge of the circuit board). Refer to Figure 5-5 to verify correct wire color and location.

36. Insert the POWER-switch-extension shaft through both the support bracket and the front-panel hole (from the rear of the instrument).

37. Lift the rear of the Trigger circuit board and slide the transformer into position (mounting studs must align with the mounting holes in both the chassis and transformer bracket).

38. Reinstall two Phillips-head screws (removed in step 21) used to secure the transformer bracket to the Trigger circuit board and the Interface circuit board. Press down on interboard connector J580 (on the Trigger circuit board) to ensure that the connector pins are properly seated.

39. Reinstall three 5/16-inch hex nuts (removed in step 22) used to secure the transformer bracket to the main chassis.

40. Align the POWER-switch-extension shaft with the switch shaft and gently press them together until they snap into position.

41. Reconnect P3008, a five-wire connector from the transformer (disconnected in step 20) and reinstall the Phillips-head securing screw used to hold the cable clamp to the Trigger circuit.

42. Insert the five-wire harness connected to P4008 through the slot in the rear of the main chassis and reconnect P4008 to the Trigger circuit board.

43. Lay the instrument on its Trigger circuit board side.

44. Reinstall a 5/16-inch hex nut used to secure the transformer bracket to the crt compartment side panel.

45. Remove the terminal lug from the old transformer ground wire and solder it on the replacement transformer ground wire.

46. Place the terminal lug on the grounding stud and reinstall a 5/16-inch hex nut to secure it. To prevent the wire from twisting, hold the terminal lug in place as the nut is tightened.

47. Reconnect the single-wire connectors that were removed in step 14.

48. Push the ac-power-source receptacle back into place and reinstall two Phillips-head securing screws (removed in step 15).

49. Place the Line-Selector-Switch Assembly cover in position and reinstall the Phillips-head securing screw (removed in step 13).

50. Lay the instrument on its Interface circuit board side and set the rear chassis on top of the main chassis in preparation for reinstalling the rear chassis assembly. (Rear of the assembly should be facing toward the front of the instrument.)

51. Reconnect five miniature cables that were disconnected in step 11.

52. Pull the hinged bracket down approximately 45 degrees and reroute the four miniature cables as noted in step 10. Then reconnect them.

53. Reroute the two-wire connector to P160 as noted in step 9 and reconnect it.

54. Push the hinged bracket into its fully up position and reinstall two small Phillips-head securing screws (one in each side).

55. Lift the rear chassis assembly, rotate it downward 180 degrees, and set it down behind the main chassis.

56. Reconnect P380 (two-wire connector from the Fan that was disconnected in step 6).

57. Reconnect P199 (five-wire connector that was disconnected in step 5).

58. Slide the rear chassis assembly into the main chassis until the mounting-screw holes are aligned and reinstall four large Phillips-head securing screws across the top of the assembly (removed in step 2).

59. Reconnect P138 (50-conductor ribbon cable to the Storage Display circuit board) with the edge stripe oriented as noted in step 3.

60. Reinstall two Phillips-head securing screws (removed in step 1) into the rear chassis (one at each lower corner).

LINE VOLTAGE SELECTOR SWITCH REMOVAL AND REPLACEMENT

The Line Voltage Selector switch may be removed and replaced using the following procedure:

1. Remove two Phillips-head screws from the rear panel of the instrument (one in each lower corner).

2. Remove four large Phillips-head screws from the top of the rear chassis assembly.

3. Slide the rear chassis assembly to the rear until all the components are clear of the main chassis.

4. Lift the rear chassis assembly, rotate it upward 180 degrees, and place it on top of the main chassis. Align the two innermost mounting holes with the corresponding threaded inserts on the main chassis and install two of the screws removed in step 2.

5. Remove the Phillips-head screw from the side cover of the Line-Selector-Switch Assembly and remove the cover from the instrument.

6. Disconnect the single-wire connectors listed below. Note wire color and location for reinstallation reference.

   a. P230, gray with brown and white stripes.

   b. P222, gray with an orange stripe.

   c. P206, gray with a red stripe.

d. P204, black with a gray stripe.

e. P224, gray with yellow and black stripes.

f. P214, gray with a green stripe.

g. P212, gray with yellow and black stripes.

h. P110, gray with red and black stripes.

i. P108, gray with brown and black stripes.

7. Insert a scribe (or similar tool) in the notch between the POWER-switch control shaft and the extension shaft and gently pry them apart.

8. Remove two Phillips-head screws securing the ac-power-input receptacle and push it through the mounting hole until it clears the Line-Voltage Selector Switch circuit board.

9. Use a 9/16-inch wrench to remove the securing nut on the fuse holder and push the holder through the mounting hole until it clears the Line-Voltage Selector Switch circuit board.

10. Remove three Phillips-head screws securing the Line-Voltage Selector Switch circuit board and remove the board from the instrument.

Replace the Line-Voltage Selector Switch Assembly using the following steps:

11. Set the Line-Voltage Selector Switch Assembly in position and secure it with three Phillips-head screws (removed in step 10).

12. Reinsert the fuse holder in the mounting hole and secure it with a 9/16-inch nut.

13. Reinsert the power-input receptacle in its mounting hole and secure it with two Phillips-head screws (removed in step 8).

14. Align the POWER-switch control shaft and the extension shaft and press them together gently until they snap into position.

15. Reconnect the single-wire connectors that were disconnected in step 6.

16. Remove two Phillips-head screws that secure the rear chassis to the main chassis.

17. Lift the rear chassis assembly, rotate it 180 degrees, and slide it into the main instrument chassis until the mounting-screw holes are aligned.

18. Reinstall four Phillips-head screws (removed in step 2) in the mounting holes across the top of the rear chassis assembly.

19. Reinstall two Phillips-head screws (removed in step 1) in the rear panel.

REMOVAL AND REPLACEMENT OF TRANSISTORS AND INTEGRATED CIRCUITS

Transistors and integrated circuits should not be replaced unless they are actually defective. If removed from their sockets during routine maintenance, return them to their original sockets. Unnecessary replacement or switching of semiconductor devices may affect the adjustment of the instrument. When a semiconductor is replaced, check operation of the instrument part that may be affected.

Any replacement component should be of the original type or a direct replacement. Bend the leads to fit the socket and cut the leads to the same length as on the component being replaced. See Figure 8-2 for lead-configuration illustrations.

To remove dual-in-line-packed (DIP) integrated circuits, pull slowly and evenly on both ends of the device. Avoid disengaging one end of the integrated circuit from the socket before the other, since this may damage the pins.

WARNING

Handle silicone grease with care. Avoid getting silicone grease in the eyes. Wash hands thoroughly after use.

WARNING

Voltages are present on the exterior surface of the chassis-mounted power supply transistors if power is applied to the instrument and the POWER switch is ON.

The chassis-mounted power supply transistors and their mounting bolts are insulated from the chassis. In addition, silicone grease is used to increase heat transfer capabilities. Reinstall the insulators and replace the silicone grease when replacing these transistors. The grease should be applied to both sides of the mica insulators and should be applied to the bottom side of the transistor where it comes in contact with the insulator.

NOTE

After replacing a power transistor, check that the collector is not shorted to ground before applying power to the instrument.

REMOVAL AND REPLACEMENT OF INTERCONNECTING PINS

Two methods of interconnection are used in this instrument to connect the circuit boards with other boards and components. When the interconnection is made with a coaxial cable, a special end-lead connector plugs into a socket on the board. Other interconnections are made with pins soldered onto the board. Two types of mating connections are used for these interconnecting pins. If the mating connector is on the end of a lead, an end-lead pin connector is used that mates with the interconnecting pin. The following information provides the replacement procedure for the various interconnecting methods.

Coaxial-Type End-Lead Connectors

Replacement of the coaxial-type end-lead connectors requires special tools and techniques; only experienced maintenance personnel should attempt replacement of these connectors. It is recommended that the cable or wiring harness be replaced as a unit. For cable or wiring harness part numbers, see the "Replaceable Mechanical Parts" list in Volume II. An alternative solution is to refer the replacement of the defective connector to your local Tektronix Field Office or representative.

End-Lead Pin Connectors

Pin connectors used to connect the wires to the interconnecting pins are factory assembled. They consist of machine-installed pin connectors mounted in plastic holders. The plastic holders are easily replaced as individual items; but if the connectors are faulty, the entire cable assembly should be replaced. Individual pin connectors are listed in the "Replaceable Mechanical Parts" list in Volume II, but special tools are required for installation.

When pin connectors are grouped together and mounted in a plastic holder, they are removed and installed as a multi-pin connector. To provide correct orientation of this multi-pin connector when it is replaced, an arrow is stamped on the circuit board, and a matching arrow is molded into the plastic housing of the multi-pin connector. Be sure these arrows are aligned when the multi-pin connector is reinstalled. If the individual end-lead pin connectors are removed from the plastic holder, note the color of each individual wire to facilitate replacement.

REMOVAL AND REPLACEMENT OF CERAMIC TERMINAL STRIPS

Replacement strips (including studs) and spacers are supplied under separate part numbers. However, the old spacers may be reused if they are not damaged. The applicable Tektronix part numbers for the ceramic strips and spacers used in this instrument are given in the "Replaceable Mechanical Parts" list in Volume II.

Remove ceramic terminal strips as follows:

1. Unsolder all components and connections on the strip. To aid in replacing the strip, it may be advisable to mark each lead or draw a sketch to show locations of the components and connections.

2. Gently pry or pull the damaged strip from the circuit board.

3. If spacers come out with the strip, remove them from the stud pins for use on the new strip (spacers should be replaced if they are damaged).

Install ceramic terminal strips as follows:

4. Place spacers in the chassis holes.

5. Carefully press the studs of the strip into the spacers until they are completely seated.

6. If the stud extends through the spacers, cut off the excess.

7. Replace all components and resolder connections. Observe the soldering precautions under "Soldering Techniques" in this section.

READJUSTMENT AFTER REPAIR

After any electrical component has been replaced, the adjustments for that particular circuit should be checked, as

well as the adjustments of other closely related circuits. Since the Power Supply affects all circuits, adjustment of the entire instrument should be checked if work has been done in the Power Supply or if the Power transformer has been replaced.

INSTRUMENT REPACKAGING

Should reshipment become necessary, reuse the carton in which your instrument was shipped. If the original packaging is unfit for use or is not available, contact your local Tektronix Field Office or representative to order a replacement shipping carton.

If the instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag containing the following information:

1. Owner's name and address, with the name of an individual at your firm who can be contacted.

2. Complete instrument serial number.

3. Description of the services required.

WARNING

During rackmount installation, interchanging the left and right slide-out track assemblies defeats the extension stop (safety latch) feature of the tracks. Equipment could, when extended, come out of the slides and fall from the rack, possibly causing personal injury and equipment damage.

When mounting the supplied slide-out tracks, inspect both assemblies to find the LH (left hand) and RH (right hand) designations to determine correct placement. Install the LH assembly to your left side as you face the front of the rack and install the RH assembly to your right side. Refer to the rackmounting instructions in this manual for complete information.

SERVICE TESTS

SERVICING SETUP

The 468 is mechanically structured to allow access to digital storage components while the instrument is operating. The rear section of the frame may be removed from the main oscilloscope frame and repositioned on top of the main frame by lifting and rotating it 180 degrees. Holes for mounting screws are arranged to secure the rear frame in the servicing position.

Place the 468 in the servicing position as follows:

1. Disconnect the 468 from the power source.

2. Remove the instrument cabinet (see "Cabinet Removal" in this section).

3. Remove six screws holding the rear chassis assembly to the main chassis. Four screws are located across the top, and one is at each lower rear corner of the rear panel.

4. Lift the rear chassis assembly slightly to separate it from the main chassis and carefully rotate it 180 degrees and forward to position it on top of the main chassis.

5. Align two screw holes in the rear chassis assembly with screw holes in the main chassis and use two of the screws removed in step 3 to secure the rear chassis assembly to the main chassis (see Figure 5-6). Verify that the 50-conductor ribbon cable is securely in place at both end connectors.

6. To gain access to the Memory and Time Base/Power Supply circuit boards, remove the two screws on either end of the holding bracket. The two rear boards are mounted on a hinged plate to allow them to swing away from the rear frame.

CAUTION

The lead arrangement and spacing of the five 10-wire cables between the Time Base and the Memory circuit boards must be maintained to prevent possible failure.

TRAP TEST

This test is programmed into the Microprocessor and ROM. It is used to check the Microprocessor address sequencing and the address-generated strobes. It is not necessary to remove or exchange any ROM for this test.

To initiate the test, momentarily unplug P262 (see Figure 5-7) and then reconnect it. Microprocessor operation will be interrupted, and the Trap Test routine will begin. To end the test, cycle the POWER switch OFF then ON. The Microprocessor will return to its normal operating routines.

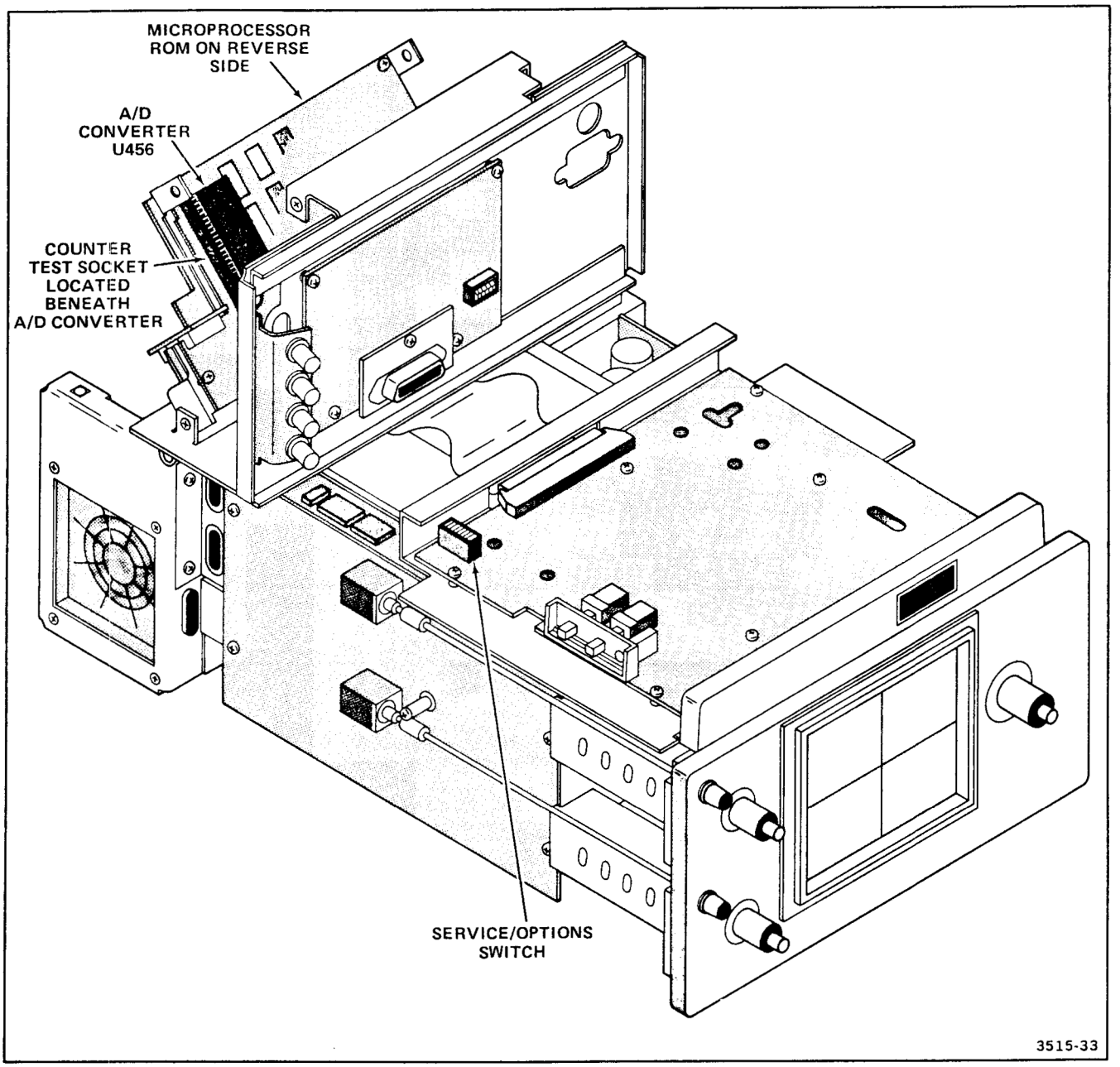


Figure 5-6. The 468 in the servicing position.

KERNEL TEST

This test isolates the Microprocessor from the return loops to allow a check of the Microprocessor operation as it free runs. Bus Buffers U452 and U558 are removed to unload the Microprocessor AD0 through AD7 lines. Set up the 468 Kernel test as follows:

1. With the instrument in the servicing position, disconnect it from the power-input source.

2. Carefully remove U452 and U558 (see Figure 5-7) while observing the "Static Sensitive" precautions given at the beginning of the "Corrective Maintenance" portion of this section. Store the IC in a static-safe location until they are reinstalled.

3. To start the Kernal Test, reconnect the 468 to the power source and set the POWER switch to ON. To restart the test, momentarily place Power-on Restart Jumper P182 to the RESET position and then return it to the RUN position (see Figure 5-7).

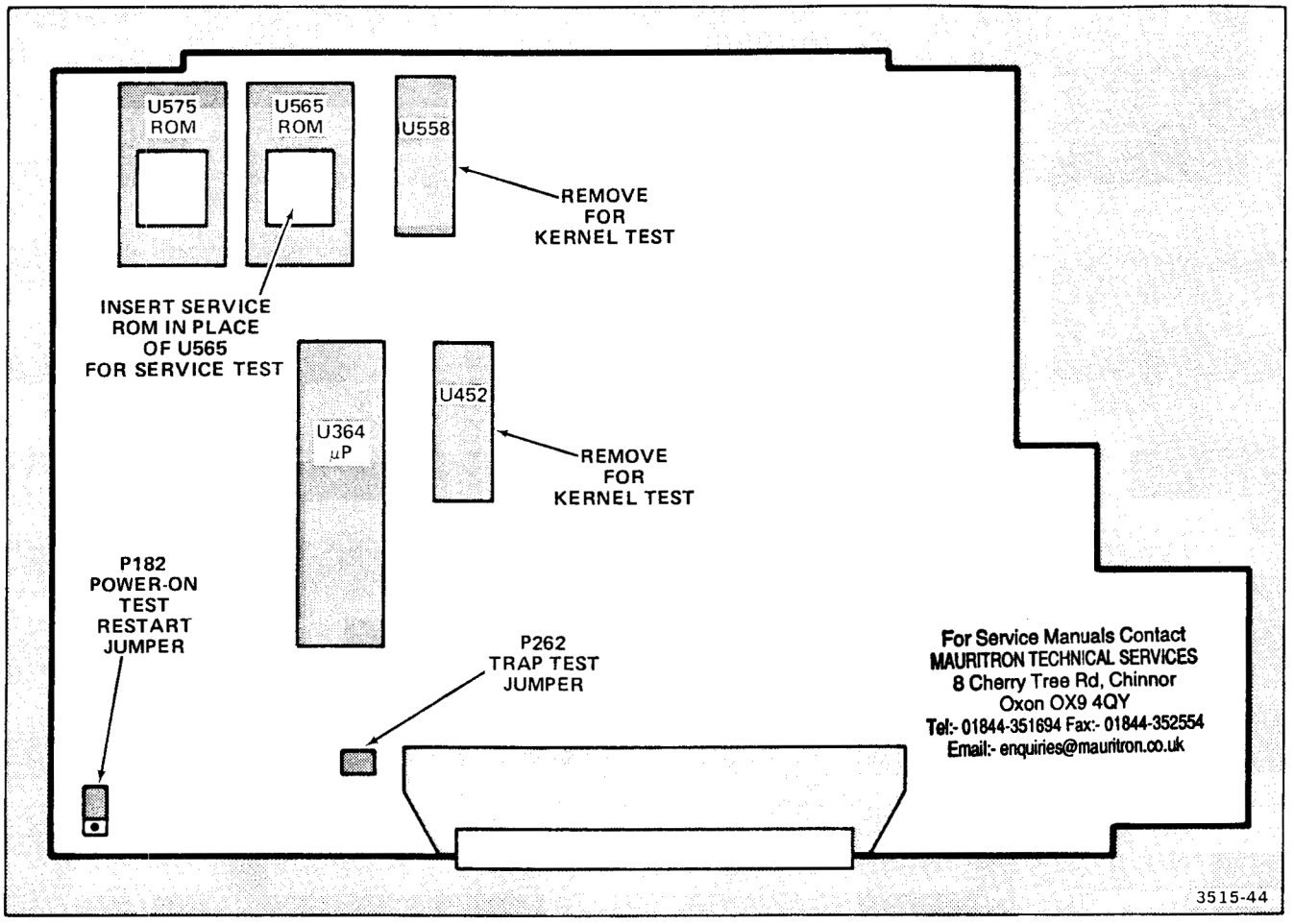


Figure 5-7. Location of the test ROM and test jumpers on the Microprocessor circuit board.

A/D CONVERTER SIMULATOR

An optional accessory (a Test-Counter IC) may be installed to simulate operation of A/D Converter U456. This Test-Counter IC produces a ramp signal that exercises the digital circuitry for testing purposes. See Table 5-3 "Maintenance Aids" in this section of the manual for its part number (included in the Service Accessory package).

Install the A/D Converter Simulator as follows:

1. With the instrument in the servicing position, disconnect it from the power-input source.

2. Carefully remove U456 (see Figure 5-7) while observing the "Static Sensitive" precautions given at the beginning of the "Corrective Maintenance" portion of this section. Pull evenly on both ends of the IC so that all pins come free together. Carefully removing U456 will prevent bending the pins. Store the IC in a static-safe location until it is reinstalled.

3. Install the Test-Counter IC in the smaller socket located beneath U456.

4. Reconnect the 468 to the power-input source and set the POWER switch to ON. The ramp display will begin, with the 468 in any storage mode, as soon as the power-on self-test is completed.

SERVICE ROUTINE PROCEDURES

A Service ROM accessory contains the programming for the selectable service routines used for testing digital circuitry in the 468. Some of these routines are display routines and some are used only for signature analysis testing. See Table 5-3 "Maintenance Aids" in this section of the manual for the part number of the optional Service ROM.

One of the Microprocessor ROM must be exchanged with the Service ROM to obtain the programmed routines. Install the Service ROM as follows:

1. With the 468 in the servicing position, disconnect it from the power-input source.

2. Remove ROM U565 from its socket (see Figure 5-7) while observing the "Static Sensitive" precautions given at the beginning of the "Corrective Maintenance" portion of this section. Pull evenly on both ends of the IC so that all pins come free together. Carefully removing U565 will prevent bending the pins. Store the IC in a static-safe location until it is reinstalled.

3. Install the Service ROM in the U565 socket.

Selecting a Service Routine

To select a specific service routine, set Service/Options switch S707 (an eight-section DIP-switch assembly) to the number of the test desired. Figure 5-6 shows the location of the switch on the Storage Display circuit board, and Table 5-4 lists the test routines and corresponding test numbers to be set into S707. Position 1, at the rear of the switch assembly, corresponds to the least-significant bit (LSB) of the test number. Position 8 is the Options-bit switch. If the GPIB option is not installed in the instrument, or when the GPIB option is not going to be used, switch 8 should be open. The GPIB service routines can be executed only when switch 8 is closed and the option installed. If you select a GPIB test, verify that the option bit is set to 1 (closed).

NOTE

When servicing of the instrument is completed, section 7 of Service/Options Switch S707 must be set to the closed position to enable the RAM Verification portion of the power-on self-test, and switch section 8 must be set to the closed position to enable the GPIB option.

Beginning a Service Routine

Once the service routine number has been set, power may be applied to the 468. The selected routine will begin to run in place of the normal power-on self-test. If the oscilloscope is already in operation, a routine can be started by removing Restart Jumper P182 from the RUN position and placing it momentarily in the RESTART position; then returning it to the RUN position. See Figure 5-7 for the location of the Restart Jumper on the Microprocessor circuit board.

Restarting a Service Routine

To restart a routine already in progress, remove Restart Jumper P182 from the RUN position and place it momentarily in the RESTART position; then return it to the RUN position. Cycling the POWER switch OFF then ON will also restart a service routine.

Table 5-4

Service Routine Switch Settings

Routine	Switch Setting
ROM Checksum	X0000000[a]
Lamp Test	X0000001
System and Scratch RAM Exercise	X0000010
I/O Registers	X0000011
Position-Rate Counter	X0000100
Switch Closure	X0000101
Basic Display System	X0001000
Stop at 256/Jitter Correction	X0001001
Stop at 512/Dot RAM	X0001010
Time Base Counter String (Signature Analysis Testing)	X0010000
Time Base Record String (Signature Analysis Testing)	X0010001
Time Base Jitter Counters (Signature Analysis Testing)	X0010010
Acquisition RAM	X0010011
GPIB Data Bus	11111000
Acceptor Handshake	11111001
Source Handshake	11111010
Default to 8888 display	Any other setting

[a]X in the switch setting column means "don't care." Either position of that switch selection is acceptable.

Selecting Another Routine

To select a different service routine, set the number of the desired new routine in the Service/Options switch and perform the service routine restart procedure. If the switch is inadvertently set to an invalid routine number, the seven-segment LED readout will display 8888. If you determine that the Service/Options DIP switch is set correctly but is not being read correctly, check the outputs of U522 (DIP Switch Register). The output of U522 is an inverted copy of the Service/Options switch setting.

SERVICE ROUTINE DESCRIPTIONS

ROM Checksum

This routine computes a checksum for the Service ROM. If the checksum computed by the routine is the same as the checksum stored in the ROM, the seven-segment display will read out all zeros. If there is a checksum failure, no display will appear and the Microprocessor will halt. If the checksum routine does not execute, oscilloscope operation is undefined.

Lamp Test

The lamp test routine will light each of the Microprocessor-controlled LED indicators on the instrument front panel (and the $\overline{\text{TIDS}}$/SRQ LED if the GPIB option is installed) in a predefined order. One LED at a time will be illuminated, and the test will continue until it is manually terminated. The order in which each LED illuminates is as follows:

1. Scaling: V/S, mV/ns, then DIV/μs.

2. The four digits of the seven-segment display will show a moving "8." from right to left (decimal points also illuminate).

3. CH 1 VOLTS/DIV Scale-factor: X1, then X10.

4. CH 2 VOLTS/DIV Scale-factor: X1, then X10.

5. $\overline{\text{TIDS}}$/SRQ: shows red then green.

NOTE

The red portion of the scaling LED will be illuminated when VOLTS CURSOR FUNCTION is selected and the green portion will be illuminated when the VOLTS CURSOR FUNCTION push button is released.

Position-Rate Counter

This routine exercises the Position-rate Counter circuitry. The contents of the counter (three binary-coded decimal characters) will be read and transferred directly to the seven-segment LED display. As the CURSOR control knob is rotated, the observed display should change. The range of the counter outputs should be within 000 to 800, with 80 being an average low-end count and 480 being an average high-end count. As the rate region of the control knob rotation is entered, the top scale-factor LED should illuminate. The bottom scale-factor LED should illuminate when the CURSOR SELECT push button is pressed in.

Switch Closure

This routine reads all of the Microprocessor-accessible switches and displays them in a logic analyzer type display. Four waveform displays will indicate the operation of 40 switches. The EXT trigger position of the SOURCE switch is not displayed, but it is indicated by illumination of the scale-factor LED when an external trigger is selected. See Figure 5-8 for an illustration of the waveform and the assigned area for each switch.

Each switch is assigned to one graticule division. A HI level means that the switch is closed, and a LO means that the switch is open. However, in the case of the AC-GND-DC switch, a three-level presentation is used to indicate all three possible switch positions. Switch operation can be checked by changing the switch position and observing the change seen on the display.

Basic Display System

No crt display is produced by this routine. A looping routine continually fills the Display RAM with a ramp to generate signatures. These signatures verify circuit operation when checked against the correct signatures contained in the Signature Tables. The following circuitry is exercised: display bus, counter addressing functions, Z-axis control circuitry used with the display bus, the Display RAM chip select circuitry, and the display address bus.

The vertical and horizontal digital-to-analog converters in the Storage Display circuitry will also be exercised, and their outputs may be checked with a test oscilloscope.

Stop at 256/Jitter Correction

This routine will fill the Display RAM with a 256-point waveform consisting of two ramps (see Figure 5-9A). The waveform data-point values range from 0 to 255 to obtain a display with both full vertical and full horizontal ranges. The jitter-correction circuitry is checked by selecting the X10 MAG function and using the Horizontal POSITION control to align the falling edge of the ramp with the center vertical graticule line. The waveform is cycled through the maximum value, the middle value, and the minimum value of the jitter correction, and the resulting display is three vertical lines. The lines should have a spacing of no more than 0.4 division between two adjacent lines, as illustrated in Figure 5-9B.

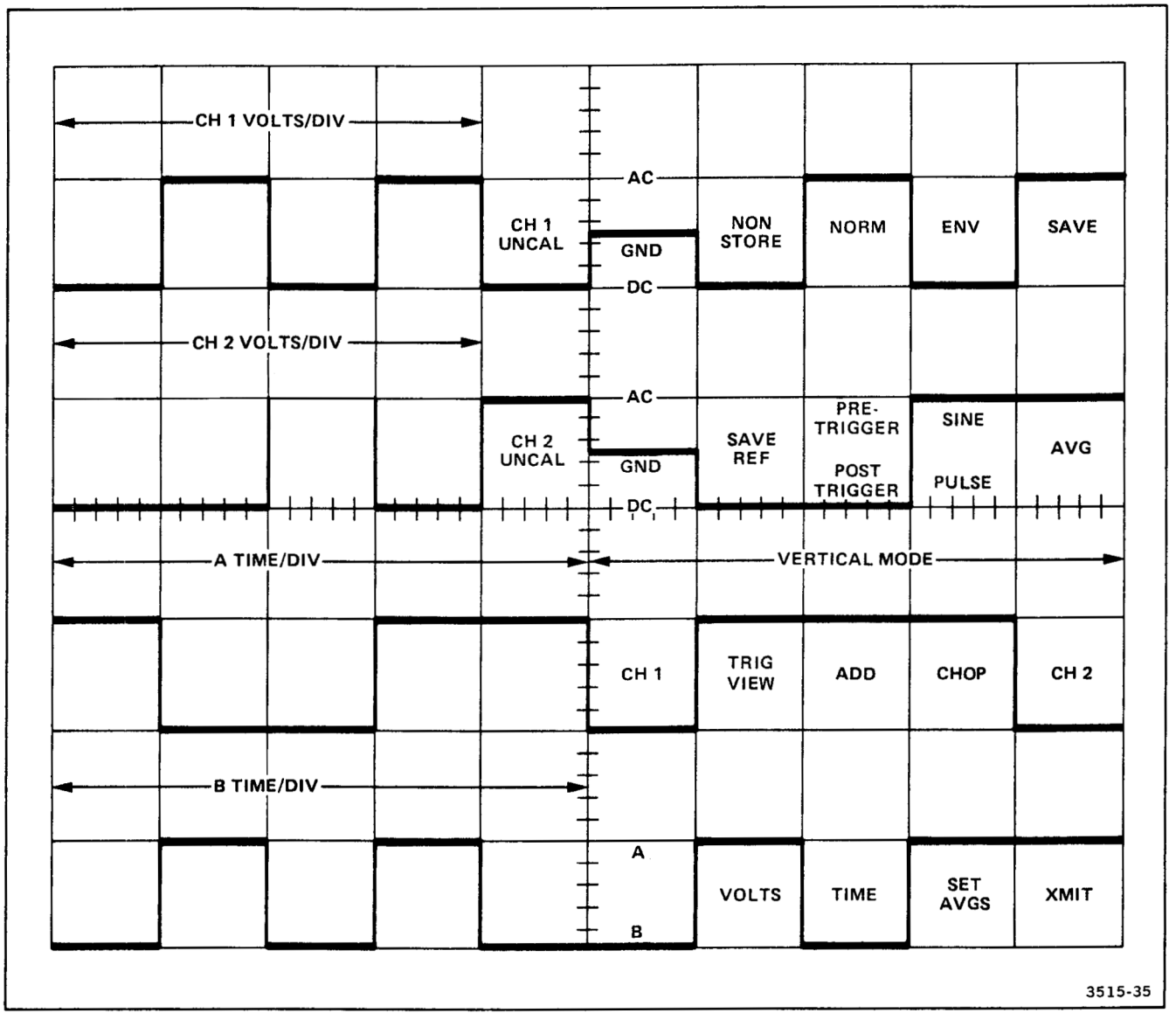


Figure 5-8. Switch closure test crt display.

Stop at 512/Dot RAM

This routine stores a 512-point waveform into the Display Memory. The display will consist of four 128-point ramps, with data-point values ranging from 65 to 190 (a five-division display). At the end of the waveform, four-point steps will appear. These steps have data-point values of 65, 128, and 190 respectively. The steps can be used to calibrate the vertical display gain by aligning the levels with both the dotted reference lines and the center horizontal graticule line (see Figure 5-10).

A dot display from the Dot RAM is moved through the ramp display to verify that a dot can be displayed on all 512 data points of the display.

Time Base Routine

The Time Base verification routines listed in Table 5-5 are used to generate signatures for signature-analysis testing. The portions of the Time Base circuitry not listed in the table cannot be controlled by the Microprocessor, and other troubleshooting methods are required (see "Troubleshooting Charts" in Volume II of this manual).

Acquisition RAM

This routine is used to generate signatures for testing the acquisition random-access memory. Data is written into each address in the RAM and then read back in a continuous loop routine. No crt display is generated by the routine.

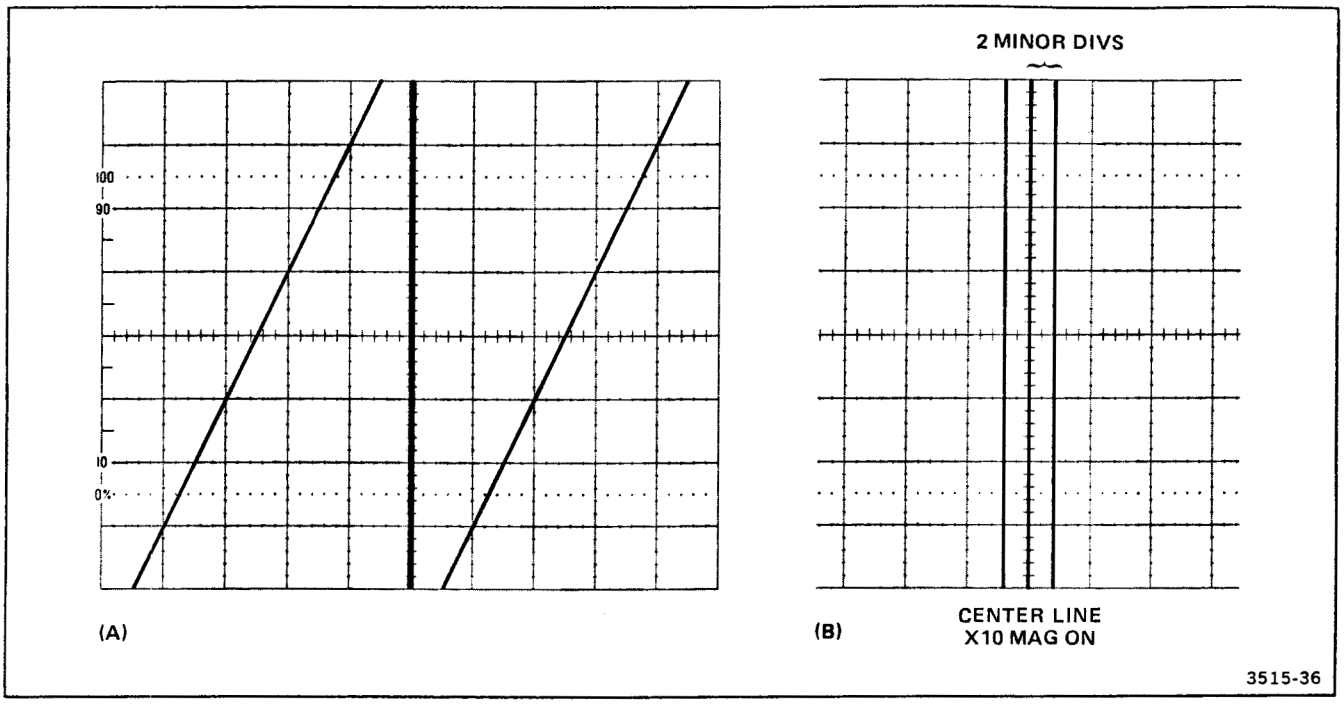


Figure 5-9. Stop at 256/jitter correction test crt display.

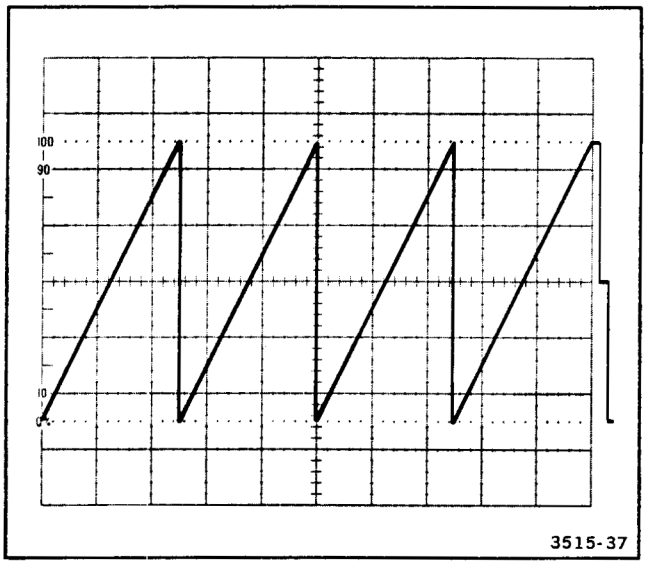


Figure 5-10. Stop at 512/dot RAM test crt display.

Table 5-5

Time Base Verification Routines

Test	Setup Requirements	Test Number
Time Base Counter String	Counter chain test jumper (P420) set to "Test" and triggers disabled.	X0010000
Time Base Record String	No additional requirements.	X0010001
Time Base Jitter Counters	No additional requirements.	X0010010

GPIB Data Bus

This routine toggles all the bits of the data path from the output data register through the bus bidirectional buffers and back to the Microprocessor bus through the data input buffer. The Microprocessor reads the Service/Options switch register and status buffer and compares the data against known values. The check value for the switch register must be manually set. The GPIB control register is also toggled, but only the TADS condition can be tested by the Microprocessor. The generated signatures can be checked by using signature-analysis testing to compare them with the Signature Tables.

Error codes are displayed in the seven-segment display and are updated at the completion of each pass through the routine. Table 5-6 shows the digit assignments and error indications.

To run the GPIB Data Bus routine, the following preliminary steup must be performed:

1. Disconnect the GPIB output cable.

2. Set the Service/Options switch to 111111000.

3. Set the GPIB switch talk address to 00000.

4. Set the TALK ONLY switch (switch-section 8) off (0).

Table 5-6

GPIB Data Bus Error Display

	Digit 1 Data Bus	Digit 2 Status Check	Digit 3 Switch Register	Digit 4 TADS
Pass	0	0	0	0
Fail	1-9	1-2	1	1-2

Acceptor Handshake

This rountine executes an acceptor handshake of the GPIB circuitry. Unused bits of the Interface Control register are used to drive the ATN and DAV lines, enabling the handshake to be executed. Signatures generated can be compared with the Signature Tables.

First perform the following preliminary setup:

1. Disconnect the GPIB output cable.

2. Set the Service/Options switch to 11111000.

3. Connect TP335 to TP112 on the GPIB board to drive ATN.

4. Connect TP333 to TP114 on the GPIB board to drive DAV.

Source Handshake

In this routine, a source handshake loop is executed and the bits of the Interface Status register are tested by the Microprocessor. Errors are displayed in the seven-segment display. Generated signatures can be compared with the Signature Tables. A jumper is needed to assert DAC, and RFD is always True to enable the handshake routine.

First perform the following preliminary setup:

1. Disconnect the GPIB output cable.

2. Set the Service/Options switch to 11111010.

3. Connect TP335 to TP111 on the GPIB board to assert DAC.

4. Connect TP333 to TP113 on the GPIB board to assert IFC.

If no errors occur during execution of the routine, the readout in the seven-segment display will be 0000. If a status-bit error occurs, a number from 1 through 7 will appear in the LSB of the readout. The remaining digits are not used.

SIGNATURE-ANALYSIS TESTING

The 468 is designed for signature-analysis testing when troubleshooting digital circuit malfunctions. The Service ROM, installed in place of one of the Microprocessor ROM, contains selectable looping routines suitable for signature generation.

The looping routines are continuous, and the resulting data enclosed between a defined starting point and stopping point results in a predictable data string. The data string produces a signature (type of checksum) that may be used as a check of circuit operation. A correct signature obtained at a testing point indicates that the circuit operation is correct to that point.

A list of signatures obtained from properly operating instruments is included in this section of the manual. The Signature Tables include required 468 setup procedures; start, stop, and clock pulse information; and check signatures to verify that the Signature Analyzer in use is set correctly to obtain the listed signatures.

Refer to the Operators Manual of the Signature Analyzer in use to obtain the necessary information regarding its operation.

Table 5-7 lists the current firmware and hardware versions applicable to the 468. Future firmware or hardware changes to the instrument may require updates to some of the Signature Tables. When update pages are received for later versions, they should be inserted behind the corresponding earlier versions, which should remain in the manual.

The signature lists are contained in Tables 5-8 through 5-23.

Table 5-7

468 Digital Storage Oscilloscope Signature Versions

Assy Number	Board Name	Signature Versions			
		1.0 & 2.0			
A14	Vertical Mode Switch	670-6375-00			
A16	Storage Display	670-6377-00 670-6377-01 670-6377-02			
A17	GPIB	670-6378-00			
A18	Memory	670-6379-00			
A19	Time Base/Power Supply	670-6380-00			
A21	Microprocessor	670-6382-00,-01			

Table 5-8

Kernel Test Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A21	Microprocessor	670-6382-00 and 670-6382-01	8-20	18

Test 1—Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U364-31	A21
Start	↑	TP580	A21
Stop	↓	TP580	A21

Test 2—Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U364-31	A21
Start	↓	TP580	A21
Stop	↑	TP580	A21

468 Setup (Both Tests)

468 in Servicing Setup. U452 and U558 removed. To re-start test with POWER ON, move P182 to RESET position momentarily; then return it to RUN position. (Service ROM is not required.)

Test 1
+5 V Check Signature—4P0A

Component	Pin	Signature
U364	21	P3P4
	22	99UF
	23	FP52
	24	0056
	25	P2HH
	26	759F
	27	762H
	28	3C55
U472	2	P2HH
	3	P2HH
	4	0056
	5	0056
	6	FP52
	7	FP52
	8	99UF
	9	99UF
	11	P3P4
	12	P3P4
U550	2	8CU3
	5	0H5H
	6	A44P
	9	404A
	12	1C51
	15	8598
	16	A0C1
	19	939A
U478	1	759F
	2	762H
	3	3C55
	9	5FU8
	10	A50A
	11	8FAH
	14	CHHP
	15	AF5P

Component	Pin	Signature
U246A	3	H327
	4	H327
	5	H327
	6	9H2H
U246B	8	H327
U246C	1	3827
	2	3C55
	12	A50A
	13	759F
U272B	3	PC00
	17	A50A
U272F	7	AFH7
	13	P2HH
U278A	1	3827
	2	762H
U278C	8	A50A
	9	P2HH
	10	57HF
U278D	11	A50A
	12	AFH7
	13	CFHF
U378	11	8P49
	12	HA27

Test 2
+5 V Check Signature—P254

Component	Pin	Signature
U378	5	79PF
	6	P4HF
	7	84P6

Table 5-9

ROM Test Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A21	Microprocessor	670-6382-00 and 670-6382-01	8-20	18

ROML Test—Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U364-31	A21
Start	↓	U478-15	A21
Stop	↓	TP580	A21

ROMH Test—Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U364-31	A21
Start	↓	U478-14	A21
Stop	↓	U478-15	A21

468 Setup (Both Tests)

U452 and U558 removed. To start or restart test with POWER ON, move P182 to RESET position momentarily, then return it to RUN position. (Service ROM is not required.)

ROML Test
+5 V Check Signature-P254

Component	Pin	Signature	
		Version 1.0	Version 2.0
U565	9	54F2	954U
	10	43PA	H3P1
	11	60U2	660F
	13	HA4U	34A6
	14	P522	F6H0
	15	PU35	2H6H
	16	97H8	98A3
	17	6139	A99F

ROMH Test
+5 V Check Signature-P254

Component	Pin	Signature	
		Version 1.0	Version 2.0
U575	9	6507	A42C
	10	0AUF	PH78
	11	FP66	3289
	13	2AH0	A34P
	14	059U	8CA1
	15	049F	A542
	16	1C16	FF59
	17	HPPF	96A8

Table 5-10

Trap Test Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A21	Microprocessor	670-6382-00,-01	8-20	18
A19	Time Base/Power Supply	670-6380-00	8-23	19
A14	Vertical Mode Switch	670-6375-00	8-15	4

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	TP477	A21
Start	↓	U478-14	A21
Stop	↓	U478-13	A21

468 Setup

Reinstall U452 and U558 if previously removed. To start or restart test, momentarily remove Service Jumper P262 on A21; then replace it. To end test, cycle POWER switch OFF then ON. (Service ROM will not affect the test, may be installed or removed as desired.)

+5 V Check Signature—5FU8

A21

Component	Pin	Signature Version 1.0	Signature Version 2.0
U364	12	4305	0A16
	13	CHC7	35PA
	14	4332	UHCA
	15	852P	312H
	16	43F0	U34H
	17	FF10	99H5
	18	9131	5FP0
	19	1552	2262
U558	1	5FU8	5FU8
	2	1552	2262
	3	9131	5FP0
	4	FF10	99H5
	5	43F0	U34H
	6	852P	312H
	7	4332	UHCA
	8	CHC7	35PA
	9	4305	0A16
	11	4305	0A16
	12	CHC7	35PA
	13	4332	UHCA
	14	852P	312H
	15	43F0	U34H
	16	FF10	99H5
	17	9131	5FP0
	18	1552	2262
	19	0000	0000
U452	1	0000	0000
	2	4305	0A16
	3	CHC7	35PA
	4	4332	UHCA
	5	852P	312H
	6	43F0	U34H
	7	FF10	99H5
	8	9131	5FP0
	9	1552	2262
	11	1552	2262
	12	9131	54P0
	13	FF10	99H5
	14	43F0	U34H
	15	852P	312H
	16	4332	UHCA
	17	CHC7	35PA
	18	4305	0A16
	19	0000	0000

A14

Component	Pin	Signature Version 1.0	Signature Version 2.0
P142	2	4305	0A16
	3	CHC7	35PA
	4	4332	UHCA
	5	852P	321H
	6	43F0	U34H
	7	FF10	99H5
	8	9131	5FP0
	9	1552	2262

A19

Component	Pin	Signature Version 1.0	Signature Version 2.0
P125	1	852P	312H
	2	4332	UHCA
	3	CHC7	35PA
	4	4305	0A16
P135	6	1552	2262
	7	9131	5FP0
	8	FF10	99H5
	9	43F0	U34H

Table 5-11

I/O Register Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A21	Microprocessor	670-6382-00,-01	8-20	18
A19	Time Base/Power Supply	670-6380-00	8-23	19
A16	Storage Display	670-6377-00 670-6377-01 670-6377-02	8-22	15,17
A14	Vertical Mode Switch	670-6375-00	8-15	4

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	TP477	A21
Start	↑	TP358	A21
Stop	↓	TP358	A21

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to X0000011. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—1886

A16

Component	Pin	Signature
U207	2	C5P2
	5	343A
	9	3860
	19	03PF
U213	1	C5P2
	2	03PF
	3	343A
	5	890U
	6	H36F
	7	1886
	9	1886
	10	1886
	11	1886
	12	1886
	13	A580
	14	76PF
	15	1886
U218	1	C5P2
	2	03PF
	3	343A
	5	890U
	6	3860
	10	5A0P
	11	3005
	12	1886
	13	1886
	14	593P
	15	1541

A16

Component	Pin	Signature
U223	2	F623
	5	HPA9
	6	H927
	9	013A
	12	340A
	16	U748
	19	58HP
U228	2	311U
	5	U549
	6	F93F
	9	09H7
	12	7FP3
	15	1F6H
	16	CA45
	19	F6U0
U748	2	1801
	5	1801
	6	1801
	9	1801
	12	UP0F
	15	UP0F
	16	UP0F
	19	UP0F
U753	5	1801
	6	0087
	7	1801
	10	UP0F
	12	1801
	15	UP0F

A16

Component	Pin	Signature
U759	5	5A0P
	9	H6P6
	10	1766
	11	1766
	12	H6P6
	13	1766
	14	F180
	15	1766
U723	5	5C7A
	6	H364
	15	7H0P
	9	P004
	12	5F34
	19	9963
	2	0318
	16	FCHH
U643B	4	5C7A
	5	5C7A
	6	43UF
U523	8	43UF
	9	1886
	10	43UF
U737	1	H927
	11	76PF
U776	4	F6U0
	10	U549
	13	CA45
U466	10	1F6H
	11	F93F

Table 5-11 (cont)
I/O Register Signatures

A14

Component	Pin	Signature
U358[a]	1	C5P2
	2	03PF
	3	343A
	6	1948
	5	890U
	4	0000
	15	1886
	13	1886
	12	1886
	10	1886
	9	01FP
	11	1886
	14	1886
P355[a]	5	C5P2
	6	03PF
	7	343A
	2	1948
	3	890U
	8	0000
U310[b]	19	2903
	16	P520
	15	HFA4
	12	HC94
	9	7C72
	6	FU6P
	2	1P64
	5	79PH
P307[b]	1	2903
	2	P520
	3	HFA4
	4	HC94
	5	7C72
	6	FU6P
	7	1886
P130	7	1P64

[a] P355 may be used for easy access to U358 inputs (pins 1 through 6). Outputs of U358 (pins 9 through 15) can be readily probed from the top of the instrument.

[b] P307 may be used for easy access to U310 outputs.

A19

Component	Pin	Signature
U436	5	9F84
	6	5390
	19	6A72
	16	AH4P
	15	15A9
	12	A41H
	2	P246
	9	322C
	11	C48U
U236	5	2900
	6	A165
	12	9069
	15	3648
	16	A28F
	19	7014
	2	4A47
	9	6CF5
	11	15P5
U140	2	C5P2
	5	03PF
	7	343A
U146	1	C5P2
	2	03PF
	3	343A
	4	324U
	13	C48U
	14	15P5
	10	4159
	12	32H7
	15	CH96
	9	4H1C
	11	857U
	7	8HHU
U100D	12	2PFP
U434A	2	2PFP
U110A	4	32H7
	1	CH96
	5	12U8
	6	0A7P
U118	1	853F
	15	853F
	2	6CF5
	14	7014
U120	2	322C
	14	P246

Table 5-12

Display RAM Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A16	Storage Display	670-6377-00 670-6377-01 670-6377-02	8-22	15
A21	Microprocessor	670-6382-00,-01	8-20	18

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↓	U278-10	A21
Start	↑	TP358	A21
Stop	↓	TP358	A21

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to X0001000. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—7A70

Component	Pin	Signature
U723	5	0000
	12	7A70
U618B	8	7A70
	9	0000
	12	0000
U643A	1	7A70
	2	0000
	3	7A70
U643D	11	0000
	12	7A70
	13	7A70
U523B	4	7A70
	5	7A70
	6	7A70
U238B	4	0000
	5	7A70
	6	7A70
U238C	9	7A70
	10	0000
U238D	11	7A70
	12	7A70
	13	0000
U407	1	7A70
	3	C21A
	4	HA07
	5	H0AA
	6	P030
	7	0000
	9	0000
	10	0000
	11	H0AA
	12	HA07
	13	C21A
	14	0000
	15	0000

Component	Pin	Signature
U413	1	7A70
	3	4442
	4	4U2A
	5	0772
	6	9635
	7	0000
	9	0000
	10	0000
	11	0772
	12	4U2A
	13	4442
	14	P030
	15	0000
U418	1	7A70
	3	9635
	4	1734
	5	8P54
	7	0000
	9	0000
	10	0000
	12	8P54
	13	1734
	14	9635
U637	1	4U2A
	2	4442
	3	P030
	4	9635
	5	9270
	6	74PF
	8	C21A
	9	HA07
	10	H0AA
	13	0772
U631A	1	4U2A
	2	4442
	4	H0AA
	5	HA07
	6	8F88

Component	Pin	Signature
U631B	8	C06F
	9	C21A
	10	9635
	12	P030
	13	0772
U648	1	0000
	2	HA07
	3	74PF
	4	9270
	5	74PF
	6	F783
	12	8F88
	13	C06F
U731	1	7A70
	2	C21A
	3	HA07
	4	H0AA
	5	P030
	6	4442
	7	4U2A
	8	0772
	9	9635
	11	9635
	12	0772
	13	4U2A
	14	4442
	15	P030
	16	H0AA
	17	HA07
	18	C21A

Table 5-12 (cont)
Display RAM Signatures

Component	Pin	Signature
U737	1	7A70
	2	C21A
	3	C21A
	4	H0AA
	5	H0AA
	6	4442
	7	4442
	8	0772
	9	0772
	11	7A70
	12	9635
	13	9635
	14	4U2A
	15	4U2A
	16	P030
	17	P030
	18	HA07
	19	HA07
U334	1	9635
	2	1734
	3	8P54
	4	4U2A
	5	0772
	6	H0AA
	7	HA07
	8	0000
	10	7A70
	11	HA07
	12	9635
	13	C21A
	14	0772
	15	C21A
	16	4442
	17	P030

Component	Pin	Signature
U328	1	9635
	2	1734
	3	8P54
	4	4U2A
	5	0772
	6	H0AA
	7	HA07
	8	0000
	10	7A70
	11	H0AA
	12	P030
	13	4442
	14	4U2A
	15	C21A
	16	4442
	17	P030
U234	1	0000
	2	0000
	3	C21A
	4	HA07
	5	H0AA
	6	1734
	7	F256
	9	4442
	10	4U2A
	11	0772
	12	9635
	13	P030
	14	7A70
	15	C21A
U770	3	C21A
	5	H0AA
	7	4442
	9	0772
	11	9635
	13	4U2A
	15	P030
	17	HA07

Table 5-13

System and Scratch RAM Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A21	Microprocessor	670-6382-00,-01	8-20	18

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U364-32	A21
Start	↑	TP358	A21
Stop	↓	TP358	A21

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket. Service/Options switch set to X0000010. To start or restart routine with POWER ON, move P182 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—1HF9

Component	Pin	Signature
U525	1	C71C
	2	4HCU
	3	9A55
	4	UC76
	5	HP24
	6	9C73
	7	UH73
	8	PAP7
	11	H9PP
	12	U0H1
	13	U38F
	14	U820
	15	H5C4
	16	9U82
	17	AU7U
U530	1	C71C
	2	4HCU
	3	9A55
	4	UC76
	5	HP24
	6	9C73
	7	UH73
	8	PAP7
	11	8826
	12	87A8
	13	U1FC
	14	5F49
	15	H5C4
	16	9U82
	17	AU7U

Component	Pin	Signature
U540	1	C71C
	2	4HCU
	3	9A55
	4	UC76
	5	HP24
	6	9C73
	7	UH73
	8	3999
	11	H9PP
	12	U0H1
	13	U38F
	14	U820
	15	H5C4
	16	9U82
	17	AU7U
U545	1	C71C
	2	4HCU
	3	9A55
	4	UC76
	5	HP24
	6	9C73
	7	UH73
	8	3999
	11	8826
	12	87A8
	13	U1FC
	14	5F49
	15	H5C4
	16	9U82
	17	AU7U

Component	Pin	Signature
U558	1	1HF9
	2	H9PP
	3	U0H1
	4	U38F
	5	U820
	6	8826
	7	87A8
	8	U1FC
	9	5F49
	11	5F49
	12	U1FC
	13	87A8
	14	8826
	15	U820
	16	U38F
	17	U0H1
	18	H9PP
	19	0000
U472A	3	0000
U472B	5	U72P
U472C	7	0000
U472D	9	9U82
U472E	11	H5C4
U550	2	C71C
	5	4HCU
	6	9A55
	9	UC76
	12	HP24
	15	9C73
	16	UH73
	19	AU7U

Table 5-14

Acquisition RAM (Write) Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A18	Memory	670-6379-00	8-21	14

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↓	U220-10	A18
Start	↑	U206-6	A18
Stop	↑	U206-6	A18

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to X0010011. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—4596

Component	Pin	Signature
U120	8	791C
	9	3F8H
	10	4596
	11	4596
	12	3F8H
	13	4596
U216	1	0000
	2	4596
	3	4596
	4	4596
	7	0000
	9	791C
	12	3F8H
U220	8	791C
	11	3F8H
U240	2	3F8H
	3	3F8H
	4	PC84
	5	PC84
	6	627P
	7	627P
	8	CHU8
	9	CHU8
	11	HFP7
	12	HFP7
	13	41F7
	14	41F7
	15	FA11
	16	FA11
	17	8C36
	18	8C36
U206	2	4596
	3	FA11
	4	41F7
	5	HFP7
	11	UPA2
	12	HFP7
	13	41F7
	14	FA11
	15	57P4

Component	Pin	Signature
U210	2	4596
	3	PC84
	4	627P
	5	CHU8
	6	8C36
	11	8C36
	12	CHU8
	13	627P
	14	PC84
U306	1	FA11
	2	41F7
	3	HFP7
	4	UPA2
	5	8C36
	6	CHU8
	7	627P
	9	8C36
	11	FA11
	13	41F7
	15	HFP7
U312	1	FA11
	2	41F7
	3	HFP7
	4	UPA2
	5	8C36
	6	CHU8
	7	627P
	9	3F8H
	11	PC84
	13	627P
	15	CHU8
U508	1	FA11
	2	41F7
	3	HFP7
	4	UPA2
	5	8C36
	6	CHU8
	7	627P
	9	8C36
	11	FA11
	13	41F7
	15	HFP7

Component	Pin	Signature
U512	1	FA11
	2	41F7
	3	HFP7
	4	UPA2
	5	8C36
	6	CHU8
	7	627P
	9	3F8H
	11	PC84
	13	627P
	15	CHU8
U112	2	3F8H
	3	PC84
	4	627P
	5	PC84
	6	627P
	7	CHU8
	8	8C36
	9	CHU8
	11	4596
	12	HFP7
	13	UPA2
	14	HFP7
	15	41F7
	16	FA11
	17	41F7
	18	FA11
	19	8C36

Table 5-15

Acquisition Data Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A18	Memory	670-6379-00	8-21	14

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	TP446	A18
Start	↑	TP252	A18
Stop	↓	TP252	A18

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to X0010000. A/D Converter Simulator installed in U456 socket on A18. Counter chain test jumper P420 on A19 set to TEST position. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—6PCP

Component	Pin	Signature	Alternate Signature
U312[a]	9	0000	6PCP
	11	7232	3919
	13	8C4P	9F46
	15	P39F	282U
U248	2	6PCP	
	3	6PCP	
	4	3CPF	
	5	3CPF	
	6	5A34	
	7	5A34	
	8	1F8F	
	9	1F8F	
	12	2595	
	13	2595	
	14	U97F	
	15	U97F	
	16	91FC	
	17	91FC	
	18	A70F	
	19	A70F	
U448	2	57A7	7232
	3	1F8F	1F8F
	4	5A34	5A34
	5	74UC	P39F
	6	F417	CCPA
	7	3CPF	3CPF
	8	6PCP	6PCP
	9	C75U	5CAU
	12	8A67	1FH2
	13	A70F	A70F
	14	91FC	91FC
	15	9104	9163
	16	A55U	8C4P
	17	U97F	U97F
	18	2595	2595
	19	0000	6PCP

[a] If initial signature on U312-9 is 0000, use "Signature" column throughout this test. If initial signature on U312-9 is 6PCP, use "Alternate Signature" column. Should an incorrect signature be obtained, recheck the signature on U312-9 to verify that logic state did not change.

Component	Pin	Signature	Alternate Signature
U320	2	5CAU	AHH7
	3	C75U	5CAU
	4	8A67	1FH2
	5	1FH2	5788
	6	CCPA	8414
	7	F417	CCPA
	8	9104	9163
	9	9163	1150
	12	0000	6PCP
	13	0000	6PCP
	14	57A7	7232
	15	7232	3919
	16	8C4P	9F46
	17	A55U	8C4P
	18	74UC	P39F
	19	P39F	282U
U432	1	5A34	5A34
	5	00FU	00A8
	6	0000	0000
	7	6P71	6P16
	9	2595	2595
	10	0000	6PCP
	11	1F8F	1F8F
	12	57A7	7232
	13	A55U	8C4P
	14	U97F	U97F
	15	74UC	P39F
U426	1	6PCP	6PCP
	2	6P71	6P16
	3	0000	0000
	4	00FU	00A8
	5	0000	0000
	9	91FC	91FC
	10	9104	9163
	11	3CPF	3CPF
	12	F417	CCPA
	13	8A67	1FH2
	14	A70F	A70F
	15	C75U	5CAU

Table 5-16

Acquisition Address Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A18	Memory	670-6379-00	8-21	14

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	TP446	A18
Start	↑	U206-11	A18
Stop	↑	U206-11	A18

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to X0010000. A/D Converter Simulator installed in U456 socket on A18. Counter chain test jumper P420 on A19 set to TEST position. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—4596

Component	Pin	Signature
U206	9	4596
	7	P254
	15	57P4
	14	FA11
	13	41F7
	12	HFP7
	11	UPA2
	2	791C
U210	7	4596
	10	4596
	15	P254
	14	PC84
	13	627P
	12	CHU8
	11	8C36
	1	4596
	2	791C
U440A	1	4596
	2	791C
	3	0000
	4	4596
	5	3F8H
	6	791C

Component	Pin	Signature
U540	1	0000
	2	0000
	3	4596
	6	0000
	7	791C
	9	3F8H
	10	0000
	11	3F8H
	13	4596
	14	4596
	15	0000
U216	1	4596
	3	791C
	4	791C
	6	0000
	7	0000
	9	791C
	10	791C
	11	4596
	12	791C
	13	791C
	15	0000

Table 5-17

Acquisition RAM (Read) Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A18	Memory	670-6379-00	8-21	14

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U108-1	A18
Start	↑	TP358	A21
Stop	↓	TP358	A21

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to X0010011 To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—4596

Component	Pin	Signature
U108	2	3F8H
	3	3F8H
	4	PC84
	5	PC84
	6	627P
	7	627P
	8	CHU8
	9	CHU8
	11	HFP7
	12	HFP7
	13	41F7
	14	41F7
	15	FA11
	16	FA11
	17	8C36
	18	8C36
	19	0000

Component	Pin	Signature
U512	10	3F8H
	12	PC84
	14	627P
	16	CHU8
U508	10	8C36
	12	FA11
	14	41F7
	16	HFP7
U312	10	3F8H
	12	PC84
	14	627P
	16	CHU8
U306	10	8C36
	12	FA11
	14	41F7
	16	HFP7

Table 5-18

Stop at 512 Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A16	Storage Display	670-6377-00 670-6377-01 670-6377-02	8-22	15,16

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U245-3	A16
Start	↑	U618-9	A16
Stop	↑	U623-4	A16

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to X0001010. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—4596

Component	Pin	Signature
U407	11	CHU8
	12	627P
	13	PC84
	14	3F8H
U413	11	HFP7
	12	41F7
	13	FA11
	14	8C36
U418	12	0000
	13	0000
	14	CC34
U234	2	3F8H
	3	PC84
	4	627P
	5	CHU8
	6	0000
	7	4596
	9	FA11
	10	41F7
	11	HFP7
	12	CC34
	13	8C36

Component	Pin	Signature
U328	1	CC34
	2	0000
	3	0000
	4	41F7
	5	HFP7
	6	CHU8
	7	627P
	11	5641
	12	HU41
	13	UCHH
	14	31AU
	15	PC84
	16	FA11
	17	8C36
U334	1	CC34
	2	0000
	3	0000
	4	41F7
	5	HFP7
	6	CHU8
	7	627P
	11	HPH7
	12	590C
	13	6FU4
	14	1F9H
	15	PC84
	16	FA11
	17	8C36

Component	Pin	Signature
U623	1	HFP7
	2	0000
	3	0000
	5	4596
	6	4596
	10	0000
	11	0000
	12	CC34
	13	0000
U435	4	590C
	5	1F9H
	6	31AU
	7	UCHH
	8	HU41
	9	5641
	10	HPH7
	11	6FU4

Table 5-19

GPIB Data Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A17	GPIB	670-6378-00	8-24	23
A21	Microprocessor	670-6382-00,-01	8-20	18

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U460-4	A17
Start	↑	TP358	A21
Stop	↓	TP358	A21

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to 11111000. GPIB cable J135 disconnected. GPIB switch talk address set to 00000 and TALK ONLY switch set to 0 (off). To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—5456

Component	Pin	Signature
U450	1	5456
	10	54A7
	12	62UP
	15	3396
U460	1	3396
	2	62UP
	3	54A7
	5	0000
	6	5456
	7	75C4
	9	177A
	10	4672
	11	701C
	12	5446
	13	5476
	14	5416
	15	54H7
U340	2	40A3
	5	7C49
	6	040F
	9	0104
	12	0203
	16	4C32
	19	PA2A
U320[a]	1	54H7
	2	5456
	4	5456
	6	5456
	10	5456
	12	5456
	14	5456
	15	54H7
U320[b]	1	54H7
	2	0000
	4	0000
	6	0000
	10	0000
	12	0000
	14	0000
	15	54H7

Component	Pin	Signature
U330	1	75C4
	2	5456
	4	0000
	6	0000
	8	PA2A
	12	0000
	14	5456
	16	0000
	18	0000
	19	75C4
U310D	8	5456
U310E	10	505A
	11	040F
U350	1	5456
	2	U706
	5	UU73
	6	PUU4
	9	1PUF
	11	701C
	12	7CUP
	15	CUHU
	16	UHF2
	19	HF17
U442A	1	0000
	2	505A
	3	5456
U442B	4	5456
	5	0000
	6	0000
U434B	3	PA2A
	5	5456
	6	CP7F

[a] Signatures with all switches on GPIB switch (S210) set to OPEN (OFF).

[b] Signatures with all switches on GPIB switch (S210) closed (ON).

Table 5-19 (cont)
GPIB Data Signatures

Component	Pin	Signature
U434C	8	0000
	9	5456
	10	5456
	11	5456
U152	1	0000
	2	8840
	3	HF16
	4	HF17
	5	U706
	6	U707
	7	A351
	9	A995
	10	UHF3
	11	UHF2
	12	CP7F
	13	UU73
	14	UU72
	15	AC24
U168	1	0000
	2	CCA3
	3	PUU5
	4	PUU4
	5	CUHU
	6	CUHP
	7	PC88
	9	4AAC
	10	1PUH
	11	1PUF
	12	CP7F
	13	7CUP
	14	7CUU
	15	2UA9
U342	1	4672
	2	HF16
	4	UHF3
	6	CUHP
	8	7CUU
	12	1PUH
	14	PUU5
	16	UU72
	18	U707
	19	4672
U121	3	0000
	4	0000
	11	7C49
	12	CP7F
	14	0000
U110	2	5456
	7	5456
	9	5456
	12	5456
	15	1U64
U410A	1	5476
	3	0000
	5	0000

Table 5-20

Acceptor Handshake Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A17	GPIB	670-6378-00	8-24	23
A21	Microprocessor	670-6382-00,-01	8-20	18

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U460-4	A17
Start	↑	TP358	A21
Stop	↓	TP358	A21

468 Setup

468 in Servicing setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to 11111001. GPIB cable J135 disconnected. TP335 connected to TP112. TP333 connected to TP114. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—0UP7

Component	Pin	Signature
U460	1	0ACC
	2	0UP7
	3	0UA5
	6	0UP7
	7	055P
	9	0AUC
	12	0UP5
	13	0UA7
U330	2	0UP7
	4	03U8
	6	03FA
	8	0000
	12	0000
	14	0U16
	16	0081
	18	03U8
U121	2	0U16
	3	00U1
U110	2	0U16
	3	00U1
	6	03FA
	7	0F2H
	9	0F1H
	10	03UA

Component	Pin	Signature
U430A	3	0UP5
	4	0F1H
	5	03U8
	6	0F1U
U410A	1	0UA7
	2	03UA
	3	00U1
	5	0081
U410B	8	0UH7
	11	0UA7
	13	00U1
U421A	1	03UA
	2	00U1
	12	00U1
	13	03UA

Table 5-21

Source Handshake Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A17	GPIB	670-6378-00	8-24	23
A21	Microprocessor	670-6382-00,-01	8-20	18

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U460-4	A17
Start	↑	TP358	A21
Stop	↓	TP358	A21

468 Setup

468 in Servicing setup. Service Test ROM installed in U565 socket on A21. Service/Options switch set to 11111010. GPIB cable J135 disconnected. TP335 connected to TP111. TP333 connected to TP113. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—UFP6

Component	Pin	Signature	Alternate Signature
U450	10	U8PF	
	12	U8PF	
	15	54C6	
U460	1	54C6	
	2	U8PF	
	3	U8PF	
	7	AF5A	
	9	54C6	
	14	U8PF	
U330	2	UFH5	
	4	0000	
	6	P4HC	
	8	7UF7	
	12	183H	
	14	UFP6	
	16	0000	
	18	0000	
U340	2	78FA	
	6	0007	
	19	7UF7	
U121	2	9F11	
	4	60U7	
	12	8321	
	14	0032	
	15	UFH4	
U110	2	UFP6	
	3	0000	
	6	P4HC	
	7	183H	
U310A	1	9F11	
	2	60U7	
U310E	10	UFP1	
	11	0007	
U310F	12	UFP6	
	13	0000	

Component	Pin	Signature	Alternate Signature
U442A[a]	1	0003	(0000)
	2	UFP1	
	3	UFH5	(0000)
U442B[a]	4	UFH5	(183H)
	5	0003	
	6	0032	
U442C[a]	9	60U7	
	10	9F11	(0000)
U442D[a]	11	9F11	(0000)
	12	P4HC	
	13	0000	(183H)
U434A	1	78FA	
	2	UFP6	
	13	P4HC	
U434B	3	7UF7	
	4	UFH5	
	6	8321	
U434C	8	0033	
	11	UFH5	
U421C	8	67UA	
	10	7UF7	
	11	P4HC	
U430B	8	9F11	
	10	9F11	
	13	67UA	
U440A[a]	1	U8PF	
	3	0000	(183H)
	5	183H	
	6	P4HC	

[a] Signatures in parentheses are derived by jumpering +5 V to U442-8 to break feedback path.

Table 5-22
Record Counter String Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A19	Time Base/Power Supply	670-6380-00	8-23	19

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U120-9	A19
Start	↑	U110B-9	A19
Stop	↑	U524-13	A19

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket. Service/Options switch set to X0010001. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—991H

Table 5-23
Time Base Counter String Signatures

Version 1.0

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A19	Time Base/Power Supply	670-6380-00	8-23	19

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	U220B-9	A19
Start	↑	P420-1	A19
Stop	↑	P420-1	A19

468 Setup

468 in Servicing Setup. Service Test ROM installed in U565 socket. Service/Options switch set to X0010000. P420 moved to TEST position. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—53UC

OPTIONS

Your instrument may be equipped with one or more options. This section provides a description of the available options and indicates, if necessary, where more detailed information is located in this manual.

NOTE

The 468 Oscilloscope cannot be equipped with both Option 02 and Option 11 due to use of common space.

OPTION 02—GPIB

When equipped with this option, the 468 has the capability to transmit a waveform message on a GPIB (General Purpose Interface Bus). During transmission, the last waveform acquired by the 468 will be sent to either a bus controller or a listener instrument. The waveform message format will conform to the Waveform Transmission Standard as specified in the Tektronix Standard, "General Purpose Interface Bus (GPIB, Codes and Formats (Rev C)".

Option 02 operating information and circuit descriptions are contained in this section of this manual. The schematic diagram, circuit board illustration, and block diagram are located in Section 8 of Volume II. Electrical and mechanical replaceable parts of Option 02 are integrated into the standard Replaceable Parts lists also located in Volume II of this manual.

NOTE

Section 8 of the internal Service/Options switch must be set to the closed position for the GPIB option to be enabled. Refer to Figure 5-6 in the Maintenance section of this manual for the switch location.

OPTION 04—EMC ENVIRONMENTAL

The instrument is modified to meet certain specification requirements related to conducted and radiated electromagnetic interference. This option does not affect the basic instrument operating instructions presented in this manual. Option 04 reduces conducted interference over the frequency range of 150 kHz to 25 MHz and radiated interference over the frequency range of 150 kHz to 1 GHz by the following modifications:

1. A cathode-ray tube mesh is installed to minimize crt faceplate radiation.
2. Capacitors are added acros the transformer secondary windings and from the B +GATE connector to ground to reduce conducted interference.
3. Shielding is added over the Storage Display circuit board and at the front rame to reduce radiated interference.
4. If the Option 02 GPIB circuit board is installed, additional shielding is added over the top of the board to reduce radiated interference.

Electrical circuitry changes are reflected in the partial schematic diagram of the power-input and transformer circuitry shown in Figure 6-1.

Electrical and mechanical replacement parts for Option 04 are integrated into the standard Replaceable Parts List located in Volume II of this manual.

OPTION 05—TV SYNC SEPARATOR

This option provides the instrument with front-panel selection of additional trigger-signal processing capabilities to facilitate observation and measurement of composite video and related television waveforms. A choice of either FIELD 1 or FIELD 2 sync is made available to the A Trigger Generator via the A TRIGGER SLOPE switch.

Option 05 operating information and circuit descriptions are located in this section. The schematic diagrams and circuit board illustration are located in the Diagrams section of Volume II of this manual. Replaceable electrical and mechanical parts lists are located in Volume II of this manual.

OPTION 11—X-Y OUTPUT

This option enables the 468 to convert the digital data stored in memory into analog X and Y outputs for driving an X-Y Plotter. Because the operation is largely automatic, only a few switch settings are required.

Option 11 operating information and circuit descriptions are located in this section. The schematic diagrams and circuit board illustration are located in the Diagrams section of Volume II of this manual. Replaceable electrical and mechanical parts list are located in Volume II of this manual.

OPTION 12—AVERAGING
(Standard SN B032430 and up)

This option enables the 468 digital storage circuitry to average the input signal for a selected number of sweeps. The displayed waveform will be updated at the end of each averaging cycle, and then the cycle will be repeated. Acquisition of low-amplitude waveforms is greatly enhanced by noise cancellation that occurs in the averaging process.

Operating information and circuit descriptions are located in Section 2 and 3 of this volume. Averaging option circuitry is integrated into the standard instrument schematic diagrams located in Section 8 of Volume II of this manual. Electrical and mechanical replaceable parts of Option 12 are integrated into the standard Replaceable Parts list also located in Volume II of this manual.

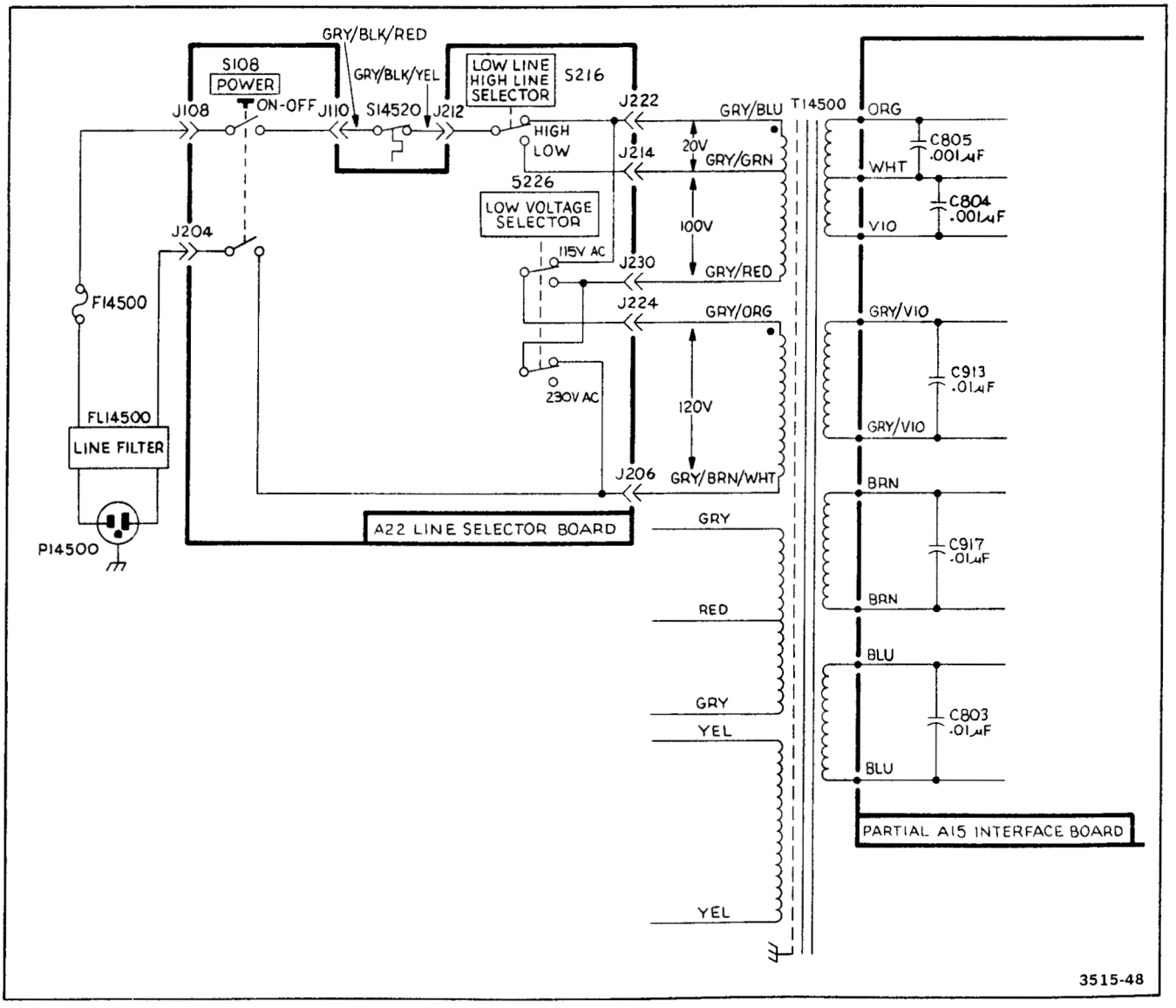


Figure 6-1. The 468 Option 04 power-input and transformer circuitry.

OPTION 02—GPIB

GENERAL INFORMATION

The GPIB is a digital interface that allows efficient communication between the components of an instrumentation system. It is used for transmitting and receiving data between self-contained instruments or devices and acts as an interface system that is independent of device functions.

If the 468 is to be used without a GPIB hookup, service personnel can disable the GPIB option by setting section 8 of the internal Service/Options switch (S707) to the "OPEN" position. To enable the GPIB option prior to connecting the 468 to a GPIB system, service personnel must set section 8 of the Service/Options switch to the closed position. The Service/Options switch is located on the A16 STORAGE DISPLAY board and is shown in Figure 5-6 in the Maintenance section of this manual.

A Typical System on the GPIB

Figure 6-2 illustrates a typical system using the GPIB and shows the nomemclature established for the 16 active signal lines. While only four instruments are shown, the GPIB can support up to 15 independent devices connected directly to the bus. It is possible, however, to interface more than 15 instruments to a single bus. This is accomplished by connecting several instruments to a primary device, and then connecting only the primary device to the bus. Such a scheme can be used for programmable plug-in units housed in a mainframe. In this configuration the mainframe can be addressed with a primary address code, and the plug-in units can be addressed with a secondary address code.

Instruments connected to a single bus cannot be physically separated by more than 20 meters (total cable length), and at least one more than half the number of instruments on a bus must be in the power-on state. To maintain the electrical characteristics of the bus, one device load must be connected for each two meters of cable length.

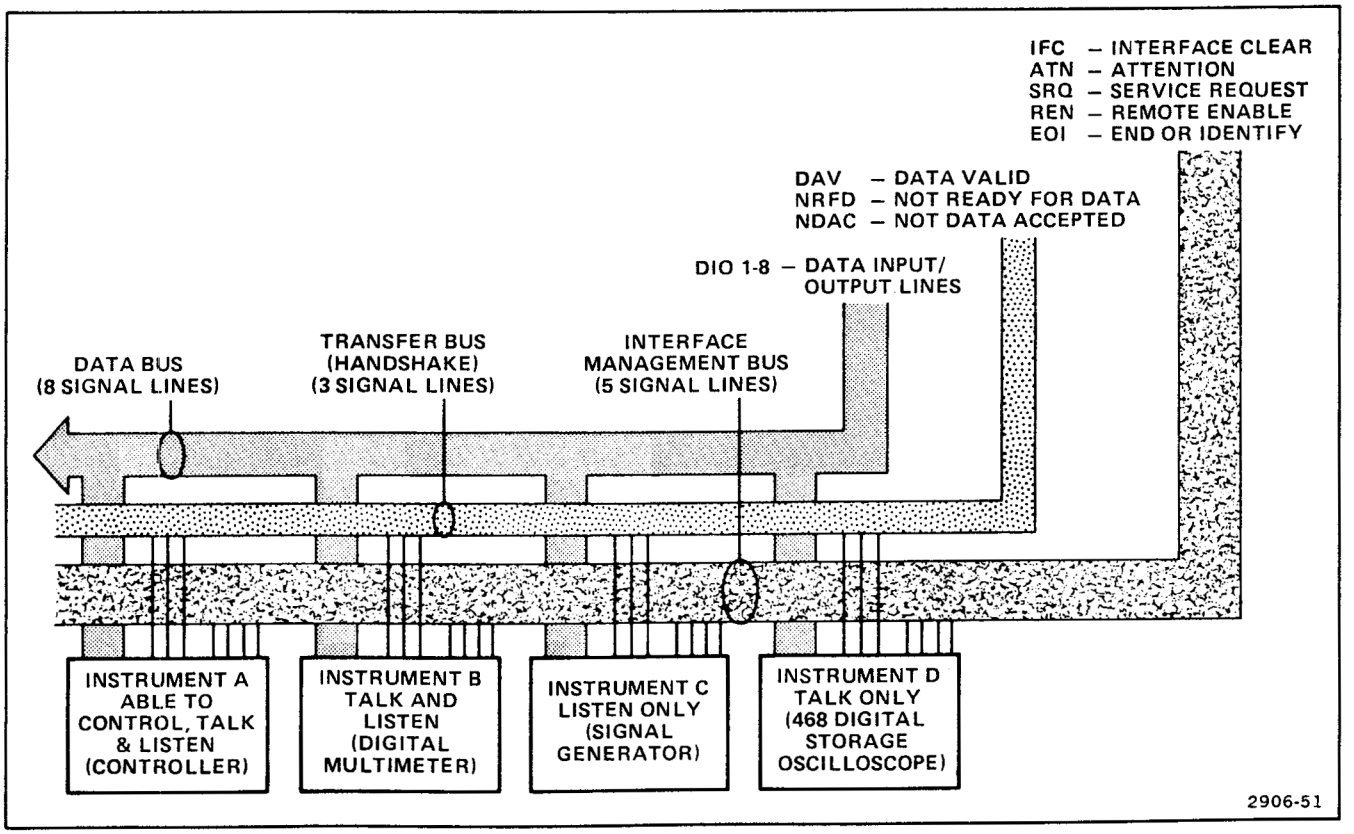


Figure 6-2. Atypical system using the general purpose interface bus (GPIB).

Controllers, Talkers, and Listeners

A talker is an instrument that can send data over the bus, while a listener is an instrument that can accept data from the bus. No instrument can communicate until it is enabled by the controller in charge of the bus. The 468 is a talker only. By setting the TALK ONLY switch (located on the 468 back panel) to the TALK ONLY position, it can be set up to operate as a talker without needing a controller on the bus. This setup is used when the 468 is in a system that has only listeners on the bus.

A controller is an instrument that determines which of the other instruments on a bus will talk and which instruments will listen during any given time interval. The controller also has the ability to assign itself as either a talker or a listener, whenever the program routine requires. In addition to designating the current talker and listeners for a particular communication sequence, the controller has the task of sending special codes and commands (called interface messages) to any or all of the instruments on the bus.

GPIB Signal Line Definitions

Figure 6-2 shows the 16 signal lines of the GPIB functionally divided into three component busses: an eight-line data transfer bus, a three-line transfer control (handshake) bus, and a five-wire management bus.

THE DATA BUS. The data bus has eight bidirectional signal lines, DIO1 through DIO8. Information, in the form of data bytes, is transferred over this bus. A handshake sequence between an enabled talker and the enabled listeners transfers one data byte (eight parallel bits) at a time. Data bytes in either an interface or device-dependent message are sent in a byte-serial, bit-parallel fashion over the data bus.

Since the GPIB handshake sequence is an asynchronous operation, the data transfer rate at any one time is only as fast as the slowest instrument involved in the data-byte transfer. A talker cannot place data bytes on the bus faster than any one listener can accept them.

THE TRANSFER BUS (HANDSHAKE). Each time a data byte is sent over the data bus, an enabled talker and all enabled listeners execute a handshake sequence via the transfer bus. A typical handshake routine showing the activity on the transfer-bus signal lines is illustrated in Figure 6-3. The attention (ATN) line is also shown to illustrate the controller's role in the process.

NOTE

On the GPIB signal lines, the TRUE level is the low voltage amplitude and the FALSE level is the high voltage amplitude.

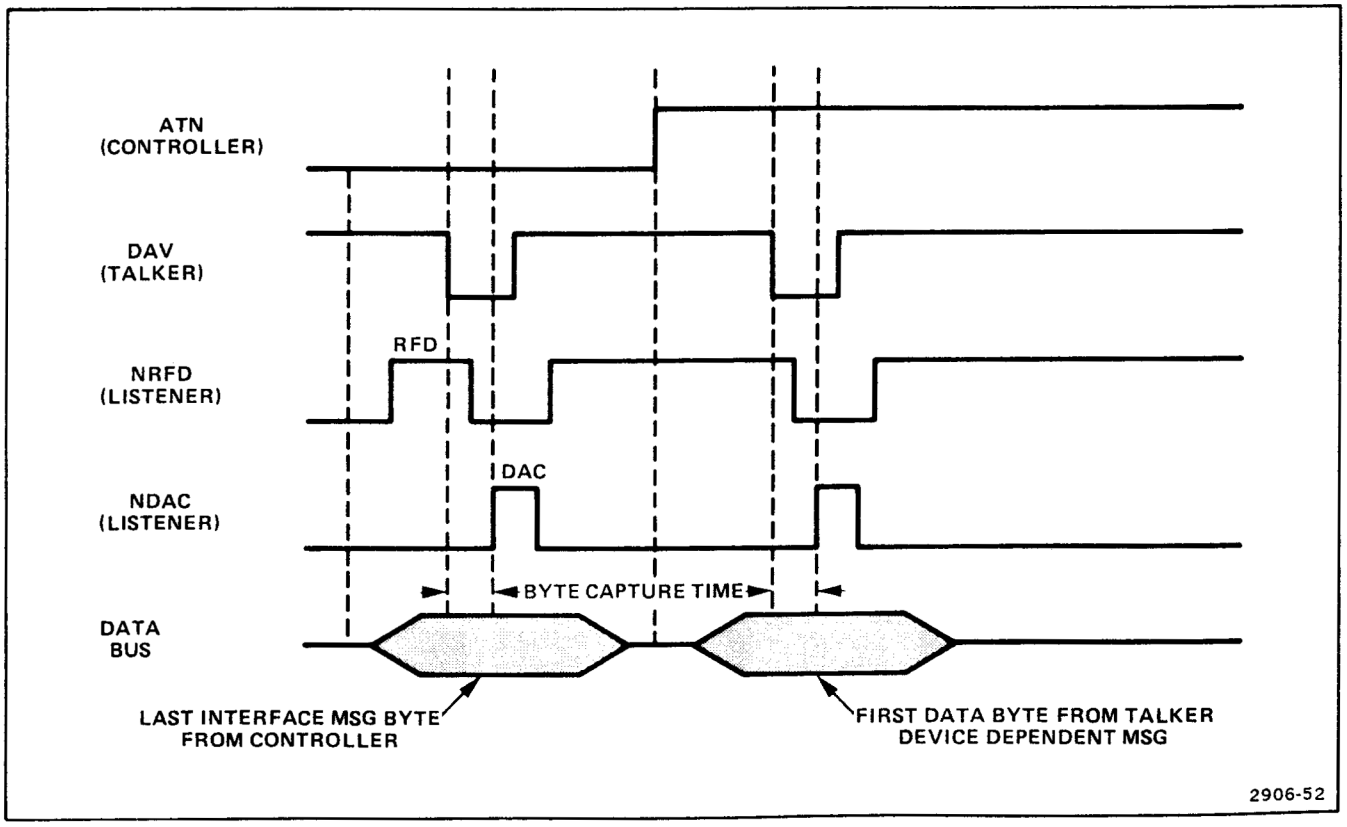


Figure 6-3. A typical handshake timing sequence (idealized).

NOT READY FOR DATA (NRFD)—An asserted (TRUE) NRFD message indicates that one or more assigned listeners are not ready to receive the next data byte from the talker. When all of the assigned listeners for a particular data-byte transfer have released their NRFD, the NRFD message becomes FALSE. This RFD (Ready for Data) message tells the talker it may place the next data byte on the data bus.

DATA VALID (DAV)—The DAV message is asserted TRUE by the talker after the talker places a data byte on the data bus. When TRUE, DAV tells each assigned listener that a new data byte is on the data bus. The talker is inhibited from asserting DAV as long as any listener asserts the NRFD message.

NOT DATA ACCEPTED (NDAC)—Each assigned listener holds the NDAC message asserted TRUE until that listener accepts the data byte currently on the data bus. When all assigned listeners accept the current data byte, the NDAC message becomes FALSE. This DAC (Data Accepted) message tells the talker that all assigned listeners have accepted the current data, and the data may be removed from the bus.

When both NDAC and NRFD are FALSE at the same time, an invalid state exists on the bus, indicating that no listener is on the bus.

THE MANAGEMENT BUS. The management bus is a group of five signal lines (IFC, ATN, SRQ, REN, and EOI) which are used to control the operation of the GPIB.

INTERFACE CLEAR (IFC)—The system controller asserts the IFC message TRUE to place all interface circuitry in a predetermined quiescent state (this may or may not be the power-on state). Only the system controller can generate this signal. While IFC is TRUE, no other messages will be recognized.

ATTENTION (ATN)—A controller asserts the ATN message TRUE when instruments connected to the bus are being enabled as either talkers or listeners and when there is other interface-control traffic. As long as the ATN message is TRUE, only instrument address codes and control messages can be transferred over the data bus. With the ATN message FALSE, only those instruments enabled as a talker and listener(s) can transfer data. Only a controller can generate the ATN signal.

SERVICE REQUEST (SRQ)—Any instrument connected to the bus can request the controller's attention by sending the SRQ message. The controller may respond by executing a serial poll to determine which instrument is requesting service. An instrument requesting service identifies itself by asserting its DIO7 line TRUE in its status byte. When polled, the instrument requesting service removes the SRQ message.

REMOTE ENABLE (REN)—The system controller sends the REN message TRUE whenever the interface system is operating under remote program control. Used with other control messages, the REN message causes an instrument on the bus to select between two alternate sources of programming data. A remote-local interface function indicates to an instrument that it will receive information input from either the front-panel control (LOCAL) or from the interface (REMOTE). Since the 468 does not have a remote capability, it transmits data as determined by the setting of its front-panel controls.

END OR IDENTIFY (EOI)—A talker can use the EOI message to indicate the end of a data-transfer sequence. The talker sends the EOI message TRUE as the last byte of data is transmitted. In this sense, EOI is essentially a ninth data line and must observe the same setup times as the data bus lines.

GPIB Connector

Physical arrangement of the 24-pin GPIB connector (located on the rear panel of the 468) meets IEEE-488 (1978) GPIB standards. Sixteen pins are assigned to specific signals, and eight to shields and grounds. Voltage and current values required at the connector nodes are based on TTL technology (power source not to exceed +5.5 volts referenced to ground). The logic levels are defined as follows. Logical 1 is a TRUE state, low-voltage level ($\leq +0.8$ V), that is implemented when the signal line is asserted. Logical 0 is a FALSE state, high-voltage level ($\geq +2$ V), that is implemented when the signal line is not asserted. See Figure 6-4 for an illustration of connector pin assignments and physical arrangement.

Use a standard shielded GPIB cable with all the shields and grounds correctly connected to interconnect the 468 to other instruments on the bus. See the "Accessories" tab page at the back of Volume II of this manual for recommended part numbers.

Interface Functions and Commands

Since the 468 is a talker only, not all of the interface functions are enabled. Table 6-1 is a listing of the function subsets, including a description of the 468 capabilities with regard to those subsets. Table 6-2 is a listing of the interface commands to which the 468 responds, along with a brief description of each response.

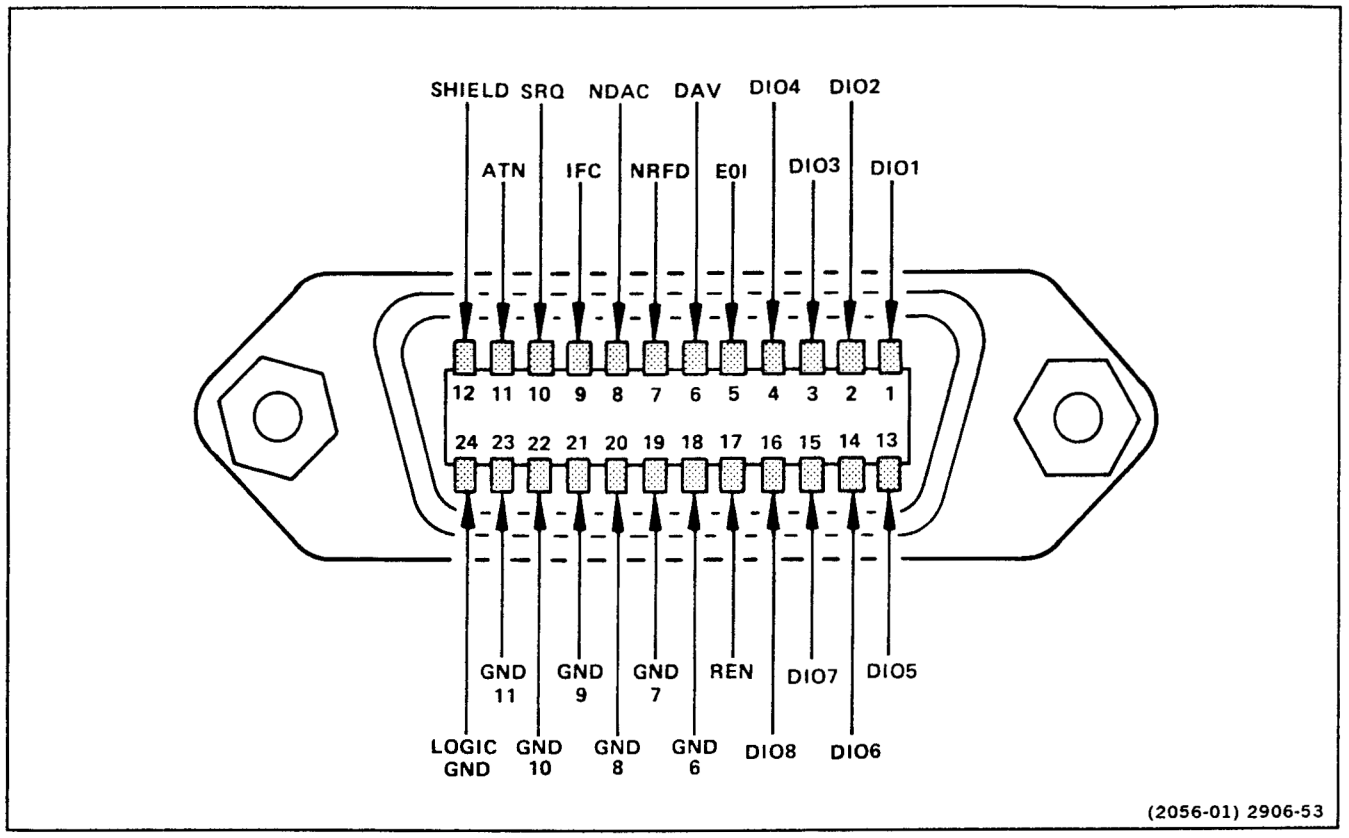


Figure 6-4. GPIB connector and pin assignments.

Table 6-1
468 GPIB Function Subsets

Identification	Description	States Omitted	Other Requirements	Other Required Subsets Used
SH1 (Source Handshake)	Complete Capability	None	None	T1
AH1 (Acceptor Handshake)	Complete Capability	None	None	None
T1 (Talker)	Basic Talker, Serial Poll, Talk Only Mode	None	Omit [MLA∧(ACDS)]	SH1 and AH1
L0 (Listener)	No Capability	All	None	None
SR1 (Service Request)	Complete Capability	None	None	T1
RL0 (Remote/Local)	No Capability	All	None	None
PP0 (Parallel Poll)	No Capability	All	None	None
DC2 (Device Clear)	Omit Selective Device Clear	None	Omit [SDC∧(LADS)]	AH1
DT0 (Device Trigger)	No Capability	All	None	None
C0 (Controller)	No Capability	All	None	None

Table 6-2

Interface Commands

GPIB Message	468 Interface Response
Interface Clear (IFC)	The 468 returns to the serial-poll-idle state (SPIS) and enters the talker-idle state (TIDS). End or Identify (EOI) and new byte available (nba) become unasserted. Talker LED (TIDS) goes out, but the service request LED (SRQ) remains on if asserted. The 468 interface then waits for IFC to become unasserted before processing other GPIB traffic, including attention (ATN).
Device Clear (DCL)	If received during transmission of data, the 468 goes to a state of having completed the transmission. The SRQ is unasserted, and the 468 must receive a new My Talk Address (MTA) before it will begin transmitting again. DCL will not clear an SRQ issued by the 468 as part of the power-on routine. To remove the power-on SRQ, the instrument must be made a talker and the status byte sent. This ensures that the controller knows the 468 is powered up on the bus.
Serial Poll Enable (SPE)	The 468 interface enters the serial-poll-mode state (SPMS).
Serial Poll Disable (SPD)	The 468 leaves serial-poll-mode state (SPMS).
My Talk Address (MTA)	Binary address set by the GPIB switch on the 468 rear panel. Bus controller sends MTA to the 468 to obtain its status byte (serial poll) or to start its transmission of waveform data.
Untalk (UNT) or Other Talk Address (OTA)	468 untalks.

GPIB Switch Operation

The GPIB switch is located on the 468 rear panel (see Figure 2-10). It is used for selecting the talk address (MTA) to which the interface will respond and for controlling the TALK ONLY switch, and the remaining five sections of the switch select a five-binary talk address. Section 2 is the most significant bit of the address, and section 6 is the least significant bit (see Figure 6-5).

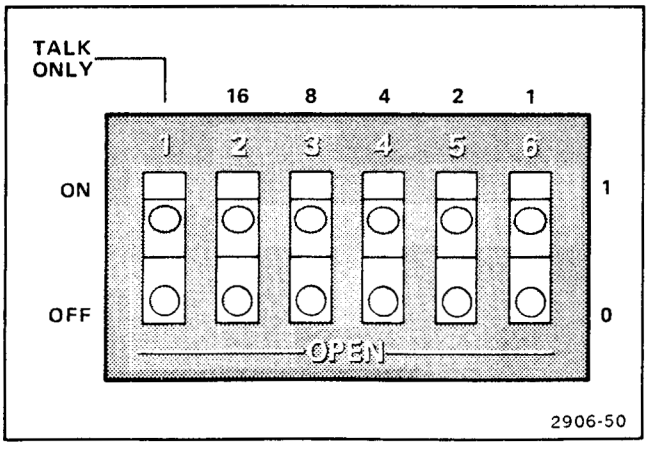


Figure 6-5. GPIB switch register.

The 468 waveform data transmission can be initiated in two ways: either by pressing the TRANSMIT push button (located on the digital storage right-side panel), or by being under the direction of a bus controller. Either method will cause the waveform to be transmitted, but the sequence of events that occur in the 468 GPIB interface and on the bus depends on the setting of the TALK ONLY switch.

TALK ONLY OFF. With a controller on the bus, the TALK ONLY mode should be OFF. This gives the controller maximum control of bus transactions. In this mode, a possible series of actions that may occur when the operator wants to send a waveform is as follows:

1. The TRANSMIT push button is pressed in.

2. A service request message (SRQ) is sent to the controller, and the 468 interface waits for the controller to respond.

3. The controller may respond by doing a serial poll. (This is optional and would not be required if the 468 were the only instrument on the bus.) A typical serial poll routine would be in the following sequence:

   a. Controller asserts the attention message (ATN) TRUE to gain control of the bus, then sends

unlisten (UNL) and untalk (UNT). This prevents the listeners from receiving status bytes and prevents the current talker from sending data when the ATN is removed.

b. Controller then sends the serial-poll-enable message (SPE) to place all devices on the bus in the serial-poll mode.

c. During the poll, the controller sends ATN and each device's talk address (MTA), one at a time. As each device receives its own talk address, the controller will remove the ATN message, and the addressed device will send its status byte. The status byte will indicate to the controller each device's present state and which one(s) require servicing. (The 468 status byte will indicate that a waveform is available when the TRANSMIT button has been pressed.)

NOTE

The 468 will send (or attempt to send) its status byte as soon as the controller removes the ATN message. Should the controller fail to assign a listener for the status byte, the 468 status byte will be lost when ATN is asserted TRUE at a later time.

d. Upon finishing the serial poll, the controller sends ATN and the serial-poll-disable message (SPD), placing all devices in the serial-poll-idle state.

4. After the poll, the controller may reconfigure the bus, assigning listeners to receive the waveform data, if necessary.

5. With the listeners assigned, the controller then sends the 468 its talk address (MTA) to make the 468 a talker. When the controller removes the ATN message this time, the 468 sends waveform data. The waveform message is then handshaked out to the listeners, one byte at a time, and the message is terminated by the 468 sending LF (line feed) and EOI (end or identify) concurrently.

NOTE

Once the waveform message is completed and EOI sent, the 468 must receive its My Talk Address (MTA) again before it will transmit any other messages. The controller cannot cause the 468 to be a permanent talker.

Under the direction of a bus controller, the 468 will initiate a message transmission whenever it receives its talk address. Either a status byte or a waveform message (depending on the state of the 468 GPIB interface when the MTA is sent) will be transmitted by the 468, when the controller removes the ATN message.

TALK ONLY ON. When the 468 is in the TALK ONLY mode, the controller has less control of the 468 GPIB interface. In this mode the 468 will never enter the talker idle state (TIDS), because it is permanently addressed as a talker. The TALK ONLY mode is most useful when there is no controller on the bus, and the 468 is used to transmit waveform data to a listener. In the TALK ONLY mode with no bus controller, a typical series of actions that may occur when the operator wants to send a waveform is as follows:

1. The TRANSMIT button is pressed in.

2. A service request (SRQ) is sent, and the 468 begins to handshake the waveform data to a listener.

3. The transmission is completed, the message is terminated with line feed (LF) and end or identify (EOI), and the SRQ message is removed.

In the TALK ONLY mode with a controller on the bus, a typical series of actions that may occur when the operator wants to send a waveform is as follows:

1. The TRANSMIT button is pressed in.

2. The SRQ message is sent, and the 468 begins the handshake routine. At this point a controller may interrupt to respond to the SRQ and perform a serial poll. A response from the controller is not necessary; and if listeners are on the bus, the 468 GPIB interface will send the waveform message unless interrupted. If a controller either performs a serial poll or interrupts the message for any reason, the 468 will resume transmitting the message as soon as ATN is removed if it is out of the serial poll mode.

3. Again, the waveform message is terminated with LF and EOI, and the SRQ message is removed.

NOTE

If a listener or controller is not present to receive the waveform data when the TRANSMIT button is pressed, the 468 will remain in the SAVE Storage Mode while attempting to send the message. To exit this condition, it is necessary to cycle the POWER switch OFF, then ON again.

When a bus controller is used, any ATN message on the bus will cause the 468 interface to respond with a message when the ATN message is removed. In the TALK ONLY mode, the 468 is permanently addressed as a talker and does not require receipt of its talk address (MTA) before commencing a message transmission. The message to be sent depends on the state of the interface when the ATN message is removed. If the interface is in the serial-poll-active state (SPAS), a status byte will be sent; and if the interface is in the talker-active state (TACS), a waveform message will be sent.

NOTE

If the 468 is in the TALK ONLY mode, a bus controller cannot assign any other talkers on the bus. Therefore, when operating with a bus controller, the TALK ONLY switch should be OFF. The TALK ONLY switch must be set to ON when the bus has only listeners and when there is no controller to respond to a service request.

Power-up State

The state of the GPIB existing when the 468 is powered up is as follows:

1. If the 468 is powered on during a transmission on the bus, an error may occur in the handshake routine.

2. A power-on service request is issued. The power-on service request must be handled by a controller to remove it from the bus. When a controller receives the power-on status byte, it may reinitiate a bus transmission if one was in progress during the 468 power-on period.

3. The 468 interface is in the talker-idle and serial-poll-idle states.

4. Each power up completely resets the 468 interface, and the interface will be ready to transmit waveform data as soon as the 468 power-up routine is completed.

NOTE

When no waveform has been acquired, only the instrument ID portion of the waveform message will be transmitted.

Power-Down State

The 468 does not have any capability for handling momentary power interrupts. No settings are retained on power down, and no power-down routine is used. If the power level drops below the logic circuitry operating level, the 468 will fail in its processing.

GPIB Status Indicator

The GPIB Status LED ($\overline{\text{TIDS}}$/SRQ), located on the left side panel of the digital storage section, will be illuminated red when the service request (SRQ) is issued by the 468. During the serial poll (when the status byte is sent), it will flash green. During the transmission of data, it will be illuminated green to indicate to the user that the interface is not in the talker-idle state (TIDS).

GPIB Status Bytes

Status information relating to the state of the 468 GPIB interface is sent to the controller in the status byte during a serial poll. Two possible conditions exist: status with a service request asserted and status with no service request asserted. Table 6-3 contains a listing of the status bytes available.

When the controller is responding to a service request from another device, the 468 status bytes without a service request asserted tell the controller the state of the 468.

Table 6-3

468 Status Bytes

Status		Status Byte			
		Binary	Octal	Hexidecimal	Decimal
SRQ ASSERTED	POWER ON	01000001	101	41	65
	TRANSMIT RQST	11000011	303	C3	195
	TON TRANSMIT RQST	11000100	304	C4	196
SRQ NOT ASSERTED	POWER ON	00000001	001	01	1
	TRANSMIT RQST	10000011	203	83	131
	TON TRANSMIT RQST	10000100	204	84	132
	NO STATUS	00000000	000	00	0

After the other device service request is handled, the controller uses the status reported by all the devices on the bus to determine what action occurs next. The action depends on controller programming.

As an example, assume that the 468 is in the middle of a transmission and some other device on the bus issues a service request. The controller interrupts the transmission of the 468 by asserting attention (ATN) TRUE, and then does a serial poll to determine the status of each device on the bus. Having handled the service request, the controller can then use the status reported by the 468 to restart or continue the transmission.

The controller may interrupt the transmission either synchronously (in step with the handshake) or asynchronously (no regard to handshake progress). If the controller interrupts synchronously, the last data byte sent will be data accepted (DAC) by all the assigned listeners, and it will not be lost. An asynchronous interruption may or may not cause the loss of a byte, depending upon the point of interruption.

The method of interruption may determine what action takes place to restart the 468 transmission. If no data is lost, the controller can reassign listeners and remove attention (ATN) to cause the 468 to resume transmission at the point of interruption. If data was lost, the controller might send a device clear (DCL) to reset the 468 (and all the listeners on the bus) and assign listeners. It will then send the 468 talk address to restart the waveform transmission.

468 GPIB Message Protocol

When the 468 is connected to a bus having a bus controller, it will send a message whenever it receives its talk address (MTA). The talk address is set by the GPIB switch located on the 468 rear panel (see GPIB Switch Operation).

If a Device Clear (DCL) message is received by the 468 during a transmission, the 468 stops transmitting and moves to a state equivalent to a completed transmission. The MTA message must be sent by the controller before another transmission can begin. A DCL message will not turn off the SRQ issued by the 468 as part of the power-on routine. To remove the power-on SRQ, the instrument must first be made a talker and the status byte sent. This ensures that the bus controller knows the 468 is powered up on the bus.

468 Message

The message sent by the 468 conforms to Tektronix Standard General Purpose Interface Bus (GPIB), Codes and Formats, Revision C and Appendices.

The term "message" as used here, refers to a device-dependent remote message. It is not an interface message, and it does not interfere with interface message coding or use.

A message represents a given amount of information, with the beginning and ending clearly defined. It is communicated between the 468 (as a talker) and one or more devices acting as listeners. The message begins when the 468

first begins functioning as a talker and receiving devices begin functioning as listeners.

MESSAGE FORMAT. A waveform message consists of an identification block and 0, 1, 2, or 3 waveforms, separated by delimiters. The following message format is described using BNF notation. The BNF symbols used are defined in Table 6-4.

Table 6-4
BNF Symbol Notation

Symbol	Definition
<>	Defined element.
::=	Is defined as.
()	Explanation.
{}	Grouping.
[]	Optional, may be omitted.
¦	Exclusive OR.
&	AND — designates concurrent messages on the bus (the element on the right of & is concurrent with the last element of the expression on the left.
"	String argument delimiter.
:	Link argument delimiter.
;	Message unit delimiter.
,	Argument delimiter.
%	Precedes a binary block argument.

The transmitted message is in the following format:

<MESSAGE>::=<ID>;
[<WAVEFORM>[;<WAVEFORM>]]]<TERMINATOR>

Each defined element is further broken down as follows:

<ID>::=ID <SCOPE TYPE>,<C AND F VERSION>,<FIRMWARE VERSION>

These message elements are further defined as follows:

<SCOPE TYPE>::=TEK/468 (Identifies the instrument as a Tektronix 468 Digital Storage Oscilloscope).

<C AND F VERSION>::=V79.1 (States the version of Tektronix Standard GPIB Codes and Formats in use—Version 79.1).

<FIRMWARE VERSION>::=FV:00000 (States the firmware version installed in the instrument).

An example of the identification element is:

ID TEK/468,V79.1,FV:1.0

NOTE

All punctuation, including spaces, must be as shown.

The waveform element is in the following format:

<WAVEFORM>::=<PREAMBLE>,<BLOCK BINARY CURVE>

These message elements are further defined as follows:

<PREAMBLE>::=WFMPRE <WPA>[{,<WPA>}...]

Where <WPA>::=(WAVEFORM PREAMBLE ARGUMENTS)

The following waveform preamble arguments are listed in the order in which they are transmitted in a message. After each, a brief description is given.

<WAVEFORM ID>::=WFID:"{CH1¦CH2¦ADD}{AC¦DC¦GND¦UNK}"

The defined elements of <WAVEFORM ID> are: the Vertical Mode selected for the waveform, the Input Coupling, and the Storage Mode. UNK will be sent for the Input Coupling when ADD is sent and when the Input Coupling is not the same for both channels.

<NUMBER OF POINTS>::=NR.PT:{256¦512}

The defined element is the length of the data record for the waveform being transmitted (256 or 512).

<POINT FORMAT>::=PT.FMT:Y

The Y-coordinate is transmitted, but the X-coordinate is determined from the data point number and the X INCREMENT.

<X INCREMENT>::=XINCR:{100¦40¦20¦10¦4¦2¦1¦400¦200}

The defined element increment multiplied by the X UNITS is the time between data points.

<X ORIGIN>::=XZERO:0

X ORIGIN is defined as zero.

<POINT OFFSET>::=PT.OFF:{32!64!224!448}

The defined element is the trigger point, determined by the STORAGE WINDOW (PRE TRIG or POST TRIG). Actual trigger point is within ±3 of the given example values for point offset.

<X UNITS>::=XUNIT:{S!MS!US!NS}

X UNITS are used with the X INCREMENTS for the time scale of the waveform.

<Y MULTIPLIER>::=YMULT:{200!400!800'2!4!8!20!40!80!25!50!100!250!500!1000}

The defined element is a vertical scaling quantity determined by the VOLTS/DIV setting.

<Y ORIGIN>::=YZERO:0

Y ORIGIN is defined as zero.

<Y VALUE OFFSET>::=YOFF:<GND REF VALUE>

The defined element is the value of the vertical position of ground reference.

<Y UNITS>::=YUNIT:{V!MV!UV!DIV}

Defined element is the unit attached to the vertical value of each data point.

<DATA ENCODING>::=ENCDG:BIN

Curve data encoding is in low-level binary code.

<BINARY FORMAT>::=BN.FMT:RP

Each number sent is a binary, positive integer.

<BYTES PER NUMBER>::=BYT/NR:1

One byte is sent for each number.

<BITS PER NUMBER>::=BIT/NR:8

Eight bits are in each byte.

This ends the message preamble. The message continues with the waveform binary information.

<BLOCK BINARY CURVE>::=%<BINARY COUNT><BINARY DATA POINT>...<CHECKSUM>

These defined elements contain the waveform data and are further broken down as follows:

<BINARY COUNT>::=

(A two-byte binary integer to specify the number of data bytes plus the checksum byte—data bytes + 1. The high-order byte is sent before the low-order byte.)

<BINARY DATA POINTS>

(The binary value of the waveform at a specific data point.) This area contains a binary data-point-defined element for each data point in the waveform message.

<CHECKSUM>::=

(The two's complement of the modulo 256 sum of the preceding binary data bytes and the binary count bytes. Does not include the % symbol preceding the binary count.)

After the binary information of all the displayed waveforms is transmitted, the message is ended with the terminator.

<TERMINATOR>::=LF&EOI

(Line Feed and End or Identify). Line Feed sent concurrently with End or Identify terminates the message transmission.

The following example illustrates a typical waveform message with the ID element added to make a complete message.

ID TEK/468,V79.1,FV:1.0;WFMPRE WFID:"CH1 DC",NR.PT:512,PT.FMT:Y,XINCR:40,XZERO:0,PT.OFF:64,XUNITS:NS,YMULT:40,YZERO:0,YOFF:43,YUNIT:MV,ENCDG:BIN,BN.FMT:RP,BYT/NR:1,BIT/NR:8,%<BINARY COUNT><BINARY DATA POINT>....<CHECKSUM>LF&EOI

A more detailed explanation of the codes and formats is contained in Tektronix Standard General Purpose Interface Bus (GPIB), Codes and Formats (Rev. C).

Calculating Coordinate Values

The absolute coordinate values of the waveform data points are calculated using the information obtained from the message. In the point format used (PT.FMT:Y), only the Y-values are transmitted; the X-values are determined from both the data point number and the X-increment value. The transmitted data is used in the following formulas:

$X_n = X0 + DX\ (n - N0)$ and

$Y_n = Y0 + SY\ (y_n - YR)$,

where the symbols used are defined as follows:

X_n, Y_n::=Absolute X- and Y-coordinate values at point n.

n::=data point number in the waveform curve (n = 1,2,3, ...512).

DX::=X-increment (horizontal distance between data points).

N0::=X-point offset (trigger point).

X0::=X-origin.

Y0::=Y-origin.

SY::=Y-multiplier (scaling factor).

y_n::=Y-data point value.

YR::=Y-value offset (ground reference).

X-COORDINATE VALUES. For example, the following information obtained from a sample message is used to find the X-coordinate of data point 14.

n = 14
X0 = 0
DX = 40
N0 = 64
X-units = ns

Substituting these values into the formula for X_n:

$$X_{14} = 0 + 40\ (14 - 64)$$

$$X_{14} = 40\ (-50) = -2000.$$

Adding the X-units, we find that the absolute coordinate value at data point 14 with respect to the trigger point (N0 = 64) is:

$$X_{14} = -2000 \text{ ns} = -2\ \mu\text{s}.$$

Positive X-coordinate values will be obtained for data points occurring after the trigger point.

NOTE

The position of the trigger point is determined by the selection of either PRE TRIG or POST TRIG Storage Window and by the manner in which dual-trace waveforms are stored (either ALT or CHOP).

The TIME/DIV switch setting and the horizontal graticule locations of data points 14 and 64 (trigger point) can then be determined from the X-increment, X-units, and absolute X-coordinate values.

Since there are 500 data points spanning the full 10 horizontal graticule divisions, the TIME/DIV switch setting can be found by the equation:

$$\text{TIME/DIV switch setting} = \frac{500\ DX}{10} = 50\ DX$$

where the units of DX are as specified by the X-units message element.

Substituting values into the formula, we obtain:

$$\text{TIME/DIV switch setting} = 50 \text{ data points/div} \times 40 \text{ ns/data point}$$
$$= 2000 \text{ ns/div}$$
$$= 2\ \mu\text{s/div}$$

The horizontal distance of data point 14 from the beginning of the trace can then be calculated from the formula:

$$\text{Horizontal distance} = \frac{DX\ (n)}{\text{TIME/DIV switch setting}}$$

Substituting values into the formula, we obtain:

$$\text{Horizontal distance} = \frac{40 \text{ ns/data point} \times 14 \text{ data points}}{2\ \mu\text{s/div}}$$

$$= \frac{560 \text{ ns}}{2\ \mu\text{s/div}} = \frac{0.56\ \mu\text{s}}{2\ \mu\text{s/div}}$$

$$= 0.28 \text{ divisions}$$

The horizontal distance from the beginning of the trace at which the trigger occurs can also be calculated using the same formula:

$$\text{Horizontal distance} = \frac{40 \text{ ns/data point} \times 64 \text{ data points}}{2\ \mu\text{s/div}}$$

$$= \frac{2500 \text{ ns}}{2\ \mu\text{s/div}} = \frac{2.5\ \mu\text{s}}{2\ \mu\text{s/div}}$$

$$= 1.25 \text{ divisions}$$

Y-COORDINATE VALUES. In a similar manner the absolute value of the Y-coordinate at data point 14 can

also be calculated using the transmitted information. Continuing with the preceding example, the following Y-axis values are obtained from the sample message:

y_n = 63 (assumed value)

YO = 0

SY = 40

YR = 43

Y-units = mV

Substituting these values into the equation for Y_n:

$$Y_n = YO + SY(y_n - YR)$$

$$Y_{14} = 0 + 40\ (63 - 43)$$

$$Y_{14} = 40\ (20) = 800$$

Adding the Y-units, we find that the absolute Y-coordinate value at data point 14 is:

$$Y_{14} = 800\ mV.$$

The positive value of Y_{14} indicates that the data point is located above the ground reference. Negative Y-coordinate values will be obtained for data points occurring below the ground reference. The Vertical POSITION control may be adjusted to place the ground reference at any desired location within the graticule area. Therefore the physical location of any data point (along the vertical axis) is determined by the positioning of the ground reference.

Knowing that the vertical resolution is 25 data points per division and using the given Y-axis example value, the vertical displacement of data point 14 above the ground reference can then be calculated from the formula:

$$\text{Vertical displacement} = \frac{Y_n}{25\ SY}$$

where the units of SY are as specified by the Y-units message element.

Substituting values into the formula, we obtain:

$$\text{Vertical displacement} = \frac{800\ mV}{25\ \text{data points/div} \times 40\ \text{mV/data point}}$$

$$= \frac{800\ mV}{1000\ mV/div}$$

= 0.8 divisions above ground reference

Driver Program

A sample program listing, useful when using the Tektronix 4051 Active Terminal, is given below. This program will act as a driver for the 4051 to control a bus with the 468 connected. In order to handle the service request issued by the 468 as part of the power-up self test, the driver program, or an operator-developed program, must be running when the 468 is powered up. This program will handle the 468 SRQ, copy the waveform message, and display the waveform with graticule and preamble.

When entering the program for use, the remarks (REM) may be omitted from the program. Additionally, the program lines less than 100 must be numbered as listed.

```
  1 ON SRQ THEN 2000
  2 REM: FOR INSTRUCTIONS ON USING THIS
    PROGRAM, SEE LINE 1000
  3 GO TO 100
  4 REM USER KEY #1: RUNS PROGRAM FROM
    BEGINNING WITH INSTRUCTIONS
  5 GO TO 100
  8 REM: USER KEY #2: DEVICE CLEAR
  9 WBYTE @20,95:
 10 GO TO 100
 12 REM: USER KEY #3: REQUEST WFM FROM
    INSTRUMENT
 13 WBYTE @A+64:
 14 RETURN
 99 REM: NOTE THAT INIT SENDS AN IFC
100 INIT
105 GOSUB 1000
106 H=1
108 T=1
110 ON SRQ THEN 3000
120 ON EOI THEN 4000
130 SET KEY
140 DIM X(512),Y(512),Q(10),P$(1)
150 X=0
160 Y=0
175 E=0
180 REM: PROCESS REQUEST QUEUE
185 REM: THE QUEUE ALLOWS UP TO 9 SRQ'S TO
    BE RECEIVED AND SAVED FOR
186 REM: PROCESSING IF THIS PROGRAM IS
    ALREADY PROCESSING A PREVIOUSLY
187 REM: RECEIVED SRQ.
195 PRINT "WAITING FOR GPIB INTERRUPT"
200 IF H=T THEN 200
210 GO TO Q(H) OF 270,215,290,320
215 PRINT "ILLEGAL REQUEST"
219 REM: REMOVE REQUEST FROM QUEUE
220 Q(H)=0
223 REM: DON'T LET SRQ INTERRUPT NEXT FEW
    LINES
225 OFF SRQ
230 H=H+1
```

```
235 REM: SEE IF PAST QUEUE END; IF SO, WRAP
    AROUND TO BEGINNING
240 IF H<=10 THEN 260
250 H=1
255 REM: TURN SRQ ENABLE BACK ON
260 ON SRQ THEN 3000
265 GO TO 195
269 REM: POWER-ON SERVICE REQUEST ROUTINE
270 PRINT "POWER-ON SERVICE REQUEST
    RECEIVED"
275 PRINT
280 GO TO 220
289 REM: REQUEST TO SEND WAVEFORM
290 PRINT "READY TO SEND WAVEFORM"
295 PRINT
300 GOSUB 500
310 GO TO 220
320 REM: TALKER-ONLY SERVICE REQUEST
330 PRINT "TALKER-ONLY SERVICE REQUEST
    RECEIVED"
340 PRINT "UNABLE TO PROCESS REQUEST;
    ISSUING DEVICE CLEAR"
345 PRINT
350 GO TO 8
500 REM:################################
501 REM:
502 REM: SUBROUTINE TO ASSIGN TALKER AND
    PICK UP WAVEFORM
503 REM:
504 REM:################################
505 REM: SEND TALK ADDRESS TO DEVICE
506 REM: ADD 64 TO DEVICE ADDRESS (SET BIT 7
    TO TALK DEVICE)
510 WBYTE @A+64:
515 PAGE
519 REM: CALL ROUTINE TO DRAW GRATICULE
520 GOSUB 6000
550 REM: SET FIELD TO 0
560 F=0
564 REM: SET OUTPUT FLAG TO FALSE (0)
565 O=0
568 REM: SET COORDINATES OF FIRST PRINT
    FIELD OF SCREEN
570 X1=0
580 Y1=98.176
585 REM: DEFINE LIMITS OF SCREEN
586 VIEWPORT 0,130,0,100
587 WINDOW 0,130,0,100
590 REM: PICK UP A BYTE AND DECIDE WHETHER
    OR NOT TO PRINT IT
600 MOVE X1,Y1
605 RBYTE P
606 IF E=0 THEN 609
607 E=0
608 RETURN
609 REM: CHECK INPUT
610 IF P<0 THEN 605
620 IF P=10 THEN 605
630 REM: CONVERT BYTE TO A CHARACTER
635 P$=CHR(P)
638 REM: IF ;, THEN END OF WFM ID OR END OF A
    WAVEFORM
640 IF P$=";" THEN 830
645 REM: IF % , MEANS BEGINNING OF WAVEFORM
    POINT DATA
650 IF P$="%" THEN 860
655 REM: IF ANYTHING OTHER THAN COLON, GO
    ON TO SEE IF SHOULD PRINT IT
660 IF P$<>":" THEN 710
665 REM: HAVE ENCOUNTERED A COLON; END OF
    FIELD, INCREMENT FIELD COUNT
670 F=F+1
675 REM: SEE IF WE HAVE ENCOUNTERED TOO
    MANY FIELDS (SHOULD HAVE 16 MAX)
680 IF F<16 THEN 700
685 REM: RESET FIELD COUNT TO 1 IF HAVE
    EXCEEDED COUNT OF 16
690 F=1
695 REM: TURN OUTPUT FLAG ON (1)
700 O=1
705 REM: CHECK FIELD #'S TO SEE IF SHOULD
    PRINT THIS FIELD
710 IF F=1 THEN 760
720 IF F=4 THEN 760
730 IF F>5 AND F<9 THEN 760
740 IF F>9 AND F<12 THEN 760
745 REM: IF NOT A FIELD TO BE PRINTED, GO
    BACK AND GET NEXT BYTE
750 GO TO 605
760 REM: SEE IF WE SHOULD PRINT THIS PART OF
    THE FIELD
765 IF O=0 THEN 605
766 REM: OUTPUT FLAG SET TRUE
769 REM: DON'T WANT TO PRINT COLONS
770 IF P$=":" THEN 605
775 REM: PRINT CHARACTER AND SUPPRESS LINE
    FEED
780 PRINT P$;
785 IF P$<>"," THEN 605
786 REM: COMMA MEANS END OF FIELD. TURN
    OFF OUTPUT FLAG.
790 O=0
794 REM: CHECK TO SEE IF WE SHOULD GO TO
    NEXT LINE OF SCREEN
795 REM: IF HAVE JUST FINISHED FIELD 1 OR 7,
    NEXT LINE
796 IF F=1 THEN 800
797 IF F=7 THEN 800
798 GO TO 605
800 REM: CHANGE YCOORD TO POINT TO NEXT
    LINE
810 Y1=Y1-2.816
820 GO TO 600
825 REM: HAVE COME TO END OF ID OR END OF
    WAVEFORM. RESET FIELD, OUTPUT
830 F=0
835 O=0
838 REM: MOVE TO NEXT X PRINT FIELD
```

```
840  X1=X1+26.88
850  GO TO 580
860  REM: PICK UP WAVEFORM DATA. FIRST GET
     HIGH BYTE COUNT.
865  RBYTE B1
869  REM: GET LOW BYTE OF BYTE COUNT.
870  RBYTE B2
872  REM: INITIALIZE CHECKSUM TO SUM OF HIGH
     AND LOW BYTES
875  C=B1+B2
879  REM: CONVERT TWO BYTES OF COUNT TO
     ONE NUMBER
880  B=B1*256+B2-1
885  REM: REDIMENSION WAVEFORM DATA
     ARRAYS
886  DIM Y(B),X(B)
890  REM: READ IN WAVEFORM DATA POINTS
895  FOR I=1 TO B
900  RBYTE Y(I)
905  X(I)=I
908  REM: ADD BYTE TO CHECKSUM TOTAL
910  C=C+Y(I)
920  NEXT I
925  C=C-INT(C/256)*256
930  REM: READ IN CHECKSUM FROM GPIB NOW
935  RBYTE C1
936  REM: VERIFY CHECKSUM
940  IF C1+C<>256 THEN 990
950  REM: IF CHECKSUM WAS OKAY, GO AHEAD
     AND DRAW WAVEFORM
960  GOSUB 1350
965  REM: GO BACK NOW AND SEE IF MORE
     WAVEFORMS BEING SENT
970  GO TO 605
990  PRINT "CHECKSUM INCORRECT"
995  GO TO 8
999  REM:################################
1000 REM:################################
1001 REM:
1002 REM: INSTRUCTIONS FOR RUNNING THIS
     PROGRAM
1003 REM:
1004 REM:--------------------------
1005 PAGE
1006 PRI "THIS IS A PROGRAM TO DEMONSTRATE
     THE GPIB OPTION OF THE 468."
1007 PRINT
1008 PRINT "INSTRUCTIONS:"
1009 PRINT
1010 PRINT "USER KEYS USED IN THIS PROGRAM:"
1011 PRINT
1012 PRINT " #1: STARTS THIS PROGRAM
     RUNNING"
1013 PRINT
1014 PRINT " #2: ISSUES A DEVICE CLEAR TO THE
     468 AND RESTARTS PROGRAM "
1015 PRINT
1016 PRINT " #3: ASSIGNS INSTRUMENT AS
     TALKER (REQUESTS A WAVEFORM)"
1017 PRINT
1018 PRI "WHEN A WAVEFORM IS SENT THE
     FOLLOWING INFORMATION IS PRINTED"
1019 PRINT
1020 PRINT "VERSION NO.  CHANNEL, COUPLING"
1021 PRINT "                XMULTIPLIER,
                            TRIGGER POINT, X
                            UNITS"
1022 PRINT "                YMULTIPLIER,
                            GROUND POINT, Y
                            UNITS"
1023 PRINT
1024 PRINT "AFTER ALL WAVEFORMS HAVE BEEN
     DRAWN, YOU MUST PRESS <CR>"
1025 PRINT " TO PAGE THE SCREEN AND GO BACK
     TO WAITING FOR THE NEXT"
1026 PRINT " GPIB REQUEST."
1027 PRINT
1028 PRINT "MAKE SURE THE GPIB CABLE IS
     CONNECTED BEFORE SENDING A"
1029 PRINT " WAVEFORM OR REQUESTING ONE
     USING THE 4051."
1030 PRINT
1031 PRINT "THIS PROGRAM CAN BE
     AUTOLOADED IF IT IS FILE #1 ON TAPE."
1032 PRINT
1033 PRINT "PRESS <CR> TO CONTINUE"
1034 DIM I$(1)
1035 INPUT I$
1038 PAGE
1040 PRINT "ENTER GPIB ADDRESS OF 468
     (NUMBER BETWEEN 0 AND 30):";
1045 INPUT A
1050 IF A<0 THEN 1065
1055 IF A>30 THEN 1065
1060 RETURN
1065 PRINT "ADDRESS IS OUTSIDE 0-30 RANGE.
     RE-ENTER ADDRESS:";
1070 GO TO 1045
1350 REM:################################
1351 REM:
1352 REM:  ROUTINE TO PLOT WAVEFORM
1353 REM:
1354 REM:################################
1355 VIEWPORT 20,122.4,0,102.4
1358 REM: CHECK NUMBER OF WAVEFORM BYTES
1360 IF B=256 THEN 1375
1363 REM: IF 512 POINTS, SET PLOT FOR 512 PTS
1365 WINDOW 1,512,0,255
1370 GO TO 1380
1374 REM: IF 256 POINTS, ONLY SET FOR 256 PTS
1375 WINDOW 1,256,0,255
1378 REM: MOVE TO ORIGIN OF PLOT
1380 MOVE 0,0
1385 REM: DRAW WAVEFORM
1390 DRAW X,Y
1394 REM: RETURN CURSOR TO UPPER LEFT
     CORNER OF SCREEN
1395 HOME
```

```
1398  RETURN
2000  REM: THIS IS HERE IN CASE AN SRQ IS
      ASSERTED BEFORE THIS PROGRAM
2001  REM:  IS STARTED RUNNING.
2005  DIM Q(10)
2010  GOSUB 1000
2015  H=1
2020  T=1
2025  GOSUB 3000
2030  GO TO 110
3000  REM:################################
3001  REM:
3002  REM:  SRQ SERVICE ROUTINE
3003  REM:
3004  REM:################################
3005  REM: POLL DEVICES TO SEE WHICH
      INSTRUMENT REQUESTED SERVICE
3010  POLL D,S;A
3020  REM: ONLY 1 DEVICE ATTACHED, NO NEED
      TO CHECK DEVICE NUMBER (D)
3021  REM: ADJUST STATUS SO IT IS A NUMBER
      BETWEEN 1 AND 4
3022  REM: STATUSES: PON = 65, TRANSMIT
      REQUEST = 195, TON = 196
3025  IF S<64 THEN 3100
3030  S=S-64
3035  REM: NOW CHECK TO SEE IF IT IS TRANSMIT
      OR TON
3040  IF S<100 THEN 3060
3045  REM: IF TRANSMIT OR TON, MUST ADJUST
      AGAIN (SUBTRACT 128)
3050  S=S-128
3055  REM: NOW SET TASK TO BE PROCESSED (ADD
      TO TASK QUEUE)
3060  Q(T)=S
3065  T=T+1
3070  IF T<=10 THEN 3080
3075  T=1
3080  IF H=T THEN 3090
3085  RETURN
3090  REM: A QUEUE ERROR OCCURRED. QUEUE IS
      FULL.
3095  PRINT "QUEUE FULL – PROGRAM ABORTED"
3099  GO TO 8
3100  REM: ILLEGAL STATUS BYTE PICKED UP
3110  PRINT "ILLEGAL STATUS BYTE RECEIVED.
      STATUS = ";S
3115  PRINT "ISSUING DEVICE CLEAR"
3120  GO TO 8
4000  REM:################################
4001  REM:
4002  REM:  EOI ROUTINE
4003  REM:
4004  REM:################################
4005  REM: SET FLAG TO SAY EOI ENCOUNTERED
4006  REM: UNTALK AND UNLISTEN ALL DEVICES
4007  WBYTE @63,95:
4008  DIM C$(1)
4010  E=1
4015  REM: WAIT FOR OPERATOR TO ENTER A KEY
      BEFORE RETURNING
4020  INPUT C$
4025  PAGE
4030  RETURN
6000  REM:################################
6001  REM:
6002  REM:  ROUTINE TO DRAW GRATICULE FOR
      WAVEFORM DISPLAY
6003  REM:
6004  REM:################################
6005  REM: DRAW GRATICULE IN LOWER RIGHT
      PORTION OF SCREEN
6010  VIEWPORT 20,120,10,90
6015  REM: SET LIMITS OF GRAPHICS
6020  WINDOW 0,511,101.4,920.6
6025  REM: POSITION CURSOR TO BEGIN DRAWING
      GRATICULE
6030  MOVE 0,101.4
6040  DRAW 511,101.4
6050  DRAW 511,920.6
6060  DRAW 0,920.6
6070  DRAW 0,101.4
6080  AXIS 10.24,20.48,255,511
6090  FOR I=1 TO 9
6100  AXIS 0,0,I*51.2,I*102.4+101.4
6110  NEXT I
6120  VIEWPORT 30,130,0,100
6130  WINDOW 0,511,0,1023
6140  HOME
6150  RETURN
```

OPTION 05—TV SYNC SEPARATOR

The information and instructions presented here apply to the use of the 468 Option 05 instrument in TV applications. Refer to the appropriate sections of the Operator's or Service manuals for use and operation of the instrument for non-TV applications.

GENERAL INFORMATION

Option 05 includes a TV Sync Separator and provides the instrument with front-panel selection of additional trigger-signal processing to facilitate observation and measurement of composite video and related television sync recognition. Vertical (field rate) and horizontal (line rate) trigger signals are selected with the A TRIGGER COUPLING switch for A Sweep triggering. Horizontal (line rate) trigger signals for B Sweep triggering are selected with the B TRIGGER SOURCE switch.

For interlaced video signals, the TV FIELD trigger signals may start the A Sweep on either Field 1 or Field 2 ("even" or "odd" fields respectively in CCIR System B terminology). Trigger signal selection is accomplished with the A TRIGGER SLOPE switch.

When the A TRIGGER COUPLING switch is set to either TV FIELD or TV LINE (see Figure 6-6), the A TRIGGER SOURCE switch selects the source of the signals to be processed in the Sync Separator. This includes NORM (composite vertical signal), CH 1, CH 2, EXT, or EXT/10. (LINE source is not a usable function with TV FIELD or TV LINE coupling.)

With the A TRIGGER COUPLING switch set to either TV FIELD or TV LINE, the selected sync output from the Sync Separator is automatically applied to the A Sweep TRIGGER circuit for use as the triggering signal for the A Sweep. For the B Sweep, the horizontal-sync signal (line-rate sync) from the Sync Separator is fed only to the TV LINE position of the B TRIGGER SOURCE switch to be selected at the option of the user.

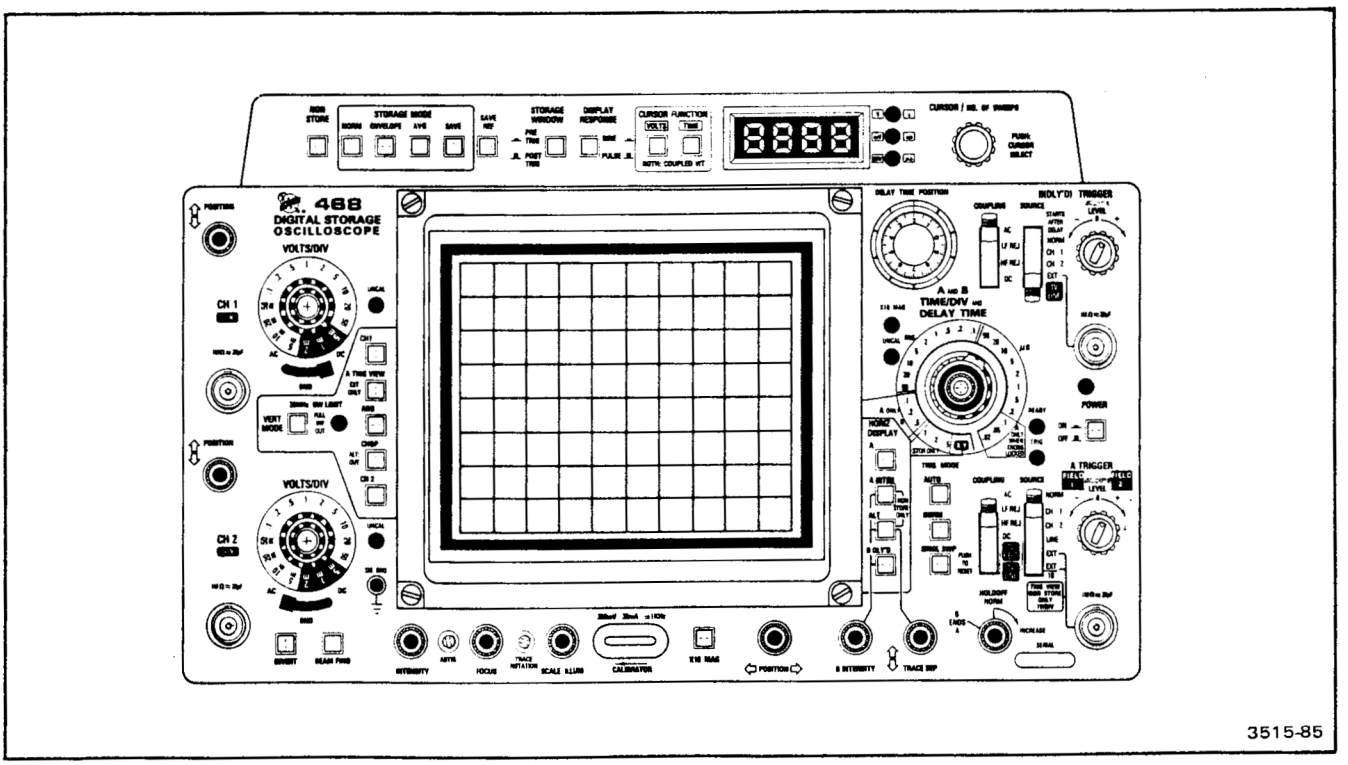


Figure 6-6. The 468 Oscilloscope with Option 05.

Option 05 circuitry requires sync-negative composite video for proper operation. This signal polarity is used with most standard broadcast systems employing 405 to 819 lines at 50- or 60-Hz field rates and with closed-circuit systems having up to 1201 lines at a 60-Hz field rate. Sync-positive video may be used as discussed later under "Operation of the Sync Separator."

To optimize video measurements, the vertical amplifier AC coupling input capacitors are increased from 0.019 μF to 0.2 μF. The larger physical size of these capacitors increases the input shunt capacitance to a normalized value of 24 pF.

SPECIFICATION

Electrical characteristics and performance requirements listed in the "Specification" part of this manual are applicable to the 468 Option 05 oscilloscope with the following exceptions or additions.

Vertical Input

Resistance	1 MΩ ±2%
Capacitance	24pf±10%
Time Constant	24μs±12%

AC Input Coupling

Low Frequency −3dB Point

Direct	1 Hz
Via 10X Passive Probe	0.1 Hz

Tilt (10-ms pulse)

Direct	2.5%
Via 10X Passive Probe	0.25%

Triggering

Sync Separation	Stable video rejection and sync separation from sync-negative composite video, 525- to 1201-line, 50- or 60-Hz field rate.

Sync-positive composite video can be separated by applying the input signal to the CH 2 input connector and using the CH 2 INVERT feature.

FIELD 1 and FIELD 2 trigger signals are selectable with the A TRIGGER SLOPE switch for interlaced field systems. A trigger signal is generated for every field in noninterlaced field systems.

Trigger Amplitude		Min	Max
Internal	Composite Video (nominal)[a]	1.5 div	15 div
	Composite Sync	0.5 div	20 div
External	Composite Video (nominal)	150 mV	1.5 V
	Composite Sync	50 mV	2.0 V
EXT/10	Composite Video (nominal)	1.5 V	15 V
	Composite Sync	500 mV	20 V

[a]Peak video is approximately 7/3 sync amplitude.

Furnished Accessories

The following accessories are provided with Option 05 instruments:

1 Graticule, NTSC (CCIR System M): −40 to +100 units, with 7.5-unit setup line; horizontal divisions along line zero (for part number see Option 05 "Accessories" in Volume II of this manual).

1 Graticule, CCIR (CCIR System B): zero to +100 units, 35-unit setup line; horizontal divisions along line 30 (for part number see Option 05 "Accessories" in Volume II of this manual).

OPERATING INSTRUCTIONS

Installation of the Video Graticule

To install a video graticule:

1. Loosen the four captive bezel securing screws about six turns and remove the bezel.

2. Remove the implosion shield from the two bosses on the bezel and install the desired graticule ensuring that the markings are on the surface away from the crt face. The graticule can be positioned horizontally a small amount to align the external graticule and mask with the internal crt graticule lines.

NOTE

The extended tab at the bottom of the video graticule mates with the slightly wider bottom margin of the graticule cover.

3. Position the bezel in place and secure it with the four captive screws.

Vertical Calibration for CCIR and NTSC Video Graticules

When the video graticule is installed, the 10 horizontal divisions along line 0 correspond to the internal graticule divisions, and the TIME/DIV calibration of the oscilloscope remains unchanged. However, the vertical divisions represent only proportions of the 100-unit (CCIR) or the 140-unit (NTSC) video waveform, and the vertical VOLTS/DIV calibration is inapplicable.

To calibrate for a standard 1-volt (nominal) video signal, apply the 300-mV CALIBRATOR square-wave signal to either the CH 1 or CH 2 vertical input and adjust the associated VOLTS/DIV and VOLTS/DIV VAR controls so that the displayed waveform occupies either 30 units on the CCIR graticule or 42 units on the NTSC graticule. This adjustment may be made with a well-focused, free-running display.

Operation of the Sync Separator

To trigger the 468 on a video signal, perform the following steps:

1. Set the A TRIGGER COUPLING switch to either TV FIELD or TV LINE.

2. Determine the polarity of the composite video or composite sync waveform applied to the 468. The Sync Separator requires normal (sync-negative) video sync at the negative peak. To obtain proper Sync Separator operation from inverted (sync-positive) video (sync at the positive peaks and peak video at the negative peaks), apply the signal to the CH 2 input connector, select CH 2 as the A TRIGGER SOURCE, and use the CH 2 INVERT feature to obtain the proper signal polarity.

NOTE

Composite Sync is the vertical and horizontal sync signals combined in a single waveform, but without video (picture) information. Composite Video is the picture waveform complete with vertical and horizontal blanking and sync components.

3. Use the A TRIGGER SLOPE switch to select the desired field for use as the trigger signal if the A TRIGGER SOURCE switch is set to the TV FIELD position.

For special considerations in dual-trace modes (ALT or CHOP), refer to "Vertical Operating Modes-Special Considerations" in this section. For internal triggering, the sync portion of the displayed waveform should be at least 0.5 cm high (7 units, or 0.35-division, on the CCIR graticule; on the NTSC graticule it should be 10 units, or about 0.5-division). For external triggering, the sync portion of the waveform should be at least 50 mV in amplitude (or 0.50 V with the SOURCE switch set to EXT/10). To avoid circuit overload and partial or complete loss of sync, do not exceed the specified maximum composite video amplitude (15 div for internal triggering; 1.5 V for external triggering).

Triggering the Sweep

The output of the Sync Separator is fed via the A TRIGGER COUPLING switch to the A Sweep Trigger circuit and via the B TRIGGER SOURCE switch to the B Sweep Trigger circuit. Triggering the A Sweep from the TV FIELD or TV LINE sync signal rerquires only the proper setting of the A TRIGGER LEVEL control.

When TV FIELD rate triggering is used, selecting either Field 1 or Field 2 sync is accomplished by setting the A TRIGGER SLOPE switch to the desired field. In the PAL four-field TV system, the FIELD 1 position selects either Field 1 or Field 3, and the FIELD 2 position selects either Field 2 or Field 4. Refer to "Identifying Fields, Frames, and Lines in 525/60 and 625/50 TV Systems" to identify the specific field being viewed.

To trigger the B Sweep from the line-rate trigger output of the Sync Separator, perform the following steps:

1. Set the A TRIGGER COUPLING switch to either TV FIELD or TV LINE and ensure that the A Sweep is running.

NOTE

The B Sweep cannot be operated independently of the A Sweep and cannot run more than once for each A Sweep cycle. For composite line displays, refer to "Special Measurements" in this section.

2. Set the B TRIGGER SOURCE switch to TV LINE.

3. Adjust the B TRIGGER LEVEL control for a stable, triggered sweep.

Vertical Operating Modes-Special Considerations

DUAL-TRACE MODES. For dual-trace operation, the Sync Separator input must be taken from CH 1, CH 2, or an external source. (When only one trace is displayed on the crt, the NORM position of the A TRIGGER SOURCE switch may be used.) The Sync Separator cannot correctly process switched (composite vertical deflection) waveforms present on the NORM trigger signal line in either the ALT or CHOP dual-trace vertical mode; it is therefore not possible to obtain stable simultaneous displays of two independent video signals that are not time related.

SINGLE-CHANNEL TRIGGERING. When triggering from Channel 1 or Channel 2, the waveform fed to the Sync Separator is the same (except for positioning) as that displayed on the crt when the channel is selected to display a signal. If the VOLTS/DIV VAR control is used to reduce displayed ampliltude, then the signal to the Sync Separator is also reduced. When the Channel 2 INVERT switch is pressed in, the CH 2 signal to the A TRIGGER SOURCE switch is also inverted. Since the Sync Separator requires sync-negative waveforms for proper operation, it will be necessary to observe correct signal polarity when selecting the A TRIGGER SOURCE signal.

It is not necessary to display the Channel 1 or Channel 2 signal to obtain CH 1 or CH 2 triggering. Whenever the AC-GND-DC input coupling switch for the channel is not set to GND, the input amplifier and trigger channel are active, regardless of the selection of VERT MODE push buttons.

ADD MODE. A single-channel trigger signal amplitude is not affected by contribution of the other channel to an ADD vertical mode display. When the ADD mode, with Channel 2 inverted, is used to compare two video waveforms by subtraction, the Channel 1 or Channel 2 signal to the Sync Separator will be adequate for stable triggering, providing the individual channel signal meets the triggering requirements (including correct polarity).

When the ADD mode is used to display the full signal from both sides of a balanced line, it may be necessary to use the NORM (composite vertical signal) A TRIGGER SOURCE switch position (if neither side of the line has sufficient amplitude for suitable triggering or if common-mode signals interfere with stable sync-separation and triggering).

Typical Operation

NOTE

The following procedures for selecting individual lines, fields, or frames are applicable to the operation of the 468 as a conventional (nonstorage mode) oscilloscope only. Due to the signal processing time required by the digital microprocessor when storing a waveform, the holdoff time between sweeps is increased in all storage modes. Therefore, the A TRIGGER HOLDOFF control has reduced action over the holdoff timing, except near its maximum clockwise rotation.

In a typical operating mode for the Option 05 instrument, the A Sweep establishes the basic frame and field presentation, and the B Sweep allows detailed observation and measurement of various portions of the video waveform.

For 50- and 60-Hz field rates, the 2 ms/division setting of the A TIME/DIV switch is usually selected. For some PAL system observations, a setting of 5 ms/division (approximately a 2 1/2-field display), with the A TRIGGER HOLDOFF control set to approximately the four-o'clock position (additional one-field holdoff), may be desirable to maintain a stable display relationship to the four-field PAL burst-blanking sequence.

All detailed measurements are then made using the B Sweep, (HORIZ DISPLAY switches set either to B DLY'D or ALT) with the B TRIGGER SOURCE switch set either to STARTS AFTER DELAY (continuously variable B Sweep start point) or to TV LINE (B Sweep starts after the next horizontal sync pulse following the delay interval set by the DELAY TIME POSITION control and the A TIME/DIV switch setting).

Because the leading edge of the sync pulse will not be displayed, the typical B TIME/DIV switch setting for width measurement (front porch, back porch and horizontal-blanking intervals, horizontal sync, serration, and equalizing pulses) is 10 μs/division. This setting will allow display of two consecutive pulses. Use the X10 MAG switch to display the second pulse at 1 μs/division sweep rate.

For rise- and fall-time measurements on blanking and sync waveforms, trigger the A or B Sweep directly from the displayed waveform (avoiding the processing delay of the Sync Separator). This permits viewing the trigger edge at sweep rates from 0.5 μs/division to 0.02 μs/division.

Selecting an Individual Line

NOTE

For field and line identification systems, refer to "Identifying Fields, Frames, and Lines in 525/60 and 625/50 TV Systems" at the end of these Operating Instructions.

ONE-FRAME CYCLE. To display an entire vertical blanking interval for locating a specific line (e.g., one of the lines containing a specific VIT waveform), set the A TIME/DIV switch to 2 ms/division and the B TIME/DIV switch (pull to unlock from A) to 10 μs/division. Ensure that the A TRIGGER HOLDOFF control is set to NORM (fully ccw) and the A TRIGGER COUPLING switch is set to TV FIELD. Then, select the desired field (FIELD 1 or FIELD 2) with the A TRIGGER SLOPE switch.

Press in the A INTEN push button and use the DELAY TIME POSITION control to position the intensified zone (B Sweep) on the desired line. Pressing the B DLY'D button will then display the desired line on the B trace. Set HORIZ DISPLAY to ALT to view the A INTEN trace and B DLY'D trace simultaneously.

TWO-FRAME CYCLE. If PAL burst blanking is to be checked, set the A Sweep time for a 3 1/2-field cycle (5 ms/division, with the A TRIGGER HOLDOFF control set to about the four o'clock position). Then, use the B Sweep (ALT HORIZ DISPLAY is recommended) to identify fields and lines. At 5 ms/division, only slightly more than two fields will be displayed, while the trigger holdoff interval covers a full field. Putting a specific field on screen in a particular location will typically require several operations of the A TRIGGER SLOPE switch (switching back and forth between FIELD 1 and FIELD 2) to select the proper frame cycle.

Special Measurements

OVERSCANNED DISPLAYS. For various video measurements it may be desirable to expand the video waveform vertically beyond the limits of the screen. Under these circumstances either the trigger amplifiers or Sync Separator may be overloaded, blocking out some sync pulses in the vicinity of strong video transitions, or losing sync pulses altogether. To avoid overload problems, use either an external sync signal or the other vertical channel to supply a constant-amplitude signal to the Sync Separator while overscanned observations are being made. Note, however, that transient-response aberrations in the main vertical amplifier will be increased when the signal is driven offscreen, and the aberrations will become relatively serious if the amplifier is driven to saturation and cutoff.

HORIZONTAL-SYNC PULSE MEASUREMENTS. Measurements of the rise and fall times and the width of horizontal sync pulses typically do not require use of the Sync Separator, except when only certain lines or groups of lines appear abnormal. A bright display of all horizontal sync pulses is obtained when the A Sweep is triggered on the appropriate slope using LF REJ coupling and an A Sweep TIME/DIV switch setting of 5 μs or less. Triggering stability may be upset by sharp luminance transitions at the right side of the picture, but a careful setting of the LEVEL control will typically permit accurate measurements. Use of the 5 μs/division basic rate locks out most of the video (for 525- or 625-line systems) from triggering the A Sweep. When faster sweeps are needed, the A TRIGGER HOLDOFF control may be adjusted to block out video information.

RF INTERFERENCE. Operation in the vicinity of some FM and TV transmitters may cause objectionable amounts of rf signal energy in the display, even when coaxial cables are used to make signal connections to the instrument. The front-panel 20 MHz BW LIMIT switch will usually eliminate such interference from the display, but it will not affect the signal applied to the Sync Separator. Where rf energy interferes with Sync Separator operation, external filters will be required. Use of probes designed for 10- to 30-MHz bandwidth oscilloscopes will provide 6- to 10-dB attenuation in the 50- to 100-MHz range and may be beneficial in reducing rf interference.

Identifying Fields, Frames, and Lines in 525/60 and 625/50 TV Systems

NTSC (CCIR SYSTEM M). Field 1 is defined as the field whose first equalizing pulse is one full H interval (63.5 μs) from the preceding horizontal-sync pulse. The Field 1 picture starts with a full line of video, and lines are numbered 1 through 263, starting with the leading edge of the first equalizing pulse. The first regular horizontal-sync pulse after the second equalizing interval is the start of line 10.

Field 2 starts with an equalizing pulse a half-line interval from the preceding horizontal-sync pulse. The Field 2 picture starts with a half line of video, and lines are numbered 1 through 262, starting with the leading edge of the second equalizing pulse. After the second equalizing interval, the first full line is line 9.

In the M/NTSC four-field color system, Fields 3 and 4 are defined identically to Fields 1 and 2 respectively, except for the phase of the color reference subcarrier. In Fields 1 and 4, positive-going zero crossovers of the reference subcarrier nominally coincide with the leading edge of even-numbered horizontal sync pulses. In Fields 2 and 3, negative-going zero crossovers of the reference subcarrier nominally coincide with the leading edge of even-numbered horizontal sync pulses.

CCIR SYSTEM B AND SIMILAR 625/50 SYSTEMS. Except for PAL systems, identification of parts of the picture in most 625-line, 50-Hz field-rate systems relies primarily on continuous line numbering rather than on field-and-line identification.

The CCIR frame starts with the first (wide) vertical-sync pulse following a field which ends with one-half line of video. The first line after the second equalizing interval is line 6; the first picture line is line 23 (one-half line of video). The first field of the frame contains lines 1 through the first half of line 313; the picture ends with a full line of video (line 310).

The second field of the frame commences with the leading edge of the first (wide) vertical sync pulse (in the middle of line 313) and runs through line 625 (end of the equalizing interval). The first full line after the equalizing interval is line 318; the picture starts on line 336 (full line of video).

The first field is referred to as "odd," and the second field is referred to as "even." Note that while the identification systems for System M and System B are reversed, the correct field sync (Field 1 or Field 2) (as indicated by the A TRIGGER SLOPE switch setting) is selected.

In the four-field PAL sequence with Bruch Sequence Color-Burst blanking, the fields are identified as follows:

Field 1: Field that follows a field ending in one-half line of video, when the preceding field has color burst on the last full line. Field 1 lines are 1 through 312 and half of line 313. Color burst starts on line 7 of Field 1; one-half line of video appears on line 23.

Field 2: Field that follows a field ending in a full line of video which does not carry color burst. Field 2 lines are the last half of line 313 through line 625. Color burst starts on line 319 (one line without burst following the last equalizing pulse); a full line of video appears on line 336.

Field 3: Field that follows a field ending in a half line of video when preceding field has no color burst on the last full line. Field 3 lines are 1 through the first half of line 313. Burst starts on line 6 (immediately following the last equlizing pulse); one-half line of video appears on line 23.

Field 4: Field that follows a field ending in a full line of video carrying color burst. Field 4 lines are the second half of line 313 through line 625. Color burst for Field 4 starts on line 320 (two full lines without burst follow the last equalizing pulse); video starts with a full line on line 336.

NOTE

The FIELD 1 position of the A TRIGGER SLOPE switch selects NTSC or PAL Field 1 or 3 to start the display; the FIELD 2 position selects NTSC or PAL Field 2 or 4.

THEORY OF OPERATION

Introduction

This text describes circuitry unique to Option 05. Refer to the Theory of Operation section of this manual for information concerning those portions of the oscilloscope circuitry that are unchanged by Option 05. Figure 6-7 shows in a simplified block diagram, those circuits added or changed by Option 05. The following discussion is limited to a description of those stages. Schematic diagrams 24 and 25, pertaining to circuitry added to or changed from the standard instrument, are located in Service Volume II.

Switching

The added TV FIELD and TV LINE positions of the A TRIGGER COUPLING switch open the usual signal path to the A Trigger circuitry and couple the appropriate output of the Sync Separator stage to the A Trigger Generator circuitry.

The Option 05 TV LINE position on the B (DLY'D) TRIGGER SOURCE switch couples the line-rate trigger signal from the Sync Separator output to the B Trigger Generator circuitry.

Trigger Pickoff

A Trigger Pickoff stage composed of source follower Q520 and emitter follower Q521 provides isolation and impedance matching to Trigger Amplifier U315 and minimizes loading of the input signal. Gain of the Trigger Pickoff stage is slightly less than unity. The video trigger signal (internal or external) from the A TRIGGER SOURCE switch is coupled to the input of Q520, while the output of the Trigger Pickoff stage (emitter follower Q521) is fed through P520 and P2810 to the Trigger Amplifier. Diode CR519 prevents high amplitude negative-going signals from damaging the input of Q520. High-amplitude positive-going signals are limited by the gate-to-drain current that flows when the source-gate junction of Q520 become forward biased.

Trigger Amplifier

Trigger Amplifier U315 and associated components provide adequate drive for the Sync-Separator. Output from the Trigger Amplifier stage is fed to Q325, the Sync Separator circuitry input transistor. Feedback resistor R310 (from

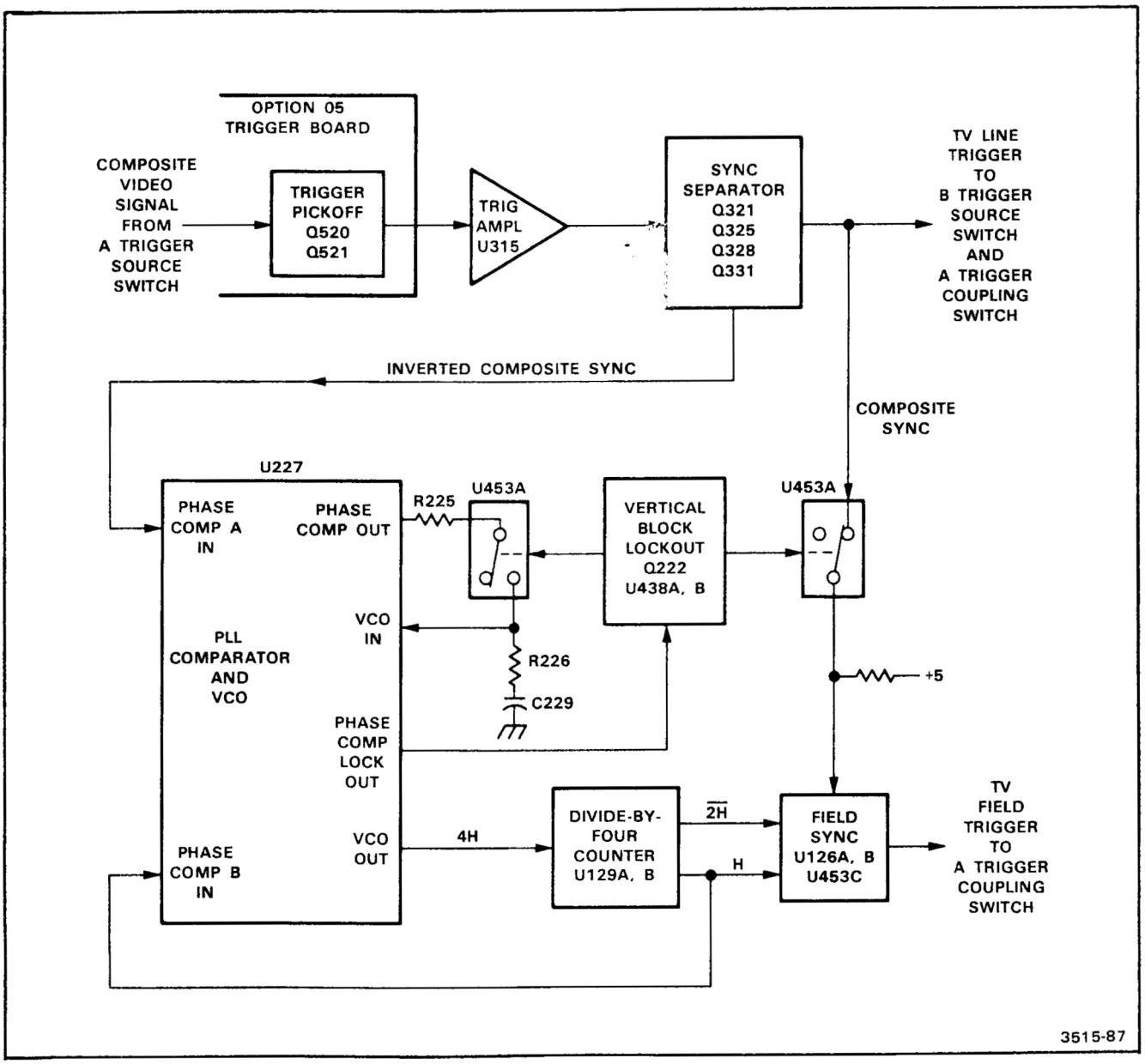


Figure 6-7. Option 05, TV Sync Separator, simplified block diagram.

U315 pin 8 to U315 pin 3) controls the gain of U315 for low-amplitude signals, while R311, CR310, and CR311 control the gain for higher amplitude signals.

Sync Separator

The Sync Separator circuit (composed of Q321, Q325, Q328, Q331, and associated components) is arranged as a wide-band, high-gain, self-biasing clipping amplifier that performs several functions:

1. Positive video information is removed (stripped) from incoming sync-negative, composite video signals.

2. Negative sync tips are clipped to eliminate possible noise or, in some systems, subsidiary signals.

3. The "middle" portion of the resulting composite sync is amplified for use as the A and B Sweep (TV LINE) sync. The amplified signal is further processed by the Field Selection circuitry to obtain the TV Field trigger signal to apply to the A Sweep trigger circuitry.

SYNC STRIPPER. With no signal applied (quiescent state), Q325 and Q321 are biased to produce approximately +5 V on the Q321 collector, and Q331 is biased into saturation. The collector of Q331 will be at approximately 0 V.

When the composite video signal from U315 is applied to the base of Q325 (via R324 and C323) the negative-sync portion increases the forward bias of Q325 thereby lowering the Q325 emitter voltage. This negative-going emitter voltage,applied directly to the base of Q321, reduces the forward bias on Q321 and allows the Q321 collector voltage level to rise. Thus, the negative-sync portion of the composite video signal is amplified and inverted. However, transistor Q321 remains saturated during the positive voltage changes at the Q321 collector, so the negative sync tips are not passed on to the composite sync bus.

The amount of dc feedback applied to the base of Q325 is determined by the sync-tip amplitude, Current through CR333 rapidly charges C329, and the forward bias on Q328 increases. The increased current flow through Q328 applies a negative dc feedback to Q325 through the parallel combination of R327, C321, and R321, thereby limiting the positive output level of Q321.

The negative transition of the sync pulse output from Q321 is applied to C329 through R331 and R332, thus producing a relatively long time-constant-discharge path. Between sync pulses, the charge on C329 reduces only a small amount, and the dc feedback remains at the level determined by the sync tip amplitude. If the signal amplitude were to reduce, the sync tip amplitude would also be less. The negative feedback generated would be reduced, increasing the gain and thus adjusting to lower input signal level.

The gain for positive-going portions of the input signal is over 100 (limited primarily by the finite gain of Q321). The positive video portions of the input signal saturate Q321 whenever the peak-to-peak input amplitude exceeds about 60 mV. Any signal applied to Q321 while it is saturated will not be amplified. This results in the positive portion of the composite-video signal being clipped. However, the negative-sync portion of the input signal is amplified to nearly 6 V peak-to-peak and inverted at the output of Q321. This inverted composite sync signal is fed (via R409 and R408) to the Phase Comparator A input of U227, to control the phase-locked-loop oscillator, and applied via R326 to the base of Sync Clipper Q331.

SYNC CLIPPER. Transistor Q331 passes a signal only during a narrow input signal level range, During the quiescent state, and also whenever the sync tips drive the collector of Q321 positive, Q331 is saturated. On the negative transition of a sync pulse, Q331 comes out of saturation as the Q321 output signal level drops through +4 V, but it becomes cutoff as the signal level continues to drop through +3 V. Sync Clipper Q331 then amplifies only the middle portion of the sync signal, clipping off the sync tips and any excursions of color subcarrier peaks which may have extended into the sync area. The amplified composite sync is fed to a voltage divider composed of R101 and R102 to reduce the signal amplitude to the correct level for application via P2834 to the A and B Trigger Generator circuits. This composite-sync signal is also applied via U453A, a MOSFET bilateral switch, to the Field Selection circuitry.

Field Selection

The Field Selection circuitry consists of the following:

1. A phase-locked-loop oscillator, operating at four times the television horizontal line rate (4H).

2. A sync block lockout circuit that opens the error-correction input to the phase-locked-loop oscillator during the vertical sync interval to prevent equalizing pulses, serrations, or (in some systems) the absence of horizontal sync pulses from affecting the oscillator frequency.

3. Sampling circuits that, after each horizontal sync pulse, interrogate the state of the composite sync bus at the one-quarter and three-quarter points in a line interval and then generate the FIELD output sync signal.

PHASE-LOCKED LOOP. The phase-locked loop is composed of U227, a CMOS phase comparator and voltage-controlled oscillator (VCO), and U129A and B, a divide-by-four counter. The VCO operates at four times the horizontal frequency, while the output of U129A and B is one-fourth the VCO frequency (the horizontal frequency). The minimum

VCO frequency is set by C228 to less than 40 kHz, or four times the line rate of a 405-line, 50-Hz video system. Range-setting resistor R224 extends the upper frequency range to above 144 kHz (four times the line rate of a 1201-line, 60-Hz system).

Inverted composite sync is applied to U227 at pin 14 (the Phase Comparator A input). The VCO output is divided by four by U129A and B, and the Q output signal of U129A at pin 1 is applied to the Phase Comparator B input of U227 at pin 3. Positive-going edges of the two signals are compared to produce the required correction voltage to the VCO. If the positive-going leading edge of the incoming inverted horizontal sync pulse occurs before the positive-going edge of the U129A output, the comparator produces a +5 V pulse at pin 13. If the U129A output comparison point occurs prior to the inverted composite sync positive-going leading edge, a 0-V pulse is produced by the comparator.

The duration of any generated correction pulse is the time difference between the sync signal and counter output edges. The greater the phase difference, the wider the correction pulse. Between correction pulses, the phase-comparator output at pin 13 is an open circuit and has no effect on the oscillator frequency.

Correction signals are applied to the VCO input of U227 at pin 9 via a low-pass filter composed of R225, R226, C229, C425, and U453B (one-third of a CMOS triple bilateral switch). The low-pass filter circuit compensates the phase-locked loop and attenuates the fast switching transients of the comparator ouput. When pin 10 of U453B is HI, VCO IN is connected to COMP OUT through the low-pass filter. When pin 10 of U453B is LO, COMP OUT is disconnected from VCO IN, and only the voltage level stored on C229 is applied to VCO IN. This voltage level remains constant between correction pulses to maintain the oscillator frequency. Resistor R425 supplies a bias current to the filter network to cause the signal at VCO IN to always slightly lead the incoming sync pulses at COMP IN (pin 14). This results in improved VCO output jitter characteristics.

SYNC BLOCK LOCKOUT. The phase comparator produces a "lock" signal at U227 pin 1. As long as the input comparison edges are exactly coincident, the lock signal remains HI, but it goes LO for the duration of any corrction pulses. The lock signal is applied to the Vertical-Block-Lockout circuit for use in recognizing changes in the vertical sync block that would cause the VCO to be forced off frequency. During such periods, the correction loop is opened to allow the VCO to maintain a constant frequency without correction.

The negative-going out-of-lock pulse from the phase comparator is applied via R222 and R221 to the base of Q222. Capacitor C213, connected between the junction of the two resistors and ground, must discharge before Q222 can be biased off. The time constant of R221 and C213 is long enough that the duration of the out-of-lock pulse must exceed about 10 μs before the collector voltage of Q222 goes high enough to cross the threshold level of U438A. Errors of such a duration are introduced by either the 2H equalizing pulses and sync pulse serrations in the vertical sync block (VCO attempts to increase frequency) or by the absence of H pulses in the sync bolck, as is common in 405/50 and many closed-circuit TV systems (VCO attempts to decrease frequency).

When the error exceeds 10 μs in duration, the voltage level at the collector of Q222 crosses the threshold level of U438A and the one-shot multivibrator is triggered. The resulting signal from U438A is an approximately 1 ms, negative-going pulse from the $\overline{Q}$ output (pin 7) that opens bilateral switch U453B. The phase comparator output is opened to prevent correction pulses from being applied to the VCO input. The VCO maintains its previous frequency, as determined by the charge present on C229, for the duration of the 1-ms pulse. Current through R124 holds Q222 on during this time to inhibit the output of U227 pin 1 from resetting U438A.

A second one-shot circuit composed of U438B is triggered by the rising edge of the end of the 1-ms negative pulse from U438A pin 6 (Q output). An approximately 10-ms positive inhibit pulse from U438B pin 10 is fed back to the base of Q222. This inhibit pulse prevents any further lockouts for approximately 10 ms, thus ensuring that in the event of severe frequency or phase discrepancies, the phase comparator will actively compare the loop signal with the incoming sync signal for at least 90% of the time. The VCO circuit is then able to ignore 1-ms-long blocks that occur at intervals no closer than 10 ms, but the 90% active cycle still provides a quick lockup when a new video signal is applied.

A negative pulse from U438B pin 9 opens bilateral switch U453A for the duration of the 10 ms inhibit pulse. This prevents the incoming composite sync from being clocked through U126B in the Field Selection circuit while U227 is relocking to the signal.

FIELD SYNC. In all standard interlaced television signals, the vertical sync pulse ahead of a field which starts with a full line of video will occur halfway between two horizontal sync pulses (Field 1 in NTSC terminology, Even field in CCIR system B). A field starting with a half line of video will be preceded by a vertical sync pulse which starts at the end of a line.

The Field Sync circuit uses the $\overline{2H}$ and H rate outputs of divide-by-four counter U129A and B to sample the state of the composite sync bus at two points in the line interval between H pulses. This sampling determines when a vertical sync block has started. One sample point is at about the one-quarter point in the H interval, and the other is at about the three-quarter point.

A positive-going edge used to clock U126B at both the one-quarter and three-quarter points is provided from the U129B $\overline{Q}$ output (pin 12). The composite sync level applied to U126B at pin 9 (the D input of the flip-flop) is sampled and latched into U126B on each rising clock edge. If the level is HI when it is sampled (no vertical sync pulse present), the U126B $\overline{Q}$ output (pin 12) will go LO and remain there. If the sync level is LO when sampled (signifying a vertical sync pulse), the $\overline{Q}$ output of U126B will go from LO to HI to clock U126A at pin 3 (refer to the timing diagram, Figure 6-8). When the vertical sync pulse has ended, the $\overline{Q}$ output of U126B clocks back to LO.

The Q output of U129A is applied to the U126A D input. This output level is HI for the first half of each H interval (horizontal line) and LO for the second half. When the rising edge clock transistion occurs at U126A (pin 3), the state of the D input (pin 5) will be transferred to the Q output (pin 1), and the complement will appear on the $\overline{Q}$ output (pin 2).

Thus, each occurrence of a vertical sync pulse is detected by U126B, and U126A determines whether it occurred in the first half or second half of a line. If the vertical sync pulse is present in the first half of the line, the Q output of U126A at pin 1 will go HI; and if it occurs in the second half, the Q output will go LO.

Therefore, in an interlaced system, the outputs of U126A will toggle at the full frame rate, with transitions occurring just after the start of each vertical sync pulse. The Q output will be HI during Field 1 and LO during Field 2.

Bilateral switch U453C is used to automatically select either the "Field 1/Field 2" trigger signal from the $\overline{Q}$ output of U126A (for interlaced video) or the "Field" trigger signal from the $\overline{Q}$ output of U126B (for noninterlaced systems.) In an interlaced video system, U126A toggles at the frame rate. The circuit composed of C404, CR404, R113, CR112, C405, and R110 rectifies the ac-coupled U126A Q output to produce a HI level at pin 9 of U453C. This causes the $\overline{Q}$ output of U126A to be passed to R404. In a noninterlaced system, U126A does not toggle. The level at pin 9 of U453C is LO, and the $\overline{Q}$ output of U126B is passed to R404 to produce a trigger signal on each field. Resistors R404, R405, and R406 attenuate and level shift the output of U453C to produce levels suitable for the A Sweep Trigger Generator.

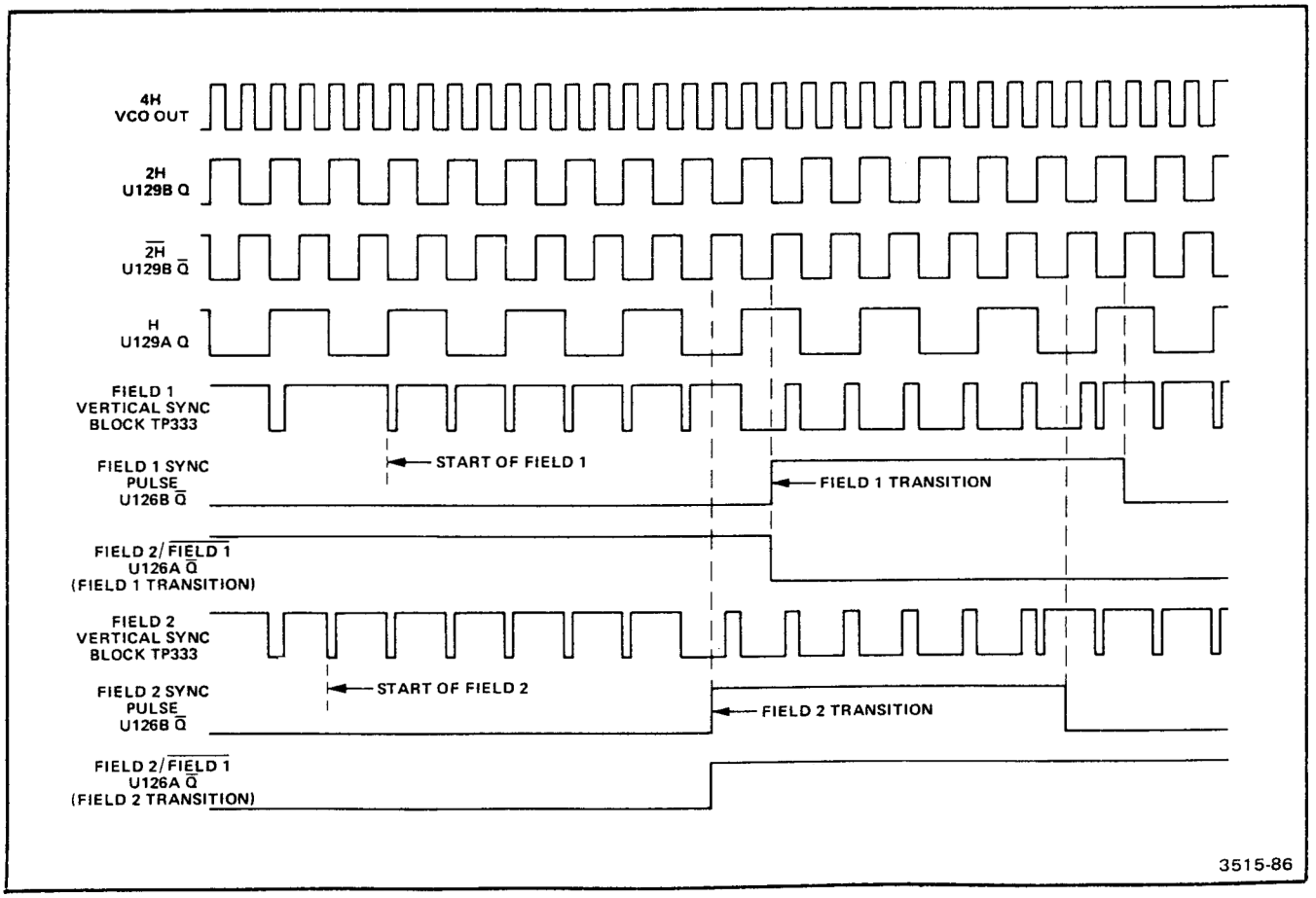


Figure 6-8. Field selection timing diagram.

OPTION 11—ANALOG X-Y OUTPUT

INTRODUCTION AND SPECIFICATION

This Option enables the 468 to convert the digital data stored in the storage display memory into analog X and Y outputs for driving an external X-Y Plotter. The analog outputs will conform to most currently produced X-Y Plotters. Electrical specifications for Option 11 are given in Table 6-5. All other specifications given in Volume I of this manual remain unchanged.

Table 6-5

Electrical Characteristics

Characteristics	Performance Requirement	Supplemental Information
X and Y Output		
Sensitivity	200 mV per division.	Within ±3%, measured with respect to on-screen cursors.
Range	0 to 2.048 V.	0 to 10.24 divisions.
Resolution		
Y-Axis		8 bit.
X-Axis		8 or 9 bit.
PEN LIFT		Relay contact closure to ground, polarity switchable. Maximum relay current is 200 mA, fused at 250 mA. Maximum applied voltage is 30 V peak. A 10-kilohm pull-up resistor to the +5-V supply is switchable to provide TTL pen-lift levels.
PLOT SPEED		Switch selectable between fast and slow.
Switch Open	Fast plot.	40 ms ±10% per data point.
Switch Closed	Slow plot.	320 ms ±10% per data point.

OPERATING INSTRUCTIONS

SETTING UP THE OPTION

Operation of the Analog X-Y Output Option is largely automatic. Only a few switch settings are required before pressing the PLOT switch to start the operation. Refer to the Operators information of the X-Y Plotter in use for set-up and operation procedures required for using it. Information required for the correct setup of the Analog X-Y Output Option switches on the 468 rear panel should also be obtained from the instructions for the X-Y Plotter in use.

The required switch settings of the Analog X-Y Output switches shown in Figure 6-9 are as follows:

1. The PLOT SPEED switch must be set to match the X-Y Plotter characteristics. Choices of plot speed are 40 ms per data point (fast plot) and 320 ms per data point (slow plot).

2. The PEN POLARITY switch must be set to match the X-Y Plotter pen-lift signal requirements. When the switch is OPEN, the pen control relay will be open when the plotting pen should be down on the paper. When the switch is CLOSED, the pen control relay will be closed when the plotting pen should be down on the paper.

3. The PEN PULL-UP switch must be set to provide the proper level pen-lift signal for the plotter pen. The pen-lift voltage may be set either for no pull-up to the +5-V supply or for pull-up through a 10-kΩ resistor. The pen-lift voltage is pulled up when the switch is CLOSED and not pulled up when the switch is OPEN.

4. The RESET switch must be set to the OPEN (off) position for normal operation.

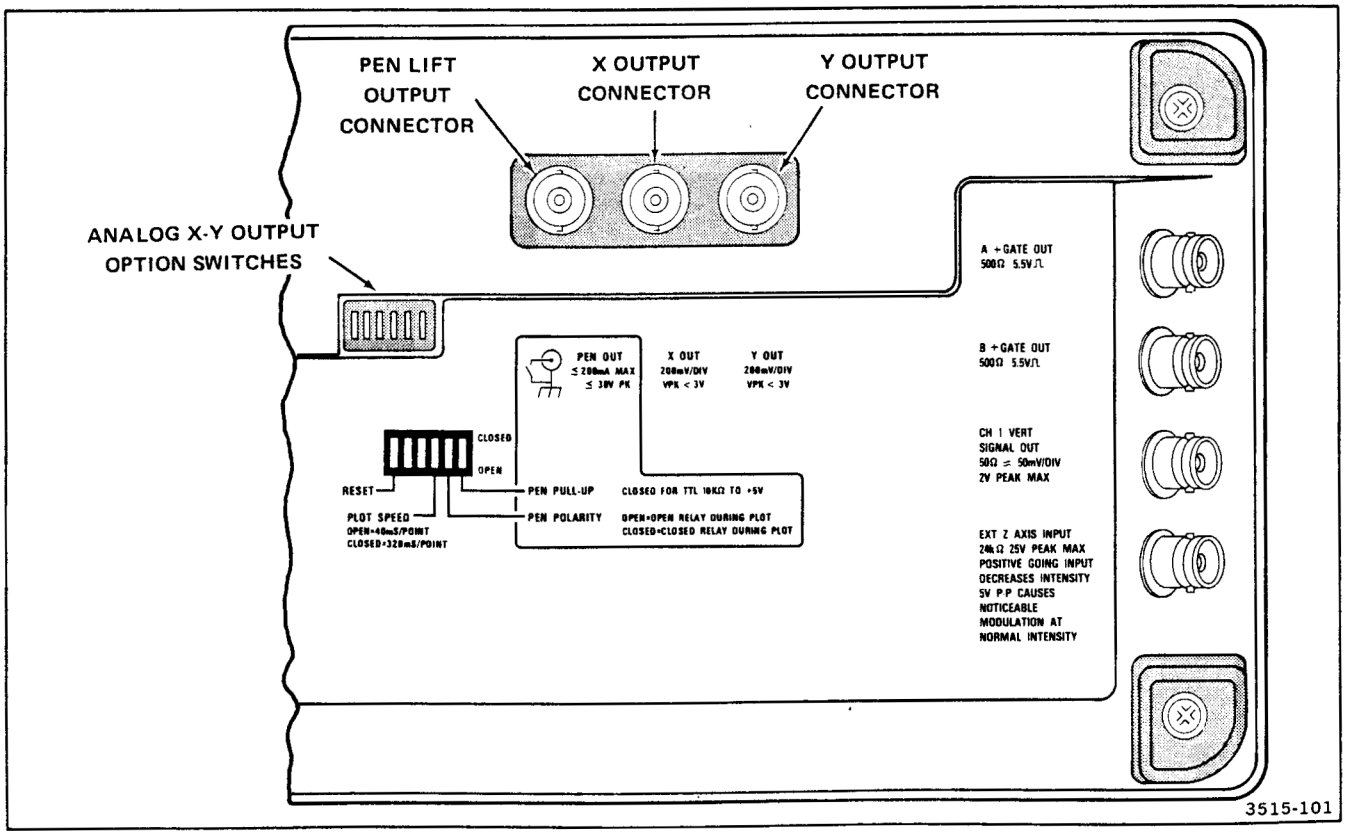


Figure 6-9. Location of Analog X-Y Output Option switches and output connectors.

NOTE

The RESET switch is maintenance only. If the switch is inadvertently closed while a waveform plot is occurring, the switch must remain closed until the remaining waveform data is dumped. Returning the switch to the OPEN position before the waveform data has finished dumping will cause a state control malfunction. If this should occur, cycle the POWER switch OFF; then ON again to clear the malfunction.

In addition to the external switch settings required, section 8 of the internal OPTIONS/SERVICE switch must be in the CLOSED position when power is applied to the instrument for the Analog X-Y Output Option to be enabled. If the PLOT switch is inoperable, refer the instrument to a qualified service person to check the switch position. Refer to Figure 5-6 in the "Maintenance" section of Volume I for the location of the OPTIONS/SERVICE switch.

Refer to Figure 6-9 for the location of the Analog X-Y Output switches and the PEN OUT, X OUT, and Y OUT BNC connectors.

After the Analog X-Y Output switches are set for the X-Y Plotter to be used, no further setting of the switches is required. Connect the X OUT, Y OUT, and PEN OUT connectors to the X-Y Plotter, and set up the X-Y Plotter by following the operating instructions of the plotter in use.

USING THE OPTION

Acquire a storage mode waveform to be plotted as per the operating instructions given both in this manual and in the 468 Operators manual, then press in the PLOT push button. The 468 will go into the SAVE Storage Mode, and the stored waveform will be plotted. If you wish to do more than one plot of the same waveform, press in the SAVE Storage Mode push button either prior to pressing in the PLOT push button or during the time the waveform is being plotted. The waveform will be saved for as long as the SAVE Storage Mode remains selected. At the completion of the plot, the 468 will return to the operating mode selected by the front-panel controls. If SAVE Storage Mode has not been selected, new waveform data will be acquired.

Only the actual waveform data points are output to the X OUT and Y OUT connectors. No scale factors or interpolated data are sent. When the PLOT push button is pressed, the plotter pen will move to the first data point after about two seconds. The pen will stay at the first data point for five seconds. After 2.5 seconds, the plotter pen will be lowered to the plot paper. The remaining data points will be plotted at the rate selected by the PLOT SPEED switch. On the last data point plotted, the pen again remains for five seconds, with the pen lifting at about 2.5 seconds into the delay. The five-second delay at the first and last data points allows the operator time to manually control the pen position on some X-Y Plotters. For multiple waveforms to be plotted, the sequence just described is repeated for each waveform, including a two-second wait in the home position before going to the first data point of the next waveform to be plotted. When all the waveform data has been sent, the 468 returns to front-panel control.

THEORY OF OPERATION

INTRODUCTION

The following text begins with a general description of the Analog X-Y Output Option circuitry and its relationship to the 468 Digital Oscilloscope. It then continues with a detailed description of the Option circuitry. Refer to Figure 6-10 for a block diagram and to Diagram 26 in the foldout section of Volume II of this manual for a schematic representation of the circuitry.

GENERAL DESCRIPTION

The Analog X-Y Output Option provides the 468 user with a hard-copy output that is compatible with a large number of currently available X-Y Plotters. The Option 11 circuit board is designed to physically replace the GPIB Option circuit board, and it uses the GPIB Option firmware for data communications between the 468 and the Analog X-Y Output Option circuitry.

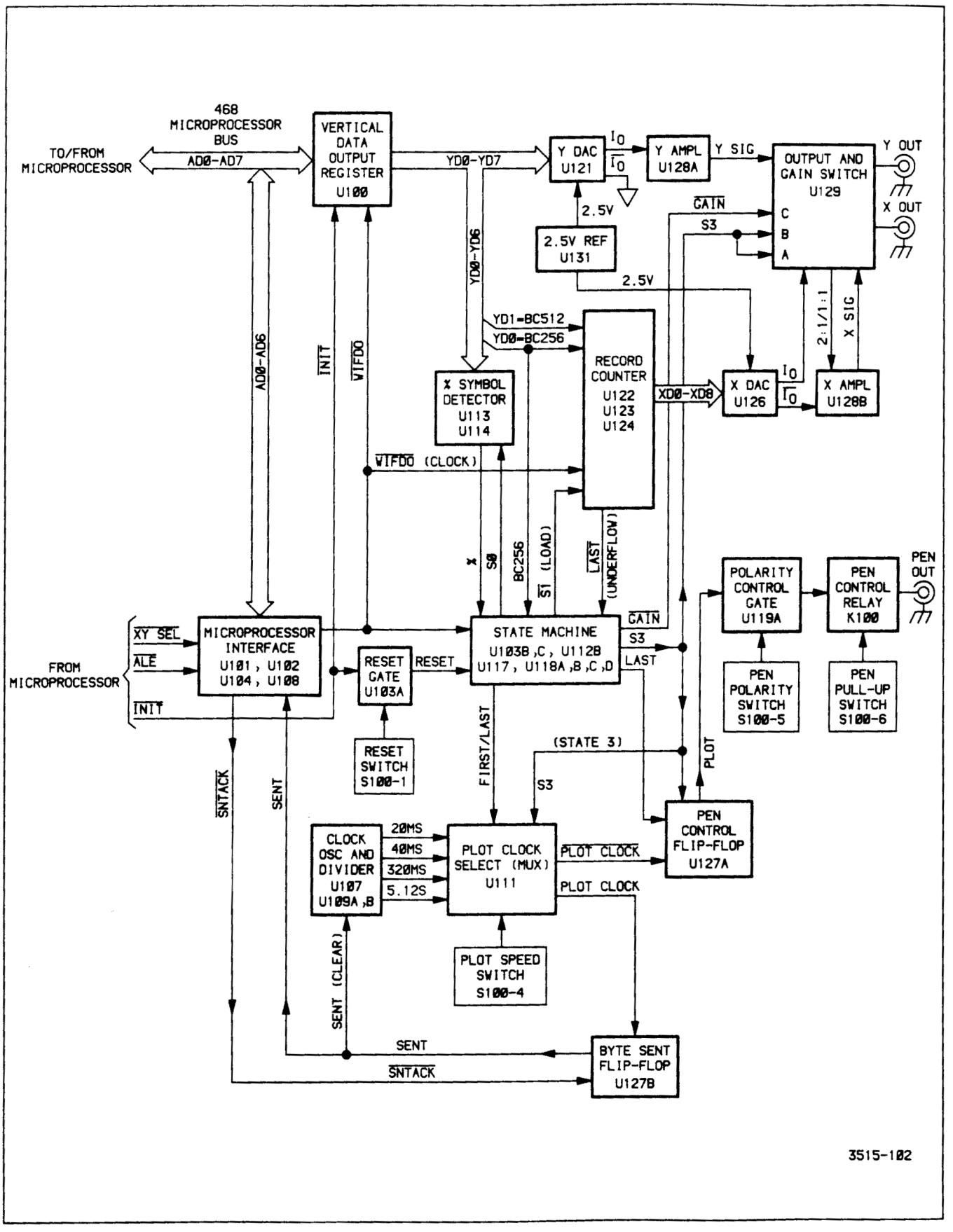


Figure 6-10. Block diagram of Analog X-Y Output Option.

When the user presses the PLOT push button on the 468 left-side panel, the 468 Microprocessor begins to transmit the stored waveform data to the Analog X-Y Output Option board. This transmission includes a preamble, scale-factor information, byte-count information, and the waveform data. (Refer to the GPIB information in the 468 Operators manual for a detailed description of the transmission format.) The entire transmission would be used by the GPIB Option. The Analog X-Y Output Option, however, requires only the byte count and waveform data portion of the transmission. It thus waits for the ASCII % (percent) character that precedes the byte count in the transmission before it commences to process the data. All of the preamble and scale-factor information that comes before the % character is ignored.

Upon detection of the % character, the Analog X-Y Output Option loads the first byte-count byte into the Record Counters, discards the second byte-count byte, and prepares to receive the waveform data points that follow.

The waveform data points are then processed through a digital-to-analog converter (DAC) to provide the Y-Axis output to the X-Y Plotter attached. A second DAC uses the count contained in the Record Counters to generate the X-Axis signal to the X-Y Plotter. At the end of the current waveform plot, the Analog X-Y Output Option returns to the mode of searching for the % symbol.

Detailed control of the circuit operations is provided by a State Machine. Other circuits provide for interfacing with the 468 Microprocessor and for timing the operation of the Option circuitry.

DETAILED CIRCUIT DESCRIPTION

MICROPROCESSOR INTERFACE CIRCUITS

The Microprocessor Interface Circuits consist of Talk Register U102, Address Demultiplexer Register U104, Address Decoder U108, and Status Buffer U101. These circuits accomplish the address communication and basic timing functions that occur between the Analog X-Y Output Option and the 468 Microprocessor.

Talk Register U102 forces the 468 GPIB firmware into a talk-only mode whenever power is applied to the 468.

NOTE

Section 8 of the 468 OPTIONS/SERVICE switch must be closed when power is applied to the 468 to enable the Analog X-Y Output Option.

At power on, the $\overline{\text{TALKREG}}$ strobe is generated by the Address Decoder, and the Microprocessor reads the data on the AD0 through AD4 bus lines and the AD7 bus line placed there by U102. All of these bus lines have a zero, due to the hardwired ground on all of the U102 input pins. The Microprocessor interprets the data as the GPIB Talk-Only Mode and sets up to transmit waveform data whenever the PLOT push button is pressed.

Adress Demultiplexer Register U104 receives the address information from the bidirectional Microprocessor bus lines AD0, AD1, and AD2. On the rising edge of the $\overline{\text{ALE}}$ (Address Latch Enable) signal from the Microprocessor, the address bits at the input pins of U104 are transferred to the output pins of U104. From U104, the three-bit address demultiplexed from the bus lines is applied to Address Decoder U108 (a 1-in-8 decoder). When enabled by the $\overline{\text{XYSEL}}$ (X-Y Select) signal, the Address Decoder produces one of four possible output strobe signals. The $\overline{\text{XYSEL}}$ signal is decoded from the high-order Microprocessor address bits and is timed to be active (LO) during the data portion of the Microprocessor cycle. Refer to the Microprocessor portion of the 468 Theory of Operation for the decoding description.

NOTE

On GPIB Option schematic diagrams and in the circuit descriptions, $\overline{\text{XYSEL}}$ is termed $\overline{\text{GPIBSEL}}$. Since the Analog X-Y Output Option replaces the GPIB Option, the signal name is also changed.

Possible control strobes decoded by U108 are:

1. $\overline{\text{TALKREG}}$—used at power on to force the 468 GPIB firmware into the talk-only mode.

2. $\overline{\text{SNTACK}}$—used to reset the Sent Flip-flop and acknowledge that the SENT signal has been received by the Microprocessor.

3. $\overline{\text{RIFSTAT}}$—used to enable the Status Buffer so the Microprocessor can read the status of the Analog X-Y Output Option. The Microprocessor is checking the SENT bit to determine if the current data byte has been sent. If not, the Microprocessor does not place a new data byte on the bus, but waits until the SENT bit goes HI.

4. $\overline{\text{WIFDO}}$—used to enable the Vertical Data Output Register to transfer the data byte at the input pins to the output pins. This control strobe also clocks the Record Counter, which keeps a count of the number of bytes sent, and the State Machine, which determines the operation that the Analog X-Y Output Option performs.

When the Analog X-Y Output Option is to be addressed to start processing waveform data, the Microprocessor puts the Option address (binary 100) on the AD0, AD1, and AD2 bus lines and places address bits on the high-order address lines that will be decoded to cause the $\overline{\text{XYSEL}}$ signal to be LO during the data portion of the Microprocessor cycle. The Microprocessor then applies a byte of data to the AD0 through AD7 bus lines, and $\overline{\text{XYSEL}}$ enables Address Decoder U108. The Address Decoder produces the $\overline{\text{WIFDO}}$ strobe to Vertical Data Output Register U100, and on the strobe's rising edge, U100 latches the data byte in. That data byte remains on the output pins of U100 until the next data byte is latched in.

Status Buffer U101 is read by the Microprocessor to determine if the Analog X-Y Output Option is ready to receive another data byte. At the end of processing each data byte, the Sent Flip-flop (U127B) is clocked to make SENT HI at U127B, pin 9. When the Microprocessor polls the Option Status Buffer, a HI on the SENT line tells the Microprocessor that the next data byte can be transmitted. The Microprocessor places the address to produce the $\overline{\text{SNTACK}}$ strobe on the AD0 through AD2 bus lines and enables the Address Decoder to decode the address and reset the Sent Flip-flop.

VERTICAL DATA OUTPUT REGISTER

The Vertical Data Output Register consists of eight-bit register U100 which accepts data from the Microprocessor bus lines and holds that data for one byte count. The waveform data is loaded into U100 on the rising edge of the $\overline{\text{WIFDO}}$ strobe produced by the Microprocessor from Address Decoder U108, pin 11. From the output pins of U100, data bytes are supplied to the Percent Symbol Detector and to the Y-Output circuits.

Y-OUTPUT CIRCUITS

The Y-Output circuits consist of Y Digital-to-Analog Converter (DAC) U121, Operational Amplifier U128A, and one section of Field-Effect Transistor (FET) Switch U129. These circuits convert the eight-bit digital output of the Vertical Data Output Register into the analog voltage required for providing Y-Axis deflection for plotting the waveform by an external X-Y Plotter.

Y-DAC U121 is a 10-bit current output converter with the two most significant bits hardwired to ground. The eight-bit data bytes are converted into a current signal output at pin 4 of U121. Operational Amplifier U128A transforms the current signal into a voltage signal for use by the external X-Y Plotter. One section of FET switch U129 is used to turn the Y-output on during the plot. When off, FET switch U129 isolates the plot pen from any data transmitted by the Microprocessor during nonplotting times and holds the plot pen at the home position. The Y-output is turned on when the S3 signal is HI (State Three of the State Machine).

PERCENT SYMBOL DETECTOR

The Percent Symbol Detector circuit consists of comparators U113 and U114 which compare each byte of the input data with a fixed reference byte. Input lines B0 through B3 of U113 and U114 are hardwired to HI and LO levels in the configuration of the ASCII % symbol. When the % symbol occurs in the data transmission from the Microprocessor, the comparators output the % signal to the State Machine to tell it that the next byte is the first byte-count byte at the beginning of the waveform block. Bytes that precede the % symbol are the GPIB waveform preamble and scale factor information and are not needed by the Analog X-Y Output Option. The % signal causes the State Machine to move to State One, and the comparators are disabled from searching for a % symbol.

STATE MACHINE

The State Machine consists of register U117 (a quad-D flip-flop), First Flip-flop U112, and associated AND, NAND, and exclusive-OR gating composed of U103, U118, and U119 respectively. These circuits produce the state signals that control the detailed operation of the Analog X-Y Output Option. Inputs to the State Machine include the % symbol from the Percent Symbol Detector, the $\overline{\text{WIFDO}}$ clocking signal from Address Decoder U108, the Byte Count 256 (BC256) signal from the Microprocessor bus via Vertical Data Output Register U100, and the $\overline{\text{LAST}}$ signal from U122 in the Record Counter. Outputs from the State Machine include the $\overline{\text{GAIN}}$ signal, the

State signals (S0, S1, S2, and S3), the LAST signal, and the combined FIRST/LAST signal.

State conditions for the states are described in the following paragraphs. The overall flow sequence of the states is illustrated in Figure 6-11.

State Zero is established when the $\overline{S1}$, $\overline{S2}$, and $\overline{S3}$ state signals are all HI at the input of AND-gate U103C. The HI S0 state signal from U103C pin 8 is applied to pin 3 of comparator U114 in the Percent Symbol Detector to enable the circuit to compare the incoming waveform data from the Microprocessor bus with the fixed ASCII % symbol configuration hardwired on the B input pins. When the % symbol is detected, pin 6 of U113 is switched HI and applied to pin 5 of register U117.

On the next rising edge of the $\overline{WIFDO}$ strobe at U117 pin 9, S1 is clocked HI at U117 pin 7, and State One is established. At this time $\overline{S1}$ goes LO and the byte count (256 or 512) is loaded into the Record Counters. The BC256 signal logic level at pin 4 of U118B is used to determine the gain setting of X-Output Amplifier U128B during this state, through the gating of U118A, U118B, and U103B. S1 will remain HI for the first byte count only, because the S0 signal goes LO at the output of U103C during State One. This action causes the % signal at the output of U113 at pin 6 to also go LO, and on the next $\overline{WIFDO}$ strobe rising edge, S1 is clocked LO.

On the same clocking pulse that clocks S1 LO, the HI present on U117 pin 12 (S1 before being clocked LO) is gated through to U117 pin 10 to set up State Two. The HI S2 signal is applied to the D input of U112B, pin 12, in preparation for the next clocking signal to generate the FIRST signal, and pin 13 of U117 goes HI through the gating of U118C and U118D. No action is taken with the second byte-count byte that is sent prior to the waveform data points.

The next clocking pulse clocks both S3 and the FIRST signal (at pin 9 of U112B) HI to set up State Three of the State Machine. State Three will remain in effect until the $\overline{LAST}$ signal from the Record Counter signals that the last waveform data byte is being processed. The FIRST signal is gated through exclusive-OR gate U119B, in combination with the LAST signal, to select the timing for the first waveform data point. Both the first and last data points have a five-second delay to allow for manual pen control on some X-Y Plotters. See the "Plot Timing Circuits" discussion for an explanation of the timing. On the next clocking pulse, the FIRST signal becomes LO, and the remaining data points are plotted at the speed established by the PLOT SPEED switch.

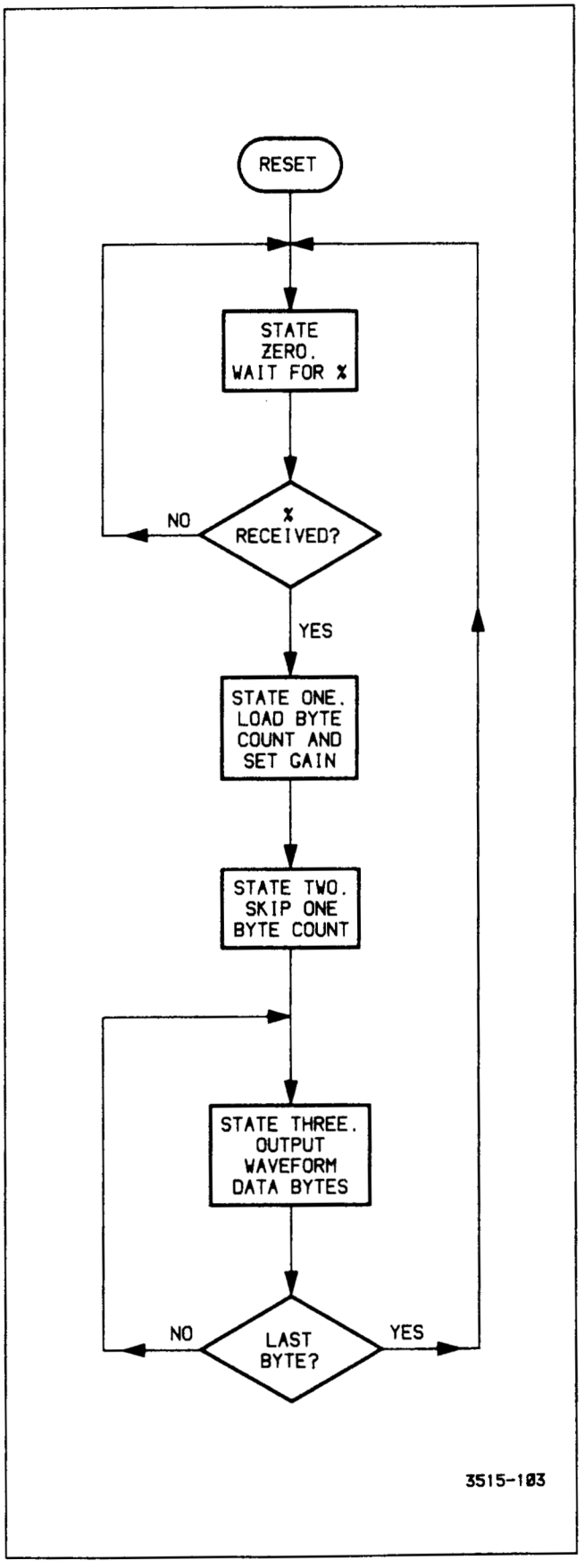


Figure 6-11. Analog X-Y Output Option stste flow chart.

RECORD COUNTER

The Record Counter consists of hexadecimal counters U122, U123, and U124. These counters count either 512 or 256 bytes, depending on the byte count loaded during State One. In State One, the LO $\overline{S1}$ signal from the State Machine enables the counters to be set to the maximum count (either 512 for single and alternate storage acquisitions or 256 for chopped acquisitions). The maximum count, except for the BC512 and BC256 inputs, is hardwired into the counters. When BC256 is HI, the counters are loaded with 010000000000_2 or 256_{10}. The $\overline{WIFDO}$ strobe that sets up State Two also decrements the counters to either 511 or 255, as appropriate, for the start of the waveform plot.

As the waveform is plotted, the counters are continually decremented one count for each plot point (data byte) until the underflow output from U122 pin 12 (the $\overline{LAST}$ signal) goes LO. This indicates to the State Machine that the last byte plot is being processed and causes the State Machine to return to State Zero. The $\overline{LAST}$ signal is also applied through exclusive-OR gate U119B to allow Pen Control flip-flop U127A to be reset at the end of the last plot.

During State Three, the byte count contained in the Record Counter is applied via nine lines to the X-Output circuits for processing into the analog X-Axis signal for the external X-Y Plotter.

X-OUTPUT CIRCUITS

The X-Output circuits consist of X Digital-to-Analog Converter (DAC) U126, Operational Amplifier U128B, and two sections of Field-Effect Transistor (FET) switch U129. These circuits convert the nine-bit hexadecimal byte count from the Record Counter into the analog voltage required for time base (X-Axis) of the wavefrom plotted by the external X-Y Plotter.

X-DAC U126 is a current output type converter as is the Y-DAC. Signal currents at output pins 2 and 4 increase or decrease differentially according to the digital input. Operational Amplifier U128B transforms the DAC output current into a voltage signal for use by the external Plotter. Configured as an inverting amplifier, U128B, in combination with the gain-switching section of U129, provides either a 2:1 gain (for 256-point waveforms) or a 1:1 gain (for 512-point waveforms).

For chopped-mode signal acquisitions, 256 data points define the full waveform. Therefore, the gain of U128B must be changed to still accomplish full-scale deflection of the X-Y Plotter X-Axis. Amplifier gain is controlled by switching pin 5 of U128B either to ground for a signal gain of one or to pin 4 of U126 and R135 for a signal gain of two. The $\overline{GAIN}$ signal from the State Machine controls the gain-switching section of U129. When $\overline{GAIN}$ is LO, pin 5 of U129 connects to pin 4 of U129, and the gain of U128B is two. $\overline{GAIN}$ is HI for a 512-point waveform, and pin 3 of U129 (ground) is connected to pin 4 of U129 for a gain of one.

Another section of FET switch U129 is used to turn the X-Output to the Plotter on or off and is controlled by the S3 (State 3) signal from the State Machine. The X-Output switch section is turned on when S3 is HI. When off, this switch holds the X-Y Plotter plot pen at the home position by effectively isolating the Plotter from the data transmitted by the Microprocessor during nonplotting times.

PLOT TIMING CIRCUITS

The Plot Timing circuits consist of Oscillator U107, Clock Divider U109, Plot-Clock Select Multiplexer U111, Byte-Sent Flip-flop U127B, and Pen Control Flip-flop U127A. These circuits control the pen-lift timing of the external X-Y Plotter and signal to the Microprocessor when the current waveform data point has been plotted.

The basic clocking frequency is produced by Oscillator U107 which free runs at a frequency of 50 Hz. The 50-Hz output from U107 pin 3 is applied to both Clock Divider U109 and Plot-Clock Select Multiplexer U111. In the Clock Divider circuitry, the 50-Hz frequency is divided down to provide three additional clocking frequency outputs. (For ease of description, the clocking signals will be defined by cycle period, not frequency.) Since the 50-Hz input signal period is 20 ms; the cycle period at U109 pin 3 is 40 ms (divided by two), the cycle period at U109 pin 6 is 320 ms (pin 3 output divided by eight), and the cycle period at U109 pin 8 is 5.12 s (pin 6 output divided by 16). These four clocking frequencies (the basic 50 Hz plus the three divided down signals) are all applied to the input pins of Plot-Clock Select Multiplexer U111, where they are available for selection according to the output state of the State Machine and the setting of the PLOT SPEED switch. See Table 6-6 for Multiplexer U111 switching logic.

From Table 6-6, it can be seen that during nonplot periods when S3 is LO, the clock period is 20 ms. This clocking period is used to transfer the data as rapidly as possible from the Microprocessor while the Percent Symbol

Table 6-6

Multiplexer U111 Switching Logic

Select Inputs			Clock Period Selected	Function
C Plot Speed	B S3	A First/ Last		
0	0	0	20 ms	Fast Data Xfer
0	0	1	20 ms	Fast Data Xfer
0	1	0	320 ms	Slow Plot
0	1	1	5.12 s	First or Last
1	0	0	20 ms	Fast Data Xfer
1	0	1	20 ms	Fast Data Xfer
1	1	0	40 ms	Fast Plot
1	1	1	5.12 s	First or Last

Detector is looking for the beginning of the waveform data block. 20-ms clocking signals to Byte-Sent Flip-flop U127B are continuous, and the SENT output signal from U127B will become HI on the first clock rising edge that occurs after being reset by the $\overline{\text{SNTACK}}$ strobe. Since the Microprocessor responds quickly during data transfer, the transfer byte rate is nearly 50 Hz for the preamble and scale-factor data bytes.

When the % symbol is detected, the State Machine switches to State One, and the byte count is loaded into the Record Counter. State Two is entered for one data byte, and First Flip-flop U112B is clocked to make the FIRST signal HI for the first waveform data byte; then State Three is entered, and S3 becomes HI.

From Table 6-6, when S3 and FIRST/LAST are both HI with either PLOT SPEED chosen, the clock period selected is 5.12 seconds. At the output pins of U111, $\overline{\text{PLOT CLOCK}}$ from pin 6 is applied to the clock input of Pen Control Flip-flop U127A, the PLOT CLOCK (the complement of $\overline{\text{PLOT CLOCK}}$) from pin 5 is applied to the clock input of Byte-Sent Flip-flop U127B.

The rising edge of the PLOT CLOCK signal on pin 13 of U127B causes the SENT signal to switch HI. A HI on the SENT line clears the Clock Dividers and signals the Microprocessor, via Status Buffer U101, that the current data byte has been sent. When the Microprocessor acknowledges with the $\overline{\text{SNTACK}}$ strobe, Byte-Sent Flip-flop U127B is reset to make SENT LO. The clear on the Clock Dividers is thereby released, and they start dividing to produce the next clock cycle.

At about 2.5 seconds into the 5.12-second period of the first waveform data byte (one-half of the period), the rising edge of the $\overline{\text{PLOT CLOCK}}$ clocks Pen Control Flip-flop U127A to switch U127A pin 6 LO. The 2.5-second delay allows the plot pen time to reach the first data point to be plotted and settle down before the pen is lowered.

The output of U127A is applied to Polarity Control Gate U119A, an exclusive-OR gating circuit, on pin 1. PEN POLARITY switch S100-5 controls the logic level on pin 2 of the gate. Polarity Control Gate U119A acts as a switchable inverter to allow the use of external X-Y Plotters that require either open-contact or closed-contact pen control signals. If the PEN POLARITY switch is closed, Pen Control Relay K100 will have closed contacts when the plot pen should be down. The opposite is true when the PEN POLARITY switch is open.

The plot pen remains down until the last byte is indicated by the Record Counters. At that time, the LAST signal going HI at pin 2 of U127A enables the Pen Control Flip-flop to be reset by the next clock rising edge. On the last data byte, the reset occurs again at about 2.5 seconds into the 5.12-second clock period. The delay on the last data byte prevents a retrace from being drawn.

Between the first and last waveform data bytes, S3 remains HI, but the FIRST/LAST signal is LO. From Table 6-6, the clock period chosen with these logic levels on the select inputs of U111 is either 40 ms or 320 ms, depending on the setting of PLOT SPEED switch S100-4. When the switch is open, the plot speed is 40 ms (fast plot); when closed it is 320 ms (slow plot).

When each byte is loaded into the Vertical Data Output Register U100, the Microprocessor begins polling the Status Buffer, waiting to find the SENT bit HI. When the clock cycle is completed, SENT goes HI, and as soon as the Microprocessor acknowledges with $\overline{\text{SNTACK}}$, the next clock cycle is started.

If RESET switch S100-1 is closed while waveform data is being plotted, the RESET signal is produced from U103A and applied to U117 at pin 1 and to U112B (the First Flip-flop) at pin 13. The RESET signal returns the State Machine to State Zero and resets First Flip-flop U112B. Any remaining waveform data is then transferred at the 20-ms clock rate, while the X- and Y-Outputs are held off by U129.

PERFORMANCE CHECK

PURPOSE

This performance check is used to verify the Performance Requirements of the Analog X-Y Output Option as listed in Table 6-5. Introductory information contained at the beginning of the 468 Performance Check in this volume is applicable for preparing to complete this procedure.

TEST EQUIPMENT REQUIRED

The following equipment is required to perform the complete Performance Check procedure. The numbers preceding equipment types correspond to the items listed in Table 4-1 is this volume.

Equipment Required:

4. Test Oscilloscope
8. Low-Frequency Sine-Wave Generator
12. 42-in, 50-Ω BNC Cable (4 required)

CHECK PROCEDURE

NOTE

Section 8 of the 468 internal OPTIONS/SERVICE switch must be closed when the instrument is powered up to enable the Analog X-Y Output Option. Refer to Figure 5-6 in the "Maintenance" section of this manual for the switch location if necessary to set this switch.

468 CONTROL SETTINGS

POWER	ON (button in)

CRT

INTENSITY	As required for visible display
FOCUS	Best focused display
SCALE ILLUM	As desired

Vertical (Both Channels if Applicable)

VERT MODE	CH 1
POSITION	Midrange
VOLTS/DIV	5 mV
VOLTS/DIV VAR	Calibrated detent
AC-GND-DC	DC
INVERT	Normal (button out)
20 MHz BW LIMIT	Full Bandwidth (button out)

Trigger

COUPLING	AC
LEVEL	Midrange
SLOPE	+
A SOURCE	CH 1
TRIG MODE	AUTO
A TRIGGER HOLDOFF	NORM

Sweep

HORIZ DISPLAY	A
TIME/DIV	5 μs
TIME/DIV VAR	Calibrated detent
X10 MAG	Off (button out)
POSITION (horizontal)	Midrange

Digital Storage

STORAGE MODE	NORM
SAVE REF	Off (button out)
CURSOR FUNCTION	Off (both out)

Analog X-Y Output

RESET	Open (RESET off)
PLOT SPEED	Closed (Slow Plot)
PEN POLARITY	Closed (relay closed)
PEN PULL-UP	Closed (10 kΩ pull-up)

1. Check Analog X-Y Option Operation

a. Connect the Analog X-Y Output Option to the test oscilloscope as follows, using 50-Ω BNC coaxial cables. Use no terminations.

X OUT to CH 1 OR X

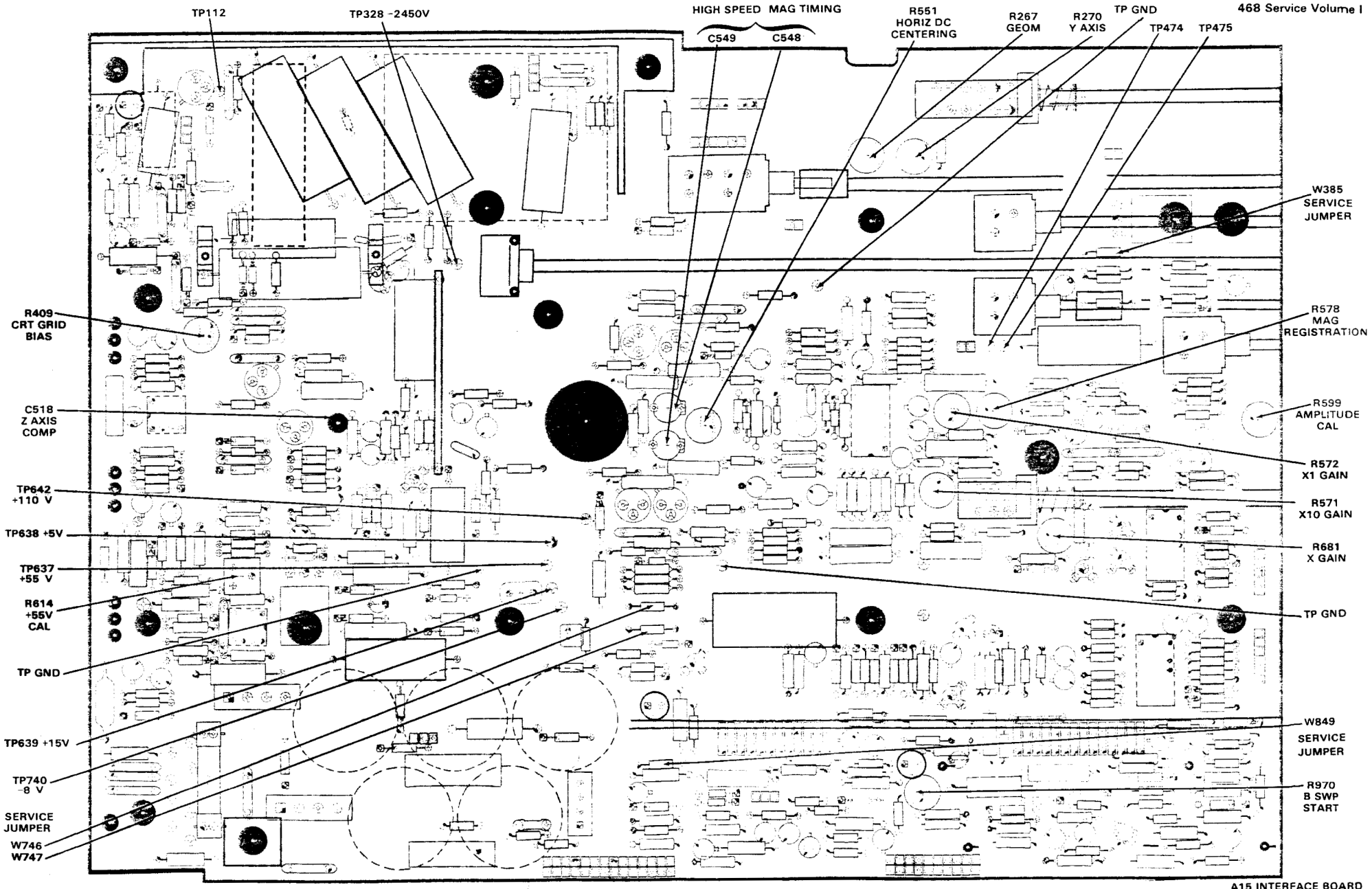
Y OUT to CH 2 OR Y

PEN OUT to EXT Z-AXIS
(on test oscilloscope rear panel)

b. Set the test oscilloscope controls:

Volts/Div (Ch 1 and Ch 2)	0.2 V
A and B Time/Div	X-Y
Ac-Gnd-Dc (Ch 1 and Ch 2)	Dc
Vert Mode	As required for X-Y display

c. Use the test oscilloscope Position controls to place the X-Y display spot at the lower left-hand corner of the crt graticule and adjust the Intensity control for a spot that is just visible.



Interface circuit board adjustment locations.

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d. Connect the low-frequency sine-wave generator via a 50-Ω unterminated cable to the 468 CH 1 OR X input connector.

e. Set the generator controls for a frequency of 50 kHz and adjust the output amplitude for a vertical display of 6 divisions.

f. Use the 468 CH 1 Vertical POSITION control to align the negative peaks of the sine-wave signal with the bottom horizontal graticule line.

g. Set the 468 VERT MODE switches for a CHOP display of CH 1, CH 2, and ADD.

h. Use the 468 CH 2 POSITION control to superimpose the ADD waveform over the CH 1 waveform. Do not move the CH 1 waveform from the position set in part f.

i. Press in the PLOT push button (located on the 468 upper right side panel).

j. CHECK—Waveform freezes (468 enters SAVE Storage Mode; if this does not occur, see note at beginning of this procedure). Immediately observe the test oscilloscope display.

k. CHECK—Spot becomes intensified and plots a sine-wave trace having 6 divisions of amplitude. Watch the entire waveform to determine if all the data points are plotted correctly (none either missing or away from the sine-wave trace).

l. Set PEN POLARITY switch to OPEN.

m. CHECK—Spot intensity on test oscilloscope decreases.

n. Set PEN PULL-UP switch to OPEN.

o. CHECK—Spot intensity on test oscilloscope increases.

p. Set PEN POLARITY and PEN PULL-UP switches back to CLOSED.

q. Set PLOT SPEED switch to OPEN (Fast Plot).

r. CHECK—Plot speed on test oscilloscope increases (by eight times; from 320 ms per data point to 40 ms per data point).

s. CHECK—All three traces saved on the 468 display (two sine-wave traces and one baseline trace) are plotted, and the 468 exits the SAVE Storage Mode and returns to NORM Storage Mode at the completion of the last plot.

t. Disconnect all test equipment from the 468.

MAINTENANCE

The information contained here pertains to specific troubleshooting of the Analog X-Y Output Option. General maintenance information and specific information pertaining to Service Test and Signature Analysis testing contained in the "Maintenance" section of this manual also apply to the Analog X-Y Output Option.

Signatures for the option circuitry consist of the Microprocessor Trap Test signatures (located in Table 5-10 in the "Maintenance" section of this volume) and the Analog X-Y Output Data Test signatures (found in Table 6-7). Analyzer and 468 setups required to perform the signature tests are also included in the signature tables.

CORRECTIVE MAINTENANCE

Troubleshooting procedures for the Analog X-Y Output Option are detailed in the troubleshooting chart (Figure 6-12) and associated notes. Illustrated in the specific notes are pertinent waveforms generated in the option circuitry under normal operating conditions.

The Option 11 schematic diagram and circuit board illustration are located in Volume II of this manual. Figure 6-13 indicates the location of test points on the Option 11 circuit board.

TROUBLESHOOTING CHART NOTES

The following text is divided into General and Specific notes. General notes pertain to information that must be observed when doing any troubleshooting or maintenance on the instrument. Specific notes are associated with certain steps in the troubleshooting chart. The note number corresponds to the number called out in the troubleshooting chart.

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.

SPECIFIC NOTES

1. Analog X-Y Output Option setup.

   a. Set OPTIONS/SERVICE switch section 8 to CLOSED position. (Refer to Figure 5-6 in the "Maintenance" section of this volume for switch location.) This switch must be closed when the 468 is powered on to enable the Analog X-Y Output Option.

   b. Set rear panel X-Y Option switches as follows:

RESET	Open (reset off)
PLOT SPEED	Open (fast plot)
PEN POLARITY	Closed (relay contact closed)
PEN PULL-UP	Closed (10 k pull-up)

   c. Check X-Y Output Options power supplies at the following points (refer to Figure 6-10 for test point locations):

+5 V	TP101
-12 V	TP103
+2.5 V	U131-2

   d. Verify that clock frequency is approximately 50 Hz at U107-3.

2. Microprocessor Interface Test.

   a. Perform Microprocessor Trap Test. Refer to Table 5-10 for signatures and test setup.

      (1) Start Trap Test by momentarily removing P262, then replacing it. (Refer to Figure 5-7 in the "Maintenance" section of this volume for jumper location.)

      (2) Verify +5-V Check Signature at TP101 (on the Analog X-Y Output circuit board).

      (3) If +5-V signature is OK, then verify remaining Trap Test signatures given in Table 5-10.

   b. Perform Analog X-Y Output Data Test. Refer to Table 6-7 for signatures and test setup.

      (1) Turn off the 468. Remove ROM U565 and install the Service Test ROM in its place.

      (2) Set the OPTIONS/SERVICE switch to 11111000 (see Figure 5-6 for switch location).

      (3) Turn 468 power on (Record Counters will free run for checking X-Axis output).

      (4) Verify +5-V Check Signature at TP101.

      (5) If +5 V signature is OK, then verify remaining Output Data Test signatures given in Table 6-7.

3. Pen Lift Test.

   a. Turn 468 power off.

   b. Check pen-lift fuse F100 on Analog X-Y Output Option board.

   c. Turn 468 power on.

   d. Check voltage at relay K100-8. Voltage should be +5 V.

   e. Set rear panel PEN POLARITY swtich to OPEN.

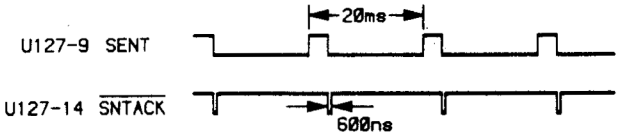
   f. Check voltage at relay K100-8 again. Voltage should be 0 V.

4. Byte Send Handshake Test.

   a. Set rear panel RESET switch to CLOSED.

   b. Connect test oscilloscope or logic analyzer probes to U127-9 (SENT signal) and U127-15 (SNTACK signal).

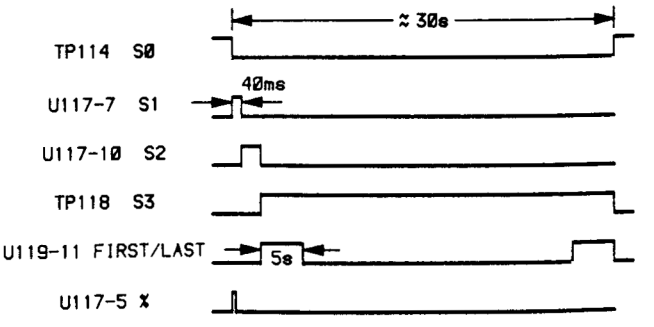
   c. Press in PLOT push button and check for waveforms as shown:



5. State Machine Test.

   a. Connect logic analyzer probes to the following points:
   TP114-SO signal
   U117-7-S1 signal
   U117-10-S2 signal
   TP118-S3 signal
   U119-11-FIRST/LAST signal
   U117-5-% signal

   b. Press in PLOT push button and check for waveforms as shown:



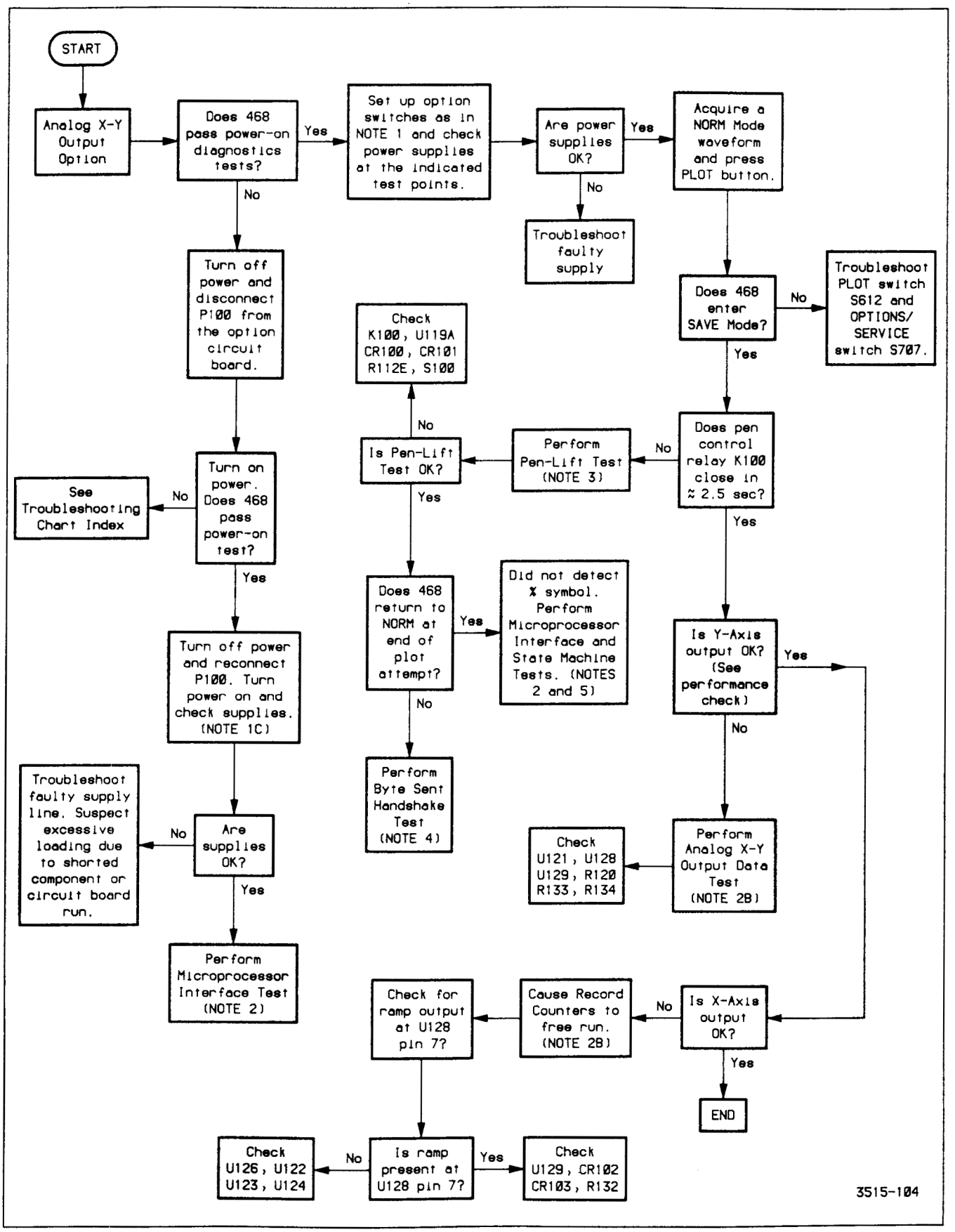


Figure 6-12. Analog X-Y Output Option troubleshooting chart.

Table 6-7

Version 2.0

Analog X-Y Output Data Test Signatures

Assy Number	Board Name	Part Number	Board Illustration	Schematic Diagram
A27	Analog X-Y Output	670-7551-00	8-27	26

Analyzer Setup

	Analyzer Setting	Probe Connect	Assy
Clock	↑	TP102	A27
Start	↑	TP358	A21
Stop	↓	TP358	A21

468 Setup

468 in Servicing Setup (see "Maintenance" section of this volume). Service Test ROM installed in U565 socket on A21. OPTIONS/SERVICE switch set to 11111000. Analog X-Y Output switches (on 468 rear panel) all OPEN. LED readout at completion of power-on should be 9211. To start or restart routine with POWER ON, move P182 on A21 to RESET position momentarily; then return it to RUN position.

+5 V Check Signature—5456

Component	Pin	Signature
U101	1	75C4
	2	5456
	4	5456
	6	5456
	14	0000
	16	0000
	18	0000
	19	75C4
U102	1	54H7
	2	0000
	4	0000
	6	0000
	10	0000
	12	0000
	14	0000
	15	54H7
U104	1	5456
	2	3396
	7	62UP
	15	54A7

Component	Pin	Signature
U108	1	3396
	2	62UP
	3	54A7
	5	0000
	6	5456
	7	75C4
	9	177A
	10	4672
	11	701C
	12	5446
	13	5476
	14	5416
	15	54H7
U100	1	5456
	2	7CUP
	5	PUU4
	6	CUHU
	9	1PUF
	11	701C
	12	HF17
	15	U706
	16	UHF2
	19	UU73

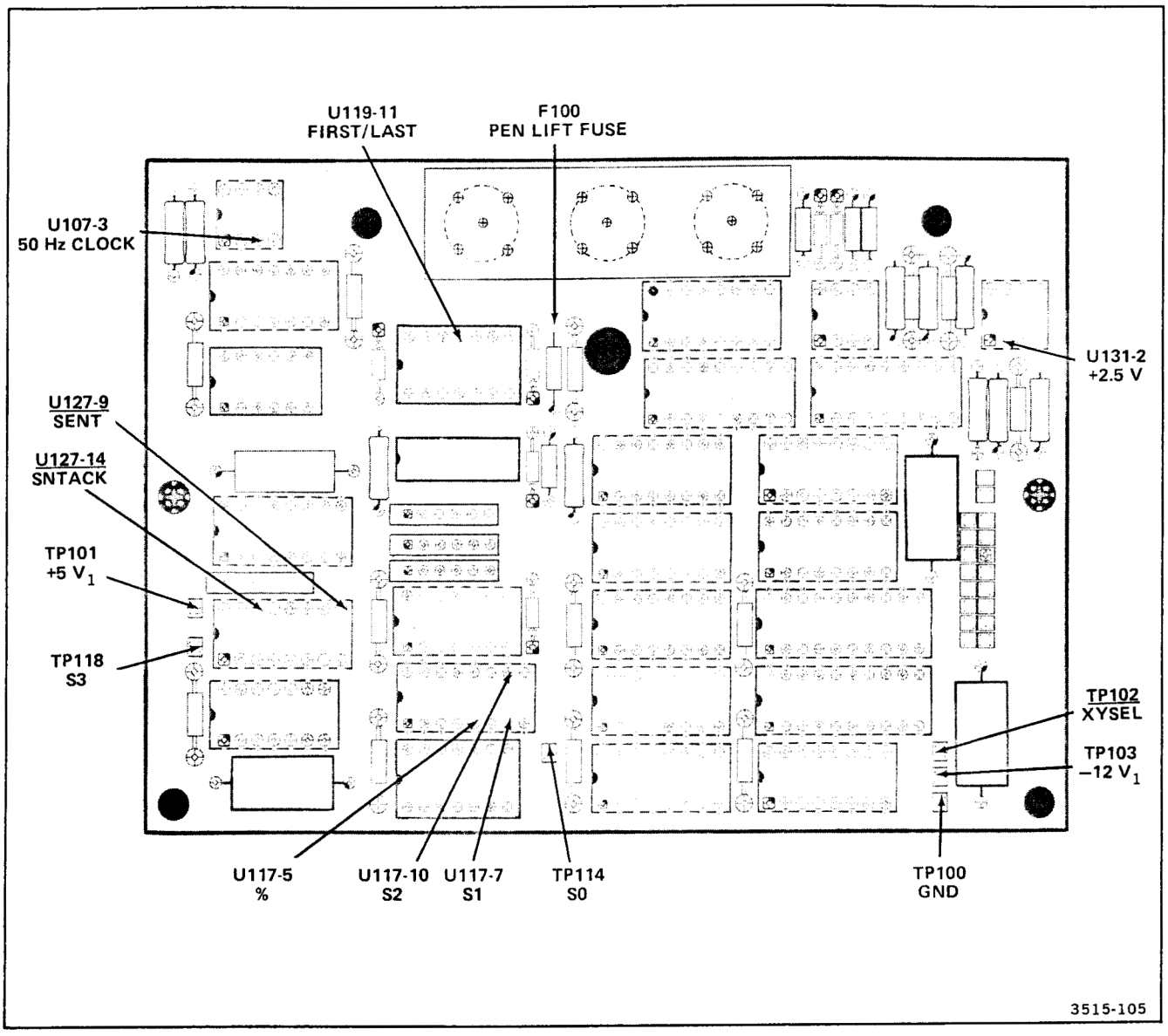
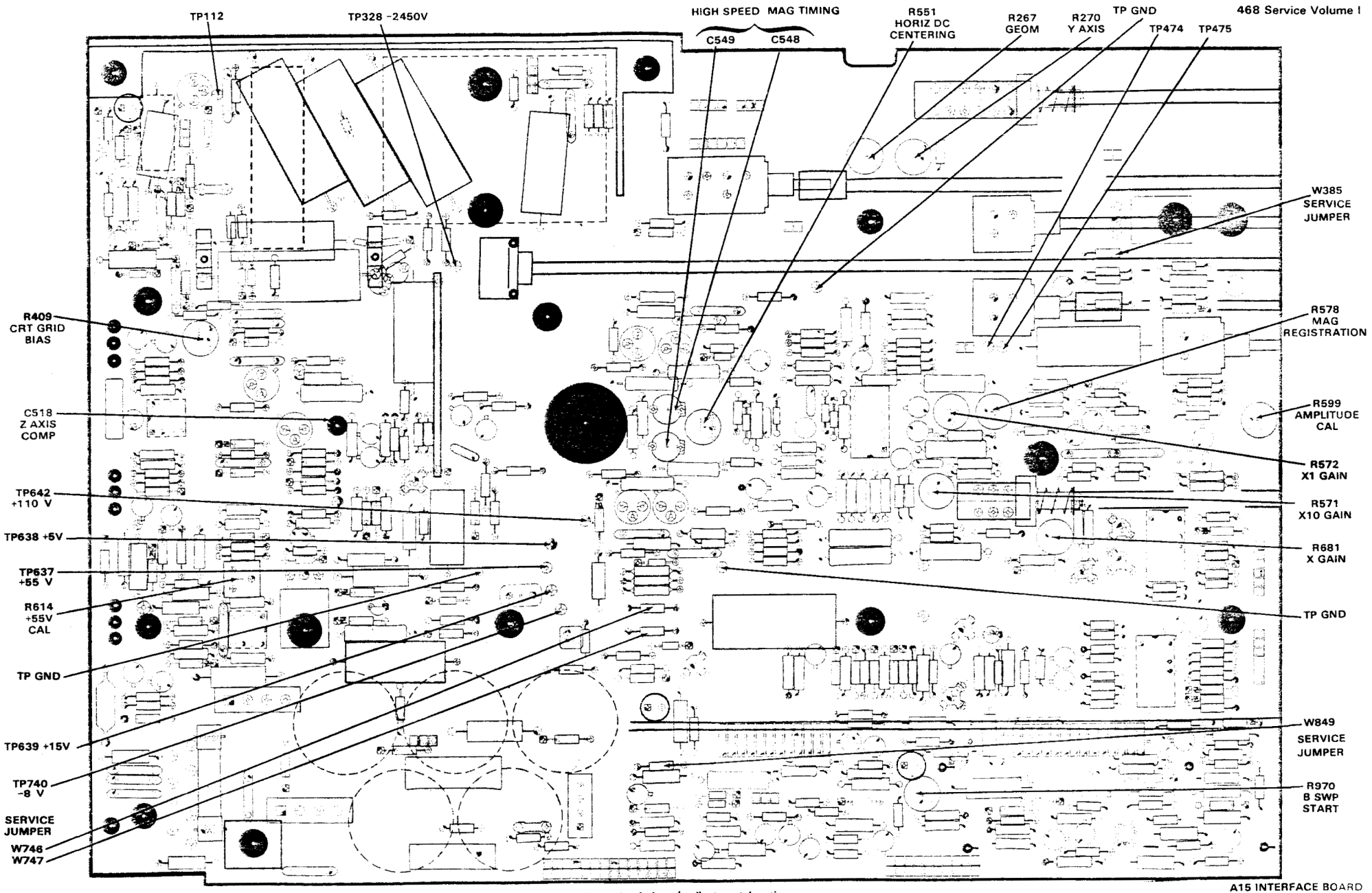


Figure 6-13. Analog X-Y Output Option test point locations.



Interface circuit board adjustment locations.

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A15 INTERFACE BOARD

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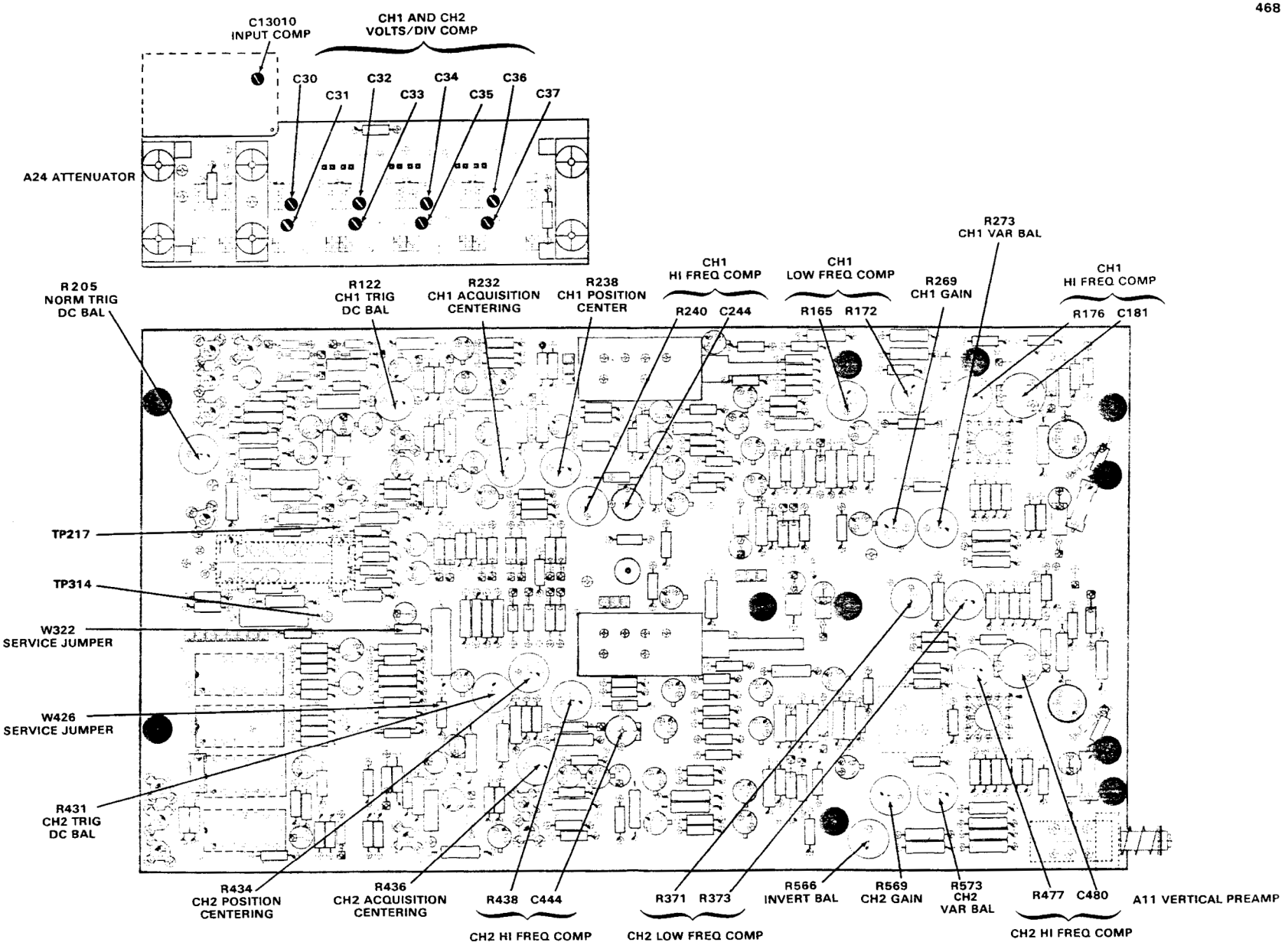

Vertical Preamplifier circuit board adjustment locations.

3515-74A

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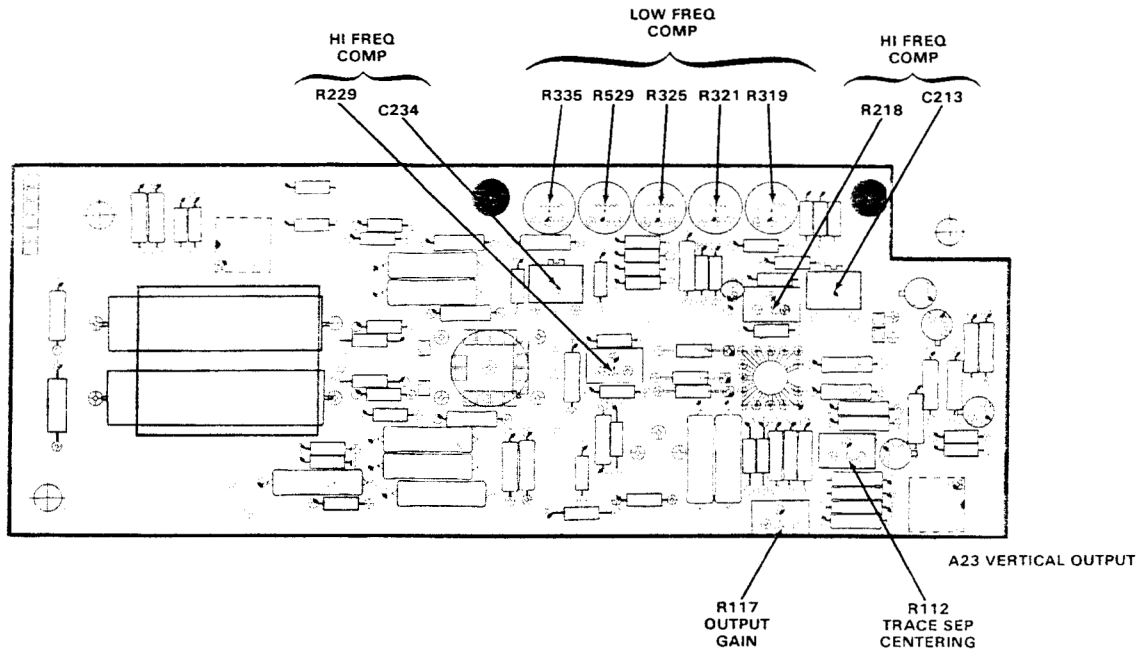
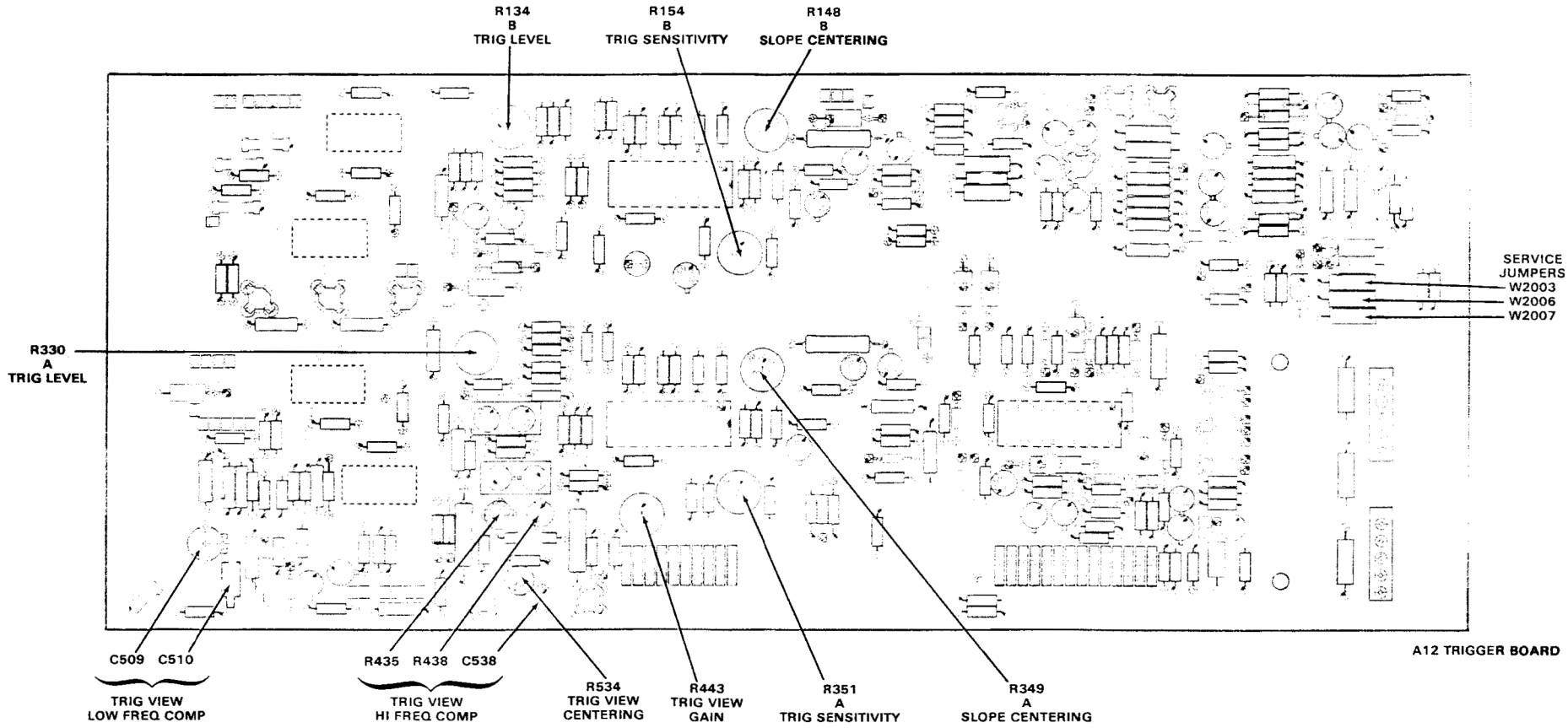


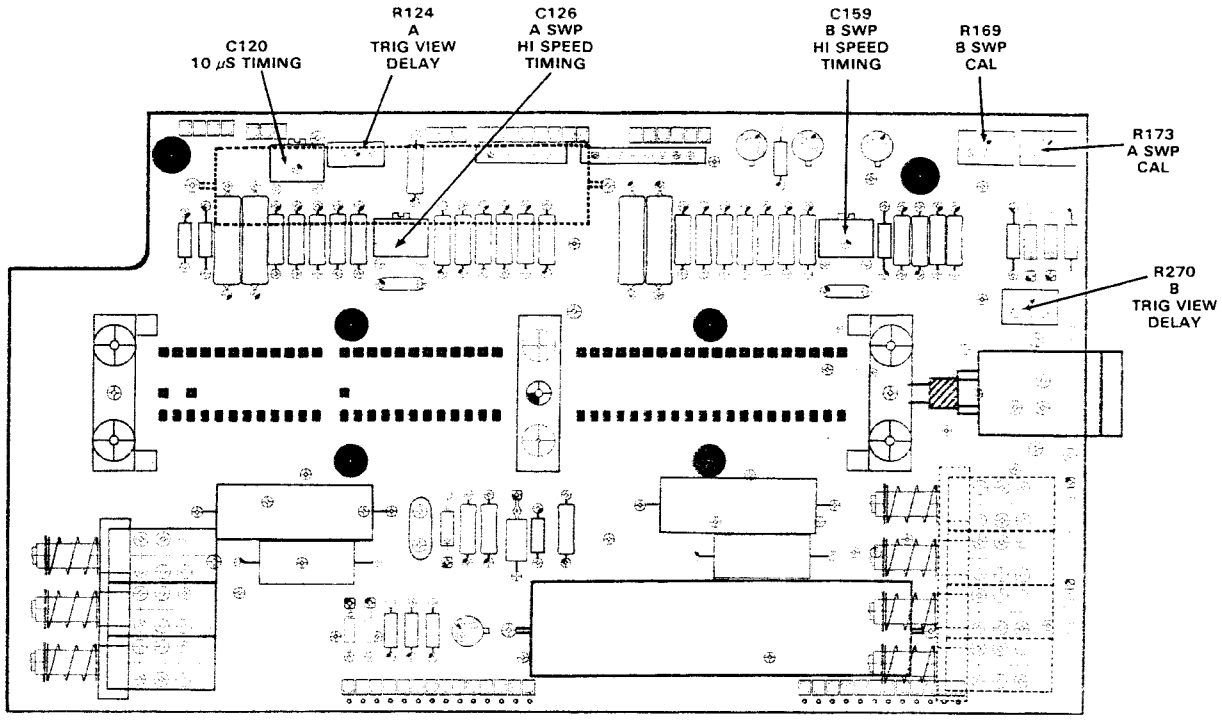
3515-75

Vertical Output board adjustment locations.



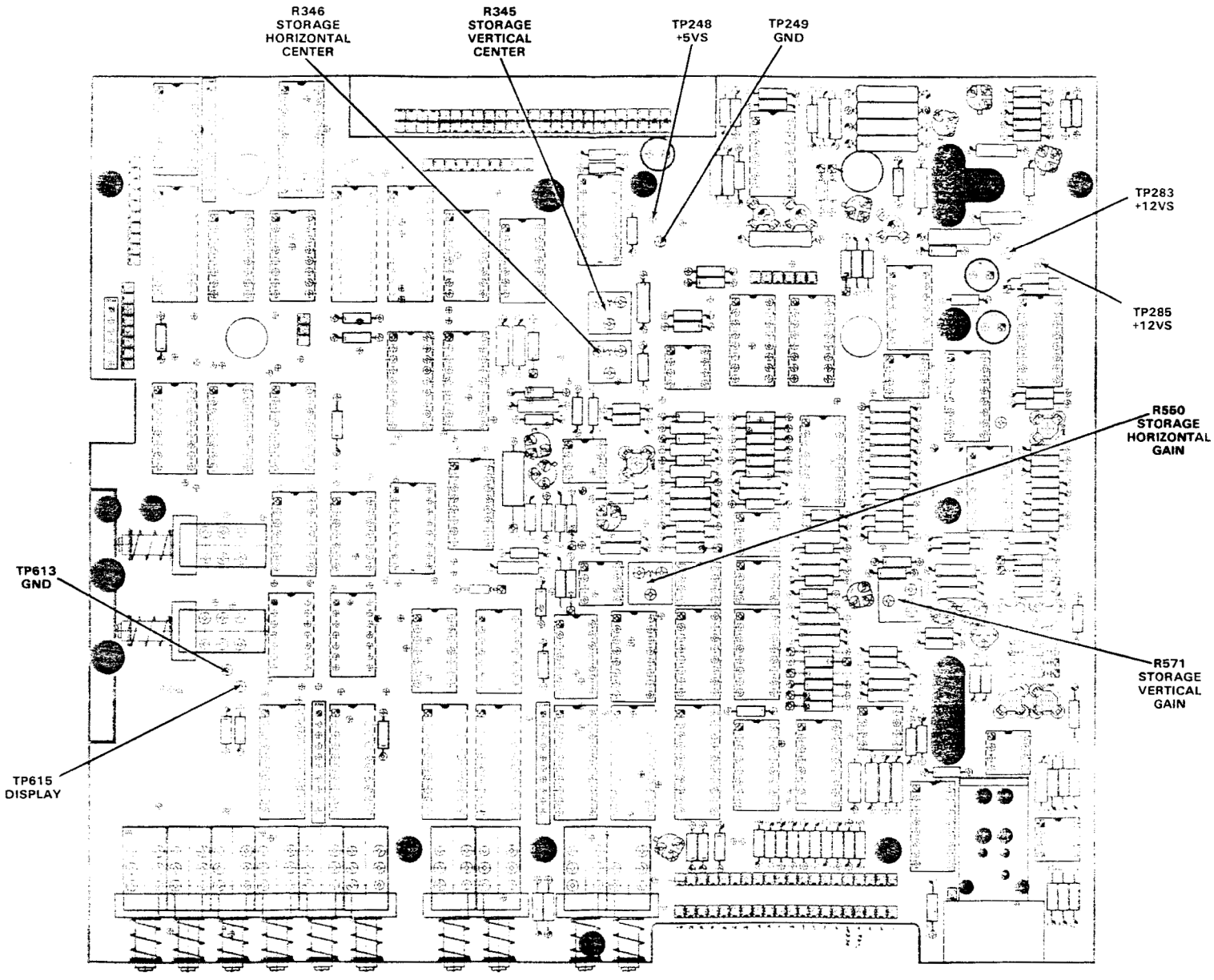
3515-76

Trigger Generator and Sweep Logic circuit board adjustment locations.



Timing board adjustment locations.

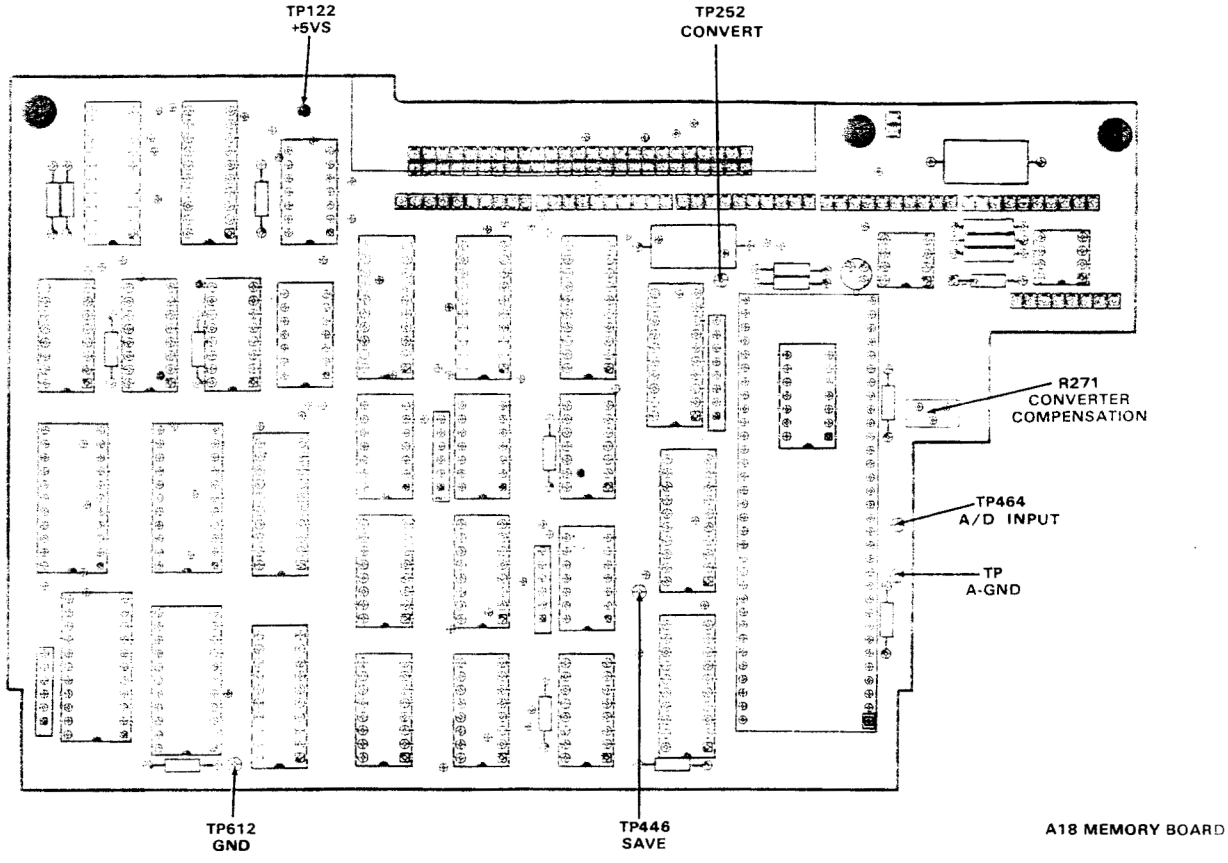
3515-77



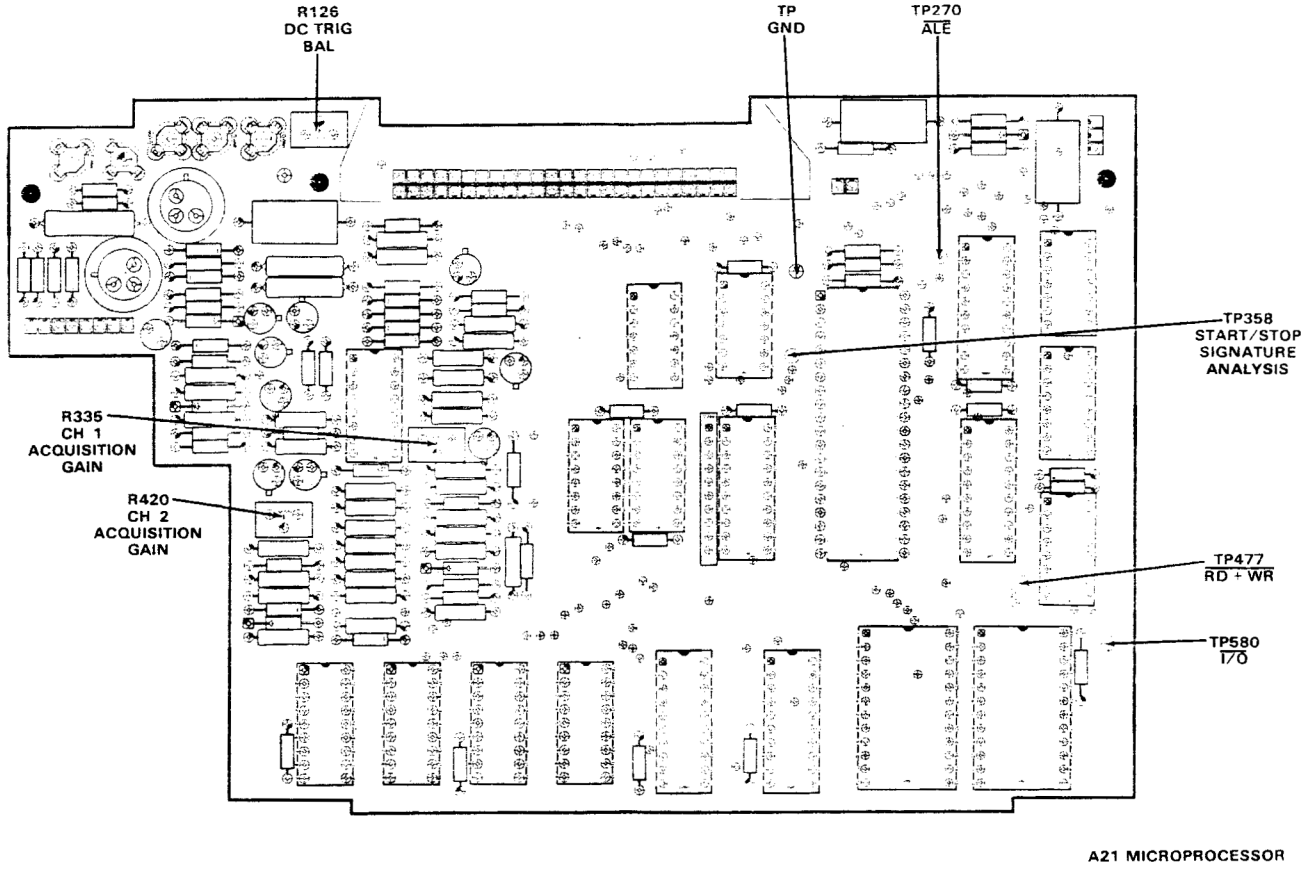
Storage Display board adjustment locations.

A16 STORAGE DISPLAY BOARD

3515-78

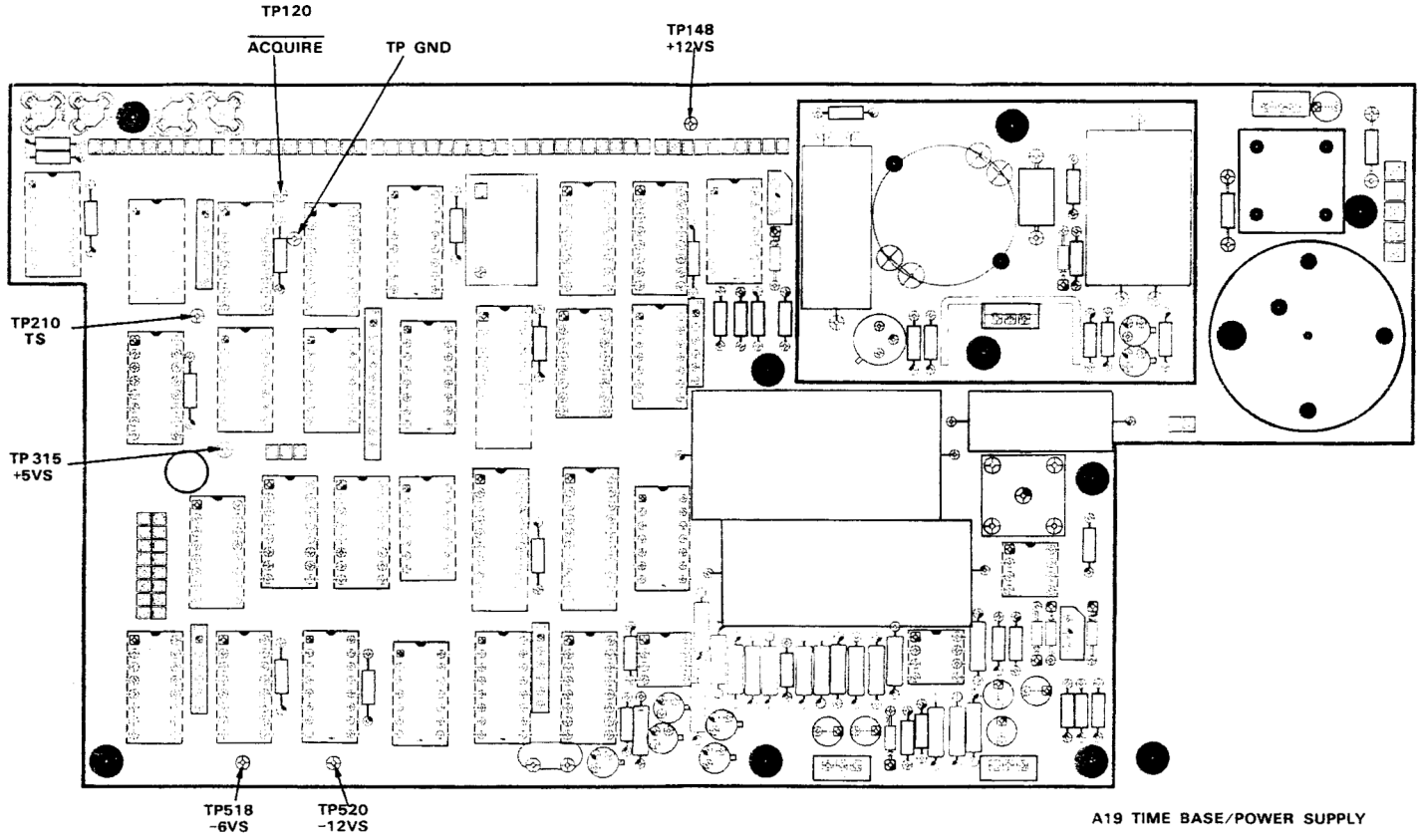


Memory board adjustment locations.



Microprocessor board adjustment locations.

3515-80



Time Base/Power Supply test point locations.

@

SPECIFIC NOTES

1. Initial control settings and connections:

NON STORE	On (button in)
TRIG MODE	AUTO
A and B TIME/DIV	1 ms
HORIZ DISPLAY	A
CH 1 VOLTS/DIV	.1 V
CH 1 AC-GND-DC	DC
VERT MODE	CH 1
CH 1 Signal Input	Calibrator square wave via 10X probe
Service/Options Switch	X1000000

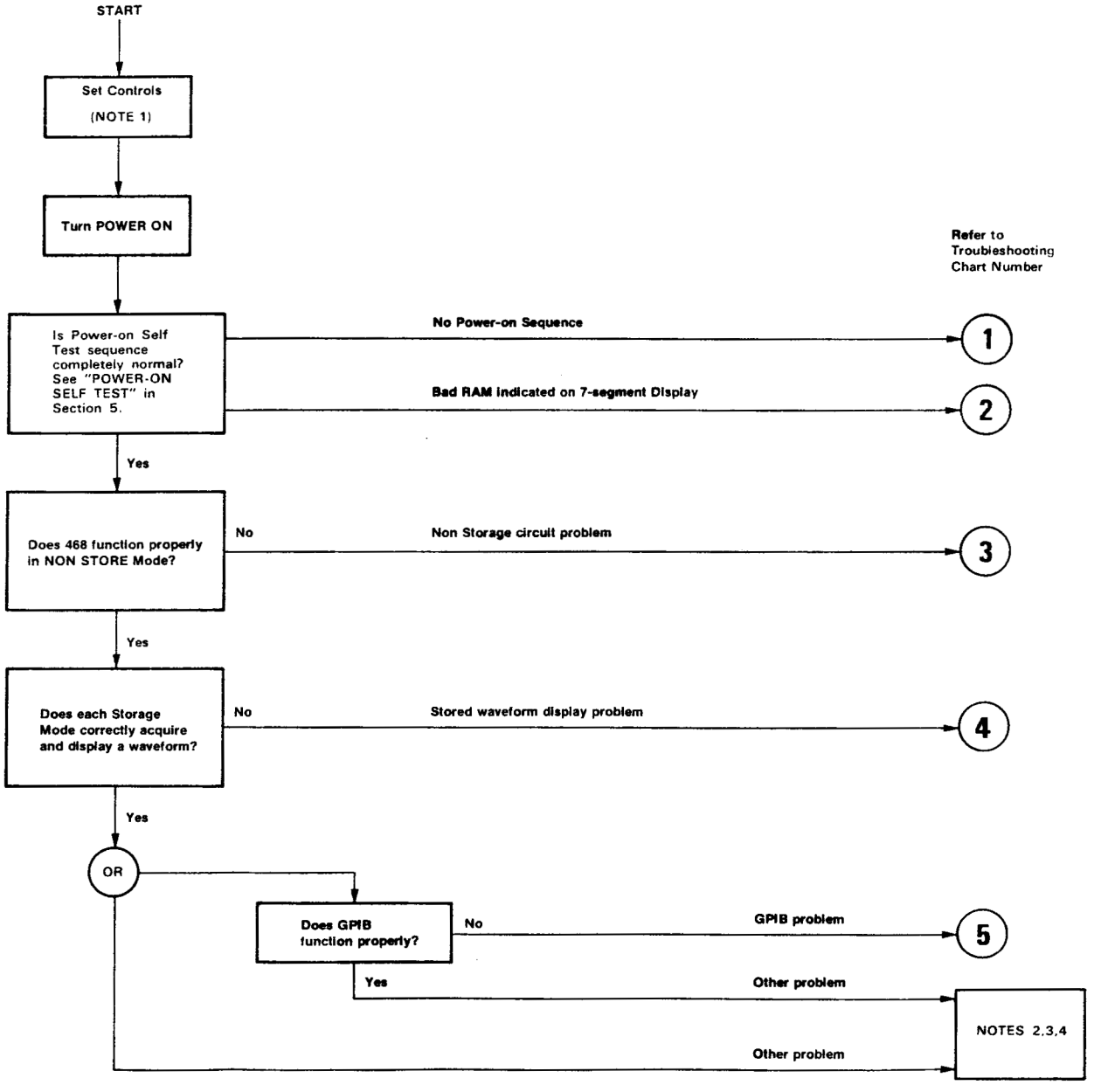
2. Isolate the nonstorage circuitry from the digital storage circuitry to allow checkout of conventional oscilloscope functions:
   a. Disconnect power and remove the oscilloscope cabinet (see "Maintenance", Secction 5).
   b. Disconnect P3008 from the A12 Trigger Generator Sweep Logic board (see Figure 8-17).
   c. Disconnect P483 from the A12 circuit board and connect a jumper between the two square-pin connectors on the board.
   d. Move P307 (at the rear of A14 Vertical Mode Switch board) to the Test Mode position (see Figure 8-15).
   e. Reapply power. This procedure enables the 468 to function as a conventional oscilloscope set up to chop between CH 1 and CH 2 inputs.
3. Perform the following sequence to check 468 operation:
   a. Verify operation in NON STORE mode (Troubleshooting Chart 3).
   b. Verify Microprocessor Kernel and AD0-AD7 Bus (Troubleshooting Chart 1).
   c. Perform the following Service Routines (see "SERVICE TEST", Section 5): Basic Display System, Switch Closure, Lamp Test.
   d. Remove the IC from U456 socket on A18 Memory board and insert Service Counter U356 in test socket. Verify digital data path (Troubleshooting Chart 4.3, NOTE 4).
   e. Reinstall U456.
4. If any Service Routine fails or if front panel controls have no effect or if any +5 V Check Signature fails, verify Microprocessor Kernel and AD0-AD7 Bus (Troubleshooting Chart 1).

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.

TROUBLESHOOTING CHART INDEX



3515-61

SPECIFIC NOTES

1. Digital Storage Power Supplies.

   +4.8 V to +5.2 V at TP 248 (Diagram 17 and Figure 8-22).

   +11.4 V to +12.6 V at TP285 (Diagram 16 and Figure 8-22).

   -11.4 V to -12.6 V at TP283 (Diagram 16 and Figure 8-22).

   -5.8 V to -6.2 V at TP518 (Diagram 19 and Figure 8-23).

2. Kernel Test Procedure.

   a. Set POWER switch OFF.

   b. Remove U452 and U558.

   c. Set POWER switch ON.

   d. Move P182 momentarily to the RESET position, then return it to the RUN position.

   e. Verify presence of the following signals and signatures in the order listed. See waveform illustrations on Diagram 18 in Volume II (numbers in parentheses).

      (1) +5 V on U364-40

      (2) 5-MHz Clock on U272-15 and U364-1 (135 and 136)

      (3) 2.5-MHz Clock on U364-37 (137)

      (4) 50 kHz on U440-1 (138)

      (5) 500 Hz on U364-7 (139)

      (6) PRDONE on U472-16 (140)

      (7) $\overline{\text{ALE}}$ on TP270 (141)

      (8) Waveform on TP477 (142)

      (9) $\overline{\text{RD}}$ on U364-32 (143)

      (10) $\overline{\text{WR}}$ on U364-31 (144)

      (11) Signal on U255-5 (145)

      (12) All Signatures of Kernel Test 1 and Kernel Test 2

      (13) All Signatures of ROML and ROMH (ensure that correct ROMs are installed)

      (14) U255-9 is not stuck either HI or LO

   f. SET POWER switch OFF.

   g. Reinstall U452 and U558.

3. Trap Test Procedure.

   a. Remove P262 momentarily, then reinstall it to cause a TRAP Interrupt to U364-6.

   b. Verify the +5-V signature.

   c. If +5-V signature is OK, then verify remaining Trap Test signatures on A21, A14, or A19, as applicable.

4. Service ROM Checksum Test.

   a. Set POWER switch OFF.

   b. Remove U464 (ROML) and install Service ROM at U565 socket.

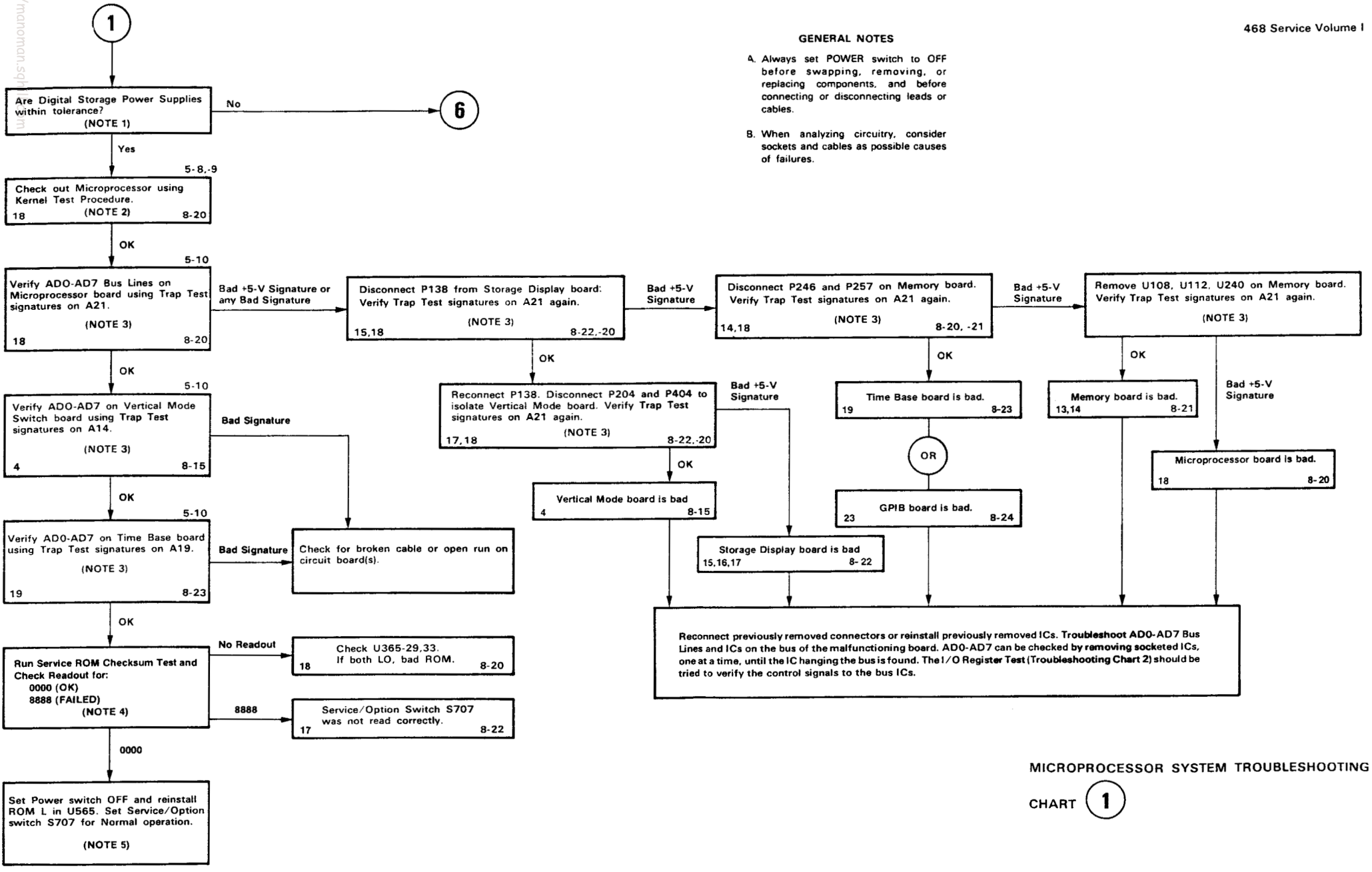
   c. Set Service ROM switch to 00000000 (all OPEN).

   d. Set POWER switch ON.

   e. Observe Readout Display for any one of the following indications:

      0000 (Test OK)
      8888 (Test Failed)
      No readout or any other readout (Test Failed)

5. Other service routines can be run at this time to verify other areas of the instrument. Service Switch 7 is ON for normal operation, and 8 is ON for GPIB. All others are "don't care".



GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.

MICROPROCESSOR SYSTEM TROUBLESHOOTING

CHART 1

3515-62

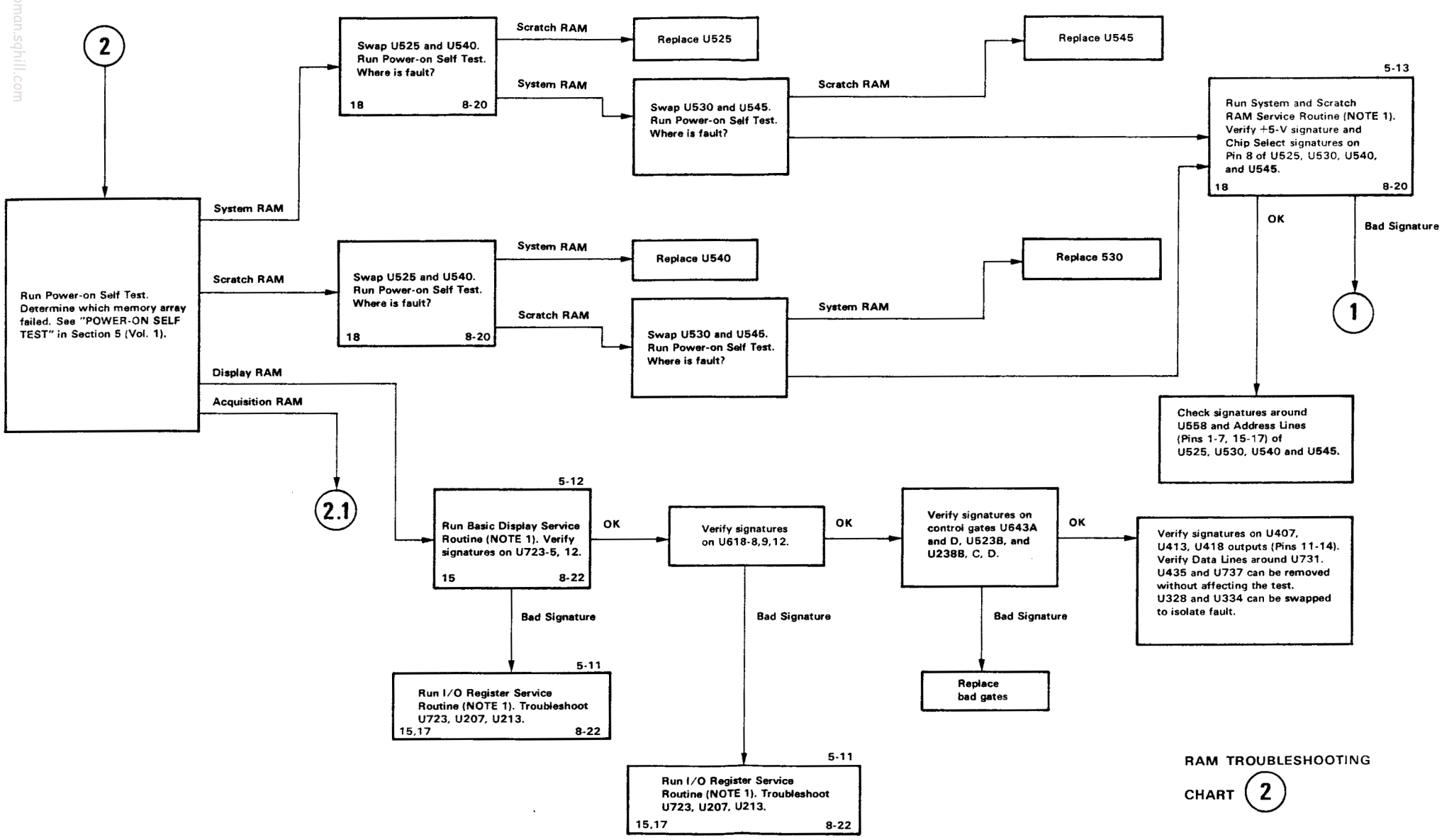
SPECIFIC NOTES

1. The procedures for running all Service Routine tests (using the Service ROM) are contained under "SERVICE TEST" in Section 5 of this volume.

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



RAM TROUBLESHOOTING CHART 2

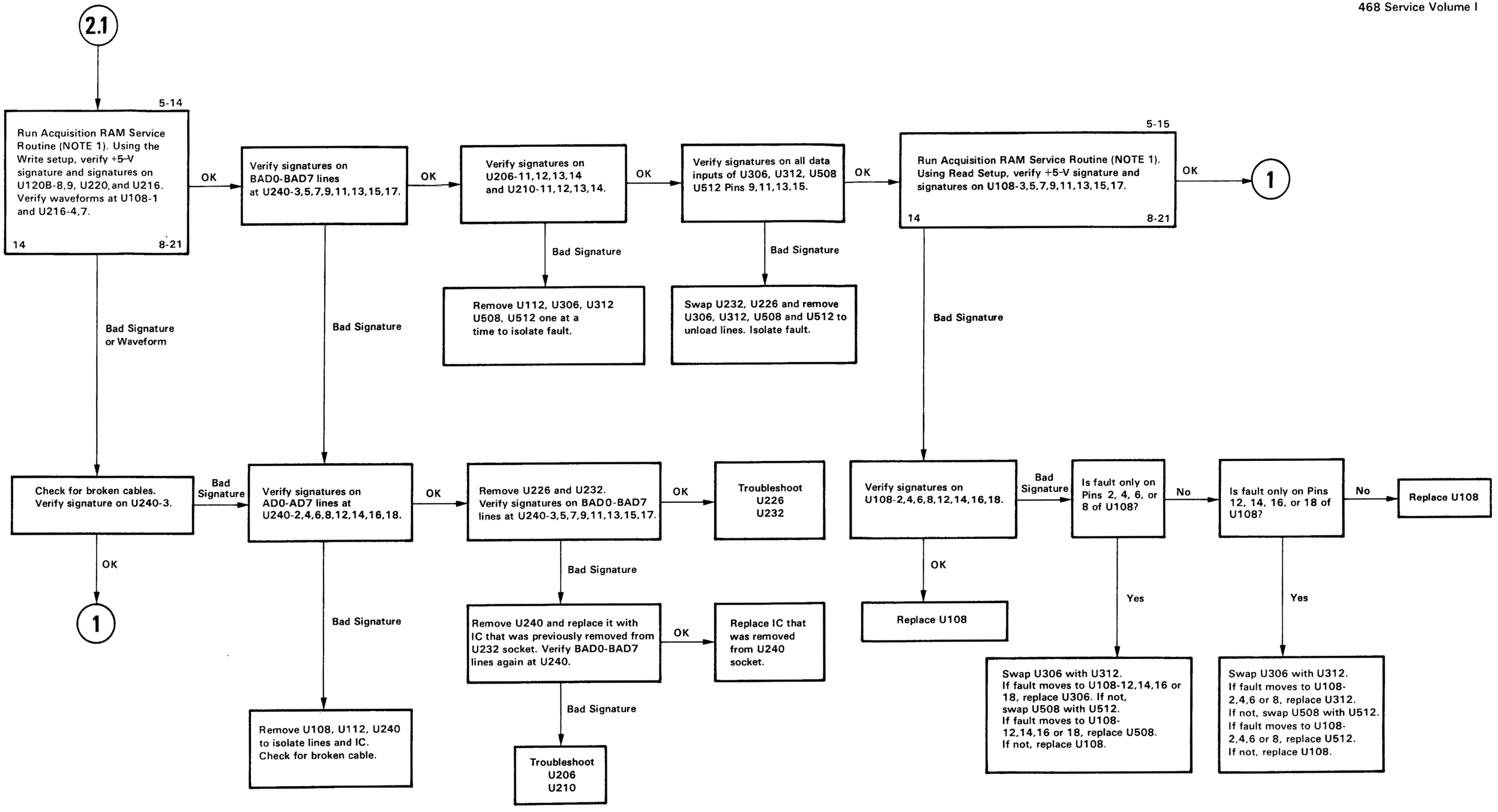
SPECIFIC NOTES

1. The procedures for running all Service Routine tests (using the Service ROM) are contained under "SERVICE TEST" in Section 5 of this volume.

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



RAM TROUBLESHOOTING

CHART 2.1

SPECIFIC NOTES

1. Isolate the nonstorage circuitry from the digital storage circuitry to allow checkout of conventional oscilloscope functions:
   a. Disconnect power and remove the oscilloscope cabinet (see "Maintenance", Section 5, Vol. I).
   b. Disconnect P3008 from the A12 Trigger Generator Sweep Logic board (see Figure 8-17).
   c. Disconnect P483 from the A12 circuit board and connect a jumper between the two square-pin connectors on the board.
   d. Move P307 (at the rear of A14 Vertical Mode Switch board) to the Test Mode position (see Figure 8-15).
   e. Reapply power. This procedure enables the 468 to function as a conventional oscilloscope set up to chop between CH1 and CH2 inputs.

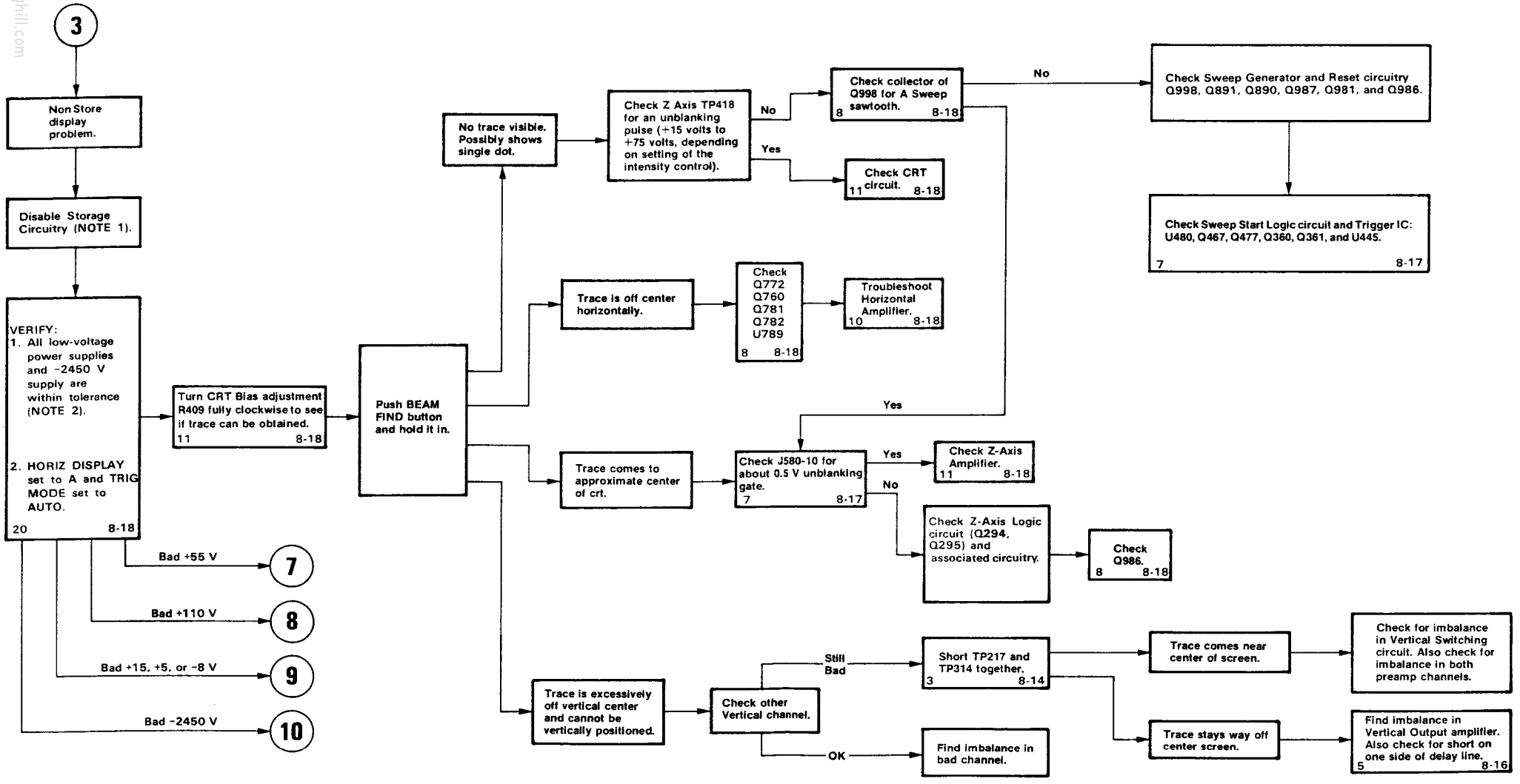
2. Verify the following voltages at A15 Interface board (Diagram 20 and Figure 8-18):

   a. −8 V at TP740
   b. +5 V at TP638
   c. +15 V at TP639
   d. +55 V at TP637
   e. +110 V at TP642.
   f. -2450V at TP328.

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



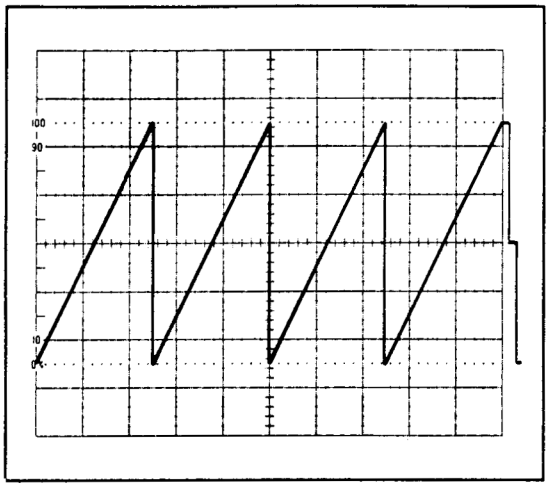
NONSTORAGE FUNCTIONS TROUBLESHOOTING

CHART 3

SPECIFIC NOTES

1. The procedures for running all Service Routine tests (using the Service ROM) are contained under "SERVICE TEST" in Section 5 of this volume.

2.

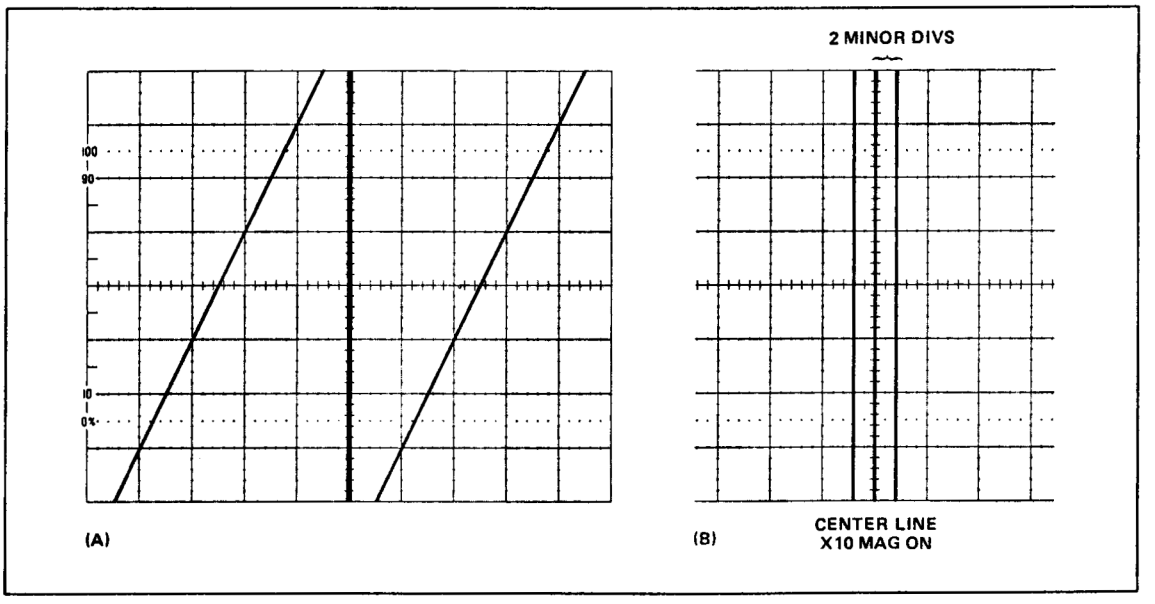


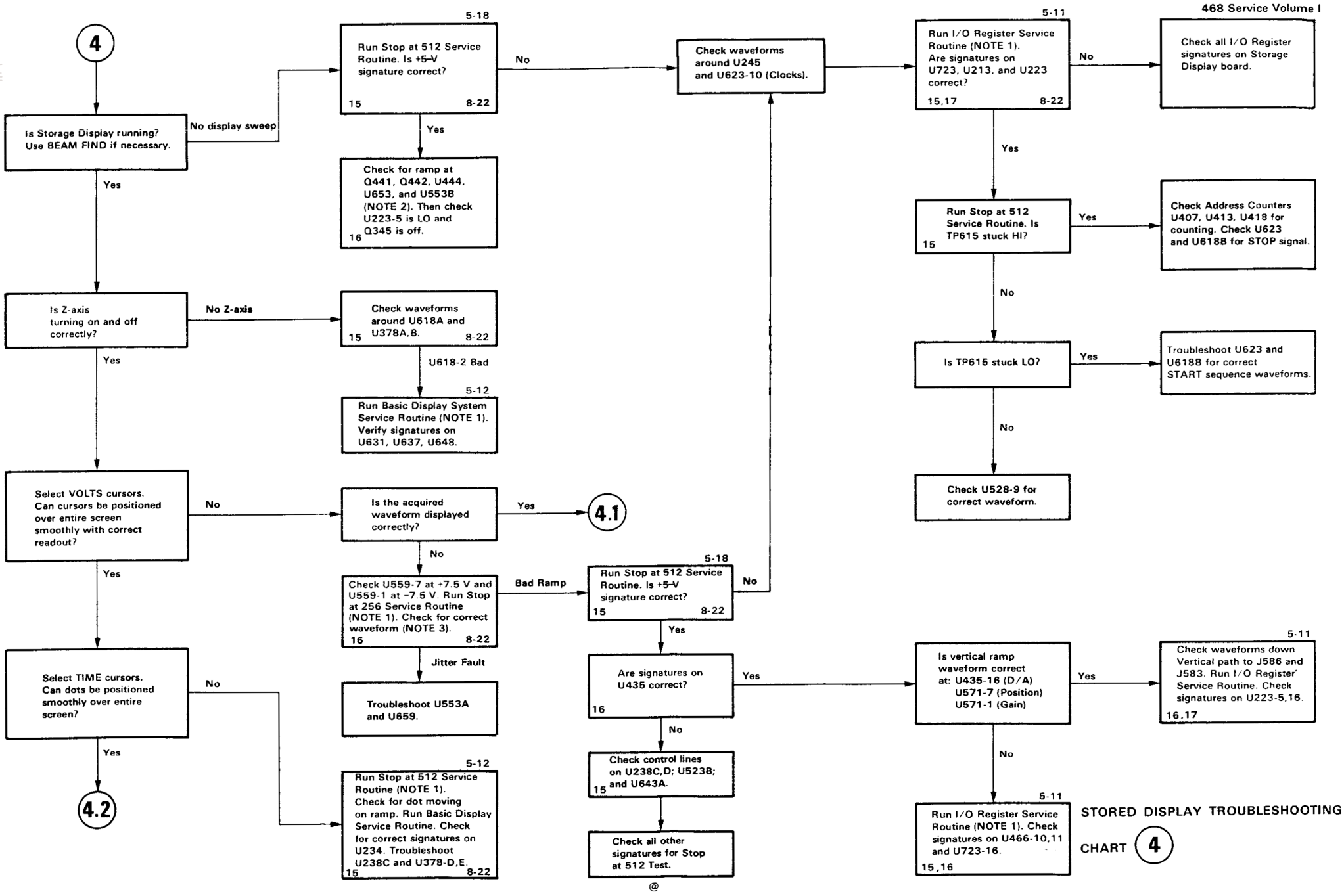
GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.

3.





STORED DISPLAY TROUBLESHOOTING

CHART 4

SPECIFIC NOTES

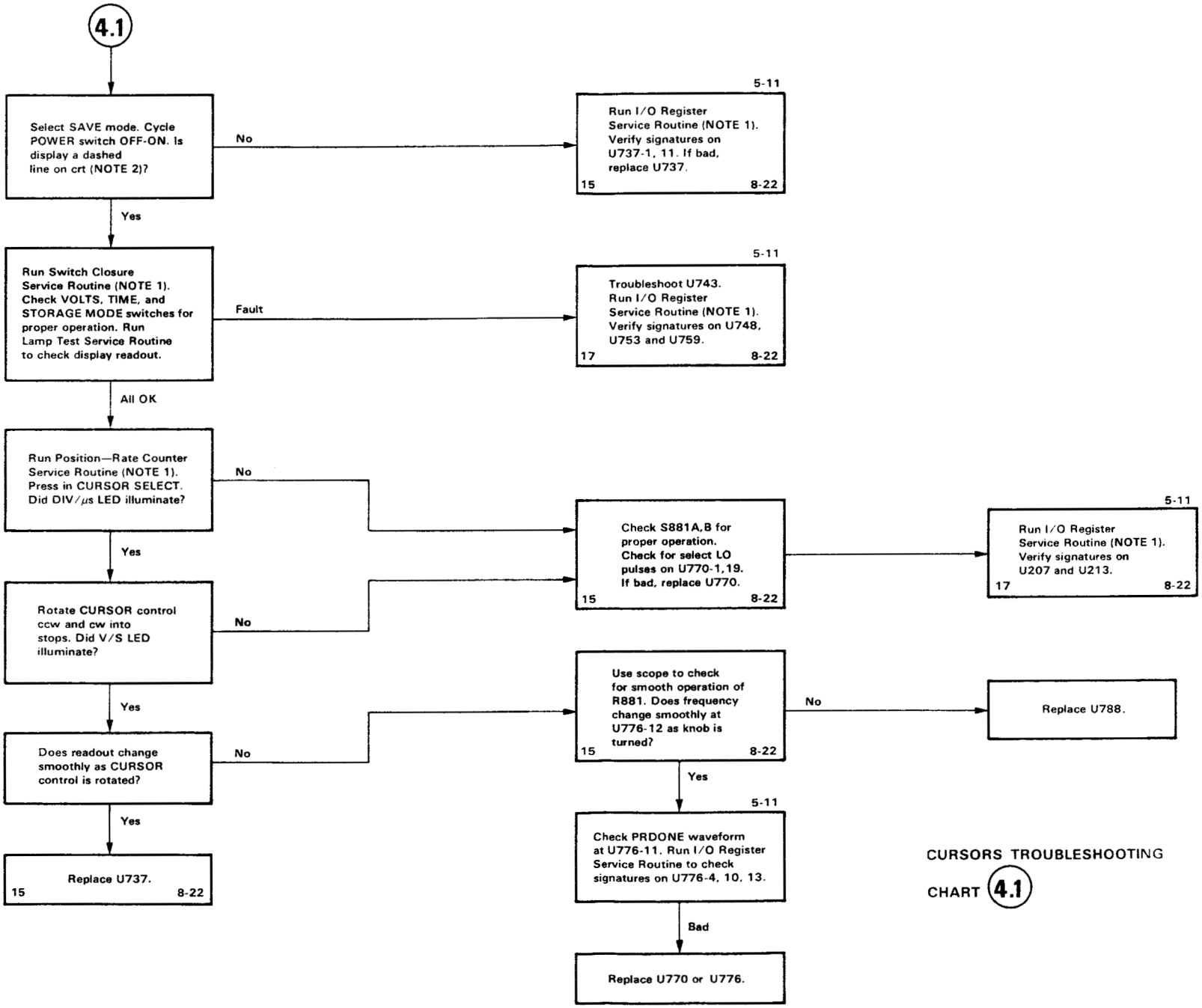
1. The procedures for running all Service Routine tests (using the Service ROM) are contained under "SERVICE TEST" in Section 5 of this volume.

2. Adjust R345 on Storage Display board (Diagram 16) to vertically center trace.

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



CURSORS TROUBLESHOOTING CHART 4.1

3515-66

SPECIFIC NOTES

1. The procedures for running all Service Routine tests (using the Service ROM) are contained under "SERVICE TEST" in Section 5, Volume 1.

2. Use the following table to determine Sample Clock periods at TP446 TP210 and U120-13.

Table A

TIME/DIV Switch Setting	Sample Clock Periods		
	TP446 (Diagram 14)	TP210 (Diagram 19)	U120-13 (Diagram 19)
0.02—2 μs	40 ns	40 ns	Not Running
5 μs	100 ns	100 ns	Not Running
10 μs	200 ns	200 ns	Not Running
20 μs	400 ns	40 ns	Not Running
50 μs	1 μs	100 ns	Not Running
0.1 ms	2 μs	200 ns	Not Running
0.2 ms	4 μs	400 ns	400 ns
0.5 ms	10 μs	1 μs	1 μs
1 ms	20 μs	2 μs	2 μs
2 ms	40 μs	4 μs	4 μs
5 ms	100 μs	10 μs	10 μs
10 ms	200 μs	20 μs	20 μs
20 ms	400 μs	40 μs	40 μs
50 ms	1 ms	100 μs	100 μs
0.1 s	2 ms	200 μs	200 μs
0.2 s	4 ms	400 μs	400 μs
0.5 s	10 ms	1 ms	1 ms
1 s	20 ms	2 ms	2 ms
2 s	40 ms	4 ms	4 ms
5 s	100 ms	10 ms	10 ms

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.

3. Use the following table to determine Sample Clock periods and frequencies at U120-10, 11 and 12.

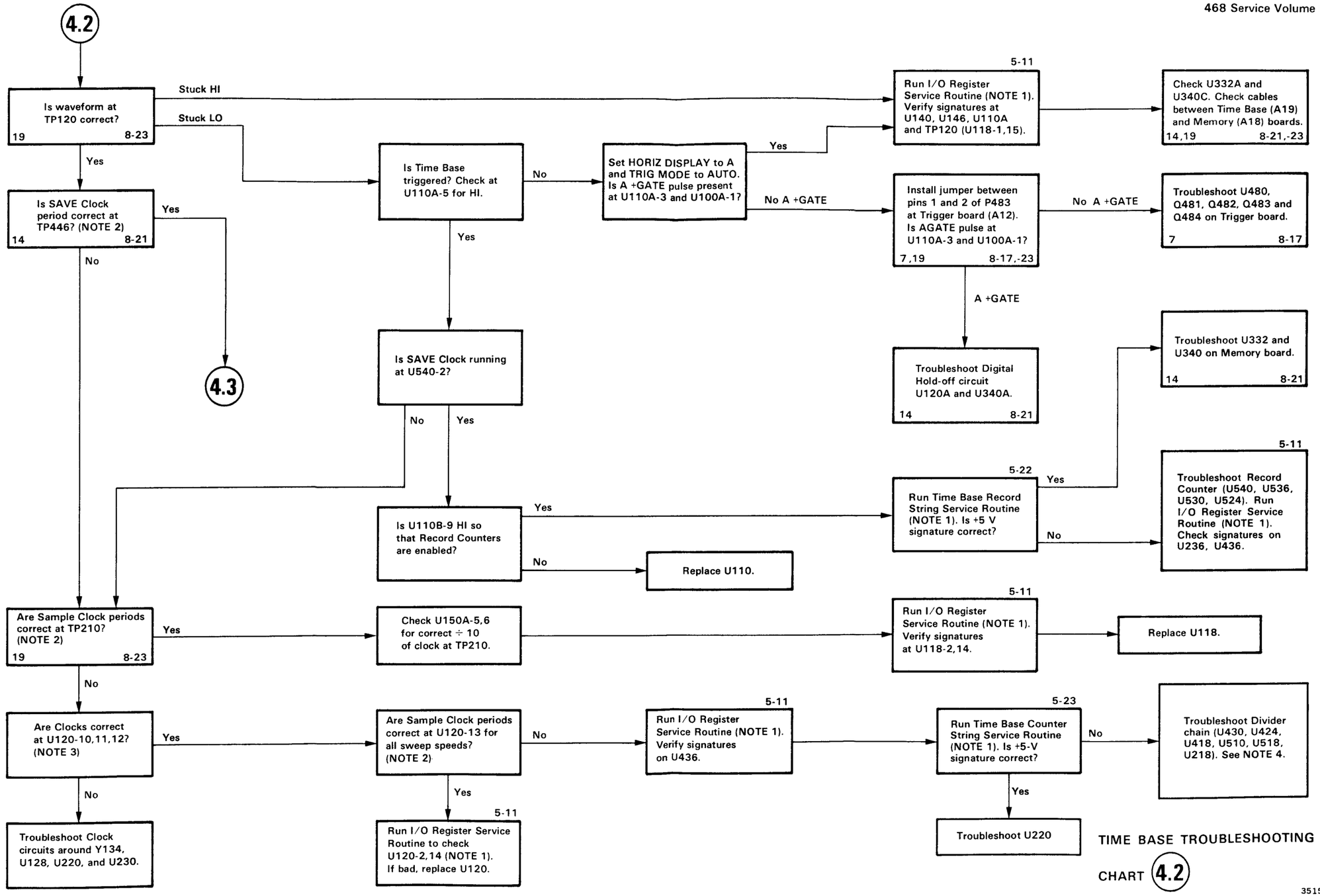
Table B

Test Point	Sample Clocks	
	Period	Frequency
U120-10	40 ns	25 MHz
U120-11	100 ns	10 MHz
U120-12	200 ns	5 MHz

4. Use the following table to determine Divider Chain output periods. When observing waveforms, disregard the characteristic glitch associated with synchronous counters.

Table C

Test Point	Period	Duty Cycle (%)
U430-15	400 ns	50
U424-15	4 μs	10
U418-15	40 μs	10
U510-15	400 μs	10
U518-15	4 ms	10



TIME BASE TROUBLESHOOTING

CHART 4.2

3515-67

SPECIFIC NOTES

1. The procedures for running all Service Routine tests (using the Service ROM) are contained under "SERVICE TEST" in Section 5 of this volume.

2. Jitter Correction Check. Perform the following procedure to check jitter correction:

   a. Set controls:

VERT MODE	CH 1
A TIME/DIV	20 μs
CH 1 VOLTS/DIV	5 mV
STORAGE MODE	NORM
HORIZ DISPLAY	A
X10 MAG	On (button in)
TRIGGER LEVEL	As necessary for a stable, triggered display.

   b. Connect a sine-wave generator to the CH 1 input via a 50 Ω bnc cable and a 50 Ω bnc termination. Set the generator for a 50 kHz, 6-division display.

   c. Observe display jitter. Is the display stable, or is it shifting continually over 0.4 of a division?

   d. Change the A TIME/DIV switch to 0.02 μs and turn off the X10 MAG function (button out).

   e. Set the generator for a 5 MHz, 6-division display.

   f. Observe the display jitter. Is the display stable, or is it shifting continually over 4-divisions? (An occasional shift should be expected, see Theory of Operation.)

3. Vertical Signal Path Check. Perform the following procedure to check the vertical Signal path.

   a. Set controls:

VERT MODE	CH 1
VOLTS/DIV (both)	5 mV

   b. Connect a sine-wave generator to the CH 1 input via a 50 Ω bnc cable and a 50 Ω bnc termination. Set the generator for a 50 kHz, 6-division display.

   c. Check signal at TP 464 for ≈1.2 V p-p, centered at −1 V.

   d. Move the test signal to CH 2 and set VERT MODE switch to CH 2 only.

   e. Check signal at TP464 for ≈1.2 V p-p, centered at −1 V.

4. After Service Counter is installed at U456, obtain Test Ramp display as follows:

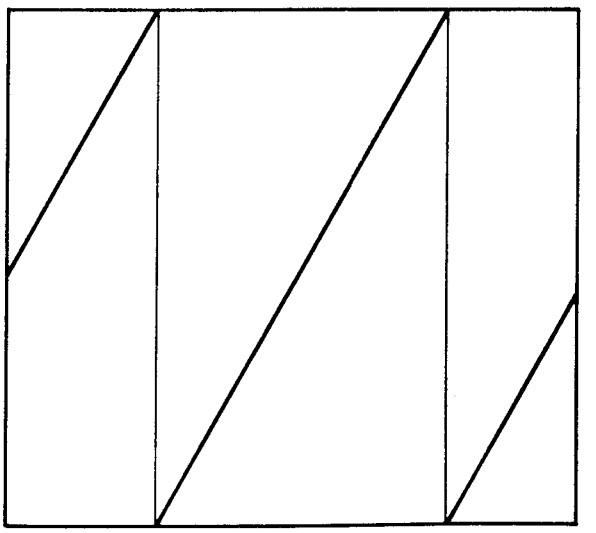
   a. Set controls:

STORAGE MODE	NORM
TIME/DIV	10 μs
TRIGGER SOURCE	LINE

   b. Set POWER switch to ON.

   c. Press and release SINGL SWP push button.

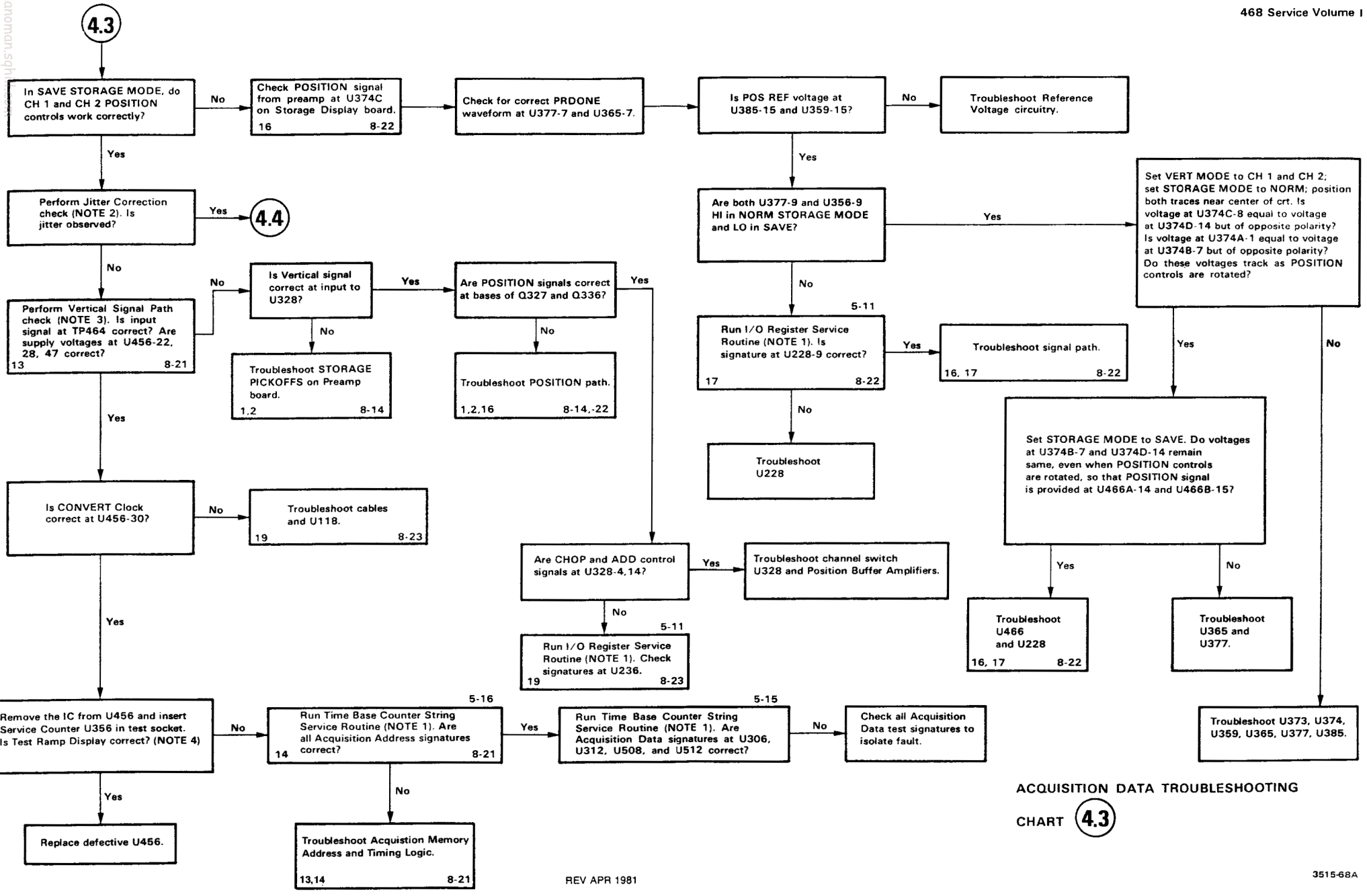
   d. Observe Test Ramp. Test Ramp display consists of two complete ramps. To shift ramp through the display, press in and release SINGL SWP push button.



GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.

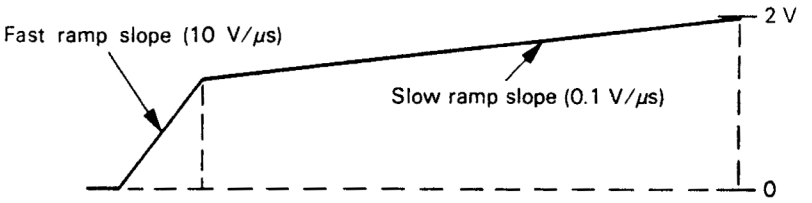


ACQUISITION DATA TROUBLESHOOTING CHART 4.3

SPECIFIC NOTES

1. The procedures for running all Service Routine tests (using the Service ROM) are contained under "SERVICE TEST" in Section 5, Volume 1.

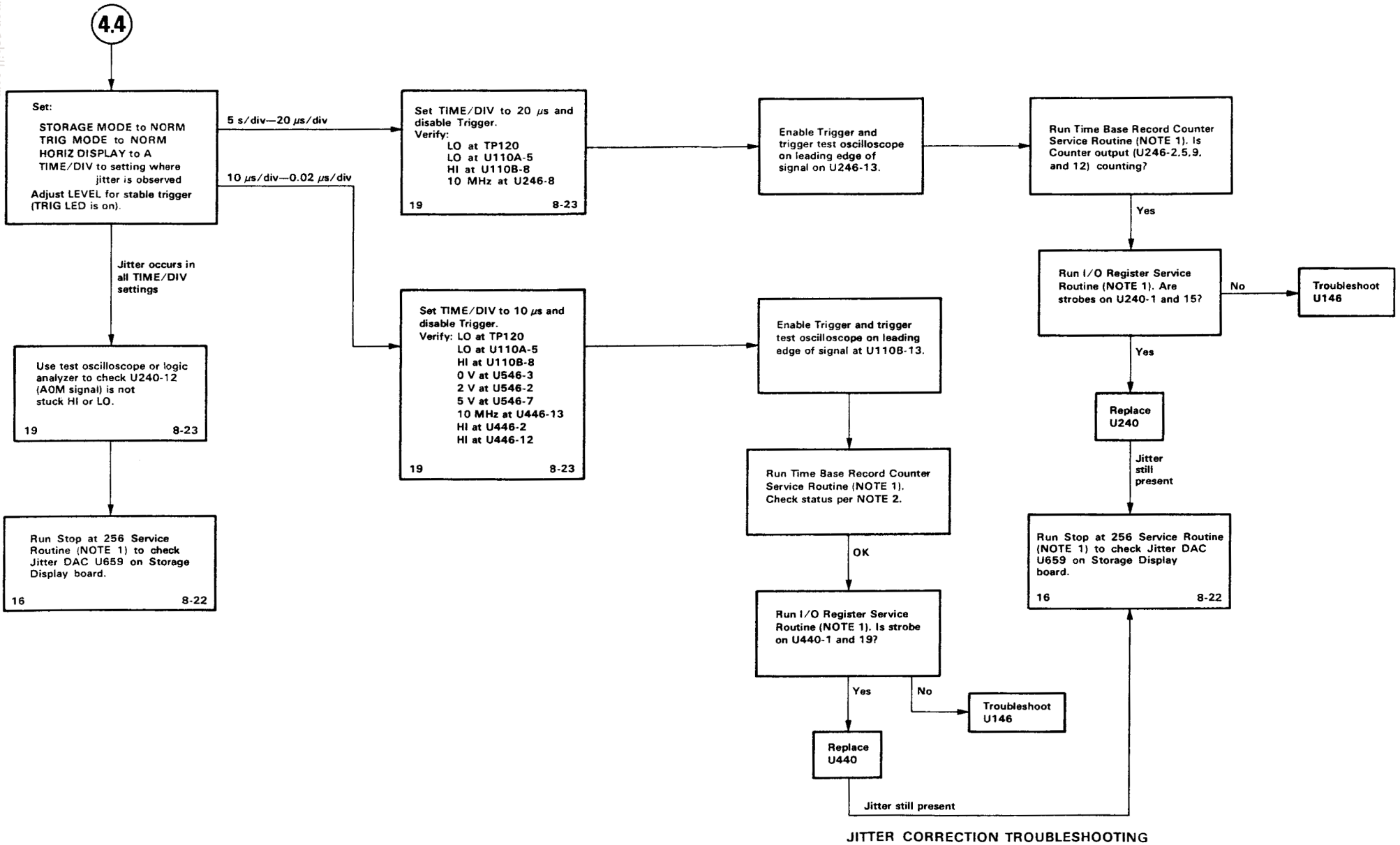
2. Signal at U546-3 should ramp fast then slow (up to 2 V in about 20 μs). Outputs of U446 should be counting during slow ramp. When ramp reaches 2 V, U546-7 switches to turn off clock at U218A.



GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



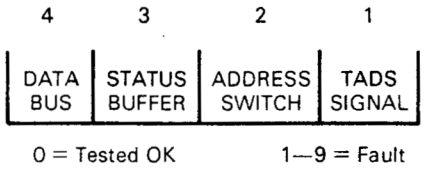
JITTER CORRECTION TROUBLESHOOTING CHART 4.4

3515-69

SPECIFIC NOTES

1. The procedures for running all Service Routine tests (using the Service ROM) are contained under "SERVICE TEST" in Section 5 of this volume.

2. 7-SEGMENT LED READOUT

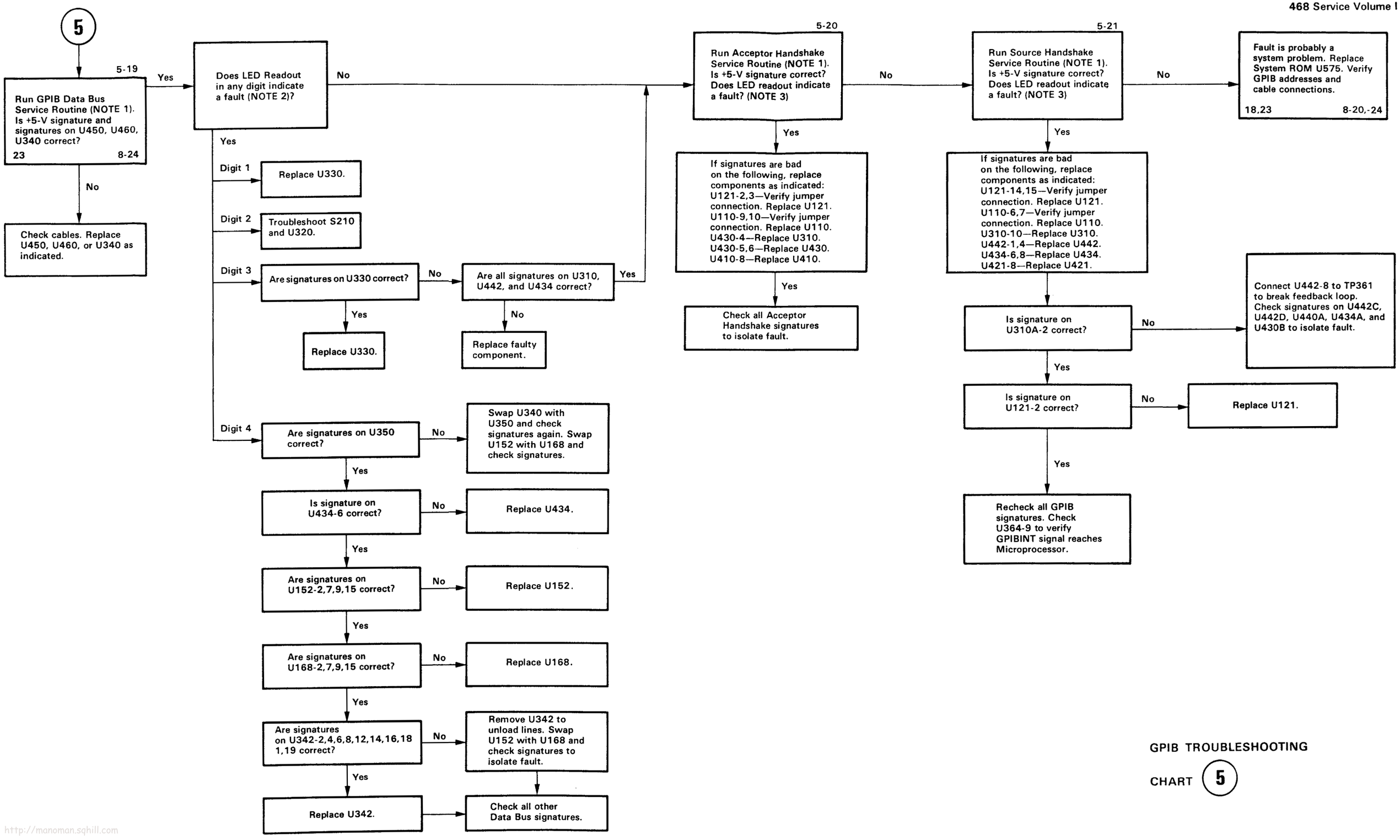


3. A fault is detected if Digit 1 of the Readout is any number except 0. If digits 2, 3, and 4 are not 0, the Service Routine is not running correctly.

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



GPIB TROUBLESHOOTING

CHART 5

SPECIFIC NOTES

1. Digital Storage Power Supplies.

   +4.8 V to +5.2 V at TP248 (Diagram 17 and Figure 8-22).

   +11.4 V to +12.6 V at TP285 (Diagram 16 and Figure 8-22).

   -11.4 V to -12.6 V at TP283 (Diagram 16 and Figure 8-22).

   -5.8 V to -6.2 V at TP518 (Diagram 19 and Figure 8-23).

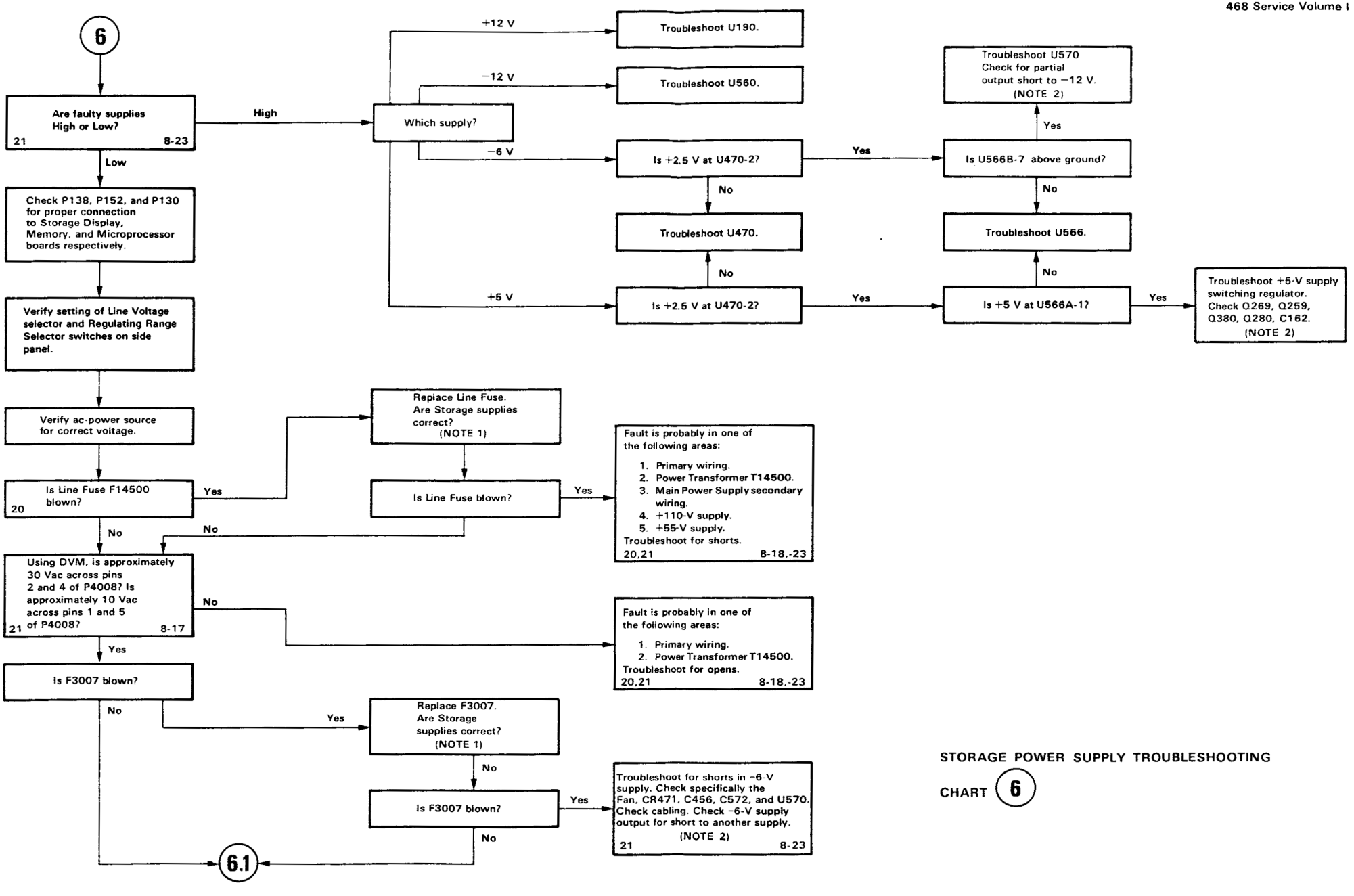
2. The following nominal values of dc resistance to ground with the 468 POWER Switch OFF should be measured with a TEKTRONIX DM 501 Digital Multimeter or equivalent.

Supply	Dc Resistance to Ground (nominal)	Measured at
+5 V	80 Ω	TP315
-6 V	500 Ω	TP518
+12 V	250 Ω	TP148
-12 V	350 Ω	TP520

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



STORAGE POWER SUPPLY TROUBLESHOOTING

CHART 6

SPECIFIC NOTES

1. Digital Storage Power Supplies.

   +4.8 V to +5.2 V at TP248 (Diagram 17 and Figure 8-22).

   +11.4 V to +12.6 V at TP285 (Diagram 16 and Figure 8-22).

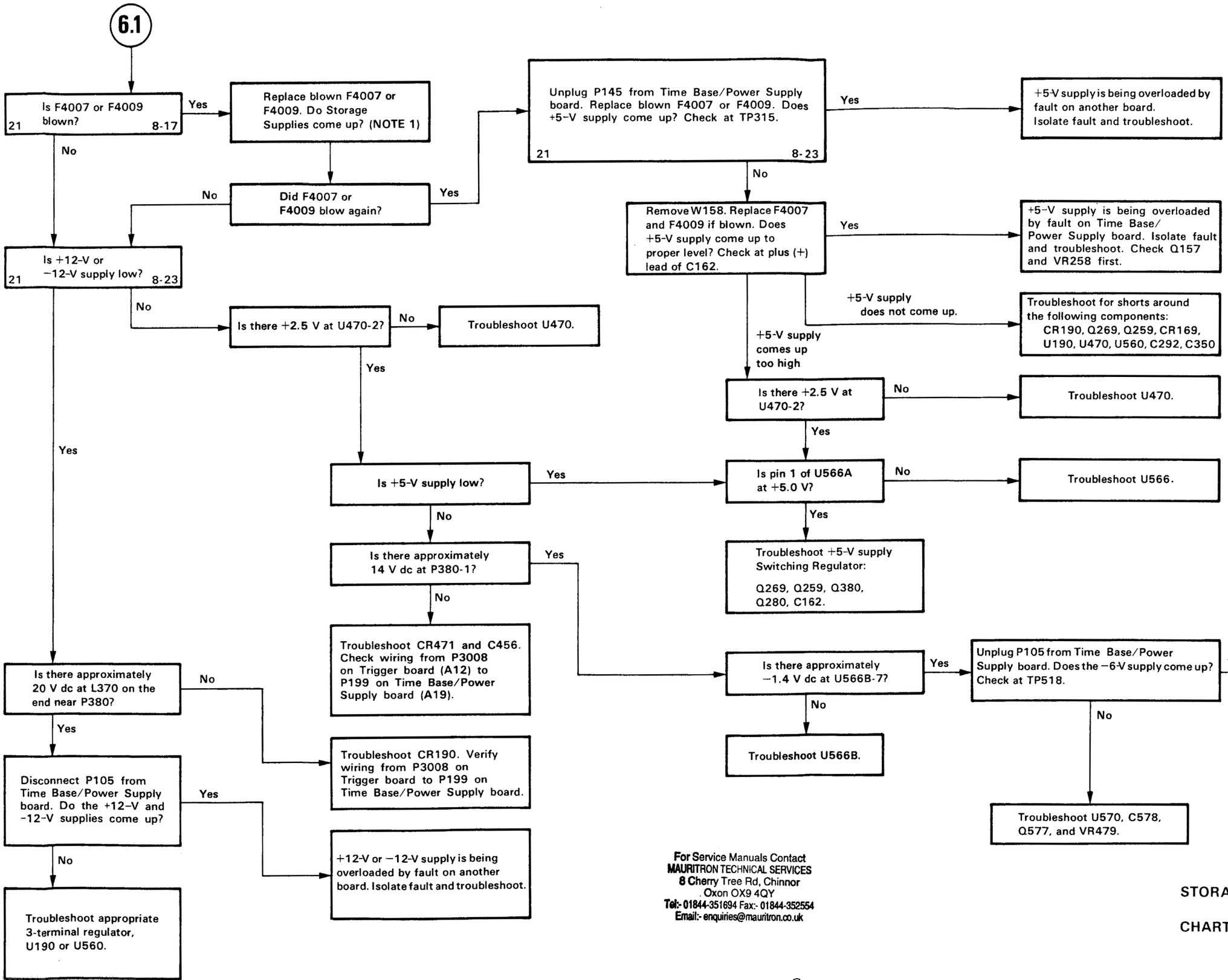
   -11.4 V to -12.6 V at TP283 (Diagram 16 and Figure 8-22).

   -5.8 V to -6.2 V at TP518 (Diagram 19 and Figure 8-23).

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



STORAGE POWER SUPPLY TROUBLESHOOTING

CHART 6.1

POWER SUPPLY ISOLATION PROCEDURE

The following procedure is used as an aid in localizing the area in which loading of a power supply occurs. If the power supply comes up after isolating a circuit, it is very probable the problem is in that circuit. This can sometimes, however, lead to erroneous conclusions as a supply may pass through one circuit to another circuit. For instance, the +5 volt supply enters the Timing Board through P555-4. It then passes through the timing switch (in the X-Y position only) and J885-9 to CR486 in the Horizontal Amplifier circuit. From P885-9 it also passes through P970-4 to the sweep control IC on the Trigger board. Watch for these types of conditions when trying to localize a loading problem.

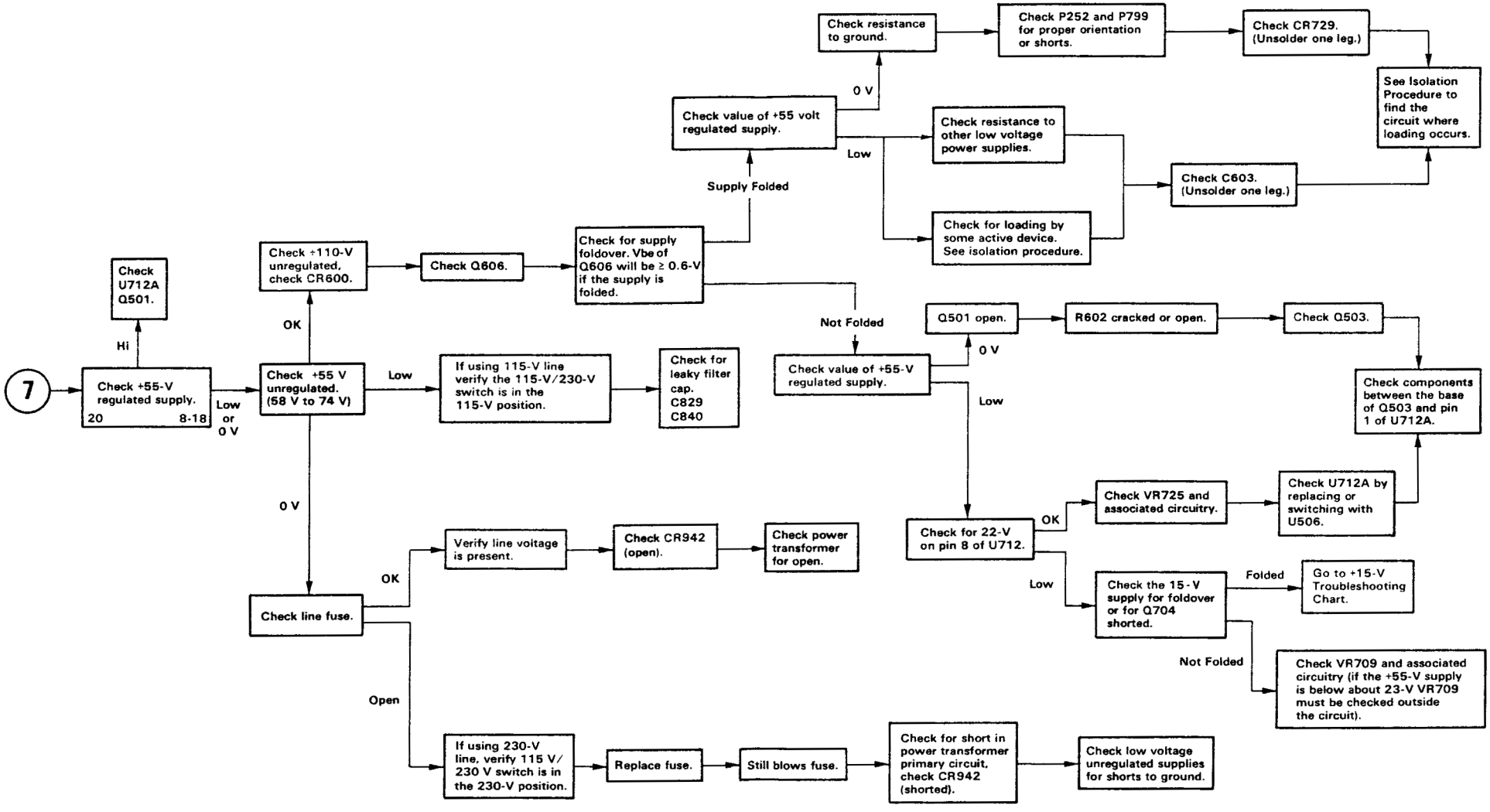
+55-V Supply

1. Unsolder service jumper W880 from the Interface board (see Figure 8-18). This isolates the Timing board and the Holdoff potentiometer.
2. Pull P252 from the Interface board. This isolates the Vertical Output Amplifier board.
3. To isolate the Trigger board from the +55-V supply, it is necessary to remove the Trigger board from the instrument. The +55-V supply connects to the Trigger board through P970-9.
4. Unsolder one end of R877 and R850 on the Interface board (see Figure 8-18). This isolates the A & B Sweep Generator circuitry.
5. Unsolder one end of R387 and R391 from the Interface board (see Figure 8-18). This isolates the Calibrator circuitry.
6. If the +55-V supply is still loaded, suspect the CRT circuitry, or the Horizontal Amplifier circuitry. Refer to Diagram 10 to locate +55-V connections to the Horizontal Amplifier circuitry and to Diagram 11 to locate +55-V connections to the CRT circuity.

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



+55 V SUPPLY TROUBLESHOOTING

CHART 7

POWER SUPPLY ISOLATION PROCEDURE

The following procedure is used as an aid in localizing the area in which loading of a power supply occurs. If the power supply comes up after isolating a circuit, it is very probable the problem is in that circuit. This can sometimes, however, lead to erroneous conclusions as a supply may pass through one circuit to another circuit. For instance, the +5 volt supply enters the Timing Board through P555-4. It then passes through the timing switch (in the X-Y position only) and J885-9 to CR486 in the Horizontal Amplifier circuit. From P885-9 it also passes through P970-4 to the sweep control IC on the Trigger board. Watch for these types of conditions when trying to localize a loading problem.

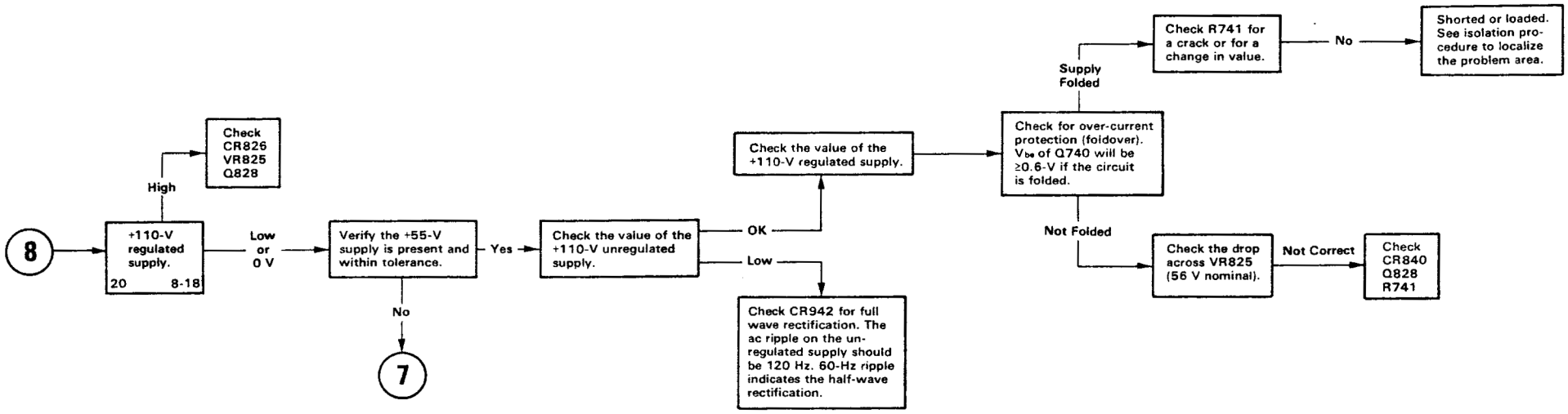
+110-V Supply

1. Unsolder one end of VR643, R438, and R647 (see Figure 8-18). This isolates the Horizontal Amplifier circuit.
2. Unsolder one end of CR727 and R633 (see Figure 8-18). If loading still exists, check adjustment of R267 (Geometry) and R377 (ASTIG). If either does not adjust and an internal short is suspected, it will be necessary to remove R267 and R377 to isolate the CRT circuitry (Z-Axis Amplifier).

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



+110 V SUPPLY TROUBLESHOOTING

CHART 8

POWER SUPPLY ISOLATION PROCEDURE

The following procedure is used as an aid in localizing the area in which loading of a power supply occurs. If the power supply comes up after isolating a circuit, it is very probable the problem is in that circuit. This can sometimes, however, lead to erroneous conclusions as a supply may pass through one circuit to another circuit. For instance, the +5-V supply enters the Timing Board through P555-4. It then passes through the timing switch (in the X-Y position only) and J885-9 to CR486 in the Horizontal Amplifier circuit. From P885-9 it also passes through P970-4 to the sweep control IC on the Trigger board. Watch for these types of conditions when trying to localize a loading problem.

+15-V Supply

1. Pull P154 from the Interface board. This isolates the Vertical Preamplifier board.
2. Pull P151 from the Interface board. This isolates the Vertical Mode board.
3. Pull P252 from the Interface board. This isolates the Vertical Output board.
4. Pull P699 from the Interface board. This isolates the Horizontal POSITION potentiometers.
5. Unsolder service jumper W2006 on the Trigger board (see Figure 8-17). This isolates the Trigger board.
6. Unsolder service jumper W780 from the Interface board (see Figure 8-18). This isolates the Timing board.
7. Unsolder service jumper W747 on the Interface board (see Figure 8-18). This isolates the A & B Sweep Generator circuitry and the Horizontal Amplifier circuitry.
8. If the +15-V supply is still loaded, suspect the CRT circuitry (Z-Axis Amplifier). Refer to Diagram 11 to locate the +15-V connection to the CRT circuity.

+5-V Supply

1. Pull P154 from the Interface board. This isolates the Vertical Preamplifier board.
2. Pull P151 from the Interface board. This isolates the Vertical Mode board.
3. Pull P252 from the Interface board. This isolates the Vertical Output board.
4. Pull P799 from the Interface board. This isolates the HOLDOFF potentiometer.
5. Unsolder service jumper W866 from the Interface board (see Figure 8-18). This isolates the Timing board.
6. Unsolder service jumper W2003 from the Trigger board (see figure 8-17). This isolates the A & B Sweep Generator circuitry and part of the Horizontal Amplifier circuitry.
7. Unsolder service jumper W746 from the Interface board (see Figure 8-18). This isolates the A & B Sweep Generator circuitry and part of the Horizontal Amplifier circuitry.
8. Unsolder one end of R453 and R554 from the Interface board (see Figure 8-18). This isolates the rest of the Horizontal Amplifier circuity.
9. Unsolder L494 from the Interface board (see Figure 8-18). This isolates the Calibrator circuitry.
10. If the +5-V supply is still loaded, the CRT circuitry should be suspected. Refer to Diagram 11 to locate the +5-V connections to the CRT circuitry.

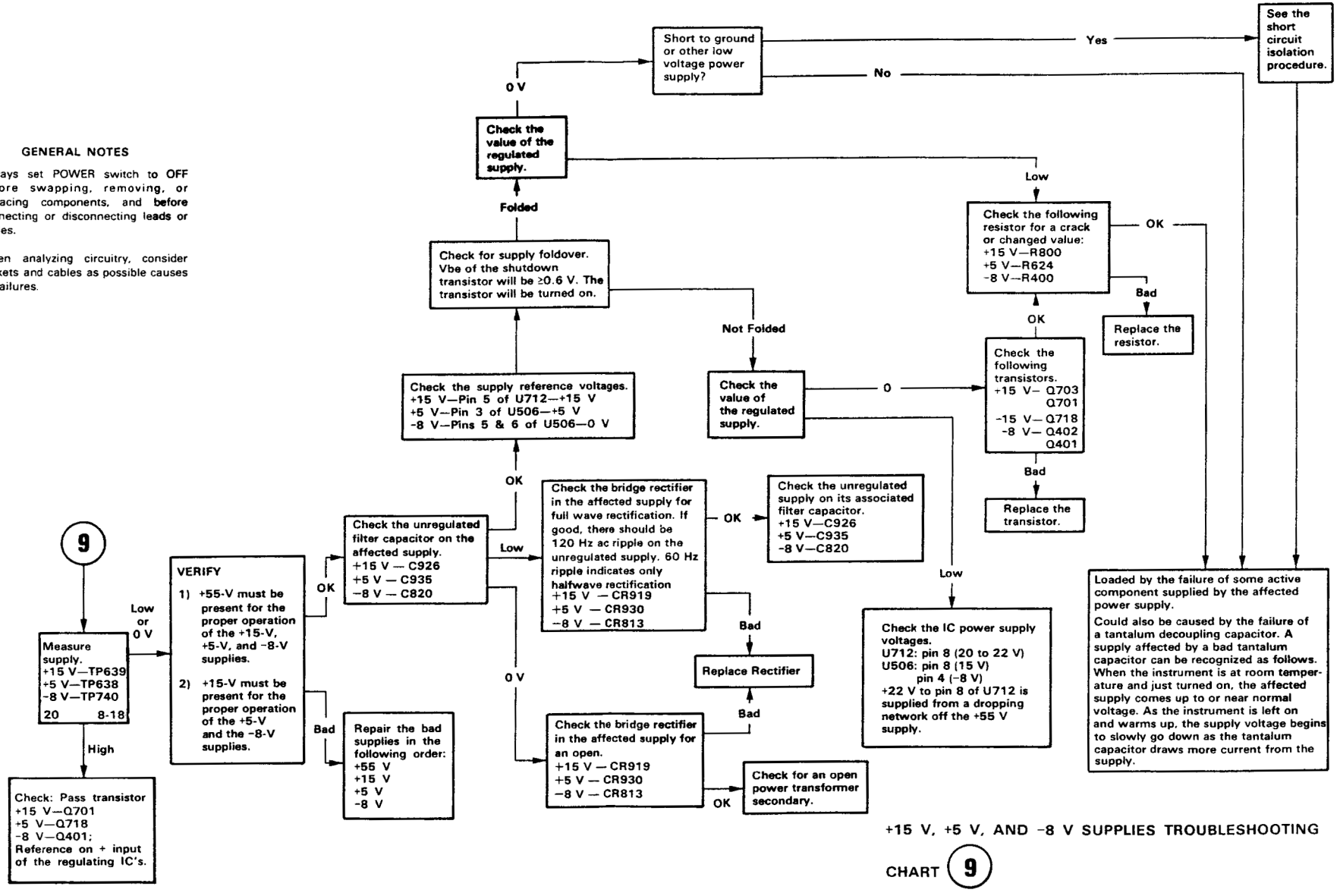
-8-V Supply

1. Pull P154 from the Interface board. This isolates the Vertical Preamplifier board.
2. Pull P151 from the Interface board. This isolates the Vertical Mode board.
3. Pull P252 from the Interface board. This isolates the Vertical Output Amplifier board.
4. Pull P699 from the Interface board. This isolates the Horizontal POSITION and B INTENSITY potentiometers.
5. Unsolder service jumper W2007 from the Trigger board to isolate part of the Trigger board. Unsolder one end of R509 from the Trigger board to isolate the rest of the Trigger board (see Figure 8-17).
6. Unsolder service jumper W849 from the Interface board (see Figure 8-18). This isolates the Timing board, A & B Sweep Generator circuitry, and part of the Horizontal Amplifier circuitry. It will also completely remove the -8-V from the Trigger board if step 5 is not done.
7. Check C848 on the Interface board for a short or leakage (see Figure 8-18).
8. If the -8-V supply is still loaded, suspect the CRT circuitry (Z-Axis Amplifer), or the Horizontal Amplifier circuitry. Refer to Diagram 10 for the -8-V connections to the Horizontal Amplifier and to Diagram 11 for the -8-V connections to the CRT circuitry.

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



+15 V, +5 V, AND -8 V SUPPLIES TROUBLESHOOTING

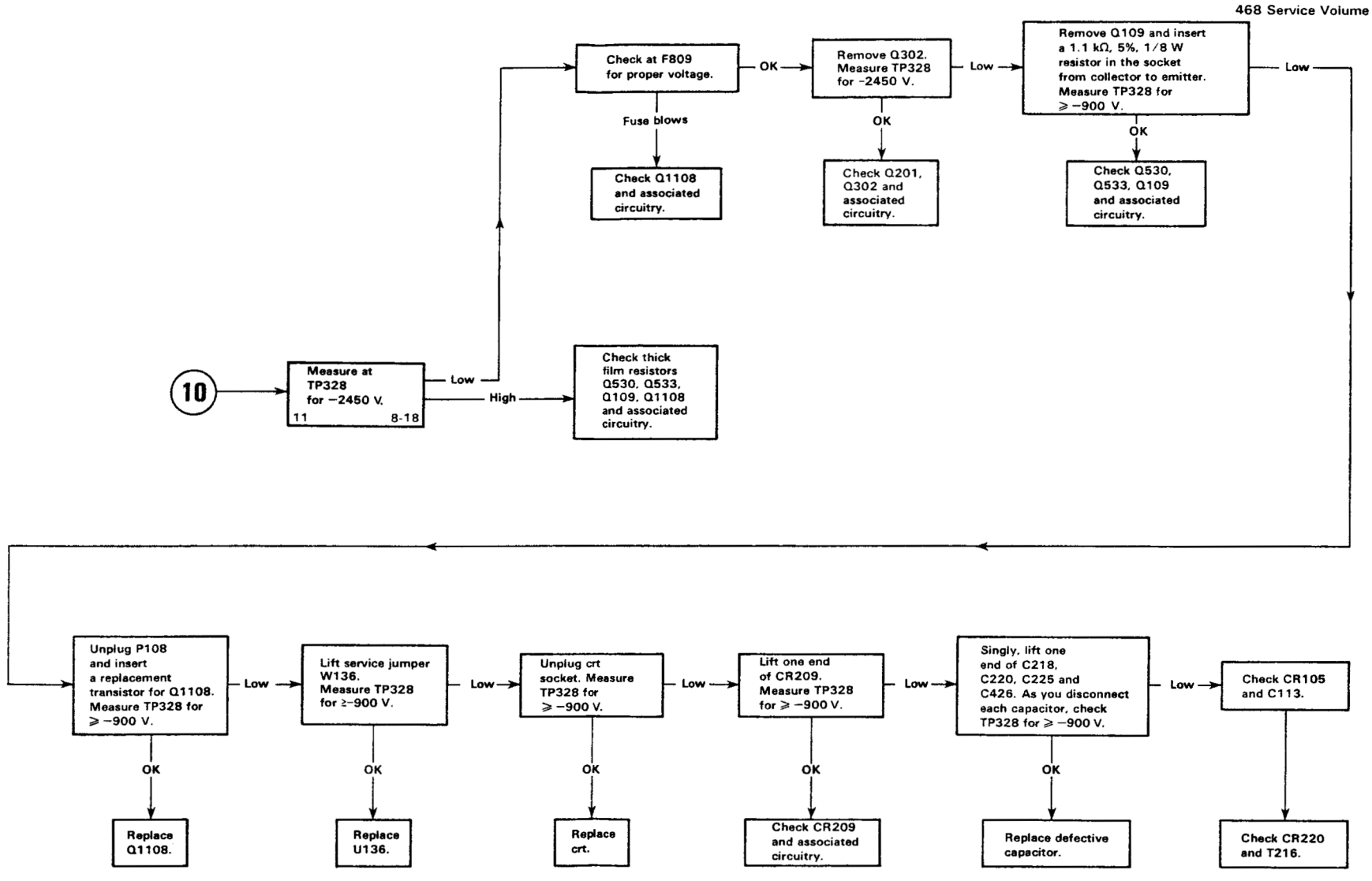
CHART 9

(2757-55) 3515-56

GENERAL NOTES

A. Always set POWER switch to OFF before swapping, removing, or replacing components, and before connecting or disconnecting leads or cables.

B. When analyzing circuitry, consider sockets and cables as possible causes of failures.



−2450 V SUPPLY TROUBLESHOOTING

CHART 10

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

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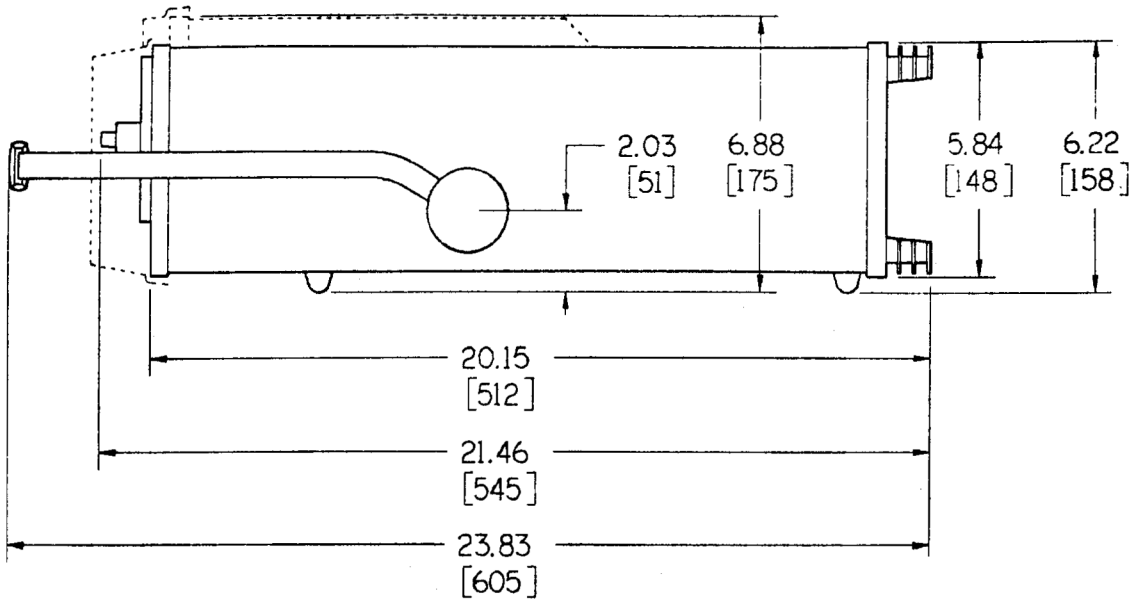
MANUAL CHANGE INFORMATION

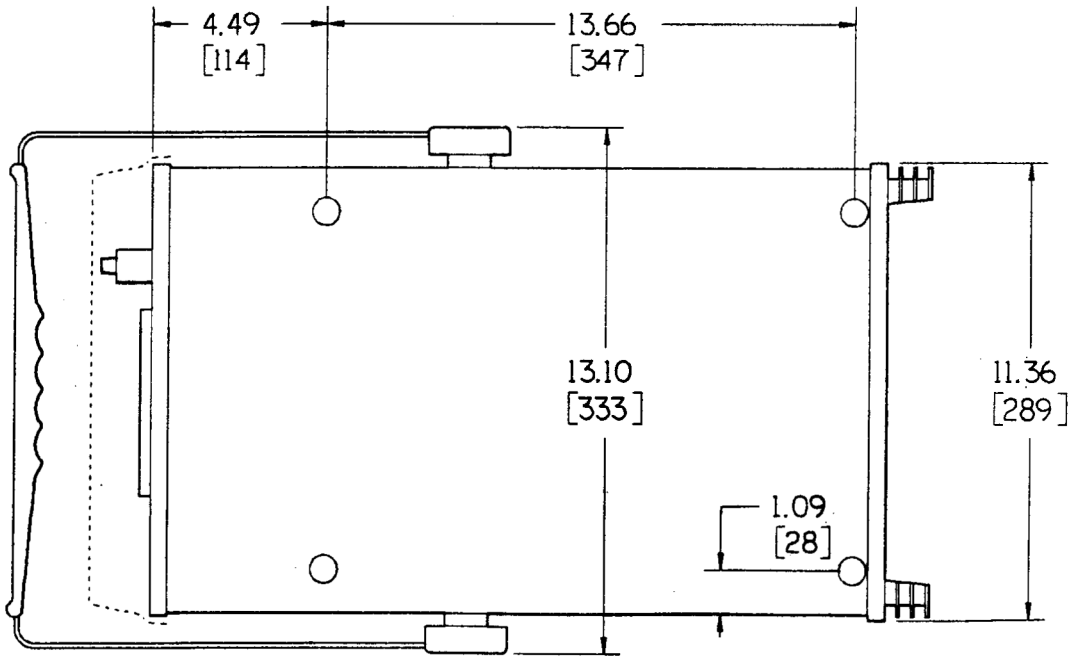
Date: 8-11-84 Change Reference: C6/0884

Product: 468 SERVICE VOLUME I Manual Part No.: 070-3515-00

DESCRIPTION PG 40

DIMENSIONAL DRAWING OF THE 468





Dimensions are in inches [mm]