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067-0859-00

4663 DIAGNOSTIC TEST FIXTURE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

MANUAL PART NO.
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PRODUCT 067-0859-00 4663 Diagnostic Test Fixture

This manual supports the following versions of this product: B010100 and up

MANUAL REVISION STATUS

REV.	DATE	DESCRIPTION
@	4/80	Original Issue

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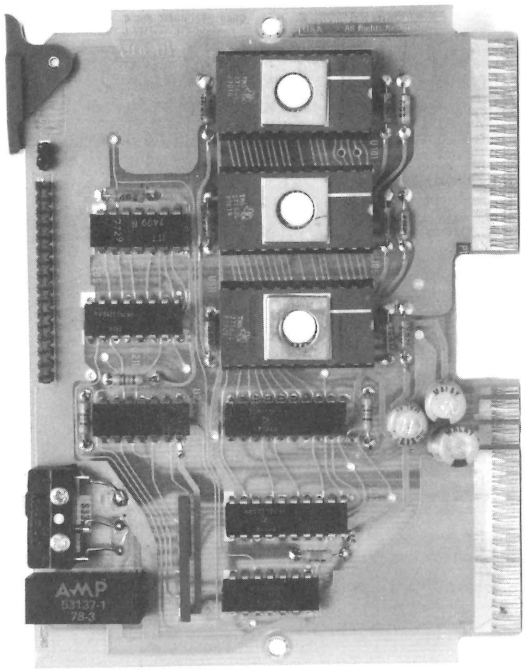
WARNING

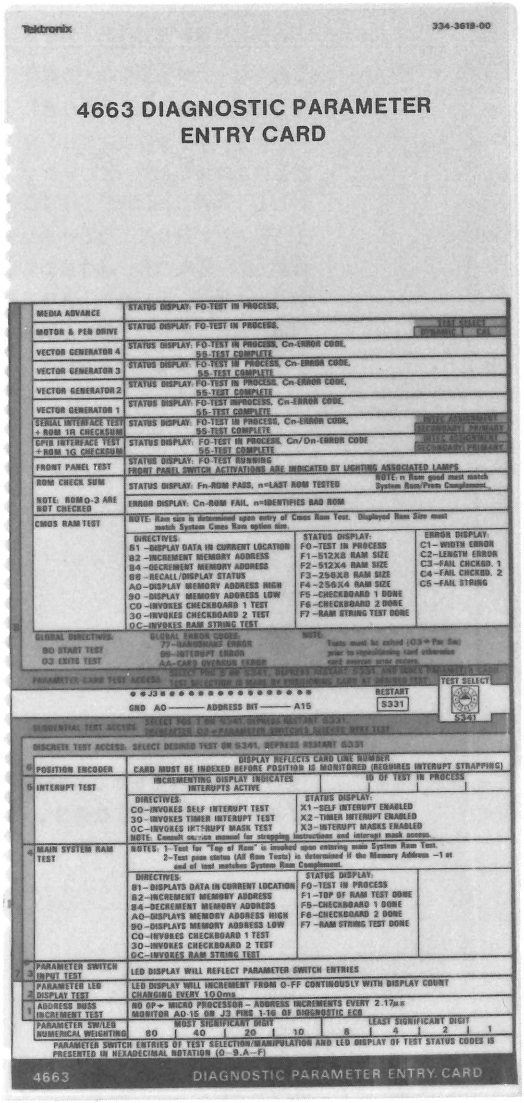
The following servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing other than that contained in operating instructions unless you are qualified to do so.

ILLUSTRATIONS

TABLES

TEST FIXTURE CIRCUIT CARD





2842-1

Figure 1-1. 067-0859-00 Diagnostic Test Fixture.

Section 1

INTRODUCTION

The 067-0859-00 4663 Diagnostic Test Fixture is shown in Figure 1-1. It consists of a circuit card and a Diagnostic Parameter Entry Card for use by the customer or service technician when troubleshooting or verifying plotter operation. The Diagnostic card contains a select switch, test points, and test instructions (stored in PROM).

EQUIPMENT REQUIRED

STANDARD ACCESSORIES

PBUS Diagnostic Card
4663 Diagnostic Instruction Manual
4663 Diagnostic Parameter Card
25 Pin Female RS-232 Test Adapter
25 Pin Male RS-232 Test Adapter
24 Pin Male GPIB Test Adapter

OPTIONAL ACCESSORIES

PBUS Extender Card

TEST CONSIDERATIONS

The tests will check both the standard RAM and the CMOS RAM in the plotter. These tests will write all memory locations with test data and then read the data back to verify proper operation. Any operating parameters stored in CMOS RAM are destroyed by the test data and will have to be restored before the plotter is returned to normal operation.

The Test Fixture card (Figure 1-2) contains test points and two switches. The test points are:

J4-1	GND		
-2	GND		
J3-1	A0	J3-9	A8
-2	A1	-10	A9
-3	A2	-11	A10
-4	A3	-12	A11
-5	A4	-13	A12
-6	A5	-14	A13
-7	A6	-15	A14
-8	A7	-16	A15

The RESTART switch (S331) is used to issue a RESET to the plotter logic. The TEST SELECT switch (S341) positions are shown in Table 1-1.

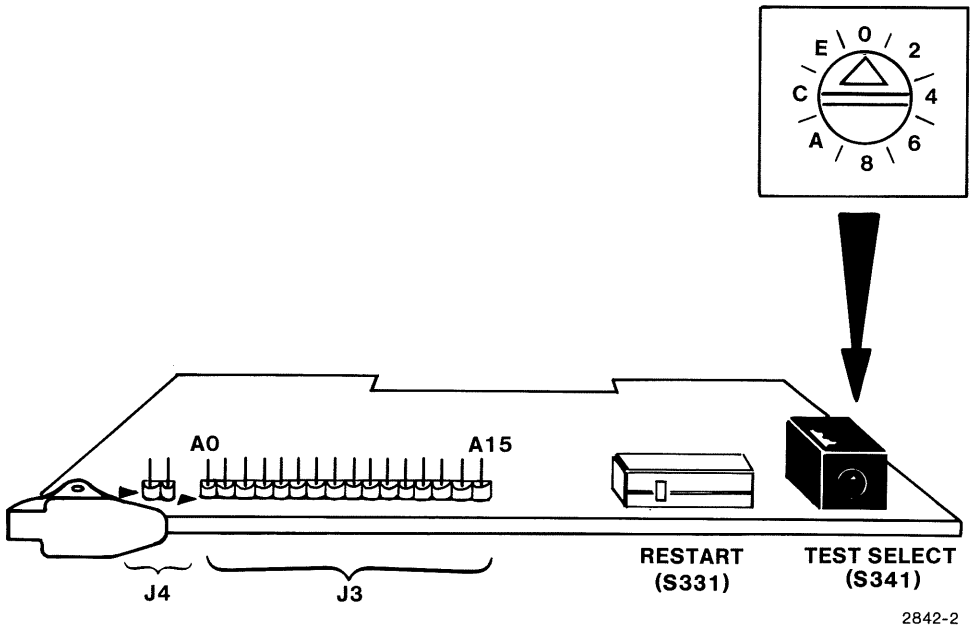


Figure 1-2. Test Points and Switches.

Table 1-1

TEST SELECT SWITCH POSITIONS

Test Select Switch (S341) POSITIONS	Description
0	Diagnostic card disabled.
1	Selects Address Bus Increment Test.
2	Selects Parameter LED Display Test.
3	Selects Parameter Entry Input Test.
4	Selects Main System RAM Tests.
5	Selects Interrupt Tests.
6	Selects Card Position Encoder Test.
7	Allows user to access tests 3-6 via FW Control.
8	Enables Test Selection of ROM Checksum, Interfaces, etc., via Diagnostics Parameter Card.

PHYSICAL AND ELECTRICAL SPECIFICATIONS

Power Requirements:

+5V $\pm$ 5% at 110 ma, Typical 265 ma max.
+12V $\pm$ 5% at 80 ma, Typical 135 ma max.
-5V $\pm$ 5% at 30 ma, Typical 60 ma max.

Package Power Dissipation: $\leq$ 2.3 watts

PROM Capacity: 6K bytes total, 3 ea. 2K byte

Compatible PROM Type: TMS 2716

PROM Access Time: 450 n.s. max.

Physical Dimensions: approx. 5.25" X 3.9"

Operating Temperature: 10°C to 45°C

Storage Temperature: -55°C to 75°C

Operating and Storage Relative Humidity: 0 - 95% noncondensing

Special Handling Requirements:

1. When you clean the Test Fixture card, do not immerse the rotary DIP switch (S341) in the liquid cleaning solution.

2. Because some of the components on the Test Fixture card are susceptible to damage by static electricity, use care when handling and transporting the circuit card.

3. Do not insert or remove the Test Fixture card when power is applied to the plotter.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

Section 2

INITIAL SETUP

INTRODUCTION

This section describes how to install the Test Fixture in preparation for running the test programs. Following the installation procedure there is a brief description of how to run the tests and any special operator interaction required.

INSTALLATION

1. Turn on plotter power and record the customer's parameter settings by pulling out the Parameter Entry card. Note and record any preset parameters for each position of the card.

2. Turn off power to the plotter and disconnect the line cord.

3. Remove the access cover above the Parameter Entry card by inserting the blade of a screwdriver into the slot on the top of the cover and gently lifting up on the handle of the screwdriver. (See Figure 2-1.)

4. Remove the ROM Patch card B (if present) and install the 4663 Diagnostic Test Fixture card (Figure 2-1) in its place.

NOTE

You may want to place a support under the front of the operator's panel so the Parameter Entry switches and indicators are visible while running the tests.

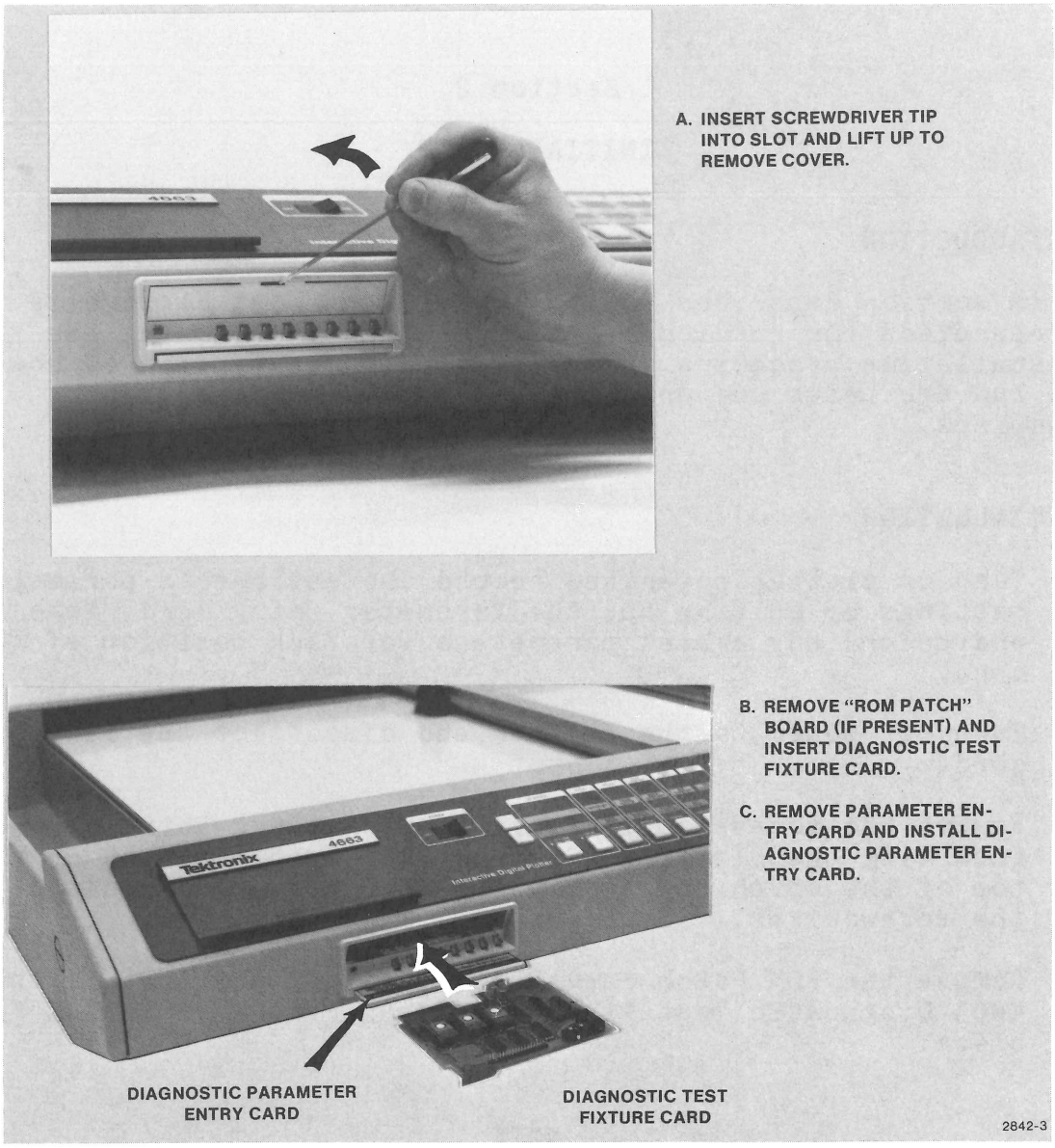


Figure 2-1. Diagnostic Test Fixture Installation.

5. Remove the Parameter Entry card and replace it with the 4663 Diagnostic Parameter card (Figure 2-2).

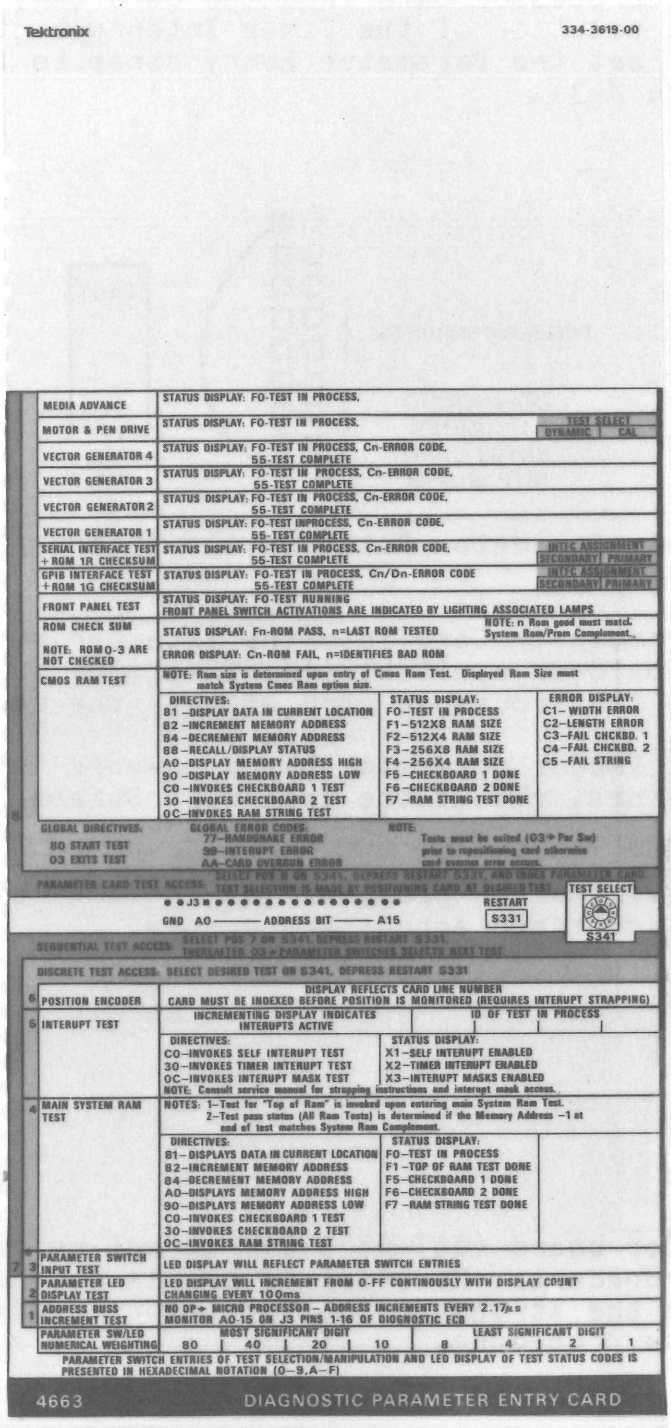


Figure 2-2. 4663 Diagnostic Parameter Entry Card.

6. Lift the Pen Drive Assembly (refer to Appendix C in Volume 2 of the 4663 Service manual for procedure) and remove the Processor Card from the card cage. Note and record the position of the Timer Interrupt strap on the card. Now, set the Parameter Entry strap to position 0 (see Figure 2-3).

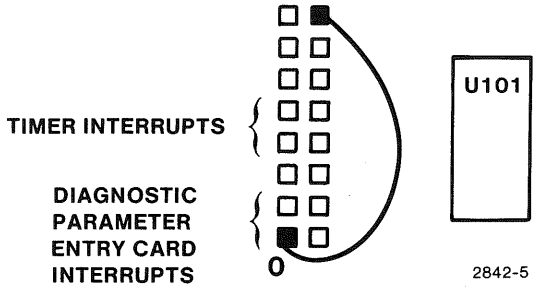


Figure 2-3. Parameter Entry Device Interrupt Strap.

7. Plug the Processor Card into the Extender board if the Extender board is available(1). Then plug the Extender board into the Processor card slot in the card cage.

8. Remove the Vector Generator board, record the Interrupt Strap settings, remove the Interrupt Straps, and replace the board.

9. Restore power to the plotter. You are now ready to run the tests and troubleshoot any errors.

(1)The Extender board (067-0813-00) is not necessary for these test procedures. However, if one is used it is easier to reposition the straps on the Processor Card as required throughout the procedure.

The remainder of this section describes the format and conventions used to describe and run the tests. For a complete description of how to run the tests, refer to Section 3.

RUNNING THE TESTS

Run all tests sequentially. Each succeeding test involves more of the hardware and uses the hardware already tested.

If a test is not completed satisfactorily, or does not indicate an error, return to the previous test. Any time the plotter logic "locks up" performing a test, press the RESTART switch. This will interrupt the test in process and return the logic to the start-of-test condition.

All tests are selected via the rotary Test Select switch (S341) on the Diagnostic card. The switch positions are shown in Table 2-1. In some cases, additional tests are selected (to run under control of the rotary switch setting) using the Parameter Entry Switches.

Table 2-1

TEST SETTINGS

S341	Parameter Entry Switches	Test	Description
0	-	-	Disables the Diagnostic Test Fixture. Enables normal plotter operation. NOTE **If the plotter interrupt straps have been changed to run diagnostics, the ROM Patch Board B has been replaced by the test board, or memory has been changed by running tests, the plotter may not run normally. Check these items before returning the plotter to the customer for normal operation.**
1	-	Address Bus Increment	Monitor bits A0 through A15 (J3-1 to J3-15 on Diagnostic card) with an oscilloscope.
2	-	Parameter LED Display	Parameter Entry lights will increment from 00 to FF. To stop test change switch setting (S341) and press RESTART.
3	All	Parameter Switch Input	As each Parameter Entry Switch is pressed, the corresponding LED will turn on (or off).
4	-	Main System RAM	When initiated, the test writes alternating zeroes and FFs into memory and reads the data back. Completion is indicated by F1 on LED display.
	C0	Checkerboard 1	Starts writing at top of memory and alternates writing 55s and AAs into sequentially lower memory locations. Completion is indicated by F5 in LED display.
	30	Checkerboard 2	Same as Checkerboard 1 except AA starts at top of memory. Completion is indicated by F6 in LED display.
	0C	RAM String	Pseudo random data is written from top to bottom of memory. Completion is indicated by F7 in LED display.
	03	-	Exit test.
5	C0	Interrupt	Low order nibble (4 bits) of LED display is set to 1, indicating Self Interrupt Test in process. High order bits will increment (LEDs flash) from 0 to F indicating proper operation.
	30	Timer Interrupt	As the Timer Interrupt strap is set to each position on the Processor board, the LEDs will indicate (flash) a binary count. Low nibble (4 bits) of display will be 2.
	0C	Interrupt Mask	Interrupt Mask Priority is set using the Parameter Entry switches. Low nibble of display will be 3.

Table 2-1 (cont)

TEST SETTINGS

S341	Parameter Entry Switches	Test	Description
6		Parameter Card Position Encoder	As the diagnostic parameter card is pulled out (one notch at a time), the LEDs will indicate a binary count. The binary count is decremented for each notch the card is pushed in.
7		Auto	Sequences tests 3 through 6. Enter 03 on Parameter Entry switches to increment to next test.
8	80	CMOS RAM	Push the Diagnostic Parameter Entry Card all the way in. Press the RESET button on the Test Fixture Board; then pull the card back out to test position 8 (CMOS RAM TEST).
	C0	Checkerboard 1	Same as Checkerboard 1 test for Test 4.
	30	Checkerboard 2	Same as Checkerboard 2 test for Test 4.
	0C	RAM String	Same as RAM String test for Test 4.
	03	-	Exit test.
	80	ROM Checksum	Set the Diagnostic Parameter card to ROM CHECKSUM position. Completion indicated by FX in LED display. (X = number of ROMs installed; CX = number of failing ROMs)
	03	-	Exit test.
	80	Front Panel	Set the Diagnostic Parameter card to FRONT PANEL TEST. The plotter bell will ring. As each front panel switch is pressed, the LED will light (or turn off).
	03	-	Exit test.
	80	GPIB Interface	Install GPIB test adapter on GPIB connector on back of plotter. Set the Diagnostic Parameter card to GPIB INTERFACE TEST position. 01 on LED display indicates test is waiting for 01 or 02.
	01		Tests GPIB Interface if strapped as primary interface.
	02		Tests GPIB Interface if strapped as secondary interface. Handshake, Interrupt, GPIB ROM checksum, and interface performance is checked. Satisfactory completion indicated by 55 in LED display.
	03	-	Exit test. Remove GPIB Test Adapter.

Table 2-1 (cont)

TEST SETTINGS

S341	Parameter Entry Switches	Test	Description
8 (cont)	80 01 or 02	Serial Interface	Install RS-232 Test Adapter on RS-232 connector on back of plotter. Set Diagnostic Parameter card to SERIAL INTERFACE. 01 on the LED display indicates the program is waiting for interface bank assignment. ENTER 01 or 02 DEPENDING ON CARD STRAP SETTING. THIS TEST WILL FAIL IF THE WRONG LEVEL IS SPECIFIED. Handshake, control, transmit, ROM checksum, and receive lines are tested. **NOTE** **Tests are run at 300 and 9600 baud. The entire test requires approximately 12 seconds to complete.** Satisfactory completion indicated by 55 in LED display.
	03	-	Exit test. Remove RS-232 Test Adapter.
	80	Vector Generator Test 1	Tests Motor and Pen Drive hardware, motion and interrupt hardware. Set Diagnostic Parameter card to VECTOR GENERATOR 1. Satisfactory completion indicated by 55 in LED display.
	03	-	Exit test.
	80	Vector Generator Test 2	Tests DMA and Vector Generator hardware. Set Diagnostic Parameter card to VECTOR GENERATOR 2. **NOTE** **When the test is started an audible tone will be heard from the plotter motors. This tone will last several seconds (depending on the amount of optional RAM in the plotter).** Successful completion indicated by 55 on the LED display.
	03	-	Exit test.
	80	Vector Generator Test 3	Set Diagnostic Parameter card to VECTOR GENERATOR 3. Tests the DMA read and write operations. Successful completion indicated by 55 in LED display.
	03	-	Exit test.

Table 2-1 (cont)

TEST SETTINGS

S341	Parameter Entry Switches	Test	Description
8 (cont)	80	Vector Generator Test 4	Set Diagnostic Parameter card to VECTOR GENERATOR 4. Tests queue pointer logic of DMA. Successful completion indicated by 55 in LED display.
	03	-	Exit test.
	80	Motor and Pen Drive	Set Diagnostic Parameter card to MOTOR/PEN DRIVE. Tests handshaking and memory of Vector Generator logic. Operator selects 01 (calibration) or 02 (system test).
	01	Calibration	Test for a maximum sine wave voltage of 80mv on TP 430, 335, and 330. Adjust R530 (Motor/Pen Drive Board) for 8 V (±1%) for the cosine value on the above test points.
	02	System	Moves the pen and draws a triangle on the plotter. Plotter exercises both pens.
	03	-	Exit test.
	80	Media Advance	Set Diagnostic Parameter card to MEDIA ADVANCE. Tests media advance logic by moving paper. Test continues until 03 is entered.
	03	-	Exit test.
9 ↓ F	-	-	Not used.

IF SOMETHING GOES WRONG

There are several errors detected by the program that pertain to the test selection. The error indication is seen on PED LED (Parameter Entry Device Light Emitting Diodes). These errors are described in the following paragraphs.

99: Interrupt error:

An unexpected interrupt was detected. Check the IRQ-0 line and determine which card is causing the interrupt. Disable the interrupt. If an interrupt error is still present, the PED Interrupt Status Register at address FFA2 may be bad. Run the Interrupt Test to isolate and correct the problem.

AA: Card Overrun Error:

Card Overrun Error bit in Paramenter Entry Device (PED) is set.

Push Diagnostic Parameter card all the way in and pull the card out to reselect the desired test.

77: Handshake Error:

The board tested does not handshake to the P-BUS.

The processor is in a scope loop reading (or writing - depending upon failure) from the board. Check circuits associated with handshake logic. Specific logic to be checked is describe for each individual test.

55: Finished:

Some tests do not need operator's interaction. A 55 on PED LED's indicates that the test was performed with no errors and exited.

Section 3

TEST DESCRIPTIONS

TEST DESCRIPTION FORMAT

Each of the diagnostic tests using the diagnostic test fixture are described in the following format:

TEST NAME

SETUP - How to start and run the test.

DESCRIPTION - Brief overview of the logic being tested and additional information on running the test.

COMPLETION/EXIT - How to determine if the test is satisfactorily completed or how to stop the test.

TROUBLE ISOLATION CHART - A listing of additional test parameters, error indications, probable logic areas to be checked, and schematic references for the logic. The schematic references are to the specific schematic page numbers in the 4663 Interactive Digital Plotter Service Manual.

References in the test descriptions to the Parameter Entry Device (PED) switches, LEDs, high nibble, and lower nibble refer to the PED Switch/Indicators (Figure 3-1).

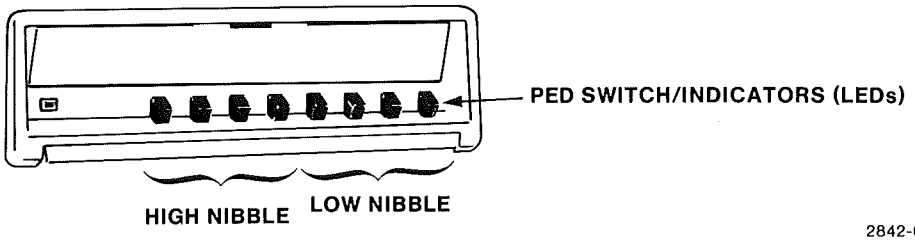


Figure 3-1. PED Switch/Indicators.

TEST: ADDRESS BUS INCREMENT

SETUP: Set S341 to 1, press RESTART (S331)

DESCRIPTION: The Diagnostic card places a NOP (hex 01) instruction on the data bus, sets PGODIS-0 and DDIS-0 low (enabling proper P-BUS handshaking), and increments the bus addresses. Monitor address lines on connector J3 of the diagnostic board using an oscilloscope. The address lines should be pulsing low at a 2 usec rate (Address strobe ASTB and Data strobe DSTB at 1 usec duty cycle. A0 is on J3-1, A15 is on J3-16.

COMPLETION/EXIT: Operation is continuous until RESTART is pressed (S331) or the next test is selected (change S341 to 2).

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
Processor	1-1	U681, Processor board.
Clock Generator	1-2	U901, U911, and U811.
Clocks	1-1	01 (Phase 1) U885-10. Clock duty cycle 1.05 usec.
	1-1, 1-3	02 (phase 2) U885-13. If stretched, check for a bus error (BERR-1, U891-3 high). If high, locate the source of the bus data or hardware error.
	1-2	BCK-1 (Bus pin 77).
NOP Instruction not present at Processor	1-1, 1-5	Processor (U681) data pins and associated logic (U675-3, U775-3, U331-5, and U341-5). Also check for proper operation of the Diagnostic card.
Processor Buffer Handshake	1-1	U691, U791 and associated logic.
PBUS Handshake	1-4	U621 and associated circuits. NOTE **If DDIS and PGODIS (U661) are low, the handshake logic should operate properly.**
Additional Checks BRP0-1 to BRP2-1 and IRP0-1 to IRP2-1	1-3	Power supply voltages. Check for proper switching of signals (U941, U751 and associated circuits).

TEST:	PARAMETER LED DISPLAY
SETUP:	S341 to position 2, press RESTART
DESCRIPTION:	The processor writes into the Parameter Entry LEDs (FFA3), enters a delay loop and increments the display in binary fashion. The display LEDs will start at zero, count to FF, and return to zero. The test will continue to run until an error is detected or the test is stopped by the operator.
COMPLETION/EXIT:	Operation is continuous until S341 is set to position 3 and RESTART is pressed.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
No countup on LEDs	2-1	INIT light (extreme left LED) off. Check power supply voltages.
Signal checks		Scope all address and data lines (repeat NOP test if these lines are suspected).
	1-3	HALT-0, BRQ-0 should be "1", IRP0-1, IRP1-1, IRP2-1, BRP0-1, BRP1-1, and BRP2-1 should be pulsing.
	1-1	IOADD-1 and WRITE-0 should be pulsing.
	1-4	PGODIS-0, RST-0, and IRQ-0 should be "1". ASTB-0, DSTB-0, and BDDIS-0 should be pulsing.
		If any of the above signals are wrong, check the associated circuit drivers.
		Check the Display Register (U251) input signals, clock enable, LEDs, and related logic.
Bus Error (BERR-1)	1-3	Repeat NOP test and check address lines, data lines and control lines for opens, shorts, etc. Also check for bad drivers, and the PBUS Handshake logic (U845, U941 and associated circuits).

TEST:	PARAMETER ENTRY INPUT
SETUP:	S341 to position 3, press RESTART
DESCRIPTION:	When the test is initiated (RESTART), code F0 will be displayed on the LEDs. When any key is pressed, the corresponding LED will turn on and the remaining LEDs will turn off. If the same key is pressed again the LED will remain on. The operation of each PED key and its corresponding LED should be checked.
COMPLETION/EXIT:	Enter 03 on the keys or set S341 to position 4 and press RESTART to terminate the test.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
LED does not come on	2-1	Check for bad LED. Run PARAMETER ENTRY LED TEST to check LED operation.
PED logic	2-1	Check for proper key operation and output. Check output of PED Register (U271). Verify proper PED Register Address decode. NOTE The PED Register is being read in a close loop routine. Trigger scope on U411-4 (or U271-1 or -19). Press key and verify low on the appropriate data line at the strobe time.

TEST: MAIN SYSTEM RAM TEST

SETUP: S341 to position 4, press RESTART

DESCRIPTION: This test actually consists of four separate tests, a RAM write/read test, two checkerboard tests, and a RAM string test. The first test is started automatically when the test is initiated; the remaining tests are initiated by the operator.

Commands which are available to the operator are:

C0	Perform Checkerboard test 1.
03	Perform Checkerboard test 2.
0C	Perform RAM string test.
A0	Displays high address byte currently interrogated.
90	Displays low address byte currently interrogated.

NOTE

When the address bytes are displayed on the LEDs the following logic levels are indicated:

logic 0 - LED on
logic 1 - LED off

This is the opposite of the LED indications on other tests.

81	Displays the data at the interrogated address.
82	The CPU will read and display the data from the present address +1. It continues to read from this address (and display the contents of the address) until the test is ended or another command is entered. If 82 is entered again, the CPU starts reading from the next higher address.

84 The CPU will read and display the data from the present address -1. It continues to read from this address (and display the contents of the address) until the test is ended or another command is entered. If 84 is entered again, the CPU starts reading from the next lower address.

Each of the SYSTEM RAM tests are described in detail on the following pages. It should be noted that the checkerboard tests and RAM string test can be selected at random and do not have to be run in the sequence listed.

TEST: RAM WRITE/READ (MAIN SYSTEM RAM TEST cont.)

SETUP: S341 to position 4, Press RESTART.

DESCRIPTION: This test is run automatically when the system RAM Test is initiated. The CPU starts at address 0000 of memory and writes zeroes and FFs into each memory address. After each address is written, the CPU reads the contents of memory and compares it with the value written. If the data compares, the CPU will step to the next address. Regardless of whether an error was detected or not, an F1 is displayed on the LEDs and the CPU loops on the last address interrogated.

COMPLETION/EXIT: To determine if an error was detected, enter A0 on the PED switches. This displays the current high address byte. To display the low address byte, enter 90 on the PED switches. The high address and low address bytes together should be greater than 1FFF hexidecimal for 8k of memory.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
RAM address within range of installed RAM	1-5	Enter A0 and/or 90 on PED switches to determine fault address. Enter 81 on PED switches to display the data at the selected address. Trace the faulty bit through drivers and associated logic (trigger oscilloscope on CE - pin 8 of associated RAM IC if needed.)
Wrong data	1-1, 1-4, 1-5	Check write logic and RAM addressing logic. Verify that the proper data is being written into RAM. **NOTE** **Data is only written between the start command and the end of test indication. When looping, the memory will only be read.** If the input data is correct, check the output data on a read operation. Check the RAM and associated read logic.

TEST: CHECKERBOARD TEST 1 (MAIN SYSTEM RAM TEST cont.)

SETUP: S341 to position 4, enter C0 on PED switches

DESCRIPTION: The CPU locates top of RAM, writes 55 into the highest RAM address, decrements the address and writes AA into the next location, decrements the address and writes 55, etc., until it reaches address zero. When address zero is reached the CPU reads the data back and compares it with the information originally written, incrementing the address after each successful read/compare.

COMPLETION/EXIT: Successful completion or error is indicated by F5 on the LEDs. Enter A0 and 90 to determine the RAM address. If the address is above the top of installed RAM the test was completed normally. Any other address indicates an error.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
RAM address within range of installed RAM	1-5	Enter A0 and/or 90 on PED switches to determine fault address. Enter 81 on PED switches to display the data at the selected address. Trace the faulty bit through drivers and associated logic (trigger oscilloscope on CE - pin 8 of associated RAM IC if needed.)
Wrong data	1-1, 1-4, 1-5	Check write logic and RAM addressing logic. Verify that the proper data is being written into RAM. If the input data is correct, check the output data on a read operation. Check the RAM and associated read logic.

TEST:	CHECKERBOARD TEST 2 (MAIN SYSTEM RAM TEST cont.)
SETUP:	S341 to position 4, enter 30 on PED switches
DESCRIPTION:	Same as CHECKERBOARD 1 test except the pattern is reversed. The CPU starts at the top of RAM memory, writes AA into the first location, decrements the address by 1, writes 55, decrements and writes AA, etc.
COMPLETION/EXIT:	Same as CHECKERBOARD 1 test except F6 will be displayed in the LEDs.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
RAM address within range of installed RAM	1-5	Enter A0 and/or 90 on PED switches to determine fault address. Enter 81 on PED switches to display the data at the selected address. Trace the faulty bit through drivers and associated logic (trigger oscilloscope on CE - pin 8 of associated RAM IC if needed.)
Wrong data	1-1, 1-4, 1-5	Check write logic and RAM addressing logic. Verify that the proper data is being written into RAM. If the input data is correct, check the output data on a read operation. Check the RAM and associated read logic.

TEST: RAM STRING TEST (MAIN SYSTEM RAM TEST cont.)

SETUP: S341 to position 4, enter 0C on PED switches

DESCRIPTION: Top of RAM is found, then a string is written from the memory top to zero. The string is as follows:

TOP:

00, 01, 02, ..., FE, 00,
01, 02, 03, ..., FF, 01,
02, 03, 04, ..., 00, 02, etc.

This creates a pseudo random string, which is then read back. The CPU will stop and loop at the point where the string is incorrect. If the address is above the top of RAM, the test was completed satisfactorily.

COMPLETION/EXIT: F7 on LED display indicates test complete. Set S341 to position 5 and press RESTART to select next test.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
Test failed	1-5	Check the Address lines by stepping up/down in memory or by running the NOP test. Exchange or replace the suspected RAM. Use commands from the PED switches to further isolate problem. **NOTE** **The Processor loops through the entire command table, so any test can be selected at random and run over again if desired.**

TEST: INTERRUPT TESTS

SETUP: S341 to position 5, press RESTART

DESCRIPTION: This test actually consists of three tests, a Self Interrupt test, a Timer Interrupt test, and an Interrupt Mask test. The tests verify the interrupt hardware on the Processor board. The tests start with the minimum hardware configuration and work up to more complex situations. The lower nibble (4 bits) of the LEDs will indicate the test in progress, 1 indicates Self Interrupt test, 2 indicates Timer Interrupt test, and 3 indicates Interrupt Mask test.

The tests are described in detail on the following pages.

TEST: SELF INTERRUPT TEST (INTERRUPT TESTS cont.)

SETUP: S341 to position 5, press RESTART

DESCRIPTION: The Self Interrupt flip-flop is set (Write 0 at FFA1). The LEDs are stepped by 10 (hex) by the interrupt routine. The interrupt resets the Self Interrupt flip-flop and the CPU enters a short WAIT loop. The Self Interrupt flip-flop is set and the cycle is repeated. The resulting binary count-up on the high nibble (4 bits) of the LEDs indicates proper operation of the interrupt logic.

NOTE

Since hardware interrupts have priority over self interrupts, the display will count very fast (LEDs will appear very dim) if INTERRUPT 0 pin is grounded.

COMPLETION/EXIT: Enter 30 on the PED switches to select the TIMER INTERRUPT test. Tests and exit conditions can be selected at random.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
SINT-0	1-4	U511-8 is high; check U511, U521, and U411
	1-3, 1-1, 1-4	U511-8 is low but LEDs are not counting: Check signal path through U851, U745, U741, U641, U681 (CPU), U881, U685, U785, U771, and U981 where CSI-1 resets the Self Interrupt Request.
Routine never returns	1-3	Address All is not altered properly via U651 or, U471 and U951 are bad.

TEST: TIMER INTERRUPT (INTERRUPT TESTS cont.)

SETUP: S341 to position 5, enter 30 on PED switches

DESCRIPTION: The Interrupt mask is off and the timer interrupt is enabled resulting in an interrupt pulse every 8 msec. The LED display is cleared. With no strap on the Timer Interrupt pins (Figure 3-2) the display should not change. If any Interrupt pin is connected to one of the Timer Interrupt pins, the display will indicate a binary count-up. A 2 will be present in the lower nibble (4 bits) of the LEDs.

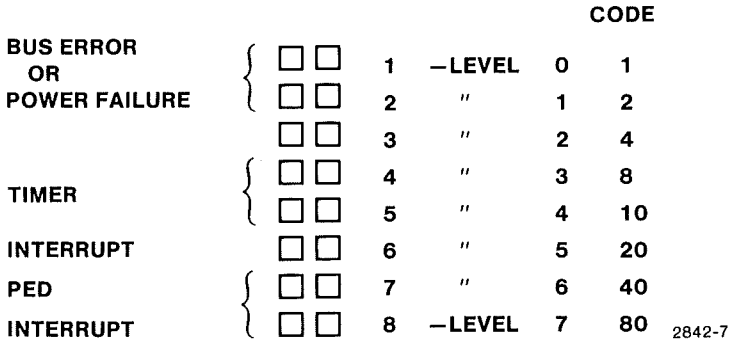


Figure 3-2. Interrupt Straps.

COMPLETION/EXIT: Enter OC on the PED switches to select the Interrupt Mask test. Other tests or exit can be selected at random.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
Signal Path	1-4, 1-3	U111, U101, U651, U861, U745, U751, U741 and U471.
Timer Logic	1-4	U401, U845, U501 and U601

TEST: INTERRUPT MASK TEST (INTERRUPT TESTS cont.)

SETUP: S341 to position 5, enter 0C on PED switches

DESCRIPTION: The interrupt mask is set according to the PED key depressed. The leftmost key represents the lowest priority, the right-most key represents the highest priority. Therefore, if the timer interrupt is strapped to level 3 (pin 4 on Figure 3-2), the PED display should not be counting if code 04, 02, or 01 is entered. A complete list of codes (and corresponding strap settings) is shown in Figure 3-2).

If Code 20 is entered, nothing happens. Now connect the straps to pin 1, 2 or 3 and it should start counting. Interrupt level 0 (pin 1) cannot be masked off.

NOTE

The interrupts must be running to step the tests.

COMPLETION/EXIT: Set S341 to position 6, press RESTART. Other tests or exit condition can be selected at random.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
Interrupt mask (FFA0)	1-4	Bits 0, 1 and 2 of U201
Signal path	1-4, 1-3	Check U111, U101, U651, U861, U745, U751, U741 and U471.

TEST: PARAMETER ENTRY CARD POSITION ENCODER

SETUP: S341 to position 6, press RESTART

DESCRIPTION: The test is interrupt driven and requires that the card Interrupt Flag be set to any one of the eight interrupt levels.

The card should then be fully pushed in. When the card is then pulled out, it generates an interrupt every time it passes a line (audible click is heard). The PED display will count up a binary count for each line that the card is pulled out. It will decrement the count for every line it is pushed.

COMPLETION/EXIT: S341 to position 7, press RESTART

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
Display off, does not increment	1-4, 2-1	The interrupt is not seen, check PED enable U201 (FFA0). Also check U211, U111, U221, U141, U121, U131, U231 and U241.
	2-1	Check for bad indicator (LED) or bad phototransistor.

TEST: SEQUENTIAL TEST ACCESS

SETUP: S341 to position 7, press RESTART

DESCRIPTION: Sequences through tests 3 thru 7

Enter 03 to select RAM test.
   Enter C0 to select Checkerboard 1 test.
   Enter 30 to select Checkerboard 2 test.
   Enter 0C to select RAM String test.
Enter 03 to increment to next test.
   Enter C0 to select Interrupt test.
   Enter 30 to select Timer Interrupt test.
   Enter 0C to select Interrupt Mask test.
Enter 03 to increment to the next test.

NOTE

The checkerboard tests, RAM string test, or the various Interrupt tests can be selected at random since they require operator selection.

TEST: CMOS RAM

SETUP: S341 to position 8. Push the Diagnostic Parameter Entry card all the way in ; press the RESET button on the Diagnostic Test Fixture board, and then pull the Diagnostic Parameter Entry card back out to test position 8. Select CMOS RAM test on Diagnostic Parameter Entry card, and enter 80 on the PED switches.

DESCRIPTION: This is a test similar to main RAM test. It is, however, custom tailored for CMOS RAM. This test will definitely destroy information in the CMOS RAM. The system parameters will have to be entered again when the tests are completed. There are four parts of the test. The first test is to determine the amount of CMOS RAM installed in the plotter. The remaining tests are write/read tests to verify operation.

The following commands are available to the operator:

CODE C0: Perform checkerboard test 1. (F5 on completion)

CODE 30: Perform checkerboard test 2. (F6 on completion)

CODE 0C: Perform RAM STRING test. (F7 on completion)

CODE 03: Exit the test.

NOTE

The previous three tests are described under tests Checkerboard Test 1, Checkerboard Test 2, and RAM STRING test later on in this section.

The following commands can be used with each of the previous tests if additional information is needed.

CODE A0: Displays high address byte currently interrogated.

NOTE

LED on = Logic 0, LED off = Logic 1.

CODE 90: Displays low address byte currently interrogated.

CODE 88: Return to "After Test" status.

CODE 84: Decrement interrogated location and display new data.

CODE 82: Increment interrogated location and display new data.

CODE 81: Display data at present address.

TEST: RAM SIZE DETERMINATION (CMOS RAM TESTS cont.)

SETUP: S341 to position 8, Diagnostic Parameter Entry card to CMOS RAM TEST, 80 entered from PED switches.

DESCRIPTION: Test is entered when CMOS RAM Test is started. Both memory length and width is established, with the limitation that the RAM width be consistent throughout the RAM length. RAM size is evaluated by writing 00 and reading/comparing the stored data. The process is repeated with data = FF. The process is repeated for successive RAM locations until an error is encountered or the logical end of RAM is determined. Upon completion of the test, RAM size or an error code (whichever is appropriate) is displayed on the Parameter LED Display.

COMPLETION/EXIT: The LEDs will indicate the status on completion of the test. The following is a list of the display codes.

F2 = NIBBLE (4 bits), 512 ADDRESSES

F4 = NIBBLE (4 bits), 256 ADDRESSES

F1 = BYTE (8 bits), 512 ADDRESSES

F3 = BYTE (8 bits), 256 ADDRESSES

C1 = ERROR, NEITHER NIBBLE, NOR BYTE

C2 = ERROR, NEITHER 256, NOR 512 ADDRESSES

The CPU keeps looping on an error location or on the top of CMOS RAM. It also keeps scanning the PED switches, waiting for a command.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
ERROR CODE displayed	1-1, 1-5	U971, U445, U731, U641 and U421 are used to generate CE signal on CMOS RAM. Make sure that the CE signal is present on pin 13 of the addressed RAM. Triggering on this signal, all address and data lines can be interrogated. The memory IC's are U345, U351, U355 and U361.

TEST: CHECKERBOARD 1 (CMOS RAM TESTS cont.)

SETUP: S341 to position 8, CMOS RAM TEST selected on Diagnostic Parameter Entry card, enter C0 on PED switches.

DESCRIPTION: The CPU writes alternate 55 and AA's starting at address F800. It then reads the data back and verifies that the pattern did not change.

COMPLETION/EXIT: Satisfactory completion is indicated by F5 in the LED display. An error is indicated by a C3 in the display.

TROUBLE ISOLATION CHART:

Symptom/Logic	**Schematic Reference**	Check
ERROR CODE displayed	1-1, 1-5	U971, U445, U731, U641 and U421 are used to generate CE signal on CMOS RAM. Make sure that the CE signal gets to pin 13 of the addressed RAM. Triggering on this signal, all address and data lines can be interrogated. The memory IC's are U345, U351, U355 and U361.

TEST: CHECKERBOARD 2 (CMOS RAM TESTS cont.)

SETUP: S341 to position 8, CMOS RAM TEST selected on Diagnostic Parameter Entry card, enter 30 on PED switches.

DESCRIPTION: This test is identical to Checkerboard Test #1 except it starts with AA at address F800.

COMPLETION/EXIT: Satisfactory completion is indicated by F6 in the LED display. An error is indicated by C4 in the display.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
ERROR CODE displayed	1-1, 1-5	U971, U445, U731, U641 and U421 are used to generate CE signal on CMOS RAM. Make sure that the CE signal gets to pin 13 of the addressed RAM. Triggering on this signal, all address and data lines can be interrogated. The memory IC's are U345, U351, U355 and U361.

TEST: RAM STRING (CMOS RAM TESTS cont.)

SETUP: S341 to position 8, CMOS RAM TEST selected on Diagnostic Parameter Entry card, enter 0C on PED switches.

DESCRIPTION: A long string is written into the RAM. It starts with 0 at address F800 and it skips every 256 value. The string is then read and checked.

COMPLETION/EXIT: Satisfactory completion is indicated by F7 in the LED display. CX(1) in the display indicates an error was detected. As in all these tests, the CPU loops on top-of-RAM (or on error location) and the input command set can be used to isolate the problem.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
ERROR CODE displayed	1-1, 1-5	U971, U445, U731, U641 and U421 are used to generate CE signal on CMOS RAM. Make sure that the CE signal gets to pin 13 of the addressed RAM. Triggering on this signal, all address and data lines can be interrogated. The memory IC's are U345, U351, U355 and U361.

(1) "C" is the high byte of the hexidecimal number. "X" can be any value and is the low byte of the hexidecimal number.

TEST: ROM CHECKSUM

SETUP: S341 to position 8, select ROM CHECKSUM on Diagnostic Parameter Entry card, enter 80 on PED switches.

DESCRIPTION: The CPU calculates checksums for ROMs 4 and up. A binary count is displayed on the LEDs to indicate satisfactory completion or failure. The testing technique used is to scan downwards in address space, starting at ROM 4 and continuing to ROM 9. If all these ROMs pass the checksum test, the test will continue to scan downwards, looking for Option Proms. The test cannot check ROMs 0 through 3 because the diagnostic firmware occupies their address space.

COMPLETION/EXIT: If the test finds that all ROMs found have good checksums, FS will be displayed on the PED LEDs, where X is the number of good ROMs found. The number X should be checked according to the following table. The table shows the number of good ROMs which should be found depending on whether the instrument is equipped with firmware options.

If the ROM is found to have a bad checksum, CX will be displayed on the PED LEDs where X is the number of the bad ROM. When a bad ROM is found, the CPU loops, reading the bad ROM for trouble isolation. Enter 03 on the PED switches to exit the test.

The minimum number that is displayed should be F9, indicating that 9 ROMs were found to be good. If less than F9 is displayed, a ROM may be missing or faulty in a way such that it does not output data. If either Firmware Option 31 or Option 32 are installed, the minimum response should be FB (1111 1011), as either option adds two logical (not physical in the case of Option 32) ROMs to the system. If a smaller number is returned on this test, try checking to see that the Options are really installed, then check all the ROMs. If both Option 31 and 32 are installed, the test should return FD (1111 1011). Again, if a smaller

number is returned, check the ROMs. A common problem in early instruments is faulty sockets causing intermittent contact on the ROM legs. Try removing all the ROMs and reinserting them.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
CX on LED	1-6	Replace ROM that failed. Pin 20 (CE) of ROM that failed should be pulsing. IC's generating the CE are U451, U971, U531, U541 and U461 on Processor Board.

TEST: FRONT PANEL

SETUP: S341 to position 8, FRONT PANEL TEST selected on Diagnostic Parameter Entry card, enter 80 on PED switches

DESCRIPTION: This tests the bell, lights and switches on the front panel of the instrument and an associated circuitry on the vector generator board. It first checks the P-bus handshake through the register located in FDE3. In case of error, the test will be in a loop at the register, so that the handshake logic may be investigated.

The PED then displays F0 and the bell is turned on for about a second. The lights are then enabled and the front panel switch status monitored, via FDE0. The value of FDE0 will be negative (BIT 7 = 0) if a switch was depressed. The processor then reads the key combination and converts it into an inverted bit in a pseudo-register, corresponding to the light to be turned on or off. The first time the switch is depressed, the corresponding bit is set; the second time it is reset. There are four pseudo-registers (118-11B). The first two pseudo-registers are used on front panel, second two are available for key and light extension. The CPU transfers these pseudo-registers into FPLITE register (FDE2). Data is then shifted serially out in highest first, lowest last order. Together with the register data, the shift-out clock is sent and the data is shifted to parallel-out registers on the front panel and by high current drivers turning on or off appropriate lights.

COMPLETION/EXIT: As each front panel switch is pressed, the corresponding indicator will come on; pressing the switch again will turn the indicator off.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
77 on LEDs (Hand-shake error)	5-1	Investigate U40, U55, U180, U290, U160, U155, U175 or U225.
Indicator does not turn on (or off) when switch is pressed	7-1, 5-1	On front panel: U121, U113, U115, U125, U127, U131, U135, U133, U13, U15, U25, U11 and U111. The U121-14 should be clocking and SWICHG-0 signal shold be pulsing low every time any switch is depressed or released. SWPOL-1 should be pulsing as long as switch is held depressed. SWCHG-0 then follows this path on vector generator: U190, U5, U215, U5, U215, U10, U220, U45, U35, U115, and U15. When the switch status is read, the following logic is used: U65, U145, U215, U115, U110 (FDE0). The key status is present via registers U46, U455 at FDE1. The data is shifted out via U470 and U110, and shifted in through U43 and U151 on the front panel. The U141, U142, U145, U146, U147, U148, U156 and U155 are lamp drivers. The bell signal uses U25, U195 and U192.

TEST: GPIB INTERFACE

SETUP: S341 to position 8, GPIB INTERFACE TEST selected on Diagnostic Parameter Entry card, install GPIB Test Adapter (see Figure 3-3 for adapter wiring) on GPIB connector (rear of Plotter), enter 80 on PED switches. Enter appropriate secondary or primary PED switch under INTFC ASSIGNMENT.

DESCRIPTION: The GPIB interface hardware is tested for compatability with the P-bus, for interrupt handling and for GPIB interface performance. It uses a loopback connector to loop the control, handshake and data lines back into the interface connector.

After the start of test, Code 01 is displayed signaling that the CPU needs to have the operator to indicate if the GPIB is primary or secondary. Enter 01 on the PED switches if the GPIB Interface strap is set for primary or 02 if the strap is set for secondary.

NOTE

The base address of the primary bank is FF40; the base address of the secondary bank is FF60.

After the bank is determined, the CPU tests the P-bus handshake during read and then during write at the base address. If a bus error occurs on PED and the CPU loops on that address, the program remains in the loop until the error is corrected or test is exited.

After the handshake test, the GPIB interface registers and drivers are tested.

The CPU then performs a series of tests. Each time it completes a test, it steps an error code, starting with 2.

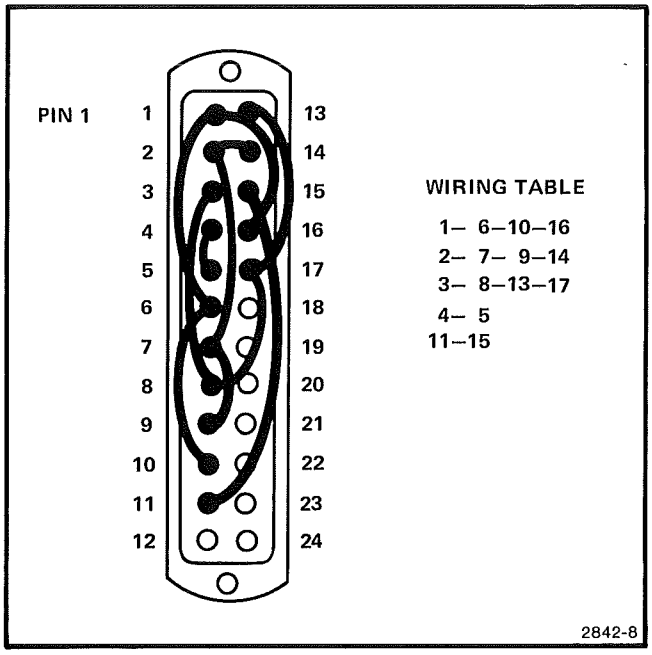


Figure 3-3. GPIB Test Adapter Wiring.

COMPLETION/EXIT: Satisfactory completion is indicated by 55 in the LED display. An error is indicated by 77 or CX error code in the LED display.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
ERROR 77	4-1	There is following signal flow for the handshake: U391, U691 buffer the address lines, decode via U481, U277, U681, U981, U471, U671. The handshake is then generated by U771, U677, U471, U781, U977, U881, U877, and U871. Make sure that the interface board is properly strapped and that the proper bank level is selected at the beginning of the test.
ERROR C2	4-3	SRQ test failed. SRQ is sent via the command register (FFX3) (U121) and via the GPIB driver U311. It is then received and read from the data register (FFX2) (U117) via the GPIB data drivers U511, U521.
ERROR C3	4-3	IFC test failed. This signal is sent via the same path as SRQ.
ERROR C4	4-3	REN test failed. This signal is sent via the same path as SRQ. Low. Acceptor state. The NDAC should be low and the NRFD should be high on the GPIB.

Symptom/Logic	Schematic Reference	Check
ERROR C5	4-3	The handshake logic may be faulty. Investigate NRFD-1 and NDAC-1 via U311, U141, U151, U341, U147, U347.
ERROR C6	4-3	(Acceptor mode) SRQ is brought low, taking DAV low. NRFD and NDAC should now be both low on GPIB. That is verified by reading the data register U117(FFX2 after a delay (to make sure that the DEBOUNCE delay (U137) has settled down). DAV enters via U311, U137 and checks the handshake logic U141, U151, U341 and U311. The NRFD and NAAC are tested via U511, GPIB driver and U117 (FFA2) data register.
ERROR C7	4-3	The handshake is given a command to acknowledge the acceptance of data. The increment FFX0 command will read a ground strapped D0 at this address. It then returns with a high back to this address, giving a shake command via SHAKE-1. NDAC on the GPIB bus will then go high, indicating all data accepted to the talker. Same path as in Error 7 section is taken for the handshake and data logic. The handshake command register (FFX0) is U317 for read and U351, U551 for write cycle.
ERROR C8	4-2	Data valid (DAV) on the GPIB bus is taken high via command register (FFX3) (U121). After a debounce wait, NRFD is back high and NDAC should be brought low. Same path taken as in previous test.
ERROR C9	4-3	(The instrument is a talker.) The data register is cleared; the handshake driver is disabled. The data is then read to make sure that no one is pulling the data driver low on GPIB. U117 (FFA2) is in data write register, U317 and U517 are the read registers. U311 should be disabled by high on pin 12, U111 should have all outputs (pins 2, 7, 15 and 9) high because U121 should have all outputs low.
ERROR CA	4-2, 4-3	The error of the handshake logic is monitored. The CPU writes transmit and address bits high into the command register (18 at FFX3). If NRFD and NDAC are both high on the GPIB, it is detected as an error condition. The CPU then reads 20 at FFX3. Cause of an error may be the command register (U121). The GPIB driver (U311) or the handshake logic (U141, U151, U331, U347, U361, U341 or U147).

Symptom/Logic	Schematic Reference	Check
ERROR CB	4-3	NDAC is brought low on GPIB bus via DIO3 (write 04 into FFX2). The error bit (bit 5 at FFX3) is now tested again. If set, the possible error hardware is same as in Error A.
ERROR CC	4-3	It is now indicated to the handshake logic, that all devices are ready NRFD=1 and no data is accepted NDAC=0. A handshake command is sent (Increment FFX0). This should bring Data Valid Strobe (DAV) low. Possible areas of error are same as for ERROR CA.
ERROR CD	4-3	NRFD and NDAC are both set low, signalling that not all data are yet accepted. The error flag is interrogated again. Same logic circuits are affected as in ERROR CA.
ERROR CE	4-3	All data accepted is signalled NDAC=1 and NRFD=0. This should bring data valid strobe (DAV) back high. Also here, the same logic hardware is affected as during ERROR CA.
ERROR CF	4-3	Send NDAC=0 and NRFD=1 to restore the conditions on the GPIB bus. Read the data register (FFX2) and make sure that the handshake logic does not override it. Possible areas of fault are the handshake logic (ERRORCA). The GPIB driver (U511). The data registers (U117 and U317).
ERROR D0	4-2	EOI test failure. EOI is sent on the bus, and read on the data register are the loopback connector. Possible areas of error are the control register (U121) the GPIB drivers U511 and U311, U347 or U317.
ERROR D1	4-2	Interrupt flag test failed. In this test, the handshake interrupt and the status change interrupt are enabled. The GPIB completes one transaction, and the interrupt flag registers are used. Both the handshake interrupt and the status change interrupt should be set (93 at FFX1). The possible problem areas are U337, U531, U331, U131, U547, and U537.
ERROR D3	4-1	CHECKSUM ERROR. In this test, the ROM is enabled and checksum calculated. The ROM checksum program is run. Possible problem hard wave is U761 or the associated ROM (U171, U181). Checksum Error exit is possible using 03.

TEST: SERIAL INTERFACE

SETUP: S341 to position 8, SERIAL INTERFACE TEST selected on Diagnostic Parameter Entry card, install RS-232 test adapters (see Figure 3-4) on RS-232 connector (on back of plotter), enter 80 on PED switches. Enter appropriate secondary or primary PED switch under INTFC ASSIGNMENT.

NOTE

The adapters are installed on the plotter rear panel connectors labeled TERMINAL and MODEM.

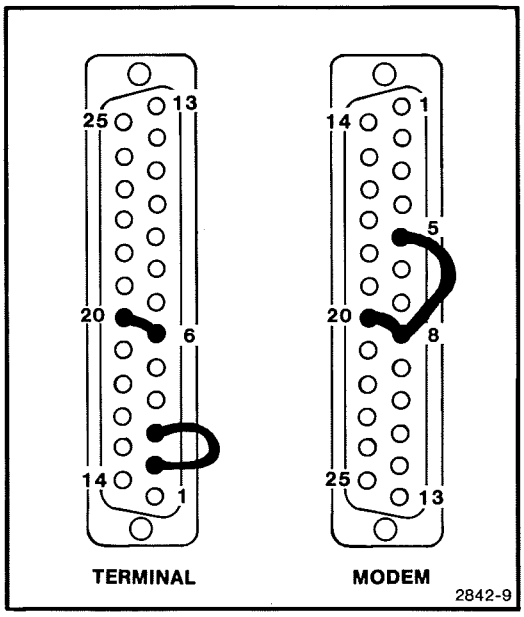


Figure 3-4. RS-232 Test Adapters.

DESCRIPTION: The serial interface hardware is tested for it's compatability with the P-bus and with its ability to supply logic signals to RS-232 and other interfaces. In case of RS-232, the interface will be tested through adaptors placed on the back of the instrument.

NOTE

The TTY Port Interface can also be tested using these prodedures. Refer to the 4663 Service manual for schematics and component locations required for fault isolation.

After the test is started, Code 01 is on, signaling that the level for the serial interface is to be entered. Enter 01 if the RS-232 Interface is strapped for Primary or 02 if the Interface is strapped for secondary.

After the bank is selected, the processor performs P-bus handshake test at the base address (FF40-primary/FF60-secondary).

In case of handshake error, the CPU will be continuously reading and writing into tested address, depending upon the error.

The CPU will then test the control lines, transmit and receive lines. It will perform a series of tests, stepping the count on LEDs every time the next test starts, beginning with C1. In case of an error, the test number that failed will be displayed and the CPU will be looping on the test.

NOTE

A series of characters is sent at a 300 baud rate. This test requires approximately 12 seconds to complete and F0 will be displayed on the LEDs while the test is in progress.

COMPLETION/EXIT: Satisfactory completion is indicated by 55 in the LED display; 77 or CX indicates a handshake error was detected.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
ERROR C1	4-4, 4-1	The ACIA is reset, it is set to operate at 9600 baud, sending 8 bits, 1 stop bit and the clock is 16X the baud rate. The RTS (DTR) lead is set high. This lead is strapped to CTS and DCD leads via an adapter. The DC D status (FFX0) is read and if not found high, an error occurs. Possible areas of problem are: ACIA (U741) control line drivers U911, U931, U737, p-bus interface IC's U391, U691, U191, U277, U681, U677, U781, U977, U877, U971.
ERROR C2	4-4	CTS line is tested much the same way as DCD line. If it is not found high, possible errors are: U737, U931, U731, RS-232 buffers.
ERROR C3	4-4, 4-1	RTS lead is now brought low, and DCD is interrogated. Error occurs if it is not found low. The problem areas are the same as for error C1.
ERROR C4	4-4	CTS should be low. If it is not, the error will stay on. The problem areas are the same as Error C2.
ERROR C5	4-4	256 characters 0 through FF are sent at 9600 baud rate out and received back. The interrupt request is interrogated (bit 8 at FFX0). When set, the receiver full is indicating received character. This character is then compared with character that was sent. Error indicates that character was either not sent and received, U741 (ACIA) clock circuitry U961, U951, U737, U941, U751, U851, U837, or the data multiplexers U931, U831, or the data buffers U731, U911 are faulty. The baud rate clocks are on pins 3 and 4 of U741.
ERROR C6	4-4	The baud rate is now set for 300 baud and Test 5 is repeated. This test takes around 10 seconds. The possible areas of error are baud rate registers, U751, U851, U951, U937 or U837 or U741 ACIA.
ERROR C8	4-1	ROM Checksum Error - Same as for GPIB error D3.

TEST: VECTOR GENERATOR TEST 1

SETUP: S341 to position 8, VECTOR GENERATOR 1 selected on Diagnostic Parameter Entry card, enter 03 on the PED switches, then enter 80 on the PED switches to run the tests.

DESCRIPTION: There are two sets of programs needed for the test. One resides in the 6800 address space, the other is accessed with the 8x300 processor. The 6800 inputs a command to the 8x300 and monitors proper response. In case of error, the 6800, the 8x300 or both will get into a scope loop and an error code will be displayed. The tests start from simpler hardware involvement and get more and more complex. Passing of lower order tests is a prerequisite for higher order tests. Passing of the vector generator tests is necessary for the motor and pen drive board tests. Vector generator tests require motor and pen drive board.

At the beginning of each vector generator test a P-bus handshake test is performed via the register at FDF0.

The CPU then performs a test of RAM top. If it is found to be less than 3K, not enough RAM is available and the test will terminate.

If the test continues, the 6800 restarts the 8x300, checks task complete interrupt flag, motion sinc interrupt flag, integration clocks 8x300 scratch RAM and the DMA Pointer Register. If any of these tests fail, an error code will be displayed, and a test will get into a loop.

COMPLETION/EXIT: Satisfactory completion is indicated by 55 in the LED display, 77 indicates a handshake error.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
ERROR 77	5-1	Handshake error. Following logic circuits are used to complete the handshake transaction: U225, U155, U290, U160, U65, U55, U155, U175, U180.
ERROR C2	5-1, 5-2, 5-3, 5-4	The Task Complete Interrupt Test failed. The 6800 first resets the 8x300 and starts it with a self test bit set (A6 at FDF0). If a flag is not set within a limited time period, the error is indicated. The 6800 starts the test again. The 6800 is looking for D7=1, D 6=0 at FDF1. Possible areas of error are: U245, U475, U555 or from the 8x300 family the U330 (8x300), U310, U510, U540 ROM's) U210, U510, U340, U235, U70, U225, U230, U240 or output interface U465, U355.
ERROR C3	5-1, 5-2, 5-3, 5-4	The motion sync interrupt flag test failed. This error involves same hardware as in Error 2. The 6800 looks for D7=0, D6=1 and D5=0 at FDF1. If not seen, the 6800 displays Error C3 on PED and loop all the way to the beginning of the test.
ERROR C4	5-1, 5-2, 5-3, 5-4	The motion error interrupt flag test failed. This error involves same hardware as Error 2. The 6800 looks for D7=0, D6=0 and D5=1 at FDF1. There is 128 usec delay between motion sync test and motion error test. The 6800 then loops all the way to the beginning of the test.
ERROR C5	5-4, 6-1	Integration Clock Error. If the 8x300 does not see integration clock, it loops on U565. The 6800 displays error C5 and loops waiting for test exit command (any PED key depressed). Presence of integration clock is signalled by task complete interrupt bits (D7=1, D6=0, D5=0 at FDF1). The integration clock originates from MCK-1 on Vector Generator, it is conducted into Motor/Pen Drive Board via Pin 15 on the P-bus. On Motor/Pen Drive it passes U15, U415, U515, U315, U115 and U425. It then returns via pin 16 on the P-bus as INTCK-1 to the Vector Generator Board where it is buffered by register U565.

Symptom/Logic	Schematic Reference	Check
ERROR C6	5-3	8x300 Scratch RAM test failed. The 8x300 tests one byte of RAM, if it fails, it will loop on read and write cycle of RAM at address 15. Task complete interrupt signals test OK. Otherwise, the 6800 goes into a wait loop after displaying Error C6. Pressing PED key CODE 03 will allow test to exit. Possible areas of error are U570, U310, U510 or U540, 8x300 (U330) or U340.
ERROR C7	5-2, 5-4	DMA Pointer Register (U480) test failed. The 6800 writes AA into U480. The 8x300 checks it and loops on it if it does not find the right data. The 6800 then displays error 7 and goes into wait loop. PED key CODE 03 depressed will exit the test. The hardware involved in this test U490, U480, U580, U355, U135, U140, U550.

TEST: VECTOR GENERATOR TEST 2

SETUP: S341 to position 8, VECTOR GENERATOR 2 selected on the Diagnostic Parameter Entry card, enter 80 on the PED switches.

DESCRIPTION: Same as Test #1 until after the top of RAM is found and test continues. General purpose DMA facility of the Vector Generator Hardware is tested. It supplies the 8x300 with the address to read via DMA and the 2's complement of the data which the diagnostics should read. It sends this information via FDF2 and looks for task complete flag (D7=1, D6=0, D5=0 at FDF1) which signals that 8x300 found the test ok. If the test is not successfully completed within several seconds, the processors will keep looping on the error DMA address.

NOTE

When the test is started an audible tone will be heard from the drive motors. This is normal and the tone will last several seconds (actual time duration depends on the amount of optional RAM in the plotter).

COMPLETION/EXIT: Satisfactory completion is indicated by 55 in the LED display; C8 or CB indicates an error occurred.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
ERROR C8	5-2, 5-4	The possible area of failure is U275 and U280 DMA address drive registers, U250, U165, DMA request registers and drivers U190, U555, U70, U75, U80, U85, U60, U170 and U185. The DMA processing hardware on the processor board U711, U821, U941, U875, U881-, U961, U945, U975, and U831 or the Systems RAM.
ERROR CB	5-2, 5-3, 5-4	Indicates bus error of the DMA CONTROLLER or any other bus error during the DMA cycle. There are two major reasons for bus handshake error during Vector Generator DMA cycle: a. The bus handshake is not supervised properly (ADSTBO not asserted or similar problems). The circuits involved are U190, U70, U85, U80, U60, U170, U185, U240. b. The controller has a defective address line and is actually addressing a memory area that does not exist or does not return handshake. The possible circuits that are defective are U560, U285, U280, U275, U260, U265, U270.

TEST: VECTOR GENERATOR TEST 3

SETUP: S341 to position 8, VECTOR GENERATOR 3 selected on the Diagnostic Parameter Entry card, enter 80 on the PED switches.

DESCRIPTION: Preliminary tests, same as in Vector Generator Test 1, through memory top. Then if the test continues, general purpose DMA write and read facility is tested. The 8x300 DMA writes low byte of address into each address space between 200 and memory top low byte of the address, DMA reads it and compares it. It sets the task complete flag (D7=1, D6=0, D5=0 at FDF1) if the test is successful. If the flag is not seen after few seconds, an error is indicated and the 8x300 and the 6800 keep testing at that address.

COMPLETION/EXIT: Satisfactory completion is indicated by 55 in the LED display; C9 or CB indicates an error was detected.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
ERROR C9	5-2	The write-0 signal is generated by U250 and U190.
ERROR CB	5-2, 5-3, 5-4	Indicates bus error of the DMA CONTROLLER or any other bus error during the DMA cycle. There are two major reasons for bus handshake error during Vector Generator DMA cycle: a. The bus handshake is not supervised properly (ADSTB0 not asserted or similar problems). The circuits involved are U190, U70, U85, U80, U60, U170, U185, U240. b. The controller has a defective address line and is actually addressing a memory area that does not exist or does not return handshake. The possible circuits that are defective are U560, U285, U280, U275, U260, U265, U270.

TEST: VECTOR GENERATOR TEST 4

SETUP: S341 to position 8, VECTOR GENERATOR 4 selected on Diagnostic Parameter Entry card, enter 03 followed by 80 on the PED switches.

DESCRIPTION: Preliminary tests are same as in Vector Generator Test #1, through the memory top test.

Then, if the test is allowed to continue, the queue pointer DMA facility of the Vector Generator is tested. The 6800 fills a 64 byte field with the low byte of the addresses. The 8x300 gets the address pointer and checks the contents of the field with the data that 6800 passes to it. When the task complete (interrupt flag is seen), the next field is tested.

COMPLETION/EXIT: Satisfactory completion is indicated by 55 in the LED display.

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
ERROR CA	5-2, 5-3, 5-4	Indicates that queue Pointer DMA test failed. And that the 8x300 could not match data in the memory with data expected. The same hardware is used during this test as during test #2. In addition, U270, U285, U260 and U265 are used.
ERROR CB	5-2, 5-3, 5-4	Indicates bus error of the DMA CONTROLLER or any other bus error during the DMA cycle. There are two major reasons for bus handshake error during Vector Generator DMA cycle: a. The bus handshake is not supervised properly (ADSTB0 not asserted or similar problems). The circuits involved are U190, U70, U85, U80, U60, U170, U185, U240. b. The controller has a defective address line and is actually addressing a memory area that does not exist or does not return handshake. The possible circuits that are defective are U560, U285, U280, U275, U260, U265, U270.

TEST: MOTOR AND PEN DRIVE TEST

SETUP: S341 to position 8, MOTOR & PEN DRIVE selected on Diagnostic Parameter Entry card, enter 03 followed by 80 to on the PED switches to start the test, enter 01 on the PED switches to select the CALIBRATION TEST, enter 02 to select the SYSTEM TEST.

The successful completion of Vector Generator Tests is a prerequisite for this test. Test starts with basic handshake and memory tests as the Vector Generator Tests.

Upon the selection of the Motor and pen drive tests, the display on PED will indicate that it sees the selection of either the calibration test or systems test by displaying code 01.

The calibration test is selected by entering code 01, the system test is selected by entering code 02. The tests can be alternately selected back and forth, and are completely aborted by entering 03.

The tests are described in detail on the following pages.

TEST: CALIBRATION (MOTOR AND PEN DRIVE TESTS cont.)

SETUP: Same as previous page, enter 01 on PED switches.

DESCRIPTION: Test is selected through the parameter entry switches. Once selected, the Vector Generator provides 1.08us MCK required to generate the conversion windows on the Motor/Pen Drive logic drive. Motion Enable (which originates on the Vector Generator card) is disabled, forcing the three axes of motor data and pen data to zero. Calibration of the M/P Drive D/A circuits is monitored on the sine and cosine test points of the motor references.

COMPLETION/EXIT: Verify a maximum of 80mV on the following test points:

TP 430
TP 335
TP 330

Adjust R530 for 8 V $\pm$1% on the following test points:

TP 440
TP 345
TP 340

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
Voltages out of tolerance	6-2	U431, U441, U335, U336, or U435 may be faulty.

TEST: SYSTEM TEST (MOTOR AND PEN DRIVE TEST cont.)

SETUP: Same as previous test, enter 02 on PED switches.

DESCRIPTION: Axis movement and pen activations are generated on the Vector Generator and translated to physical movement by the axis motors and the Motor/Pen drive module. Movement of axis will be at a constant 2IPS (inches per second) with no acceleration or deceleration. As the pen assembly moves in a triangular pattern, the pens are enabled and disabled, resulting in the pattern shown in Figure 3-5.

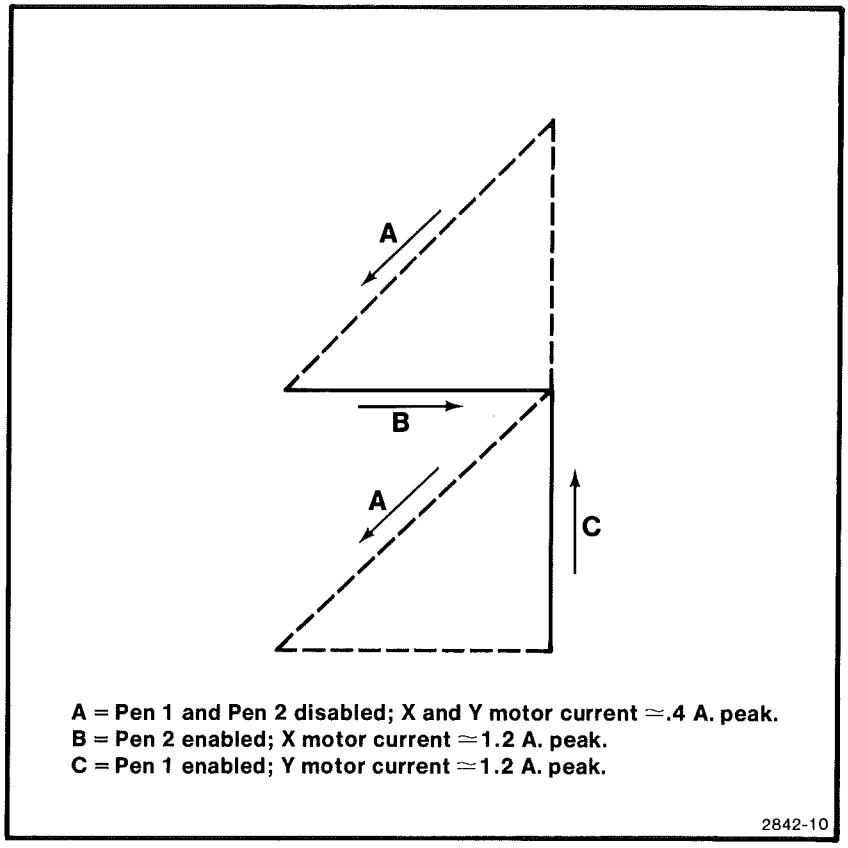


Figure 3-5. Motor/Pen Drive System Test Pattern. Dashed lines indicate movement of disabled pen(s). Solid lines indicated movement of enabled pen.

COMPLETION/EXIT: Operation is continuous until 03 is entered on the PED switches. An 05 in the LED display indicates satisfactory completion (also check the actual pattern drawn on the plotter for proper operation of the Motor/Pen Drive logic).

TROUBLE ISOLATION CHART:

Symptom/Logic	Schematic Reference	Check
FUSE blown	6-3	A fault is indicated, if any motor does not turn or if any pen does not draw. If a motor does not turn, and a fuse is blown on Motor and Pen drive board, the associated drive transistors are probably destroyed. From the schematics locate and then check and replace bad drive transistors. Associated with the bad motor and replace blown fuse.
Fuse not blown	5-4, 6-1, 6-2	If none of the motors turn and fuses are not blown, check U370, U375, U365 and U383 on Vector Generator, U215, U244, U325, U125, U135 and U431 on Motor and Pen Drive board. Check test points TP340, TP330, TP335, TP345, TP430 and TP440 for presence of Haversine patterns, when triggering an oscilloscope at approximately 2 ms/div. The signals should be approximately 8V p-p. Check U335, U336, U435, U441, U525, U535 and U431 if these signals are not seen. High current should be enabled. If the amplitude of these signals is 4V p-p, the low current shift logic is enabled. Check U215, U415, U525 and Q530.

Symptom/Logic	Schematic Reference	Check
Fuse not blown (cont)	6-2, 6-3	Check for sawtooth signal on emitter of Q242 of frequency of 33 KHZ and 4V p-p. Check Q235, Q234 and Q242 if the signal is not present. Check U561, U361, U161, U461, U565, U261, U365, U61 and U165.
Pen not operating	5-4, 6-1, 6-2, 6-4	Check U380 on Vector Generator board, U525, U441 and U235 on Motor and Pen Drive board. The TP230 should be switching between approx. 0 and 8V. U125-6 should also be switching at logic levels. Check U125. Check U525, U25, U15, Q184, Q185, U191, Q85 and Q95.

TEST: MEDIA ADVANCE

SETUP: S341 to position 8, MEDIA ADVANCE selected on the Diagnostic Parameter Entry card, enter 80 on the PED switches.

DESCRIPTION: Handshake of the Media Advance board is first tested via the register at FDC1. The processor keeps loading the value of the optical scanner and storing it at location 10C. It also keeps turning the magnetic field of the media advance stepping motor (via U530 at address FDC1).

COMPLETION/EXIT: 77 on the LED display indicates a handshake error was detected. Normally the paper should continue to advance until 03 is entered on the PED switches.

TROUBLE ISOLATION CHART:

Symptom/Logic	**Schematic Reference**	**Check**
Handshake Error (77 on LEDs)	21-1	Check U760, U860, U580, U480, U660, U680, U780, U560.
Motor does not turn	21-1	Check U460, U530, U330, Q125, Q225, Q255 or Q155.

RESTORING THE PLOTTER TO NORMAL OPERATION

When all tests have been completed (and plotter operation has been verified), the plotter should be returned to normal operation. This is accomplished by the following steps.

1. Turn off power to the plotter.
2. Remove the Diagnostic Parameter Entry card and install the standard Parameter Entry card.
3. Remove the Diagnostic Test Fixture board and install the ROM Patch board (if applicable).
4. Replace the access cover over the ROM Patch board (by fitting the cover into the opening and pressing gently until it snaps into place).
5. Return the Parameter Entry Device, Timer Interrupt, and Vector Generator board Interrupt Straps to the proper settings (as recorded when performing the initial setup to run these tests).
6. Remove the Processor and Extender boards from the card cage, and reinstall the Processor board.
7. Close the platen.
8. The plotter is now ready for normal operation by the customer.

NOTE

It may be necessary to reload the operating parameters before the customer uses the plotter. These parameters and the contents of RAM may have been destroyed when running the diagnostic tests.

Section 4

THEORY OF OPERATION

P-BUS DIAGNOSTICS BOARD - FUNCTIONAL DESCRIPTION

The Diagnostics board contains hardware necessary to select and perform tests to determine the hardware condition of the P-Bus System.

The board occupies the same space as provided for the ROM Patch board B. This space, located in slot above parameter entry device, is user accessible. The ROM Patch board (if present) has to be removed from that slot in order to insert the Diagnostics Board. A block diagram of the Test Fixture is shown in Figure 4-1.

The user has an access to RESTART Switch (S331) which resets the whole system when depressed. Rotary switch S341 is provided to select an appropriate test. When in position 0, the diagnostics board is transparent to the P-Bus system with the exception of the RESTART switch. When in position 1, the diagnostics board asserts PGODIS-0, DDIS-0 and 01 (NOP Code) on data bus. This will force the processor unit to increment address lines. The address lines can be monitored on the 16 square pins of J3. Two square pins (J4) are provided for ground reference for test equipment, since system chassis ground may not be common to signal ground. When Rotary switch S341 is in positions 2 through F, and PGODIS-0 signal is in logic level 1, the Diagnostics hardware overlays ROM0, ROM2 and ROM3 by asserting DDIS-0 and data on the MD-0 to MD-7 bus.

The hexadecimal value of the switch position is presented as a lower nibble in address space C000 through C7FF.

The board contains sockets for three 16K EPROMs (TMS 2716). These EPROMs may contain up to 6K bytes of program, and are activated when PGODIS-0 signal is high, test select switch S-341 is in position 2 through F, and the processor addresses area F000 - F7FF or D000 - DFFF. The plotter firmware is disabled and the tests stored in the Diagnostic Test Fixture EPROMs are run.

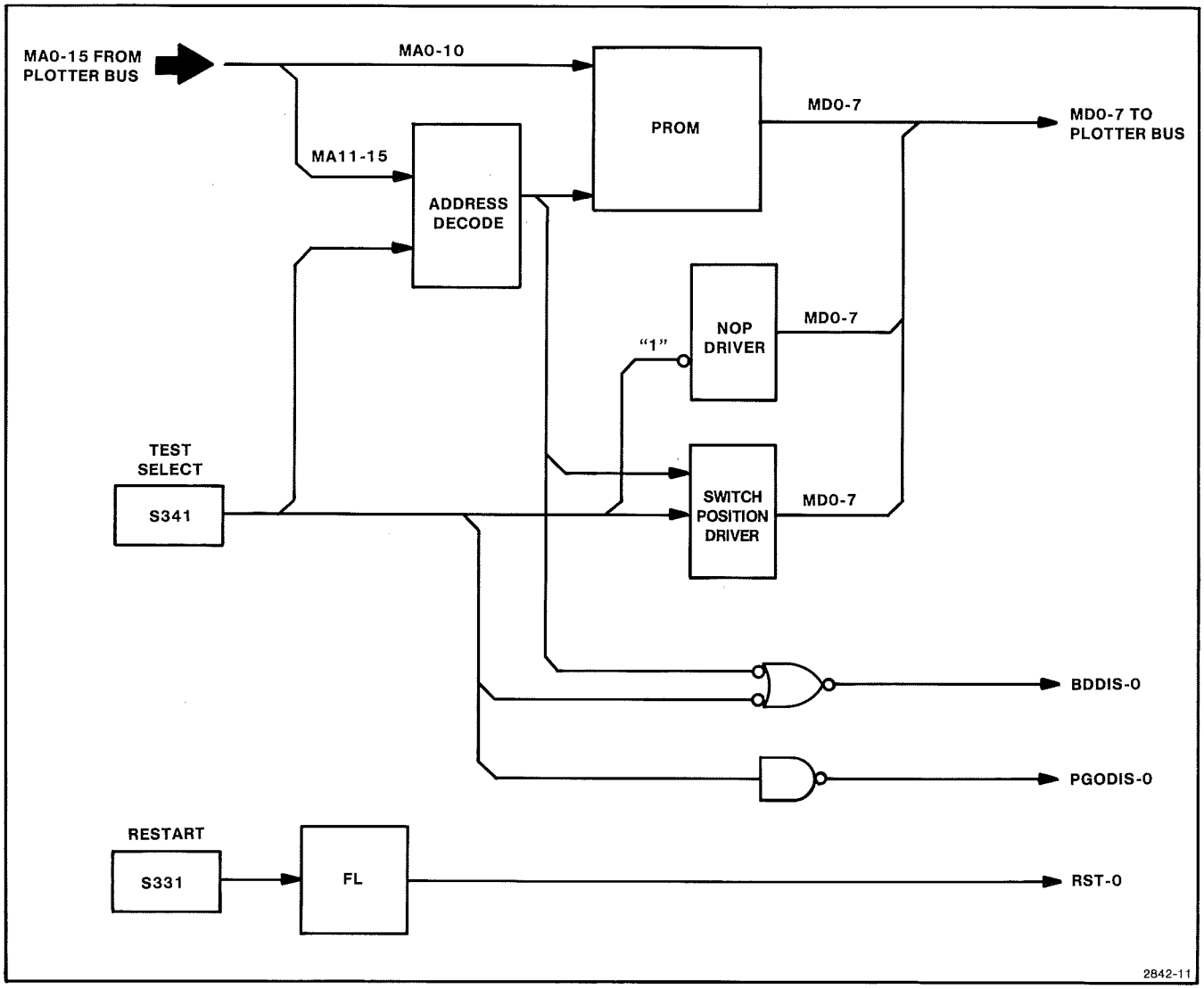


Figure 4-1. Diagnostic Test Fixture Block Diagram.

Section 5
REPLACEABLE PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

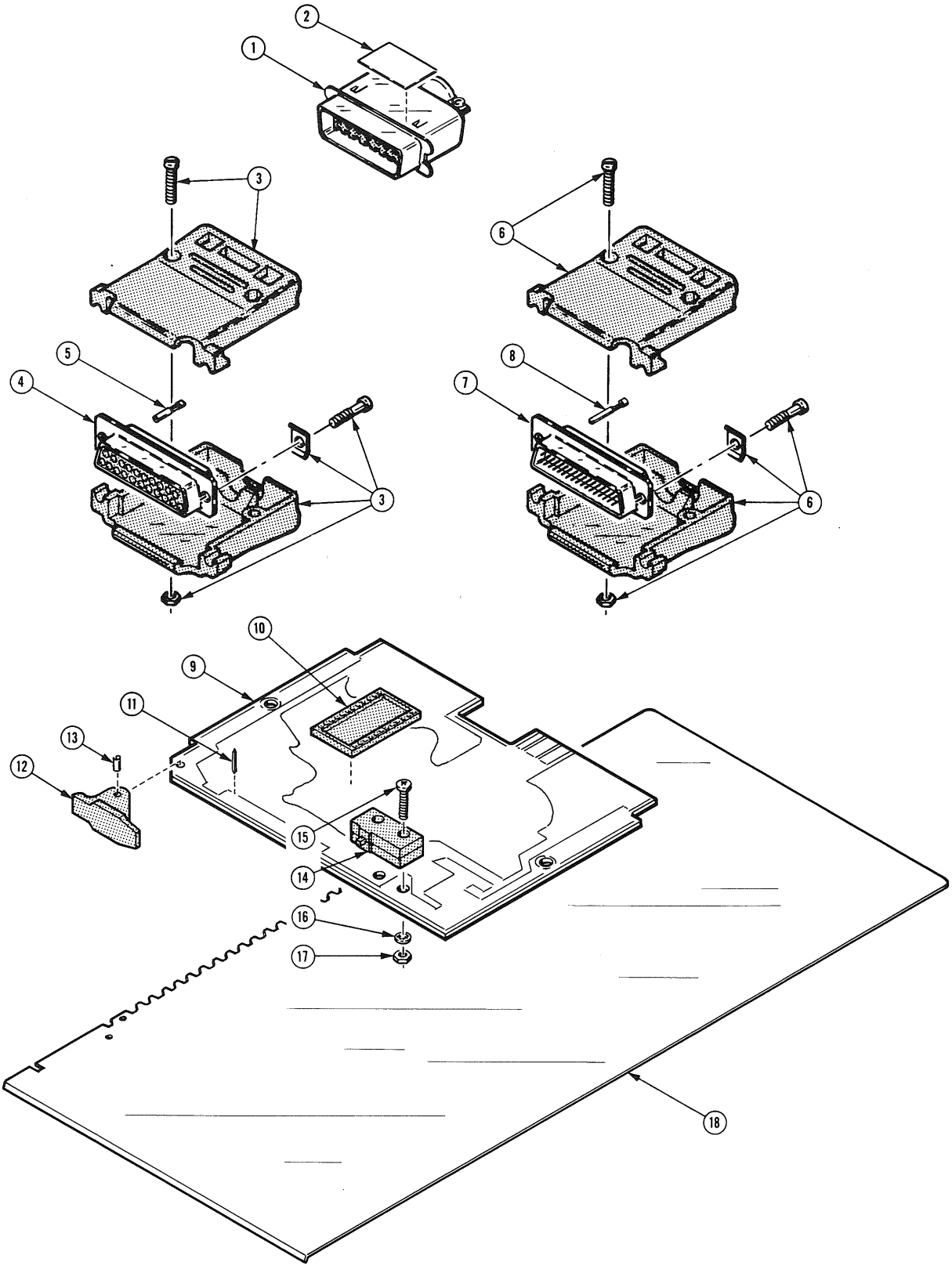
"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
01963	CHERRY ELECTRICAL PRODUCTS CORPORATION	3600 SUNSET AVENUE	WAUKEGAN, IL 60085
07111	PNEUMO DYNAMICS CORPORATION	4800 PRUDENTIAL TOWER	BOSTON, MA 02199
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
71785	TRW, CINCH CONNECTORS	1501 MORSE AVENUE	ELK GROVE VILLAGE, IL 60007
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-5222-01			CKT BOARD ASSY:DIAGNOSTIC	80009	670-5222-01
C11	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
C31	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
C101	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C103	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C105	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C107	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C109	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C111	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C113	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C120	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	56289	502D226
C131	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C201	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C205	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
C211	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8005D9AABZ5U104M
J3	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL (QUANTITY OF 16)	22526	47357
J4	131-0608-00 ----- -----			TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL (QUANTITY OF 2)	22526	47357
R121	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
R221	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
R241	307-0502-00			RES,NTWK,THK FI:1.8 OHM,20%,(9) RES	91637	CSP10E01182M
R321	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
S331	260-0760-00			SWITCH,SENS:10A,250V,SPDT,SNAP ACTION	01963	E62-10A
S341	260-1777-00			SWITCH,ROTARY:16 POSN,28VDC,100MA	00779	53137-1
U101	160-0213-02			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGRM	80009	160-0213-02
U105	160-0269-02			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGRM	80009	160-0269-02
U111	160-0214-01			MICROCIRCUIT,DI:2048 X 8 EPROM,PRGRM	80009	160-0214-01
U121	156-0914-00			MICROCIRCUIT,DI:OCT ST BFR W/3-STATE OUT	80009	156-0914-00
U131	156-0956-00			MICROCIRCUIT,DI:OCTAL BFR W/3STATE OUT	80009	156-0956-00
U141	156-0403-00			MICROCIRCUIT,DI:HEX. INV W/OPEN COLL OUTPS	01295	SN74S05N
U205	156-0460-00			MICROCIRCUIT,DI:QUAD 2 INP AND GATE	07263	7409PC
U211	156-0469-00			MICROCIRCUIT,DI:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
U221	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	013-0186-00			1		ADAPTER ASSY:SELF TEST,24 PIN MALE	80009	013-0186-00
	131-0325-00			1		. CONN,PLUG,ELEC:24 CONTACT,MALE	71785	57-30240(398)
-2	334-3682-00			1		. MARKER IDENT:MRKD SELF TEST ADAPTER	80009	334-3682-00
	013-0185-00			1		ADAPTER ASSY:SELF TEST,25 PIN,FEMALE	80009	013-0185-00
-3	200-1667-00			1		. COVER,ELEC CONN:25 POSN,W/HDW	00779	206472-1
-4	131-1461-00			1		. CONNECTOR BODY,:25 FEMALE CONTACT POSN	00779	205207-1
-5	131-1279-01			2		. CONTACT,ELEC:FEMALE	00779	205311-4
	131-1451-00			1		. CONTACT,ELEC:CONN FEMALE,CU ALY,GOLD PL	00779	205201-6
	013-0184-00			1		ADAPTER ASSY:SELF TEST,25 PIN,MALE	80009	013-0184-00
-6	200-1667-00			1		. COVER,ELEC CONN:25 POSN,W/HDW	00779	206472-1
-7	131-1316-00			1		. CONNECTOR BODY,:25 MALE-CONT POSITIONS	00779	205208-1
-8	131-1279-00			4		. CONTACT,ELEC:MALE,28-24 AWG WIRE,0.040 DIA	00779	205310-4
-9	----- -----			1		CKT BOARD ASSY:DIAGNOSTIC(SEE A1 EPL)		
-10	136-0743-00			2		. SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PROFILE		
-11	131-0608-00			18		. TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL	22526	47357
-12	105-0160-02			1		. EJECTOR,CKT CD:BLUE PLASTIC	80009	105-0160-02
						(ATTACHING PARTS)		
-13	214-1337-00			1		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
						- - - * - - -		
-14	----- -----			1		. SWITCH:(SEE S331 EPL)		
						(ATTACHING PARTS)		
-15	211-0185-00			2		. SCREW,MACHINE:2-56 X 0.438",PNH,STL	07111	OBD
-16	210-0001-00			2		. WASHER,LOCK:INTL,0.092 ID X 0.18"OD,STL	78189	1202-00-00-0541C
-17	210-0405-00			2		. NUT,PLAIN,HEX.:2-56 X 0.188 INCH,BRS	73743	2X12157-402
						- - - * - - -		
-18	334-3619-00			1		CARD,PRMTR,DIAG:MRKD W/OPERATOR INFO	80009	334-3619-00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Section 6
SCHEMATIC AND DIAGRAM

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF).
Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

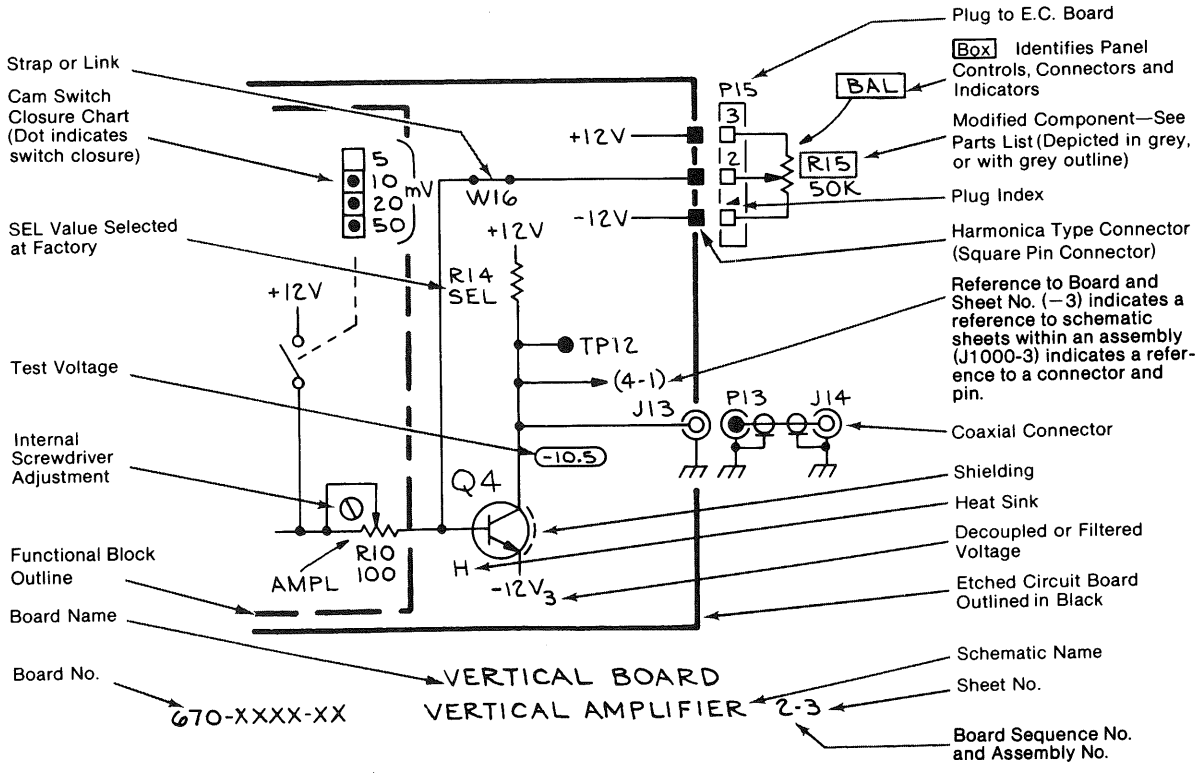
Abbreviations are based on ANSI Y1.1-1972.
Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc)
AT	Attenuator, fixed or variable
B	Motor
BT	Battery
C	Capacitor, fixed or variable
CB	Circuit breaker
CR	Diode, signal or rectifier
DL	Delay line
DS	Indicating device (lamp)
E	Spark Gap, Ferrite bead
F	Fuse
FL	Filter
H	Heat dissipating device (heat sink, heat radiator, etc)
HR	Heater
HY	Hybrid circuit
J	Connector, stationary portion
K	Relay
L	Inductor, fixed or variable
M	Meter
P	Connector, movable portion
Q	Transistor or silicon-controlled rectifier
R	Resistor, fixed or variable
RT	Thermistor
S	Switch or contactor
T	Transformer
TC	Thermocouple
TP	Test point
U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
V	Electron tube
VR	Voltage regulator (zener diode, etc.)
W	Wirestrap or cable
Y	Crystal
Z	Phase shifter

The following special symbols may appear on the diagrams:



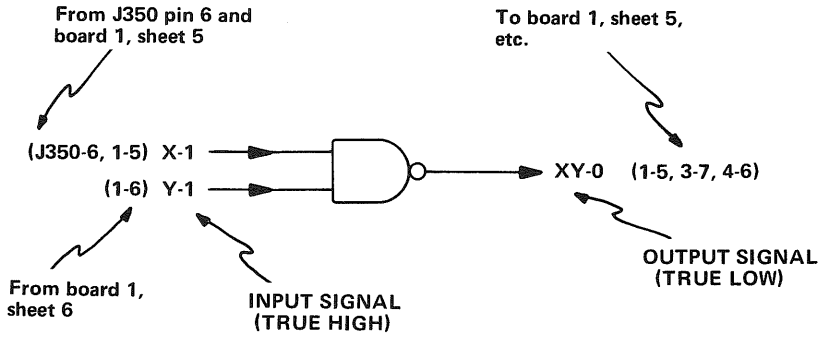
1. TRUE HIGH and TRUE LOW Signals

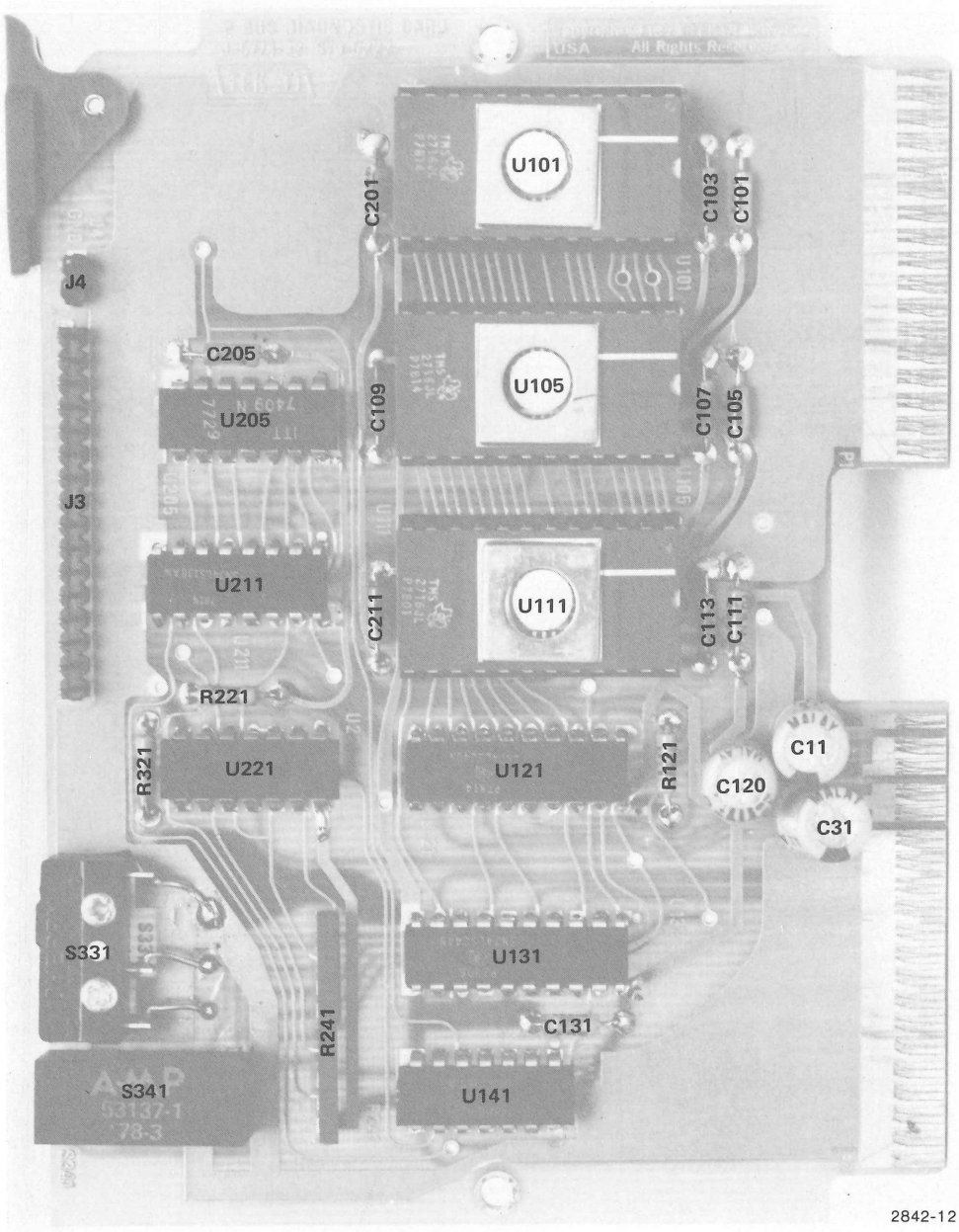
Signal names on the schematics are followed by −1 or −0. A TRUE HIGH signal is indicated by −1, and a TRUE LOW signal is indicated by −0.

SIGNAL−1 = TRUE HIGH
SIGNAL−0 = TRUE LOW

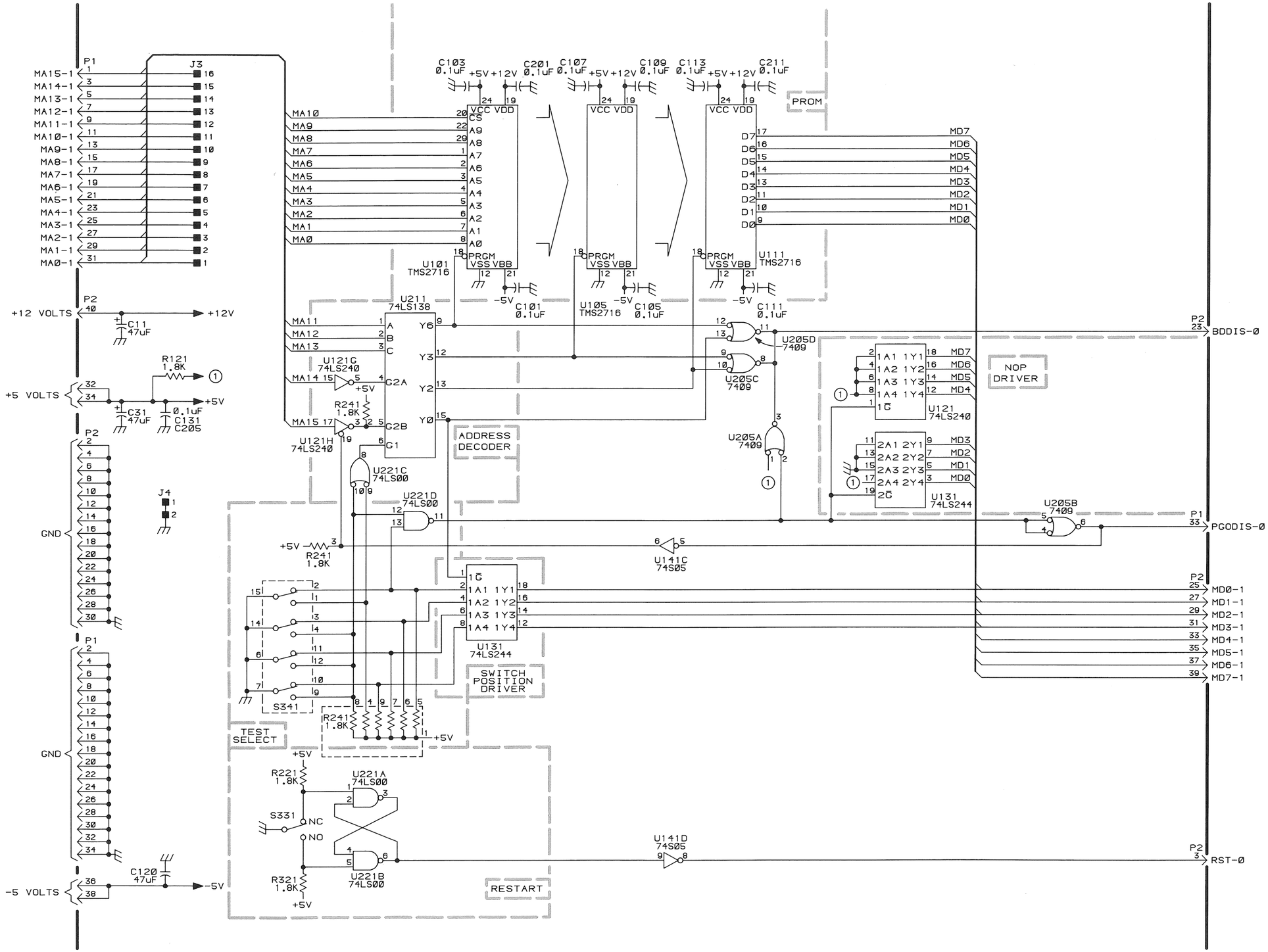
2. Cross-References

Schematic cross-references (from/to information) are included on the schematics. The "from" reference only indicates the signal "source," and the "to" reference lists all loads where the signal is used. All from/to information will be enclosed in parentheses.





Diagnostic Card Component Location (670-5222-00).



DIAGNOSTIC CARD
670-5222-00

067-0859-00
(FOR USE WITH 4663)

@
2842-1

670-5222-00 DIAGNOSTIC CARD