35MHz four channel digital oscilloscope
PM3305(U)

Service Manual

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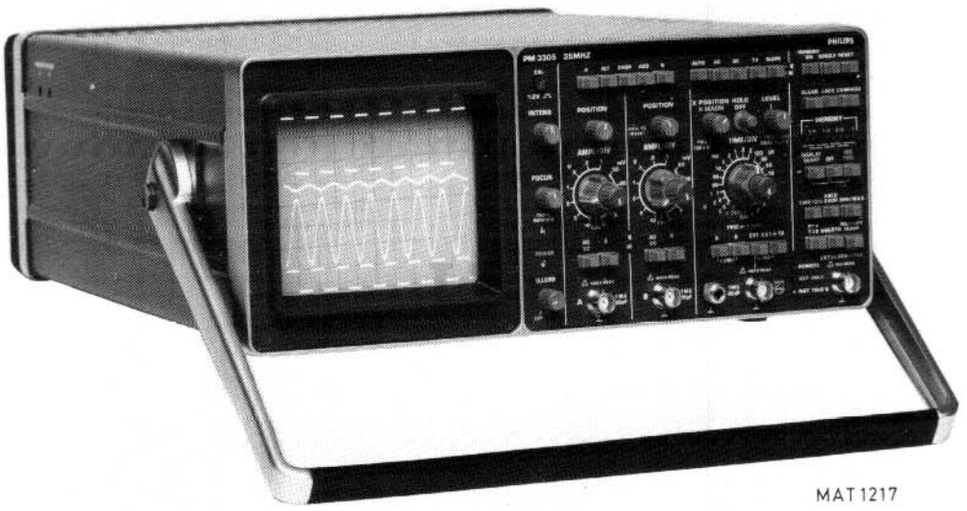

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WARNING! These servicing instructions are of use by qualified personnel only. To reduce the risk of electric shock do not perform any servicing other then that specified in the Operating Instructions unless you are fully qualified to do so.

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LIST OF FIGURES

1. SAFETY INSTRUCTIONS

Read these pages carefully before installation and use of the instrument.

The following clauses contain information, cautions and warnings which must be followed to ensure safe operation and to retain the instrument in a safe condition.
Adjustment, maintenance and repair of the instrument shall be carried out only by qualified personnel.

1.1. SAFETY PRECAUTIONS

For the correct and safe use of this instrument it is essential that both operating and servicing personnel follow generally-accepted safety procedures in addition to the safety precautions specified in this manual.
Specific warning and caution statements, where they apply, will be found throughout the manual.
Where necessary, the warning and caution statements and/or symbols are marked on the apparatus.

1.2. CAUTION AND WARNING STATEMENTS

CAUTION: is used to indicate correct operating or maintenance procedures in order to prevent damage to or destruction of the equipment or other property.

WARNING: calls attention to a potential danger that requires correct procedures or practices in order to prevent personal injury.

1.3. SYMBOLS

	High voltage $\geq$ 1000 V	(red)
	Live part	(black/yellow)
	Read the operating instructions.	(black/yellow)
	Protective earth (grounding) terminal	(black)

1.4. IMPAIRED SAFETY-PROTECTION

Whenever it is likely that safety-protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation. The matter should then be referred to qualified technicians.
Safety protection is likely to be impaired if, for example, the instrument fails to perform the intended measurements or shows visible damage.

1.5. GENERAL CLAUSES

1.5.1. WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts and accesible terminals which can be dangerous to live.

1.5.2. The instrument shall be diconnected from all voltage sources before it is opened.

1.5.3. Bear in mind that capacitors inside the instrument can hold their charge even if the instrument has been separated from all voltage sources.

1.5.4. WARNING: Any interruption of the protective earth conductor inside or outside the instrument, or disconnection of the protective earth terminal, is likely to make the instrument dangerous. Intentional interruption is prohibited.

1.5.5. Components which are important for the safety of the instrument may only be renewed by components obtained through your local Philips organisation. (See also section 8).

1.5.6. After repair and maintenance in the primary circuit, safety inspection and tests, as mentioned in Section 8 have to be performed.

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2. GENERAL INFORMATION

2.1. INTRODUCTION

The PM 3305 Digital Storage oscilloscope is a compact instrument, featuring ergonomic design and extensive measurement capabilities.

A large 8x10 screen, with internal graticule lines, provides easier viewing and an 10 kV accelerating potential gives a high intensity trace with a well-defined spot.

As a real time oscilloscope the PM 3305 is characterised by the following features:
- 2 mV/div sensitivity at 35 MHz.
- A wide choice of display modes, including the an ADD facility.
- X/Y display.
- TV triggering.

As a digital storage oscilloscope the versatile circuit arrangement, combined with the software for the microprocessor offers a wide range of facilities, including:
- Brilliant display.
- Excellent resolution because of 4K x 8 bits memory to be displayed on one full screen.
- 4k bytes pre-trigger view (one screen).
- COMPARE mode.
- MIN/MAX mode.
- 4 Channels.
- Max. 8 signals on the screen in COMPARE mode.
- 2 MHz AD conversion rate (maximum).
- IEEE-488 interface option.

The instrument operates on an a.c. mains voltage of 100 V, 120 V, 220V or 240V. In addition, field applications for the oscilloscope are facilitated by external battery operation.

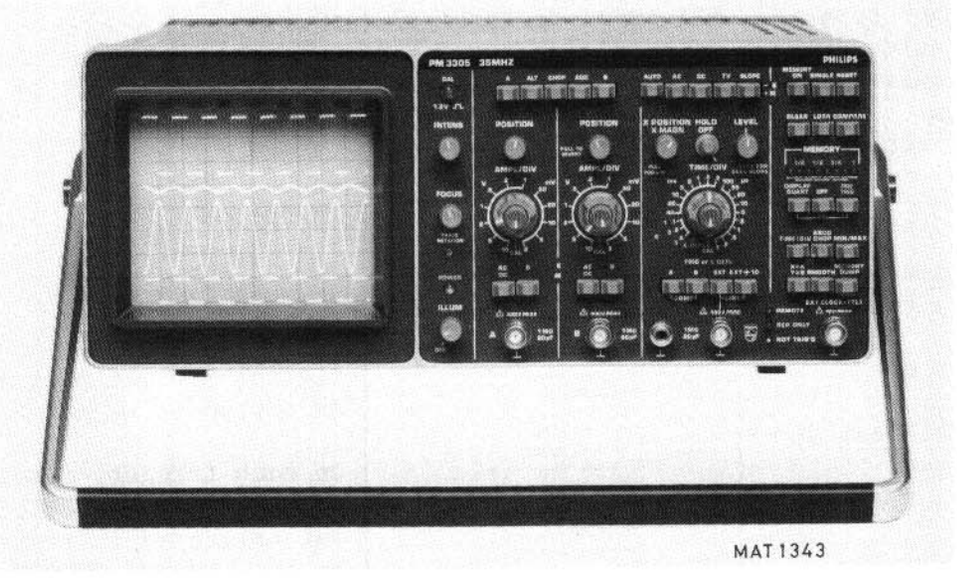


FIG. 2.1. 35 MHz Digital storage oscilloscope PM 3305

2.2. CHARACTERISTICS

A. Performance Characteristics

-Properties expressed in numerical values with stated tolerance are guaranteed by N.V. Philips' Gloeilampenfabrieken. Specified non-tolerance numerical values indicate those that could be nominally expected from the mean of a range of identical instruments.
-This specification is valid after the instrument has warmed up for 30 minutes (reference temperature 23°C).

B. Safety Characteristics

This apparatus has been designed and tested in accordance with Safety Class I requirements of IEC Publication 348, Safety Requirements for Electronic Measuring Apparatus, UL 1244 and CSA 556B, and has been supplied in a safe condition.

C. Initial Characteristics

-Overall dimensions:
 .Height (excluding feet) : 137 mm.
 .Width (excluding handle) : 337 mm.
 .Depth (excluding controls) : 452 mm.

-Maximum Weight (Mass) : 11 kg.

-Operation position a) horizontally on bottom feet
b) vertically on rear feet
c) any angle between a) and b)

2.2.1. Cathode ray tube:

-Type	D14-125 GH/117
-Total accelerating voltage	10 kV
-Screen	8x10 cm, metal-backed (1 div. equals 1 cm)
-Phosphor type	P31 (GH). Optional P7 (GM).
-Graticule	internal
-Graticule illumination	continuously variable
-Trace rotation	screwdriver adjusted

2.2.2. Operation modes:

	MEMORY OFF	MEMORY ON
-Memory off	Only analog part in operation	
-Memory on		Digital storage part in operation
-SINGLE not depressed		On each trigger, memory contents are overwritten Not triggered is indicated by the LED NOT TRIG'D
-SINGLE depressed		After "RESET" memory contents are overwritten on first trigger pulse received. Armed status is indicated by the LED "NOT TRIG'D"

		MEMORY OFF	MEMORY ON
	-Direct/sampling		With time-base setting, sampling mode or direct mode is selected automatically depending on sweep speed. For time-base 100 µs/div. to 0,1 µs/div. the "REP ONLY" LED indicates that sequential sampling is selected.
2.2.3.	Vertical:		
	-Number of channels	2 channels (A and B)	2 channels (A and B) and 2 auxiliary channels (C and D)
	-Channel display/ acquisition modes	A only	A only
		±B only	±B only
		A and ±B alternated	
		A and ±B added	A and ±B added
		A and ±B chopped	A and ±B chopped Pushing ALT or CHOP gives chop mode, except with MIN/MAX pushed. This gives alternate mode for A and B
			A, ±B, C and D chopped
			AvsB (A=X,Y=B)
	-Polarity inversion	Channel B can be inverted	Channel B can be inverted
	-Chopping frequency	≈ 500 kHz	Depends on sampling frequency
	-Display time per channel	≈ 600 ns	
	-Acquisition		
	-Compare		50 % of memory capacity is displayed continuously (each second dot on screen) The other memory places are displayed and continuously refreshed. Each time that the COMPARE button is released and pressed again, the compare memory is filled with the latest information in the active memory.
	-Min/Max		When button is depressed 2 peak detectors are operative. Maximum peaks are stored on each second clock-pulse. Minimum peaks on the other clock pulses. Works for channel A, ±B or A and ±B alternated.
	-Dynamic range		
	-channel A and B	24 divisions for frequencies ≤ 10 MHz	24 divisions for frequencies ≤ 10 MHz
	-channel C and D		10 divisions

	MEMORY OFF	MEMORY ON
-Bandwidth		
-channel A and B (DC)	DC - 35 MHz	DC - 35 MHz (-3 dB)
-channel A and B (AC)	2Hz - 35 MHz	2Hz - 35 MHz (-3 dB)
-in Min/Max respectively		DC - 30 MHz (-3 dB) 2Hz - 30 MHz (-3 dB)
-channel C and D		DC - 1 MHz (-3 dB)
-Risetime		
-channel A and B	< 10 ns	< 10 ns
-in Min/Max		< 11,6 ns
-channel C and D		< 350 ns
-Pulse aberrations		
-channel A and B (testpulse 6 div risetime 1 ns)	< ± 3% (peak-peak < 4%)	< ± 4% (peak-peak < 5%)
-channel C and D (testpulse 6 div risetime 1 ns)		< ± 3%
-Deflection coefficients		
-channel A and B	2mV - 10V per division 1-2-5 sequence	2mV - 10V per division 1-2-5 sequence
-channel C and D		0,1V/div (rear BNC) 1,0V/div (rear BNC)
-Continuous control (non calibrated)		
-channel A and B	1 : > 2,5	1 : > 2,5
-Vertical positioning		
-channel A and B	> ± 8 divisions	> ± 8 divisions
-channel C and D		> ± 5 divisions
-Input impedance		
-channel A and B	1Mohm // 20pF	1Mohm // 20 pF
-channel C and D		10 Kohm ± 3%
-Input coupling		
-channel A and B	AC-O-DC	AC-O-DC
-channel C and D		DC
⚠ -Maximum rated input voltage		
-channel A and B	400V (dc + ac peak) below 100 kHz	400V (dc + ac peak) below 100 kHz
⚠ -Maximum rated input voltage		
-channel C and D	42V (dc + ac peak) below 100 kHz	42V (dc + ac peak) below 100 kHz
-Deflection accuracy		
-channel A and B	< ± 3%	< ± 4%
-channel C and D		< ± 3%
-CMRR		
-In A-B mode after adjustment at DC.	> 40 dB at 1 MHz	> 40 dB at 1 MHz
-channel C and D		> 50 dB at 50 KHz

	MEMORY OFF	MEMORY ON
-Rated common mode voltage		
-channel C and D		< ± 20V
at 0,1 V/div at 1,0 V/div		see maximum rated input voltage
-Trace jump		
-attenuator control	< 0,1 div	< 0,1 div
-between 10mV -> 20mV/div	< 1 div	< 1 div
-continuous control	< 0,5 div	< 0,5 div
-normal/invert channel B	< 1 div	< 1 div
-memory ON/OFF	< 0,3 div	< 0,3 div
-temperature drift at 23°C	< 0,3 div/hour	< 0,3 div/hour
-Crosstalk between channels	> -40 dB at 10 MHz > -30 dB at 35 MHz	> -40 dB at 10 MHz > -30 dB at 35 MHz
-Linearity error reference IEC 351	< 3%	< 3%
2.2.4. Horizontal:		
-Time-base		
-time coefficients	0,5 s/div to 0,1 µs/div 1-2-5 sequence	0,5 s/div to 0,1 µs/div and 5 s/div to 1 s/div when TIME/DIV is depressed 1-2-5 sequence
-continuous control	1 : > 2,5 (uncal)	1 : > 2,5 (uncal) works only for the time-base settings 100 µs/div to 0,1 µs/div.
-magnifier	x 10 calibrated	x 10 calibrated
-positioning	> ± 5 divisions	> ± 5 divisions
-coefficient accuracy		
-x 1	< ± 3%	< ± 3%
-additional magnifier x 10	< ± 2% (first div. excluded)	< ± 2% (first div. excluded)
-resolution		
-single trace		400 samples/div.
-dual trace		200 samples/div.
-four trace		100 samples/div. in COMPARE respectively 200 samples/div. 100 samples/div. 50 samples/div.
-maximum conversion frequency		2 MHz
-visible signal delay	> 1,5 divisions at 10 ns/div	> 2 divisions at 10 ns/div.

	MEMORY OFF	MEMORY ON
-trace jump		
-Memory ON/OFF		
-5s/div...		
0,5ms/div.	< 0,3 div (in x 1)	< 0,3 div (in x 1)
-0,2ms/div...		
0,1 µs/div	increasing to < 0,8 div (in x 1)	increasing to < 0,8 div (in x 1)
-X-Deflection		
-source	channel A, channel B, EXT, EXT : 10 or LINE, selected by trigger-source switch	
-deflection coefficients		
-channel A or B	as selected by AMPL/DIV rotary switch	
-EXT	0,2V/div	
-EXT : 10	2V/div	
-LINE	> 8 div	
-bandwidth		
-DC	DC to 1 MHz	
-AC	5 Hz to 1 MHz	
-phase shift between X and Y	< 3^{o} at 100 kHz	
-dynamic range	24 divisions up to 100 kHz	
-deflection accuracy	< ± 10%	
2.2.5. Triggering:		
-source	channel A, channel B external, external : 10, line and composite	channel A, channel B external, external : 10, line. (No composite)
-mode	AUTO (free-run in absence of trigger after 100 ms; see also level range)	AUTO (free-run in absence of trigger after 100 ms; see also level range)
	AC coupled	AC coupled
	DC coupled	DC coupled
	TV (TV line or frame switched by TIME/DIV rotary switch).	TV (TV line or frame switched by TIME/DIV rotary switch).
	TV line :< 20 µs/div	TV line :< 20 µs/div
	TV frame:> 50 µs/div	TV frame:> 50 µs/div
-trigger bandwidth		
-AUTO	20 Hz - 50 MHz	20 Hz - 50 MHz
-AC	5 Hz - 50 MHz	5 Hz - 50 MHz
-DC	0 - 50 MHz	0 - 50 MHz
-trigger sensitivity		
-internal	< 1/2 div at 5 MHz	< 1/2 div at 5 MHz
-internal	< 1 div at 35 MHz	< 1 div at 35 MHz
-external		
(external : 10)	< 0,2 (2) Vpp at 35 MHz	< 0,2 (2) Vpp at 35 MHz
	< 0,1 (1) Vpp at 5 MHz	< 0,1 Vpp at 5 MHz
-TV internal	< 0,7 div sync. pulse amplitude	< 0,7 div sync pulse amplitude
-TV external		
(external : 10)	< 0,15 (1,5) V sync pulse amplitude	< 0,15 (1,5) V sync pulse amplitude

	MEMORY OFF	MEMORY ON
-trigger level range		
-AUTO	proportional to peak-peak value of trigger signal	proportional to peak-peak value of trigger signal
-internal	> ± 6 div	> ± 6 div
-external	> ± 0,8 V	> ± 0,8 V
-external : 10	> ± 8 V	> ± 8 V
-trigger slope		
- + or -	pos/neg-going	pos/neg-going
-dual		works from 5s to 0,2ms/div trigger occurs when signal goes out of a fixed window of > ± 0,5 div; window can be shifted by LEVEL
-external trigger input impedance	1 Mohm // 20 pF	1 Mohm // 20 pF
⚠ -maximum rated input voltage	400V (dc + ac peak) below 100 kHz.	400V (dc + ac peak) below 100 kHz.
-pre trigger		trigger point can be set on beginning, 1/4, 1/2, 3/4 and end of screen.
2.2.6. Memory:		
-number of memories		1
-resolution horizontal		1 : 4096 (max)
-resolution vertical		1 : 256 (8 bits)
-memory modes		
-CLEAR		first push clears the memory, trace in middle of screen; second push (within ≃ 1 second) blanks the trace
-LOCK		memory input is blocked
2.2.7. Display:		
-memory		covers 10 cm screen height
-horizontal expand		4 x 7 overlapping memory quarters can be selected (with X-MAGN 40 x)
-channel B versus channel A		
-mode		X=A/Y=B
-accuracy		< ± 5%
-phase difference		distance between signal derived from A and signal derived from B is 1/400 div.; the mean of two adjacent B values is displayed versus one A value

		MEMORY OFF	MEMORY ON
	-position		0 of stored A signal will be at centre of screen
	-smooth		Switches RC-filter in display channel with time-constant of 7 /us.
2.2.8.	External clock:		
	-input levels (TTL)		
	-V_{IL}		< 0,8 V
	-V_{IH}		> 2,8 V (at I_I < 0,8 mA)
	-frequency		1 MHz max.
	-switching to external clock		freq > 40 Hz automatic freq < 40 Hz by internal switch
⚠	-maximum rated input voltage		+ and -10 V
2.2.9.	Calibration output:		
	-output voltage	1,2 Vpp square-wave	1,2 Vpp square-wave
	-accuracy	< ± 1%	< ± 1%
	-frequency	2 kHz	2 kHz
2.2.10.	Outputs:		
	-ADC OUT (rear of the instrument)		Words from analog/digital converter are available with conversion ready signal pin 1: CONV READY pin 2: ADC 0 pin 3: ADC 1 pin 4: ADC 2 pin 5: ADC 3 pin 6: ADC 7 pin 7: ADC 6 pin 8: ADC 5 pin 9: ADC 4
	-rated output levels (TTL)		-V_{OL} 0,5 V max. -I_{OL} 2 mA max. -V_{OH} 2,4 V min. -I_{OH} - 200 /uA max. (outputs have TTL configuration)
	-optionally instrument bus IEEE-488 (rear of the instrument)		
	-IEEE-488		Memory contents and apparatus settings may be sent and received.
	-memory dump (listen only/ talk only)		Memory dump via IEEE-488 bus to and from data cassette recorder. For full specification see Operating manual of the PM8955

2.2.11. Power supply:

-line voltage (AC)	100,120,220 or 240 V (nominal ± 10%)
-line frequency	50 - 400 Hz ± 10%
-power consumption	≃ 70 W
-DC supply (connector rear of instrument)	
-voltage range (DC)	24 - 27 V floating minus (-) of battery connected to chassis
-current consumption	2 A (with option)

2.3. ENVIRONMENTAL CHARACTERISTICS

The environmental data mentioned in this manual are based on the results of the manufacturer's checking procedures.
Details on these procedures and failure criteria are supplied on request by the PHILIPS organisation in your country, or by PHILIPS INTERNATIONAL B.V., SCIENTIFIC & INDUSTRIAL EQUIPMENT DIVISION, EINDHOVEN, THE NETHERLANDS.

-ambient temperature	
-rated range of use	+ 5°C to +40°C
-operating range	-10°C to +40°C
-storage and transit	-40°C to +70°C
-operation position	a) horizontally on bottom feet b) vertically on rear feet c) any angle between a) and b)
-altitude	
operating	5000 m (15000 ft)
non-operating	15000 m (45000 ft)
-humidity	21 days cyclic damp heat 25°C - 40°C, RH 95%
-shock	300m/s, half sine-wave shock of 11 ms duration (3 shocks per direction for a total of 18 shocks)
-vibration	5-55 Hz, 15 minutes per direction, amplitude 0,7mm (peak-to-peak) and 30m/s^2 (3g) acceleration
-electromagnetic interference	meets VDE 0871 and VDE 0875 Grenzwert Klasse B
-safety	IEC 348 Class I prepared for UL 1244
-warm up time	30 minutes at 23°C
-recovery time	operates within 30 min. of being subjected to - 10°C, soak then taken into room conditions of 60% rel. hum. at 20°C

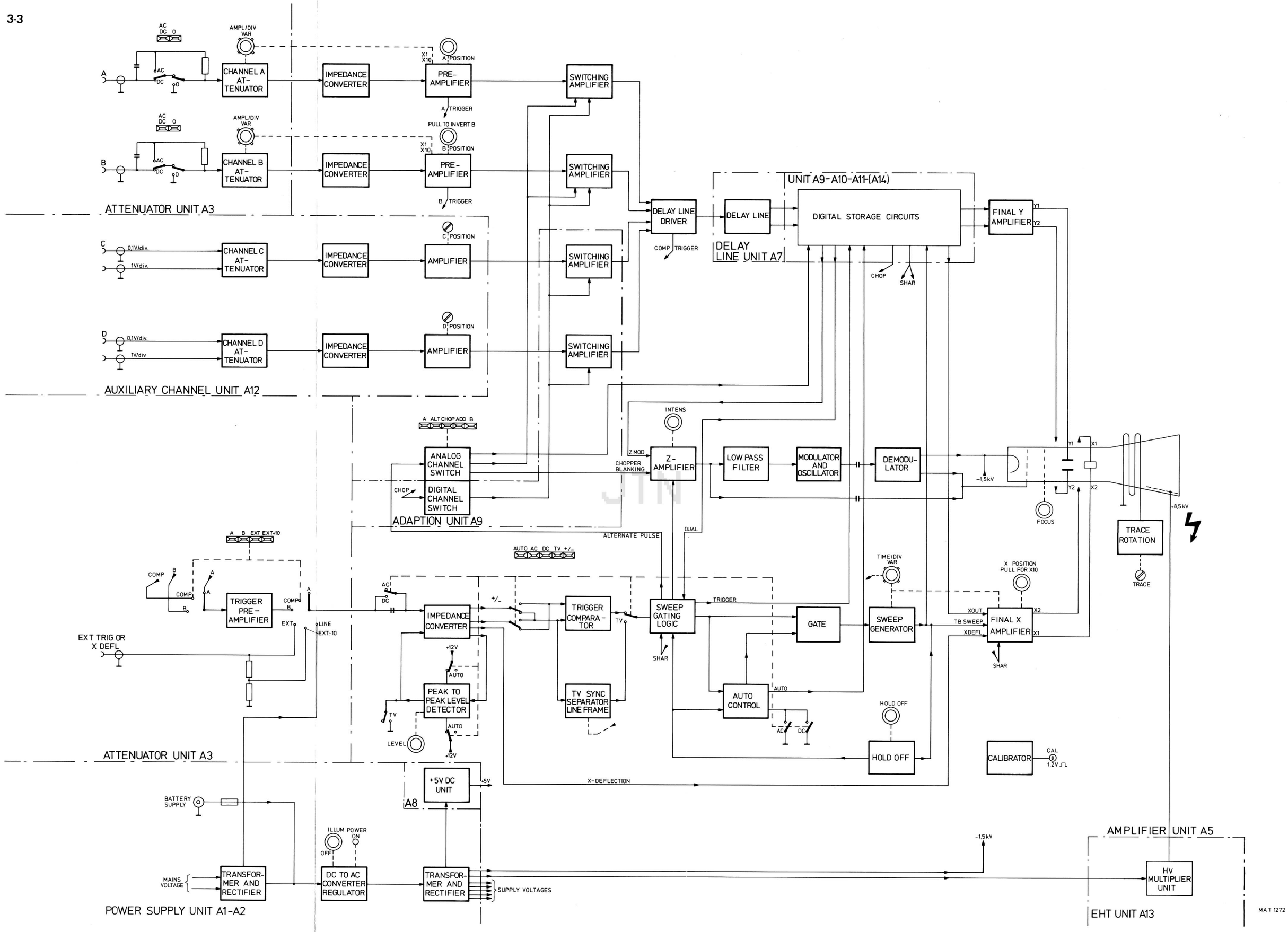


Fig. 3.1. Detailed blockdiagram I.

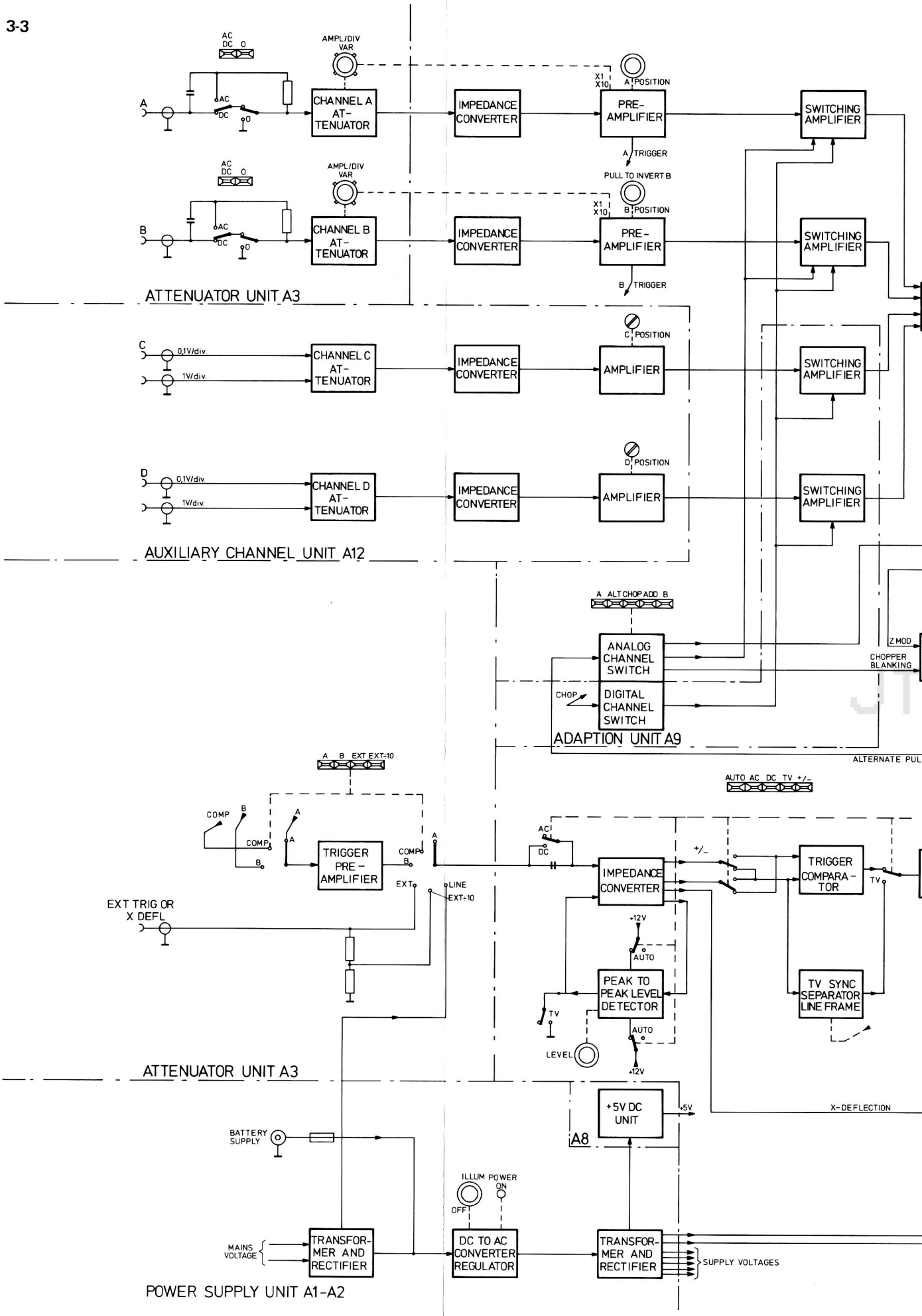
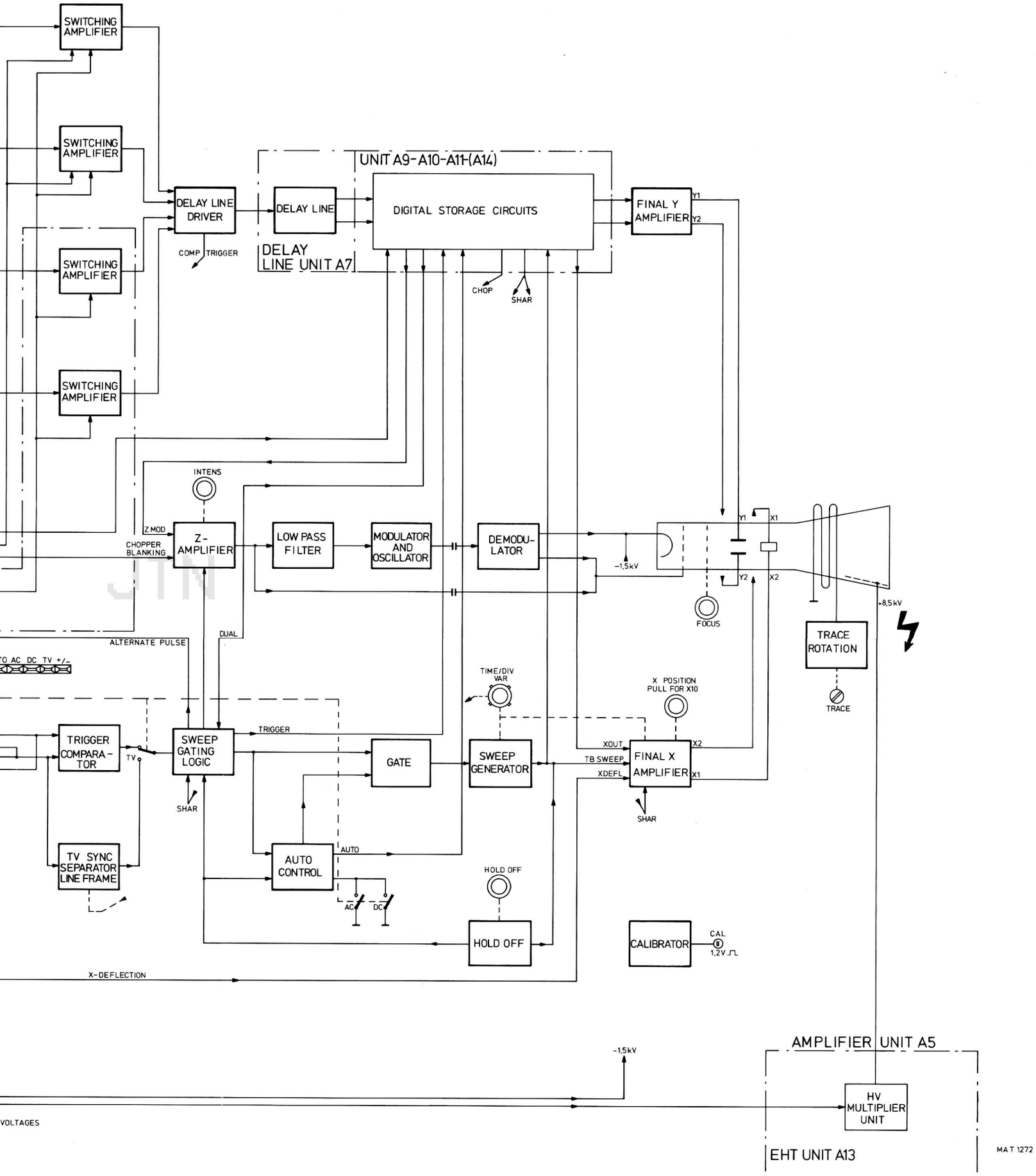


Fig. 3.1. Detailed blockdiagram I.


SWITCHING AMPLIFIER
SWITCHING AMPLIFIER
SWITCHING AMPLIFIER
SWITCHING AMPLIFIER
UNIT A9-A10-A11-(A14)
DELAY LINE DRIVER
DELAY LINE
DIGITAL STORAGE CIRCUITS
FINAL Y AMPLIFIER
Y1
Y2
COMP TRIGGER
DELAY LINE UNIT A7
CHOP
SHAR
INTENS
Z MOD
CHOPPER BLANKING
Z-AMPLIFIER
LOW PASS FILTER
MODULATOR AND OSCILLATOR
DEMODU-LATOR
-1,5kV
Y1
X1
Y2
X2
FOCUS
+8,5kV
TRACE ROTATION
TRACE
ALTERNATE PULSE
DUAL
TO AC DC TV +/-
TIME/DIV VAR
X POSITION PULL FOR X10
TRIGGER COMPARA-TOR
TV
SWEEP GATING LOGIC
TRIGGER
GATE
SWEEP GENERATOR
XOUT
TB SWEEP
XDEFL
FINAL X AMPLIFIER
X2
X1
SHAR
SHAR
TV SYNC SEPARATOR LINE FRAME
AUTO CONTROL
AUTO
HOLD OFF
AC
DC
HOLD OFF
CALIBRATOR
CAL
1,2V
X-DEFLECTION
-1,5kV
AMPLIFIER UNIT A5
HV MULTIPLIER UNIT
VOLTAGES
EHT UNIT A13
MAT 1272

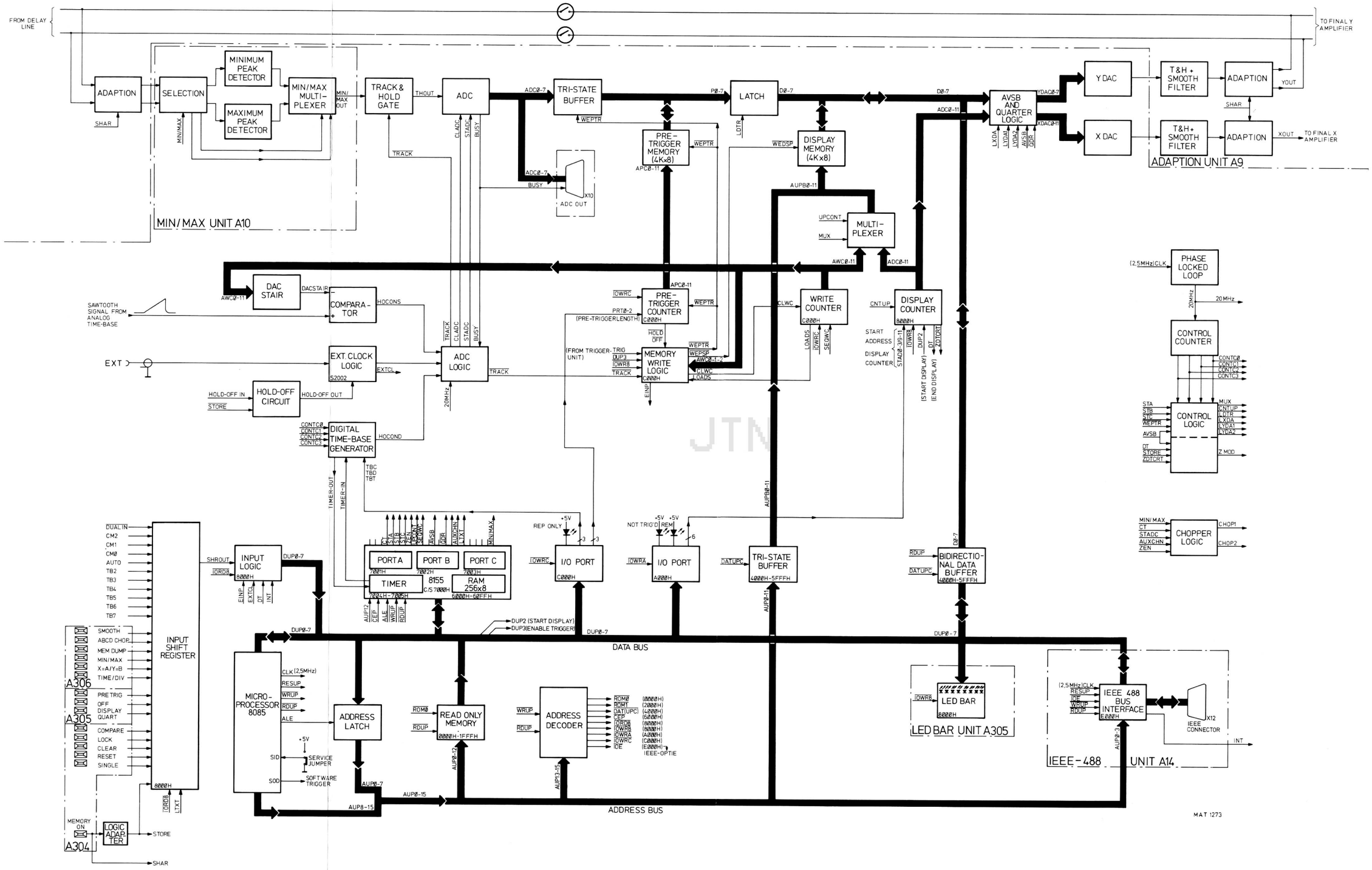


Fig. 3.2. Detailed blockdiagram II.

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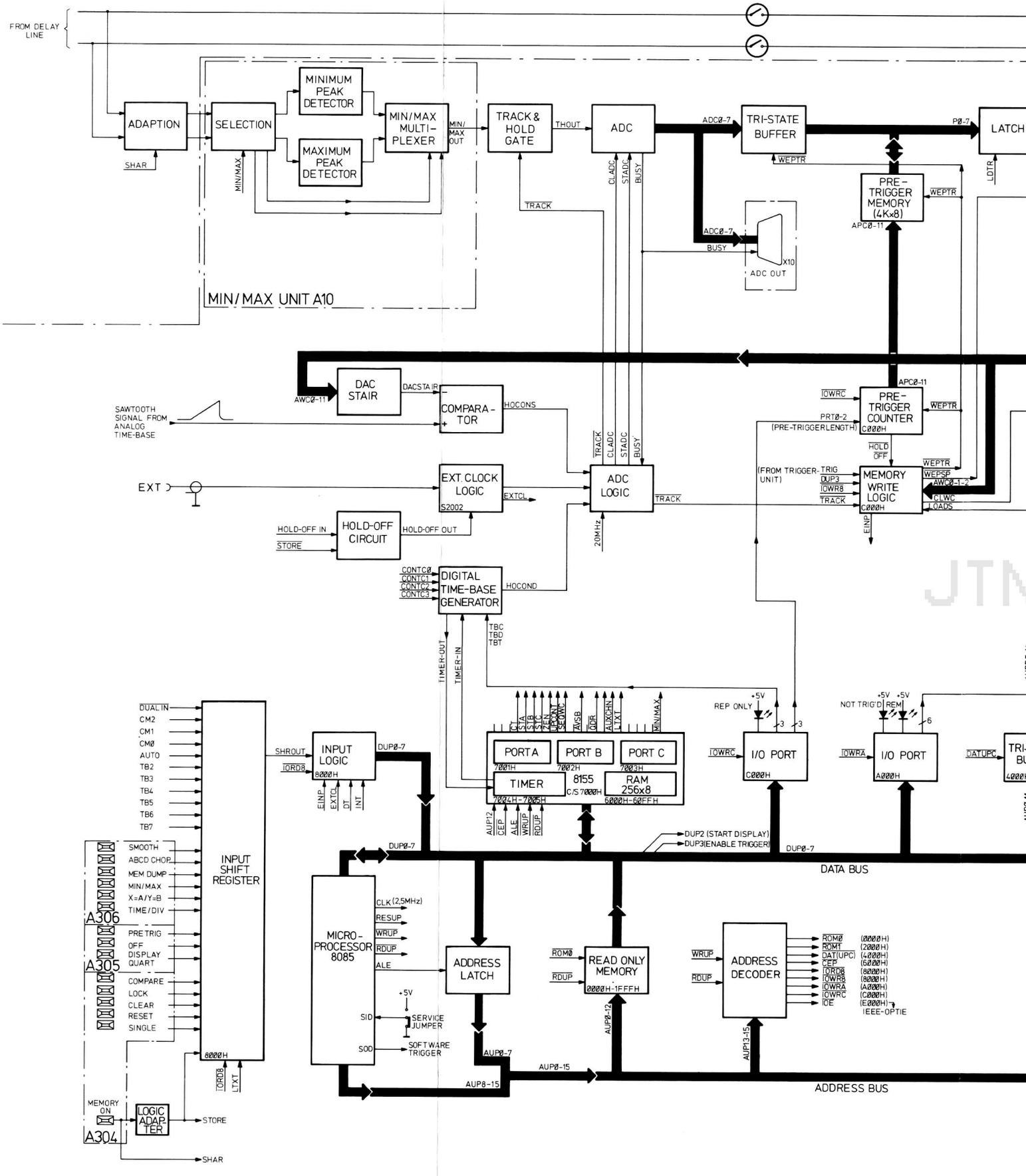
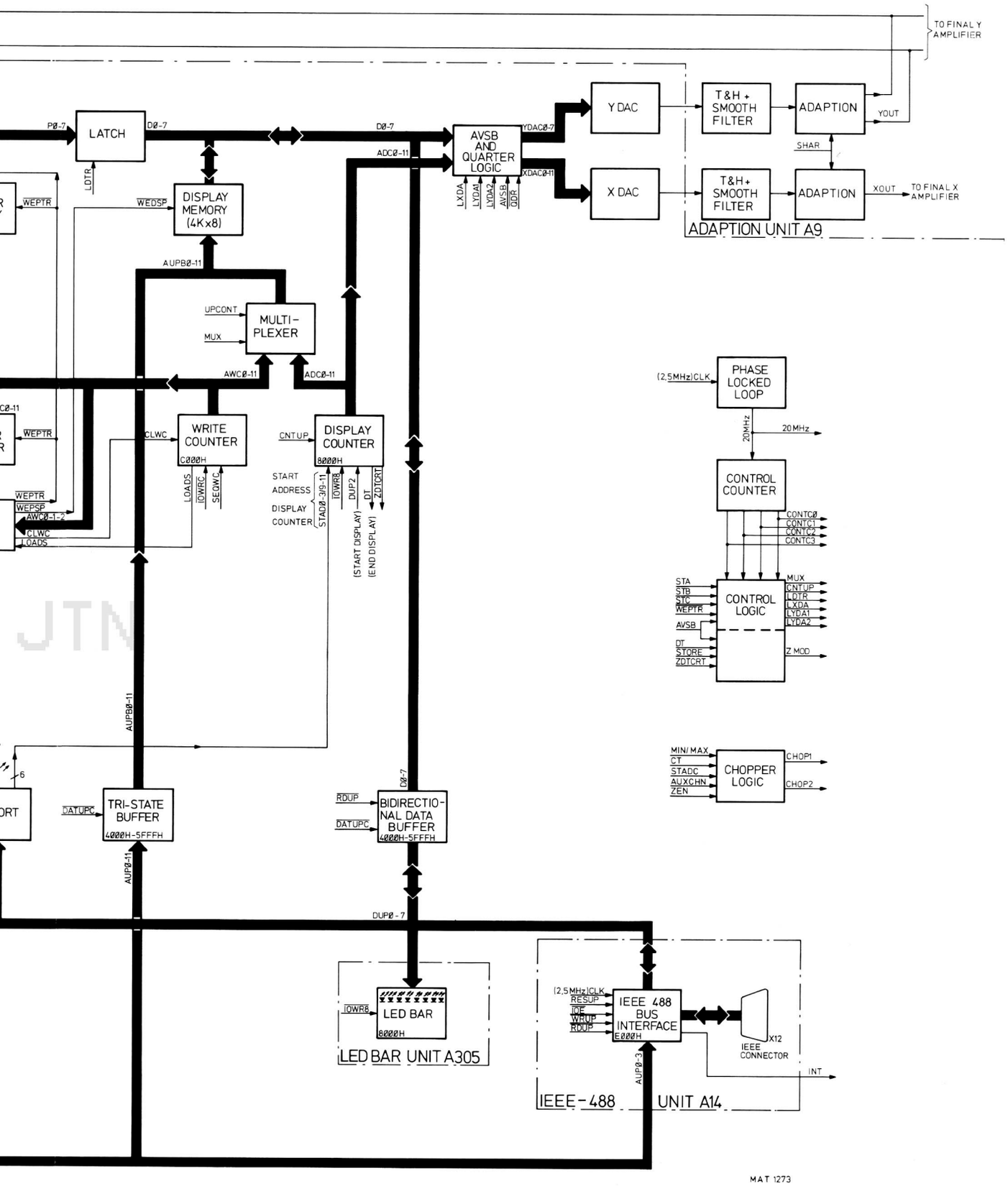


Fig. 3.2. Detailed blockdiagram II.



LOGIC UNIT A11

3. CIRCUIT DESCRIPTIONS

In chapter 3.1. the block diagram is described and in the chapters 3.2. and further the detailed circuit information is described.

3.1. BLOCK DIAGRAM DESCRIPTION (FIG. 3.1 and FIG. 3.2)

This chapter serves to explain the main functions of the oscilloscope.

This instrument can be used as a normal analog real-time oscilloscope (pushbutton MEMORY ON released) and as a digital storage oscilloscope (pushbutton MEMORY ON depressed).
With this pushbutton MEMORY ON a selection can be made between an analog and a digital signal path. At the same time a selection is done between an analog time-base circuitry and a digital time-base circuitry.

3.1.1. Vertical channel.

The vertical channels A and B for the signals to be displayed are identical except for the invert facility included in the B channel amplifier.

Each channel comprises an input coupling switch for AC-DC-0, an input step ATTENUATOR and an IMPEDANCE CONVERTER.

The AMPL/DIV switch provides x1 or x10 gain control of the PRE-AMPLIFIER, which offers in conjunction with the step attenuator a full range of Y deflection coefficients in a 1-2-5 sequence.

This stage is followed by a PRE-AMPLIFIER with trigger pick-off point. The pre-amplifier also contains the continuous control of the AMPL/DIV switch and the POSITION control for vertical shift of the trace. Both channels are applied to an electronic SWITCHING AMPLIFIER.

The SWITCHING AMPLIFIERS of both A and B channels are controlled by an ANALOG CHANNEL SWITCH which in turn is set for different display modes by operating the display mode pushbuttons A-ALT-CHOP-ADD-B.

In the ALT mode, the ANALOG CHANNEL SWITCH is operated by a pulse at the end of the MTB sweep, and offers alternate uninterrupted display of the channel A and B waveforms.

In the CHOP mode, the ANALOG CHANNEL SWITCH (channel multivibrator) is free-running at a fixed frequency of approximately 500 kHz to drive the SWITCHING AMPLIFIERS alternately, which then are opened and closed successively, so that discrete parts of the signals of channel A and B are displayed in rapid succession, giving the appearance of two continuous traces.

In the ADD mode, both SWITCHING AMPLIFIERS couple the signals through, thus adding channels A and B.
By inverting the B channel (PULL TO INVERT B) the A-B mode is obtained.

In MEMORY ON mode two more channels C and D can be added to the system, selected by the ABCD CHOP pushbutton, resulting in a total of four channels A,B,C and D.

Both channels C and D are identical, each comprising two separate input BNC's, mounted at the rear of the instrument, with a fixed deflection coefficient of 0,1V/DIV and 1V/DIV. Furthermore an IMPEDANCE CONVERTER and an AMPLIFIER with a screwdriver POSITION control (to be operated on the instruments leftside). Each AMPLIFIER is followed by a SWITCHING AMPLIFIER which is controlled by a DIGITAL FOUR CHANNEL SWITCH under the control of the microprocessor system.

The ANALOG CHANNEL SWITCH is blocked in MEMORY ON mode and its function is taken over by a DIGITAL FOUR CHANNEL switch which is controlled by the switches A-ALT-CHOP-ADD-B and ABCD CHOP via the microprocessor system.
In that case all four SWITCHING AMPLIFIERS of the channels A,B,C and D are controlled by the DIGITAL FOUR CHANNEL switch.

The resulting output signals of the four SWITCHING AMPLIFIERS are supplied via the DELAY LINE DRIVER and DELAY LINE to the Digital storage circuits. (See blockdiagram II FIG. 3.2).

Depending on the selection of MEMORY OFF or MEMORY ON the signal is applied via the so-called "analog signal path" or the so-called "digital signal path".

Selection of the analog signal path means that the DELAY LINE output is directly coupled to the input of the Y FINAL AMPLIFIER.

Selection of the digital signal path means that the DELAY LINE output is coupled to the ADAPTION circuit and then to the MIN/MAX unit.
With MIN/MAX selected the DELAY LINE is coupled to the MIN/MAX detectors in the "digital signal path". This circuit, which can be switched off via the microprocessor system by operating pushbutton MIN/MAX, determines the minimum and maximum amplitude of the analog input signal. These MIN and MAX values are applied to a MIN/MAX multiplexer.
The resulting analog signal is digitized in an Analog to Digital Converter (ADC) under the control of the ADC logic and the microprocessor system.

The timing of the conversion is determined by one of the 3 following sources :

- In positions 0.5s/div. ... 0.2ms/div of the TIME/DIV switch (DIRECT-mode) by the digital time-base generator.
- In positions 100/us/div. ... 0,1/us/div. of the TIME/DIV switch (sequential SAMPLING-mode) by the analog time-base generator saw-tooth signal and the trigger signal.
  (See digital storage circuits section 3.7.7. ADC logic).
- In (EXTERNAL-mode) by a frequency applied to the EXT. CLOCK input.

After digitizing by the ADC the information is shifted via a TRI-STATE BUFFER through a PRE-TRIGGER MEMORY. The ADC output information is also applied to an ADC OUT connector on the rear panel. This PRE TRIGGER MEMORY which consists of a RAM MEMORY, a PRE TRIGGER COUNTER and a LATCH is configurated as a shift register with a variable length. The LATCH can be seen as the output of this shift register system.
The length of this shiftregister can be varied by presetting the PRE-TRIGGER COUNTER via the microprocessor system and depends on the operator's PRE-TRIGGER selection with pushbuttons PRE-TRIG and OFF. Furthermore the PRE TRIGGER MEMORY is controlled by the MEMORY WRITE LOGIC.

On receipt of a trigger pulse a coupling is realized between the PRE-TRIGGER shift register output (LATCH output) and a DISPLAY MEMORY of 4096 x 8bits.
Starting at the moment of triggering the DISPLAY MEMORY will be completely filled with information which is shifted through the PRE-TRIGGER shift register system.
The information, which was stored already in the PRE-TRIGGER MEMORY at the moment of triggering is shown on the C.R.T. display as PRE-TRIGGER information.

The contents in the DISPLAY MEMORY is influenced by the selected acquisition modes MIN/MAX, COMPARE, ABCD CHOP, A, B, ALT, CHOP, ADD and/or B.

Two address counters "WRITE COUNTER" and "DISPLAY COUNTER" can be connected to the DISPLAY MEMORY address lines via a MULTIPLEXER.
The WRITE COUNTER is addressing to the DISPLAY MEMORY when new information has to be written in the memory and the DISPLAY COUNTER is addressing to the DISPLAY MEMORY when memory contents has to be displayed on the C.R.T. screen.
It is also possible to write or read information to or from the DISPLAY MEMORY by a controller via an IEEE-488 option. This is done via a TRI-STATE BUFFER.

The contents of the DISPLAY MEMORY can be visualized on the C.R.T. screen under the control of the DISPLAY COUNTER and the microprocessor system.
Different display modes can be selected by operating one or more of the pushbuttons X=A/Y=B, SMOOTH, DISPLAY QUART.
The digital output information of the DISPLAY MEMORY is applied via an AVSB AND QUARTER LOGIC to a vertical Digital to Analog converter (Y-DAC).
The resulting analog signal information is then applied via a SMOOTH filter and ADAPTION circuit to the vertical FINAL Y AMPLIFIER which directly drives the vertical (Y) plates of the C.R.T.

3.1.2. Horizontal channel.

Trigger signals can be derived from the A and B channels, from the mains supply or externally from the EXT-input and are selected by the trigger- source switch A - B - EXT - EXT÷10 - COMP - LINE. With the A and B pushbuttons both depressed, composite triggering is derived from the DELAY LINE DRIVER. (Composite triggering is not possible when the oscilloscope is used as digital storage oscilloscope). The trigger coupling switch provides the facility of AUTO, AC, DC or TV triggering.

The polarity of the trigger signal, negative or positive-going, on which the display will start is determined by the +/- SLOPE control, which changes the output polarity of the TRIGGER COMPARATOR.

With the AUTO switch depressed, the peak-to-peak level of the signal then determines the range of the LEVEL control.
With AC or DC selected, the range of the LEVEL control is fixed.
Selection of DUAL enables the display to be triggered on either the positive-going or the negative-going edge of the input signal.

For normal time-base operation (MEMORY ON released) the FINAL X-AMPLIFIER is fed by sweeps from the TIME-BASE circuit.

When AUTO is selected, in the absence of trigger signals, the time-base generator output is directly fed back via the HOLD-OFF CIRCUIT and gate to its input. This causes the sweep to free-run and a trace is always visible.

The AUTO mode can be used in all instances where the TRIG mode is valid, except for signals below 20 Hz or pulse trains with an off period exceeding 100 ms.
As soon as trigger pulses are available, the free-running state of the time-base generator is automatically terminated and normal triggering is resumed.

When either DC or AC is selected, AUTO is inoperative. Sweeps are then only produced when a trigger signal is present and the LEVEL control is set correctly.

The HOLD-OFF CIRCUIT, as its name implies, 'holds off' trigger pulses from the time-base input until the flyback trace has completely returned and the time-base circuits are completely reset.

The TIME/DIV switch positions control the speed of the time-base sweep in a 1-2-5 sequence together with the uncalibrated continuous control. Setting the TIME/DIV switch in the X DEFLECTION position inhibits the time-base output of the FINAL X AMPLIFIER and permits horizontal deflection from another source.

Horizontal shift of the time-base line is achieved with the X POSITION control and it can be magnified by a factor of 10 using the X MAGN push-pull switch.

The FINAL X-AMPLIFIER drives the horizontal (X) plates of the CRT.

With MEMORY ON selected the addresses for the DISPLAY MEMORY are converted to an analog staircase signal by the microprocessor controlled X DAC and then applied to the FINAL X-AMPLIFIER via a SMOOTH filter and ADAPTION circuit.

In X=A/Y=B mode the AVSB and QUARTER logic applies the signal value of channel A to the X DAC and the mean value of 2 adjacent channel B values to the Y DAC. This is controlled by the DISPLAY MEMORY COUNTER. Now the channel A signal is displayed horizontally and the channel B signal is displayed vertically.

QUARTER display is realized by the AVSB and QUARTER logic under the control of the microprocessor system.

3.1.3. Micro-processor control system

The micro-processor control system consists of a micro-processor, ROM and RAM memories, latches, input and output ports, address decoder and relevant logic circuits.

The following functions are under its control:
- -Reading of switch settings used in MEMORY ON mode.
- -Reading of the TIME/DIV switch settings.
- -Reading of the display mode pushbuttons.
- -Control of pilot lamps for DISPLAY QUART and PRE-TRIG.
- -Control of pilot lamps REMOTE, REP ONLY and NOT TRIG'D.
- -Control of the C.R.T. display.

Furthermore the microprocessor system controls several sections in the oscilloscope.

In addition to these oscilloscope functions, the micro-processor control system also supervises the handling of the IEEE-488 Bus-interface option.

3.1.4. Timing

Time-base frequencies and control and timing signals are generated by the PHASE LOCKED LOOP, CONTROL COUNTER, CONTROL LOGIC and CHOPPER LOGIC.

3.1.5. CRT display section.

In MEMORY OFF the Z-amplifier is controlled by timing signals derived from the horizontal time-base channels to provide trace blanking of the C.R.T. during the flyback and hold-off time.
In addition, controlled by the vertical logic, it blanks the sweep during switching transients in CHOP mode.

The l.f. components of the blanking signal are modulated and demodulated (for voltage isolation purposes) before they are applied together with the a.c. - coupled h.f. voltage components to the Wehnelt cylinder.

In MEMORY ON the way in which the contents of the DISPLAY MEMORY is displayed on the C.R.T. screen depends on the functions which are selected by the operator.
The contents of the DISPLAY MEMORY are 4096 words, each consisting of 8 bits. Each 8-bit word is capable of indicating 256 different amplitudes (i.e. $2^8 = 256$) : Y values.
Each address of the memory corresponds to a by the selected function specified vertical line of the display along the X-axis.

The 4000 words of the DISPLAY MEMORY contents of 4096 words are displayed in a display area of more than 8 vertical divisions and 10 horizontal divisions which is divided into 256 x 4000 dots. (96 dots are displayed outside the 10 horizontal divisions).
A µP-controlled DISPLAY COUNTER sends 4096 different addresses sequentially (starting with address 0 and ending with address 4095) to the DISPLAY MEMORY and to the Digital-to-Analog-Converter (DAC) of the X-system. To provide the discrete steps for the horizontal time-base display the output of the X-DAC is a linear staircase voltage, which is applied to the FINAL X-AMPLIFIER. The resulting output of the FINAL X-AMPLIFIER is routed to the horizontal deflection plates of the C.R.T.

Similarly, the 8-bit instantaneous values for each address (i.e. the Y-information) are converted into analog signals by means of the Y-DAC. The converted signal is then applied to the FINAL-Y-AMPLIFIER.
Trace intensity is controlled by the Z AMPLIFIER and can be adjusted by means of the INTENS control.

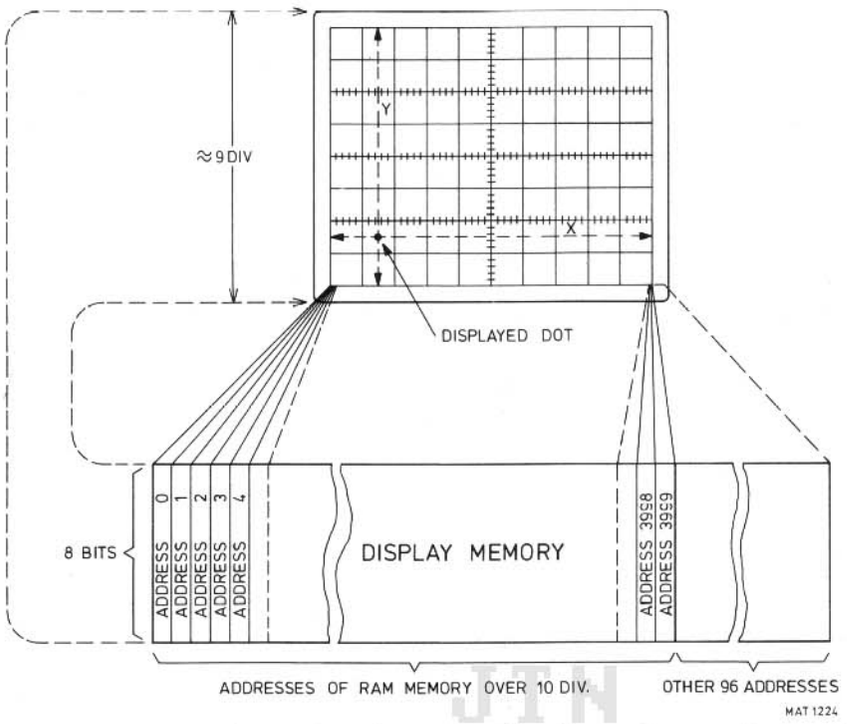


FIG. 3.3. Complete display of all the values of one channel.

The FOCUS control drives the focussing electrode of the CRT to regulate the sharpness of the trace.

The trace should lie in parallel with the horizontal graticule lines, if any deviation occurs, it can be corrected with the TRACE ROT potentiometer.

In MEMORY ON mode (signal STORE is active) the blanking pulse is controlled by the display memory logic for the different display modes.

3.1.6. Power supply

The power suply operates either from a.c. mains voltages of nominally 100V, 120V, 220V or 240V or optional from a d.c. source of 24-27 V. A switched-mode circuit employing an integrated circuit provides smoothed d.c. outputs of +180V, -180V, +38V, +5V, +12V, -12V, +60V, -60V.

A separate DC unit supplies a +5V DC voltage for the logic circuits.

The EHT voltage for the accelerator anode of the C.R.T. is derived from a voltage quadrupler circuit taken from the converter transformer secondary circuit that supplies the -1500 V for the cathode of the C.R.T.

The brilliance of the graticule illumination lamps can be varied with the ILLUM control.

The CAL unit provides the calibration square-wave voltage.

3.2. DESCRIPTION OF THE VERTICAL DEFLECTION SYSTEM (Diagram 1)

The vertical channels A and B for the signals to be displayed are identical, each comprising an input coupling switch, an input step attenuator, an impedance converter and a preamplifier with trigger pick-off.
A channel multivibrator, controlled by the display mode pushbuttons, switches either channel A or channel B to the final Y amplifier via the delay line driver and the delay line. The final Y amplifier feeds the Y deflection plates of the cathode-ray tube.
The individual stages of the vertical deflection system are now described in some detail.
As the signal paths for channel A and channel B are basically identical, only the channel B signal path is described.

3.2.1 Input coupling (unit A3)

Input signals connected to the B input socket X3 can be a.c. coupled or internally disconnected.
In the AC position of S14, there is a capacitor (C401) in the signal path. This capacitor prevents the DC component of the input signal from being applied to the amplifier.
In position DC of switch S14, the input signal is coupled directly to the step attenuator.
At the same time, blocking capacitor C401 is discharged via R402, to prevent damage of the circuit under test by a possible high charge.
S15 (0) isolates the B input signal and earths the channel input for reference purposes; e.g. for calibration or centering the trace.

3.2.2. Input attenuator (unit A3)

The input attenuator is a frequency-compensated, high-impedance voltage divider with twelve positions. The overall attenuation of the stage is determined by the combination of the selected sections of two voltage dividers. The various combinations are selected by the twelve positions of the frontpanel AMPL/DIV attenuator switch S8.
The first divider sections attenuate by factor of 1.25, 3.125 and 6.25 and the second divider sections attenuate by a factor of 1x, 10x and 100x.
With the overall combinations of attenuation, nine different deflection coefficients are realised from 20 mV/div to 10 V/div in a 1-2-5- sequence. Only for the most sensitive positions 2 mV/div, 5 mV/div and 10 mV/div of AMPL/DIV attenuator switch S8, the gain of the Y amplifier is increased by a factor of 10.
The input capacitance of the attenuator cannot be adjusted in the individual positions. Small differences of approx. 1 pF are allowed. Capacitor networks are provided in the voltage divider sections to make them frequency independent.

3.2.3. Impedance converter (unit A5)

The impedance converter is formed by V604 (two matched field-effect transistors). The two FET transistors are used in source follower configuration.
The signal level on the gate (and on the source) of the upper FET amounts to 1,6 mV/div or 16 mV/div.
Diode V601 together with the output impedance of the attenuator and also the attenuator action protects the input source follower, against excessive negative input signals. The d.c. balance of the circuit can be adjusted with R604, providing attenuator balance for the 10 mV/div and 20 mV/div positions.

3.2.4. Pre-amplifier (unit A5)

The input stage formed by D601 (5 transistors) is switched in a Cherry-Hooper configuration and direct coupling is employed throughout.
In the positions 20 mV/div. - 10 V/div. of the AMPL/DIV switch S8, contact K601 is open and the gain is determined by

$$\frac{R628 + R632}{R611 + R612} = \text{approx. } 1{,}8 \text{ x}$$

If K601 is closed (in positions 2 mV/div., 5 mV/div. and 10 mV/div) the gain of this stage is increased by a factor of 10. This is accurately adjusted with R621.
To prevent jumping of the trace when K601 is switched with the input short circuited, no voltage must be present across these contacts. R604 (attenuator balance) serves this purpose.
R8 in conjunction with R622,R623 R624 and R626 forms the vernier control. In the calibrated position (R8 is 1 kohm) the transfer of this network is 0,85 x. With R8 to its minimum position (0 ohm) the transfer is 0,3 x. Thus we have a control range of 3 x.
V608, V609, V613, V614, V616 and V617 form a symmetrical cascode circuit supplying an output CURRENT to the channel switch.

The transfer conductance of this stage is:

$$\frac{Iout}{Uin} = \frac{1}{R641 \;//\; (R637+R638) \;//\; (R646+R647+R648)} = 7 \text{ mA/V}$$

The signal level at the input of this stage is approx. 24 mV/div equivalent to approx. 170 µs/div. at the output.

Note: The channel A gain can be equalised to the channel B gain with the aid of R543 (gain x 1 in channel A amplifier).

3.2.5. Trigger pick-off (unit A5)

The trigger signal is picked-off at the emitters of V608 and V609, a signal source with a low internal resistance, by the series feed-back stage V611 and V612.
From this stage the trigger signal current is fed asymmetrically to the trigger selector via a 50 ohm cable.

3.2.6. Normal invert switch (unit A5)

The B channel has a provision for inverting the polarity of the Y signal. Push-pull switch S4, PULL TO INVERT B, is mounted on the shaft of front-panel control B POSITION. In the invert position of the switch the normal signal paths are blocked because V613 and V614 are switched off.
Inversion is achieved by V616 and V617 providing alternative paths for the signal when their bases are switched less positive by S4. Possible unbalance between the two positions of the switch can be compensated by preset potentiometer R647 (Norm invert balance).

3.2.7. Position control (unit A5)

Potentiometer R3 is the vertical POSITION control. Its balance is adjustable by means of R674 (shift balance).

3.2.8. Analog channel switch (unit A5)

The ANALOG CHANNEL SWITCH consists of two circuits (SWITCHING AMPLIFIERS) which are inserted in the A and B channel signal paths. The A channel circuit consists of the transistors V524, V526 and the diodes V521, V522 and V523. The B channel circuit consists of the transistors V624 and V626 and the diodes V621, V622 and V623.
When the junction of the three diodes is positive in relation to mass, the diodes are non-conductive. The transistors, and thus, the signal path are conductive.
If the current drained from the junction exceeds 6 mA, the diodes are conductive and the transistors are turned off.
The circuits are driven from the flip-flop formed by the transistors V703 and V704.

With A (S1A) depressed: only channel A is displayed.
The base of V703 is connected to the -12V supply voltage. V703 is turned-off then, its collector voltage is high and channel A is switched on. At the same moment channel B is switched off.

With ALT (S1B) depressed: channels A and B are alternately displayed. This pushbutton is a dummy and has no contacts, but it releases all the other pushbuttons of the display mode controls. In this mode there is a DC path via V704 between the two emitters, the circuit is bi-stable and one of the diodes is conductive.
V1201 in not conducting in ALT mode and negative going alternate pulses derived from the time-base generator are fed to the circuit. These pulses switch the circuit at the end of each sweep and the channels A and B are alternately displayed.

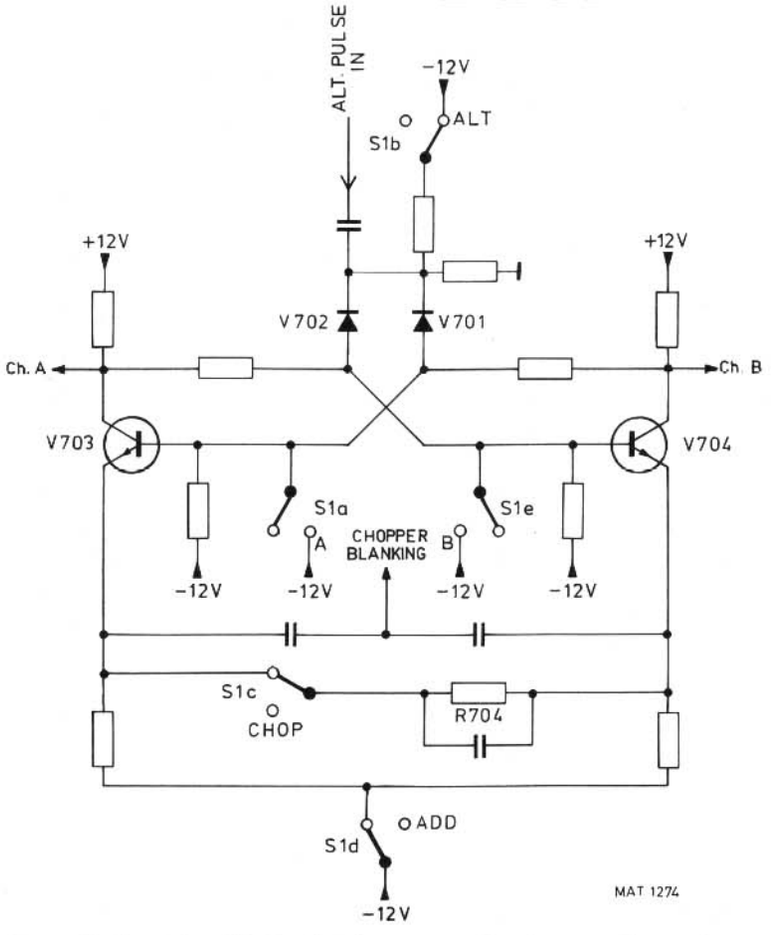


FIG. 3.4. Simplified diagram of the analog channel switch.

In the ALT mode -12V is aplied via S1A, S1C, S1D and S1E and R710 to transistor V1506 in the beam blanking amplifier.
This transistor is the blocked and the only control signal for the beam unblanking amplifier is the normal unblanking pulse coming from the time-base circuit.

With CHOP (S1C) depressed: channels A and B are chopped.
In this mode the circuit acts as a chopper generator. S1C is open then, the DC path between the emitters of V703 and V704 is interrupted and the circuit is a-stable. Both diodes V701 and V702 are then turned-off and the circuit starts oscillating, the oscillating frequency being approx. 500 kHz.
During the switching transients in the CHOP-mode, the C.R.T. is blanked with the aid of differentiated chopper blanking pulses (at the junction of R703 and C702) which are fed to the Z-amplifier.

With ADD (S1D) depressed: channel A and B are added.
Both transistors are turned-off, both collector voltages are high and both channels are switched on.

With B (S1E) depressed: only channel B is displayed.
The base of V704 is connected to the -12V supply voltage. V704 is then turned-off, its collector voltage is high and channel B is switched on. At the same moment channel A is switched off.

3.2.9. C and D channels (unit A12 - diagram 2)

In MEMORY ON mode two more channels C and D can be added to the system, selected by the ABCD CHOP pushbutton, resulting in a total of four channels A,B,C and D.
Both channels C and D are identical, each comprising two separate input BNC's, mounted at the rear of the instrument, with a fixed deflection coefficient of 0,1V/DIV and 1V/DIV. Furthermore an IMPEDANCE CONVERTER and an AMPLIFIER with a screwdriver POSITION control (R13 for channel C and R14 for channel D).

3.2.10. Digital channel switch (unit A9 - diagram 3)

Each AMPLIFIER is followed by a SWITCHING AMPLIFIER which is controlled by a DIGITAL FOUR CHANNEL SWITCH.

The ANALOG CHANNEL SWITCH is blocked in MEMORY ON mode by signal $\overline{\text{DIGCH}}$ via D1802, D1903 and transistors V1901 and V1902. Its function is taken over by a DIGITAL FOUR CHANNEL switch which is controlled by the switches A-ALT-CHOP-ADD-B and ABCD CHOP via the microprocessor system.
The DIGITAL CHANNEL SWITCH is enabled by the signal $\overline{\text{DIGCH}}$ from the microprocessor and controlled by the signals CHOP1 and CHOP2 from the CHOPPER LOGIC on unit A11 (see section 3.7.6.).

In decoder D1901 four select signals are generated as follows:

CHOP2	CHOP1	Output
0	0	CHANA
0	1	CHANB
1	0	CHANC
1	1	CHAND

Signals CHANA and CHANB are then via FET 1903 applied to the cathodes of V523 and V623, thus controlling the channel A and B switching amplifiers.
Signals CHANC and CHAND are directly applied to the channel C and D switching amplifiers.

3.2.11. Delay line driver (unit A5) and delay line (unit A7)

The resulting output signals of the four SWITCHING AMPLIFIERS are supplied to the DELAY LINE DRIVER and DELAY LINE to the Digital storage circuits.

The symmetrical delay line is sandwiched between a series feed-back push-pull amplifier (called CHERRY) and a shunt feed-back push-pull amplifier (called HOOPER), consisting of integrated circuit D801.
Such an amplifier combination is called "CHERRY-HOOPER".
The series feed-back stage receives a signal of approx. 30 mV/div which is obtained from a signal current of 0,17 mA/div. from the channel switch, multiplied by the value of the load resistance R803 + R804 = 200 ohm.
The emitter impedance of the series feed-back stage consists besides RE = R819 + R821 of the parallel circuit of a number of RC networks.
As the delay line is a source of distortion for higher frequencies, these networks are realizing the necessary delay line compensation.
At the input side, delay line D802 terminates in R828 and R829 (totally 200 ohm).
The delay line itself is a symmetrically mount spiralized cable with a characteristic impedance of 200 ohm and a delay of 110 ns/m. At the output side, the cable terminates via R831 and R832 in the virtual earth points of the parallel feed-back stage (HOOPER). The input impedance on these virtual earth points is 14 ohm. This value in series with the 86,6 ohm of R 831 and R832 forms the correct termination for the delay line.

3.2.12. Composite trigger pick-off (unit A5)

The composite trigger signal is picked-off at the emitters of the CHERRY stage (D801), a signal source with a low internal resistance, by the series feed-back stage V802 and V803. From this stage the composite trigger signal current is fed asymmetrically to the trigger selector via a 50 ohm cable.

3.2.13. Digital storage circuits (units A9 - A10 - A11)

The output signals from the DELAY LINE CIRCUIT are connected to the digital storage circuits.
Depending on the selection of MEMORY OFF or MEMORY ON the signal is applied via the so-called "analog signal path" or the so-called "digital signal path".
Selection of the analog signal path means that the DELAY LINE output is directly coupled to the input of the Y FINAL AMPLIFIER via the ADAPTION unit A9.

Selection of the digital signal path means that the DELAY LINE output is coupled to the ADAPTION circuit on unit A9 and then to the MIN/MAX unit A10. After passing this unit the signal is digitized and afterwards stored on LOGIC UNIT A11.
For display on the C.R.T. screen the stored signal information is converted into analog again and then applied via ADAPTION unit A9 to the FINAL Y AMPLIFIER on unit A5.

For more detailed information about the digital storage units A9 - A10 and A11 see section 3.7.

3.2.14. Final Y amplifier (unit A5)

The output signals of the HOOPER stage are applied to the FINAL Y AMPLIFIER stage consisting of the transistors V804, V806, V807 and V808, which are configurated as two series feed-back amplifiers in parallel fed by a constant current source.
The gain of the FINAL Y AMPLIFIER can be set by means of potentiometer R848. The centre taps of the coils L801 and L802 are connected to the Y deflection plates of the C.R.T. The Y deflection plates form filters together with the coils L801 and L802. These filters terminate in resistors R859, R861, R862 and R863.

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3.3. TRIGGERING (Diagram 4)

The trigger source switches for triggering the time-base generator, can select any of the following input sources:
- an internal signal from the vertical A channel
- an internal signal from the vertical B channel
- an internal composite signal of channel A and channel B
- a signal derived from the mains supply
- an external source
- an external source divided by 10

All these sources can be used for both triggering and X deflection purposes. Source selection is done by means of a trigger selector switch S16 that feeds the trigger signals to the trigger amplifier.

3.3.1. Trigger source selection and preamplifier (unit A3)

The signal currents (60 uA/div.) of the three trigger pick-off stages are, after selection by S16C and S16D, amplified to a level of 100 mV/div. by a shunt feed-back stage + emitter follower stage consisting of V351 and V352. After this stage there is a selection between its output signal, a signal on the external socket and a signal with the line frequency by means of S16A and S16B. Signals that are not used are short-circuited to mass.
The externally applied signal is attenuated by a factor of two or twenty (depending on position of EXT and EXT ÷ 10) allowing standardisation of the input impedance of the EXT socket to 1 Mohm // 20 pF.

3.3.2. Impedance converter (unit A5)

The trigger signal of 100 mV/div. is fed via the AC-DC coupling switch S2C to a FET (V1006) in source follower configuration.
From here the signal is applied via an emitter follower to the ± slope selection switch S3. This selection switch enables triggering on either the positive-going or the negative-going edge of the triggering signal.

3.3.3. Trigger comparator (unit A5)

From the ± slope selector switch S3 the signal is fed via a common emitter amplifier D1001 (123/345) to the output shunt feed-back amplifier V1014 via the TV mode switch S2D. The voltage gain is high (28 x) but its dynamic range is small (2,8 Vp-p at the output). This is because of the tail current of the symmetrical common emitter stage is 2 mA. The current sweep at the output of this stage is consequently 2 mA at max. which is transformed into a 2,8 V max. voltage sweep at the output of the shunt feed-back amplifier V1014. This means that the trigger amplifier is completely driven at a trace height of 1 div. Which division on the screen this is, depends on the position of the LEVEL control R5.
With AC (S2B) or DC (S2C) depressed, the range of the LEVEL control is fixed. The DC voltage at the wiper of LEVEL control R5 , which is fed to the FET (V1006) can vary between + 3,5 V and - 3,5 V. Diodes V1001 and V1002 are then turned-off, and the voltage on the gate of the FET is then adjustable between + 0,9 and - 0,9 V. At a signal level on the gate of the other FET of 100 mV/div., there will be a control range of ± 9 div.

3.3.4. Peak to peak level detector (unit A5)

If the AUTO pushbutton S2A is depressed, the supply voltages for the level control circuit are interrupted.

A trigger signal (300 mV/div.) which is derived from the emitter follower stage and amplified by V1008, gives after peak to peak detection a DC voltage across the level control. This DC voltage is approx. proportional to the amplitude of the trigger signal. This is the auto trigger level control. The peak to peak level of the signal then determines the range of the level control.

3.3.5. T.V. synchronisation separator (unit A5)

If the TV mode pushbutton S2D is depressed, the LEVEL control is switched-off. The wiper of R5 is then connected to mass. A synchronisation separator for the television signals is then inserted into the trigger signal path.
A composite video signal contains, besides the video information, also synchronisation pulses with line and frame frequency which can be distinguished by their pulse width.
The TV synchronisation separator circuit is able to:
1. separate the synchronisation pulses from the video information.
2. distinghuish between frame synchronisation pulses and line synchronisation pulses.

The first requirement is met by V1013 acting as a DC restorer and limiter, the second requirement by the integrating network R1047, C1011 and C1012.
The TV signal is picked-off at the ± slope selector switch which in this case can be set for the right polarity of the TV signal. The TV trigger signal is then amplified by the series feed-back push-pull stage V1009, V1011 and applied to synchronisation separator V1013 via emitter follower V1012. The signal on the base of V1013 could be as follows:

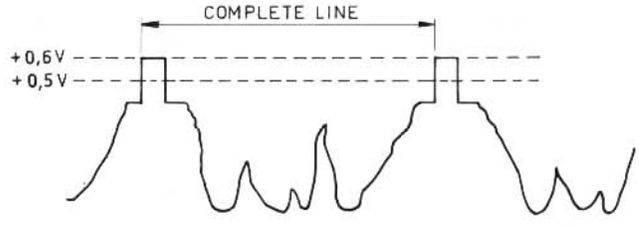

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FIG. 3.5. Signal on the base of transistor V1013.

The peaks of the synchronisation pulses are all at one level by the DC restorer action of C1007, R1039 and the base emitter diode of V1013. The base voltage will never exceed + 0,6 V by a large amount, but the complete waveform will appear at the base. The signal level is at this point approx. 280 mV per screen div. Change in signal of approx. 100 mV is sufficient to turn off V1013. V1013 looks only to the peaks of the synchronisation pulses.
The rest of the TV signal has no influence. On the collector of V1013 we find exclusively the synchronisation signal consisting of line synchronisation pulses and the wider frame synchronisation pulses.

In the time-base positions 20 µs/div. and faster, this complete signal is transmitted to the time-base generator and we have line triggering.

In the time-base positions 50 /us/div. and slower, C1011 and C1012 are connected to mass. The narrower line synchronisation pulses are then, integrated out of the signal, but the wider frame synchronisation pulses remain, and frame triggering is obtained. A second threshold is built-up by V1016. V1017 reacts to the signal that still passes and consists of pure line or frame synchronisation pulses. After this the signal is fed to the time-base generator via V1014.

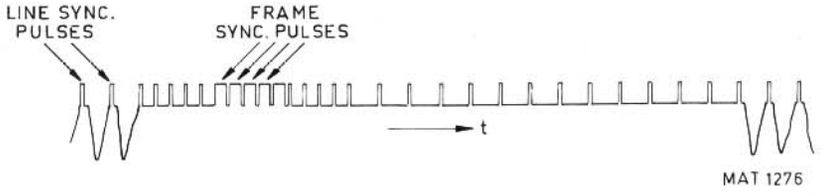


FIG. 3.6. A vertical interval with frame synchronisation pulse group.

DUAL SLOPE triggering.

Selection of DUAL enables the display to be triggered on either the positive-going or the negative-going edge of the input signal.
This DUAL SLOPE trigger mode can only be selected in MEMORY ON.

Without DUAL SLOPE triggering selected, the trigger signal from the trigger shunt feedback amplifier V1014 is applied via NAND D1931 (1-2-3) and NAND D1931 (11-12-13) to NAND D1931 (8-9-10), which reacts on the positive slope of the signal, to the sweep gating logic.
The circuit is blocked during the generation of a sweep by the signal on input 2 of NAND D1931.

With DUAL SLOPE triggering selected, the microprocessor generates a control signal DUALOUT which is applied to NAND D1931 (4-5-6). This circuit reacts on the negative slope of the signal.
At the same time a level correction is achieved via transistor V1938 and resistor R1936.

3.4. TIME-BASE GENERATOR (Diagram 5)

The time-base generator comprises a sweep gating logic, a sweep generator, a hold-off circuit, an auto sweep circuit and X final amplifier.
Before considering these stages in detail, the general principle is briefly described. Basically, the sweep gating logic, under the control of trigger signals from the trigger comparator and also feedback pulses from the hold-off circuit, supplies square-wave pulses to the switching transistor V1213 off the sawtooth generator.
The time-base capacitors (effectively in parallel with the switching transistor) are charged linearly through a constant-current source to provide the forward sweep, and are discharged rapidly by the switching transistor to provide the flyback period. The resulting sawtooth is fed to the X-final amplifier.

3.4.1. Sweep generator (unit A5)

The sweep speed or time coefficient is determined by the value of the time-base capacitance in circuit, and also by the magnitude of the charging resistor selected.
The time-base capacitors are C1204 and C1207. Capacitor C1204 is always in circuit, the other one is selected by the transistor V1216. This transistor operates as an electronic switch and is either fully cut-off or fully-conducting. It is switched on by the application of a positive voltage to its base from the TIME/DIV switch S10.
According to the position of S10, this transistor V1216 switches in the capacitor C1207 in parallel with C1204.
As mentioned, the sweep speed is also dependent upon the magnitude of the accurate constant-current supplied by transistor V1212. This current can be adjusted in steps by selecting the emitter resistance of V1212 by means of the TIME/DIV switch S10. Continuous control of the charging current can be effected by varying the base drive to V1212 with the continuous sweep control, TIME/DIV potentiometer R9. In the CAL position of this potentiometer, switch S11 closes and the charging current is solely determined by the calibrated emitter resistance.
To compensate for the temperature coefficient of the transistor, the base voltage of V1212 is supplied via transistor V1214.
This also has the advantage of reducing the load on the TIME/DIV potentiometer R9.
This transistor, in turn, has its base controlled by preset potentiometer R1232 when TIME/DIV switch S10 is in one of the positions 0,5 s/div. ... 0,5 ms/div.. This provides a fine adjustment for the timing circuit in the slower sweep speeds. In these positions the preset potentiometer R1232 provides an additional measure of control over the base voltage of V1212. In the positions of S10 when C1207 is not in circuit, the diode V1218 is blocked and the preset control R1232 is inoperative.

The discharge circuit for the capacitors C1204 and C1207 consists of resistor R1219 and transistor V1213. This switching transistor is driven by the sweep gating logic via a number of diodes. Diodes V1207 and V1208 form an AND-gate for positive logic. V1209 and V1211 adapt the level to control transistor V1213. The resulting sawtooth voltage is taken from two transistors V1219 and V1221 in a kind of Darlington pair configuration.
C1209 improves the transfer of faster sawtooth signals at the expense of the input impedance which need not to be that high then. The sawtooth voltage amplitude is approx. 5V. This sawtooth voltage is then fed to the X-final amplifier.

This sawtooth voltage is also applied as signal SAWTH to the comparator D2016 in the digital storage circuits. It is then used in MEMORY ON mode for the sequential sampling mode.

3.4.2. Hold-off circuit (unit A5)

The hold-off circuit prevents the sweep gating logic from responding to trigger pulses before the time-base capacitor has fully discharged. The sawtooth output from the Darlington pair V1219 and V1221 is applied to the base of emitter follower V1223.
The switching transistor V1217 switches the hold-off capacitor C1208 in circuit, parallel to C1206, according to the position of the TIME/DIV switch S10, in a similar manner to that described for the time-base integrator timing capacitor. Capacitor C1206 is always in circuit irrespective of the TIME/DIV switch position.
Charging current for the hold-off capacitors flows via transistor V1223. When V1223 cuts off the discharge current flows through R1228 and hold-off control R12. This current is adjustable to change the hold-off time. The voltage across hold-off capacitor C1206 or C1206 + C1208 follows the sawtooth voltage fairly fast in positive going direction via emitter follower V1223. When a certain value is reached, integrated Schmitt-trigger D1201 reacts and the end of the sweep is initiated.
This is followed by a hold-off period in which the voltage across the hold-off capacitor decreases fairly slowly until the lower switching level of the Schmitt trigger is reached. The system can now be triggered again. In the mean-time also the time-base integrator timing capacitor C1204 or C1204 + C1207 has reached its quiescent state. The output (point 6) of D1201 is low during the hold-off time, at any other moment this output is high.

3.4.3. Sweep gating logic (unit A5)

The sweep gating logic which consists of TTL logic circuits is controlled by the following signals:
- The trigger signals supplied by the trigger comparator.
- The voltage supplied by the hold-off circuit.
- The voltage supplied by the auto circuit via the hold-off circuit.

The TTL circuit D1201 contains four 2-input NAND-gates with Schmitt-trigger properties.
D1202 contains four normal 2-input NAND-gates and D1203 contains three normal 3-input NAND-gates.
With the aid of the various gates two flip-flops are formed.

See for the following explanation time relation diagram FIG. 3.7.

1 The incoming trigger signal from the trigger comparator switches the Schmitt-trigger output (D1201, point 11) to zero after a positive going edge has exceeded the upper switching level (+ 1,7 V) of this Schmitt-trigger.

2 After this, the first flip-flop output (D1202, point 3) is set to the logic 1-state.

3 If the negative going edge of the incoming trigger signal drops below the lower switching level (+ 0,9 V) of the Schmitt-trigger, the output (D1201, point 11) switches to logic 1 level again.

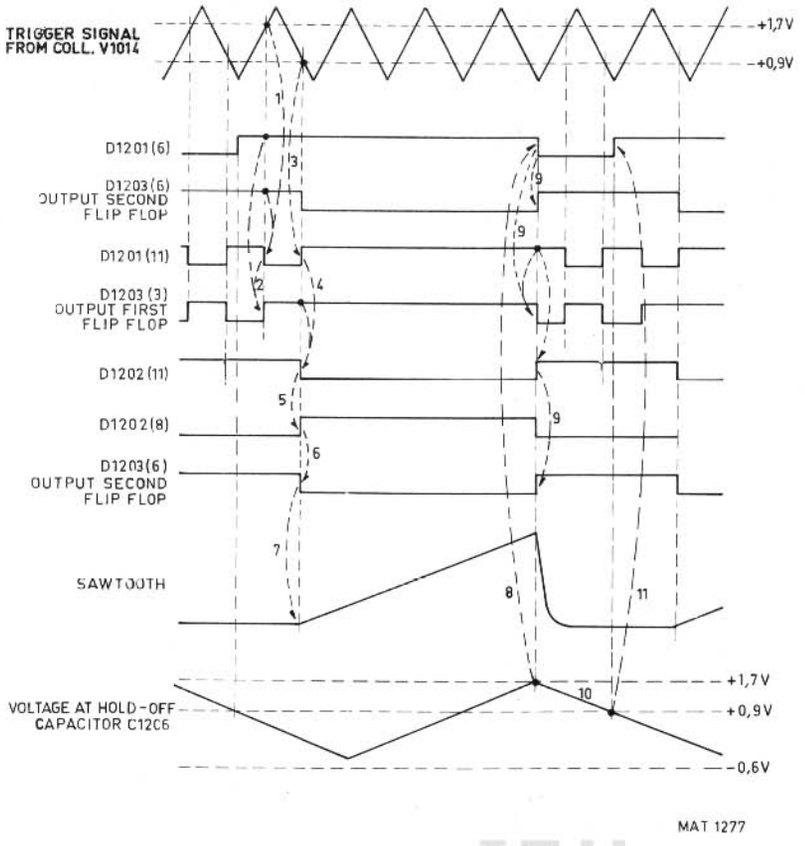


FIG. 3.7. Time relation diagram of the sweep-gating logic in the AC or DC mode.

4,5,6 The logic 1 state of the first flip-flop and the output signal of the Schmitt-trigger allows the setting of the second flip-flop output (D1203, point 6) to the zero state by means of the NAND output (D1202, point 11).

7 The output signal of the second flip-flop is applied to switching transistor V1213 via an OR-gate which consists of R1216, V1207 and V1208. This signal causes the sweep to start.

8 The end of the sweep is reached when the signal across the hold-off capacitor C1206 exceeds the upper switching level (+ 1,7 V) of the hold-off Schmitt-trigger. The output of this Schmitt-trigger switches then to zero.

9 Both flip-flops are now reset. Switching transistor V1213 starts conducting and time-base capacitor C1204 will discharge.

10 The voltage across the hold-off capacitor C1206 decreases slowly until the lower switching level (+ 0,9 V) of the Schmitt-trigger is reached.

11 This is the end of the hold-off period. The output (D1201, point 6) of the hold-off Schmitt-trigger rises to 1 again and the system can be triggered again.

3.4.4. Auto sweep circuit (unit A5)

In the absence of a trigger signal and with AUTO selected we would still like to see a display on the screen. The auto sweep circuit serves this purpose. After selection of the AUTO mode (AC and DC off) the voltage across capacitor C1202 starts increasing until after approximately 100 ms., transistor V1204 starts conducting and causes transistor V1206 to conduct. The collector of V1206 rises to approximately + 5 V and the signal AUTO will be logic "1". This is seen by the µP which in turn makes signal HTRG logic "1". The hold-off signal on point 6 of D1201 can now reach via gate D1201 (3) and the OR-gate, the switching transistor V1213. The loop is then closed and the time base generator is in the free running mode.
As soon as trigger pulses are available, the free-running state of the time-base generator is automatically terminated and normal triggering is resumed.

3.4.5. Final X amplifier (unit A5)

For normal time-base operation (MEMORY ON released) the FINAL X AMPLIFIER is fed by sweeps from the TIME-BASE circuit.

Transistor V1407 is then driven by the time-base generator via diodes V1411 and V1409 when R1406 is kept at + 12 V level TIME/DIV switch S10 (in all the TIME/DIV positions of this switch). With the TIME/DIV switch in the XDEFL position horizontal deflection from an other source than the time-base output is permitted. The amplifier stage V1404 when R1407 is then kept at + 12 V level via TIME/DIV switch S10 (in position X DEFL).
Transistor V1404 receives its input signal from D1001 point 8 of the trigger amplifier.
This signal is derived from one of the sources, channel A, channel B, line or an external source, depending on the setting of the X deflection selector switch S16.

The final X amplifier consists of two amplifier stages in parallel (one for each deflection plate).
Only one half is described.
The actual amplifier is the cascode circuit with transistors V1414 and V1416.
The resistors R1428 and R1429 are feedback resistors. The bias current for the amplifier is supplied by transistor V1413. The average voltage on the deflection plate is kept at + 26 V by means of zener diodes V1424 and V1426. Capacitor C1413 improves the h.f. response.
This final stage is supplied from the + 180 V and - 180 V because the X plates of the C.R.T. are mechanically displaced such that they are less sensitive than the Y plates.
The cascode amplifier stages are controlled via the transistors V1406 and V1407.
The bias of transistor V1406 can be varied with the X POSITION potentiometer R4, which consists of a tandem potentiometer with backlash, giving a nice vernier control. Variation of the bias causes the balance of the amplifier to be disturbed, which results in a horizontal trace shift on the screen.

The X amplifier allows choice from X deflection by the time base signal or one of the sources, channel A, channel B, line or an external signal. The deflection source is selected with the aid of the TIME/DIV switch S10 and the X-deflection source selector switch S16.

The X amplifier offers the possibility of using either the nominal gain (x 1 position of X MAGN switch S5), or the gain increased by a factor of 10 (x 10 position of X MAGN switch S5).

When the front-panel X MAGN switch is operated for 10 x magnification, the emitter resistance R1416 + R1417 of transistors V1406 and V1407 is shunted by resistors R1418 + R1419 reducing the value by a factor of 10. Consequently, the gain of the stage is increased by the same factor.
The x 1 gain can be set by potentiometer R1417 and the x 10 gain by potentiometer R1419. The x 10 gain is also operative when X DEFL is selected.

Both outputs of the X final amplifier are connected to the X-deflection plates of the C.R.T..

With MEMORY ON selected the addresses for the DISPLAY MEMORY are converted to an analog staircase signal by the microprocessor controlled X DAC and then applied as signal XOUT to the base of transistor V1407 in the FINAL X-AMPLIFIER via a SMOOTH filter and ADAPTION circuit.
At the same time the time-base sweep signal path via diodes V1411 and V1409 will be blocked by signal SHAR which is applied to the junction between diodes V1409 and V1411.

In X=A/Y=B mode the AVSB and QUARTER logic applies the signal value of channel A to the X DAC and the mean value of 2 adjacent channel B values to the Y DAC. This is controlled by the DISPLAY MEMORY COUNTER. Now the channel A signal is displayed horizontally and the channel B signal is displayed vertically.

QUARTER display is realized by the AVSB and QUARTER logic under the control of the microprocessor system.

For more detailed information about the digital storage units see section 3.7.

3.5. CATHODE-RAY TUBE CIRCUIT (Diagram 6)

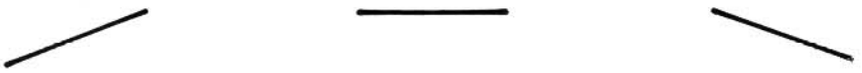
The cathode-ray tube circuit consists of the C.R.T. and its associated controls: focus, intensity, trace rotation and the beam blanking amplifier.

3.5.1. C.R.T. controls (unit A5)

By means of the INTENS potentiometer R1, the brightness of the display can be continuously controlled.
The display can be focused by means of the FOCUS potentiometer R6.
Both INTENS and FOCUS controls are front panel controls.
Furthermore the C.R.T. circuitry comprises preset potentiometers for trace rotation, astigmatism and geometry.
The FOCUS control R6 forms a part of a voltage divider network across the 1.5 kV output of the power supply.
The slider of this potentiometer is connected direct to the focus, grid G3.

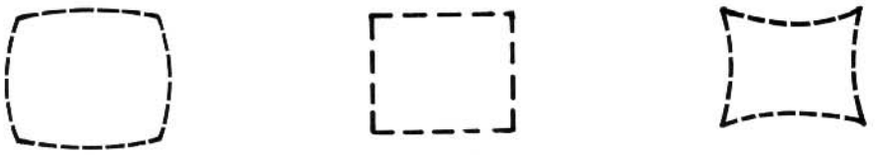
TRACE ROTATION is achieved by means of the trace rotation coil L1501. This coil mounted inside the mu-metal screen, provides a magnetic field for rotational control of the entire scan. The degree and direction of rotation is determined by the setting of front panel potentiometer R10 (srewdriver operated). The slider of R10 is connected to the bases of the complementary transistors V1521 and V1522.

The trace rotation coil L1501 is supplied by these transistors.



With the ASTIGMATISM control R1543, the form of the spot can be adjusted by influencing the voltage on the grids G2 and G4.

With the GEOMETRY control R1549 the barrel and pin-cushion distortion is corrected by influencing the voltage on the grid G7.



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3.5.2. Z amplifier (unit A5)

In MEMORY OFF the Z-amplifier receives two input signals. One signal originates in the time-base generator and is applied to the amplifier to unblank the trace during the sweep.
The other one is supplied by the ANALOG CHANNEL SWITCH to blank the trace during switching from channel to channel in the CHOP-mode.
The INTENS potentiometer R1 determines the amount of input current fed to the amplifier.

The 1.f. components of the blanking signal are modulated and demodulated (for voltage isolation purposes) before they are applied together with the a.c. - coupled h.f. voltage components to the Wehnelt cylinder.

In all TIME/DIV switch positions of the TIME/DIV switch S10, the anode of diode V1202 is kept at approx. + 12 V, resulting in a logic 1 level at input 1 of NAND D1203.
The output point 12 of this NAND is now at logic 1 level when either input 2 or input 3 is low. In other words only during a sweep.
In the X DEFL position of the TIME/DIV switch S10, input 1 of NAND D1203 is at logic 0 level, and in that case the output point 12 of this NAND is steady at logic 1 level. This output signal is inverted by a NAND and fed via diodes V1501 to diodes V1502 and V1503 of the beam blanking amplifier.
The CHOP mode blanking signal from the channel switch is fed to transistor V1506 via R1502. The inverted and amplified signal is applied to diode V1508.
Both signals are joined together at the base of transistor V1514 (point A in figure 3.8.). This is the virtual earth point of a shunt feedback amplifier.

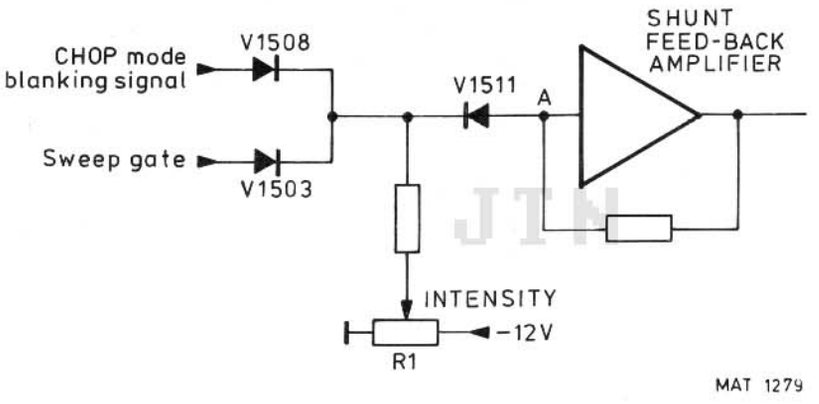

FIG. 3.8. Shunt feed back amplifier.

Assume that V1503 and V1508 are turned-off by applying a logic zero to both inputs.
Then the output voltage of the amplifier can be varied with the aid of INTENS potentiometer R1. The light on the screen is variable then e.g. during a sweep or in the X deflection mode. A logic 1 on either one or both inputs of the diodes V1503 and V1508 turns V1511 off. The C.R.T. is then blank e.g. between sweeps or during the sweep when there is channel switching in the CHOP mode.

The blanking signal is amplified in the stage with transistors V1512, V1513 and V1514. At the output of this amplifier the a.c. and d.c. components of the blanking signal are guided along different paths. The a.c. path runs straight to the Wehnelt cylinder of the C.R.T. via capacitor C1512.
A d.c. signal is fed to the emitter of transistor V1517 via a low-pass filter R1528/C1508/R1527. Transistor V1517 constitutes a multivibrator together with transistor V1516. The a.c. voltage on the collector of V1517 has a peak-to-peak value which depends on the voltage fed to the emitter of V1516 by the shunt feed back amplifier.

The a.c. voltage supplied by multivibrator V1516/V1517 is applied to a peak detector. This peak detector rectifies this a.c. voltage.

The reason for the a.c. and d.c. paths is isolation of the cathode and Wehnelt cylinder, which are on a - 1,5 kV potential, from the other circuits. The a.c. component of the blanking signal is transmitted straight away to the high-voltage part via blocking capacitor C1512, which is a high voltage capacitor. The d.c. signal, however, is converted into an a.c. voltage and then transmitted to the high-voltage part, via capacitor C1509,after which it is rectified by means of diode V1519.
The dark level can be adjusted with the aid of potentiometer R1534 in the emitter circuit of transistor V1517 in the d.c. amplifier.

In MEMORY ON the way in which the contents of the DISPLAY MEMORY is displayed on the C.R.T. screen depends on the functions which are selected by the operator.
The contents of the DISPLAY MEMORY are 4096 words, each consisting of 8 bits. Each 8-bit word is capable of indicating 256 different amplitudes (i.e. $2^8 = 256$) : Y values.
Each address of the memory corresponds to a by the selected function specified vertical line of the display along the X-axis.

The 4000 words of the DISPLAY MEMORY contents of 4096 words are displayed in a display area of more than 8 vertical divisions and 10 horizontal divisions which is divided into 256 x 4000 dots. (96 dots are displayed outside the 10 horizontal divisions).
A µP-controlled DISPLAY COUNTER sends 4096 different addresses sequentially (starting with address 0 and ending with address 4095) to the DISPLAY MEMORY and to the Digital-to-Analog-Converter (DAC) of the X-system. To provide the discrete steps for the horizontal time-base display the output of the X-DAC (signal XOUT) is a linear staircase voltage, which is applied to the FINAL X-AMPLIFIER.

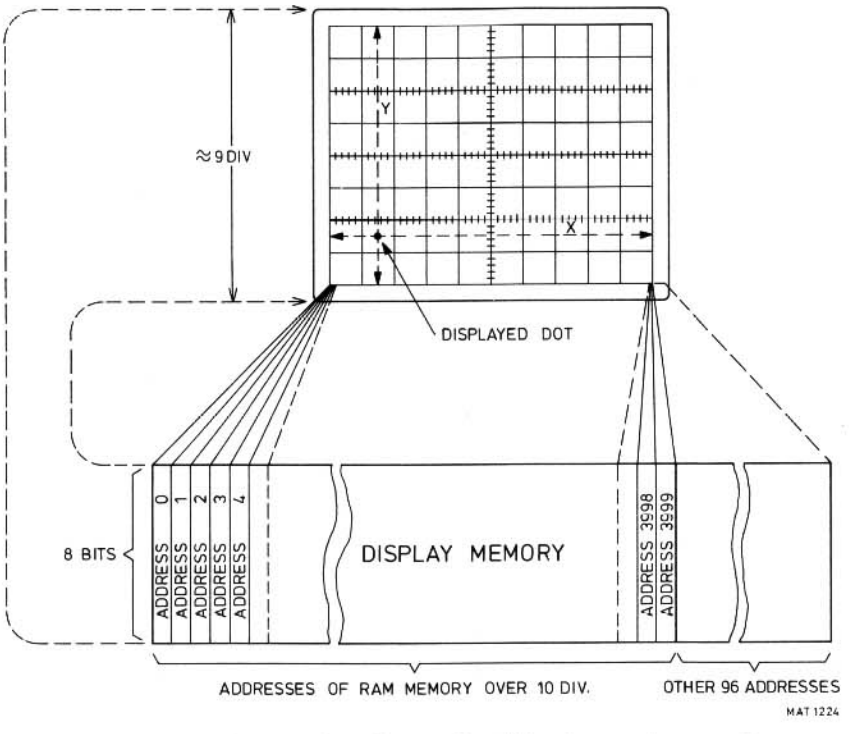

FIG. 3.9. Complete display of all the values of one channel.

Similarly, the 8-bit instantaneous values for each address (i.e. the Y-information) are converted into analog signals by means of the Y-DAC. The converted signal is then applied to the FINAL-Y-AMPLIFIER.

In MEMORY ON mode (signal ZMODE is active) the blanking pulse ZMOD for the different display modes is generated by the display memory logic. This ZMOD pulse is guided via NAND D1203 to the cathode of diode V1501.

3.5.3. Calibrator (unit A5)

The calibrator circuit consists of transistors V1601 and V1603, which are configurated as a stable multivibrator such as used in the channel switch. Good shape of the wave-form is obtained by a constant current supplied by transistor V1602 which will flow in turns through the left hand or right hand transistor. The amplitude is 1,2 V or 6 div. in the 20 mV/div. attenuator positions. (The straight through position of the attenuator).
Potentiometer R1607 allows accurate adjustment of the amplitude of the calibrator output voltage. This square-wave output voltage is taken off from the collector of transistor V1603 and fed to socket X1. This is the front panel CAL terminal.
The calibrator output signal can be used for probe compensation and/or checking the vertical deflection accuracy.

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3.6. POWER SUPPLY (Diagram 7)

3.6.1. General

The power supply is designed on the switching regulator principle and permits the instrument to be connected to nominal mains voltages of 100V, 120V, 220V or 240V by switch selection, or to an external battery supply of 24...27 V.
The mains supply via POWER ON switch S17 is protected by fuse F202. The battery input is protected by fuse F201 and diode V206 safe-quards the circuit against reversed battery connection.
Basically, the power supply consists of:

- Mains transformer
- Converter and stabilized power supply
- Illumination circuit

3.6.2. Mains transformer (unit A1)

An incoming mains voltage is fed via the thermal fuse (F101) and the voltage selector S101 to the appropriate primary taps on the mains transformer T101. Transformer T101 has three primary windings which can be combined by means of voltage adapter S18. This combination allows the instrument to be used with mains voltages of 100V,120V,220V or 240V.

The voltage on the secundary windings of this transformer is full-wave rectified. The resulting negative d.c. voltage (approx. 24 V) across electrolytic capacitor C203, or alternatively a negative d.c. voltage on the rear panel DC POWER IN input socket X11, is applied to the voltage stabilizer and converter.

Part of the a.c. voltage on the secundary winding of the mains transformer is fed via C201, R373 and R372 to LINE trigger source selector switch S16A, to enable internal triggering on the line frequency.

3.6.3. Converter and stabilized power supply (unit A1)

The converter is a square-wave generator operating at a frequency of approx. 18 kHz and driven by the d.c. voltage across the electrolytic capacitor C203.
A basic diagram of the converter is shown in figure 3.10.

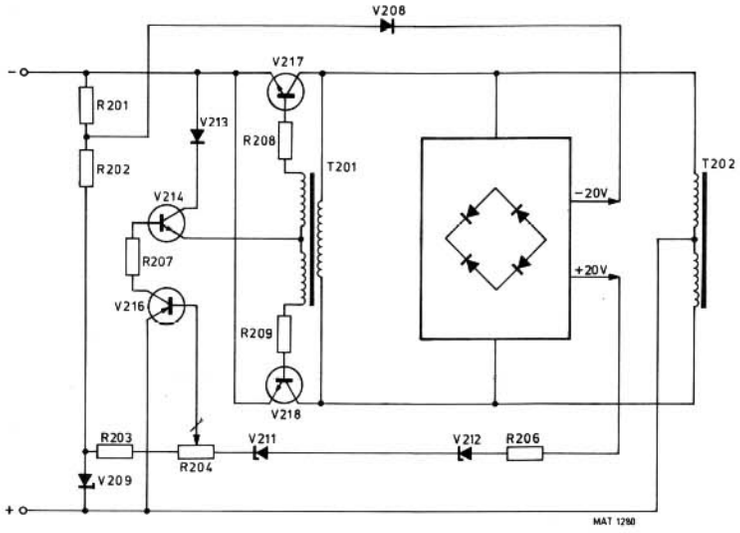

FIG. 3.10. Basic diagram of the converter.

In the converter, transistors V217 and V218 function as switches and regulators and alternately connect the negative supply voltage to either end of the primary of T201/T202. Assume that transistor V217 has a slightly higher current gain than V218. Then the positive voltage from the feedback winding quickly drives transistor V217 into saturation. The current in the top half of the primary of T201/T202 increases linearly at a rate determined by the inductance of the primary. This current increase continues until the iron in transformer coil T201 is saturated.
Then the magnetic lines of flux stop changing and consequently no voltage is induced any longer in the feedback winding. When its base drive ceases, the transistor is cut off.
This reverses the polarity of the feedback voltage and transistor V218 is turned hard on. The bottom half of the primary then passes an increasing current until the core is saturated in the opposite direction.
The subsequent absence of feedback voltage initiates the switching back to V217 and the cycle starts again.

The regulation works as follows. When an input voltage is applied to the converter, the negative voltage across Zener diode V209 turns transistor V216 fully on, as there is no positive voltage from temperature compensation stabistors V211 and V212.
Then a bias current flows via transistor V216 through resistor R207, through the base-emitter junction of transistor V214 (operating as a diode since diode V213 interrupts the collector circuit) and from base to emitter of both transistors V217 and V218.
As there is then an a.c. voltage across the primary of T201/T202, diodes V222 and V223 produce a positive d.c. voltage of + 20 V across capacitor C209. This voltage reduces the current through transistors V216 and V214 sufficiently to limit the drive to transistors V217 and V218 and produce the desired output level.
The setting of potentiometer R204 determines the value of the regulated output voltage. Possible differences from the set output voltage are fed back via the temperature compensation stabistors V211 and V212 to transistor V216 so that the drive of transistors V217 and V218 is adapted so as to compensate for the differences. This also applies to mains voltage fluctuations.

After rectifying and smoothing, the secundary voltages + 5V, + 12V, - 12V, + 38V, + 180V, - 180V, - 1500V and post acceleration voltage + 8500V are obtained. The voltage quadrupler which supplies the + 8500 V cannot be repaired and must be replaced when it breaks down. T202 contains a separate secundary winding for the heater voltage for the C.R.T.
All supply voltages except the + 8500V and the - 1500V can be continuously short-circuited without damage to the components. Resistor R202 limits the collector current when the output is short-circuited and the switching action is stopped, thereby holding the dissipated power in transistors V217 and V218 at a safe level.
Thus, the power supply of the oscilloscope is fully protected against short-circuts. A short-circuit is indicated either by a squeeking noise coming from the power supply or by the pilot lamp B1, which indicates the ON state of the oscilloscope, failing to light up.
If supplied by an external d.c. voltage, the instrument is protected against overloads and wrong polarity by internal fuse F201 and diode V206.

3.6.4. Illumination circuit (unit A6 - Diagram 7)

The graticule of the C.R.T. can be illuminated by means of the bulbs E1. The intensity can be varied with the aid of ILLUM potentiometer R11 which controls the collector current (which is the current through the bulbs) of transistor V207. The illumination circuit is not short-circuit proof.

3.6.5. + 5V DC unit (unit A8 - diagram 7)

The voltages on points A, B and C on the secundary windings of transformer T202 are applied to a separate 5V DC unit (UNIT A8). These voltages are full-wave rectified and the resulting positive and negative d.c. voltages over capacitors C252 and C251 are applied to logic unit A11.

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3.7. DIGITAL STORAGE CIRCUITS

3.7.1. General

The digital storage circuits consisting of the ADAPTION unit A9, the MIN/MAX unit A10 and the LOGIC unit A11 are described now.

Because the complete system is controlled by a microprocessor control system, first this system will be described.

3.7.2. Microprocessor control circuit (unit A11 - diagram 8).

3.7.2.1. Input shift register.

This circuit consists of four digital shift registers D2011, D2046, D2078 and D2104 which are connected in serial.

The data inputs are connected to the front panel switches of which the settings must be known by the microprocessor system.

Input switches and signals:

CML0, CML1, CML2 — A-ALT-CHOP-ADD-B settings from the vertical mode switch S1 of the analog oscilloscope part.

	CML0	CML1	CML2
A	0	0	0
ALT	1	1	1
CHOP	1	0	0
ADD	1	1	0
B	1	1	0

$\overline{\text{DUAL IN}}$ — Signal from DUAL SLOPE switch S32.

AUTO — Signal from collector V1206.

TB2, TB3, TB4, TB5, TB6, TB7 — Signals from TIME/DIV switch S10.

X	X	TB2	TB3	TB4	TB5	TB6	TB7	
1	1	0	0	0	1	1	0	0,1/us/div.
1	1	0	0	1	1	1	0	0,2/us/div.
1	1	0	0	1	1	1	1	0,5/us/div.
1	1	0	0	0	0	1	1	1/us/div.
1	1	0	1	0	0	1	1	2/us/div.
1	1	0	1	0	0	0	1	5/us/div.
1	1	1	0	0	0	0	1	10/us/div.
1	1	1	0	0	1	0	1	20/us/div.
1	1	0	1	0	1	0	1	50/us/div.
1	1	0	1	0	0	1	0	0,1ms/div.
1	1	1	1	1	0	1	0	0,2ms/div.
1	1	1	1	1	0	0	0	0,5ms/div.
1	1	1	1	0	0	0	0	1ms/div.
1	1	1	1	0	0	0	1	2ms/div.
1	1	1	1	1	0	0	1	5ms/div.
1	1	1	0	1	0	0	0	10ms/div.
1	1	1	0	1	1	0	0	20ms/div.
1	1	0	0	1	1	0	0	50ms/div.
1	1	0	0	1	0	1	0	0,1s/div.
1	1	0	1	1	0	1	0	0,2s/div.
1	1	0	1	1	1	0	0	0,5s/div.

SMOOTH
ABCDCHOP
MEMDUMP
MIN/MAXI
X=A/Y=B
TIME/DIV
PRETRIG
OFF
QUART
COMPARE
LOCK
CLEAR
RESET
SINGLE
STORE

Shift register parallel operation:

If signal LTXT (load text) = logic "1", the input signals on the data inputs are latched into the digital shift register.

Shift register serial operation:

When the microprocessor places address 8000H on the multiplexed address/data bus, the $\overline{IO8}$ signal is going to logic "0".
The $\overline{IO8}$ signal combined with $\overline{RDUP}$ results in $\overline{IORD8}$ which is used as clockpulse for the shiftregister. The register reacts on the positive going edge of the $\overline{IORD8}$ signal.

To read the complete shift register contents by the microprocessor system, 32 clockpulses (32 x $\overline{IORD8}$) are needed.

As result an output signal SHROUT (shiftregister output) is applied to the INPUT LOGIC circuit D2116.

Furthermore the signals STORE and SHAR are derived from the MEMORY ON pushbutton on the front panel.
Signal SHAR (store-hardware) is on a + or - 12 V level to switch the diode switches on the amplifier board and is converted into a signal STORE with TTL level.

3.7.2.2. Microprocessor system.

The microprocessor system basically consists of the following circuit elements:

- A microprocessor for controlling and organizing data flow. (8085 - D2121).
- Erasable and programmable read-only memory (EPROM) for system programming. (D2082).
- Integrated peripheral circuit with random access memory (RAM) with I/O ports and TIMER. (8155H2 - D2064).
- Address selection latch for the address-bus. (74LS373 - D2096)
- Decoders for RAM and ROM selection and address decoding. (74LS138 - D2113).
- Two way buffer to the system data-bus. (74LS245 - D2101).
- Tri-state buffer to the system address-bus. (74LS244 - D2122/D2127).
- Input port. (74LS244 - D2116).
- Two output ports. (74LS373 - D2118/D2117).
- Shift register and LED BAR UNIT. (74LS164 - D541).

The heart of the microprocessor control circuit is integrated circuit D2121, an 8-bit microprocessor type 8085 with 16 address lines.
The first eight address lines are time-multiplexed with the eight data lines and are defined as AD0 ... AD7.
Demultiplexing is performed with the aid of the signal ALE from the 8085.
The groups of output signals AUP0 ... AUP7 and AUP8 ... AUP15 constitute the address bus.

/uP cristal connections X_1 and X_2.

A 5 MHz crystal is connected to the clock inputs X_1 and X_2 of the microprocessor to provide an accurate timing reference source.

/uP $\overline{\text{RESIN}}$ input

After switching ON a reset level of logic "0" is available on the $\overline{\text{RESIN}}$ input.
This reset signal forces the microprocessor to initiate the main programm, beginning at the address 0000H. After a certain RC-time the reset level becomes logic "1" and the microprocessor is ready for use.

/uP SID (Serial input data)

The microprocessor will receive on this SID input the information from the SERVICE jumper.

/uP SOD (Serial output data)

The microprocessor generates on this SOD output a software trigger for the Service Routines.

Connection to the internal address-bus via the address latch D2096

The first eight address bits placed by the microprocessor on its multiplexed address-data bus lines AD0 ... AD7 have to be separated from the eight data bits.
This is achieved by address latch D2096.
Demultiplexing is performed with the aid of the signal ALE from the 8085.
The groups of output signals AUP0 ... AUP7 and AUP8 ... AUP15 constitute the address bus.

Connection to the system data-bus via the bidirectional data buffer D2101.

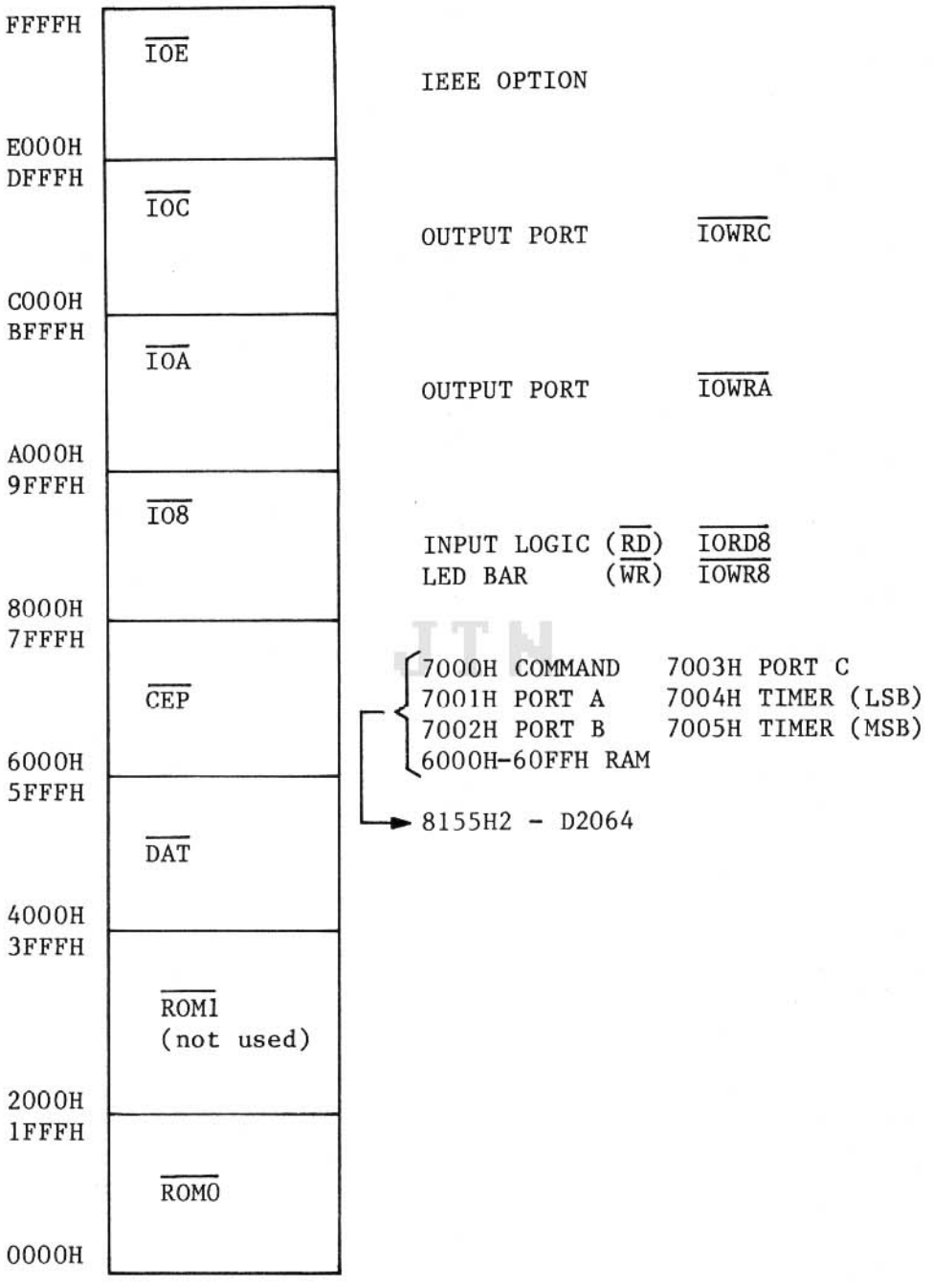
The eight data bits from the microprocessor have to be coupled to the system data bus.
This coupling is done by the bidirectional data buffer D2101.
This buffer is selected if $\overline{\text{DATUPC}}$ is logic "0".
Input or output data depends on the logic level of signal $\overline{\text{RDUP}}$.
$\overline{\text{RDUP}}$ = logic "1" means OUTPUT
$\overline{\text{RDUP}}$ = logic "0" means INPUT

Data is transported between the D2101 in- and outputs and the system data-bus over the lines D0 ... D7.

Connection to the system address bus via the tri-state buffer D2122 + D2127.

The address bus lines are connected to the system address bus lines AUPB0 ... AUPB11 via the tri-state buffer D2122 + D2127.
The lines AUPB0 ... AUPB11 are applied to the DISPLAY MEMORY for DATA handling.
Signal $\overline{\text{DATUPC}}$ is then low.

SYSTEM MEMORY MAP



ADDRESS DECODING

ROM -/uP RAM -I/O ports-DATA selection.

In decoder D2113, 8 select signals are generated as follows:

AUP15	AUP14	AUP13	Output signal	Addresses	
0	0	0	$\overline{ROM0}$	0000H-1FFFH	ROM select signal.
0	0	1	$\overline{ROM1}$	2000H-3FFFH	Not used.
0	1	0	$\overline{DAT}$	4000H-5FFFH	DISPLAY MEMORY select signal for /uP control of DISPLAY MEMORY.
0	1	1	$\overline{CEP}$	6000H-6FFFH	RAM select (8155)
				7000H-7FFFh	I/O select (8155)
1	0	0	$\overline{IO8}$	8000H-9FFFH	Select for input logic + led bar + start input and display cycle.
1	0	1	$\overline{IOA}$	A000H-BFFFH	I/O select signal.
1	1	0	$\overline{IOC}$	C000H-DFFFH	I/O select signal.
1	1	1	$\overline{IOE}$	E000H-FFFFH	Select signal for IEEE option.

The following select signals are derived from the output decoder I/O select signals $\overline{IO8}$ - $\overline{IOA}$ and $\overline{IOC}$.

$\overline{IO8}$ --> $\overline{IORD8}$	points to INPUT LOGIC	(Read action).
$\overline{IO8}$ --> $\overline{IOWR8}$	points to LED BAR UNIT and start input and display cycle.	(Write action).
$\overline{IOA}$ --> $\overline{IOWRA}$	points to OUTPUT PORT	(Write action).
$\overline{IOC}$ --> $\overline{IOWRC}$	points to OUTPUT PORT	(Write action).

ROM MEMORY

The ROM (read-only memory), which contains the system programm, consists of the EPROM chip D2082 of 4k bytes (4096 x 8 bits).
If an IEEE-488 option is installed, an EPROM of 8K bytes is used.
The reserved ROM addresses are 0000H up to 1FFFH.
Because the microprocessor's first eight address lines AD0 ... AD7 are time-multiplexed in the microprocessor with the data lines, the addresses have to be latched by the address latch D2096 on the ALE signal.
These signals are placed on the microprocessor board internal address bus lines AUP0 ... AUP7.

Each ROM memory address can be selected by the address lines AUP0 ... AUP7 together with address lines AUP8 - 9 - 10 - 11 and 12.

The ROM memory chip is selected by the read signal $\overline{RDUP}$ and the ROM selection signal $\overline{ROM0}$.

When a certain ROM address is selected in this way, the contents of the selected location are placed on the data bus lines DUP0 ... DUP7.

/uP-RAM MEMORY

The /uP-RAM (microprocessor random access memory) is used by the microprocessor for stack purposes and for storage of variable data.
It is a part of the chip D2064 (8155H2) which is a RAM + I/O ports + TIMER. The RAM consists of 256 x 8 bits.

Each µP-RAM memory address can be selected by the internal data/address lines DUP0 ... DUP7 on the signal ALE.
The RAM is selected when the signals $\overline{CEP}$ and AUP12 are logic "0".

Reading the RAM contents or writing data into a RAM location is controlled by the signals $\overline{RDUP}$ and $\overline{WRUP}$.

The data to be written into, or read from the RAM memory is also transported via the multiplexed address/data bus DUP0 ... DUP7.

INPUT LOGIC

When the microprocessor places the address 8000H on the multiplexed address bus, this results in signal $\overline{IO8}$ going to logic "0".
This $\overline{IO8}$ combined with the $\overline{RDUP}$ signal to $\overline{IORD8}$ enables the INPUT LOGIC buffer D2116 to place its input data byte on the internal data/address bus lines DUP0 ... DUP7.

This byte consists of the following signals:

Bit 0	TRGRD	Triggered.	
Bit 1	EINP	End input.	When "0", input cycle is going When "1", input cycle is ready
Bit 2	EXTCL	External clock.	
Bit 3	DT	Display timing pulse.	When "0", display cycle is going When "1", display cycle is ready
Bit 4	INT(option)	Interrupt from IEEE option.	
Bit 5	+ 5 V	Not used.	
Bit 6	+ 5 V	Not used.	
Bit 7	SHROUT	Input shift register output signal containing the setting of the front panel switches which are communicating with the µP.	

OUTPUT PORT D2118.

When the microprocessor places the address A000H on the multiplexed address/data bus, this results in signal $\overline{IOA}$ going to logic "0".
This $\overline{IOA}$ signal combined with the $\overline{WRUP}$ signal enables the data latch (output port) D2118 to latch the byte of data present on the multiplexed address/data bus.

The data byte consists of the following signals:

Bit 0	STAD0	3 L.S.B.'s of the start address for the display counter.	(for 1,2,4,or 8 trace display.)
Bit 1	STAD1		
Bit 2	STAD2		
Bit 3	STAD9	3 M.S.B.'s of the start address for the display counter.	(for quarter display.)
Bit 4	STAD10		
Bit 5	STAD11		
Bit 6	Control signal for the NOT TRIG'D lamp.		
Bit 7	Control signal for the REMOTE lamp.		

OUTPUT PORT D2117.

When the microprocessor places the address C000H on the multiplexed address/data bus, this results in signal $\overline{IOC}$ going to logic "0".
This $\overline{IOC}$ signal combined with the $\overline{WRUP}$ signal enables the data latch (output port) D2117 to latch the byte of data present on the multiplexed address/data bus.

The data byte consists of the following signals:

Bit 0 TBT — Signal to block the time-base TIMER OUT signal in 0,2ms/div., 0,5ms/div. and 1ms/div..

Bit 1 TBC, Bit 2 TBD — TB:2/:5/:10

TBD	TBC	
1	0	= :2
0	1	= :5
0	0	= :10

Bit 3 PRTR0, Bit 4 PRTR1, Bit 5 PRTR2 — PRE-TRIGGER LENGTH

PRTR2	PRTR1	PRTR0	
1	1	1	= 0
1	1	0	= 1/4
1	0	0	= 1/2
0	1	0	= 3/4
0	0	0	= 1

Bit 6 Control line for the REP ONLY lamp.
Bit 7 Not used.

LED BAR UNIT

When the microprocessor places the address 8000H on the multiplexed address/data bus, this results in signal $\overline{IO8}$ going to logic "0".
This $\overline{IO8}$ signal combined with the $\overline{WRUP}$ signal to $\overline{IOWR8}$ enables the LED BAR driver shift register D541 to react on input clock signals derived from DUP1.
The shift register input data is applied to the shift register data input via the DUP0-line.

Data line DUP2 has a function as "start display" (D2087 Pt12) STDIS and data line DUP3 has a function as "start input" (D2006 Pt12) STINP.

8155 RAM with I/O PORTS and TIMER (D2064).

The RAM portion is organized as 256 x 8 bit and is used as /uP-RAM as described before. (RAM addresses: 6000H -60FFH).
The I/O portion consists of the three general purpose I/O ports A, B and C.
(I/O addresses: PORT A - 7001H / PORT B - 7002H / PORT C - 7003H).
A 14 bit programmable counter/timer is included to provide pulses for the TIME/BASE system, and its timer modes are programmable.
Input - TIMER IN
Output - TIMER OUT
(TIMER addresses: 7004H for the LSB and 7005H for the MSB of the internal Count Length Register.
The command/status address is 7000H.

IEEE option

Communication with the IEEE interface option is done via the 8 data/address lines DUP0 .... DUP7.
The address selection signal for the interface is signal IOE which is active in the address range E000H and higher.

3.7.3. Adaption circuit (unit A9 - diagram 9)

The DELAY LINE output is coupled to the ADAPTION UNIT A9.

Depending on the selection of MEMORY OFF or MEMORY ON the signal is applied via the so-called "analog signal path" or the so-called "digital signal path".

Selection of the analog signal path (MEMORY OFF) means that the DELAY LINE output is directly coupled to the input of the FINAL Y AMPLIFIER via relay-contacts K1701 and K1702.
Signal $\overline{\text{SHAR}}$ is then + 12V.

Selection of the digital signal path (MEMORY ON) means that the DELAY LINE output is coupled to the ADAPTION circuit and then to the MIN/MAX unit.

The DELAY LINE is terminated by resistors R1704 and R1706.
With SHAR = +12V transistors V1707 and V1708 are conducting, thus coupling the DELAY LINE output signals to the MIN/MAX unit inputs.

JTN

3.7.4. Min/max circuit (unit A10 - diagram 10)

If no MIN/MAX mode is selected (signal MIN/MAX = 0) the DELAY LINE is coupled via amplifier stage D2501 to the transistors V2517 and V2518 of the common base circuits before the output CHERRY-HOOPER stage.

With MIN/MAX selected (signal MIN/MAX = 1) the DELAY LINE is coupled via amplifier stage D2501 to the transistors V2504 and V2506 of the common base circuits before the CHERRY-HOOPER stage consisting of transistors D2502.

From here the signals are applied to the MINimum and MAXimum peak detectors D2503 and D2504.
These circuits determine the minimum and maximum amplitude of the analog input signal during two periods of the sampling frequency.

The resulting MIN and MAX values are applied to a MIN/MAX multiplexer consisting of the two circuits D2507 and D2508.
The MIN value only appears at the output of D2507 when signal $\overline{\text{MIP}}$ is active and the MAX value appears at the output of D2508 when signal $\overline{\text{MAP}}$ is active.
The output of the MIN/MAX multiplexer is coupled to transistors V2517 and V2518 of the output stage.

At the end of each cycle the peak detectors are resetted by pulses RESMIN and RESMAX (see timing diagram).

The resulting analog signal MIN/MAX OUT is applied to a track and hold (T&H) gate D2092 and then digitized in an Analog to Digital Convertor (ADC) D2112 on logic unit A11.

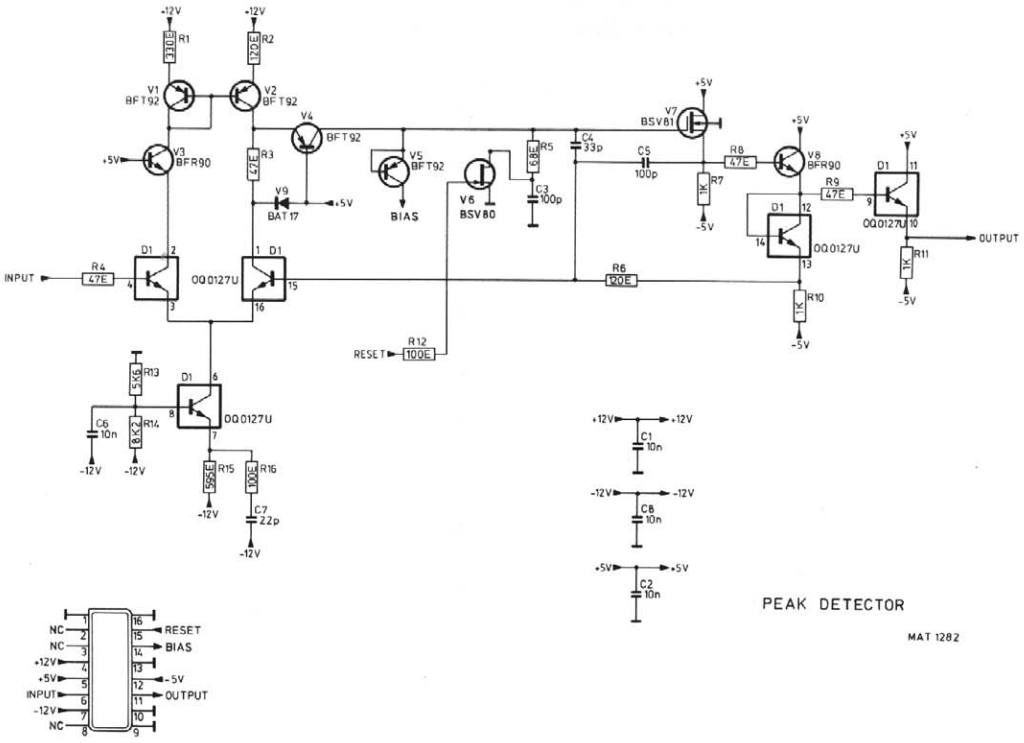
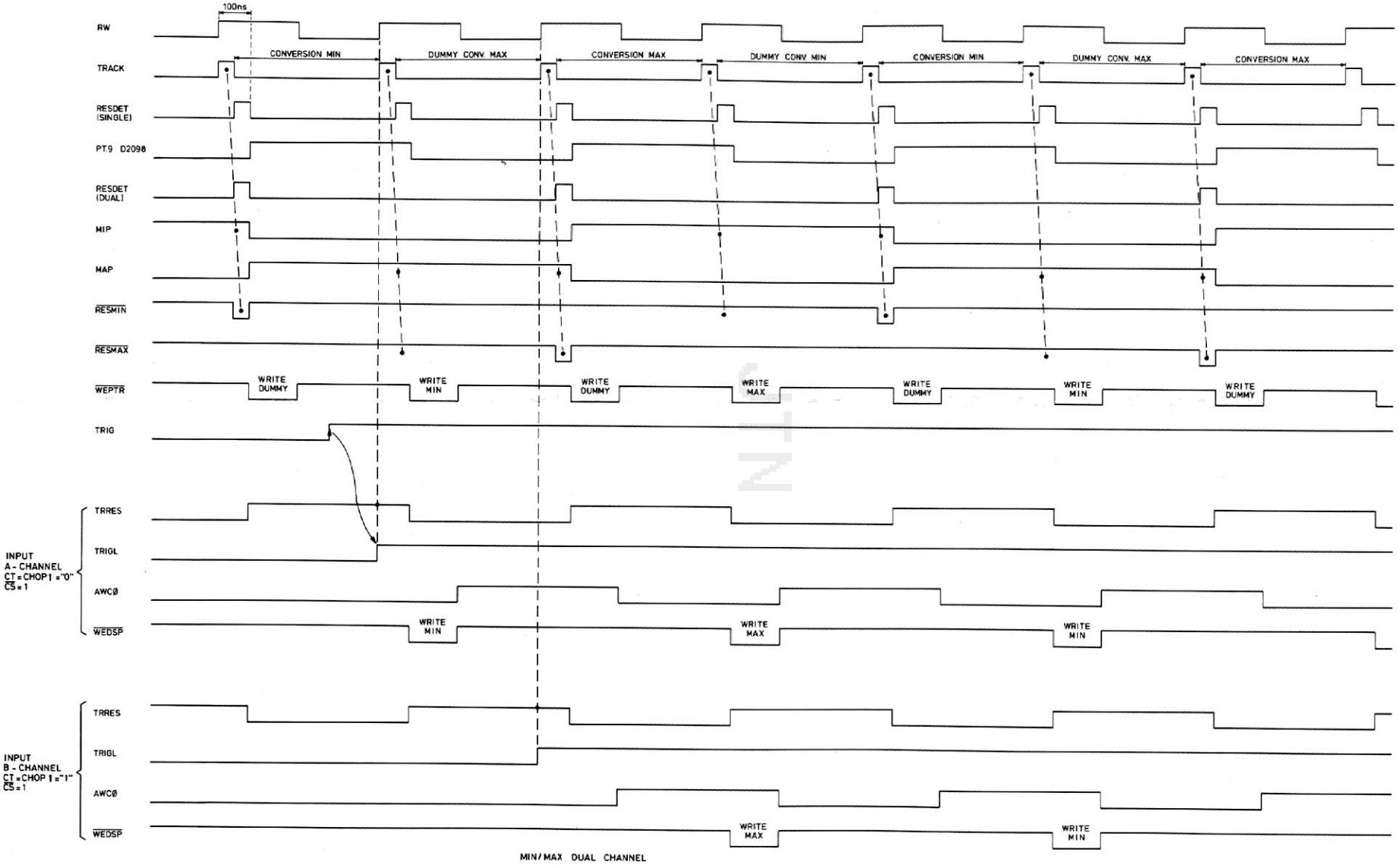


FIG. 3.11. Min/max timing diagram + peak detector.



MIN/MAX DUAL CHANNEL

MAT 1261

3.7.5. Input/display circuit (unit A11 - diagram 11)

Analog to digital conversion.

The analog signal to be digitized is applied from the MIN/MAX circuitry to a track and hold gate (T&H) D2092.
This T&H gate tracks the input signal continuously and at a command TRACK its output is held to the momentary value of the input signal.
Signal TRACK is generated in the ADC logic.

$\overline{\text{TRACK}}$ = logic "0" The circuit only tracks the input level.
$\overline{\text{TRACK}}$ = logic "1" The circuit holds the input level that was present at the positive going edge of the $\overline{\text{TRACK}}$ signal. (= HOLD).

The T&H output signal THOUT is applied to the ADC input (D2112-Pt16) and must be held to the same value at least for the time that is needed by the ADC for conversion (the so-called conversion time of about 450 ns.). It is converted into an 8-bit digital number. (ADC00 ... ADC07).

The ADC needs a reference voltage of about 0,5V $\pm$ 0,5%. This VREF voltage can be measured on testpoint X2027 and can be adjusted with potentiometer R 2086.

Conversion is controlled by the 10 clockpulses CLADC and by the signal STADC (start ADC) which are generated in the ADC logic.
After the first clockpulse the ADC switches the BUSY-signal to logic "1".
At the end of the conversion of an input signal sample into 8 bits digital information, the ADC switches the signal BUSY to logic "0" again, thus indicating that conversion is completed.

The ADC output signals are applied now to tri-state buffer D2111. They are also connected to the ADC OUT connector X10 on the rear panel of the instrument.

The timing of the conversion is determined by one of the following three sources:

1. In DIRECT-mode by the TIME-BASE GENERATOR. (5 s/div. ... 0,2 ms/div.)
2. In SAMPLING-mode by comparing the analog time-base sawtooth signal and a staircase signal DACSTAIR. (100 µs/div. ... 0,1 µs/div.)
3. In EXTERNAL-CLOCK-mode by the external clock input on the front panel.

At the end of each conversion, the ADC logic generates the positive going edge of the TRACK signal.

This means that new data is ready. The TRACK signal is applied to Pt 11 of flip flop D2077.
The setting of this flip flop results in signal NDR (new data ready) going to logic "1".
Now the conversion ritm has to be synchronized to the read/write ritm of the pretrigger memory. This is done by the TRIGL flip flop.

The MEMORY WRITE LOGIC derives from each NDRL signal a pulse $\overline{\text{WEPTR}}$ (write enable pre-trigger). This circuit detects whether an NDR is present or not.
With $\overline{\text{WEPTR}}$ the tri-state buffer D2111 is enabled with as result that the ADC output bits are placed on the P0 ...P7 pretrigger memory

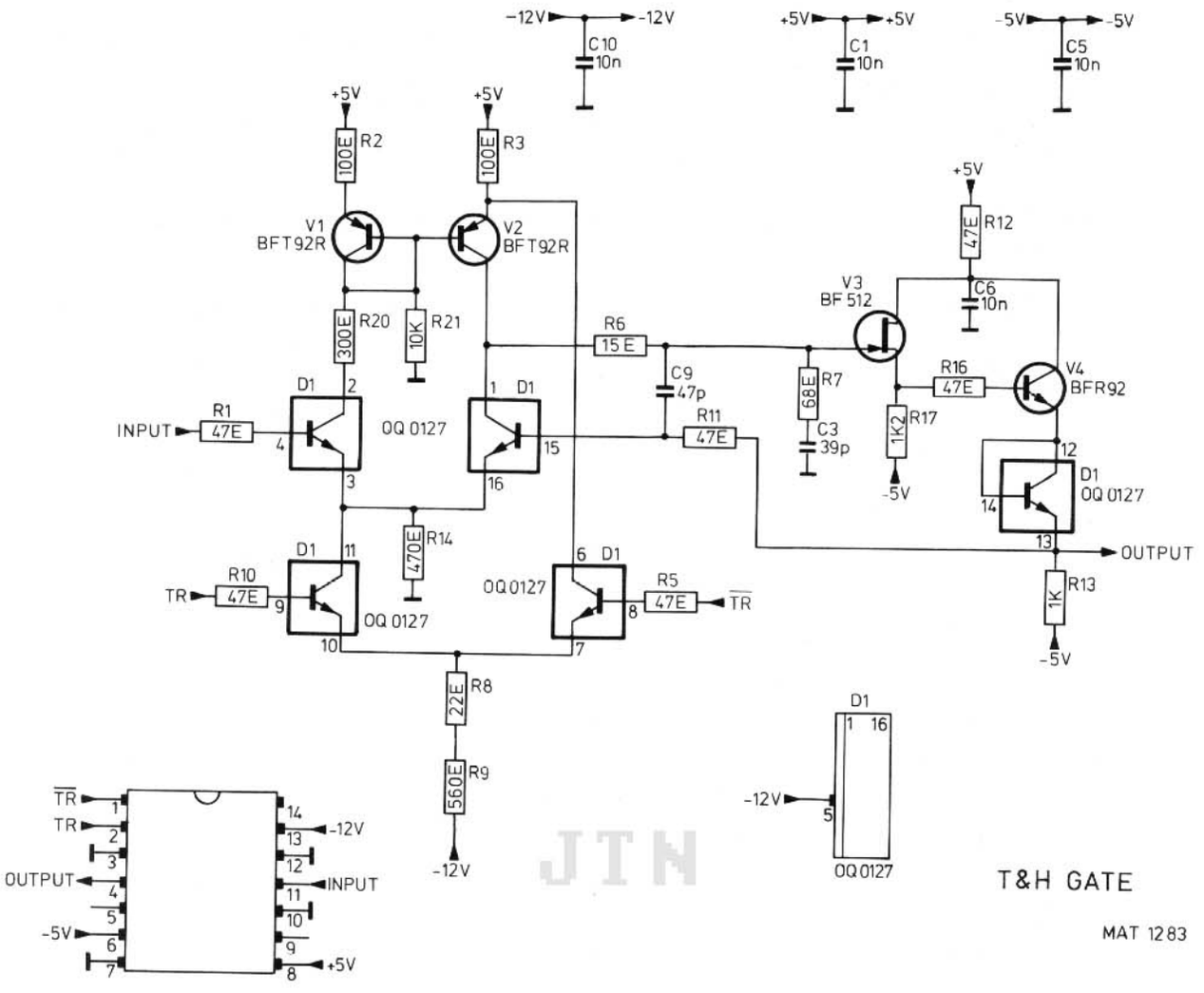


FIG. 3.12. T&H gate.

databus system. This digital number is then stored in the PRE-TRIGGER MEMORY at an address location which is determined by the PRE-TRIGGER counter.
The combination PRE-TRIGGER COUNTER / PRE-TRIGGER MEMORY / LATCH functions like a digital shift register with a variable length.
The length is directly depending on the front panel pre-trigger setting given by the operator.
Depending on this setting which varies between 0 - 1/4 - 1/2 - 3/4 and 1 the length of the shift register will respectively be 0 - 1024 - 2048 - 3072 or 4096 locations.
This variable length is reached by varying the count length of the PRE-TRIGGER counter which generates the input addresses for the PRE-TRIGGER MEMORY. (APC0 ... APC11).

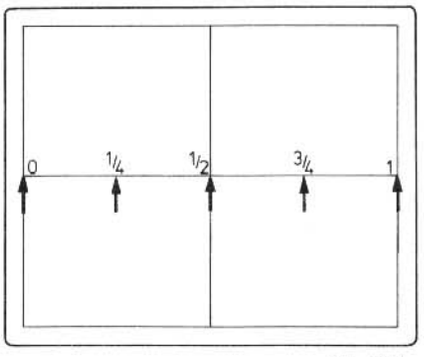


FIG. 3.13. Trigger positions on C.R.T. display.

The PRE-TRIGGER counter is presetted to the required value by the microprocessor system with address C000H and the signals $\overline{\text{IOWRC}}$ and PRTR0 - PRTR1 and PRTR2.

Shift register length:	Preset value:	PRTR2	PRTR1	PRTR0
0	FFEH	1	1	0
1024	C00H	1	1	0
2048	800H	1	0	0
3072	400H	0	1	0
4096	000H	0	0	0

The PRE-TRIGGER COUNTER can be loaded in two different ways with command $\overline{\text{LOADPC}}$ (load pre-trigger counter).

1) The counter can be loaded with the value of PRTR0 - 1 and 2 at the moment that the counter has reached the state 4095. Loading is carried out via the carry signal on point 15 of the last counter D2039.
2) During $\overline{\text{IOWRC}}$, the load signal $\overline{\text{LOADPC}}$ will be generated. $\overline{\text{IOWRC}}$ switches D-flip flop D2043 output Pt 5 to "0" during the generation of the signals PRTR0 - 1 and 2.
   Signal $\overline{\text{HOLDOFF}}$ is also "0" then.

   After $\overline{\text{IOWRC}}$ the $\overline{\text{LOADPC}}$ signal can not longer be generated in this way. The first $\overline{\text{WEPTR}}$ pulse on the clock input of D-type flip flop D2043 Pt 3 switches this flip flop to logic "1" so that signal $\overline{\text{LOADPC}}$ only can be generated via D2004.

Incoming triggers are suppressed until the PRE-TRIGGER COUNTER reaches for the first time the state 4095 after loading on $\overline{\text{IOWRC}}$ by the microprocessor. This is done via the signal $\overline{\text{HOLDOFF}}$ when it is active "low".

Suppression is stopped when the PRE-TRIGGER COUNTER has reached for the first time the state 4095 and RW goes to "1". HOLDOFF is switched to "1" thus enabling the trigger flip flops D2077 and D2084 to react on a new incoming trigger.

PRE-TRIGGER-MEMORY as digital shift register with variable length:

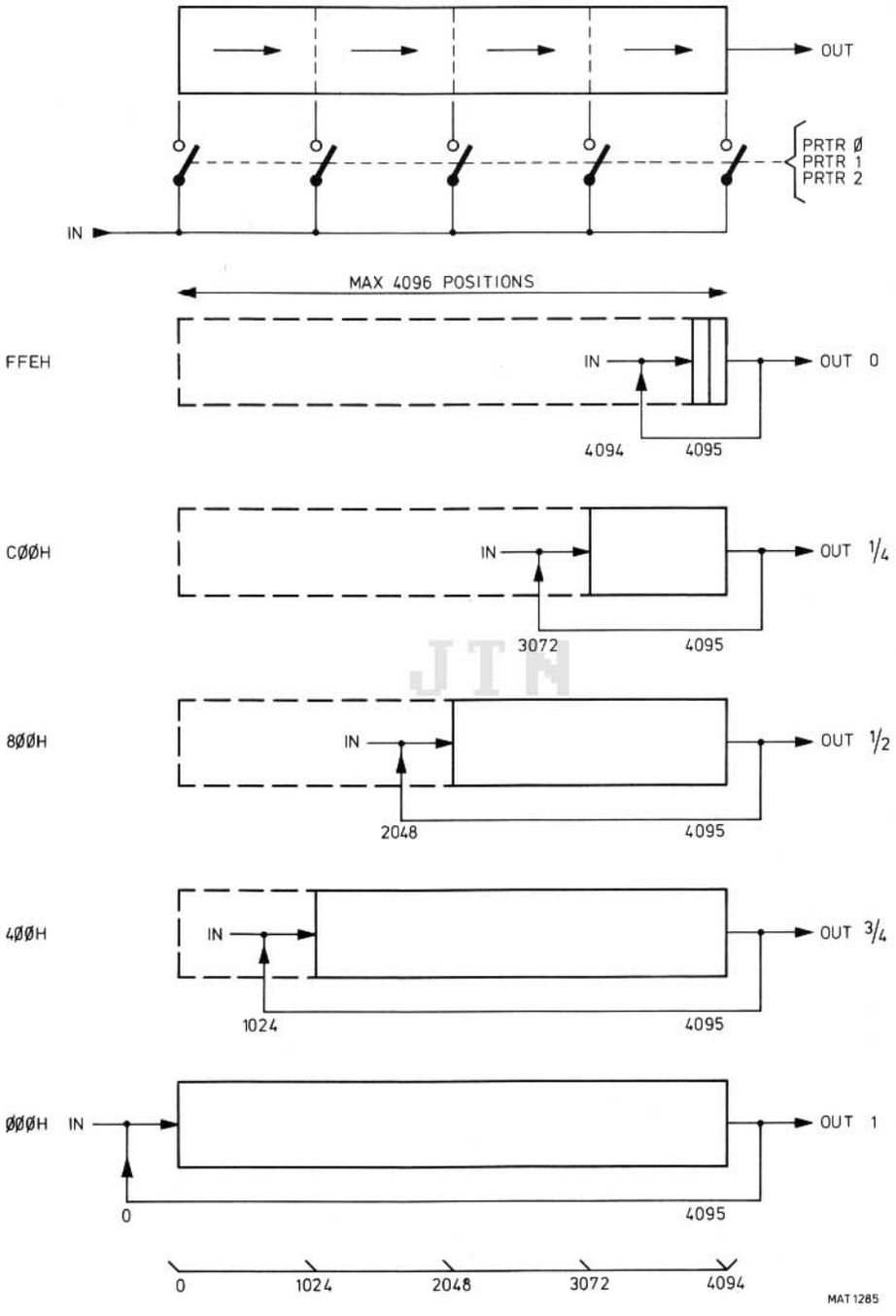


FIG. 3.14. Variable length of the pre-trigger memory/counter.

After storage of a digital number in the PRE-TRIGGER MEMORY with signal WEPTR, the PRE-TRIGGER COUNTER is increased by one on the positive going edge of WEPTR.

This means that now the next PRE-TRIGGER MEMORY location is addressed and that is the location in which the oldest signal value since the last WEPTR is stored. Now the oldest signal sample can be written into LATCH D2109 by means of signal LDTR (Latch delayed trigger).
So the LATCH D2109 can be considered as the output of the PRE-TRIGGER MEMORY shift register system.

The PRE-TRIGGER MEMORY itself consists of two chips which are selected with signal APC11 as chip select signal.

APC11 = "0" --> RAM I (D2103) 000H - 7FFH
APC11 = "1" --> RAM II (D2091) 800H - FFFH

On receipt of an input trigger the shift register output (LATCH output) is coupled to the input of a DISPLAY MEMORY (D2103, D2091) of 4096 x 8 bits.
From this moment the MEMORY WRITE LOGIC derives not only $\overline{\text{WEPTR}}$ pulses from the NDRL signal but also $\overline{\text{WEDSP}}$ pulses (Write enable display) for the DISPLAY MEMORY.
The DISPLAY MEMORY location in which the PRE-TRIGGER MEMORY output information is placed depends on the state of the WRITE COUNTER, of which the outputs are connected to the DISPLAY MEMORY via a multiplexer D2022,D2037 and $\overline{\text{D2058}}$.
The counter starts counting WEDSP pulses at the trigger moment. Counting is done from the 0 - state to the state 4095 after which the trigger logic is resetted. The system can react then on a new trigger, after which the DISPLAY MEMORY can be refreshed again.

In this way digital numbers are shifted continuously through the PRE-TRIGGER MEMORY shift register system with variable length. At the trigger moment this shift register will already contain information from before the trigger moment.
This information (a variable number of samples) is first shifted into the DISPLAY MEMORY and then followed with "after trigger" samples until the DISPLAY MEMORY is filled completely.

EXAMPLE

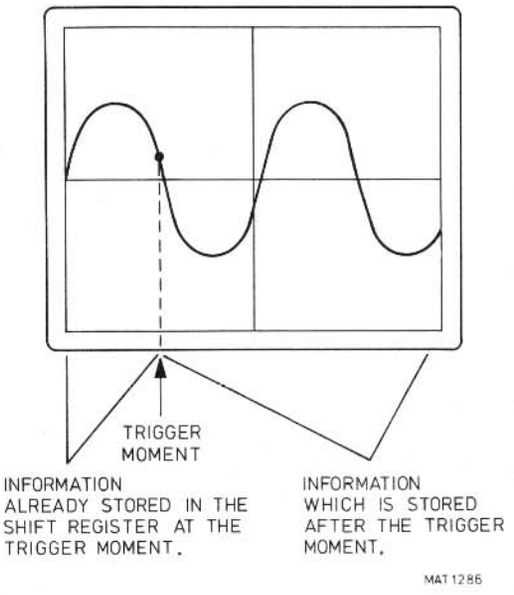


FIG. 3.15. Pre-triggering.

$\overline{\text{WEDSP}}$ pulses are generated in the following way:

1) $\overline{\text{WEDSP}}$ is derived from $\overline{\text{WRUP}}$ in case of microprocessor control (UPCONT = "1"). (For CLEAR or the use of the IEEE option).
2) A $\overline{\text{WEDSP}}$ is generated in case of no microprocessor control (UPCONT = "0") and after a trigger when NDRL and TRIGL are logic "1".
   Furthermore generation of WEDSP pulses depend on selection of NORMAL-mode or COMPARE-mode and SINGLE-channel, DUAL-channel or FOUR-channel mode.

   In NORMAL-mode points 3 - 11 and 12 of NAND D2032 are made "1" by the signals CS - CR and CQ. The counter outputs AWC0 - AWC1 and AWC2" are then not active in this circuit.

   In COMPARE-mode one of the three WRITE COUNTER output bits AWC0....AWC2 can be applied in an inverted or non-inverted way to the inputs of NAND D2032 to suppress the $\overline{\text{WEDSP}}$ pulses, depending on the situations:

   SINGLE channel
   DUAL channel
   FOUR channel
   and ODD or EVEN

   This is done under the control of the "microprocessor-generated" signals CQ, CR, CS and CT.

CQ	CR	CS	CT		
0	0	0	0	Normal-mode	Normal
0	0	0	1	Normal-mode	
0	0	1	0	Single channel - compare - odd	Compare
0	0	1	1	Single channel - compare - even	
0	1	0	0	Dual channel - compare - odd	
0	1	0	1	Dual channel - compare - even	
0	1	1	0	---	
0	1	1	1	---	
1	0	0	0	Four channel - compare - odd	
1	0	0	1	Four channel - compare - even	
1	0	1	0	---	
1	0	1	1	---	
1	1	0	0	---	
1	1	0	1	---	
1	1	1	0	---	
1	1	1	1	---	

Storage of samples in display memory.

Normal-mode

A A A A A A A A	Single channel	(Channel A)
B B B B B B B B	Single channel	(Channel B)
A B A B A B A B	Dual channel	(Channel A and B)
A B C D A B C D	Four channel	(Channel A, B, C and D)

Compare-mode

A A A A A A A A	Single channel	(Channel A)
B B B B B B B B	Single channel	(Channel B)
A B A B A B A B	Dual channel	(Channel A and B)
A B C D A B C D	Auxiliary channel	(Channel A, B, C and D)

In ODD the underlined samples are fixed and in EVEN the other samples are fixed.

	ODD CT = 0			EVEN CT = 1		
Write counter state	AWC2*	AWC1*	AWC0*	AWC2*	AWC1*	AWC0*
0	0	0	0	1	1	1
1	0	0	1	1	1	0
2	0	1	0	1	0	1
3	0	1	1	1	0	0
4	1	0	0	0	1	1
5	1	0	1	0	1	0
6	1	1	0	0	0	1
7	1	1	1	0	0	0

	ODD CT = 0			EVEN CT = 1		
Write counter state	AWC2**	AWC1**	AWC0**	AWC2**	AWC1**	AWC0**
	CQ=1 Four	CR=0	CS=0	CQ=1 Four	CR=0	CS=0
0	1	1	1	0	1	1
1	1	1	1	0	1	1
2	1	1	1	0	1	1
3	1	1	1	0	1	1
4	0	1	1	1	1	1
5	0	1	1	1	1	1
6	0	1	1	1	1	1
7	0	1	1	1	1	1

	ODD CT = 0			EVEN CT = 1		
Write counter state	AWC2**	AWC1**	AWC0**	AWC2**	AWC1**	AWC0**
	CQ=0	CR=1 Dual	CS=0	CQ=0	CR=1 Dual	CS=0
0	1	1	1	1	0	1
1	1	1	1	1	0	1
2	1	0	1	1	1	1
3	1	0	1	1	1	1
4	1	1	1	1	0	1
5	1	1	1	1	0	1
6	1	0	1	1	1	1
7	1	0	1	1	1	1

	ODD CT = 0			EVEN CT = 1		
Write counter state	AWC2**	AWC1**	AWC0**	AWC2**	AWC1**	AWC0**
	CQ=0	CR=0	CS=1 Single	CQ=0	CR=0	CS=1 Single
0	1	1	1	1	1	0
1	1	1	0	1	1	1
2	1	1	1	1	1	0
3	1	1	0	1	1	1
4	1	1	1	1	1	0
5	1	1	0	1	1	1
6	1	1	1	1	1	0
7	1	1	0	1	1	1

[0 --> $\overline{\text{WEDSP}}$ suppressed.]
[1 --> $\overline{\text{WEDSP}}$ generated.]

CLWC (clockpulse for WRITE COUNTER):

The WRITE COUNTER is increased by one with signal CLWC.
CLWC is generated if all signals NDRL and TRIGL and WR are active.

Loading the WRITE COUNTER is done synchronously with a clockpulse CLWC derived from LOADS.WR.

NDRL latch:

Each TRACK signal is latched in a D-flip flop D2077 of which the output point 9 goes to "1". This circuit detects whether an NDR is present or not.
The information is clocked in a second D-flip flop with clocksignal CONTC2 to synchronize the conversion ritm to the read/write ritm of the pre trigger memory. This results in NDRL (NDRL latch) going to logic "1". The first D-flip flop is resetted on leading edge of the NDRL signal and the second D-flip flop is resetted with signal CONTC3.

TRIGGER latch:

As long as triggerpulses TRIG are generated, the output TRGRD of retriggerable one shot D2119 will be logic "1". This output will be switched to logic "0" if for a period of about 100 ms no trigger pulses appear.
Signal TRGRD is read by the microprocessor system.

Signal TRAUT (trigger automat) used as clockpulse for D-flip flop D2077 can be generated in two ways:

1) Instrument is triggered and not set in AUTO-mode:

   Signal TRGRD has then a logic "1" level and RW used as artificial trigger is then enabled by signal HTRG from the microprocessor to generate TRAUT.
   The TRIG pulses can set now the D-flip flop D2077 (Pt 5 --> logic "1").

2) Instrument is not triggered and set in AUTO-mode:

   When no trigger signals TRIG are generated, signal TRGRD will be logic "0". With AUTO-mode selected, the signal HTRG will be switched to logic "1" by the microprocessor.
   HTRG together with RW results then in signal TRAUT which can set the D-flip flop D2077 to carry out the AUTO function.

The flip flop output information can be clocked into a second D-flip flop D2084 on the positive going edge of the NDRL signal resulting in signal TRIGL going to logic "1". In this way the incoming trigger is synchronized to the memory read/write cycle.

Both flip flops can be reset in two ways:

a) As long as the signal $\overline{\text{HOLDOFF}}$ is low. So from the moment of loading the PRE-TRIGGER COUNTER untill for the first time the state 4095 is reached.
b) As long as signal EINP (End input) is active (logic "1").

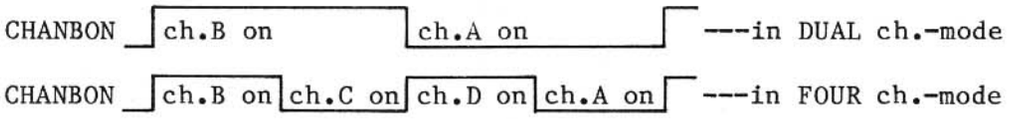
   During EINP (end input) active (Pt 9 of D2006 is "0") which is read by the microprocessor, the microprocessor is able to clock the value of DUP3 (enable trigger) in the D-flip flop using $\overline{\text{IOWR8}}$ as clocksignal to start a new input cycle.
   Via OR-circuit D2033 (4-5-6) the flip flop clock input will be blocked directly during an input cycle.
   The flip flop enables the trigger latch to react on a new incoming trigger and is really active at the end of the holdoff period.

   EINP is activated again at the end of a DISPLAY - MEMORY input cycle with signal LOADS. EINP is then read again by the microprocessor which then can start a new input cycle.

Between the D-type flip flop D2077 and the TRIGL D-type flip flop D2084 a circuit is inserted by which is determined that channel A samples always will be stored on even addresses in the DISPLAY MEMORY (starting with address 0000H).

```
          0000          0002          0004
So          A     B       A     B       A     B  --- in DUAL ch.-mode

          0000                        0004
and         A     B       C     D       A        --- in FOUR ch.-mode
```



With no MIN/MAX selected (MIN/MAX = "0") signal CHANBON will together with the logic "1" level of signal TRRES determine the moment on which signal TRIGL is switched to logic "1" after the appearance of a trigger signal. Flip flop TRIGL is switched on the positive going edge of NDRL.

With MIN/MAX selected (MIN/MAX = logic"1") signal CHANBON will be overruled. Signal TRRES only, determines now the moment of switching of signal TRIGL. Flip flop TRIGL is switched on the positive going edge of NDRL.

After the setting of the TRIGL flip flop, this flip flop is hold in this position with signal TRIGL via NAND D2067 (11-12-13).

On receipt of an input trigger the PRE-TRIGGER MEMORY output is coupled via LATCH D2109 to the input of a digital DISPLAY MEMORY which consists of 4096 locations of 8 bits.

The LATCH is disabled under microprocessor control when UPCONT = "1". The LATCH will be enabled if no microprocessor control, so when UPCONT = "0", and if $\overline{\text{WEPTR}}$ is active "0".
If enabled, the output of the PRE-TRIGGER MEMORY shift register system can be latched into this LATCH. This is done under the control of signal LDTR (Latch delayed trigger).
In sequential sampling mode LDTR is steady "1" so that the LATCH is transparant. There is no pretrigger possibility in sequential sampling mode.

There are three ways in which the DISPLAY MEMORY can be addressed:

1. Generation of addresses AWC0 ... AWC11 by a WRITE COUNTER for writing new signal information into the MEMORY.
2. Generation of addresses ADC0 ... ADC11 by a DISPLAY COUNTER for reading the contents of the DISPLAY MEMORY to display it on the C.R.T. screen.
3. Generation of addresses AUPB0 ... AUPB11 by the microprocessor system via tri-state buffer (D2122-D2127) for writing and reading when using the IEEE - option and for the CLEAR function.

Selection between addresses generated by the microprocessor or by one of the counters is done by signal UPCONT which is applied to the enable inputs of the MULTIPLEXER (D2022, D2037, D2058).

UPCONT = "0" means: WRITE COUNTER or DISPLAY COUNTER selected.
UPCONT = "1" means: Microprocessor generated addresses can be selected.

If no microprocessor control, selection between the WRITE COUNTER or the DISPLAY COUNTER is done by the MULTIPLEXER circuit consisting of D2022, D2037 and D2058 which is controlled by the signal MUX.

MUX = "1" means: DISPLAY COUNTER selected.
MUX = "0" means: WRITE COUNTER selected.

WRITE COUNTER (D2023, D2038 and D2059)

During the process of writing new signal information into the DISPLAY MEMORY the memory location in which information has to be stored is determined by the state of the WRITE COUNTER. Depending on the selected TIME/DIV switch setting the system functions in one of the three modes DIRECT, SAMPLING I or SAMPLING II.

DIRECT and SAMPLING I - mode

In DIRECT-mode as well as SAMPLING I-mode (0,5 s/div. ... 0,2 ms/div. respectively 5 µs/div. ... 0,1 µs/div.) the counter state is increased step by step with signal CLWC.
This process starts with counter state 0000.

Signal SEQWC (sequence write counter) is logic "0" in these modes and the counter i.c.'s are switched as follows:

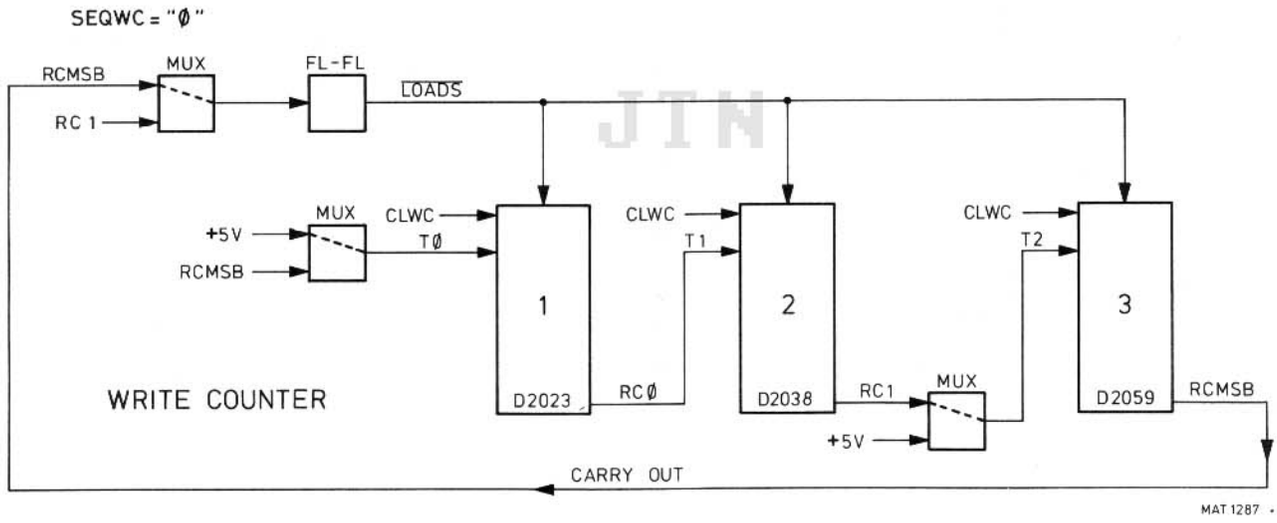


FIG. 3.16. WRITE COUNTER in SAMPLING I mode.

The counter counts to state 4095 and is then presetted to the zero- state. In SAMPLING I - mode DACSTAIR makes one step per sawtooth signal. 4096 sweeps are needed to build a complete picture on the C.R.T. screen.

SAMPLING II-mode.

In SAMPLING II - mode (100 /us/div. .... 10 /us/div.) the signal SEQWC is switched to logic "1" by the microprocessor. The WRITE COUNTER i.c.'s are now connected together in an other sequence by the microprocessor. Counting is then done in steps of 256.

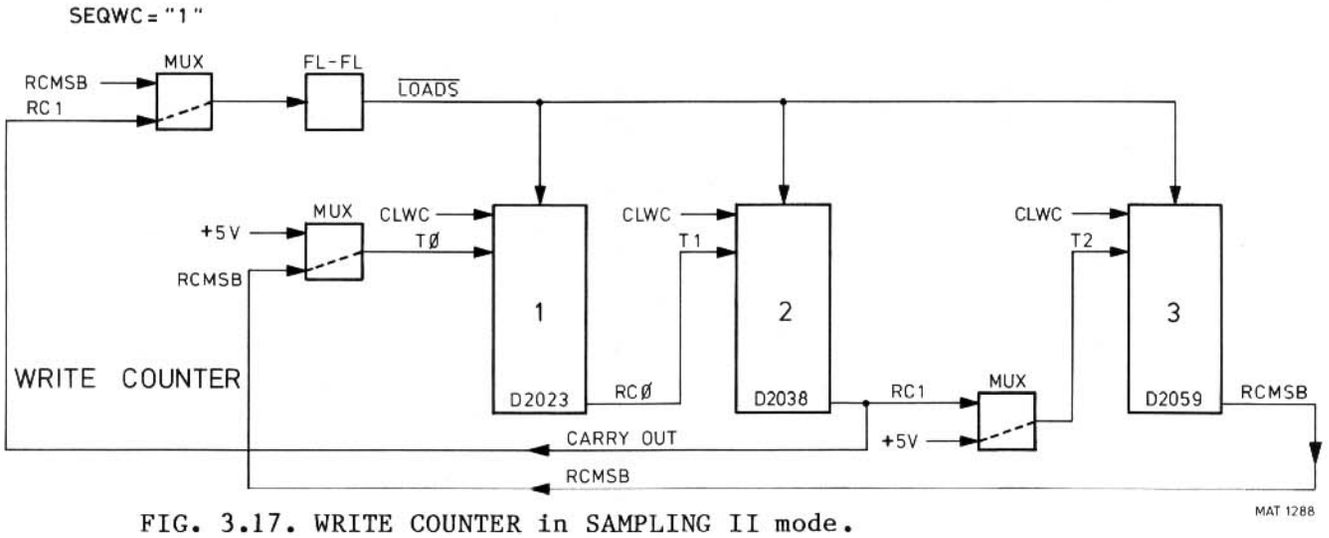


FIG. 3.17. WRITE COUNTER in SAMPLING II mode.

In SAMPLING II - mode DACSTAIR makes sixteen steps per sawtooth signal. 256 sweeps are needed to build a complete picture on the C.R.T. screen.

The countsequence of the counter is now:

```
   0,   256,   512,   768, ..... 3840  (at 1st sweep)
   1,   257,   513,   769, ..... 3841  (at 2nd sweep)
   2,   258,   514,   770, ..... 3842  (at 3rd sweep)
   :     :     :     :            :
   :     :     :     :            :
   :     :     :     :            :
 255,   511,   767,  1023, ..... 4095  (at sweep 256)
```

In all modes DIRECT, SAMPLING I and SAMPLING II the counter will be presetted to the 0 - state when the counter state 4095 is reached. For this a signal LOADS is derived from the carry output signals RC1 or RCMSB via D-flip flop D2006.

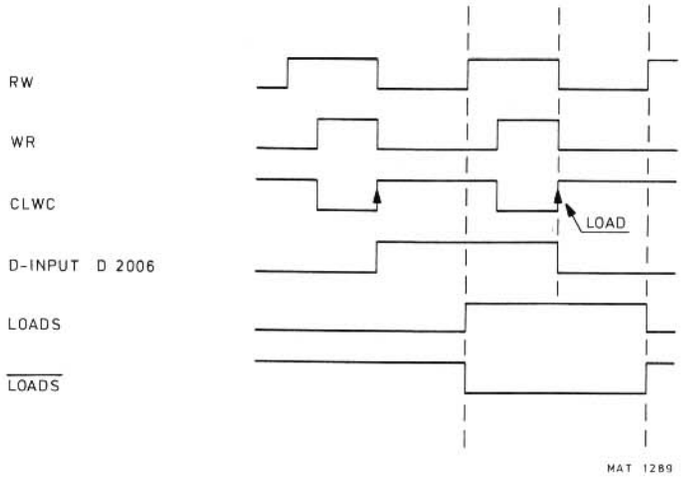


FIG. 3.18. Loading of the WRITE COUNTER.

DISPLAY COUNTER (D2021, D2036 and D2057)

The location in the display memory of an input signal sample which has to be displayed on the C.R.T. screen at a certain moment is determined by the state of the DISPLAY COUNTER. This counter is connected to the address inputs of the DISPLAY MEMORY via MULTIPLEXER D2022, D2037 and D2058.

A display cycle is started by the microprocessor system via signal DUP2 (enable display counter). The value "1" of this signal is clocked into the D- flip flop D2087 using signal IOWR8 as a clocksignal. After this the flip flops clock input is disabled by its output signal via OR-circuit D2033 (8-9-10).
The second D-type flip flop D2087 is switched now on the first negative going edge of the signal TRSHXY.
After the presetting of the counter with the value of STAD0, 1, 2, 9, 10, and 11 the counter starts counting CNTUP (Count up) pulses until the state 4095 is reached.

Note that CNTUP pulses can be generated in different ways depending on the selected modes SINGLE channel, DUAL channel or FOUR channel.

The output carry signal of the counter (state 4095) is applied via an inverter D2062 (anti glitch circuit) and AND-circuit D2018 to the RESET input of D-flip flop D2087. This flip flop is resetted then and resets in turn the next D-flip flop D2087. The signal DT (pulse for display timing) which was logic "1" during display is switched to zero now, indicating that the end of the display cycle is reached. At the same moment ZDTCRT will be resetted (switched to "0"). As long as ZDTCRT is logic "0" the C.R.T. beam will be blanked. The microprocessor is also informed about the end of the display cycle by reading signal DT.

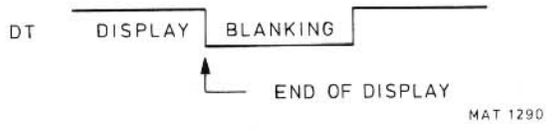


FIG. 3.19. Display timing.

With signal DT logic "0" the counter can now be presetted again.

DISPLAY COUNTER in MEMORY-QUARTERS - mode.

In MEMORY - QUARTERS - mode the DISPLAY COUNTER can be presetted again at the end of the display of the selected QUARTER (D2007).

Presetting is done by the microprocessor system via the signals STAD0-1-2 and STAD9-10-11 (Start address display counter) according to the following table.

QUARTERS	11 DATS	10 DATS	9 DATS	8 DATS	7 DATS	6 DATS	5 DATS	4 DATS	3 DATS	2 DATS	1 DATS	0 DATS	START
	0	0	0	0	0	0	0	0	0	0	0	0	000H <- Preset value
	0	0	0	1	1	1	1	1	1	1	1	1	1FFH
1													
	0	0	1	0	0	0	0	0	0	0	0	0	200H <- Preset value
	0	0	1	1	1	1	1	1	1	1	1	1	3FFH
2			↓										<- End of Quarter 1
	0	1	0	0	0	0	0	0	0	0	0	0	400H <- Preset value
	0	1	0	1	1	1	1	1	1	1	1	1	5FFH
3													<- End of Quarter 2
	0	1	1	0	0	0	0	0	0	0	0	0	600H <- Preset value
	0	1	1	1	1	1	1	1	1	1	1	1	7FFH
4			↓										<- End of Quarter 3
	1	0	0	0	0	0	0	0	0	0	0	0	800H <- Preset value
	1	0	0	1	1	1	1	1	1	1	1	1	9FFH
5													<- End of Quarter 4
	1	0	1	0	0	0	0	0	0	0	0	0	A00H <- Preset value
	1	0	1	1	1	1	1	1	1	1	1	1	BFFH
6			↓										<- End of Quarter 5
	1	1	0	0	0	0	0	0	0	0	0	0	C00H <- Preset value
	1	1	0	1	1	1	1	1	1	1	1	1	DFFH
7													<- End of Quarter 6
	1	1	1	0	0	0	0	0	0	0	0	0	E00H
	1	1	1	1	1	1	1	1	1	1	1	1	FFFH
			↓										<- End of Quarter 7

The table shows that the display counter bits STAD3 ... STAD8 are always "0" when presetting the display counter.

The ends of each of the seven quarters are decoded by exclusive - OR circuit D2099 in the following way:

STAD9	ADC9	TI9
0	0	0
0	1	1
1	0	1
1	1	0

Such an end is reached when signal TI9 is going from logic "1" to logic "0", so:

a) When startaddress bit STAD9 is set to logic "0" and DISPLAY COUNTER output ADC9 is going from logic "1" to logic "0".
or b) When startaddress bit STAD9 is set to logic "1" and DISPLAY COUNTER output ADC9 is going from logic "0" to logic "1".

In QUARTER-mode ($\overline{QDR}$ = "0") the D-flip flop D2007 functions as inverter of signal TI9. At the end of the selected quarter a second D-flipflop D2007 is switched by TI9 and a preset of the DISPLAY COUNTER is given then.

At the end of a display cycle the Z-control is switched such that the display is blanked via signal DT which is going to "0" then.

MULTIPLEXER

The multiplexer consisting of D2022, D2037 and D2058 is switched in tri-state under microprocessor control (UPCONT = "1").
If no microprocessor control (UPCONT = "0"), the multiplexer will be enabled and will select the WRITE COUNTER outputs AWC0 ... AWC11 or the DISPLAY COUNTER outputs ADC0 ... ADC11 depending on the level of signal MUX.

MUX = 1 -> DISPLAY COUNTER selected.
MUX = 0 -> WRITE COUNTER selected.

AVSB and Quarter LOGIC

X=t - mode (AVSB = "0")

Horizontal deflection

The DISPLAY MEMORY address information ADC0 ... ADC11 from the DISPLAY COUNTER is clocked on signal LXDA into multiplexer D2019 and latches D2034 and D2056.
Furthermore latch D2069 is switched in tri-state.

a) No DISPLAY QUART selected.
$\overline{QDR}$ = "1"
Multiplexer D2019 is switched by control signal QDR in such a way that signals ADC0 - ADC1 - ADC2 and ADC3 are placed on the XDACI bus. Latch D2056 is enabled and latch D2034 is switched in tri-state which results in placing the signals ADC4 ... ADC11 on the XDACI bus.
Signals ADC0 ... ADC11 are now applied to the horizontal "DIGITAL TO ANALOG" converter XDAC as XDACI0 ... XDACI11.
This will result in a signal XDAC for horizontal deflection.

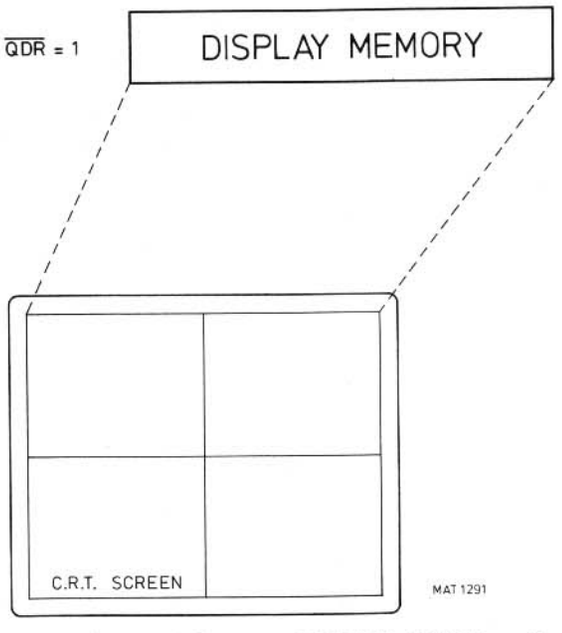


FIG. 3.20. Display without DISPLAY QUART selection.

b) DISPLAY QUART selected.
$\overline{QDR}$ = "0"
In DISPLAY QUART - mode only a quarter of the DISPLAY MEMORY contents has to be displayed.
The address input information for the XDAC must be multiplied now by a factor of 4 to display this quarter over the whole 10 divisions screen width.

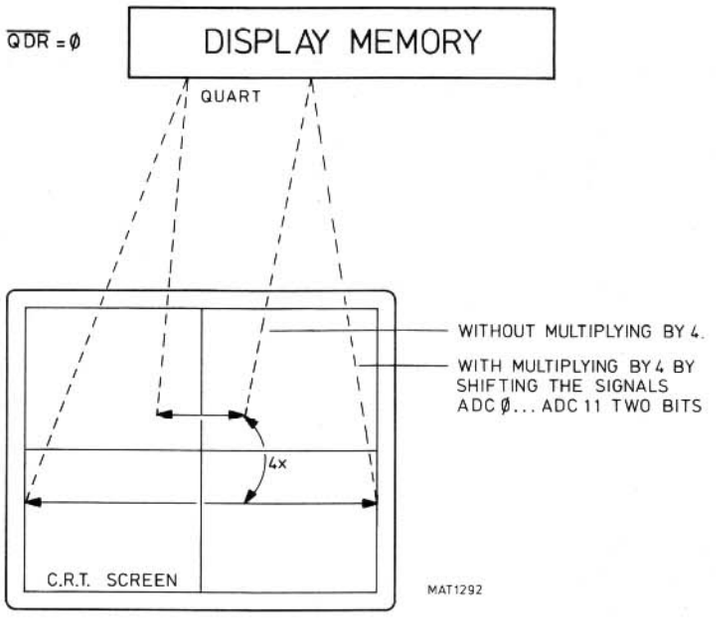


FIG. 3.21. Display with DISPLAY QUART selection.

This is realized if $\overline{QDR}$ = "0" by shifting all the bits ADC0 ... ADC11 two bits to the left with the aid of multiplexer D2019 and latches D2034 and D2056.
Multiplexer D2019 is switched by control signal $\overline{QDR}$ in such a way that signals "0", "0", ADC0 and ADC1 are placed on the XDACI bus.
Latch D2034 is enabled and latch D2056 is switched in tri-state which results in placing the signals ADC2 ... ADC9 on the XDACI bus.
Signals ADC0 ... ADC9 and two times "0" for the two l.s.b.'s are now applied to the horizontal "DIGITAL TO ANALOG" converter XDAC as XDACI0 ... XDACI11.
In this case bit 9 has to be inverted to prevent the system from starting with the display of the signal in the centre of the screen.

The offset of the operational amplifier D2070 can be adjusted with potentiometer R2052.

Vertical deflection

In X=t - mode the same signal value is stored in latches D2128 and D2123 with LYDA1 and LYDA2. Both informations are applied to an adder consisting of D2124 and D2129 and added to each other.
The output of the adder (shifted one bit to the left) is applied to the vertical digital to analog converter YDAC.
With this shifting of one bit of the adder output this output value is divided by a factor two again.
In this situation the lowest adder output bit will be steady "0".

X=A / Y=B - mode (AVSB = "1")

Horizontal deflection

The signal path DISPLAY COUNTER --> XDAC is now blocked.
Signal information from channel A in now placed on the 8 highest input bits (XDACI4 ... XDACI11) for the XDAC input via tri-state

latch D2069.
This latch is enabled by AVSB = "1" and the data is clocked in this latch with signal LXDA.
The four lowest input bits for the XDAC are then connected to "0". This is realized by signal DT by latching the state of the display counter in latch D2019 before the start of an AVSB display cycle.
Latches D2034 and D2056 are switched in tri-state.

Vertical deflection

The channel B data will now be offered to the YDAC.
One signal value is clocked into D2128 with LYDA1, the next signal value is clocked into D2123 with LYDA2 and the next again into D2128 with LYDA1 and so on.
In this way there are always two adjacent channel B signal values available at a time and they are applied to an adder consisting of D2124 and D2129 and added to each other. The output of the adder (shifted one bit to the left) is applied to the vertical digital to analog converter YDAC. With this shifting of one bit of the adder output this output is divided by a factor two again. This results in an average signal value on the YDAC input.

In X=A / Y=B - mode it is possible that the lowest adder output bit will go to logic "1". This information is added to the YDAC output signal via an adjusting network, to correct (round off) the output signal. Round off in AVSB-mode can be realized by adjusting potentiometer R2084.

Communication with IEEE option.

The DISPLAY MEMORY can be addressed via the AUPB0 ... AUPB11 bus system. (UPCONT = "1").
Data communication is done via the D0 ... D7 bus system.

MULTIPLEXER D2008

This multiplexer controls not only the WRITE COUNTER but generates also the signal SALT (Sequential alternating).

SEQWC "1" ---> Signal SALT equals signal $\overline{\text{TRIGL}}$.
(SAMPLING II - mode).
SEQWC "0" ---> Signal SALT is steady logic "1".
(DIRECT + SAMPLING I - mode).

MULTIPLEXER D2088

This multiplexer generates the signals $\overline{\text{DATUPC}}$, $\overline{\text{UPCONT}}$, $\overline{\text{OEDM}}$ and $\overline{\text{LATEN}}$ depending on the level of signal UPCONT which is generated by the microprocessor.

	$\overline{\text{DATUPC}}$	$\overline{\text{UPCONT}}$	$\overline{\text{OEDM}}$	$\overline{\text{LATEN}}$
UPCONT = "1"	$\overline{\text{DAT}}$	"0"	$\overline{\text{RDUP}}$	"1"
UPCONT = "0"	"1"	"1"	$\overline{\text{OE}}$	$\overline{\text{WEPTR}}$

3.7.6. Control logic (unit A11 - diagram 12)

PHASE LOCKED LOOP

A 20 MHz signal is needed for different functions inside the instrument. This 20 MHz signal is derived from the 2,5 MHz clockpulse output from the µ Processor by means of a voltage controlled oscillator (VCO) D2108 that has an output frequency of 40 MHz.
To obtain this stable VCO output, the 40 MHz output signal is divided by a factor of 16 with the aid of flip flop D2098 and counter D2107.
The resulting 2,5 MHz signal (FEEDBACK signal at point 3 of D2108) is then compared with the reference signal of 2,5 MHz of the microprocessor clockfrequency at point 6 of D2108 in a phase detector, which is used to control the VCO frequency.
The circuit can be locked with potentiometer R2044.

CONTROL COUNTER

The control counter which is needed for timing purposes counts 20 MHz pulses. The control counter is presetted to the value 1011 (11) at the moment that the counter state 0100 (4) is reached and the next count pulse appears. The next counting cycle is then started.

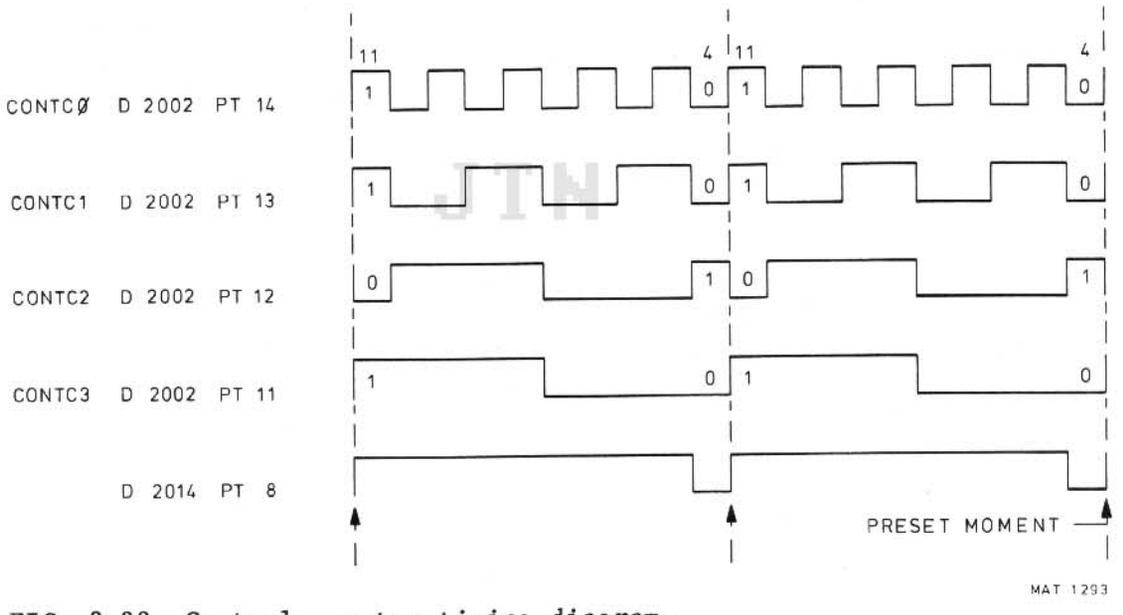


FIG. 3.22. Control counter timing diagram.

A number of timing signals CONTC1 - CONTC2 - CONTC3 - RW - MUX - $\overline{OE}$ and WR is derived from the control counter output signals.
Signal RW determines the time in which new data can be written in the DISPLAY MEMORY or in which data can be read from the DISPLAY MEMORY for display.

RW = "1" means: WRITE (data input)
RW = "0" means: READ (display)

See the timing diagram.

Count pulses (CNTUP) for the DISPLAY COUNTER

Depending on the selected mode 1 - 2 - 4 or 8, CNTUP pulses will be generated per LYDA (Latch Y DAC) cycle.

The CNTUP circuit consisting of D2081 + D2029 is programmed by the /uP via the signals STA (Step A), STB (Step B) and STC (Step C).

Mode	Steps	STA	STB	STC
SINGLE	Step 1	1	1	1
DUAL or SINGLE+COMPARE	Step 2	1	1	0
FOUR or DUAL+COMPARE	Step 4	1	0	0
FOUR and COMPARE	Step 8	0	0	0

See also the timing diagram!

Latch enable signals LXDA, LYDA1 and LYDA2 for the horizontal DAC (XDAC) and for the vertical DAC (YDAC).

Signals LXDA, LYDA1 and LYDA2 have to be generated only during a READ cycle when signal RD = logic "1".
This is done in a different way for the X=t and the X=A/Y=B modes as shown in the timing diagram.

The multiplexer D2073 in the circuit where the latch enable signals are generated is functioning according to the tabel below.

Position of multiplexer D2073.	Control inputs AVSB	Control inputs ADC0*	Output Pt 7	Output Pt 9	
0	0	0	RT1	RT1	X=t
1	0	1	RT1	RT1	
2	1	0	0	RT1	X=A/Y=B
3	1	1	RT1	0	

D2073 is only enabled when signal RT2 is logic "1".

LDTR

LDTR is the latch enable signal for the LATCH D2109.

- This signal is in DIRECT-mode ($\overline{DIR}$ = "0") always derived from signal $\overline{RD}$.
- Signal LDTR is always logic "1" in SAMPLING-mode ($\overline{DIR}$ = "1").

BLANKING CIRCUIT

This circuit provides for a blanking signal ZMOD (Z-modulation) for blanking the trace on the C.R.T. display.
This ZMOD signal functions only in MEMORY ON mode when signal STORE is active (logic "1").

ZMOD = logic "1" means: unblanking
ZMOD = logic "0" means: blanking

The trace on the C.R.T. screen is only present if all the input signals of NAND circuit D2029 (1-2-4-5-6) are logic "1" at the same time.

- pin 5 ZEN : The signal ZEN (Z-enable) is generated by the microprocessor.
- pin 4 ZDTCRT : This signal is active during a display cycle.

Signal TRSHXY.

This signal is generated for deglitching of the DAC.

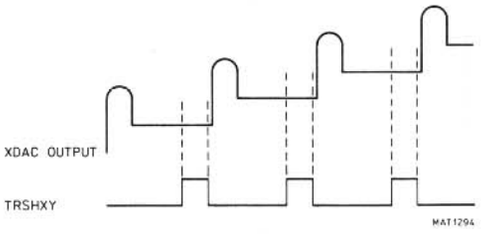


FIG. 3.23. Deglitching of the XDAC.

CHOPPER LOGIC

With this circuit the signals CHOP1 and CHOP2 are generated. These signals are used to control the channel selector in a way which depends on the selected modes SINGLE channel, DUAL channel, FOUR channel, MIN/MAX-mode, DIRECT-mode, and SAMPLING I or SAMPLING II mode.

Signal CHOPB is only active in four channel-mode and is always logic "0" in SINGLE- or DUAL-channel-mode.

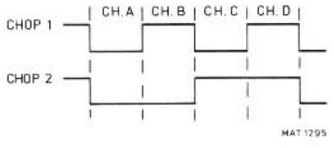


FIG. 3.24. Chopper signals in four-channel mode.

SINGLE channel.

Signal DIGCH is logic "1" in SINGLE channel mode. The analog channel switch is switched in instead of the digital channel switch. This means that the chopper logic has no function in this mode.

DUAL channel and no MIN/MAX-mode in DIRECT- and SAMPLING I-mode:

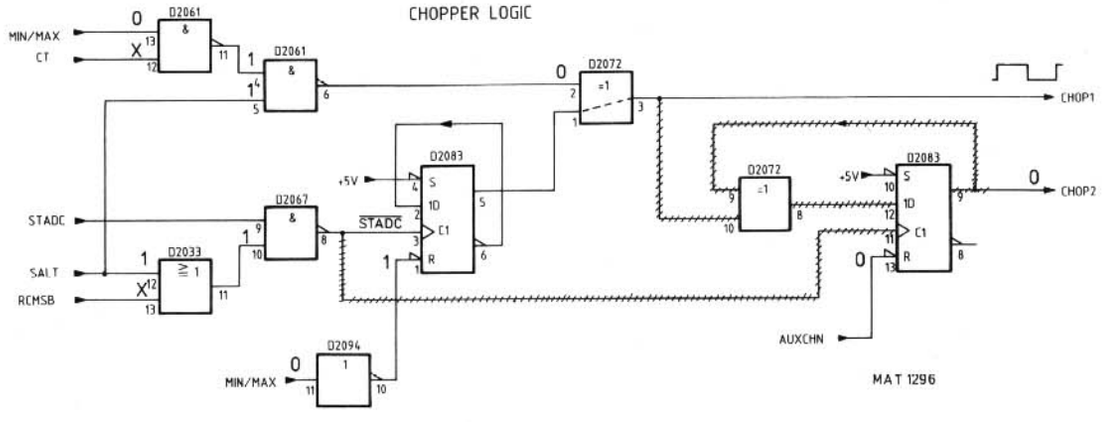


FIG. 3.25. Chopper circuit.

Signal SALT is logic "1" in DIRECT and SAMPLING I - mode.

Signal CHOP2 is steady "0" and signal CHOP1 is switched during each conversion cycle by signal STADC.

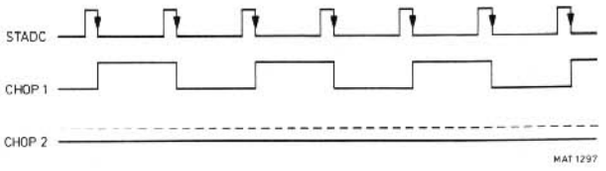


FIG. 3.26. Chopper signals.

DUAL channel and no MIN/MAX-mode in SAMPLING II-mode:

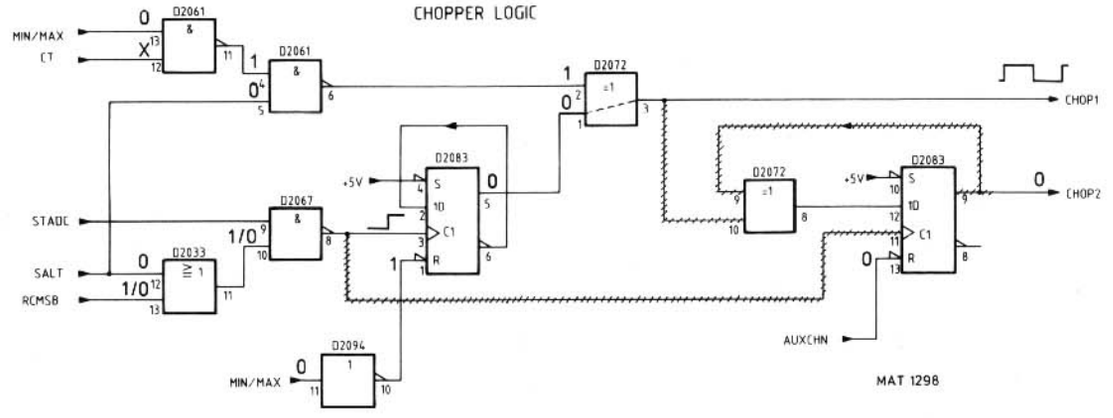


FIG. 3.27. Chopper circuit.

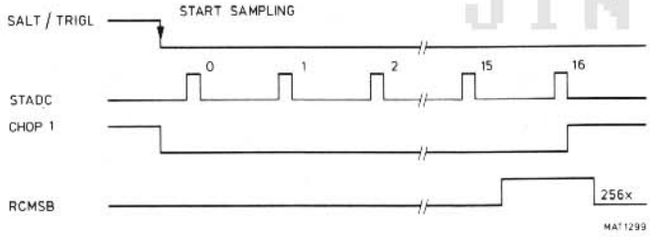


FIG. 3.28. Chopper signals.

The circuit functions in such a way that the SAMPLING II-mode cycle always starts with channel A.
The trigger signal on which the SAMPLING II cycle is started, switches signal SALT to logic "0". On the same moment signal CHOP1 will be switched to "0" in the following way:

If output point 5 of flip flop D2083 is switched to "1", exclusive-or circuit D2072 will be switched as an inverting stage. The low level of signal SALT results then in a signal CHOP1 with logic level "0".

From the moment that signal SALT is switched to logic "0", the CHOP1 signal will be switched by signal RCMSB after each group of 16 conversions.
In this way first 16 samples of channel A are stored, then 16 samples of channel B, then again 16 of channel A and so on.

DUAL channel and MIN/MAX-mode in DIRECT-mode:

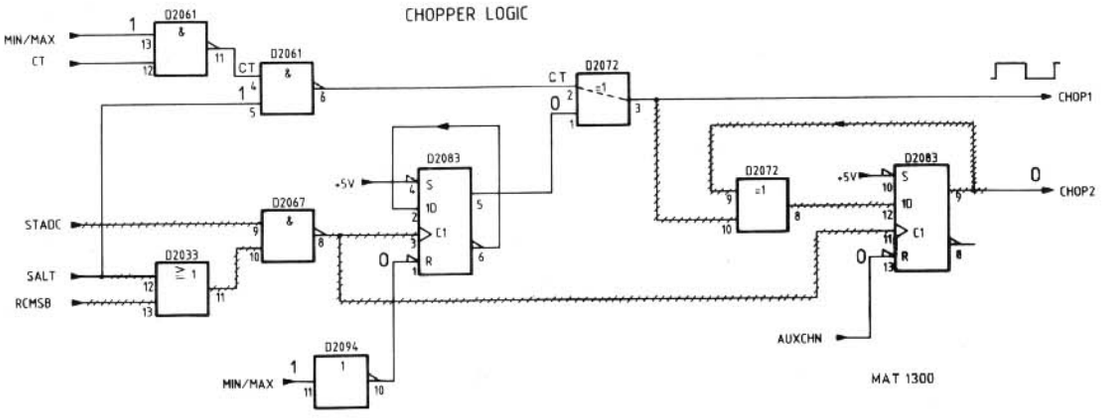


FIG. 3.29. Chopper circuit.

CHOP1 = CT CHOP2 = logic "0"

In DUAL channel MIN/MAX-mode, the system is alternating between channel A and B. This is completely determined by the signal CT from the microprocessor.

FOUR channel and no MIN/MAX-mode in DIRECT- and SAMPLING I-mode:

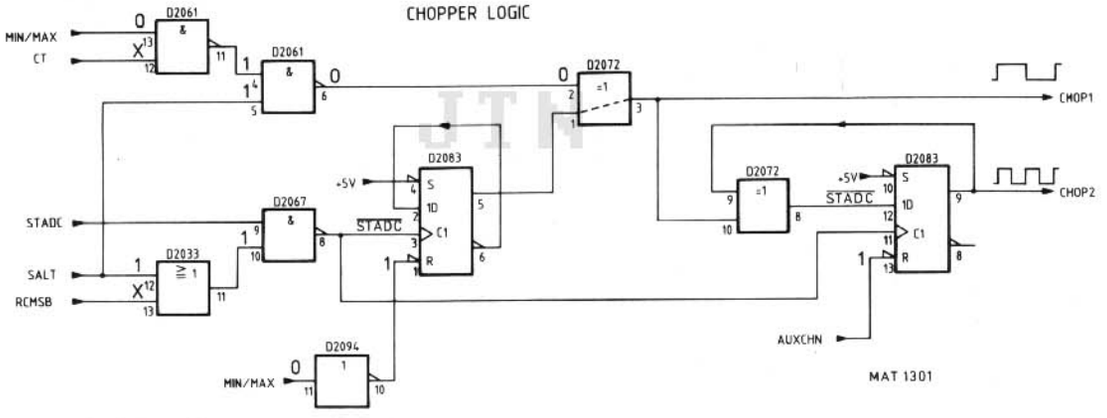


FIG. 3.30. Chopper circuit.

Note: Auxiliary channel can never be combined with the MIN/MAX mode!

The circuit acts as a simple two-bits synchronous counter. This counter has two outputs CHOP1 and CHOP2 and is clocked by the signal STADC. The circuit switches to the next state during each conversion thus selecting the next channel.

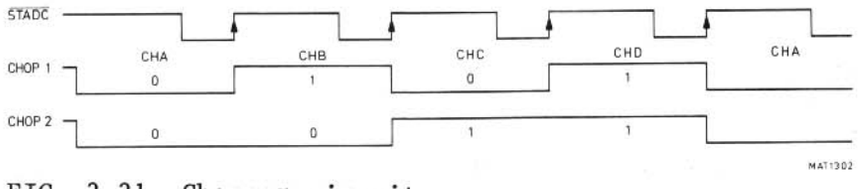


FIG. 3.31. Chopper circuit.

FOUR channel and no MIN/MAX-mode in SAMPLING II-mode:

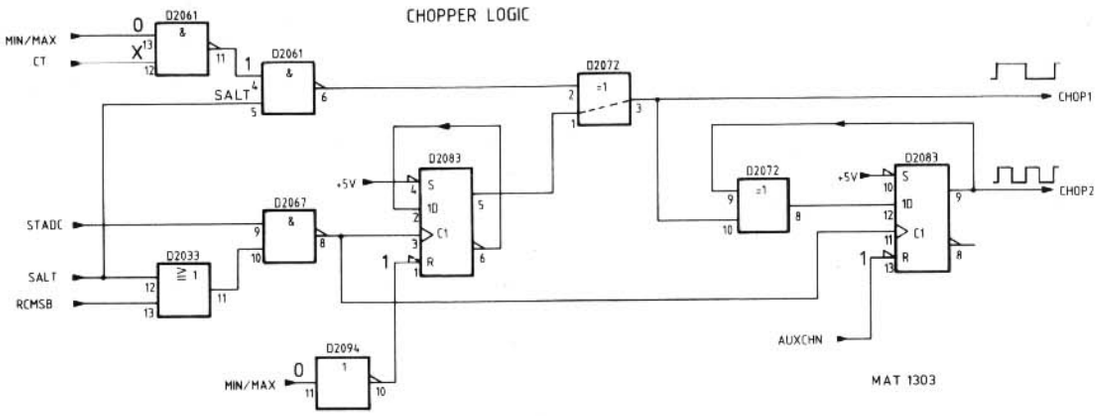


FIG. 3.32. Chopper circuit.

Note: Auxiliary channel can never be combined with the MIN/MAX mode!

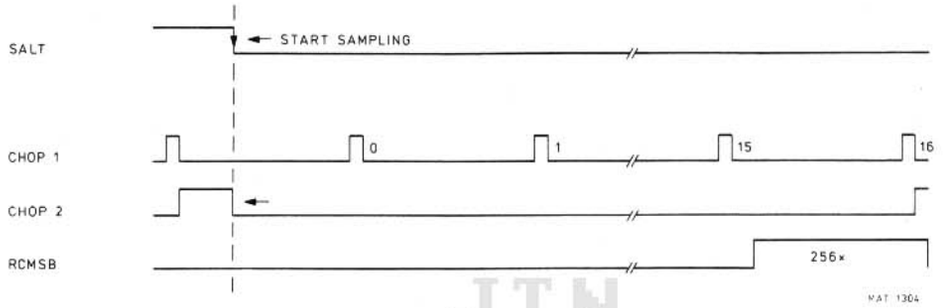


FIG. 3.33. Chopper signals.

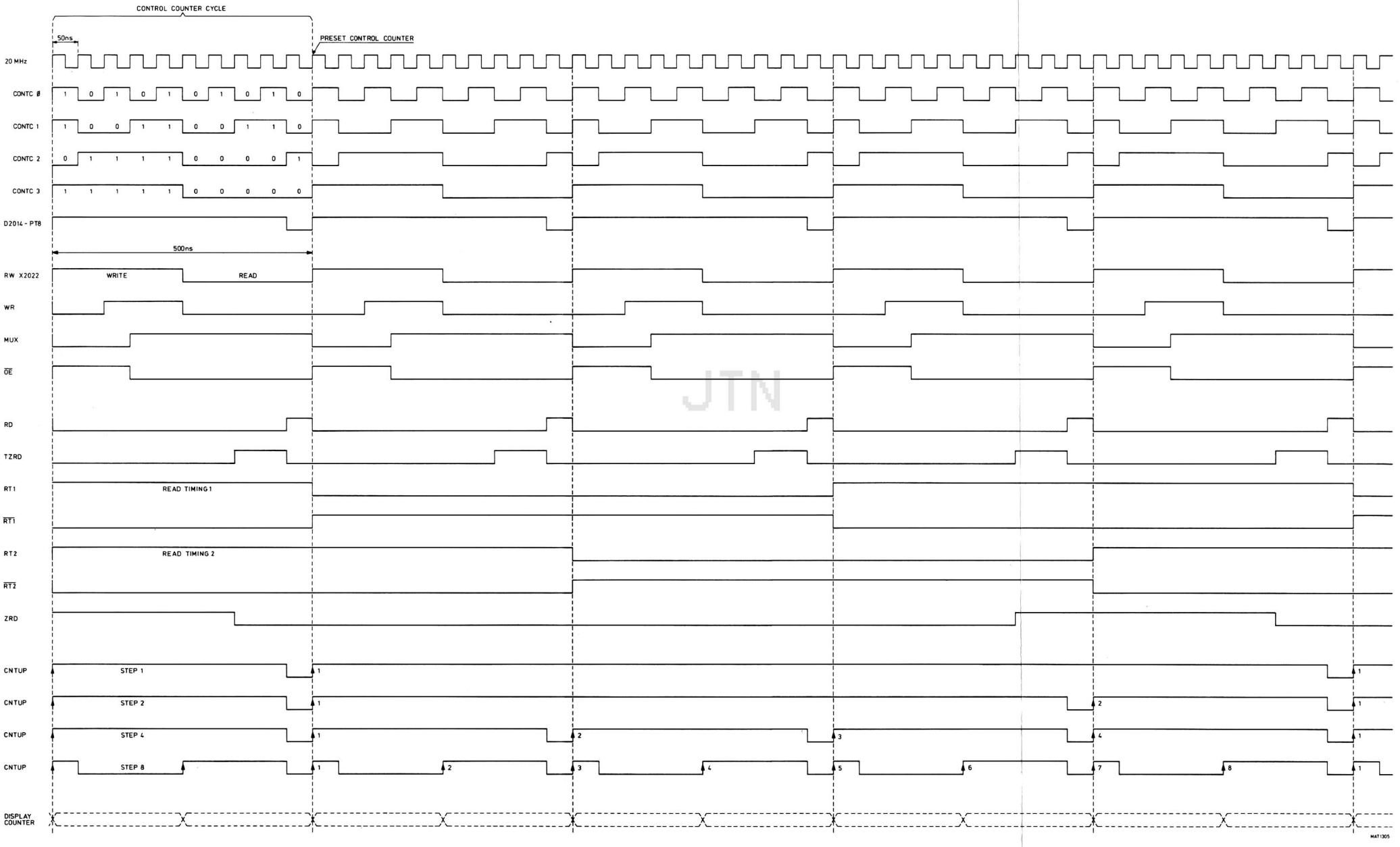


FIG. 3.34. Display timing I.

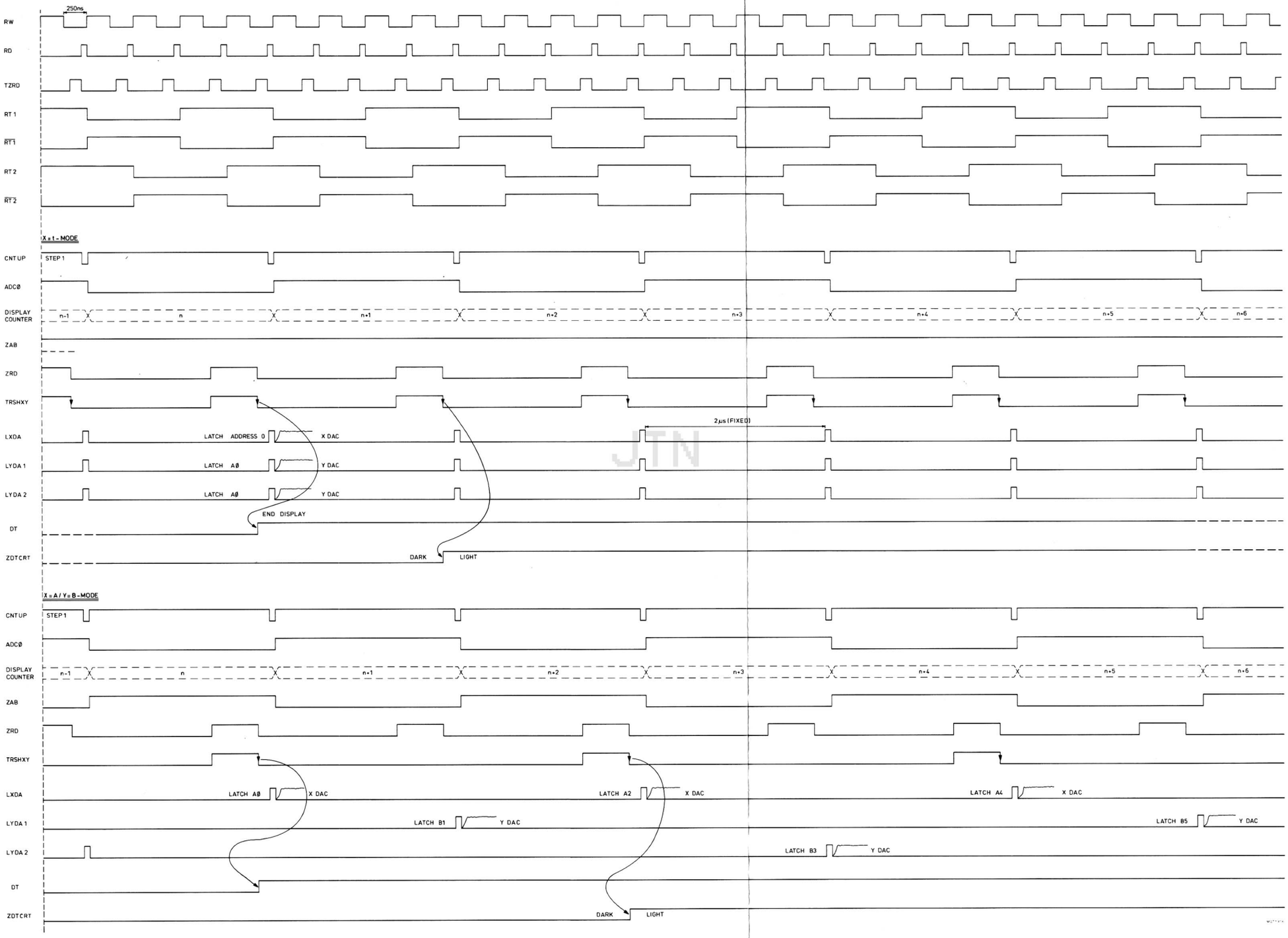
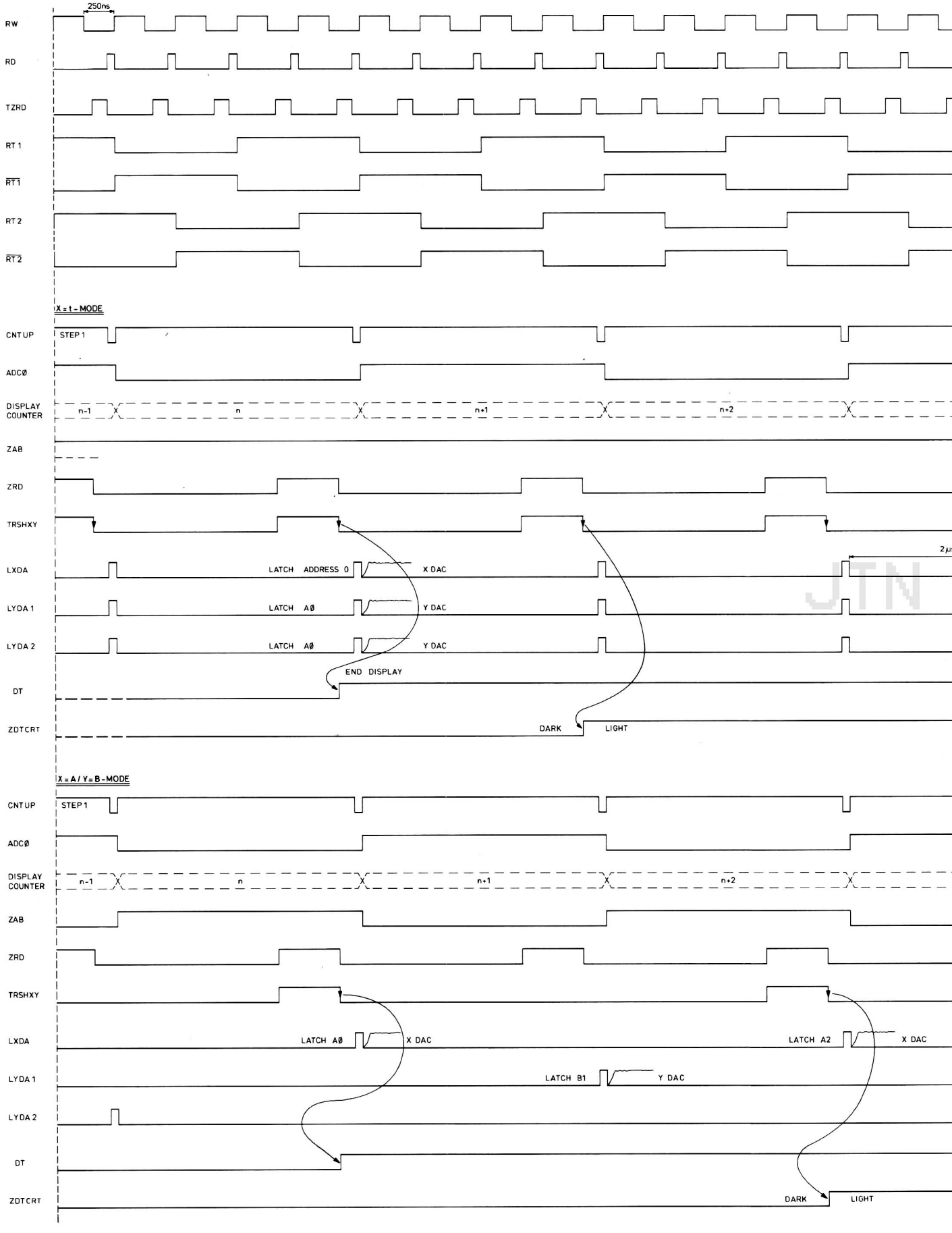


FIG. 3.35. Display timing II.


250ns
RW
RD
TZRD
RT 1
RT 1
RT 2
RT 2
X = t - MODE
CNT UP
STEP 1
ADCØ
DISPLAY COUNTER
n-1
n
n+1
n+2
ZAB
ZRD
TRSHXY
LXDA
LATCH ADDRESS 0
X DAC
LYDA 1
LATCH AØ
Y DAC
LYDA 2
LATCH AØ
Y DAC
END DISPLAY
DT
ZDTCRT
DARK
LIGHT
X = A / Y = B - MODE
CNT UP
STEP 1
ADCØ
DISPLAY COUNTER
n-1
n
n+1
n+2
ZAB
ZRD
TRSHXY
LXDA
LATCH AØ
X DAC
LATCH A2
X DAC
LYDA 1
LATCH B1
Y DAC
LYDA 2
DT
ZDTCRT
DARK
LIGHT

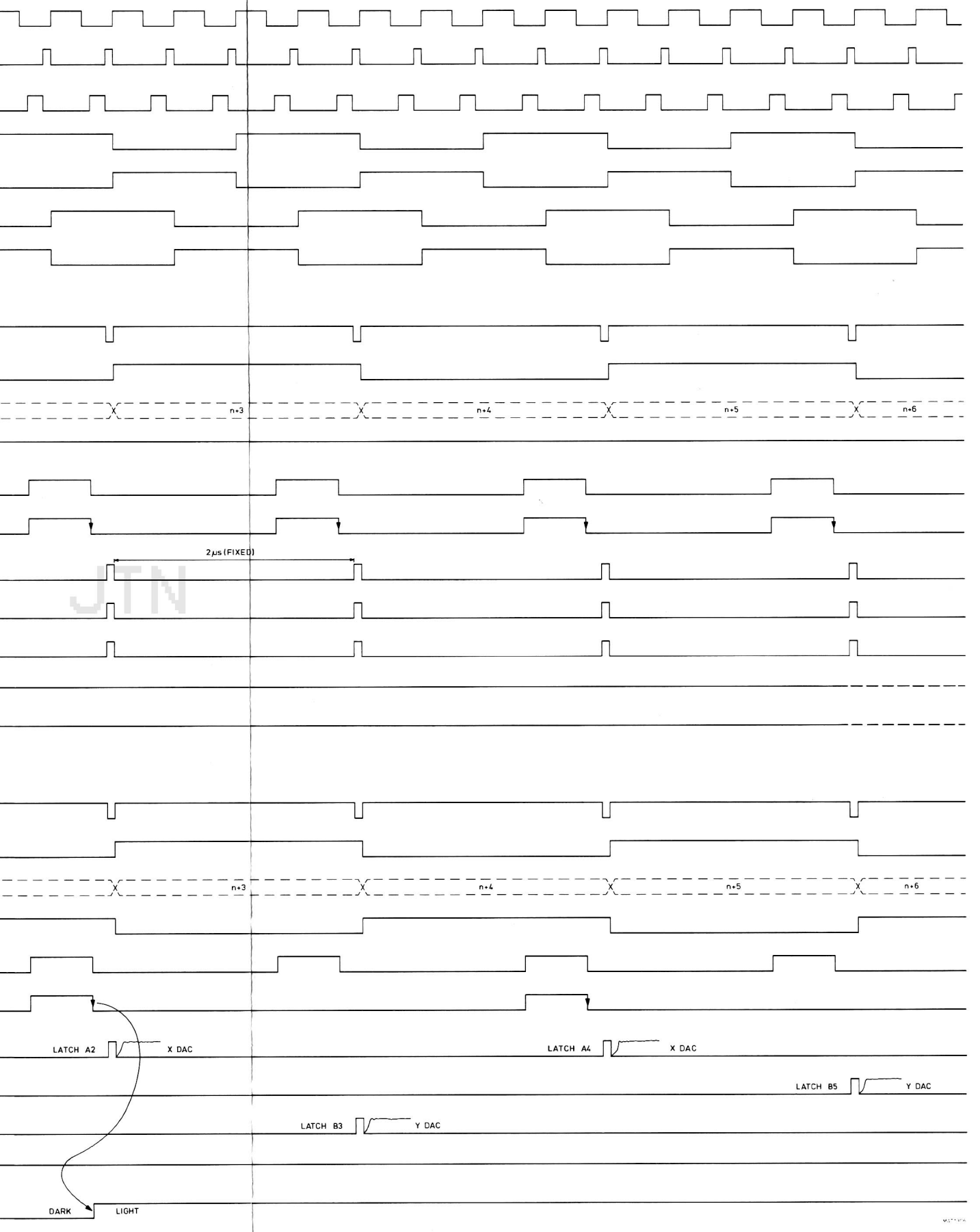


FIG. 3.35. Display timing II.

3.7.7. ADC logic (unit A11 - diagram 13)

Digital time-base generator.

The time-base circuit generates a number of signals with different frequencies which determine the sampling/conversion rate. These frequencies are derived from the 20 MHz from the PHASE LOCKED LOOP circuit by frequency dividing. These signals are synchronized with the 2,5 MHz clockpulse output of the microprocessor.

The digital time-base functions only in the TIME/DIV switch positions 0,2 ms/div. ... 0,5 s/div. in the so-called DIRECT-mode. This digital time-base is not used for the SAMPLING mode (TIME/DIV switch positions 100 µs/div. ... 0,1 µs/div.).

Encoding TIME/DIV settings.

Depending on the setting of the TIME/DIV switch, one of these frequencies is selected and called TIMER OUT.
The relation between the TIME/DIV switch settings and the signal TIMER OUT is such that there are always 400 pulses TIMER OUT per horizontal division. (Not in DISPLAY QUART mode and x10).

The digital time-base consists of a multiplexer D2001, a decimal counter D2012 and a timer (part of the circuit 8155H2 D2064).
With the multiplexer a signal CTB with a frequency of 4 MHz is generated.
The counter realizes the dividing of the 4 MHz signal by factors :2 / :5 / or :10.
Dividing factors of :10 / :100 / :1000 / or :10000 are realized with the timer under the control of the microprocessor.

Multiplexer D2001.

Timing control counter			$\overline{CTB}$	CTB
D	C	B	Output Pt. 5	Output Pt. 6
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

This multiplexer is always enabled.

The multiplexer which is controlled by the signals (CONTC0, CONTC1, CONTC2 and CONTC3) from the control counter produces the signals CTB and $\overline{CTB}$ according to the timing diagram below.

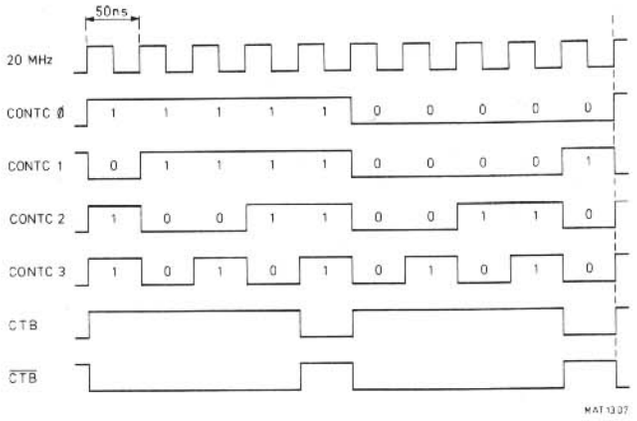


FIG. 3.36. Timing of signal CTB.

The settings of the TIME/DIV switch are read by the microprocessor system. The microprocessor in turn loads the counter circuit D2012 via the signals TBC and TBD according to the next table.

Setting	Frequency	TBD	TBC	TBT	D2012 factor + reload number	8155 factor	TB*10 factor (TIME/DIV pushed)
0,2 ms/div.	2 MHz	1	0	0	2 1000	1	-
0,5 ms/div.	800 KHz	0	1	0	5 0101	1	-
1 ms/div.	400 KHz	0	0	0	10 0000	1	-
2 ms/div.	200 KHz	1	0	1	2 1000	10	-
5 ms/div.	80 KHz	0	1	1	5 0101	10	-
10 ms/div.	40 KHz	0	0	1	10 0000	10	-
20 ms/div.	20 KHz	1	0	1	2 1000	100	-
50 ms/div.	8 KHz	0	1	1	5 0101	100	-
0,1 s/div.	4 KHz	0	0	1	10 0000	100	1000 (1s/div.)
0,2 s/div.	2 KHz	1	0	1	2 1000	1000	10000 (2s/div.)
0,5 s/div.	800 Hz	0	1	1	5 0101	1000	10000 (5s/div.)

Reloading the counter is done when ripple carry output RC is logic "1" and signal $\overline{CTB}$ is logic "1". The counter is loaded then with a value which is determined by the microprocessor system depending on the current setting of the TIME/DIV switch.
Especially for the setting 0,2 ms/div. of the TIME/DIV switch it is necessary to preset the counter only during the time that signal CONTC3 = logic "1" to realize a correct timing for the rest of the circuitry.
(In reality D2093 functions always when TBD = "1").

After loading, the counter will count the 20 MHz input clockpulses, but is only able to do this when the counter is enabled by the signal $\overline{CTB}$ (of 4 MHz).
In this way the counter counts with a speed of 4 MHz and synchronously with the 20 MHz signal.

At the moment that the signal RC is switched to logic "1", the counter will automatically be reloaded again. In this way a continuous counting process is realized.

Dividing by a factor of 2 is done by loading the number 8 (1000) and counting up to 9.
Dividing by a factor of 5 is done by loading the number 5 (0101) and counting up to 9.
Dividing by a factor of 10 is done by loading the number 0 (0000) and counting up to 9.

The resulting output signal RC is applied to the timer circuit. This timer circuit is programmed by the microprocessor system for counting by factors of 1, 10, 1000 or 10000 depending on the setting of the TIME/DIV switch position.
The internal 14 bit COUNT LENGTH REGISTER of the 8155 can be programmed via two addresses 7004H for the L.S.B. and 7005H for the M.S.B.

		7005H						7004H							
M2	M1	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
1	1														

MAT 1308

FIG. 3.37. 14-bit count length register.

The timer is programmed for automatic reloading and generation of a single pulse everytime TC is reached.

In the TIME/DIV switch positions 0,2 ms/div., 0,5 ms/div. andl ms/div. the TIMER OUT signal-path is blocked with signal TBT via NAND-gate D2061. This is done because the timer is not able to divide by a factor of 1.

As result of the time-base generator, HOCOND (hold and convert pulse in DIRECT-mode) pulses are derived when $\overline{\text{SYNCH}}$ = "0". In each TIME/DIV switch position in DIRECT-mode 400 HOCOND pulses will be generated per horizontal division.
Each HOCOND pulse starts the analog to digital conversion of a new input signal sample.

SAMPLING-mode.

Depending on the setting of the TIME/DIV switch, one out of two possible sampling modes is automatically selected. These modes are called SAMPLING I and SAMPLING II mode.

SAMPLING I mode in 0,1 µs/div. ... 5 µs/div.
SAMPLING II mode in 10 µs/div. ... 100 µs/div.

Correct functioning in this mode requires that signals of a repetitive nature are applied to the input channels of the instrument.

Each sampling cycle is started with the WRITE counter in the zero position.

First the SAMPLING I-mode principle will be described.

During one sampling cycle 4096 samples of the input signal are stored in the DISPLAY MEMORY to build a complete signal picture. On each input trigger signal one sample of the input signal is taken in a way as now described.

In SAMPLING I-mode the WRITE COUNTER will be able to count 4096 WEDSP pulses. For this purpose the counter is configurated as follows.

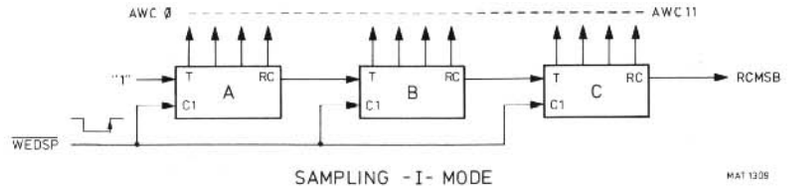


FIG. 3.38. WRITE COUNTER in SAMPLING I mode.

See also the explanation about the functioning of the WRITE COUNTER.

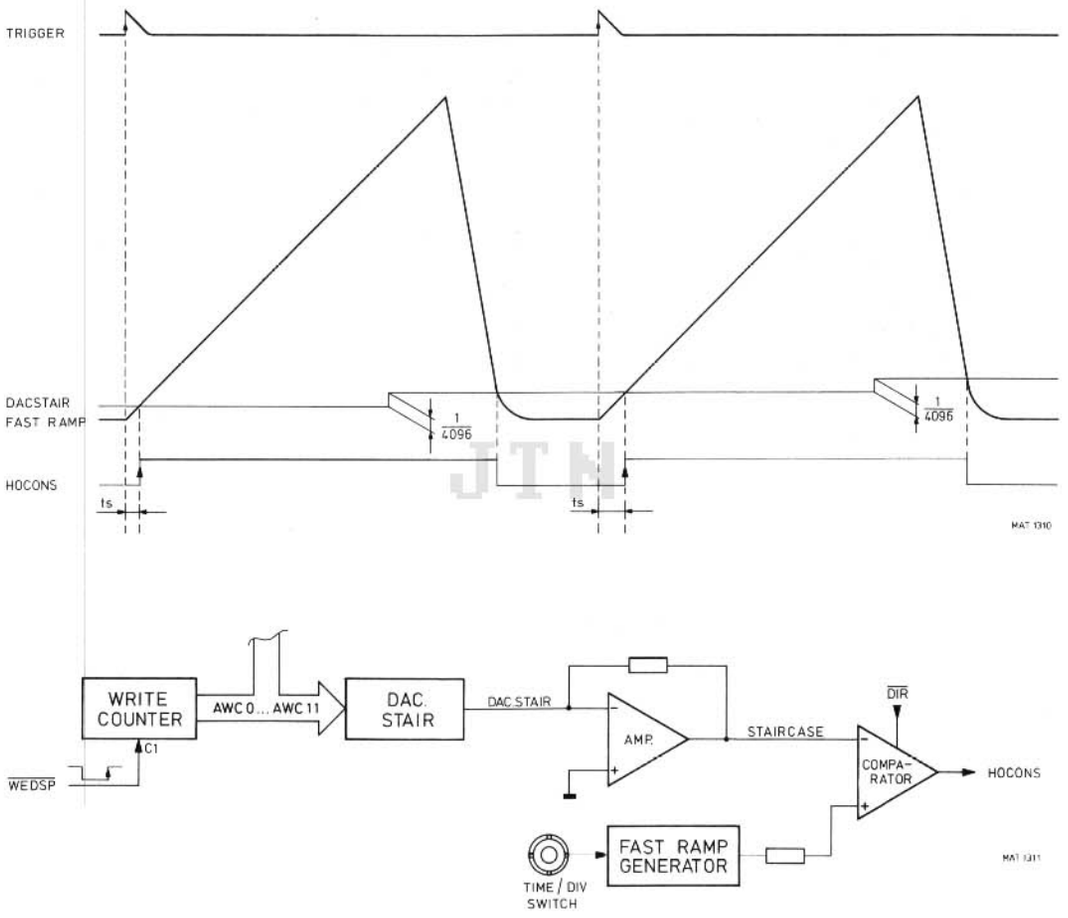


FIG. 3.39. SAMPLING I mode principle.

On each trigger signal a fast ramp is generated (by the normal analog time-base generator), which is compared by a comparator (D2016) with the output signal of a DAC circuit DACSTAIR (D2009).
The WRITE COUNTER output signals AWC0 ... AWC11 are coupled to the DAC STAIR. The WRITE COUNTER runs after flip flop NDRL is switched by the first active trigger. The counter state is then converted into an analog signal DACSTAIR. The comparator is only active in sampling mode. Signal DIR is then logic "0".
At the cross-over point determined by each comparison of the fast ramp signal and the DACSTAIR signal, an HOCONS (hold and convert pulse in SAMPLING-mode) pulse is generated to start the ADC conversion of the new signal sample.

The time between the samples depends on the fast ramp speed, which in turn, is determined by the time-base setting.

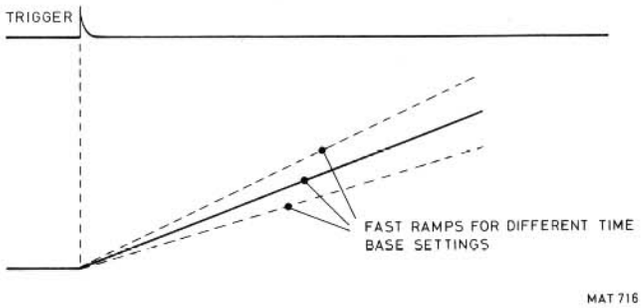


FIG. 3.40. Fast ramp.

After each conversion the WRITE counter state is increased by one step, which causes the DACSTAIR output signal to increase by one step. (1 mV/step on D2024 - pt 6). This can be adjusted by potentiometer R2033 (ampl. staircase).

In this way, the time (ts) between the trigger pulses and the generation of the HOCONS signal increases so that each new sample is taken one step later.
When the WRITE counter reaches the state 4095, the last sample will be taken and a complete picture will be formed.
A new sampling cycle can now be started again.

COMPARATOR

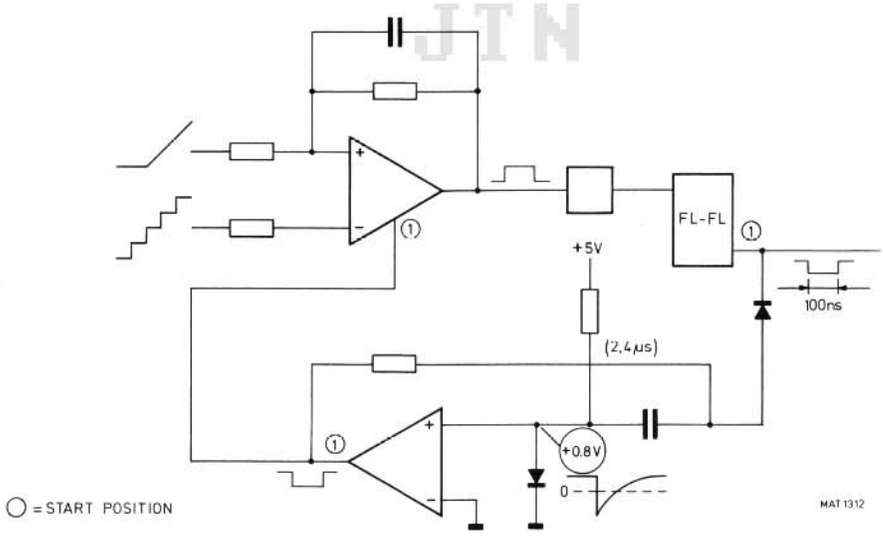


FIG. 3.41. Comparator.

The fast ramp sawtooth voltage is applied to the positive input Pt 12 of comparator D2016. To the negative input Pt 11, a voltage DACSTAIR is applied.
If the fast ramp reaches the potential of the preset voltage DACSTAIR, the comparator output HOCONS goes high. D-type flip flop D2052 will be set and HOCONSE will be "1", thus initiating a new conversion cycle. On the inverted output Pt 8 of this flip flop, a negative going pulse appears, which is applied via diode V2003 and capacitor C2003 to the positive input of a second comparator, which was already on a positive level of 0,7V. This results in a negative going pulse on this "+" input.
The output Pt 4 of this second comparator (with on its "-" input a 0V) is switched to "0" and this "0" is applied to the strobe input Pt 8 of the first comparator and via R2012 and C2003 to the "+" input Pt 1 of the second comparator. In this way the output signal HOCONS of the first comparator will stay high.

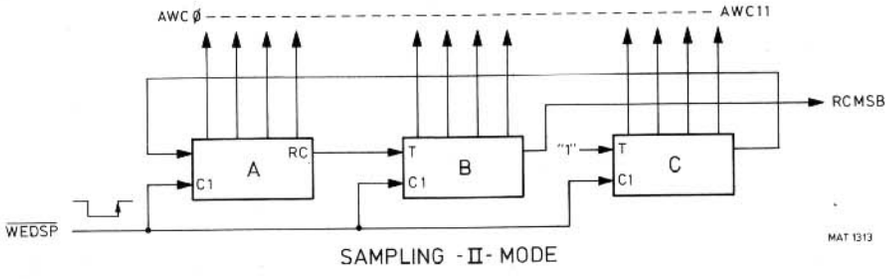
Output Pt 8 of flip flop D2052 and output Pt 4 of D2016 form an AND function, so as long as output Pt 4 of D2016 is low, the anode of V2003 is low.

Capacitor C2003 is reloaded via R2011 from the +5V. When input 1 of D2016 has reached + 0,7 V again (duration about 2,4 μs) output 4 of D2016 is switched to high and the first comparator can be used again because it is enabled again by the high level on its strobe input Pt 8.

This is done to prevent the first comparator from switching more than once for one step made by DACSTAIR.

The SAMPLING II mode principle is now described below.

16 samples per fast ramp instead off 1 sample per fast ramp are digitized in this mode.
This means that this mode is 16x faster. Only 256 sweeps instead off 4096 are needed to built a complete picture. (trace).
The WRITE counter is now configured in such a way that it is counting with steps of 16.



SAMPLING -II- MODE

FIG. 3.42. WRITE COUNTER in SAMPLING II mode.

See also the explanation about the functioning of the WRITE COUNTER.

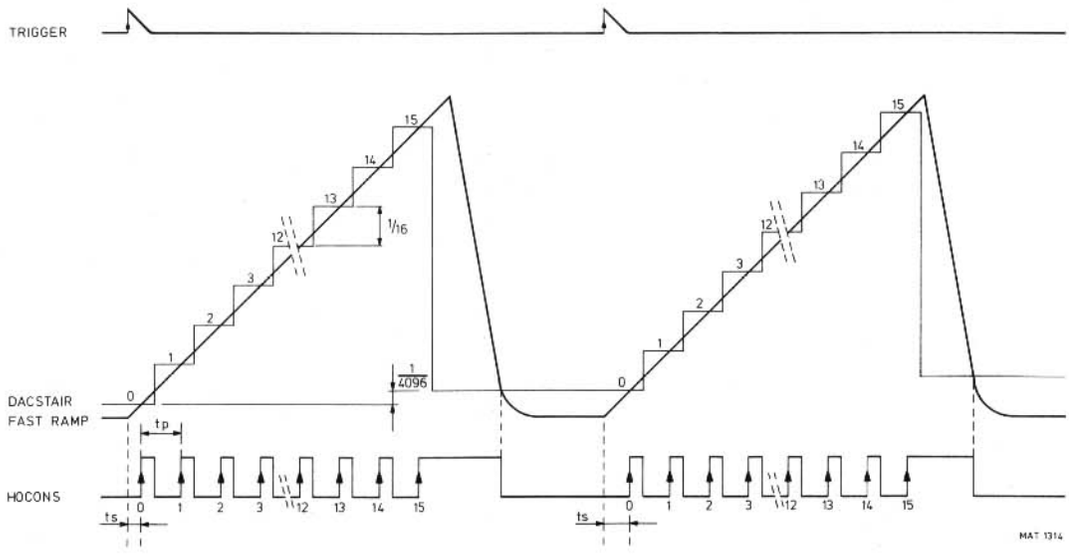


FIG. 3.43. SAMPLING II mode principle.

After 16 samples the system is waiting for a new active trigger and a new fast ramp to produce the next 16 samples and so on.
When the WRITE counter reaches the state 4095 the last sample will be taken and a complete cycle can now be started again.

Note that first 16 samples of channel A are taken, then 16 of channel B and so on.

External clock logic

The conversion ritm can also be determined by the operator by connecting a TTL signal of the required frequency to the EXT CLOCK input socket X6.
These external clockpulses are applied to a retriggerable one shot D2119 resulting in a signal EXTCL when the frequency is $\geq$ 40 Hz.
This signal opens the AND-gate D2093 so that the external clockpulses can pass this gate. These pulses can also pass OR-gate D2079 as long as the signal HOLD OFF OUT = logic "0". This signal is always "0" in EXTERNAL CLOCK mode, because of signal DIR which is "0" then.
For clockfrequencies $\leq$ 40 Hz the one shot D2119 can be switched by means of switch S2002. This is an internal switch located on unit A11.
With S2002 closed, signal EXTCL will be steady "1".

Hold off logic.

The HOLD OFF IN and the HOLD OFF OUT signal are the same in MEMORY OFF mode.

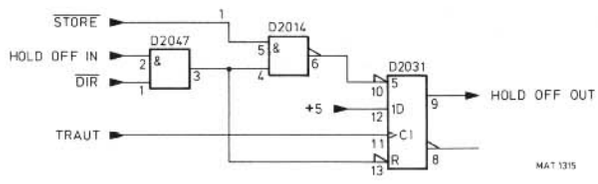


FIG. 3.44. Hold-off logic.

In MEMORY ON ($\overline{\text{STORE}}$ = "0") and DIRECT-mode ($\overline{\text{DIR}}$ = "0") signal HOLD OFF OUT will steady be "0" and the sawtooth generator will be blocked.(Not in the AUTO - mode).

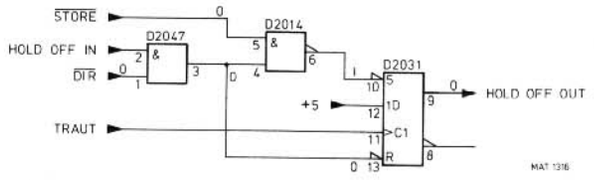


FIG. 3.45. Hold-off logic.

In MEMORY ON ($\overline{\text{STORE}}$ = "0") and SAMPLING - mode the upgoing edge of the HOLD OFF OUT signal is made synchronous with the triggers.

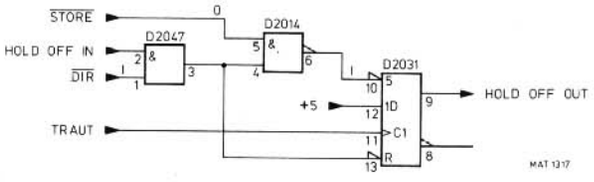


FIG. 3.46. Hold-off logic.

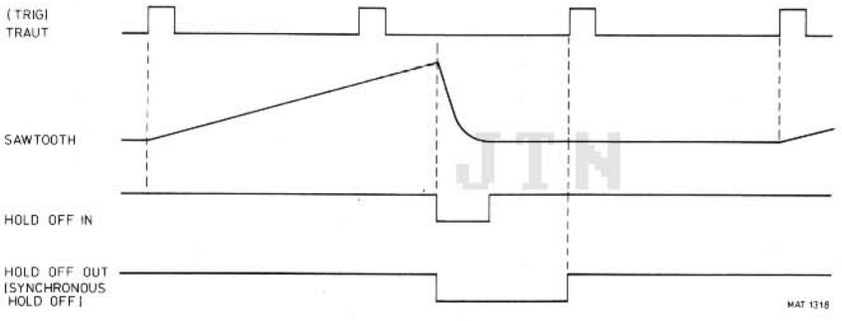


FIG. 3.47. Hold-off timing.

Because of internal drift in the oscilloscope, it can happen in the SAMPLING mode that no HOCONSE pulses are generated because the sawtooth level is higher than the DACSTAIR level, so that the comparator will not switch at all, it gives constantly logic "1" at the output.

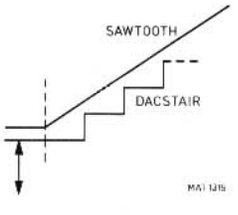


FIG. 3.48. Adjustment of correct DACSTAIR level.

With the aid of the HOLD OFF circuit a HOLD OFF OUT signal (derived from TRAUT) applied to Pt. 4 of OR-circuit D2079 causes the generation of a HOCONSE pulse to start the SAMPLING cycle.

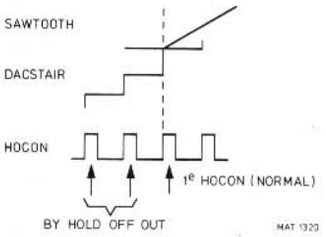


FIG. 3.49. Adjustment of startpoint.

After the correct adjustment of the starting point with the aid of potentiometer R2034 the HOLD OFF OUT signal is not needed any longer as a start signal for the SAMPLING cycle.

ADC logic. (Conversion timing).

This circuit contains the timing circuits that generate the signals required to control the conversion of an analog signal sample to a digital signal sample.
Each conversion is started by a HOCOND, a HOCONS or an EXTCL signal.

HOCOND in DIRECT-mode. (see timing diagram)

Output H of D-type flipflop D2066 is switched to one on the first 20 MHz pulse when HOCOND is active. At the same moment the second D-type flip flop D2052 will switch, resulting in signal STADC (Start ADC) going to logic "1" because the HOCOND pulse is applied via OR-gate D2076 to the D-input of this second flip flop. The ADC will start now the analog-to-digital conversion.
Directly when HOCOND disappears, the first flipflop will be resetted and one 20 MHz pulse later the second flip flop will be resetted resulting in signal STADC going to logic "0".
On the first clockpulse after STADC is made active, the signal TRACK is switched to logic "0".
The ADC answers with generating the BUSY signal. As long as the BUSY signal is logic "1", signal TRACK will be held "low" and the analog sample is hold in the Track and Hold circuit.
Conversion is controlled by the clockpulses CLADC which are directly derived from the 20 MHz clocksignal from the VCO.
During conversion in the ADC, the signal BUSY is at logic "1". After conversion, this signal BUSY goes to logic "0", indicating that conversion is completed.
Output TRACK of D-type flipflop D2066 is now switched to "1" again by the signal BUSY on the D-input of the flip flop.
The track and hold circuit now returns to tracking the input signal.

HOCON in SAMPLING and EXTERNAL CLOCK mode (see timing diagram).

In SAMPLING and EXTERNAL CLOCK the HOCONSE signal will be generated asynchronously with the 20 MHz signal.
In these situations signal TRACK will be switched directly to "0" via the $\overline{\text{HOCONSE}}$ signal on the "direct set" input point 10 of the TRACK flip flop D2066. The conversion cycle starts then according to the description above.

Signal RESDET.

Reset signal for the peak detectors in the MIN/MAX circuits. The signal is drawn in the figure below for SINGLE-channel as well as for DUAL-channel mode.

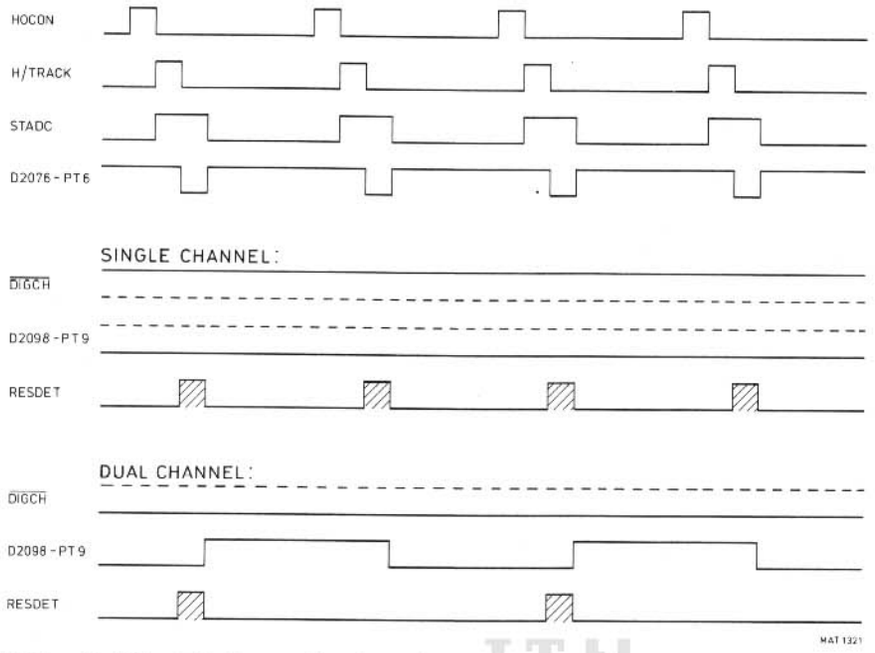


FIG. 3.50. Timing of signal RESDET.

Signal TRRES.

Signal TRRES (trigger reset) is steady "1" if MIN/MAX mode is not selected.
With MIN/MAX selected signal TRRES is switched under the influence of signal CT.
Depending on signal $\overline{\text{DIGCH}}$ the period time is divided by a factor two or not. (For SINGLE- and DUAL channel).
See also the timing diagram for the MIN/MAX mode.

3.7.8. Adaption circuit (Diagram 14)

The output signals YDAC and XDAC from the LOGIC UNIT A11 are each applied to a T&H circuit controlled by the control signal TRSHXY. These circuits are needed for deglitching and correct dot joining.

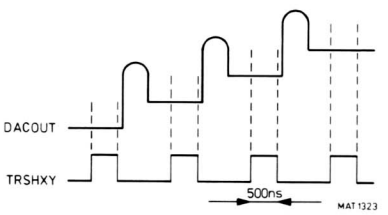


FIG. 3.52. Deglitching DAC

Signals YDAC and XDAC are then smoothed by a SMOOTH filter, consisting of C1758 - C1759 - R1726 - C1706 and C1707 for YDAC and C1761 - C1762 - R1769 - C1752 and C1753 for XDAC.
They are controled by signal SMOOTH.

The resulting YOUT signals are fed via an adaption circuit to the vertical FINAL Y AMPLIFIER. This amplifier directly drives the (Y) plates of the C.R.T.

The resulting XOUT signal is applied to the horizontal FINAL X AMPLIFIER which directly drives the (X) plates of the C.R.T.

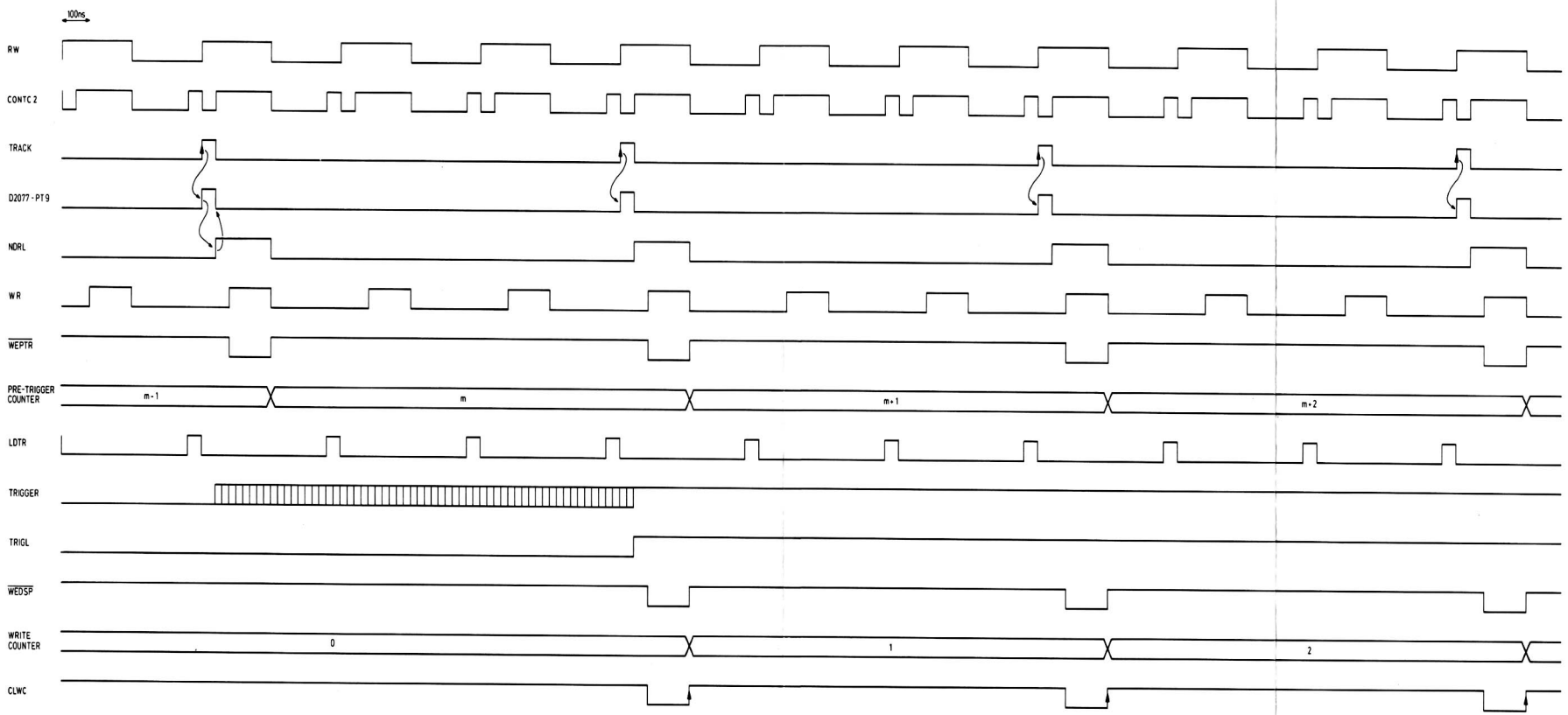


FIG. 3.51. Timing conversion + write cycle.

JTN

3.7.9. IEEE-488/IEC-625 option (Diagram 15)

General:

An IEEE-488 interface unit PM8955 can be added to the PM3305 oscilloscope to enable the oscilloscope to be used in a measuring system together with other IEEE-bus compatible instruments.

For installation instructions refer to the sheet which is delivered with the PM8955 option.

For more detailed operating information refer to the separate Operating Manual of the PM8955.

- PM3305C instruments are already provided with an IEEE-488 interface unit which has been built in in the factory.

- For service spareparts refer to chapter "PARTS LISTS".

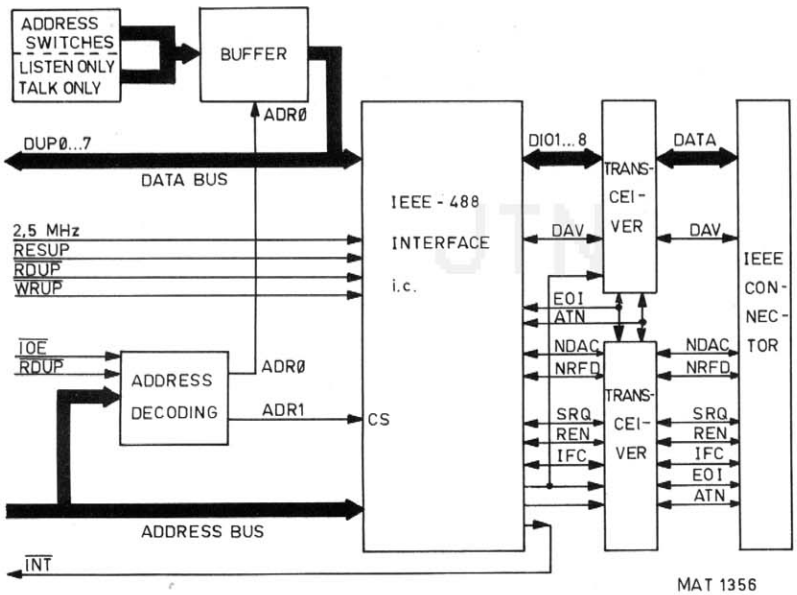


FIG. 3.53. Blockdiagram.

General description: (refer to block diagram).

An IEEE bus interface is used in multidevice systems to connect the instruments in parallel to the same interface lines. Each instrument has its own specific address (selected with switches in the instrument) so that an instrument is only listening after it has received its specific address, in IEEE terms is called My Listen Address (MLA). The listen addresses are generated by the controller of the system (e.g. a computer) and are transmitted via the data lines of the bus during an address or interface message the attention line

(ATN) is active to indicate that the information on the data lines have a special interface function.
The IEEE bus can be split up into three functional parts: the data bus, the handshake bus and the management bus.
- The data bus is used to transport messages for the device functions as well as for the interface functions and consists of 8 lines (DIO1...8).
- The handshake bus controls the correct transfer of data bytes with the next three signals.

Data valid (DAV) indicated the condition of information on the 8 DIO lines.
Not ready for data (NRFD) indicates the condition of readiness of device(s) to accept data.
Not data accepted (NDAC) indicates the condition of acceptance of data by devices.
A timing diagram for the handshake cycle is shown in the figure, take notice that the cycle is as fast as the slowest instrument.

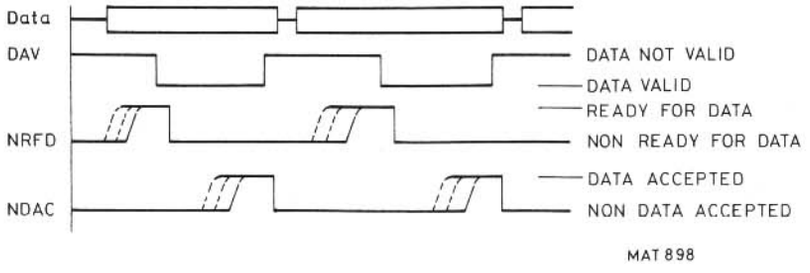


FIG. 3.54. Handshake cycle.

- The management bus is used to manage an orderly flow of information accross the interface.

Herefore the next five signals are available:

Attention (ATN) specifies how data on the DIO lines are to be interpreted. Active indicates a message is transferred via the data bus (for example a listen address), not active status is present during normal data transfer (for example a command for the oscilloscope).
Interface clear (IFC) places the interface of all interconnected devices in a known quiescent state.
Service request (SRQ) indicates that one of the instruments wants the attention of the controller for example to give an error message.
Remote enable (REN) sets an instrument to its remote-control mode, if it is in the addressed state.
End or identify (EOI) indicates the end of a multiple byte transfer.

NOTE: Because of the negative logic used for the IEEE bus the signals are "true" (active) when they have a low level.

Initiation of the interface:

When the oscilloscope is switched-on, the CPU checks whether the hardware is available or not. If yes, the CPU starts with the initiation of the interface by sending control signals to the IEEE interface i.c. D2401. The integrated circuit D2401 then reads the

status of the address selection switches S2401(1-2-3-4-5), LISTEN ONLY S2401(6) and TALK ONLY S2401(7) via buffer D2404 which is activated by address E008 (IPTADR). The device address is placed into an internal register of D2401.

Bit 0 - hardware available
1 - TON
2 - LON
3 - 5 }
4 - 4 |
5 - 3 } Device address
6 - 2 |
7 - 1 }

Now the interface is ready to operate.

Receiving:

First the system-controller sends a listener address via the DIO lines (so ATN is "true"). If the address is equal to the device address in the internal register of D2401, the interface becomes the listener status, this action is performed without intervention of the CPU of the osciloscope. Once in the listener state all succeeding data (without ATN = "true") is read by the CPU of the oscilloscope.
The i.c. D2401 realizes the bus handshake.

First Not Ready For Data (NRFD) is made "false" by the PM8955, so the interface is ready to receive data. Then the controller puts data on the DIO lines and makes DAta Valid (DAV) "true". DAV is received by D2401. Data can then be accepted by the interface. DAV is also supplied to the interrupt logic, so the CPU of the oscilloscope interrupts its current programm (via signal $\overline{INT}$) and checks the interrupt status.
The oscilloscope then reads the data from i.c. D2401. Subsequently the CPU gives a "ready for the next message" to D2401 thus enabling D2401 to interrupt the oscilloscope for the next data byte.

Transmitting:

The PM3305 in combination with the PM8955 is capable to send status messages to a controller in case of an error condition. If the oscilloscope has such a message, it asks the attention of the controller by means of the Service ReQuest (SRQ) line. This line becomes active after the CPU has set the request for service bit. All the connected instruments use the same SRQ line so the controller must check which of the instruments has caused the service request. This is called SERIAL POLLING therefore the controller must address the instruments one by one as talker and read the status-byte: The seventh bit of the status-byte indicates that the corresponding instrument has asked for service, the other bits give the status condition of the instrument.
The sequence of signals during an error condition is as follows. First the CPU activates the request for service signal and activates D2401. The result is an active SRQ-line.
The controller sends talk addrresses, once become talker the CPU puts the status-byte on the bus and gives the information "new byte available" to i.c. D2401.
Subsequently the PM8955 waits till NRFD becomes "false" and the DAV is made "true" and NRFD is resetted by the controller.
When the controller has received the data, it makes the signal NDAC "false", the PM8955 then answers with setting DAV "false" and then the controller resets the NDAC signal.

Address decoding:

To select I/O ports of the IEEE interface, the inputs of the address decoding circuit D2406 must have the logic levels as given in the next table.

INPUTS					ADDRESS	OUTPUT	SELECTED FUNCTION	
$\overline{IOE}$	AUP3	AUP2	AUP1	AUP0	Hex.			
0	0	0	0	0	E000	ADR1	DATAIO	Data input/output
0	0	0	0	1	E001	ADR1	INSTA1	Interrupt status 1
0	0	0	1	0	E002	ADR1	INSTA2	Interrupt status 2
0	0	0	1	1	E003	ADR1	SERPOL	Serial poll status
0	0	1	0	0	E004	ADR1	ADRSTA	Address status
0	0	1	0	1	E005	ADR1	COMMND	Command pass through
0	0	1	1	0	E006	ADR1	ADRES0	Address 0
0	0	1	1	1	E007	ADR1	ADRES1	Address 1
0	1	0	0	0	E008	ADR0	IPTADR	Input address

Address selection:

With switches S2401 (1-2-3-4-5) the device address is selected.
Do not use the code 00000 or 11111, the first is generally used as the address of the system controller, the latter is the code for the commands "unlisten" and "untalk".
The switch settings are placed in an internal buffer of D2401 via buffer D2404.

"Talk only" and " Listen only" are only used for the MEM DUMP function.

Interrupt logic, interrupt status:

The output signal $\overline{INT}$ of D2401 gives an interrupt to the CPU of the oscilloscope. This is for example done by DAV "true".
The CPU of the oscilloscope will then interrupt his program and will read the interrupt status to check the status of the interface board after an interrupt has been received.

Clock signal, RESUP signal:

The clockpulse of 2,5 MHz from the PM3305 is used for the internal synchronisation of D2401.

The RESUP signal is used to reset the i.c. D2401 to initial values.
The figure shows the signals when the instrument is switched on.

Transceivers:

As tranceiver for the eight DIO lines and the DAV line D2402 is used.
The remaining transceiver D2403 is used for the other handshake line and for the management lines.

Cable + connectors:

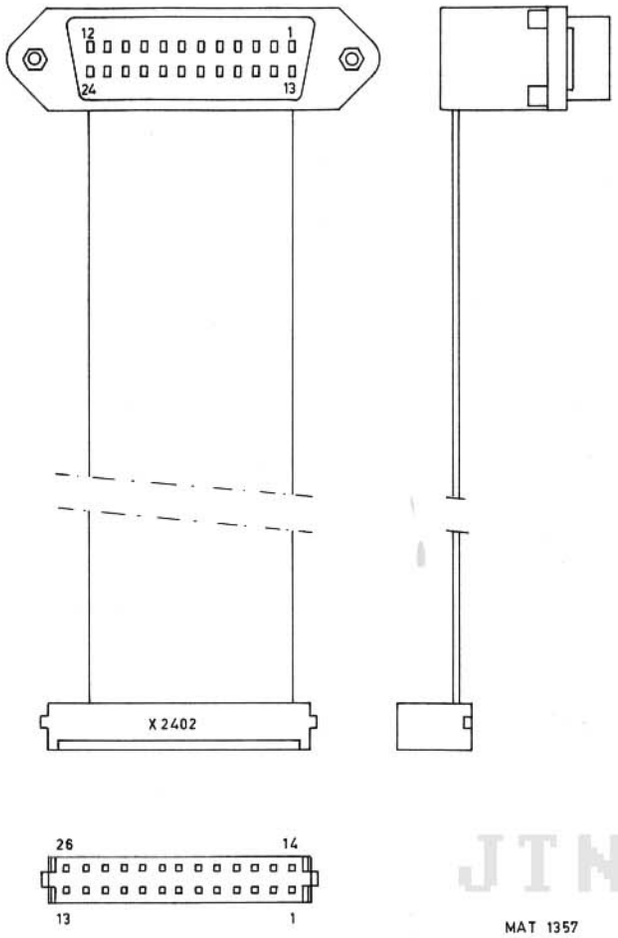


FIG. 3.55. Cable + connectors.

4. DISMANTLING THE INSTRUMENT

4.1. GENERAL INFORMATION

This section provides the dismantling procedures required for the removal of components during repair operations.
All circuit boards removed from the instrument must be adequately protected against damage, and all normal precautions regarding the use of tools must be observed.
During dismantling a careful note must be made of all disconnected leads so that they can be reconnected to their correct terminals during assembly.

CAUTION: Damage may result if:
- The instrument is switched on when a circuit board has been removed.
- a circuit board is removed within one minute after switching-off the instrument.

4.2. REMOVING THE INSTRUMENT COVERS

The instrument is protected by three covers: a front panel protection cover, an instrument cover with carrying handle and a rear panel.
To facilitate removal of the instrument cover and the rear panel, first ensure that the front cover is in position.

Then proceed as follows:

- Hinge the carrying handle clear of the front cover; to this end, push both pivot centre buttons (Fig. 4.1.)
- Stand the instrument on its protective front cover on a flat surface.
- Slacken the two coin-slot screws located at the rear panel.
- Lift the rear panel.
- Lift off the instrument cover (if necessary bend the cover at the side of the rubber feet so that the feet do not stick behind frame parts or components).
- For acces to the front panel, stand the instrument horizontally and snap off the front cover.

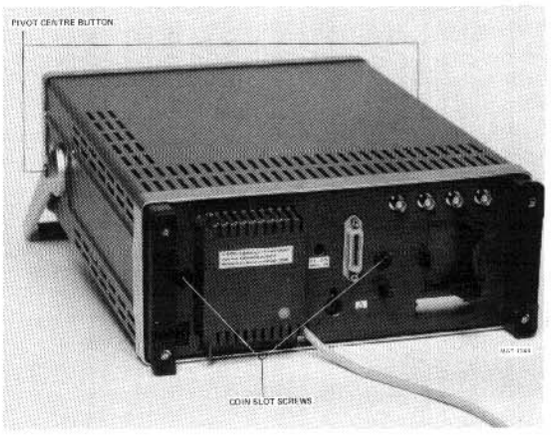


FIG. 4.1. Removing the instrument covers.

4.3. ACCESS TO PARTS FOR CHECKING AND ADJUSTING PROCEDURES.

All adjusting elements are accessible after removing the covers.

5. PERFORMANCE CHECK

5.1. GENERAL INFORMATION

WARNING: Before switching-on, ensure that the instrument has been installed in accordance with the Installation Instructions outlined in Section 3 of the Operating Manual.

This procedure is intended to:
check the instruments' specification.
- be used for incoming inspection to determine the acceptability of newly purchased instruments and/or recently recalibrated instruments.
- check the necessity of recalibration after the specified recalibration intervals.

NOTE: The procedure does not check every facet of the instruments calibration; rather, it is concerned primarily with those parts of the instrument which are essential to measurement accuracy and correct operation. Removing the instruments covers is not necessary to perform this procedure. All checks are made from the outside of the instrument.

If the test is started within a short period after switching-on, bear in mind that steps may be out of specification, due to insufficient warming-up time.

NOTE: At the start of every check, the controls should always be left in the last position, unless otherwise stated.

NOTE: Set the TIME/DIV switch to a suitable position; unless otherwise stated.

5.2. PRELIMINARY SETTINGS

- Start the procedure with NO input signals connected, ALL pushbuttons released and ALL switches in the CAL position.

5.3. RECOMMENDED TEST EQUIPMENT

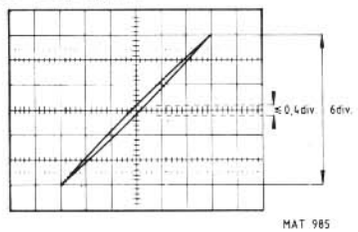
TYPE INSTRUMENT	REQUIRED SPECIFICATION	EXAMPLE OF RECOMMENDED INSTRUMENT
Function generator	Freq.:1mHz...10MHz Sine-wave/Square-wave Ampl.:0...40Vp-p DC offset:0...±10V Rise time:<30ns Duty cycle:50%	Philips PM 5167
Constant amplitude sine-wave generator	Freq.:100kHz...40MHz Constant ampl. 120Vp-p and 3Vp-p	Tektronix SG503
Square-wave calibration generator	Freq.:10Hz...1MHz Ampl.:50mV...60V Rise time:<1ns Duty cycle:50%	Tektronix PG506
Time marker generator	Repetition rate: 0,5s...0,01s	Tektronix TG501
Counter	Freq.:25MHz	Philips PM 6661
Variable mains transformer	Well-insulated voltage:90...264V	Philips ord.nr. 2422 529 00005
DC power supply	Adjustable output: 20...28V, 2A	Philips PE 1540
Moving iron meter		
Dummy probe 2 : 1	1Mega Ohm±0,1%//25pF	
Cables T-piece	General radio types for fast rise-time generators. BNC types for other applications	

5.4. CHECKING PROCEDURE

STEP	OBJECTIVE	INPUT SIGNAL	SETTINGS	REQUIREMENTS	MEASURING RESULTS
1.	POWER ON				
1.1a	Start power supply	Mains voltage 50 Hz...400 Hz ±10%	Depress pushbutton POWER ON S17	-Starts at selected mains voltage ± 10 % -Pilot lamp B1 lights	
1.1b	Power consumption			-70 W from a.c.	
1.2a	Start Power supply	24 V (X 11 rear side)	Depress pushbutton POWER ON S17	-Starts at d.c. voltages from 24 V...28 V -Pilot lamp B1 lights	
1.2b	Current consumption			-2 A max. including PM 8955	
2.	CRT SECTION				
2.1.	Intens		Turn INTENS control R1	-Normal intensity adjustment possible	
2.2.	Focus		Turn FOCUS control R6	-Trace sharpness adjustment possible	
2.3.	Trace rotation		Turn TRACE ROT screw R10	-Trace rotation adjustment possible	
2.4.	Graticule illumination		Turn ILLUM control R11	-Graticule illumintion possible	
MEMORY OFF					
3.	VERTICAL AXES				
3.1.	Display modes	Sine wave signal 2kHz 60mVp-p to A and B A and B inputs	Set AMPL/DIV to 20mV(S8) S6 Depress A S1 Depress CHOP S1 Depress ALT S1 Depress ADD S1 Depress B S1	-Sine wave 2kHz 3 div. displayed (A) -Traces of A and B chopped displayed -Traces of A and B alternated displayed -Sine wave 2kHz 6 div. displayed (A+B) -Trace of B displayed	
3.2.	Polarity inversion B	as 3.1.	Pull PULL TO INVERT S4	-Trace of B inverted displayed	
3.3.	Dynamic range	Sine wave signal 10MHz 2,4Vp-p to (B)A input	Set AMPL/DIV to 0,1V(S8) S6 Turn POSITION (R3) R2	-24 div. amplitude distorsion-free displayed	
3.4.	Bandwidth	Sine wave signal 1MHz, 120mV to (B)A input Increase to 35MHz	Set AMPL/DIV to 20mV(S8) S6	-Adjust input signal for 6 div. amplitude -Amplitude ≥4,2 div.	
3.5.	Rise time	Square wave signal 1MHz, 100mVp-p to (B)A input rise time ≤1ns	As 3.4.;Depress SLOPE(-) S3 Set the input signal between the dotted lines (R3) R2	-Rise time measured between 10% and 90% (4 div.) must be ≤7ns (second pos. slope)	

STEP	OBJECTIVE	INPUT SIGNAL	SETTINGS	REQUIREMENTS	MEASURING RESULTS
3.6.	Pulse abberations	As 3.5.	As 3.4.	-Amplitude 5 div.,+ and - 2,5 div. from -Aberrations ≤3% (≤4%p-p)	
3.7.	Vertical deflection coefficients	Square wave signal 2kHz to (B)A input. Ampl: 10mVp-p 20mVp-p 50mVp-p 100mVp-p 200mVp-p 500mVp-p 1 Vp-p 2 Vp-p 5 Vp-p 10 Vp-p 20 Vp-p 50 Vp-p	Set AMPL/DIV (B)A (S8) S6 to: 2 mV/div. 5 mV/div. 10 mV/div. 20 mV/div. 50 mV/div. 0,1V/div. 0,2V/div. 0,5V/div. 1 V/div. 2 V/div. 5 V/div. 10 V/div.	-Amplitude 5 div. ±3% -Amplitude 4 div. ±3% -Amplitude 5 div. ±3% -Amplitude 5 div. ±3% -Amplitude 4 div. ±3% -Amplitude 5 div. ±3% -Amplitude 5 div. ±3% -Amplitude 4 div. ±3% -Amplitude 5 div. ±3% -Amplitude 5 div. ±3% -Amplitude 4 div. ±3% -Amplitude 5 div. ±3%	
3.8.	Continuous control	Square wave signal 2kHz, 120mVp-p to (B)A input (B)A input	Set AMPL/DIV to 20mV(S8) S6 (S8) S6 Turn CONT. control (R8) R7	-Range 1:≥2,5	
3.9.	Vertical positioning	Sine wave signal 10kHz 1,6Vp-p to (B)A input	Set AMPL/DIV to 20mV(S8) S6 Turn POS control (R3) R2	-top and bottom peaks of sine wave possible to display at screen centre	
3.10.	Input impedance (MAT 1053)	Square wave signal 2kHz to A(B) input via dummy 200mVp-p 5 Vp-p 50 Vp-p	Set AMPL/DIV (B)A (S8) S6 to: 20mV/div. 0,5V/div. 10 V/div.	-Amplitude 5 div. -Amplitude 5 div. -Amplitude 2,5 div.	
3.11.	Input coupling	Sine wave signal 2kHz + dc offset to (B)A input	Depress 0 (S15) S13 Set the trace in the screen centre R2 R3 Depress AC (S14) S12 Depress DC (S14) S12	-Centre of the sine wave is displayed at screen centre -Centre of the sine wave is displayed at DC offset level	
3.12.	CMMR	Sine wave signal 1MHz 480mVp-p to A and B	Set AMPL/DIV to 20mV(S8) S6 Pull PULL TO INVERT S4 Depress ADD S1	-Rejection >40dB (0,24 div.)	

STEP	OBJECTIVE	INPUT SIGNAL	SETTINGS	REQUIREMENTS	MEASURING RESULTS
3.13.	Trace jump		Depress 0 (S15) S13		
	a. Attenuator		Set traces at screen centre		
			Set AMPL/DIV (B)A to all		
			positions except for b.	-Trace jump $\leq$0,1 div.	
	b. 20mV<->10mV		Switch AMPL/DIV (B)A between		
			20mV<->10mV (S8) S6	-Trace jump $\leq$1 div.	
	c. Continuous control		Turn CONT. control (R8) R7	-Trace jump $\leq$0,5 div.	
	d. Normal/Invert B		Pull PULL TO INVERT B S4	-Trace jump $\leq$1 div.	
	e. MEMORY ON/OFF		Depress MEMORY ON S17	-Trace jump $\leq$0,3 div.	
	f. Temp. drift at 23°C			-Trace jump $\leq$0,3 div./hour	
3.14.	Cross talk between channel A and B	Sine wave signal 10MHz, 120mVp-p to A input	Set AMPL/DIV to 20mV(S8) S6		
			Depress B S1	-Cross talk from A to B 0,06 div.(40dB)	
		Increase freq. to 35MHz		-Cross talk from A to B 0,19 div.(30dB)	
4.	HORIZONTAL OR X-AXES				
4.1.	Time coefficients	Marker pulse signal to A input. Rep. time:	Set TIME/DIV to: S10		
		0,1/us	0,1/us/div.	-Coefficient error $\leq$3% (0,3 div.)	
		0,2/us	0,2/us/div.	-Coefficient error $\leq$3% (0,3 div.)	
		0,5/us	0,5/us/div.	-Coefficient error $\leq$3% (0,3 div.)	
		1 /us	1 /us/div.	-Coefficient error $\leq$3% (0,3 div.)	
		2 /us	2 /us/div.	-Coefficient error $\leq$3% (0,3 div.)	
		5 /us	5 /us/div.	-Coefficient error $\leq$3% (0,3 div.)	
		10 /us	10 /us/div.	-Coefficient error $\leq$3% (0,3 div.)	
		20 /us	20 /us/div.	-Coefficient error $\leq$3% (0,3 div.)	
		50 /us	50 /us/div.	-Coefficient error $\leq$3% (0,3 div.)	
		0,1ms	0,1 ms/div.	-Coefficient error $\leq$3% (0,3 div.)	
		0,2ms	0,2 ms/div.	-Coefficient error $\leq$3% (0,3 div.)	
		0,5ms	0,5 ms/div.	-Coefficient error $\leq$3% (0,3 div.)	
		1 ms	1 ms/div.	-Coefficient error $\leq$3% (0,3 div.)	
		2 ms	2 ms/div.	-Coefficient error $\leq$3% (0,3 div.)	
		5 ms	5 ms/div.	-Coefficient error $\leq$3% (0,3 div.)	
		10 ms	10 ms/div.	-Coefficient error $\leq$3% (0,3 div.)	
		20 ms	20 ms/div.	-Coefficient error $\leq$3% (0,3 div.)	
		50 ms	50 ms/div.	-Coefficient error $\leq$3% (0,3 div.)	
		0,1 s	0,1 s/div.	-Coefficient error $\leq$3% (0,3 div.)	
		0,2 s	0,2 s/div.	-Coefficient error $\leq$3% (0,3 div.)	
		0,5 s	0,5 s/div.	-Coefficient error $\leq$3% (0,3 div.)	
4.2.	Continuous control	Marker pulse signal to A input. Rep. time 0,1ms	Set TIME/DIV to 10/us S10		
			Turn CONT. control R9	-Continuous range 1:$\geq$2,5	
4.3.	Magnifier	As 4.2.	Set TIME/DIV to 1ms S10	-Coefficient error $\leq$5% (0,5 div.)	
			Pull X MAGN S5	(first div. excluded)	
4.4.	Horizontal positioning		Turn X POS. cw and ccw R4	-Trace-start and trace-end at screen centre	

STEP	OBJECTIVE	INPUT SIGNAL	SETTINGS		REQUIREMENTS	MEASURING RESULTS
5.	X-DEFLECTION					
5.1.	Mode (B)A	Sine wave signal 2kHz, 120mVp-p to (B)A input	Depress (B)A Depress (B)A Set TIME/DIV to X DEFL Set AMPL/DIV to 20mV (S8)	S1 S16 S10 S6	-A line under an angle of 45° with respect to horizontal graticule lines is displayed Amplitude horizontal and vertical 6 div. ±10% (0,6 div.)	
5.2.	Mode EXT	Sine wave signal 2kHz, 1,6Vp-p to EXT input	Depress EXT Set TIME/DIV to X DEFL	S16 S10	-Amplitude 8 div. ±10%	
5.3.	Mode EXT :10	Sine wave signal 2kHz, 16Vp-p to EXT :10 input	Depress EXT :10	S16	-Amplitude 8 div. ±10%	
5.4.	Mode LINE		Depress LINE Set TIME/DIV to X DEFL	S16 S10	-Amplitude 8 div. ±10%	
5.5.	Bandwidth	Sine wave signal 2kHz to EXT input 1MHz 1MHz	Depress EXT Set TIME/DIV to X DEFL Depress DC Depress AC	S16 S10 S2 S2	-Adjust for 8 div. amplitude -Amplitude ≥5,6 div. -Amplitude ≥5,6 div.	
5.6.	Dynamic range	Sine wave signal 100kHz				
5.7.	Phase shift between X and Y ampl.	Sine wave signal to A input: 2kHz 100kHz	Set TIME/DIV to X DEFL Set AMPL/DIV to 20mV Adjust the input signals for 6 div. amplitude	S10 S6	-A line under an angle of 45° with respect to the horizontal graticule line is displayed. 	
6.	TRIGGERING					
6.1.	Trigger source A and B	Sine wave signal 10kHz, to A input; square wave signal 2kHz to B input	Depress ALT Adjust the input signals for 6 div. amplitude Depress A Depress B Depress COMP	S1 S16 S16 S16	-Well triggered display of channel A -Well triggered display of channel A -Well triggered display of channel B -Well triggered display of channel A and B	
6.2.	Trigger source EXT	Sine wave signal 2kHz, 240mVp-p to A and EXT	Depress EXT	S16	-Well triggered display	

STEP	OBJECTIVE	INPUT SIGNAL	SETTINGS		REQUIREMENTS	MEASURING RESULTS
6.3.	Trigger source LINE	Sine wave signal related to line frequency to A	Depress LINE	S16	-Well triggered display	
6.4.	Slope	Sine wave siganl 2kHz, 120mVp-p to A input	Release SLOPE Depress SLOPE	S3 S3	-Signal triggers on positive going edge -Signal triggers on negetive going edge	
6.5.	Sensitivity INT	Sine wave signal to A 1Hz 5Hz 20Hz 5MHz 35MHz	 Depress DC Depress AC Depress AUTO	 S2 S2 S2	 -Signal triggers at 0,5 div. amplitude -Signal triggers at 0,5 div. amplitude -Signal triggers at 0,5 div. amplitude -Signal triggers at 0,5 div. amplitude -Signal triggers at 1 div. amplitude	
6.6.	Sensitivity EXT (EXT:10)	Sine wave signal to A 5MHz 35MHz	Depress EXT (EXT:10)	S16	 -Signal triggers at 0,1Vp-p (1Vp-p) -Signal triggers at 0,2Vp-p (2Vp-p)	
6.7.	Sensitivity TV	TV signal to A input	Depress A Depress TV	S16 S2	 -Signal triggers at 0,7 div.amplitude	
6.8.	Level range	Sine wave signal 2kHz, 60mVp-p to A input Sine wave signal 2kHz, 1Vp-p to A and EXT input	Set AMPL/DIV to 10mV Depress AUTO Turn LEVEL control Depress DC Turn LEVEL control Depress EXT (EXT:10) Turn LEVEL control	S6 S2 R5 S2 R5 S16 R5	 -Signal triggers at complete LEVEL range -Signal triggers over ±6 div. amplitude -Signal triggers over ±0,8(8)V amplitude	
6.9.	EXT trigger input impedance	Sine wave signal 2kHz, 1Vp-p to A and EXT input via dummy Sine wave signal 2kHz, 2Vp-p to A and EXT input via dummy	Depress EXT Turn LEVEL control Turn LEVEL control	S16 R5 R5	 -Signal not triggered in the most extreme positions of the LEVEL control -Signal triggers at complete LEVEL range	
7.	CALIBRATION				-Calibration voltage is 1,2Vpp frequency about 2kHz	

MEMORY ON

STEP		INPUT SIGNAL	SETTINGS		REQUIREMENTS	MEASURING RESULTS
8.	Channes A,B,C and D					
8.1.	Display modes	Sine wave signal 2kHz, 120mVp-p to A and B 0,6Vp-p to 0,1V c and D	Depress A	S16		
			Depress AUTO	S2		
			Set TIME/DIV to 0,2ms	S10		
			Set AMPL/DIV to 20mV	S8 S6		
			Depress A	S1	-Sine wave 2kHz, 6div. displayed (A)	
			Depress B	S1	-Sine wave 2kHz, 6div. displayed (B)	
			Depress ALT	S1	-Traces of A and B displayed	
			Depress CHOP	S1	-Traces of A and B displayed	
			Depress ADD	S1	-Clamped traces of A+B displayed	
			Depress ABCD CHOP	S27	-Traces of A,B,C and D displayed	
			Release ABCD CHOP			
			Depress A	S1		
8.2.	Compare	As 8.1.	As 8.1 plus:		-Sine wave 2kHz, 6 div. displayed	
			Depress COMPARE	S22	-2 sine waves displayed, one possible to shift with POSITION A (R2)	
			Release COMPARE	S22		
			Depress CHOP	S1	-2 sine waves displayed (A and B)	
			Depress CHOP	S22	-4 sine waves displayed, two possible to shift with POSITION A and B (R2 and R3)	
			Release COMPARE	S22		
			Depress ABCD CHOP	S27	-4 sine waves displayed (A,B,C and D)	
			Depress COMPARE	S22	-8 sine waves displayed, four possible to shift with POSITION A,B,C,D (R2,3,13,14)	
			Release COMPARE	S22		
8.3.	Single, Reset, Clear Not trig'd, Lock	No input signal	Depress A	S1		
			Depress A	S16		
			Depress DC	S2		
			Set TIME/DIV to 0,2ms	S10		
			Set AMPL/DIV to 20mV	S6	-NOT TRIG'D led is on	
		Sine wave signal 2kHz, 120mVp-p to A input			-NOT TRIG'D led extinguished -Sine wave 2kHz 6 div. displayed	
			Depress SINGLE	S18	-NOT TRIG'D led extinguished	
			Depress RESET	S19	-Fixed sine wave 2kHz, 6 div. displayed	
			Depress 0	S13	-Display remains unchanged	
			Depress RESET	S19	-NOT TRIG'D led is on; display unchanged	
		Square wave signal 2kHz, 120mVp-p to A input	Release 0	S13	-Fixed square wave 2kHz 6 div. displayed with switching on phenomena	
			Depress RESET	S19		
			Depress 0	S13		
			Depress CLEAR	S20	-NOT TRIG'D led is on; zero line displayed	
		Sine wave signal 2kHz, 120mVp-p to A input	Release 0	S13	-NOT TRIG'D led extinguished; sine wave 2kHz 6 div. displayed	

STEP	OBJECTIVE	INPUT SIGNAL	SETTINGS	REQUIREMENTS	MEASURING RESULTS
			Depress 0 S13		
			Depress CLEAR 2 X S20	-NOT TRIG'D led is on; screen is blank	
			Release 0 S13	-NOT TRIG'D led extinguished Sine wave 2kHz 6 div. displayed	
			Release SINGLE S18	-Sine wave 2kHz 6 div. displayed	
			Depress LOCK S21		
			Depress CLEAR S20	-Display remains unchanged, the display is only changed by: POWER ON; DISPLAY QUART; X=A,Y=B; SMOOTH; INTENS; FOCUS; TRACE ROT. -NOT TRIG'D led is on	
			Release LOCK S21		
8.4.	Display Quart, Off	Sine wave signal 2kHz, 120mVp-p to A input	Depress A S1		
			Depress A S16		
			Depress AUTO S2		
			Set TIME/DIV to 0,2ms S10		
			Set AMPL/DIV to 20mV S6	-Sine wave 2kHz, 6 div. displayed	
			Turn LEVEL R5	-Adjust triggerpoint at zero level	
			Depress DISPLAY QUART S23	-1 sine wave, positive part left, displayed -Led's on: oooooooo	
			Depress DISPLAY QUART S23	-1 sine wave, negative part left, displayed -Led's on: oooooooo	
			Depress DISPLAY QUART S23	-1 sine wave, positive part left, displayed -Led's on: oooooooo	
			Depress DISPLAY QUART S23	-1 sine wave, negative part left, displayed -Led's on: oooooooo	
			Depress DISPLAY QUART S23	-1 sine wave, positive part left, displayed -Led's on: oooooooo	
			Depress DISPLAY QUART S23	-1 sine wave, negative part left, displayed -Led's on: oooooooo	
			Depress DISPLAY QUART S23	-1 sine wave, positive part left, displayed -Led's on: oooooooo	
			Depress OFF S24	-Sine wave 2kHz 6 div. displayed -All Led's extinguished	
8.5.	Pretrigg, Off	Sine wave signal 250Hz, 120mVp-p to A input	Settings as 8.4.	-Positive slope starts at left screen centre	
			Depress PRETRIG S25	-Positive slope is shifted 2.5 div. -Led 1/4 blinks	
			Depress PRETRIG S25	-Positive slope is shifted 5 div. -Led 1/2 blinks	
			Depress PRETRIG S25	-Positive slope is shifted 7.5 div. -Led 3/4 blinks	
			Depress PRETRIG S25	-Positive slope is shifted 10 div. -Led 1/1 blinks	
			Depress OFF S24	-Positive slope starts at left screen centre -All Led's extinguished	

STEP	OBJECTIVE	INPUT SIGNAL	SETTINGS		REQUIREMENTS	MEASURING RESULTS
8.6.	X=A/Y=B mode	Sine wave signal 2kHz, 120mVp-p to A input	Depress CHOP	S1		
			Depress A	S16		
			Depress AUTO	S2		
			Set TIME/DIV to 0,2ms	S10		
			Set AMPL/DIV to 20mV	S6	-Sine wave 2kHz 6 div. + zero line displayed	
			Depress X=A/Y=B	S29	-Horizontal line displayed possible to shift with POSITION A and B hor. and vert. resp.	
			Set TIME/DIV to 100/us	S10	-Horizontal line displayed possible to shift with POSITION A and B hor. and vert. resp.	
		Sine wave signal 200kHz, 120mVp-p to A input	Set TIME/DIV to 2/us	S10	-Horizontal line displayed possible to shift with POSITION A and B hor. and vert. resp.	
			Release X=A/Y=B			
8.7.	Smooth	Sine wave signal 20kHz, 120mVp-p to A input	Depress ABCD CHOP	S27		
			Depress A	S16		
			Depress AUTO	S2		
			Set AMPL/DIV to 20mV	S6		
			Set TIME/DIV to 0,2ms	S10	-1 sine wave and 3 base lines displayed	
			Depress LOCK	S21		
			Pull X MAGN	S5	-Little lines (like the tail of a comet) are written between the displayed dots	
			Depress SMOOTH	S30	-Separate dots are disappeared and the amplitude decreases about 10%	
			Release LOCK	S21		
			Depress X MAGN	S5		
			Release SMOOTH	S30		
8.8.	Time/div, Ext	Marker pulses to A input 80mV, rep. time:	Depress A	S1		
			Depress A	S16		
			Depress DC	S2		
			Set AMPL/DIV to 20mV	S6		
			Set TIME/DIV to:	S10		
		0,2ms	0,2ms/div		-10 marker pulses displayed	
		0,5ms	0,5ms/div		-10 marker pulses displayed	
		1 ms	1 ms/div		-10 marker pulses displayed	
		2 ms	2 ms/div		-10 marker pulses displayed	
		5 ms	5 ms/div		-10 marker pulses displayed	
		10 ms	10 ms/div		-10 marker pulses displayed	
		20 ms	20 ms/div		-10 marker pulses displayed	
		50 ms	50 ms/div		-10 marker pulses displayed	
		0,1 s	0,1 s/div		-10 marker pulses displayed	
		0,2 s	0,2 s/div		-10 marker pulses displayed	
		0,5 s	0,5 s/div		-10 marker pulses displayed	
			Depress TIME/DIV	S26	-10 marker pulses displayed	
		1 s	1 s/div		-10 marker pulses displayed	
		2 s	2 s/div		-10 marker pulses displayed	
		5 s	5 s/div		-10 marker pulses displayed	
			Release TIME/DIV	S26		

STEP	OBJECTIVE	INPUT SIGNAL	SETTINGS		REQUIREMENTS	MEASURING RESULTS
		Marker pulses to A input 80mV, rep. time:	Set TIME/DIV to:	S10		
		0,1ms	100 /us/div		-10 marker pulses displayed	
		50 /us	50 /us/div		-10 marker pulses displayed	
		20 /us	20 /us/div		-10 marker pulses displayed	
		10 /us	10 /us/div		-10 marker pulses displayed	
		5 /us	5 /us/div		-10 marker pulses displayed	
		2 /us	2 /us/div		-10 marker pulses displayed	
		1 /us	1 /us/div		-10 marker pulses displayed	
		0,5/us	0,5/us/div		-10 marker pulses displayed	
		0,2/us	0,2/us/div		-10 marker pulses displayed	
		0,1/us	0,1/us/div		-10 marker pulses displayed	
					-REP ONLY Led is on	
		Marker pulses to A input 80mV, rep. time 0,2ms	Set TIME/DIV to 0,2ms	S10		
		TTL square wave, 1MHz to EXT CLOCK input			-10 marker pulses displayed	
					-20 marker pulses displayed TIME/DIV setting not operative	
		TTL square wave, 40Hz to EXT CLOCK input				
		Marker pulses to A input 80mV, rep. time 5s			-20 marker pulses displayed, TAKE CARE: trace is built up in about 100s	
		TTL square wave, 20Hz to EXT CLOCK input	Depress TIME/DIV	S26		
			Set TIME/DIV to 0,5s	S10	-10 marker pulses displayed, TAKE CARE: trace is built up in about 50s	
8.9.	Min/Max		Depress A	S1		
			Depress A	S16		
			Depress DC	S2		
			Set AMPL/DIV to 20mV	S6		
			Set TIME/DIV to 5ms	S10		
			Depress MIN/MAX	S28	-Zero line displayed	
			Depress CHOP	S1	-Two zero lines displayed	
		Positive pulses, width 10ns, rep. time 5ms amplitude 120mV	Depress A	S1		
					-10 positive pulses, amplitude 3 div. displayed	
		Negative pulses, width 10ns, rep. time 5ms amplitude 120mV				
					-10 negative pulses, amplitude 3 div. displayed	
			Release MIN/MAX	S28		
8.10.	Dual Slope triggering	Sine wave signal 2kHz 120mVp-p to A input	Depress A	S1		
			Depress A	S16		
			Depress AUTO	S2		
			Set AMPL/DIV to 20mV	S6		
			Pull PULL FOR DUAL SLOPE	S32	-Sine wave random triggered on positive or negative going slope	
			Depress PULL FOR DUAL SLOPE			

PHILIPS

6. CHECKING AND ADJUSTING

6.1. GENERAL INFORMATION

The following information provides the complete checking and adjusting procedure for the instrument. As various control functions are interdependent, a certain order of adjustment is necessary.
The procedure is, therefore, presented in a sequence which is best suited to this order, cross-reference being made to any circuit which may affect a particular adjustment.
Before any check or adjustment, the instrument must attain its normal operating temperature.

- Warming-up time under average conditions is 30 minutes.
- Where possible, instrument performance should be checked before any adjustment is made.
- All limits and tolerances given in this Section are calibration guides, and should not be interpreted as instrument specifications unless they are also published in Section 2.
- Tolerances given are for the instrument under test and do not include test equipment error.
- The most accurate display adjustments are made with a stable, well-focused low intensity display.
- All controls which are mentioned without item numbers are located on the outside of the instrument.

6.2. SURVEY OF ADJUSTING ELEMENTS AND AUXILIARY EQUIPMENT

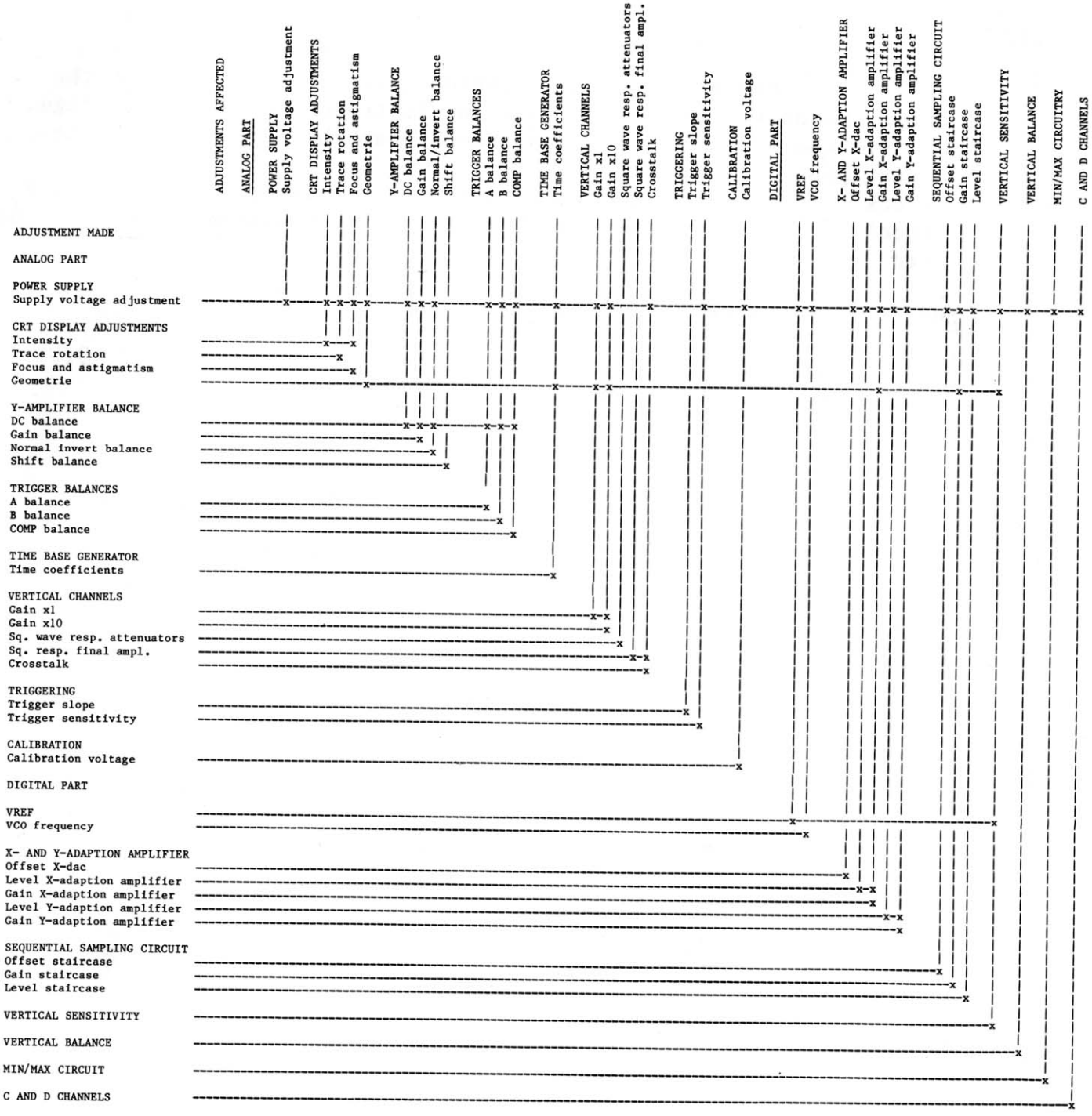
ADJUSTMENT	ADJUSTING ELEMENT	ADJUSTING RESULT	RECOMMENDED INSTRUMENT AND INPUT SIGNALS	CHAPTER	FIGURES
Power supply				6.4.	
Supply voltage adjustment	R204	12V ±0,025V across C224	Digital multimeter	6.4.2.	6.1.
Cathode-ray tube circuit				6.5.	
Intensity	R1534	Spot just visible (INTENS 90° from left stop)	-	6.5.1.	6.2.
Trace rotation	R10	Trace in parallel with horizontal graticule lines	-	6.5.2.	
Focus and astigmatism	R1543	Sharp and well difined trace	Function generator, sine wave 10kHz	6.5.3.	6.1.
Geometrie	R1549	Displayed lines as straight as possible	Function generator, sine wave 10kHz	6.5.4.	6.1.
ANALOG ADJUSTINGS				6.6.	
Y-Amplifier balance				6.6.1.	
DC balance	R504(R604)	Minimum jump when switching between 10 and 20mV	-	6.6.1.2.	6.2.
Gain balance	R514(R614)	Minimum jump when rotating AMPL/DIV control	-	6.6.1.3.	6.2.
Normal/invert balance B	R647	Minimum jump when switching normal/invert	-	6.6.1.4.	6.2.
Shift balance	R547(R674)	Signal displayed distorsion-free when rotating the POSITION control	Function generator, sine wave 10kHz	6.6.1.5.	6.2.
Trigger balances				6.6.2.	
A balance	R356	Spot situated at screen-centre	-	6.6.2.	6.3.
B balance	R361	Spot situated at screen-centre	-	6.6.2.	6.3.
COMP balance	R358	Spot situated at screen-centre	-	6.6.2.	6.3.
Time base generator				6.6.3.	
Time coefficients	R1417	Centre 8 cycles at 8 div.	Time marker generator: 1 /us	6.6.3.	6.2.
	R1419	Centre 8 cycles at 8 div.	Time marker generator: 0,1/us	6.6.3.	6.2.
	R1232	Centre 8 cycles at 8 div.	Time marker generator: 1 ms	6.6.3.	6.2.
	C1409	Start of sweep lineair in MAGN	Time marker generator: 1 ns	6.6.3.	6.2.

ADJUSTMENT	ADJUSTING ELEMENT	ADJUSTING RESULT	RECOMMENDED INSTRUMENT AND INPUT SIGNALS	CHAPTER	FIGURES
Vertical channels				6.6.4.	
Gain sensitivity x1 A(B)	R848(R543)	Amplitude 6 div.	Function generator, square wave signal 2kHz	6.6.4.2.	6.2.
Gain sensitivity x10 A(B)	R621(R521)	Amplitude 6 div.	Function generator, square wave signal 2kHz	6.6.4.2.	6.2.
Square wave response attenuators	C407(C307) C413(C313) C414(C314) C416+C418 (C316+C318) C417+C419 (C317+C319)	Optimal square-wave response pulse-top errors $\pm$0,1div. Trace height 6div. $\pm$0,1div.	Square wave calibration generator frequency 10kHz, rise time $\leq$100ns, amplitude for 6 div. display	6.6.4.3.	6.3.
Square wave response final amplifier	R813 R812 R814 C809 C811 R817 L801 L802 C607(507) C818	Optimal square wave response freq: 10kHz pulse top errors $\pm$0,1div. 100kHz Trace height 6 div. $\pm$0,1div. 100kHz 100kHz 100kHz 1MHz 1MHz 1MHz 1MHz 1MHz	Square wave calibration generator frequency 10kHz...1MHz, rise time $\leq$1ns, amplitude for 6 div. display	6.6.4.4.	6.2./6.4.
Cross talk	R813	Minimum cross talk	Square wave calibration generator frequency 10kHz, rise time $\leq$1ns	6.6.4.5.	6.2.
Triggering					
Trigger slope	R1014	Output at collector V1014 unchanged when operating the SLOPE switch	-	6.6.5.1.	6.2.
Trigger sensitivity	R1041	Lowest signal with a triggered trace	Function generator sine wave 2kHz	6.6.5.2.	6.2.
Calibration					
Calibration voltage	R1607	Square wave voltage 1,2Vp-p $\pm$1%, 2kHz approx.	-	6.6.7.	6.2.

DIGITAL ADJUSTINGS

ADJUSTMENT	ADJUSTING ELEMENT	ADJUSTING RESULT	RECOMMENDED INSTRUMENT AND INPUT SIGNALS	CHAPTER	FIGURES
VREF	R2086	-0,5V ±2,5mV at testpoint VREF	Digital multimeter	6.7.	6.5.
VCO frequency	R2044	20MHz at pin 5 of D2098	Digital counter	6.7.	6.5.
X- and Y-adaption amplifier				6.7.1.	
Offset X-dac	R2052	Smoothed sine wave	Function generator, sine wave 2kHz	6.7.1.1.	6.5.
Level X-adaption amplifier	R1771	Minimum shift when operating MEMORY ON	Time marker generator, 1ms markers	6.7.1.2.	6.6.
Gain X-adaption amplifier	R1784	Centre 8 markers at 8 div.	Time marker generator, 1ms markers	6.7.1.2.	6.6.
Level Y-adaption amplifier	R1728	Zero line at screen-centre	Function generator, sine wave 2kHz	6.7.1.3.	6.6.
Gain Y-adaption amplifier	R1738	Dynamic range 10 div.	Function generator, sine wave 2kHz		
Sequential sampling circuit				6.7.2.	
Offset staircase	R2036	Smoothed sine wave with X MAGN pulled	Function generator, sine wave 50kHz	6.7.2.1.	6.5.
Gain staircase	R2033	Centre 8 markers at 8 div.	Time marker generator, 1/us markers	6.7.2.2.	6.5.
Level staircase	R2034	Starting point 0,2 div. out of screen	Function generator, sine wave 1MHz	6.7.2.2.	6.5.
Square wave response	C2152	Best square wave performance	Function generator, square wave 1MHz	6.7.2.3.	6.5.
Vertical sensitivity	R2512	6 div. amplitude	Function generator, square wave 500Hz	6.7.4.	6.7.
Vertical balance	R2638	Trace jump ≤0,1 div. when operating MEMORY ON	Function generator, square wave 500Hz	6.7.4.	6.7.
MIN/MAX circuit adjusting	R2642	Sharp line displayed	-	6.7.6.	6.7.
	R2534	Trace jump ≤ 0,1 div. when operating MIN/MAX	-	6.7.6.	6.7.
	R2567	Sharp line displayed	-	6.7.6.	6.7.
	R2598	Sharp line displayed	-	6.7.6.	6.7.
C and D channel adjusting	R2324	6 div. amplitude	Square wave calibration generator, 2kHz	6.7.7.	6.8.
	R2374	6 div. amplitude	Square wave calibration generator, 2kHz	6.7.7.	6.8.

6.3. INTERACTION TABLE



AMPLIFIER UNIT A5

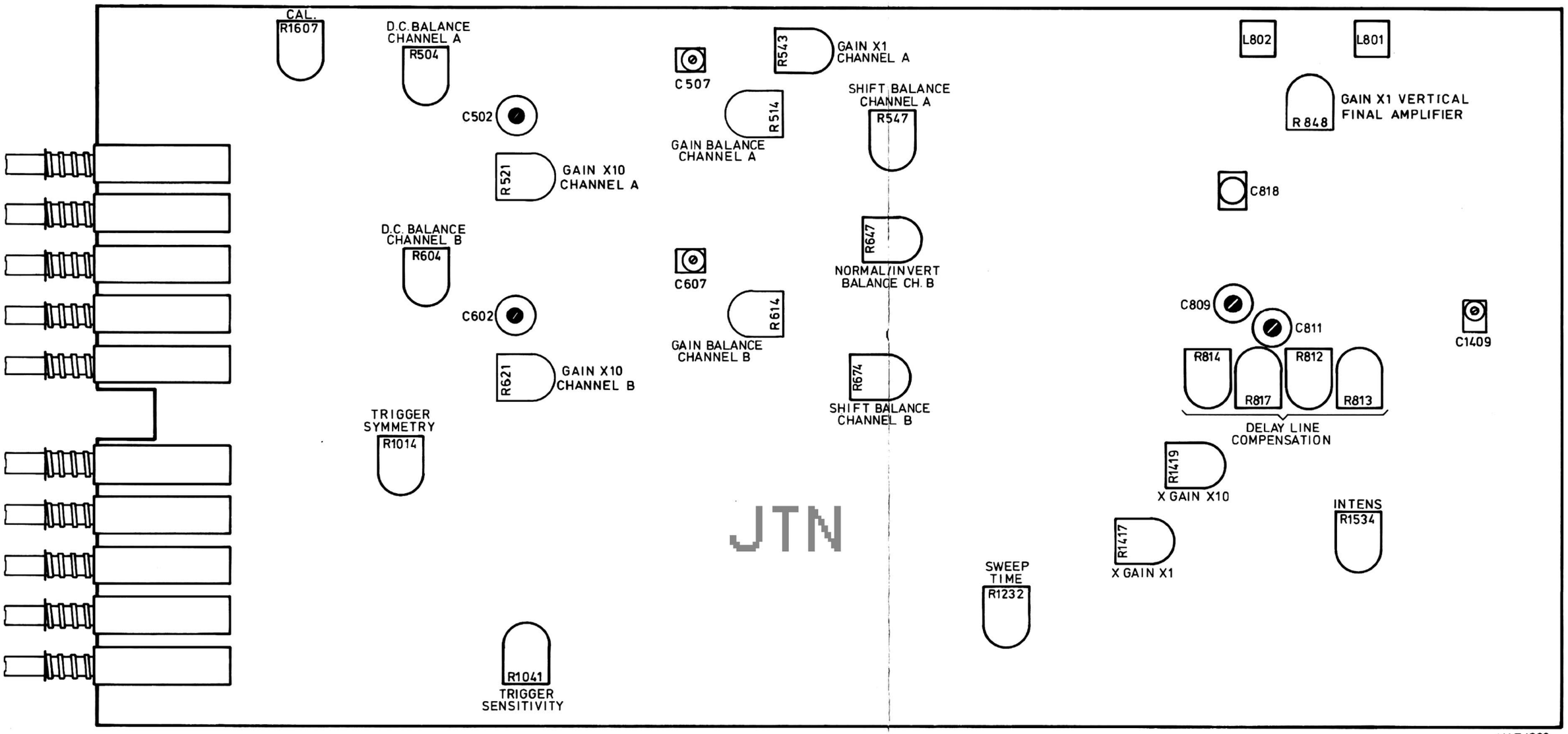


FIG. 6.2. Adjusting elements amplifier board A5.

6.4. POWER SUPPLY ADJUSTINGS

6.4.1. Mains current

- Check that the mains voltage adapter (S101) has been set to the local mains voltage and connect the instrument to such a voltage.
- Switch the oscilloscope on and check that the pilot lamp on the front panel lights up.
- Check that the current consumption does not exceed 310 mA at 220V local mains and 300 mA at 117V local mains. (Measured with a moving iron meter.)

6.4.2. Supply voltages (R204, Fig. 6.1.)

- Check that the voltage across capacitor C224 is +12V, + or -0,035V; if necessary readjust potentiometer R204.

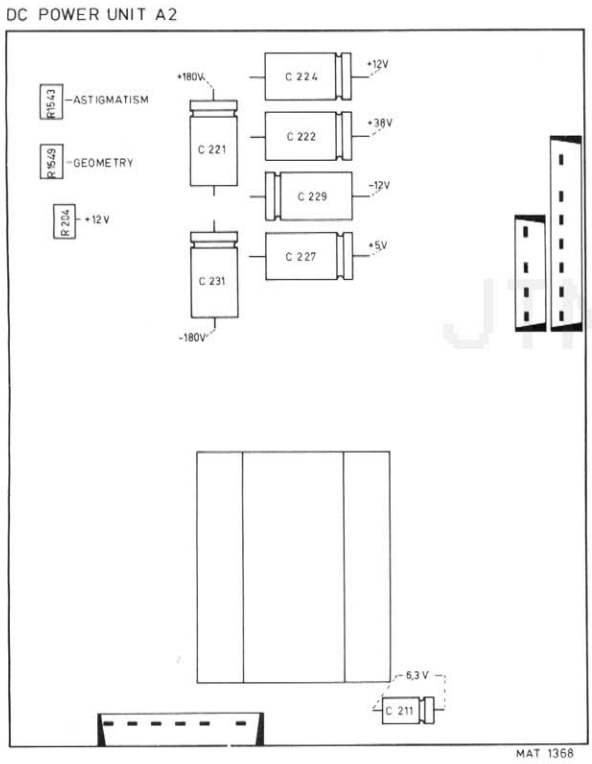


FIG. 6.1. Adjusting and checking the power supply.

- Check the supply voltages in accordance with the following table:

Voltage across:	Required value:	Max. allowable ripple
C227	+ 5V, ± 0,2V	≤ 2 mV p-p
C224	+ 12V, ± 0,25V	≤ 4 mV p-p
C229	- 12V, ± 0,25V	≤ 4 mV p-p
C222	+ 38V, ± 2V	≤ 40 mV p-p
C231	-180V, ± 9V	≤ 1 V p-p
C221	+180V, ± 9V	≤ 1 V p-p
C211	6,3V, ± 0,6V	

POWER UP ROUTINE
Check the power up routine (section 7.7.1.).

6.5. CATHODE-RAY-TUBE-CIRCUIT ADJUSTINGS

6.5.1. Intensity (R1534, Fig. 6.2.)

- Depress pushbutton A of the display mode switch S1.
- Set TIME/DIV switch S10 to position EXT X DEFL.
- Depress pushbutton EXT of the trigger source selector switch S16.
- Set A POSITION potentiometer R2 and X POSITION potentiometer R4 to their mid-positions.
- Set INTENS potentiometer R1 to 90° from its left hand stop.
- Adjust potentiometer R1534 in such a way that the spot is just visible.

6.5.2. Trace rotation (R10)

- Depress pushbutton AUTO of the trigger mode switch S2.
- Set TIME/DIV switch S10 to 100 µs/div.
- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress the input coupling switch S13 (0).
- Center the time-base line using A POSITION potentiometer R2.
- Check that the time-base line runs exactly in parallel with the horizontal lines of the graticule.
  If necessary, readjust front panel TRACE ROTATION screwdriver potentiometer R10.

6.5.3. Focus and astigmatism (R1543, Fig. 6.1.)

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress the input coupling switch S12 (AC).
- Release the input coupling switch S13 (0).
- Set A AMPL/DIV switch S6 to 0,1V/div. and A AMPL/DIV potentiometer R7 to CAL.
- Set TIME/DIV switch S10 to 50 µs/div. and TIME/DIV potentiometer R9 to CAL.
- Apply a sine-wave voltage of approx. 600 mVp-p, 10 kHz, to the A input socket X2.
- Set INTENS potentiometer R1 for normal brightness.

  Use an insulated screwdriver.

- Adjust FOCUS potentiometer R6 and astigmatism potentiometer R1543 for a sharp and well-defined trace.

6.5.4. Geometry (R1549, Fig. 6.1.)

- Set the controls as in the previous section.
- Set A AMPL/DIV switch S6 to 5 mV/div. and A AMPL/DIV potentiometer R7 to CAL.
- Apply a sine-wave voltage of approx. 600 mVp-p, 10 kHz, to the A input socket X2.

  Use an insulated screwdriver.

- Check that the displayed vertical lines are as straight as possible.
  If necessary readjust potentiometer R1549.

6.6. ADJUSTING AND CHECKING OF THE ANALOG OSCILLOSCOPE PART

6.6.1. Y-amplifier balance

6.6.1.1. General information

The adjustments of the vertical amplifier channels A and B are identical. The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.

6.6.1.2. D.C. balance (R504, R604, Fig. 6.2.)

- Depress pushbutton A (B) of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress the input coupling switch S13 (S15) (0).
- Set AMPL/DIV potentiometer R7 (R8) to CAL.
- Centre the trace using A (B) potentiometer R2 (R3).
- Check that the trace does not jump if AMPL/DIV switch S6 (S8) is switched from 10 mV/div. to 20 mV/div.
  If necessary, adjust potentiometer R504 (R604) for minimum jump.
- Repeat the measurement for channel B.

6.6.1.3. Gain balance (R514,R614, Fig. 6.2.)

- Depress pushbutton A (B) of the display mode switch S1.
- Depress the input coupling switch S13 (S15) 0.
- Check that the trace does not move when the AMPL/DIV potentiometer R7 (R8) is rotated.
  If necessary readjust R514 (R614).
- Repeat the measurement for channel B.

6.6.1.4. Normal/invert balance channel B (R647, Fig. 6.2.)

- Depress pushbutton B of the display mode switch S1.
- Depress the input coupling switch S15 (0).
- Check that the trace does not jump when PULL TO INVERT B switch S4 is switched between normal and invert.
  If necessary readjust R647 for minimum jump.

6.6.1.5. Shift balance (R547,R674, Fig. 6.2.)

- Depress pushbutton A (B) of the display mode switch S1.
- Depress pushbutton A (B) of the trigger source selector switch S16.
- Depress the input coupling switch S12 (S14) (AC).
- Release the input coupling switch S13 (S15) (0).
- Set the AMPL/DIV switch S6 (S8) to 20 mV/div. and AMPL/DIV potentiometer R7 (R8) to CAL.
- Set the TIME/DIV switch S10 to 50 µs/div. and TIME/DIV potentiometer R9 to CAL.
- Apply a sine-wave voltage of 480 mVp-p, 10 kHz, to the A (B) input socket.
- Check if the extremes of the sine-wave can be displayed distortion free on the screen by rotating the POSITION potentiometer R2 (R3).
  If necessary readjust potentiometer R547 (R674).
- Repeat the measurement for channel B.

6.6.2. Trigger balance (R356, R358, R361, Fig. 6.3.)

- Depress pushbutton A of the display mode switch S1.
- Depress the input coupling switch S13 (0).
- Set X MAGN switch S5 to position x1.
- Set TIME/DIV switch S10 to 100/us/div. and TIME/DIV potentiometer R9 to CAL.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set X POSITION potentiometer R4 in such a way that the time base line starts at the most left graticule line.
- Set TIME/DIV switch S10 to X DEFL.
- Reduce the intensity
- Depress pushbutton EXT of the trigger source selector switch S16.
- Check that the spot lies in the center of the screen; tol. 2 div.
- Set the X POSITION potentiometer R4 so that the spot is situated in the centre of the screen.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress pushbutton DC of the trigger mode switch S2.
- Check that the spot lies in the center of the screen.
  If necessary readjust potentiometer R356.
- Depress pushbutton B of the trigger source selector switch S16.
- Check that the spot lies in the center of the screen.
  If necessary readjust potentiometer R361.
- Depress both A and B pushbuttons (composite) of the trigger source selector switch S16.
- Shift the spot to the central horizontal graticule line using A POSITION potentiometer R2.
- Check that the spot lies in the center of the screen.
  If necessary readjust potentiometer R358.

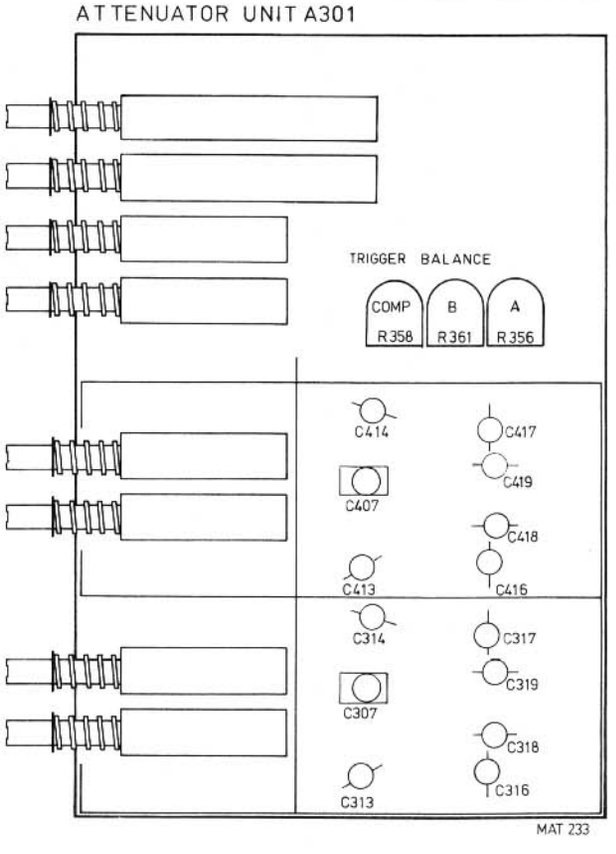


Fig. 6.3. Adjusting elements attenuator board.

6.6.3. Time coefficients and sweep linearity (R1417, R1419, R1232, C1409) (Fig. 6.2.)

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set X MAGN switch S5 to position x1.
- Set A AMPL/DIV switch S6 to 20 mV/div.
- Release the input coupling switch S13 (0).
- Depress pushbutton A of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 1 /us/div. and TIME/DIV potentiometer R9 to CAL.
- Apply a time marker voltage with repetition time of 1 /us and an amplitude of 80 mVp-p to the A input socket X2.
- Check that the central 8 cycles occupy 8 divisions.
  If necessary readjust potentiometer R1417.
- Pull X MAGN switch S5 to position x10.
- Change the repetition time of the applied input signal to 0,1 /us.
- Check that the central 8 cycles occupy 8 divisions.
  If necessary readjust potentiometer R1419.
- Check that the trace can be shifted over 100 divisions with the aid of X POSITION potentiometer R4.
- Set TIME/DIV switch S10 to 0,1 /us/div.
- Apply a pulse of 10 ns to the A input socket X2.
- Turn X POSITION potentiometer R4 fully clockwise.
- Check that the start of the trace is linear.
  If necessary readjust C1409.
- Turn X POSITION potentiometer R4 in its midposition and check that the start of the trace is still linear.
- Set X MAGN switch S5 to position x1.
- Set TIME/DIV switch S10 to 1 ms/div.
- Change the repetition time of the applied input signal to 1 ms.
- Check that the central 8 cycles occupy 8 divisions.
  If necessary readjust potentiometer R1232.
- Check all the other positions of the TIME/DIV switch S10. The repetition time of the applied input signal should correspond to the position of the TIME/DIV switch S10.
  The central 8 cycles should always occupy 8 divisions: tolerance ± 1 subdivision (2 subdivisions with X MAGN switch S5 to position x10).
- Check that in all the positions of the TIME/DIV switch S10 the time-base length is at least 10 divisions.
- Check the control range of the TIME/DIV potentiometer R9 in the position 100/us/div. of the TIME/DIV switch S10.
  This should be: 1 : $\geq$ 2,5.

6.6.3.1. Hold off check

- Set the TIME/DIV switch S10 to 2 /us/div.
- Turn R12 (HOLD OFF) counter clockwise and check that the display blinks.
- Turn R12 (HOLD OFF) clockwise in the CAL position and check that a bright line is displayed.

6.6.4. Vertical amplifiers

6.6.4.1. General information

The adjustments of the vertical amplifier channels A and B are identical. The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.

6.6.4.2. Deflection sensitivity (gain)

The adjustments of the vertical amplifier sensitivity must follow the specified sequence.

Channel B	x1	Gain	(R848)
Channel A	x1	Gain	(R543)
Channel B	x10	Gain	(R621)
Channel A	x10	Gain	(R521)

Deflection sensitivity x1 (R848,R543, Fig. 6.2.)

- Depress pushbutton B (A) of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress pushbutton B (A) of the trigger source selector switch S16.
- Set AMPL/DIV potentiometer R8 (R7) to CAL.
- Release input coupling switch S14 (S12) (DC).
- Release input coupling switch S15 (S13) (0).
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Set AMPL/DIV switch S8 (S6) to 20 mV/div.
- Apply a square-wave voltage of 120 mV, frequency approx. 2 kHz, to the B (A) input socket X3 (X2).
- Check that the signal occupies 6 divisions.
  If necessary readjust potentiometer R848 (R543).
- Repeat the measurement for channel A.

Deflection sensitivity x10 (R621, R521, Fig. 6.2.)

- Depress pushbutton B (A) of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress pushbutton B (A) of the trigger source selector switch S16.
- Set AMPL/DIV potentiometer R8 (R7) to CAL.
- Release input coupling switch S14 (S12) (DC).
- Release input coupling switch S15 (S13) (0).
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Set AMPL/DIV switch S8 (S6) to 2 mV/div.
- Apply a square-wave voltage of 12 mVp-p, frequency approx. 2 kHz, to the B (A) input socket.
- Check that the signal occupies 6 divisions.
  If necessary readjust R621 (R521).

Repeat the measurement for channel A.

6.6.4.3. Input attenuators (Fig. 6.3.)

- Depress pushbutton A (B) of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress pushbutton A (B) of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 0,2 ms and the TIME/DIV potentiometer R9 to CAL.
- Release input coupling switch S12 (S14) (DC).
- Release input coupling switch S13 (S15) (0).
- Set AMPL/DIV potentiometer R7 (R8) to CAL.
- Apply a square-wave voltage with an amplitude as indicated in the following table, a repetition rate of approx. 2 kHz and a rise time $\leq$ 100 ns, to the A (B) input socket.
- Check that no overshoot is visible (max. pulse top errors 2 %), and check that the trace height is 6 divisions $\pm$ 3 % (1 subdivision).

S6 (S8) ampl. to	Input signal	Adjust with
20 mV	120 mV	C307 (C407)
50 mV	0,3 V	C313 (C413)
0,1 V	0,6 V	C314 (C414)
0,2 V	1,2 V	C316+C318 (C416+C418)
2 V	12 V	C317+C319 (C417+C419)

Repeat the measurement for channel B.

6.6.4.4. Square-wave response final amplifier (Fig. 6.2.)

- Depress pushbutton B of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress pushbutton B of the trigger source selector switch S16.
- Push NORMAL/INVERT switch S4 to position NORMAL.
- Set B AMPL/DIV switch S8 to 20 mV/div. and B AMPL/DIV potentiometer R8 to CAL.
- Apply a square-wave voltage of approx. 120 mVp-p, with rise time $\leq$ 3 ns, to the B input socket. The pulse repetition should be in accordance with the table below.
- Check the square-wave response, pulse top errors may not exceed 1 subdivision.
- Check that the rise time does not exceed 10 ns.

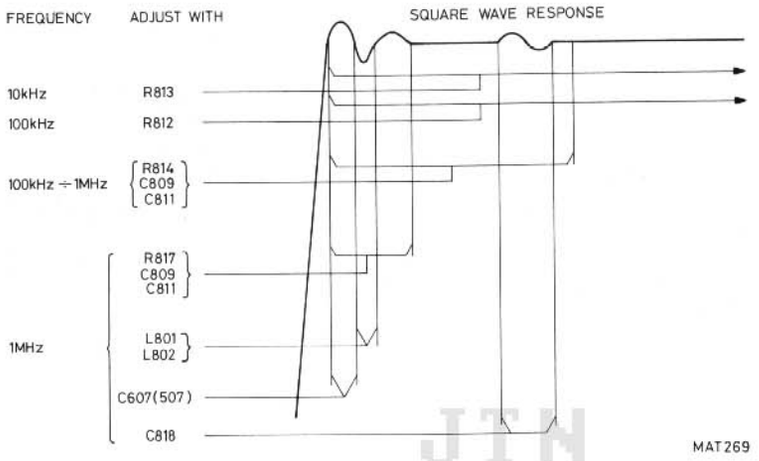


Fig. 6.4. Adjusting the square wave response

* L801 and L802 should be operated simultaneously and in the same direction and by the same amount.
  If necessary repeat above adjustments until the best response is obtained.

- Check and readjust the square-wave response according to the table below.

Channel	Ampl/div.	Input signal	Trace height	Rep.rate	Time/div	Adjust with	Max. error
B	2 mV/div.	12 mV	6 div.	1 MHz	0,2 µs	C602/606	1 subdiv.
A	20 mV/div.	120 mV	6 div.	1 MHz	0,2 µs	C507	1 subdiv.
A	2 mV/div.	12 mV	6 div.	1 MHz	0,2 µs	C502/506	1 subdiv.
B	2 mV/div.	12 mV	6 div.	1 MHz	0,2 µs	C606**	1 subdiv.
A	2 mV/div.	12 mV	6 div.	1 MHz	0,2 µs	C506**	1 subdiv.

** C506 and C606 may have a value of 0...15 pF.

6.6.4.5. Cross talk (R813, Fig. 6.2.)

- Depress pushbutton CHOP of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress pushbutton B of the trigger source selector switch S16.
- Push NORMAL/INVERT switch S4 to position NORMAL.
- Set A and B AMPL/DIV switches S6 and S8 to 20 mV/div. and the AMPL/DIV potentiometer R7 and R8 to CAL.
- Set the TIME/DIV switch S10 to 0,5 ms/div. and the TIME/DIV poten tiometer R9 to CAL.
- Depress the input coupling switch S13 (0).
- Apply a square-wave voltage of 120 mVp-p, rise time $\leq$ 3ns and a repetition rate of approx. 10 kHz to the B input socket.
- Adjust potentiometer R813 for minimum cross talk between both channels.

6.6.4.6. Bandwidth check of channel A(B)

- Depress pushbutton A(B) of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress pushbutton A(B) of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 100 µs/div. and the TIME/DIV potentiometer R9 to CAL.
- Set AMPL/DIV switch S6 (S8) to 2 mV/div. and AMPL/DIV potentiometer R7 (R8) to CAL.
- Release input coupling switch S12 (S14) (DC).
- Release input coupling switch S13 (S15) (0).
- Apply a sine-wave signal of 12 mVp-p, frequency aprox. 100 kHz to the A (B) input socket.
- Increase the frequency of the input signal to 35 MHz, the amplitude of the signal must remain 12 mV.
- Check that the trace height is at least 4,2 divisions at an input frequency of 35 MHz.

Repeat the measurement for channel B.

6.6.5. Triggering

6.6.5.1. Trigger slope (R1014, Fig. 6.2.)

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress input coupling switch S13 (0).
- Set LEVEL potentiometer R5 to its midposition.
- Check with a multimeter that the DC output voltage of the trigger amplifier (collector of V1014) does not change if SLOPE pushbutton S3 is switched between + and -.
  If necessary readjust potentiometer R1014.
- Set AMPL/DIV switch S6 to 20 mV/div. and AMPL/DIV potentiometer R7 to CAL.
- Release input coupling switch S12 to (DC).
- Release input coupling switch S13 (0).
- Apply a sine-wave signal of 120 mVp-p, frequency approx. 2 kHz, to the A input socket.
- Release SLOPE switch S3 to the + position and check that the trace starts with a positive going edge.
- Depress SLOPE switch S3 to the - position and check that the trace starts with a negative going edge.

6.6.5.2. Trigger sensitivity (R1041, Fig. 6.2.)

- Set the controls as in the previous section.
- Depress AC of trigger mode switch S2.
- Apply a sine-wave signal of 12 mVp-p, frequency approx. 2 kHz to the A input socket.
- Set the LEVEL potentiometer R5 to mid position.
- Check that the trace is triggered, if necessary readjust R1041

6.6.5.3. Trigger level internal DC

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton DC of the trigger mode selector switch S2.
- Depress pushbutton A of the trigger source selector switch S16.
- Apply a sine-wave signal for a trace height equivalent of 12 divisions to the A input socket X2.
- Check that the starting point of the sine-wave can be shifted between + 6 and - 6 divisions with the aid of LEVEL potentiometer R5.
- Enlarge the vertical deflection to 16 divisions and check that the level range of R5 does not exceed 16 divisions.

6.6.5.4. Trigger level auto

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress pushbutton A of the trigger source selector switch S16.
- Release input coupling switch S13 (0).
- Apply a sine-wave voltage at a frequency of approx. 100 Hz for 6 divisions trace height to the A input socket.
- Check that the starting point of the sine-wave can be shifted across approx. 3 divisions with the aid of LEVEL potentiometer R5.

6.6.5.5. Trigger level external

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton AC of the trigger mode switch S2.
- Depress pushbutton EXT of the trigger source selector switch S16.
- Release input coupling switch S12 (DC).
- Release input coupling switch S13 (0).
- Set A AMPL/DIV switch S6 to 1 V/div. and A AMPL/DIV potentiometer R7 to CAL.
- Set TIME/DIV switch S10 to 0,2 ms/div. and TIME/DIV potentiometer R9 to CAL.
- Apply a sine-wave signal of 1,2 Vp-p, frequency approx. 2 kHz to the A and EXT input sockets.
- Check that the starting point of the sine-wave can be shifted across the entire amplitude of the signal with the aid of LEVEL potentiometer R5.

6.6.5.6. Trigger level external ÷ 10

- Set the controls as in the preveous section.
- Depress EXT ÷ 10 of the trigger source selector switch S16.
- Apply a sine wave of 12 Vp-p, frequency approx. 2 kHz to the A and EXT input sockets.
- Check that the starting point of the sine-wave can be shifted across the entire amplitude of the signal with the aid of LEVEL potentiometer R5.

6.6.5.7. Trigger sensitivities.

- Check the trigger sensitivity in accordance with the table below or better.

Trigger source	Trigger mode	+/-	Trace ampl.	Signal to	Freq.	Shape	Ampl. input voltage
A	Auto	+	0,7 div.	X2(YA)	100 Hz	Sine	14 mVp-p
A	Auto		0,7 div.	X2(YA)	10 kHz	Sine	14 mVp-p
A	Auto		1 div.	X2(YA)	35 MHz	Sine	20 mVp-p
A	AC		0,7 div.	X2(YA)	20 Hz	Sine	14 mVp-p
A	AC		1 div.	X2(YA)	35 MHz	Sine	20 mVp-p
A	DC		1 div.	X2(YA)	35 MHz	Sine	20 mVp-p
B	DC		0,7 div.	X3(YB)	20 Hz	Sine	14 mVp-p
B	DC		1 div.	X3(YB)	35 MHz	Sine	20 mVp-p
A+B	DC		1 div.	X3(YB)	35 MHz	Sine	20 mVp-p
A+B (comp) (S1 - ALT)	DC			X2(YA) X3(YB)	± 2 kHz ± 2 kHz	Square* Sine*	± 20 mVp-p ± 20 mVp-p
B	TV	+	0,7 div. Sync. pulse	X3(YB)		+ Video	14 mVp-p Sync. pulse
B	TV	-	0,7 div. Sync. pulse	X3(YB)		- Video	14 mVp-p Sync. pulse
B	TV	-	± 2 div. Sync. pulse	X3(YB)		- Video	± 40 mVp-p Sync. pulse
EXT	DC		140 mV	X4(EXT)	20 Hz 35 MHz	Sine Sine	140 mVp-p 140 mVp-p
EXT ÷10	DC		1,4 V	X4(EXT)	20 Hz 35 MHz	Sine Sine	1,4 Vp-p 1,4 Vp-p

* Originating from different sources!

- Set LEVEL potentiometer R5 as required.
- Set TIME/DIV switch S10 to such a position that a reasonable number sine-waves is displayed.
- Set A and B AMPL/DIV switches S6 and S8 to 20 mV/div. and the A and B AMPL/DIV potentiometers R7 and R8 to CAL.

6.6.5.8. Triggering on the line frequency

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress pushbutton B of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 5 ms/div. and TIME/DIV potentiometer R9 to CAL.
- Set A AMPL/DIV switch S6 to 20 mV/div. and A AMPL/DIV potentiometer R7 to CAL.
- Release input coupling switch S12 (DC).
- Release input coupling switch S13 (0).
- Apply a signal of approx. 10 mVp-p at the mains frequency to the A input socket.
  The trace is not triggered.
- Depress pushbutton LINE (EXT + EXT ÷ 10) of the trigger source selector switch S16 and check that the trace is triggered.

6.6.6. X Deflection

6.6.6.1. Sensitivity

- Set TIME/DIV switch S10 to X DEFL.
- Depress pushbutton EXT (EXT ÷10) of the trigger source selector switch S16.
- Apply a sine-wave voltage of 1,6 (16) Vp-p frequency approx. 2 kHz to the EXT input socket.
- Check that the trace length is 8 divisions $\pm$ 1 division.

6.6.6.2. Frequency response

- Set TIME/DIV switch S10 to X DEFL.
- Depress pushbutton EXT of the trigger source selector switch S16.
- Apply a sine-wave voltage of 16 Vp-p (trace length 8 divisions), frequency approx. 10 kHz, to the EXT input socket.
- Increase the frequency to 1 MHz.
- Check that the trace length is at least 5,6 divisions.

6.6.6.3. X Deflection with a line signal.

- Set TIME/DIV switch S10 to X DEFL.
- Depress pushbuttons LINE (EXT + EXT ÷ 10) of the trigger source selector switch S16.
- Check that the trace length is $\geq$8 divisions.

6.6.6.4. Horizontal sensitivity via input A

- Set A AMPL/DIV switch S6 to 20 mV/div. and A AMPL/DIV potentiometer R7 to CAL.
- Depress pushbutton B of display mode switch S1.
- Set TIME/DIV switch S10 to X DEFL.
- Depress pushbutton A of the trigger source selector switch S16.
- Apply a sine-wave voltage of 120 mVp-p, frequency approx. 2 kHz, to the A input socket.
- Check that the trace length is 6 divisions $\pm$ 0,6 division.

LOGIC UNIT A11

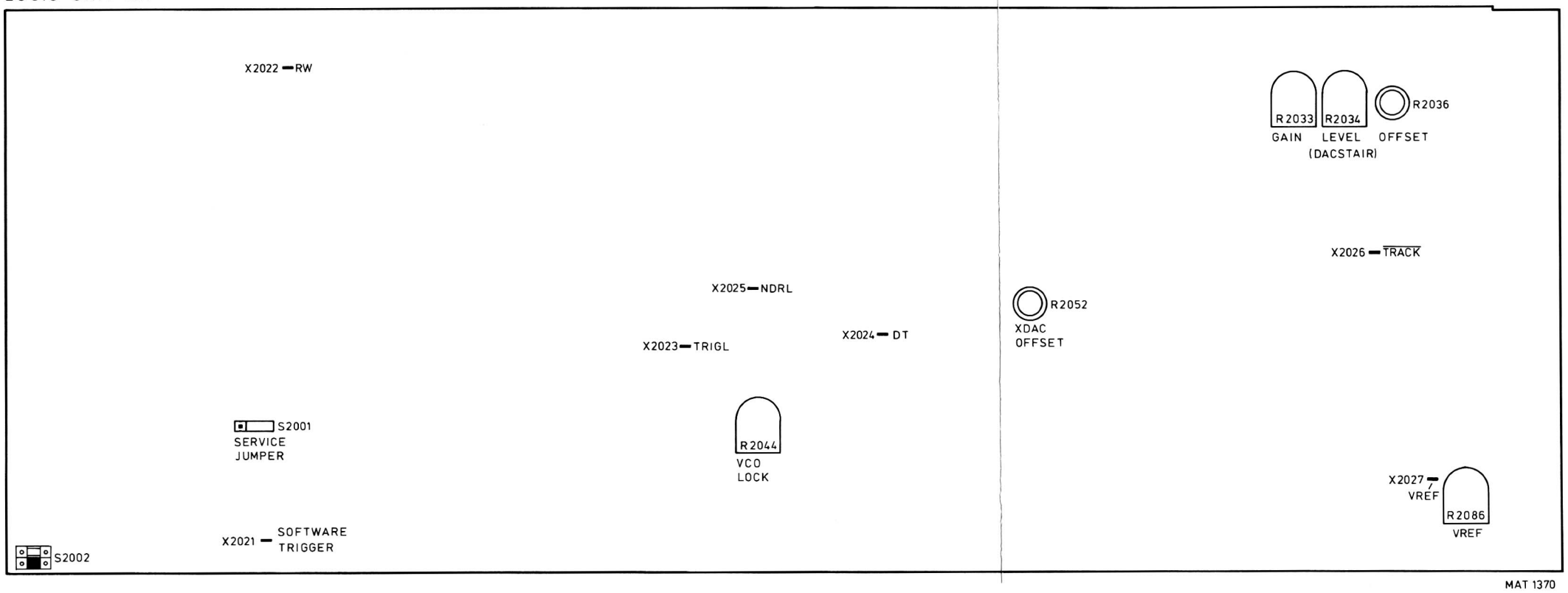


FIG. 6.5. Adjusting elements logic unit A11.

AUXILIARY CHANNEL UNIT A12

T&H UNIT A1103

FIG. 6.8. Adjusting elements AUX. channel unit A12.

ADAPTION UNIT A9

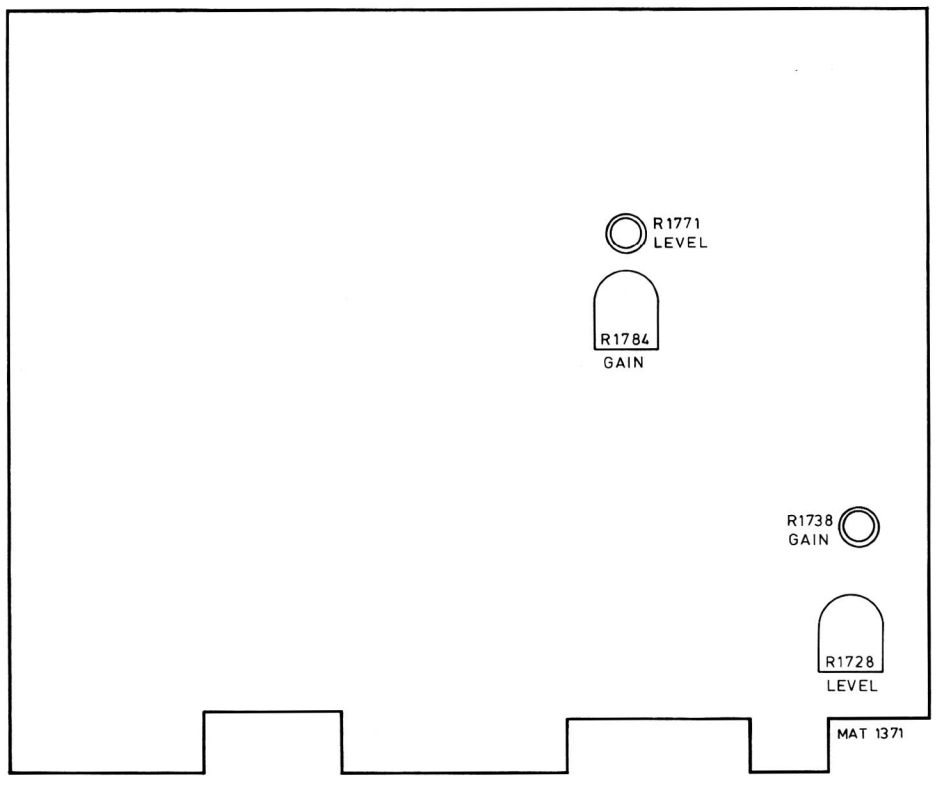


FIG. 6.6. Adjusting elements adaption unit A9.

MIN/MAX UNIT A10

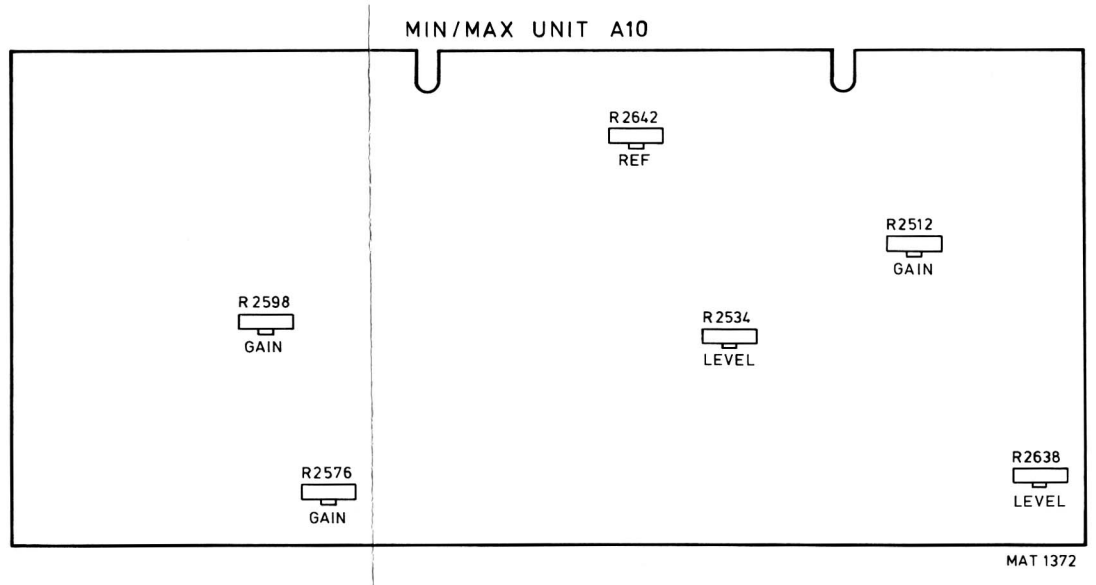


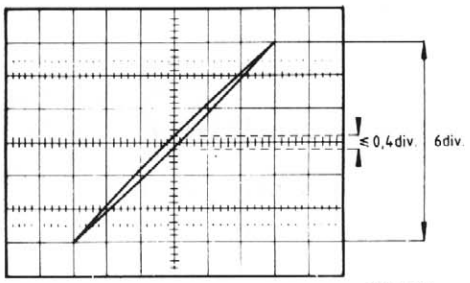
FIG. 6.7. Adjusting elements MIN/MAX unit A10.

6.6.6.5. Horizontal sensitivity via input B

- Set B AMPL/DIV switch S8 to 20 mV/div. and B AMPL/DIV potentiometer R8 to CAL.
- Depress pushbutton A of display mode switch S1.
- Set TIME/DIV switch S10 to X DEFL.
- Depress pushbutton B of the trigger source selector switch S16.
- Apply a sine-wave voltage of 120 mVp-p, frequency approximately 2 kHz, to the B input socket.
- Check that the trace length is 6 divisions $\pm$ 0,6 division.

6.6.6.6. Phase difference between X and Y channels.

- Input signal and control settings as in the previous section.
- Depress pushbutton AC of trigger mode switch S2.
- Depress pushbutton B of the display mode switch S1.
- Check that the line is displayed under an angle of 45^{o}.
- Increase the frequency to 100kHz.
- Check that the phase error does not exceed 3^{o}.



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6.6.7. Calibration voltage (R1607, Fig. 6.2.)

- Check that the voltage on the CAL output socket is 1,2 V $\pm$ 1 %. If necessary readjust potentiometer R1607.
- Check that the frequency is 2 kHz $\pm$ 10%.

6.6.8. Mains voltage variation

- Depress pushbutton CHOP of the display mode switch S1.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Pull X MAGN switch S5 to position x10.
- Set TIME/DIV switch S10 to 0,2 ms/div. and TIME/DIV potentiometer R9 to CAL.
- Depress pushbutton A of the trigger source selector switch S16.
- Set A (B) AMPL/DIV switch S6 (S8) to 0,2 V/div.
- Connect the CAL output socket X1, to the channel A and B input sockets X2 and X3.
- Vary the a.c. voltage to which the instrument is connected with + or - 10% of the nominal voltage.
- Check that no changes in horizontal and vertical deflection are visible on the C.R.T. screen and that the intensity remains unchanged.

6.7. ADJUSTING AND CHECKING THE DIGITAL OSCILLOSCOPE PART

- Pushbutton MEMORY ON must be depressed in all the following sections, unless otherwise stated.
- Adjust VREF (testpoint VREF on logic unit A11) to - 0,5 V ± 2,5 mV with potentiometer R2086 (Fig. 6.5.).
- Check the 20 MHz VCO frequency (pin 5 of counter D2098 on logic unit A11.
- If necessary readjust with potentiometer R2044 (Fig. 6.5.).

6.7.1. Adjusting X- and Y- adaption amplifiers

6.7.1.1. Offset X-dac (Fig.6.5.)

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set LEVEL control R5 in its midposition.
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Set A AMPL/DIV switch S6 to 20 mV/div.
- Apply a sine-wave voltage of 120 mVp-p, 2kHz to A input socket X2. A sine-wave of four periods is now displayed on the C.R.T. screen.
- Adjust potentiometer R2052 on logic unit A11 for a nice and smoothed sine-wave.
- Check this for the complete range of X POSITION control R4 when XMAGN switch S5 is pulled.
- Depress XMAGN switch S5.

6.7.1.2. Level and Gain X-adaption amplifier (R1771,R1784, Fig. 6.6.)

Start with the same settings as before.

- Set TIME/DIV switch S10 to 1 ms/div.
- Apply a time marker pulse of 80 mVp-p, 1 ms to A input socket X2. 10 marker pulses are now displayed on the C.R.T. screen.
- Release pushbutton MEMORY ON S17.
- Position the fifth markerpulse with the aid of X POSITION control R4 to the horizontal centre of the screen.
- Depress pushbutton MEMORY ON S17.
- The level can be adjusted with the aid of potentiometer R1771 on adaption unit A9 by positioning the fifth marker pulse to the horizontal centre of the screen.
- Check that the fifth markerpulse is not shifted more than 0,1 division when switching pushbutton MEMORY ON S17.
- Adjust the gain with potentiometer R1784 on adaption unit A9 such that the distance between the second and the nineth markerpulse is 8 divisions.

Note: The adjusting procedure of the LEVEL AND GAIN X-ADAPTION AMPLIFIER must be repeated if, when operating several times the MEMORY ON switch, the second, the fifth and the nineth marker pulse are shifting more than 0,1 div.

6.7.1.3. LEVEL and GAIN Y-ADAPTION amplifier (R1728,R1738, Fig. 6.6.)

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set the LEVEL control R5 in its midposition.
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Set A AMPL/DIV switch S6 to 10 mV/div.
- Apply a sine-wave voltage of 120 mVp-p, 2 kHz to A input socket X2.
- Depress pushbutton CLEAR S20 and keep it depressed until pushbutton LOCK S21 is depressed.
  A horizontal line is now displayed on the C.R.T. screen.
- Position this horizontal line one division below the centre horizontal graticule line with the aid of potentiometer R1728 on adaption unit A9.
- Release pushbutton LOCK S21.
- Turn potentiometer R1738 on adaption unit A9 fully anti-clockwise.
- Adjust gain potentiometer R1738 on adaption unit A9 so that the signal tops are situated at the upper horizontal graticule line.
- Depress pushbutton CLEAR S20 and keep it depressed until pushbutton LOCK S21 is depressed.
- Set the zero line to the screen centre with the aid of R1728.
- Release pushbutton LOCK S21.

6.7.2. Adjusting of the sequential sampling circuit (100 µs/div. .... 0,1 µs/div.

6.7.2.1. Offset staircase (R2036, Fig. 6.5.)

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set LEVEL control R5 in its midposition.
- Set TIME/DIV switch S10 to 10 µs/div.
- Set A AMPL/DIV switch S6 to 20 mV/div.
- Apply a sine-wave voltage of 120 mVp-p, 50 kHz to A input socket X2.
  A sine-wave of five periods is now displayed on the C.R.T. screen.
- Adjust potentiometer R2036 on logic unit A11 for a nice and smoothed sine-wave.
- Check this for the complete range of X POSITION control R4 when XMAGN switch S5 is pulled.
- Depress XMAGN switch S5.

6.7.2.2. Level and gain staircase (R2033,R2034, Fig. 6.5.)

Start with the same settings as in the previous section.

- Set TIME/DIV switch S10 to 1 /us/div. and TIME/DIV continuous control potentiometer R9 to CAL.
- Apply a time marker pulse of 80 mVp-p, 1/us to A input socket X2.
- Adjust potentiometer R2034 on logic unit A11 in such a way that the first marker pulse is just visible (The starting distorsion of the displayed sweep has to be just outside the visible range).
- 10 markerpulses are now displayed on the C.R.T. screen.

- Adjust the gain with potentiometer R2033 on logic unit A11 such that the distance between the second and the nineth markerpulse is 8 divisions.
- Set TIME/DIV switch S10 to 0,1 /us/div.
- Apply a sine-wave voltage of 120 mVp-p, 1 MHz to A input socket X2. A sine-wave which starts with an horizontal line is now displayed on the C.R.T. screen.
- Set X-POSITION control R4 so that the start of the trace is visible on the screen.

- Adjust now the startpoint. This is done with potentiometer R2034 on logic unit A11 in such a way that the horizontal line is just disappeared from the screen.
  Shift now the sine-wave 0,2 division more to the left with potentiometer R2034 on logic unit A11.

6.7.2.3. Square wave response MEMORY ON (C2152, Fig. 6.5.)

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress AUTO of the trigger mode switch S2.
- Set TIME/DIV switch S10 to 0,1/us/div.
- Set A AMPL/DIV switch to 20mV.
- Apply a square wave voltage 120mVp-p, 1MHz to the A input socket.
- Adjust C2152 for optimal square wave response.

6.7.3. Time-base check

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress pushbutton DC of the trigger mode switch S2.
- Set LEVEL control R5 in its midposition.
- Set A AMPL/DIV switch S6 to 20 mV/div.
- Apply a time marker pulse of 80 mVp-p, with A frequency according to the TIME/DIV switch settings to A input socket X2.
- Check all the positions of the TIME/DIV switch S10 with the continuous control R9 to CAL.
  Check also the positions 1, 2 and 5s/div. by depressing TIME/DIV pushbutton S26.
  The distance between the second and the nineth markerpulse is 8 divisions + or - 2,5 %.
- Release TIME/DIV pushbutton S26.
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Apply a time marker pulse of 80 mVp-p, 20 /us/div. to A input socket X2.
- Pull XMAGN switch S5 to x10.
- Check for the complete range of XPOSITION control R4 that the distance between the second and the nineth markerpulse doesn't

exceed + or - 4%.
- Set TIME/DIV switch S10 to 0,1 /us/div.
- Apply a time marker pulse of 80 mVp-p, 0,01 /us/div. to A input socket X2.
- Check for the complete range of XPOSITION control R4 the distance between the second and the nineth marker pulse doesn't exceed + or - 4%.

6.7.4. Vertical balance and sensitivity (R2512,R2638, Fig. 6.7.)

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of trigger source selector switch S16.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set LEVEL control R5 in its midposition.
- Set TIME/DIV switch S10 to 1 ms/div.
- Set A AMPL/DIV switch S6 to 20 mV/div.
- Apply a calibrated square-wave voltage of 120 mVp-p, 500 Hz to A input socket X2.
  A square-wave voltage of five periods is now displayed on the C.R.T.screen.
- Adjust the amplitude of the square-wave voltage for a trace height of 6 divisions with the aid of potentiometer R2512 on MIN/MAX unit A10.
- Depress the input coupling switch S13 (0).
  A horizontal line is now displayed which can be shifted with the aid of A POSITION control R2.
- Release pushbutton MEMORY ON S17.
- Position the trace on the centre horizontal graticule line with A POSITION control R2.
- Check that the trace does not jump more than 0,1 division when pushbutton MEMORY ON S17 is operated.
  If necessary readjust potentiometer R2638 on the MIN/MAX unit A10

6.7.5. Equality between memory on and off

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of the trigger source selector switch S16.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set LEVEL control R5 in its midposition.
- Set TIME/DIV switch S10 to 1 ms/div.
- set A AMPL/DIV switch S6 to 20 mV/div.
- Apply a sine-wave voltage of 120 mVp-p, 500 Hz to the A input socket X2.
  A sine-wave of five periods and an amplitude of 6 divisions is now displayed on the C.R.T screen.
- Check that the sine-wave does not jump horizontally as well as vertically more than 0,1 division when pushbutton MEMORY ON S17 is operated.

  Repeat 6.7.1.2. in case of horizontal deviations.
  Repeat 6.7.1.3. and 6.7.1.4. in case of vertical deviations.

- Apply a time marker pulse of 80 mVp-p, 0,5 ms to the A input socket X2.
- Check that in the TIME/DIV switch S10 positions 0,5 ms/div. ..... 0,1 /us/div. the markers do not jump more than 0,6 divisions horizontally.

6.7.6. Adjusting of the MIN/MAX circuit (R2534,R2576,R2598,R2642, Fig. 6.7.)

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A ot the trigger source selector switch S16.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Set A AMPL/DIV switch S6 to 20 mV/div.
- Depress the input coupling switch S13 (0).
- Depress pushbutton MIN/MAX S28.
  A wide band is now displayed.
- Adjust potentiometer R2642 on MIN/MAX unit A10 for a sharp line on the screen.
- Adjust potentiometer R2534 on the MIN/MAX unit A10 for a trace jump of the zero line of less than 0,1 division when MIN/MAX pushbutton S28 is operated.
- Depress pushbutton MIN/MAX S28.
- Release the input coupling switch S13.
- Apply a calibrated square-wave voltage of 120 mVp-p, 2 kHz to the A input socket X2.
  A square-wave is now displayed of which the minimum and maximum values are represented by a wide band.
- Adjust potentiometers R2576 and R2598 on the MIN/MAX unit A10 to change the wide band in sharp lines and to adjust the square-wave for 6 divisions amplitude.

6.7.6.1. Check of the MIN/MAX circuit.

Settings as in the previous section.

- Check that the square-wave does not jump more than 0,1 division when pushbutton MIN/MAX S28 is operated.
  If necessary readjust according to the previous section 2.6.
- Depress pushbutton MIN/MAX S28.
- Depress pushbutton CHOP of the display mode switch S1.
- Check that a square-wave is displayed for channel A and a zero line for channel B.
- Depress pushbutton A of the display mode switch S1.
- Depress the input coupling switch S13 (0)
- Set TIME/DIV switch S10 to 0,5 s/div.
- Depress pushbutton TIME/DIV S26.
- Check that one zero line is now displayed.
  Note that the complete line is built up in about 50 seconds.

  Note: If two zero lines are displayed it will be caused by defective peak detectors D2503 and D2504. (See also fault finding at chapter 7.7.3.1.)
- Release pushbutton TIME/DIV S26.
- Release pushbutton MIN/MAX S28.
- Release input coupling switch S13 (0).
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Release pushbutton MEMORY ON S17.
- Apply a calibrated sine-wave voltage of 120 mVp-p, 35 MHz to A input socket X2.
- Check that the amplitude on the screen is 4,2 divisions or more.
- Depress pushbutton MIN/MAX S28
- Depress pushbutton MEMORY ON S17.
- Check that the amplitude on the screen is 4,2 divisions or more.
- Release pushbutton MIN/MAX S28.

6.7.7. Adjusting of the C and D channels (R2324,R2374, Fig. 6.8.)

- Depress pushbutton ABCD CHOP S27.
- Depress pushbutton EXT of the trigger source selector switch S16.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Set TIME/DIV S10 to 0,2 ms/div.
- Apply a calibrated square-wave voltage of 0,6 Vp-p, 2 kHz to the C and D 0,1 V/div. sockets X14 and X16 on the rear panel of the instrument.
- Toe trigger the oscilloscope apply the same square-wave voltage also to EXT input socket X5.
- Adjust potentiometers R2324 and R2374 on AUX. CHANNEL unit A12 for a trace height of 6 divisions for both square-waves.
  If necessary operate the C and D POSITION controls R13 and R14 on the instruments left side.

6.7.7.1. Check of the C and D channels.

Settings as in previous section

- Turn C POSITION control R13 and D POSITION control R14 so that the traces are shifting upwards completely (potentiometers to the stops).
- Check that the remaining part of the displayed square-wave does not exceed 0,5 division.
- Turn the C and D POSITION controls R13 and R14 to their opposite stops.
- Check that the remaining part of the displayed square-wave does not exceed 0,5 division.
- Set the C and D POSITION controls R13 and R14 to midrange
- Apply a calibrated square-wave voltage of 6 Vp-p, 2 kHz to the C and D 1 V/div. input sockets X13 and X15.
- Check that the amplitude of the square-waves is 6 divisions + or - 2%
- Apply a calibrated square-wave voltage of 6 Vp-p, 1 MHz to the C and D 1V/div. input sockets X13 and X15.
- Check that the amplitudes of the square-waves exceed 4,2 divisions.
- Apply a common mode sine-wave voltage of 10 Vp-p, 50 kHz to the C and D 0,1 V/div. input sockets X14 and X16.
  (Common mode voltage: voltage between chassis and both short-circuited BNC's X14 and X16).
- A from this signal derived trigger signal must be applied to the EXT input socket X5.
- Check that the amplitude of the signal on the screen does not exceed 0,3 division.
- Apply a common mode sine-wave voltage of 10 Vp-p, 50 kHz to the C and D 1 V/div. input sockets X13 and X15.
- Check that the amplitude of the signal on the screen does not exceed 0,03 division.
- Release pushbutton ABCD CHOP S27.

7. CORRECTIVE MAINTENANCE

7.1. REPLACEMENTS

7.1.1. Standard parts

Electrical and mechanical parts replacements can be obtained through your local Philips organisation or representative. However, many of the standard electronic components can be obtained from other local suppliers. Before purchasing or ordering replacement parts, check the parts list for value, tolerance, rating and description.

NOTE: Physical size and shape of a component may affect instruments performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade the instruments performance.

7.1.2. Special parts

In addition to the standard electronic components, some special components are used:
- Components, manufactured or selected by Philips to meet specific performance requirements.
- Components which are important for the safety of the instrument.

ATTENTION: Both type of components may only be replaced by components obtained through your local Philips organisation or representative.

7.1.3. Transistors and Integrated Circuits

- Return transistors and I.C.'s to their original positions, if removed during routine maintenance.

- Do not renew or switch semi-conductor devices unnecessary, as it may affect the calibration of the instrument.

- Any replacement component should be of the original type or a direct replacement. Bend the leads to fit the socket or pcb-holes and cut the leads to the same lenght as on the component being renewed.

- When a device has been renewed, check the operation of the part of the instrument, that may be affected.

- When re-installing power-supply transistors, use silicon grease to increase the heat-transfer capabilities.

WARNING: Handle silicon grease with care. Avoid contact with the eyes. Wash hands thoroughly after use.

7.1.4. Static sensitive components

This instrument contains electrical components that are suspectible to damage from static discharge. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

7.1.5. Handling MOS devices

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

CAUTION: Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

7.1.5.1. Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or a special IC carrier that either short-circuits all leads or insulates them from external contact.

7.1.5.2. Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord to a chain. Connect all testing and handling equipment to the same surface. Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected either to the supply voltage or to ground.

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7.1.5.3. Mounting

Mount MOS integrated cicuits on printed circuit boards after all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board, the person mounting the circuits should touch the board before bringing the MOS circuits into contact with it.

7.1.5.4. Soldering

Soldering iron tips, including those of low voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

7.1.5.5. Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the proper handling precautions should still be observed.
Until the sub-assemblies are inserted into the complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape is put on the circuit board terminals.

7.1.5.6. Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed circuit boards with MOS devices, from test sockets or systems with power on.

7.1.5.7. Voltage surges

Beware of voltage surges due to switching electrical equipment ON or OFF, relays and d.c. lines.

7.1.6. Removing printed circuit boards (Fig. 7.1. and 7.2.)

7.1.6.1. Removing the logic unit A11

- Disconnect all connectors.
- Unscrew the fixing screws.
- Eventually lift the unit out of the connector of option A14.
- Remount the unit in reverse order.

7.1.6.2. Removing of the MIN/MAX unit A10

- Disconnect all connectors.
- Unscrew the fixing screws.
- Shift the unit out of its connector and the unit supports.
- Reinstall the unit in reverse order.

7.1.6.3. Removing the adaption unit A9

- Remove the MIN/MAX unit A10 (See 7.1.6.2.)
- Disconnect all connectors.
- Unsolder the remaining connections.
- Unscrew the delay line fixing bracket.
- Unscrew the fixing screws.
- Take out the unit.
- Reinstall the unit in the reverse order.

7.1.6.4. Removing the AC power supply unit A1

- Unscrew the four frame fixing screws.
- Take out the unit.
- Take care of the eventually built in option-flat-cable.
- Disconnect the connector(s).
- Reinstall the unit in reverse order.

7.1.6.5. Removing the DC power supply unit A2

- Unscrew the two heat sink fixing screws of the power transistors at the chassis side.
- Disconnect all connectors.
- Unscrew the seven fixing screws.
- Take out the unit carefully without damaging the cables.
- Reinstall the unit in reverse order.

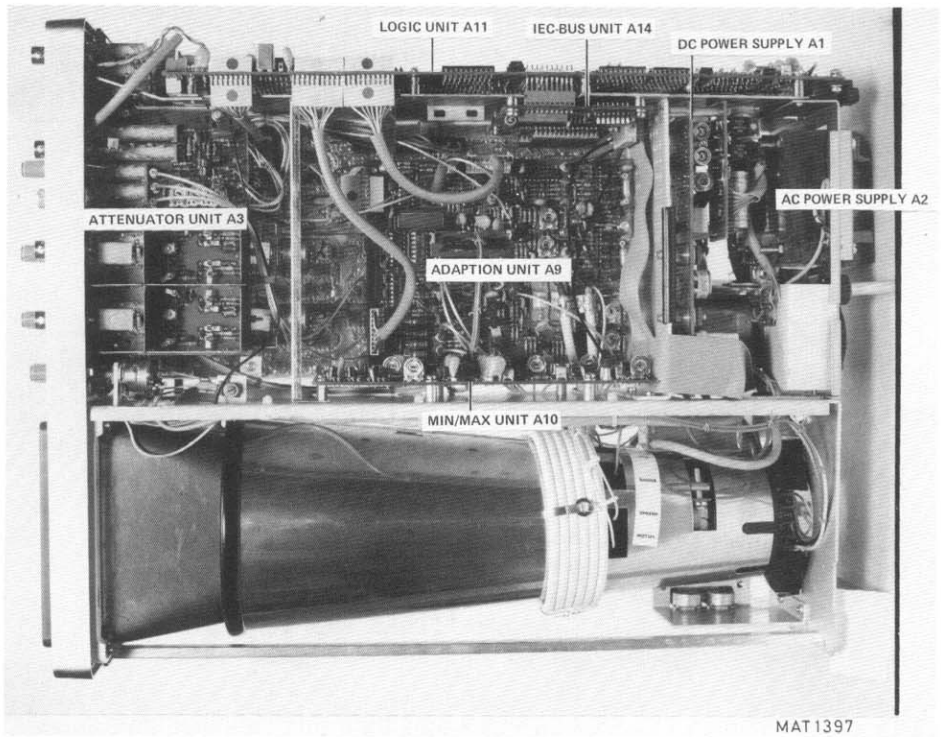

FIG. 7.1. Removing printed circuit boards.

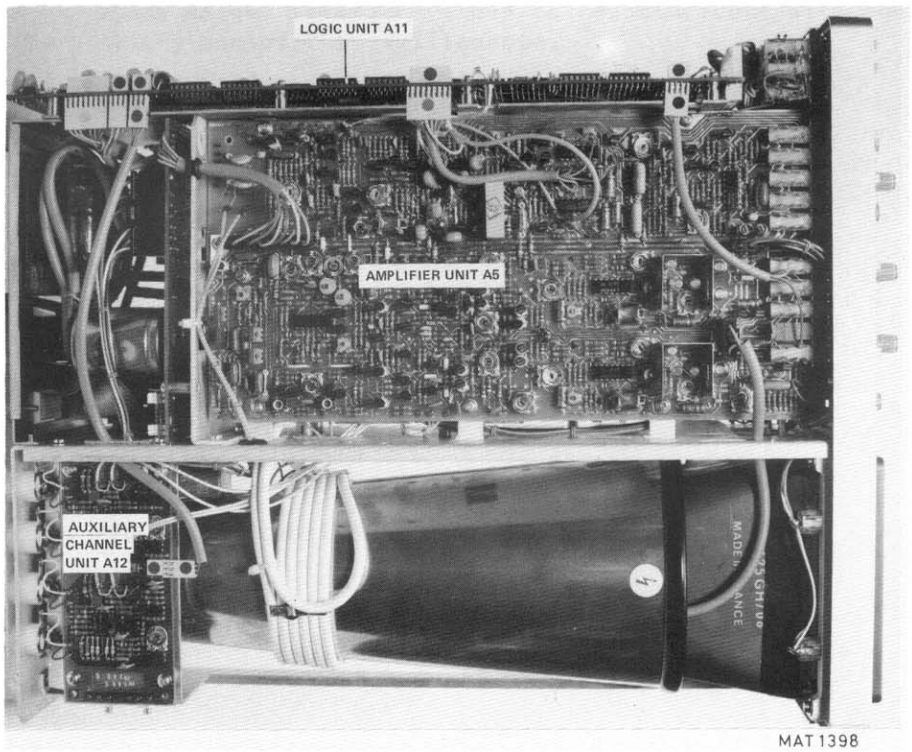

FIG. 7.2. Removing printed circuit boards.

7.1.6.6. Removing the amplifier unit A5

- Disconnect all connectors.
- Also disconnect the connectors at the bottom side of the unit.
- Unsolder the remaining connections.
- Take out the unit.
- Reinstall the unit in reverse order.

7.1.7. Replacing knobs, textplate and front unit

7.1.7.1. Removing single knobs (fig. 7.3.).

The channel B position, X position and LEVEL control knobs can be removed as follows:
- Prise off cap A
- Slacken the slotted nut B
- Pull off the knob of the spindle

When fitting a knob or cap, ensure that the spindle is in a position which allows reference lines to be coincident with the markings on the text plate of the oscilloscope.
All other single knobs can be pulled off from the spindles.

7.1.7.2. Removing double knobs

- Pull off the small knob
- Slacken the hexagonal nut and pull off the outer knob from its spindle.

When fitting a knob or a cap, ensure that the spindle is in a position which allows reference lines to be coincident with the markings on the text plate of the oscilloscope.

7.1.7.3. Removing the textplate

After having removed the knobs, the textplate can be removed after unscrewing the three hexagonal nuts of the AMPL/DIV and TIME/DIV switches.

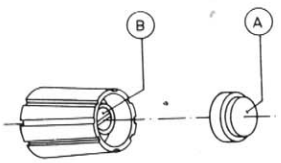

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FIG. 7.3. Removing the knobs.

7.1.7.4. Removing the front unit

In order to gain access to parts on the AMPL/DIV and TIME/DIV switches and components on the attenuator board, it is best to remove the front panel assembly complete in accordance with the following procedure:

- Remove the instrument covers in accordance with section 4.2.
- Remove the INTENS, FOCUS and ILLUM knob by pulling them off the shafts.
- Remove the earthing terminal-nut D at the front inside (Fig.7.4).
- Remove three screws A (Fig.7.5).
- Remove two screws B (Fig.7.4.) and the two screws E that are accessible after removing the logic unit A 11 completely, (as described in chapter 7.1.6.1.) that fix the attenuator to the frame (Fig.7.5).
- Remove the three screws C (Fig.7.6).
- Make a note of the positions of the miniature connectors on the printed circuit board.
- Remove the three fixing screws of the MIN/MAX unit A 10 and shift it a bit out of its supports in order to remove the connector X506.
- Disconnect all plugs, miniature sockets, coaxial sockets and clamping terminals from the attennuator unit.
- Now shift the complete front unit through the front; screening covers can be removed in order to get access to parts.
- When the front unit is reinstalled, make sure that the connections of the Y position controls are correctly mounted: when the Y POSITION controls are rotated clockwise, the trace should shift upwards.

7.1.7.5. Replacing pushbutton switches

The pushbutton switches and the LED-bar of the memory section can be replaced as follows:

- Remove the logic unit A11.
- Press the plastic fixing brackets of the relevant switch or LED-bar/switch combination and pull it out of the frame.
- Replace the defective switch combination complete.

NOTE: It is possible to replace one single switch (See 7.1.7.6.). If one LED of the LED-bar is defective it can be replaced seperately. Make sure that the connection wires are bend equal to those of the defective LED.

When remounting the LED-bar/switch combination take care that the LED-bar engages with the holes in the frame and in the text plate.

7.1.7.6. Replacing one switch of a pushbutton unit

- Straighten the 4 retaining lugs of the relevant switch as shown in Fig. 7.7.
- Break the body of the defective switch by means of a pair of pliers and remove the pieces. The soldering pins are then accessible.
- Remove the soldering pins and clean the holes in the printed wiring board (e.g. with a sucking soldering iron).
- Solder a new switch onto the printed wiring board.
- Bend the four retaining lugs to their original positions.

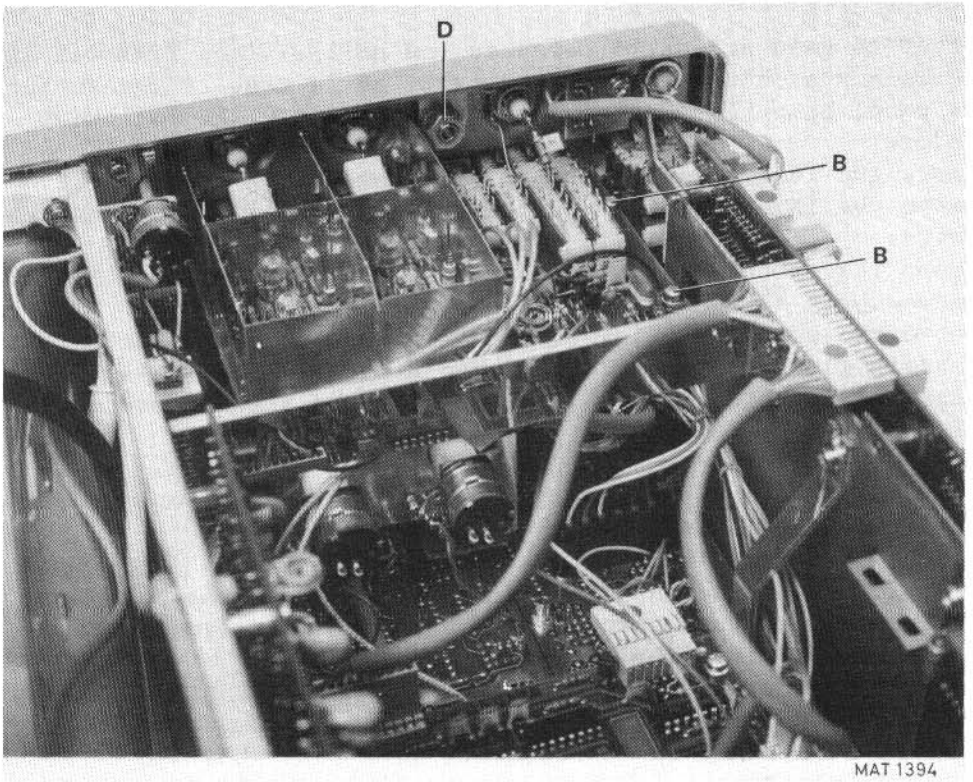

FIG. 7.4. Removing the front unit.

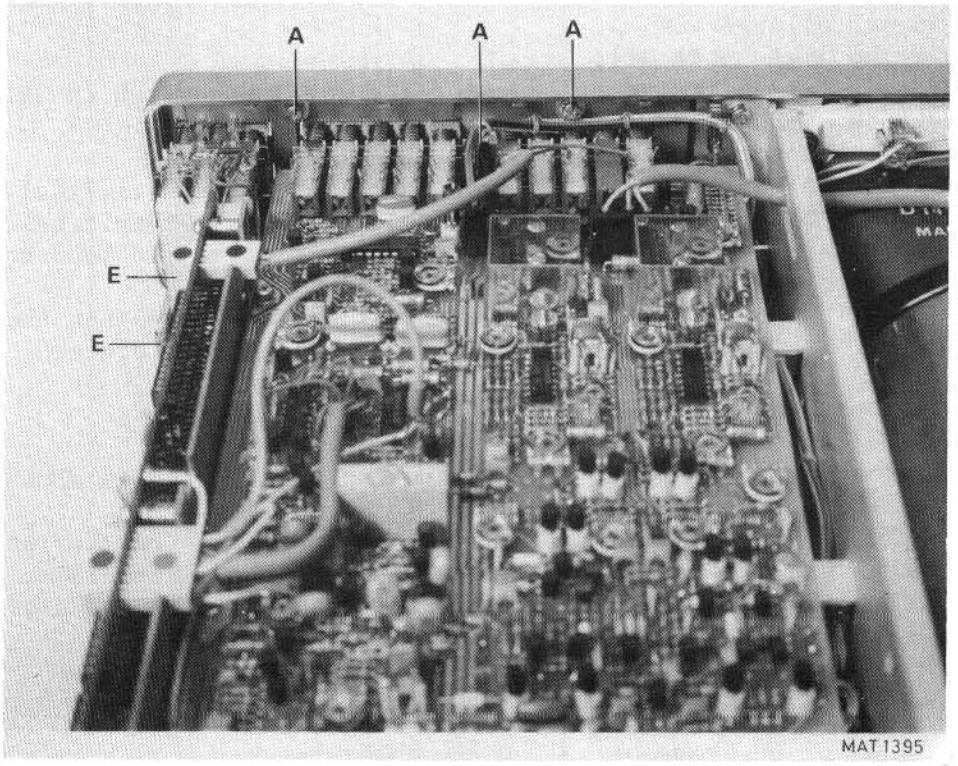

FIG. 7.5. Removing the front unit.

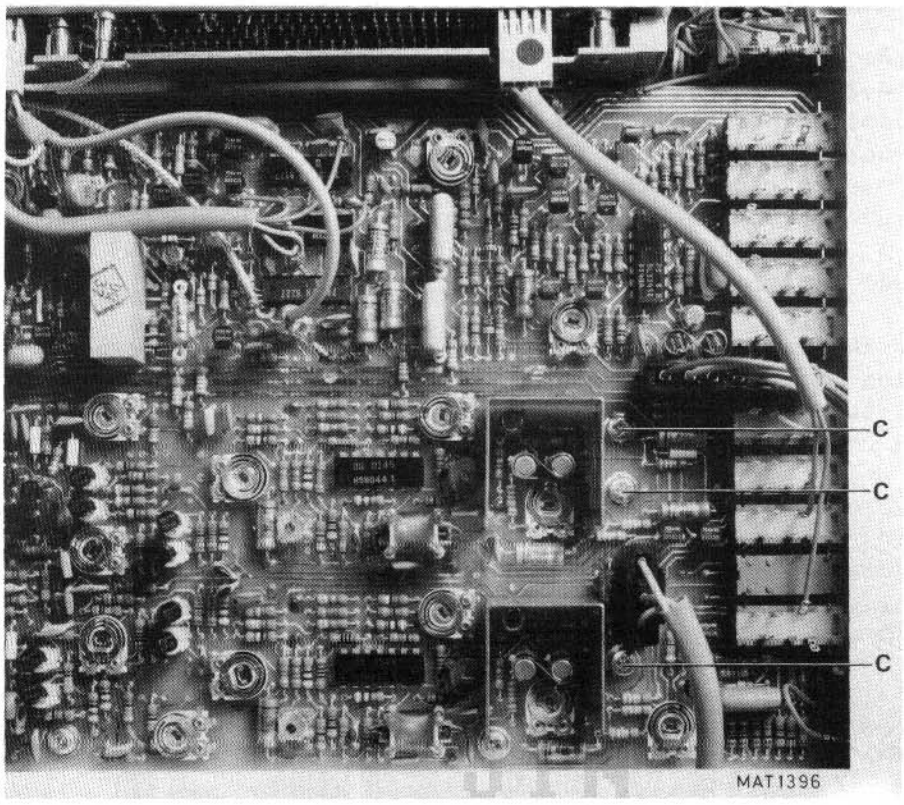

FIG. 7.6. Removing the front unit.

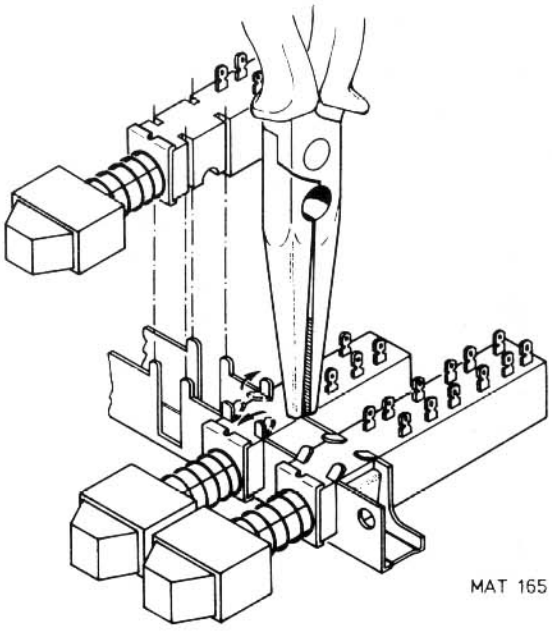

FIG. 7.7. Replacing a switch of a pushbutton unit.

7.1.8. Replacing internal fuses

- Remove the rear cover and the instrument cover as described in chapter 4.2.
- Now the following three fuses are accessible:
  1. The thermal fuse of the transformer.
  2. The fuse to protect the external battery supply input.
  3. The fuse to protect the power supply for overload.

7.1.8.1. Thermal fuse replacement (Fig. 7.8.).

- Unsolder the fuse connection wires 1 and 2 situated underneath the protection paper.
- Pull out the fuse.
- Insert a new fuse and resolder the connection wires.

7.1.8.2. Replacement of fuses F 201 and F 202 (Fig. 7.8.).

Fuse F 202 is accessible now and fuse F 201 can be replaced after disconnecting X 1504 and X 201. Both fuses have the same value: 1,4 A / 250 V Delayed Action.

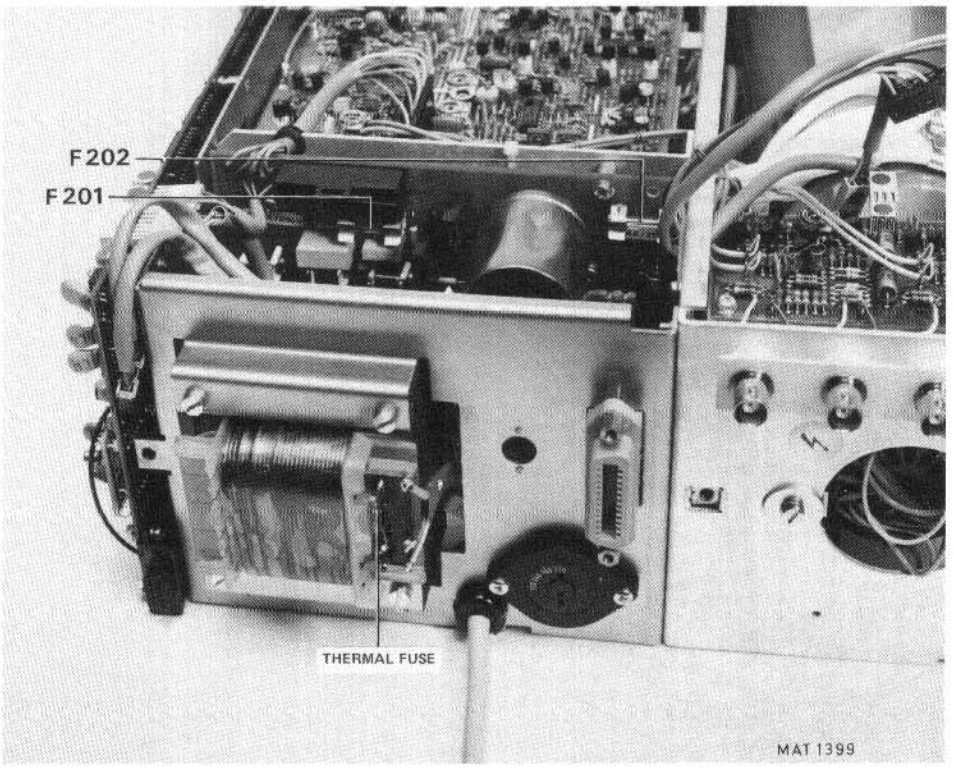

FIG. 7.8. Replacement of the thermal fuse.

7.1.9. Replacing the C.R.T.

- Remove the covers (See chapter 4.2.).
- Remove the bezel and contrast plate.

WARNING: Handle the C.R.T. carefully. Rough handling or scratching can cause the C.R.T. to implode. In particular be very carefully with the side connections of the C.R.T. If the connector pins are bent the C.R.T. is likely to develop a loss of vacuum.

- Disconnect the C.R.T. socket.
- Disconnect the side connections very carefully.
- Disconnect the trace rotation coil connector and pull the cable and plug through the hole in the frame.

WARNING: The EHT cable is unbreakably connected to the EHT unit. When the EHT cable to the post acceleration anode is disconnected, the cable as well as the CRT terminal must be discharged by shortening the terminals to earth.

- Loosen the screw that fixes the bracket around the C.R.T.-neck.
- Loosen the screws that fix the plastic brackets at the front of the C.R.T.
- Take the C.R.T. out of the instrument via the front panel until the EHT-side connection is accessible.
- Remove the EHT connector and take out the complete C.R.T.
- Install the new C.R.T. in reverse order and position the C.R.T. screen flush with the contrast plate.
- The torque applied to the screw of the bracket around the C.R.T.-neck is 0,4 Nm $\pm$ 0,1 Nm.

7.1.9.1. Replacing the delay line and or the C.R.T. screening

- Disconnect the delay line connections at the adaption unit A9 and at the amplifier unit A5.
- Remove the C.R.T. (See 7.1.9.).
- Remove the C.R.T. screening.
- Carefully pull off the delay line of the screening.
- Remount the delay line and stick it on the screening by means of dual adhesive tape.
- Take care that the connection leads of the delay line are mounted so that they can be directed through the hole in the frame.
- Remount the the screening and the C.R.T.

7.1.10. Removing cabinet parts

7.1.10.1. Removing the carrying handle

- Prise off the centre knobs from each pivot, using a screwdriver in one of the small slots at the sides of the knobs.
- Remove the cross-head screws that are now accessible.
- Bend both arms of the handle slightly outwards and take it off the cabinet.
- Grip and arms of the carrying handle must be ordered seperately (see mechanical parts list). A complete carrying handle can easily be constructed by pressing the arms into the grip.

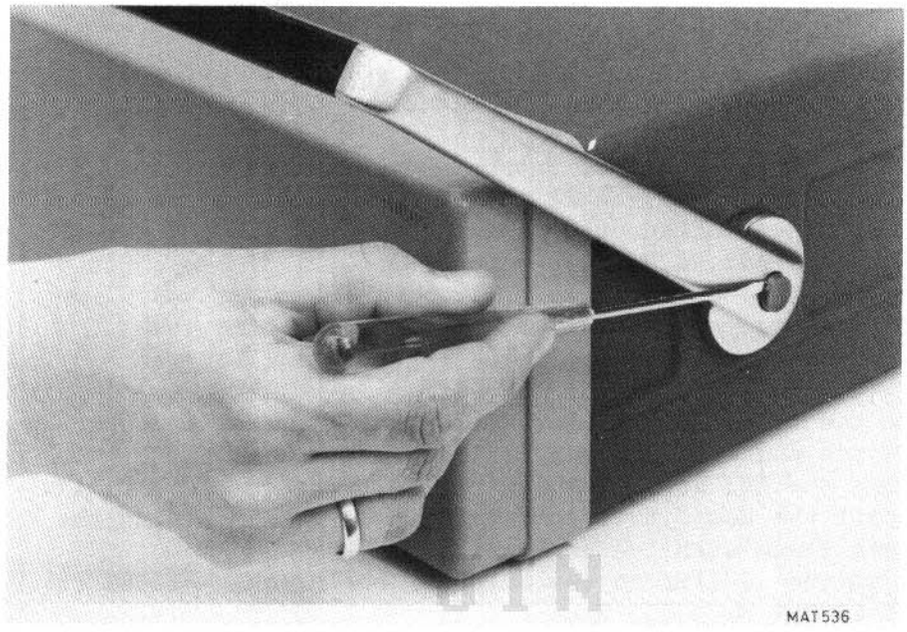

Fig. 7.9. Removing the carrying handle

7.1.10.2. Removing the bezel and the contrast plate

- Take hold of the bezel's bottom corners and gently pull it from the front panel.
- The contrast filter can be removed by pressing it gently out of the bezel.

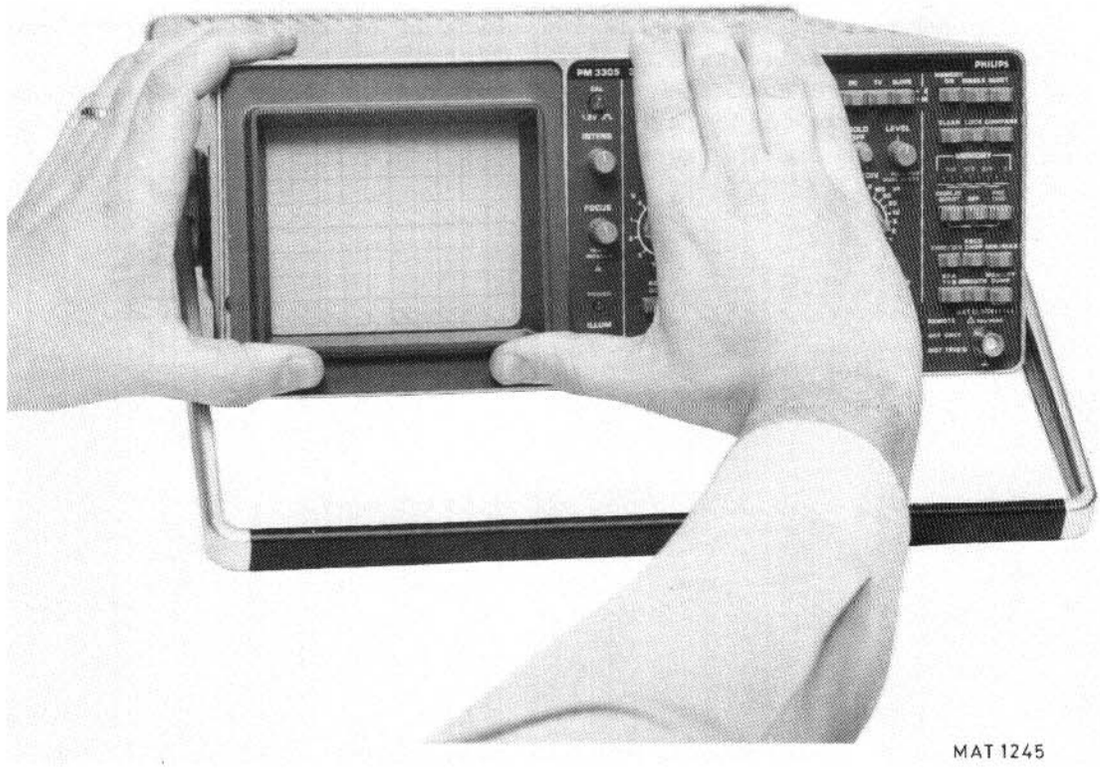

Fig. 7.10. Removing the bezel and the contrast plate

7.2. SOLDERING TECHNIQUES

Working method:
- Carefully unsolder one after the other the soldering tags of the semi-conductor.
- Remove all superfluous soldering material. Use a sucking iron or sucking litze wire.
- Check that the tags of the replacement part are clean and pre-tinned on the soldering places.
- Locate the replacement semi-conductor exactly on its place, and solder each tag to the relevant printed conductor on the circuit board.

NOTE: Bear in mind that the maximum permissible soldering time is 10 seconds during which the temperature of the tags must not exceed 250°C. The use of solder with a low melting point is therefore recommended.
Take care not to damage the plastic encapsulation of the semi-conductor (softening point of the plastic is 150°C).

ATTENTION: When you are soldering inside the instrument it is essential to use a low-voltage soldering iron, the tip of which must be earthed to the mass of the oscilloscope.

Suitable soldering irons are:

- ORYX micro-miniature soldering instrument, type 6A, voltage 6 V, in combination with PLATO pin-point tip type 0-569.

- ERSA miniature soldering iron, type minor 040 B, voltage 6 V.

- Low Voltage Mini Soldering Iron, type 800/12 W-6 V, power 12 W, voltage 6 V, order no. 4822 395 10004, in combination with 1 mm pin-point tip, order no. 4822 395 10012.

Ordinary 60/40 solder with core and 35-to 40 W pencil type soldering iron can be used to accomplish the majority of the soldering. If a higher wattage-rating soldering iron is used on the etched circuit boards, excessive heat can cause the etched circuit wiring to separate from the board base material.

7.3. TRIMMING TOOL KIT

This useful kit contains 3 twin-couloured holders, 2 extension holders and 21 interchangeable trimming pins. The wide variety of pins allows almost every type of trimming function to be carried out in instruments to be calibrated.
Type number: 800/NTX
Ordering number: 4822 310 50015.
A spare set containing the 8 most commonly used pins is available under the Ordering number:
4822 310 50016

Fig. 7.11. Trimming tool kit.

7.4. RECALIBRATION AFTER REPAIR

After any electrical component has been renewed the calibration of that particular circuit should be checked, as well as the calibration of other closely-related circuits.
Since the power supply affects all circuits, calibration of the entire instrument should be checked if work has been done in the power supply or if the transformer has been renewed.

7.5. INSTRUMENT REPACKING

If the instrument is to be shipped to a Service Centre for service or repair, attach a tag showing the full addres and the name of the individual at the users firm that can be contacted. The Service Centre needs the complete instrument, its serial number and a fault description. If the original packing is not available, repack the instrument in such a way that no damage occurs during transport.

7.6. TROUBLE SHOOTING

7.6.1. Introduction

The following information is provided to facilitate trouble shooting. Information contained in other sections of the manual should also be used to locate the defect. An understanding of the circuit is helpful in locating troubles, particularly where integrated cicuits are used. Refer to the Circuit description for this information.

7.6.2. Trouble shooting techniques

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If a fault appears, the following test sequence can be used to find the defective part:

- Check if the settings of the controls of the oscilloscope are correct. Consult the Operating Instructions.
- Check the equipment to which the oscilloscope is connected and the interconnection cables.
- Check if the osciloscope is well-calibrated. If not refer to Section 6 "Checking and Adjusting".
- Visually check the part of the oscilloscope in which the fault is suspected. In this way, it is possible to find faults such as bad soldering connections, bad interconnection plugs and wires, damaged components or transistors and IC's that are not correctly plugged into their sockets.
- Location of the circuit part in which the fault is suspected: the symptom often indicates this part of the circuit. If the power supply is defective the symptom will appear in several circuit parts.

After having carried out the previous steps, individual components in the suspected circuit parts must be examined:

- Transistors and diodes. Check the voltage between base and emitter (0,7 V approx. in conductive state) and the voltage between collector and emitter (0,2 V approx. in saturation) with a voltmeter or an oscilloscope. When removed from the p.c.b. it is possible to test the transistor with an ohmmeter since the base/collector junctions can be regarded as diodes. Like a normal diode, the resistance is very high in one direction and low in the other direction. When measuring take care that the current from the ohmmeter does not damage the component under test.
  Replace the suspected component by a new one if you are sure that the circuit is not in such condition that the new component will be damaged.
- Integrated circuits. In circuit testing can be done with an oscilloscope or voltmeter. A good knowledge of the circuit part under test is essential. Therefore first read the circuit description in Section 3.
- Capacitors. Leakage can be traced with an ohmmeter adjusted to its highest resistance range. When testing take care of polarity and maximum allowed voltage. An open capacitor can be checked if the response for AC signals is observed. Also a capacitance meter can be used: compare the measured value with the value and tolerance indicated in the parts list.
- Resistors. Can be checked with an ohmmeter after having unsoldered one side of the resistor from the p.c.b. Compare the measured value with the value and tolerance indicated in the parts list.
- Coils and transformers. An ohmmeter can be used for tracing an open circuit. Shorted or partially shorted windings can be found by checking the wave-form response when HF signals are passed through the circuit. Also an inductance meter can be used.
- Data latches. To measure on inputs and outputs of data latches a measuring oscilloscope can be triggered by the clock signal which is connected to the clock input of the data latch.
  Check the input data lines one by one during the active edge of the clock signal.
  This measurement can only be done in this way when there is an acceptable repetition time of the clock signal. A too low clock pulse repetition time results in a low intensity of the trace on the measuring oscilloscope screen.
  The outputs can easily be checked by a voltmeter or oscilloscope.

Oscilloscope checking of micro-processor bus signals.

The 8085 micro-processor is provided with the following busses:
- Address bus
- Data bus
- Control bus

In general, if signals on these bus lines are checked with an oscilloscope, a very unstable display will be the result.
This is due to the fact that these signals vary with time in a rather unpredictable way.
If anyhow a stable display of signals from one of these busses is obtained, this may be an indication that the micro-processor runs in a small program loop.

7.7. SERVICE ROUTINES

7.7.1. Power-up routine

Every time the instrument is switched-on the following test program is executed:

1. Checking if service routine is required (if yes the program will continue with the service routine).
2. Testing the checksum of PROM D2082.
3. Testing the internal RAM of D2064 and initialisation of D2064.
4. Testing the display memory D2089 and D2102.
5. Clearing the Display memory D2089 and D2102 and the internal RAM of D2064.
6. Switching-on all LED's on the front panel for about 3 seconds.
7. Eventually initialisation of the IEEE option PM8955.
8. Starting the main program.

If during the test a circuit is found to be faulty, the test stops. It is recommended to switch-off and after a few seconds switch-on again. This will reset the micro processor controlled system automatically. If the instrument goes in the same faulty situation again the table below will indicate what circuit may be defective:

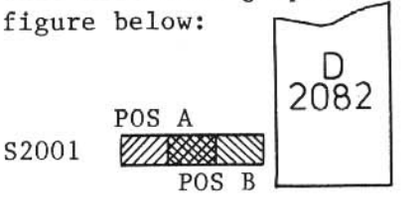
Failure in	NOT TRIG'D LED	REM LED	REP ONLY LED	four right LEDs of LED bar	four left LEDs of LED bar
first part of D2082	off	off	on	not applicable	not applicable
second part of D2082	on	off	on	not applicable	not applicable
RAM of D2064	on	on	on	off	off
Display memory	on	on	on	on	off

If no failure is found, all LED's in the LED bar will be lighting for about 3 seconds. After this the normal program is executed.

7.7.2. Service routines

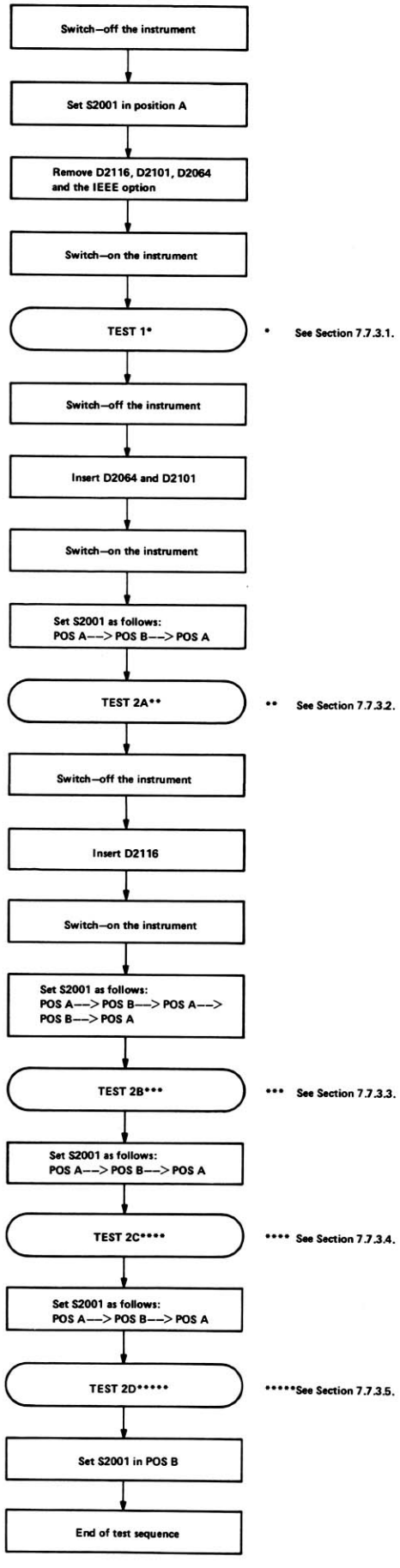
General

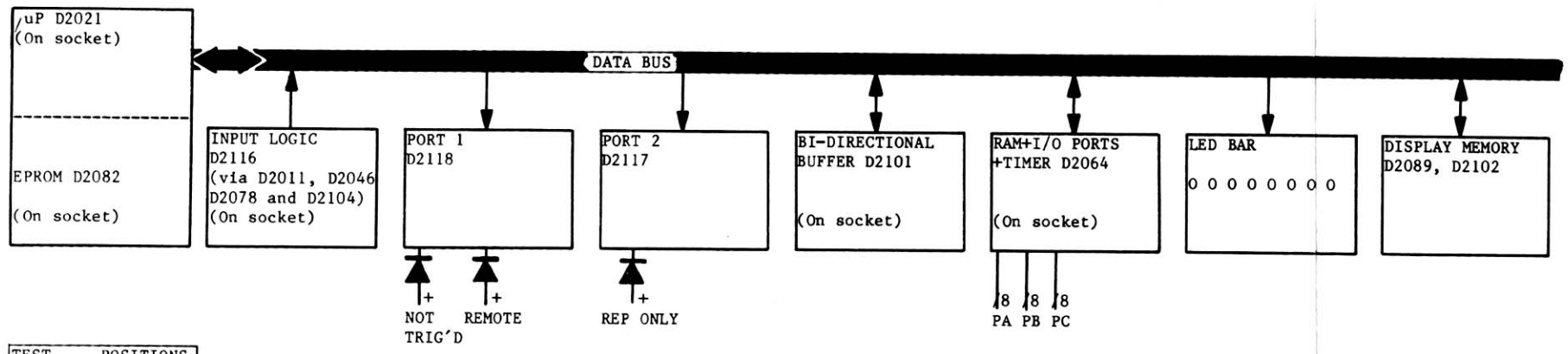
Five service routines are built in to trace failures in the digital sections of the instrument. In the further descriptions the routines are called: TEST 1; TEST 2A; TEST 2B; TEST 2C and TEST 2D.
The routines can be switched on by means of jumper S2001 on the Logic Unit A11. This jumper can be set into two positions according to the figure below:



Note: If the jumper is in position B the instrument will execute the normal program.

The following flow gives the procedure for fault finding in the digital section:





TEST	POSITIONS OF S2001 (sequent.)							
TEST 1	POWER OFF POS A ■· POS B POWER ON ■·	REMOVE D2116	1 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1 WRITTEN INTO D2118, REPETITION TIME 0,5s LED's BLINKING	1 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1 WRITTEN INTO D2117, REPETITION TIME 0,5s LED BLINKING	REMOVE D2101	REMOVE D2064	ONE LED SCROLLS WITH A REPETITION TIME OF 0,5s	
TEST 2A	POWER OFF INSERT D2064,2101 POWER ON ■·				INSERT D2101	INSERT D2064 1 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1 WRITTEN INTO OUTPUT PORTS OF D2064 REPETITION TIME 0,8s APPROX.		
TEST 2B	POWER OFF INSERT D2116 POWER ON ■·	INSERT D2116	NOT TRIG'D LED BLINKS IF THE DISPLAY MEMORY IS DEFECTIVE	REP ONLY LED BLINKS IF THE INTERNAL RAM OF D2064 IS DEFECTIVE		RAM CHECK		RAM CHECK
TEST 2C	■·	CHECKS ALL INPUT SWITCHES OF THE MEMORY SECTION + A,ALT,CHOP,ADD,B AUTO,AC/DC TIME/DIV PULL FOR DUAL					BINARY COUNTER DISPLAY. READ OUT STARTS RANDOM AND INCREASES BY 2 IF A SWITCH IS DEPRESSED AND RELEASED	
TEST 2D	■·		FIXED OUTPUTS (See table)	FIXED OUTPUTS (See table)		FIXED OUTPUTS (See table)		

7.7.3. Description of the Service Routines

7.7.3.1. TEST 1

This test is a functional check of:
- micro processor and PROM
- Output ports D2117 and D2118
- LED bar unit

Actions executed by this test:
- A pattern 10101010/01010101 is written into D2117 and D2118 with a repetition time of 0,5 s approx.
  The LED's NOT TRIG'D, REP ONLY and REMOTE will blink in the following sequence: REMOTE
  REP ONLY + NOT TRIG'D
  The other outputs can be measured by means of an oscilloscope.
- One LED of the LED bar scrolls.

7.7.3.2. TEST 2A

This test is a functional check of the output ports of D2064.

Actions executed by this test:
- Initialisation of D2064
- A pattern 10101010/01010101 is written to the output ports.
  (Can be measured by means of an oscilloscope, repetition time 0,8s approx.)

7.7.3.3. TEST 2B

This test is a functional check of:
1. The internal RAM of D2064
2. The display memory (D2089 and D2102)

Actions executed by this test:
1. In the the D2064 RAM-test a pattern is written into the LED bar and the REP ONLY LED and the REMOTE LED are ON.
   The REP ONLY LED blinks if the internal RAM of D2064 is defective.
After this test the REMOTE LED extinguishes.
2. In the display memory test a pattern is written into the LED bar and the NOT TRIG'D LED and the REMOTE LED are ON.
   The NOT TRIG'D LED blinks if the display memory is defective.

Note: The LED bar acts as a binary down counter during this test.

7.7.3.4. TEST 2C

This test is a functional check of:
- Input logic circuits (D2011, D2046, D2078, D2104 and D2116)
  The check can be carried out by means of an oscilloscope.
- Checking of the switches of the memory part.
- Checking of the switches: A, ALT, CHOP,ADD and B.
- Checking of the switches: AUTO, AC and DC.
- Checking of the TIME/DIV switch and the PULL FOR DUAL switch.

Actions executed by this test:
- Normal read-in routine for the switches is operative.
- When operating one of the above mentioned switches, the binary representation in the LED bar will be increased by 1 (binary).

Note: When releasing the pushbuttons the representation in the LED bar will be increased by 1 another time.
The LED bar acts as the display of a binary counter.

7.7.3.5. TEST 2D

Functional check of the instruments hardware. When measuring with an oscilloscope the following signals can be used:
RW (X2022, unit A11) repetition time 2MHz,
TRGL (X2023, unit A11) repetition time 500Hz max.,
DT (X2024, unit A11) repetition time 120Hz approx.,
NDRL (X2025, unit A11) repetition time 2MHz,
TRACK(X2026, unit A11) repetition time 2MHz.
It is necessary to apply a signal to the Channel A input socket.

Actions executed by this test:
- The instrument is in a fixed mode:
  Single channel (Select channel A)
  TIME/DIV is set 0,2ms/div.
  PRETRIG is set to zero
  No COMPARE
  No X=A/Y=B display (X=t disp)
  No SMOOTH
  No QUART display
  No DUAL slope triggering
  No MIN/MAX mode
  All LED's extinguished

The positions of the output ports is given in the following table.
- Constantly starting the take-in cycle by means of the signals IOWR8 and DUP3 (D2033 pin 3 and D2006 pin 12).
- Constantly starting the display cycle by means of the signals IOWR8 and DUP2 (D2033 pin 10 and D2087 pin 12).

The starting will be preceeded by setting SOD at High level, what can be used to trigger the measuring oscilloscope.

PORT	SIGNAL	PIN	LEVEL	
D2118	STADØ	2	low	
	STAD1	19	low	
	STAD2	5	low	
	STAD9	16	low	
	STAD1Ø	6	low	
	STAD11	15	low	
	NOTTRIG'D	9	high	
	REMOTE	12	high	
D2117	TBT	2	low	
	TBC	19	low	
	TBD	5	high	
	PRTRØ	16	high	
	PRTR1	6	high	
	PRTR2	15	high	
	REPONLY	9	high	
	n.c.	12	--	
PA D2064	CQ	21	low	
	CR	22	low	
	CS	23	low	
	CT	24	low	
	STA	25	high	
	STB	26	high	
	STC	27	high	
	ZEN	28	high	
PB D2064	UPCONT	29	low	
	SEQWC	30	low	
	HTRG	31	pulse	500Hz max.
	AVSB	32	low	
	DOTS	33	low	
	$\overline{QDR}$	34	high	
	DIR	35	high	
	AUXCH	36	low	
PC D2064	LTXT	37	low	
	SYNCH	38	high	
	$\overline{DIGCH}$	39	high	
	DUALOUT	1	low	
	n.c.	2	--	
	MIN/MAX	5	low	
TIMER D2064	TIMERIN	3	2MHz	
	TIMEROUT	6	20kHz	

7.7.4. Detailed description of measuring in circuits

7.7.4.1. Measuring the MIN/MAX circuits

The following procedure is helpful to check the correct operating of the MIN/MAX circuits.

- Depress pushbutton A of the display mode switch S1.
- Depress pushbutton A of the trigger source switch S16.
- Depress pushbutton AUTO of the trigger mode switch S2.
- Depress the MIN/MAX switch S26.
- Set the TIME/DIV switch S10 to 0,2ms/div.
- Set the AMPL/DIV switch S6 to 20mV/div.
- Apply a calibrated square wave of 120mVp-p, 2kHz to the A input socket.

If the trace jumps more than 0,1 division when operating the MIN/MAX pushbutton, the adjusting procedure according section 6.7.6.1. should be carried out.

- Check that the display of channel A is one square wave.
- Depress pushbutton B of the display mode switch S1.
- Check that one zero line is displayed.
- Depress pushbutton A of the display mode switch S1.
- Depress 0 of input coupling switch S13.
- Set the TIME/DIV switch to 0,5ms/div.
- Depress pushbutton TIME/DIV S26
- Check that one single zero line is displayed.

Note : The display is built up from left to right in about 50s.
Note : If in this case two zero lines are displayed one or both peak detectors D2503 and/orD2504 are defective.

The following procedure is intended to find the defective component.

- Release pushbutton 0 (S13).

A. - Apply a pulse signal with the following characteristics to the A input socket: positive going pulse width: 50ns
period time : 100ms
amplitude : 120mV

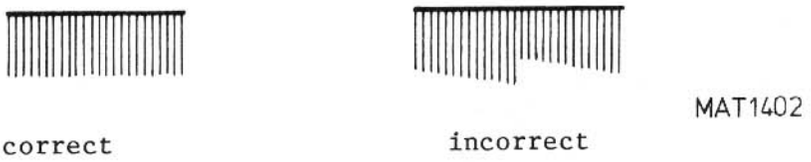
The display will be according the figure below:

MAT 1401

correct incorrect

If the incorrect shape is displayed, replace D2503 and adjust according section 6.7.6.1.

B. - Apply a pulse signal with the following characteristics to the A input socket: negative going pulse width: 50ns
period time : 100ms
amplitude : 120mV
- The display will be according to the figure below:



MAT1402

correct incorrect

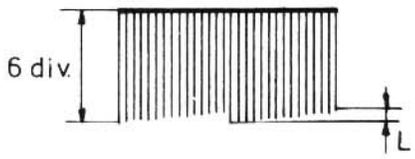
If the incorrect shape is displayed, replace D2504 and adjust according section 6.7.6.1.

C. - Apply a pulse signal with the same characteristics as at point A.
- The display will be according the figure below:

MAT 1403

If L exceeds 0,04 div., replace D2503 and adjust according section 6.7.6.1.

D. - Apply a pulse signal with the same characteristics as at point B.
- The display will be according the figure below:



MAT 1404

If L exceeds 0,04 div., replace D2504 and adjust according section 6.7.6.1.

8. SAFETY INSPECTION AND TESTS AFTER REPAIR AND MAINTENANCE IN THE PRIMARY CIRCUIT.

8.1. GENERAL DIRECTIVES

- Take care that the creepage distances and clearances have not been reduced.
- Before soldering, the wires should be bent through the holes of solder tags, or wrapped around the tag in the form of an open U, or, wiring ridigity shall be maintained by cable clamps or cable lacing.
- Replace all insulating guards and -plates.

8.2 SAFETY COMPONENTS

Components in the primary circuit may only be renewed by components selected by Philips, see also clause 7.1.2.

8.3. CHECKING THE PROTECTIVE EARTH CONNECTION

The correct connection and condition is checked by visual control and by measuring the resistance between the protective lead connection at the plug and the cabinet/frame. The resistance shall not be more than 0,1 ohm. During measurement the mains cable should be moved. Resistance variations indicate a defect.

8.4. CHECKING THE INSULATION RESISTANCE

Measure the insulation resistance at U = 500 V dc between the mains connections and the protective lead connections. For this purpose set the mains switch to ON. The insulation resistance shall not be less than 2 megaohm.

NOTE: 2 megaohm is a minimum requirement at 40°C and 95 % Relative Humidity. Under normal conditions the insulation resistance should be much higher (10...20 megaohm).

8.5. CHECKING THE LEAKAGE CURRENT

The leakage current shall be measured between each pole of the mains supply in turn, and all accessible conductive parts connected together (including the measuring earth terminal).
The leakage current is not excessive if the measured currents from the mentioned parts is $\leq$ 3,5 mA rms.

8.6 VOLTAGE TEST

The instrument shall withstand, without electrical breakdown, the application of a test voltage between the supply circuit and accessible conductive parts that are likely to become energized.
The test potential shall be 1500 V rms at supply-circuit frequency, applied for one second.
The test shall be conducted when the instrument is fully assembled, and with the primary switch in the ON position.
During the test, both sides of the primary circuit of the instrument are connected together and to one terminal of the voltage test equipment; the other voltage test equipment terminal is to be connected to the accessible conductive parts.

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9. PARTS LISTS

(Subject to alteration without notice)

9.1. MECHANICAL PARTS

Fig./Item	Qty.	Ordering number	Designation	
9.1. 1	1	5322 447 90325	Cabinet brown without handle	
9.1. 2	4	5322 462 44297	Foot (cabinet)	
9.1. 3	1	5322 498 54077	Grip for handle	
9.1. 4	2	5322 498 54072	Bracket for handle	
9.3. 1	2	5322 520 14267	Bearing bush for handle	
9.3. 2	2	5322 528 34128	Ratchet for handle	
9.3. 3	2	5322 530 84075	Spring for handle	
9.3. 4	2	5322 414 30043	Knob brown for handle	
9.3. 5	2	4822 502 30085	Screw for handle	
9.3. 6	2	4822 532 10582	Washer for handle	
9.1. 5	1	5322 447 90322	Front cover brown	
9.1. 6	1	5322 459 20271	Bezel brown	
9.1. 7	1	5322 480 34074	Contrast filter blue	
9.1. 8	1	5322 455 81009	Textplate	
9.1. 9	1	5322 447 90323	Cast aluminium front frame	
9.1. 10	1	5322 447 94647	Cast aluminium rear frame	
9.1. 11	1	5322 264 24015	Calibration terminal	X1
9.1. 12	1	5322 325 80235	Grommet for calibration terminal	
9.1. 13	8	5322 267 10004	BNC connector	X2 - X3 - X5 - X6 - X13 - X14 - X15 - X16
9.1. 14	1	5322 535 84346	Earthing terminal	X4
9.1. 15	1	5322 505 14178	Knurled nut for earthing terminal	
9.1. 16	1	5322 506 14005	Hexagonal nut for earthing terminal	
9.2. 1	1	5322 267 54187	ADC OUT connector	X10
9.2. 2	1	4822 265 20051	D.C. power input socket incl. switch	X11
9.1. 17	1	5322 255 44088	Led holder	B1
9.1. 18	3	5322 255 40231	Led holder	B10 - B11 - B12
9.1. 19	2	5322 381 14151	Lightreflector assembly	
9.1. 20	2	5322 255 24015	Lamp holder	E1 - E2

Fig./Item	Qty.	Ordering number	Designation	
9.4. 21	3	5322 414 30046	Knob brown, dia 10 mm	R1 - R6 - R11/S17
9.4. 21	3	5322 492 64337	Clamping spring for knob	R1 - R6 - R11/S17
9.4. 21	3	5322 414 70016	Knob cover, brown with dash	R1 - R6 - R11/S17
9.4. 22	3	5322 414 30044	Knob brown, dia 10 mm shaft dia 4 mm	R3/S4 - R4/S5 - R5/S32
9.4. 22	3	5322 414 70016	Knob cover, brown with dash	R3/S4 - R4/S5 - R5/S32
9.4. 23	1	5322 414 30046	Knob brown, dia 10 mm	R2
9.4. 23	1	5322 492 64337	Clamping spring for knob	R2
9.4. 23	1	5322 414 70016	Knob cover, brown with dash	R2
9.4. 24	1	5322 414 30047	Knob brown, dia 6.7-10 mm shaft dia 4 mm	R12
9.4. 24	1	5322 492 64337	Clamping spring for Knob	R12
9.4. 25	3	5322 414 30046	Knob brown, dia 10 mm	R7/S7 - R8/S9 - R9/S11
9.4. 25	3	5322 492 64337	Clamping spring for knob	R7/S7 - R8/S9 - R9/S11
9.4. 25	3	5322 414 70018	Knob cover, blue with dash	R7/S7 - R8/S9 - R9/S11
9.4. 26	3	5322 414 30045	Knob brown, dia 18,7 mm shaft dia 6 mm	S6 - S8 - S10
9.4. 27	18	5322 414 20038	Knob brown/green for pusbutton Switch	S1A - B - C - D - E S2A - B - C - D - S3 - S12 - S13 - S14 - S15 - S16A - B - C - D
9.4. 28	1	5322 414 20037	Knob brown/green spec. for pushbutton switch	S17
9.4. 29	6	5322 414 20036	Knob brown for pushbutton switch	S19 - S20 - S23 - S24 - S25 - S31
9.4. 30	8	5322 414 20038	Knob brown/green for pushbutton switch	S18 - S21 - S22 - S26 - S27 - S28 - S29 - S30
9.2. 3	1	5322 447 90324	Rear panel brown without other materials	
9.2. 4	2	5322 462 44298	Foot (rear panel)	
9.2. 5	2	5322 500 14228	Coin slot screw for rear panel	
9.2. 6	2	5322 530 70324	Circlip for coin slot screw	
9.2. 7	1	5322 272 10226	Line voltage adapter (4 positions + fuseholder)	S101
9.2. 8	1	5322 325 64061	Line cable cleat	
9.2. 9	1	4822 321 10084	Line cable, european type 10A-250V	

Fig./Item	Qty.	Ordering number	Designation
9.2. 9	1	4822 321 10092	Line cable, U.S.A. type
	16	5322 276 14102	Self-releasing pushbutton segment
	17	5322 276 14117	Mutual-releasing pushbutton segment
	1	4822 266 20014	D.C. Power input cord set
	2	5322 255 40331	Heatsink for V217/V218 on unit A2
	1	5322 401 10793	S-clip for V2504/V2506 on UNIT A10
	1	5322 466 30124	Magnetic shield for C.R.T.
	1	5322 492 64767	Clamping strip for C.R.T.
	1	4822 502 11154	Screw for C.R.T. clamping strip
	1	5322 505 10706	Square nut for C.R.T. clamping strip
	1	5322 532 74014	C.R.T. (rubber C.R.T. socket)
	3	5322 528 20333	Coupling disc for R7/S7 - R8/S9 - R9/S11
	3	5322 532 60758	Coupling bush for R7/S7 - R8/S9 - R9/S11
	3	5322 528 20335	Coupling disc for R7/S7 - R8/S9 - R9/S11
	3	5322 532 11068	Ring for R7/S7 - R8/S9 - R9/S11
	6	5322 466 94649	Plastic coupling plate for A304 - A305 - A306

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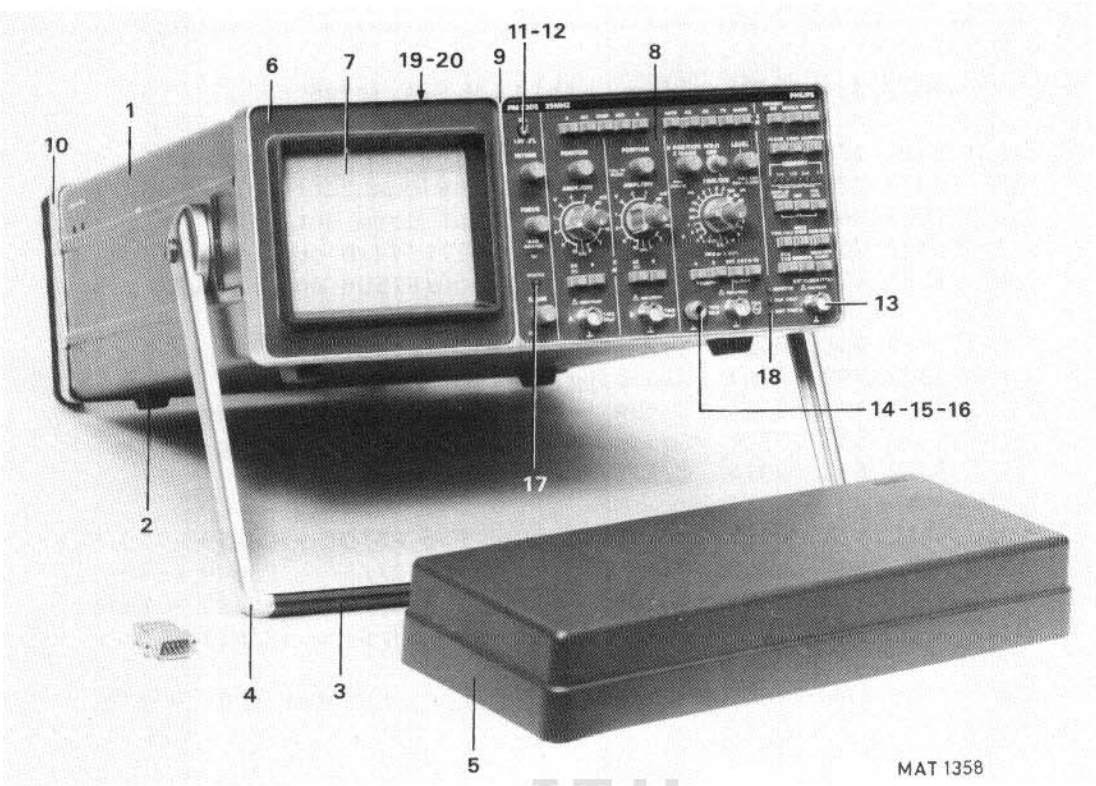

FIG. 9.1. Front view showing item numbers.

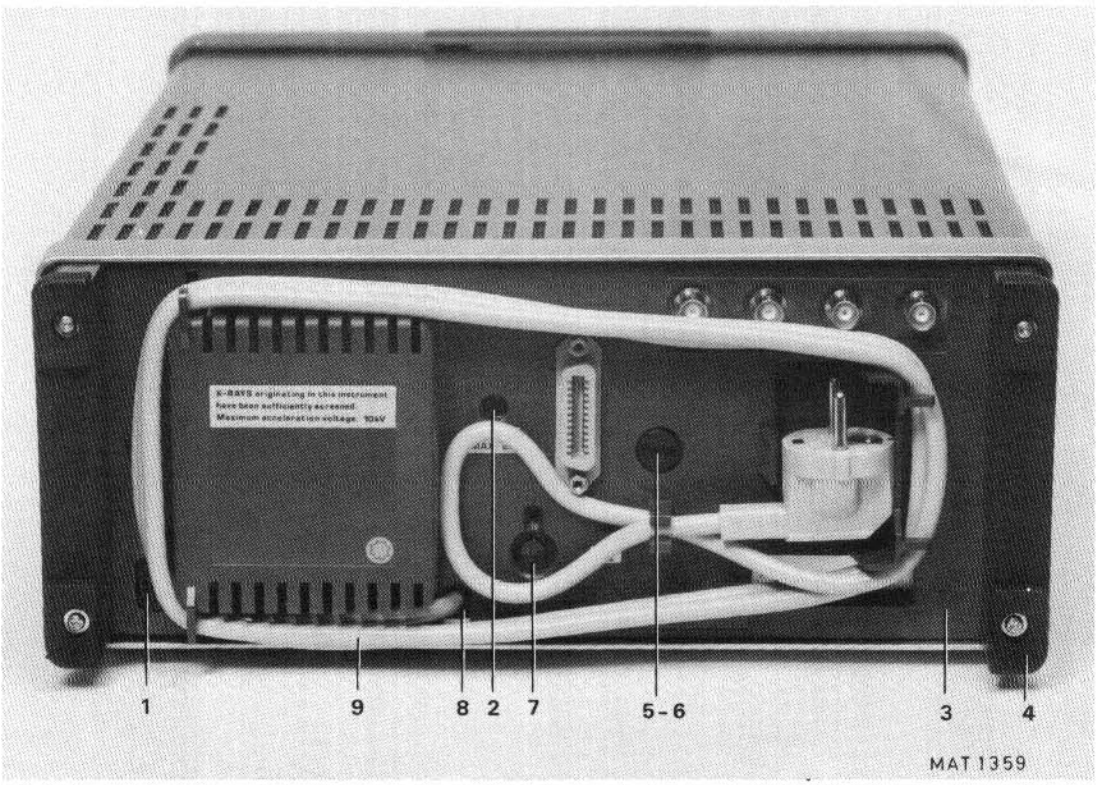

FIG. 9.2. Rear view showing item numbers.

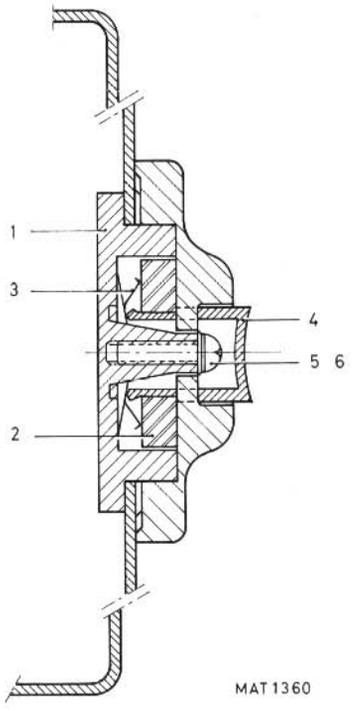

FIG. 9.3. Handle itemnumbers.

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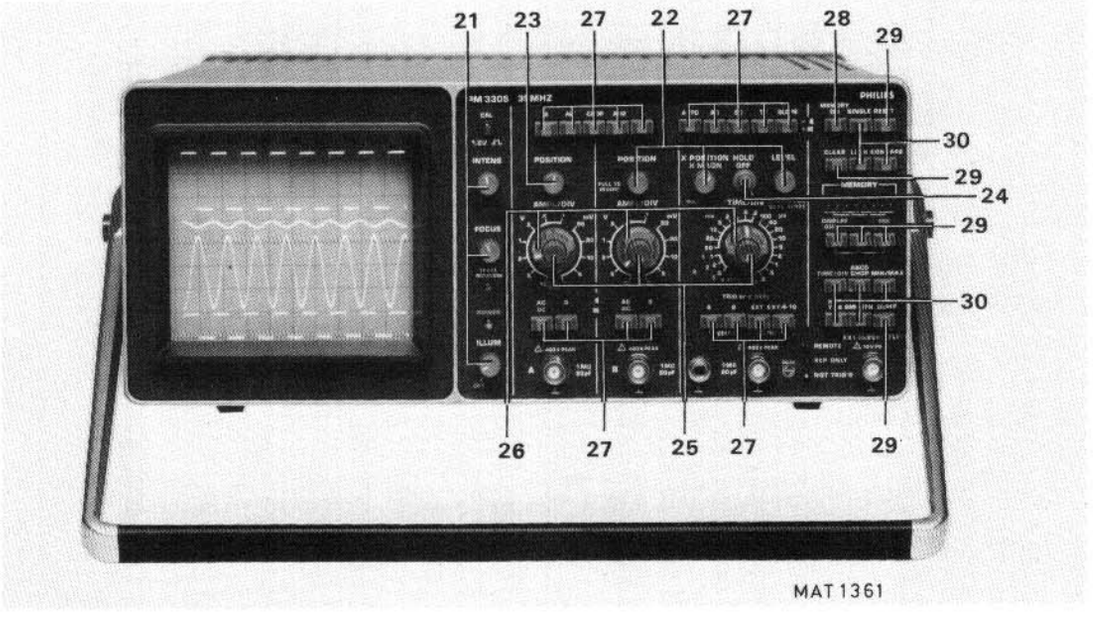

FIG. 9.4. Knobs.

9.2. ELECTRICAL PARTS

UNITS

1	5322 219 80576	A1	AC power unit
1	5322 216 51032	A2	DC power print unit
1	5322 219 80577	A3	Frontplate unit
1	5322 216 51039	A301	Attenuator print
1	5322 105 34034	A302	Attenuator switch unit (2x att. switch + components)
1	5322 282 10198	A303	TB switch unit (switch + components)
1	5322 276 60221	A304	Memory switch unit + cable
1	5322 219 80578	A305	Led bar unit + cables
1	5322 276 60222	A306	Smooth switch unit
1	5322 216 51051	A307	Triple led unit
1	5322 320 40097	A7	Delay line unit
1	5322 216 51033	A8	5V DC print unit
1	5322 216 51034	A9	Adaption print unit
1	5322 216 51035	A10	MIN/MAX print unit
1	5322 216 51036	A11	Logic print unit
1	5322 216 51049	A1103	T&H unit
1	5322 216 51037	A12	Aux. channel unit
1	5322 219 80579	A13	EHT unit (D201)
1	5322 216 51038	A14	IEEE INTERFACE print unit (optional)

Capacitors

POSNR	DESCRIPTION			ORDERING CODE
C 10	SOCKET,LED	LED HOLDER		5322 255 40231
C 1001	CAPACITOR,FOIL	470NF 10%	100V	4822 121 40438
C 1002	CAPACITOR,FOIL	470NF 10%	100V	4822 121 40438
C 1003	CAPACITOR,FOIL	220NF 10%	100V	4822 121 40427
C 1004	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1006	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 1007	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1008	CAPACITOR,CERAM	0,56PF 0,25PF	100	5322 122 34039
C 101	CAPACITOR,PAPER	220NF 10%	250V	5322 121 44142
C 1011	CAPACITOR,CERAM	4,7NF 10	100	4822 122 30128
C 1012	CAPACITOR,CERAM	4,7NF 10	100	4822 122 30128
C 1013	CAPACITOR,CERAM	3,9NF 10	100	4822 122 30098
C 1016	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 1017	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1018	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 1019	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 1201	CAPACITOR,CERAM	150PF 2	100	4822 122 31085
C 1202	CAPACITOR,FOIL	150NF 10%	100V	4822 121 40423
C 1203	CAPACITOR,CERAM	270PF 10	100	4822 122 30095
C 1204	CAPACITOR,FOIL	2.4NF 1%	63V	5322 121 54054
C 1205	CAPACITOR,CERAM	82PF 2	100	4822 122 31243
C 1206	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1207	CAPACITOR,FOIL	2.2UF 5%	100V	5322 121 44246
C 1208	CAP,ELECTROLYT.	4,7UF-10+50	63	4822 124 20726
C 1209	CAPACITOR,CERAM	1NF 10	100	4822 122 30027
C 1210	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1211	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1212	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1213	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 1214	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 1216	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 1401	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1402	CAPACITOR,CERAM	1NF 10	100	4822 122 30027
C 1404	CAPACITOR,FOIL	220NF 10%	100V	4822 121 40427
C 1406	CAPACITOR,CERAM	0,56PF 0,25PF	100	5322 122 34039
C 1407	CAPACITOR,CERAM	0,56PF 0,25PF	100	5322 122 34039
C 1408	CAPACITOR,CERAM	0,56PF 0,25PF	100	5322 122 34039
C 1409	CAPACITOR,TRIMM	3,5PF		5322 125 50048
C 1411	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1412	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1413	CAPACITOR,FOIL	22NF 10%	250V	4822 121 40407
C 1414	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1416	CAPACITOR,FOIL	22NF 10%	250V	4822 121 40407
C 1417	CAPACITOR,FOIL	100NF 10%	250V	4822 121 41161
C 1418	CAPACITOR,FOIL	100NF 10%	250V	4822 121 41161
C 1419	CAPACITOR,FOIL	100NF 10%	250V	4822 121 41161
C 1421	CAPACITOR,FOIL	100NF 10%	250V	4822 121 41161
C 1501	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1502	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1503	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1504	CAPACITOR,CERAM	1PF 0,25PF	100	4822 122 30104
C 1506	CAPACITOR,CERAM	10NF-20+80	40	4822 122 30043
C 1507	CAPACITOR,FOIL	10NF	630V	4822 121 41134
C 1508	CAPACITOR,CERAM	3,3NF 10	100	4822 122 30099
C 1509	CAPACITOR,FOIL	1,5NF 10%	1600V	4822 121 40354
C 1511	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 1512	CAPACITOR,FOIL	1,5NF 10%	1600V	4822 121 40354
C 1513	CAPACITOR,FOIL	1,5NF 10%	1600V	4822 121 40354
C 1601	CAPACITOR,FOIL	330NF 10%	100V	4822 121 40434
C 1602	CAPACITOR,CERAM	47PF 2	100	4822 122 31072
C 1701	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1702	CAPACITOR,CERAM	10PF 2	100	4822 122 31054

POSNR	DESCRIPTION			ORDERING CODE
C 1703	CAPACITOR,CERAM	10PF 2	100	4822 122 31054
C 1704	CAPACITOR,FOIL	1NF 1%	630V	4822 121 50591
C 1706	CAPACITOR,CERAM	220PF 2	100	4822 122 31506
C 1707	CAPACITOR,CERAM	33PF 2	100	4822 122 31067
C 1708	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1709	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1710	CAPACITOR,CERAM	1NF 10	100	4822 122 30027
C 1751	CAPACITOR,FOIL	1NF 1%	630V	4822 121 50591
C 1752	CAPACITOR,CERAM	220PF 2	100	4822 122 31506
C 1753	CAPACITOR,CERAM	33PF 2	100	4822 122 31067
C 1754	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1755	CAPACITOR,CERAM	1NF 10	100	4822 122 30027
C 1756	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1801	CAPACITOR,CERAM	220PF 2	100	4822 122 31506
C 1802	CAPACITOR,CERAM	220PF 2	100	4822 122 31506
C 1851	CAP,ELECTROLYT.	33UF-10+50	16	4822 124 20688
C 1852	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1853	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1854	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1855	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 1857	CAP,ELECTROLYT.	33UF-10+50	16	4822 124 20688
C 1858	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1859	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1862	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1863	CAP,ELECTROLYT.	33UF-10+50	16	4822 124 20688
C 1864	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1866	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1867	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1868	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1869	CAP,ELECTROLYT.	33UF-10+50	16	4822 124 20688
C 1871	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1872	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1873	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1901	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1902	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 1903	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1904	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 1905	CAPACITOR,CERAM	150PF 2	100	4822 122 31085
C 1906	CAPACITOR,CERAM	150PF 2	100	4822 122 31085
C 1907	CAPACITOR,CERAM	330PF 2	100	5322 122 34148
C 1908	CAPACITOR,CERAM	330PF 2	100	5322 122 34148
C 1909	CAPACITOR,CERAM	330PF 2	100	5322 122 34148
C 1910	CAPACITOR,CERAM	330PF 2	100	5322 122 34148
C 1931	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 200	CAPACITOR,FOIL	100NF 10%	100V	5322 121 40323
C 2001	CAPACITOR,CERAM	470PF 10	100	4822 122 30034
C 2003	CAPACITOR,CERAM	330PF 2	100	5322 122 34148
C 2004	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2006	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2007	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2008	CAP,ELECTROLYT.	220UF-10+50	10	4822 124 20681
C 2009	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 201	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 2010	CAP,ELECTROLYT.	33UF 40%	10V	4822 124 20945
C 2011	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2012	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2013	CAPACITOR,CERAM	18PF 2	100	4822 122 31061
C 2014	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2015	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2016	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2017	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2018	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2019	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 202	CAPACITOR,FOIL	680NF 10%	100V	5322 121 40233
C 2021	CAPACITOR,CERAM	47PF 2	100	4822 122 31072

POSNR	DESCRIPTION			ORDERING CODE
C 2022	CAPACITOR,CERAM	100PF 2	100	4822 122 31504
C 2023	CAPACITOR,CERAM	100PF 2	100	4822 122 31504
C 2024	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2026	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2027	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2028	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2029	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 203	CAP,ELEC.TANTAL	4700UF-10+30	40	4822 124 70326
C 2031	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2032	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2033	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2034	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2035	CAPACITOR,CERAM	470PF 10	100	4822 122 30034
C 2036	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2037	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2038	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2039	CAPACITOR,CERAM	18PF 2	100	4822 122 31061
C 204	CAPACITOR,FOIL	100NF 10%	100V	5322 121 40323
C 2040	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2041	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2042	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2043	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2044	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2046	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2047	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2048	CAPACITOR,CERAM	33PF 2	100	4822 122 31067
C 2049	CAP,ELEC.TANTAL	6,8UF 20%	16V	5322 124 14069
C 2050	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2051	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2052	CAPACITOR,CERAM	5,6PF 0,25PF	100	4822 122 31047
C 2053	CAPACITOR,CERAM	4,7NF 10	100	4822 122 30128
C 2054	CAPACITOR,CERAM	4,7NF 10	100	4822 122 30128
C 2056	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2057	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2058	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2059	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 206	CAP,ELECTROLYT.	3,3UF-10+50	63	4822 124 20725
C 2061	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2062	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2063	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2064	CAP,ELEC.TANTAL	2,2UF 20%	16V	4822 124 10204
C 2066	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2067	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2068	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2069	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 207	CAPACITOR,FOIL	680NF 10%	100V	5322 121 40233
C 2071	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2072	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 208	CAP,ELECTROLYT.	47UF-10+50	25	4822 124 20699
C 209	CAP,ELECTROLYT.	10UF-10+50	63	4822 124 20728
C 211	CAP,ELECTROLYT.	68UF-10+50	16	4822 124 20689
C 218	CAPACITOR,FOIL	22NF 10%	1600V	4822 121 40196
C 219	CAPACITOR,FOIL	22NF 10%	1600V	4822 121 40196
C 221	CAP,ELECTROLYT.	4,7UF-10+50	250	4822 124 21157
C 222	CAP,ELECTROLYT.	100UF-10+50	40	4822 124 20715
C 223	CAP,ELECTROLYT.	150UF-10+50	16	4822 124 20586
C 224	CAP,ELECTROLYT.	150UF-10+50	16	4822 124 20586
C 226	CAP,ELECTROLYT.	68UF-10+50	6,3	4822 124 20671
C 227	CAP,ELECTROLYT.	470UF-10+50	6,3	4822 124 20673
C 228	CAP,ELECTROLYT.	150UF-10+50	16	4822 124 20586
C 229	CAP,ELECTROLYT.	150UF-10+50	16	4822 124 20586
C 2301	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2302	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2303	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2304	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414

POSNR	DESCRIPTION			ORDERING CODE
C 2306	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2307	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2308	CAP,ELECTROLYT.	33UF-10+50	16	4822 124 20688
C 2309	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 231	CAP,ELECTROLYT.	4,7UF-10+50	250	4822 124 21157
C 2311	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2312	CAP,ELECTROLYT.	33UF-10+50	16	4822 124 20688
C 2324	POTM,TRIMMING	220E CERM LIN	0,5W	5322 101 14009
C 2351	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2352	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2353	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2354	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2374	POTM,TRIMMING	220E CERM LIN	0,5W	5322 101 14009
C 2500	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2501	CAPACITOR,CERAM	22PF 2	100	4822 122 31063
C 2503	CAPACITOR,CERAM	22PF 2	100	4822 122 31063
C 2504	CAPACITOR,CERAM	150PF 2	100	4822 122 31085
C 2506	CAPACITOR,CERAM	150PF 2	100	4822 122 31085
C 2508	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2509	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 251	CAP,ELECTROLYT.	1000UF-10+50	10	5322 124 24249
C 2510	CAPACITOR,CERAM	1NF 10	100	4822 122 30027
C 2512	CAPACITOR,CERAM	22PF 2	100	4822 122 31063
C 2513	CAPACITOR,CERAM	100PF 2	100	4822 122 31504
C 2514	CAPACITOR,CERAM	22PF 2	100	4822 122 31063
C 2515	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2516	CAPACITOR,CERAM	22PF 2	100	4822 122 31063
C 2517	CAPACITOR,CERAM	100PF 2	100	4822 122 31504
C 2518	CAPACITOR,CERAM	22PF 2	100	4822 122 31063
C 252	CAP,ELECTROLYT.	100UF-10+50	10	5322 124 24268
C 2520	CAPACITOR,CERAM	1NF 10	100	4822 122 30027
C 2521	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2523	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2524	CAPACITOR,CERAM	150PF 2	100	4822 122 31085
C 2525	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2526	CAPACITOR,CERAM	680PF 10	100	4822 122 30053
C 2527	CAPACITOR,CERAM	150PF 2	100	4822 122 31085
C 2528	CAPACITOR,CERAM	680PF 10	100	4822 122 30053
C 2529	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2530	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2531	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2532	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2533	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2534	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2536	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2537	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 2538	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2539	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2542	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 2543	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 2544	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 2547	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 2548	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2549	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2551	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414

POSNR	DESCRIPTION			ORDERING CODE
C 2552	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 2553	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2554	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2556	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2557	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 2558	CAP,ELEC.TANTAL	6,8UF 20%	25V	5322 124 14081
C 2559	CAP,ELECTROLYT.	33UF 40%	10V	4822 124 20945
C 2562	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2563	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2564	CAP,ELECTROLYT.	33UF 40%	10V	4822 124 20945
C 2566	CAP,ELECTROLYT.	33UF 40%	10V	4822 124 20945
C 2567	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2568	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2569	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2571	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2572	CAP,ELECTROLYT.	33UF 40%	10V	4822 124 20945
C 2573	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2574	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2576	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 2577	CAP,ELECTROLYT.	33UF 40%	10V	4822 124 20945
C 2578	CAP,ELECTROLYT.	33UF 40%	10V	4822 124 20945
C 2691	CAPACITOR,CERAM	1NF 10	100	4822 122 30027
C 301	CAPACITOR,FOIL	100NF 10%	400V	4822 121 40012
C 305	CAPACITOR,CERAM	47PF 2	500	4822 122 31072
C 307	CAPACITOR,TRIMM	2,0-18P TRIM		5322 125 50051
C 308	CAPACITOR,CERAM	47PF 2	500	4822 122 31072
C 309	CAPACITOR,CERAM	15PF 2	500	4822 122 31197
C 310	CAPACITOR,CERAM	15PF 2	500	4822 122 31197
C 311	CAPACITOR,CERAM	12PF 2	500	4822 122 31196
C 312	CAPACITOR,CERAM	3,9PF 0,25PF	500	4822 122 31217
C 313	CAPACITOR,TRIMM	5,5PF		5322 125 54027
C 314	CAPACITOR,TRIMM	5,5PF		5322 125 54027
C 315	CAPACITOR,CERAM	1,5PF 0,25PF	500	4822 122 31184
C 316	CAPACITOR,TRIMM	3PF		5322 125 54026
C 317	CAPACITOR,TRIMM	3PF		5322 125 54026
C 318	CAPACITOR,TRIMM	3PF		5322 125 54026
C 319	CAPACITOR,TRIMM	3PF		5322 125 54026
C 320	CAPACITOR,CERAM	3,3PF 0,25PF	500	4822 122 31188
C 321	CAPACITOR,CERAM	27PF 2	100	4822 122 30045
C 322	CAPACITOR,CERAM	120PF 2	100	4822 122 31348
C 324	CAPACITOR,CERAM	120PF 2	100	4822 122 31348
C 351	CAPACITOR,CERAM	39PF 2	500	4822 122 31203
C 353	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 354	CAPACITOR,CERAM	2,2PF 0,25PF	100	5322 122 34198
C 356	CAPACITOR,FOIL	150NF 10%	100V	4822 121 40423
C 357	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 358	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 359	CAPACITOR,CERAM	15PF 2	500	4822 122 31197
C 361	CAPACITOR,CERAM	18PF 2	500	4822 122 31198
C 362	CAPACITOR,CERAM	150PF 2	100	4822 122 31413
C 401	CAPACITOR,FOIL	100NF 10%	400V	4822 121 40012
C 405	CAPACITOR,CERAM	47PF 2	500	4822 122 31072
C 407	CAPACITOR,TRIMM	2,0-18P TRIM		5322 125 50051
C 408	CAPACITOR,CERAM	47PF 2	500	4822 122 31072
C 409	CAPACITOR,CERAM	15PF 2	500	4822 122 31197
C 410	CAPACITOR,CERAM	15PF 2	500	4822 122 31197
C 411	CAPACITOR,CERAM	12PF 2	500	4822 122 31196
C 412	CAPACITOR,CERAM	3,9PF 0,25PF	500	4822 122 31217
C 413	CAPACITOR,TRIMM	5,5PF		5322 125 54027
C 414	CAPACITOR,TRIMM	5,5PF		5322 125 54027
C 415	CAPACITOR,CERAM	1,5PF 0,25PF	500	4822 122 31184
C 416	CAPACITOR,TRIMM	3PF		5322 125 54026
C 417	CAPACITOR,TRIMM	3PF		5322 125 54026
C 418	CAPACITOR,TRIMM	5,5PF		5322 125 54027
C 419	CAPACITOR,TRIMM	3PF		5322 125 54026

POSNR	DESCRIPTION			ORDERING CODE
C 420	CAPACITOR,CERAM	3,3PF 0,25PF	500	4822 122 31188
C 421	CAPACITOR,CERAM	27PF 2	100	4822 122 30045
C 422	CAPACITOR,CERAM	120PF 2	100	4822 122 31348
C 424	CAPACITOR,CERAM	120PF 2	100	4822 122 31348
C 451	CAPACITOR,CERAM	10NF-20+50	100	4822 122 31414
C 501	CAPACITOR,CERAM	47PF 2	100	4822 122 31072
C 502	CAPACITOR,TRIMM	20PF		4822 125 50045
C 503	CAPACITOR,CERAM	180PF 2	100	4822 122 31352
C 504	CAPACITOR,CERAM	5,6PF 0,25PF	100	4822 122 31047
C 507	CAPACITOR,TRIMM	3,5PF		5322 125 50048
C 509	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 510	CAPACITOR,CERAM	33PF 2	100	4822 122 31067
C 511	CAPACITOR,CERAM	18PF 2	100	4822 122 31061
C 513	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 517	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 518	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 519	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 521	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 522	CAPACITOR,CERAM	150PF 2	100	4822 122 31085
C 523	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 524	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 527	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 528	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 529	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 530	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 531	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 532	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 601	CAPACITOR,CERAM	47PF 2	100	4822 122 31072
C 602	CAPACITOR,TRIMM	20PF		4822 125 50045
C 603	CAPACITOR,CERAM	180PF 2	100	4822 122 31352
C 604	CAPACITOR,CERAM	5,6PF 0,25PF	100	4822 122 31047
C 607	CAPACITOR,TRIMM	3,5PF		5322 125 50048
C 609	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 610	CAPACITOR,CERAM	33PF 2	100	4822 122 31067
C 611	CAPACITOR,CERAM	10PF 2	100	4822 122 31054
C 613	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 616	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 617	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 618	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 619	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 621	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 622	CAPACITOR,CERAM	150PF 2	100	4822 122 31085
C 623	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 627	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 629	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 630	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 631	CAP,ELECTROLYT.	15UF-10+50	16	4822 124 20687
C 632	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 701	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 702	CAPACITOR,CERAM	270PF 10	100	4822 122 30095
C 703	CAPACITOR,CERAM	2,7NF 10	100	4822 122 30057
C 704	CAPACITOR,CERAM	2,7NF 10	100	4822 122 30057
C 705	CAPACITOR,CERAM	4,7NF-20+80	40	4822 122 31125
C 706	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 707	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103

POSNR	DESCRIPTION			ORDERING CODE
C 801	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 802	CAPACITOR,CERAM	18PF 2	100	4822 122 31061
C 803	CAPACITOR,FOIL	10NF	630V	4822 121 41134
C 804	CAPACITOR,CERAM	180PF 2	100	4822 122 31352
C 805	CAPACITOR,CERAM	1PF 0,25PF	100	4822 122 30104
C 806	CAPACITOR,CERAM	1NF 10	100	4822 122 30027
C 807	CAPACITOR,CERAM	56PF 2	100	4822 122 31521
C 808	CAPACITOR,CERAM	47PF 2	100	4822 122 31072
C 809	CAPACITOR,TRIMM	40PF		4822 125 50092
C 810	CAPACITOR,CERAM	1PF 0,25PF	100	4822 122 30104
C 811	CAPACITOR,TRIMM	40PF		4822 125 50092
C 812	CAPACITOR,CERAM	33PF 2	100	4822 122 31067
C 813	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 814	CAPACITOR,CERAM	10PF 2	100	4822 122 31054
C 815	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103
C 816	CAPACITOR,CERAM	10PF 2	100	4822 122 31054
C 818	CAPACITOR,TRIMM	3,5PF		5322 125 50048
C 821	CAPACITOR,CERAM	22NF-20+80	40	4822 122 30103

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Integrated Circuits

POSNR	DESCRIPTION		ORDERING CODE
D 451	INTEGR.CIRCUIT	N74LS164N	5322 209 81487
D 1001	INTEGR.CIRCUIT	SL3145E	5322 130 34854
D 1201	INTEGR.CIRCUIT	N74LS132N	5322 209 85201
D 1202	INTEGR.CIRCUIT	N74S00N	5322 209 84167
D 1203	INTEGR.CIRCUIT	N74S10N	5322 209 84954
D 1801	INTEGR.CIRCUIT	GXB10116P	5322 209 86441
D 1802	INTEGR.CIRCUIT	LM358N	4822 209 81472
D 1803	INTEGR.CIRCUIT	UA 741 CN	4822 209 80617
D 1804	INTEGR.CIRCUIT	LM78L05ACZ	5322 209 80903
D 1805	INTEGR.CIRCUIT	LM79L05ACZ	5322 209 86434
D 1901	INTEGR.CIRCUIT	N74LS139N	5322 209 85839
D 1902	INTEGR.CIRCUIT	74LS04	4822 209 80783
D 1903	INTEGR.CIRCUIT	SD5000N	5322 209 85748
D 1931	INTEGR.CIRCUIT	SN74S132N-00	5322 209 85267
D 2001	INTEGR.CIRCUIT	N74S151N	5322 209 85453
D 2002	INTEGR.CIRCUIT	SN74S163N-00	5322 209 85454
D 2004	INTEGR.CIRCUIT	74LS04	4822 209 80783
D 2006	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2007	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2008	INTEGR.CIRCUIT	74LS257	5322 209 86392
D 2009	INTEGR.CIRCUIT	AD7541JN	5322 209 86245
D 201	UNIT,ELECTRICAL	R	5322 218 61003
D 2011	INTEGR.CIRCUIT	HEF4021BP	4822 209 10049
D 2012	INTEGR.CIRCUIT	N74LS160AN	5322 209 81079
D 2013	INTEGR.CIRCUIT	74LS08	5322 209 84995
D 2014	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 2016	INTEGR.CIRCUIT	NE521N	5322 209 14441
D 2017	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 2018	INTEGR.CIRCUIT	74LS08	5322 209 84995
D 2019	INTEGR.CIRCUIT	SN74LS298N-00	5322 209 85937
D 2021	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2022	INTEGR.CIRCUIT	74LS257	5322 209 86392
D 2023	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2024	INTEGR.CIRCUIT	LF357N	5322 209 80861
D 2026	INTEGR.CIRCUIT	74LS04	4822 209 80783
D 2027	INTEGR.CIRCUIT	N74S02N	5322 209 85407
D 2028	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2029	INTEGR.CIRCUIT	N74LS20N	5322 209 85569
D 2031	INTEGR.CIRCUIT	SN74S74N-00	5322 209 84183
D 2032	INTEGR.CIRCUIT	74LS30	5322 209 84985
D 2033	INTEGR.CIRCUIT	74LS32	5322 209 85311
D 2034	INTEGR.CIRCUIT	SN74LS374N-00	5322 209 85869
D 2036	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2037	INTEGR.CIRCUIT	74LS257	5322 209 86392
D 2038	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2039	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2041	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2042	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2043	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2044	INTEGR.CIRCUIT	GXB10114P	5322 209 81525
D 2046	INTEGR.CIRCUIT	HEF4021BP	4822 209 10049
D 2047	INTEGR.CIRCUIT	74LS08	5322 209 84995
D 2048	INTEGR.CIRCUIT	LM324N	4822 209 80587
D 2049	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2051	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 2052	INTEGR.CIRCUIT	SN74S74N-00	5322 209 84183
D 2053	INTEGR.CIRCUIT	N74LS10N	5322 209 84996

POSNR	DESCRIPTION		ORDERING CODE
D 2054	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 2056	INTEGR.CIRCUIT	SN74LS374N-00	5322 209 85869
D 2057	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2058	INTEGR.CIRCUIT	74LS257	5322 209 86392
D 2059	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2061	INTEGR.CIRCUIT	N74S00N	5322 209 84167
D 2062	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 2063	INTEGR.CIRCUIT	N74LS11N	5322 209 85604
D 2064	INTEGR.CIRCUIT	P8155H-2	5322 209 10402
D 2066	INTEGR.CIRCUIT	SN74S74N-00	5322 209 84183
D 2067	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 2068	INTEGR.CIRCUIT	74LS04	4822 209 80783
D 2069	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 2070	INTEGR.CIRCUIT	LF357N	5322 209 80861
D 2071	INTEGR.CIRCUIT	AD7541JN	5322 209 86245
D 2072	INTEGR.CIRCUIT	N74LS86N	5322 209 84997
D 2073	INTEGR.CIRCUIT	N74LS153N	5322 209 85488
D 2074	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2076	INTEGR.CIRCUIT	N74S32N	5322 209 85679
D 2077	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2078	INTEGR.CIRCUIT	HEF4021BP	4822 209 10049
D 2079	INTEGR.CIRCUIT	74LS32	5322 209 85311
D 2081	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 2082	INTEGR.CIRCUIT		5322 209 50091
D 2082	INTEGR.CIRCUIT	PROM ASSY	5322 209 50091
D 2083	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2084	INTEGR.CIRCUIT	SN74S74N-00	5322 209 84183
D 2086	INTEGR.CIRCUIT	N74S03N	5322 209 84321
D 2087	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2088	INTEGR.CIRCUIT	SN74LS157N-00	5322 209 85489
D 2089	INTEGR.CIRCUIT	HM6116LP-4	5322 209 81081
D 2091	INTEGR.CIRCUIT	HM6116LP-4	5322 209 81081
D 2092	INTEGR.CIRCUIT	GATE	5322 209 81528
D 2093	INTEGR.CIRCUIT	74LS08	5322 209 84995
D 2094	INTEGR.CIRCUIT	74LS04	4822 209 80783
D 2096	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 2098	INTEGR.CIRCUIT	SN74S74N-00	5322 209 84183
D 2099	INTEGR.CIRCUIT	N74LS86N	5322 209 84997
D 2101	INTEGR.CIRCUIT	SN74LS245N-00	5322 209 86225
D 2102	INTEGR.CIRCUIT	HM6116LP-4	5322 209 81081
D 2103	INTEGR.CIRCUIT	HM6116LP-4	5322 209 81081
D 2104	INTEGR.CIRCUIT	HEF4021BP	4822 209 10049
D 2106	INTEGR.CIRCUIT	74LS32	5322 209 85311
D 2107	INTEGR.CIRCUIT	N74LS163AN	5322 209 85863
D 2109	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 2111	INTEGR.CIRCUIT	74LS244	5322 209 86017
D 2112	INTEGR.CIRCUIT	TDC1001J	5322 209 81526
D 2113	INTEGR.CIRCUIT	N74LS138N	5322 209 85647
D 2116	INTEGR.CIRCUIT	74LS244	5322 209 86017
D 2117	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 2118	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 2119	INTEGR.CIRCUIT	SN74LS123N-00	5322 209 85266
D 2121	INTEGR.CIRCUIT	P8085-AH	5322 209 50032
D 2122	INTEGR.CIRCUIT	74LS244	5322 209 86017
D 2123	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 2124	INTEGR.CIRCUIT	N74LS283N	5322 209 86052
D 2126	INTEGR.CIRCUIT	NE5008N	5322 209 85791
D 2127	INTEGR.CIRCUIT	74LS244	5322 209 86017
D 2128	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 2129	INTEGR.CIRCUIT	N74LS283N	5322 209 86052
D 2131	INTEGR.CIRCUIT	LM358N	4822 209 81472
D 2501	INTEGR.CIRCUIT	OQ 0012	5322 209 85484
D 2502	INTEGR.CIRCUIT	CA3086	5322 209 86236
D 2503	INTEGR.CIRCUIT		5322 209 81527
D 2504	INTEGR.CIRCUIT		5322 209 81527

POSNR	DESCRIPTION		ORDERING CODE
D 2506	INTEGR.CIRCUIT	LM358N	4822 209 81472
D 2507	INTEGR.CIRCUIT	OQ 0012	5322 209 85484
D 2508	INTEGR.CIRCUIT	OQ 0012	5322 209 85484
D 2509	INTEGR.CIRCUIT	CA3086	5322 209 86236
D 2511	INTEGR.CIRCUIT	74LS04	4822 209 80783
D 2512	INTEGR.CIRCUIT	74LS74A	4822 209 80782
D 2513	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 501	INTEGR CIRCUIT	ARRAY OQ-0145	5322 209 81324
D 601	INTEGR.CIRCUIT	ARRAY OQ-0145	5322 209 81324
D 801	INTEGR.CIRCUIT	ARRAY OQ-0145	5322 209 81324

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Resistors

POSNR	DESCRIPTION				ORDERING CODE
R 1	POTM,CARBON	10K	20	0.1W	5322 101 24117
R 10	POTM,CARBON	100K	20	0,1W	5322 101 24178
R 1001	RESISTOR,M.FILM	110K	1	MR25	5322 116 54701
R 1002	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 1003	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 1004	RESISTOR,M.FILM	110K	1	MR25	5322 116 54701
R 1006	RESISTOR,M.FILM	3,65K	1	MR25	5322 116 54587
R 1007	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 1008	RESISTOR,M.FILM	301K	1	MR25	5322 116 54743
R 1009	RESISTOR,M.FILM	511K	1	MR30	5322 116 55636
R 1011	RESISTOR,M.FILM	4,02K	1	MR25	5322 116 55448
R 1012	RESISTOR,M.FILM	100K	1	MR25	4822 116 51268
R 1013	RESISTOR,M.FILM	12,7K	1	MR25	5322 116 50443
R 1014	POTM,TRIMMING	470	20	0,5W	5322 101 14047
R 1016	RESISTOR,M.FILM	12,7K	1	MR25	5322 116 50443
R 1017	RESISTOR,M.FILM	2,87K	1	MR25	5322 116 55279
R 1018	RESISTOR,M.FILM	562	1	MR25	4822 116 51231
R 1019	RESISTOR,M.FILM	562	1	MR25	4822 116 51231
R 1021	RESISTOR,M.FILM	3,65K	1	MR25	5322 116 54587
R 1022	RESISTOR,M.FILM	1,54K	1	MR25	5322 116 50586
R 1023	RESISTOR,M.FILM	1,54K	1	MR25	5322 116 50586
R 1024	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 1026	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 1027	RESISTOR,M.FILM	619	1	MR25	4822 116 51232
R 1028	RESISTOR,M.FILM	619	1	MR25	4822 116 51232
R 1029	RESISTOR,M.FILM	10,5K	1	MR25	5322 116 50731
R 1031	RESISTOR,M.FILM	4,02K	1	MR25	5322 116 55448
R 1032	RESISTOR,M.FILM	12,1K	1	MR25	5322 116 50572
R 1033	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1034	RESISTOR,M.FILM	16,2K	1	MR25	5322 116 55361
R 1036	RESISTOR,M.FILM	3,65K	1	MR25	5322 116 54587
R 1037	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 1038	RESISTOR,M.FILM	2,61K	1	MR25	5322 116 50671
R 1039	RESISTOR,M.FILM	1M	1	MR30	4822 116 51279
R 1041	POTM,TRIMMING	22K	20	0.5W	5322 101 14069
R 1042	RESISTOR,M.FILM	20,5K	1	MR25	5322 116 54643
R 1043	RESISTOR,M.FILM	1,4K	1	MR25	5322 116 54562
R 1044	RESISTOR,M.FILM	1,87K	1	MR25	5322 116 50728
R 1046	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1047	RESISTOR,M.FILM	3,01K	1	MR25	4822 116 51246
R 1048	RESISTOR,M.FILM	1M	1	MR30	4822 116 51279
R 1049	RESISTOR,M.FILM	4,64K	1	MR25	5322 116 50484
R 1051	RESISTOR,M.FILM	196K	1	MR25	5322 116 55364
R 1052	RESISTOR,M.FILM	5,9K	1	MR25	5322 116 50583
R 1053	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 1054	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 1056	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 11	POTM,CARB+SW.	22K	20	0.1W	5322 101 44025
R 12	POTM,CARBON	47K	20	0.1W	5322 101 24197
R 1201	RESISTOR,M.FILM	100K	1	MR25	4822 116 51268
R 1202	RESISTOR,M.FILM	48,7K	1	MR25	5322 116 50442
R 1203	RESISTOR,M.FILM	3,48K	1	MR25	5322 116 55367
R 1204	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 1207	RESISTOR,M.FILM	10	1	MR25	5322 116 50452
R 1208	RESISTOR,HT	3,3M	10	CR25	4822 110 72201

POSNR	DESCRIPTION				ORDERING CODE
R 1209	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1211	RESISTOR,M.FILM	2,49K	1	MR25	5322 116 50581
R 1212	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1213	RESISTOR,M.FILM	681	1	MR25	4822 116 51233
R 1214	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 1216	RESISTOR,M.FILM	1,05K	1	MR25	5322 116 54552
R 1217	RESISTOR,SAFETY	7,87K	1	MR25	5322 116 50458
R 1218	RESISTOR,M.FILM	32,4	0,5	MR25	5322 116 55421
R 1219	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 1220	RESISTOR,M.FILM	9,09	1	MR25	5322 116 50863
R 1221	RESISTOR,M.FILM	1,4K	1	MR25	5322 116 54562
R 1222	RESISTOR,M.FILM	9,53K	1	MR25	5322 116 54617
R 1223	RESISTOR,M.FILM	15,4K	1	MR25	5322 116 55459
R 1224	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 1226	RESISTOR,M.FILM	1,54K	1	MR25	5322 116 50586
R 1227	RESISTOR,M.FILM	7,5K	1	MR25	5322 116 54608
R 1228	RESISTOR,SAFETY	7,87K	1	MR25	5322 116 50458
R 1229	RESISTOR,M.FILM	37,4K	1	MR25	5322 116 54663
R 1230	RESISTOR,M.FILM	26,1K	1	MR25	5322 116 54651
R 1231	RESISTOR,M.FILM	33,2K	1	MR25	4822 116 51259
R 1232	POTM,TRIMMING	22K	20	0.05W	4822 100 10051
R 1233	RESISTOR,M.FILM	348	1	MR25	5322 116 54515
R 1234	RESISTOR,M.FILM	2,26K	1	MR25	5322 116 50675
R 1236	RESISTOR,M.FILM	21,5K	1	MR25	5322 116 50451
R 1237	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 1238	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 1239	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 1276	RESISTOR,M.FILM	412K	0,5	MR25	5322 116 55424
R 1277	RESISTOR,M.FILM	205K	0,5	MR25	5322 116 55387
R 1278	RESISTOR,M.FILM	41,2K	0,5	MR25	5322 116 55423
R 1279	RESISTOR,M.FILM	8,06K	0,5	MR25	5322 116 55428
R 1281	RESISTOR,M.FILM	2K	0,5	MR25	4822 116 51243
R 1282	RESISTOR,M.FILM	365	0,5	MR25	5322 116 55422
R 1283	RESISTOR,M.FILM	412K	0,5	MR25	5322 116 55424
R 1284	RESISTOR,M.FILM	82,5K	0,5	MR25	5322 116 55374
R 1286	RESISTOR,M.FILM	20,5K	0,5	MR25	5322 116 55419
R 1287	RESISTOR,M.FILM	4,02K	0,1	MR24E	5322 116 54283
R 1288	RESISTOR,M.FILM	768	0,5	MR25	5322 116 55427
R 1289	RESISTOR,M.FILM	6,19K	0,5	MR25	5322 116 55426
R 1290	RESISTOR,M.FILM	953K	0,5	MR30	5322 116 55382
R 1291	RESISTOR,M.FILM	261K	0,5	MR25	5322 116 54736
R 13	POTM,CARBON	2,2K	20	0.1W	4822 101 20456
R 14	POTM,CARBON	2,2K	20	0.1W	4822 101 20456
R 1401	RESISTOR,M.FILM	3,16K	1	MR25	5322 116 50579
R 1402	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1403	RESISTOR,M.FILM	4,02K	1	MR25	5322 116 55448
R 1404	RESISTOR,M.FILM	3,16K	1	MR25	5322 116 50579
R 1406	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 1407	RESISTOR,M.FILM	681	1	MR25	4822 116 51233
R 1408	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 1409	RESISTOR,M.FILM	3,01K	1	MR25	4822 116 51246
R 1411	RESISTOR,M.FILM	9,09K	1	MR25	4822 116 51284
R 1412	RESISTOR,M.FILM	2,37K	1	MR25	5322 116 54576
R 1414	RESISTOR,M.FILM	3,01K	1	MR25	4822 116 51246
R 1416	RESISTOR,M.FILM	3,32K	1	MR25	5322 116 54005

POSNR	DESCRIPTION				ORDERING CODE
R 1417	POTM,TRIMMING	1K	20	0,5W	5322 100 10112
R 1418	RESISTOR,M.FILM	287	1	MR25	5322 116 54506
R 1419	POTM,TRIMMING	100	20	0,5W	5322 101 14011
R 1421	RESISTOR,M.FILM	8,66K	1	MR25	5322 116 54613
R 1422	RESISTOR,M.FILM	16,2K	1	MR25	5322 116 55361
R 1423	RESISTOR,M.FILM	20,5K	1	MR25	5322 116 54643
R 1424	RESISTOR,M.FILM	36,5K	1	MR25	5322 116 50726
R 1425	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1426	RESISTOR,M.FILM	12,1K	1	MR25	5322 116 50572
R 1427	RESISTOR,M.FILM	154K	1	MR25	5322 116 54714
R 1428	RESISTOR,M.FILM	33,2K	1	MR25	4822 116 51259
R 1429	RESISTOR,M.FILM	33,2K	1	MR25	4822 116 51259
R 1431	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1432	RESISTOR,M.FILM	33,2K	1	MR25	4822 116 51259
R 1433	RESISTOR,M.FILM	33,2K	1	MR25	4822 116 51259
R 1434	RESISTOR,M.FILM	154K	1	MR25	5322 116 54714
R 1436	RESISTOR,M.FILM	1,1K	1	MR25	4822 116 51236
R 1437	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 1438	RESISTOR,M.FILM	3,01K	1	MR25	4822 116 51246
R 1439	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 1440	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 1441	RESISTOR,M.FILM	1,1K	1	MR25	4822 116 51236
R 1442	RESISTOR,M.FILM	13,3K	1	MR25	5322 116 55276
R 1443	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 1444	RESISTOR,M.FILM	365K	1	MR30	5322 116 54762
R 1445	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 1446	RESISTOR,M.FILM	365K	1	MR30	5322 116 54762
R 1447	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1448	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1450	RESISTOR,M.FILM	64,9K	1	MR25	5322 116 50514
R 1501	RESISTOR,M.FILM	6,81K	1	MR25	4822 116 51252
R 1502	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 1503	RESISTOR,M.FILM	3,48K	1	MR25	5322 116 55367
R 1506	RESISTOR,M.FILM	162K	1	MR25	5322 116 54716
R 1507	RESISTOR,M.FILM	3,48K	1	MR25	5322 116 55367
R 1508	RESISTOR,M.FILM	100K	1	MR25	4822 116 51268
R 1509	RESISTOR,M.FILM	11K	1	MR25	5322 116 54623
R 1511	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 1512	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 1513	RESISTOR,M.FILM	26,1K	1	MR25	5322 116 54651
R 1514	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 1516	RESISTOR,M.FILM	22,6K	1	MR25	5322 116 50481
R 1517	RESISTOR,M.FILM	2,05K	1	MR25	5322 116 50664
R 1518	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 1519	RESISTOR,M.FILM	464	1	MR25	5322 116 50536
R 1521	RESISTOR,M.FILM	226K	1	MR25	5322 116 54729
R 1522	RESISTOR,NTC	680	5	0.5W	5322 116 34049
R 1523	RESISTOR,M.FILM	4,02K	1	MR25	5322 116 55448
R 1524	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1525	RESISTOR,M.FILM	511	1	MR30	5322 116 54835
R 1526	RESISTOR,M.FILM	64,9K	1	MR30	4822 116 51175
R 1527	RESISTOR,M.FILM	17,8K	1	MR25	5322 116 54637
R 1528	RESISTOR,M.FILM	33,2K	1	MR25	4822 116 51259
R 1529	RESISTOR,M.FILM	4,87K	1	MR25	5322 116 55445
R 1531	RESISTOR,M.FILM	11,5K	1	MR25	5322 116 55358
R 1532	RESISTOR,M.FILM	1M	1	MR30	4822 116 51279
R 1533	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1534	POTM,TRIMMING	10K	20	0,5W	5322 100 10113
R 1535	RESISTOR,M.FILM	1K	1	MR30	5322 116 54207
R 1536	RESISTOR,M.FILM	4,64K	1	MR25	5322 116 50484
R 1537	RESISTOR,M.FILM	1M	1	MR30	4822 116 51279
R 1538	RESISTOR,HT	1,2M	5	VR37	4822 110 42189
R 1539	RESISTOR,HT	2,2M	5	VR37	4822 110 42196
R 1541	RESISTOR,HT	5,6M	5	VR37	4822 110 42207
R 1542	RESISTOR,M.FILM	78,7K	1	MR25	5322 116 50533

POSNR	DESCRIPTION				ORDERING CODE
R 1543	POTM,TRIMMING	100K	20	0.05W	4822 100 10072
R 1544	RESISTOR,M.FILM	121K	1	MR25	5322 116 54704
R 1546	RESISTOR,M.FILM	16,2K	1	MR25	5322 116 55361
R 1547	RESISTOR,M.FILM	26,1K	1	MR25	5322 116 54651
R 1548	RESISTOR,M.FILM	196K	1	MR25	5322 116 55364
R 1549	POTM,TRIMMING	1M	20	0.05W	4822 100 10103
R 1551	RESISTOR,M.FILM	383K	1	MR30	5322 116 54761
R 1552	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 1553	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 1554	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 1601	RESISTOR,M.FILM	301	1	MR25	5322 116 55366
R 1602	RESISTOR,M.FILM	12,1K	1	MR25	5322 116 50572
R 1603	RESISTOR,M.FILM	2,05K	1	MR25	5322 116 50664
R 1604	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1606	RESISTOR,M.FILM	681	1	MR25	4822 116 51233
R 1607	POTM,TRIMMING	22K	20	0.5W	5322 101 14069
R 1608	RESISTOR,M.FILM	38,3K	1	MR25	5322 116 55369
R 1609	RESISTOR,M.FILM	953	1	MR25	5322 116 54547
R 1611	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1612	RESISTOR,M.FILM	681	1	MR25	4822 116 51233
R 1613	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 1614	RESISTOR,M.FILM	3,48K	1	MR25	5322 116 55367
R 1616	RESISTOR,M.FILM	2,05K	1	MR25	5322 116 50664
R 1617	RESISTOR,M.FILM	301	1	MR25	5322 116 55366
R 1618	RESISTOR,M.FILM	26,1K	1	MR25	5322 116 54651
R 1619	RESISTOR,M.FILM	12,1K	1	MR25	5322 116 50572
R 1700	RESISTOR,M.FILM	2,37K	1	MR25	5322 116 54576
R 1701	RESISTOR,M.FILM	7,5K	1	MR25	5322 116 54608
R 1702	RESISTOR,M.FILM	4,22K	1	MR25	5322 116 50729
R 1703	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1704	RESISTOR,M.FILM	61,9	1	MR25	5322 116 54451
R 1706	RESISTOR,M.FILM	61,9	1	MR25	5322 116 54451
R 1707	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 1708	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1709	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1710	RESISTOR,M.FILM	2,15K	1	MR25	5322 116 50767
R 1711	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1712	RESISTOR,M.FILM	61,9K	1	MR25	5322 116 50872
R 1713	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1714	RESISTOR,M.FILM	5,62K	1	MR25	4822 116 51281
R 1716	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1717	RESISTOR,M.FILM	422	1	MR25	5322 116 50459
R 1718	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1719	RESISTOR,M.FILM	2,15K	1	MR25	5322 116 50767
R 1721	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1722	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1723	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1724	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1725	RESISTOR,M.FILM	21,5K	1	MR25	5322 116 50451
R 1726	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 1727	RESISTOR,M.FILM	11K	1	MR25	5322 116 54623
R 1728	POTM,TRIMMING	1K	20	0,5W	5322 100 10112
R 1729	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1731	RESISTOR,M.FILM	3,48K	1	MR25	5322 116 55367
R 1732	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558

POSNR	DESCRIPTION				ORDERING CODE
R 1733	RESISTOR,M.FILM	422	1	MR25	5322 116 50459
R 1734	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1736	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 1737	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 1738	POTM,TRIMMING	4,7K	20	0.5W	5322 100 10114
R 1739	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 1741	RESISTOR,M.FILM	1,78K	1	MR25	5322 116 50515
R 1742	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1743	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 1744	RESISTOR,M.FILM	1,47K	1	MR25	5322 116 50635
R 1746	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1747	RESISTOR,M.FILM	2,37K	1	MR25	5322 116 54576
R 1750	RESISTOR,M.FILM	2,15K	1	MR25	5322 116 50767
R 1752	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1753	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1754	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1756	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1757	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1758	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1759	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1761	RESISTOR,M.FILM	422	1	MR25	5322 116 50459
R 1762	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1763	RESISTOR,M.FILM	2,15K	1	MR25	5322 116 50767
R 1764	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 1766	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1767	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1768	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1769	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 1770	RESISTOR,M.FILM	21,5K	1	MR25	5322 116 50451
R 1771	POTM,TRIMMING	10K	20	0,5W	5322 100 10113
R 1772	RESISTOR,M.FILM	56,2K	1	MR25	4822 116 51264
R 1773	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 1774	RESISTOR,M.FILM	38,3K	1	MR25	5322 116 55369
R 1776	RESISTOR,M.FILM	909	1	MR25	5322 116 55278
R 1777	RESISTOR,M.FILM	4,22K	1	MR25	5322 116 50729
R 1778	RESISTOR,M.FILM	7,5K	1	MR25	5322 116 54608
R 1779	RESISTOR,M.FILM	464	1	MR25	5322 116 50536
R 1781	RESISTOR,M.FILM	750	1	MR25	4822 116 51234
R 1782	RESISTOR,M.FILM	2,15K	1	MR25	5322 116 50767
R 1783	RESISTOR,M.FILM	750	1	MR25	4822 116 51234
R 1784	POTM,TRIMMING	4,7K	20	0.5W	5322 100 10114
R 1786	RESISTOR,M.FILM	4,22K	1	MR25	5322 116 50729
R 1787	RESISTOR,M.FILM	6,81K	1	MR25	4822 116 51252
R 1788	RESISTOR,M.FILM	2,15K	1	MR25	5322 116 50767
R 1789	RESISTOR,M.FILM	3,16K	1	MR25	5322 116 50579
R 1791	RESISTOR,M.FILM	31,6K	1	MR25	5322 116 54657
R 1792	RESISTOR,M.FILM	2,37K	1	MR25	5322 116 54576
R 1793	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 1802	RESISTOR,M.FILM	2,87K	1	MR25	5322 116 55279
R 1803	RESISTOR,M.FILM	9,09K	1	MR25	4822 116 51284
R 1804	RESISTOR,M.FILM	6,81K	1	MR25	4822 116 51252
R 1806	RESISTOR,M.FILM	2,15K	1	MR25	5322 116 50767
R 1807	RESISTOR,M.FILM	215	1	MR25	5322 116 55274
R 1808	RESISTOR,M.FILM	215	1	MR25	5322 116 55274
R 1809	RESISTOR,M.FILM	348	1	MR25	5322 116 54515
R 1811	RESISTOR,M.FILM	348	1	MR25	5322 116 54515
R 1812	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1851	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 1852	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 1853	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 1854	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 1901	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1904	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1906	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1907	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253

POSNR	DESCRIPTION				ORDERING CODE
R 1908	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1909	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1911	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1912	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1913	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1914	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1916	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1917	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1918	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 1919	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1921	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 1922	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 1923	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1924	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 1926	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 1927	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 1931	RESISTOR,M.FILM	2,15K	1	MR25	5322 116 50767
R 1932	RESISTOR,M.FILM	2,15K	1	MR25	5322 116 50767
R 1933	RESISTOR,M.FILM	3,16K	1	MR25	5322 116 50579
R 1934	RESISTOR,M.FILM	2,37K	1	MR25	5322 116 54576
R 1936	RESISTOR,M.FILM	7,5K	1	MR25	5322 116 54608
R 1937	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 1938	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2	POTM,CARBON	1K	20	0.1W	5322 101 24118
R 200	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2001	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2002	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 2003	RESISTOR,M.FILM	19,6K	1	MR25	5322 116 54641
R 2004	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 2005	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2006	RESISTOR,M.FILM	19,6K	1	MR25	5322 116 54641
R 2007	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 2008	RESISTOR,M.FILM	19,6K	1	MR25	5322 116 54641
R 2009	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 201	RESISTOR,M.FILM	23,7K	1	MR25	5322 116 54646
R 2010	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2011	RESISTOR,M.FILM	19,6K	1	MR25	5322 116 54641
R 2012	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 2013	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2014	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2015	RESISTOR,M.FILM	100K	1	MR25	4822 116 51268
R 2016	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2017	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2018	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2019	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 202	RESISTOR,M.FILM	1,21K	1	MR25	5322 116 54557
R 2020	RESISTOR,M.FILM	21,5K	1	MR25	5322 116 50451
R 2021	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2022	RESISTOR,M.FILM	4,64K	1	MR25	5322 116 50484
R 2023	RESISTOR,M.FILM	3,48K	1	MR25	5322 116 55367
R 2024	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2025	RESISTOR,M.FILM	215	1	MR25	5322 116 55274
R 2026	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2027	RESISTOR,M.FILM	1,47K	1	MR25	5322 116 50635
R 2028	RESISTOR,M.FILM	511	1	MR25	4822 116 51282

POSNR	DESCRIPTION				ORDERING CODE
R 2029	RESISTOR,M.FILM	422	1	MR25	5322 116 50459
R 203	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2031	RESISTOR,M.FILM	422	1	MR25	5322 116 50459
R 2032	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2033	POTM,TRIMMING	47K	20	0,5W	5322 101 14048
R 2034	POTM,TRIMMING	100K	20	0.5W	5322 101 14071
R 2036	POTM,TRIMMING	22K	20	0.75W	5322 101 14042
R 2037	RESISTOR,M.FILM	287	1	MR25	5322 116 54506
R 2038	RESISTOR,M.FILM	287	1	MR25	5322 116 54506
R 2039	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 204	POTM,TRIMMING	220	20	0.5W	5322 101 14051
R 2040	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2041	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2042	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2043	RESISTOR,M.FILM	1,96K	1	MR25	5322 116 54571
R 2044	POTM,TRIMMING	10K	20	0,5W	5322 100 10113
R 2045	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2046	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 2047	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 2048	RESISTOR,M.FILM	383	1	MR25	5322 116 55368
R 2049	RESISTOR,M.FILM	383	1	MR25	5322 116 55368
R 2051	RESISTOR,M.FILM	383	1	MR25	5322 116 55368
R 2052	POTM,TRIMMING	22K	20	0.75W	5322 101 14042
R 2053	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 2054	RESISTOR,M.FILM	16,2K	1	MR25	5322 116 55361
R 2056	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2057	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 2058	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 2059	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 206	RESISTOR,M.FILM	2,87K	1	MR25	5322 116 55279
R 2061	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 2062	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 2063	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 2064	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 2066	RESISTOR,M.FILM	34,8K	1	MR25	5322 116 54661
R 2067	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2068	RESISTOR,M.FILM	3,83K	1	MR25	5322 116 54589
R 2069	RESISTOR,M.FILM	2,37K	1	MR25	5322 116 54576
R 207	RESISTOR,M.FILM	2,74K	1	MR25	5322 116 50636
R 2071	RESISTOR,M.FILM	2,37K	1	MR25	5322 116 54576
R 2072	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2073	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2074	RESISTOR,HT	3,3M	5	VR25	4822 110 72201
R 2076	RESISTOR,M.FILM	1M	1	MR25	5322 116 55535
R 2077	RESISTOR,M.FILM	2,37K	1	MR25	5322 116 54576
R 2078	RESISTOR,M.FILM	7,5K	1	MR25	5322 116 54608
R 2079	RESISTOR,M.FILM	1,33K	1	MR25	5322 116 55422
R 208	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 2081	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2082	RESISTOR,M.FILM	3,83K	1	MR25	5322 116 54589
R 2083	RESISTOR,M.FILM	237	1	MR25	5322 116 50679
R 2084	RESISTOR,M.FILM	464K	1	MR25	5322 116 55207
R 2086	POTM,TRIMMING	220	20	0,5W	5322 101 14009
R 209	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 2091	RESISTOR,M.FILM	10	1	MR25	5322 116 50452
R 2092	RESISTOR,M.FILM	10	1	MR25	5322 116 50452
R 2093	RESISTOR,M.FILM	21,5	1	MR25	5322 116 50677
R 210	RESISTOR,M.FILM	1M	1	MR30	4822 116 51279
R 212	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 227	RESISTOR,M.FILM	237	1	MR25	5322 116 50679
R 2301	RESISTOR,M.FILM	16,2K	0,1		5322 116 51704
R 2302	RESISTOR,M.FILM	16,2K	0,1		5322 116 51704
R 2303	RESISTOR,M.FILM	100K	0,1		5322 116 51703
R 2304	RESISTOR,M.FILM	11K	1	MR25	5322 116 54623
R 2306	RESISTOR,M.FILM	100K	0,1		5322 116 51703

POSNR	DESCRIPTION				ORDERING CODE
R 2307	RESISTOR,M.FILM	11K	1	MR25	5322 116 54623
R 2308	RESISTOR,M.FILM	16,2K	0,1		5322 116 51704
R 2309	RESISTOR,M.FILM	16,2K	0,1		5322 116 51704
R 2311	RESISTOR,M.FILM	1,96K	0,1		5322 116 51705
R 2312	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2313	RESISTOR,M.FILM	1,96K	0,1		5322 116 51705
R 2314	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2316	RESISTOR,M.FILM	9,09K	1	MR25	4822 116 51284
R 2317	RESISTOR,M.FILM	2,61K	1	MR25	5322 116 50671
R 2318	RESISTOR,M.FILM	1,96K	1	MR25	5322 116 54571
R 2319	RESISTOR,M.FILM	1,96K	1	MR25	5322 116 54571
R 2321	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 2322	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 2323	RESISTOR,M.FILM	619	1	MR25	4822 116 51232
R 2326	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 2327	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 2328	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 2329	RESISTOR,M.FILM	3,83K	1	MR25	5322 116 54589
R 2331	RESISTOR,M.FILM	1,96K	1	MR25	5322 116 54571
R 2332	RESISTOR,M.FILM	1,96K	1	MR25	5322 116 54571
R 2333	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2334	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2351	RESISTOR,M.FILM	16,2K	0,1		5322 116 51704
R 2352	RESISTOR,M.FILM	16,2K	0,1		5322 116 51704
R 2353	RESISTOR,M.FILM	100K	0,1		5322 116 51703
R 2354	RESISTOR,M.FILM	11K	1	MR25	5322 116 54623
R 2356	RESISTOR,M.FILM	100K	0,1		5322 116 51703
R 2357	RESISTOR,M.FILM	11K	1	MR25	5322 116 54623
R 2358	RESISTOR,M.FILM	16,2K	0,1		5322 116 51704
R 2359	RESISTOR,M.FILM	16,2K	0,1		5322 116 51704
R 2361	RESISTOR,M.FILM	1,96K	0,1		5322 116 51705
R 2362	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2363	RESISTOR,M.FILM	1,96K	0,1		5322 116 51705
R 2364	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2366	RESISTOR,M.FILM	9,09K	1	MR25	4822 116 51284
R 2367	RESISTOR,M.FILM	2,61K	1	MR25	5322 116 50671
R 2368	RESISTOR,M.FILM	1,96K	1	MR25	5322 116 54571
R 2369	RESISTOR,M.FILM	1,96K	1	MR25	5322 116 54571
R 2371	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 2372	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 2373	RESISTOR,M.FILM	619	1	MR25	4822 116 51232
R 2376	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 2377	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 2378	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 2379	RESISTOR,M.FILM	3,83K	1	MR25	5322 116 54589
R 2381	RESISTOR,M.FILM	1,96K	1	MR25	5322 116 54571
R 2382	RESISTOR,M.FILM	1,96K	1	MR25	5322 116 54571
R 2501	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2503	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2504	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2506	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2508	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2509	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2511	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 2512	POTM,TRIMMING	220	20	0.5W	5322 101 14051

POSNR	DESCRIPTION				ORDERING CODE
R 2513	RESISTOR,M.FILM	178	1	MR25	5322 116 54492
R 2514	RESISTOR,M.FILM	147	1	MR25	5322 116 50766
R 2516	RESISTOR,M.FILM	147	1	MR25	5322 116 50766
R 2517	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 2518	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2519	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2521	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 2522	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2523	RESISTOR,M.FILM	464	1	MR25	5322 116 50536
R 2524	RESISTOR,M.FILM	464	1	MR25	5322 116 50536
R 2526	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2527	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2528	RESISTOR,M.FILM	1,62K	1	MR25	5322 116 55359
R 2529	RESISTOR,M.FILM	1,62K	1	MR25	5322 116 55359
R 2531	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 2532	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2533	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2534	POTM,TRIMMING	100	20	0.5W	5322 101 14072
R 2536	RESISTOR,M.FILM	909	1	MR25	5322 116 55278
R 2537	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2538	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2539	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 2541	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2542	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2543	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2544	RESISTOR,M.FILM	215	1	MR25	5322 116 55274
R 2546	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2547	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2549	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2551	RESISTOR,M.FILM	4,64K	1	MR25	5322 116 50484
R 2552	RESISTOR,M.FILM	422	1	MR25	5322 116 50459
R 2553	RESISTOR,M.FILM	100	0,1		5322 116 51701
R 2554	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2557	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2558	RESISTOR,M.FILM	100	0,1		5322 116 51701
R 2559	RESISTOR,M.FILM	4,64K	1	MR25	5322 116 50484
R 2561	RESISTOR,M.FILM	422	1	MR25	5322 116 50459
R 2562	RESISTOR,M.FILM	10K	0,1		5322 116 51702
R 2563	RESISTOR,M.FILM	10K	0,1		5322 116 51702
R 2564	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 2566	RESISTOR,M.FILM	215	1	MR25	5322 116 55274
R 2567	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2568	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2569	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2571	RESISTOR,M.FILM	215	1	MR25	5322 116 55274
R 2572	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 2573	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2574	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 2576	POTM,TRIMMING	220	20	0.5W	5322 101 14051
R 2577	RESISTOR,M.FILM	261	1	MR25	5322 116 54502
R 2578	RESISTOR,M.FILM	162	1	MR25	5322 116 50417
R 2579	RESISTOR,M.FILM	162	1	MR25	5322 116 50417
R 2581	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 2582	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2583	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2584	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 2586	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2587	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 2588	RESISTOR,M.FILM	215	1	MR25	5322 116 55274
R 2589	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2591	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2592	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2593	RESISTOR,M.FILM	215	1	MR25	5322 116 55274
R 2594	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 2596	RESISTOR,M.FILM	100	1	MR25	5322 116 55549

POSNR	DESCRIPTION			ORDERING CODE	
R 2597	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 2598	POTM,TRIMMING	220	20	0.5W	5322 101 14051
R 2599	RESISTOR,M.FILM	261	1	MR25	5322 116 54502
R 2601	RESISTOR,M.FILM	162	1	MR25	5322 116 50417
R 2602	RESISTOR,M.FILM	162	1	MR25	5322 116 50417
R 2603	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 2604	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2606	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2607	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 2608	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2609	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 2611	RESISTOR,M.FILM	42,2	1	MR25	5322 116 51052
R 2612	RESISTOR,M.FILM	464	1	MR25	5322 116 50536
R 2613	RESISTOR,M.FILM	464	1	MR25	5322 116 50536
R 2614	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2616	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2617	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 2618	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2619	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2621	RESISTOR,M.FILM	909	1	MR25	5322 116 55278
R 2622	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2623	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2624	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 2626	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2627	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2628	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 2629	RESISTOR,M.FILM	261	1	MR25	5322 116 54502
R 2631	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 2632	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 2634	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 2636	RESISTOR,M.FILM	3,16K	1	MR25	5322 116 50579
R 2637	RESISTOR,M.FILM	6,81K	1	MR25	4822 116 51252
R 2638	POTM,TRIMMING	2,2K	20	0.5W	5322 100 10117
R 2639	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 2642	POTM,TRIMMING	10K	20	0.5W	5322 101 14066
R 2643	RESISTOR,HT	2,2M	5	VR25	4822 110 72196
R 2645	RESISTOR,M.FILM	750K	1	MR25	5322 116 55532
R 2646	RESISTOR,M.FILM	34,8K	1	MR25	5322 116 54661
R 2647	RESISTOR,M.FILM	34,8K	1	MR25	5322 116 54661
R 2648	RESISTOR,M.FILM	3,83K	1	MR25	5322 116 54589
R 2649	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 2650	RESISTOR,M.FILM	13,3K	1	MR25	5322 116 55276
R 2651	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2652	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2653	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2654	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 2656	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2657	RESISTOR,M.FILM	10K	1	MR25	4822 116 51253
R 2658	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 2659	RESISTOR,M.FILM	511	1	MR25	4822 116 51282
R 2661	RESISTOR,M.FILM	1,78K	1	MR25	5322 116 50515
R 2662	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 2663	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 2664	RESISTOR,M.FILM	26,1K	1	MR25	5322 116 54651
R 2666	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235

POSNR	DESCRIPTION				ORDERING CODE
R 2667	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2668	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2669	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2671	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2672	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2673	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2674	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2676	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2677	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2678	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2679	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2681	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2682	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 2691	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 3	POTM,CARB+SW.	1K	20	0.1W	5322 101 64018
R 302	RESISTOR,M.FILM	1M	1	MR30	4822 116 51279
R 303	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 304	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 306	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 307	RESISTOR,M.FILM	191K	1	MR30	5322 116 55319
R 308	RESISTOR,M.FILM	681K	1	MR30	5322 116 54263
R 309	RESISTOR,M.FILM	845K	1	MR30	5322 116 55379
R 311	RESISTOR,M.FILM	549K	1	MR30	5322 116 55139
R 312	RESISTOR,M.FILM	205K	1	MR25	5322 116 54727
R 313	RESISTOR,M.FILM	732K	1	MR30	5322 116 55321
R 314	RESISTOR,M.FILM	806K	1	MR30	5322 116 55078
R 316	RESISTOR,HT	8,2M	10	CR25	4822 110 72212
R 317	RESISTOR,M.FILM	1M	1	MR30	4822 116 51279
R 318	RESISTOR,M.FILM	90,9K	0,25	MR24C	5322 116 50859
R 319	RESISTOR,M.FILM	8,25K	0,25	MR24C	5322 116 50979
R 351	RESISTOR,M.FILM	1M	1	MR30	4822 116 51279
R 352	RESISTOR,M.FILM	1K	1	MR25	4822 116 51235
R 353	RESISTOR,M.FILM	953K	1	MR30	5322 116 55257
R 354	RESISTOR,M.FILM	487K	1	MR30	5322 116 55243
R 355	RESISTOR,M.FILM	133K	1	MR25	5322 116 54708
R 356	POTM,TRIMMING	22K	20	0.5W	5322 101 14069
R 357	RESISTOR,M.FILM	20,5K	1	MR25	5322 116 54643
R 358	POTM,TRIMMING	22K	20	0.5W	5322 101 14069
R 359	RESISTOR,M.FILM	20,5K	1	MR25	5322 116 54643
R 360	RESISTOR,M.FILM	121	1	MR25	5322 116 54426
R 361	POTM,TRIMMING	22K	20	0.5W	5322 101 14069
R 362	RESISTOR,M.FILM	20,5K	1	MR25	5322 116 54643
R 363	RESISTOR,M.FILM	8,25K	1	MR25	5322 116 54558
R 364	RESISTOR,M.FILM	4,02K	1	MR25	5322 116 55448
R 365	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 366	RESISTOR,M.FILM	2,49K	1	MR25	5322 116 50581
R 367	RESISTOR,M.FILM	1,62K	1	MR25	5322 116 55359
R 368	RESISTOR,M.FILM	5,11	1	MR25	5322 116 54192
R 369	RESISTOR,M.FILM	1,62K	1	MR25	5322 116 55359
R 370	RESISTOR,M.FILM	10	1	MR25	5322 116 50452
R 371	RESISTOR,M.FILM	10	1	MR25	5322 116 50452
R 372	RESISTOR,M.FILM	154K	1	MR25	5322 116 54714
R 373	RESISTOR,M.FILM	511K	1	MR30	5322 116 55636
R 374	RESISTOR,M.FILM	10	1	MR25	5322 116 50452
R 4	POTM,TANDEM+SW.	5K 10T	LIN		5322 102 40061
R 402	RESISTOR,M.FILM	1M	1	MR30	4822 116 51279
R 403	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 404	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 406	RESISTOR,M.FILM	75	1	MR25	5322 116 54459
R 407	RESISTOR,M.FILM	191K	1	MR30	5322 116 55319
R 408	RESISTOR,M.FILM	681K	1	MR30	5322 116 54263
R 409	RESISTOR,M.FILM	845K	1	MR30	5322 116 55379
R 411	RESISTOR,M.FILM	549K	1	MR30	5322 116 55139
R 412	RESISTOR,M.FILM	205K	1	MR25	5322 116 54727
R 413	RESISTOR,M.FILM	732K	1	MR30	5322 116 55321

POSNR	DESCRIPTION			ORDERING CODE
R 414	RESISTOR,M.FILM	806K	1	MR30 5322 116 55078
R 416	RESISTOR,HT	8,2M	10	CR25 4822 110 72212
R 417	RESISTOR,M.FILM	1M	1	MR30 4822 116 51279
R 418	RESISTOR,M.FILM	90,9K	0,25	MR24C 5322 116 50859
R 419	RESISTOR,M.FILM	8,25K	0,25	MR24C 5322 116 50979
R 451	RESISTOR,M.FILM	274	1	MR25 5322 116 54504
R 452	RESISTOR,M.FILM	274	1	MR25 5322 116 54504
R 453	RESISTOR,M.FILM	274	1	MR25 5322 116 54504
R 454	RESISTOR,M.FILM	274	1	MR25 5322 116 54504
R 456	RESISTOR,M.FILM	274	1	MR25 5322 116 54504
R 457	RESISTOR,M.FILM	274	1	MR25 5322 116 54504
R 458	RESISTOR,M.FILM	274	1	MR25 5322 116 54504
R 459	RESISTOR,M.FILM	274	1	MR25 5322 116 54504
R 5	POTM,CARB+SW.	100K	20	0.1W 5322 101 44044
R 500	RESISTOR,M.FILM	51,1	1	MR25 5322 116 54442
R 501	RESISTOR,M.FILM	51,1	1	MR25 5322 116 54442
R 502	RESISTOR,M.FILM	806K	1	MR30 5322 116 55078
R 503	RESISTOR,M.FILM	12,7K	1	MR25 5322 116 50443
R 504	POTM,TRIMMING	470	20	0,5W 5322 101 14047
R 506	RESISTOR,M.FILM	12,7K	1	MR25 5322 116 50443
R 507	RESISTOR,M.FILM	6,19K	1	MR25 5322 116 55426
R 508	RESISTOR,M.FILM	6,49K	1	MR25 5322 116 54603
R 509	RESISTOR,M.FILM	619	1	MR25 4822 116 51232
R 511	RESISTOR,M.FILM	511	0,5	MR25 4822 116 51282
R 512	RESISTOR,M.FILM	511	0,5	MR25 4822 116 51282
R 513	RESISTOR,M.FILM	105	1	MR25 5322 116 54472
R 514	POTM,TRIMMING	22K	20	0.5W 5322 101 14069
R 516	RESISTOR,M.FILM	51,1K	1	MR25 5322 116 50672
R 517	RESISTOR,M.FILM	5,9K	1	MR25 5322 116 50583
R 518	RESISTOR,M.FILM	909	1	MR25 5322 116 55278
R 519	RESISTOR,M.FILM	162	1	MR25 5322 116 50417
R 521	POTM,TRIMMING	1K	20	0,5W 5322 100 10112
R 522	RESISTOR,M.FILM	44,2	1	MR25 5322 116 50818
R 523	RESISTOR,M.FILM	44,2	1	MR25 5322 116 50818
R 524	RESISTOR,M.FILM	100	0,5	MR25 5322 116 55549
R 526	RESISTOR,M.FILM	100	0,5	MR25 5322 116 55549
R 527	RESISTOR,M.FILM	5,62K	0,5	MR25 4822 116 51281
R 528	RESISTOR,M FILM	909	0,5	MR25 5322 116 55278
R 529	RESISTOR,M.FILM	51,1	1	MR25 5322 116 54442
R 531	RESISTOR,M.FILM	51,1	1	MR25 5322 116 54442
R 532	RESISTOR,M.FILM	909	0,5	MR25 5322 116 55278
R 533	RESISTOR,M.FILM	5,62K	0,5	MR25 4822 116 51281
R 534	RESISTOR,M.FILM	825	1	MR25 5322 116 54541
R 535	RESISTOR,M.FILM	825	1	MR25 5322 116 54541
R 536	RESISTOR,M.FILM	30,1	1	MR25 5322 116 50904
R 537	RESISTOR,M.FILM	866	1	MR25 5322 116 54543
R 538	RESISTOR,NTC	1,5K	5	0.5W 5322 116 34054
R 539	RESISTOR,M.FILM	30,1	1	MR25 5322 116 50904
R 540	RESISTOR,M.FILM	402	1	MR25 5322 116 54519
R 541	RESISTOR,M.FILM	348	1	MR25 5322 116 54515
R 542	RESISTOR,M.FILM	249	1	MR25 5322 116 54499
R 543	POTM,TRIMMING	100	20	0,5W 5322 101 14011
R 546	RESISTOR,M.FILM	909	1	MR25 5322 116 55278
R 547	POTM,TRIMMING	220	20	0,5W 5322 101 14009
R 548	RESISTOR,M.FILM	909	1	MR25 5322 116 55278

POSNR	DESCRIPTION				ORDERING CODE
R 549	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 550	RESISTOR,M.FILM	10	1	MR25	5322 116 50452
R 551	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 552	RESISTOR,M.FILM	121	1	MR25	5322 116 54426
R 553	RESISTOR,M.FILM	121	1	MR25	5322 116 54426
R 554	RESISTOR,M.FILM	909	1	MR25	5322 116 55278
R 558	RESISTOR,M.FILM	17,8K	1	MR25	5322 116 54637
R 559	RESISTOR,M.FILM	5,11K	1	MR25	5322 116 54595
R 568	RESISTOR,M.FILM	17,8K	1	MR25	5322 116 54637
R 569	RESISTOR,M.FILM	5,9K	1	MR25	5322 116 50583
R 571	RESISTOR,M.FILM	178	1	MR25	5322 116 54492
R 572	RESISTOR,M.FILM	178	1	MR25	5322 116 54492
R 573	RESISTOR,M.FILM	2,26K	1	MR25	5322 116 50675
R 577	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 581	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 582	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 583	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 584	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 586	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 587	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 6	POTM,CARBON	2,2M	20	0.1W	5322 101 24098
R 600	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 601	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 602	RESISTOR,M.FILM	806K	1	MR30	5322 116 55078
R 603	RESISTOR,M.FILM	12,7K	1	MR25	5322 116 50443
R 604	POTM,TRIMMING	470	20	0,5W	5322 101 14047
R 606	RESISTOR,M.FILM	12,7K	1	MR25	5322 116 50443
R 607	RESISTOR,M.FILM	6,19K	1	MR25	5322 116 55426
R 608	RESISTOR,M.FILM	6,49K	1	MR25	5322 116 54603
R 609	RESISTOR,M.FILM	619	1	MR25	4822 116 51232
R 611	RESISTOR,M.FILM	511	0,5	MR25	4822 116 51282
R 612	RESISTOR,M.FILM	511	0,5	MR25	4822 116 51282
R 613	RESISTOR,M.FILM	105	1	MR25	5322 116 54472
R 614	POTM,TRIMMING	22K	20	0.5W	5322 101 14069
R 616	RESISTOR,M.FILM	51,1K	1	MR25	5322 116 50672
R 617	RESISTOR,M.FILM	5,9K	1	MR25	5322 116 50583
R 618	RESISTOR,M.FILM	909	1	MR25	5322 116 55278
R 619	RESISTOR,M.FILM	162	1	MR25	5322 116 50417
R 621	POTM,TRIMMING	1K	20	0,5W	5322 100 10112
R 622	RESISTOR,M.FILM	44,2	1	MR25	5322 116 50818
R 623	RESISTOR,M.FILM	44,2	1	MR25	5322 116 50818
R 624	RESISTOR,M.FILM	100	0,1	MR24E	5322 116 50746
R 626	RESISTOR,M.FILM	100	0,1	MR24E	5322 116 50746
R 627	RESISTOR,M.FILM	5,62K	0,5	MR25	4822 116 51281
R 628	RESISTOR,M.FILM	909	0,5	MR25	5322 116 55278
R 629	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 631	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 632	RESISTOR,M.FILM	909	0,5	MR25	5322 116 55278
R 633	RESISTOR,M.FILM	5,62K	0,5	MR25	4822 116 51281
R 634	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 635	RESISTOR,M.FILM	825	1	MR25	5322 116 54541
R 636	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 637	RESISTOR,M.FILM	866	1	MR25	5322 116 54543
R 638	RESISTOR,NTC	1,5K	5	0.5W	5322 116 34054
R 639	RESISTOR,M.FILM	30,1	1	MR25	5322 116 50904
R 640	RESISTOR,M.FILM	402	1	MR25	5322 116 54519
R 641	RESISTOR,M.FILM	158	0,5	MR25	5322 116 55418
R 646	RESISTOR,M.FILM	953	1	MR25	5322 116 54547
R 647	POTM,TRIMMING	100	20	0,5W	5322 101 14011
R 648	RESISTOR,M.FILM	953	1	MR25	5322 116 54547
R 649	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 650	RESISTOR,M.FILM	10	1	MR25	5322 116 50452
R 651	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 652	RESISTOR,M.FILM	121	1	MR25	5322 116 54426
R 653	RESISTOR,M.FILM	121	1	MR25	5322 116 54426

POSNR	DESCRIPTION			ORDERING CODE
R 654	RESISTOR,M.FILM	909	1	MR25 5322 116 55278
R 658	RESISTOR,M.FILM	17,8K	1	MR25 5322 116 54637
R 659	RESISTOR,M.FILM	5,11K	1	MR25 5322 116 54595
R 661	RESISTOR,M.FILM	31,6K	1	MR25 5322 116 54657
R 662	RESISTOR,M.FILM	17,8K	1	MR25 5322 116 54637
R 663	RESISTOR,M.FILM	14K	1	MR25 5322 116 55571
R 664	RESISTOR,M.FILM	8,25K	1	MR25 5322 116 54558
R 668	RESISTOR,M.FILM	17,8K	1	MR25 5322 116 54637
R 669	RESISTOR,M.FILM	5,9K	1	MR25 5322 116 50583
R 671	RESISTOR,M.FILM	178	1	MR25 5322 116 54492
R 672	RESISTOR,M.FILM	178	1	MR25 5322 116 54492
R 673	RESISTOR,M.FILM	2,26K	1	MR25 5322 116 50675
R 674	POTM,TRIMMING	47K	20	0,5W 5322 101 14048
R 676	RESISTOR,M.FILM	3[illegible],2K	1	MR25 4822 116 51259
R 677	RESISTOR,M.FILM	100	1	MR25 5322 116 55549
R 682	RESISTOR,M.FILM	4,99	1	MR25 5322 116 50568
R 683	RESISTOR,M.FILM	4,99	1	MR25 5322 116 50568
R 684	RESISTOR,M.FILM	4,99	1	MR25 5322 116 50568
R 7	POTM,CARB+SW.	1K	20	0.1W 5322 101 44024
R 701	RESISTOR,M.FILM	100	1	MR25 5322 116 55549
R 702	RESISTOR,M.FILM	1,27K	1	MR25 5322 116 50555
R 703	RESISTOR,M.FILM	750	1	MR25 4822 116 51234
R 704	RESISTOR,M.FILM	402	1	MR25 5322 116 54519
R 705	RESISTOR,M.FILM	4,99	1	MR25 5322 116 50568
R 706	RESISTOR,M.FILM	1,27K	1	MR25 5322 116 50555
R 707	RESISTOR,M.FILM	20,5K	1	MR25 5322 116 54643
R 708	RESISTOR,M.FILM	6,81K	1	MR25 4822 116 51252
R 709	RESISTOR,M.FILM	2,49K	1	MR25 5322 116 50581
R 710	RESISTOR,M.FILM	4,99	1	MR25 5322 116 50568
R 711	RESISTOR,M.FILM	2,49K	1	MR25 5322 116 50581
R 712	RESISTOR,M.FILM	4,02K	1	MR25 5322 116 55448
R 713	RESISTOR,M.FILM	4,02K	1	MR25 5322 116 55448
R 714	RESISTOR,M.FILM	4,02K	1	MR25 5322 116 55448
R 716	RESISTOR,M.FILM	4,02K	1	MR25 5322 116 55448
R 717	RESISTOR,M.FILM	100	1	MR30 5322 116 54852
R 8	POTM,CARB+SW.	1K	20	0.1W 5322 101 44024
R 801	RESISTOR,M.FILM	4,02K	1	MR25 5322 116 55448
R 802	RESISTOR,M.FILM	8,25K	1	MR25 5322 116 54558
R 803	RESISTOR,M.FILM	100	1	MR25 5322 116 55549
R 804	RESISTOR,M.FILM	100	1	MR25 5322 116 55549
R 806	RESISTOR,M.FILM	121	1	MR25 5322 116 54426
R 807	RESISTOR,M.FILM	121	1	MR25 5322 116 54426
R 808	RESISTOR,M.FILM	2,61K	1	MR25 5322 116 50671
R 809	RESISTOR,M.FILM	1,33K	1	MR25 5322 116 55422
R 811	RESISTOR,SAFETY	7,87K	1	MR25 5322 116 50458
R 812	POTM,TRIMMING	4,7K	20	0.5W 5322 100 10114
R 813	POTM,TRIMMING	10K	20	0,5W 5322 100 10113
R 814	POTM,TRIMMING	2,2K	20	0.5W 5322 101 14003
R 816	RESISTOR,M.FILM	30,1	1	MR25 5322 116 50904
R 817	POTM,TRIMMING	100	20	0.05W 4822 100 10075
R 818	RESISTOR,M.FILM	30,1	1	MR25 5322 116 50904
R 819	RESISTOR,M.FILM	28,7	1	MR25 5322 116 54068
R 821	RESISTOR,M.FILM	28,7	1	MR25 5322 116 54068
R 823	RESISTOR,M.FILM	169	1	MR25 5322 116 54489
R 824	RESISTOR,SAFETY	7,87K	1	MR25 5322 116 50458

POSNR	DESCRIPTION				ORDERING CODE
R 825	RESISTOR,M.FILM	4,99	1	MR25	5322 116 50568
R 826	RESISTOR,M.FILM	2,26K	1	MR25	5322 116 50675
R 827	RESISTOR,M.FILM	4,22K	1	MR25	5322 116 50729
R 828	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 829	RESISTOR,M.FILM	100	1	MR25	5322 116 55549
R 831	RESISTOR,M.FILM	86,6	1	MR25	5322 116 54464
R 832	RESISTOR,M.FILM	86,6	1	MR25	5322 116 54464
R 833	RESISTOR,M.FILM	909	1	MR25	5322 116 55278
R 837	RESISTOR,M.FILM	909	1	MR25	5322 116 55278
R 838	RESISTOR,M.FILM	1,21K	1	MR25	5322 116 54557
R 839	RESISTOR,M.FILM	1,21K	1	MR25	5322 116 54557
R 843	RESISTOR,M.FILM	681	1	MR25	4822 116 51233
R 847	RESISTOR,M.FILM	90,9	1	MR25	5322 116 54466
R 848	POTM,TRIMMING	100	20	0,5W	5322 101 14011
R 849	RESISTOR,M.FILM	90,9	1	MR25	5322 116 54466
R 851	RESISTOR,M.FILM	90,9	1	MR25	5322 116 54466
R 852	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 853	RESISTOR,M.FILM	51,1	1	MR25	5322 116 54442
R 854	RESISTOR,M.FILM	90,9	1	MR25	5322 116 54466
R 856	RESISTOR,M.FILM	140	1	MR25	5322 116 55568
R 857	RESISTOR,M.FILM	3,48K	1	MR25	5322 116 55367
R 858	RESISTOR,M.FILM	3,01K	1	MR25	4822 116 51246
R 859	RESISTOR,M.FILM	1,78K	1	MR25	5322 116 50515
R 861	RESISTOR,M.FILM	1,78K	1	MR25	5322 116 50515
R 862	RESISTOR,M.FILM	1,78K	1	MR25	5322 116 50515
R 863	RESISTOR,M.FILM	1,78K	1	MR25	5322 116 50515
R 9	POTM,CARB+SW.	10K	20	0.1W	5322 101 40096

JTN

Semi Conductors/Diodes

POSNR	DESCRIPTION		ORDERING CODE
V 1	CATHODERAY TUBE	D14-125GH/117	5322 131 20093
V 1001	DIODE	OA95	4822 130 30191
V 1002	DIODE	OA95	4822 130 30191
V 1003	DIODE	BAV45	5322 130 34037
V 1004	TRANSISTOR	BC548C	4822 130 44196
V 1006	TRANSISTOR	ON561	5322 130 41807
V 1008	TRANSISTOR	BC558B	4822 130 44197
V 1009	TRANSISTOR	BC548C	4822 130 44196
V 1011	TRANSISTOR	BC548C	4822 130 44196
V 1012	TRANSISTOR	BC548C	4822 130 44196
V 1013	TRANSISTOR	BC548C	4822 130 44196
V 1014	TRANSISTOR	BF450	4822 130 44237
V 1016	DIODE	BAW62	4822 130 30613
V 1017	TRANSISTOR	BC558B	4822 130 44197
V 1201	TRANSISTOR	BC548C	4822 130 44196
V 1202	DIODE	BAW62	4822 130 30613
V 1203	TRANSISTOR	BC558B	4822 130 44197
V 1204	TRANSISTOR	BC548C	4822 130 44196
V 1206	TRANSISTOR	BC558B	4822 130 44197
V 1207	DIODE	BAW62	4822 130 30613
V 1208	DIODE	BAW62	4822 130 30613
V 1209	DIODE	BAW62	4822 130 30613
V 1211	DIODE	BAW62	4822 130 30613
V 1212	TRANSISTOR	BC558B	4822 130 44197
V 1213	TRANSISTOR	BSX20	4822 130 41705
V 1214	TRANSISTOR	BC548C	4822 130 44196
V 1216	TRANSISTOR	BC548C	4822 130 44196
V 1217	TRANSISTOR	BC548C	4822 130 44196
V 1218	DIODE	BAW62	4822 130 30613
V 1219	TRANSISTOR	BC548C	4822 130 44196
V 1221	TRANSISTOR	BC548C	4822 130 44196
V 1222	DIODE	BAW62	4822 130 30613
V 1223	TRANSISTOR	BC548C	4822 130 44196
V 1401	TRANSISTOR	BC548C	4822 130 44196
V 1402	TRANSISTOR	BC548C	4822 130 44196
V 1403	DIODE	BAW62	4822 130 30613
V 1404	TRANSISTOR	BC558B	4822 130 44197
V 1406	TRANSISTOR	BF199	4822 130 44154
V 1407	TRANSISTOR	BF199	4822 130 44154
V 1408	DIODE	BAW62	4822 130 30613
V 1409	DIODE	BAW62	4822 130 30613
V 1411	DIODE	BAW62	4822 130 30613
V 1412	DIODE,REFERENCE	BZX79-C5V1	4822 130 34233
V 1413	TRANSISTOR	BFT45	5322 130 44603
V 1414	TRANSISTOR	BF338	5322 130 41713
V 1416	TRANSISTOR	BSX20	4822 130 41705
V 1417	DIODE	BAW62	4822 130 30613
V 1419	TRANSISTOR	BF450	4822 130 44237
V 1421	TRANSISTOR	BFT45	5322 130 44603
V 1422	TRANSISTOR	BF338	5322 130 41713
V 1423	DIODE,REFERENCE	BZX79-C5V1	4822 130 34233
V 1424	DIODE,REFERENCE	BZX79-C36	4822 130 34368
V 1426	DIODE,REFERENCE	BZX79-C36	4822 130 34368
V 1427	DIODE,REFERENCE	BZX79-C36	4822 130 34368
V 1428	DIODE,REFERENCE	BZX79-C75	4822 130 34685
V 1501	DIODE	BAW62	4822 130 30613
V 1502	DIODE	BAW62	4822 130 30613
V 1503	DIODE	BAW62	4822 130 30613
V 1504	DIODE	OA95	4822 130 30191
V 1506	TRANSISTOR	BC548C	4822 130 44196
V 1508	DIODE	BAW62	4822 130 30613
V 1511	DIODE	BAW62	4822 130 30613
V 1512	TRANSISTOR	BC558B	4822 130 44197
V 1513	TRANSISTOR	BC548C	4822 130 44196

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POSNR	DESCRIPTION		ORDERING CODE
V 1514	TRANSISTOR	BC548C	4822 130 44196
V 1516	TRANSISTOR	BC548C	4822 130 44196
V 1517	THYRISTOR	BSS68	5322 130 44247
V 1518	DIODE	BAW21	4822 130 30842
V 1519	DIODE	BAW21	4822 130 30842
V 1521	TRANSISTOR	BC548C	4822 130 44196
V 1522	TRANSISTOR	BC558B	4822 130 44197
V 1601	TRANSISTOR	BC548C	4822 130 44196
V 1602	TRANSISTOR	BC548C	4822 130 44196
V 1603	TRANSISTOR	BC548C	4822 130 44196
V 1604	DIODE	BAW62	4822 130 30613
V 1701	DIODE	BAW62	4822 130 30613
V 1702	TRANSISTOR	BC548C	4822 130 44196
V 1703	DIODE	BAW62	4822 130 30613
V 1704	DIODE	BAW62	4822 130 30613
V 1706	DIODE	BAW62	4822 130 30613
V 1707	TRANSISTOR	BC548C	4822 130 44196
V 1708	TRANSISTOR	BC548C	4822 130 44196
V 1709	TRANSISTOR	BC558B	4822 130 44197
V 1710	TRANSISTOR	BC548C	4822 130 44196
V 1711	TRANSISTOR	BC558B	4822 130 44197
V 1712	TRANSISTOR	BC548C	4822 130 44196
V 1713	TRANSISTOR	BC548C	4822 130 44196
V 1714	DIODE	BAW62	4822 130 30613
V 1716	DIODE	BAW62	4822 130 30613
V 1717	TRANSISTOR	BC548C	4822 130 44196
V 1718	TRANSISTOR	BC548C	4822 130 44196
V 1719	TRANSISTOR,FET	BF410C	4822 130 41482
V 1721	DIODE	BAW62	4822 130 30613
V 1723	TRANSISTOR	BC548C	4822 130 44196
V 1724	TRANSISTOR,FET	BSV78	5322 130 44093
V 1726	TRANSISTOR	BC558B	4822 130 44197
V 1727	TRANSISTOR	BC548C	4822 130 44196
V 1728	TRANSISTOR	BC558B	4822 130 44197
V 1729	TRANSISTOR	BC558B	4822 130 44197
V 1731	TRANSISTOR	BC548C	4822 130 44196
V 1732	DIODE	BAW62	4822 130 30613
V 1733	DIODE	BAW62	4822 130 30613
V 1734	DIODE	BAW62	4822 130 30613
V 1736	TRANSISTOR	BC548C	4822 130 44196
V 1737	TRANSISTOR	BC548C	4822 130 44196
V 1738	DIODE,REFERENCE	BZX79-C6V8	4822 130 34278
V 1750	TRANSISTOR	BC548C	4822 130 44196
V 1751	TRANSISTOR	BC558B	4822 130 44197
V 1752	TRANSISTOR	BC558B	4822 130 44197
V 1753	TRANSISTOR	BC548C	4822 130 44196
V 1754	TRANSISTOR	BC548C	4822 130 44196
V 1756	DIODE	BAW62	4822 130 30613
V 1757	DIODE	BAW62	4822 130 30613
V 1758	TRANSISTOR	BC548C	4822 130 44196
V 1759	TRANSISTOR	BC548C	4822 130 44196
V 1761	TRANSISTOR,FET	BF410C	4822 130 41482
V 1762	DIODE	BAW62	4822 130 30613
V 1763	TRANSISTOR	BC548C	4822 130 44196
V 1764	TRANSISTOR	BC548C	4822 130 44196
V 1766	TRANSISTOR,FET	BSV78	5322 130 44093
V 1767	TRANSISTOR	BC558B	4822 130 44197
V 1768	TRANSISTOR	BC558B	4822 130 44197
V 1769	TRANSISTOR	BC558B	4822 130 44197
V 1771	TRANSISTOR	BC548C	4822 130 44196
V 1772	TRANSISTOR	BC548C	4822 130 44196
V 1773	TRANSISTOR	BC548C	4822 130 44196
V 1774	DIODE	BAW62	4822 130 30613
V 1776	DIODE	BAW62	4822 130 30613
V 1801	DIODE,REFERENCE	BZV46-C1V5	5322 130 34865

POSNR	DESCRIPTION		ORDERING CODE
V 1901	TRANSISTOR	BC548C	4822 130 44196
V 1902	TRANSISTOR	BC548C	4822 130 44196
V 1903	DIODE,REFERENCE	BZV46-C2V0	4822 130 31248
V 1904	TRANSISTOR	BC548C	4822 130 44196
V 1906	TRANSISTOR	BC558B	4822 130 44197
V 1907	DIODE,REFERENCE	BZV46-C2V0	4822 130 31248
V 1908	TRANSISTOR	BC548C	4822 130 44196
V 1909	TRANSISTOR	BC558B	4822 130 44197
V 1911	DIODE,REFERENCE	BZV46-C2V0	4822 130 31248
V 1912	TRANSISTOR	BC548C	4822 130 44196
V 1913	TRANSISTOR	BC558B	4822 130 44197
V 1914	DIODE,REFERENCE	BZV46-C2V0	4822 130 31248
V 1916	TRANSISTOR	BC548C	4822 130 44196
V 1917	TRANSISTOR	BC558B	4822 130 44197
V 1918	DIODE	BAW62	4822 130 30613
V 1919	DIODE	BAW62	4822 130 30613
V 1921	DIODE	BAW62	4822 130 30613
V 1922	TRANSISTOR	BF324	4822 130 41448
V 1923	TRANSISTOR	BF324	4822 130 41448
V 1924	DIODE	BAW62	4822 130 30613
V 1926	DIODE	BAW62	4822 130 30613
V 1927	DIODE	BAW62	4822 130 30613
V 1928	TRANSISTOR	BF324	4822 130 41448
V 1929	TRANSISTOR	BF324	4822 130 41448
V 1931	DIODE	BAW62	4822 130 30613
V 1932	DIODE	BAW62	4822 130 30613
V 1933	DIODE	BAW62	4822 130 30613
V 1934	DIODE	BAW62	4822 130 30613
V 1936	DIODE	BAW62	4822 130 30613
V 1937	DIODE	BAW62	4822 130 30613
V 1938	TRANSISTOR	BC548C	4822 130 44196
V 1939	DIODE	BAW62	4822 130 30613
V 2001	DIODE	BAW62	4822 130 30613
V 2002	DIODE	BAW62	4822 130 30613
V 2003	DIODE	BAW62	4822 130 30613
V 2004	DIODE	BAW62	4822 130 30613
V 2006	DIODE	BAW62	4822 130 30613
V 2007	DIODE,REFERENCE	BZV46-C1V5	5322 130 34865
V 2008	DIODE,REFERENCE	BZV11	5322 130 34294
V 2009	DIODE	HSCH-1001	4822 130 31689
V 201	DIODE	BY225-200	4822 130 50312
V 2011	DIODE	HSCH-1001	4822 130 31689
V 206	DIODE	BYX49-1200	5322 130 31641
V 207	TRANSISTOR	BD237	4822 130 44235
V 208	DIODE	BAW62	4822 130 30613
V 209	DIODE,REFERENCE	BZX79-C5V6	4822 130 34173
V 211	DIODE,REFERENCE	BZX75-C3V6	4822 130 30765
V 212	DIODE,REFERENCE	BZX75-C3V6	4822 130 30765
V 213	DIODE	BAW62	4822 130 30613
V 214	TRANSISTOR	BC548C	4822 130 44196
V 216	TRANSISTOR	BC558B	4822 130 44197
V 217	TRANSISTOR	BDX77 SEL PAIR	5322 130 44899
V 219	DIODE	BAW62	4822 130 30613
V 221	DIODE	BAW62	4822 130 30613
V 222	DIODE	BAW62	4822 130 30613
V 223	DIODE	BAW62	4822 130 30613
V 224	DIODE	BAW62	4822 130 30613
V 2301	DIODE	BAW62	4822 130 30613
V 2302	DIODE	BAW62	4822 130 30613
V 2303	DIODE	BAW62	4822 130 30613
V 2304	DIODE	BAW62	4822 130 30613
V 2306	TRANSISTOR	ON561	5322 130 41807
V 2307	TRANSISTOR	BC548C	4822 130 44196
V 2308	TRANSISTOR	BC548C	4822 130 44196
V 2309	TRANSISTOR	ON561	5322 130 41807

POSNR	DESCRIPTION		ORDERING CODE
V 2311	TRANSISTOR	BC548C	4822 130 44196
V 2312	TRANSISTOR	BC548C	4822 130 44196
V 2313	TRANSISTOR	BC558B	4822 130 44197
V 2314	TRANSISTOR	BC558B	4822 130 44197
V 2316	TRANSISTOR	BC548C	4822 130 44196
V 2317	TRANSISTOR	BC548C	4822 130 44196
V 232	DIODE	BY509	4822 130 41485
V 233	DIODE,REFERENCE	BZX[illegible]-C110	5322 130 34671
V 234	DIODE	BY206	4822 130 30839
V 2351	DIODE	BAW62	4822 130 30613
V 2352	DIODE	BAW62	4822 130 30613
V 2353	DIODE	BAW62	4822 130 30613
V 2354	DIODE	BAW62	4822 130 30613
V 2356	TRANSISTOR	ON561	5322 130 41807
V 2357	TRANSISTOR	BC548C	4822 130 44196
V 2358	TRANSISTOR	BC548C	4822 130 44196
V 2359	TRANSISTOR	ON561	5322 130 41807
V 236	DIODE	BY206	4822 130 30839
V 2361	TRANSISTOR	BC548C	4822 130 44196
V 2362	TRANSISTOR	BC548C	4822 130 44196
V 2363	TRANSISTOR	BC558B	4822 130 44197
V 2364	TRANSISTOR	BC558B	4822 130 44197
V 2366	TRANSISTOR	BC548C	4822 130 44196
V 2367	TRANSISTOR	BC548C	4822 130 44196
V 237	DIODE	BAW62	4822 130 30613
V 238	DIODE	BAX12 DO-35	5322 130 34605
V 239	DIODE	BAX12 DO-35	5322 130 34605
V 241	DIODE	BAX12 DO-35	5322 130 34605
V 242	DIODE	BAX12 DO-35	5322 130 34605
V 243	DIODE	BAX12 DO-35	5322 130 34605
V 244	DIODE	BAX12 DO-35	5322 130 34605
V 246	DIODE	BAW62	4822 130 30613
V 247	DIODE	BY206	4822 130 30839
V 2501	TRANSISTOR	BC548C	4822 130 44196
V 2502	TRANSISTOR	BC548C	4822 130 44196
V 2503	TRANSISTOR	BC548C	4822 130 44196
V 2504	TRANSISTOR	BF324	4822 130 41448
V 2506	TRANSISTOR	BF324	4822 130 41448
V 2507	TRANSISTOR	BF324	4822 130 41448
V 2508	TRANSISTOR	BF324	4822 130 41448
V 2509	TRANSISTOR	BC548C	4822 130 44196
V 251	DIODE	BAX12A	5322 130 34605
V 2511	TRANSISTOR	BC548C	4822 130 44196
V 2512	TRANSISTOR	BC548C	4822 130 44196
V 2513	TRANSISTOR	BC548C	4822 130 44196
V 2514	TRANSISTOR	BC548C	4822 130 44196
V 2516	TRANSISTOR	BC548C	4822 130 44196
V 2517	TRANSISTOR	BF324	4822 130 41448
V 2518	TRANSISTOR	BF324	4822 130 41448
V 2519	TRANSISTOR	BF324	4822 130 41448
V 252	DIODE	BAX12A	5322 130 34605
V 2521	TRANSISTOR	BC558B	4822 130 44197
V 2522	DIODE	BAW62	4822 130 30613
V 2523	TRANSISTOR	BC558B	4822 130 44197
V 2524	DIODE	BAW62	4822 130 30613
V 2526	DIODE,REFERENCE	BZV11	5322 130 34294
V 2527	DIODE,REFERENCE	BZV46-C1V5	5322 130 34865
V 2528	DIODE,REFERENCE	BZX79-C4V7	4822 130 34174
V 253	DIODE	BAW29-150	5322 130 34711
V 254	DIODE	BAW29-150	5322 130 34711
V 256	DIODE	BAX12A	5322 130 34605
V 257	DIODE	BAX12A	5322 130 34605
V 351	TRANSISTOR	BF450	4822 130 44237
V 352	TRANSISTOR	BF450	4822 130 44237
V 353	TRANSISTOR	BC548C	4822 130 44196

POSNR	DESCRIPTION		ORDERING CODE
V 354	DIODE	BAW62	4822 130 30613
V 356	DIODE	BAW62	4822 130 30613
V 357	DIODE	BAW62	4822 130 30613
V 501	DIODE	BAV45	5322 130 34037
V 504	TRANSISTOR,FET	BFS21A	5322 130 40709
V 508	TRANSISTOR	BF450	4822 130 44237
V 509	TRANSISTOR	BF450	4822 130 44237
V 511	TRANSISTOR	BF450	4822 130 44237
V 512	TRANSISTOR	BF450	4822 130 44237
V 513	TRANSISTOR	BC558B	4822 130 44197
V 514	TRANSISTOR	BC558B	4822 130 44197
V 518	TRANSISTOR	BC548C	4822 130 44196
V 519	TRANSISTOR	BC548C	4822 130 44196
V 521	DIODE	BAW62	4822 130 30613
V 522	DIODE	BAW62	4822 130 30613
V 523	DIODE	BAW62	4822 130 30613
V 524	TRANSISTOR	BF324	4822 130 41448
V 526	TRANSISTOR	BF324	4822 130 41448
V 601	DIODE	BAV45	5322 130 34037
V 604	TRANSISTOR,FET	BFS21A	5322 130 40709
V 608	TRANSISTOR	BF450	4822 130 44237
V 609	TRANSISTOR	BF450	4822 130 44237
V 611	TRANSISTOR	BF450	4822 130 44237
V 612	TRANSISTOR	BF450	4822 130 44237
V 613	TRANSISTOR	BC558B	4822 130 44197
V 614	TRANSISTOR	BC558B	4822 130 44197
V 616	TRANSISTOR	BC558B	4822 130 44197
V 617	TRANSISTOR	BC558B	4822 130 44197
V 618	TRANSISTOR	BC548C	4822 130 44196
V 619	TRANSISTOR	BC548C	4822 130 44196
V 621	DIODE	BAW62	4822 130 30613
V 622	DIODE	BAW62	4822 130 30613
V 623	DIODE	BAW62	4822 130 30613
V 624	TRANSISTOR	BF324	4822 130 41448
V 626	TRANSISTOR	BF324	4822 130 41448
V 701	DIODE	BAW62	4822 130 30613
V 702	DIODE	BAW62	4822 130 30613
V 703	TRANSISTOR	BC548C	4822 130 44196
V 704	TRANSISTOR	BC548C	4822 130 44196
V 801	TRANSISTOR	BC558B	4822 130 44197
V 802	TRANSISTOR	BC548C	4822 130 44196
V 803	TRANSISTOR	BC548C	4822 130 44196
V 804	TRANSISTOR	BF199	4822 130 44154
V 806	TRANSISTOR	BF199	4822 130 44154
V 807	TRANSISTOR	BF199	4822 130 44154
V 808	TRANSISTOR	BF199	4822 130 44154
V 809	TRANSISTOR	BC548C	4822 130 44196

Miscellaneous

B 10	LED	LED CQY54/III	5322 130 34875
B 11	LED	LED CQY54/III	5322 130 34875
B 12	LED	LED CQY54/III	5322 130 34875
B 1	LED	CQY24B/IV	4822 130 31144
B 2	LED	CQY54/III	5322 130 34875
B 3	LED	CQY54/III	5322 130 34875
B 4	LED	CQY54/III	5322 130 34875
B 5	LED	CQY54/III	5322 130 34875
B 6	LED	CQY54/III	5322 130 34875
B 7	LED	CQY54/III	5322 130 34875
B 8	LED	CQY54/III	5322 130 34875
B 9	LED	CQY54/III	5322 130 34875
E 1	HOLDER,LAMP	LAMP HOLDER	5322 255 24015
E 1	LAMP,FILAMENT		5322 134 44177
E 2	LAMP,FILAMENT		5322 134 44177
F 101	FUSE	FUSE 15x20 500mA	4822 253 30017
F 102	FUSE	THERMAL FUSE	4822 252 20017
F 201	FUSE		4822 253 30023
F 202	FUSE		4822 253 30023
G 2001	CRYSTAL	CRYSTAL 5MC	5322 242 74397
K 1401	RELAY,REED	SAM.REED-RELAIS	5322 280 24131
K 1701	RELAY,REED		5322 280 20099
K 1702	RELAY,REED		5322 280 20099
K 501	RELAY,REED		5322 280 24131
K 601	RELAY,REED		5322 280 24131
L 1501	COIL,CORRECTION		5322 150 14015
L 201	COIL		5322 281 64154
L 202	COIL		5322 281 64154
L 203	COIL		5322 281 64154
L 251	COIL,CHOKE		5322 152 24092
L 801	COIL		5322 156 14074
L 802	COIL		5322 156 14074
S 101	ADAPTER,VOLTAGE	LINE VOLTAGE ADAPTER	5322 272 10226
S 1	SWITCH,PUSHBUT.		5322 276 84076
S 10	SWITCH,ROTARY		5322 273 80258
S 101	ADAPTER,VOLTAGE		5322 272 10226
S 12	SWITCH,PUSHBUT.		5322 276 20314
S 14	SWITCH,PUSHBUT.		5322 276 20314
S 16	SWITCH,PUSHBUT.		5322 276 40306
S 17	SWITCH,PUSHBUT.		5322 276 30303
S 20	SWITCH,PUSHBUT.		5322 276 30303
S 2001	PLUG,MALE		5322 265 44074
S 2002	SWITCH,SLIDE		5322 277 24053
S 23	SWITCH,PUSHBUT.		5322 276 30302
S 26	SWITCH,PUSHBUT.		5322 276 30301
S 29	SWITCH,PUSHBUT.		5322 276 30304
S 6	SWITCH,ROTARY		5322 273 74011
S 8	SWITCH,ROTARY		5322 273 74011
T 101	TRANSFORMER		5322 146 40334
T 201	TRANSFORMER		5322 158 34074
T 202	TRANSFORMER		5322 148 84047

9.3. IEEE-488 BUS INTERFACE UNIT A14 (PM 8955).

Capacitors:

C2401	cap, electrolyt.	10 uF -10+50	63		4822 124 20728
C2402	capacitor, ceram	10 nF -20+50	100		4822 122 31414
C2403	capacitor, ceram	10 nF -20+50	100		4822 122 31414
C2404	capacitor, ceram	10 nF -20+50	100		4822 122 31414
C2406	capacitor, ceram	10 nF -20+50	100		4822 122 31414
C2407	capacitor, ceram	10 nF -20+50	100		4822 122 31414

Resistors:

R2401	resistor	3,3K	2	9x0,2W	5322 111 94255

Integrated circuits:

D2401	integr. circuit	P8291A	5322 209 81264
D2402	integr. circuit	P8293	5322 209 81265
D2403	integr. circuit	P8293	5322 209 81265
D2404	integr. circuit	SN74LS245N-00	5322 209 86225
D2406	integr. circuit	N74LS139N	5322 209 85839

Miscellaneous:

X2401	connector	5322 267 74062
X2402	socket, male	5322 265 64071
	screw	5322 502 60037
	spacer	5322 500 10311
	nut	5322 500 10312
A14	IEEE interface unit	5322 216 51038
D2082	IEEE PROM assy	5322 209 10429
	Cable + connectors	5322 321 20684

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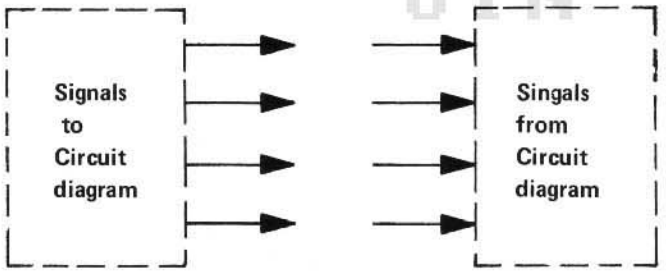
10. P.C.B.'S AND CIRCUIT DIAGRAMS

This chapter contains the drawings of the printed circuit boards and the circuit diagrams.

The drawings of the printed circuit boards are given in unit number sequence. The unit numbers are given on the circuit diagrams.

Circuit diagrams following the drawings of the printed circuit boards are given in DIAGRAM number sequence, this means the same sequence as used in the circuit descriptions chapter number 3.

References to other circuit diagrams.



AC POWER UNIT A1

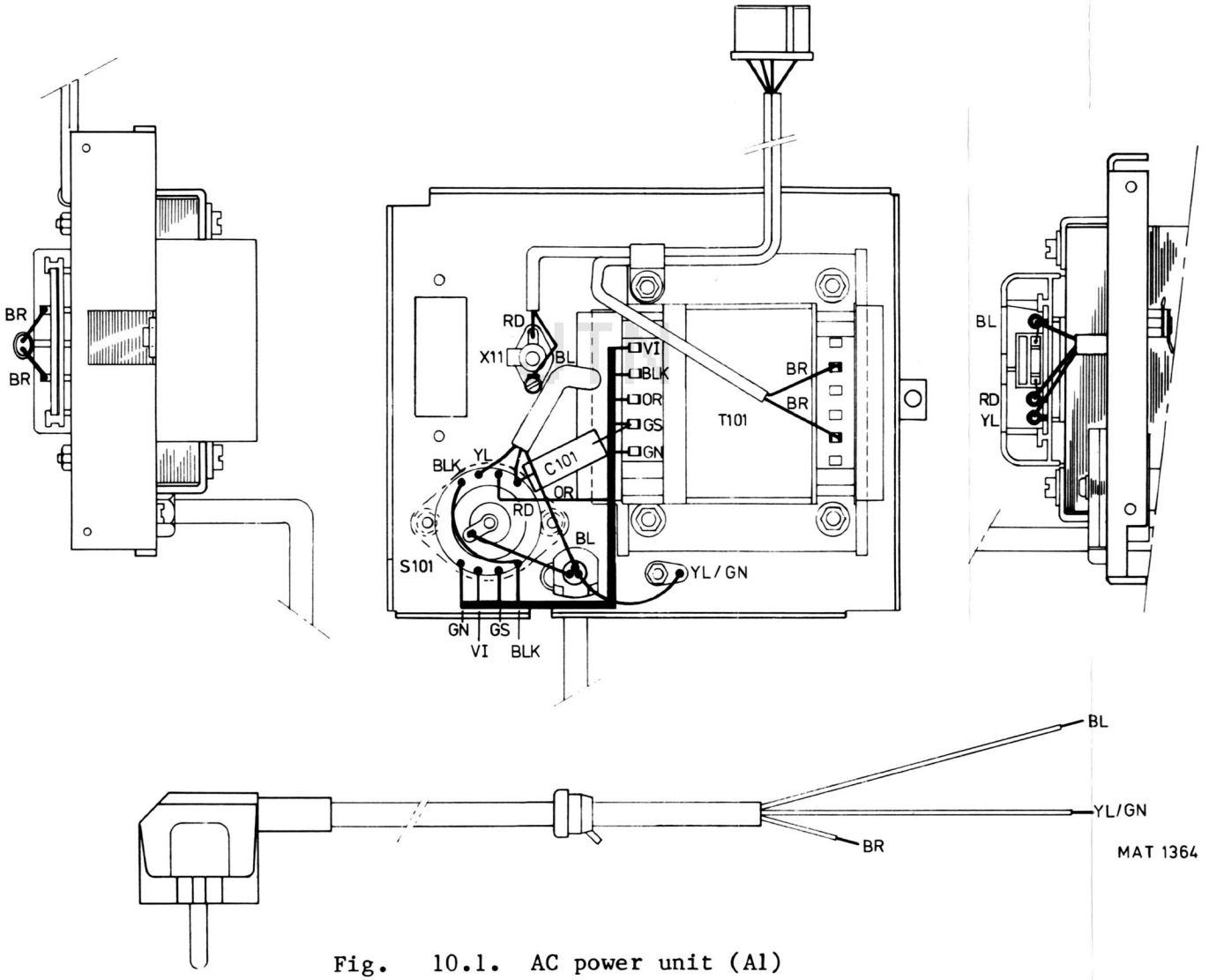


Fig. 10.1. AC power unit (A1)

FRONT UNIT A3

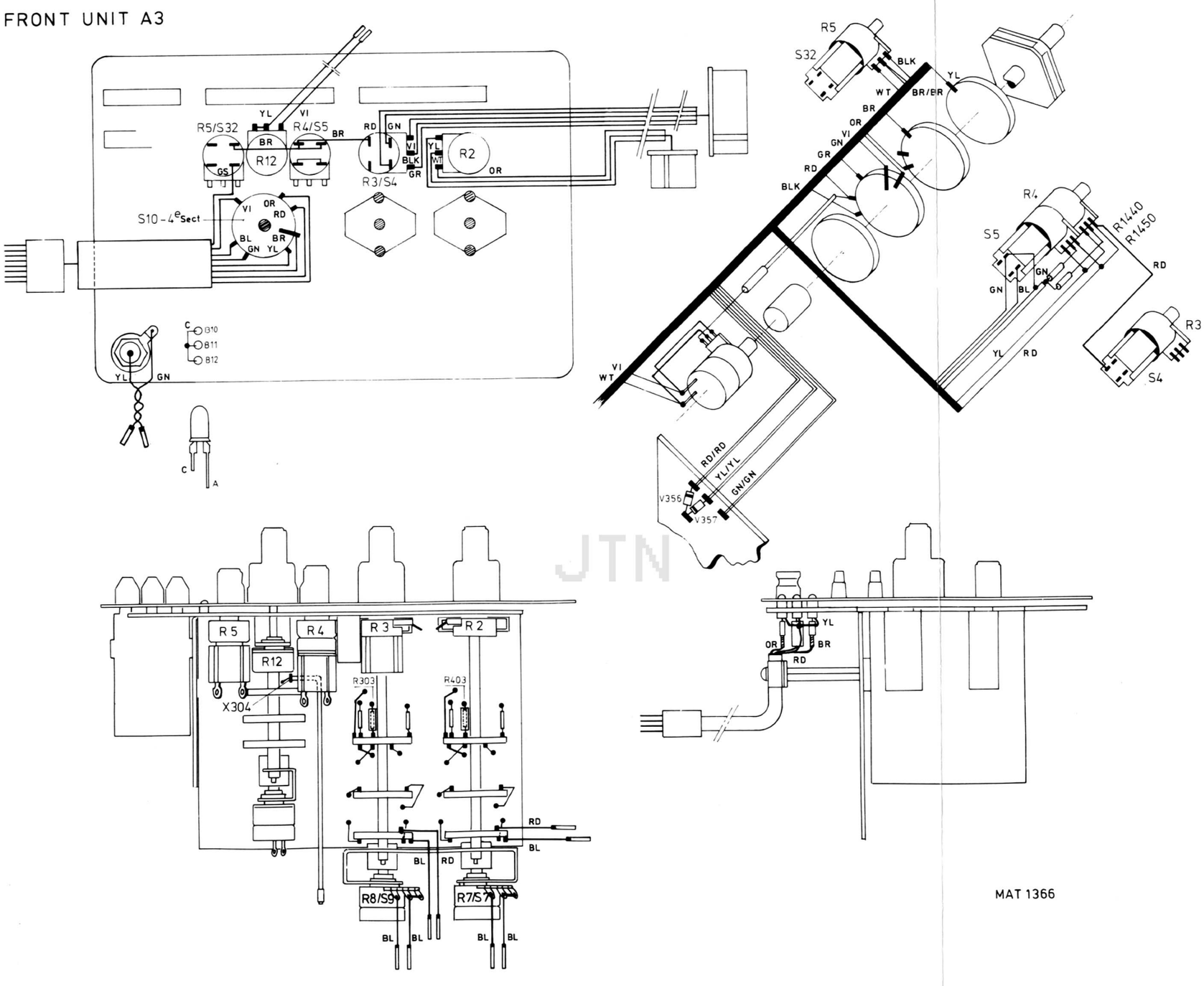


Fig. 10.3. Front unit (A3)

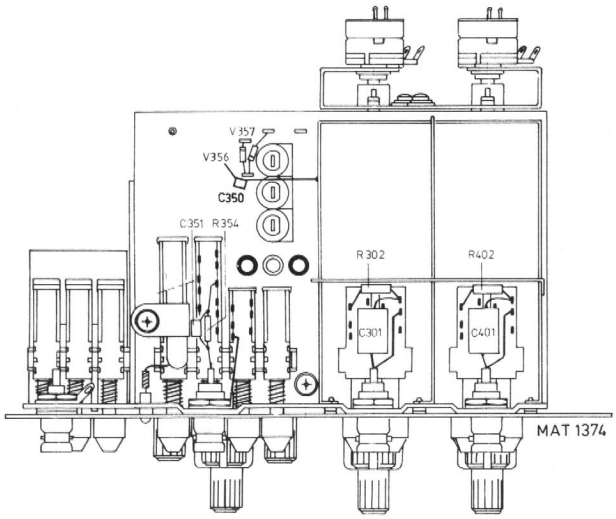


Fig. 10.4. Attenuator unit (A301)

ATTENUATOR UNIT A301

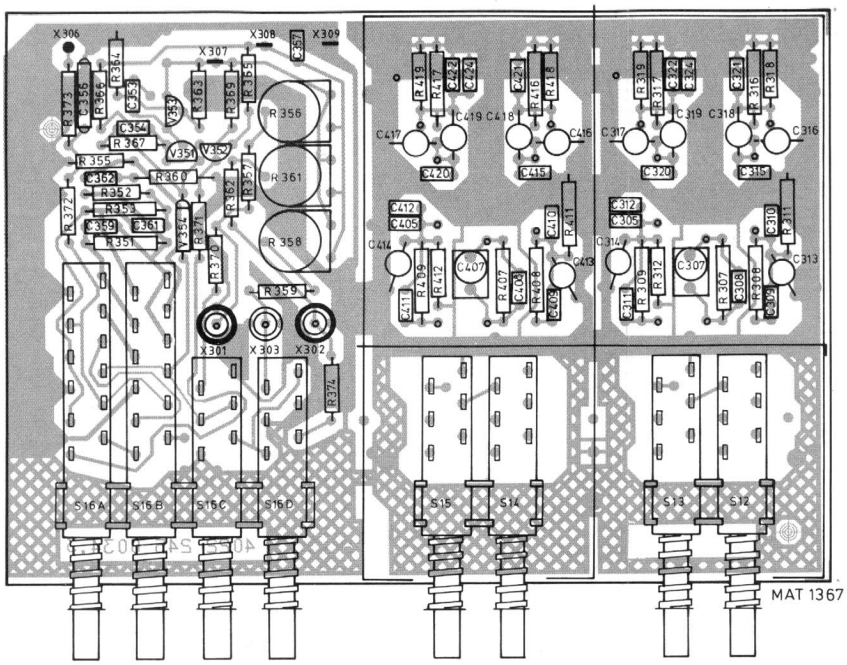


Fig. 10.5. Attenuator unit (A301)

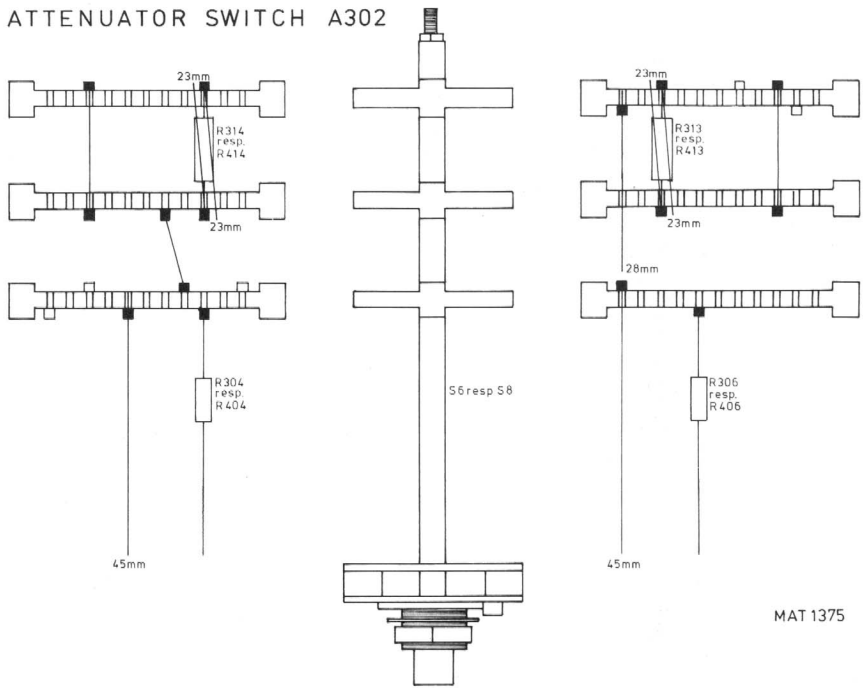


Fig. 10.6. Attenuator switch (A302)

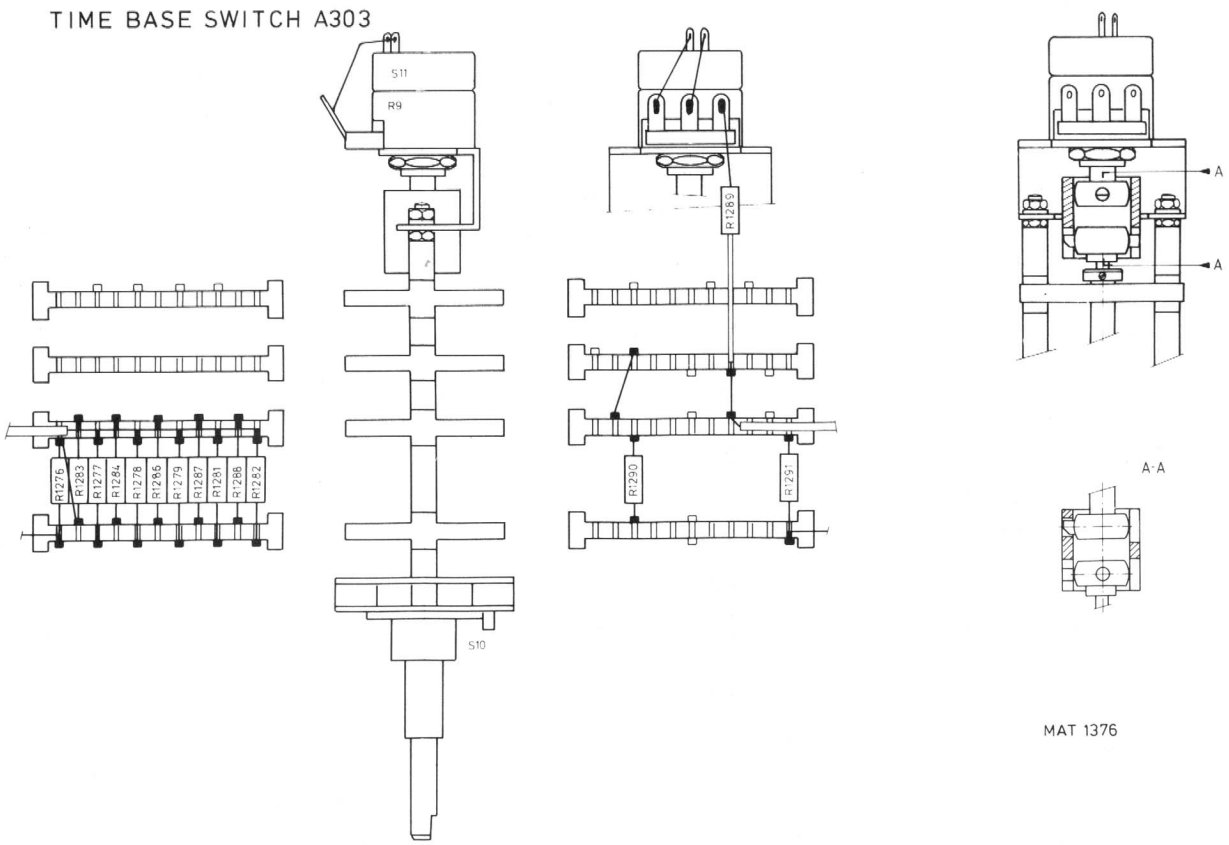


Fig. 10.7. Time-base switch (A303)

MEMORY SWITCH UNIT A304

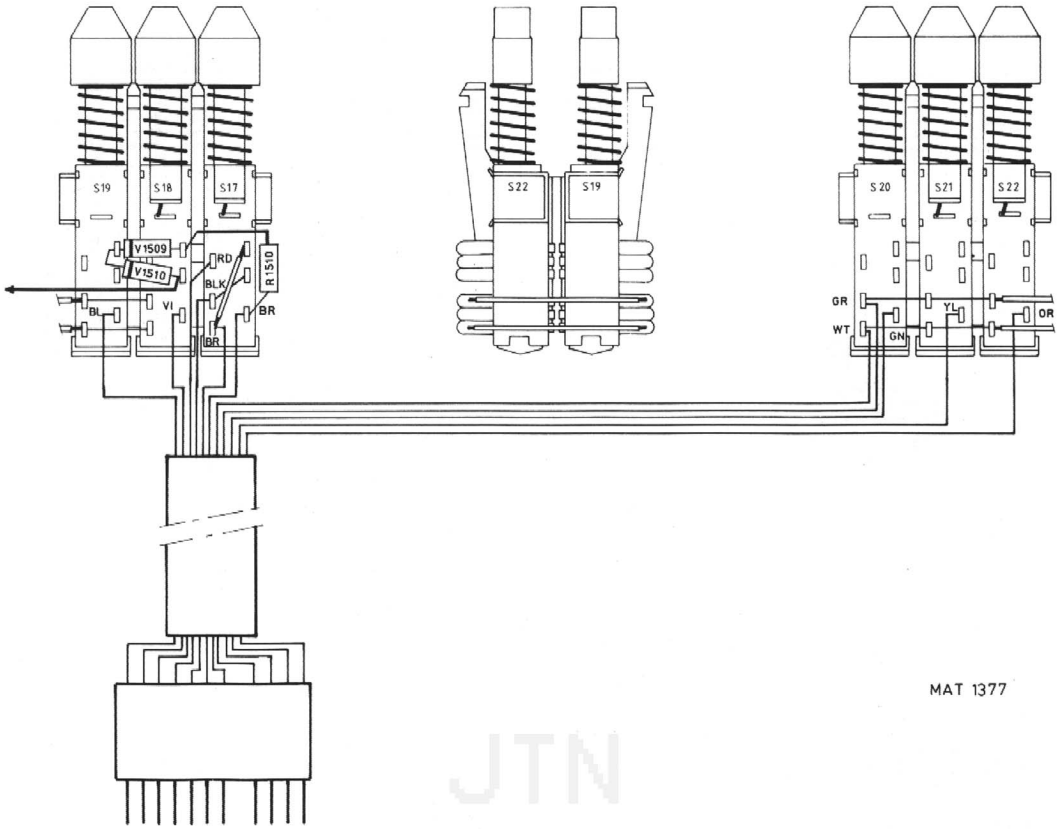
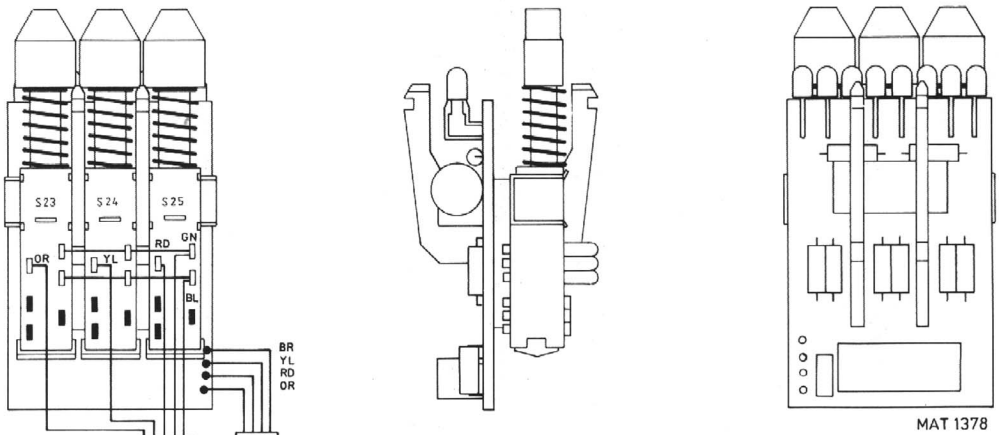


Fig. 10.8. Memory switch unit (A304)

LEDBAR UNIT A305



LEDBAR UNIT A305

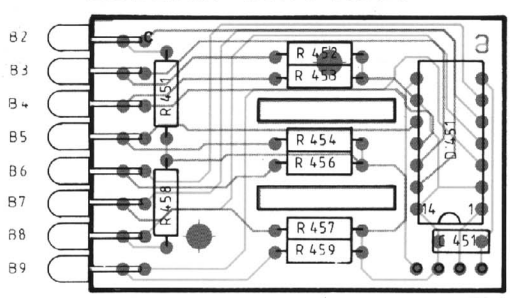


Fig. 10.9. Ledbar unit (A305)

SMOOTH SWITCH UNIT A306

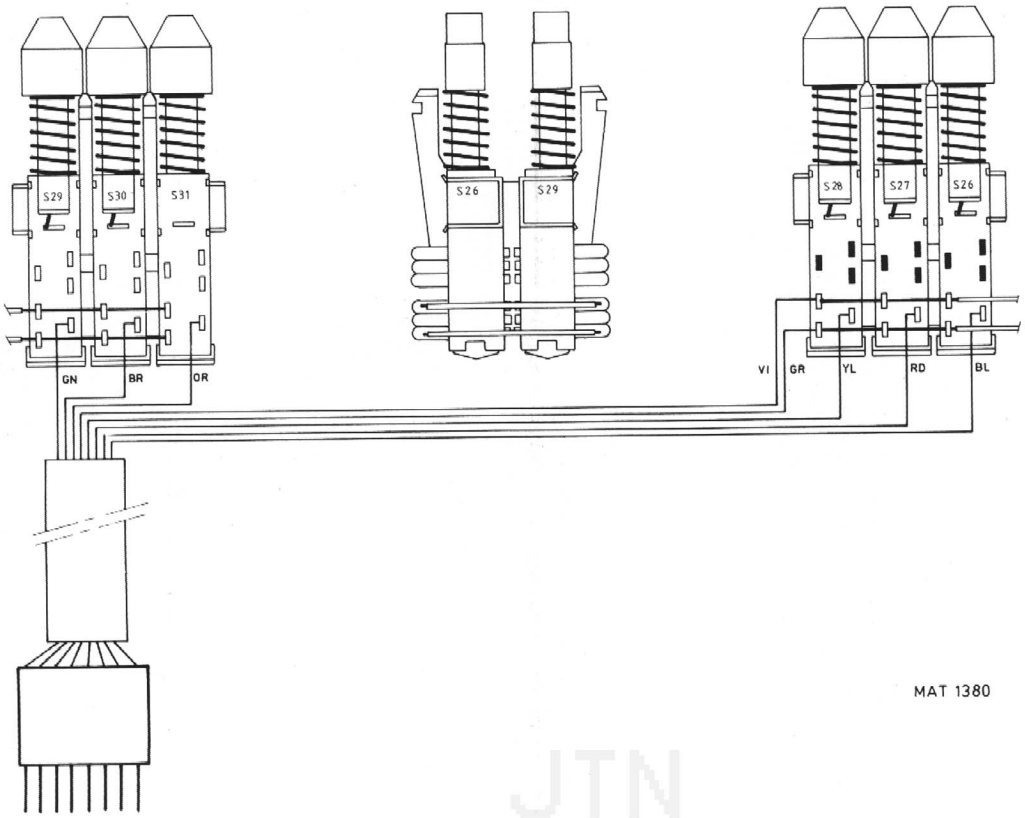


Fig. 10.10. Smooth switch unit (A306)

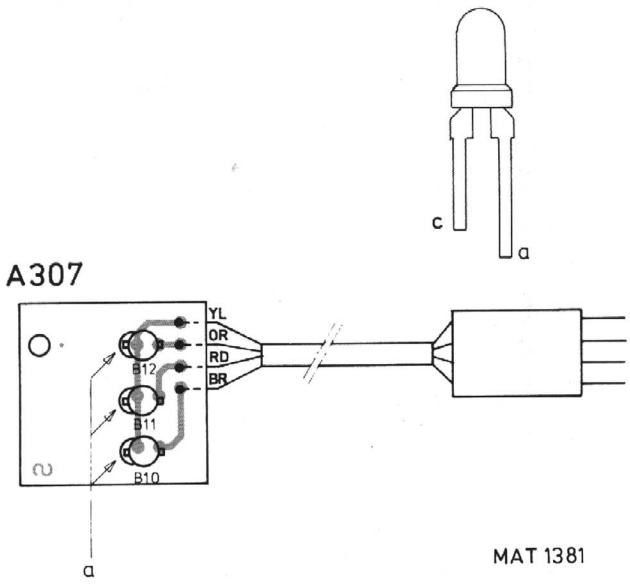


Fig. 10.11. Triple led unit (A307)

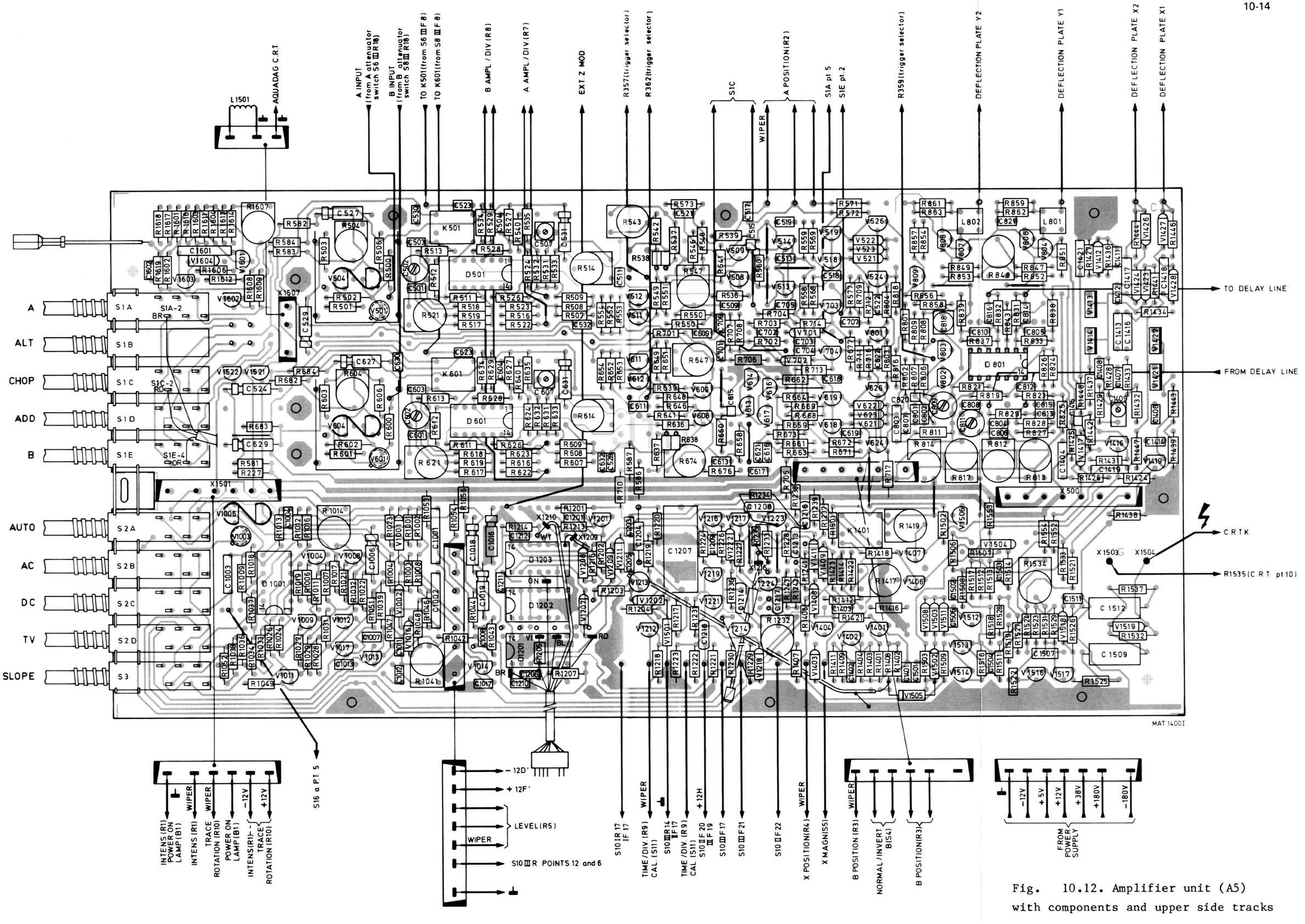
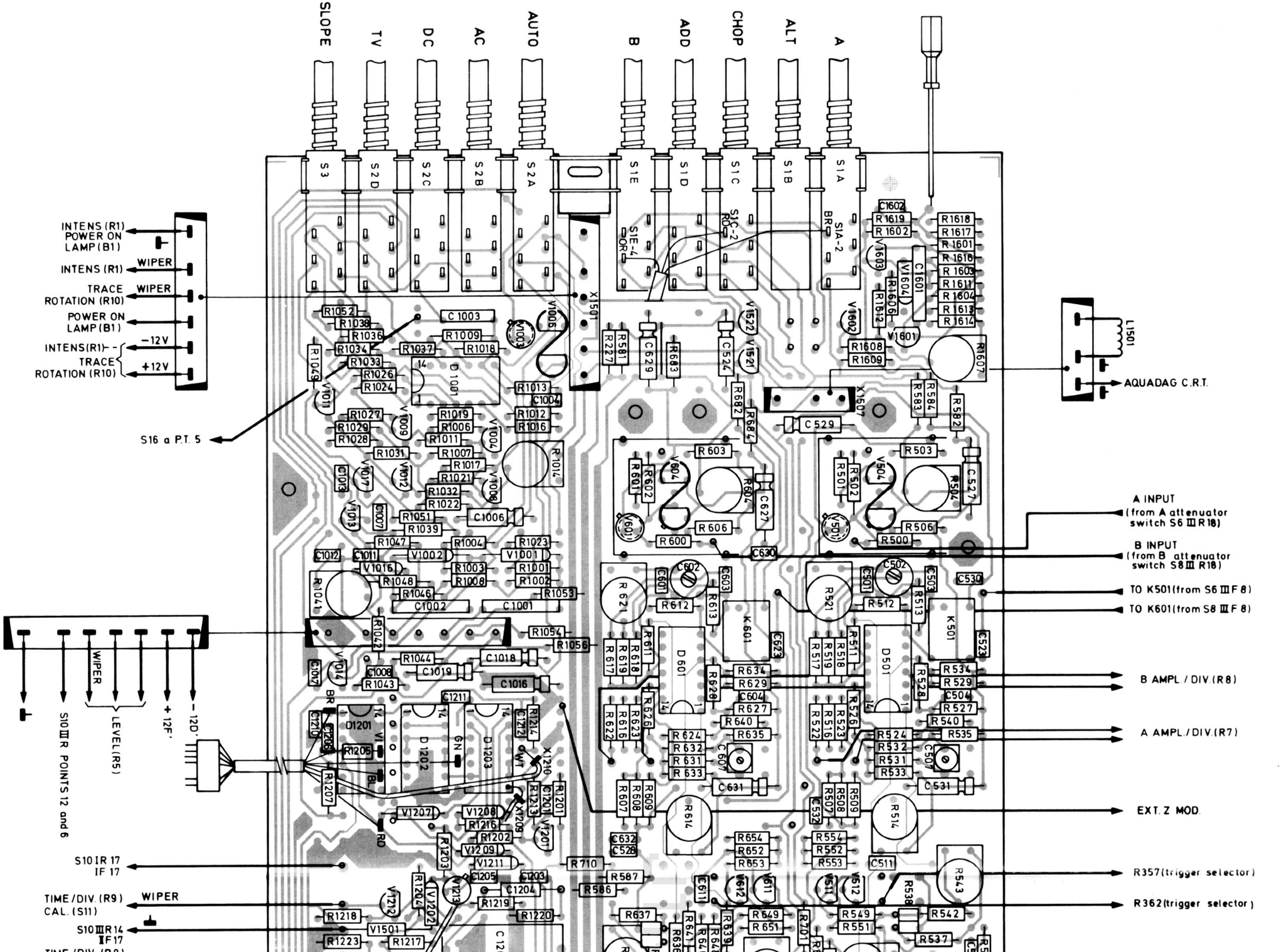


Fig. 10.12. Amplifier unit (A5) with components and upper side tracks


SLOPE
TV
DC
AC
AUTO
B
ADD
CHOP
ALT
A
S3
S2D
S2C
S2B
S2A
S1E
S1D
S1C
S1B
S1A
S1E-4
S1C-2
S1A-2
INTENS (R1)
POWER ON LAMP (B1)
INTENS (R1)
WIPER
TRACE ROTATION (R10)
WIPER
POWER ON LAMP (B1)
–12V
INTENS (R1)
+12V
TRACE ROTATION (R10)
S16 a P.T. 5
L1501
AQUADAG C.R.T.
A INPUT
(from A attenuator switch S6 III R18)
B INPUT
(from B attenuator switch S8 III R18)
TO K501 (from S6 III F 8)
TO K601 (from S8 III F 8)
B AMPL / DIV. (R8)
A AMPL. / DIV. (R7)
EXT. Z MOD.
R357 (trigger selector)
R362 (trigger selector)
S10 III R POINTS 12 and 6
WIPER
LEVEL (R5)
+ 12F'
– 12D'
S10 IR 17
IF 17
TIME / DIV. (R9)
CAL. (S11)
WIPER
S10 III R14
IF 17

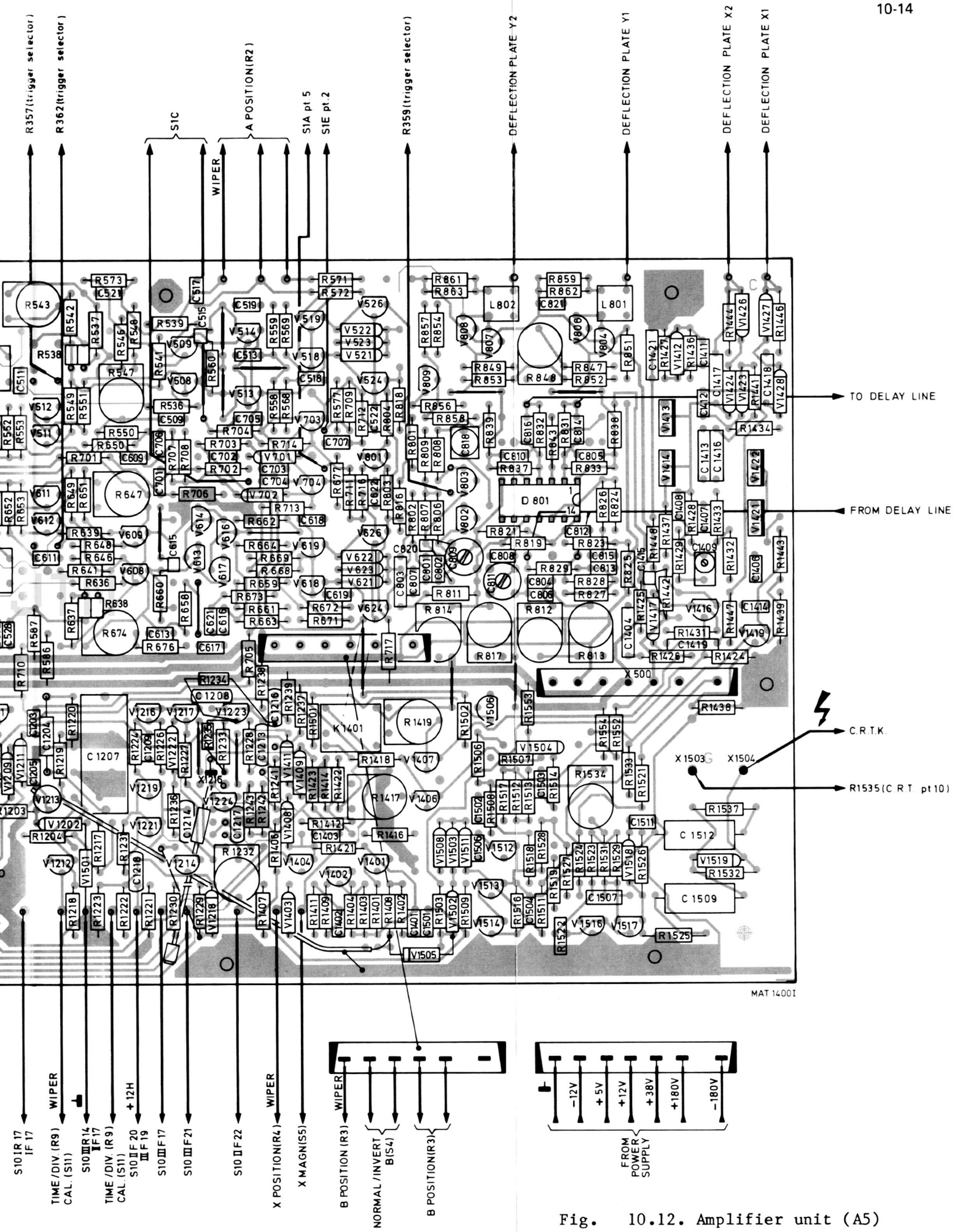


Fig. 10.12. Amplifier unit (A5) with components and upper side tracks

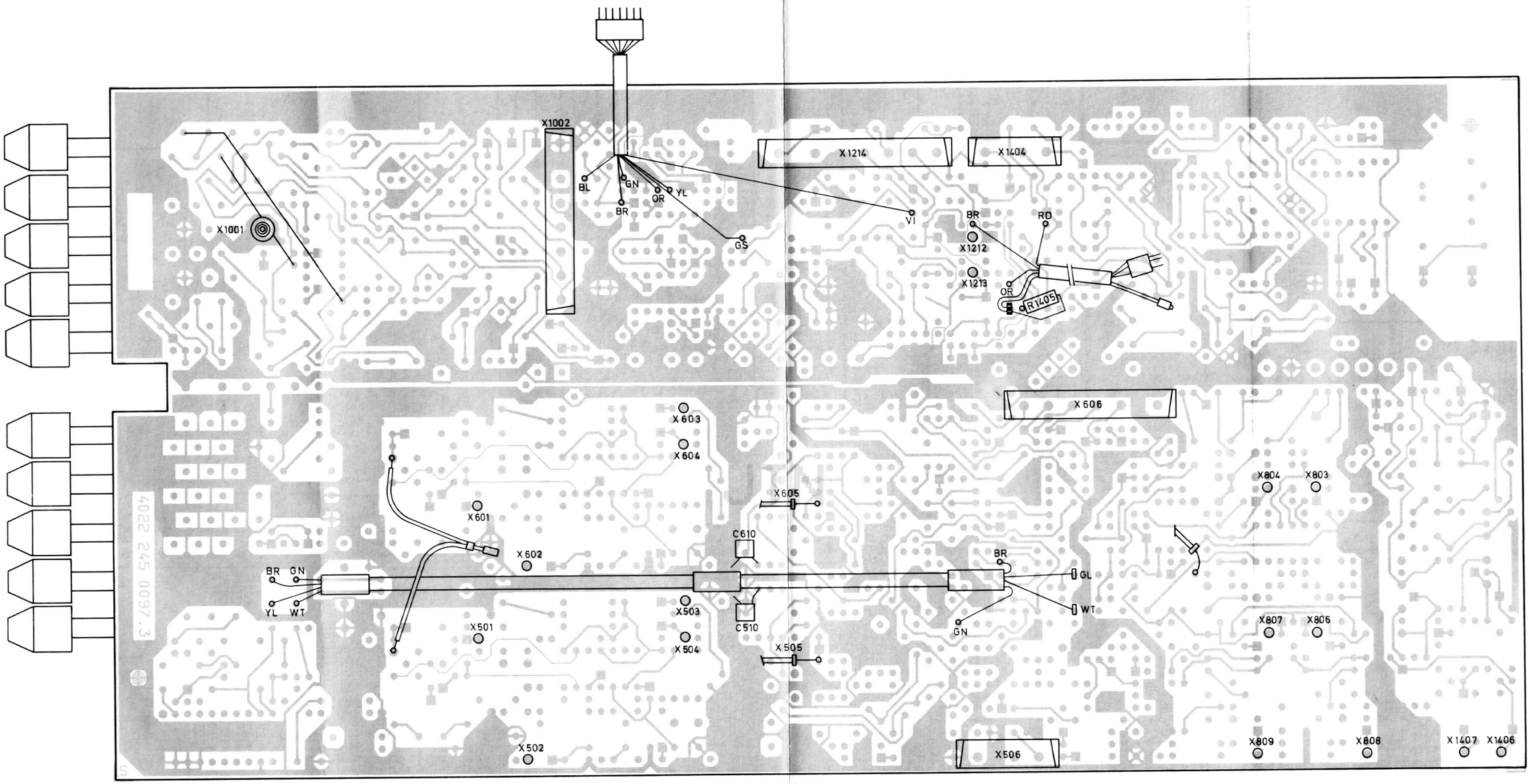


Fig. 10.13. Amplifier unit (A5) without components and rear side tracks

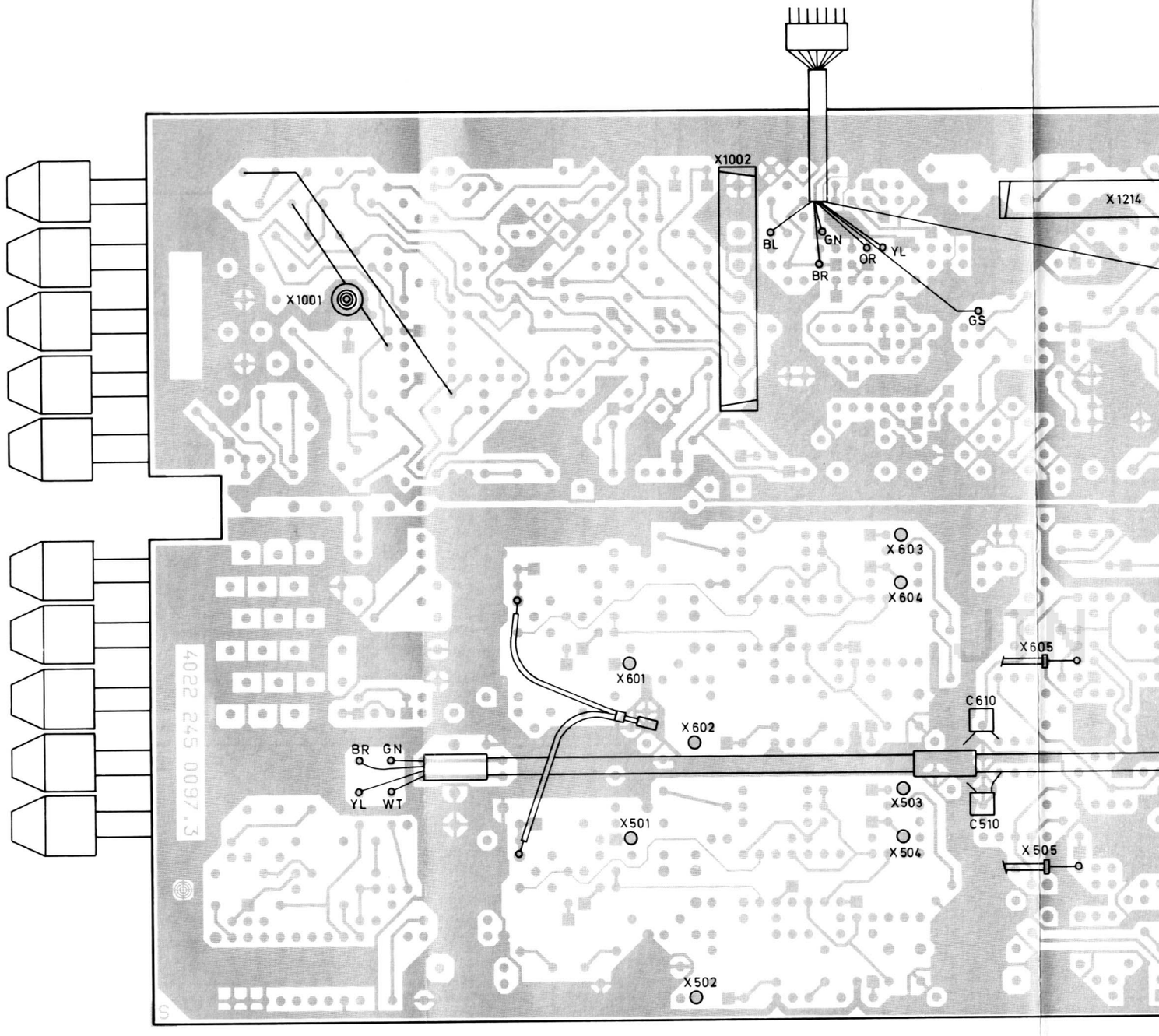

X1002
X1214
X1001
BL
GN
OR
YL
BR
GS
X603
X604
X605
X601
C610
X602
BR GN
YL WT
X503
C510
X501
X504
X505
X502
4022 245 0097.3

Fig.

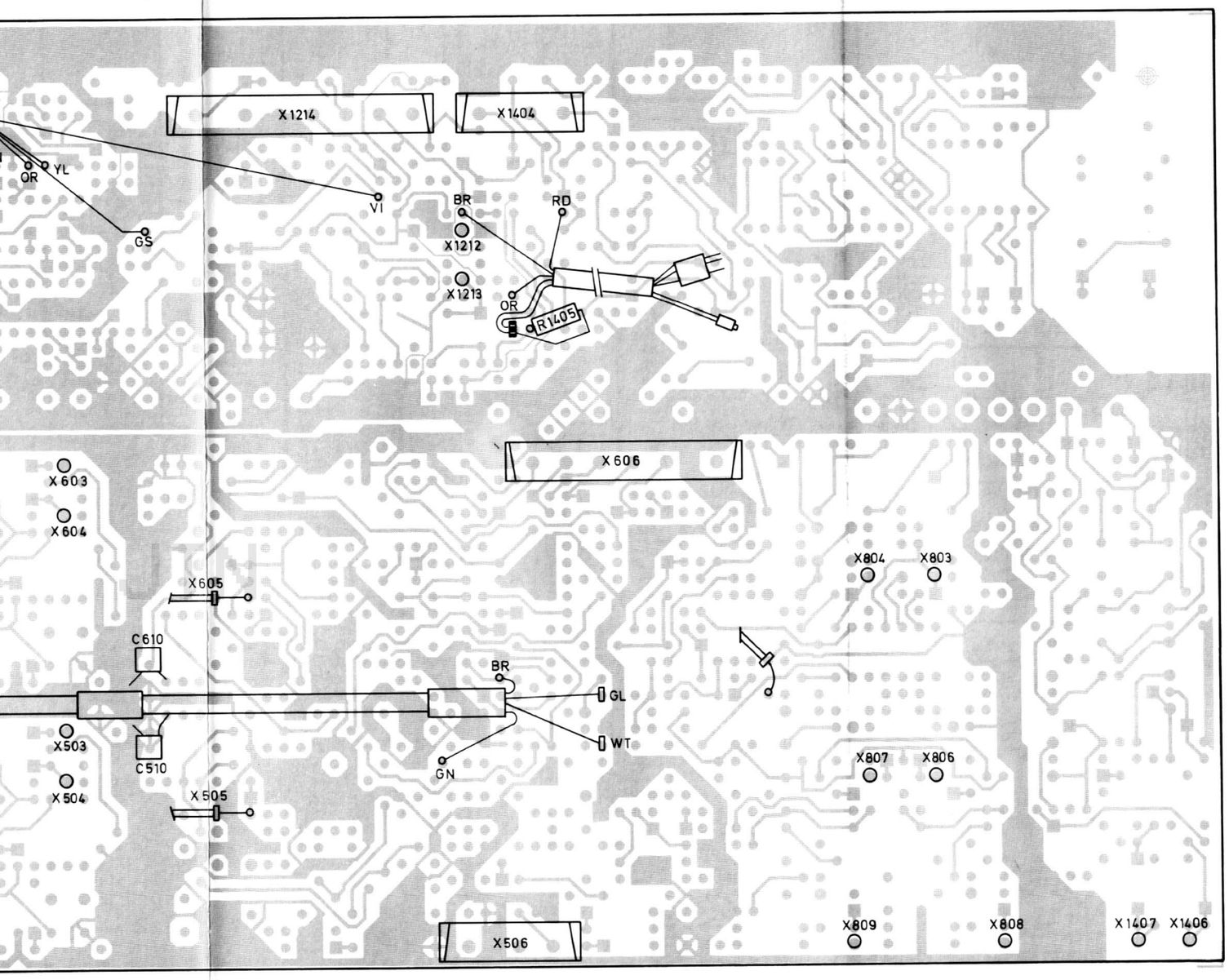


Fig. 10.13. Amplifier unit (A5) without components and rear side tracks

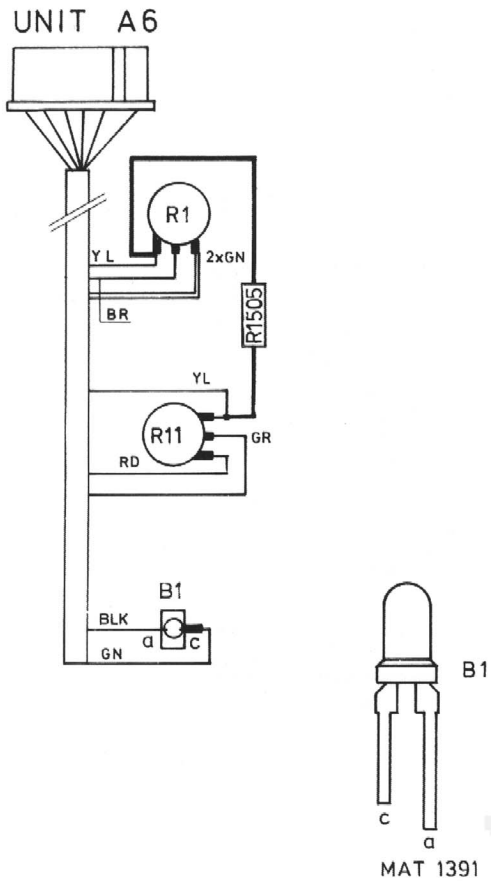


Fig. 10.14. Intens unit (A6)

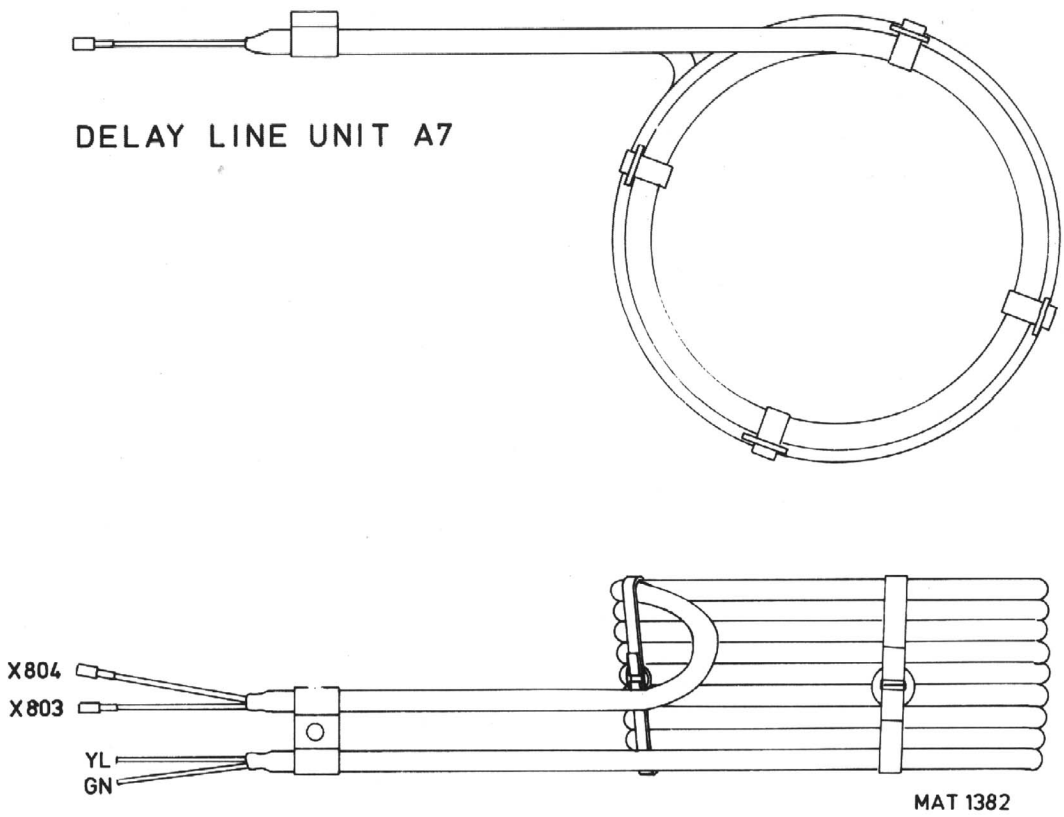


Fig. 10.15. Delay line unit (A7)

5V DC UNIT A8

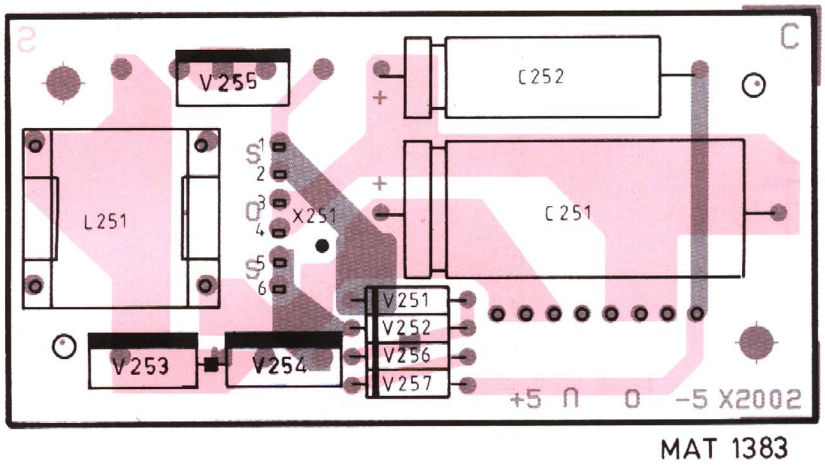


Fig. 10.16. 5V DC unit (A8)

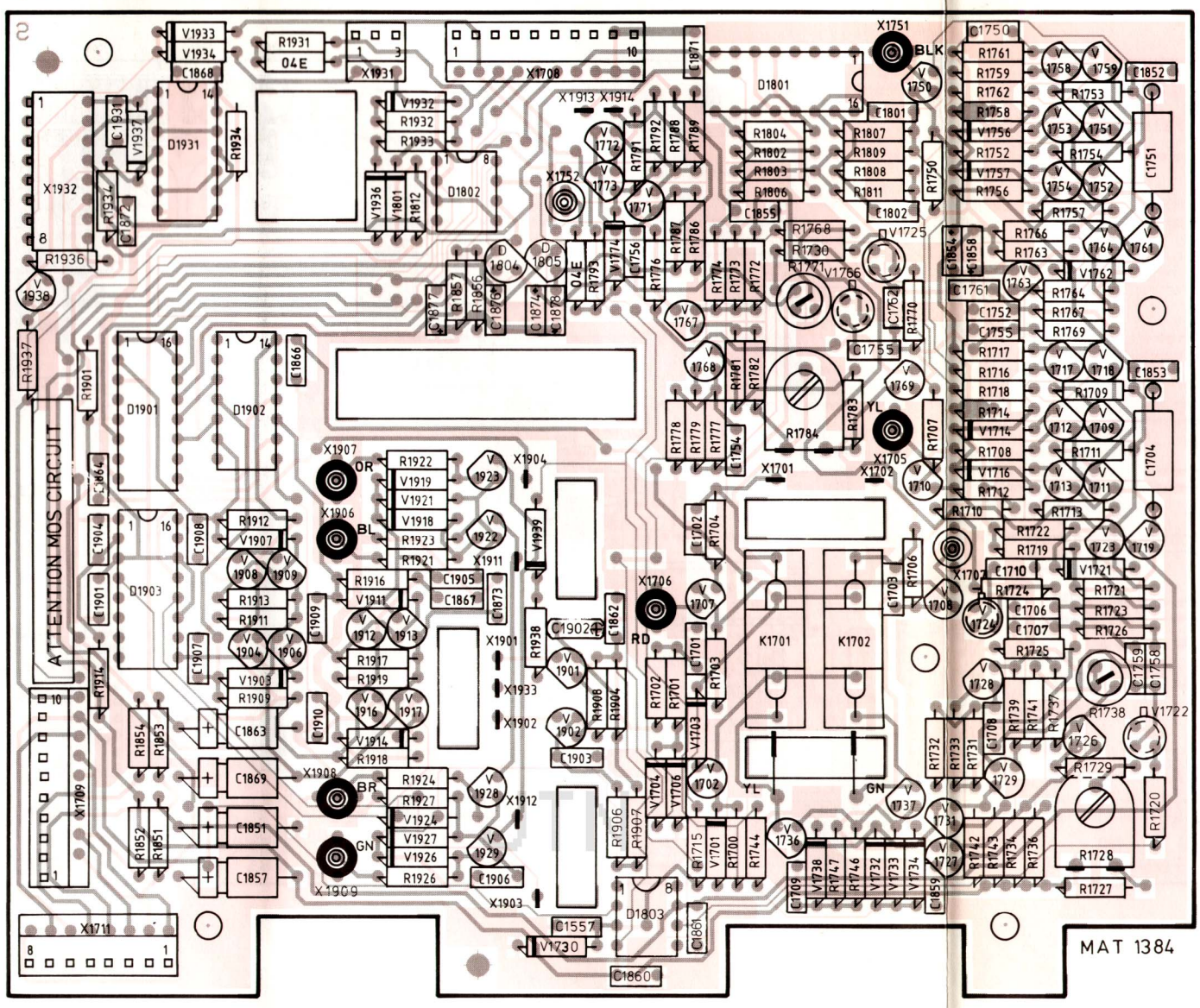


Fig. 10.17.
Adaption unit (A9)

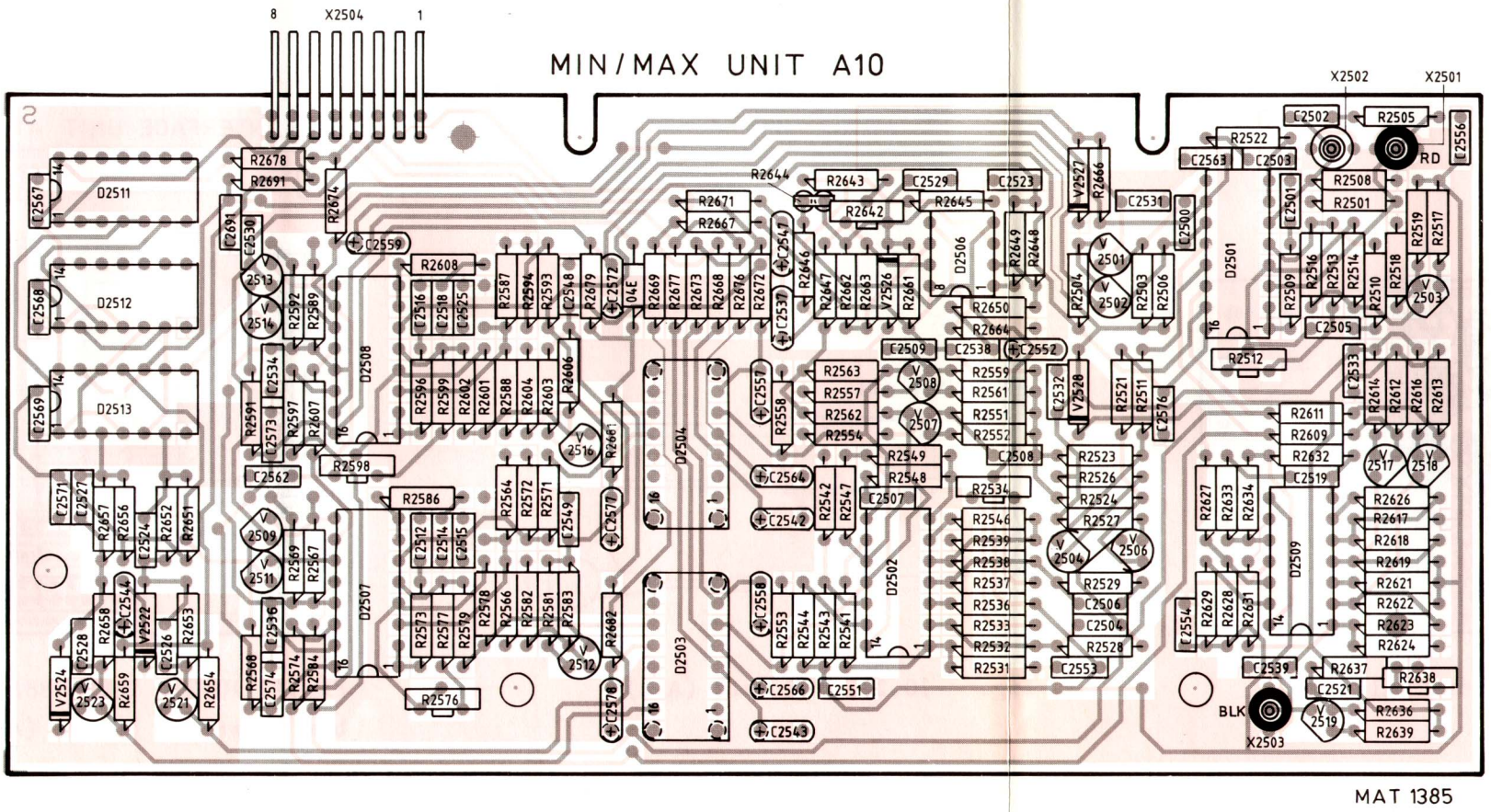


Fig. 10.18.
Min/max unit (A10)

LOGIC UNIT A11

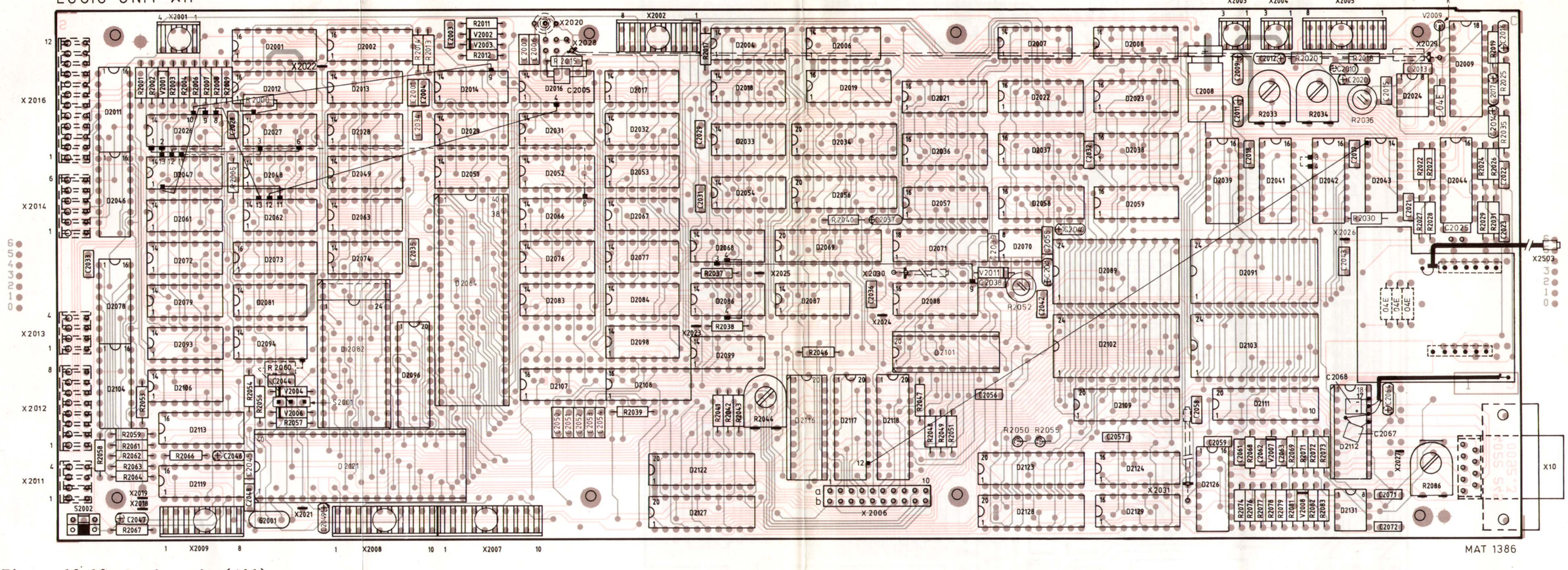


Fig. 10.19. Logic unit (A11)
This unit is a so-called multilayer (5 layers).
Only the visible print tracks are shown!

T&H UNIT A1103

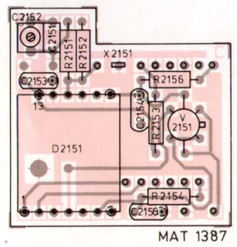


Fig. 10.20.
T&H +unit (A1103)

AUXILIARY CHANNEL UNIT A12

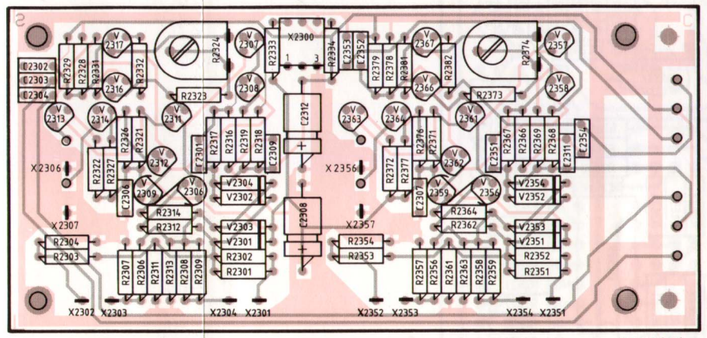


Fig. 10.21. Auxiliary channel unit (A12)

EHT UNIT A13

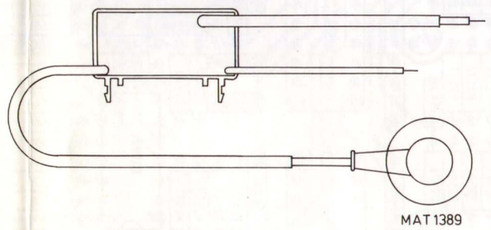


Fig. 10.22. EHT unit (A13)

IEEE INTERFACE UNIT A14

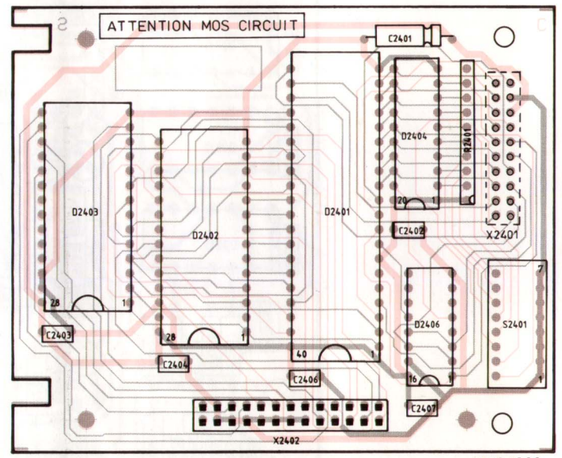


Fig. 10.23. IEEE-488/IEC-625
bus interface option (A14)

LOGIC UNIT A11

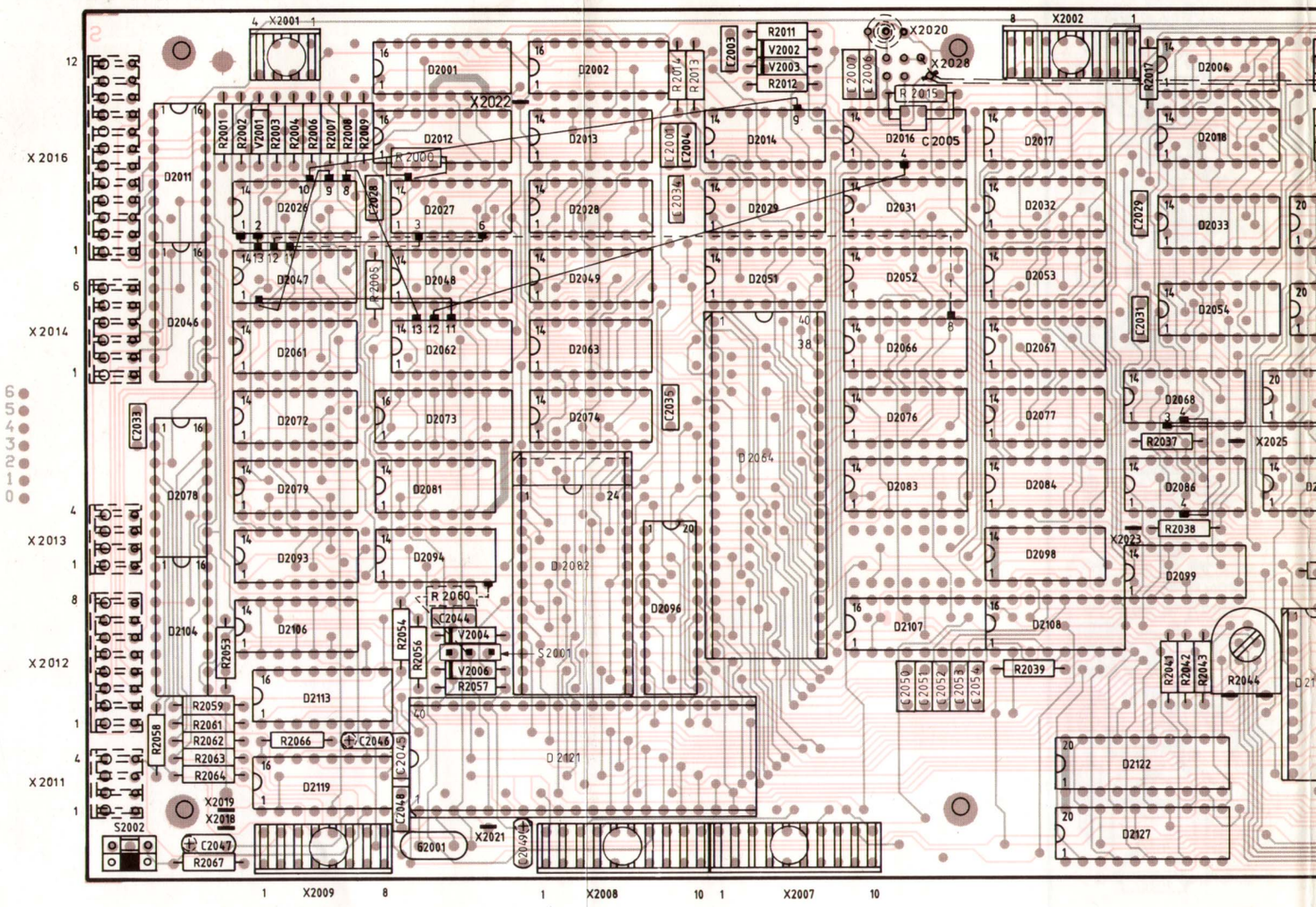
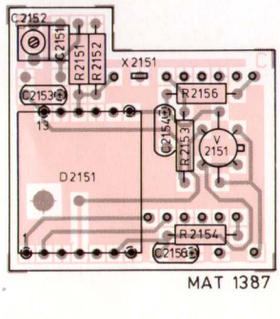


Fig. 10.19. Logic unit (A11)
This unit is a so-called multilayer (5 layers).
Only the visible print tracks are shown!

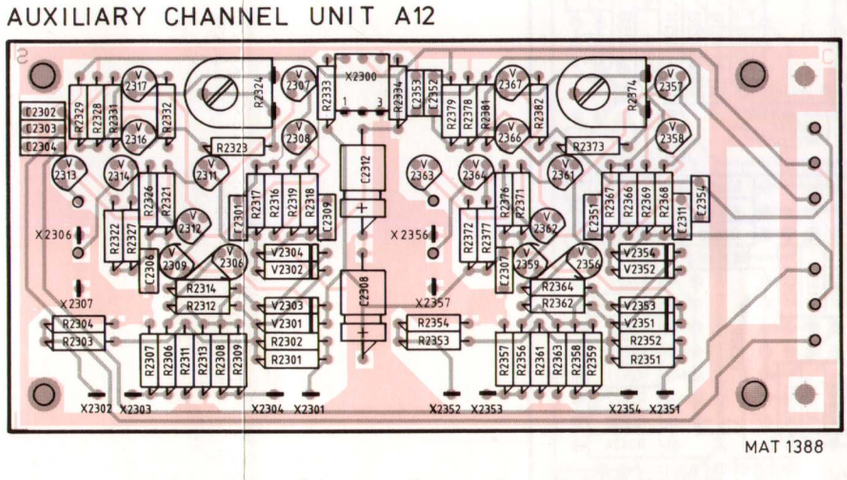
T&H UNIT A1103



MAT 1387

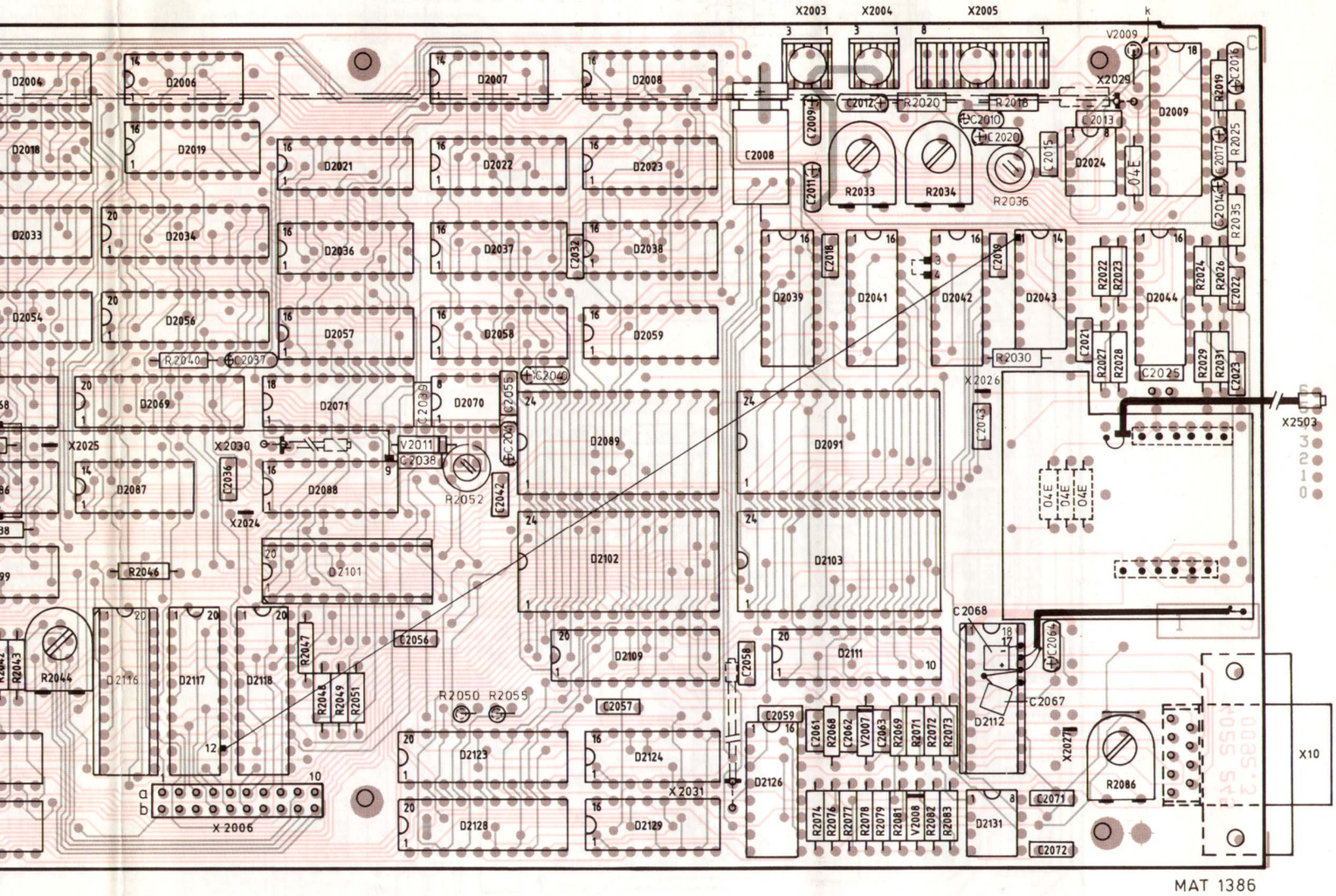
Fig. 10.20.
T&H +unit (A1103)

AUXILIARY CHANNEL UNIT A12

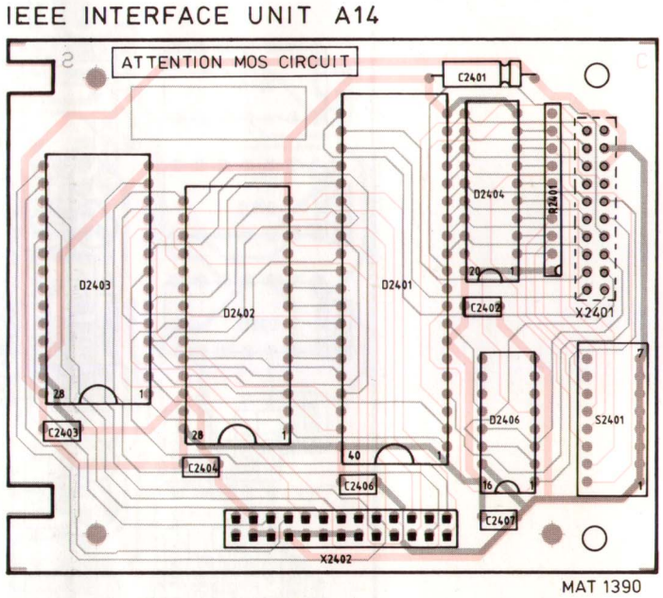


MAT 1388

Fig. 10.21. Auxiliary channel unit (A12)



IEEE INTERFACE UNIT A14



EHT UNIT A13

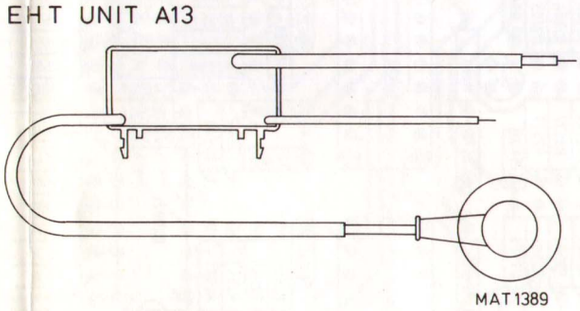


Fig. 10.22. EHT unit (A13)

Fig. 10.23. IEEE-488/IEC-625 bus interface option (A14)

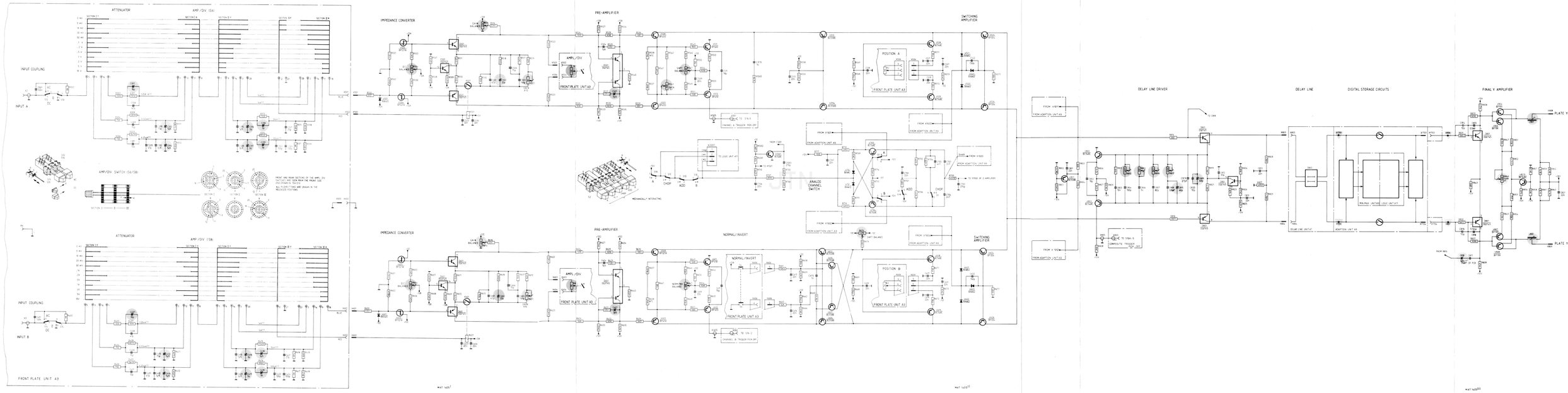
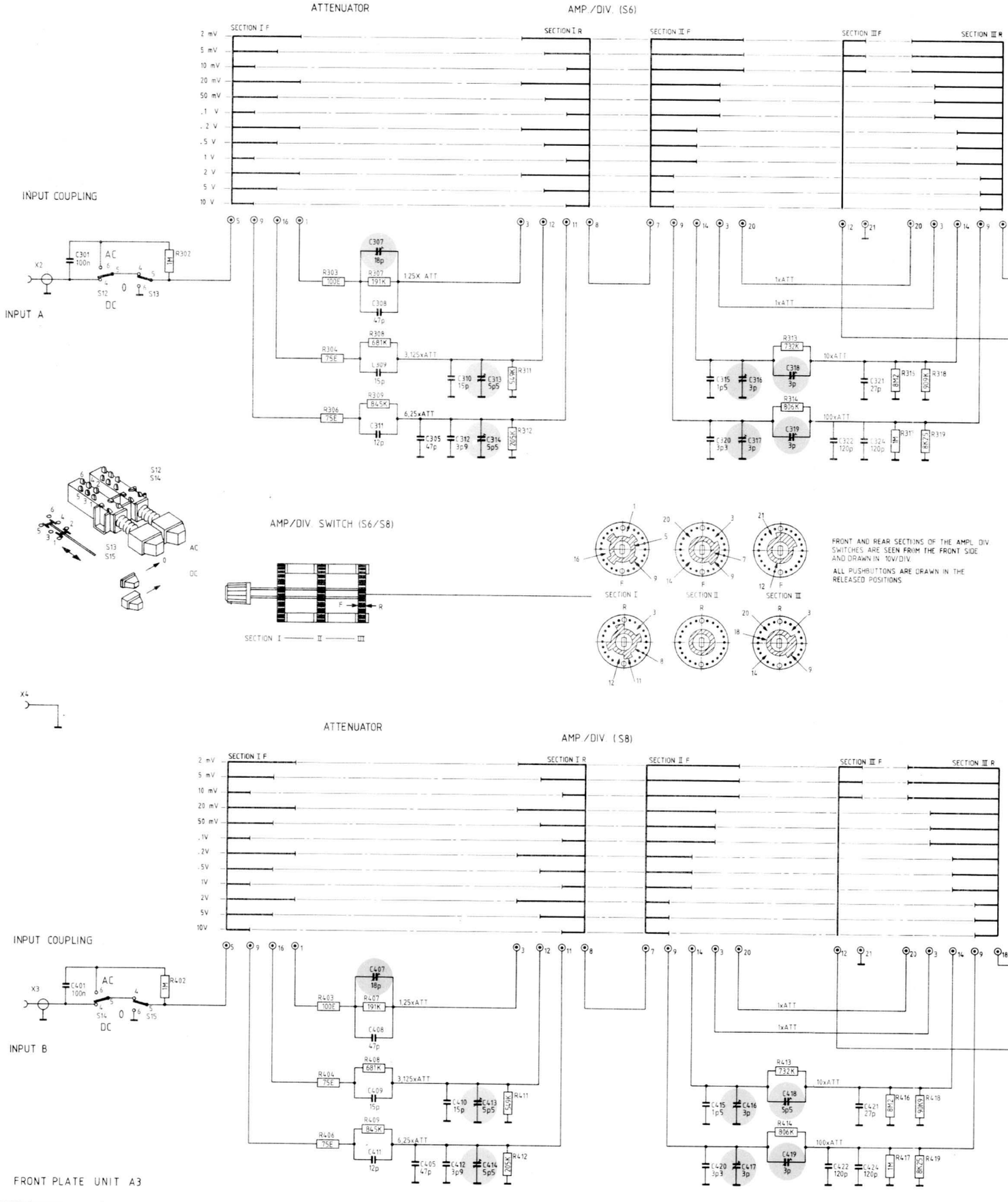
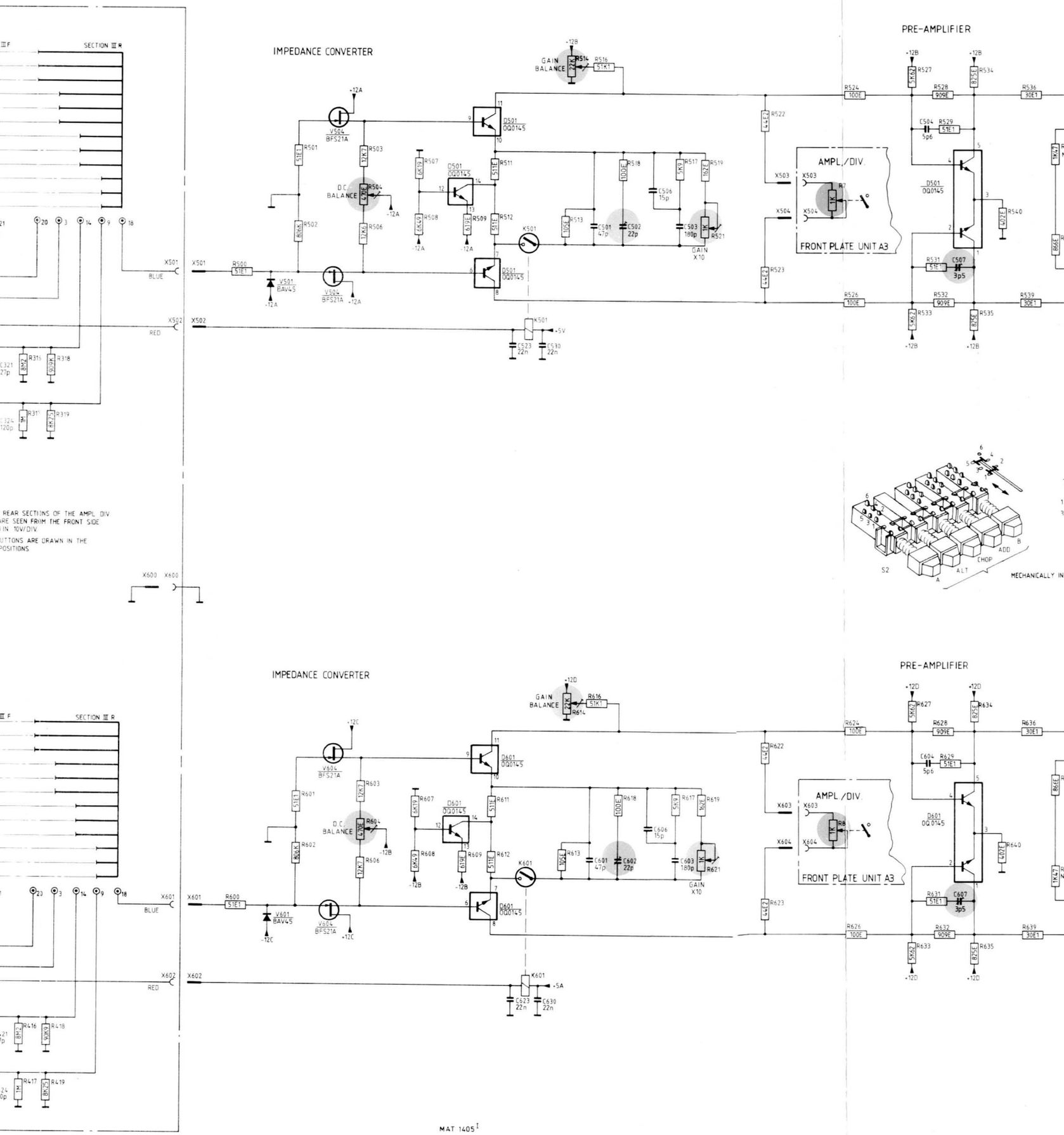
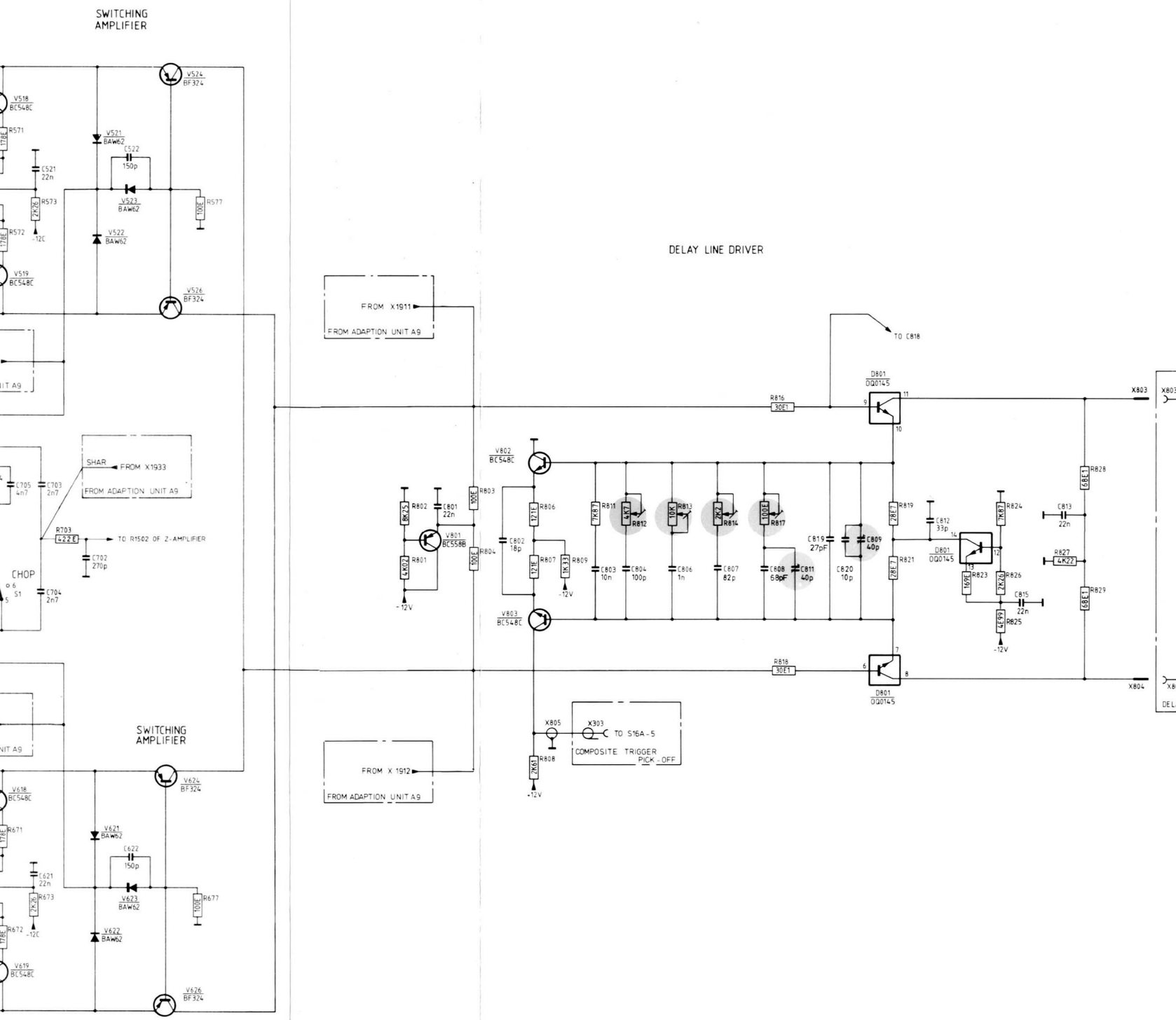


Fig. 10.24. DIAGRAM 1 Vertical channels (A5)


ATTENUATOR
AMP./DIV. (S6)
SECTION I F
SECTION I R
SECTION II F
SECTION III F
SECTION III R
2 mV
5 mV
10 mV
20 mV
50 mV
.1 V
.2 V
.5 V
1 V
2 V
5 V
10 V
INPUT COUPLING
INPUT A
X2
C301 100n
AC
R302 1M
S12
S13
DC
R303 100E
C307 18p
R307 191K
1,25X ATT
C308 47p
R304 75E
R308 681K
3,125xATT
C309 15p
C310 15p
C313 5p5
R311 5,49K
R306 75E
R309 845K
6,25xATT
C311 12p
C305 47p
C312 3p9
C314 5p5
R312 205K
1xATT
1xATT
R313 732K
10xATT
C315 1p5
C316 3p
C318 3p
C321 27p
R315 8M2
R318 909K
R314 806K
100xATT
C320 3p3
C317 3p
C319 3p
C322 120p
C324 120p
R317 1M
R319 8K25
S12 S14
S13 S15
AC
DC
AMP/DIV. SWITCH (S6/S8)
SECTION I — II — III
F
R
SECTION I
SECTION II
SECTION III
FRONT AND REAR SECTIONS OF THE AMPL. DIV SWITCHES ARE SEEN FROM THE FRONT SIDE AND DRAWN IN 10V/DIV.
ALL PUSHBUTTONS ARE DRAWN IN THE RELEASED POSITIONS
X4
ATTENUATOR
AMP./DIV. (S8)
SECTION I F
SECTION I R
SECTION II F
SECTION III F
SECTION III R
2 mV
5 mV
10 mV
20 mV
50 mV
.1V
.2V
.5V
1V
2V
5V
10V
INPUT COUPLING
INPUT B
X3
C401 100n
AC
R402 1M
S14
S15
DC
R403 100E
C407 18p
R407 191K
1,25xATT
C408 47p
R404 75E
R408 681K
3,125xATT
C409 15p
C410 15p
C413 5p5
R411 5,49K
R406 75E
R409 845K
6,25xATT
C411 12p
C405 47p
C412 3p9
C414 5p5
R412 205K
1xATT
1xATT
R413 732K
10xATT
C415 1p5
C416 3p
C418 5p5
C421 27p
R416 8M2
R418 909K
R414 806K
100xATT
C420 3p3
C417 3p
C419 3p
C422 120p
C424 120p
R417 1M
R419 8K25
FRONT PLATE UNIT A3


IMPEDANCE CONVERTER
PRE-AMPLIFIER
SECTION III F
SECTION III R
GAIN BALANCE
D.C. BALANCE
AMPL./DIV.
FRONT PLATE UNIT A3
GAIN X10
X501
X502
X503
X504
X600
X601
X602
BLUE
RED
REAR SECTIONS OF THE AMPL. DIV.
ARE SEEN FROM THE FRONT SIDE
IN 10V/DIV.
BUTTONS ARE DRAWN IN THE
POSITIONS.
MECHANICALLY IN
S2
ALT
CHOP
ADD
A
B

SWITCH
AMPLIF
POSITION A
FRONT PLATE UNIT A3
CHANNEL A TRIGGER PICK-OFF
TO S16-5
FROM X1903
FROM ADAPTION UNIT A9
FROM X1901
FROM ADAPTION UNIT A9
TO LOGIC UNIT A11
CHOP
ADD
MECHANICALLY INTERACTING
ANALOG
CHANNEL
SWITCH
FROM X1902
FROM ADAPTION UNIT A9
SHIFT BALANCE
FROM X1904
FROM ADAPTION UNIT A9
NORMAL/INVERT
POSITION B
FRONT PLATE UNIT A3
CHANNEL B TRIGGER PICK-OFF
TO S16-2
MAT 1405 II


SWITCHING AMPLIFIER
DELAY LINE DRIVER
FROM X1911
FROM ADAPTION UNIT A9
TO C818
SHAR
FROM X1933
FROM ADAPTION UNIT A9
TO R1502 OF Z-AMPLIFIER
CHOP
SWITCHING AMPLIFIER
FROM X 1912
FROM ADAPTION UNIT A9
TO S16A-5
COMPOSITE TRIGGER PICK-OFF
X803
X804
X805
X303
-12V

MAT 1405 II

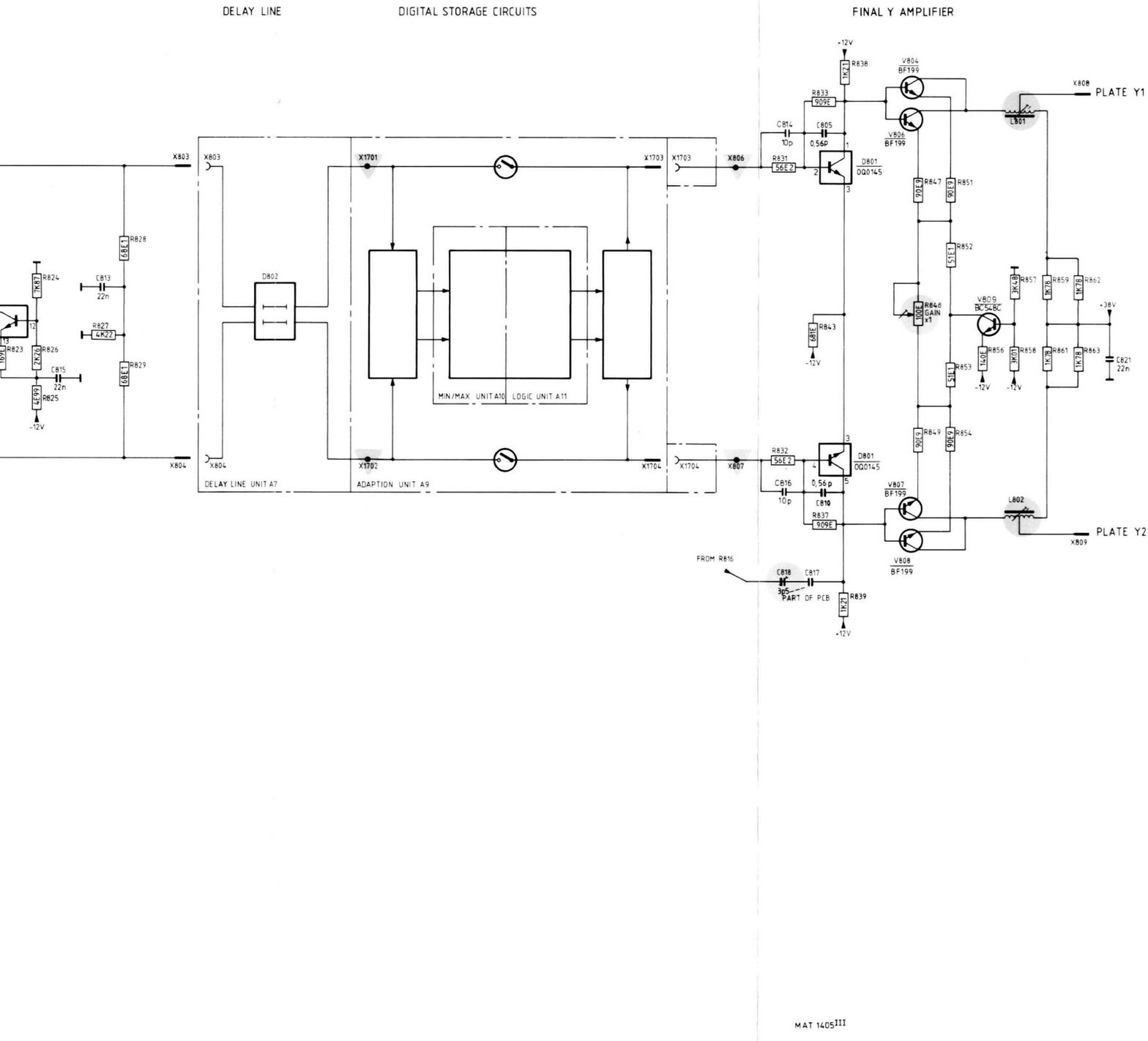


Fig. 10.24. DIAGRAM 1 Vertical channels (A5)

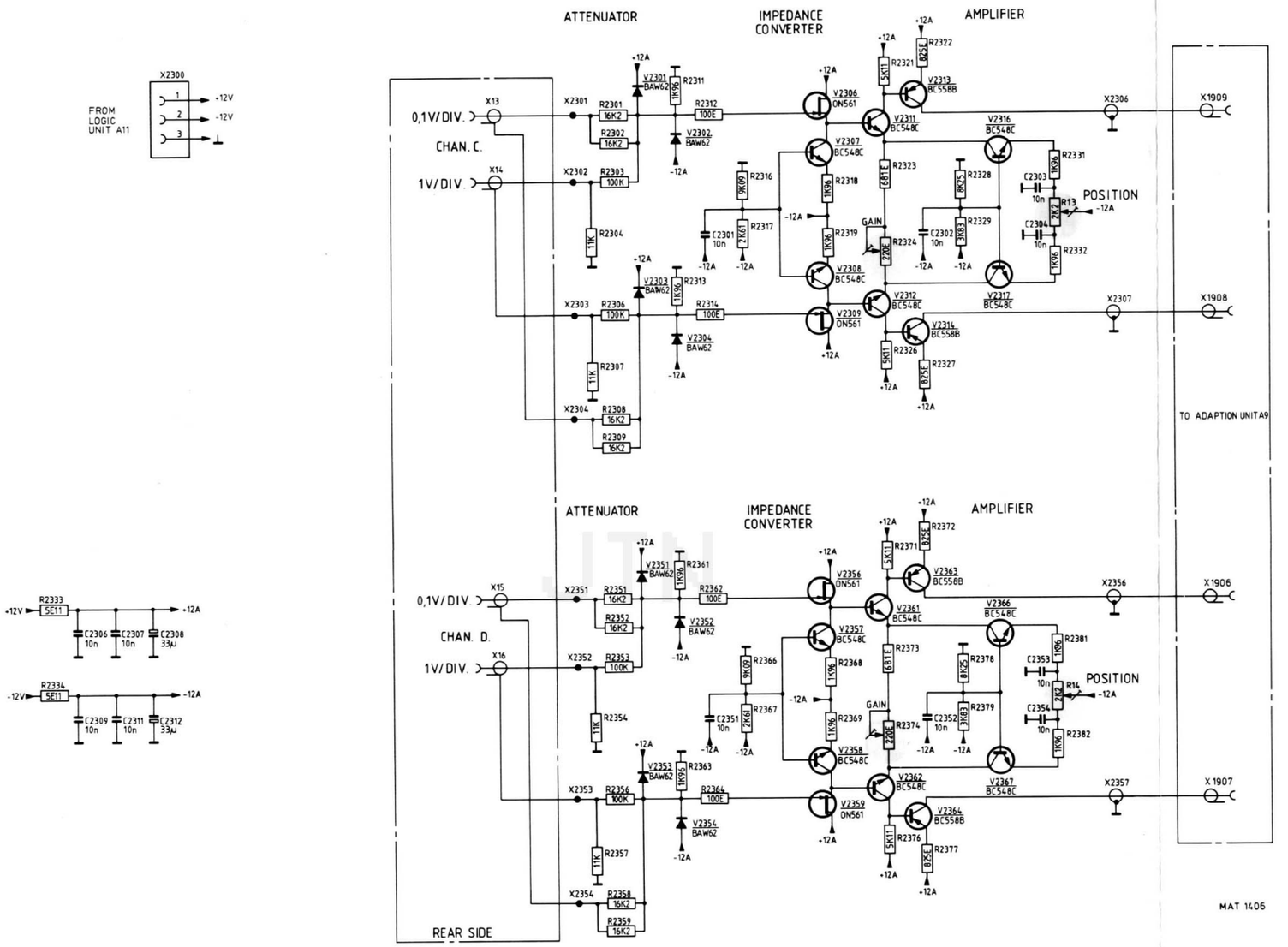
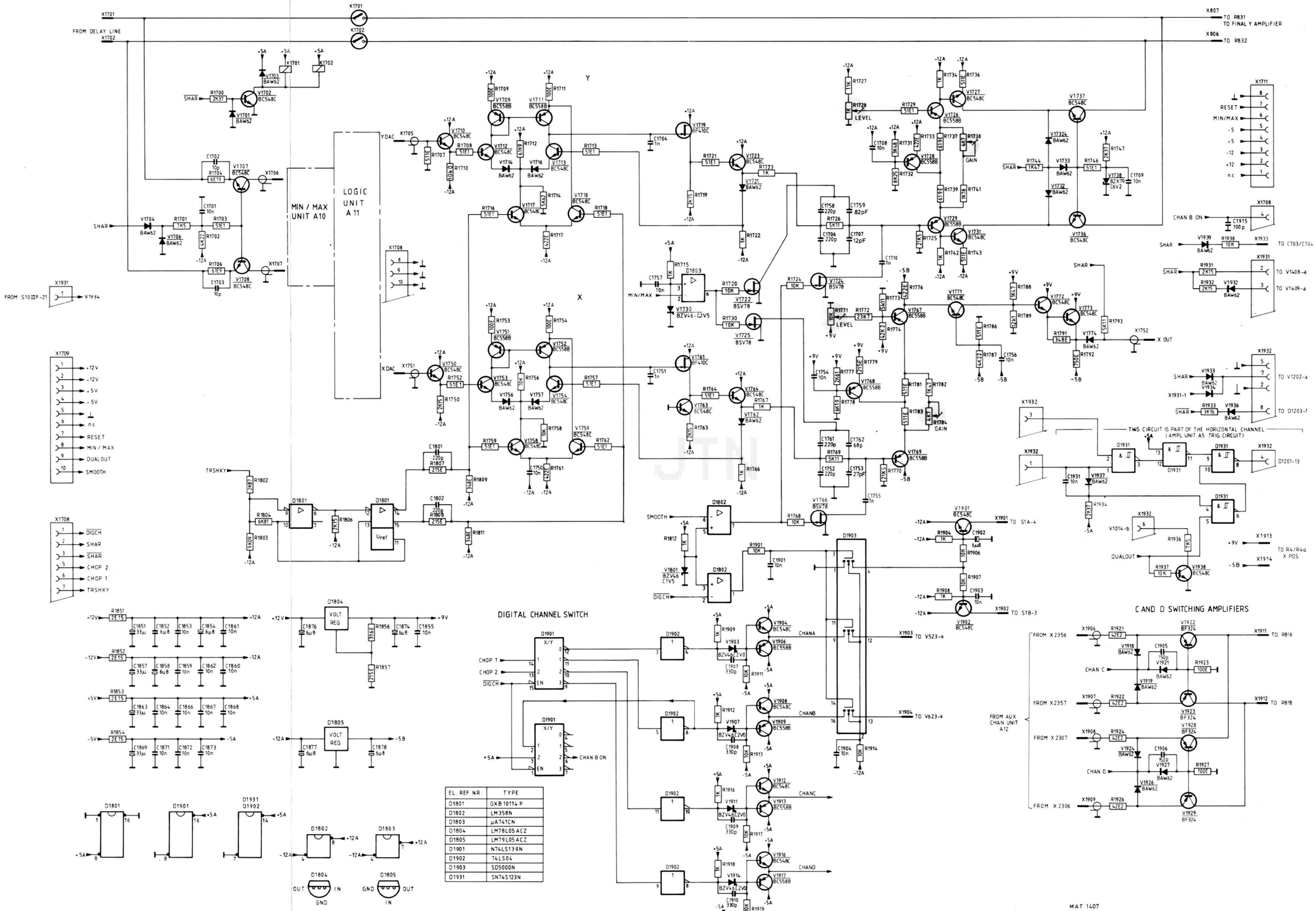
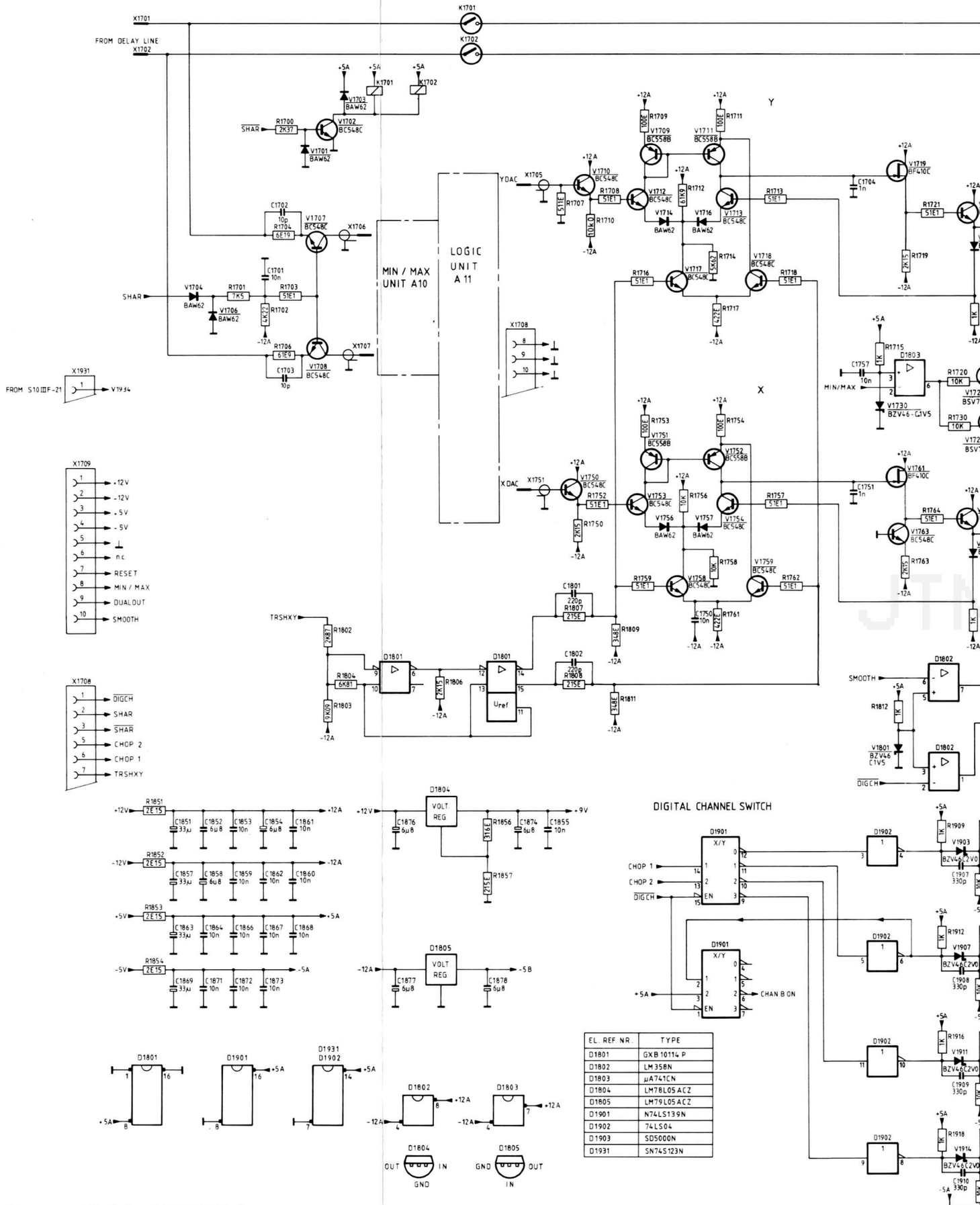


Fig. 10.25. DIAGRAM 2 Channels C and D (A12)



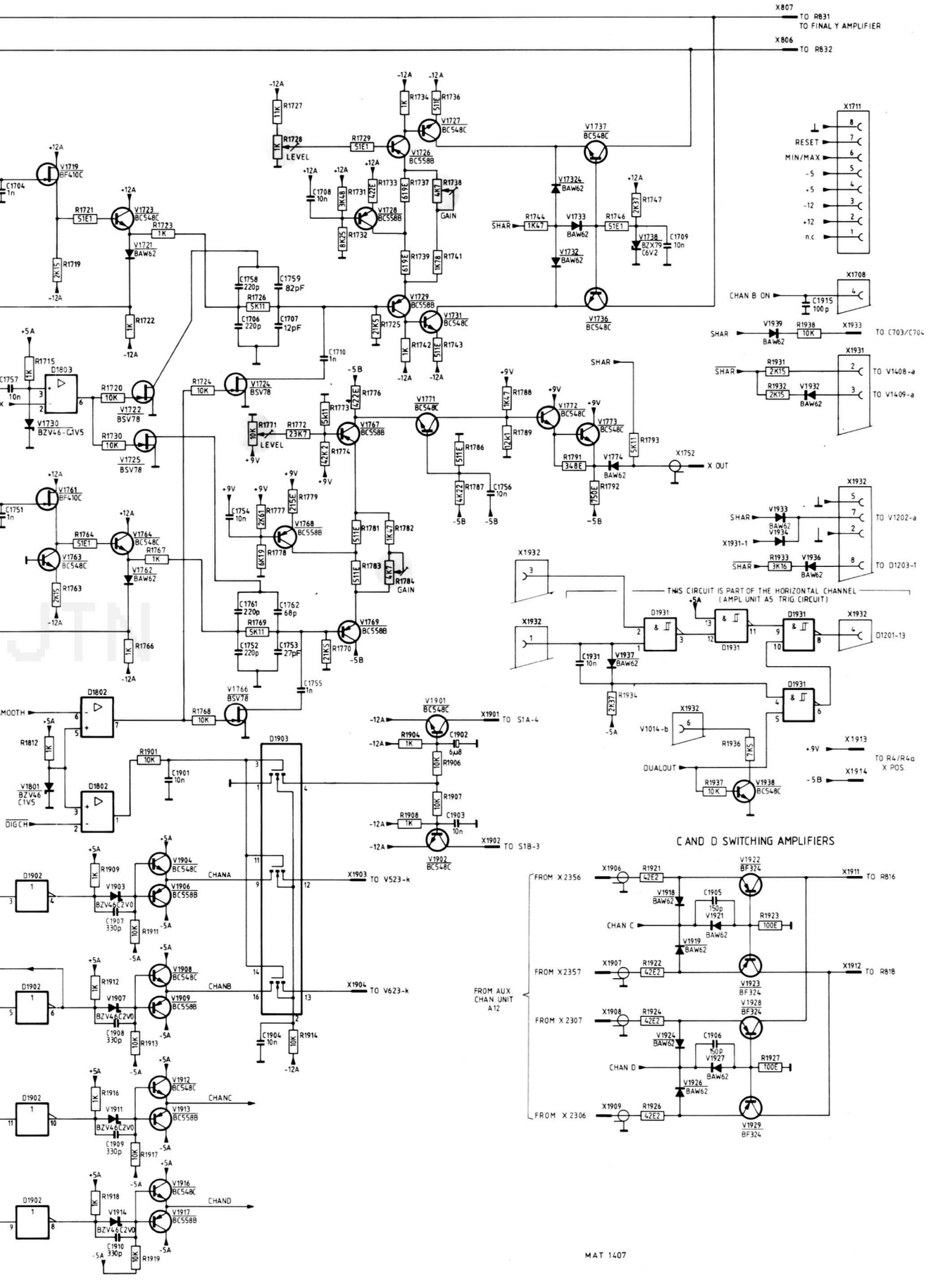
EL. REF. NR.	TYPE
D1801	GXB10114 P
D1802	LM358N
D1803	µA741CN
D1804	LM78L05ACZ
D1805	LM79L05ACZ
D1901	N74LS139N
D1902	74LS04
D1903	SD5000N
D1931	SN74S123N

Fig. 10.26. DIAGRAM 3
Digital channel switch (A9)



EL. REF. NR.	TYPE
D1801	GXB 10114 P
D1802	LM 358N
D1803	µA741CN
D1804	LM78L05 ACZ
D1805	LM79L05 ACZ
D1901	N74LS139N
D1902	74LS04
D1903	SD5000N
D1931	SN74S123N

Fig. 10.26. DIAGRAM 3
Digital channel switch (A9)


X807
TO R831
TO FINAL Y AMPLIFIER
X806
TO R832
X1711
RESET
MIN/MAX
-5
+5
-12
+12
n.c.
X1708
CHAN B ON
C1915 100p
X1933
TO C703/C704
X1931
TO V1408-a
TO V1409-a
X1752
X OUT
X1932
TO V1202-a
TO D1203-1
THIS CIRCUIT IS PART OF THE HORIZONTAL CHANNEL (AMPL UNIT AS TRIG CIRCUIT)
D1201-13
X1913
TO R4/R4a X POS.
X1914
-5B
LEVEL
GAIN
SHAR
DUALOUT
DIGCH
SMOOTH
CHANA
CHANB
CHANC
CHAND
X1903
TO V523-k
X1904
TO V623-k
X1901
TO S1A-4
X1902
TO S1B-3
C AND D SWITCHING AMPLIFIERS
FROM X2356
FROM X2357
FROM X2307
FROM X2306
FROM AUX. CHAN. UNIT A12
CHAN C
CHAN D
X1911
TO R816
X1912
TO R818
MAT 1407

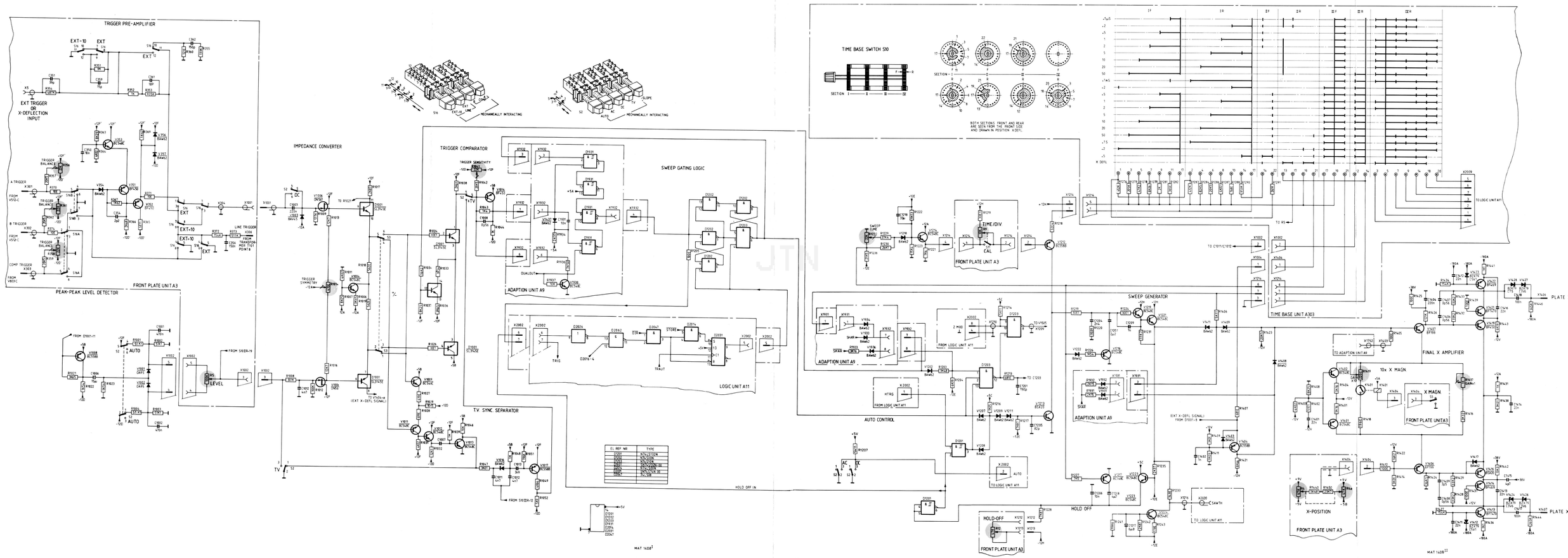
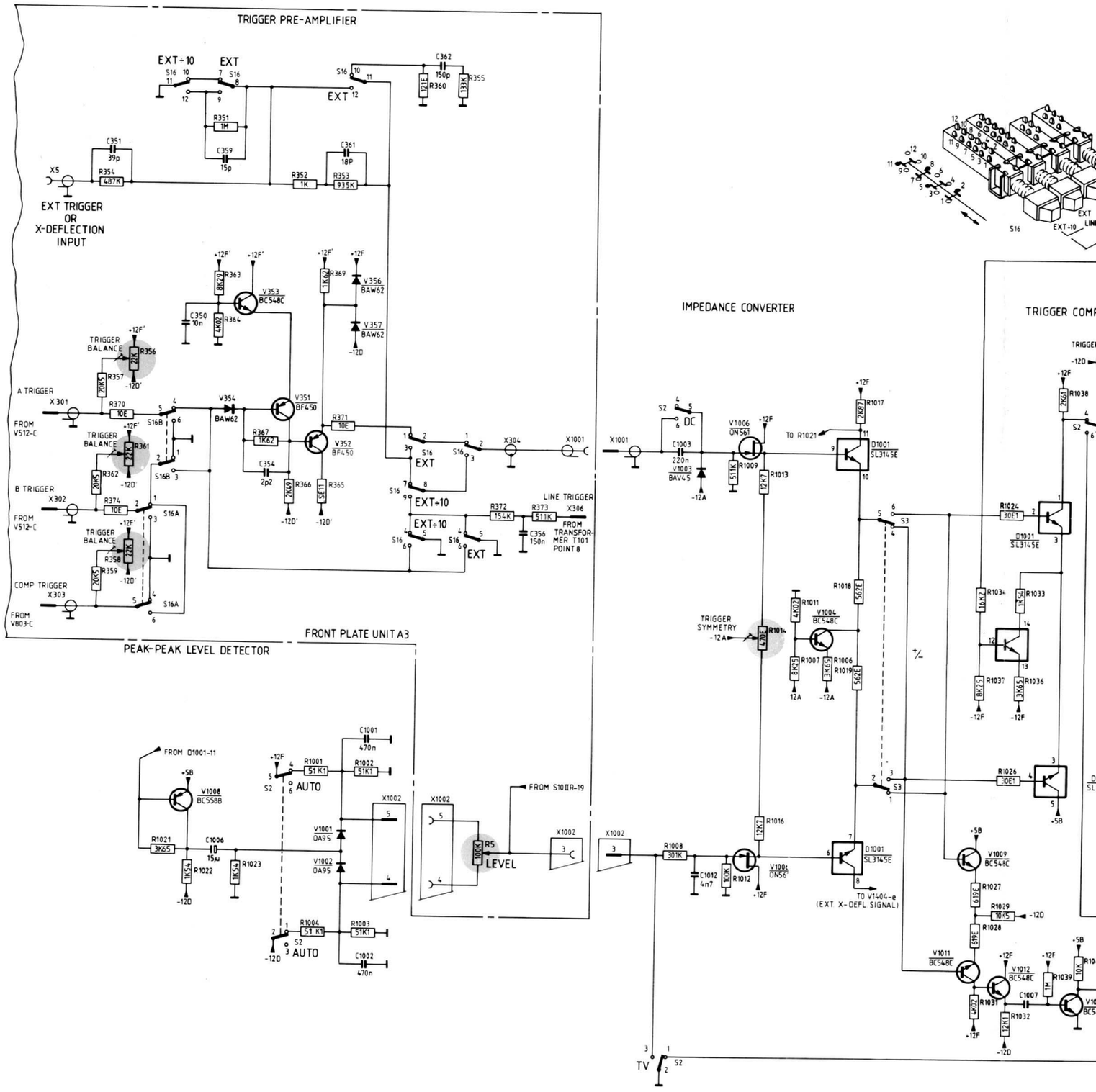
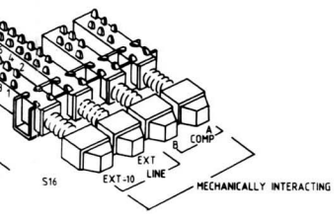
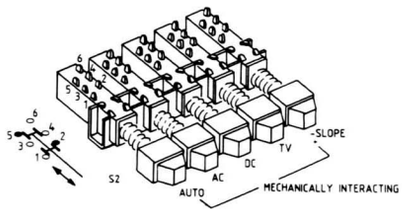


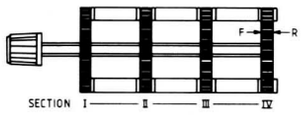
Fig. 10.27. DIAGRAM 4+5 Horizontal channels (A5)


TRIGGER PRE-AMPLIFIER
EXT-10
EXT
EXT TRIGGER OR X-DEFLECTION INPUT
X5
C351 39p
R354 487K
R351 1M
C359 15p
C361 18P
R352 1K
R353 935K
C362 150p
R360 12K1
R355 133K
A TRIGGER
B TRIGGER
COMP TRIGGER
FROM V512-C
FROM V803-C
X301
X302
X303
TRIGGER BALANCE
R356 2K
R357 20K5
R358 2K
R359 20K5
R361 2K
R362 20K5
R370 10E
R374 10E
S16A
S16B
V354 BAW62
V351 BF450
V352 BF450
R367 1K62
C354 2p2
R371 10E
R372 154K
R373 511K
X306
FROM TRANSFORMER T101 POINT 8
LINE TRIGGER
C356 150n
X304
X1001
R363 4K99
V353 BC548C
C350 10n
R364 4K02
R369 1K62
V356 BAW62
V357 BAW62
R365 5E11
R366 2K49
IMPEDANCE CONVERTER
DC
C1003 220n
V1003 BAV45
V1006 ON561
R1009 511K
R1013 12K7
R1017 2K87
TO R1021
D1001 SL3145E
TRIGGER SYMMETRY
R1014 430E
R1011 4K02
V1004 BC548C
R1007 8K25
R1006 3K65
R1019 562E
R1018 562E
R1024 30E1
R1026 30E1
R1034 16K2
R1033 1K54
R1037 8K25
R1036 3K65
R1016 12K7
R1008 301K
C1012 4n7
R1012 100K
V1005 ON561
TO V1404-8 (EXT X-DEFL SIGNAL)
V1009 BC548C
R1027 619E
R1029 10K5
R1028 619E
V1011 BC548C
V1012 BC548C
R1039 1M
R1031 4K02
C1007
R1032 12K1
TV
S2
S3
FRONT PLATE UNIT A3
PEAK-PEAK LEVEL DETECTOR
FROM D1001-11
V1008 BC558B
R1021 3K65
C1006 15µ
R1022 1K54
R1023 1K54
C1001 470n
R1001 51K1
R1002 51K1
AUTO
V1001 OA95
V1002 OA95
R1004 51K1
R1003 51K1
C1002 470n
X1002
FROM S10IIR-19
R5 100K
LEVEL
EXT-10
EXT
LINE





TIME BASE SWITCH S10



TRIGGER COMPARATOR

TRIGGER SENSITIVITY R1041 22K

SWEEP GATING LOGIC

ADAPTION UNIT A9

LOGIC UNIT A11

T.V. SYNC. SEPARATOR

AUTO CONTROL

EL REF NR	TYPE
D1201	N74LS132N
D1202	N74S00N
D1203	N74S10N
D1931	SN74S132N-00
D2014	N74S00N
D2031	SN74S74N 00
D2047	74LS08

HOLD OFF IN

MAT 1408I

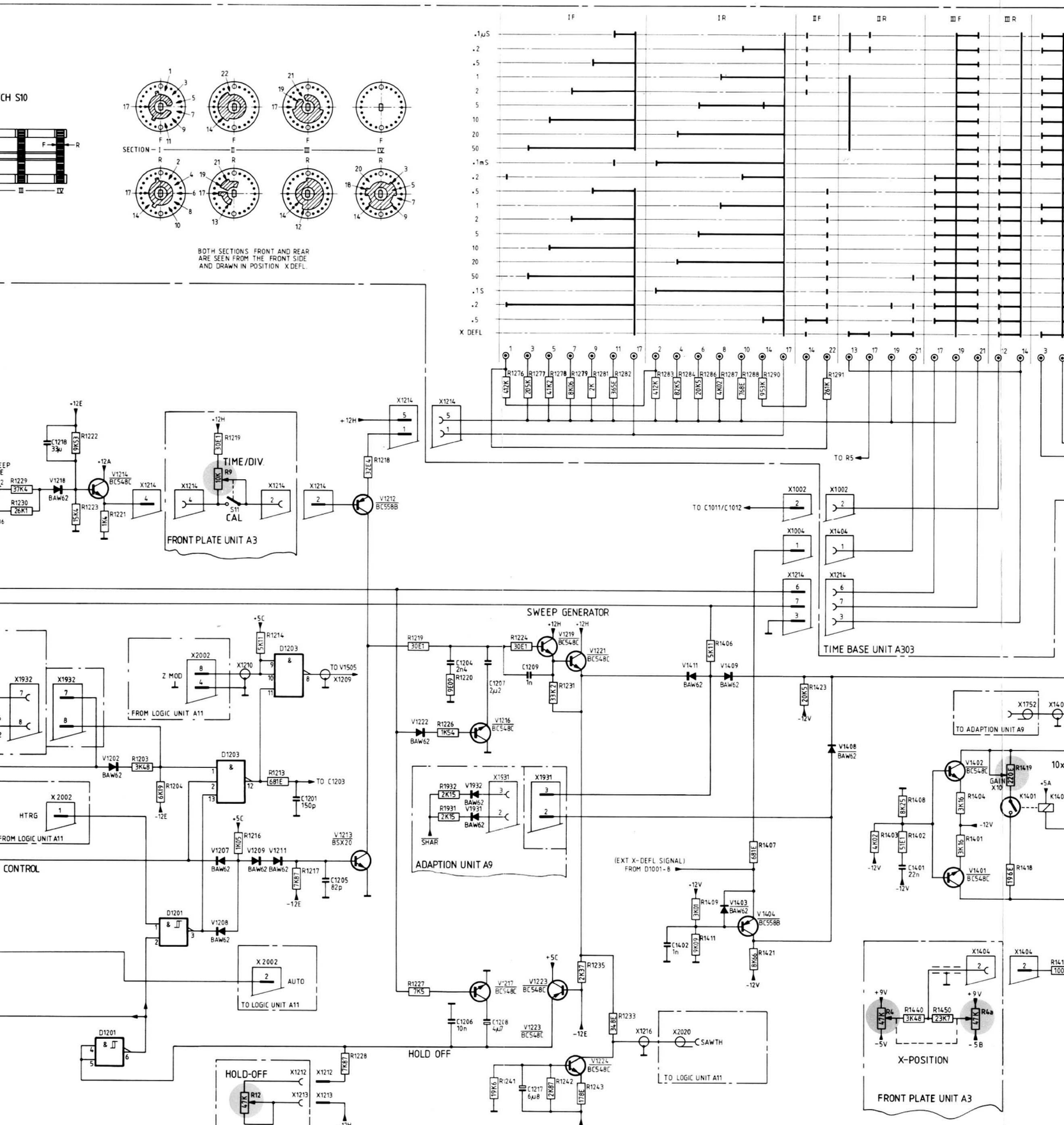

SECTION – I – II – III – IV
BOTH SECTIONS FRONT AND REAR ARE SEEN FROM THE FRONT SIDE AND DRAWN IN POSITION X DEFL.
I F
I R
II F
II R
III F
III R
X DEFL
TIME/DIV.
CAL
FRONT PLATE UNIT A3
TO R5
TO C1011/C1012
TIME BASE UNIT A303
SWEEP GENERATOR
FROM LOGIC UNIT A11
Z MOD
TO V1505
TO C1203
HTRG
CONTROL
ADAPTION UNIT A9
SHAR
(EXT X-DEFL SIGNAL) FROM D1001-8
TO ADAPTION UNIT A9
AUTO
TO LOGIC UNIT A11
HOLD OFF
HOLD-OFF
SAWTH
X-POSITION
FRONT PLATE UNIT A3

Fig. 10.27. I

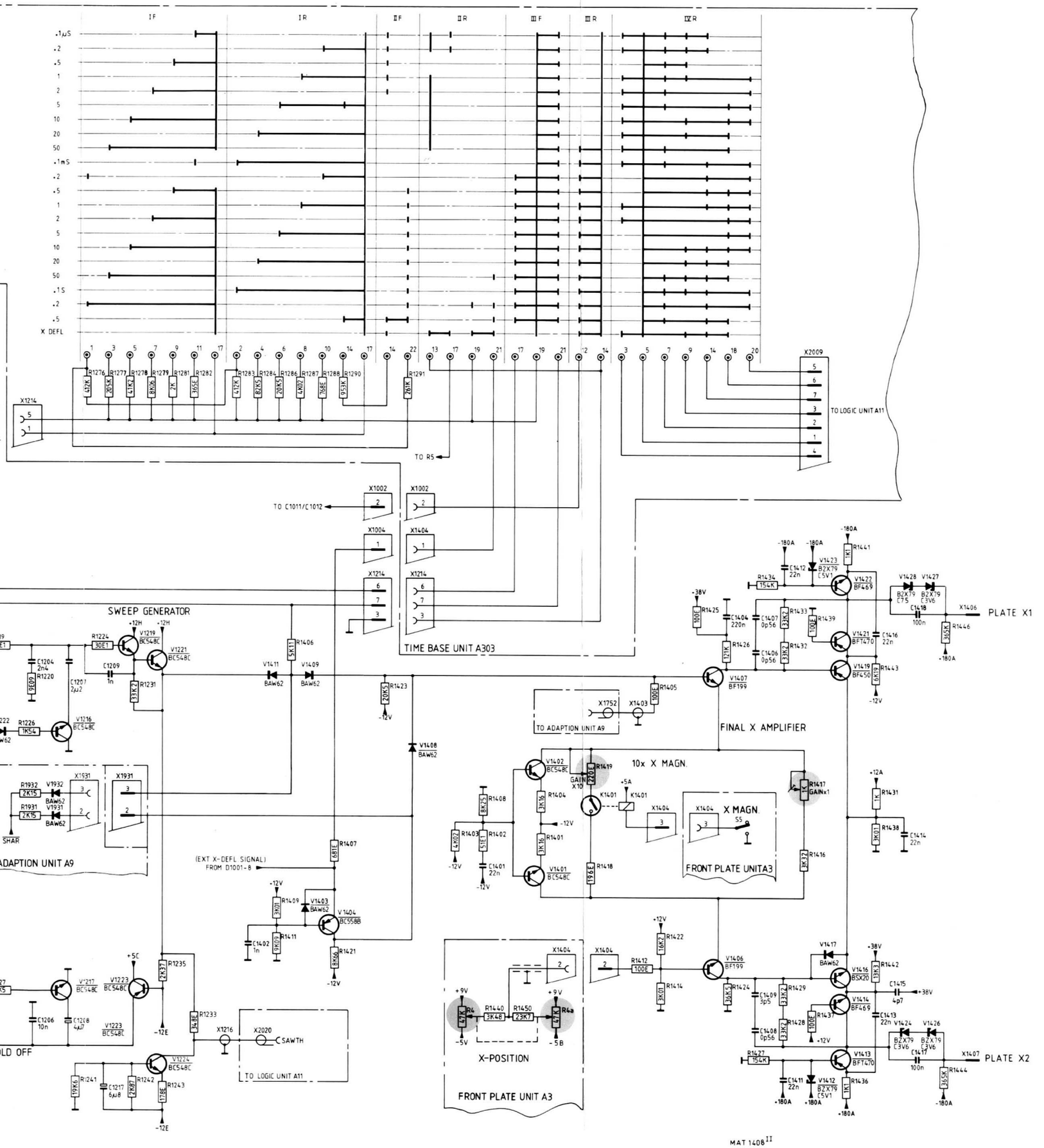


Fig. 10.27. DIAGRAM 4+5 Horizontal channels (A5)

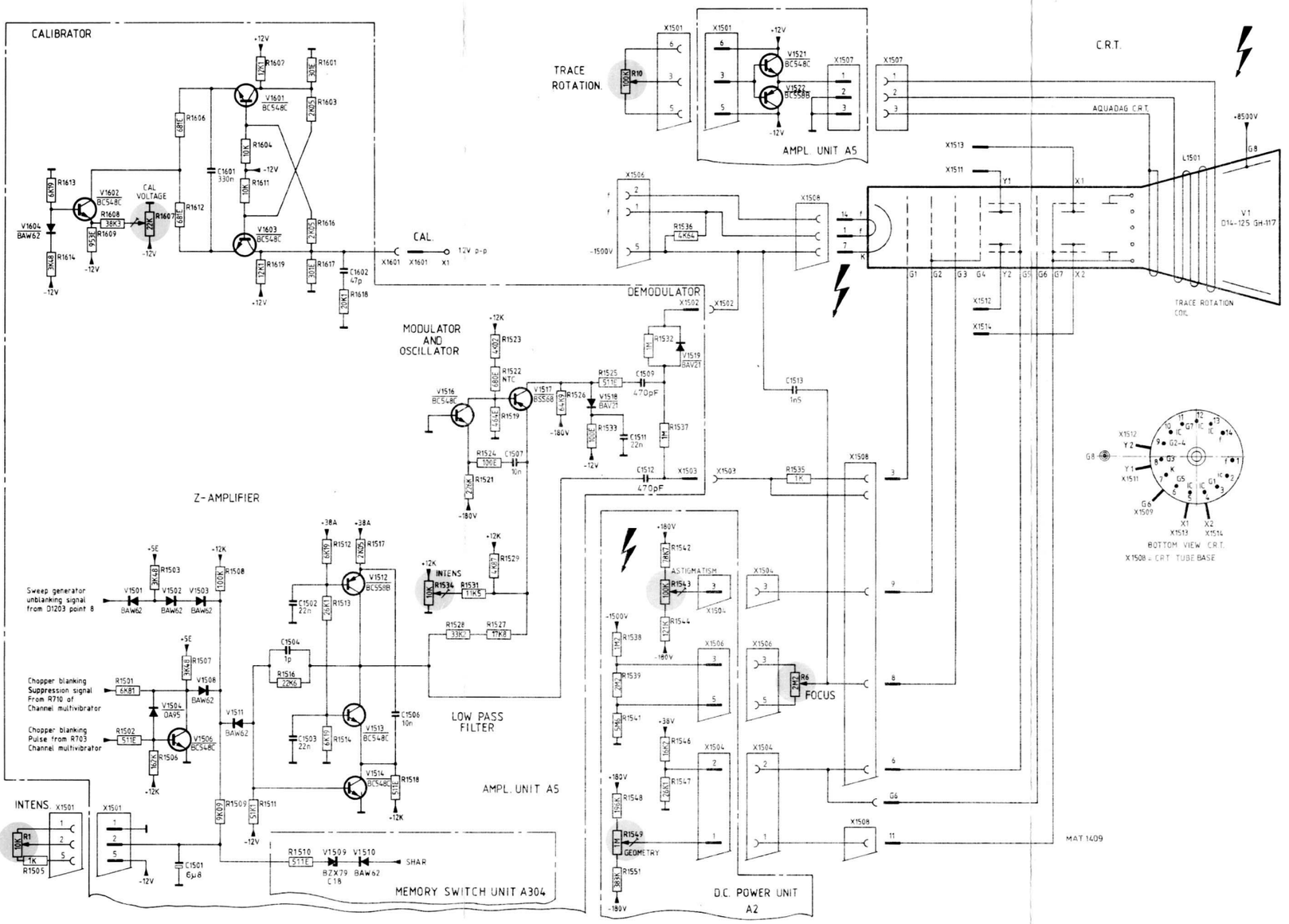


Fig. 10.28. DIAGRAM 6 Cathode-ray tube circuit (A5)

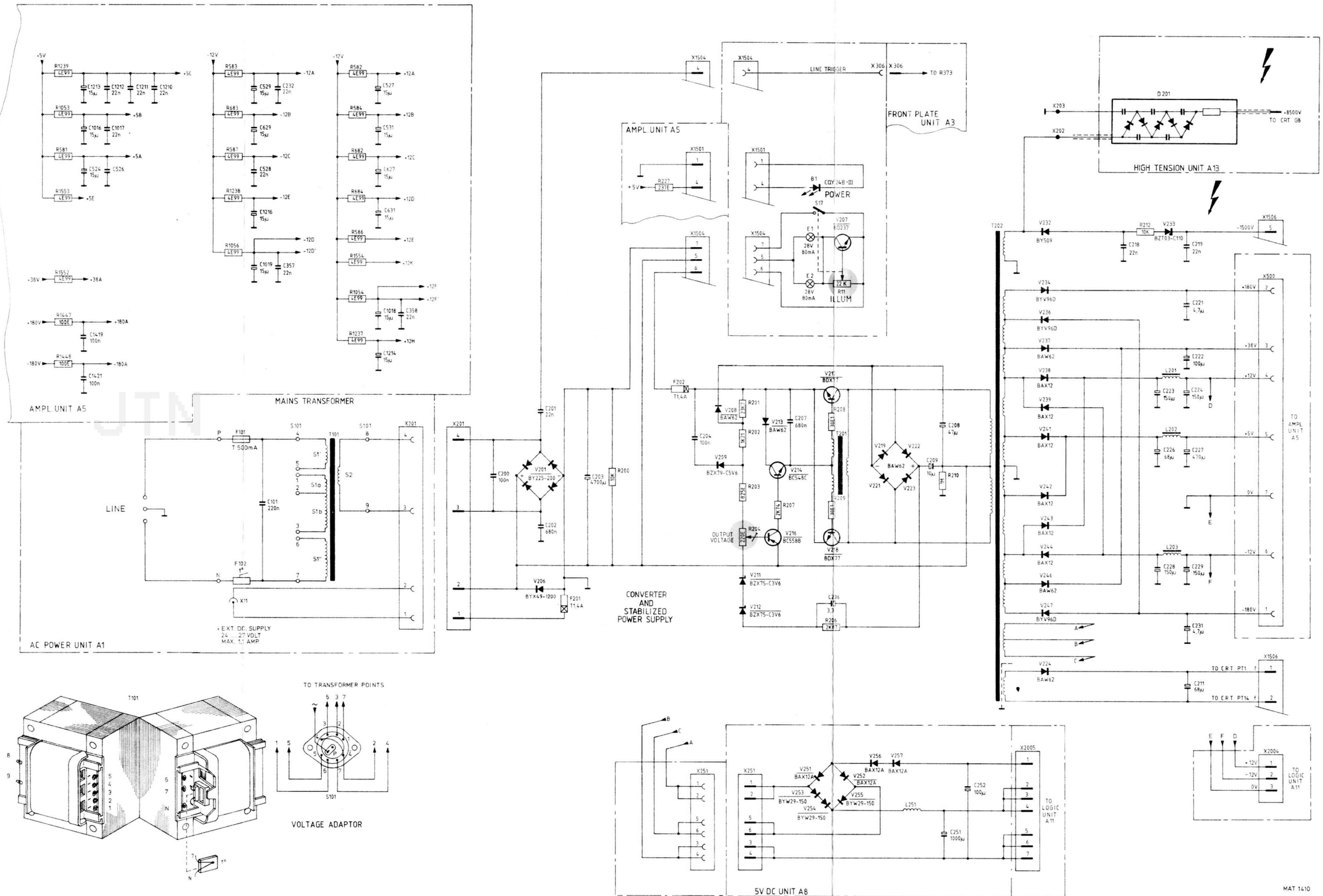
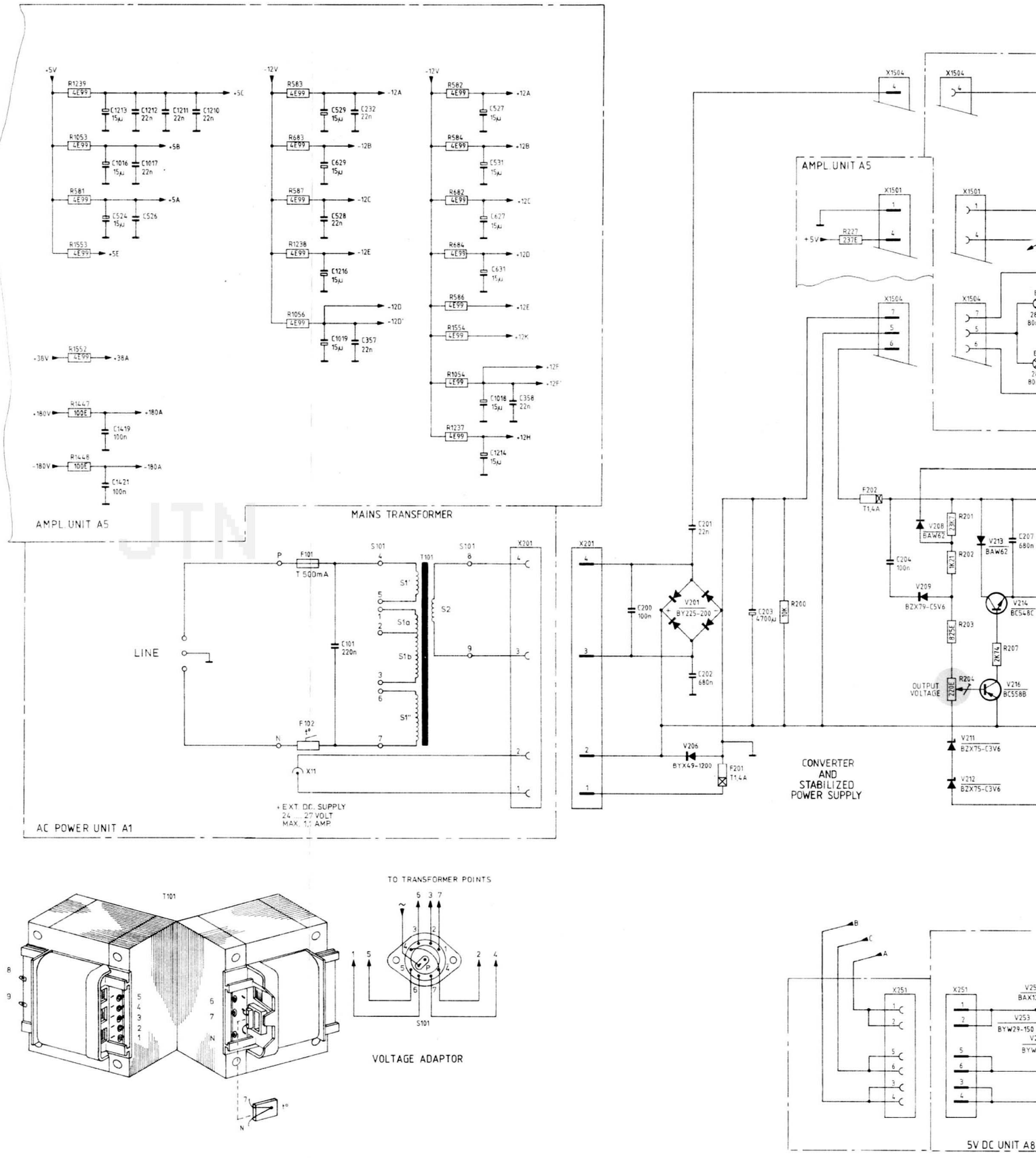


Fig. 10.29. DIAGRAM 7 Power supply (A1)


AMPL. UNIT A5
MAINS TRANSFORMER
LINE
F101
T 500mA
F102
T1.4A
F202
T1.4A
F201
T1.4A
X11
+ EXT. DC. SUPPLY
24 ... 27 VOLT
MAX. 1.1 AMP
AC POWER UNIT A1
CONVERTER
AND
STABILIZED
POWER SUPPLY
OUTPUT
VOLTAGE
BY225-200
BYX49-1200
BZX79-C5V6
BZX75-C3V6
BAW62
BC548B
BC558B
TO TRANSFORMER POINTS
VOLTAGE ADAPTOR
5V DC UNIT A8

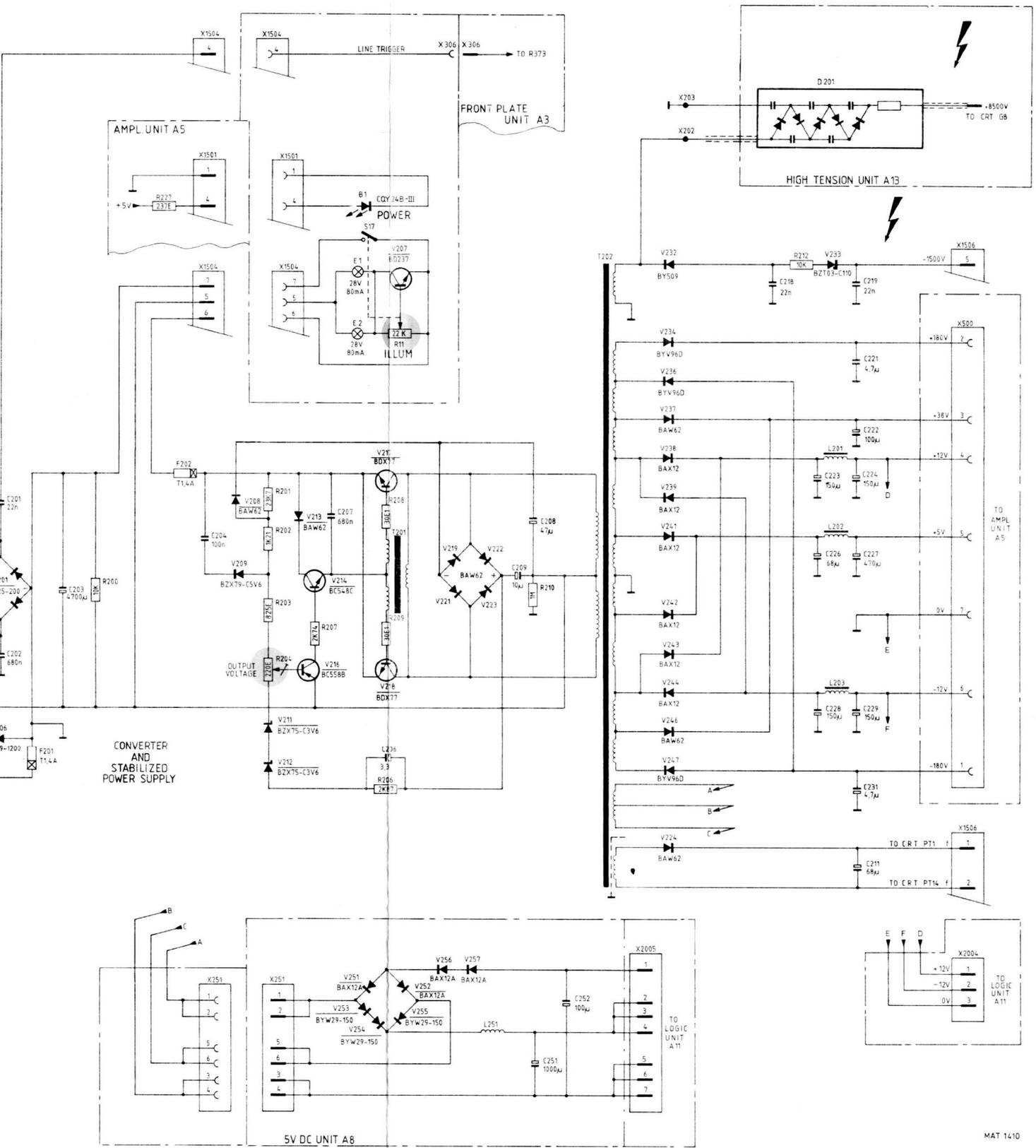
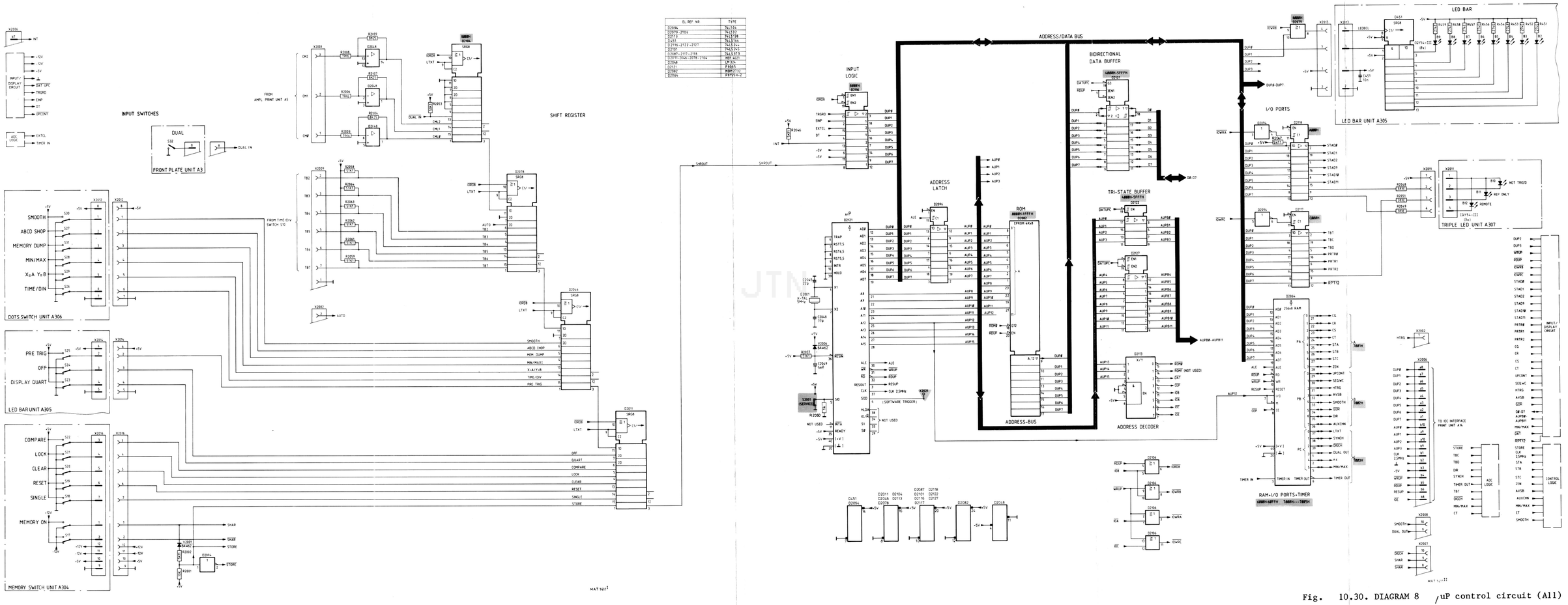


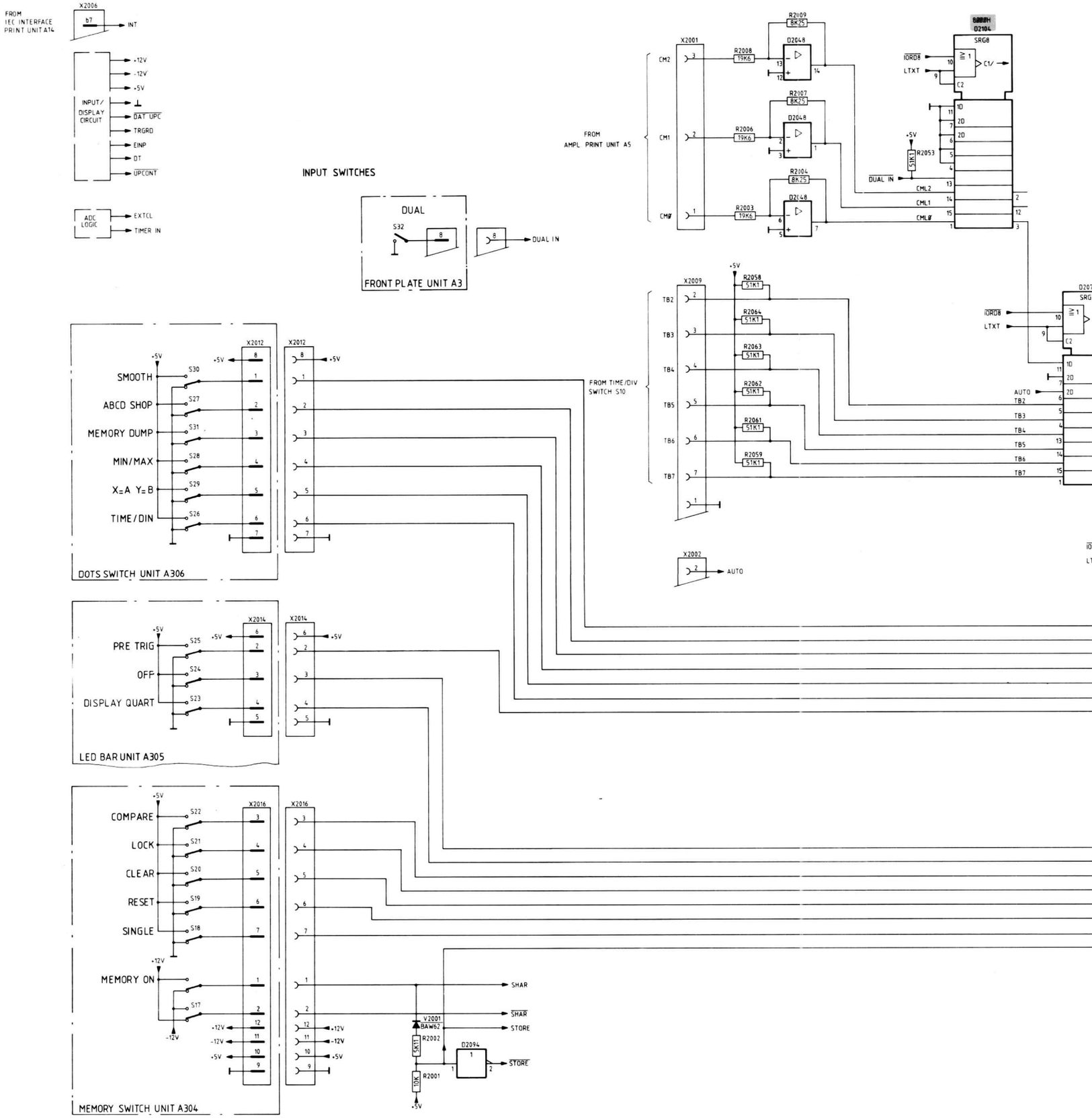
Fig. 10.29. DIAGRAM 7 Power supply (A1)



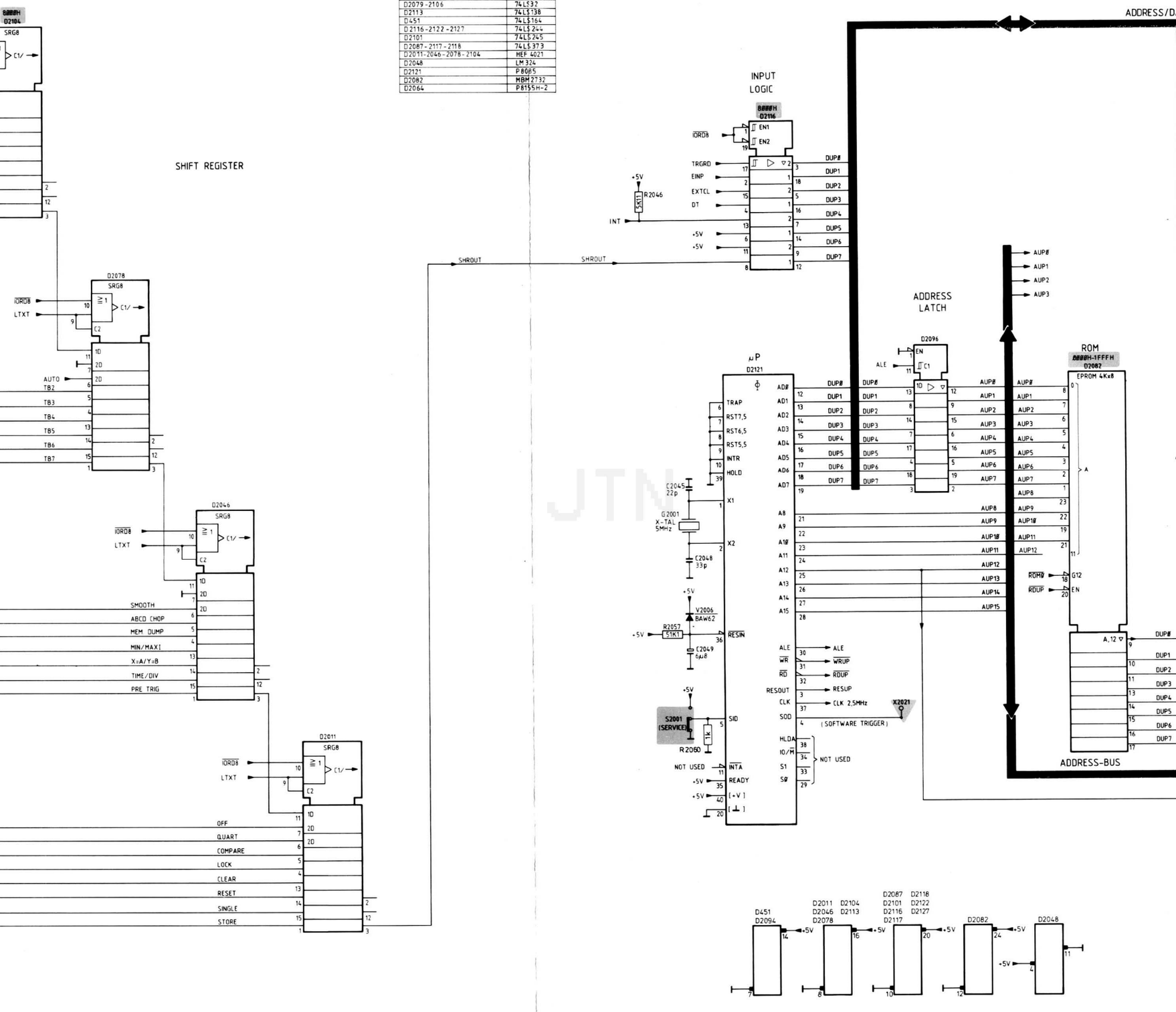
EL REF NR	TYPE
D2094	74LS04
D2078-2166	74LS32
D2113	74LS138
D157	74LS244
D2116-2122-2127	74LS244
D2101	74LS245
D2087-2117-2118	74LS373
D2111-2045-2078-2104	REF 4025
D2048	LM324
D221	P8031
D2062	M5M2732
D2044	P8755H-2

JTN

Fig. 10.30. DIAGRAM 8 µP control circuit (A11)


FROM IEC INTERFACE PRINT UNIT A14
X2006
b7
INT
+12V
-12V
+5V
INPUT/ DISPLAY CIRCUIT
DAT UPC
TRGRD
EINP
DT
UPCONT
ADC LOGIC
EXTCL
TIMER IN
INPUT SWITCHES
DUAL
S32
DUAL IN
FRONT PLATE UNIT A3
FROM AMPL PRINT UNIT A5
X2001
CM2
CM1
CM0
R2008 19K6
R2006 19K6
R2003 19K6
R2009 8K25
R2007 8K25
R2004 8K25
D2048
R2053 51K1
DUAL IN
CML2
CML1
CML0
SRG8
IORD8
LTXT
C1/
C2
D2104
2D
X2009
TB2
TB3
TB4
TB5
TB6
TB7
R2058 51K1
R2064 51K1
R2063 51K1
R2062 51K1
R2061 51K1
R2059 51K1
AUTO
X2002
X2012
SMOOTH
ABCD SHOP
MEMORY DUMP
MIN/MAX
X=A Y=B
TIME/DIV
S30
S27
S31
S28
S29
S26
DOTS SWITCH UNIT A306
FROM TIME/DIV SWITCH S10
X2014
PRE TRIG
OFF
DISPLAY QUART
S25
S24
S23
LED BAR UNIT A305
X2016
COMPARE
LOCK
CLEAR
RESET
SINGLE
MEMORY ON
S22
S21
S20
S19
S18
S17
MEMORY SWITCH UNIT A304
SHAR
SHAR
STORE
STORE
V2001 BAW62
R2002 5K11
R2001 10K
D2094

EL REF NR	TYPE
D2094	74LS04
D2079-2106	74LS32
D2113	74LS138
D451	74LS164
D2116-2122-2127	74LS244
D2101	74LS245
D2087-2117-2118	74LS373
D2011-2046-2078-2104	HEF 4021
D2048	LM324
D2121	P8085
D2082	MBM2732
D2064	P8155H-2



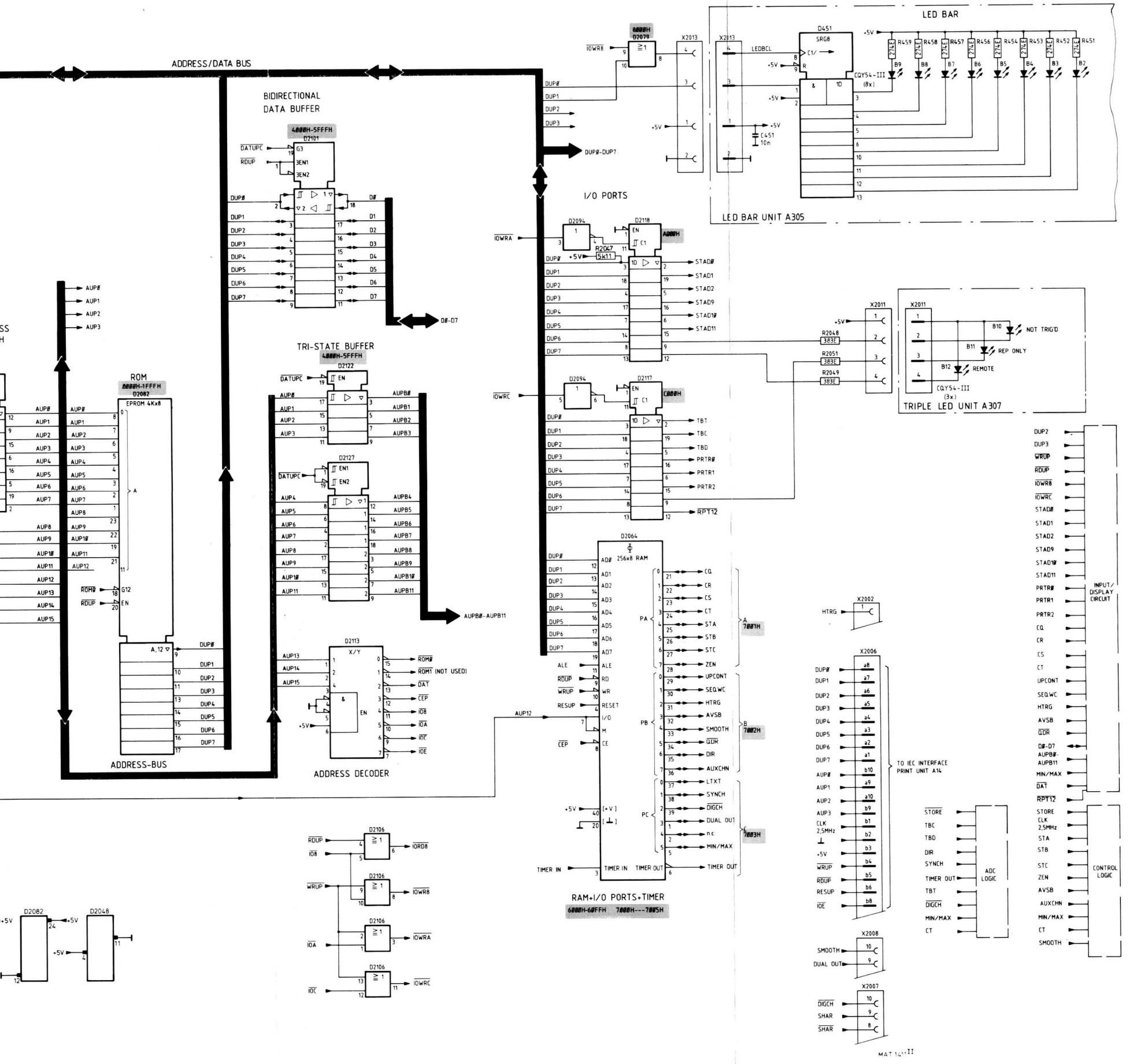
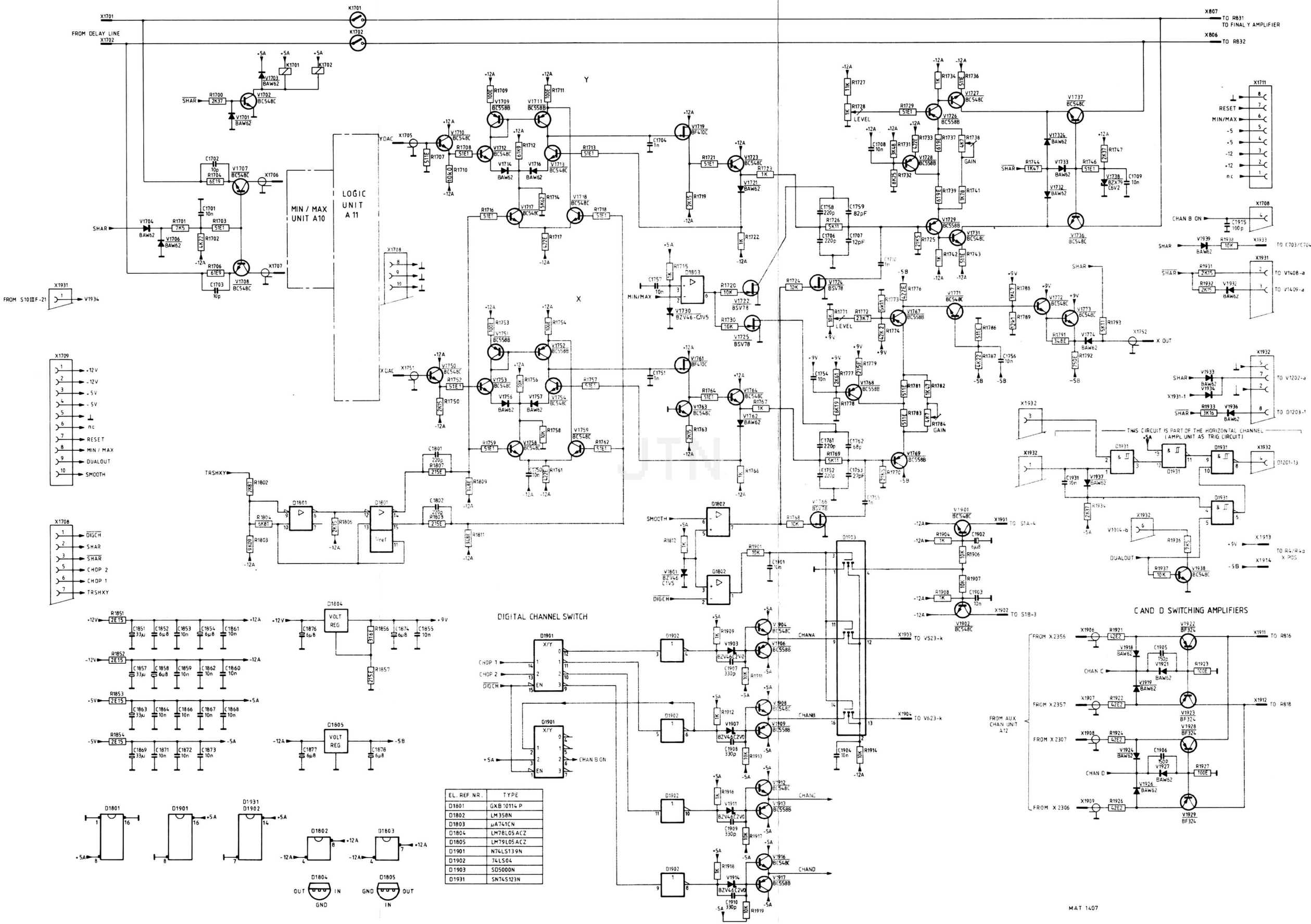


Fig. 10.30. DIAGRAM 8 /uP control circuit (A11)

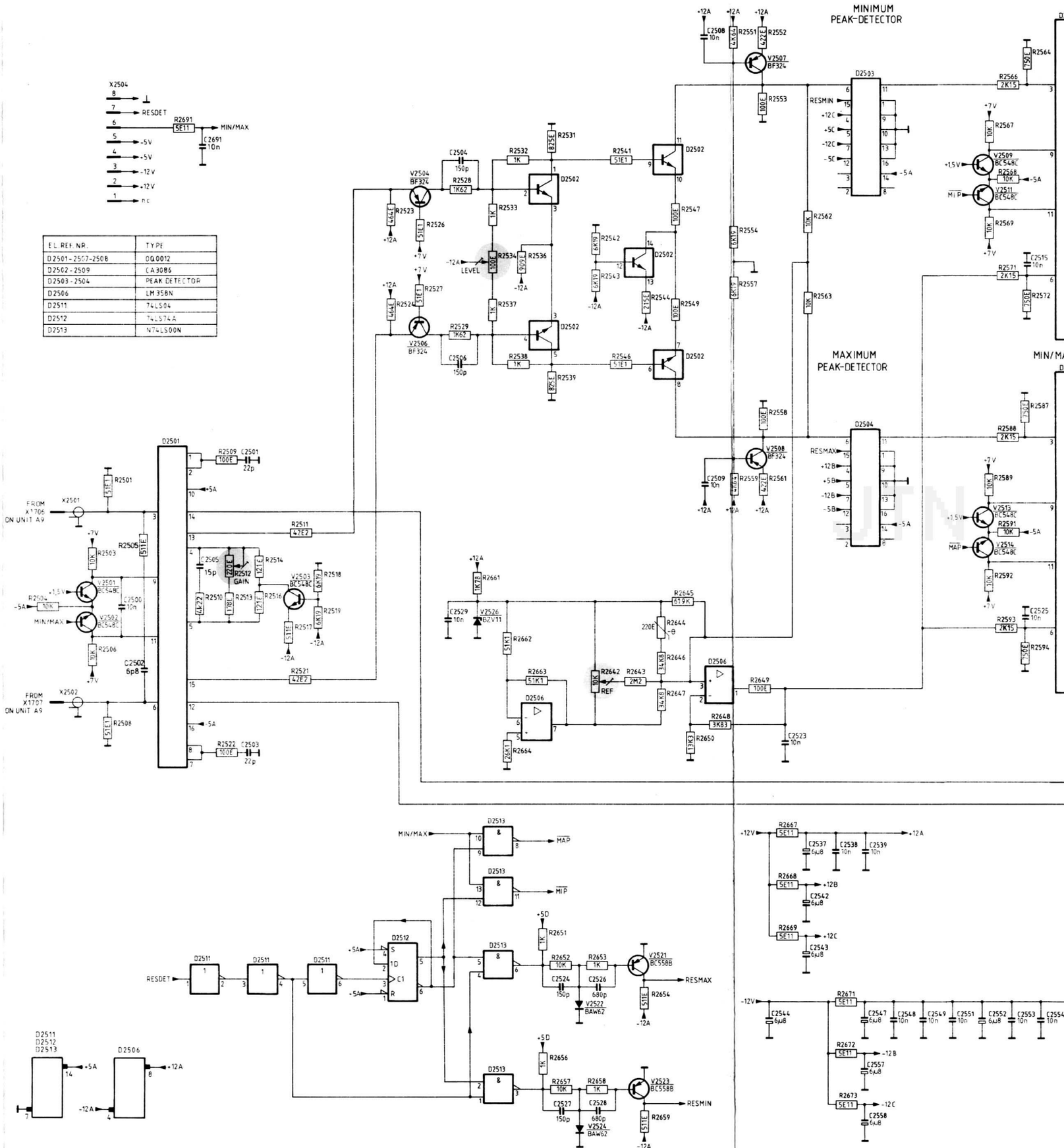


EL. REF. NR.	TYPE
D1801	GXB10114 P
D1802	LM358N
D1803	µA741CN
D1804	LM78L05ACZ
D1805	LM79L05ACZ
D1901	N74LS139N
D1902	74LS04
D1903	SD5000N
D1931	SN74S123N

Fig. 10.31. DIAGRAM 9 Adaption circuit (A9)

EL.REF.NR.	TYPE
D2501-2507-2508	OQ0012
D2502-2509	CA3086
D2503-2504	PEAK DETECTOR
D2506	LM358N
D2511	74LS04
D2512	74LS74A
D2513	N74LS00N

Fig. 10.32. DIAGRAM 10 Min/max circuit (A10)



EL. REF. NR.	TYPE
D2501-2507-2508	DQ0012
D2502-2509	CA3086
D2503-2504	PEAK DETECTOR
D2506	LM358N
D2511	74LS04
D2512	74LS74A
D2513	N74LS00N

Fig. 10.32. DIAGRAM 10

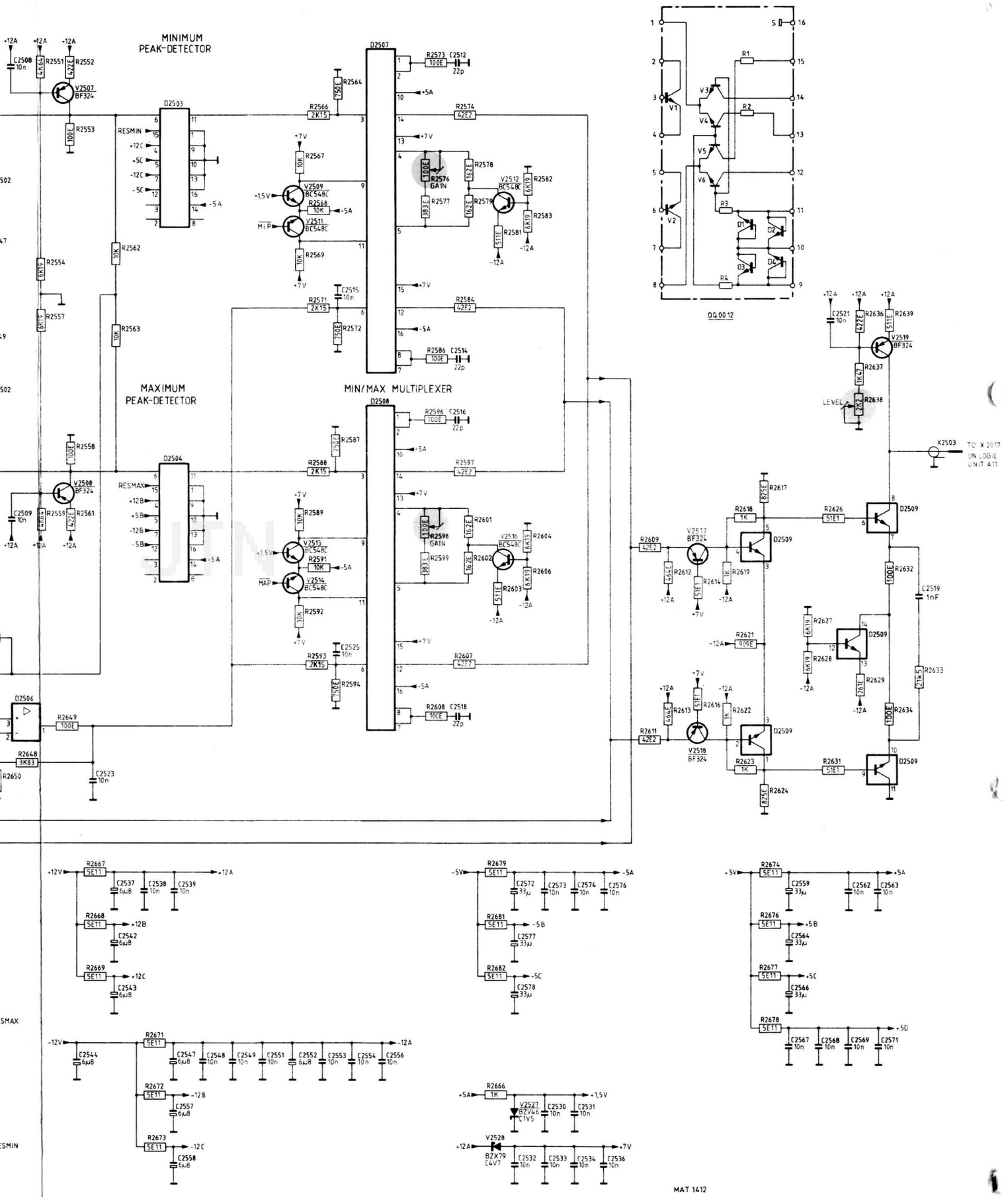


Fig. 10.32. DIAGRAM 10 Min/max circuit (A10)

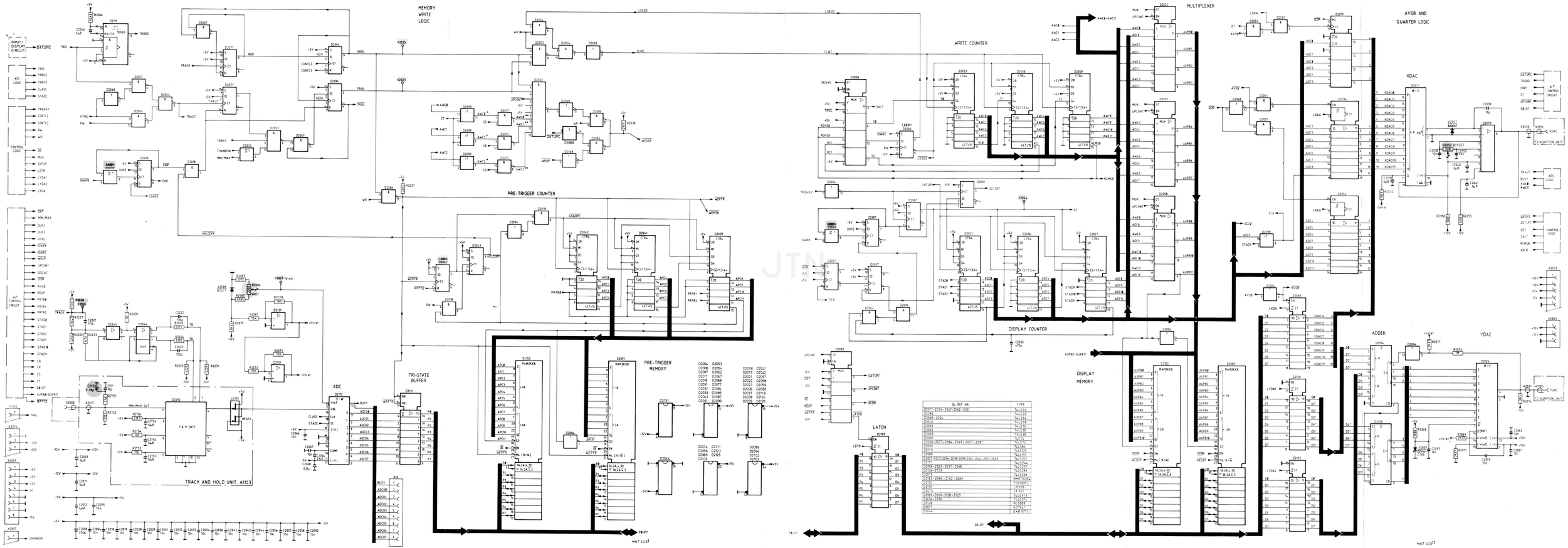
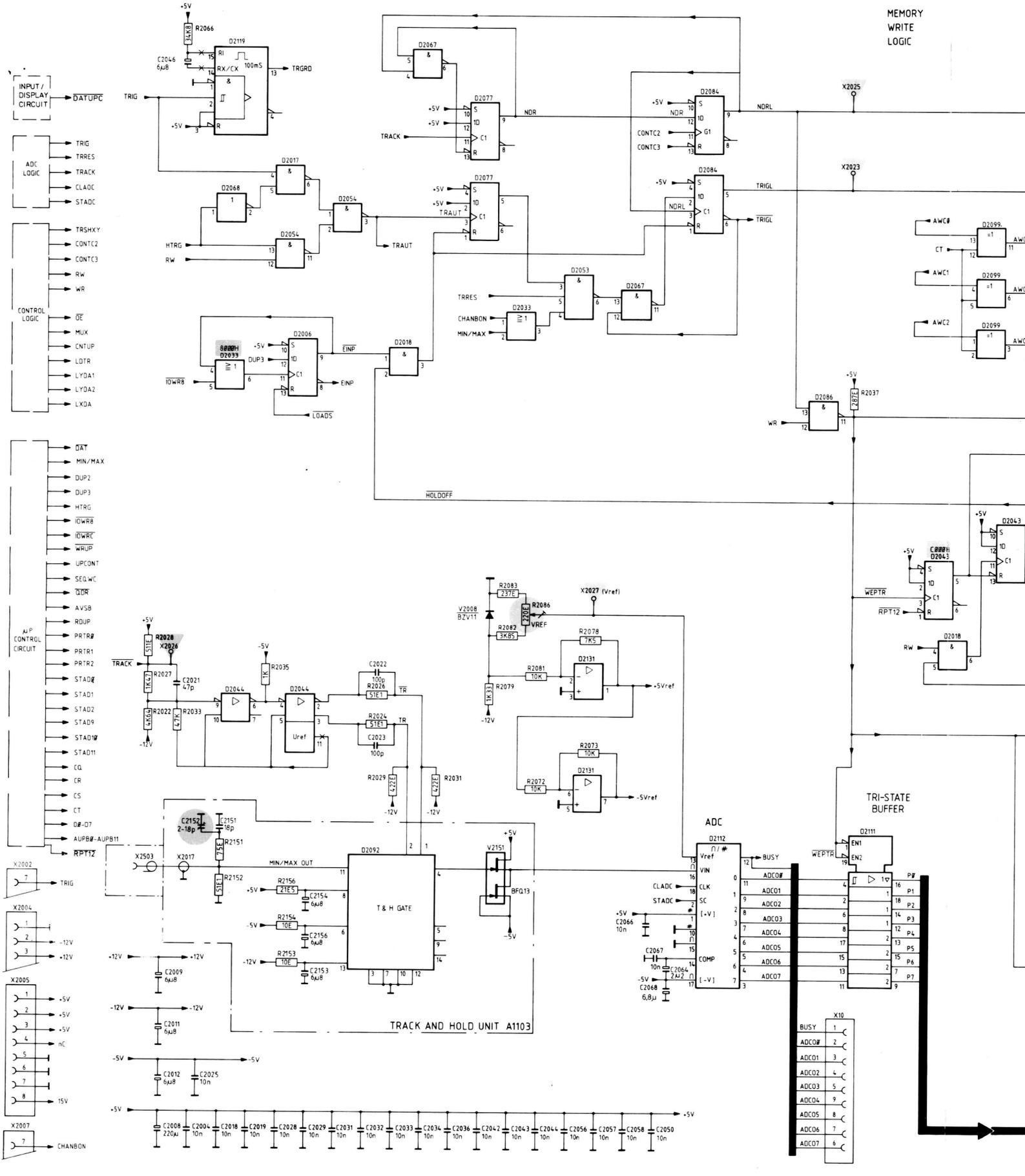
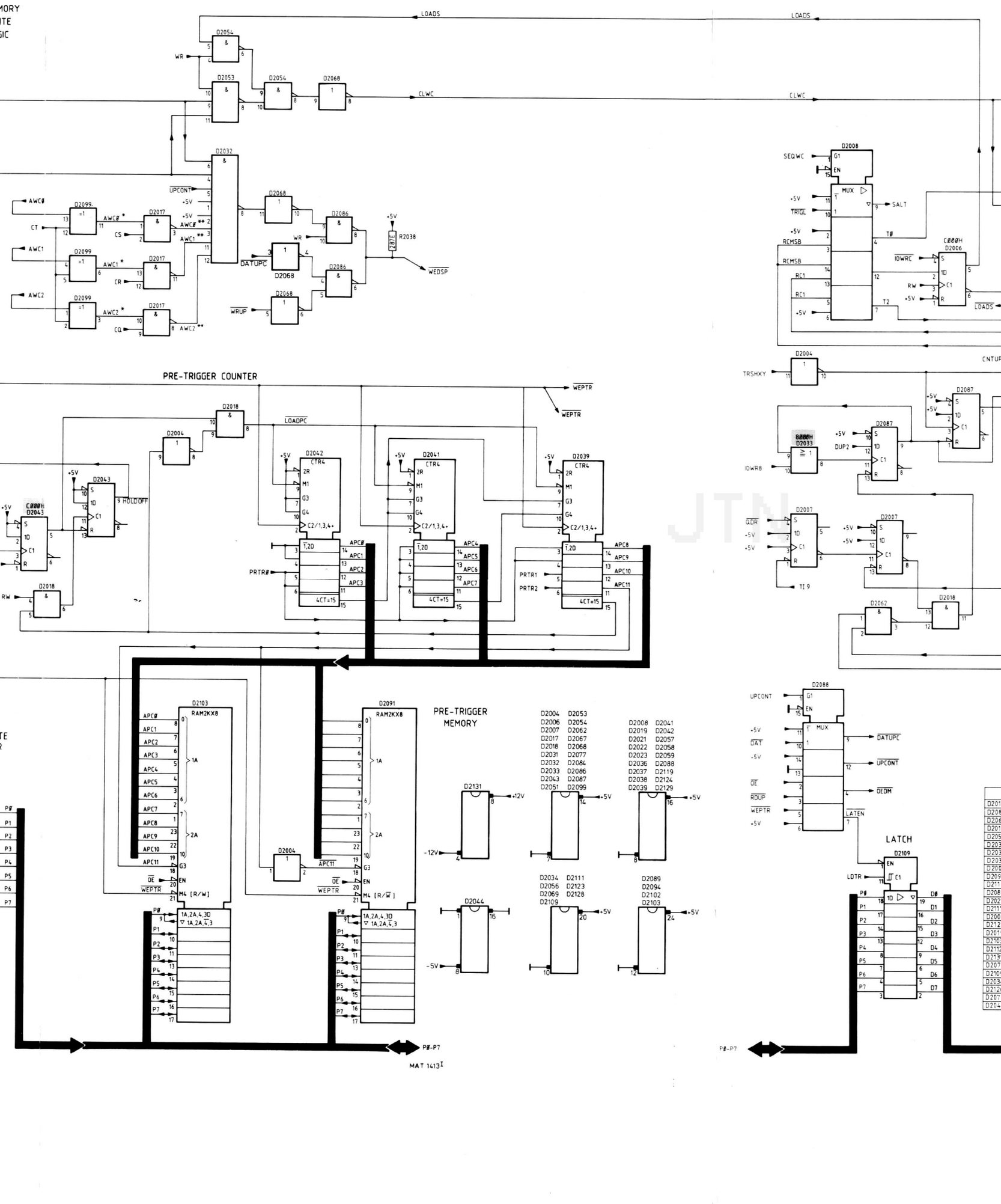
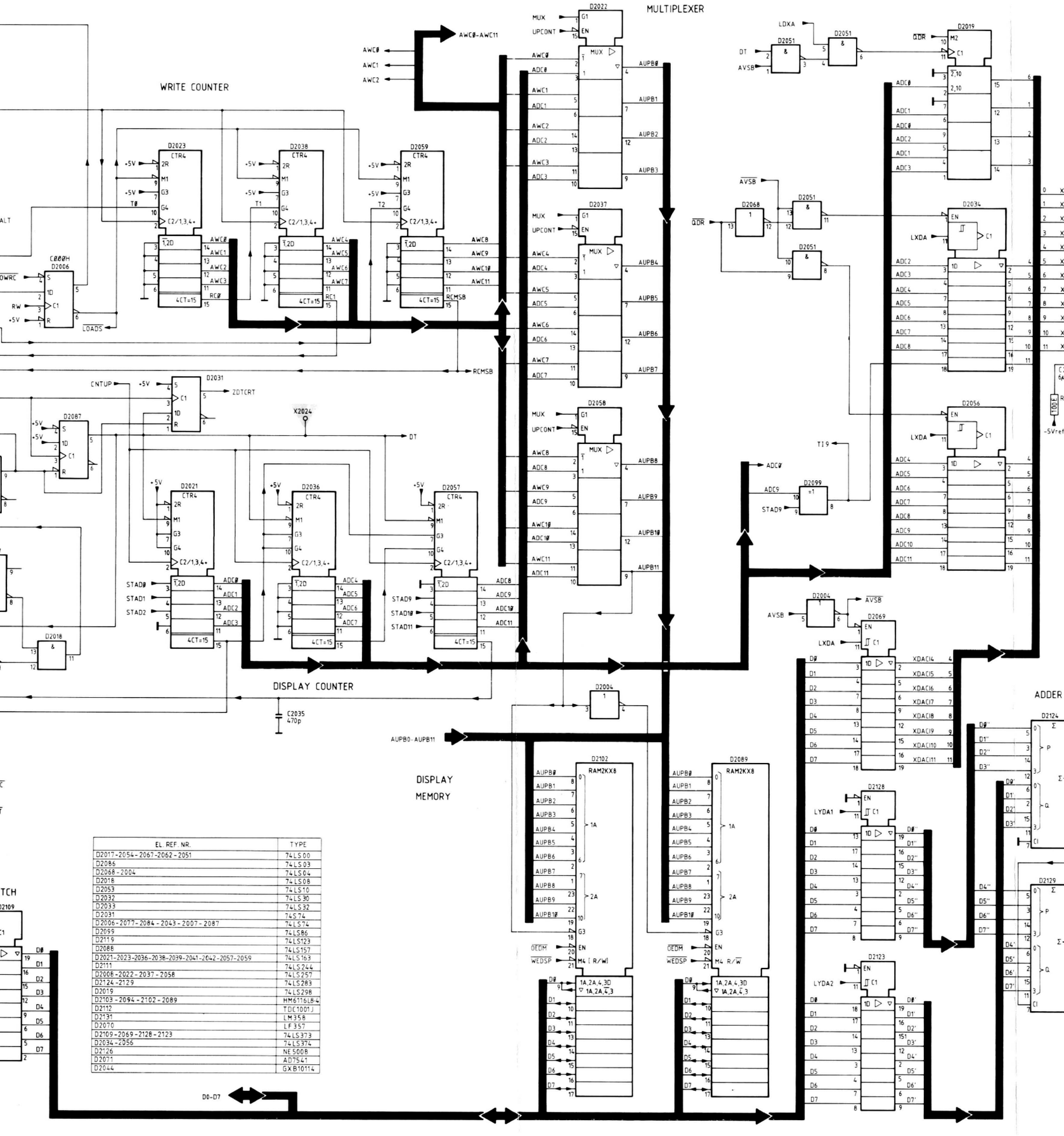


Fig. 10.33. DIAGRAM 11 Input/display circuit (A11)


MEMORY
WRITE
LOGIC
INPUT / DISPLAY CIRCUIT
DATUPC
ADC LOGIC
TRIG
TRRES
TRACK
CLADC
STADC
CONTROL LOGIC
TRSHXY
CONTC2
CONTC3
RW
WR
OE
MUX
CNTUP
LDTR
LYDA1
LYDA2
LXDA
A/P CONTROL CIRCUIT
DAT
MIN/MAX
DUP2
DUP3
HTRG
IOWR8
IOWRC
WRUP
UPCONT
SEQ.WC
LDR
AVSB
RDUP
PRTR0
PRTR1
PRTR2
STAD0
STAD1
STAD2
STAD9
STAD10
STAD11
CQ
CR
CS
CT
D0-D7
AUPB0-AUPB11
RPT12
X2002
X2004
X2005
X2007
TRIG
-12V
+12V
+5V
nC
15V
CHANBON
+5V
R2066
34K8
C2046
6µ8
D2119
RI
RX/CX
100mS
TRGRD
D2067
D2077
NDR
TRACK
D2084
NDRL
CONTC2
CONTC3
X2025
X2023
TRIGL
D2017
D2068
D2054
HTRG
RW
TRAUT
D2053
TRRES
CHANBON
MIN/MAX
D2033
D2006
DUP3
IOWR8
EINP
LOADS
D2018
HOLDOFF
D2086
WR
R2037
287E
D2099
AWC0
AWC1
AWC2
CT
D2043
WEPTR
RPT12
RW
R2083
237E
R2086
220E
VREF
V2008
BZV11
R2082
3K85
X2027 (Vref)
R2078
7K5
R2081
10K
R2079
1K33
D2131
+5Vref
R2073
10K
R2072
10K
-5Vref
R2028
X2026
R2027
1K42
C2021
47p
R2022
4K64
R2033
4,7K
R2035
1K
D2044
Uref
C2022
100p
R2026
51E1
R2024
51E1
C2023
100p
TR
R2029
422E
R2031
422E
C2152
2-18p
C2151
18p
R2151
75E
X2503
X2017
MIN/MAX OUT
R2152
51E1
R2156
21E5
C2154
6µ8
R2154
10E
C2156
6µ8
R2153
10E
C2153
6µ8
D2092
T & H GATE
V2151
BFQ13
TRACK AND HOLD UNIT A1103
ADC
D2112
Vref
VIN
CLK
SC
[+V]
COMP
[-V]
BUSY
ADC0#
ADC01
ADC02
ADC03
ADC04
ADC05
ADC06
ADC07
CLADC
STADC
C2066
10n
C2067
10n
C2064
2µ2
C2068
6,8µ
TRI-STATE BUFFER
D2111
EN1
EN2
P0
P1
P2
P3
P4
P5
P6
P7
X10
C2009
C2011
C2012
C2025
C2008
220µ
C2004
C2018
C2019
C2028
C2029
C2031
C2032
C2033
C2034
C2036
C2042
C2043
C2044
C2056
C2057
C2058
C2050


LOADS
CLWC
WR
UPCONT
DATUPC
WRUP
WEDSP
R2038
AWC0
AWC1
AWC2
CT
CR
CS
CQ
SEQWC
SALT
TRIGL
RCMSB
RC1
IOWRC
RW
TRSHXY
CNTUP
IOWR8
QDR
PRE-TRIGGER COUNTER
LOADPC
WEPTR
HOLDOFF
PRTR0
PRTR1
PRTR2
RAM2KX8
PRE-TRIGGER MEMORY
LATCH
DATUPC
OEDM
LATEN
P0-P7
MAT 1413I



EL. REF. NR.	TYPE
D2017-2054-2067-2062-2051	74LS00
D2086	74LS03
D2068-2004	74LS04
D2018	74LS08
D2053	74LS10
D2032	74LS30
D2033	74LS32
D2031	74S74
D2006-2077-2084-2043-2007-2087	74LS74
D2099	74LS86
D2119	74LS123
D2088	74LS157
D2021-2023-2036-2038-2039-2041-2042-2057-2059	74LS163
D2111	74LS244
D2008-2022-2037-2058	74LS257
D2124-2129	74LS283
D2019	74LS298
D2103-2094-2102-2089	HM6116L8-4
D2112	TDC1001J
D2131	LM358
D2070	LF357
D2109-2069-2128-2123	74LS373
D2034-2056	74LS374
D2126	NE5008
D2071	AD7541
D2044	GXB10114

Fig. 10.33. DI

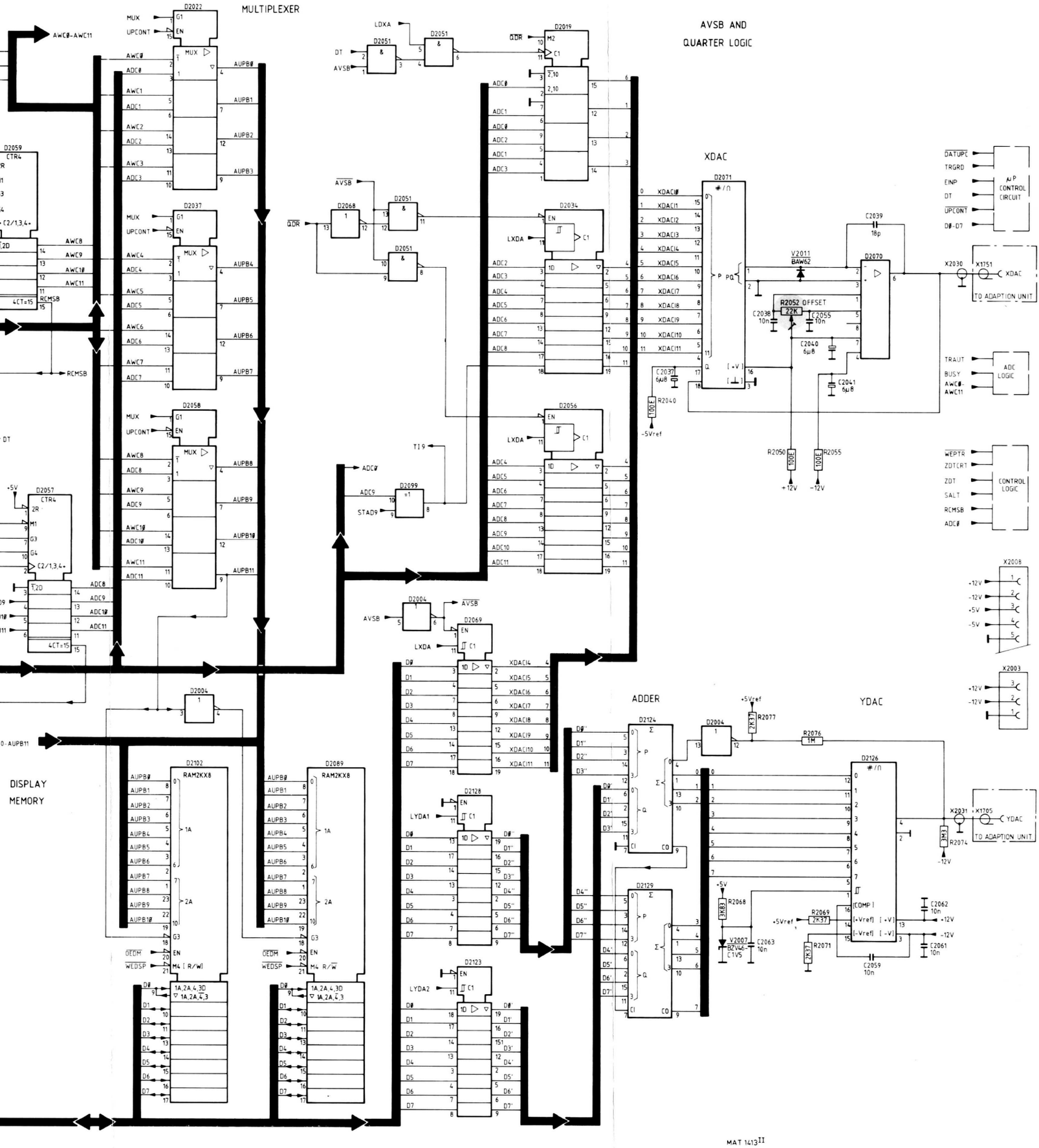
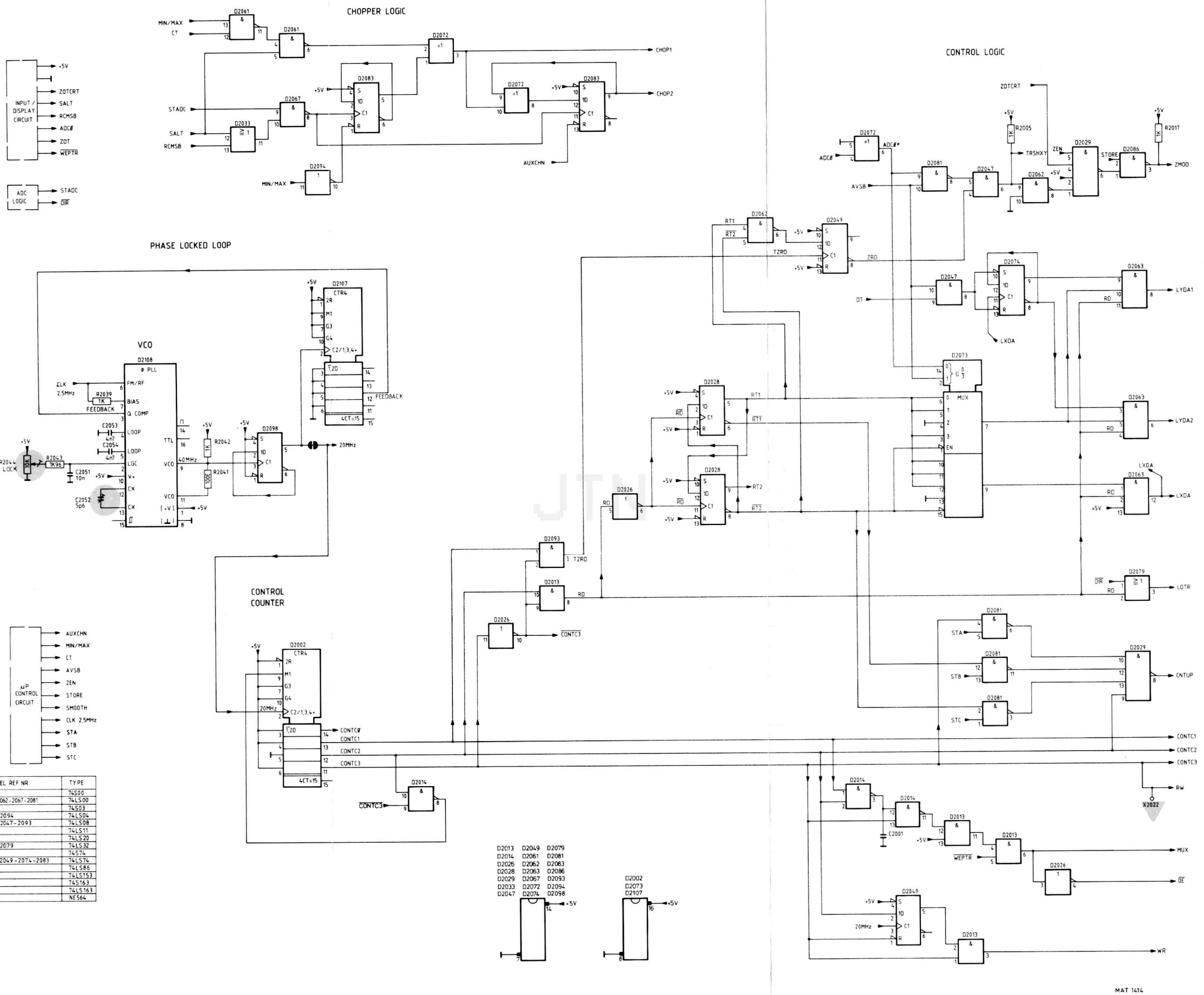


Fig. 10.33. DIAGRAM 11 Input/display circuit (A11)



EL. REF. NR.	TYPE
D2061	74S00
D2014-2062-2067-2081	74LS00
D2086	74S03
D2026-2094	74LS04
D2013-2047-2093	74LS08
D2063	74LS11
D2029	74LS20
D2033-2079	74LS32
D2098	74S74
D2028-2049-2074-2083	74LS74
D2072	74LS86
D2073	74LS153
D2002	74S163
D2107	74LS163
D2108	NE564

MAT 1414

Fig. 10.34. DIAGRAM 12 Control logic (A11)

EL REF. NR	TYPE
D2014-2061-2061	74LS00
D2027	74S02
D2026-2068-2094	74LS04
D2047-2093	74LS08
D2053	74LS10
D2076	74S32
D2079	74LS32
D2031-2052-2066-2098	74 S 74
D2072	74LS86
D2119	74LS123
D2001	74S151
D2012	74LS160
D2009	AD7541
D2024	LF357
D2016	NE521

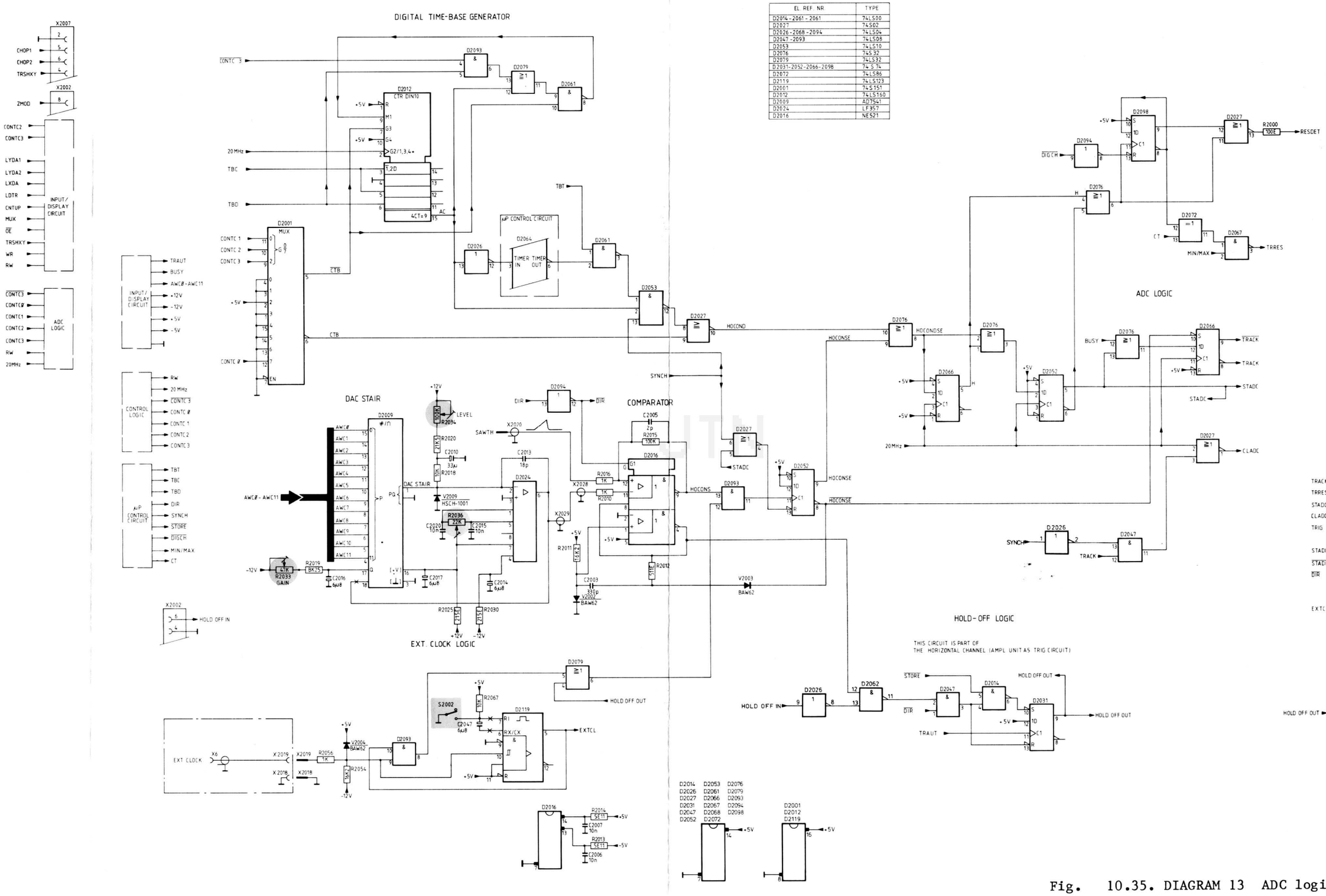
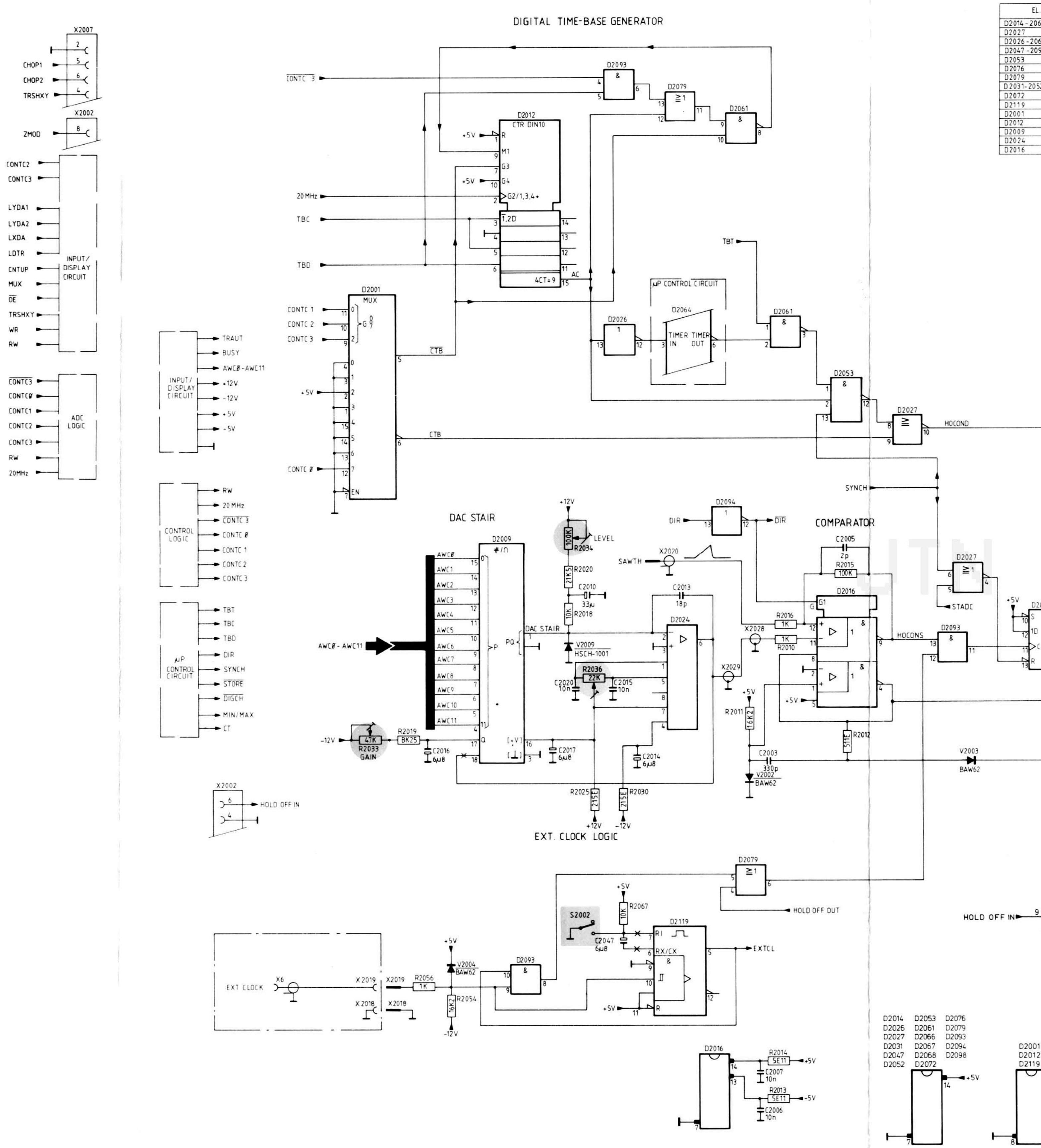
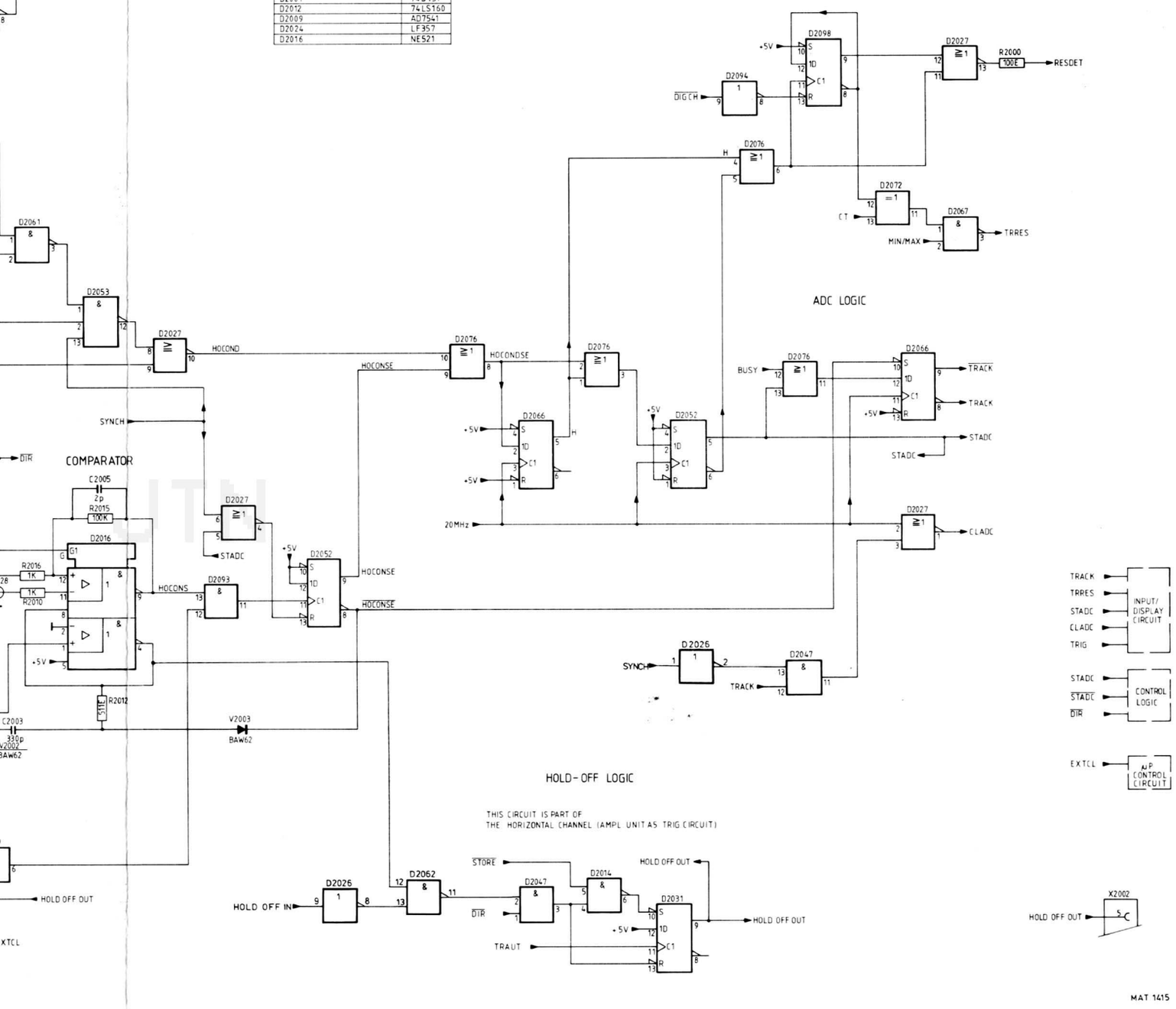


Fig. 10.35. DIAGRAM 13 ADC logic (A11)


DIGITAL TIME-BASE GENERATOR
DAC STAIR
COMPARATOR
EXT. CLOCK LOGIC
INPUT/ DISPLAY CIRCUIT
ADC LOGIC
CONTROL LOGIC
μP CONTROL CIRCUIT
μP CONTROL CIRCUIT
EXT CLOCK
HOLD OFF IN
HOLD OFF OUT
EXTCL
HOCOND
HOCONS
SYNCH
STADC
AWC0 - AWC11
X2007
X2002
D2001 MUX
D2009
D2012 CTR DIN10
D2016
D2024
D2119
R2033 GAIN
R2034 LEVEL
S2002

EL. REF. NR.	TYPE
D2014 - 2061 - 2061	74LS00
D2027	74S02
D2026 - 2068 - 2094	74LS04
D2047 - 2093	74LS08
D2053	74LS10
D2076	74S32
D2079	74LS32
D2031 - 2052 - 2066 - 2098	74 S 74
D2072	74LS86
D2119	74LS123
D2001	74S151
D2012	74LS160
D2009	AD7541
D2024	LF357
D2016	NE521



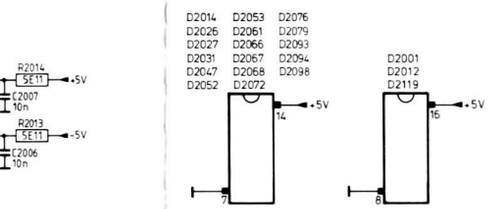
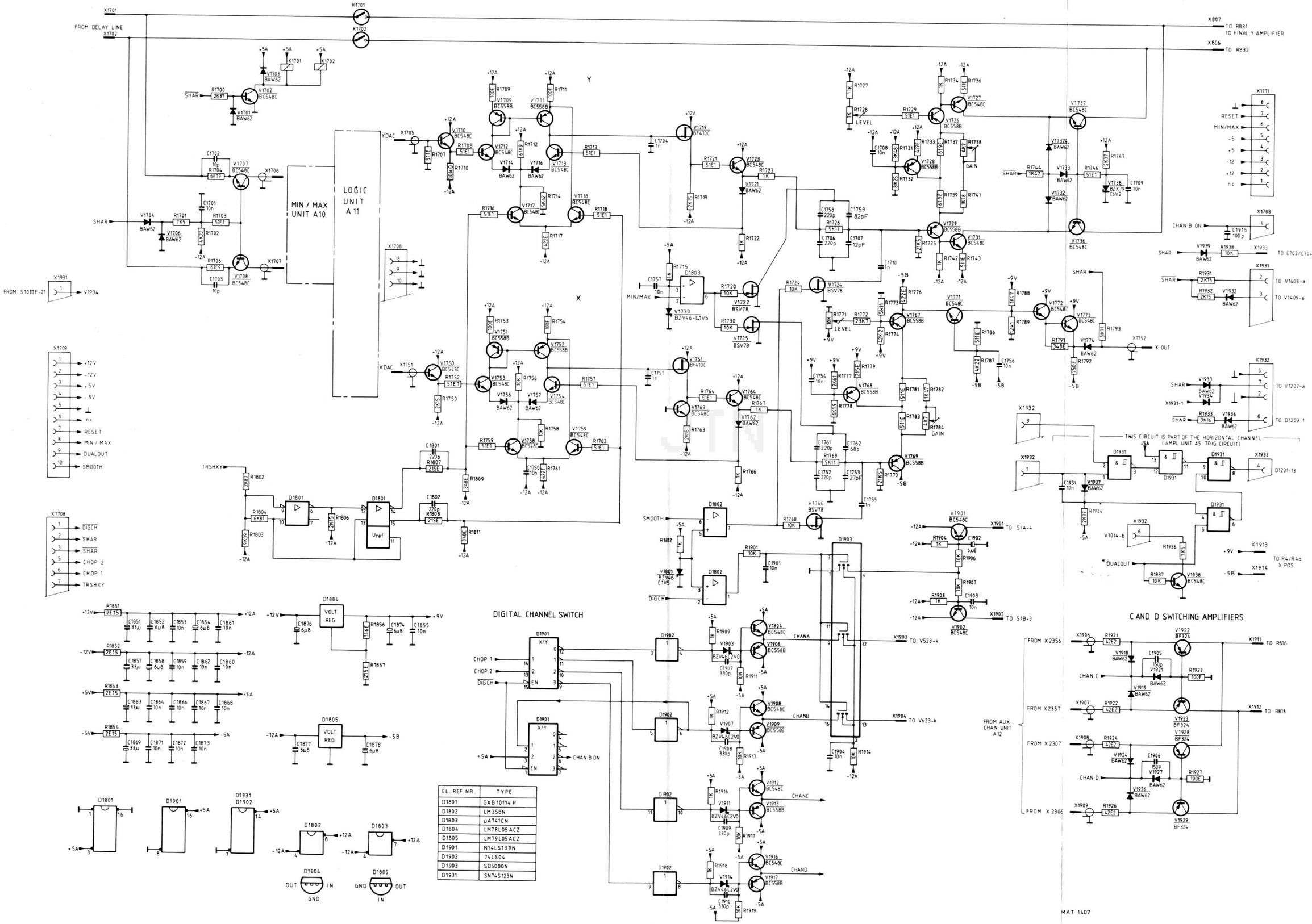
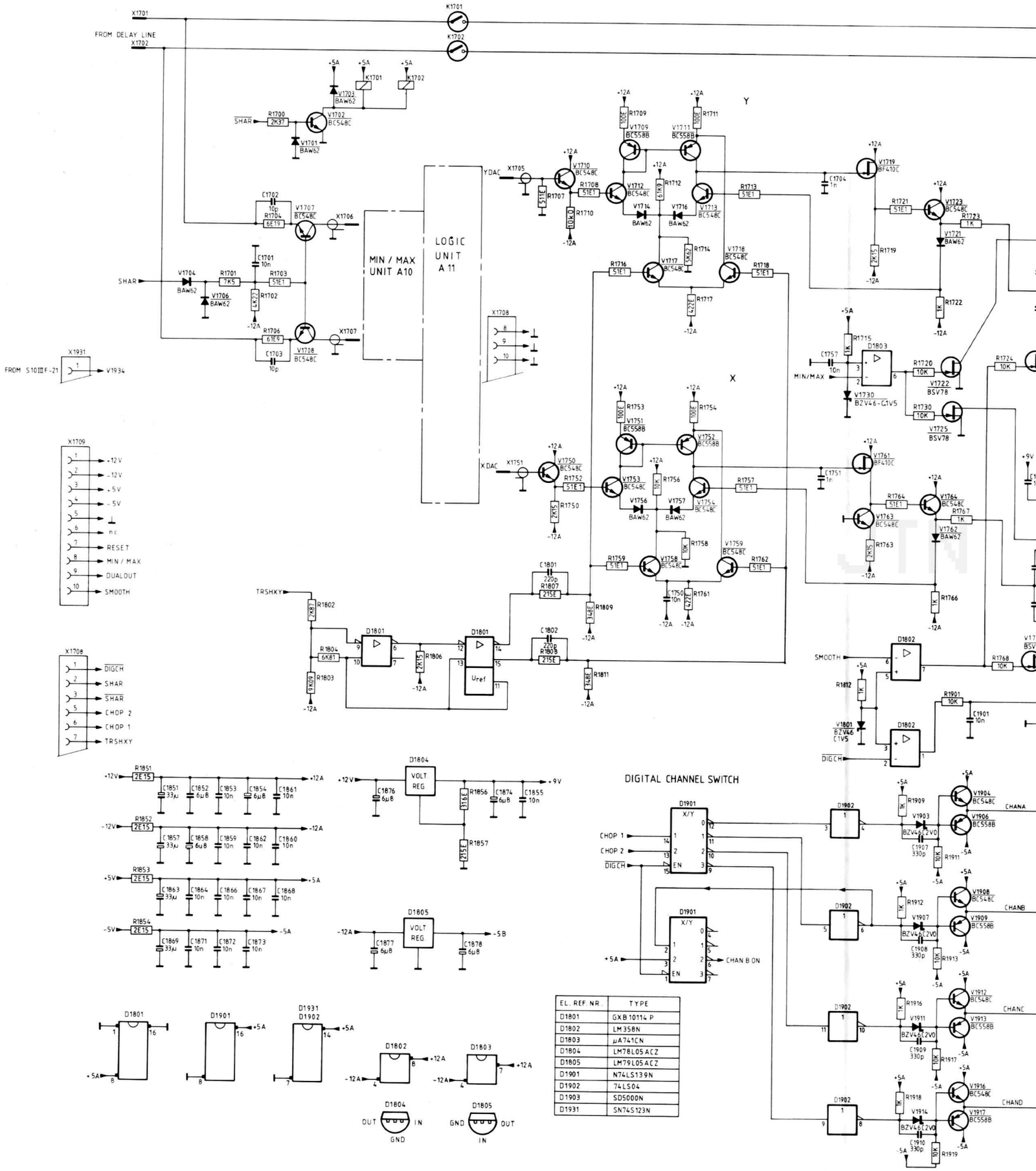


Fig. 10.35. DIAGRAM 13 ADC logic (A11)



EL. REF. NR.	TYPE
D1801	GXB10114 P
D1802	LM358N
D1803	µA741CN
D1804	LM78L05ACZ
D1805	LM79L05ACZ
D1901	N74LS139N
D1902	74LS04
D1903	SD5000N
D1931	SN74S123N

Fig. 10.36. DIAGRAM 14
Adaption circuit (A9)



EL. REF. NR.	TYPE
D1801	GXB10114 P
D1802	LM358N
D1803	µA741CN
D1804	LM78L05ACZ
D1805	LM79L05ACZ
D1901	N74LS139N
D1902	74LS04
D1903	SD5000N
D1931	SN74S123N

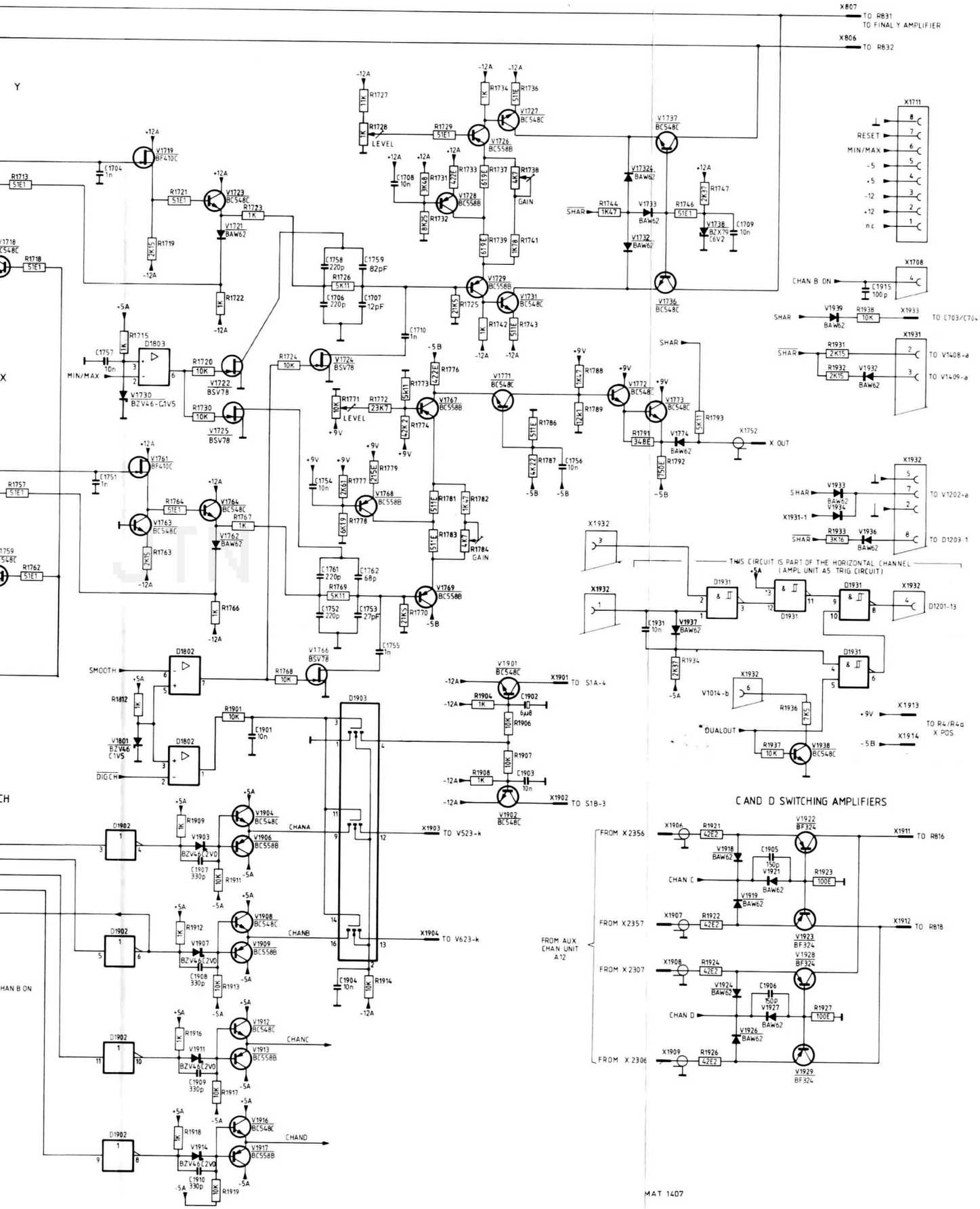
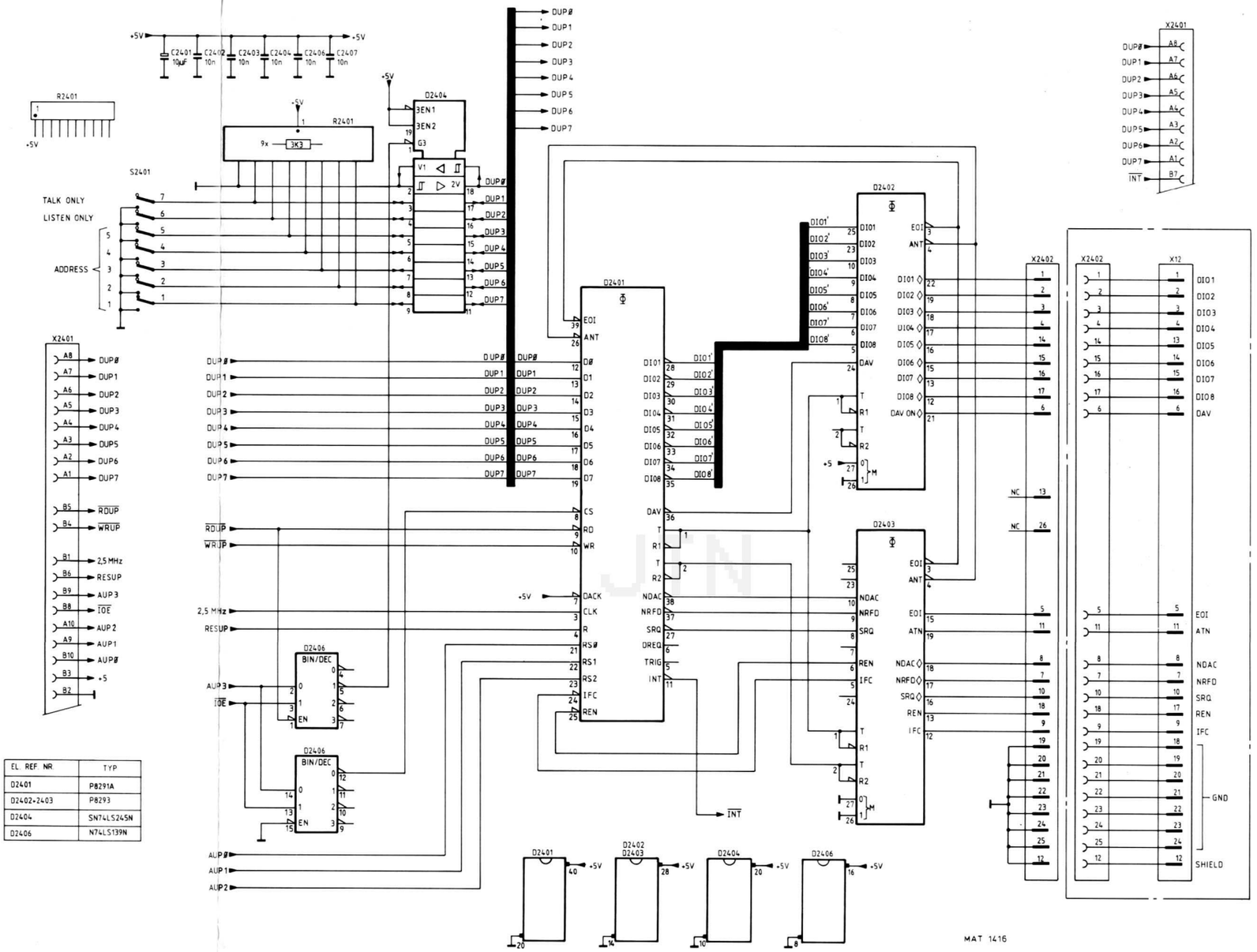


Fig. 10.36. DIAGRAM 14
Adaption circuit (A9)



EL. REF. NR.	TYP
D2401	P8291A
D2402-2403	P8293
D2404	SN74LS245N
D2406	N74LS139N

Fig. 10.37. DIAGRAM 15 IEEE-488/IEC-625 option (A14)

11. LIST OF SIGNAL DENOMINATIONS

Signal	Generated on unit	Description
ABCDCHOP	A305-S27	Signal from pushbutton ABCDCHOP.
ALE	A11	Address latch enable signal. Indication from the microprocessor when address information is applied to the bus lines.
A8-A15	A11	8 M.S.B.'s of the microprocessor address bus.
AD0-AD7	A11	Microprocessor address/data input/outputs.
AUP0-15	A11	16 bits address bus output from microprocessor.
ADC0-11	A11	12 bit address bus from the DISPLAY counter.
ADC00-7	A11	ADC output bits 0...7.
APC0-11	A11	Address pretrigger counter bits 0...11.
AUPB0-11	A11	12 bit system address bus.
AUTO	A5-S2A	Signal from AUTO switch.
AUXCHN	A11	AUXCHN signal from the microprocessor, indicating that the 4-channel mode is active.
AVSB-$\overline{\text{AVSB}}$	A11	A versus B. Active in X=A/Y=B mode.
AWC0* AWC1* AWC2*	A11 A11 A11	Write counter address bits 0, 1 and 2, directly derived from the signals AWC0, AWC1 and AWC2.
AWC0-11	A11	Address write counter bus output bits from the WRITE counter.
BUSY	A11	Busy signal from the ADC that indicates that the ADC is converting the T&H output signal into an 8-bit digital number.
$\overline{\text{CEP}}$	A11	Chip enable selection signal for the 8155 (RAM+I/O PORTS+TIMER) from address decoder. For addresses 6000H-7FFFH.
CHANBON	A9	Channel B ON. Signal from the microprocessor, indicating that channel B is switched on.
CHOP1	A11	Chopper signal 1.
CHOP2	A11	Chopper signal 2.
CLADC	A11	Clock signal for the ADC.
CLEAR	A304-S20	Signal from pushbutton CLEAR.

Signal	Generated on unit	Description
CLK 2,5 MHz	All	2,5 MHz clock output signal from the microprocessor.
CLWC	All	Clockpulse for the WRITE counter. The WRITE counter is increased by one with CLWC.
CM0	A5-S1	Signal from vertical display mode switch.
CM1	A5-S1	Signal from vertical display mode switch.
CM2	A5-S1	Signal from vertical display mode switch.
CML0	All	Signal derived from CM0.
CML1	All	Signal derived from CM1.
CML2	All	Signal derived from CM2.
CNTUP	All	Count up pulses for the DISPLAY counter.
COMPARE	A304-S22	Signal from pushbutton COMPARE.
CQ CR CS CT	All All All All	Command signals from the microprocessor for the different display modes. single channel dual channel aux channel
CTB-$\overline{\text{CTB}}$	All	Clockpulse for time-base dividers.
CONTC0	All	Control counter output bit 0.
CONTC1	All	Control counter output bit 1.
CONTC2	All	Control counter output bit 2.
CONTC3	All	Control counter output bit 3.
D0-7	All	8 bit system data bus.
D0'-D7'	All	Adder input bits.
D0"-D7"	All	Adder input bits.
$\overline{\text{DAT}}$	All	Data selection signal from address decoder. For addresses 2000H-3FFFH.
$\overline{\text{DATUPC}}$	All	Data selection signal from address decoder. (Only active under microprocessor control).
$\overline{\text{DIGCH}}$	All	Digital channel selection signal in MEMORY ON mode. DIGCH=0, when 2 or 4 channel mode is selected.

Signal	Generated on unit	Description
DIR-$\overline{\text{DIR}}$	A11	Signal indicating that the DIRECT-mode is active.
DT	A11	Display timing pulse.
DUAL OUT	A11	Signal from the microprocessor indicating that DUAL SLOPE is active.
$\overline{\text{DUAL IN}}$	A3-S32	Signal from DUAL SLOPE switch.
DUP0-7	A11	8 bit multiplexed Data-Address bus output from microprocessor.
DUP 2	A11	Data/address line 2 used as enable display signal.
DUP3	A11	Data/address line 3 used as enable trigger signal.
EINP-$\overline{\text{EINP}}$	A11	End input. Signal to indicate the end of a display memory write cycle.
EXTCL	A11	Signal indicating that the EXTERNAL CLOCK-mode is active.
EXT CLOCK	A11	Signal from EXT CLOCK input socket X6.
HOCOND	A11	Hold and convert pulse in DIRECT-mode.
HOCONS	A11	Hold and convert pulse in SAMPLING-mode.

HOCONSE HOCONSE	A11	Hold and convert pulse in SAMPLING- and EXT CLOCK-mode.
HOCONDSE	A11	Hold and convert pulse in DIRECT-, SAMPLING- and EXT CLOCK-mode.
$\overline{\text{HOLDOFF}}$	A11	Hold off signal for PRE TRIGGER counter.
HOLD OFF IN	A5	Input hold-off signal for the hold-off logic.
HOLD OFF OUT	A11	Output hold-off signal from the hold-off logic.
HTRG	A11	Auxiliary trigger signal (help trigger).
$\overline{\text{INT}}$	A14(option)	Interrupt signal from IEEE option.
$\overline{\text{IO8}}$	A11	Address decoding signal from address decoder. For addresses 8000H-9FFFH.
$\overline{\text{IOA}}$	A11	Address decoding signal from address decoder. For addresses A000H-BFFFH.

Signal	Generated on unit	Description
$\overline{\text{IOC}}$	A11	Address decoding signal from address decoder. For addresses C000H-DFFFH.
$\overline{\text{IOE}}$	A11	Address decoding signal from address decoder. For addresses E000H-FFFFH. (For IEEE).
$\overline{\text{IORD8}}$	A11	Input/output read 8. Address decoding signal for the input shiftregister.
$\overline{\text{IOWR8}}$	A11	Input/output write 8. Address decoding signal for the LED-bar unit.
$\overline{\text{IOWRA}}$	A11	Input/output write A. Address decoding signal for I/O port.
$\overline{\text{IOWRC}}$	A11	Input/output write C. Address decoding signal for I/O port.
$\overline{\text{LATEN}}$	A11	Latch enable.
LDTR	A11	Latch delayed trigger. Control pulse for the pre-trigger latch.
LEDBCL	A11	LED-bar clocksignal.
$\overline{\text{LOADS}}$ LOADS	A11 A11	Load signal for loading the WRITE counter.
$\overline{\text{LOADPC}}$	A11	Load signal for the PRE TRIGGER counter.
LOCK	A304-S21	Signal from pushbutton LOCK.
LTXT	A11	Textplate load signal for the input shiftregister to load the switch settings into the shiftregister.
LXDA	A11	Latch signal for X-DAC.
LYDA1	A11	Latch signal 1 for Y-DAC.
LYDA2	A11	Latch signal 2 for Y-DAC.
MEMDUMP	A305-S31	Signal from pushbutton MEMDUMP.
MIN/MAXI	A305-S28	Signal from pushbutton MIN/MAX.
MIN/MAX	A11	MIN/MAX signal from the microprocessor, indicating that the MIN/MAX mode is active.
$\overline{\text{MIP}}$	A10	Maximum peak detector.

Signal	Generated on unit	Description
$\overline{\text{MAP}}$	A10	Minimum peak detector.
$\overline{\text{MUX}}$	A11	Multiplexer control pulse to select the WRITE counter or DISPLAY counter.
MUX	A11	
NDRL	A11	New data ready latch. This signal indicates that a new signal sample is converted from analog to digital and can be stored in the PRE-TRIGGER memory.
$\overline{\text{OE}}$	A11	Output enable signal for PRE TRIGGER memory.
$\overline{\text{OEDM}}$	A11	Output enable display memory.
OFF	A11	Signal from pushbutton OFF.
P0-7	A11	Pretrigger memory input/output data bits 0...7.
PRETRIG	A305-S25	Signal from pushbutton PRETRIG.
PRTR0	A11	Pretrigger signals 0, 1 and 2 from the microprocessor for the presetting of the length of the pretrigger memory.
PRTR1	A11	
PRTR2	A11	
$\overline{\text{QDR}}$	A11	Active "low" in DISPLAY QUART - mode.
QUART	A305-S23	Signal from pushbutton DISPLAY QUART.
RC0	A11	Ripple carry signal 0 from the first WRITE counter ic.
RC1	A11	Ripple carry signal 1 from the second WRITE counter ic.
RCMSB	A11	Ripple carry signal from the most significant bit of the last WRITE counter ic.
RD-$\overline{\text{RD}}$	A11	Read-mode signal.
RDUP-$\overline{\text{RDUP}}$	A11	Read signal from microprocessor.
RESET	A304-S19	Signal from pushbutton RESET.
RESDET	A11	Reset detector signal for peak detectors.
$\overline{\text{RESIN}}$	A11	Reset input signal for the microprocessor.
RESUP	A11	Reset output signal from microprocessor. Used for reset of the 8155 and the IEEE option.

Signal	Generated on unit	Description
$\overline{\text{ROM0}}$	A11	Read only memory 0. Selection signal from address decoder. For addresses 0000H-1FFFH.
$\overline{\text{ROM1}}$	A11	Not used in this instrument.
RT1-$\overline{\text{RT1}}$	A11	Read timing signal 1.
RT2-$\overline{\text{RT2}}$	A11	Read timing signal 2.
RW	A11	Read/write timing signal. If RW= 0, then read action. If RW= 1, then write action.
SALT	A11	Sequential alternating.
SEQWC	A11	Sequential write counter. SEQWC= 0 --> DIRECT and SAMPLING I - mode. SEQWC= 1 --> SAMPLING II - mode.
SINGLE	A304-S18	Signal from pushbutton SINGLE.
$\overline{\text{SHAR}}$	A304-S17	Store hardware signal from pushbutton MEMORY ON.
SHAR	A304-S17	
SHROUT	A11	Shift register output signal containing the settings of the frontpanel switches.
SMOOTH	A305-S30	Signal from pushbutton SMOOTH.
SOD	A11	Serial output data signal. Used as software trigger signal for service routine.
STA	A11	Step A
STB	A11	Step B
STC	A11	Step C
STAD0	A11	3 L.S.B.'s } Start address display counter.
STAD1	A11	
STAD2	A11	
STAD9	A11	3 M.S.B.'s } Start address display counter.
STAD10	A11	
STAD11	A11	
STADC	A11	Start signal for the ADC.
$\overline{\text{STORE}}$	A304-S17	Logic signal derived from the MEMORY ON switch.
STORE	A304-S17	
$\overline{\text{SYNCH}}$	A11	Synchron/asynchron signal from the microprocessor.

Signal	Generated on unit	Description
T0	All	Count inputs for WRITE counter ic's.
T1	All	
T2	All	
TB2	A3-S10	Signals from the TIME/DIV switch.
TB3	A3-S10	
TB4	A3-S10	
TB5	A3-S10	
TB6	A3-S10	
TB7	A3-S10	
TBC	All	Time-base setting signal C.
TBD	All	Time-base setting signal D.
TBT	All	Time-base setting signal T.
THOUT	All	T&H output signal.
TIME/DIV	A305-S26	Signal from pushbutton TIME/DIV.
TIMER IN	All	Timer input signal from digital time-base circuit.
TIMER OUT	All	Timer output signal for digital time-base circuit.
TI9	All	End of quarter in DISPLAY QUART mode.
TR-$\overline{TR}$	All	TRACK control signals for T&H circuit.
$\overline{TRACK}$	All	TRACK command for the T&H circuit.
TRACK	All	TRACK= 0 --> Hold TRACK= 1 --> Track
TRAUT	All	Trigger automat signal.
TRGRD	All	TRIGGERED. Indication that triggerpulses are generated in the trigger circuit.
TRIG	All	Trigger signal from the trigger circuit.
$\overline{TRIGL}$	All	Trigger latch signal indicating that a trigger signal is latched.
TRIGL	All	
TRRES	All	Trigger reset signal.
TRSHXY	All	Track and hold signal.
TZRD	All	Timing Z-pulse in read mode.
$\overline{UPCONT}$	All	Microprocessor control signal.
UPCONT	All	
VREF	All	Reference voltage for the ADC.

Signal	Generated on unit	Description
$\overline{\text{WEDSP}}$	A11	Write enable display pulse for the display memory, generated by the memory write logic and functions also as a clockpulse for the WRITE counter.
$\overline{\text{WEPTR}}$	A11	Write enable pretrigger pulse for the pre-trigger memory and clockpulse for the PRETRIGGER counter, directly derived from each NDRL pulse.
WR	A11	Write timing signal.
$\overline{\text{WRUP}}$	A11	Write signal from microprocessor.
X=A/Y=B	A305-S29	Signal from pushbutton X=A/Y=B.
X DAC	A11	Horizontal digital to analog converter output signal.
XDACI0- XDACI11	A11 A11	Horizontal digital to analog converter input signals.
YDAC	A11	Vertical digital to analog converter output signal.
ZAB	A11	Z-pulse for A versus B mode.
ZDTCRT	A11	Z-pulse for display timing.
ZEN	A11	Z enable pulse.
ZRD-$\overline{\text{ZRD}}$	A11	Z-pulse in read.
ZMOD	A11	Z mode pulse. Blanking/unblanking pulse in STORE mode.
Ground		
+ 5V		
+ 12V		
- 12V		
20 MHz	A11	20 MHz output signal from oscillator.

12. ACCESSORIES

12.1. ACCESSORIES SUPPLIED WITH THE INSTRUMENT

12.1.1. 10:1 Passive probe PM 8927A

The PM 8927A is a probe with an attenuation factor of 10, designed for real-time oscilloscopes up to 100 MHz, with BNC input jack and input resistance 1 Mohm. The cable length of this probe is 1,5 m.

Characteristics
==========

Electrical

Attenuation	10x ± 2% (oscilloscope input 1 Mohm).
Input resistance d.c.	10 Mohm ± 2% (oscilloscope input 1 Mohm).
a.c.	See graph FIG. 12.1.
Input capacitance d.c. and l.f.	11pF ± 1pF (oscilloscope input 1 Mohm ± 5% paralleled by 25pF ± 5pF).
Input reactance h.f.	See graph FIG. 12.1.
Useful bandwidth	See graph FIG. 12.3.
Maximum rated input voltage	500Vd.c. + a.c.peak, derating with frequency. See FIG. 12.2. Oscilloscope input 1Mohm and voltage applied between probe tip and earthed part of probe body. Test voltage 1500Vd.c. for 1 s. at a temperature between 15 and 25°C, a rel. hum. of 80% at maximum and at sea level.
Check-zero button probe shell	Same function as 0 position of input coupling switch on oscilloscope.
Compensation range	14 ... 40pF (input capacitance of oscilloscope).

Environmental

Probe operates within specification over the following ranges:

Temperature	-25°C to +70°C
Altitude	Up to 5000 metres (15000 feet)
Other environmental data	Same as for any PHILIPS oscilloscope the probe is used with.

Mechanical

Dimensions	Probe body 103 mm x 11 mm dia (max.) Cable length 1500 mm. Correction box 55 x 30 x 15 mm incl. BNC
Mass	Incl. standard accessories 140 g.

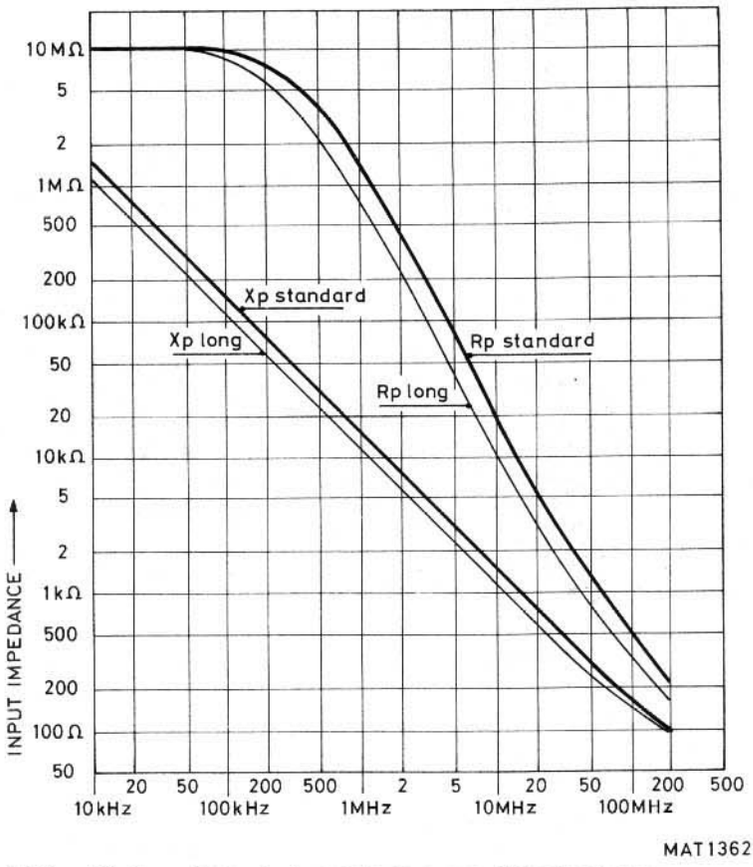


FIG. 12.1. Input impedance vs frequency.

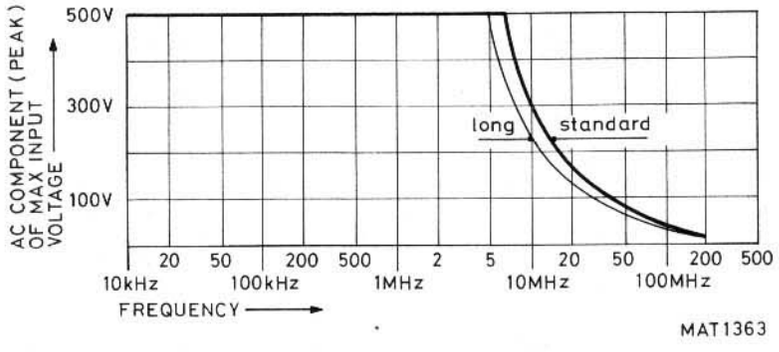


FIG. 12.2. a.c. component (peak) of maximum rated input voltage vs frequency.

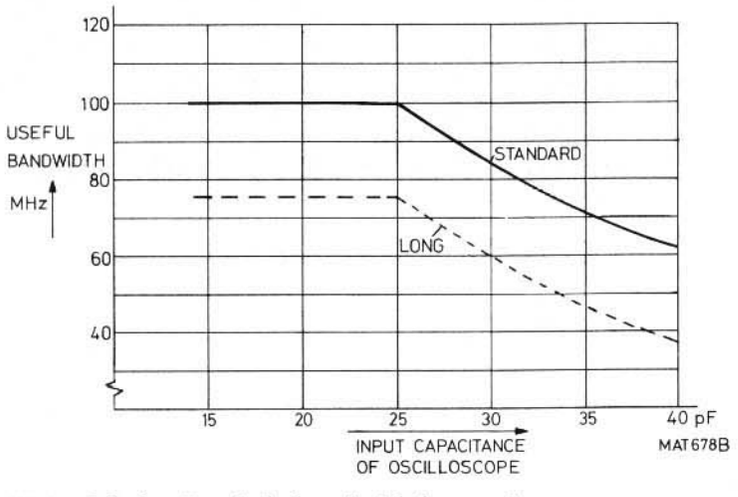


FIG. 12.3. Useful bandwidth vs frequency.

12.1.2. Matching the probe to your oscilloscope

The measuring probe has been adjusted and checked by the manufacturer. However, to match the probe to your oscilloscope, the following procedure is necessary.
Connect the measuring pin to the CAL socket of the oscilloscope.
A trimmer can be adjusted through a hole in the compensation box to obtain optimum square-wave response. See FIG. 12.4. , 12.5. and 12.6.

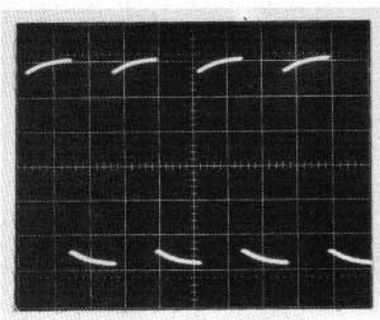


FIG. 12.4.
Under-compensation

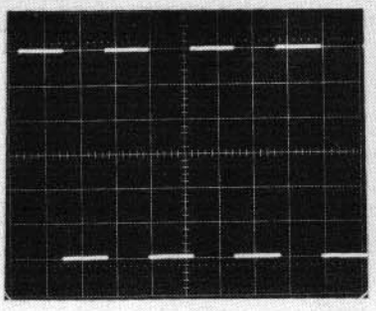


FIG. 12.5.
Correct compensation

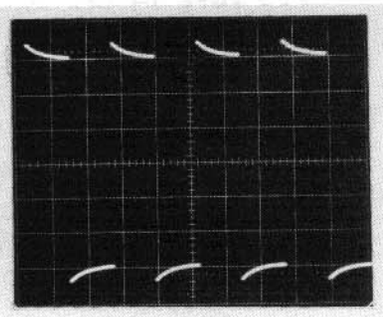


FIG. 12.6.
Over-compensation

12.1.3 Adjusting the h.f. step response

The h.f. step response correction network has been adjusted by the manufacturer to match an average oscilloscope input. For optimum pulse response, however, the probe can be adjusted to match your particular oscilloscope. Later adjustment is only necessary if the probe is to be used with a different type of oscilloscope, or after replacement of an electrical component.
For the adjustment, proceed as follows:
Connect the probe to a pulse generator (rise time not exceeding 1 ns) which is terminated by its characteristic impedance. Dismantle the compensation box as is described in section 12.1.5. Set the generator to 100 kHz. Adjust R2 and R3 alternatively to obtain a display as shown in FIG. 12.7. It is important that the leading edge is as steep, and the top is as flat, as possible. Incorrect settings of R2 and R3 five a rise to pulse distortions as shown in Fig. 12.8. and 12.9.

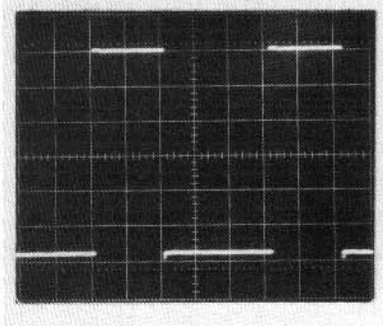


FIG. 12.7.
Preset potentiometers correctly adjusted

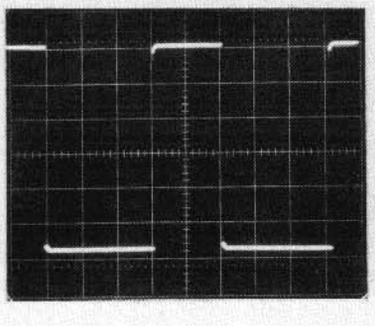


FIG. 12.8.
Rounding due to incorrectly adjusted potentiometers

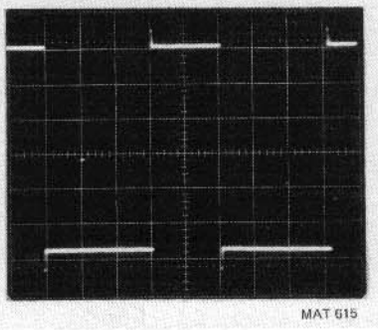


FIG. 12.9.
Overshoot due to incorrectly adjusted potentiometers

12.1.4. Dismantling the probe (See FIG. 12.7)

The front part 11 af the probe can be screwed from the part 13. Item 11 can be slid from 12 and 13. The RC combination part 12 is soldered to 13. For replacement of 12 refer to the next section.

12.1.5. Dismantling the compensation box (See FIG. 12.7)

Unscrew the ribbed collar of the compensation box to the cable. The case 14 can be slid sideways off the compensation box. The electrical components an the printed wiring board are accessible now.

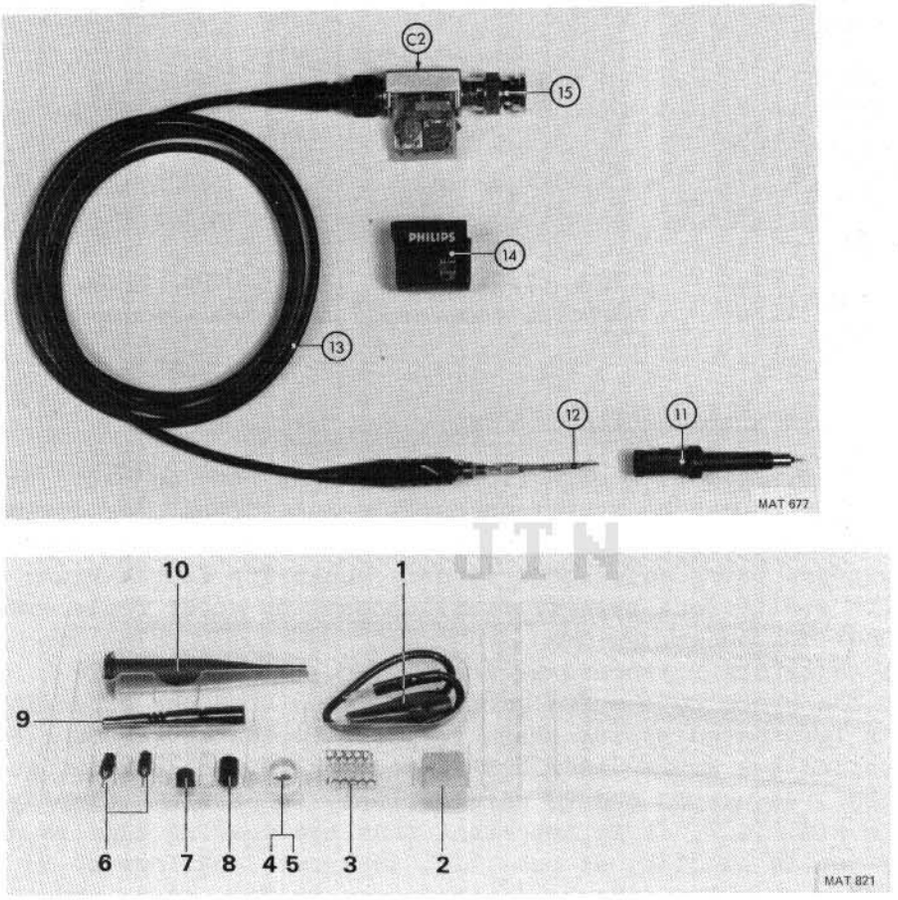


FIG. 12.10. Dismantling and accessories

12.1.6. Replacing parts

12.1.6.1. Assembling the probe:

A new RC network is slid over the cable nipple, after which the cable core is soldered on to the resistor wire. When the measuring probe is assembled, the RC network must be at dead centre in the probe tip.

12.1.6.2. Replacing the cable assembly:

Dismantle the compensation box.
Unsolder the connection between the inner conductor and the printed wiring board. Keep the frame of the compensation box steady and loosen the cable nipple with a 5 mm spanner on the hexagonal part. Replace the cable and and fit it, working in the reverse order.

12.1.6.3.Replacing the BNC:

Dismantle the compensation box.
Unsolder the connection to the printed wiring board. Hold the frame of the compensation box firmly and loosen the BNC with a 3/8 inch spanner. Replace the BNC and fix it, working in the reverse order.

12.1.6.4.Replacing the probe tip

The damaged tip can be pulled out by means of a pair of pliers. A new tip must be firmly pushed in.

12.1.7. Parts list

12.1.7.1.Mechanical parts (See FIG. 12.7 and 12.8)

Items 1 to 10 are standard accessories and are supplied with the probe.

Item	Ordering number	Qty	Description
1	5322 321 20223	1	Earth cable
2	5322 256 94136	1	Probe holder
3	5322 255 44026	10	Soldering terminals which may serve as a test pin in circuits
4/5	5322 310 34134	6	Set of six marking rings
6	5322 268 14017	2	Probe tip
7	5322 562 44319	1	Insulating cap
8	5322 462 44318	2	Insulating cap fir DIL measurements
9	5322 462 24019	1	Wrap pin adaptor
10	5322 264 24019	1	Spring-loaded test clip
11	5322 264 24021	1	Probe shell with check-zero button
12	5322 216 54152	1	RC network
13	5322 320 14063	1	Cable assembly
14	5322 447 61006	1	Cap
15	5322 268 44019	1	BNC connector

12.1.7.2.Electrical parts

Item	Ordering code	Qty	Description
C1	-	1	Part of RC network (not seperately supplied)
C2	5322 125 54003	1	Trimmer 60 pF, 300 V
R1	-	1	Part of RC network (not seperately supplied)
R2	5322 101 14047	1	Potmenter 470 Ohm, 20%, 0,5 W
R3	5322 100 10112	1	Potmeter 1 kilo Ohm, 20%, 0,5 W

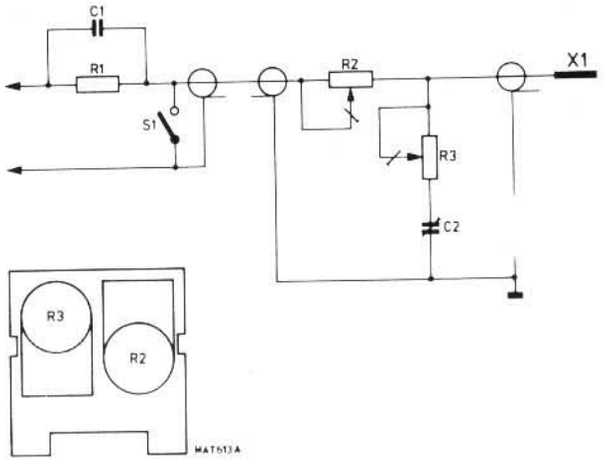


FIG. 12.11. Printed wiring board showing adjusting elements, circuit diagram.

12.2. ACCESSORY INFORMATION FOR OPTIONAL ITEMS

12.2.1. IEEE-488 BUS - interface PM 8955.

JTN

General
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The PM 8955 option is a general-purpose bus interface, in according with the IEEE-488 standard, for use with the PM 3305 Oscilloscope.

This option enables the oscilloscope to be used in a measuring system together with other IEEE BUS-compatible instruments.

For more detailed operating information refer to the separate booklet of the PM 8955.

For installation instructions see information delivered with the PM 8955.

For spare parts see chapter 9.3. in this manual.