Service Manual

H 52380-900E
Vol. 2

Spectrum Analyzer
Display Unit
2380

Code No. 52380-900E

AMENDMENT RECORD

The following amendments are incorporated in this manual.

Amendment No.	Date	Issued at Serial number prefix
-	June 86	152027

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CONTENTS

HAZARD WARNING SYMBOLS

The following symbols appear on the equipment:

Symbol	Type of hazard	Reference
⚠	Static sensitive device	Page (iv)
⚠	Dangerous voltages present	Page (iii)
⚠	Supply voltage	Page (iii)

Note ...

Each page bears the date of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ▶ .... ◀ to show the extent of the change. When a chapter is reissued the triangles do not appear.

Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

NOTES AND CAUTIONS

ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus', and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers ⚠

Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be allowed to discharge through the bleed resistors fitted for the purpose; do not attempt to remove the safety covers from the power supply until the lamp under the top cover stops blinking. Should the unit be reconnected to the supply with the safety covers removed then disconnected, do not attempt to discharge the power supply unit's main reservoir capacitors using a shorting link as the equipment may be damaged. Discharge should always be allowed to occur gradually.

Note also that the 12 kV e.h.t. circuit for the cathode ray tube retains its charge for a considerable time after switch off. Therefore before any handling is carried out in the vicinity of the cathode ray tube or e.h.t. unit it is essential that the supply is disconnected from the instrument and the final anode lead is shorted to the chassis several times immediately after unplugging. The residual charge on the c.r.t. itself must also be removed by shorting the anode connection to ground.

AC supply plug ⚠

The supply plug shall only be inserted in a socket outlet provided with a protective ground contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

Fuses - primary and secondary

Note that there is a supply fuse in both the live and neutral wires of the supply lead. If only one of these fuses should rupture, certain parts of the equipment could remain at supply potential.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided. A number of secondary fuses are fitted to boards in the upper and lower units. For details of both primary and secondary fuses, refer to Performance data in the Operating Manual.

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol ⚠ on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange disks, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disk or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with a grounded conductive surface.

Metallic tools grounded either permanently or by repeated discharges.

A low-voltage grounded soldering iron.

A grounded wrist strap and a conductive grounded seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

(4) If using a freezer aerosol in fault finding, take care not to spray programmable ICs as this may affect their contents.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

Cathode ray tube. When exposing or handling the tube take care to prevent implosion and possible scattering of glass fragments. Handling should only be carried out by experienced personnel and the use of a safety mask and gloves is recommended. A defective tube should be disposed of in a safe manner by an authorized waste contractor.

WARNING : TOXIC HAZARD

Many of the electronic components used in this instrument employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

RADIO FREQUENCY INTERFERENCE

This equipment conforms with the requirements of IEC Directive 76/889 as to limits of r.f. interference.

LOGIC MNEMONICS USED IN THE LOGIC SECTION

A OR A-B SEL	A OR A-B trace SEL
ADSR	A channel Display Shift Register
AVG	A Video Generator
B SEL	B trace SELect
BDC	B Data Comparator
BDML	B DeMultiplex Latch
BDSR	B channel Display Shift Register
BVG	B Video Generator
COL	Current Ordinate Latch
DACK1	Direct memory access ACKnowledge 1
DDM	Data Display Mask
DIV H	DIVIDE Higher bit
DIV L	DIVide Lower bit
DMA	Direct Memory Access
DMARL	Direct Memory Access Request Latch
DREQ 1	Direct memory access REQuest 1
DRQ	Direct memory access ReQuest
DRQ 1	Direct memory access ReQuest 1
DSR	Display Shift Registers
EOC	End Of Conversation
ERSD	Even Row Start Detector
ESPG	Extra line Sync Pulse Generator
ESTB	Extra Sync Trigger Bistable
GCHM	Gated Clock & Horizontal Mask generator
GDSR	Graticule Display Shift Register
HRTC	Horizontal ReTraCe
HRTCS	Horizontal RetraCe Sync
HSTB	Horizontal Sync Trigger Bistable
HSYNC	Horizontal SYNC
IOW	Input/Output Write
LCVM	Line Count & Vertical Mask generator
MPY	Multiply
SDA	Spectrum Display Area
VML	Vertical Mask Latch
VRTC	Vertical ReTraCe
VRTCS	Vertical ReTraCe Sync
VSYNC	Vertical SYNC
WD	Write Display
WE	Write Even
WO	Write Odd
WPG	Write Pulse Generator
XV1DEN	Y VIDeo ENable
YVIDEN	Y VIDeo ENable

Chapter 4-2

TECHNICAL DESCRIPTION

CONTENTS

INTRODUCTION

1. The following description should be read in conjunction with the appropriate diagrams in this chapter and with the circuit diagrams in Chap. 7. The circuits are summarized in paras. 3 to 8 and then described in detail in the paras. that follow.

2. The spectrum analyzer comprises one or more lower units containing the frequency synthesizer plus a common upper unit described in this volume containing the display and power supply. Communication is via a two-way serial 9600 baud 20 mA current loop for housekeeping data whilst a one-way high speed serial link is used for the display data. The upper unit's power supply will power up to two lower units with only one selected at any one time. The lower units are internally wired to be self-addressing, therefore any configuration of units may be controlled via the front panel or remotely via a single GPIB socket as if it were a single instrument.

CIRCUIT SUMMARY

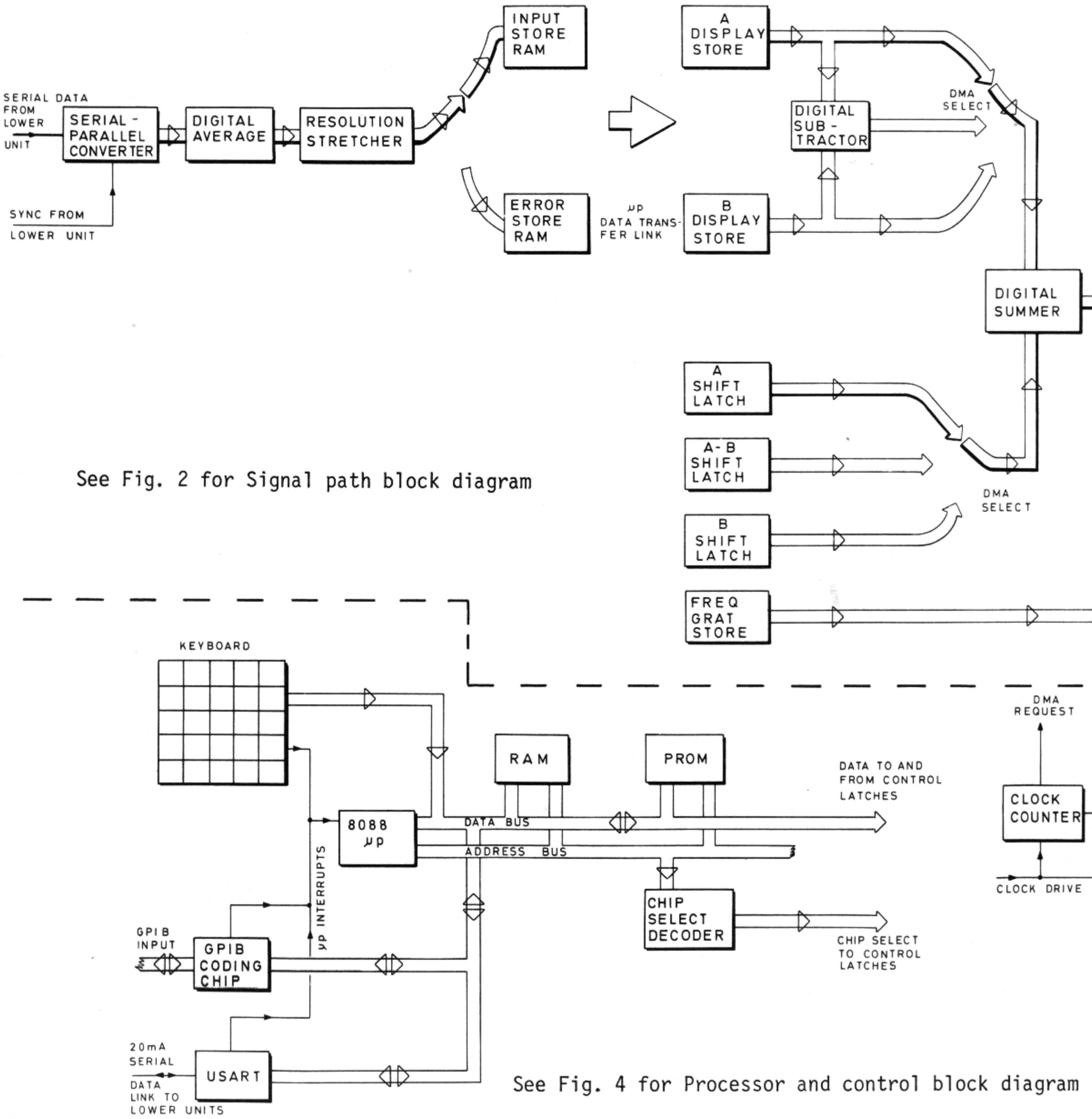
Signal path, display, pen plot & RGB video

3. The serial data input from the selected lower unit at the 2.5 MHz bit rate (see Fig. 1) is converted to 16-bit parallel data and is subjected to a running digital averaging process to simulate the customary video filter. A normal analogue RC network is inappropriate since, due to the inclusion of the high resolution switched gain logarithmic amplifier, no full range detected analogue signal exists anywhere in the system.

4. Since the final stored picture has a resolution of 500 slots across the displayed frequency span, it is necessary to ensure that any spectral responses less than one slot wide do not get missed or attenuated. The Resolution Stretcher is designed to do this whilst at the same time not exaggerating the noise level, as a simple peak hold circuit would do.

5. The processed data word is now transferred under Direct Memory Access (DMA) control to RAM space dedicated as Input Store or Error Store depending on whether the current sweep is a measurement scan or a calibration scan. The data in these two stores is now selectively subtracted (the data space in the Error Store permits correction over the range 100 Hz to 400 MHz) and loaded into the appropriate dedicated RAM spaces known as A Store and B Store under microprocessor control.

6. Each Display Store shift register contains 500 bytes representing the data for the currently displayed image. These data can be used to produce an infilled display or an outlined display depending on the option selected. On the completion of each horizontal scanning line (one complete recirculation of data in the shift register), the Clock Counter generates a DMA request. This results in a DMA transfer of a single display slot of data from the appropriate Display Store to the appropriate shift register. During this transfer the 16-bit word in the Display Store is added to the 16-bit word in the Shift Latch to arrive at the correct vertical display value and is then subject to the correct hardware multiplication to give the selected scaling factor before the 8 bits appropriate to the selected display range are loaded into the recirculating shift register. The output from the shift register is used to produce a solid (infilled) display or is subjected to further line draw processing to produce an outlined display. The resulting signal is then mixed with the graticule and character symbol data before being applied to the video amplifier and thence to the c.r.t.

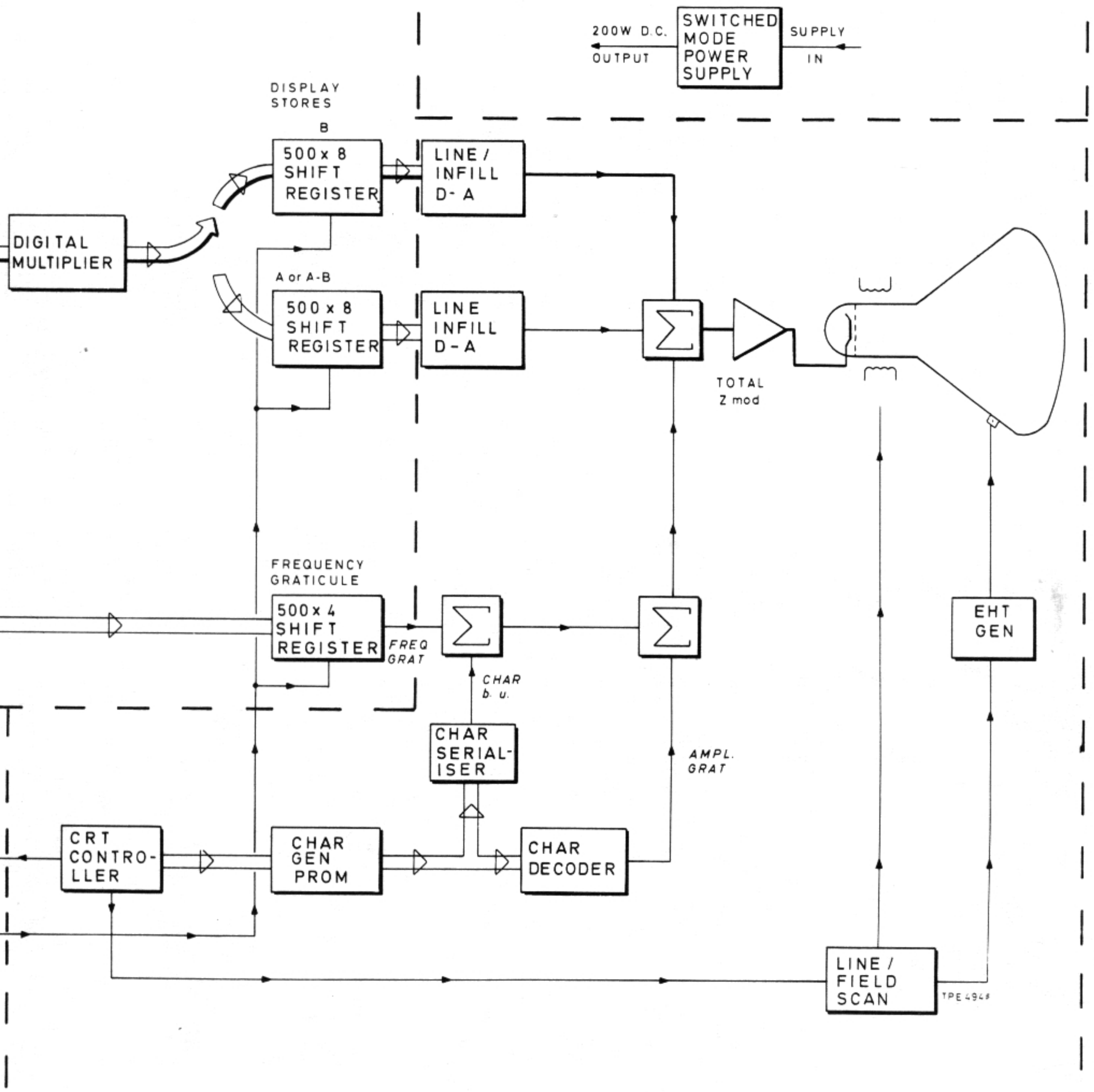


See Fig. 2 for Signal path block diagram

See Fig. 4 for Processor and control block diagram

Block schemati

See Fig. 8 for Power supply block diagram



See Fig. 3 for Display block diagram

7. The frequency graticule data and marker data are similarly refreshed, two bits being used for Graticule brightness information and two bits being used for Steady or Flashing Markers.

8. The c.r.t. controller chip organizes the display drive waveforms and also drives the character generator EPROM to annotate the graticule and display mode status information. The first character of each line is used as a control character and is suppressed, decoded and used to generate the amplitude graticule. Thus the graticule for both axes is under microprocessor control and may draw in any type of ruling to suit the needs of the display.

9. An optional board supplies the drives for the x and y axes of a pen recorder, as well as RGB outputs for use with a colour monitor and a composite video output for a monochrome monitor.

Processor and control

10. Front panel controls are serviced via microprocessor interrupt procedures. Additionally, the processor shares the data and address buses with a DMA controller to allow direct memory access to selected peripherals. All system switching, control and flag reads are done via a two-way buffer on the microprocessor bus. In this way, bus wiring is free from the continuous data train of pulses on the normal microprocessor bus thus reducing the possibility of interference to the analogue circuits. Housekeeping data between the processor and the r.f. units is conveyed by 20 mA current loop. The GPIB interface housed in the display unit allows the spectrum analyzer to form part of a system acting under the direction of a controller.

Power supply

11. Besides powering the display unit, the power supply supplies one r.f. unit on full power and a second on standby power. The switched mode power supply controller operates in synchronism with the associated r.f. unit's frequency standard. The controller shorts down to provide protection against overload, overvoltage or overheat conditions while rear panel l.e.d's illuminate to warn of overvoltage, undervoltage and overload as well as to indicate when no r.f. unit is connected.

SIGNAL PATH

12. The signal path block diagram is shown in Fig. 2. Serial data for display from the r.f. unit at a 2.5 MHz bit rate and accompanied by a synchronizing pulse is applied for processing by board AB2. Only the least significant 13 bits of the 23-bit word are used by the r.f. unit. The data is serial to parallel converted and simultaneously averaged in a shift register. Here, up to the full 23 bits may be used for addition during the averaging process used to simulate a video filter. Synchronizing pulses are counted on AB2 to indicate to the processor when data for the next ordinate (out of the 500 displayed) is to be written into the data store, as well as indicating end of sweep, according to display mode. Maximum and minimum data latches on AB2 implement the resolution stretcher used to ensure that spectral responses less than one slot wide do not get missed. The data is next transferred under direct memory access to either the input store or the error store in RAM depending upon whether the current sweep is for data or measurement purposes. After selective subtraction, the now calibrated data is loaded into the A or B display store in RAM.

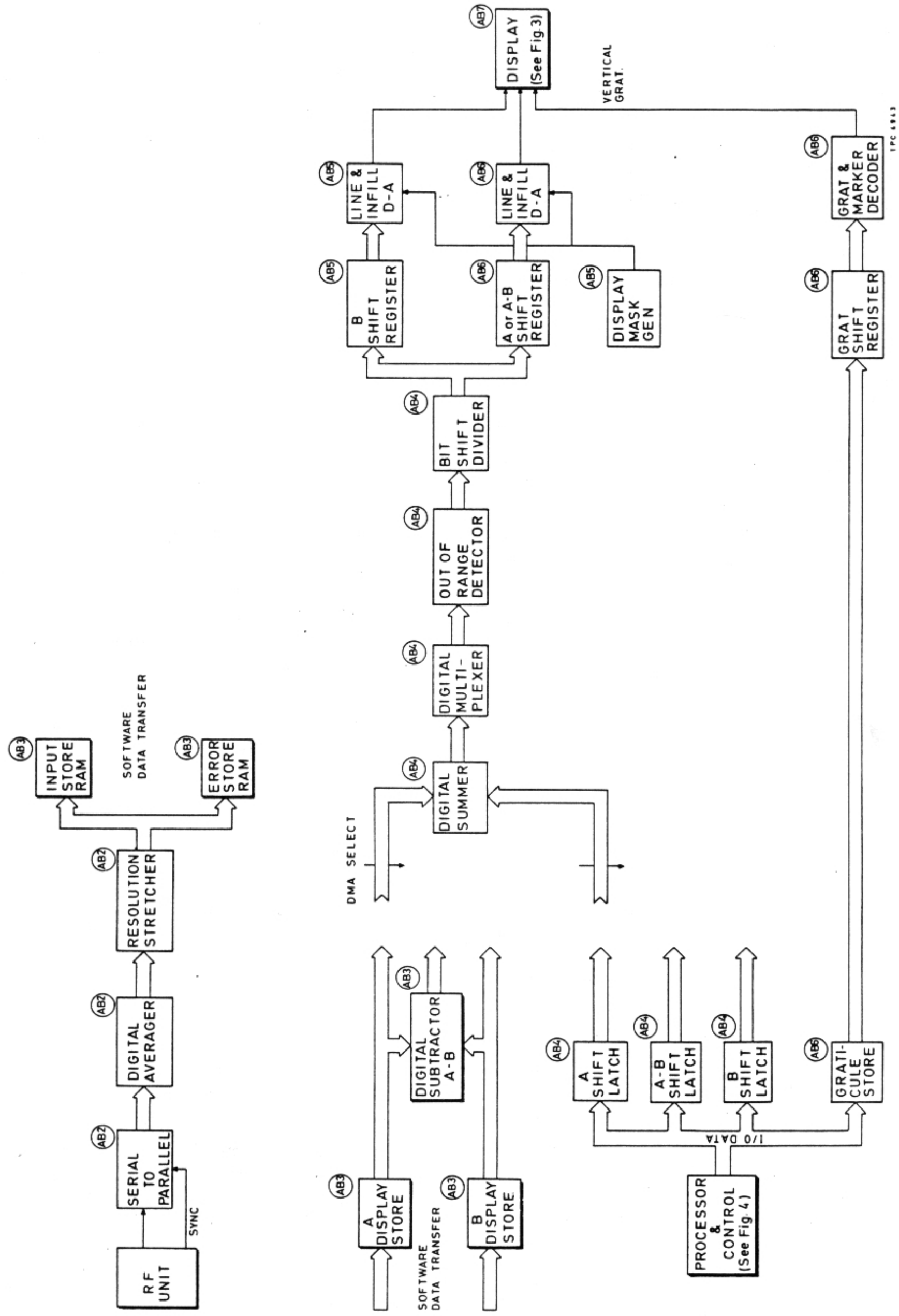


Fig. 2 Signal path block diagram showing main functions of boards

13. Data from the A store, the B store or the result of A-B is summed on AB4 with the A,B or A-B shift latch respectively to determine the vertical display position. A x1 or x5 multiplier on AB4 provides the required scaling factor. The following bit shift divider, responding to controls such as for reference level, operates in conjunction with out of range detectors. The B data is fed to AB5 while the A or A-B data together with the graticule data is fed to AB6.

14. 8-bit data for each of 502 ordinates is held in Display Shift Registers (DSR) on boards AB5 and AB6. The A store DSR on AB6 holds either A or A-B data, while the graticule DSR on the same board holds 4-bit data for the vertical graticule lines (horizontal line data is processed on AB7). All shift registers are recirculating to enable the data to be read non-destructively in byte serial form. Each circulation represents one horizontal display scan. At each ordinate position, the 8-bit display data is decoded to determine which picture elements are to be lit up to provide the selected infilled or outlined display. In the case of the graticule, the elements are lit up to form the vertical line when the scan reaches the appropriate position. The 4-bit graticule data in fact contains both graticule and marker information, 2 bits are decoded to define a major, minor, dashed or no graticule line, while the remaining 2 bits are used for steady or flashing marker selection.

15. Clock generators on AB5 control the operation of the shift registers on both AB5 and AB6, as well as providing the horizontal and vertical masks used for screen blanking to prevent spurious data from appearing outside the 502 x 250 element display area. Outputs for the different displays are taken to the video mixer on AB7.

Board AA1 - Mother board &
Board AA2 - Auxiliary connector

Circuit diagrams : Chap. 7, Figs. 4,5 & 14

16. Mother board AA1 connects together eight 60-way 2-side edge connectors and five smaller connectors. The eight hold the main logic boards, AB1 to AB8. The backplane behind them consists of two sets of bused signal lines and an area of daisy-chained lines. The bused signals are common to many of the boards, e.g. power rails, data bus, processor read and write signals and clock signals. The daisy chain area is used to connect 'private' signals between adjacent boards. Included in the bused signals are some which will allow expansion at a later date, mainly on the options board AB8. Examples of this are colour video output and the addition of a second interrupt controller.

17. The small connectors on AA1 are as follows : PLA is used to transfer signals from the backplane to the lower unit via the data connector on the rear panel. PLB connects the backplane to the INTENSITY controls and the SUPPLY ON l.e.d. on the front panel. PLC connects the main power rails from the power supply to the backplane. PLD connects some signals and the minor power rails from the power supply to the backplane. SKJ connects the TV unit to the backplane.

18. Auxiliary connector AA2 transfers some 'private' signals between AB5 and AB6, there being too many to fit in the daisy-chain area of the mother board alone.

Board AB2 - Input signal data processing

Circuit diagrams : Chap. 7, Figs. 8 & 9

19. The circuit of AB2 can be split into two major blocks, following roughly the same break line as the two sheets of the circuit diagrams. The first section deals with the gathering of the data from the lower unit, which is in serial form, and producing a parallel data word. In this section of the circuit the data is averaged. There is also a number of ICs employed in the synchronization of the serial to parallel conversion, and the calculation of the Ordinate Rate, which is the rate at which data is input to the data stores of the analyzer.

20. The second section of the circuit includes a maximum and a minimum detector which acts on the parallel data word produced by the averaging process in the first part of the circuit. An algorithm is used to determine which of the two detectors is used as the source of data which will be stored in the data stores.

Parallel to serial conversion and averaging

21. The data from the lower unit is sent in a serial format and is packaged as a 23-bit word every 10 ms at a 2.5 MHz bit rate. Only 13 of the bits are used by the lower, r.f. unit, and occupy the least significant 13 bits of the 23-bit word. The least significant bit is sent first. To enable the data to be synchronized as it arrives from the lower unit, an END OF CONVERSION pulse is provided by the r.f. unit. This negative-going pulse arrives on a separate line. The positive-going edge marks the beginning of the first data bit.

22. The circuit based on IC30 serves to provide clock pulses that have edges about half way through each data bit period. This part of the circuit (a divide by 5) has a 2:3 mark space ratio. The divider is held in the reset state during the END OF CONVERSION synchronizing pulse, and it is clocked at a clock rate 5 times faster than the required clock frequency. In this way, the divider produces on its output a clock frequency at 2.5 MHz which is used to clock the data into the shift registers. The active edge is 2/3 of the way through the data periods.

23. As with standard serial to parallel practice, the two clock frequencies (the one clocking the data out of the lower unit, and the one clocking the data into the upper unit) need not be exactly the same, so long as the difference in frequency does not cause the clocking edges to drift outside the data bit periods. In this case, since the clock pulses may start within 1/3 of the clock period from the edges of the data periods, and there are 23 such data periods, the accuracy of the clock should be better than 1 part in 69. It is for this reason, that the difference in the master clocks of the two units (about 1 part in 400) is of no consequence since both master clocks are crystal controlled and phase locked together.

24. The actual serial to parallel conversion takes place using three 8-bit shift registers, ICs 15 to 17. The data is input via a one bit full adder. The action of this adder is to add together the incoming data with the data which is being shifted through the shift registers. By selecting the correct tap on the shift registers (the 23rd tap, since the data words are 23-bits long), the recirculated data bits will have the same bit value as the bits to which they are to be added. After two data words have been added, the value in the shift register will be twice the value of the two individual data words

(assuming both data words had the same numerical value). Hence the correct value can be obtained from the shift register by performing a one bit shift in the correct direction (a one bit shift to the right is a divide by two). If the two data words were different, then the value obtained would be the average of the two words.

25. By taking four words at a time, adding them in the same manner as above, and then performing a two bit shift, the average of four words can be obtained. Averages over other numbers of data words can also be done, but to enable simple division by the application of bit shifts, these are restricted to simple binary numbers. Since the total of the additions must be stored in the shift register until the time when the final shift/division takes place, there is a maximum number of additions that can take place before the 23 bit capability of the shift register is exceeded.

26. The controlling of the shift register, the adder and the final shift/division is achieved by the Average Clock Counter, IC20. This counter is programmed with the total number of clock pulses to be applied to the shift register. To clock in one complete word, 23 clock pulses are required. To add two words together, 46 clock pulses would be required etc. These numbers are modified by two factors: the final shift/division, and the positions of the 13-bit parallel taps. Since the taps are on the first thirteen bits of the shift register, the number of clock pulses required for the first word to appear at the output taps is only 13. However it still takes 23 pulses before it reaches the end of the shift register and is ready to be added to the next data word should this be required.

27. To allow for the final shift/division, extra pulses must be applied to the shift register to move the data through by the correct number of bits. The final division ratio becomes 23 x N - 10 + 2LOG(N), where LOG is to the base 2. This formula is derived from; 23 bits x N, where N is the number of averages of 23-bit words; -10 for the offset due to the position of the taps; and LOG(N) for the number of bits of shift to perform the correct division.

28. After the correct number of clock pulses, the output of the Average Clock Counter causes the data appearing on the shift register taps to be latched into ICs 32 and 33. At the same time the shift register is reset ready for the next average, and the pulse is passed to the second block of the circuit on the ENABLE line to signal that data is available.

29. The one bit full adder, mentioned earlier is made from separate gates. The CARRY OUT is latched from one data bit period, and applied to the carry input during the next data bit period.

30. Some very slow sweep rates using narrow filters require that the averaging be done over a period of greater than 210 data input words. This is not possible, as stated earlier, because the shift register cannot contain the total of that number of data words. However, the data words produced by such a sweep are necessarily varying at a very slow rate due to the band limiting effect of the i.f. filters, and thus two or more consecutive words cannot differ by any significant amount. Under these circumstances a proportion of the input words is lost, without any fear of losing required data. The programmable Input Word Rate Divider and the latch IC18a provide a gating signal to the STROBED 2.5 MHz clock used to clock the shift register. In this way, a gating signal is provided to extend the data averaging period by up to 216 times greater than the basic 10 microsecond sampling rate.

Clock generation

31. The Ordinate Clock Generator and the Sweep Terminator Generator are two closely related parts of the circuit. During normal (swept linear frequency) scans, the incoming END OF CONVERSION pulses are counted, and a pulse is produced which signals to the processor that it is time for the next data ordinate to be written into the data stores. The END OF SWEEP pulse produced by the Sweep Terminator Generator is, on these 'normal' sweeps, a pulse produced by a division by 502 (by IC20) on the ORDINATES pulse. The division is by 502 because there are 50 ordinates in each of the 10 frequency segments across the display, and 2 more are on the last graticule line.

32. It should be noted that, although the averaging and the ordinate clocks are both derived from the same END OF CONVERSION pulses, they are not locked together; the averaging clock is a 1 2 4 8 16... division on the END OF CONVERSION pulses, and the ORDINATES clock is a 1 2 5 10 20... division on the END OF CONVERSION pulses.

33. For the Zero Span modes, the r.f. unit defines the ordinate rate and therefore the Ordinate Clock Generator division ratio must be set to one. Since this is an inadmissible division ratio for this programmable section, the divider has to be bypassed. This is done by programming its output to be high impedance, pulled to a logic 1 by the pull-up resistor, and using only monostable pulse generator IC34 to produce the 1:1 END OF CONVERSION to ORDINATES pulse ratio. The Sweep Terminator Generator still produces its pulses every 502 ordinates.

34. In the Log Scan mode, each decade is swept separately by the lower unit. Each decade sweep is used to fill 1/nth of the data stores, where n is the number of decades requested for the display. The total number of ordinates in n decades is not exactly 502 (or 500 for that matter) for all values of n, since there must be the same number of ordinates in each decade, and 500 is not divisible by 3, 6, 7 etc.

35. During these Log sweeps, the Sweep Terminator Generator is used in a different manner. It is used to create the log shaping to the frequency scale of each decade. The linear decade frequency scan produced by the lower unit is divided into ten segments. Each segment will have the same number of ordinates, but will represent a different amount of the frequency scan, the proportions being in a logarithmic ratio. The Sweep Terminator Generator is used to signal the end of each of these segments. It is programmed to interrupt the processor after the (fixed) number of ordinates in each segment. The Ordinate Clock Generator is programmed with a different number for each segment, and by using the facilities of the programmable counter, viz preselecting the next count ratio before the last count has been completed, the interrupt from the Sweep Terminator Generator need not be very high priority.

36. On Logarithmic sweeps, where the number of decades is low, the number of END OF CONVERSION pulses per ordinate is small. It is not possible to produce a good approximation to a logarithmic scan by using the same number of END OF CONVERSION pulses for each ordinate in any one segment. Since the overhead of programming the Ordinate Clock Counter differently for each ordinate is too great, a much faster clock is used so that the gradation from one segment to the next can be much finer and more exact. The clock chosen is a 2.5 MHz output from the CLOCK TICK generator prescaler IC31. It is

gated (in the programmable divider) by a signal from IC25a which starts with the first END OF CONVERSION pulse, and stops when the Sweep Terminator Generator produces its END OF SWEEP pulse.

37. Divider IC29 in this section of the circuit provides a glitch-free 6.25 MHz clock for the microprocessor and the UART; the clock produced by the 6.25 MHz phased clock generator may have glitches until the CRT generator is set up. Another divider, IC20 and IC31 produces the CLOCK TICK signal for the real time executive. The clock rate is 10 ms.

Maximum and minimum detectors

38. The maximum detector consists of the 16-bit comparator formed by ICs 9 to 12 which compares the incoming PARALLEL AVERAGED DATA with the data already stored in the Max Data Latches, IC23 and IC24. The presence of new data is signalled by the ENABLE pulse from the Averager Clock Counter. Should the new data be smaller, no action is taken, but should it be larger it is transferred to the Max Data Latches and becomes the new maximum data value. IC12 pin 5 'greater than' output is ANDed with ENABLE by IC13a and used to set max latch IC14a to show that a new maximum value has been found. If the data value did not rise above that stored in the Max Data Latches during an ordinate period, the max latch IC14a will not be set.

39. The minimum detector formed by ICs 5 to 8 works in a similar way to the maximum detector. The comparator finds the minimum values of the data, and stores them in the Min Data Latches ICs 21 and 22, setting min latch IC14b at the same time. If the data value did not fall during an ordinate period, the min latch IC14b will not be set.

Max/min select logic

40. At the end of each ordinate period, signalled by the ORDINATES pulse from the Ordinate Clock Generator, the Max/Min Latch Select Logic circuit (IC29a pin 1) and the DMA controller (DRQ Latch IC41 pin 13) are strobed. The Max/Min Select Logic operates using the algorithm described below.

41. Two of the several requirements of the spectrum analyzer display are that it should show the maximum value of any signals, and should at the same time show a reasonable representation of noise, and not just its peak and minimum values.

42. In a display where the IF filter bandwidth used is relatively wide compared with the scan width, the signal appears as a wide, rounded topped, display. Noise on the other hand would appear more ragged, and may well appear as 'grass', having a very fine amplitude v time display. During any one ordinate time period, when the analyzer is scanning through the signal part of the display, the max and min detectors, and their associated max and min latches would be detecting either a rise or a fall, but not both, since the signal amplitude is changing smoothly from one value to the next. When the scan is in the noise part of the display, it is likely that during any one ordinate period, new maximum and minimum values will be found, and both the max and the min latches will be set.

43. To form an acceptable display for this type of scan a very simple algorithm is used. When the signal amplitude is rising only, the peak detector is used. When the signal amplitude is falling only, the minimum detector is used. When the signal amplitude both rises and falls, then the state of the max and the min latches during the previous ordinate is checked. Should

this previous state be rise only, then the max latch is read for this ordinate; should the state be fall only, then the min latch is read for this ordinate; should the state be both rise and fall, then the opposite latch to that last read, is read for this ordinate. In this way, during periods of noise, the detector latches will be set during each of the ordinates, and the max and min data latches will be read alternately. However at a signal peak, the max latch will be read even though the signal both rises and falls, since the detector latches would have been showing 'rise only' during the previous ordinate.

44. To satisfy the algorithm, the outputs of max latch IC14a and min latch IC14b are ANDed by IC27a to produce a change-over signal to the following gates. These gates select either the state of the max latch if max.min= '0', or the J-K bistable IC29a if max.min = '1'. When the signal does not both rise and fall, i.e. max.min = '0', then the max or min data latches are read depending on the state of the max latch - when max.min = '1' then the J-K bistable performs the needed algorithm. It is clocked on the falling edge of the ordinates pulse, and therefore at the start of the next ordinate pulse the history of what happened at the last ordinate is available. Should the detector latches both be set, the J-K will toggle ready to select the opposite latch to that used on the current ordinate in the event of the next ordinate having max.min = '1'. If the detector latches have differing outputs (max.min = '0') then the outputs of the J-K will reflect the input state after the clocking pulse. Hence the output will select the same latch as the previous ordinate if max.min = '0'.

45. The data enters the max output latches IC37 and IC39 and the min output latches IC35 and IC36 as a 16-bit word under DMA transfer. Since the DMA process transfers 8 bits at a time, two transfers per word have to take place, with the least significant byte being sent first. The ORDINATES pulse from the Ordinate Clock Generator sets the cross-coupled NAND R-S bistable IC41a, IC41d, causing DRQ 0 to become active. The High/Low Byte Select Generator then selects which of the two data bytes must be sent first. This m.s.b./l.s.b. signal is further gated with the max/min latch select signal so that the correct byte from the correct data latch is selected. When the second byte is selected, the R-S bistable is reset which removes the DRQ 0 signal.

46. It is possible, since the ordinate rate and the rate at which averaged data words are produced are not synchronized, that new averaged data will arrive during the data transfer process, and a change in the detector latch outputs could occur. This would cause corruption of the data levels since half of the data word would be read from one latch and half from the other. To stop this happening, the output of the change-over gate, selecting either the max or min data, is latched so that it remains constant during the time that the data is read into the input store of the display.

47. The rules about resetting the max and the min data latches are quite simple. Each time data is output to the data stores, the min data latches and the min latch are reset. The min data latches are reset to the current value of the data from the averager. The resetting of the max data latches occurs whenever they are read, and also whenever the min data latches are read as a result of a min only signal (max.min = 0). It too is reset to the current value of the data from the averager. The max latch is reset each time data is read, at the same time as the min latch and the min data latches.

48. Bypass of the display detector, (for use during Sampled Zero Span displays), is provided via IC38 (CS1E). The detector circuit is enabled whenever IC38 pin 2 is at a logical ´1´ state. It will be seen that under these conditions the three most significant bits of the new data being compared in the max and in the min data identify logic comparators will be set, and will match exactly the three m.s. bits applied to the other inputs. The comparison will then ignore these identical bits, and compare the bits of lesser significance. When IC38 pin 2 is at a logical ´0´ state, the m.s. bit of the max comparator new data input is at a ´0´ and hence the new data input must always be judged ´less´ by this comparator, and hence the max latch will not be set, and no data will be transferred to the max data latches. The minimum detector has its inputs controlled in the same way, and will therefore set the min latch and transfer the data to the min data latches. The detector circuit is hence disabled since its output is always set to give the ´min´ signal (i.e. no max and min stitching), and the data transferred to the input data stores is always that applied to the min latch immediately before the data transfer.

Sweep flyback

49. When a new sweep is started, data from the previous sweep will still be held on the board and would, incorrectly, both be averaged with the new data and displayed as the first ordinate of the new sweep. The DISPLAY DETECTOR FORCE MAX, FORCE EOC and MISS FIRST ORDINATE signals from octal latch IC38 prevent this from occurring. The sequence is as follows: DISPLAY DETECTOR FORCE MAX is asserted low to IC12 pin 1 in preparation for the next data byte. Averager Clock Counter IC20 then generates a pulse during flyback which resets the Serial to Parallel Converter IC15,16,17 to zero and latches the zero into the paralled averaged data latch IC32,33 while also providing the ENABLE pulse to the next stage. With its most significant bit pin 1 set low, IC12 recognizes the applied zero data as a new maximum so that, at the end of the ENABLE pulse, the zero data is latched into max data latches IC23,24 and max latch IC14a is set. At this point the DMA controller on AB3 causes extra DMA cycles to be made to dump the unwanted data in the output latches to spare memory locations. FORCE EOC is next asserted high to IC42 pin 10. Then ZERO SPAN MODE is asserted low to IC19 pin 4 and when FORCE EOC is removed, the falling edge causes IC34 to generate an ORDINATES pulse to High/low Byte Select Gen IC43b and latches the zero data into max output latches IC37,39. But to prevent this data from being accepted into the data store, IC38 asserts MISS FIRST ORDINATE high to prevent a DMA request from being made. To do this, the signal is inverted to reset IC25b causing IC41b to gate off the ORDINATES pulse from DRQ latch IC41a,b so preventing DRQ being asserted high to the DMA controller on AB3. When the data for the new sweep arrives it is recognized as a new maximum (since the previous data was zero) and thus replaces the zero data in the max output latches.

Board AB4 - Mathematics operations

Circuit diagrams : Chap. 7, Figs. 12-14

DMA control and input data selection

50. Board AB4 receives two sets of data, A and B, and from these generates a third, A-B. Data enters the A latches IC38, IC40 and the B latches IC39, IC23 under DMA (Direct Memory Access) control. DMA request latch IC19 output pin 5 goes high at the trailing edge of the WD signal to pin 3. WD goes low when data is to be written to the display shift registers. Since the WD

pulses occur at the line refresh rate, AB4 has about 64 μs in which to process new data before it is required for display.

51. The A and B latch sets each accept 16-bit data (although only the lower 15 bits are actually used), which are presented in the byte sequence; B low, B high, A low, A high. The DMA controller, in fact, follows these with a byte of graticule data, but this is not used on AB4, being latched on AB6 instead. The input latches are controlled by the DMA byte counter IC35 and the associated B, A, graticule demultiplexer IC18. The DMA byte counter counts 5 DACK1 + IOWR clock pulses before resetting DMA request latch IC19 on pin 1.

52. The WD pulse when active low to pin 1 IC35, resets the DMA byte counter to point at the B low latch IC39, ready for the first byte in the sequence. When the DACK1 + IOWR signal becomes active it clocks DMA byte counter IC35 which causes demultiplexer IC18 Y1 output to go active low and the Y0 output to go inactive high. Thus the B low latch IC39 receives a positive-going clock edge on its pin 11 and the first byte enters that latch. As succeeding DACK1 + IOWR pulses arrive, so Y1, Y2, Y3 and Y4 each in turn supply a positive-going edge to their associated latches IC23, IC38, IC40 and that on AB6 respectively. When the fifth pulse arrives, IC35 pin 12 goes high and, via IC24d, IC37c and IC36a, resets DMA request latch IC19a. The whole sequence repeats when the next WD pulse arrives, with the exception of the period when FRAME is active low to IC36 pin 2; the signal prevents DMA channel 1 getting out of step with the display.

53. Once both bytes of B data have been latched, the data can be processed by the rest of AB4. That the B data is available is signalled by the B SEL pulse on IC18 Y2 output which clocks the A low byte latch IC38. Similarly, when both bytes of A data have been latched, the fact is signalled by the A OR A-B SEL pulse on the Y4 output which clocks the graticule byte latch on AB6. The trailing edge (positive-going) of B SEL is used to clock the processed data from AB4 into the latch on AB5, and A OR A-B SEL does the same on AB6.

54. A OR B SEL is gated with the outputs of the A/A-B select latch IC19 to give A SEL from IC37 pin 11 and A-B SEL from IC37 pin 3. These together with B SEL are used to decide which pair of tristate buffers, ICs 20 and 25, ICs 2 and 4 or ICs 1 and 3, will be enabled so as to send data forward for processing. The signals also control the outputs of the shift latches. The processor writes to the A/A-B select latch IC19b using CS36.

55. The A-B data is produced by adding the two's complement of the B data to the A data. This is done by ICs 21, 22 and 24 and ICs 14 to 17. The A-B data is then buffered by ICs 2 and 4 ready for selection if required.

Multiplier

56. In order that the displayed spectra can be moved up and down the screen, it is necessary to add a variable offset to the data. This is achieved by part of the circuit on sheet 2.

57. The 16-bit offset values for the three sets of data are loaded by the processor into the three pairs of shift latches ICs 41 and 44, ICs 42 and 45, and ICs 43 and 46. The processor addresses the latches individually via the local chip select decoder IC49. Maths function latch IC47 controls the multiply and divide circuits. This latch and the A/A-B select latch IC19b are addressed simultaneously using CS36; the latter accepts bit 0 of the byte

which the processor writes, while the former accepts bits 1 to 6. The multiply and divide circuits may need to operate differently for the B data and the A OR B-A data, so the maths function latch contains two sets of control bits at any time. The appropriate set is selected by the maths function multiplexer IC48 according to the states of the B SEL and the A OR A-B SEL signals.

58. When the outputs of the appropriate data buffers and shift latches are enabled the combined data appears at the outputs of the shift adder formed by ICs 26 to 29. Since the data is in two's complement form, the m.s.b. of the combined data on IC29 pin 13 represents the sign bit. And since no data is displayed whose value is less than zero this bit provides the UNDERRANGE signal used to limit the display to bottom of screen (i.e. any data which has a value less than zero is presented as zero on the display). The rest of the combined data is passed to the multiplier circuit formed by ICs 5 to 9, 30, 13a and 36b.

59. The multiplier can multiply by 5 or by 1, according to the state of the MPY signal from IC48 pins 5 and 16. To multiply by 5 (when MPY = 0), a copy of the data is moved 2 bits left (equivalent to multiplying by 4), and then added to the original. The original data is applied to the A inputs of the multiplicant adders, ICs 5,7,8 and 9. The x4 data is applied, via multiplier drive buffer IC6 and IC30, to the B inputs, with the exceptions that the two least significant B inputs and the least significant carry input, are all set to zero by the MPY signal. Thus the output of the multiplicand adders represents the input data x5. Because a 16-bit number is added to a 14-bit number, the m.s.b. of the multiplicand adders is output by IC36 pin 6.

60. To multiply by 1, the multiplier drive buffer (IC6 and IC30) outputs are disabled by MPY being high, and are pulled high by R3 and R4, so that the B inputs of the multiplicand adders and the input to inverter IC13 are all high. Thus the effect of the B inputs is negated; firstly by making all the B inputs logical '1', then adding 1 to the carry input pin 7 of IC5 so that an overflow occurs from IC9 pin 9, and finally by disabling IC36 so as to gate off the overflow.

Overrange detector and divider

61. The bit shift divider selects the appropriate set of 8 bits from the 17 available at the output of the multiplier circuit, but since the smallest division ratio is 2, the l.s.b. of the multiplier output is simply ignored. The bit shift divider formed by ICs 51, 31, 32 and 50 selects sets of 8 bits which give effective ratios of 2,4,8 or 16 under the control of the division select decoder, which is, in turn, controlled by the maths function latch.

62. Even after the data has been passed through the divider circuit, it is possible for its value to exceed that which can be represented on the display (maximum is 250). Therefore, the overrange detector formed by ICs 10,11,12 and 34a, and controlled by the logic on the DIV L and DIV H lines checks the data for illegal values before it is finally sent to the output. For example, when the division ratio is set to 8, bits 2 to 9 are sent via IC32 to the display, while bits 10 to 15 are checked. If any of the latter are on then the data is overrange. The higher the division ratio, the fewer are the bits checked by the overrange circuits. Table 1 shows which bits are checked for the various division ratios.

63. Normally, division select decoder IC33 will enable one of the bit shift divider buffers by taking one of its Y outputs low. However, if the overrange detector finds that the value of the input data is too large, it disables the decoder via IC12c thus preventing any of the Y outputs from going low. The tristated output of the divider buffer will be pulled to all ones by the action of pull-up resistors R5. Similarly, if the UNDERRANGE signal is active, decoder IC33 outputs are disabled via IC12d while the underrange clamp IC52 is enabled thus pulling the output data to all zeros. The resulting processed display data is passed out to AB5.

TABLE 1 OVERRANGE DETECTOR OPERATION - AB4

Division ratio	16	8	4	2
Control signals:-				
DIV L	L	H	L	H
DIV H	L	L	H	H
Bits checked:-				
8				✓
9			✓	✓
10		✓	✓	✓
11	✓	✓	✓	✓
12	✓	✓	✓	✓
13	✓	✓	✓	✓
14	✓	✓	✓	✓
15	✓	✓	✓	✓

Example: For ÷16 DIV L and DIV H are both low and bits 11 to 15 are checked for overrange.

Board AB5 - Timing & B display dynamic store

Circuit diagrams : Chap. 7, Figs. 15 & 16

Circuit Sheet 1

64. The method of displaying frequency spectra on the TV screen and the operation of the A channel, B channel, and Graticule Channel Display Shift Registers (ADSR, BDSR, GDSR) are very closely related. Note that the ADSR and GDSR circuits are on AB6, but all three DSR's are considered here, since they are governed by common timing circuits which appear on this board. The Spectrum Display Area (SDA) on the TV screen is essentially a histogram, nominally 500 ordinates along the X, or Frequency, axis, and 250 levels along

the Y, or Amplitude, axis. The histogram can be overlain by a graticule, and, depending on the contents of the GDSR, the SDA can be made to represent graphs which are lin/lin, lin/log, log/lin, or log/log. Since it is desirable, for linear graphs, that the graticule should encompass an even number of ordinates, the DSRs are actually designed to hold data representing 502 ordinates on the X axis. In the A and B DSR's, one byte (8 bits, using 250 of 256 possible levels) is used for each ordinate.

65. The GDSR is used to hold data which represents the frequency (vertical) graticule lines only: the display of amplitude (horizontal) graticule lines is due to circuits on AB7. Also, the graticule is displayed at half the resolution of the spectra, and thus the GDSR is only half the length of the A and B DSRs. The GDSR holds just two bits of data for each graticule line position since it is only necessary to define a major, minor, dashed or no graticule line. The remaining two bits of the GDSR are used to hold marker data, and are discussed in the description for AB6.

66. The DSRs are provided with data feedback paths, so that the data may be read non-destructively in byte-serial form. The method and rates of clocking the DSRs are such that the data makes one complete rotation in the time the TV scan takes to pass across the SDA. On a given SDA scan line, the spectrum data for each ordinate is compared with the scan line number, and the result passes to logic which decides whether or not to light up the pixel (picture element) corresponding to the ordinate on that line. The graticule data is used directly to light pixels as the scan reaches the appropriate positions.

67. In order that new data may be written into the DSRs from time to time, they have multiplexers at their inputs. These select either data fed back from the DSR outputs, or new data which has been processed by AB4. They are under the control of the even/odd Write Pulse Generator (WPG), which allows one new byte to be written into each DSR during each SDA scan line period.

68. Each 8-bit DSR is formed by running 4-bit banks in parallel; the LSB bank which holds bits 0 to 3, and the MSB bank for bits 4 to 7. Each bank is comprised of two physical SRs, EVEN and ODD. New data is written to the EVEN registers of each bank simultaneously; similarly, the ODD registers. The EVEN and ODD pairs are written alternately. The register output multiplexers select, in parallel, the outputs of the EVEN pair alternately with the ODD pair, and the overall effect is thus of an 8-bit DSR whose length and clocking rate are each twice that of the physical SRs.

69. Each shift register is formed from three ICs, and since all four registers are similar, a description of the operation of the EVEN register of the LSB BANK can serve for all. The heart of the register is IC13 which is a 4-bit by 256 word device. This m.o.s. IC is driven by a high level bi-phase non-overlapping clock derived from the 6.25 MHz SHIFT REGISTER GATED CLOCK. The signal, with a pulse width of 70 ns, is applied to pin 4 (Φ1) and pin 11(Φ2). IC13's clock-to-data-output delay is such that it cannot directly recirculate data and therefore an extra register stage, IC14a follows whose output delay is very much shorter. IC14a consists of 4 D-type bistables and is clocked by 6.25 MHz SHIFT REGISTER GATED CLOCK. IC13 outputs are open drain and are made t.t.l. compatible by pull-down resistors R7a to d. Output is to multiplexer IC30.

70. Output multiplexers IC25 and IC30 are driven by the 6.25 MHz SHIFT REGISTER CLOCK signal and thus produce two streams of 4-bit data in parallel at a rate of 12.5 MHz. Input multiplexers ICs 26, 27, 28 and 29 are normally set to select recirculated data from the extra register stages of IC9 and IC14.

However, once every alternate TV horizontal scan (see above), the input multiplexers for the EVEN register pair, ICs 27 and 29, are made to select new data under control of the WE output from the Write Pulse Generator (WPG) to pins 1. Similarly, the ODD pair, ICs 26 and 28, are written due to WO once every other scan. Since data is written into the registers at a much slower rate than it is read, the WPG must keep track of where next to write data: the way it does this is described in a succeeding paragraph.

71. The high-level bi-phase clock for the shift registers is derived from the 6.25 MHz SHIFT REGISTER CLOCK signal by ICs 41, 42, 43 and 45. IC41 acts as a phase splitter, producing Φ1 from pin 5 and Φ2 from pin 6. The positive-going leading edges of Φ1 trigger monostable IC42a which emits 70 ns positive-going pulses. These are a.c. coupled to clock drivers IC43 and IC45 which convert the pulses to high level (+5 V, -12 V) to supply Φ1a and Φ1b for the shift registers. Similarly, Φ2 triggers monostable IC42b, and the 70 ns pulses which this emits are converted to Φ2a and Φ2b. The width of the Φ1a,b pulses is set by R4, Φ2a, b by R3.

72. Because the data in the DSRs must complete just one rotation during each TV horizontal scan, it is necessary to stop the DSR clocks periodically. This is done by the Gated Clock and Horizontal Mask Generator (GCHM). Although the A and B DSRs each hold 502 bytes of data to be sent to the display, they are actually 514 stages long. Hence, after allowing the DSRs to receive 502 clocks, the GCHM sets a mask which prevents the display of further "data", while the DSRs are given another 12 clocks. The GCHM then stops the DSR clocks completely, and awaits the next horizontal scan before resetting the mask, and re-enabling the DSR clocks. It should be noted that the DSRs operate over the whole vertical scanning cycle; in particular, the DSR clocks are NOT gated by any vertical retrace signals. The SDA, however, is defined with reference to vertical retrace (see below).

73. In order to maintain alignment between displayed data and displayed characters, the GCHM synchronizes its activities to the leading edge of HRTC (L) to pin 13 of IC40. Before HRTC goes low, the counter formed by ICs 16, 31 and 48 is held in the load state by IC40 pin 8, and START from IC16 pin 12 therefore is low. When HRTC goes low (beginning of horizontal retrace), it resets IC40 whose Q(L) output goes high. The counter is released from the load state and begins to count PHASED 12.5 MHz CLOCKS. Since the data display appears within an annotated border on the screen (i.e. the SDA), the counter is preloaded with a value such that when IC16 pin 12 goes high to assert START, an interval corresponding to the horizontal retrace period plus the chosen width of the border has elapsed. The rising edge of START clocks IC15b taking CLOCK EN low, which, via IC47b and IC46b produces the 6.25 MHz SHIFT REGISTER GATED CLOCK signal. Thus the DSR clock is started and data contained in the registers begins to appear at the output of multiplexers IC25 and IC30.

74. The same edge of START also clocks IC15a whose Q output supplies the X-direction video enable signal, XVIDEN. This is combined with other signals (see below) to enable the display of data within the SDA and so prevent spurious data appearing outside the SDA. When the counter has counted 502 clocks after START, all of the data in the DSRs will have been presented in the SDA. This state is detected by AND-gate IC32, and used to reset IC15a restoring XVIDEN low.

75. At this stage however, data byte 1 has not yet returned to register position 1 which it occupied before clocking began. This is because the data occupies only 502 of the available 514 positions. Therefore, the counter continues counting up to 514 clocks after START. This stage is detected by IC47a and used to reset IC15b. CLOCK EN therefore, goes high which stops the 6.25 MHz SHIFT REGISTER GATED CLOCK to the DSRs. Consequently, the shift registers stop with data byte 1 in position 1 again. At the same time, the rising edge of CLOCK EN clocks IC40a whose Q(L) output goes low, forcing the counter into the load state. This completes the horizontal scan cycle, and the whole circuit waits for the next HRTC falling edge.

76. A new data byte on the MULTIPLEXED PROCESSED DISPLAY DATA bus which is destined for the BDSR is first placed in B demultiplexing latch IC44, under control of B SEL to pin 11. IC44 outputs present the data to the NEW data inputs of the DSR input multiplexers. These normally select their recirculating inputs. However, once during every other SDA scan line period, the EVEN input multiplexers select their NEW inputs, so that the new data enters the EVEN register pair. On the alternate scans, the ODD input multiplexers select their NEW inputs, and the new data enters the ODD register pair. The signals controlling the input multiplexers are called Write Even (WE) and Write Odd (WO) and they are generated by the WPG.

77. The heart of the WPG is a 10-bit counter formed by ICs 1,17 and 33. The counter is clocked by the 6.25 MHz SHIFT REGISTER GATED CLOCK and thus receives 257 clocking edges per horizontal scan. Bit 9 output from IC33 pin 13 to the inputs of bit 9 (IC33 pin 4) and bit 0 (IC1 pin 3) allows the counter to divide by 257 and 258 alternately. Hence, on every other scan, the counter's transition to a given state will move one clock pulse later, relative to the immediately previous scan. This is used as a pointer to successive locations in the register pairs. The counter is configured to derive WD(L) from IC34 pin 6 which determines where data should be written in a register pair, and the odd/even output from IC33 pin 13 which points alternately to the ODD and EVEN register pairs. Since there are only about 320 horizontal scans per TV field, it takes the WPG the best part of two fields to put new data into all 502 DSR locations. However, if the WPG writes to a DSR location on every scan in both fields, it will cause wrap-around. To prevent this, for every two fields the WPG is resynchronized to the trailing edge of FRAME(L) to IC2 pins 2 and 4, and after 502 bytes have been written into the DSR, DREQ1 is used, which remains high to pin 5 IC34, to prevent any further WD pulses reaching the DSR. WD(L) from IC34 pin 6 is inverted and combined with odd/even output from IC33 pin 13 to form WO or WE which control the DSR input multiplexers.

78. What happens between the end of one TV frame and the start of the next, is explained from a point near the end of a frame when WD goes low for the 502nd time. Just after WD's falling edge, the 501st data byte is written into the DSR. On AB4, WD's rising edge clocks the DMA Request Latch (DMARL) making DRQ1 go high. The DMA controller on AB3 sends some data bytes, and eventually resets the DMARL so that DRQ1 goes low again with byte 502 placed in B Demux Latch (BDML), IC44. The DMA controller has now reached the end of process on channel 1 and will not send further data until reset during the next FRAME period. As WD goes low for the 503rd time, data byte 503 enters the DSR, and DRQ1 goes high. It will remain so for the rest of the frame when the DMA controller becomes inactive. DRQ1 high to pin 5 of IC34 prevents any further WD pulses from reaching the DSR, and also means that data byte 502 is left undisturbed in BDML IC44.

79. When FRAME goes low, the DMARL on AB4 is reset and held so until the end of FRAME and so DRQ1 goes, and is held, low. This does not affect the DSR, however, because the WPG is also reset by FRAME to IC2 pins 2 and 4, and so no WD pulses are produced in this period. Sometime during FRAME, the DMA controller is re-initialized by part of the processor's frame interrupt routine. Eventually, FRAME goes high again and the WPG is able to begin its first count cycle during the first horizontal scan of the new TV frame. This first cycle is of 258 states, and obviously the WPG will stop in its terminal count state as it receives only 257 6.25 MHz SHIFT REGISTER GATED CLOCKS during the scan. Thus WD is asserted and remains low, and WE holds the EVEN bank input multiplexers open, until the first clock edge of the second scan. At this point, data byte 502 is deposited in the final position of the EVEN bank, and since the WPG's first cycle is complete, WD goes high, thus setting the DMARL on AB4. The DMA controller now sends data byte 1 (for this frame) to wait in the BDML. The WPG's next cycle has 257 states, but it has already used one of the clocks of this (second) scan to complete the previous cycle. Therefore, another elongated WD pulse occurs, which, this time, results in the transfer of data byte No. 1 to the last position in the ODD bank on the first clock edge of the third scan. Simultaneously, DRQ1 goes high and the DMA controller soon sends data byte 2 to the BDML. The WPG now has a 258 state cycle again, with only 256 clocks of the present (third) scan left. Hence, terminal count does NOT coincide with the last clock edge of the scan, and a Orshort WD pulse occurs between the first and second clock edges of the fourth scan. Data byte 2 is thus written into the first position of the EVEN bank. Similarly, data byte 3 is written into position 1 of the ODD bank. This process continues until data byte 502 which concludes the sequence.

Circuit Sheet 2

80. On sheet 2 are seen the B channel Video Generator (BVG), which consists principally of the line draw and infill bright up operator, and the Line Count and Vertical Mask generator (LCVM). The vertical display mask, YVIDEN from IC40 pin 5 defines the top and bottom of the SDA. The LCVM consists mainly of a 9-bit ripple down counter formed by ICs 36 to 38 which is clocked by HRTC. When VRTC is asserted low to IC37 pin 11, the counter is parallel-loaded with 273. After the trailing (rising) edge of VRTC, which coincides with the start of the TV picture, the counter first counts down to 250. This state is detected and LINE 250 goes low from IC39 pin 11 which sets Vertical Mask Latch (VML) IC40b. This causes YVIDEN to go high, and the top of the SDA is defined. The counter continues down to zero, at which point LINE 0 from IC38 pin 13 goes low resetting VML IC40, and so defining the bottom of the SDA, YVIDEN and XVIDEN are combined with Box by AND-gates IC3a and b to produce the Data Display Mask signal TOTAL DDM. The latter has two functions: to define the SDA Window within the TV picture, and to provide blank boxes around characters which appear within the SDA.

81. The current SDA scan line number (250...0) is extracted from the LCVM as the lower 8 output bits of the counter and passed to the B Data Comparator (BDC), ICs 7 and 8 on the HIGH SPEED B CHANNEL DATA lines. The rising edge of the 12.5 MHz PHASED CLOCK is taken to the clock inputs of ICs 23a and b forming the Current Ordinate Latches (COL), and used to latch in the greater than (>) and less than (<) decision signals from IC8 pins 5 and 7 respectively. Use of the clock ensures that the BDC has enough time to reach its decision, resynchronizes the less than and greater than decision signals and results in every data byte being displaced right by one ordinate position on the display. Compensation for this is made near the beginning of each horizontal scan across the SDA. While XVIDEN from IC15 pin 5 (see Sheet 1) is low and CLOCK EN from pin 8 is high, the DSR waits with display data byte 1

present at its output. Since the 12.5 MHz PHASED CLOCK does not stop, the BDSL is repeatedly loaded with data byte 1, and the COL receives the same decision from the BDC on every clock edge. Then, as soon as XVIDEN goes high, and CLOCK EN goes low, the BVG paints up data byte 1 in the first ordinate position. However, data byte 1 will now be clocked into the BDSL once in the normal way, and will, therefore, also appear in the second ordinate position (see above). After this, operation returns to normal, leaving data byte 1 as the only double ordinate.

82. The BVG uses the BDC decisions stored in the COL and Previous Ordinate Latches (POL), IC22, to create either line draw or infill type display video. However, line 250 (top line of the SDA) is a special case since this line must be lighted over those sections where data amplitude is greater than top of SDA. B display amplitude limiter IC21 ensures that this happens for line draw displays. The algorithms for the two types of display are shown in Table 2.

TABLE 2 DISPLAY ALGORITHMS - AB5

Algorithm	COL	POL	250(L)	video
INFILL	D<L	x	x	off
	D>L	x	x	on
	D=L	x	x	on
LINE DRAW	D<L	D<=L	x	off
	D>L	D>=L	1	off
	D>L	D>=L	0	on
	D<L	D>L	x	on
	D>L	D<L	x	on
	D=L	x	x	on

Where D is data, L is line number and X is don't care

Board AB6 - Graticule & A display dynamic store

Circuit diagrams : Chap. 7, Figs. 17 & 18

Shift registers and video generator

83. For a description of the A channel Display Shift Register (ADSR) on sheet 1, and the A channel Video Generator (AVG) on sheet 2, refer to the description of the identical circuits on AB5. Note that the shift register clocks, $\phi 1$ and $\phi 2$, have their pulse widths set locally (IC35a,b), so as to avoid sending these critical signals across motherboard AA1.

84. The Graticule Display Shift Register (GDSR), on sheet 1, is also very similar to the A and B DSR's, but is only half the length (257 locations instead of 514) and half the width (4-bit words instead of 8-bit) of the former. Its output data rate is half that of the larger DSR's too, which means that vertical graticule lines are always two ordinate positions wide on the TV screen. Graticule information destined for the GDSR is placed in the Grat Input Latch, IC37, under control of circuits on AB4, but the data itself comes directly from memory (by means of the DMA controller) without passing through AB4. Since the GDSR works at half the speed of the other two DSRs, it needs to have new data written in only half as frequently. For this

reason its input multiplexer, IC23, is controlled on pin 1 by Write Odd (WO) only.

Vertical graticule and marker generation

85. On sheet 2 the GDSR output is synchronized with that of the ADSR and BDSR by latching it in IC21, using the PHASED 12.5 MHz CLOCK as the latch control to pin 9. The latched 4-bit data is then split into marker and graticule information, and each is decoded to generate various effects on the TV screen. The 2-bit graticule data from pins 10 and 15 is decoded by IC20 so as to give one of four possible effects in any vertical graticule line position (see Table 3). Dashed major lines are produced by combining the inverted output of the decoder with a suitable line count bit. Dashed and normal major graticule lines are combined into MAJOR VERT GRAT by IC4a before being sent to AB7. The minor line output is inverted to form MINOR VERT GRAT to AB7. On AB7 these vertical graticule lines are combined with the horizontal graticule lines, and then sent to the video mixer.

TABLE 3 VERTICAL GRATICULE DECODING - AB6

Input IC20		IC20 output pins				Effect selected
Pin 13	Pin 3	4	5	6	7	
L	L	H	H	H	L	No graticule line (default)
L	H	H	H	L	H	Minor graticule line
H	L	H	L	H	H	Major graticule line
H	H	L	H	H	H	Dashed major graticule line

TABLE 4 IC7 MARKER DECODING - AB6

Input pins			Active output pins								Effect selected
13	3	1,15	9	10	11	12	7	6	5	4	
L	X	L	L		L						No marker
H	X	H						L		L	Steady marker, odd ordinate
L	X	H					L		L		Steady marker, even ordinate
H	H	L				L					Flashing marker, odd ordinate
H	L	L		L							Flashing marker, even ordinate

86. Three bit data is decoded by 3 to 8 line decoder IC7 which selects the required marker effect. A marker can appear in any ordinate position and sits at the data value for that ordinate. Markers however, are available on only one channel at a time. The five possible effects decoded by IC7 are shown in Table 4. To supply the flashing marker, IC8 is configured to divide the VRTC signal by 4 to produce a square wave of about 12 Hz from pin 9 to set

the FLASH RATE for the flashing marker signal. The odd/even flashing ordinate markers are produced by a combination of the logic on the ODD/EVEN FLASHING MARKERS line (low to select even coordinates) and the level on the GATED 6.25 MHz line (i.e. half the ordinate rate). By this means selected alternate markers are flashed at a 12 Hz rate. The MARKER signal from IC5 pin 8 is gated with A/B MKRS which selects the channel to which the markers refer, and with A= and B= which determine the vertical positioning of the markers on the TV screen. Marker data is then clocked out from D-latch IC40a synchronized to the PHASED 12.5 MHz CLOCK to provide the MKR VIDEO signal for the summer on AB7.

87. Display status latch IC36 controls the main features of the TV display within the Spectrum Display Area (SDA). The processor writes control bits into the latch using pin 11. The resulting B VIEW ON and B INFILL ON are sent to AB5 where they perform the equivalent to the A view and A infill signals for this board.

DISPLAY

88. The block diagram for the display is shown in Fig. 3. The spectrum display area has 250 TV lines divided by the horizontal graticule into 10 major divisions of 25 lines. Each major division is able to display 2 rows of annotation characters. Each of these 5 x 7 dot characters is displayed within a 7 x 12 dot cell. Including the out of display area, the total number of cells is 66 x 24. The character generator is on AB7 and is a PROM which outputs 2 bits initially used for horizontal graticule type selection, and 6 bits to define each line of the character to be displayed. At the start of each line, the first character line generated defines the horizontal graticule; whether the graticule is a major one or a minor one is determined by bits 1 and 2 whose states are then held for the duration of the line. When the second or subsequent character line generated forms part of an annotation, the data configures 5 dots for the character plus a 2 dot intercharacter separator which is always blank. At the same time one of the unused graticule bits is used to control the blanking of all other video information within a character cell so that the character appears in high contrast.

89. AB7 contains the video mixer which controls the contrast of the various images making up the display. The mixer accepts 9 channels of video data and produces a single channel of mixed video for display. One channel, read-in bright-up, has fixed contrast and is used for the slower sweeps to enable the progress of the left to right sweep to be distinguished. The relative contrast for the remaining 8 channels in 3 groups is set for the mixer by the front panel INTENSITY controls for the A display, B display and graticule (which includes markers and annotating characters).

90. The board also contains the clock generators used for all data timing as well as for the production of the vertical field, and the horizontal line, synchronizing pulses.

91. AD1/1 via AT2 supplies the drive voltages to the cathode ray tube in order to display the information supplied by the c.r.t. controller and video mixer on AB7. Synchronizing signals to IC2,IC3 and IC4 supply the required horizontal and vertical electromagnetic deflection. Horizontal scanning, from left to right, is at a line rate of 15.625 kHz. Vertical scanning, from top to bottom, is at a frame rate of 48 Hz. Video modulation signals are applied to the c.r.t. cathode, and dynamic focus to anode 3. For protection purposes, AT2 (which supports the c.r.t. base) has spark gaps punched into it.

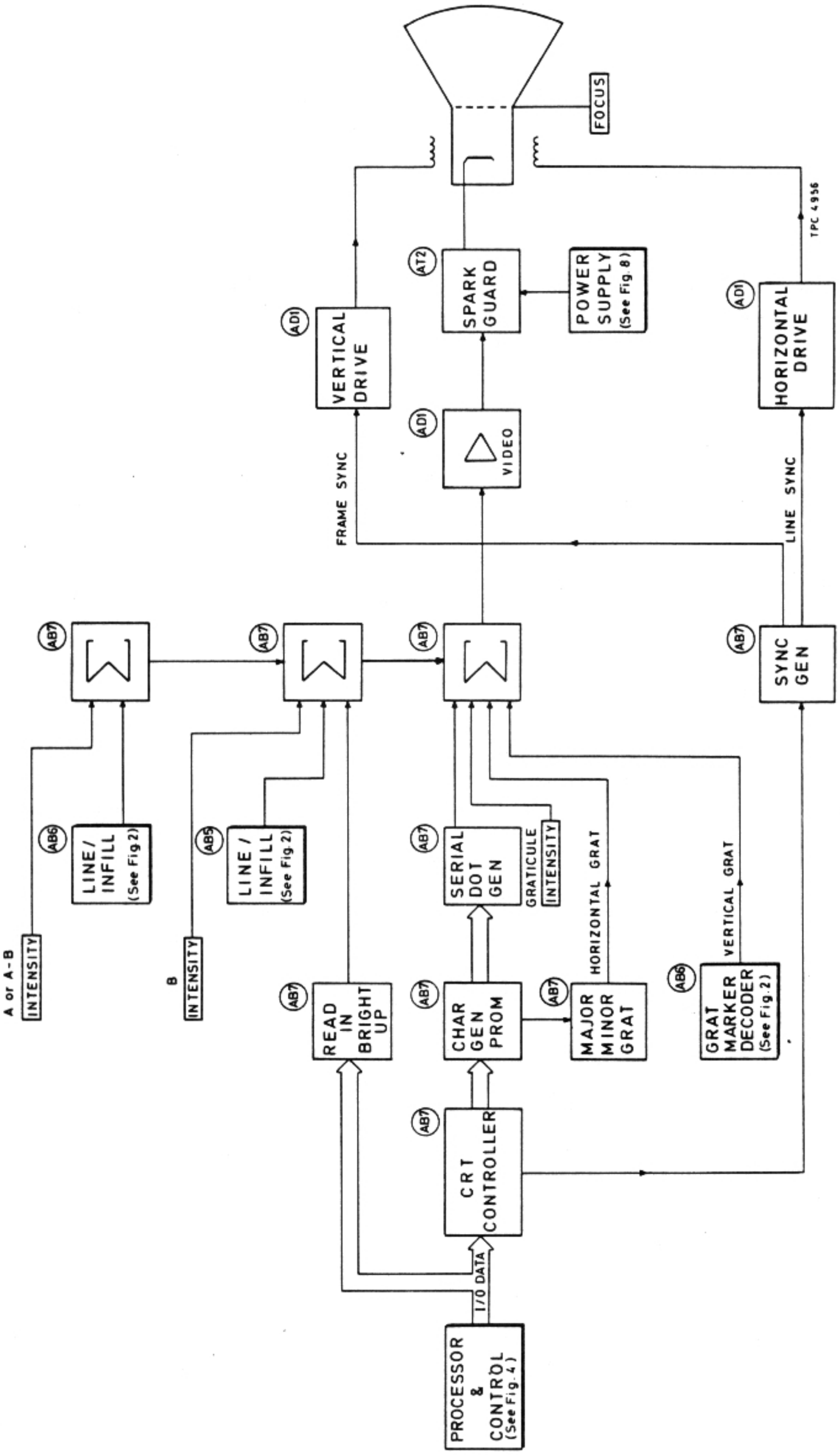


Fig. 3 Display block diagram showing main functions of boards

Board AB7 - CRT control, clock and video mixer

Circuit diagrams : Chap. 7, Figs. 19-21

Oscillator and p.l.l.

92. Sheet 1 shows the phase locked oscillator which generates the upper unit master clock using the lower unit master clock as reference. The oscillator is a modified Butler circuit built around TR13. Its output via TR16 is buffered and amplified to t.t.l. compatible levels by TR11 and TR12 and fed out as the 25 MHz CLOCK signal. This signal is also fed to the feedback loop via divider IC1 connected to divide by 5. The resulting 5 MHz is compared with the 5 MHz SYNC CLOCK for phase by EXclusive-OR gate IC2a whose output is connected to the inverting input of error amplifier and search oscillator IC42.

93. IC42 is a very low frequency Wien oscillator with feedback components R16, C78, R9 and C77. When out of lock, the square wave output from IC2a enables IC42 gain to be set by R11, R12 and R15 to just over 3 and so enable search oscillator operation. When the LC oscillator during its sweep attains lock, the IC42 inverting input becomes a virtual ground which sets the gain to 1 and halts search oscillator operation.

94. When during a fault condition or for servicing purposes the 5 MHz SYNC CLOCK is removed, integrator R7, C75 ceases operation causing TR15 to switch off and TR14 to switch on. This connects 5 V to the non-inverting input of IC42 causing the amplified output to varactor diodes D19 and D20 to hold the LC oscillator at its mid frequency and adjustment point. In this condition, the oscillator may be set to its 25 MHz operating frequency by means of C43.

Character generator

95. The character dot and clock generator on Sheet 2 determines the rate at which the dots forming the characters are sent to the screen. IC31a and b accept the 25 MHz master clock and divide it by 3 to produce the 8.3 MHz dot clock from IC31b pin 9. CHAR CLOCK, which is used as the timing reference by most of the circuits associated with the Cathode Ray Tube Controller (CRTC) IC15, is generated from the dot clock by counter IC30. IC30 also generates addresses for the dot multiplexer IC29. The data representing the dots for a given line within a particular character is latched in IC28 by CHAR CLOCK to pin 11, and emerges in serial form at the output of the multiplexer, IC29 pin 6. The CRTC uses the falling edge of CHAR CLOCK to pin 30 as its timing reference.

96. Following the falling edge of CHAR CLOCK, multiplexer IC29 inputs are addressed in the order 2,3,4,5,6,7,0,1. This, allied to the particular interconnections between latch and multiplexer, means that the dot data from the Character Gen (CG) PROM IC27 is sent to the screen in the following order: bit 2 (pin 11), bit 7 (pin 17), bit 6 (pin 16), bit 5 (pin 15), bit 4 (pin 14), bit 3 (pin 13), bit 2 (pin 11). Bit 2 is the inter-character separator which is always blank. Thus each character is 5 dots wide, and sits in a box 7 dots wide, so that there are two dot widths between adjacent characters. The two CG bits not used as dot data, bit 0 (pin 9) and bit 1 (pin 10), are used by the circuits which generate the amplitude graticule and character boxes.

Graticule generator

97. Amplitude (horizontal) graticule lines are controlled by special non-printing characters which are placed in the first position of each character row in the display area. Amplitude graticule generator operation for this purpose is examined at a time when IC33b pin 6 is high. Then, during the horizontal retrace period, the low HRTC output from IC15 pin 7 holds IC32a, IC32b and IC33a all in the reset state. Following the trailing edge of HRTC, CHAR CLOCK (inverted by IC10b) clocks IC32a to take its Q output high. This supplies a single clocking edge to IC32b and IC33a. IC32b latches the state of bit 1, and IC33a latches the state of bit 0 from character generator IC27. These states are thus held for the duration of a scan line, and are used by the video mixer to produce the horizontal graticule lines.

98. In any character position except the first within a given row, CG bit 1 from IC27 pin 10 controls the BOX signals from IC33b pins 5 and 6. These signals blank out all video information within a character cell except the character itself so that characters written in the spectrum display area are seen in high contrast. Bit 1 provides the data input for IC33b which is latched for every character. To subject the major and minor horizontal graticule lines to BOX, the Q(H) outputs of IC32b and IC33a are ANDed with the Q(L) output of IC33b. Before being sent off the board, BOX is gated with CHAR ON and EXTRA LINE by IC6b and IC20. This is done so that if the character video channel is disabled, blank boxes will not appear in the display area; similarly, during the extra line period, the display is not affected by BOX.

ERSD and ESPG

99. The Even Row Start Detector (ERSD) and the Extra line Sync Pulse Generator (ESPG) are present due to the following considerations: Firstly, the number of TV lines that the spectrum display occupies is chosen to be the largest within an 8-bit range, which is easily divisible by 2,5 and 10; so 250 is selected giving 10 major divisions of 25 lines each. Secondly, it is required to have two rows of annotation characters per major division. These requirements conflict, since the CRTC can (obviously) only display character rows which contain a whole number of TV lines. The solution used is to program the CRTC to use 12 TV lines per character row, and then to modify the operation using the ESRD/ESPG circuit. The circuit stops the CRTC for the duration of one line at the start of every other character row, and to insert an extra sync pulse so that the TV unit is unaffected.

100. During the vertical retrace period, the ERSD is held in a reset state by VRTC to IC11 pins 4 and 13; the Q(L) output of IC11a being low, that of IC11b being high. LC3 is inverted and goes high to the clock input pin 3 of IC11a at the start of each character row. After the end of VRTC, binary divider IC11a receives the clocking edge which sets its Q(L) output high. This, in turn, clocks IC11b whose Q(L) output goes low to assert EXTRA LINE. The signal stops CRTC IC15 by disabling its CHAR CLOCK input, while enabling ESPG IC23 by taking its resets low. After the end of the extra line period, the ESPG takes DETECT 76 low which resets IC11b, thus re-enabling the CRTC. The CRTC then proceeds to display two rows of characters (24 TV lines) in the normal manner. At the start of the odd-numbered character rows, IC11a also receives a clocking pulse, but this time it simply resets Q(L) output low

again. Note that the extra line does not affect the displayed characters in any way, since it is inserted between rows; similarly, the horizontal graticule lines are not affected, since they are generated within the character rows.

101. ESPG IC23, when enabled by ERSD, counts 67 character clock positive edges on its pin 1 (66 characters per row are displayed but the CRTC changes the line count one character clock before the beginning of a line, therefore an extra clock edge has to be counted), and then sets EXTRA SYNC (IC34 pin 12) active low for one character clock period. On the positive (trailing) edge of EXTRA SYNC (which, due to counting positive character clock edges, is half a character clock period later than a normal HRTC edge), the sync pulse generator (see below) emits an extra sync pulse. When the ESPG has counted on to 76 character clocks, i.e. counted out the HRTC period, it resets IC11b which re-enables the CRTC as discussed above.

DMA request disable

102. The CRTC's DMA requests are gated by IC8a with EXTRA LINE, because the CRTC simply holds the state of its outputs when the character clock is stopped. If this were not done, and DREQ from pin 5 happened to be asserted when the CHAR CLOCK stopped, the DMA controller would carry on transferring data, unable to know that the CRTC was ignoring it. IC8a prevents this by disabling the DMA request DREQ3 when the CRTC is not being clocked.

Phased clock generator

103. The Data Display Phased Clock Generator is used to obtain 12.5 MHz and 6.25 MHz clock signals whose phase is guaranteed at the start of every TV field. The phased signals are used by the Display Shift Registers on AB6 and AB5, which must have clocks of known phase in order that data is entered in the correct sequence.

104. IC5a produces a fast synchronized version of VRTC, the trailing edge of which from pin 5 is used to indicate the start of the field. IC3a divides the master clock input by two, supplying 12.5 MHz unphased to the rest of the instrument on its Q(L) output, and to the phasing circuit on its Q(H) output. At the start of a field, IC4b is clocked and latches the state (and thus the current phase) of the 12.5 MHz signal to its Q(L) output which is then used to control pass/invert gate IC2b. The latter is supplied with 12.5 MHz at its other input, and therefore its output from pin 3 is 12.5 MHz of fixed phase which is sent to AB5 and AB6. IC3b also receives the phased 12.5 MHz signal and divides it by two to supply 6.25 MHz to the phasing circuit formed by IC5b and IC2c. This operates in the same way as discussed above, producing 6.25 MHz of fixed phase at the output of IC2c.

Sync pulse generator

105. The main sync pulse generator on Sheet 3 produces HRTC, VRTC, HSYNC and VSYNC using VRTCS HRTCS and EXTRA SYNC. VSYNC from monostable IC21b is the vertical (field) sync for the TV unit, and has a pulse width of about 160 µs. HSYNC from monostable IC21a is the horizontal (line) sync and is about 4.7 µs wide.

106. At the start of every vertical retrace interval, the leading edge of VRTCS is differentiated by IC9c and C56 to produce a narrow negative-going pulse. This is used to reset, via IC22d, the Horizontal Sync Trigger Bistable (HSTB), IC19b, thereby avoiding a possible power-up lock in the loop formed by IC19b, IC7d and IC21a.

107. HSTB IC19b and Extra Sync Trigger Bistable (ESTB) IC19a are used to obtain the OR function of the positive-going edges of HRTCS and EXTRA SYNC at the output of IC7d. This is used to trigger HSYNC pulse generator IC21a, which would otherwise be difficult since HRTCS remains high during the whole extra line period. ESTB IC19a is reset by HRTCS when next it goes low after an extra sync pulse has been generated, while HSTB IC19b is reset by HRTC, the inverted version of HSYNC, from IC21a, and by VRTCS as noted above.

Read-in bright-up

108. Read-in Bright-up is used on the slower sweeps so that the user can more easily see how the sweep is progressing. The visible effect is of a slight brightening of an increasing portion of the spectrum display, starting from the left. The edge between the brighter and normal parts indicates the ordinate being read at the time. For the following description, it is assumed that bright-up is enabled, i.e. IC13a pin 1 is high.

109. The processor loads sweep position latch IC26 using CS18, when ready, with the ordinate number which represents the current read-in position. This is loaded into the bright-up down counter, IC24 and IC25, on every TV line using HRTC. Simultaneously, HRTC sets the Q output of IC12b high. When the TV line scan reaches the spectrum display area, DDM (Data Display Mask) goes high to pin 2 IC13a, which makes READ-IN BRIGHT-UP high, and the SR CLOCK starts to decrement bright-up down counter IC25. Thus, the spectrum display is brightened from the left side. When the down counter passes zero, it clocks IC12b which sets its Q output low, and takes READ-IN BRIGHT-UP low again. Outside the spectrum display area, the output of the down counter has no effect because of DDM. As the processor updates the sweep position latch, IC26, the brightened region is seen to expand from left to right across the spectrum display.

Video mixer

110. The video mixer accepts nine channels of t.t.l. level video data and produces a single channel of mixed video of 0.5 V p-p maximum. The READ-IN BRIGHT-UP channel has fixed contrast level, but the other eight channels have variable contrast, and are grouped as follows:-

CONTRA 1(A)	:	A INFILL, A LINEdraw
CONTRA 2(B)	:	B INFILL, B LINEdraw
CONTRA 3(G)	:	MAJOR graticule, MINOR graticule, MARKER, CHARacters

The contrast level of each group is controlled by an INTENSITY potentiometer on the front panel. The relative contrast level of the members of a group is fixed by the resistive divider which connects each channel to its contrast control.

111. The operation of the A INFILL channel, which is representative of all other channels (except READ-IN BRIGHT-UP), is discussed next and is assumed to be the only active channel. The contrast control voltage appearing on CONTRA A1, say V1, is converted to the required level, V2, by the divider R30, R31

and R32; hence the cathode of D1 is held at V2. D1 compensates for changes in TR1's Vbe with temperature, and C50 decouples the base voltage to prevent TV field-synchronous variations in displayed brightness due to the transistor switching. The voltage at the base of TR1 is about V2 + 0.6 V, so its emitter voltage is very nearly V2. Thus, when A INFILL is high, a known current will flow in R35 and R34. Consequently, TR1's collector voltage, V3, is established, and the 'Soft Clamp', D2 and R36, holds the output of the Video Summer at about V3 (cold end of R110).

112. The 'Soft Clamps' give the Video Summer a non-linear characteristic: however, two inputs of nominally the same level will not result in an output of twice that level. This limits the dynamic range of the video signal sent to the TV unit, and produces a more pleasing display than results if the levels of the various channels are simply added. The effect is rather like overlaying transparencies.

113. The mixed video passes to the Output Buffer, TR9, which reduces the amplitude of the signal to about 0.5 V p-p max. (so that the TV unit is not over-driven), and presents it at a suitably low impedance. The speed-up capacitor, C63, is present so that narrow horizontal and vertical lines may have the same apparent brightness.

114. The READ-IN BRIGHT-UP channel, TR10, has fixed contrast, its level having been chosen so that it is clearly seen when active, whatever the levels of the other channels. The remaining channels all operate in the same way as the A INFILL channel, described above.

Board AD1/1 - Display drive & Board AT2 - CRT base

Assembly AD0 - CRT

Circuit diagram : Chap. 7, Fig. 28

Summary

115. The display p.c.b. AD1/1 and associated p.c.b. AT2 provides the drive voltages to display the information generated by the c.r.t. controller and video mixer on AB7. Electromagnetic scanning is employed to generate a 325 horizontal line, non-interlaced raster, every 20.8 ms on a 19 cm c.r.t. with video modulation applied to the cathode. AD0 consists of the c.r.t. and deflection yoke assembly with associated wiring. AD1/1 contains six discrete sections:

Voltage regulator

116. IC1 regulates the +14.5 V supply input and provides +11.5V (±0.3 V) to AD1/1 when the display is enabled. Should the display be required to be disabled, then TR1 clamps the voltage adjust pin of IC1 to ground, reducing the supply to the board to +1.2 V. R18 bypasses IC1 to maintain the c.r.t. heaters at +7.5 V while AD1/1 is in standby; this reduces warm-up time when the display is re-enabled.

Video amplifier

117. The video signal from AB7 arrives on AD1/1 (TP17) at +3.5 V p-p positive-going with respect to ground. After attenuation by R4 and R5, the signal is a.c. coupled to the video buffer TR3 and amplified by the cascode amplifier

TR4 and TR5 to give 35V p-p negative cathode drive with respect to black level set by R17 to around +70 V (depending upon the c.r.t. gun characteristics). D2 conducts during the vertical retrace period, blanking the display to avoid vertical retrace lines appearing on the raster. TR2 clamps the input to ground during horizontal retrace, restoring the d.c. level at the input and preventing black level shifts due to display content variations.

Vertical drive

118. IC2 handles the whole of the vertical drive circuitry, taking the vertical retrace input at TP9 and producing a high output, distortion corrected, saw-tooth current and driving the vertical deflection coils directly. R45 adjusts the display height and R53 the top/bottom linearity balance. At TP10 the +11.7 V supply is allowed to rise to +23 V during vertical retrace supplying IC2 with the required high boost voltage for the output stage in the device; this signal is also used to blank the display during this time by raising the emitter of TR4. A small sawtooth voltage at TP13, generated across R55, is used to provide the vertical component of the dynamic focus correction after shaping by TR6.

Horizontal drive

119. The horizontal retrace pulse at TP11 is inverted and level shifted to trigger monostable IC3 on the rising edge of the pulse. IC3 retimes the retrace pulse and modifies the frequency of the astable oscillator IC4 causing it to lock to the frequency of the incoming pulses. R61 adjusts the phase relationship of the drive from IC4 to that of the retrace pulse by varying the pulse width generated by IC3, thereby giving control over the horizontal position of the display information at TP17 relative to the raster. The network following IC4 shapes the base drive to TR11 effecting a rapid turn-on and turn-off ensuring efficient switching of the horizontal output transformer T1 and deflection assembly. During flyback, the rate at which the voltage at the collector of TR11 is allowed to rise is taylored by the resonant circuit formed by C38 with the primary inductance of T1 and the horizontal deflection inductance. This controls the retrace period and sets the level of the supplementary supplies. TR11 collector voltage at TP12 also drives the black level clamp, TR2, during the 8.2 µs retrace period. The amplitude of the sawtooth deflection current passing through the horizontal deflection coils is modified by the series inductor L1 and the saturable inductor L2 linearizes the sweep. R73,R74,C42 and C43 are damping networks to reduce ringing after retrace.

Supplementary supply generator

120. T1 generates the supplementary supplies for the c.r.t., video amplifier and dynamic focus circuits. Autotransformer action produces a 25 V boost rail smoothed by C36 and during flyback, four further voltages are generated and rectified vis. +11 kV, +540 V, +90 V, -235 V. The Vg2 potential for the c.r.t. at TP8 is derived from the +540 V supply by potential divider R37 and R38.

Dynamic focus

121. The dynamic focus system maintains uniform spot focus as the c.r.t. beam is deflected from the centre of the screen towards the edges. This is effected by modulating the preset d.c. focus potential with an a.c. coupled parabolic waveform correction signal derived from the two deflection circuits. The vertical parabola is produced from the sawtooth generated across R55 by

amplifying and shaping circuit TR6, R22-28 and C8-10. This waveform is mixed with the horizontal parabolic waveform at TP14 into the cascode amplifier TR7 and TR8 to produce a 350V p-p modulated correction signal at TP15. This is coupled by C13 to the focus potential set by R39.

AT2

122. AT2 supports the c.r.t. base socket and has spark gaps punched into it to protect the semiconductors on AD1 in the event of a high voltage flashover inside the c.r.t. Resistors in series with the electrodes in conjunction with circuit capacitances on AD1 limit the voltage risetime of any transients generated during flashover to a safe value.

PROCESSOR AND CONTROL

123. When a front panel push-button is pressed, AB1 causes a processor interrupt (see Fig. 4). The processor responds by decoding the keyboard data from AF1 to determine the position of the button within an 8 x 8 matrix. The button position defines the function which is then acted upon by the processor. Data is routed out to the front panel by the processor to illuminate the annunciator l.e.d's. Direction of data is determined by a two-way buffer between the quiet data bus to the front panel and the I/O bus to the processor and memory. The purpose of the quiet data bus is to free the bus wiring in the keyboard area from the normally continuous trains of pulses from the processor area. Operation of the SET REF FREQ control on AZ1 similarly causes processor interrupts from AB1 and these indicate direction of movement to enable the frequency to be adjusted.

124. Parallel to serial conversion of the housekeeping data between the display unit and the r.f. unit is by means of the AB1 USART. This converts parallel data from the processor into serial data for transmission to the r.f. unit, and receives serial data from the r.f. unit for conversion to parallel data for the processor. The data is conveyed by a 20 mA current loop. Also on AB1 is the master interrupt controller and the GPIB interface. The interrupt controller manages 8 interrupt request lines and assembles the requests into priority order before communicating with the processor. The GPIB interface performs the talker and listener functions for the instrument to enable it to form part of a system acting under the direction of a controller. The instrument GPIB address is set on 5 slider switches on the rear panel. Connections to the GPIB and address switches are all made via AR1.

125. The central processor and the DMA controller on AB3 share the processor address and data buses. The DMA process allows the peripherals on the I/O bus to read or write directly from memory without involving the processor. Main memory is held in 896 K of EPROM while 16 K of RAM is used for scratchpad purposes which includes 4 K used for the A, B and A-B displays as well as for screen annotation. All data transfers between the processor and the memory and I/O data buses are via 2-way buffers. These prevent processor activity from appearing in the memory and peripheral areas. Address lines are decoded on both AB3 and AB1 to provide the chip select signals used to select the required functions. The slave interrupt controller on AB3 complements the master on AB1.

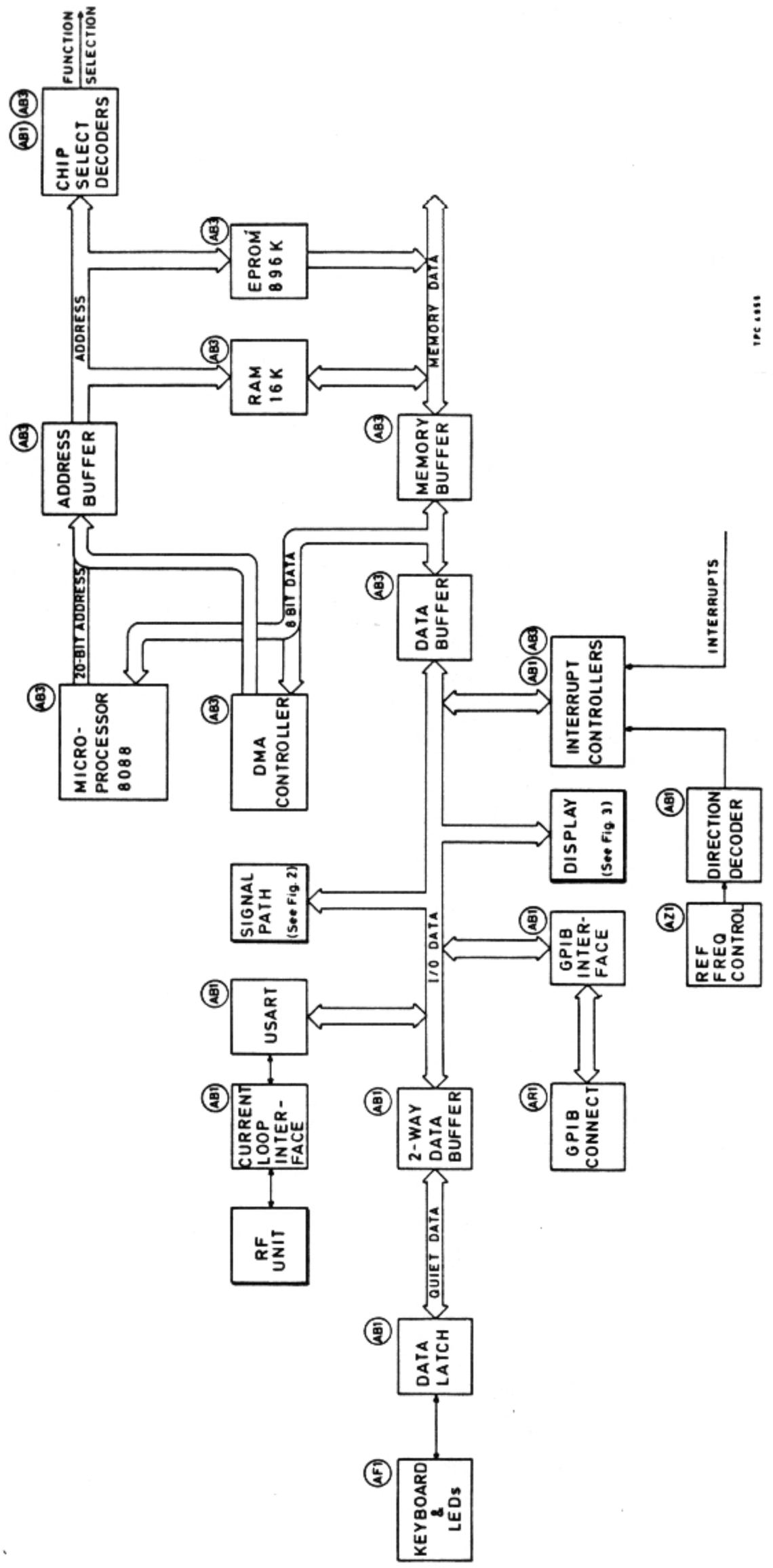


Fig. 4 Processor and control block diagram showing main functions of boards

Board AB1 - I/O & keyboard communication & Board AR1 - GPIB connector

Circuit diagrams : Chap. 7, Figs. 6 & 7

126. Board AB1 contains the keyboard interface, the USART for communication with the r.f. unit, the processor master interrupt controller and the GPIB interface.

Keyboard inputs

127. When a push-button on the front panel keyboard AF1 is pressed, the inputs to AB1 consist of a negative-going signal on the KEY PRESSED line and the push-button identity on the KD0 to 5 lines. The former signal is taken to the key debounce circuit while the latter is applied to latch IC24. The debounce circuit comprises dual multivibrator monostable IC16 and dual bistable IC1. These cater for the different settling times of the Schadow switches at make and break. When a button is pushed resulting in KEY PRESSED, the falling edge to pin 1 IC16a triggers the monostable which produces a negative-going pulse of 5 ms duration (the debounce time for make). At this time IC16b is unaffected by KEY PRESSED since its A input on pin 9 is held high by IC1a output pin 5. At the end of the pulse, IC1a is clocked taking its output pin 5 low. This has two affects. It sets IC1b Q output high, which signal is sent as KEY to the slave interrupt controller on AB3. And to IC16b pin 9 it enables the monostable to be triggered on pin 10 by the next positive edge to appear on the KEY PRESSED line; thus IC16b can detect when a button has been released. When so triggered IC16b produces a negative-going pulse of 20 ms duration (the debounce time for break). This sets IC1a output high and clocks IC1b whose Q output goes low i.e. KEY goes inactive again.

128. When KEY goes high from the debounce circuit it latches the 6-bit key code from AF1 into IC24. Two of the input bits are preset so that an 8-bit word is read from the latch by the processor when it takes CS20 low. Similarly, the bit pattern for l.e.d. illumination is latched into ICs 22 and 23 when CS1A or CS1C is taken low respectively. Latch outputs feed to the l.e.d's via the current limiting resistors R17 and R18. The direction of the data flow between the I/O data bus and the quiet data bus to the keyboard is controlled by the two-way buffer IC21. This is enabled only when one of the CS1A, CS1C or CS20 signals is asserted low. Data direction is determined by the IORD line; for a read operation this line is taken low.

Set ref. freq. control

129. The direction detector for the SET REF FREQ control receiver quadrature outputs from shaft encoder AZ1, and produces pulses on one of two output lines depending upon the direction in which the shaft is turning.

130. The output pulse trains from the encoder arrive at IC14c: let them be X to pin 9 and Y to pin 10. Y is used as the reference phase and is also connected to IC14b pins 4 and 5. When an edge occurs due to movement of the control, a delay is caused by R15, C25 so that pins 4 and 5 are momentarily logically opposite. The trailing edge of the resulting narrow pulse triggers monostable IC13a whose output on pin 13 enables IC15b and IC15c with a window pulse of about 2 µs duration. If X leads Y, then IC14c pin 8 will always be low during the window period, and negative-going pulses will appear at output pin 3 of IC15c. Conversely, if X lags Y, IC14c pin 8 will always be high

during the window period, and negative-going pulses will appear at output pin 6 of IC15b. The pulses from IC15b and IC15c will have the same duration as the window pulse but at twice the frequency of X and Y. The output from IC15b is used as SH UP (IR5) and that of IC15c as SH DOWN (IR4), when they are sent to interrupt controller IC6. An example of operation is shown in Fig. 5.

Display enable

131. When either CS10 or IOWR return high (i.e. when the data has settled), display enable latch IC20 is clocked to latch out c.r.t. control signals DISPLAY ENABLE and CHAR ON. The former signal to AD1 turns on the TV unit, while the latter enables the character data channel in the TV mixer on AB7.

Baud rate generator

132. An input from AB2 at the microprocessor clock rate of 6.25 MHz is divided by 10 by IC12a whose output takes two paths. One path is to IC12b for further division to supply the 125 kHz synchronizing pulses for AC1. The second path is to baud rate generator IC11 which divides the 625 kHz input by 4 to provide the 156.25 kHz transmit/receive clock for USART IC19.

Inter-unit bus USART

133. IC19 is a USART (universal synchronous/asynchronous receiver/transmitter) operating at 9600 baud and performing asynchronous data control between display and r.f. units. It accepts data from the processor in parallel format and converts it into a serial stream for transmission to the r.f. unit. Simultaneously, it can receive serial data from the r.f. unit and convert it into parallel format for the processor. It is interrupt driven and signals to the processor whenever it can accept a new character for transmission or whenever it has received a character from the processor. The processor can read the status of the USART at any time.

Operation

134. At initialization, the processor addresses IC19 by taking chip select line CS0B low then setting A0 to the C/D input high and the write (WR) line low to send a set of control words on the data bus. These define the operating format. Subsequently, a high RESET pulse can force the USART into an idle state to enable a new set of control words to be written in.

135. Serial housekeeping data is clocked in and out of IC19 at the 9600 baud rate derived from the 156.25 kHz input to pin 9. Serial input data is assembled in a receive buffer within the IC and, when the character is complete, RXRDY pin 14 takes the IR1 line high to interrupt controller IC6 to request a processor interrupt. If, however, the assembled character is a Break instruction, it is BD pin 16 instead which requests the interrupt via the slave interrupt controller on AB3/1. When ready to read the character, the processor addresses the USART using the CS0B line, then takes C/D and RD (read) low and accepts the data on the I/O data bus.

136. When able to accept a character for onward transmission to the r.f. unit, the USART takes TXRDY pin 15 high to request an interrupt on the IR0 line to IC6. When ready with a character, the processor places the data on the bus, addresses the USART on the CS08 line, then takes the C/D and WR lines low. The character is accepted by a transmit buffer within the IC and then serially clocked out on the TXD pin to the 20 mA current loop.

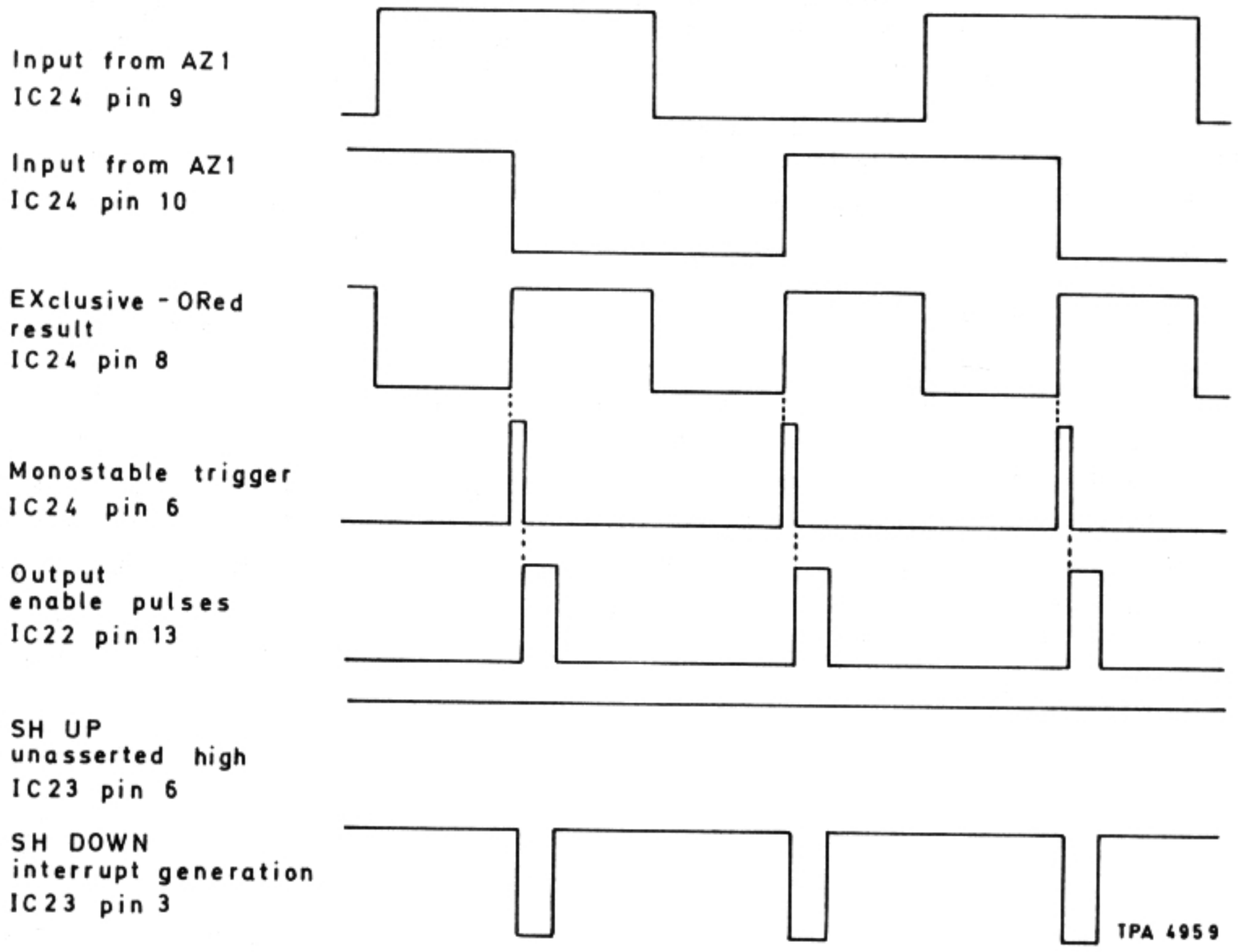


Fig. 5 SET REF LEVEL control direction detector operation. Example shows down movement - AB1

Chip select decoding

137. The 2 to 4 line decoders IC8a and IC8b decode address lines A1 to A3 to form the chip select signals for the GPIB transceiver and address reader as well as for the USART.

Status GPIB address reader

138. Tristate buffer IC5 which is enabled whenever CS0A and IORD are asserted low, performs a dual function. It provides 5 bits of the GPIB address used by GPIB transceiver IC4 for instrument address recognition, as well as providing two status bits. The instrument GPIB address is configured by the user on the 5 switches forming switch bank SA on GPIB connector board AR1. The two status bits are provided by HOT which conveys temperature sensing information from the power supply and EXT STD which is asserted low to indicate that an external frequency standard is connected to the r.f. unit in use.

Interrupt controller

139. Master interrupt controller IC6 manages 8 interrupt requests on lines IR0 to IR7 which are passed in priority order on the INT line to the processor. At initialization, IC6 is enabled by chip select line CS0E and, in conjunction with command select line A0, IOWR (write) is asserted low to allow an initialization command to be written in from the I/O data bus. Amongst its other functions the command configures the interrupt priority levels so that, for this instrument, IR0 has the highest and IR7 has the lowest priority. At a later stage, IORD (read) may be asserted low to read the status and then WR asserted to change the priority or to mask off an interrupt request line.

140. When an interrupt request occurs, IC6, unless engaged with a higher priority interrupt, passes on the request to the INTR input of the processor on AB3. On receipt, the processor completes its current instruction then acknowledges the interrupt by sending a low INTA pulse. This sets a buffer on AB3 for data input as well as being received by the interrupt controller on the INTA line. IC6 sends a call instruction back to the processor which responds by sending two further INTA pulses. These enable IC6 to release its preprogrammed address onto the bus in the order low byte, high byte. The address contains a pointer to the area in memory holding the routine to service the interrupt.

GPIB interface

Operation

141. The function of IC4 is to provide communication between the instrument and the General Purpose Interface Bus (GPIB). The IC is a talker/listener which, in conjunction with the transceivers, implements all the necessary GPIB functions for the instrument. It is processor controlled and has capabilities which include data transfer, handshake protocol, talker/listener address recognition, service request and serial poll.

142. The interface takes care of data transfer as well as decoding control messages. Control messages and addresses are passed on the the data bus by means of the handshaking process with ATN asserted to differentiate them from data. Control messages such as SPE, SPD used for serial poll are decoded and the function carried out. The IC also performs address recognition. The data on lines DIO 1 to 5 is compared for equivalence with data set on the 5 rear panel address switches (SA on board AR1). When a possible address is recognized and providing certain other conditions are satisfied, the data on DIO lines 6 and 7 is decoded to determine whether the instrument is being addressed as a talker or a listener. When designated a talker, the interface transfers data from the processor by means of a talk handshake to listeners via an internal register to the transceivers configured to send. When designated a listener, data is received via the transceivers by means of the listen handshake and stored in an internal data register.

143. IC4 contains 16 registers (8 read, 8 write), 2 for data transfer the rest for interface control, status, etc. Address lines A0, A1 and A2 are used to select the required internal read/write register in conjunction with IORD and IOWR lines. Reading or writing then takes place when the CS00 line is taken low.

144. Data outputs and inputs are via buffers IC2, 3, 17 and 18 with the direction of data transfer controlled by the T/R1 line being taken high for outputs and low for inputs. Additionally, this line is used for the

handshake process. For example, a low on the line, after inversion by IC9a, enables the listener handshake signals NRFD and NDAC to be asserted low on the bus while reinversion by IC9b ensures that the complementary DAV talker function is simultaneously disabled. The sole function of T/R2 is to set the bus management EOI line low for reception or high for transmission.

General purpose interface bus

145. The bus, which is entirely passive, uses 16 signal lines to connect all units of a system in parallel. These lines are functionally sub-divided into data, transfer and interface management buses (see Fig. 6).

Interface management bus : Manages the orderly flow of data across the interface and consists of 5 wires which carry the following signals:-

Interface clear (IFC) : Sent by the system controller to clear all interfaces so that they set to an initial condition.

Remote enable (REN) : Sent by the controller to enable instruments to be placed under remote control.

Attention (ATN) : Sent by the controller to indicate that an address or command is on the data lines.

End of identify (EOI) : An instrument or controller signal sent to indicate the end of a message.

Service request (SRQ) : Sent to a controller by an instrument to indicate that it needs service (e.g. has data to pass).

Transfer bus : Co-ordinates the flow of data and comprises 3 lines which are used for the handshaking process, by which a talker or controller synchronizes its readiness to send data with a listener's readiness to receive data. The handshake signals are:-

Not ready for data (NRFD) : Asserted (low) by a listener when it is active and not yet ready to receive data. Set high to signal its readiness to receive data.

Data valid (DAV) : Asserted by a talker to indicate that the data it has placed on the data bus has settled and may be accepted.

Not data accepted (NDAC) : Asserted by a listener when receiving data. Set high as confirmation of receipt of data.

Data bus : Comprises 8 data input/output lines DIO 1 to 8 and is used to transfer the data (commands, addresses and instructions) in bit parallel, byte serial form.

Bus operation

146. A sequence of messages may be commenced by the controller asserting IFC on the management bus to set the interface to its initial condition. The controller then asserts ATN and designates which instruments are to be listeners by sending their listen addresses on the data bus. Similarly, the controller designates the talker (only one instrument may talk at a time) by sending its talk address. Upon the controller removing ATN the talker is

free to send data to the listeners by means of the handshake process. The talker concludes the sequence by EOI and this tells the controller to resume control. The controller may now switch the talker and all listeners into the inactive state by sending UNT (untalk) and UNL (unlisten) on the data bus before selecting the next participants.

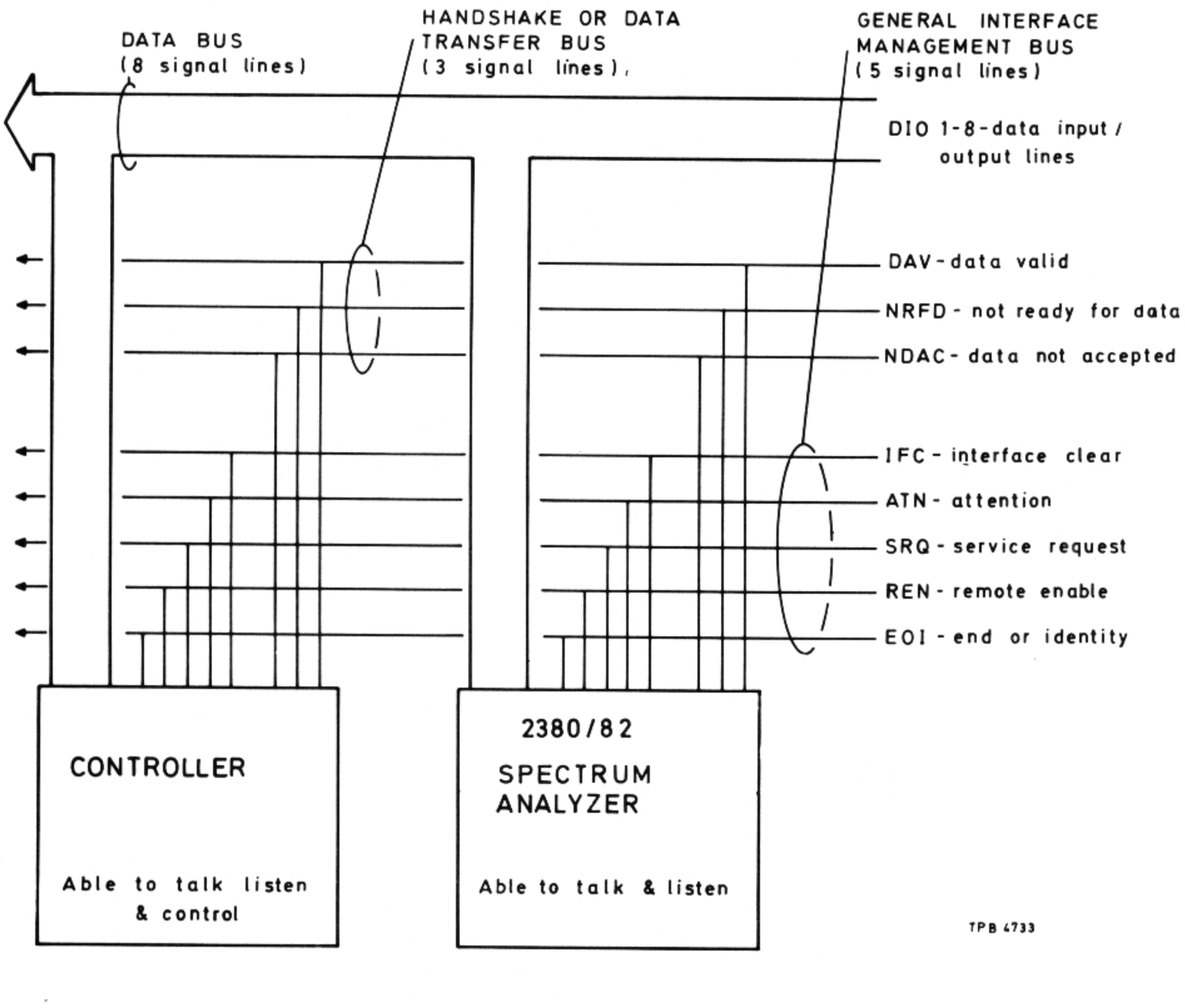


Fig. 6 General Purpose Interface Bus (GPIB) structure - AB1

Handshake

147. The handshake is used whenever data is transferred on the bus. When a signal is asserted the function indicated by the line is carried out, e.g. NRFD is asserted to signify the listener's unreadiness to receive data, and unasserted or removed when ready to receive data. Briefly, a typical handshake is as follows:-

(1) Talker (controller) places a byte on the data bus with DAV initially unasserted to show data is not yet valid.

(2) When all listeners are ready to receive data, NRFD is removed with NDAC at this time asserted.

(3) After a delay to allow data bus to settle, talker asserts DAV to show data is valid and may be accepted.

(4) Data byte is transferred, then listeners assert NRFD. When all listeners have accepted the byte, NDAC is removed to signify receipt.

(5) Talker removes DAV, listeners assert NDAC, and bus reverts to its initial condition ready for next data byte.

The handshake procedure is shown in Fig. 7.

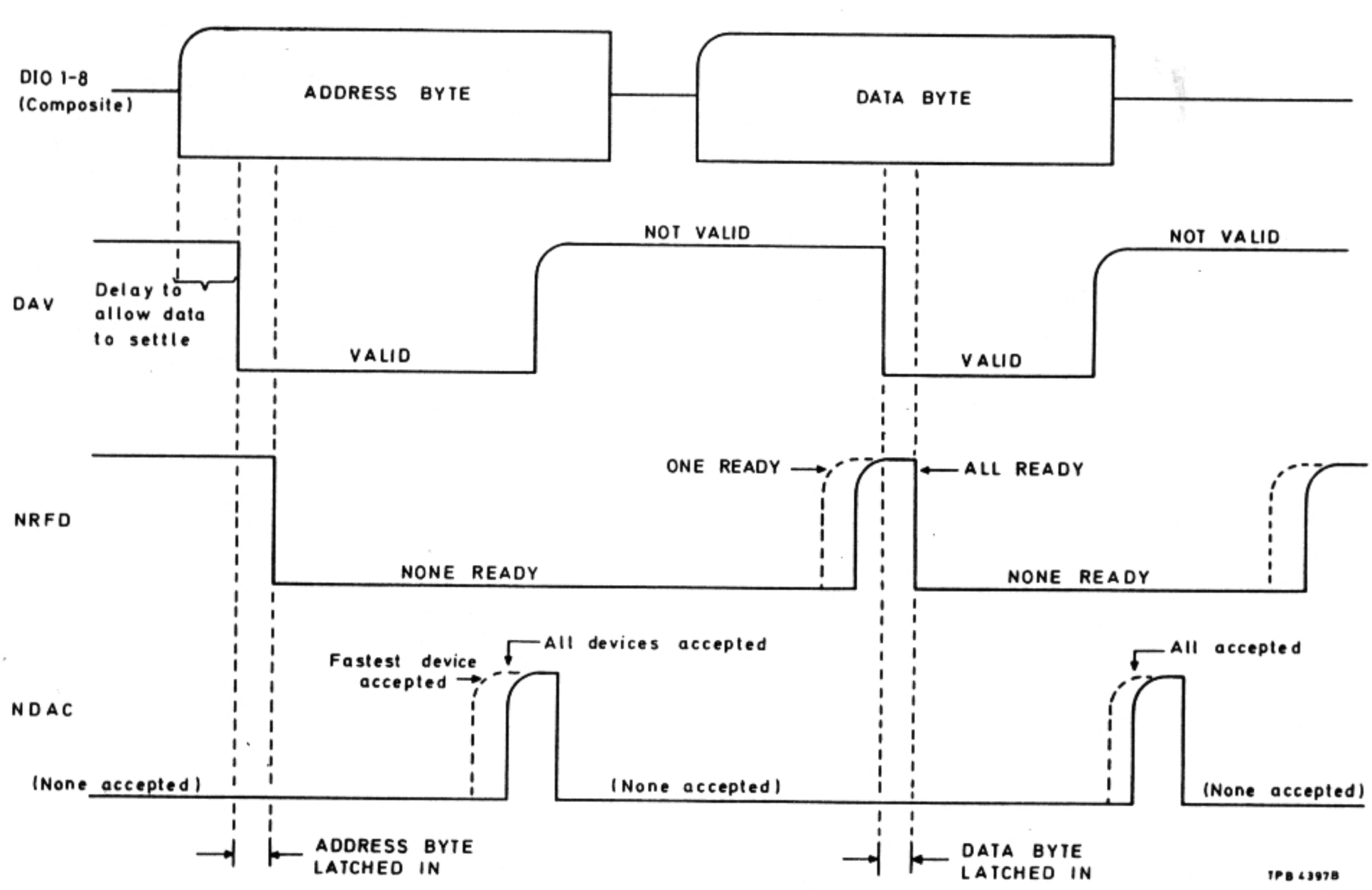


Fig. 7 Handshake procedure - AB1

Board AB3/1 - Processor, memory and chip select

Circuit diagrams : Chap. 7, Figs. 10 & 11

148. Board AB3 contains the microprocessor, the DMA controller and the RAM and EPROM memory banks.

Microprocessor

149. The central processor is an 8-bit Intel 8088 with 16-bit internal architecture. It uses a multiplexed data bus to accommodate the 20-bit address. This is split between the 8-bit high byte address bus, and the 8-bit data bus with the 4-bit upper address bus. Output lines A8 to A19 carry the high order memory address, with A8 to A15 valid for all bus clock cycles. Multiplexed input/output lines AD0 to AD7 carry the low order memory or input/output (I/O) address during the first bus clock cycle, and then carry data during the remaining clock cycles. ALE (address latch enable) is used to differentiate between data and address; when it is taken high the contents of the multiplexed data bus are treated as an address and latched by IC23. And since the upper address on lines A16 to A19 is only valid during the first clock cycle when ALE is active, this signal also latches IC4. IO/M is used to differentiate between an I/O and a memory address; when it is taken low the on-board memory is addressed. WR (write) and RD (read) asserted low enables the memory or I/O device selected by the address bus to be written into or read out from respectively. They also indicate that the data bus is available for a data transfer operation. For internal timing, IC1 supplies the CLK input with a signal at 1/3 of the frequency of the 12.5 MHz clock from AB2.

150. The 8088 has two interrupt inputs, INTR and NMI. Non-maskable interrupt NMI has the higher priority and is edge-triggered. This interrupt occurs at the conclusion of the FRAME pulse when enabled by data latch IC3b. Interrupts result in the transfer of control to a new program location. For NMI the processor automatically calls the required servicing routine. Interrupt request INTR is active high and is controlled in priority order by the interrupt controller on AB1. For INTR the processor responds with INTA (interrupt acknowledge), on receipt of which the interrupt controller sends the service routine address (vector) on the I/O data bus. To obtain this vector, INTA is also used to enable the I/O data bus buffer IC26.

Direct memory access (DMA) controller

Function

151. The primary function of DMA controller IC17 is to generate, upon a peripheral request, a sequential memory address which will allow a peripheral to read or write data directly from or to memory. DMA requests are serviced in priority order.

Internal registers

152. The DMA controller's internal registers are programmed by the processor when it selects the controller as an I/O device by taking CS4X low. The registers are then addressed on the A0 to A3 lines and data is written into them or read out from them when IOW or IOR is asserted respectively.

DMA operation

153. When the DMA controller receives a data transfer request from an enabled peripheral on one of the four DRQ lines, and it is in the idle state, i.e. not in control of the address and data buses, it asserts HRQ to request control from the processor. IC15 completes its current task then responds with HLDA to indicate that it has relinquished control. IC17 then addresses the appropriate area in memory. It outputs the most significant address byte on AD0 to AD7 which is strobed into latch IC24 by ADSTB and placed on the address bus by AEN. The least significant address byte is output on A0 to A7 to the address bus via buffer IC18. To enable the memory bank for a read or write operation, the controller takes the MRD or the MWR line respectively low. Finally, DACK is sent to the requesting peripheral as notification that it has direct access to the memory.

154. When enabled by DACK0 with IORD asserted low to IC21a, board AB2 reads 2 bytes from memory for its max and min output latches. AB4 is enabled to write 5 bytes to memory - 2 each for A and B displays and 1 for the graticule - when enabled by DACK1 with IORD asserted low to IC21d. When DACK3 is taken low, the c.r.t. controller on AB7 is enabled to read data in blocks for display.

Decoder

155. Quadruple 2 to 1 line selector IC16 decodes RD and WR into MEMR and MEMW respectively for memory read and write operations when its S input is taken low by the processor. When S is taken high, RD and WR are decoded to IOR and IOW respectively to enable the processor to read or program the DMA registers of IC17.

Buffers and latches

156. Both the processor and the direct memory access controller (DMAC) multiplex their data and address buses. When the processor has bus control, the upper and low byte parts of the address are latched out by IC4 and IC23 when strobed by the high ALE signal. The high and low bytes of the address feed directly to the address bus via buffers IC19 and IC18 respectively. And with the DMAC not in control, AEN is held low which enables buffer IC5 to complete the 20-bit address by outputting the 4-bit upper address. For a data transfer, ALE is taken low which disables the address latches.

157. When the DMAC has bus control, ADSTB is used as the strobe to latch out the high byte of the address from IC24. AEN is asserted high and this is inverted by IC20e to enable the latch as well as to select the preset upper address from buffer IC5. For a data transfer AEN is taken low to disable the address latch.

158. The data bus has two buffers in parallel, IC27 to the memory bus and IC26 to the I/O data bus. Each is enabled by a low on pin 19 only when its respective bus is read/written. For a write operation, pin 1 is taken high while for a read it is taken low.

159. The above simple scheme becomes slightly complicated under two circumstances. First, when the processor is programming the DMAC it sees the latter as being in the IO map, and since they are directly connected (i.e. on the same side of the I/O data bus buffer), the processor disables IC26 on pin 19 using the CS4X line to the DMAC in order to prevent possible bus contention. Secondly, when the processor wants to receive a vector from the

interrupt controller on AB1, which is on the I/O bus, it has to be able to 'force a path' through the buffers; for this reason, INTA from pin 24 of IC15 is combined with the other enabling/direction control signals for ICs 27 and 26.

Memory banks

160. The operating program is contained in 7 EPROMs (ultra-violet Erasable and electrically Programmable Read Only Memories) each of which contains 256 K bytes of memory. ICs 10 to 14 and 32 are directly controlled by IC7 which decodes the selection logic on address lines A15 to A18. IC33 is selected by the additional input of the A19 line to AND-gate IC22a. ICs 8 and 9 each contain 8 K bytes of RAM (Random Access Memory) used for scratchpad read/write operations. These are selected by IC6 which decodes A13 to A15 to select the required memory, and is itself enabled by A16 and A18. When the instrument is switched off the contents of these memories are lost.

Chip select decoding

161. ICs 30 and 29 perform chip select decoding for the IO map. IC29 is enabled during a processor I/O operation when AEN and IO/M are both low, and the binary address on the A4 to A6 lines is decoded to select 1 of 8 outputs. One of the outputs is used as an enable signal for IC30 and when IOEN also goes low for an I/O read/write the IC decodes the A1 to A3 address to select 1 of 8 outputs.

Interrupt controller

162. Slave interrupt controller IC28 can manage up to 8 interrupt requests on lines IR0 to IR7 and passes them in priority order on the SLAVE INT line to the master interrupt controller on AB1. The two interrupts managed are KEY to detect a keyboard button operation, and BREAK to detect a break message to the inter-unit USART. At initialization, IC28 is enabled by an output from chip select decoder IC29 and, in conjunction with command select line A0, IOWR is asserted low to allow an initialization command to be written in from the I/O data bus. The command may be used to configure the interrupt priority levels or to mask off an interrupt request line.

Board AF1 - Keyboard matrix and encoding

Circuit diagram : Chap. 7, Fig. 29

163. This board is mainly a static encoder for the 40 push-buttons which are arranged at the nodes of an 8 x 8 matrix. The code used to represent each button is derived from the node address; rows are numbered 0 to 7 and columns are numbered 8 to F hexadecimal. The code used to represent each button is derived from its node address, for example the dB button is coded A3H. Columns feed directly to decoder IC4 while rows feed to decoder IC1 via the 8 elements of ICs 2 and 3. With no buttons pressed, all the comparators' inverting inputs are held low by the elements of R2 connected to ground, while the non-inverting inputs are held slightly high by the potential divider formed by R4,R5. Consequently, the inputs to row decoder IC1 are held high as are all the inputs to column decoder IC4 due to the action of pull-up resistors R1. When a key is pressed, it shorts together a row and column of the matrix. This forms a potential divider from the respective elements of R1 and R2 causing the appropriate input lines to the decoders to be taken low. 8 to 3 line decoders IC1 and IC4 supply the l.s.b's and m.s.b's of the button

address respectively. Due to IC1 pin 5 being tied to ground, any input going low causes pin 14 also to go low and this feature is used to generate KEY PRESSED to AB1 for key debounce purposes.

164. The l.e.d's installed in some of the push-buttons have their anodes connected to the +5 V supply and their cathodes separately driven via selection logic from AB1.

Board AZ1 - Shaft encoder

Circuit diagram : Chap. 7, Fig. 30

165. This board forms part of the REF FREQ control. Its function is to indicate the direction of movement of the shaft of the control to board AB1. Power is supplied from AB1 on contacts 1 and 3 to two l.e.d's. These are optically coupled via a pierced disk mounted on the shaft to photo-detectors connected to contacts 4 and 5. By this means, as the shaft is rotated, quadrature pulses are generated for subsequent decoding in board AB1 to determine the direction and rate of movement of the control.

POWER SUPPLY

166. AC mains from the rear panel INPUT connector enters via a fuse in both the live and neutral leads and is connected by the front panel SUPPLY ON switch to the line filter on AC3 (see Fig. 8). A soft start circuit on AC1 follows which limits the maximum line current for 0.5 s after switch on. The LINE VOLTS SELECTOR on the rear panel changes the mains transformer primary tap for either 115 V or 230 V operation and reconfigures the AC1 full-wave rectifier in the 230 V position to a voltage doubler in the 115 V position. After smoothing, the h.t. supply of nominally ±170 V is fed through fuses FS1 and FS2 to the phase splitter and output switches operated by an SMPS controller. 12 V auxiliary power supplies the controller, provides the line trigger for the associated r.f. unit and, after regulation, supplies +5 V for the monitoring circuits.

167. The switched mode power supply controller on AC1/1 operates at 125 kHz in synchronism with the r.f. unit frequency standard. The current limit detector checks the supply current to the primary of the transformer used for d.c. to d.c. conversion in order to provide protection against an overload or a shorting of the secondaries. Protection is provided by the SMPS controller switch drive being inhibited. Additional protection is provided by the controller being reset, causing a soft start if possible, whenever AC2/1 detects an overload overvoltage or overheat condition, or when no r.f. unit is connected. A feedback line is used to control the switching duty cycle and hence the output power. A heatsink-mounted thermistor controls the speed of the cooling fan. If the instrument starts to overheat the processor causes a message to be displayed to that effect and, if the condition worsens a controller reset is generated. Rear panel l.e.d's illuminate on the occurrence of any of the above fault conditions.

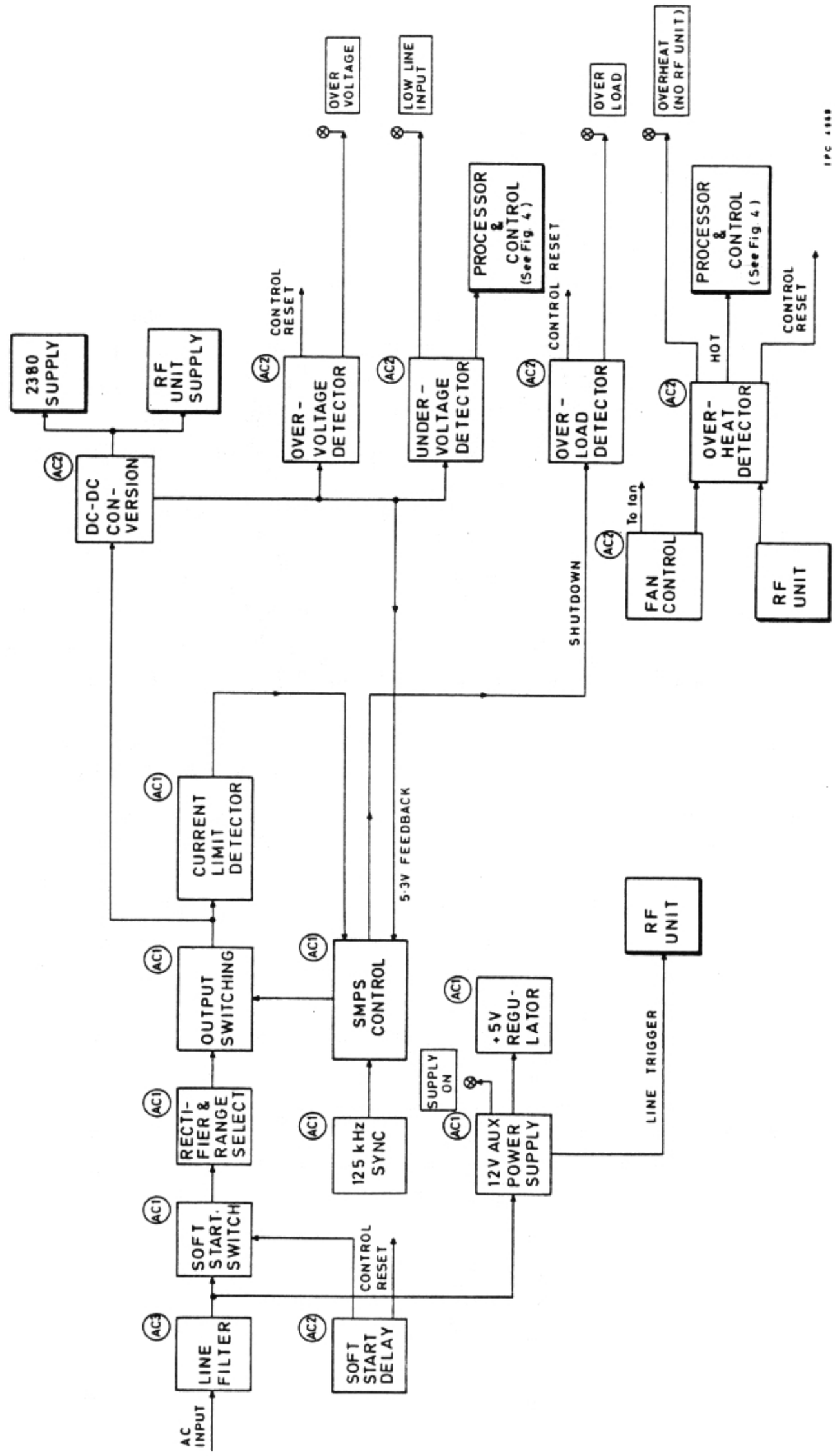


Fig. 8 Power supply block diagram showing main functions of boards

Board AC1/1 - Input control of SMPS & Board AC3/3 - Line filter

Circuit diagrams : Chap. 7, Figs. 25 & 27

General

168. AC1/1 consists of the high voltage switching circuits, the auxiliary supply and switching controller. Live and neutral from line filter AC3/1 is rectified to give a nominal +ve and -ve 170 V h.t. supply which is switched alternately by TR1 and TR2 into the h.f. power transformer on AC2/1 under control of IC2. The duty cycle on-time of both TR1 and TR2 is adjusted by IC2 to regulate the low voltage outputs of the supply against variations in line voltages and load currents by sampling one of the secondary outputs and comparing this to its own stable reference. Additional inputs to IC2 protect both the load and the supply from overload by sensing the output voltage and power transformer primary current. C1,C10,14 and 20 form part of the line filter, attenuating switching noise generated by the converter.

Soft-start

169. R1 and relay RLA form a soft-start circuit designed to limit the maximum line current taken at switch-on due to the capacitive load of the h.v. reservoir capacitors C2-5. A delay circuit on AC2/1 prevents RLA from being energized for approximately 0.5 s after switch-on. During this time C2-5 can only charge through R1. R1 limits the initial charging current to less than 3 A even under worst case conditions of maximum line input voltage and switch-on time (input waveforms at peak voltage).

170. After the soft-start delay, pin 8 on PLC is taken low and RLA energizes thereby shunting R1 which dissipates an insignificant amount of power during normal supply operation.

Rectifier and reservoirs

171. S1 selects either 115 V (105 V - 120 V) or 230 V (210 V - 240 V) line input voltage. It changes the primary tap on T1 and reconfigures D2 from a full-wave rectifier in the 230 V position, to a voltage doubler in the 115 V position maintaining an h.t. supply of nominally + and -170 V. R4 and R5 across capacitors C2-5 discharge the h.t. supply after switch-off while a relaxation oscillator C6, R6 and LP1 warns of the presence of voltages greater than 60 V across the h.t. rails; frequency, (between 1 & 5 Hz) is proportional to voltage. D3 and D4 protect the f.e.t's from high transient voltages by conducting in the event of either rail exceeding 220 V. FS1 and FS2 isolate TR1, TR2 and associated circuitry in the event of a fault which would draw heavy currents from the reservoir capacitors possibly damaging the p.c.b. L1 and L2 filter the h.t. lines of high frequency switching currents.

Auxiliary power supply

172. An auxiliary 12 V supply, T1, D7, C11, IC1 and C12 powers the control circuit and provides an isolated source of line frequency needed for the line trigger mode in the r.f. units. This 12 V line is further regulated to +5 V (+/- 2%) by IC2, TR3, R13, C13 and C15. TR3 buffers the 5 V reference from pin 18 of IC2, R13 supplies IC2's internal regulator while C13 and C15 provide decoupling of the supply lines. The stabilized +5 V is used on AC2/1 (via PLC pins 10 and 14) to supply the monitoring circuits.

Phase splitter and output switches

173. IC2 drives the two power f.e.t´s via T2 which functions both as an isolating element between the control electronics and line connected circuit and a phase splitter. During the first period of the switching cycle pin 13 is driven high (+12 V) while pin 16 is held at 0 V for time ´t´. During this period, TR1´s gate is driven 12 V positive while TR2´s gate is driven 12 V negative; consequently TR1 rapidly conducts as the gate potential rises above the f.e.t´s gate threshold of 2 V. The transition period is controlled by the time constant of R7 + R8 and the f.e.t. gate capacitance. While TR1 is on, current flows in the power transformer primary (T1 on AC2/1) via C9, a d.c. blocking capacitor, and T3 primary. Current is reversed when TR2 is on and TR1 is off in the second half of the switching cycle when IC2 pin 16 is at +12 V and pin 13 is held at 0 V for a second period ´t´. To ensure that simultaneous conduction of both TR1 and TR2 is prevented, diode D5 shunting R7, and D6 shunting R9 reduce the discharge time of the f.e.t. junction capacitance effecting rapid turn-off. Snubbers C7, R11 and C8, R12 damp any oscillation of the primary circuit during the time when neither TR1 nor TR2 are conducting.

SMPS controller

174. ´On´ period, ´t´, is dependant upon the feedback voltage from pin 15 of PLC. The variation of this as a result of line or load changes is attenuated by R19 and R20 and compared in IC2 with the +5 V reference. R19 gives a ± 300 mV adjustment around the nominal 5.35 V to accommodate tolerances in the +5 V reference and R20. The amplified and inverted difference voltage is compared again with a ramp generated by the internal oscillator in IC2 whose output controls the logic and output buffers such that, at the start of the switching cycle one output is enabled and remains active (+12 V) until the output level from the ramp generator is equal to the amplified error voltage whereupon the pulse is terminated. In this way, as the power supply output increases (leading to a reduction in the error voltage), ´t´ is reduced in duration which reduces the amount of power transferred to the secondaries. C19 and C21 with R21 and R30 in conjunction with the +5.35 V rail filter components on AC2/1 reduces the loop gain of the system above 150 Hz to maintain stability whilst giving an acceptable transient response.

175. Free running frequency of the oscillator is inversely proportional to the product of C18 and R14 and is approximately 120 kHz. When the supply is synchronized however, this is increased to 124.6875 kHz by means of the external SYNC input on pin 4 of PLC. The t.t.l. +ve going edge of sync. (at 125 kHz) is firstly a.c. coupled and differentiated by C22 and R27 and then clipped by D13 to clip negative transitions. TR4 is wire-ORed to the SYNC input of IC2 pin 12 and on driving this input low, discharges the timing capacitor, terminating the oscillator cycle prematurely and effectively synchronizing the controller by restarting the charging sequence. To stop spurious sync. inputs from upsetting the controller during power-up, a SYNC INHIBIT pulse, active for 930 ms after the supply is turned on drives TR5 into saturation and ground, any signals arriving at the base of TR4. By linking pins 2 and 3 on PLE, the external sync. may be disabled manually during the testing of the 2380 logic boards when the sync. integrity might be affected resulting in supply malfunction and shutdown.

176. Three methods are available to inhibit the controller, IC2 whilst in operation namely:- SHUTDOWN, RESET and CURRENT SENSE input.

177. The SHUTDOWN port, pin 8 of IC2, terminates the output drive when low and is wire-ORed with the output of the current sense amplifier output. It is used to drive the input of the overload sampler on AC2/1 in order to monitor overloads on the the p.s.u. and to shut it down if necessary.

178. The RESET input to pin 5 IC2 is driven from AC2/1 and when active (low) resets the controller. After 520 ms from switch-on, the soft start interval, the reset input is released and the controller itself executes a soft start whereby, under control of the soft start timing capacitor C17, the output duty cycle increases from zero until the error amplifier assumes control and regulation is maintained. This method of starting prevents supply output voltage overshoot which would occur at switch-on because of the delay inherent in the regulator feedback loop. This reset input is released as relay RLA is energized. R23 ensures that should the supply be switched on while PLC is disconnected, the controller remains reset until PLC is reconnected whereupon the supply soft starts safely.

Current limit detector

179. The Current Limit Detector, T3, R15-17, D11 and D12 protects the power f.e.t´s from damage from excessive primary current brought about by the shorting of any of the secondaries on AC2/1 or a general overload exceeding 250 W. T3 is a current to voltage transformer giving 2 V across R15 for each Ampere flowing in the primary. D11 and D12 rectify the signal while divider R16 and R17 give an input to IC2 pin 7 of 100 mV (the current sense amplifier threshold) at a primary current of 3 A. Under normal full load the primary current should not exceed 2.5 A peak.

Board AC2/1 - Output & monitors of SMPS

Circuit diagram : Chap. 7, Fig. 26

180. AC2/1 contains the power transformer, all l.t. rectifiers and smoothing components, output voltage monitoring, cooling control, and power-up sequencing.

Input and rectifiers

181. Seven l.t. supplies are produced directly from T1, and a further two, -5 V from the -8.5 V line and -12 V from the -14.5 V line. All outputs follow the same principle whereby a centre-tapped secondary is full-wave rectified by either two fast recovery diodes, for a single +ve or -ve output, or four diodes for a balanced +ve and -ve output.

182. The series R/C connection across each secondary forms a snubber to critically damp oscillations produced during switching by the junction capacitance of the diodes with the leakage inductance of the transformer secondaries. The square-wave output from the rectifiers is smoothed by a series choke and capacitors to ground with bleed resistors lightly loading the outputs to prevent them rising to an unacceptably high level should the supply be unloaded. The bleed resistors also ensure that any charge on the smoothing capacitors (especially in the case of the +80 V line) is quickly dissipated at switch-off.

183. D1 is a dual, centre-tapped Schottky rectifier mounted on a heat-sink, the temperature of which is monitored by a thermistor, R15, used to control the fan speed. R14 across the +5.35 V output loads this rail which is used as the feedback supply to the controller on AC1/1. Without sufficient load here, with the supply operating open-circuit, peak-detection at C1 will produce a sufficiently high feedback voltage to cause the controller to reduce the duty cycle to zero until the feedback decreases below +5.35 V. D2 prevents any high voltage transients on the output, by conducting at approx. 7 V, and acting as a fast over-voltage suppressor under possible fault conditions until the controller is shut down by the active over-voltage detection circuitry IC2b.

184. The auxiliary supply at +5 V from AC1/1 is decoupled by C29 and used to power the monitoring circuit on AC2/1. R1 and R2 with C30 provide a +2.5 V reference for use by comparators IC2.

Fan control

185. Fan speed is controlled indirectly by the temperature of D1 and associated heatsink. R15 is a negative temperature coefficient thermistor and in series with R16, which is normally connected to the -14.5 V line, produces a voltage at TP12 which is proportional to the temperature of the heaksink. This voltage is buffered by TR1 and drives the fan while D15 protects TR1 against reverse base emitter breakdown and D17 ensures that the fan has at least 13.8 V or 19 V applied to it (depending upon the setting of PLF) even under cold switch-on conditions when R15's resistance is high. C21 decouples the fan from the supply by providing the high current pulses required during commutation.

186. The voltage at TP12 is divided by R17 and R18 and is monitored by two comparators in IC2. IC2c's output goes low when the voltage at pin 10 rises above that at pin 11 (+1.5 V) set by potential divider R19, 22 and 23 corresponding to a voltage at TP12 of 4.8 V and a heatsink temp. of 80^{0}C. This output is taken via PLD to the processor and is used to warn the operator of an excessive rise in temperature in the instrument by means of a message on the display. Allowing the heatsink temperature to rise further, will result in the second threshold of +2 V to be exceeded and detected by IC2a. As IC2a's output drops, IC4b, an R-S latch, will be set and the supply controller will be shut down via the reset line, by IC5c. LED D25 indicates this on the back panel. A secondary function of the temperature monitoring circuit is to detect the absence of an r.f. unit power lead at switch-on and warn the user by resetting the supply and illuminating D25. Pin 28 SKA is normally looped through the power cable to -14.5 V in the r.f. unit to enable the temperature sensing circuit to function. Should this pin become open-circuit, then R51 pulls R16 up to the +14.5 V supply which activates the overheat comparator.

Voltage detection

187. The +5.35 V output is monitored by IC2b and IC2d. If the output exceeds 5.8 V then IC2b sets latch IC4c which resets the controller. D23 shows this. A secondary sense for over-voltage, D22 and R57, wire-ORed with the output of IC2b, detects a voltage on the -14.5 V line of less than -18 V again tripping the over-voltage latch. (This is in case the +5.35 V feedback line is affected i.e. D1 failing). To warn of possible instrument malfunctioning should the supply line be interrupted or fall outside the line input requirements (<95 V or <220 V), IC2d sets IC4a illuminating D24: LOW LINE INPUT. During power-up, IC2d buffered by IC5f, holds the reset inputs to the

instrument processor low until the +5.35 V line has stabilized and is wire-ORed to the reset circuits on the processor boards.

188. Line frequency input from AC1/1 is squared by IC6b and buffered by IC5e to be used by the r.f. units for triggering the sweep in line trigger mode. Also, the output from IC6b is used as the sampling period for the Overload Sampler IC7 whereby C37 and R29 differentiate the line frequency square-wave and after inversion by IC6e produce a 100 µs positive pulse to reset IC7 at line frequency. The Overload Sampler totalizes the transitions on the SHUT-DOWN line from AC1/1 and sets the overload latch, IC4d, if more than 127 pulses are received in 1 sampling period (2.2 - 22 ms depending upon line frequency). D26 gives a visual indication why the supply has reset. This arrangement protects the supply and loads against overloads (short circuits) without being susceptable to transient disturbances (during synchronization to the external sync. input for example).

Start-up sequencing

189. Two monostable circuits IC3a and IC3b provide start-up sequencing when the supply is first switched on. When the +5 V auxiliary supply is active, C22 charges through R26 and triggers the monostable outputs in IC3 to a high state. IC3a via IC6c and IC5b hold the supply controller RESET line low for approx. 520 ms during the soft start period and also resets the Overload and Overvoltage latches. After this delay, the soft start circuit on AC1/1 is bypassed and the converter begins operation. While the supply stabilizes, IC3b, via IC6a, holds the LOW LINE and OVERHEAT OR RF UNIT latches reset and inhibits the external sync. for a further 410 ms following the soft start delay.

PENPLOT AND RGB VIDEO (OPTIONAL)

190. D-A converters on board AB8 supply the drives for the X and Y axes of a pen recorder, with an additional signal provided to control the penlift operation (see Fig. 9). The RGB circuit outputs provide a red graticule, a green A display, a blue B display and a white display which is used for both markers and annotating characters. The horizontal and vertical synchronizing signals are combined for output on a single line. Provision is made for a composite video output for a monochrome monitor.

Board AB8 - Penplot & RGB video

Circuit diagrams : Chap. 7, Figs. 22 & 23

Latch selector and installed options indicator

191. During an IO read or write operation, latch selector IC13 decodes the A0 to A2 inputs to take one of its eight outputs low when enabled by CS5X going low and A3 going high. When output Y7 goes low in this way, the processor is able to read installed options indicator IC20. At the time that an option is installed, a link is inserted between the IC's input and ground so that when the processor reads a low data bit it can determine which option is fitted. When output Y2 goes low it clocks latch IC19 which controls the bleep tone generator. At the conclusion of the read or write operation, AND-gate IC7b output goes high causing all of the IC13 decoded outputs to go high. The resulting rising edge on a selected Y0, Y1 or Y3 output line is used to clock data latches IC4 or IC5 for the pen recorder or IC14 for the colour video generator.

Pen recorder drive

192. When CS58 or CS59 is taken high, data byte latch IC4 or control byte latch IC5 latches out its data to D-A converter IC3 or IC2 respectively. The data latched from IC4 supplies the pen recorder X axis, that latched from IC5 supplies the Y axis as well as operating RLA controlling the penlift operation.

193. Digital-to-analogue converter IC3 has an output resolution of 1024 steps and supplies the RECORDER X CHANNEL drive. The required 10 bits are supplied in parallel-bit, byte-serial form from IC4. Firstly, 8 bits on lines D0 to D7 are strobed into IC3 on the rising edge of LBS (Low Byte Strobe). Then a further 2 bits on lines D0 and D1 are strobed in on the rising edge of HBS (High Byte Strobe). The minimum output step size is determined by the reference output from IC6 level-shifted by Ref Volt Generator IC1a. When LDAC is taken high, D-A conversion takes place. The resulting IOUT current via IC7a varies the conduction of output buffer TR6 which supplies the feedback current to the converter's RFB input. This current produces the pen recorder X-axis voltage across R41.

194. To produce the RECORDER Y CHANNEL output, IC1a sets the minimum step size, while IC2 operates similarly to IC3 but is a 9-bit D-A converter whose output thus has a resolution of 512 steps.

Bleep tone generator

195. When CS5A goes low, it clocks latch IC19 whose outputs control the operation of the bleep tone generator which provides an audible warning signal. The generator consists of monostable IC18a, astable IC18b and piezo electric sounder XL1. The frequency and oscillation of IC18b is set to approximately 3 kHz by timing components R56, R57, C52 - and there are two pitch settings which are determined by the logic levels on the PITCH line. For interrupted sound operation, a falling edge on the BLEEP TRIG line takes IC18a output high for the period set by R52, C51 to enable oscillator operation after which the output ventures low to reset the oscillator. For uninterrupted operation, the CONTINUOUS line is held high to IC18b pin 10 to prevent a reset occurring.

Colour video generator

196. The logic level of data line D0 to D-type bistable IC14 determines whether the picture hue selected is a loud, foreground one or a quiet background one. When D0 is low and IC14 is clocked by CS5B, buffer IC15 is enabled to pass the video inputs from AB7 out to three colour combiners. The MINOR and MAJOR graticule inputs provide the RED VIDEO output, the A display INFIL and LINE inputs provide the GREEN VIDEO output and the B display INFIL and LINE inputs provide the BLUE VIDEO output. Each one of the inputs forming a pair is passed through a different value resistor. Thus the MINOR, A INFIL and B INFIL inputs are respectively fed through R9, R17 and R25 whose values are chosen so that they produce a dimmer display than the MAJOR, A LINE and B LINE inputs which are respectively fed through R10, R18 and R26. To produce a white display for the MARKER input as well as for a white character, these inputs are gated by the NOR-gates forming IC9 so that red, green and blue are selected simultaneously. When line D0 is high, the low clocked out to buffer IC16 enables quiet tone buffer IC16 to output colour of a different hue.

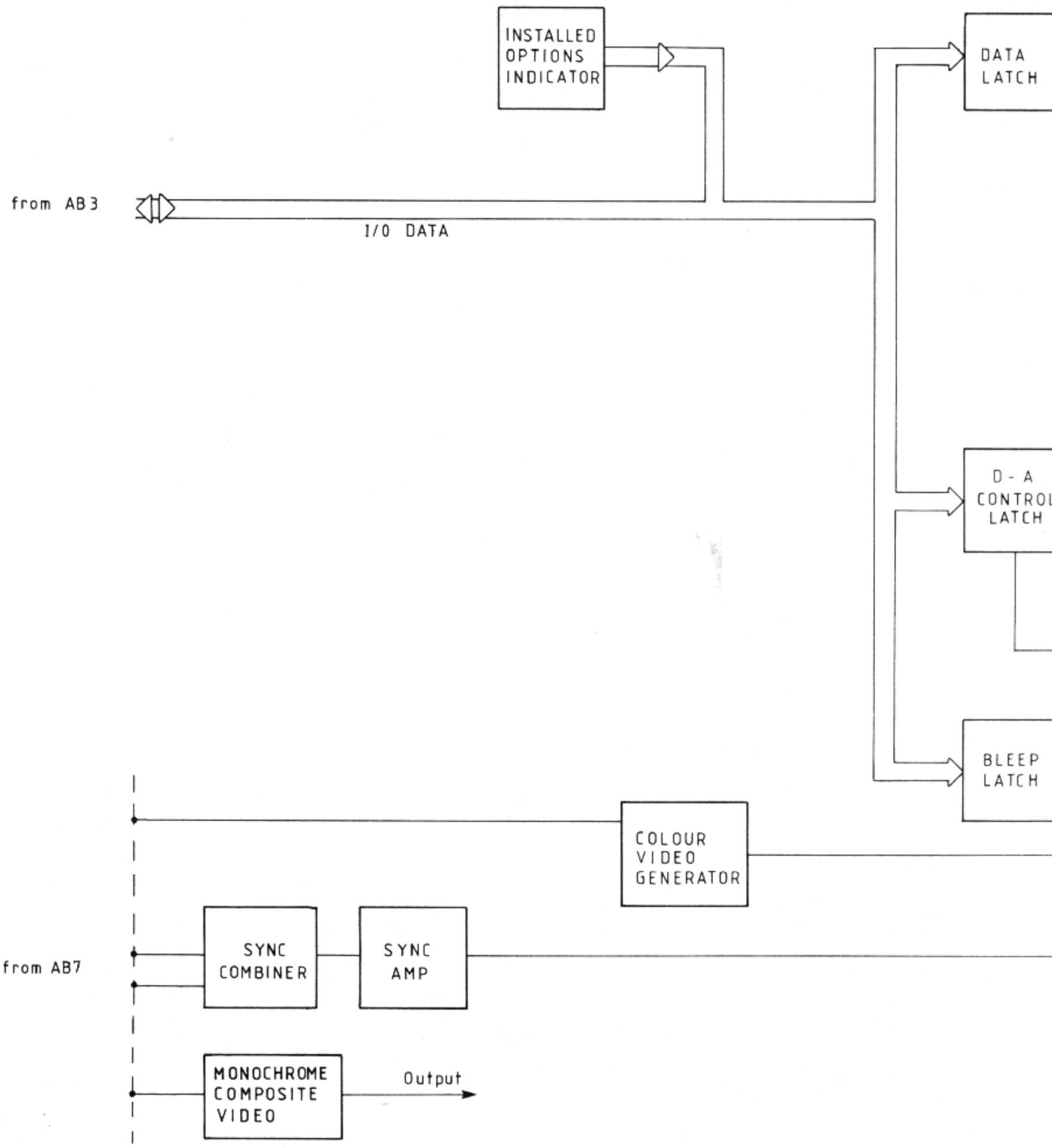
197. Character colour select decoder IC12 decodes the selection data on the GPA0S and GPA1S lines to set 1 of 4 outputs low. When enabled by CHAR to the NAND-gates forming IC10, Y0 to Y3 respectively select the required red, green, blue or white character colour in accordance with the display colour.

198. The horizontal and vertical synchronizing signals HSYNC (narrow pulse) and VSYNC (wide pulse) are combined by EXclusive-OR gate IC11d. This provides the single COMPOSITE SYNCS output from which the individual syncs may subsequently be recovered by the colour monitor.

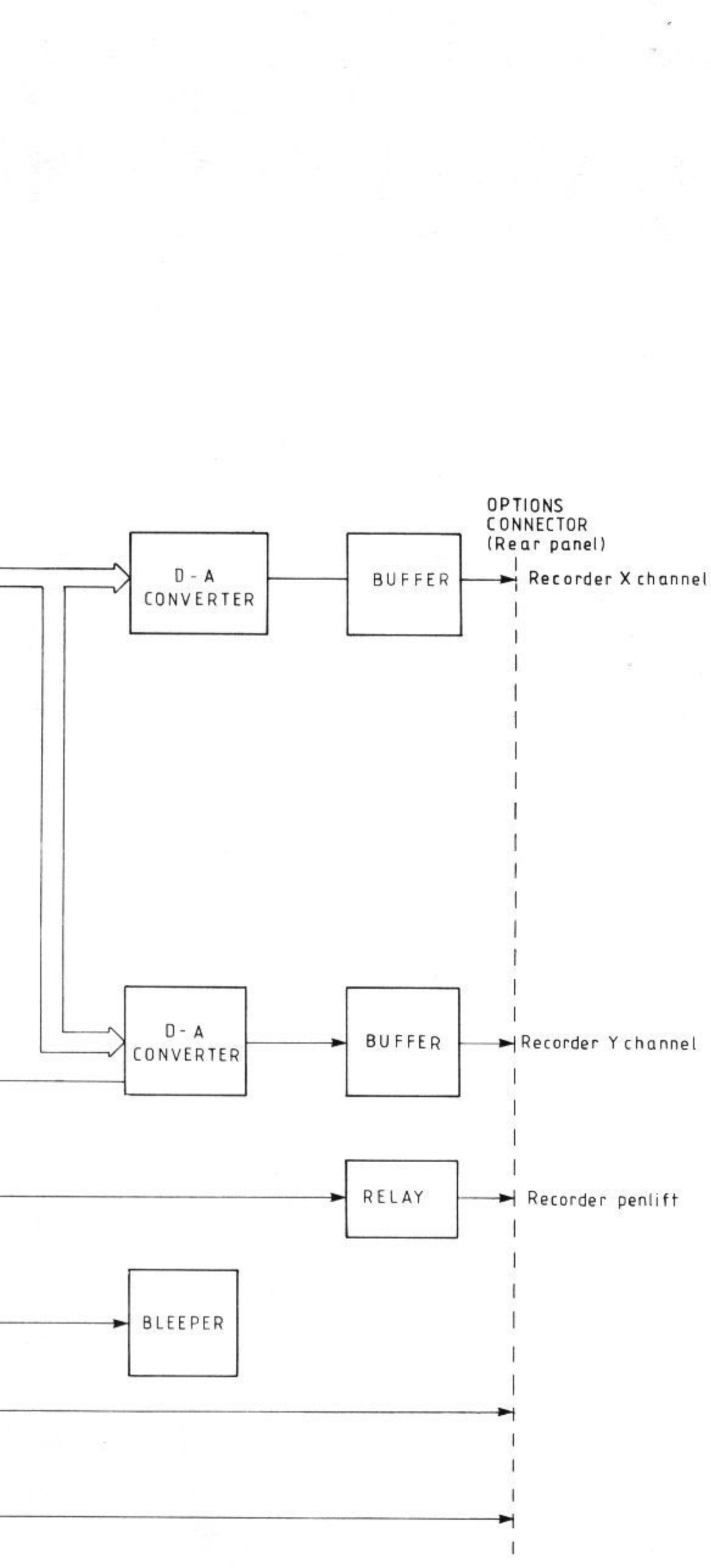
199. Outputs from the combiners operate switches TR1 to TR4 which produce a.c. coupled 1 V p-p signals to the rear panel OPTIONS connector.

Monochrome output

200. H SYNC and V SYNC via IC11d, and VIDEO from the video mixer to switch TR5, combine to operate switch TR6 which provide the COMPOSITE VIDEO OUTPUT signal for use by a monochrome monitor.



Pen plot and RGB video b



TPC 5240

ock diagram

Chapter 5-0

MAINTENANCE

CONTENTS

INTRODUCTION

1. This chapter provides servicing support information for PERFORMANCE TESTING, ADJUSTMENT & CALIBRATION and FAULT DIAGNOSIS.

2. Procedures and data for performance testing relate mainly to the complete analyzer comprising a 2380 Display and its RF Unit. For convenience, this information is published as an entity in the RF Unit service manual.

3. Likewise, the top levels of fault diagnosis relate to the complete equipment and are published in the RF service manual. The 2380 manual only includes those procedures and data that are specific to the 2380, namely the appropriate branches of the fault location charts.

4. In case of difficulties which cannot be resolved with the aid of the Display and RF Unit manuals, please contact our Service Division at the address at the rear of the manual or your nearest Marconi Instruments representative. Always quote the type number and serial number found on the instrument data plate.

SAFETY PRECAUTIONS

5. Although this equipment has been designed and constructed in accordance with international safety standards, it is important that the advice given under NOTES and CAUTIONS at the front of this manual should be observed in all maintenance procedures to ensure safe working practices. In addition to these general precautions, special handling techniques are required for certain items, as below.

6. Switched mode power supplies. This type of power supply, as used in the Display Unit, may present the following hazards:

- Exposed track and components at mains voltage.
- High d.c. voltages.
- High voltage and power circuits switching at frequencies up to 250 kHz.
- Components with stored energy which may not be immediately dissipated when the supply is disconnected.

When power supply boards are exposed for servicing appropriate precautions must be taken to avoid touching live points and to ensure capacitors have discharged before working on the board after switching off.

7. Chip components. Numerous chip capacitors and resistors are fitted in this instrument. These have silver palladium and cap terminations. When soldering these devices the following precautions should be observed.

(i) Use solder containing 3% silver, and a temperature controlled 45 W soldering iron set to 315^0C (600^0F). The use of a high voltage soldering iron will minimize the time taken to solder the device.

(ii) When soldering chip components to printed circuit boards a long fillet of solder should be laid on the track leading up to each end cap termination. This reduces the otherwise adverse inductive effects at high frequencies.

8. Static sensitive components. The c.m.o.s. integrated circuits used in this instrument have extremely high input resistance and can be damaged by accumulation of static charges (see preliminary pages, Notes and Cautions). Boards that have such integrated circuits all carry warning notices against damage by static discharge. Take care also when using freezer sprays to aid fault finding. These can create a static charge likely to change the programmed memory of (E)PROMS.

9. Transistor and diode checking. Transistors may be checked by measuring the electrode voltages and/or by measuring the resistance between electrodes by means of a multimeter. So that the meter voltage does not damage the transistors or diodes use the lowest voltage and the maximum source resistance available, e.g. the Ω range on the AVO 8 or the SEI Selectest Super 50.

RECOMMENDED TEST EQUIPMENT

10. The test equipment recommended for use in Chap. 5-1 is shown in Table 1. Alternative equipment may be used provided it complies with the stated minimum specifications.

TABLE 1 RECOMMENDED TEST EQUIPMENT

Description	Minimum specification	Example
Oscilloscope	Frequency range: d.c. to 100 MHz	Tektronix 2235
Digital multimeter	Functions: d.c. volts, resistance	Solartron 7150

ACCESS TO BOARDS AND COMPONENTS

CAUTION ...

Ensure that you are familiar with the NOTES and CAUTIONS at the beginning of both this volume and chapter before proceeding.

Removal of outer covers

11. To remove the top and bottom covers, unscrew the four retaining screws which pass through the cover flanges, slide each cover partly to the rear, then lift clear.

Removal of AB processing boards (See Fig. 1)

12. Free the p.c.b. clamp by releasing the M4 pan head screw which passes through the right hand side panel. Lift the free end of the clamp then release the other end from the slot that retains it. Disconnect sockets from board surfaces before attempting to withdraw the board completely. If board AB8 (optional) needs to be withdrawn, board AB7 should first be withdrawn completely then the connectors on the board surface unplugged. Even pressure should always be exerted on both card ejectors. Boards AB5 and AB6 should be withdrawn together cautiously as auxiliary interconnection AA2 bridges their lower edges.

Removal of display drive AD1/1

13. The unit should already have been disconnected from the supply and the warning l.e.d. which can be seen through a hole in cover AC/A should have stopped flashing. Remove the two crosshead screws from the edge slots in the top lid. Lift the lid clear by raising the released edge a little and withdraw it across the centre of the unit. Before proceeding further, as an extra precaution, the c.r.t. anode lead should be disconnected and grounded. To do this requires the release of the c.r.t. drive shield (para. 15 refers). Disconnect the sockets on AD1/1 then release the holding screws.

Removal of motherboard interconnection AA1

14. Motherboard interconnection AA1 is removeable through the top of the unit after all the AB boards and AD1/1 have been removed. Proceed by disconnecting sockets SLA, SLB, SLC and SLD. Still approaching the unit from above, release the seven crosshead screws. Carefully withdraw the motherboard.

Removal of power supply AC0

15. The supply must be disconnected. First check that the warning l.e.d. is not flashing. AC2 alone, is accessible once the bottom cover and power unit lid are removed. If only AC2 is to be removed, detach sockets on this unit alone, otherwise disconnect all sockets at the motherboard AA1 prior to complete removal of AC0. Removal of unit AC0 is achieved by removing six screws on the rear panel. Approach AC1 and AC3 by removing four slotted screws in cover AC/A. AC3 is further protected by a plastic cover which must be removed before access can be attained or the unit replaced.

Front panel AF1 and encoder AZ1

16. Remove the front handle crosshead screws and trim strips. Detach connectors to AB1 before removing the hexagonal pillars to release AF1. AZ1 encoder assembly is detached by removing the connector and the REF/FREQ knob assembly, releasing the clamping nut, then withdrawing the complete encoder rearwards.

Removal of c.r.t. assembly

17. WARNING ...

PREVENT CRT IMPLOSION; AVOID DROPPING, CARELESS HANDLING OR ALLOWING HEAVY OBJECTS TO FALL UPON THE TUBE. DISPOSE OF OLD TUBES BY AN AUTHORIZED PROCEDURE.

Disconnect the c.r.t. base AT2. Release the c.r.t. shield by removing four slotted screws, two from the upper and two from the underside. Carefully move the shield backwards to gain access to the anode cap connection and the retaining springs. Ground the flying anode lead by contact with the case. Release the springs at their forward anchorage points. Remove the remaining tube assembly which may now be placed face down on a grit free surface.

Removal and replacement of a c.r.t.

18. Unclamp the deflection coil assembly (see Chap. 7, Fig. 28) by removing the clamping screw, whilst the assembly is held in such a manner as to avoid undue strain on the tube neck. The whole coil assembly, packing strip and the clamp ring may now be removed. To replace a c.r.t. follow the above procedure in reverse order with attention to the following details;

a) The packing strip must be correctly placed on the c.r.t. neck before the deflection coil assembly is clamped.

b) Always use the correct torque loading which is 0.34 Nm for c.r.t. type 190 FB31 E7-91 7 in DE.

c) The manufacturer's fitting instructions should always be observed when installing a new tube especially the torque loading.

Removal of 'supply on' switch

19. The connections of the 'supply on' switch can be reached when the top cover is removed and the protective shrouding slid to the rear. Removal is achieved by detaching the knob assembly, loosening the clamping screw of the 'switch extender shaft', sliding the shaft forward, detaching the cable from the rear of the switch then undoing the switch clamping nut. On replacement, the extender shaft should be clamped in position and pulled forward to the

limit of play then the knob fitted, with 1 mm gap between the rear of the knob and the front panel.

Removal of 'rear panel'

20. Access to the inside of the rear panel is gained by the removal of six slotted screws. The fan and both sides of the GPIB connector can then be reached.

UNIT	PART No.
AA1	44828-500D
AA2	44828-501T
AB1	44828-503X
AB2	44828-504M
AB3/1	44829-340G
AB4	44828-506R
AB5	44828-507B
AB6	44828-508K
AB7	44828-509A
AB8	44828-510B
AC1/1	44829-296L
AC2/1	44829-297J
AC3/1	44828-512A
AD1/1	44828-519L
AF1	44828-524F
AR1	44828-516U
AT2	44828-520Y
AZ1	44828-523J

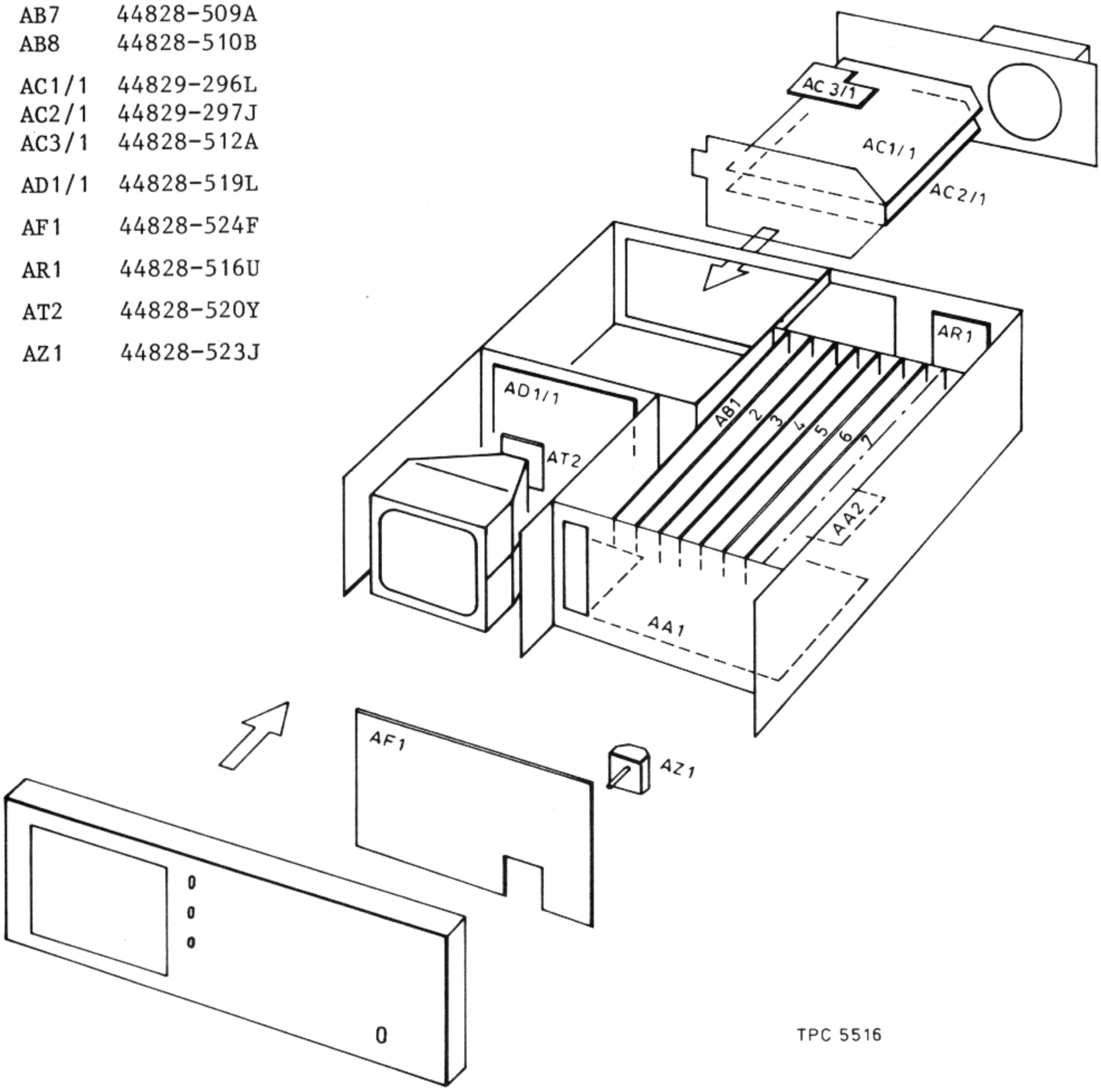


Fig. 1 Location of units and board

Chapter 5-2

ADJUSTMENT & CALIBRATION

- To be issued later -

Chapter 5-3

FAULT DIAGNOSIS

CONTENTS

INTRODUCTION

1. The practical approach to systematic fault location in this equipment is to treat the analyzer as a whole, rather than as two separate units. For this reason, the upper levels of the fault location charts and diagnostic procedures are contained in the RF Unit service manual; only those brances of the charts dealing specifically with the Display Unit are included in this chapter, where they may be more conveniently read in conjunction with their related circuit diagrams and test point waveforms.

2. If a fault is suspected, go first to the overall Fault location chart in Chap. 5-3 of the RF Unit manual. This will indicate, by reference to display symptoms, which function is suspect. The branches will lead you to area fault location charts and test procedures or to diagnostic routines which should localize the fault to a relatively small group of components or functional area.

3. At the same time it is useful to look at the overall block diagrams in Chap. 4 of the appropriate manual which show the relationship between functional areas and may suggest possible causes and effects. These diagrams also indicate the next level of block diagram where a more detailed treatment is given. For a complete understanding of the faulty area you should read the relevant part of the technical description in conjunction with the circuit diagrams.

4. A further guide to detailed fault location is provided by the test point waveforms and data shown opposite the circuit diagrams.

5. Test equipment recommended for fault finding is listed in Chap. 5-0.

6. Note that performance limits quoted in this chapter are for guidance only and should not be taken as guaranteed performance specifications unless they also appear in the Performance Data in Chap. 1.

FUSE REPLACEMENT

7. Either one or two cartridge-type fuses are located on the 2380 rear panel. These pain supply fuses are slow blow, 4 A for 95 to 130 V a.c. and 2.5 A for 190 to 260 V a.c. Two 3.15 quick acting fuses on board AC1/1 protect the ±170 V supply. Switch off the power supply when replacing a fuse.

RF UNIT
Fig. 2(i)(b)

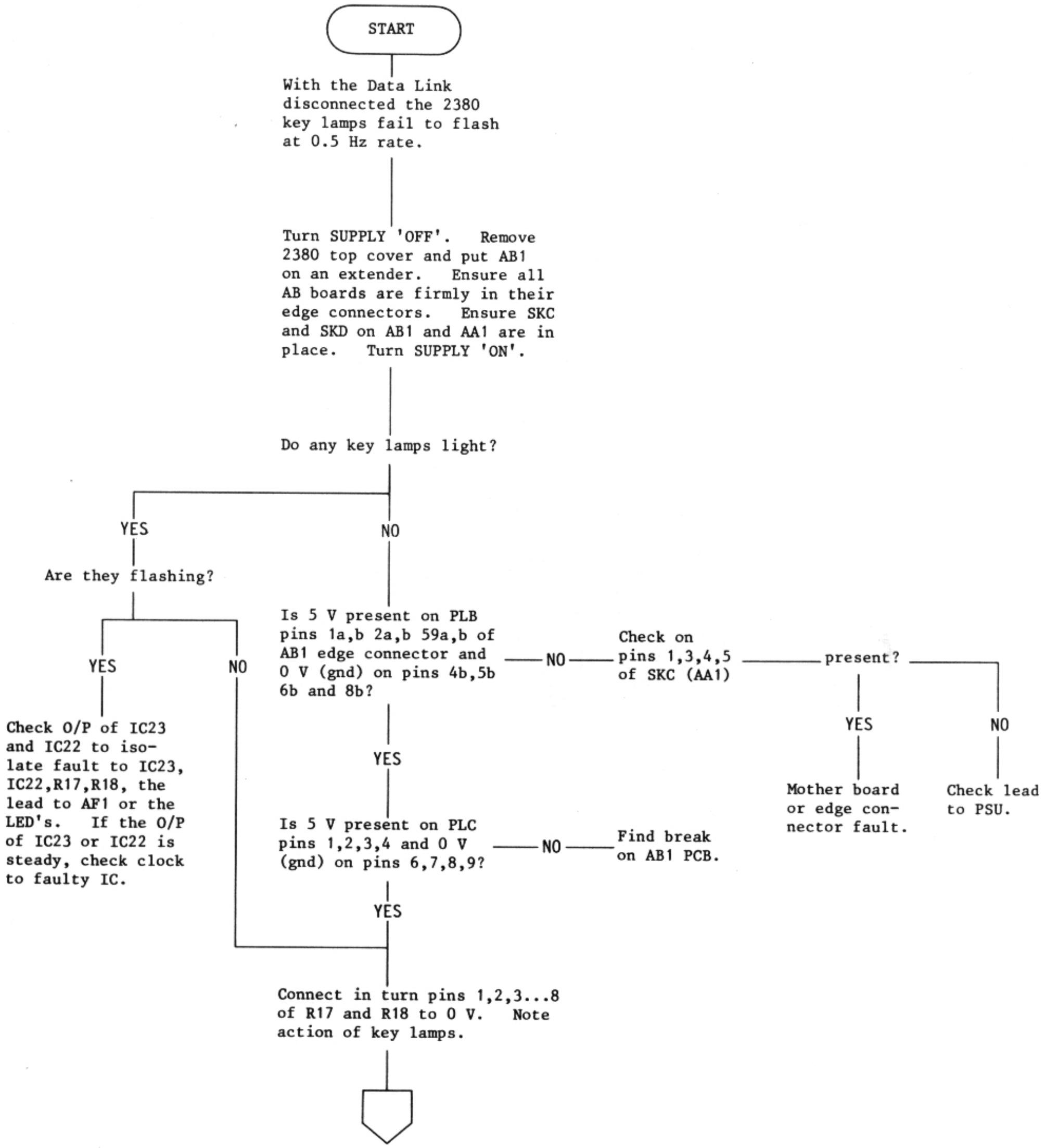


Fig. 1(b)

Fig. 1(a) Fault location chart - Logic Section A

Fig. 1(a)

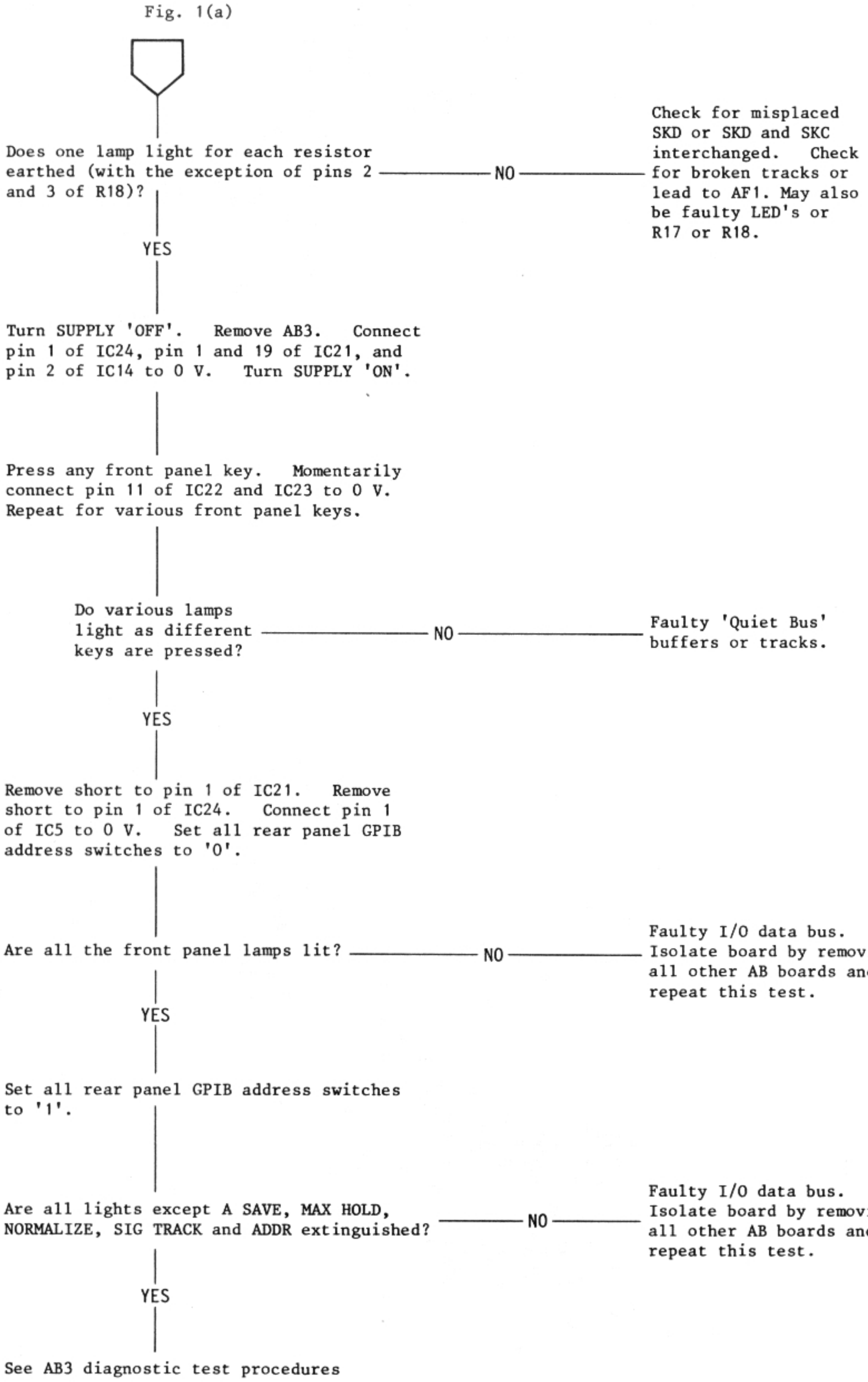


Fig. 1(b) Fault location chart - Logic Section A

RF UNIT
Fig. 2(ii)(d)

START

A fault has been found in the initial diagnostics where two ramps are not displayed.

Turn SUPPLY 'OFF'. Remove 2380 top cover and pub AB4 on an extender. Ensure all AB boards are firmly in their edge connectors. Turn SUPPLY 'ON'. Follow the diagnostics to return to this point.

Does the display show one or two ramps at the wrong expansion? — YES — Is one ramp correct? — NO — Check drive to IC6,IC30 etc. at PLBE on AB4.

Is one ramp correct? — YES — Check IC47,IC48,IC49 and IC33 on AB4.

Is one ramp correct? — NO

Does either A or B INTENSITY control change any part of the displayed picture? — YES

Use the A or B VIEW control to turn off the correctly displayed ramp. Does the display show some part of a ramp? — NO — Does either A or B INTENSITY control change any part of the displayed picture? — NO — Check AB5/6 Video drives through AB7 for faulty channel.

Does either A or B INTENSITY control change any part of the displayed picture? — YES

Fig. 2(b)

Is one ramp correct? — YES

Is the ramp a series of one or more small ramps? — NO — See 2380 Logic Section F. (Fig. 6)

Is the ramp a series of one or more small ramps? — YES

When REF FREQ is turned do the breaks in the ramp move up and down the display? — NO — See 2380 Logic Section F. (Fig. 6)

When REF FREQ is turned do the breaks in the ramp move up and down the display? — YES

Check A (or B) INPUT LATCHES or TRISTATE BUFFERS on AB4.

Does either A or B INTENSITY control change any part of the displayed picture? — YES

Fig. 2(c)

Fig. 2(a) Fault location chart - Logic Section B

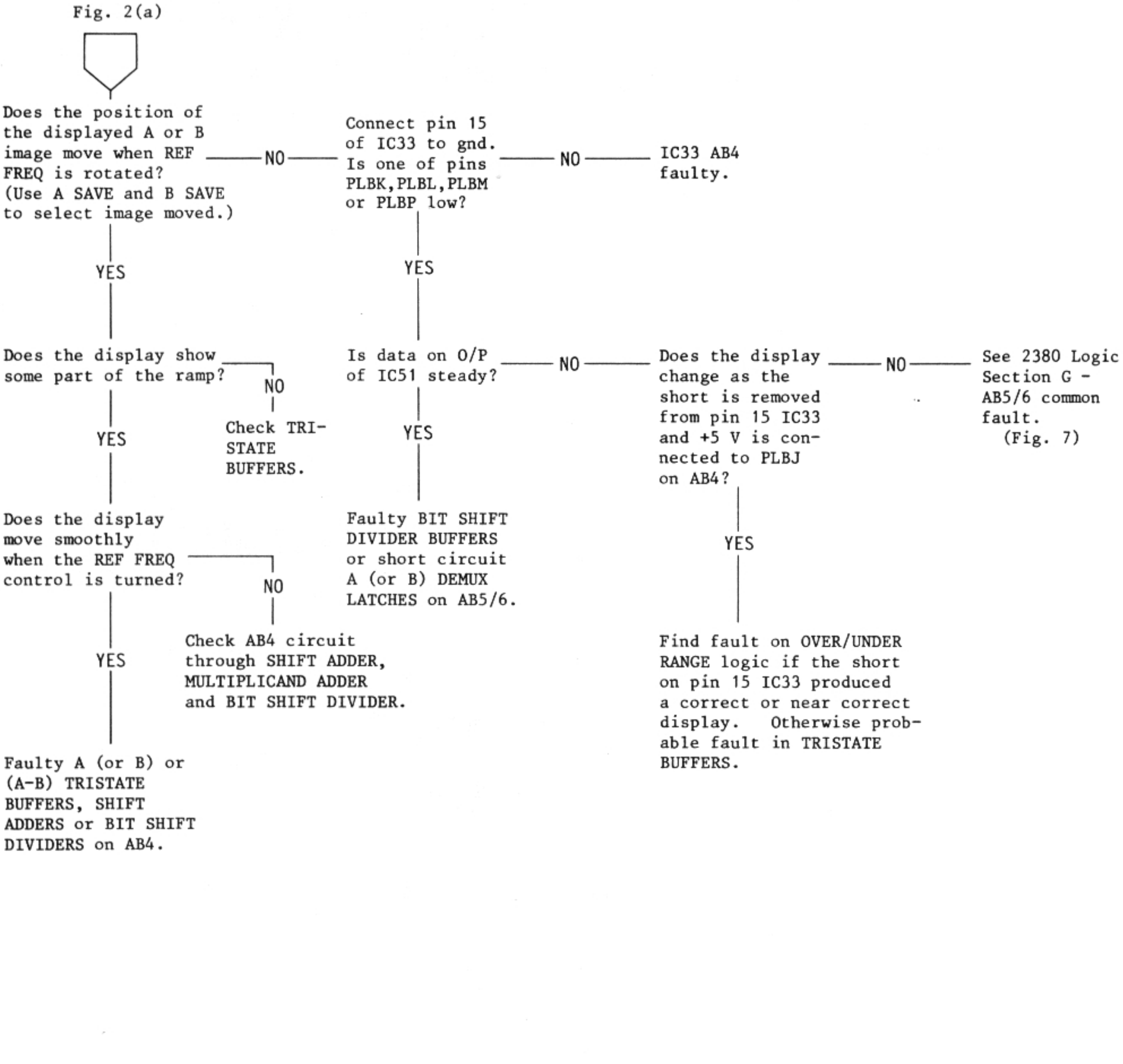


Fig. 2(b) Fault location chart - Logic Section B

Fig. 2(a)

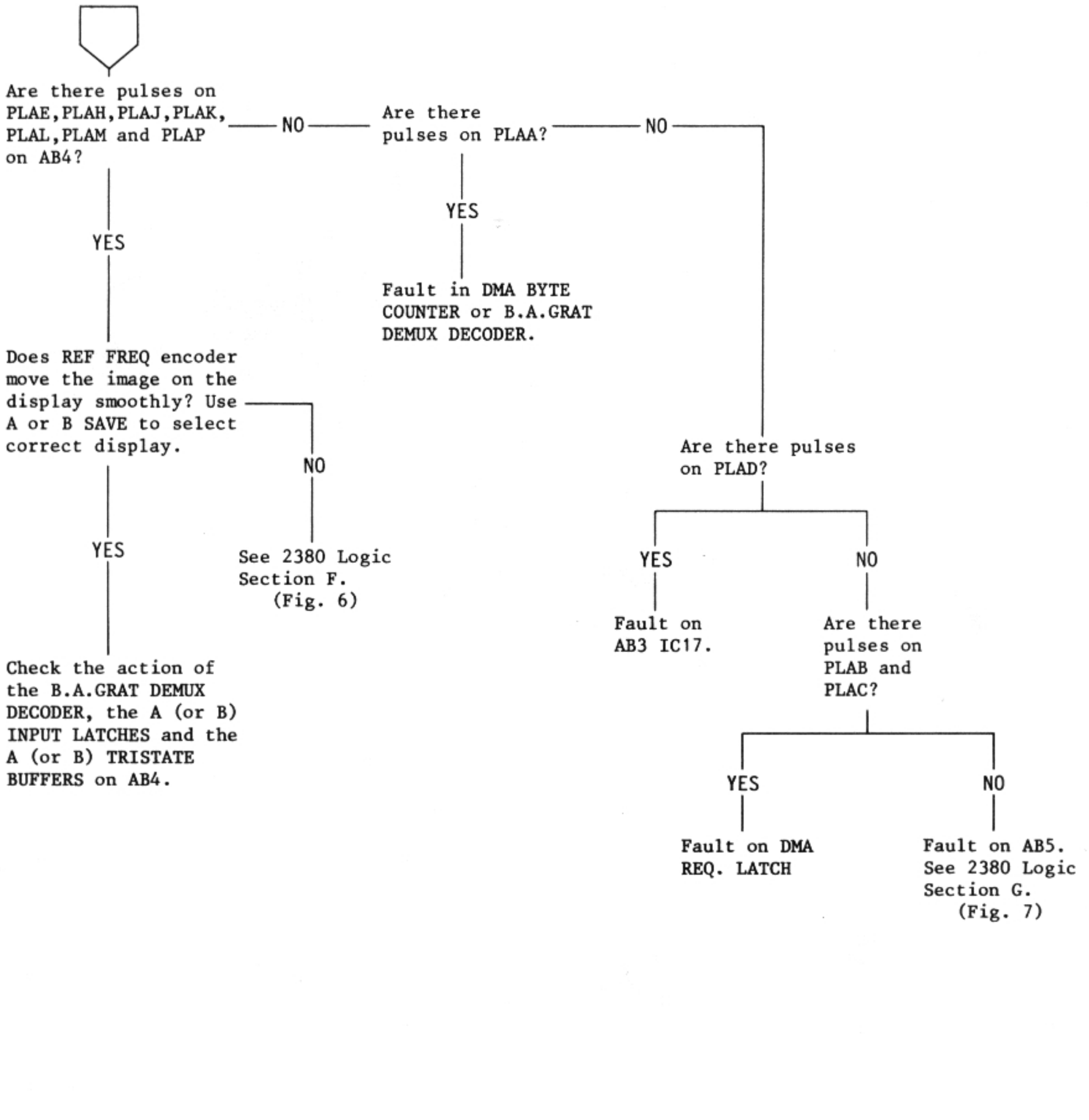


Fig. 2(c) Fault location chart - Logic Section B

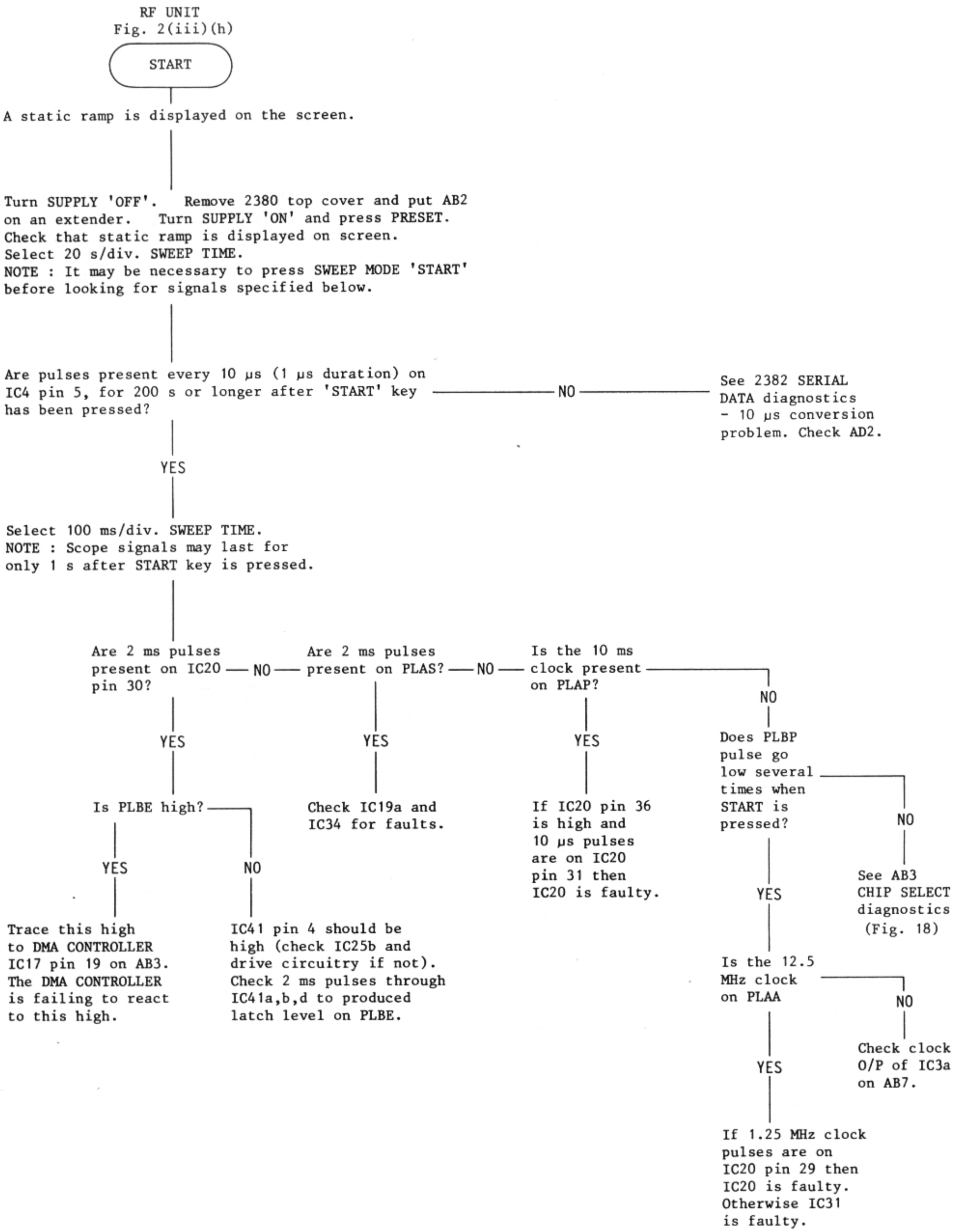


Fig. 3 Fault location chart - Logic Section C

RF UNIT
Fig. 2(ii)(e)

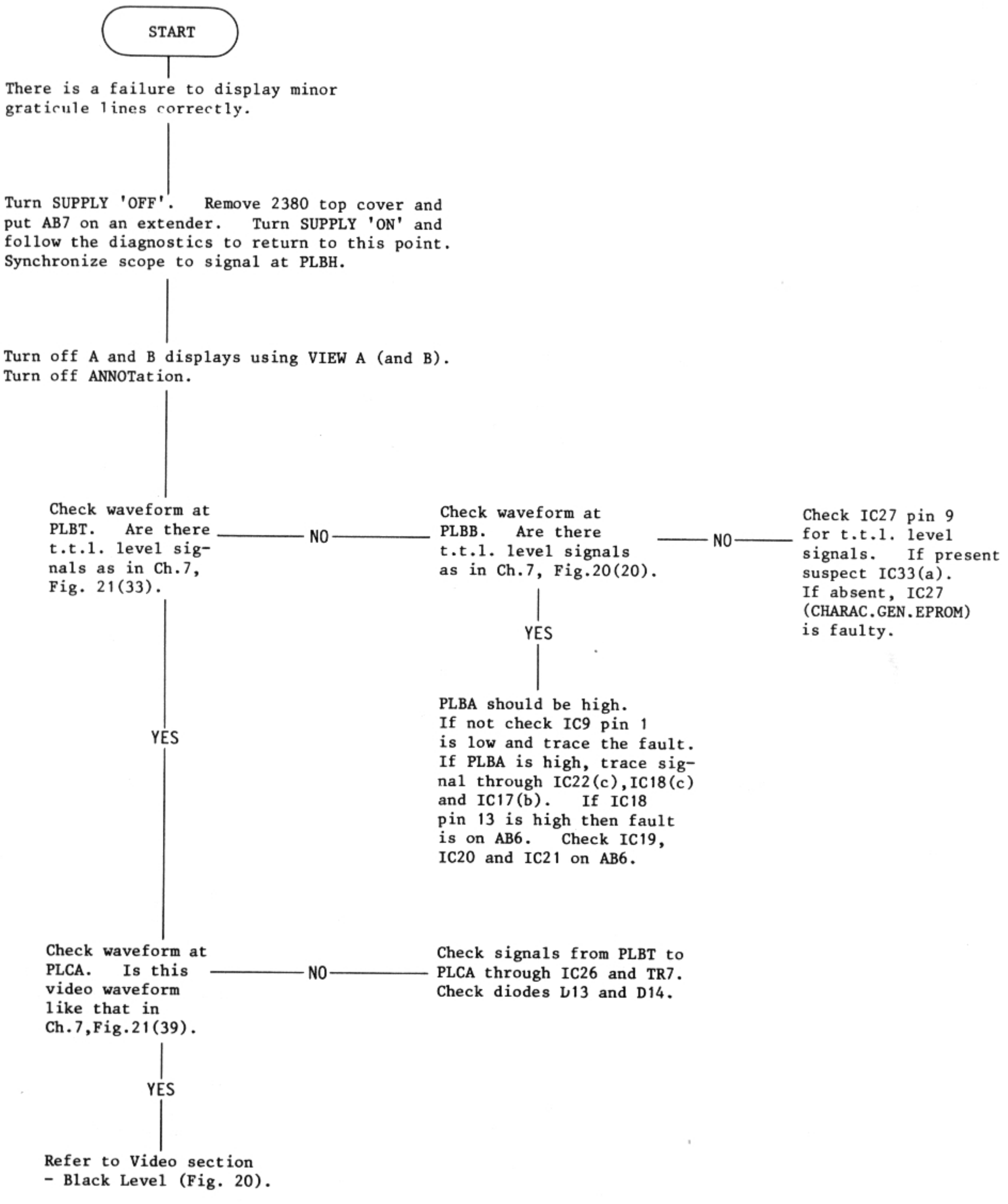


Fig. 4 Fault location chart - Logic Section D

RF UNIT
Fig. 2(ii)(e)

START

There is a fault in the graticule generation.

Turn SUPPLY 'OFF'. Remove 2380 top cover and put AB7 on extender. Turn SUPPLY 'ON' and follow the diagnostics to return to this point. Synchronize scope to signal at PLBH.

Check for +12 V on PLCH. If absent find fault in regulator or p.c.b. tracks.

Turn off A and B displays using VIEW A (and B). Turn off ANNOTation.

Does the display change when GRAT is pressed? — NO → 

YES

Connect IC18 pin 5 to 0 V.

Fig. 5(b)

Are the major horizontal lines displayed correctly? — NO → Remove short from IC18 pin 5. Connect IC18 pin 4 to 0 V.

YES

Fault on AB6, graticule generation. Refer to 2380 Logic Section H. (Fig. 8)

Are the major vertical lines displayed correctly? — NO → Is the signal on PLBS as in Ch.7, Fig.21(32)?

YES

Check PLBC for correct signals (see Ch.7,Fig.20(21). Trace fault to IC27,IC32 or IC8(c).

YES → Follow signal through IC26, TR6 and associated circuitry.

NO → Check signal path from PLBB to PLBS

Fig. 5(a) Fault location chart - Logic Section E

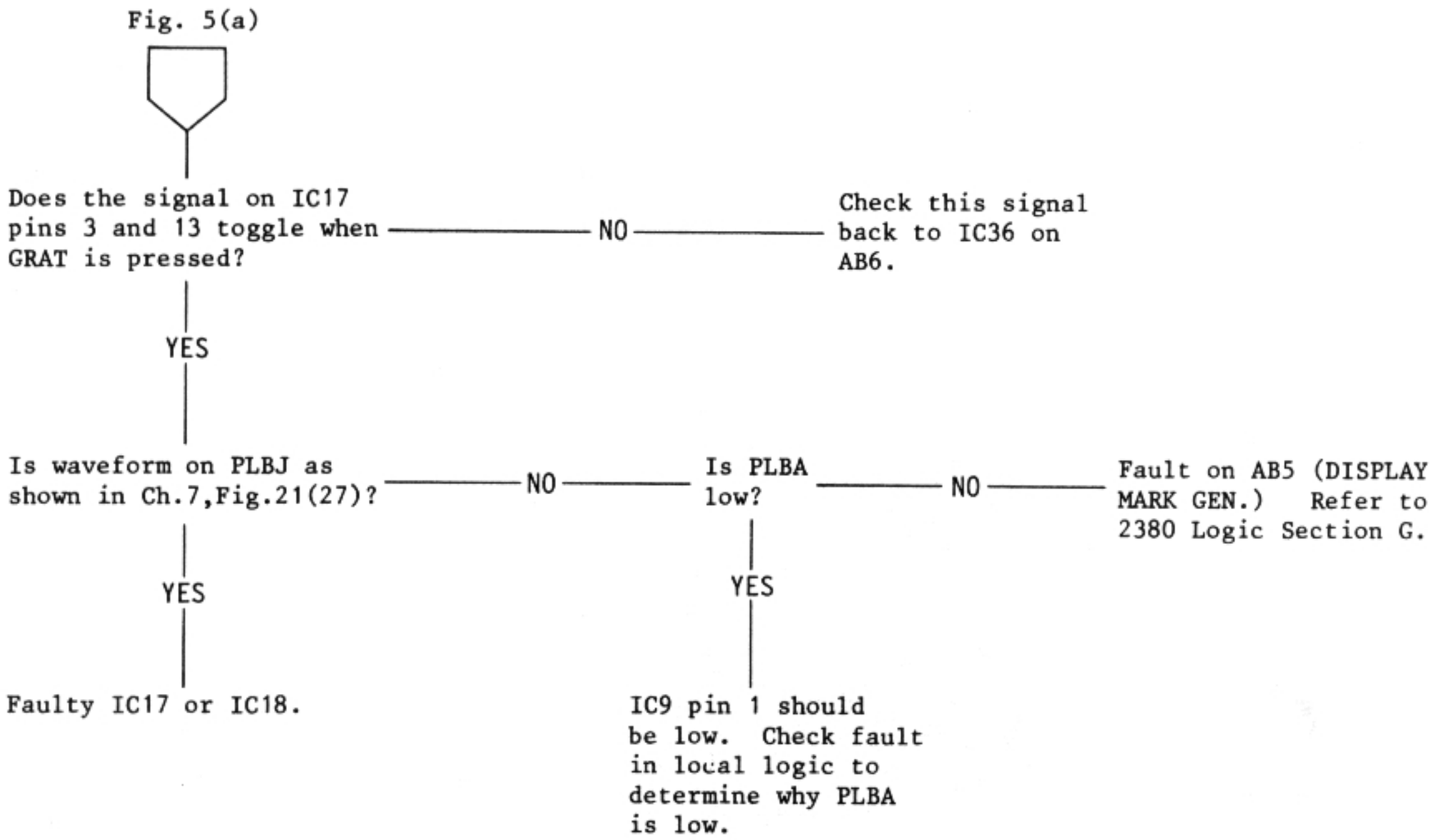


Fig. 5(b) Fault location chart - Logic Section E

Fig. 2(a)

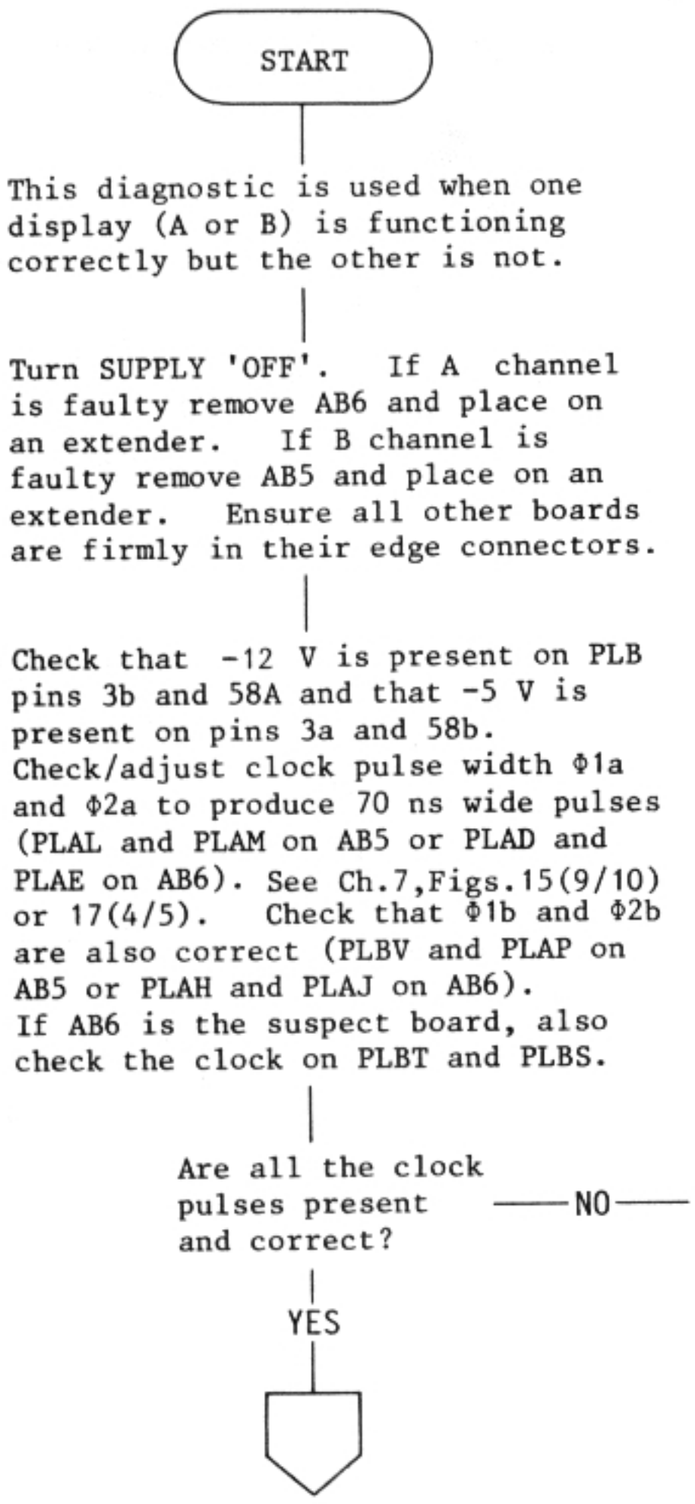


Fig. 6(b)

Fig. 6(a) Fault location chart - Logic Section F

Fig. 6(a)

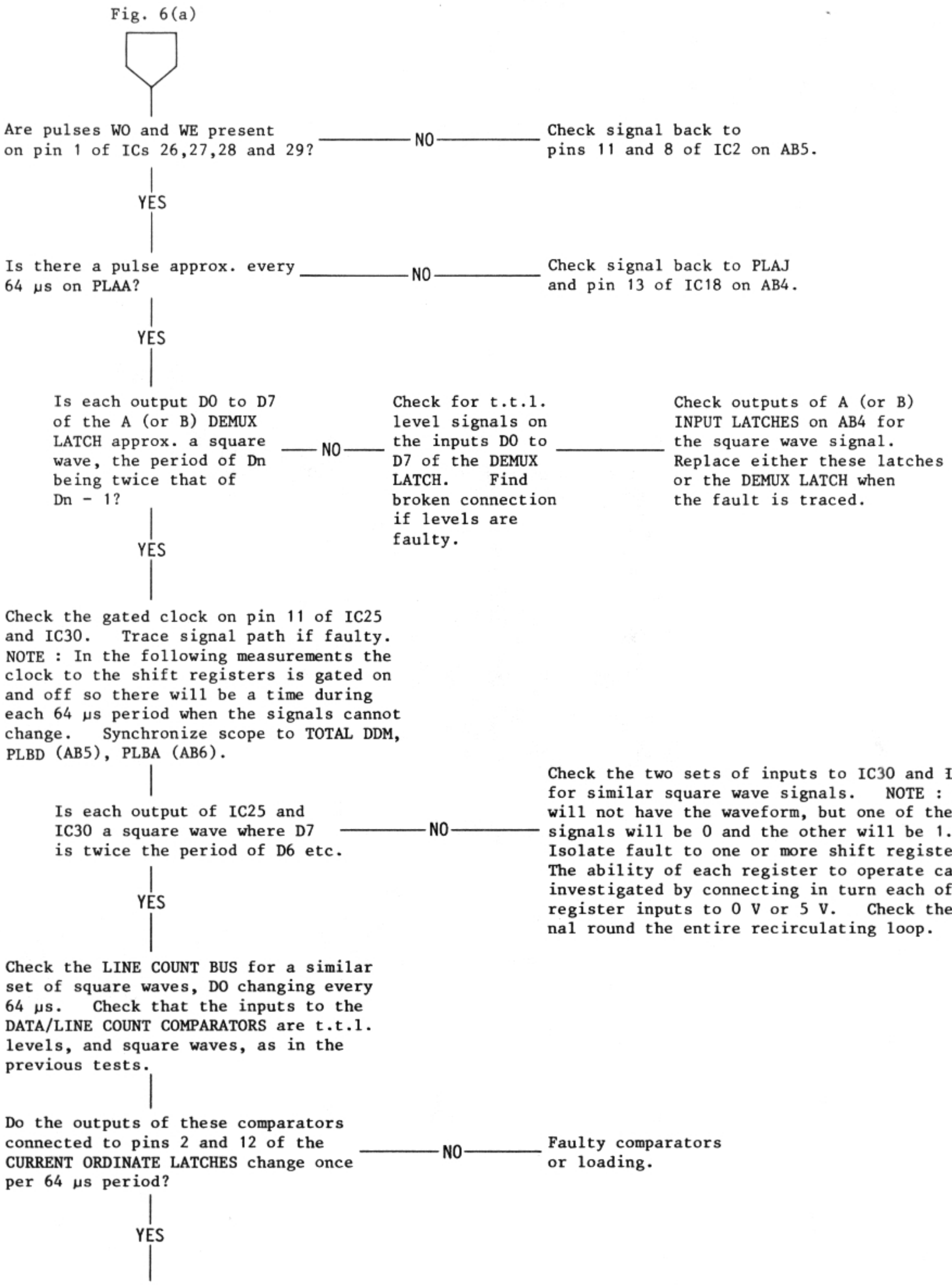


Fig. 6(b) Fault location chart - Logic Section F

Fig. 2(b)

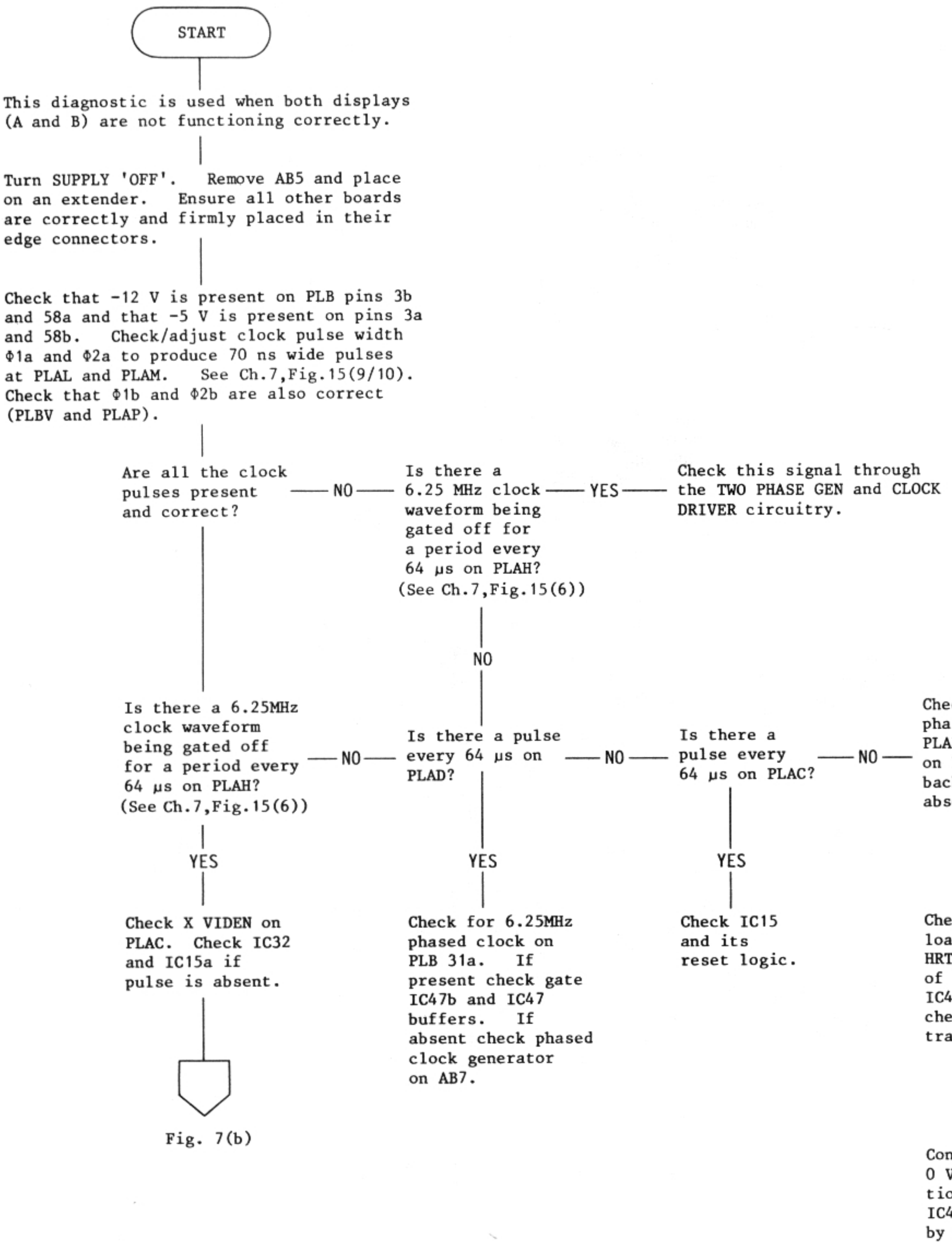
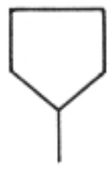


Fig. 7(b)

Fig. 7(a) Fault location chart - Logic Section G

Fig. 7(a)



Are there WD(L) pulses on PLAV at approx. the HRTC rate?

NO — Check for presence of FRAME signal (PLAZ). Locate fault if absent. Check presence of 6.25 MHz GATED CLOCK on pin 2 of IC1,IC17 and IC33.

Connect PLAS to 0 V. Sync. scope to FRAME (PLAZ). Check action of counters IC1,IC17 and IC33. Check PLAT is low for a period at the beginning of each frame. Trace signals through the local logic gates to PLAV.

YES

Are there WE and WO pulses on PLAW and PLAX produced from alternate WD(L) pulses?

NO — Check for square wave signal on PLAS at a half WD(L) rate. Check gating of WD(L) to produce WO and WE.

YES

Is there a 64 µs pulse at VRTC(L) rate on PLBK?

NO — Check clock to IC37 pin 4. Trigger scope to VRTC(L) on PLBA. Check action of counters IC37,IC36 and IC38. Check gates IC39 (a,b,c) and IC20.

YES

Check Y VIDEN on PLBB. Check LINE 0 signal and IC40(b) if absent.

Check that BOX(L) is high for most of the time (PLBC). BOX(L) is low whilst a character is displayed on the c.r.t. Check BOX(L) generation on AB7 if the signal is not correct.

Check the production of TOTAL DDM (PLBD).

Fig. 7(b) Fault location chart - Logic Section G

Fig. 5(a)

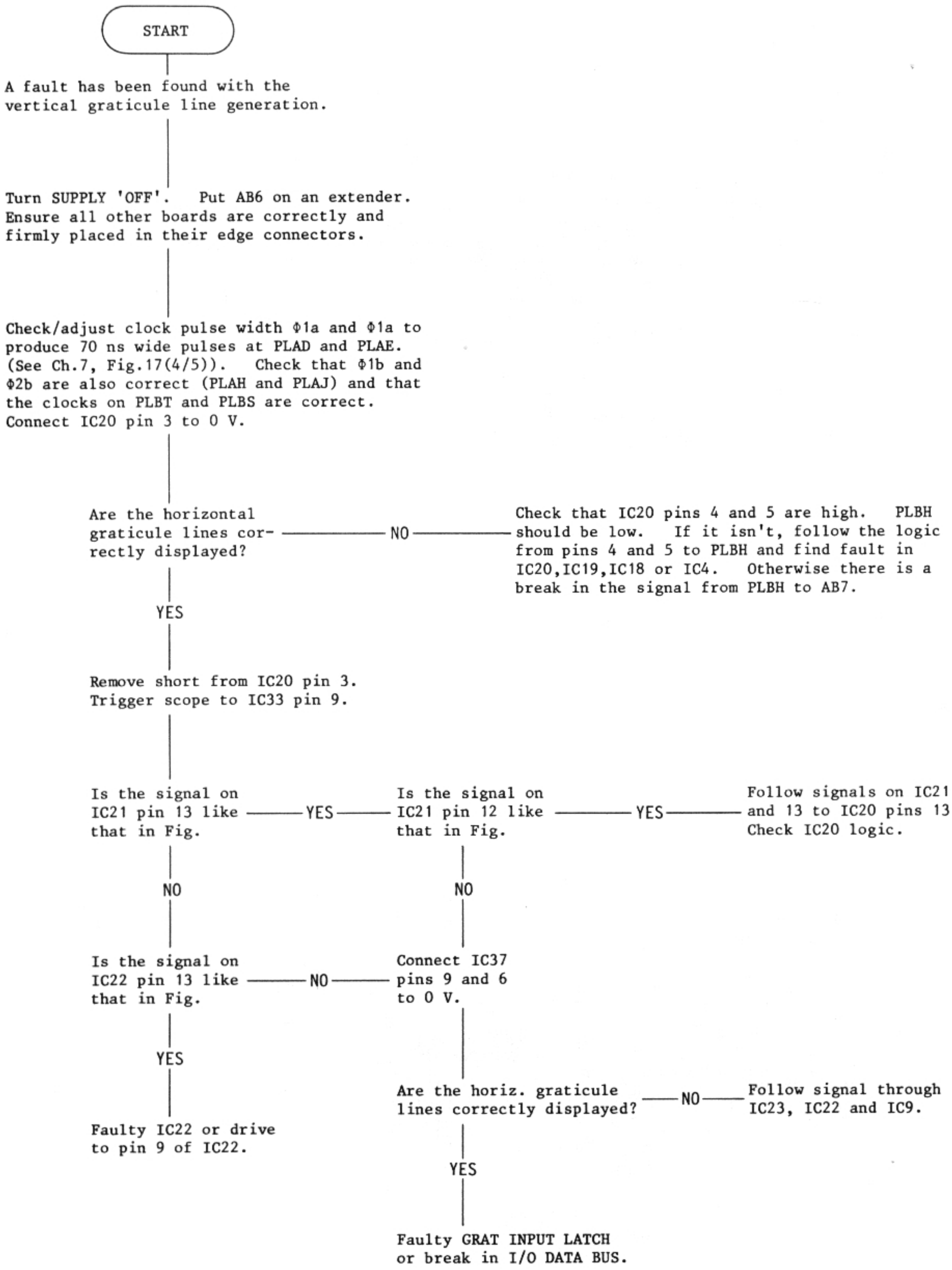


Fig. 8 Fault location chart - Logic Section H

RF UNIT
Fig. 2(iv)(k)

START

A fault has been found with the AB4 'gain adjust' circuitry. Turn SUPPLY 'OFF', put AB4 on an extender. All other boards should be in their place in the edge connectors.

The data signal paths on this board are multiplexed between A, A-B and B signals. If A display is faulty, trigger scope to PLAL otherwise trigger scope to PLAJ. The signals measured below are valid only when PLAL or PLAJ are low.

Enter the 2380 diagnostics routines (refer to para.) and select Data Upper Unit Confidence Tests : Data Displays and Linearity Test.

Having displayed the two ramps on the screen, select the following functions and observe the effects on the displayed image.

Turn REF FREQ and observe the display.

Does one of the ramps move smoothly from its original position to the top of the display?

NO

Press the 'B' SAVE key and check the movement of the B ramp. Is this movement correct?

NO

Return the ramps to their original positions. Press DATA key 4 then DATA key 0.

Is the B ramp now 0-6.25 divisions?

YES

Faulty SHIFT ADDERS IC26,IC27,IC28 and IC29. Check also the UNDERRANGE signal and gating to IC33 and IC52. This signal should not go high during these tests.

NO

Faulty MULTIPLICAN ADDERS (IC5,IC7, IC8 or IC9) or OVERRANGE DETECTOR logic (IC10,IC11, IC12 or IC34).

YES

Return the ramp to its original position using the REF FREQ control.

Fig. 9(b)

Fig. 9(a) Fault location chart - Logic Section I

Fig. 9(a)

Fig. 9(b) Fault location chart - Logic Section I

RF UNIT
Fig. 2(iii)(g)
Fig. 2(x)(ac)

START

There are two entry points to this diagnostic
1) Although the display is correctly synchronized when the rear panel DATA Link is disconnected the display becomes unsynchronized as soon as the DATA Link is reconnected (Fig. 2(ii)(g)).

2) The measured clock frequency on AB7 PLAE is not 25 MHz (Fig. 2(x)(ac)).

Turn SUPPLY 'OFF'. Remove 2380 top cover and put AB7 on an extender. Turn SUPPLY 'ON'. Press PRESET key.

Is there a 5 MHz signal of t.t.l. level on PLAA? — NO — Check circuit back through IC10(a) to the DATA Link to the lower unit. Check for the signal on pin 4 of the 2382 DATA Link socket. See 2382 logic circuits if this signal is absent - trace 5 MHz clock across AR1 to AD3 and back across AD2 to AC6, and finally the 50 MHz oscillator AC1.

YES

Connect PLAA to 0 V.

Set the Clock frequency measured on PLAE to 25 MHz using the 'SET 25 MHz' control C43.

Remove the short from PLAA. Check that the display is now synchronized. If not, check the operation of IC1,IC2(a) and IC42.

Fig. 10 Fault location chart - Logic Section J

RF UNIT
Fig. 2(iii)(j)

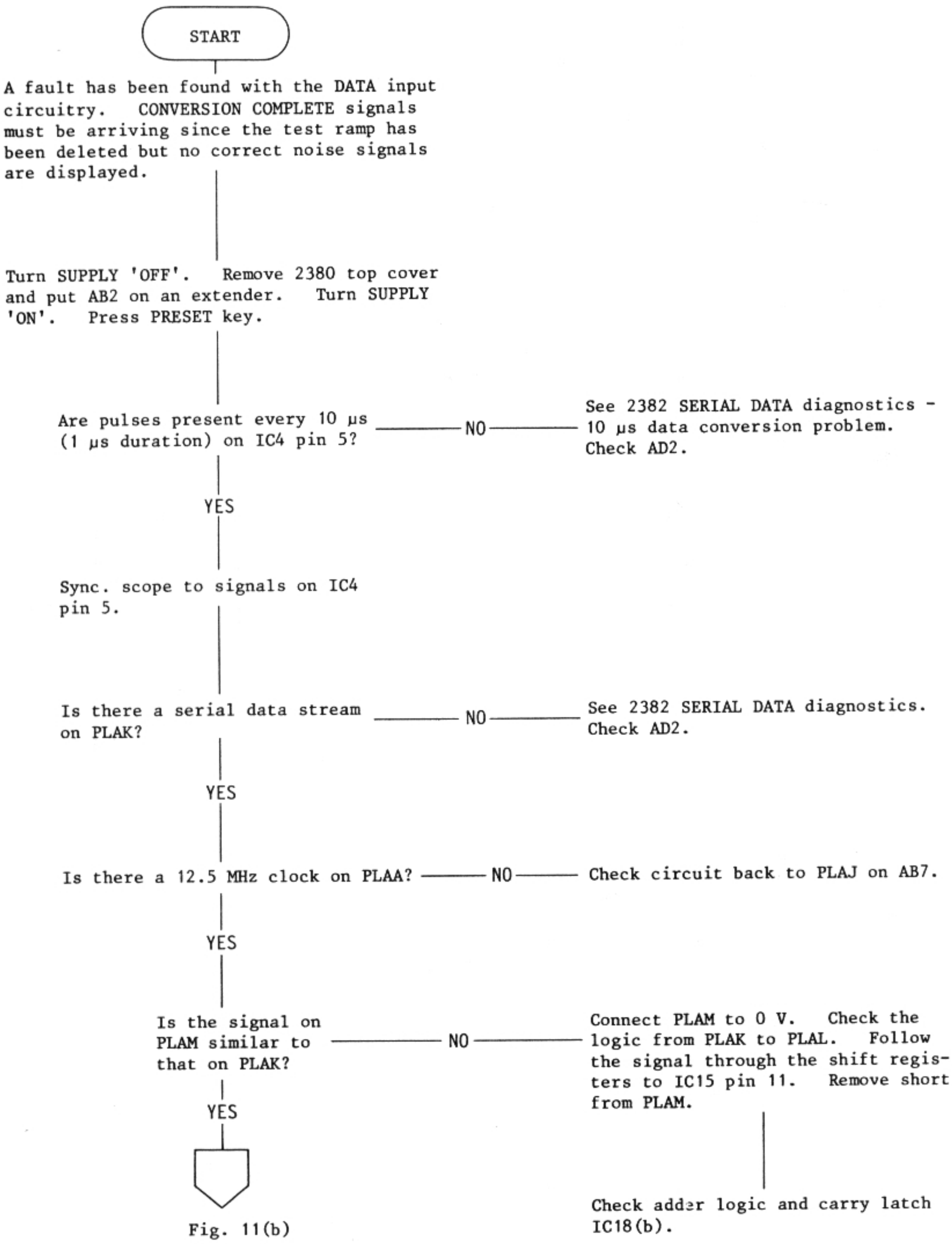


Fig. 11(b)

Fig. 11(a) Fault location chart - Logic Section K

Fig. 11(a)

Check that the INPUT WORD RATE DIVIDER is set to divide by one. There should be one burst of 2.5 MHz clock pulses on PLAH for each END OF CONVERSION pulse. Check local logic if incorrect. Sync. scope to observed signal.

Is there an ORDINATES pulse on IC34 pin 13 every 200 µs? — NO — Check for t.t.l. signals on PLAS, and local logic.

YES

The SERIAL INPUT DATA is input LSB first. Check that PARALLEL AVERAGED DATA latched on IC33 and IC32 is of similar value.

Check that the data latched on IC21,IC22, IC23 and IC24 is of similar value.

Check that pin 1 of IC12 is high.

Are there t.t.l. signals on PLAZ and PLBA? — NO — Check the signals to the relevant DETECTOR MAX/MIN LATCH.

YES

Connect PLAZ to 0 V and check PLBC is high. Remove short. Connect PLBA to 0 V and check PLBC is high. Remove short.

Check the signals on PLAZ and PLBA through to PLBC. Check that this signal gates SELECT LOW BYTE (L) and SELECT HIGH BYTE (L) to the OUTPUT LATCHES. The OUTPUT LATCHES may be faulty.

Fig. 11(b) Fault location chart - Logic Section K

RF UNIT

Fig. 2(viii)(*v*)

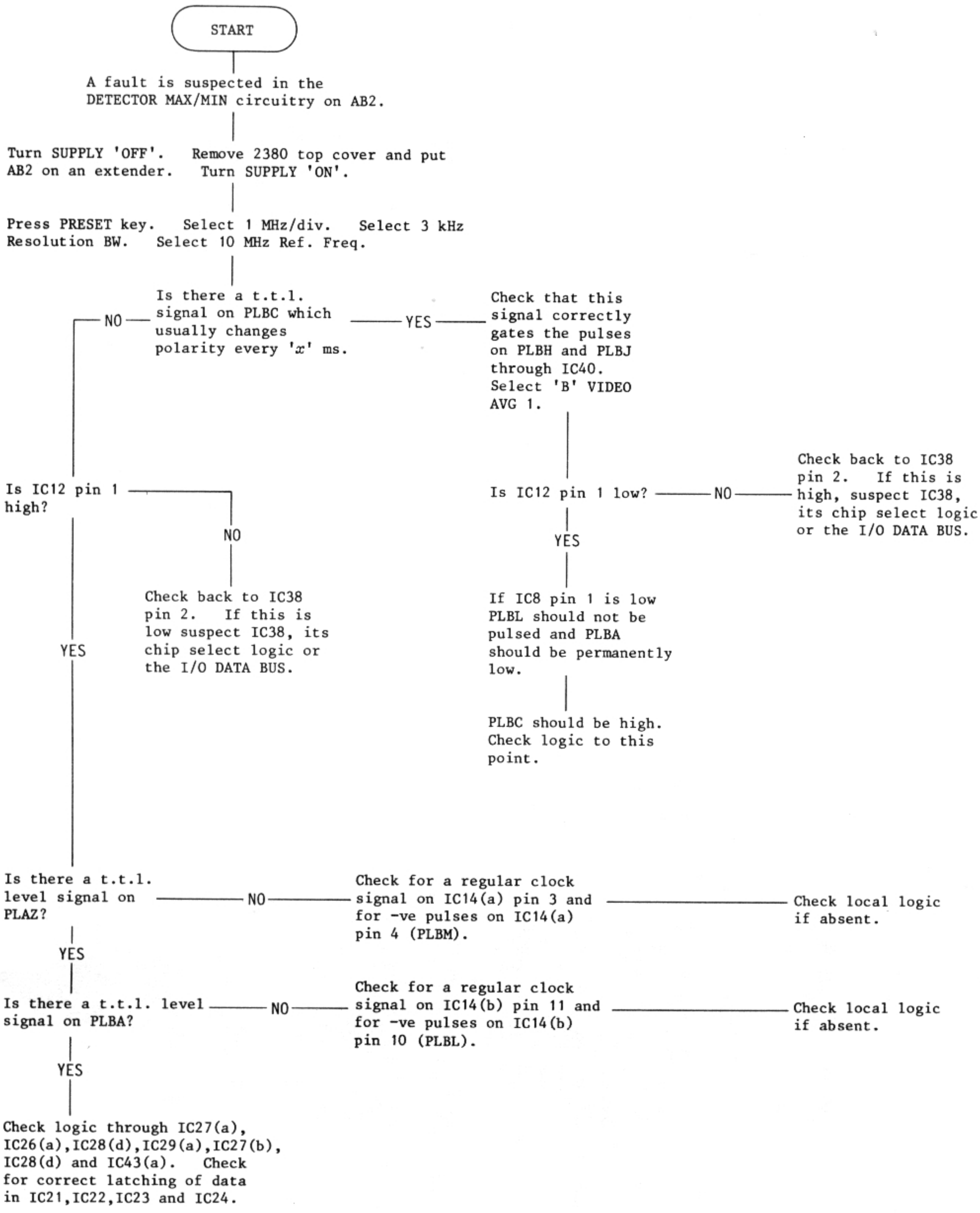


Fig. 12 Fault location chart - Logic Section L

RF UNIT
Fig. 2(viii)(w)

START

A fault is suspected in the Video filtering circuitry on AB2.

The main video filter section which operates on all ranges down to 43 Hz has already been proved to work on one range and since it is software driven through a single counter in IC20, it is unlikely that problems could occur in this area. A supplementary counter and additional logic are switched in on ranges below 43 Hz video BW.

Turn SUPPLY 'OFF'. Remove 2380 top cover and put AB2 on an extender.
Turn SUPPLY 'ON' and press the PRESET key.

Select 1 MHz/div., 3 kHz Resolution BW, 10 MHz Ref. Freq., 10 s/div. Sweep Time and 22 Hz Video BW.

Check PLAC is toggled on each END OF CONVERSION pulse by the INPUT WORD RATE DIVIDER counter IC20(1).

Check on PLAH that alternate blocks of the STROBED 2.5 MHz clock on PLAD are gated by the signal on IC3(b) pin 6.

Check reset of IC18(a) by signal on PLAE acting through the differentiator R1, R2, R3 and C52.

Fig. 13 Fault location chart - Logic Section M

RF UNIT
Fig. 2(viii)(u)

START

A fault is suspected in the Marker generation circuitry on AB6 or AB7.

Turn SUPPLY 'OFF'. Remove 2380 top cover and put AB6 on an extender. Turn SUPPLY 'ON' and press PRESET key.

Set MARKERS A B SELECT to 'A'. Select MKR1 and MARKERS 1 MOVE.

Are there narrow pulses on PLBM? —— YES —— Check this signal through to PLBV of AB7 and from there through IC26, TR5 and TR9 to the VIDEO signal. Turn GRATICULE off, ANNOTATION off and A and B INTENSITY down whilst checking the VIDEO signal.

NO

Are there narrow pulses at line rate on PLBK? —— YES —— Check logic of IC16,IC39(a),IC31(c) and IC40(a).

NO

Check for 6.25 MHz clock on IC6 pin 1.

Deselect MARKERS 1 MOVE (MKR 1 remains selected).

Are there narrow pulses at line rate on PLBK? —— NO —— Check that D1 input to IC7 is high. If incorrect, check IC21 and GRATICULE RECIRCULATING SHIFT REGISTERS.

YES

Select MARKERS 1 MOVE and check for t.t.l. signals on PLBD.

Check D1 input to IC7 is low and D0 input to IC7 is high. If incorrect, check IC21 and GRATICULE RECIRCULATING SHIFT REGISTERS.

Check IC7,IC6,IC4(b),IC4(d) and IC5 logic.

Fig. 14 Fault location chart - Logic Section N

RF UNIT
Fig. 2(i)(c)

START

A fault is suspected in the character generation circuitry on AB7.

Turn SUPPLY 'OFF'. Remove 2380 top cover and put AB7 on an extender. Turn SUPPLY 'ON'.

Check that the 25 MHz clock on PLAE is 25 MHz ±1 MHz. Adjust if necessary using C43.

Is there a CHAR. CLOCK of 7:1 ratio at about 1 MHz on PLAS?

NO — Check counter IC31 for a correct division by 3 and IC30 for correct counting.

YES

Check that pins 9,10,11,13,14,15,16 and 17 of IC27 all have t.t.l. level signals on them. Suspect IC27 if not.

Check latch IC28 for correct latching.

Check that CHAR. DOTS (PLBD) are faithfully transferred to PLBP, the only gating off being VSPS during Line and Field retrace.

Fig. 15 Fault location chart - Logic Section 0

RF UNIT
Fig. 2(i)(c)

START

A fault is suspected in the DMA channel to the CRT Controller circuitry on AB7.

Turn SUPPLY 'OFF'. Remove 2380 top cover and put AB7 on an extender. Turn SUPPLY 'ON'

Is there a pulse every 1.6 ms on PLAT? — NO — Check LC3 (PLAW) occurs every 0.8 ms. Check divide-by-two counter IC11(a).

YES

Check IC23 (a,b) for correct operation and gates IC34 (a,b). Check operation of latch IC11(b).

Check for DREQ3 pulses on PLAX. These should occur several times per 64 µs period and have a duration of about 1 to 5 µs.

Is the duration too long? — NO — Check that the pulses on PLAX are gated low by the EXTRA LINE (L) signal on PLAT.

YES

Check for DACK3(L) pulses on PLCE. If there are pulses or if PLCE is low for longer than 5 µs suspect IC15.

Fig. 16 Fault location chart - Logic Section P

RF UNIT
Fig. 2(vi)(o)

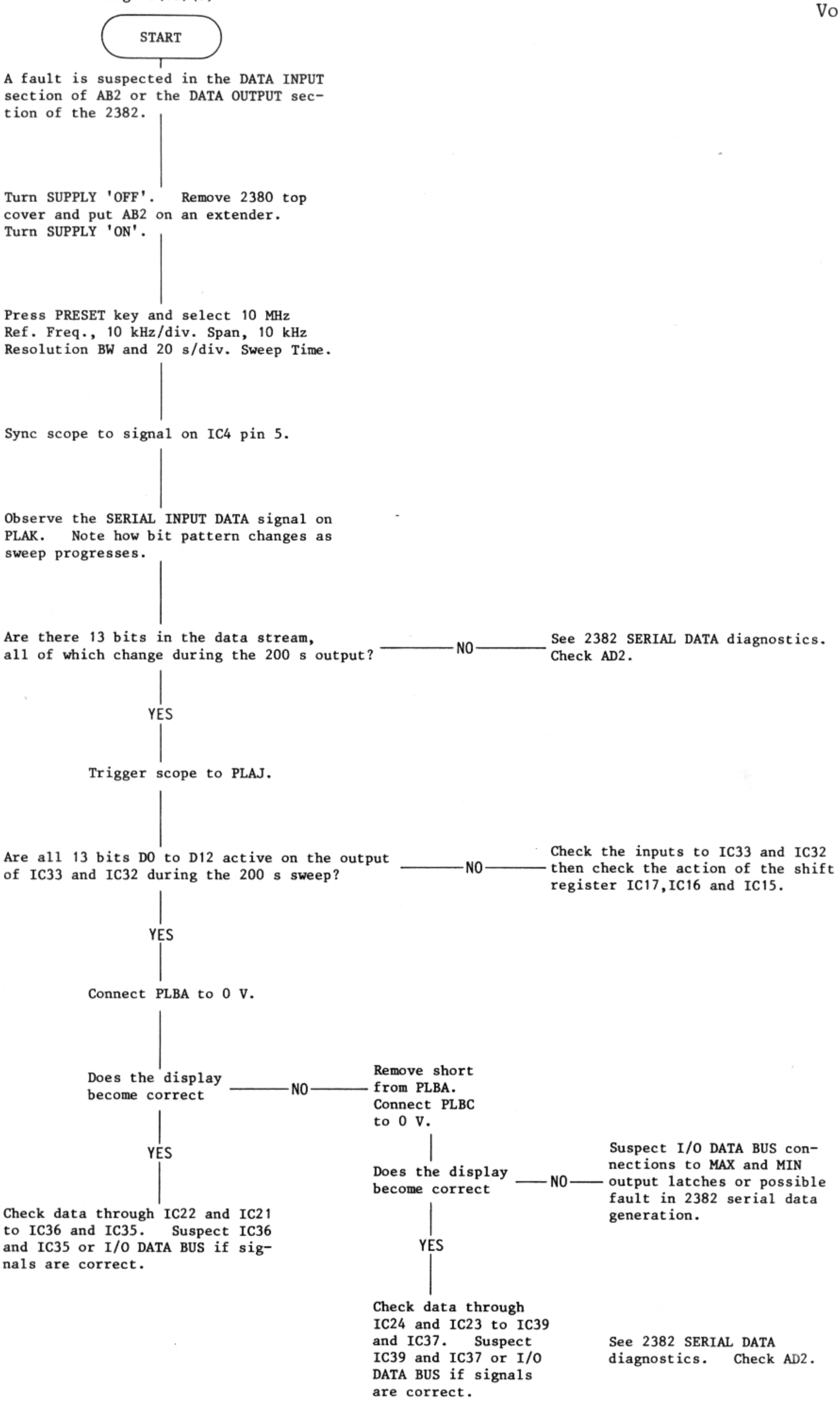
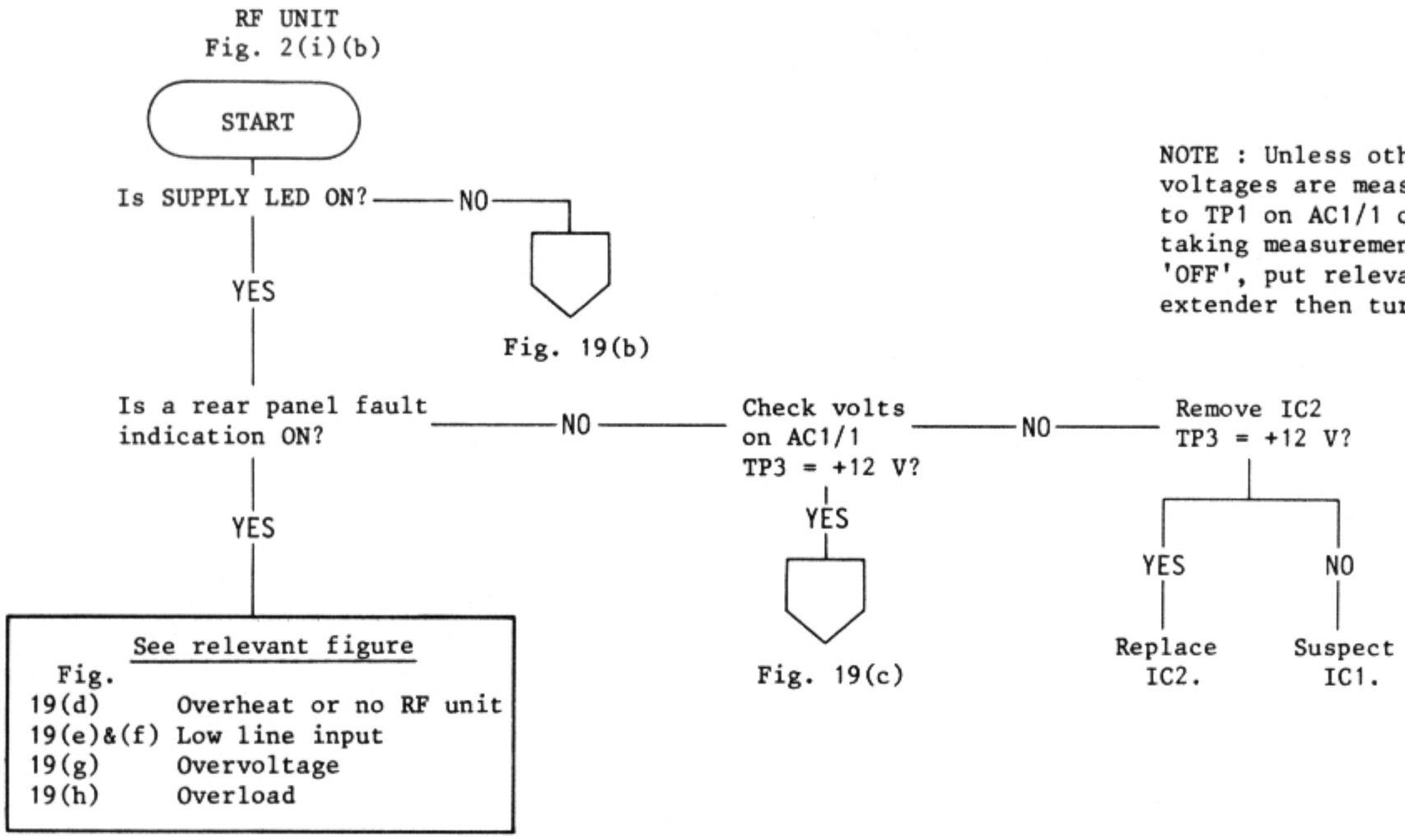


Fig. 17 Fault location chart - Logic Section Q

TO BE ISSUED LATER

Fig. 18(a) Fault location chart - AB3 fault



NOTE : Unless otherwise stated voltages are measured relative to TP1 on AC1/1 or AC2/1. Before taking measurements turn SUPPLY 'OFF', put relevant board on an extender then turn SUPPLY 'ON'.

Fig. 19(a) Fault location chart - Power Supply (PSU1)

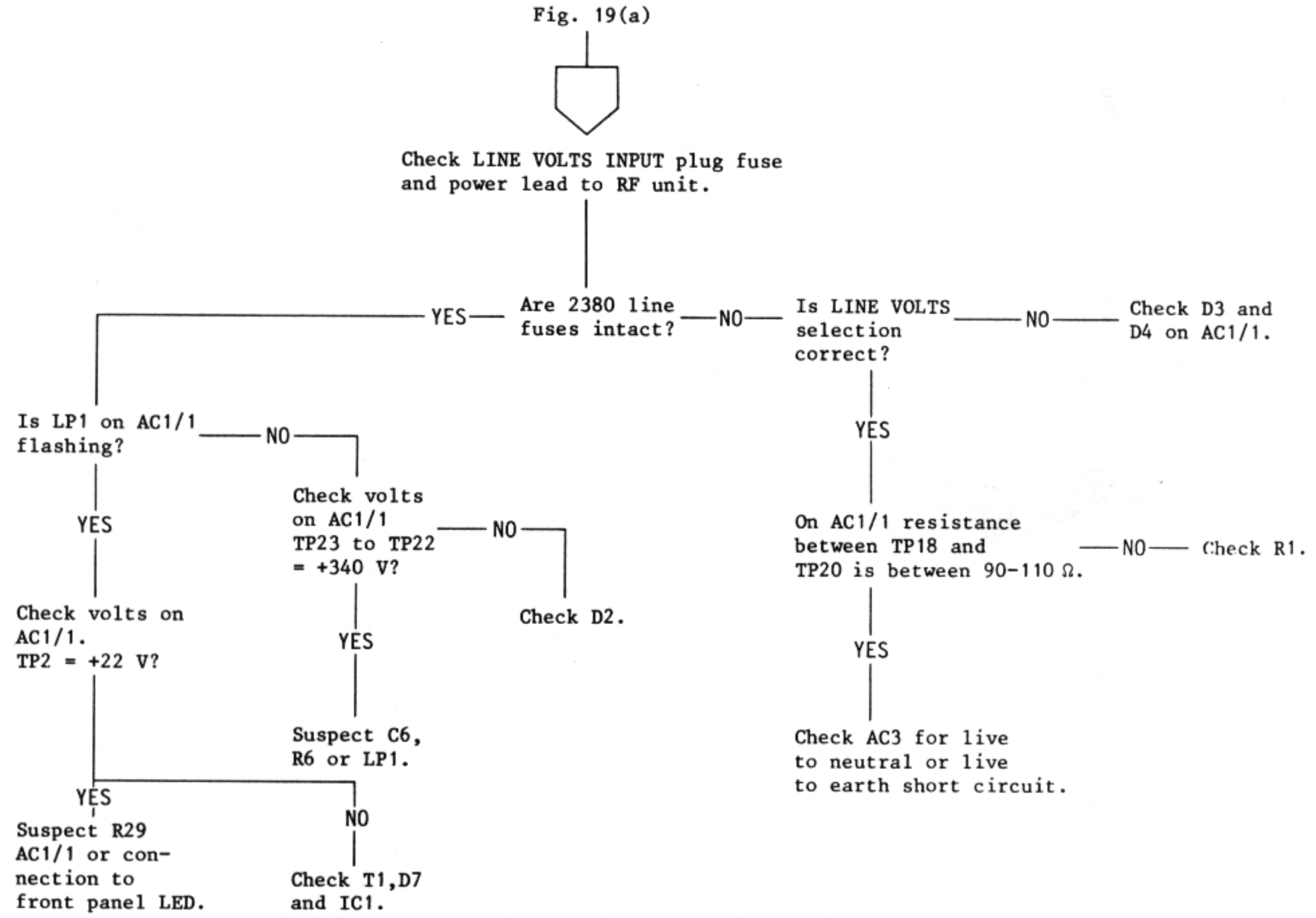


Fig. 19(b) Fault location chart - Power Supply (PSU1)

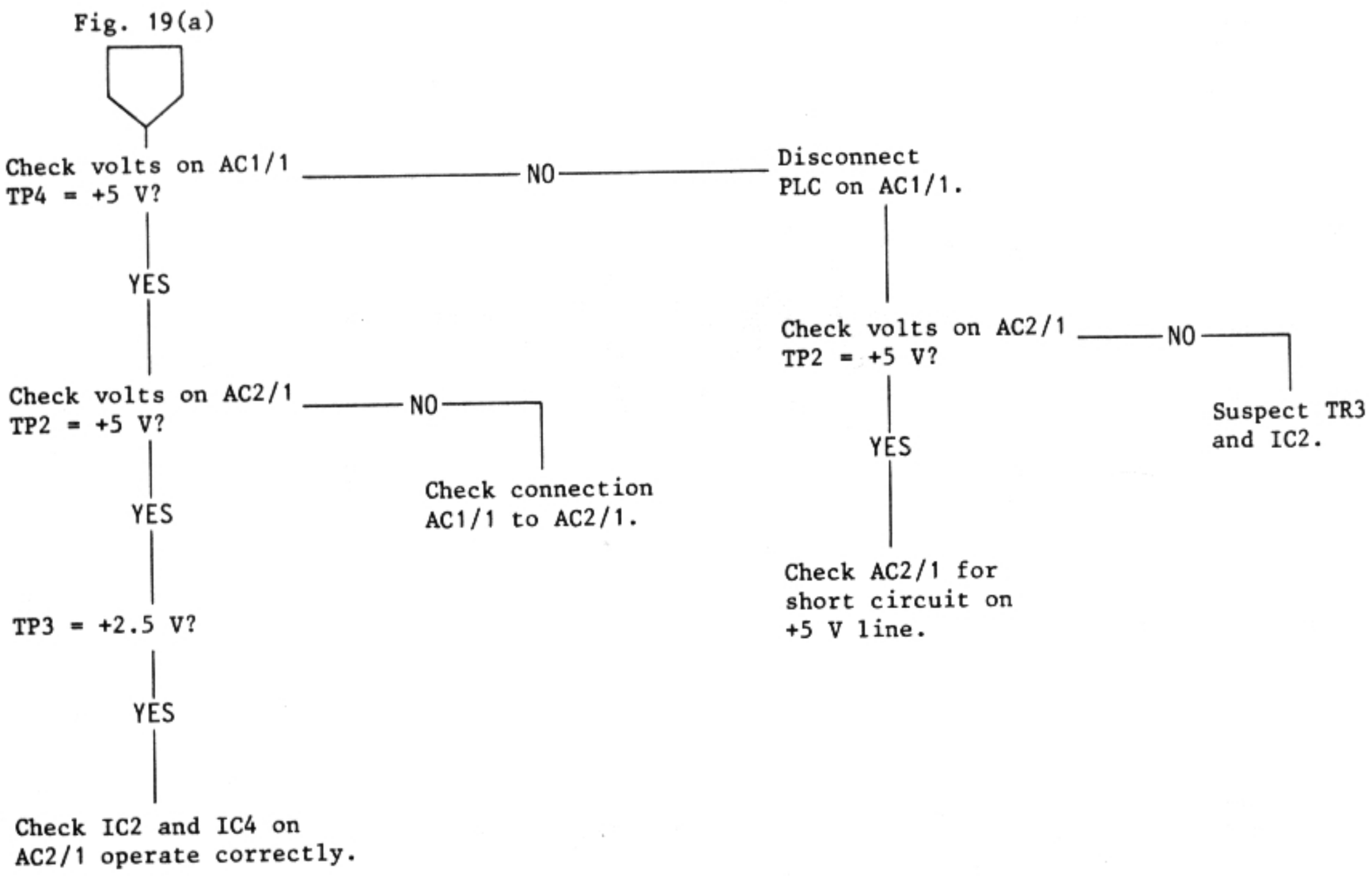


Fig. 19(c) Fault location chart - Power Supply (PSU1)

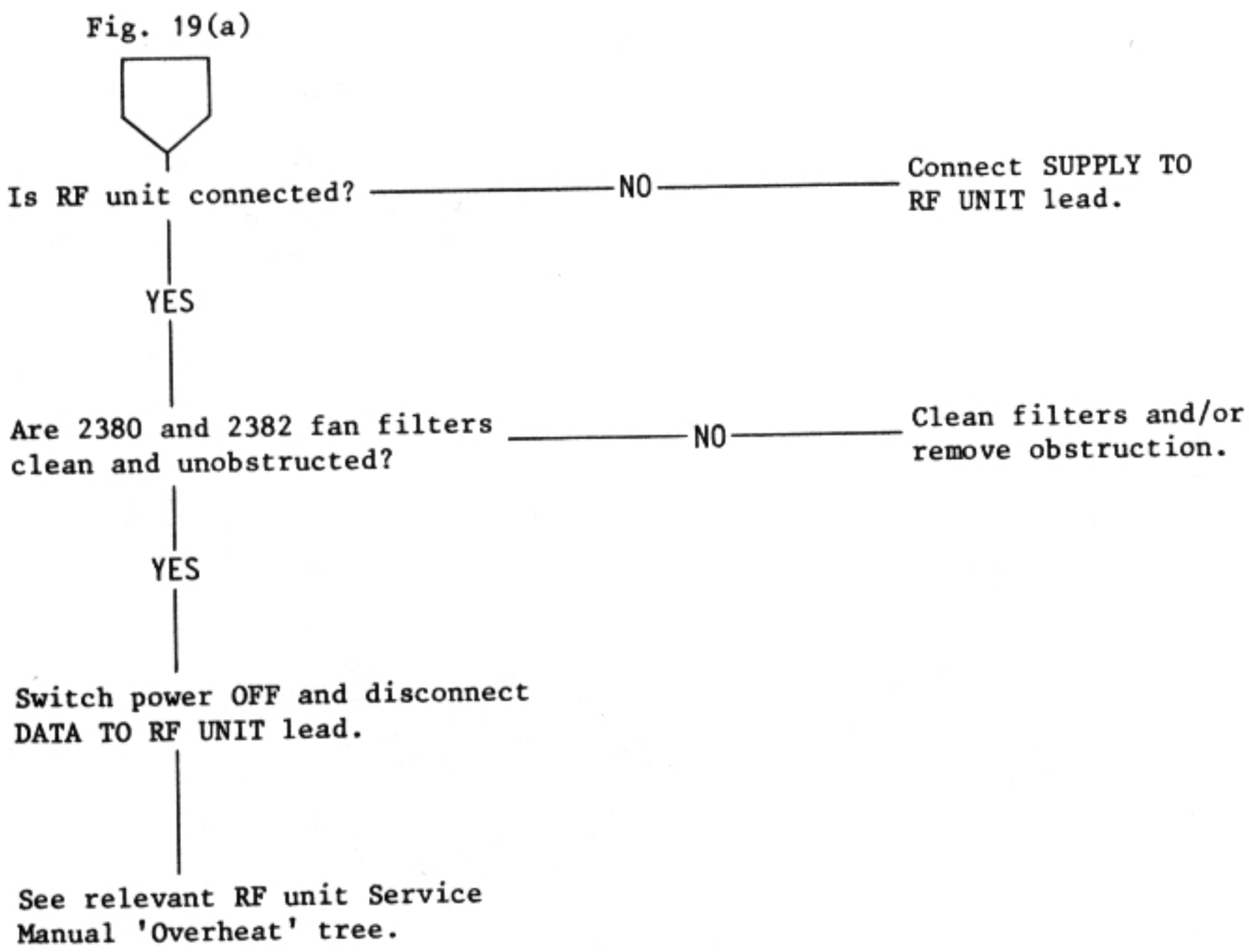


Fig. 19(d) Fault location chart - Overheat or no RF Unit

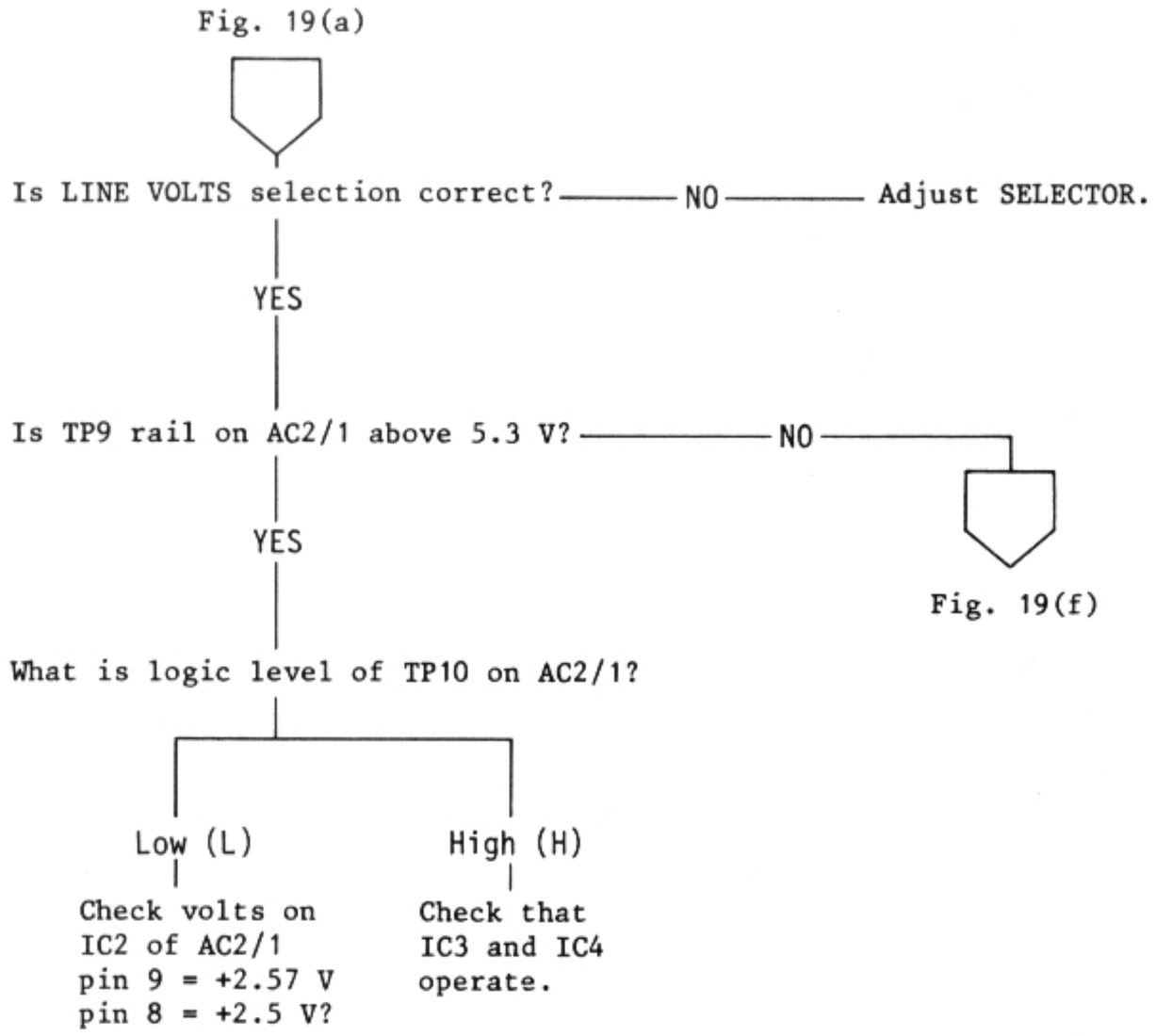


Fig. 19(e) Fault location chart - Low line input

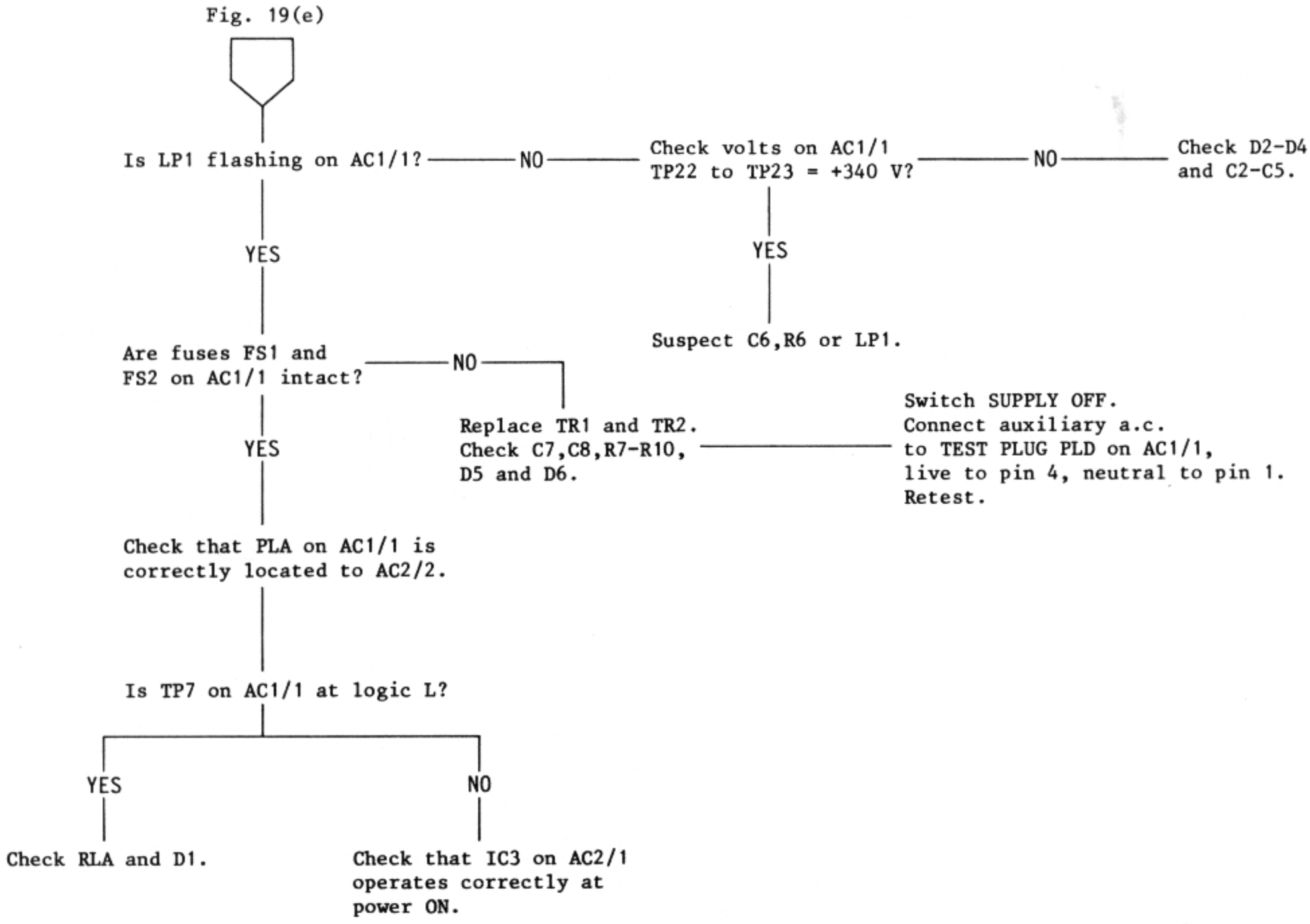
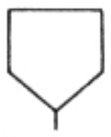


Fig. 19(f) Fault location chart - Low line input (cont.)

Fig. 19(a)



Disconnect RF unit and also PLC and PLD of AC2/1. Test with PLE TEST plug on AC2/1 shorted.

Overvoltage persists? — NO — Fault in +5.35 V OVERVOLTAGE DETECTOR. Are the voltages correct on AC2/1, IC2(b)? pin 3 = +5 V, pin 7 = +2.5 V and pin 6 = 0 V.

YES

Operate the controller section separately via PLD TEST plug on AC1/1. Monitor the +5.35 V output and the waveform on TP8 of AC1/1 whilst increasing the line input voltage.

YES — Check operation of IC3 and IC4(c) on AC2/1.

NO — Suspect IC2.

Does the +5.35 V rail stabilize at +5.35 V and the duty cycle of the waveform at TP8 of AC1/1 decrease as the line voltage increases? — NO — Feedback is not operating.

YES

Feedback is operating.
Check -14.5 V rail and D22 on AC2/1.

Does voltage of IC2 pin 1 = +5 V on AC1/1? — NO — Check on AC1/1 that TP4 is at +5 V. Suspect R18 or IC2.

YES

On AC1/1 is the voltage at TP10 +5 V when TP27 is at +5.35 V? — NO — Suspect R19 and R20 on AC1/1.

YES

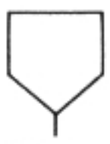
Replace IC2 on AC1/1.

Fig. 19(g) Fault location chart - Overvoltage

CAUTION.

The primary CURRENT LIMIT DETECTOR (components T3,D11,D12,R15-R17 on AC1/1) should under no circumstances be disabled by linking tags A and B or pins 6 and 7 on IC2, when there is a possibility of overload. Failure to limit the FET's current to approximately 4 A will result in their destruction.

Fig. 19(a)



Move link on TEST plug PLE on AC1/1 from 1 and 2 to 2 and 3 to disable the external sync. to the supply. On retest is OVERLOAD LED 'ON'?

NO → Sync. fault to supply exists. Check that sync from IC15 pin 8 on AB1 is 125 kHz at t.t.l. level.

YES

Disconnect RF unit and restart SUPPLY. Is any FAULT INDICATION ON?

OVERHEAT OR NO RF UNIT → Short TP12 to TP1 on AC2/1.

OVERLOAD

Disconnect PLC and PLD on AC2/1. Restart SUPPLY and check FAULT INDICATION.

No fault indication → A fault in 2380 causes overload. Reconnect PLC and PLD on AC2/1. Remove all AB p.c.b's then recheck. If overload ceases suspect AD1/1 otherwise replace AB p.c.b's in turn until faulty board is detected.

OVERLOAD

Supply fault exists. Disconnect PLA on AC1/1 then restart SUPPLY. Check FAULT INDICATION.

No fault indication → Fault with T1 secondary supplies on AC2/1.

Disconnect from AC1/1. If inductance of T1 primary on AC2/1 is less than 3 mH there may be an internal or external short circuit loading T1.

OVERLOAD

Fault exists in 'power up' reset circuit : IC3, OVERLOAD SAMPLER IC7 or latch IC6 on AC2/1.

Fig. 19(h) Fault location chart - Overload

RF UNIT
Fig. 2(i)(b)

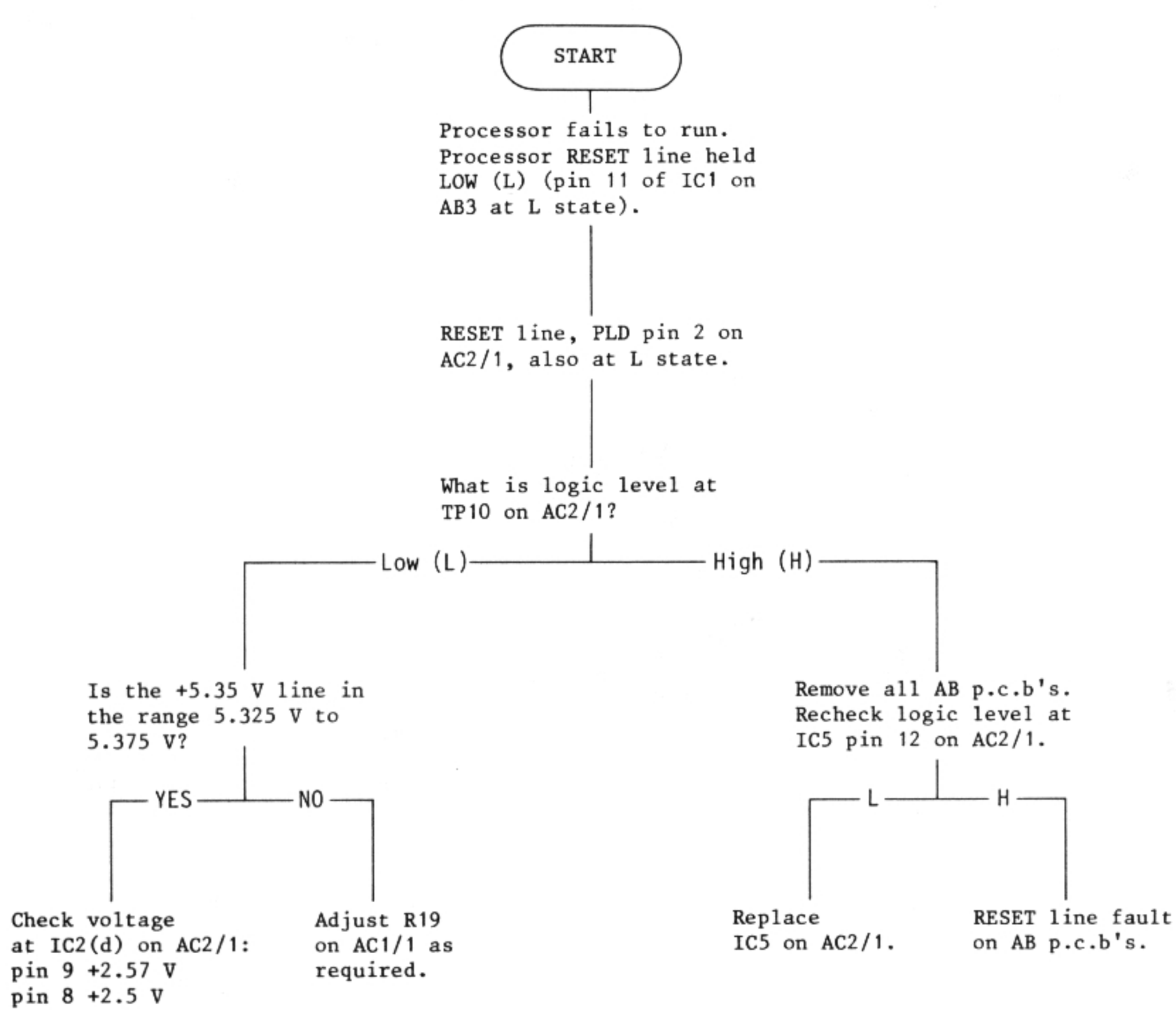


Fig. 19(j) Fault location chart - Supplementary faults (a)

RF UNIT
Fig. 2(i)(b)

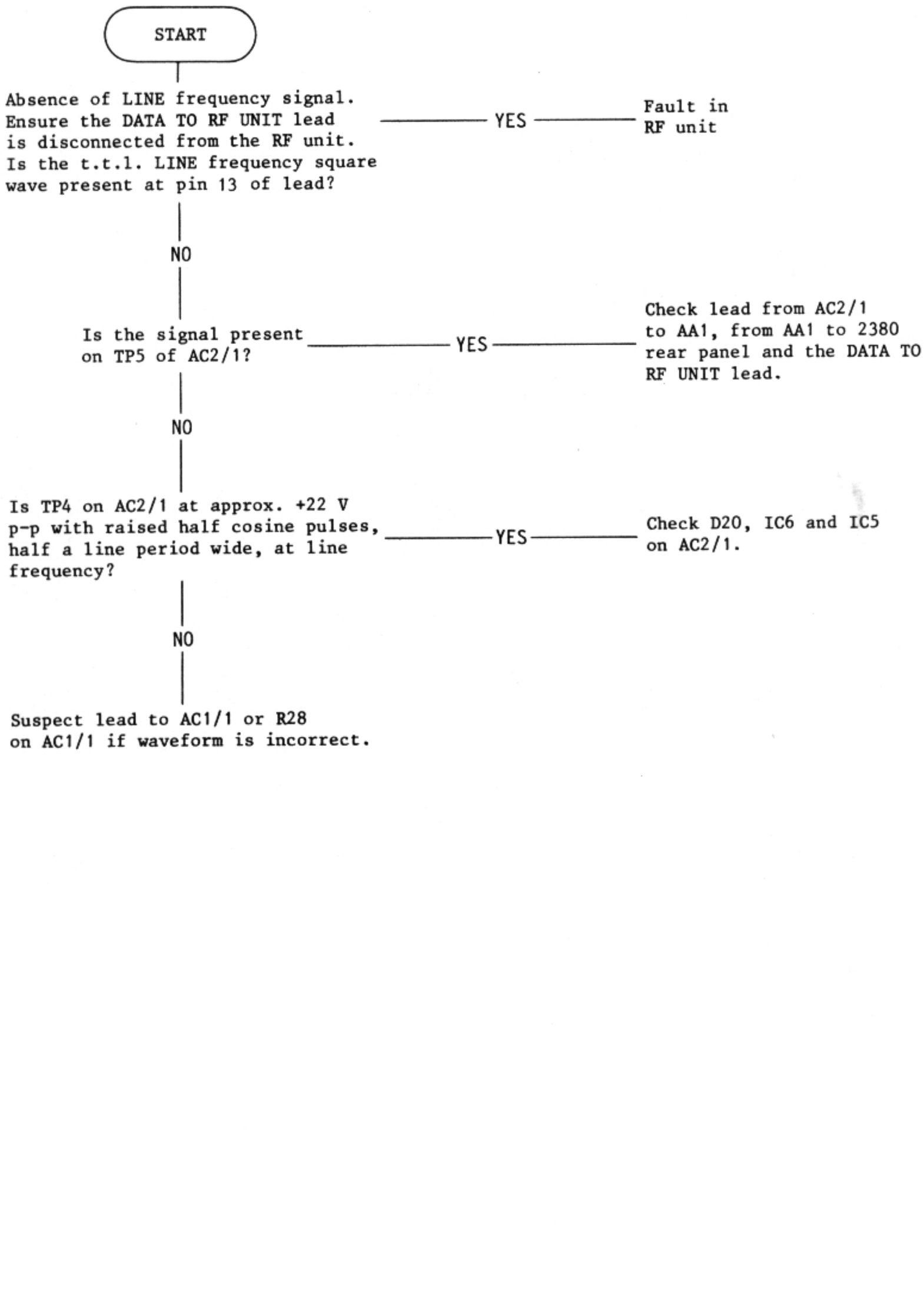


Fig. 19(k) Fault location chart - Supplementary faults (B)

RF UNIT
Fig. 2 (i)(c)

START

The p.s.u. is operating correctly - all front panel key lamps flashing, but there is a fault in the Video section.
For the following tests :
All AB p.c.b's must be present and operating.
All components and test points (TPs) are on AD1/1 unless stated otherwise.
All voltages are measured with respect to TP1 on AD1/1.
Voltages must be measured with the correct horiz. sync. frequency of 15.66 kHz. A free running (non-sync.) display board will give low ancillary voltages.

Turn SUPPLY 'OFF'. Remove 2380 top cover and put AD1/1 on an extender. Turn SUPPLY 'ON'. With front panel INTENSITY controls set to maximum and VIEW A, VIEW B and GRAT 'ON' is there a visible display?

YES

Analyse display and consult relevant figure.

1. Video not syncronized with raster (Fig. 20(c)).
2. Video not centred on screen (Fig. 20(d)).
3. Picture distorted (Fig. 20(e)).
4. Poor picture foxus (Fig. 20(f)).
5. Raster visible (Fig. 20(g)).
6. No video on raster (Fig. 20(h)).
7. Bright horizontal line on display (Fig. 20(i)).
8. Vertical strictions at left of display (Fig. 20(j)).
9. Minor graticule lines not visible at low INTENSITY settings (Fig. 20(k)).
10. Vertical retrace lines visible (Fig. 20(l)).
11. Raster visible and brightness varies with picture content (Fig. 20(m)).

NO

Increase INTENSITY R19.
Is there a visible raster?

YES

NO

Fig. 20(b)

Fig. 20(a) Fault location chart - Video section

Fig. 20(a)

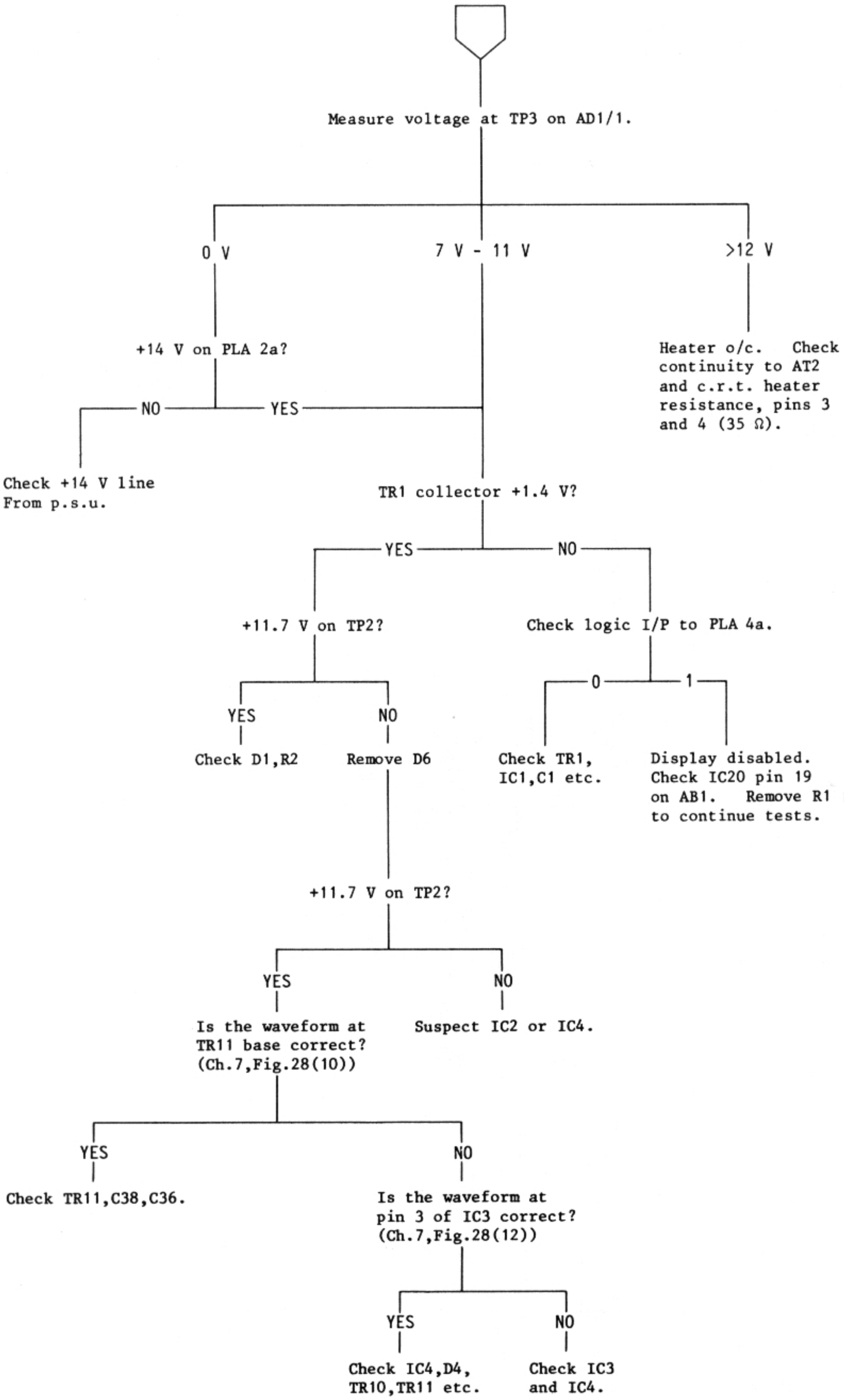


Fig. 20(b) Fault location chart - Vide section

Fig. 20(a)1

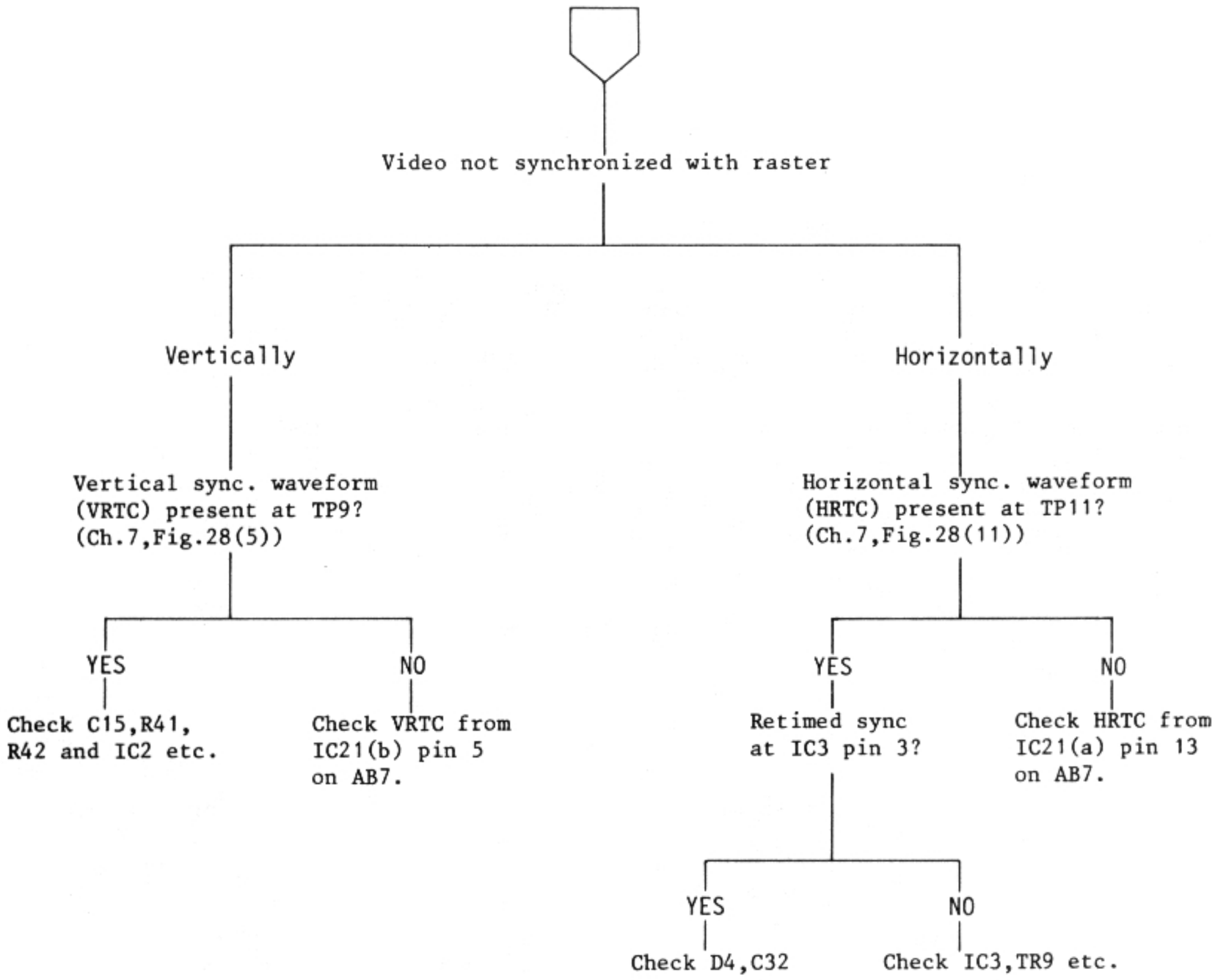


Fig. 20(c) Fault location chart - Video section

Fig. 20(a)2

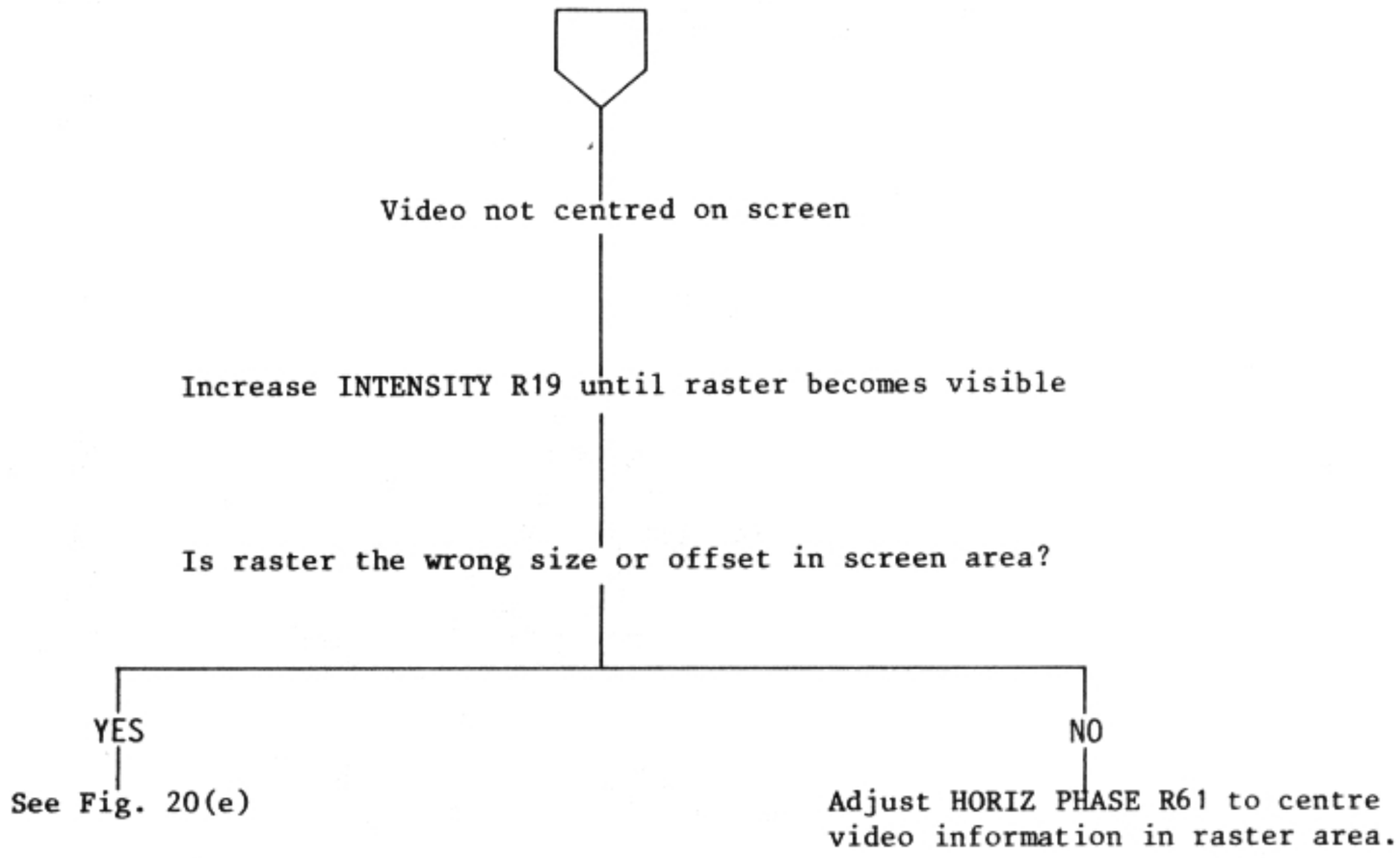


Fig. 20(d) Fault location chart - Video section

Fig. 20(a)3

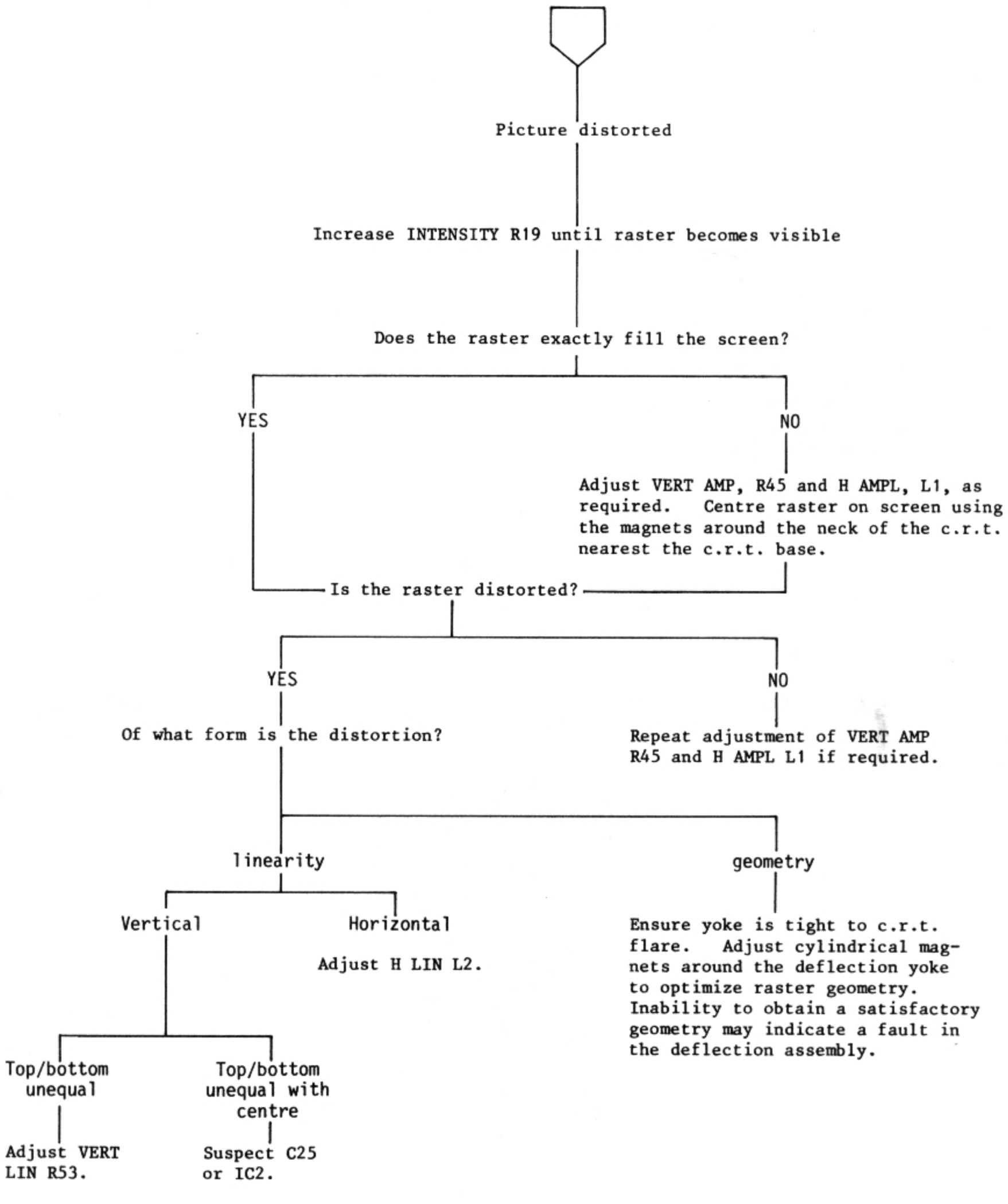


Fig. 20(e) Fault location chart - Video section

Fig. 20(a)4

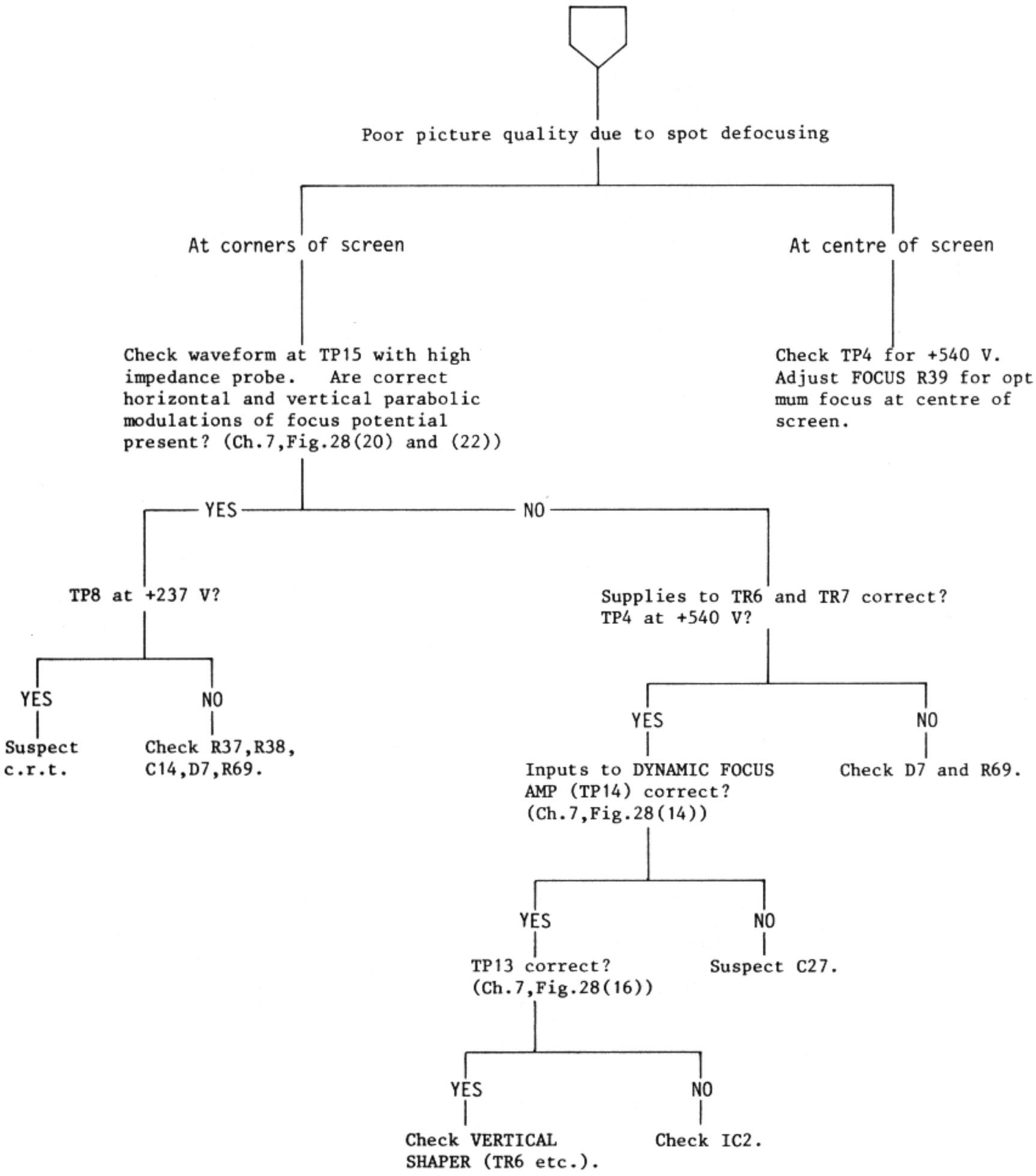


Fig. 20(f) Fault location chart - Video section

Fig. 20(a)5

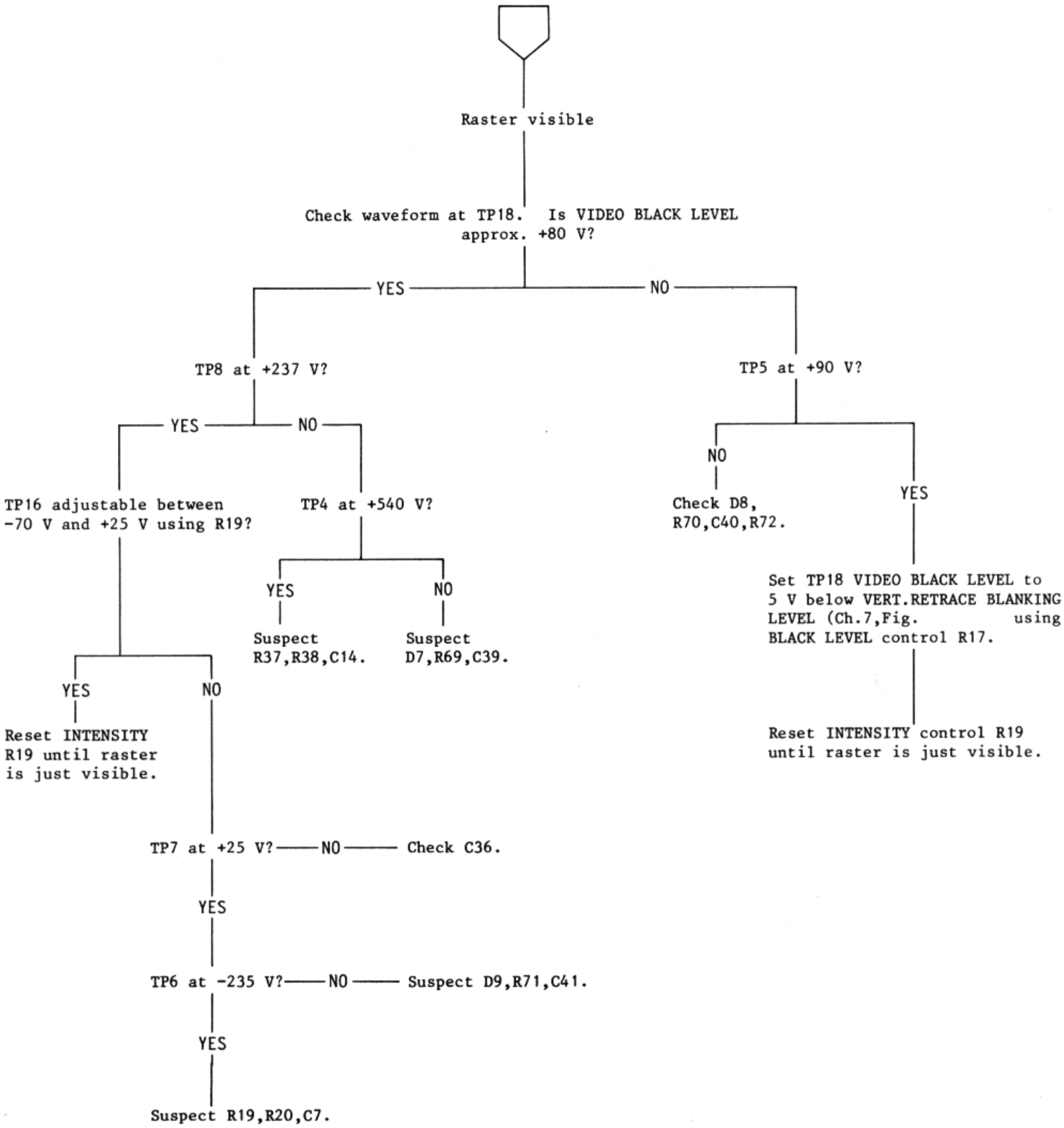


Fig. 20(g) Fault location chart - Video section

Fig. 20(a)6

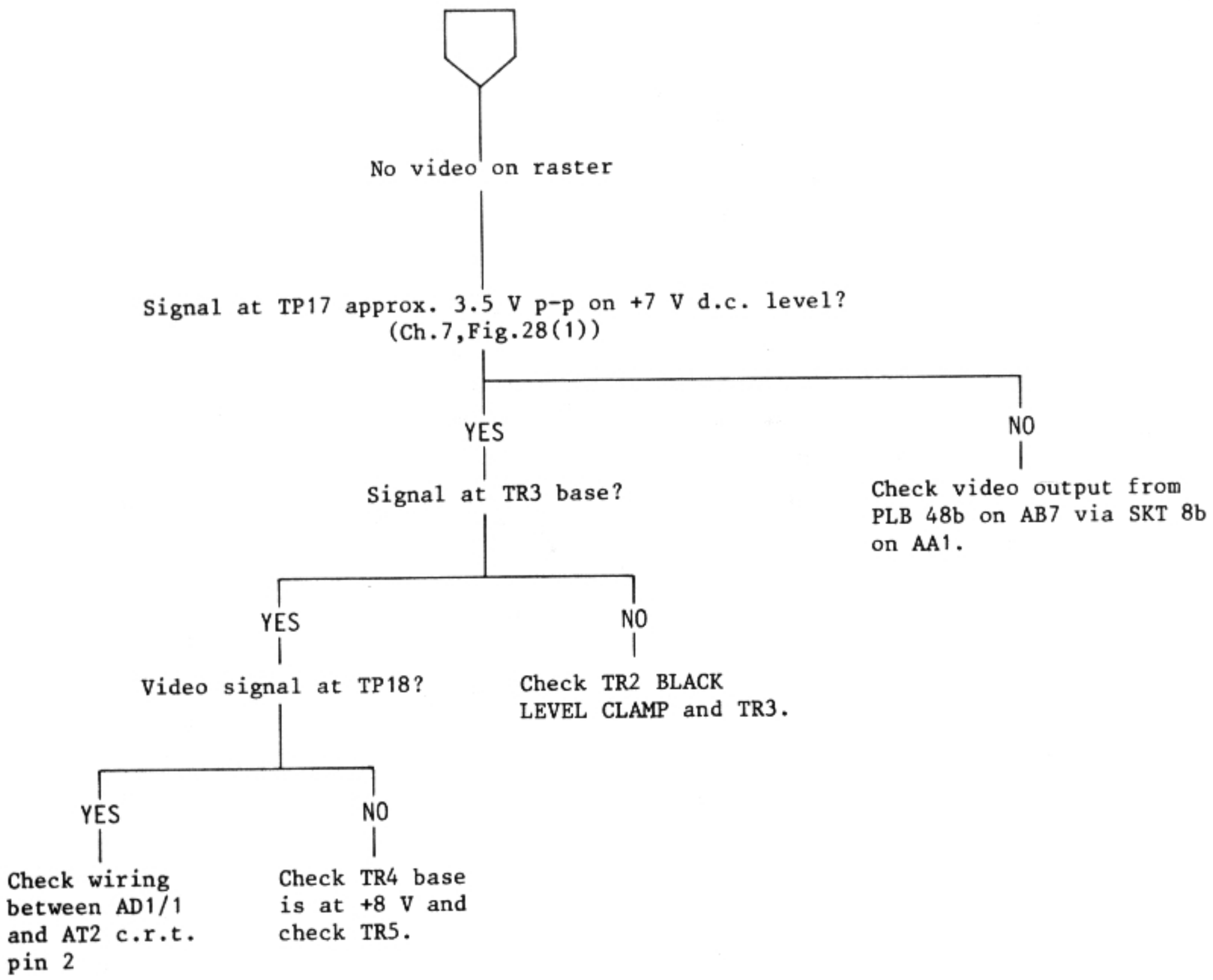


Fig. 20(h) Fault location chart - Video section

Fig. 20(a)7

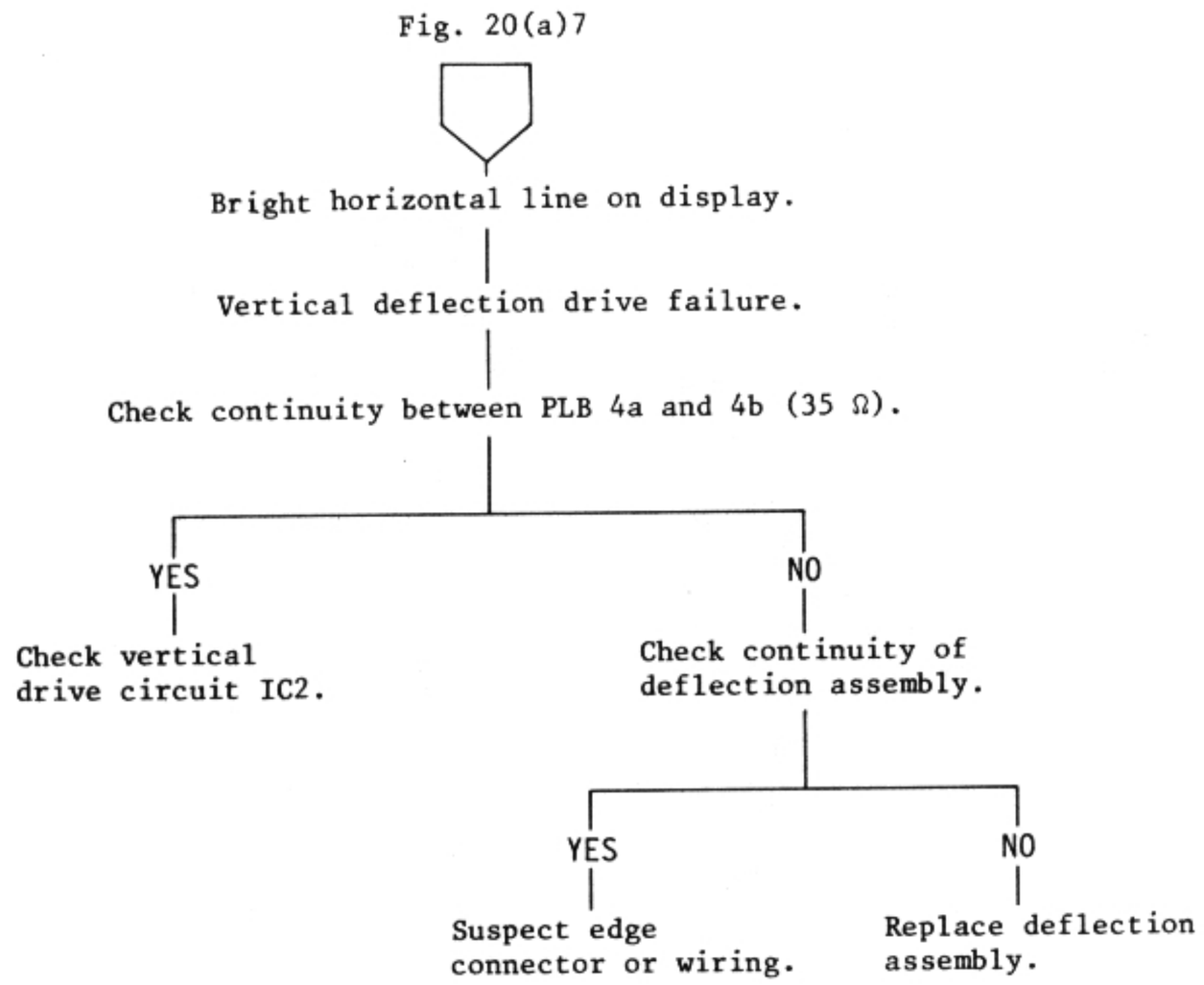


Fig. 20(i) Fault location chart - Video section

Fig. 20(a)8

Vertical strictions at left of display

H AMPL and/or H LIN (L1/L2) inductor damping network open circuit. Check C42,C43,R73 and R74.

Fig. 20(j) Fault location chart - Video section

Fig. 20(a)9

Minor graticule lines not visible at low INTENSITY settings

Incorrect BLACK LEVEL setting. Check at TP18 that VIDEO BLACK LEVEL set by R17 is 5 V below VERT. RETRACE BLANKING LEVEL (Ch.7,Fig.) then adjust R19 until raster is just visible.

Fig. 20(k) Fault location chart - Video section

Fig. 20(a)10

Vertical retrace lines visible

Vertical blanking inoperative. Check for VERT. RETRACE BLANKING pulse at TP10 (Ch.7,Fig.28(b)). Check D2.

Is VIDEO BLACK LEVEL (TP18) 5 V below VERT.RETRACE BLANKING LEVEL? (Ch.7,Fig.). If not adjust BLACK LEVEL R17.

Fig. 20(l) Fault location chart - Video section

Fig. 20(a)11

Raster visible and brightness varies with picture content

Check BLACK LEVEL CLAMP TR2.

Fig. 20(m) Fault location chart - Video section

RF UNIT
Fig. 2(i)(c)

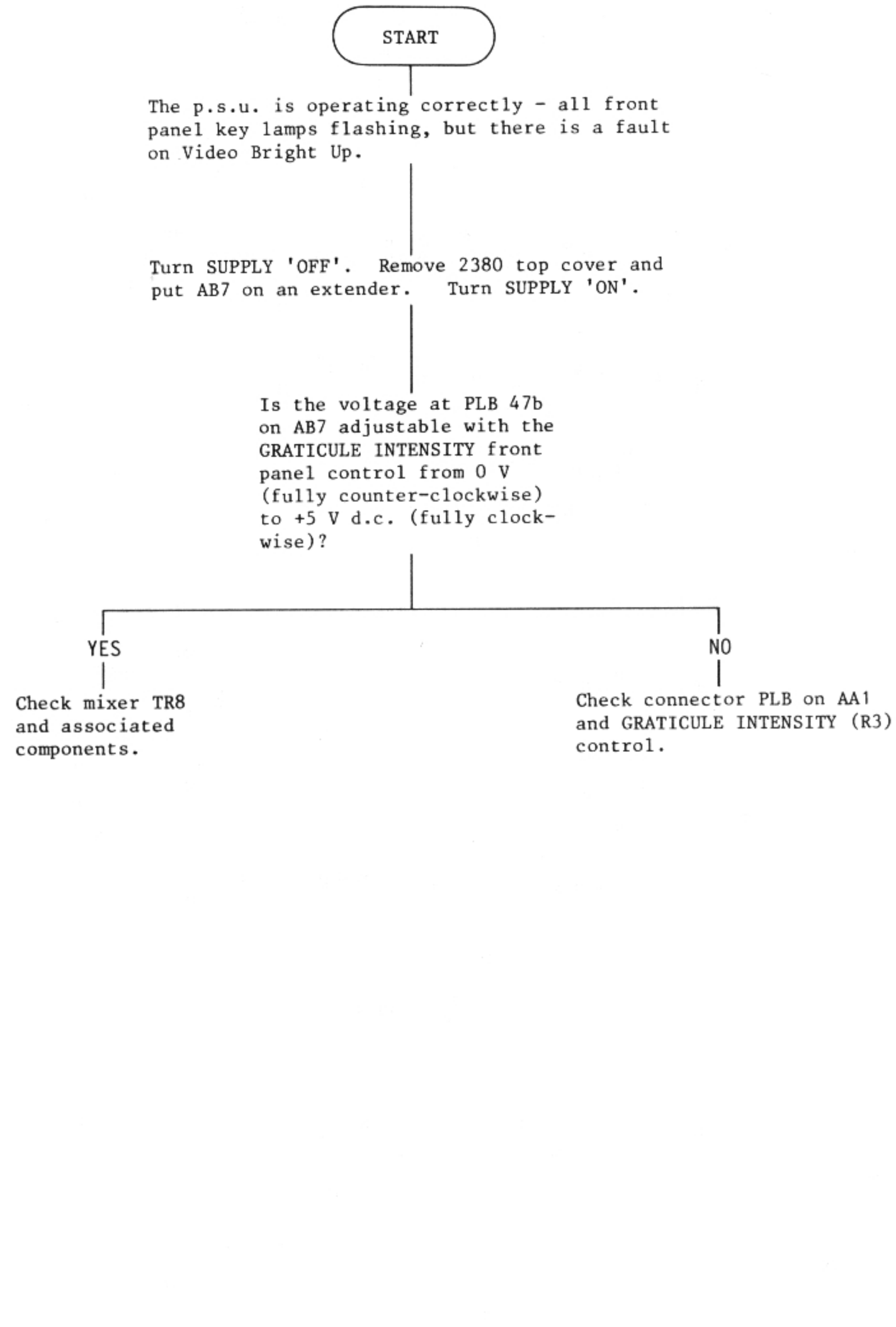


Fig. 21 Fault location chart - Video BU

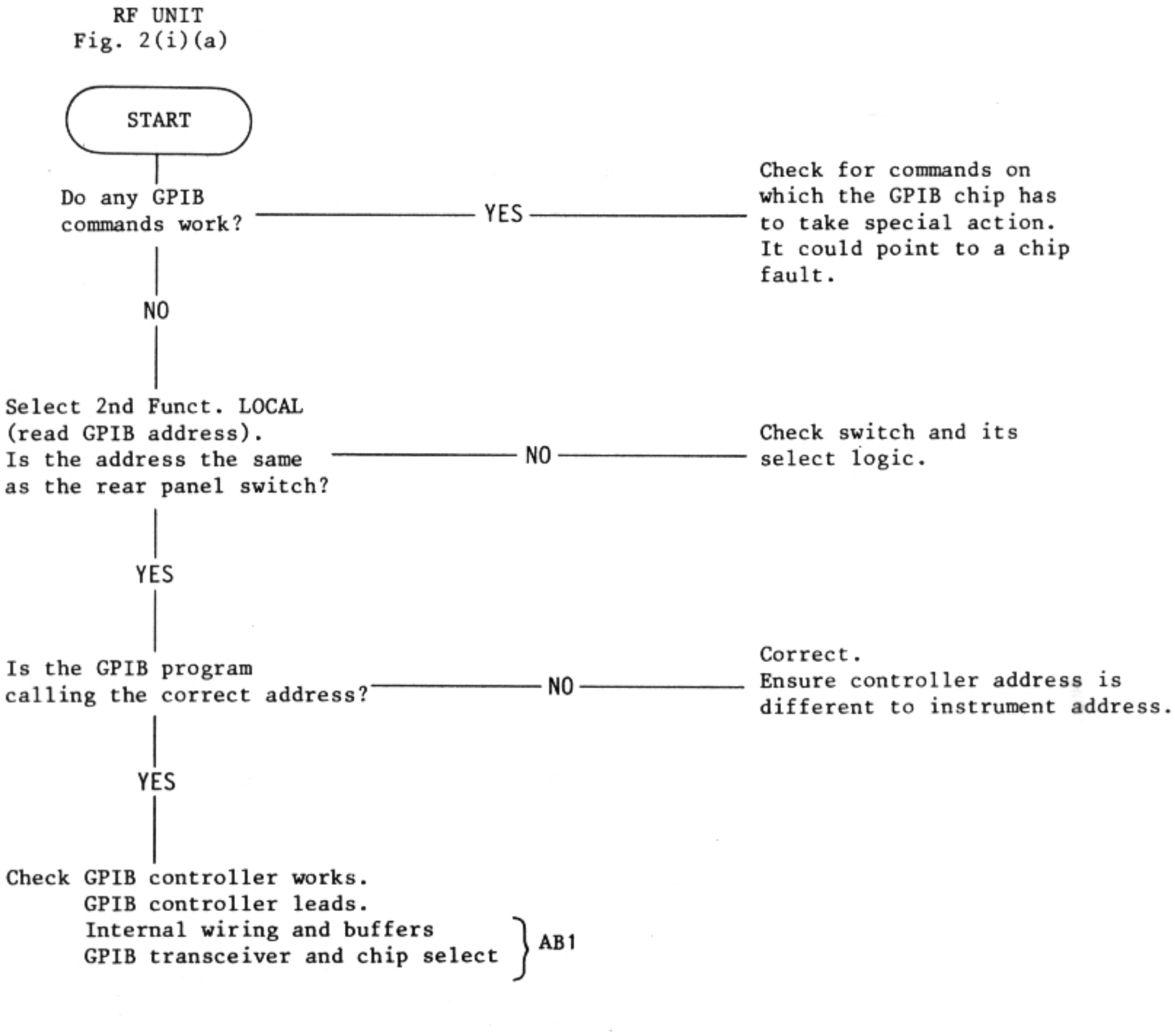


Fig. 22 Fult location chart - GPIB section

Chapter 6

REPLACEABLE PARTS

CONTENTS

INTRODUCTION

1. Each sub-assembly or printed circuit board in this instrument has been allocated a unit identification, e.g. A0, AA2.

2. The complete component reference carries its unit number as a prefix e.g. AB3C3 (capacitor C3 on the memory board) but for convenience in the text and on circuit diagrams the prefix is not used. However, when ordering replacements or in correspondence the complete component reference must be quoted.

ABBREVIATIONS

3. The components are listed in alphanumerical order of the complete circuit reference and the following abbreviations are used :

C	:	capacitor
Carb	:	carbon
Cer	:	ceramic
D	:	semiconductor diode
Elec	:	electrolytic
FS	:	fuse
IC	:	integrated circuit (package)
L	:	inductor
LP	:	lamp
ME	:	meter
Met	:	metal
Mic	:	mica
Min	:	minimum
Ox	:	oxide
PL	:	plug
Plas	:	plastic
R	:	resistor
S	:	switch
SK	:	socket
T	:	transformer
Tant	:	tantalum
TP	:	terminal
TR	:	transistor
Var	:	variable
W	:	watts at 70^{0}C
WW	:	wirewound
X	:	ferrite bead, cable, opto detector, etc.
XL	:	crystal

COMPONENT VALUES

4. One or more of the components fitted in the equipment may differ from those listed in this chapter for any of the following reasons:

(a) Components indicated by an * have their values selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the equipment is maintained.

(c) As part of a policy of continuous development, components may be changed in value or type to obtain detailed improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the equipment.

ORDERING

6. When ordering replacements, address the order to our Service Division (address at rear of manual) or nearest agent and specify the following for each component required:-

(1) Type# and serial number of equipment.
(2) Complete circuit reference.
(3) Description.
(4) Part number.

#As given on the serial number label at the rear of the equipment; if this is superseded by a model number label, quote the model number instead of the type number.

Circuit Ref	Description	Part Number
Board A0	- Display unit 2380	
7.	When ordering, prefix circuit reference with A0	
	Complete unit	02380-006
LP1	LAMP LED 5082-4950 3V GREEN	28624-113C
MP1	KNOB 14.5MM 1/8 BORE (LINE)	41149-050Y
MP2	KNOB ASSY 10.5MM 4.0 I/D	41149-058W
MP3	KNOB ASSY 32MM 4.0 I/D	41149-068R
MP6	PANEL HANDLE ASSY	41700-382P
R1	RV CERM 1K LIN 2W 10% SINGLE	25737-004W
R2	RV CERM 1K LIN 2W 10% SINGLE	25737-004W
R3	RV CERM 1K LIN 2W 10% SINGLE	25737-004W
SKA	CON EDGE FEM 8 FXD 0.15" 2S	23435-043E
X11	CABLE ASSY, AC0 TO AA1 POWER	43129-987F
X12	CABLE ASSY, AC0 TO AA1 SIGNAL	43129-996T
X13	CABLE ASSY, AA1 TO RF UNIT	43129-997P
X14	CABLE ASSY, AB8 TO OPTIONS	43129-998X
X15	CABLE ASSY, AB8 TO VIDEO OUTPUT	43129-999M
X20	MOTHER BOARD AA1	44828-500D
X21	AUX. INTERCONN. AA2	44828-501T
X22	GPIB + KEYBOARD AB1	44828-503X
X23	I/P + AVERAGER AB2	44828-504M
X24	PROCESSOR + MEM. AB3	44828-505C
X25	MATHS BOARD AB4	44828-506R
X26	B DISPLAY STORE AB5	44828-507B
X27	A DISPLAY STORE AB6	44828-508K
X28	CRT CONTROLLER AB7	44828-509A
X32	GPIB CONN. PCB AR1	44828-516U
X33	DISPLAY DRIVE AD1/1	44828-519L
X34	CRT BASE PCB AT2	44828-520Y
X36	KEYBOARD AF1	44828-524F
X39	POWER SUPPLY AC0/1	44990-540K
X40	ROTARY ENCODER AZ1	44990-455W
X204	CON PART D SCREWLOCK FEM	23435-981V
X208	MOD CRT SUP TBY5-B SCAN COIL	28231-403M
X209	VALVE CRT 190FB31 E7-91 7"90DE	28235-617C
*X210	MAGNET TBX15 3MM CRT CORRECTOR	28238-157M
X250	CABLE PWR, AC SUPPLY	43123-076Y

Note; PROGRAMMED PROMS are listed under Units AB3 & AB7

Circuit Ref	Description	Part Number
Unit AA1	- Logic mother board	
8.	When ordering, prefix circuit reference with AA1	
	Complete unit	44828-500D
PLC	CON PCB MALE 6/0.2 STR TIN	23435-917D
SKA	CON EDGE FEM 60 FXD .1" 2S K7	23435-819M
SKB	CON EDGE FEM 60 FXD .1" 2S K7	23435-819M
SKC	CON EDGE FEM 60 FXD .1" 2S K7	23435-819M
SKD	CON EDGE FEM 60 FXD .1" 2S K7	23435-819M
SKE	CON EDGE FEM 60 FXD .1" 2S K7	23435-819M
SKF	CON EDGE FEM 60 FXD .1" 2S K7	23435-819M
SKG	CON EDGE FEM 60 FXD .1" 2S K7	23435-819M
SKH	CON EDGE FEM 60 FXD .1" 2S K7	23435-819M
SKJ	CON EDGE FEM 8 FXD .1 2S K7	23435-838J
Board AA2	- Auxiliary connector	
9.	When ordering, prefix circuit reference with AA2	
	Complete unit	44828-501T
SKA	CON EDGE FEM 30 FXD .1 2S K7	23435-839F
SKB	CON EDGE FEM 30 FXD .1 2S K7	23435-839F
Board AB1	- I/O and Keyboard communication	
10.	When ordering, prefix circuit reference with AB1	
	Complete unit	44828-503X
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description	Part Number
Board AB1	- I/O and Keyboard communication (Contd.)	
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C24	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C25	CAP CER 470P 63V 10% PLATE	26383-582T
C26	CAP CER 220P 63V 2% PLATE	26343-481S
C27	CAP ELEC 1U0 50V 20% L/LEAK	26421-007Z
C28	CAP ELEC 1U0 50V 20% L/LEAK	26421-007Z
C29	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C30	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
IC1	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC2	ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC3	ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC4	ICM MP SUP 8291A GPIB TALK/LIS !	28467-014C
IC5	ICD BUFF 74LS240 OCT 3ST I	28469-187R
IC6	ICM MP SUP 8259A PROG INT CTLR !	28467-012X
IC7	ICD OR 74LS32 QUAD 2INP	28466-108U
IC8	ICD DEC/DMX 74LS139 DUAL 2-4	28465-029V
IC9	ICD INV 74LS04 HEX	28469-171L
IC10	ICD AND 74LS08 QUAD 2INP	28466-012L
IC11	ICD CTR 74LS93 4BIT BIN 2,8,16	28464-117W
IC12	ICD CTR 74LS390 DUAL 4BIT DEC	28464-127R
IC13	ICD MONO 74LS123 DUAL RETR	28468-309B
IC14	ICD XOR 74LS86 QUAD 2INP	28466-406C
IC15	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC16	ICD MONO 74LS221 DUAL	28468-404D
IC17	ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC18	ICD BUFF 3448 QUAD GPIBTXRX 3S	28469-190R
IC19	ICM MP SUP 8251A USART DIL28 !	28469-189K
IC20	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC21	ICD BUFF 74LS245 OCT TXRX	28469-188B
IC22	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC23	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC24	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
R1	RES MO 1K0 1/2W 2% 250PPM	24573-073W
R2	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R3	RES MF 1K0 1/4W 2% 250PPM	24773-073W

Circuit Ref	Description	Part Number
Board AB1	- I/O and Keyboard communication	(Contd.)
R4	RES MO 56R 1/2W 2% 250PPM	24573-043T
R5	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R6	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R7	RES NET 2K7 2% 7SIP	24681-604G
R8	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R9	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R12	RES MF 680R 1/4W 2% 100PPM	24773-269K
R13	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R14	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R15	RES MF 360R 1/4W 2% 100PPM	24773-262T
R16	RES MF 10K 1/4W 2% 100PPM	24773-297M
R17	RES NET 100R 2% 8SINGLE DIL	24681-515R
R18	RES NET 100R 2% 8SINGLE DIL	24681-515R
R19	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R20	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R21	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R22	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R23	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R24	RES MF 560R 1/4W 2% 100PPM	24773-267R
TR1	TR NSI BC237A 45V 150M - GEN	28455-421X
TR2	TR NSI BC237A 45V 150M - GEN	28455-421X
Board AB2	- Input signal data processing	
11.	When ordering, prefix circuit reference with AB2	
	Complete unit	44828-504M
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description	Part Number
Board AB2	- Input signal data processing	(Contd.)
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C24	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C25	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C26	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C27	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C28	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C29	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C30	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C31	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C32	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C33	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C34	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C35	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C36	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C37	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C38	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C39	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C40	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C41	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C42	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C43	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C44	CAP CER 180P 63V 2% PLATE	26343-480V
C45	CAP CER 180P 63V 2% PLATE	26343-480V
C46	CAP CER 120P 63V 2% PLATE	26343-478S
C47	CAP CER 680P 63V 2% PLATE	26383-583P
C48	CAP CER 470P 63V 10% PLATE	26383-582T
C49	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C50	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C51	CAP CER 470P 63V 2% PLATE	26343-582T
C52	CAP CER 470P 63V 10% PLATE	26383-582T
IC1	ICD XOR 74LS86 QUAD 2INP	28466-406C
IC2	ICD OR 74LS32 QUAD 2INP	28466-108U
IC3	ICD AND 74LS08 QUAD 2INP	28466-012L
IC4	ICD INV 74LS04 HEX	28469-171L
IC5	ICD COMP 74LS85 4BIT	28469-371E

Circuit Ref	Description	Part Number
Board AB2	- Input signal data processing	(Contd.)
IC6	ICD COMP 74LS85 4BIT	28469-371E
IC7	ICD COMP 74LS85 4BIT	28469-371E
IC8	ICD COMP 74LS85 4BIT	28469-371E
IC9	ICD COMP 74LS85 4BIT	28469-371E
IC10	ICD COMP 74LS85 4BIT	28469-371E
IC11	ICD COMP 74LS85 4BIT	28469-371E
IC12	ICD COMP 74LS85 4BIT	28469-371E
IC13	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC14	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC15	ICD SH REG 74LS164 8BIT SIPO	28467-515G
IC16	ICD SH REG 74LS164 8BIT SIPO	28467-515G
IC17	ICD SH REG 74LS164 8BIT SIPO	28467-515G
IC18	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC19	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC20	ICM MP SUP AM9513A TIM´G CTLR !	28469-416G
IC21	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC22	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC23	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC24	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC25	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC26	ICD INV 74LS04 HEX	28469-171L
IC27	ICD AND 74LS08 QUAD 21NP	28466-012L
IC28	ICD OR 74LS32 QUAD 2INP	28466-108U
IC29	ICD FF JK 74LS112 DUAL -EDG TR	28462-020M
IC30	ICD CTR 74LS90 4BIT DEC 2,5,10	28464-014S
IC31	ICD CTR 74LS90 4BIT DEC 2,5,10	28464-014S
IC32	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC33	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC34	ICD MONO 74LS221 DUAL	28468-404D
IC35	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC36	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC37	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC38	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC39	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC40	ICD OR 74LS32 QUAD 2INP	28466-108U
IC41	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC42	ICD OR 74LS32 QUAD 2INP	28466-108U
IC43	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
R1	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R2	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R3	RES MF 8K2 1/4W 2% 100PPM	24773-295P

Circuit Ref	Description	Part Number
Unit AB2	- Input signal data processing	(Contd.)
R4	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R5	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R6	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R7	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R8	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R9	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R10	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R11	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R12	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R13	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R14	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R15	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R16	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R17	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
Board AB3/1	- uP, Mem, CS, 8088	
12.	When ordering, prefix circuit reference with AB3	
	Complete unit	44828-340G
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description		Part Number
Board AB3/1	- uP, Mem, CS, 8088		(Contd.)
C21	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C24	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C25	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C26	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C27	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C28	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C29	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C30	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C31	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C32	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C33	CAP CER 10N 50V 20% X7R MON AX		26346-120Y
C34	CAP ELEC 10U 35V 20% SUBMIN		26421-112Z
C35	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
C36	CAP ELEC 33U 25V 20% SUBMIN		26421-115U
D1	DI H/CARR BAT29 5V	!	28349-014L
D2	DI H/CARR BAT29 5V	!	28349-014L
IC1	ICD MP SUP 8284A CLOCK GENR		28467-026Y
IC2	ICD INV 74LS04 HEX		28469-171L
IC3	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC4	ICD LATCH 74LS373 OCT 3ST		28462-410E
IC5	ICD BUFF 74LS244 OCT 3ST		28469-182T
IC6	ICD DEC/DMX 74LS138 3-8		28465-027F
IC7	ICD DEC/DMX 74LS138 3-8		28465-027F
IC8	ICD RAM HM6264P-15 8KX8 150NS	!	28469-312J
IC9	ICD RAM HM6264P-15 8KX8 150NS	!	28469-312J
IC10	ICD PROM 27128 16KX8 250NS UV	!	28471-019V
IC11	ICD PROM 27256 32KX8 200NS UV	!	Note (1)
IC12	ICD PROM 27256 32KX8 200NS UV	!	
IC13	ICD PROM 27256 32KX8 200NS UV	!	
IC14	ICD PROM 27256 32KX8 200NS UV	!	
IC15	ICD MP 8088 16/8BIT HMOS	!	28467-024E
IC16	ICD MUX 74LS257 QUAD 2INP 3ST		28469-712A
IC17	ICD MP SUP 8237 PROG DMA CTLR	!	28467-011P
IC18	ICD BUFF 74LS244 OCT 3ST		28469-182T
IC19	ICD BUFF 74LS244 OCT 3ST		28469-182T
IC20	ICD INV 74LS04 HEX		28469-171L

Circuit Ref	Description			Part Number
Board AB3/1	- uP, Mem, CS, 8088			(Contd.)
IC21	ICD OR 74LS32 QUAD 2INP			28466-108U
IC22	ICD AND 74LS11 TRIP 3INP			28466-014F
IC23	ICD LATCH 74LS373 OCT 3ST			28462-410E
IC24	ICD LATCH 74LS373 OCT 3ST			28462-410E
IC25	ICD AND 74LS08 QUAD 2INP			28466-012L
IC26	ICD BUFF 74LS245 OCT TXRX			28469-188B
IC27	ICD BUFF 74LS245 OCT TXRX			28469-188B
IC28	ICD MP SUP 8259A PROG INT CTLR	!		28467-012X
IC29	ICD DEC/DMX 74LS138 3-8			28465-027F
IC30	ICD DEC/DMX 74LS138 3-8			28465-027F
IC31	ICD OR 74LS32 QUAD 2INP			28466-108U
IC32	ICD PROM 27256 32KX8 250NS UV	!	}	Note (1)
IC33	ICD PROM 27256 32KX8 250NS UV	!		
R1	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R2	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R3	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R4	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R5	RES MF 10K 1/4W 2% 100PPM			24773-297M
R6	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R7	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R8	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R9	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R10	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R11	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R12	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R13	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R14	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R15	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R16	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R17	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R18	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R19	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R20	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R21	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R22	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R23	RES MF 4K7 1/4W 2% 100PPM			24773-289W
R24	RES MF 4K7 1/4W 2% 100PPM			24773-289W

Note (1) PROGRAMMED PROM
SET IC10-14, IC32,IC33 44533-191P
No interchanging should be attempted within programmed set.

Circuit Ref	Description	Part Number
Board AB3/1	- uP, Mem, CS, 8088	(Contd.)
SKC	CON JUMP FEM 2 1 ROW	23435-990X
SKD	CON JUMP FEM 2 1 ROW	23435-990X
SKE	CON JUMP FEM 2 1 ROW	23435-990X
SKF	CON JUMP FEM 2 1 ROW	23435-990X
SKG	CON JUMP FEM 2 1 ROW	23435-990X
SK10	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
SK11	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
SK12	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
SK13	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
SK14	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
SK32	S/C ACC SKT DIL28 LOW PROFILE	28488-045L
SK33	S/C ACC SKT DIL28 LOW PROFILE	28488-045L

Board AB4 - Mathematics operations

13. When ordering, prefix circuit reference with AB4

	Complete unit	44828-506R
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C24	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C25	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description	Part Number
Board AB4	- Mathematics operations	(Contd.)
C26	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C27	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C28	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C29	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C30	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C31	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C32	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C33	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C34	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C35	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C36	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C37	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C38	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C39	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C40	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C41	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C42	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C43	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C44	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C45	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C46	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C47	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C48	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C49	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C50	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C51	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C52	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C53	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C54	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
IC1	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC2	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC3	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC4	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC5	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC6	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC7	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC8	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC9	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC10	ICD OR 74LS32 QUAD 2INP	28466-108U
IC11	ICD AND 74LS08 QUAD 2INP	28466-012L
IC12	ICD OR 74LS32 QUAD 2INP	28466-108U
IC13	ICD INV 74LS04 HEX	28469-171L
IC14	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC15	ICD ADDER 74LS283 4BIT FULL	28469-397A

Circuit Ref	Description	Part Number
Board AB4	- Mathematics operations	(Contd.)
IC16	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC17	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC18	ICD DEC/DMX 74LS138 3-8	28465-027F
IC19	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC20	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC21	ICD INV 74LS04 HEX	28469-171L
IC22	ICD INV 74LS04 HEX	28469-171L
IC23	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC24	ICD INV 74LS04 HEX	28469-171L
IC25	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC26	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC27	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC28	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC29	ICD ADDER 74LS283 4BIT FULL	28469-397A
IC30	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC31	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC32	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC33	ICD DEC/DMX 74LS155 DUAL 2-4	28465-026J
IC34	ICD OR 74LS32 QUAD 2INP	28466-108U
IC35	ICD CTR 74LS161 4BIT BIN PRE	28464-118D
IC36	ICD AND 74LS08 QUAD 2INP	28466-012L
IC37	ICD OR 74LS32 QUAD 2INP	28466-108U
IC38	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC39	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC40	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC41	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC42	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC43	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC44	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC45	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC46	ICD FF D 74LS374 OCT +E TR 3ST	28462-618L
IC47	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC48	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC49	ICD DEC/DMX 74LS138 3-8	28465-027F
IC50	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC51	ICD BUFF 74LS244 OCT 3ST	28469-182T
IC52	ICD BUFF 74LS244 OCT 3ST	28469-182T
R1	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R2	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R3	RES NET 3K3 5% 9SIP	24681-612T
R4	RES NET 3K3 5% 9SIP	24681-612T
R5	RES NET 3K3 5% 9SIP	24681-612T

Circuit Ref	Description	Part Number
Board AB5	- Timing & B Display dynamic store	
14.	When ordering, prefix circuit reference with AB5	
	Complete unit	44828-507B
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C24	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C25	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C26	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C27	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C28	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C29	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C30	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C31	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C32	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C33	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C34	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C35	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C36	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C37	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description	Part Number
Board AB5	- Timing & B Display dynamic store (Contd.)	
C38	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C39	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C40	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C41	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C42	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C43	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C44	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C45	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C46	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C47	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C48	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C49	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C50	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C51	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C52	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C53	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C54	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C55	CAP CER 10P 63V .5PF PLATE	26343-465H
C56	CAP CER 180P 63V 2% PLATE	26343-480V
C57	CAP CER 10P 63V .5PF PLATE	26343-465H
C58	CAP CER 180P 63V 2% PLATE	26343-480V
C59	CAP PETP 100N 100V 10% RAD	26582-211B
C60	CAP CER 180P 63V 2% PLATE	26343-480V
C61	CAP CER 180P 63V 2% PLATE	26343-480V
C62	CAP PETP 100N 100V 10% RAD	26582-211B
C63	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C64	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C65	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C66	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C67	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C68	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C69	CAP CER 82P 63V 2% PLATE	26343-476G
IC1	ICD CTR 74LS161 4BIT BIN PRE	28464-118D
IC2	ICD AND 74LS08 QUAD 2INP	28466-012L
IC3	ICD AND 74LS08 QUAD 2INP	28466-012L
IC4	ICD INV 74LS04 HEX	28469-171L
IC5	ICD NAND 74LS10 TRIP 3INP	28466-351Y
IC6	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC7	ICD COMP 74S85 4 BIT	28461-671F
IC8	ICD COMP 74S85 4 BIT	28461-671F
IC9	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC10	ICD SH REG 2802 QUAD 256BIT !	28467-507Y
IC11	ICD SH REG 2802 QUAD 256BIT !	28467-507Y

Circuit Ref	Description	Part Number
Board AB5	- Timing & B Display dynamic store (Contd.)	
IC12	ICD SH REG 2802 QUAD 256BIT !	28467-507Y
IC13	ICD SH REG 2802 QUAD 256BIT !	28467-507Y
IC14	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC15	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC16	ICD CTR 74LS161 4BIT BIN PRE	28464-118D
IC17	ICD CTR 74LS161 4BIT BIN PRE	28464-118D
IC18	ICD INV 74LS04 HEX	28469-171L
IC19	ICD AND 74LS08 QUAD 2INP	28466-012L
IC20	ICD NAND 74LS30 8INP	28466-348Y
IC21	ICD NOR 74LS02 QUAD 2INP	28466-214Y
IC22	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC23	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC25	ICD MUX 74F157 QUAD 2INP	28469-722L
IC26	ICD MUX 74LS157 QUAD 2INP	28469-707B
IC27	ICD MUX 74LS157 QUAD 2INP	28469-707B
IC28	ICD MUX 74LS157 QUAD 2INP	28469-707B
IC29	ICD MUX 74LS157 QUAD 2INP	28469-707B
IC30	ICD MUX 74F157 QUAD 2INP	28469-722L
IC31	ICD CTR 74LS161 4BIT BIN PRE	28464-118D
IC32	ICD NAND 74LS30 8INP	28466-348Y
IC33	ICD CTR 74LS161 4BIT BIN PRE	28464-118D
IC34	ICD OR 74LS32 QUAD 2INP	28466-108U
IC35	ICD NAND 74LS00 QUAD 2INP	28466-345H
IC36	ICD CTR 74LS193 4BIT BIN U/D	28464-126C
IC37	ICD CTR 74LS193 4BIT BIN U/D	28464-126C
IC38	ICD CTR 74LS193 4BIT BIN U/D	28464-126C
IC39	ICD OR 74LS32 QUAD 2INP	28466-108U
IC40	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC41	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC42	ICD MONO 74LS221 DUAL	28468-404D
IC43	ICD DRIV DS0026CN DUAL CLOCK	28469-369U
IC44	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC45	ICD DRIV DS0026CN DUAL CLOCK	28469-369U
IC46	ICD INV 74LS04 HEX	28469-171L
IC47	ICD OR 74LS32 QUAD 2INP	28466-108U
IC48	ICD CTR 74S163 4BIT BIN PRE	28464-120W
R1	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R2	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R3	RV CERM 10K LIN .5W 10% HORZ	25711-641G
R4	RV CERM 10K LIN .5W 10% HORZ	25711-641G
R5	RES NET 3K3 5% 9SIP	24681-612T
R6	RES NET 3K3 5% 9SIP	24681-612T
R7	RES NET 4K7 5% 9SIP	24681-611D

Circuit Ref	Description	Part Number
Board AB5	- Timing & B Display dynamic store (Contd.)	
R8	RES NET 4K7 5% 9SIP	24681-611D
R9	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R10	RES CC 22R 1/8W 5%	24331-988T
R11	RES CC 22R 1/8W 5%	24331-988T

Board AB6 - Graticule & A Display dynamic store

15. When ordering, prefix circuit reference with AB6

	Complete unit	44828-508K
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C24	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C25	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C26	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C27	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C28	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C29	CAP CER 10N 50V 20% X7R MON AX	26346-120Y

Circuit Ref	Description	Part Number
Board AB6	- Graticule & A Display dynamic store	(Contd.)
C30	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C31	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C32	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C33	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C34	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C35	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C36	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C37	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C38	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C39	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C40	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C41	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C42	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C43	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C44	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C45	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C46	CAP CER 10P 63V .5PF PLATE	26343-465H
C47	CAP CER 10P 63V .5PF PLATE	26343-465H
C48	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C49	CAP CER 180P 63V 2% PLATE	26343-480V
C50	CAP CER 180P 63V 2% PLATE	26343-480V
C51	CAP PETP 100N 100V 10% RAD	26582-211B
C52	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C53	CAP CER 180P 63V 2% PLATE	26343-480V
C54	CAP CER 180P 63V 2% PLATE	26343-480V
C55	CAP PETP 100N 100V 10% RAD	26582-211B
C56	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C57	CAP CER 180P 63V 2% PLATE	26343-480V
C58	CAP CER 180P 63V 2% PLATE	26343-480V
C59	CAP PETP 100N 100V 10% RAD	26582-211B
C60	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C61	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C62	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C63	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C64	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C65	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C66	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C67	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C68	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C69	CAP CER 68P 63V 2% PLATE	26343-475F
C70	CAP CER 68P 63V 2% PLATE	26343-475F

Circuit Ref	Description		Part Number
Board AB6	- Graticule & A Display dynamic store (Contd.)		
IC1	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC2	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC3	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC4	ICD OR 74F32 QUAD 2INP		28466-111U
IC5	ICD NAND 74LS30 8INP		28466-348Y
IC6	ICD OR 74F32 QUAD 2INP		28466-111U
IC7	ICD DEC/DMX 74LS155 DUAL 2-4		28465-026J
IC8	ICD CTR 74LS93 4BIT BIN 2,8,16		28464-117W
IC9	ICD SH REG 2802 QUAD 256BIT	!	28467-507Y
IC10	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC11	ICD SH REG 2802 QUAD 256BIT	!	28467-507Y
IC12	ICD SH REG 2802 QUAD 256BIT	!	28467-507Y
IC13	ICD SH REG 2802 QUAD 256BIT	!	28467-507Y
IC14	ICD SH REG 2802 QUAD 256BIT	!	28467-507Y
IC15	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC16	ICD AND 74LS21 DUAL 4INP		28466-011N
IC17	ICD NAND 74LS10 TRIP 3INP		28466-351Y
IC18	ICD AND 74LS08 QUAD 2INP		28466-012L
IC19	ICD INV 74LS04 HEX		28469-171L
IC20	ICD DEC/DMX 74LS155 DUAL 2-4		28465-026J
IC21	ICD FF D 74F175 QUAD +EDG TR		28462-114W
IC22	ICD FF D 74LS175 QUAD +EDG TR		28462-614E
IC23	ICD MUX 74LS157 QUAD 2INP		28469-707B
IC25	ICD MUX 74F157 QUAD 2INP		28469-722L
IC26	ICD MUX 74LS157 QUAD 2INP		28469-707B
IC27	ICD MUX 74LS157 QUAD 2INP		28469-707B
IC28	ICD MUX 74LS157 QUAD 2INP		28469-707B
IC29	ICD MUX 74LS157 QUAD 2INP		28469-707B
IC30	ICD MUX 74F157 QUAD 2INP		28469-722L
IC31	ICD INV 74LS04 HEX		28469-171L
IC32	ICD COMP 74S85 4 BIT		28461-671F
IC33	ICD COMP 74S85 4 BIT		28461-671F
IC34	ICD NOR 74LS02 QUAD 2INP		28466-214Y
IC35	ICD MONO 74LS221 DUAL		28468-404D
IC36	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC37	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC38	ICD DRIV DS0026CN DUAL CLOCK		28469-369U
IC39	ICD OR 74F32 QUAD 2INP		28466-111U
IC40	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC41	ICD FF D 74LS273 OCT +EDG TR		28462-615U

Circuit Ref	Description	Part Number
Board AB6	- Graticule & A Display dynamic store (Contd.)	
IC42	ICD DRIV DS0026CN DUAL CLOCK	28469-369U
IC43	ICD DRIV DS0026CN DUAL CLOCK	28469-369U
R1	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R2	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R3	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R4	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R5	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R6	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R7	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R8	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R9	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R10	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R11	RES NET 3K3 5% 9SIP	24681-612T
R12	RES NET 3K3 5% 9SIP	24681-612T
R13	RES NET 4K7 5% 9SIP	24681-611D
R14	RES NET 4K7 5% 9SIP	24681-611D
R15	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R16	RV CERM 10K LIN .5W 10% HORZ	25711-641G
R17	RV CERM 10K LIN .5W 10% HORZ	25711-641G

Circuit Ref	Description	Part Number
Board AB7	- CRT control, Clock & Video mixer	
16.	When ordering, prefix circuit reference with AB7	
	Complete unit	44828-509A
C1	CA P CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C12	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C22	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C23	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C24	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C25	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C27	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C28	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C29	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C30	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C31	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C32	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C33	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C34	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C41	CAP CER 270P 63V 2% PLATE	26343-482W
C42	CAP CER 270P 63V 2% PLATE	26343-482W
C43	CAP VAR PLAS 65P 5P5 TRIM	26878-408Y
C44	CAP CER 47P 63V 5% PLATE	26343-473L

Circuit Ref	Description	Part Number
Board AB7	- CRT control, Clock & Video mixer (Contd.)	
C45	CAP CER 18P 63V 5% PLATE	26343-468Y
C46	CAP CER 100P 63V 2% PLATE	26343-477V
C47	CAP CER 270P 63V 2% PLATE	26343-482W
C48	CAP CER 1N0 63V 10% PLATE	26383-585M
C49	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C50	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C51	CAP CER 1P0 63V .5P PLATE	26343-502Z
C52	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C53	CAP CER 10P 63V .5PF PLATE	26343-465H
C54	CAP CER 10P 63V .5PF PLATE	26343-465H
C55	CAP CER 1P0 63V .5P PLATE	26343-502Z
C56	CAP CER 470P 63V 10% PLATE	26383-582T
C57	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C58	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C59	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C60	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C61	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C62	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C63	CAP CER 47P 63V 5% PLATE	26343-473L
C64	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C65	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C66	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C67	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C68	CAP CER 1N0 63V 10% PLATE	26383-585M
C69	CAP CER 1N8 63V 10% PLATE	26383-586C
C70	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C71	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C72	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C73	CAP CER 82P 63V 2% PLATE	26343-476G
C75	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C76	CAP CER 820P 63V 10% PLATE	26383-584X
C77	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C78	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C79	CAP PETP 22N 63V 10% RAD MIN	26582-431J
C80	CAP CER 33P 63V 5% PLATE	26343-471Y
C81	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C82	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C83	CAP CER 10P 63V .5PF PLATE	26343-465H
C84	CAP CER 270P 63V 2% PLATE	26343-482W
D1	DI SIL 1N4148 75V JUNC	28336-676J
D2	DI SIL 1N4148 75V JUNC	28336-676J
D3	DI SIL 1N4148 75V JUNC	28336-676J

Circuit Ref	Description	Part Number
Board AB7	- CRT Control, Clock & Video mixer (Contd.)	
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI SIL 1N4148 75V JUNC	28336-676J
D8	DI SIL 1N4148 75V JUNC	28336-676J
D9	DI SIL 1N4148 75V JUNC	28336-676J
D10	DI SIL 1N4148 75V JUNC	28336-676J
D11	DI SIL 1N4148 75V JUNC	28336-676J
D12	DI SIL 1N4148 75V JUNC	28336-676J
D13	DI SIL 1N4148 75V JUNC	28336-676J
D14	DI SIL 1N4148 75V JUNC	28336-676J
D15	DI SIL 1N4148 75V JUNC	28336-676J
D16	DI SIL 1N4148 75V JUNC	28336-676J
D17	DI SIL 1N4148 75V JUNC	28336-676J
D19	DI V/CAP BB809 3V 29PF	28381-132G
D20	DI V/CAP BB809 3V 29PF	28381-132G
D21	DI SIL 1N4148 75V JUNC	28336-676J
D22	DI SIL 1N4148 75V JUNC	28336-676J
IC1	ICD CTR 74S196 4BIT DEC	28464-010J
IC2	ICD XOR 74S86 QUAD 2INP	28466-405M
IC3	ICD FF JK 74S112 DUAL -EDG TR	28462-015P
IC4	ICD FF D 74S74 DUAL +EDG TR	28462-607K
IC5	ICD FF D 74S74 DUAL +EDG TR	28462-607K
IC6	ICD NOR 74LS02 QUAD 2INP	28466-214Y
IC7	ICD OR 74LS32 QUAD 2INP	28466-108U
IC8	ICD AND 74LS08 QUAD 2INP	28466-012L
IC9	ICD INV 74LS04 HEX	28469-171L
IC10	ICD INV 74LS14 HEX SCHM	28469-176S
IC11	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC12	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC13	ICD AND 74LS08 QUAD 2INP	28466-012L
IC14	ICD CTR 74LS193 4BIT BIN U/D	28464-126C
IC15	ICM MP SUP 8275 PROG CRT CTLR !	28467-013M
IC16	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC17	ICD AND 74LS11 TRIP 3INP	28466-014F
IC18	ICD OR 74LS32 QUAD 2INP	28466-108U
IC19	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC20	ICD NAND 74S00N QUAD 2INP	28466-331D
IC21	ICD MONO 74LS221 DUAL	28468-404D
IC22	ICD AND 74LS08 QUAD 2INP	28466-012L
IC23	ICD CTR 74LS393 DUAL 4BIT BIN	28464-130R
IC24	ICD CTR 74LS193 4BIT BIN U/D	28464-126C

Circuit Ref	Description	Part Number
Board AB7	- CRT Control, Clock & Video mixer (Contd.)	
IC25	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC26	ICD BUFF 74LS240 OCT 3ST I	28469-187R
IC27	ICM PROM B2716 2KX8 BIT UV (PR) !	44533-120S
IC28	ICD FF D 74LS273 OCT +EDG TR	28462-615U
IC29	ICD MUX 74LS151 8INP	28469-715E
IC30	ICD CTR 74S163 4BIT BIN PRE	28464-120W
IC31	ICD FF JK 74S112 DUAL -EDG TR	28462-015P
IC32	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC33	ICD FF D 74LS74 DUAL +EDG TR	28462-611A
IC34	ICD NAND 74LS10 TRIP 3INP	28466-351Y
IC41	ICA VREG+ 78L12C 12V .1A TO92	28461-732E
IC42	ICA AMP CA3130E GP MOS DIL8 !	28461-361J
L1	IND CHOKE .68UH 10% LAQ	23642-548N
MP4	S/C ACC PAD CBE TO TO5	28488-108E
R1	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R2	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R3	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R4	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R5	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R6	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R8	RES MF 100K 1/4W 2% 100PPM	24773-321L
R9	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R10	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R11	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R12	RES MF 22K 1/4W 2% 100PPM	24773-305R
R13	RES MF 47K 1/4W 2% 100PPM	24773-313H
R14	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R15	RES MF 51K 1/4W 2% 100PPM	24773-314E
R16	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R17	RES MF 470R 1/4W 2% 100PPM	24773-265M
R18	RES MF 300K 1/4W 2% 100PPM	24773-332T
R19	RES MF 47K 1/4W 2% 100PPM	24773-313H
R20	RES MF 270K 1/4W 2% 100PPM	24773-331D
R21	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R22	RES MF 470R 1/4W 2% 100PPM	24773-265M
R23	RES MF 100R 1/4W 2% 100PPM	24773-249J
R24	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R25	RES MF 470R 1/4W 2% 100PPM	24773-265M

(PR) = PROGRAMMED

Circuit Ref	Description	Part Number
Board AB7	- CRT Control, Clock & Video mixer	(Contd.)
R26	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R30	RES MF 470R 1/4W 2% 100PPM	24773-265M
R31	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R32	RES MF 10K 1/4W 2% 100PPM	24773-297M
R33	RES MF 91K 1/4W 2% 100PPM	24773-320N
R34	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R35	RES MF 390R 1/4W 2% 100PPM	24773-263P
R36	RES MF 11K 1/4W 2% 100PPM	24773-298C
R40	RES MF 470R 1/4W 2% 100PPM	24773-265M
R41	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R42	RES MF 10K 1/4W 2% 100PPM	24773-297M
R43	RES MF 91K 1/4W 2% 100PPM	24773-320N
R44	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R45	RES MF 390R 1/4W 2% 100PPM	24773-263P
R46	RES MF 11K 1/4W 2% 100PPM	24773-298C
R50	RES MF 470R 1/4W 2% 100PPM	24773-265M
R51	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R52	RES MF 10K 1/4W 2% 100PPM	24773-297M
R53	RES MF 91K 1/4W 2% 100PPM	24773-320N
R54	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R55	RES MF 390R 1/4W 2% 100PPM	24773-263P
R56	RES MF 11K 1/4W 2% 100PPM	24773-298C
R60	RES MF 470R 1/4W 2% 100PPM	24773-265M
R61	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R62	RES MF 10K 1/4W 2% 100PPM	24773-297M
R63	RES MF 91K 1/4W 2% 100PPM	24773-320N
R64	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R65	RES MF 390R 1/4W 2% 100PPM	24773-263P
R66	RES MF 11K 1/4W 2% 100PPM	24773-298C
R70	RES MF 15K 1/4W 2% 100PPM	24773-301P
R71	RES MF 510R 1/4W 2% 100PPM	24773-266C
R72	RES MF 10K 1/4W 2% 100PPM	24773-297M
R73	RES MF 91K 1/4W 2% 100PPM	24773-320N
R74	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R75	RES MF 390R 1/4W 2% 100PPM	24773-263P
R76	RES MF 11K 1/4W 2% 100PPM	24773-298C
R80	RES MF 470R 1/4W 2% 100PPM	24773-265M
R81	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R82	RES MF 10K 1/4W 2% 100PPM	24773-297M
R83	RES MF 91K 1/4W 2% 100PPM	24773-320N
R84	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R85	RES MF 390R 1/4W 2% 100PPM	24773-263P
R86	RES MF 11K 1/4W 2% 100PPM	24773-298C

Circuit Ref	Description	Part Number
Board AB7	- CRT Control, Clock & Video mixer	(Contd.)
R90	RES MF 360R 1/4W 2% 100PPM	24773-262T
R91	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R92	RES MF 10K 1/4W 2% 100PPM	24773-297M
R93	RES MF 91K 1/4W 2% 100PPM	24773-320N
R94	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R95	RES MF 390R 1/4W 2% 100PPM	24773-263P
R96	RES MF 11K 1/4W 2% 100PPM	24773-298C
R100	RES MF 560R 1/4W 2% 100PPM	24773-267R
R101	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R102	RES MF 10K 1/4W 2% 100PPM	24773-297M
R103	RES MF 91K 1/4W 2% 100PPM	24773-320N
R104	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R105	RES MF 390R 1/4W 2% 100PPM	24773-263P
R106	RES MF 11K 1/4W 2% 100PPM	24773-298C
R110	RES MF 270R 1/4W 2% 100PPM	24773-259T
R111	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R112	RES MF 15K 1/4W 2% 100PPM	24773-301P
R113	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R116	RES MF 11K 1/4W 2% 100PPM	24773-298C
R117	RES MF 75K 1/4W 2% 100PPM	24773-318L
R118	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R119	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R120	RES MF 82R 1/4W 2% 100PPM	24773-247N
TR1	TR NSI 2N2369 15V 500M - SW	28452-197H
TR2	TR NSI 2N2369 15V 500M - SW	28452-197H
TR3	TR NSI 2N2369 15V 500M - SW	28452-197H
TR4	TR NSI 2N2369 15V 500M - SW	28452-197H
TR5	TR NSI 2N2369 15V 500M - SW	28452-197H
TR6	TR NSI 2N2369 15V 500M - SW	28452-197H
TR7	TR NSI 2N2369 15V 500M - SW	28452-197H
TR8	TR NSI 2N2369 15V 500M - SW	28452-197H
TR9	TR PSI BC308B 20V 130M - GEN	28433-455R
TR10	TR NSI 2N2369 15V 500M - SW	28452-197H
TR11	TR PSI MPSL08 12V 700M - SW	28431-767E
TR12	TR NSI 2N2369 15V 500M - SW	28452-197H
TR13	TR NSI BC209C 20V 150M - GEN	28452-771P
TR14	TR NJF BF245B 30V 6MA	28459-048X
TR15	TR NSI BC209C 20V 150M - GEN	28452-771P
TR16	TR NSI BC209C 20V 150M - GEN	28452-771P
X1	S/C ACC SKT DIL24 LOW PROFILE	28488-044N
X2	S/C ACC PAD TO18,ETC TO .1"GRD	28488-115L
X4	CON JUMP FEM 2 1 ROW	23435-990X

Circuit Ref	Description	Part Number
Board AB8	- Pen Plot and RGB Video	
17.	When ordering, prefix circuit reference with AB8	
	Complete unit	44828-510B
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C6	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C7	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C8	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C9	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C10	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C11	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C13	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C14	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C15	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C16	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C17	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C18	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C19	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C20	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C21	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C22	CAP CER 4N7 63V 10% PLATE	26383-591B
C23	CAP CER 4N7 63V 10% PLATE	26383-591B
C31	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C32	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C40	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C41	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C42	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C43	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C44	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C45	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C46	CAP ELEC 33U 25V 20% SUBMIN	26421-115U
C50	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C51	CAP ELEC 10U 35V 20% SUBMIN	26421-112Z
C52	CAP PS 8N2 63V 1% RAD	26538-924E
C53	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C54	CAP CER 10P 63V .5PF PLATE	26343-465H
C55	CAP CER 10P 63V .5PF PLATE	26343-465H

Circuit Ref	Description		Part Number
Board AB8	- Pen Plot and RGB Video		(Contd.)
C56	CAP ELEC 470U 6V 20%+ PCB		26421-126S
C57	CAP CER 150P 63V 2% PLATE		26343-432Z
D1	DI SIL 1N4148 75V JUNC		28336-676J
D2	DI ZEN BZX79C4V7 4.7V 5%		28371-371F
IC1	ICD NAND 74LS00 QUAD 2INP		28466-345H
IC2	ICD INV 74LS04 HEX		28469-171L
IC3	ICA VREF ZN404 2V45 TO18		28461-922T
IC4	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC5	ICA DAC AD7522LN 10BIT MOS	!	28469-402K
IC6	ICA DAC AD7522LN 10BIT MOS	!	28469-402K
IC7	ICD DEC/DMX 74LS138 3-8		28465-027F
IC8	ICD XOR 74LS86 QUAD 2INP		28466-406C
IC9	ICA AMP TL072CP DUAL FET I/P		28461-348Z
IC10	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC11	ICD MONO 556 DUAL TIMER		28468-312B
IC13	ICD NOR 74LS27 TRIP 3INP		28466-216L
IC14	ICD FF D 74LS74 DUAL +EDG TR		28462-611A
IC15	ICD FF D 74LS273 OCT +EDG TR		28462-615U
IC16	ICD FF D 74LS374 OCT +E TR 3ST		28462-618L
IC17	ICD BUFF 74LS244 OCT 3ST		28469-182T
IC18	ICD AND 74LS08 QUAD 2INP		28466-012L
IC19	ICD OR 74LS32 QUAD 2INP		28466-108U
IC20	ICD DEC/DMX 74LS138 3-8		28465-027F
R1	RES MF 1K2 1/4W 2% 100PPM		24773-275H
R2	RES MF 750R 1/4W 2% 100PPM		24773-270R
R3	RES MF 1K8 1/4W 2% 100PPM		24773-279N
R4	RES MF 750R 1/4W 2% 100PPM		24773-270R
R5	RES MF 1K8 1/4W 2% 100PPM		24773-279N
R6	RES MF 750R 1/4W 2% 100PPM		24773-270R
R7	RES MF 1K8 1/4W 2% 100PPM		24773-279N
R8	RES MF 1K0 1/4W 2% 100PPM		24773-273A
R9	RES MF 15K 1/4W 2% 100PPM		24773-301P
R10	RES MF 2K7 1/4W 2% 100PPM		24773-283L
R11	RES MF 5K6 1/4W 2% 100PPM		24773-291S
R12	RES MF 5K6 1/4W 2% 100PPM		24773-291S
R13	RES MF 1K1 1/4W 2% 100PPM		24773-274Z
R14	RES MF 2K4 1/4W 2% 100PPM		24773-282N
R15	RES MF 470R 1/4W 2% 100PPM		24773-265M

Circuit Ref	Description	Part Number
Board AB8	- Pen Plot and RGB Video	(Contd.)
R16	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R17	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R18	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R19	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R20	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R21	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R22	RES MF 470R 1/4W 2% 100PPM	24773-265M
R23	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R24	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R25	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R26	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R27	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R28	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R29	RES MF 470R 1/4W 2% 100PPM	24773-265M
R30	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R31	RES MF 910R 1/4W 2% 100PPM	24773-272K
R32	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R33	RES MF 1M0 1/4W 2% 100PPM	24773-346E
R34	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R35	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R40	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R41	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R42	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R43	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R44	RES MO 470R 1/2W 2% 250PPM	24573-065J
R45	RES MO 470R 1/2W 2% 250PPM	24573-065J
R46	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R47	RES MF 16K 1/4W 2% 100PPM	24773-302X
R48	RES MF 51K 1/4W 2% 100PPM	24773-314E
R49	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R51	RES MF 22K 1/4W 2% 100PPM	24773-305R
R52	RES MF 10K 1/4W 2% 100PPM	24773-297M
R53	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R54	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R55	RES MF 200K 1/4W 2% 100PPM	24773-328D

Circuit Ref	Description	Part Number
Board AB8	- Pen Plot and RGB Video	(Contd.)
R56	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R57	RES MF 24K 1/4W 2% 100PPM	24773-306B
R60	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R61	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R62	RES MF 680R 1/4W 2% 100PPM	24773-269K
R63	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R64	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R65	RES MF 130R 1/4W 2% 100PPM	24773-252J
R66	RES MF 180R 1/4W 2% 100PPM	24773-255V
R67	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R68	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R69	RES MF 3K3 1/4W 2% 100PPM	24773-285F
R70	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R71	RES MO 220R 1/2W 2% 250PPM	24573-057E
R72	RES MF 75R 1/4W 2% 100PPM	24773-246Y
R73	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R74	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R75	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R76	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R77	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R78	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R79	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R80	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R81	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R82	RES MF 10K 1/4W 2% 100PPM	24773-297M
R83	RES MF 10K 1/4W 2% 100PPM	24773-297M
R84	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R85	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R86	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R87	RES MF 360R 1/4W 2% 100PPM	24773-262T
R88	RES MF 75R 1/4W 2% 100PPM	24773-246Y
R89	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R90	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R91	RES MF 360R 1/4W 2% 100PPM	24773-262T
R92	RES MF 75R 1/4W 2% 100PPM	24773-246Y
R93	RES MF 2K4 1/4W 2% 100PPM	24773-282N
R94	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R95	RES MF 360R 1/4W 2% 100PPM	24773-262T
R96	RES MF 75R 1/4W 2% 100PPM	24773-246Y
RLA	RELAY REED 1NO 5V 380R DIL	23486-501Z
TR1	TR PSI BC308B 20V 130M - GEN	28433-455R
TR2	TR PSI BC308B 20V 130M - GEN	28433-455R
TR3	TR PSI BC308B 20V 130M - GEN	28433-455R

Circuit Ref	Description	Part Number
Board AB8	- Pen Plot and RGB Video (Contd.)	
TR4	TR NSI BC108A&B 20V 150M - GEN	28452-787N
TR5	TR NSI 2N2369 15V 500M - SW	28452-197H
TR6	TR NSI BC108A&B 20V 150M - GEN	28452-787N
TR7	TR NSI BC108A&B 20V 150M - GEN	28452-787N
TR8	TR NSI BC108A&B 20V 150M - GEN	28452-787N
TR9	TR PSI BC308B 20V 130M - GEN	28433-455R
TR10	TR PSI BC308B 20V 130M - GEN	28433-455R
TR11	TR PSI BC308B 20V 130M - GEN	28433-455R
TR12	TR PSI BC308B 20V 130M - GEN	28433-455R
TR13	TR PSI BC308B 20V 130M - GEN	28433-455R
TR14	TR PSI BC308B 20V 130M - GEN	28433-455R
X1	BUZZER 50V MAX 10MA 4KHZ PCB	23646-151J

Circuit Ref	Description	Part Number
Board AC0/1	- Power supply (chassis)	
18.	When ordering, prefix circuit reference with AC0/1	
	Complete unit	44990-540K
C1	CAP CER 1N0 500V 20%+ L/T SCR	26373-714F
C2	CAP CER 1N0 500V 20%+ L/T SCR	26373-714F
FS1	#FUSE T/LAG 2.5A 20X5	23411-061C
FS2	#FUSE T/LAG 2.5A 20X5	23411-061C
MP119	CON PART D SCREWLOCK FEM	23435-981V
MP126	FAN ACC FILTER FOR 23535-123	23535-110L
PLA	CON PWR MALE 3 FXD CEE22 BLK	23423-159P
S1	SW ROTARY 2P2W 4A MAINS	23462-353A
S2	COVER SWITCH	37590-246W
X1	CABLE ASSY. AC1/1 - AC2/1	43130-332L
X6	INPUT & CTRL PCB AC1/1	44829-296L
X7	OUTPUT & MON PCB AC2/1	44829-297J
X8	LINE FILTER PCB AC3/1 2380	44828-512A
X106	H/W FUSE HOLDER PANEL 20X5	23416-192R
X116	CON PART MIN HOUSING 1ROW 3P	23435-171R
X117	CON PART MIN SKT 22-26AWG REEL	23435-178U
X127	FAN AX 24V DC BRUSHLESS 119MM	23535-123X

FUSE T/LAG 4A 20 x 5 is used for 110 V a.c. supply.
Refer to the Operating manual under Installation.

Circuit Ref	Description	Part Number
Board AC1/1	- Power supply (input & ctrl)	
19.	When ordering, prefix circuit reference with AC1/1	
	Complete unit	44829-296L
C1	CAP PAPER 2N2 250VAC 20% Y RAT	26144-201H
C2	CAP ELEC 470U 250V -10+30% PCB	26422-306U
C3	CAP ELEC 470U 250V -10+30% PCB	26422-306U
C4	CAP ELEC 470U 250V -10+30% PCB	26422-306U
C5	CAP ELEC 470U 250V -10+30% PCB	26422-306U
C6	CAP PETP 220N 100V 10% RAD	26582-226G
C7	CAP PP 470PF 630V 10%	26582-491U
C8	CAP PP 470PF 630V 10%	26582-491U
C9	CAP PETP 2U2 250V 20% AX 4AMPS	26582-433G
C10	CAP PAPER 2N2 250VAC 20% Y RAT	26144-201H
C11	CAP ELEC 1000U 35V 20%+ PCB	26421-130W
C12	CAP PETP 1U0 50V 10% RAD MIN	26582-432F
C13	CAP PETP 1U0 50V 10% RAD MIN	26582-432F
C14	CAP PAPER 2N2 250VAC 20% Y RAT	26144-201H
C15	CAP ELEC 22U 25V 20% SUBMIN	26421-114E
C16	CAP PETP 220N 63V 10% RAD MIN	26582-430L
C17	CAP ELEC 4U7 50V 20% L/LEAK	26421-011H
C18	CAP PS 1N2 63V 1% RAD	26538-904S
C19	CAP PS 4N7 63V 1% RAD	26538-918A
C20	CAP PAPER 2N2 250VAC 20% Y RAT	26144-201H
C21	CAP PS 4N7 63V 1% RAD	26538-918A
C22	CAP CER 150P 63V 2% PLATE	26343-479W
D1	DI RECT 1N4004 400V	28357-028K
D2	DI BRIDGE KBPC608 800V 6A	28359-199B
D3	DI S/OFF 1.5KE220A 185V	28383-989G
D4	DI S/OFF 1.5KE220A 185V	28383-989G
D5	DI SIL 1N4148 75V JUNC	28336-676J
D6	DI SIL 1N4148 75V JUNC	28336-676J
D7	DI BRIDGE 2KBB20R 200V 1.9A	28359-189D
D11	DI SIL 1N4148 75V JUNC	28336-676J
D12	DI SIL 1N4148 75V JUNC	28336-676J
D13	DI SIL 1N4148 75V JUNC	28336-676J
FS1	FUSE Q/ACT 3.15A 20X5	23411-008L
FS2	FUSE Q/ACT 3.15A 20X5	23411-008L
IC1	ICA VREG+ 7812 12V 1A TO220	28461-708V
IC2	ICA VREG SG3526J SMPS CTLR DIL	28461-731H

Circuit Ref	Description	Part Number
Board AC1/1	- Power supply (input & ctrl)	(Contd.)
LP1	LAMP NEON WIRES 90V NO LENS	23733-103R
MP1	S/C ACC H/SINK TO3 8.5K/W	28488-455N
MP2	S/C ACC WASHER TO3 INS 0.3K/W	28488-135B
MP3	S/C ACC H/SINK TO220 17K/W	28488-465W
MP4	S/C ACC WASHER TO220 IN 1.3K/W	28488-136K
MP5	S/C ACC BUSH 6BA/M3 INSUL	28488-126T
MP6	S/C ACC WASHER TO126 INS 3K/W	28488-144U
PLB	CON PCB MALE 6/0.2 STR TIN	23435-917D
R1	RES WW 100R 3W 5%	25125-048Y
R4	RES MO 56KO 2W 5% 200PPM	24587-269E
R5	RES MO 56KO 2W 5% 200PPM	24587-269E
R6	RES MG 10M 1/4W 5%	24321-885W
R7	RES MF 100R 1/4W 2% 100PPM	24773-249J
R8	RES MF 11R 1/4W 2% 100PPM	24773-226D
R9	RES MF 100R 1/4W 2% 100PPM	24773-249J
R10	RES MF 11R 1/4W 2% 100PPM	24773-226D
R11	RES WW 150R 1.5W 5%	25123-054V
R12	RES WW 150R 1.5W 5%	25123-054V
R13	RES MF 27R 1/4W 2% 100PPM	24773-235R
R14	RES MF 10K 1/4W 2% 100PPM	24773-297M
R15	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R16	RES MF 6K8 1/4W 2% 100PPM	24773-293D
R17	RES MF 100R 1/4W 2% 100PPM	24773-249J
R18	RES MF 91R 1/4W 2% 100PPM	24773-248L
R19	RV CERM 100R LIN .5W 10% HORZ	25711-635L
R20	RES MF 820R 1/4W 2% 100PPM	24773-271B
R21	RES MF 100K 1/4W 2% 100PPM	24773-321L
R22	RES MF 10K 1/4W 2% 100PPM	24773-297M
R23	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R25	RES MF 10K 1/4W 2% 100PPM	24773-297M
R26	RES MF 220R 1/4W 2% 100PPM	24773-257W
R27	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R28	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R29	RES MO 1KO 1/2W 2% 250PPM	24573-073W
R30	RES MF 10K 1/4W 2% 100PPM	24773-297M
R31	RES MF 1KO 1/4W 2% 100PPM	24773-273A

Circuit Ref	Description		Part Number
Board AC1/1	- Power supply (input & ctrl)		(Contd.)
RLA	RELAY MAG 2NO 5V 110R HI ISOL		23486-158Y
SA	SW SLIDE 2CO 250V 5A RA PCB		23467-152L
TR1	TR NMF IRF443 450V 1R1 7A PWR	!	28459-042V
TR2	TR NMF IRF443 450V 1R1 7A PWR	!	28459-042V
TR3	TR PSI BD676 45V 60K - 40W DAR		28435-239V
TR4	TR NSI BC209C 20V 150M - GEN		28452-771P
TR5	TR NSI BC209C 20V 150M - GEN		28452-771P
T1	TRANSFORMER MAINS 15V 12VA		43490-081Y
T2	TRANSFORMER 1:1:1 H.F. DRIVER		43590-155P
T3	TRANSFORMER 1:200:200 I-SENSE		43590-133A
X2	S/C ACC SKT DIL18 LOW PROFILE		28488-042U
X3	CON JUMP FEM 2 1 ROW		23435-990X
X4	H/W FUSE CARRIER OPEN 20X5		23416-151D
X5	CORE BEAD 5X.7X10LG 3S2		23635-811Z
X6	CORE BEAD 5X.7X10LG 3S2		23635-811Z

Circuit Ref	Description	Part Number
Board AC2/1	- Power supply (output & monitor)	
20.	When ordering, prefix circuit reference with AC2/1	
	Complete unit	44829-297J
C1	CAP ELEC 10000U 10V 10%+ PCB	26422-326M
C2	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C3	CAP ELEC 1000U 35V 20%+ PCB	26421-130W
C4	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C5	CAP ELEC 1000U 35V 20%+ PCB	26421-130W
C6	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C7	CAP ELEC 1000U 35V 20%+ PCB	26421-130W
C8	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C9	CAP ELEC 1000U 35V 20%+ PCB	26421-130W
C10	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C11	CAP ELEC 1000U 35V 20%+ PCB	26421-130W
C12	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C13	CAP ELEC 33U 250V -10+50% PCB	26421-134X
C14	CAP CER 220P 400V 20% DISC	26383-134W
C15	CAP CER 220P 400V 20% DISC	26383-134W
C16	CAP CER 220P 400V 20% DISC	26383-134W
C17	CAP CER 220P 400V 20% DISC	26383-134W
C18	CAP PETP 10N 63V 10% RAD MIN	26582-426N
C19	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C20	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C21	CAP ELEC 1000U 35V 20%+ PCB	26421-130W
C22	CAP ELEC 1U0 50V 20% L/LEAK	26421-007Z
C23	CAP CER 4N7 63V 10% PLATE	26383-591B
C24	CAP ELEC 47U 16V 20% L/LEAK	26421-017J
C25	CAP CER 4N7 63V 10% PLATE	26383-591B
C26	CAP ELEC 47U 16V 20% L/LEAK	26421-017J
C27	CAP CER 4N7 63V 10% PLATE	26383-591B
C28	CAP CER 4N7 63V 10% PLATE	26383-591B
C29	CAP ELEC 10U 50V 20% L/LEAK	26421-013U
C30	CAP ELEC 10U 50V 20% L/LEAK	26421-013U
C31	CAP PETP 100N 100V 10% RAD	26582-211B
C32	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C33	CAP CER 100P 63V 2% PLATE	26343-477V
C34	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C35	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C36	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C37	CAP PETP 100N 63V 10% RAD MIN	26582-429F

Circuit Ref	Description	Part Number
Board AC2/1	- Power supply (output & monitor	(Contd.)
C38	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C39	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C40	CAP CER 1N0 63V 10% PLATE	26383-585M
D1	DI RECT 20CTQ45 45V DUA SCH !	28355-165H
D2	DI S/OFF ICT5 5V SUPP	28383-994S
D3	DI RECT BA159 1000V	28359-103B
D4	DI RECT BA159 1000V	28359-103B
D5	DI RECT BYV28-100 100V FAST	28356-019N
D6	DI RECT BYV28-100 100V FAST	28356-019N
D7	DI RECT BYV32-100 100V DUAL16A	28383-907B
D8	DI RECT 1N4004 400V	28357-028K
D9	DI RECT BYV28-100 100V FAST	28356-019N
D10	DI RECT BYV28-100 100V FAST	28356-019N
D11	DI RECT BYV28-100 100V FAST	28356-019N
D12	DI RECT BYV28-100 100V FAST	28356-019N
D13	DI RECT BYV28-100 100V FAST	28356-019N
D14	DI RECT BYV28-100 100V FAST	28356-019N
D15	DI SIL 1N4148 75V JUNC	28336-676J
D16	DI ZEN BZX79C24 24V 5%	28373-270L
D17	DI RECT 1N4004 400V	28357-028K
D18	DI SIL 1N4148 75V JUNC	28336-676J
D19	DI SIL 1N4148 75V JUNC	28336-676J
D20	DI SIL 1N4148 75V JUNC	28336-676J
D21	DI SIL 1N4148 75V JUNC	28336-676J
D22	DI ZEN BZX79C18 18V 5%	28372-584H
D23	LAMP LED HLMP-3400 3V YELLOW	28624-114R
D24	LAMP LED HLMP-3400 3V YELLOW	28624-114R
D25	LAMP LED HLMP-3400 3V YELLOW	28624-114R
D26	LAMP LED HLMP-3400 3V YELLOW	28624-114R
D27	DI RECT 1N4004 400V	28357-028K
D28	DI RECT 1N5401 100V	28355-723N
D29	DI RECT 1N5401 100V	28355-723N
IC1	ICA VREG- 7905 5V 1A TO220	28461-717X
IC2	ICA COMP LM339N QUAD	28461-693H
IC3	ICD MONO 556 DUAL TIMER	28468-312B
IC4	ICD LATCH 74LS279 QUAD RS	28462-107F
IC5	ICD BUFF 7407 HEX O/C	28469-703X
IC6	ICD INV 74LS14 HEX SCHM	28469-176S
IC7	ICD CTR 74LS393 DUAL 4BIT BIN	28464-130R
IC8	ICA VREG- 7912 12V 1A TO220	28461-718M
L1	IND CHOKE 36UH	44290-924Z
L2	IND CHOKE 350UH	44190-040K

Circuit Ref	Description	Part Number
Board AC2/1	- Power supply (output & monitor)	(Contd.)
L3	IND CHOKE 350UH	44190-040K
L4	IND CHOKE 350UH	44190-040K
L5	IND CHOKE 350UH	44190-040K
L6	IND CHOKE 350UH	44190-040K
L7	IND CHOKE 1.5MH	44190-041A
MP1	S/C ACC H/SINK TO220 10.5K/W	28488-461F
MP2	S/C ACC WASHER TO220 IN 1.3K/W	28488-136K
MP4	S/C ACC H/SINK TO220 17K/W	28488-465W
MP22	LED HOLDER	37590-727W
MP23	INS BEAD 18SWG BUSH CER	23213-146D
PLC	CON PCB MALE 6/0.2 STR TIN	23435-917D
R1	RES MF 100R 1/4W 0.5% 50PPM	24753-431G
R2	RES MF 100R 1/4W 0.5% 50PPM	24753-431G
R3	RES MO 100R 1/2W 2% 250PPM	24573-049B
R4	RES MO 10K 1/2W 2% 250PPM	24573-097J
R5	RES MO 220R 1/2W 2% 250PPM	24573-057E
R6	RES MO 1K8 1/2W 2% 250PPM	24573-079C
R7	RES MO 1K8 1/2W 2% 250PPM	24573-079C
R8	RES MO 100R 1/2W 2% 250PPM	24573-049B
R9	RES MO 1K2 1/2W 2% 250PPM	24573-075T
R10	RES MO 1K2 1/2W 2% 250PPM	24573-075T
R11	RES MO 10R 1/2W 2% 250PPM	24573-025E
R12	RES MO 820R 1/2W 2% 250PPM	24573-071V
R13	RES MO 10R 1/2W 2% 250PPM	24573-025E
R14	RES WW 47R 3W 5%	25125-037R
R15	RV THERM 300K NTC 0.014W 10%	25685-520D
R16	RES MF 120K 1/4W 2% 100PPM	24773-323F
R17	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R18	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R19	RES MF 680R 1/4W 2% 100PPM	24773-269K
R20	RES MF 100K 1/4W 2% 100PPM	24773-321L
R21	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R22	RES MF 270R 1/4W 2% 100PPM	24773-259T
R23	RES MF 1K5 1/4W 2% 100PPM	24773-277U
R24	RES MF 100K 1/4W 2% 100PPM	24773-321L
R25	RES MF 1K0 1/4W 2% 100PPM	24773-273A
R26	RES MF 10K 1/4W 2% 100PPM	24773-297M
R27	RES MF 10K 1/4W 2% 100PPM	24773-297M
R28	RES MF 18K 1/4W 2% 100PPM	24773-303M
R29	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R30	RES MF 2K2 1/4W 2% 100PPM	24773-281Y

Circuit Ref	Description	Part Number
Board AC2/1	- Power supply (output & monitor)	(Contd.)
R31	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R32	RES MF 100R 1/4W 2% 100PPM	24773-249J
R33	RES MF 8K2 1/4W 2% 100PPM	24773-295P
R34	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R47	RES MO 5R6 1/2W 5% 250PPM	24552-014N
R48	RES MF 10R 1/4W 2% 100PPM	24773-225W
R49	RES MF 22K 1/4W 2% 100PPM	24773-305R
R50	RES MF 10K 1/4W 2% 100PPM	24773-297M
R51	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R52	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R53	RES MF 2KO 1/4W 2% 100PPM	24773-280U
R54	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R55	RES MF 100K 1/4W 2% 100PPM	24773-321L
R56	RES MF 510R 1/4W 2% 100PPM	24773-266C
R57	RES MF 220R 1/4W 2% 100PPM	24773-257W
R58	RES MF 1K3 1/4W 2% 100PPM	24773-276E
R59	RES MF 1K2 1/4W 2% 100PPM	24773-275H
R60	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R61	RES MF 100K 1/4W 2% 100PPM	24773-321L
R62	RES MF 10K 1/4W 2% 100PPM	24773-297M
R63	RES MF 220R 1/4W 2% 100PPM	24773-257W
R64	RES MF 220R 1/4W 2% 100PPM	24773-257W
R65	RES MF 220R 1/4W 2% 100PPM	24773-257W
R66	RES MF 220R 1/4W 2% 100PPM	24773-257W
SKA	CON D FEM 37 FXD PCB RT ANG	23435-505W
TR1	TR NSI TIP112 100V 5M DAR	28457-822L
TR2	TR PSI BC307A 45V 130M - GEN	28435-227H
TR3	TR NSI TIP112 100V 5M DAR	28457-822L
TR4	TR NSI BC449 100V 250M	28457-821N
TR5	TR NSI BC209C 20V 150M - GEN	28452-771P
TR6	TR NSI BC209C 20V 150M - GEN	28452-771P
T1	TRANSFORMER POWER H.F. SMPS	43590-153D
X2	CON JUMP FEM 2 1 ROW	23435-990X

Circuit Ref	Description	Part Number
Board AC3/1	- Line filter	
21. When ordering, prefix circuit reference with AC3/1		
	Complete unit	44828-512A
C1	CAP PETP 470N 250VAC 20% XRAT	26582-237M
C2	CAP PETP 470N 250VAC 20% XRAT	26582-237M
C3	CAP PETP 470N 250VAC 20% XRAT	26582-237M
L1	IND CHOKE 350UH	44190-040K
L2	IND CHOKE 350UH	44190-040K
T1	TRANSFORMER SUPR 1:1 13mH X 2	43590-154T
Board AD1/1	- Display (drive board)	
22. When ordering, prefix circuit reference with AD1/1		
	Complete unit	44828-519L
C1	CAP ELEC 2U2 50V 20% L/LEAK	26421-009E
C3	CAP PETP 1U0 50V 10% RAD MIN	26582-432F
C5	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C6	CAP CER 680P 63V 10% PLATE	26383-583P
C7	CAP PETP 470N 100V 10% RAD	26582-215H
C8	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C9	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C10	CAP PETP 470N 63V 10% RAD MIN	26582-427L
C11	CAP ELEC 4U7 50V 20% L/LEAK	26421-011H
C12	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C13	CAP PC 22N 630V 10% RAD	26531-114V
C14	CAP PETP 100N 250V 10% RAD	26582-208B
C15	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C16	CAP ELEC 100U 35V 20%+ PCB	26421-122J
C17	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C18	CAP ELEC 470U 16V 20%+ PCB	26421-127W
C19	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C20	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C21	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C22	CAP CER 100P 63V 2% PLATE	26343-477V
C23	CAP CER 4N7 63V 10% PLATE	26383-591B
C24	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C25	CAP ELEC 2200U 16V 20%+ PCB	26421-132T
C26	CAP ELEC 10U 50V 20% L/LEAK	26421-013U
C27	CAP PETP 2U2 100V 10% RAD	26582-220U

Circuit Ref	Description	Part Number
Board AD1/1	- Display (drive board)	(Contd.)
C28	CAP CER 470P 63V 10% PLATE	26383-582T
C29	CAP PETP 100N 63V 10% RAD MIN	26582-429F
C30	CAP PS 1N0 63V 1% RAD	26538-902G
C31	CAP CER 4N7 63V 10% PLATE	26383-591B
C32	CAP CER 1N0 63V 10% PLATE	26383-585M
C33	CAP PS 1N0 63V 1% RAD	26538-902G
C34	CAP CER 4N7 63V 10% PLATE	26383-591B
C35	CAP PETP 150N 63V 10% RAD MIN	26582-437D
C36	CAP ELEC 100U 35V 20%+ PCB	26421-122J
C37	CAP ELEC 220U 16V 20%+ PCB	26421-124G
C38	CAP PP 15N 630V 10% 2.5KV/US	26582-492Y
C39	CAP PC 22N 630V 10% RAD	26531-114V
C40	CAP ELEC 220U 100V -10+50% PCB	26421-137R
C41	CAP PETP 100N 250V 10% RAD	26582-208B
C42	CAP CER 1N0 500V 20% DISC	26383-242P
C43	CAP CER 1N0 500V 20% DISC	26383-242P
D1	DI RECT 1N4004 400V	28357-028K
D2	DI ZEN BZX79C13 13V 5%	28372-218F
D3	DI RECT 1N4004 400V	28357-028K
D4	DI SIL 1N4148 75V JUNC	28336-676J
D5	DI ZEN BZX79C3V9 3.9V 5%	28371-242D
D6	DI RECT MR854 400V 3A	28357-016W
D7	DI RECT BA159 1000V	28359-103B
D8	DI RECT BA159 1000V	28359-103B
D9	DI RECT BA159 1000V	28359-103B
IC1	ICA VREG+ LM317T ADJ 1.5A	28461-726A
IC2	MOD CRT SUP TDA1170S FLD DRIVE	28231-408A
IC3	ICD MONO 555 TIMER	28468-304P
IC4	ICD MONO 555 TIMER	28468-304P
L1	IND VAR 50-125UH 20%	44290-930U
MP1	S/C ACC H/SINK TO220 10.5K/W	28488-461F
MP2	S/C ACC WASHER TO220 IN 1.3K/W	28488-136K
MP3	S/C ACC H/SINK TO5 50K/W	28488-448H
MP4	S/C ACC PAD TO5,ETC TO 0.1"GRD	28488-113Y
MP10	S/C ACC PAD TO18,ETC TO .1"GRD	28488-115L

Circuit Ref	Description	Part Number
Board AD1/1	- Display (drive board)	(Contd.)
R1	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R2	RES MF 130R 1/4W 2% 100PPM	24773-252J
R3	RES MF 1K1 1/4W 2% 100PPM	24773-274Z
R4	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R5	RES MF 820R 1/4W 2% 100PPM	24773-271B
R6	RES MF 1MO 1/4W 2% 100PPM	24773-346E
R7	RES MF 10K 1/4W 2% 100PPM	24773-297M
R8	RES MF 100K 1/4W 2% 100PPM	24773-321L
R9	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R10	RES MF 68R 1/4W 2% 100PPM	24773-245U
R11	RES MF 470R 1/4W 2% 100PPM	24773-265M
R12	RES MF 1KO 1/4W 2% 100PPM	24773-273A
R13	RES MO 3K3 1W 5% 250PPM	24585-138F
R14	RES MF 150R 1/4W 2% 100PPM	24773-253F
R15	RES MF 100R 1/4W 2% 100PPM	24773-249J
R16	RES MF 680R 1/4W 2% 100PPM	24773-269K
R17	RV CERM 1KO LIN .5W 10% VERT	25711-602N
R18	RES MO 120R 1/2W 2% 250PPM	24573-051R
R19	RV CERM 200K LIN .5W 10% VERT	25711-614T
R20	RES MF 330K 1/4W 2% 100PPM	24773-333P
R21	RES MF 15R 1/4W 2% 100PPM	24773-229X
R22	RES MF 10R 1/4W 2% 100PPM	24773-225W
R23	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R24	RES MF 270K 1/4W 2% 100PPM	24773-331D
R25	RES MF 39K 1/4W 2% 100PPM	24773-311A
R26	RES MF 47K 1/4W 2% 100PPM	24773-313H
R27	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R28	RES MF 4K7 1/4W 2% 100PPM	24773-289W
R29	RES MF 10K 1/4W 2% 100PPM	24773-297M
R30	RES MF 39K 1/4W 2% 100PPM	24773-311A
R31	RES MO 680K 1/2W 2% 250PPM	24573-141V
R32	RES MO 220K 1W 5% 250PPM	24585-181D
R34	RES MO 680K 1/2W 2% 250PPM	24573-141V
R35	RES MF 2K7 1/4W 2% 100PPM	24773-283L
R36	RES MF 390K 1/4W 2% 100PPM	24773-335M
*R37	RES MF 560K 1/4W 2% 100PPM	24773-340R
R38	RES MF 470K 1/4W 2% 100PPM	24773-337R
R39	RV CARB 1MO LIN .25W 20% 500V	25611-193U
R40	RES MG 2M2 1/4W 5%	24321-877J
R41	RES MF 2K2 1/4W 2% 100PPM	24773-281Y

Circuit Ref	Description	Part Number
Board AD1/1	- Display (drive board)	(Contd.)
R42	RES MF 10K 1/4W 2% 100PPM	24773-297M
*R43	RES MF 300K 1/4W 2% 100PPM	24773-332T
R44	RES MF 390K 1/4W 2% 100PPM	24773-335M
R45	RV CERM 200K LIN .5W 10% VERT	25711-614T
R46	RES MF 820K 1/4W 2% 100PPM	24773-344Z
R47	RES MF 47K 1/4W 2% 100PPM	24773-313H
R48	RES MF 220K 1/4W 2% 100PPM	24773-329T
R49	RES MF 3R3 1/4W 2% 100PPM	24773-213U
R50	RES MF 18K 1/4W 2% 100PPM	24773-303M
R51	RES MF 68K 1/4W 2% 100PPM	24773-317N
R52	RES MF 680K 1/4W 2% 100PPM	24773-342K
R53	RV CERM 50K0 LIN .5W 10% VERT	25711-612W
R54	RES MF 56K 1/4W 2% 100PPM	24773-315U
R55	RES MF 0R33 0.4W 5% 300PPM	24783-001A
R56	RES MF 2K2 1/4W 2% 100PPM	24773-281Y
R57	RES MF 10K 1/4W 2% 100PPM	24773-297M
R58	RES MF 10K 1/4W 2% 100PPM	24773-297M
R59	RES MF 10K 1/4W 2% 100PPM	24773-297M
R60	RES MF 100R 1/4W 2% 100PPM	24773-249J
R61	RV CERM 20K0 LIN .5W 10% VERT	25711-611S
R62	RES MF 33K 1/4W 2% 100PPM	24773-309Z
R63	RES MF 5K6 1/4W 2% 100PPM	24773-291S
R64	RES MF 560R 1/4W 2% 100PPM	24773-267R
R65	RES MF 6K2 1/4W 2% 100PPM	24773-292W
R66	RES MF 30K8 1/4W 0.5% 50PPM	24753-580C
R67	RES MO 47R 1/2W 2% 250PPM	24573-041W
R68	RES MO 150R 1/2W 2% 250PPM	24573-053K
R69	RES MF 220R 1/4W 2% 100PPM	24773-257W
R70	RES MF 10R 1/4W 2% 100PPM	24773-225W
R71	RES MF 220R 1/4W 2% 100PPM	24773-257W
R72	RES MF 47K 1/4W 2% 100PPM	24773-313H
R73	RES MF 390R 1/4W 2% 100PPM	24773-263P
R74	RES MF 270R 1/4W 2% 100PPM	24773-259T
TR1	TR NSI BC208B 20V 150M - GEN	28452-781A
TR2	TR NSI 2N2369 15V 500M - SW	28452-197H
TR3	TR PSI BC308B 20V 130M - GEN	28433-455R
TR4	TR NSI BF338 225V 80M - 7W	28458-577X
TR5	TR NSI 2N2369 15V 500M - SW	28452-197H

Circuit Ref	Description	Part Number
Board AD1/1	- Display (drive board)	(Contd.)
TR6	TR NSI BC208B 20V 150M - GEN	28452-781A
TR7	TR NSI MJE340 300V - - 21W	28458-646P
TR8	TR NSI MJE340 300V - - 21W	28458-646P
TR9	TR NSI BC208B 20V 150M - GEN	28452-781A
TR10	TR PSI BC308B 20V 130M - GEN	28433-455R
TR11	TR NSI BU806 400V - - DAR PWR	28458-690K
T1	MOD CRT SUP 10.7005.0300 XFMR	28231-410K
Board AF1	- Keyboard Matrix and Encoding	
23. When ordering, prefix circuit reference with AF1		
	Complete unit	44828-524F
C1	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C2	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C3	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C4	CAP CER 10N 50V 20% X7R MON AX	26346-120Y
C5	CAP ELEC 47U 10V 20%+ AX	26415-809E
D1	LAMP LED HLMP1503 3.0V GRN	28624-138T
D2	LAMP LED HLMP1503 3.0V GRN	28624-138T
D3	LAMP LED HLMP1503 3.0V GRN	28624-138T
D4	LAMP LED HLMP1401 2.4V YEL	28624-137D
D5	LAMP LED HLMP1401 2.4V YEL	28624-137D
D8	LAMP LED HLMP1401 2.4V YEL	28624-137D
D9	LAMP LED HLMP1503 3.0V GRN	28624-138T
D10	LAMP LED HLMV1503 3.0V GRN	28624-138T
D11	LAMP LED HLMP1503 3.0V GRN	28624-138T
D12	LAMP LED HLMP1401 2.4V YEL	28624-137D
D13	LAMP LED HLMP1503 3.0V GRN	28624-138T
D14	LAMP LED HLMP1401 2.4V YEL	28624-137D
D15	LAMP LED HLMP1401 2.4V YEL	28624-137D
D16	LAMP LED HLMP1401 2.4V YEL	28624-137D
IC1	ICA COMP LM339N QUAD	28461-693H
IC2	ICD ENCOD 74LS148 8INP PRIOR	28465-024N
IC3	ICD ENCOD 74LS148 8INP PRIOR	28465-024N
IC4	ICA COMP LM339N QUAD	28461-693H

Circuit Ref	Description	Part Number
Board AF1	- Keyboard Matrix and Encoding	(Contd)
R1	RES NET 4K7 2% 8DIL	24681-519Z
R2	RES NET 220R 2% 8DIL	24681-501F
R3	RES NET 4K7 2% 8DIL	24681-519Z
R4	RES MF 15K 1/4W 2% 100PPM	24773-301P
R5	RES MF 220R 1/4W 2% 100PPM	24773-257W
SAA	SW PUSH 1CO 24V 10MA	23465-411B
SAB	SW PUSH 1CO 24V 10MA	23465-411B
SAC	SW PUSH 1CO 24V 10MA	23465-411B
SAD	SW PUSH 1CO 24V 10MA	23465-411B
SAE	SW PUSH 1CO 24V 10MA	23465-411B
SAH	SW PUSH 1CO 24V 10MA	23465-411B
SAJ	SW PUSH 1CO 24V 10MA	23465-411B
SAL	SW PUSH 1CO 24V 10MA	23465-411B
SBA	SW PUSH 1CO 24V 10MA	23465-411B
SBB	SW PUSH 1CO 24V 10MA	23465-411B
SBC	SW PUSH 1CO 24V 10MA	23465-411B
SBD	SW PUSH 1CO 24V 10MA	23465-411B
SBE	SW PUSH 1CO 24V 10MA	23465-411B
SCA	SW PUSH 1CO 24V 10MA	23465-411B
SCB	SW PUSH 1CO 24V 10MA	23465-411B
SCC	SW PUSH 1CO 24V 10MA	23465-411B
SCD	SW PUSH 1CO 24V 10MA	23465-411B
SDA	SW PUSH 1CO 24V 10MA	23465-411B
SEA	SW PUSH 1CO 24V 10MA	23465-411B
SEB	SW PUSH 1CO 24V 10MA	23465-411B
SEC	SW PUSH 1CO 24V 10MA	23465-411B
SEE	SW PUSH 1CO 24V 10MA	23465-411B
SEH	SW PUSH 1CO 24V 10MA	23465-411B
SEJ	SW PUSH 1CO 24V 10MA	23465-411B
SHA	SW PUSH 1CO 24V 10MA	23465-411B
SHB	SW PUSH 1CO 24V 10MA	23465-411B
SHC	SW PUSH 1CO 24V 10MA	23465-411B
SHD	SW PUSH 1CO 24V 10MA	23465-411B
SHE	SW PUSH 1CO 24V 10MA	23465-411B
SHH	SW PUSH 1CO 24V 10MA	23465-411B
SHJ	SW PUSH 1CO 24V 10MA	23465-411B
SHL	SW PUSH 1CO 24V 10MA	23465-411B
SJA	SW PUSH 1CO 24V 10MA	23465-411B
SJB	SW PUSH 1CO 24V 10MA	23465-411B
SJC	SW PUSH 1CO 24V 10MA	23465-411B

Circuit Ref	Description	Part Number
Board AF1	- Keyboard Matrix and Encoding	(Contd.)
SJD	SW PUSH 1CO 24V 10MA	23465-411B
SJE	SW PUSH 1CO 24V 10MA	23465-411B
SJH	SW PUSH 1CO 24V 10MA	23465-411B
SJJ	SW PUSH 1CO 24V 10MA	23465-411B
SJL	SW PUSH 1CO 24V 10MA	23465-411B
SLA	SW PUSH 1CO 24V 10MA	23465-411B
SLB	SW PUSH 1CO 24V 10MA	23465-411B
SLC	SW PUSH 1CO 24V 10MA	23465-411B
SLD	SW PUSH 1CO 24V 10MA	23465-411B
X1	SW CAP RECT BK "0"	37590-434A
X2	SW CAP RECT BK "1"	37590-435Z
X3	SW CAP RECT BK "2"	37590-436H
X4	SW CAP RECT BK "3"	37590-437E
X5	SW CAP RECT BK "4"	37590-438U
X6	SW CAP RECT BK "5"	37590-439Y
X7	SW CAP RECT BK "6"	37590-440E
X8	SW CAP RECT BK "7"	37590-441U
X9	SW CAP RECT BK "8"	37590-442Y
X10	SW CAP RECT BK "9"	37590-443N
X11	SW CAP RECT BK "."	37590-433K
X12	SW CAP RECT BK "DELETE"	37590-928G
X13	SW CAP RECT BK "Hz uV"	37590-944R
X14	SW CAP RECT BK "kHz mV"	37590-943C
X15	SW CAP RECT BK "MHz V"	37590-942M
X16	SW CAP RECT "REF LEVEL"	37590-927F
X17	SW CAP RECT "2ND FUNC"	37590-925L
X18	SW CAP RECT "SPAN/DIV"	37590-929V
X19	SW CAP RECT "ANNOT/GRAT"	37590-931G
X20	SW CAP RECT "STORE"	37590-654G
X21	SW CAP RECT BK "-"	37590-926J
X22	SW CAP RECT BK "VIEW" GRN	37590-948Z
X23	SW CAP RECT "RECALL"	37590-655V
X24	SW CAP RECT "A B"	37590-656S
X25	SW CAP RECT "↑" (up arrow)	37590-932V
X26	SW CAP RECT "SAVE"	37590-660W
X27	SW CAP RECT "A-B/A"	37590-661D
X28	SW CAP RECT "MAX/HOLD"	37590-662T
X29	SW CAP RECT BK "CAL"	37590-930F
X30	SW CAP RECT BK "NORM-ALISE"	37590-934W
X31	SW CAP RECT "VIDEO/AVG"	37590-935D
X32	SW CAP RECT "OPTNS"	37590-936T
X33	SW CAP RECT "ADDR/LOCAL"	37590-937P
X34	SW CAP RECT "TEXT"	37590-938X
X35	SW CAP RECT "HORIZ/POSN"	37590-939M

Circuit Ref	Description	Part Number
Board AF1	- Keyboard Matrix and Encoding	(Contd.)
X36	SW CAP RECT "SIGNAL/TRACK"	37590-940P
X37	SW CAP RECT BK "v" (down arrow)	37590-933S
X38	SW CAP RECT "GHz/dB"	37590-941X
X39	SW CAP RECT "VIEW" Black	37590-945B
X40	SW CAP RECT "REF/FREQ"	37590-946K
X41	SW CAP RECT "INC/FREQ"	37590-947A
X58	SPACER CIR - - - LED	37590-737R
X74	CABLE ASSY, AF1 TO AB1	43130-004X
Board AR1	- GPIB Connector and Address	
24. When ordering, prefix circuit reference with AR1		
	Complete unit	44828-516U
SA	SW SLIDE 5NO 25V DIL	23467-312B
SKB	CON 57 FEM 24 FXD PCB VER GPIB	23435-979S
X1	CABLE ASSY, AB1 TO AR1	43129-965P
Board AZ1	- Optical encoder	
25. When ordering, prefix circuit reference with AZ1		
	Complete unit	44990-455W

MECHANICAL COMPONENTS

26. Order without prefix.

Fig. 1

Item No.	Description	Part No.
1	Top cover	35903-884V
2	Bottom cover	35903-885S
3	Trim front, top	34900-900W
4	Trim front, bottom	34900-901D
5	Front panel, marked	35903-766Z
6	Trim rear	34900-470E
7	Rear panel marked	35903-821S
8	Filter tinted c.r.t.	37490-666S
9	Knob assembly 10.5 mm	41149-058W
	Knob cap 10.5 mm	37590-242F
10	Knob assembly 14.5 mm (3 off)	41149-050Y
	Knob cap 14.5 mm (3 off)	37590-279D
11	Knob assembly 32 mm	41149-058R
	Knob cap 32 mm	37590-282D
12	Panel handle assembly (2 off)	41700-382P
13	Clip (2 off)	35903-721D
	Shouldered washer (2 off)	37590-856J
	Insulator (2 off)	37490-701F
14	Foot plastic black 0.75 mm O/D (4 off)	22315-663B
15	Foot rear left hand	34990-913A
	Foot rear right hand	34900-912K
16	Shaft switch extender	37590-741D
17	Side rail (2 off)	24900-476F
18	Contact c.r.t. earthing	31119-087R
19	Clamp p.c.b.	35903-883G

HANDLE END CAP PLAST.C 37590-257
" " METAL 22315-584 *
SPACER FOR 33900-785

* CALLED HANDLE LINER.

To be issued later

Fig. 1 Miscellaneous mechanical parts

Chapter 7

SERVICING DIAGRAMS

CONTENTS

Fig.	Unit	Title	Comp. layout page	Cct. drg. Page
28	+AD1/1	Display drive	87/88	87/88
29	AF1	Keyboard matrix and encoding	89/90	89/90
7	AR1	GPIB connector	17	17
28	AT2	CRT base	87/88	87/88
30	AZ1	Optical encoder		91/92

* Optional unit
\+ c.r.o. display data provided

CIRCUIT NOTES

Component values

1. Resistors : Code letter R = ohms, K = kilohms (10^3), M = megohms (10^6).

Capacitors : Code letter m = millifarads (10^{-3}), μ = microfarads (10^{-6}).
n = naofarads (10^{-9}), p = picofarads (10^{-12}).

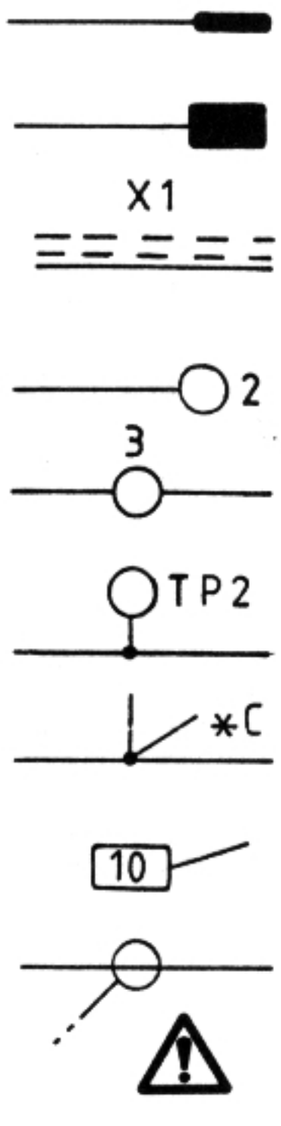
Inductors : Code letter H = henrys, m = millihenrys (10^{-3}).
μ = microhenrys (10^{-6}), n = nanohenrys (10^{-9}).

SIC : value selected during test, nominal value shown.

2. Components are marked normally with two, three or four figures according to the accuracy limit ±10%, ±1% or ±0.1%. The code letter used indicates the multiplier and replaces the decimal point. Because a marking 4m7 could be interpreted as milliohms, millifarads or millihenrys each value is placed near to its related symbol.

Symbols

3. Symbols are based on the provisions of BS 3939 with the following additions :



edge connector

on-board connector

ferrite bead

tags

test point

other point used for test

waveform no.

current probe

warning, see page (iv), Notes and Cautions

unit identification number

printed component

4. Electro-mechanical relays are all shown according to convention, in the de-energized state with all power supplies removed.

PCB layouts

5. PCB layouts are shown as viewed from the component side.

Default settings

6. The waveforms reproduced in this chapter were plotted from a digitizing c.r.o. used as a monitor on selected test points. The screen legends showed unsuppressed zeros after decimal points which were characteristic of the c.r.o. The most frequent c.r.o. settings used to obtain a c.r.o. display of a 2382/2380 under test are described in this chapter as 'default settings'. These are basic settings unless overridden by additional procedures which accompany some waveform photographs.

Sufficient information is given to go direct to a particular waveform (with reference to the Operating Manual if necessary). Attempts to curtail the procedure are likely to result in the incorrect instrument conditions.

Service engineers should be warned that a decision based on inspection of a single waveform can be misleading as the digitizing c.r.o. had a higher resolution than the models generally available to service engineers.

SCOPE SETTING [DEFAULT]
CH1 [2V/DIV]:
CH2 [OFF]:
TRIGGER [AUTO, +ve, CH1]:
MAIN TIMEBASE [ON]:
DELAY TIMEBASE [ON]:
MODE [MAIN TIMEBASE, MULTIPLE SWEEP]:

2382/2380 default setting under
PROCEDURE
1. SWITCH ON,

KEY; CH1 and CH2 are channels 1 and 2 of the c.r.o. with channel 1 displayed above channel 2 on the tube.

Debug operations

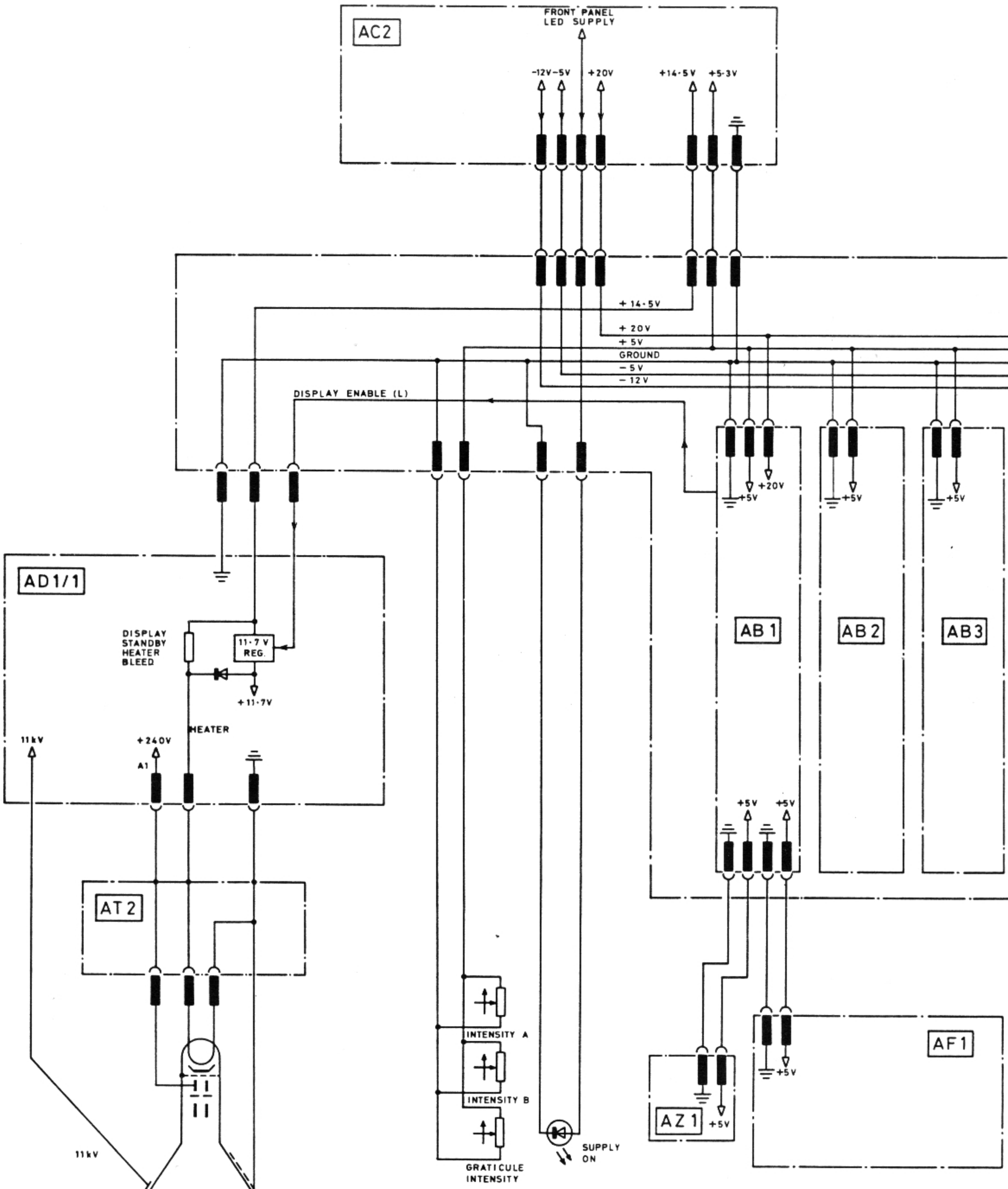
7. The terms 'debug operations mode' and 'diagnostic mode' are synonymous for the complete instrument 2382/2380.

The following procedure applies in this chapter whenever the instruction 'enter debug operations mode' appears:-

On unit 2382 hold [INTMD IDENT] key in the depressed position throughout this sequence.

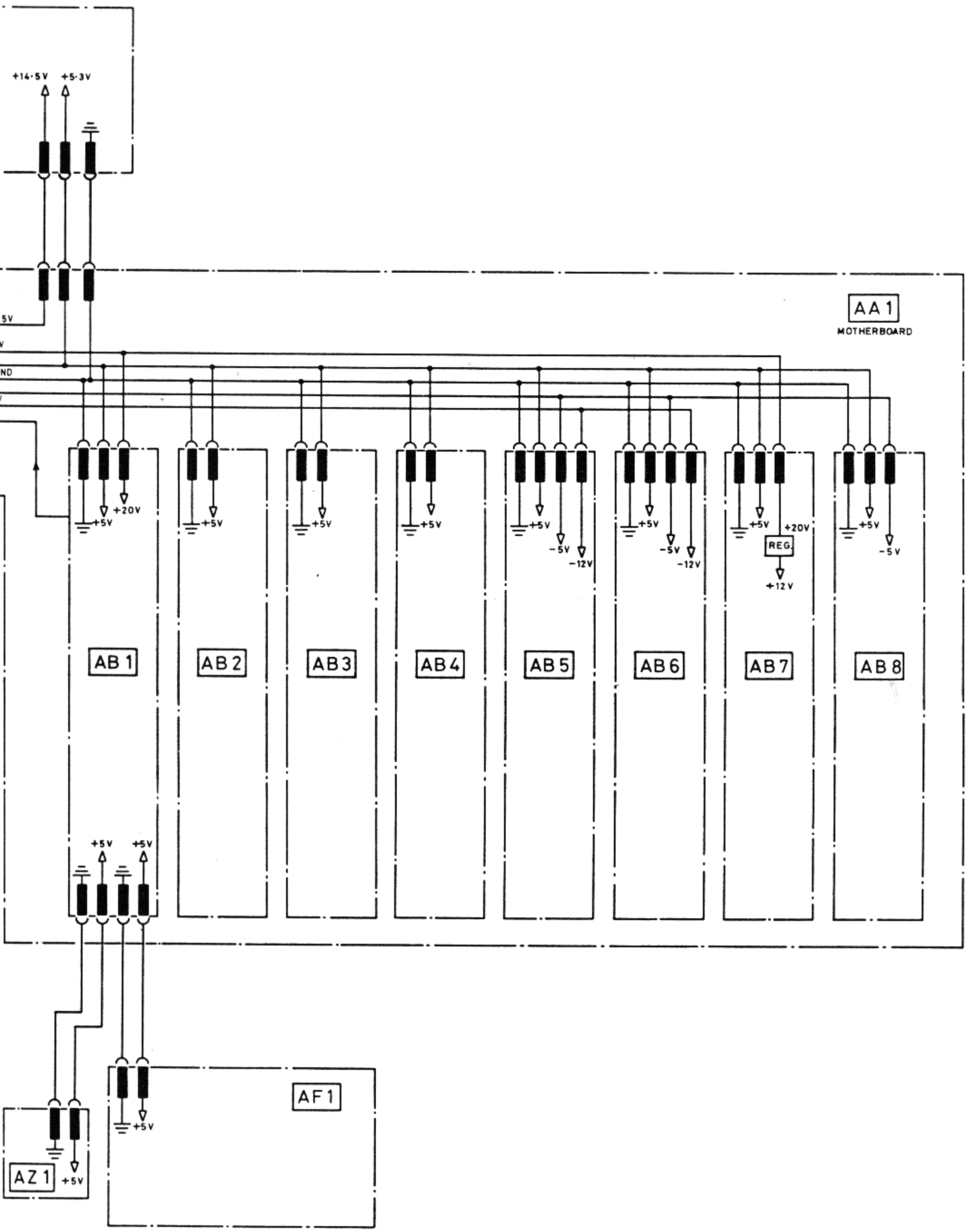
On unit 2380, press [2ND FUNCT], [SET TG], [2ND FUNCT], [REF LEVEL], 23.82 dB on function/data keypad.

Release [INTMD IDENT] key.



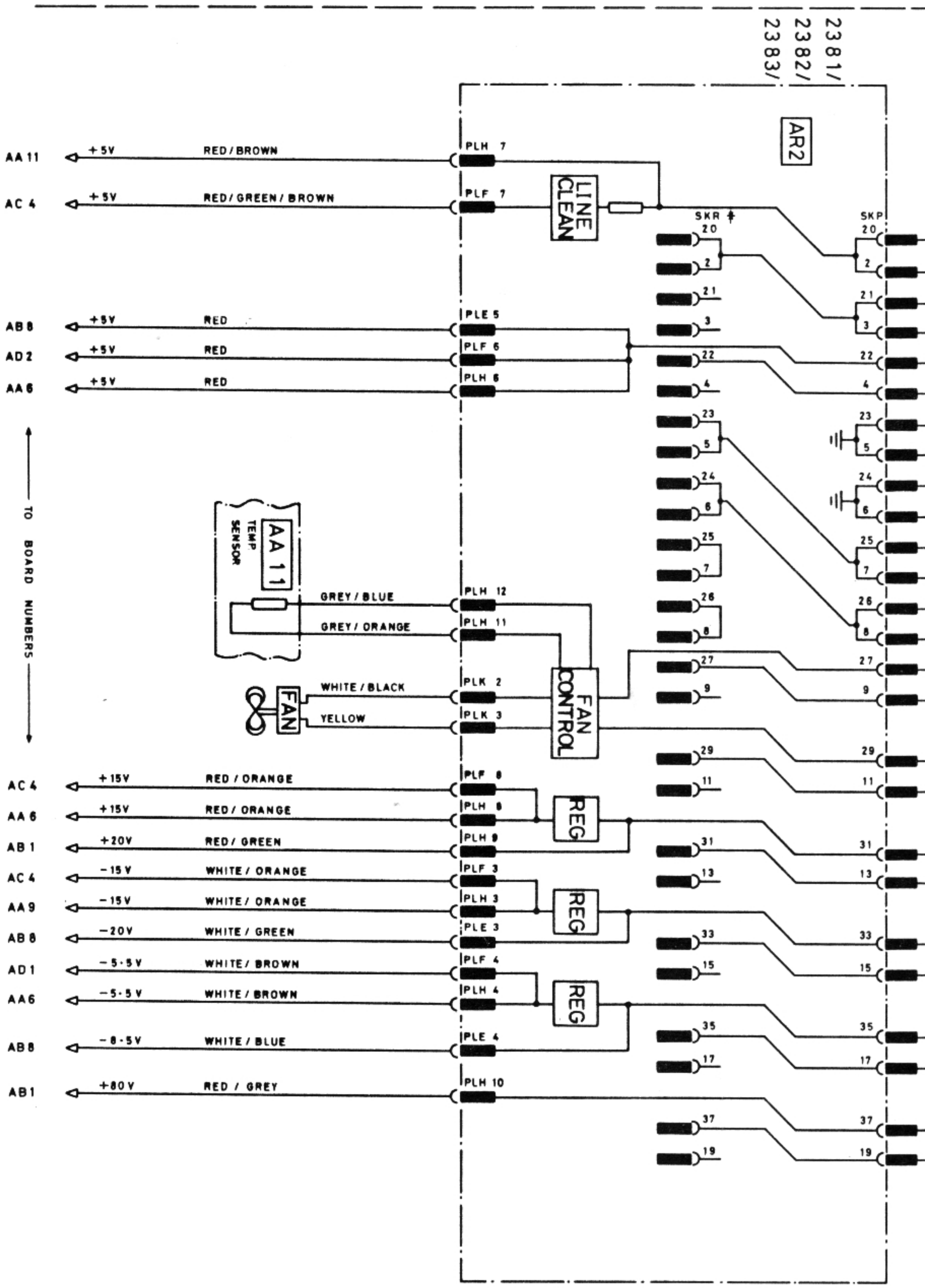
Drg.No.Z52380-900E
Sh.1 Iss.1

HT Supplies Routing Diagram



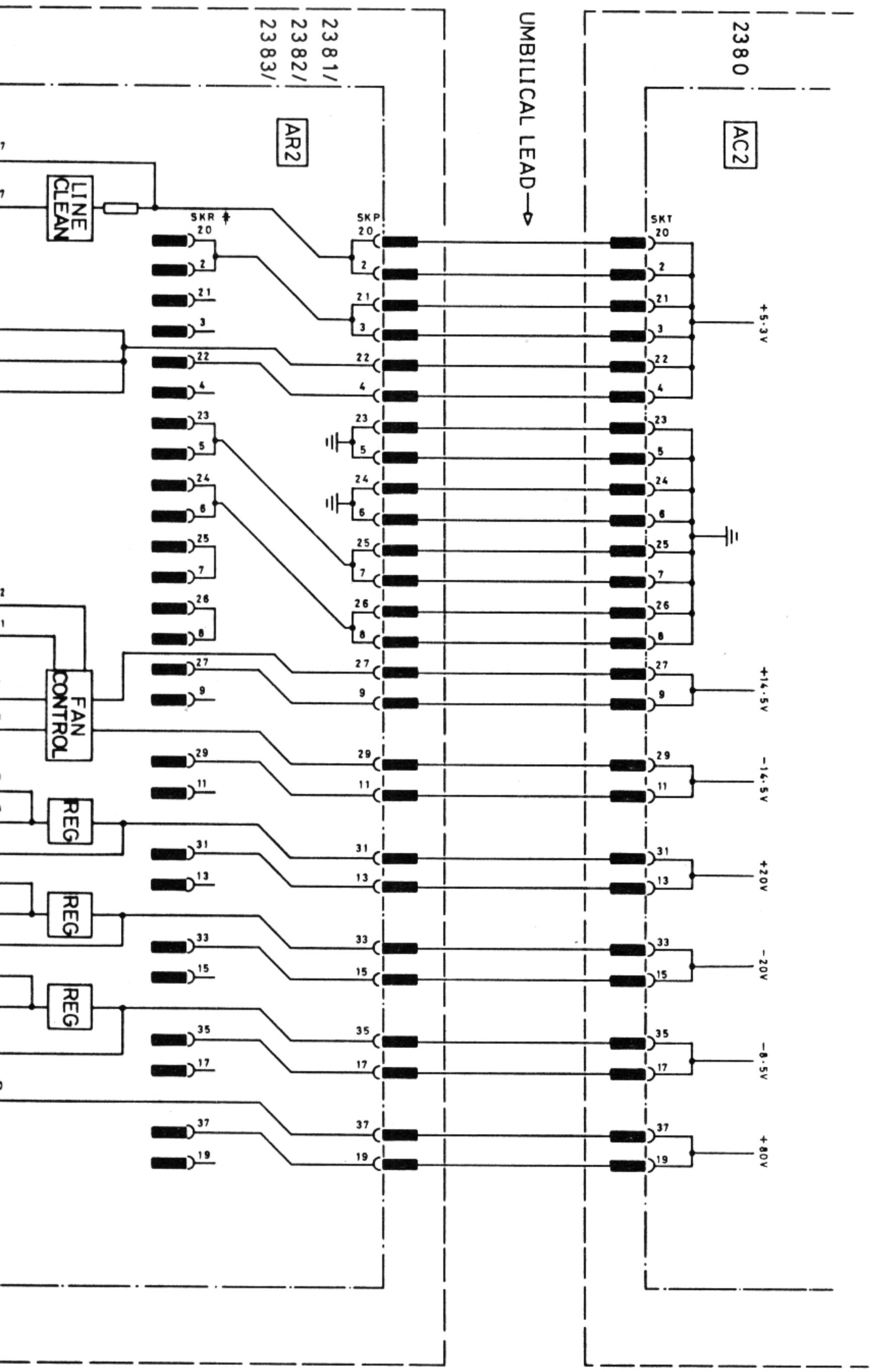
pplies Routing Diagram

Fig. 1
Chap. 7
Page 5/6



Drg.No.Z52380-900E
Sh.2 Iss.1

Inter unit power wiring diagram

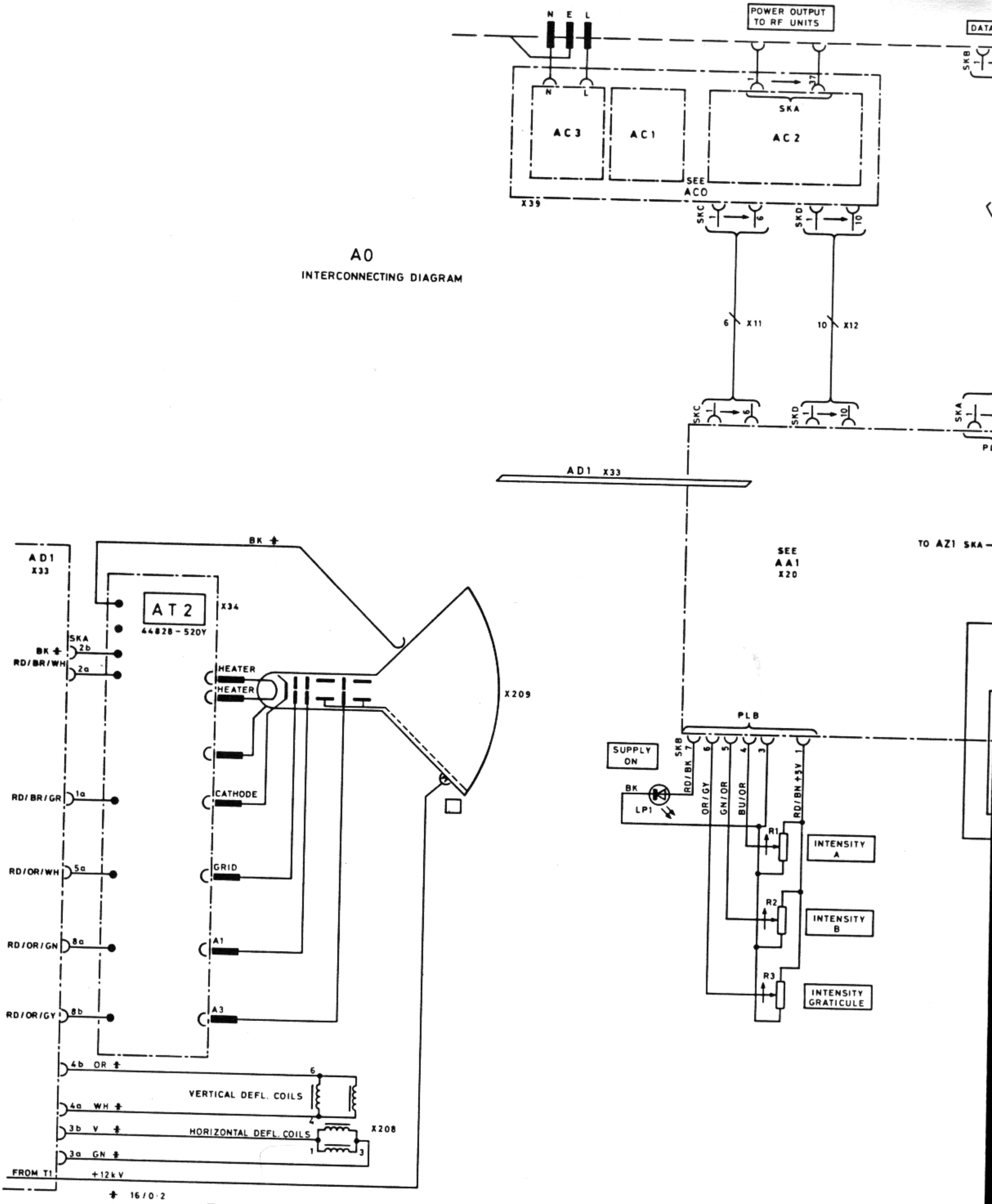


unit power wiring diagram

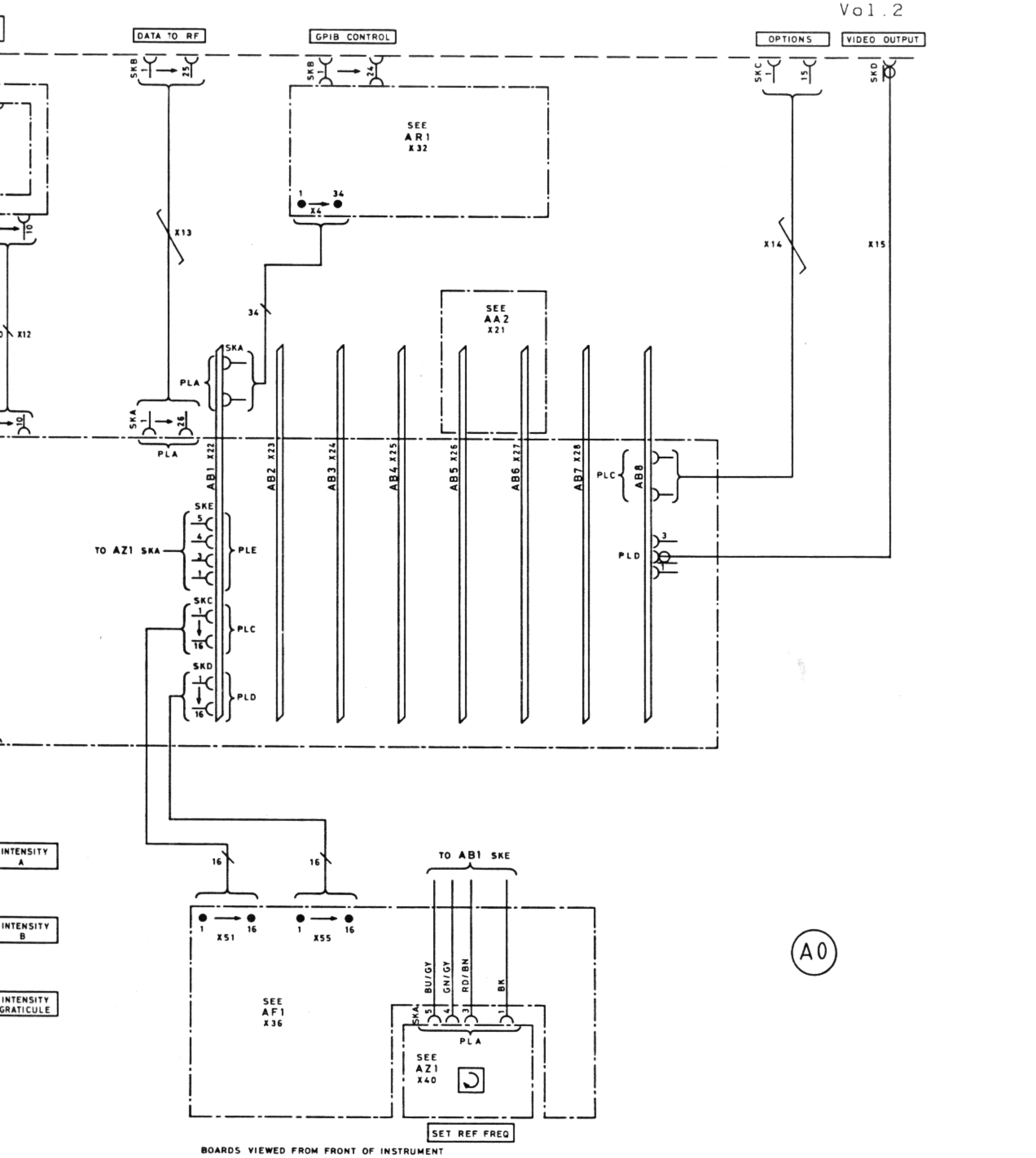
Fig. 2
Chap. 7
Page 7/8

A0

INTERCONNECTING DIAGRAM



Drg. No. Z52380-900E
Sh. 3 Iss.1



A0

nnecting diagram

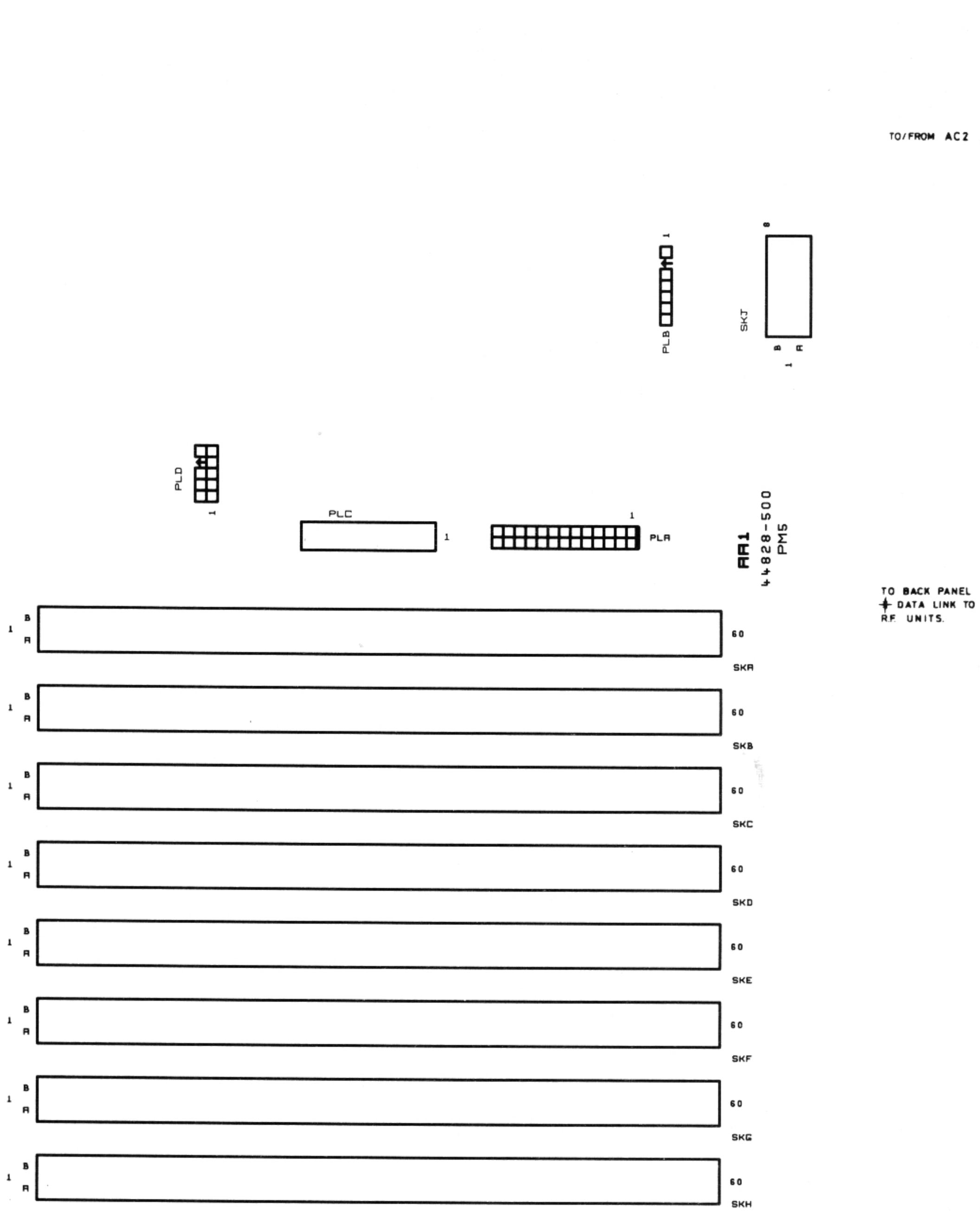


Fig. 4
May 86

Plug and edge connector connections AA1

PART OF AA1 44828-500D

CONTINUED ON SHEET TWO

TO/FROM AC2

PLD
8 +20V
9 -5V
10 -12V
4
3
7 SPARE 1
5
1
2

PLA
12
13 LINE TRIG.
14
15 REMOTE OVERHEAT (L)
21 EXT. STD. (L)
125KHz
HOT (L)
11 RESET LOW 5V LINE(L)
6 SERIAL DATA
5 END OF CONVERSION
7 UART RX-
8 UART RX+
9 UART TX-
10 UART TX+

TO BACK PANEL ⧫ DATA LINK TO RF UNITS.

4
1,2,3
16,17,18, 19,20
22,23,24, 25,26.

PLC
6 +14·5V
5
4 +5V
3
2
1

FROM AC2

PCLK	PCLK	SPARE	MD7
BREAK	BREAK	SPARE	MD6
SPARE 1	SPARE 1	SPARE	MD5
INTA (L)	INTA (L)	SPARE	MD4
INT	INT	SPARE	MD3
CS0X (L)	CS0X (L)	SPARE	MD2
CLOCK TICK [1R7]	CS1E (L)	SPARE	MD1
EOS [1R3]	CS16 (L)	SPARE	MD0
SPARE	SPARE	SPARE	SPAR
LOW 5V LINE (L)	LOW 5V LINE (L)	SPARE	SPAR
SERIAL DATA	DACK 0 (L)+ HOLD (L)	SPARE	BSEL
END OF CONVERSION (L)	DRQ 0	SPARE	A OR
CS2X (L) + IORD (L)	CS2X (L)+ IORD (L)	SPARE	WD (
CS1C (L)	CS1C (L)	SPARE	SPAR
CS1A (L)	CS1A (L)	SPARE	SPAR
CS10 (L)	CS10 (L)	SPARE	SPAR
+20V			
SPARE			
5MHz SYNC. LOCK			
SPARE			
GROUND			
12·5MHz			
GROUND			
6·25 MHz CLOCK			
GROUND			
IORD (L)			
GROUND			
IOWR (L)			
GROUND			
A3			
POLARISATION			
POLARISATION			
GROUND			
A2			
GROUND			
A1			
GROUND			
A0			
-12V			
-5V			
+5V			
+5V			
+5V			
+5V			

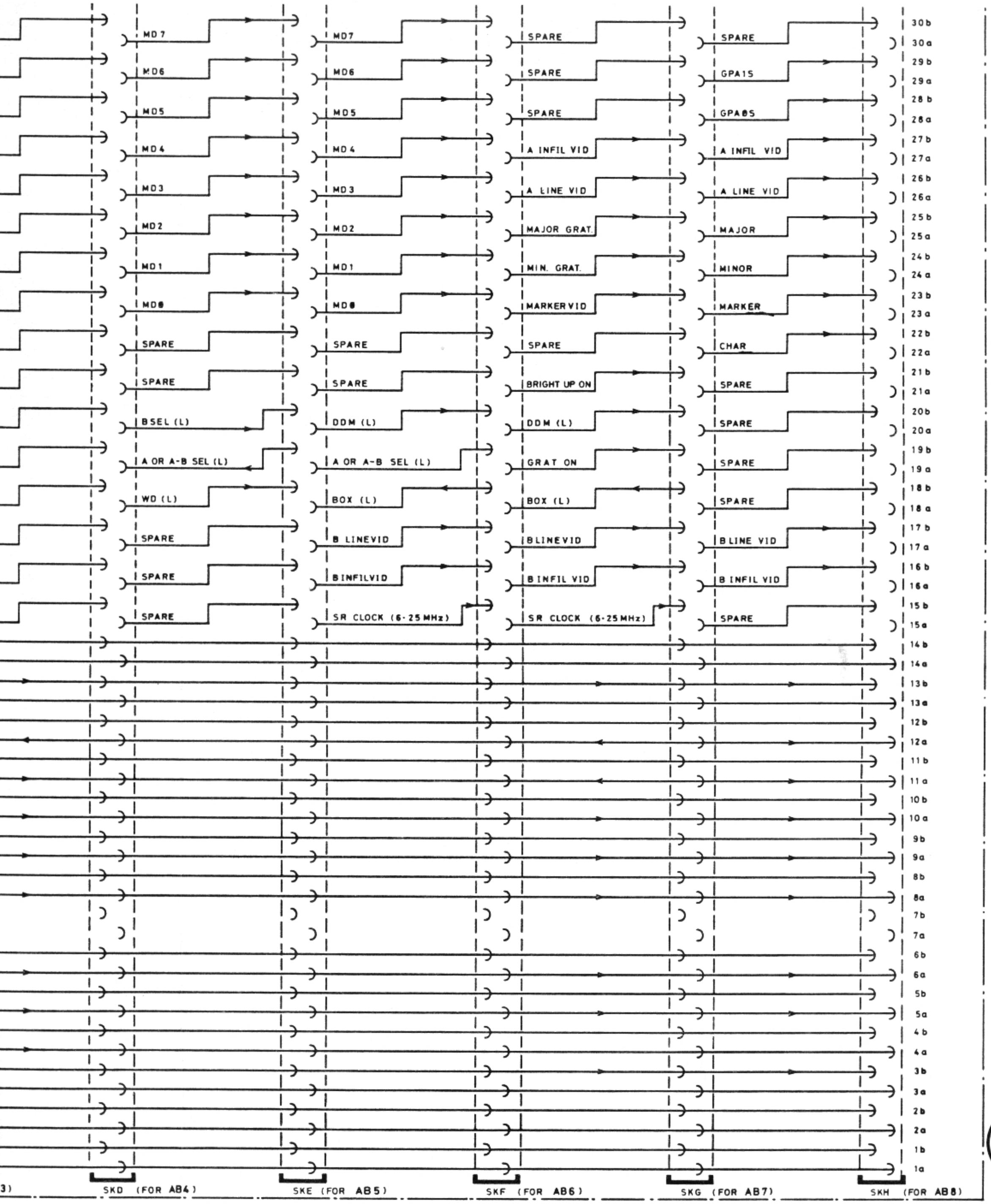
SKA (FOR AB1) SKB (FOR AB2) SKC (FOR AB3) SKD (FOR

⧫ DUPLICATED ON THIS DIAGRAM FOR CLARITY.
⧫ FOR CONNECTION DETAILS SEE CIRCUIT AO

Drg.No. Z44828-500D
Sh.1 Iss.1

AA1: Display unit, motherboa

ON SHEET TWO



nit, motherboard interconnection

Fig. 4
Chap. 7
Page 11/12

‡ FOR CONNECTION DETAILS SEE CIRCUIT A0

DUPLICATED ON THIS DIAGRAM FOR CLARITY.

PART OF
AA 1
44828-500D

SKA (FOR AB1) SKB (FOR AB2) SKC (FOR AB3) SKD (FOR

+5V
+5V
+5V
+5V
-5V
-12V
GROUND
D7
GROUND
D6
GROUND
D5
GROUND
D4
GROUND
D3
GROUND
D2
GROUND
D1
GROUND
D0
SPARE
RESET
FRAME (L)
SPARE
DACK 3 (L)
DRQ 3
SPARE
DACK 2 (L)
SPARE
DRQ 2
CAS 2
DACK 1(L)‡IOWR(L)
CAS 1
DRQ 1
CAS 0
CS3X (L).
CS0C (L)
CS1B (L)
CHAR ON
CS14 (L)
HRTC (L)
VRTC (L)
SLAVE INT
KEY
RDY 1
CS5X (L)
SPARE
+14·5V
SPARE
SPARE
SPARE
SPARE
SPARE
SPARE

SKJ
5a 5b 6a 6b 7a 7b 8a 8b
TO AD1 PLA

PLD 6 SUPPLY INDICATOR POWER
FROM AC2 PLD 6

PLB
7 VIDEO
6 CONTRA 3
5 CONTRA 2
4 CONTRA 1
3
2
1 +5V
TO FRONT PANEL ‡

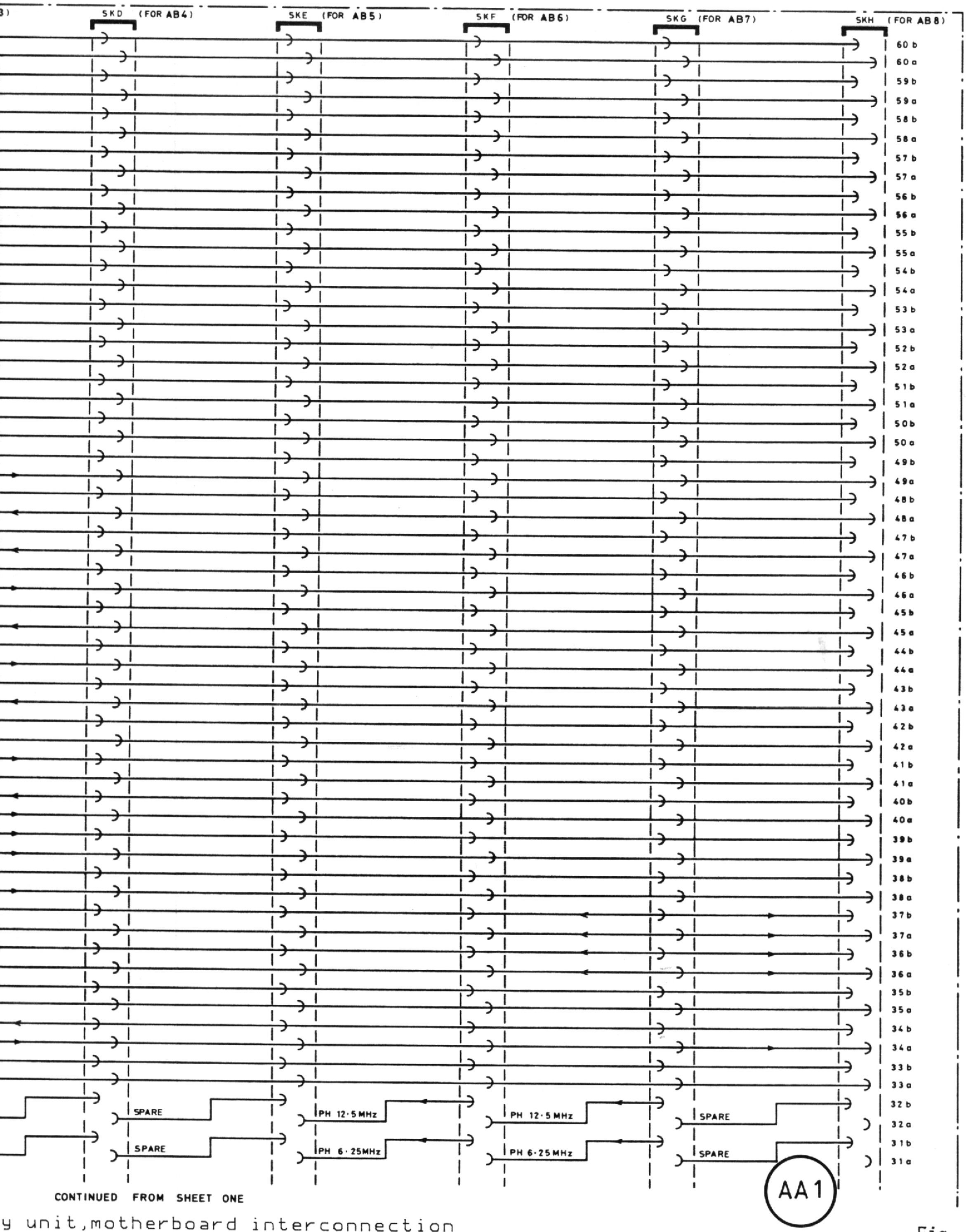
SKJ
1a HSYNC
1b VSYNC
2a 2b 3a 3b 4a 4b
TO AD1 PLA
+14·5V
+14·5V
DISPLAY ENABLE (L)

PLC 6 +14·5V
FROM AC2 ‡

CONTINUED FROM

Drg.No. Z44828-500D
Sh.2 Iss.1

AA1: Display unit, mother



y unit,motherboard interconnection

Fig. 5
Chap. 7
Page 13

BOARD : AB1
KEY OF FUNCTIONS :

1 GATED VERSION OF 'KEY PRESSED (L)'
2 'KEY' - ACTIVE HIGH TTL, DEBOUNCED KEY SIGNAL, HIGH WHILE A KEY IS DEPRESSED
3 INPUT FROM SHAFT ENCODER ASSY
4 INPUT FROM F/P SHAFT ENCODER ASSY
5 DECODED CLOCKWISE INFORMATION FROM 'REF FREQ' CONTROL
6 DECODED COUNTER-CLOCKWISE INFORMATION FROM F/P 'REF FREQ' CONTROL

continued opposite Fig. 7

1 BOARD : AB1

FUNCTION : GATED VERSION OF 'KEY PRESSED (L

TEST POINT : PLAA
GROUND POINT : C1 (end nearest edge of PCB)
SCOPE SETTING
MAIN TIMEBASE : 10 ms/DIV

PROCEDURE :

1. Check for HIGH (TTL) state.
Check for LOW (TTL) state while any ke
trying [2ND FUNCT].

2 BOARD : AB1

FUNCTION : 'KEY' - ACTIVE HIGH TTL.
(Debounced key signal, HIGH whil

TEST POINT : PLAB
GROUND POINT : C1 (end adjacent to PCB edge
SCOPE SETTING
MAIN TIMEBASE : 10 ms/DIV

PROCEDURE :

1. Check PLAA is in steady (TTL) LOW stat
Press [2ND FUNCT], check that PLAA goes

3 BOARD AB1

FUNCTION : INPUT FROM SHAFT ENCODER ASSY.

TEST POINT : PLAC
GROUND POINT : C15 (end adjacent to C14)
SCOPE SETTING
MAIN TIMEBASE : 10 ms/DIV

PROCEDURE :

1. Rotate REF FREQ control, check that PLA

SSED (L)'.

of PCB)

any key is depressed on the top unit by

GH while a key is depressed.)

CB edge)

OW state.
A goes HIGH (TTL) while key is depressed.

ASSY.

:14)

hat PLAC changes state (TTL).

4 BOARD : AB1

FUNCTION : INPUT FROM F/P SHAFT ENCODER ASSY.

TEST POINT : PLAD
GROUND POINT : C15 (end adjacent to C14)
SCOPE SETTING
MAIN TIMEBASE : 10 ms/DIV

PROCEDURE :

1. Check that PLAD changes state (TTL) as REF FREQ is rotated.

5 BOARD : AB1

FUNCTION : DECODED CLOCKWISE INFORMATION FROM REF FREQ CONTROL.

TEST POINT : PLAE
GROUND POINT : C15 (end adjacent to C14)
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 500 ns/DIV

NOTE. Full brilliance required.

PROCEDURE :

1. Temporarily put scope CH1 probe on PLAK and adjust the scope trigger level to obtain a steady scope display. Replace CH1 scope probe on PLAE. Check that LOW (TTL) pulses (1 μs long) are produced by rotating SET REF clockwise. (The faster REF FREQ is rotated, the more easily the pulses are seen).

2. Check that no pulses are present when rotating REF FREQ counter-clockwise.

6 BOARD : AB1

FUNCTION : DECODED COUNTER-CLOCKWISE INFORMATION FROM F/P REF FREQ CONTROL.

TEST POINT : PLAH
GROUND POINT : C15 (end adjacent to C14)
SCOPE SETTING
TRIGGER : -ve MANUAL
MAIN TIMEBASE : 500 ns/DIV

NOTE. Full brilliance required.

PROCEDURE :

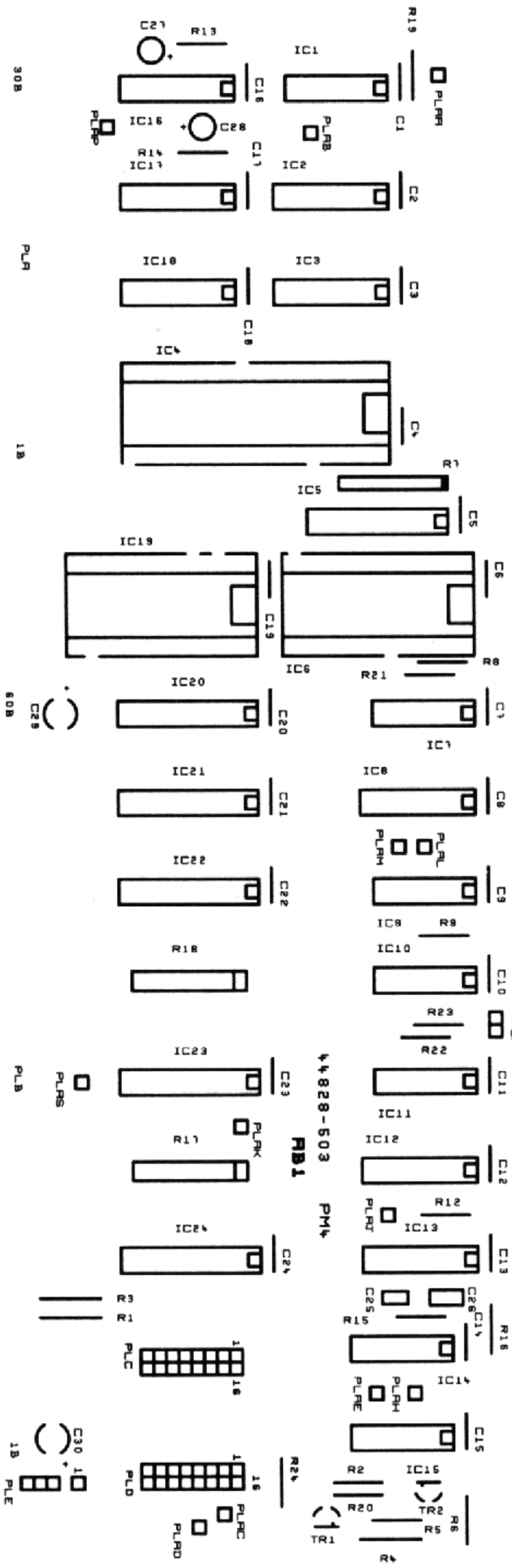
1. Temporarily put scope CH1 probe on PLAK, and adjust the scope trigger level to obtain a steady display. With CH1 scope probe on PLAH, check that LOW (TTL) pulses (1 μs long) are produced when REF FREQ is rotated counter-clockwise. (Turning REF FREQ quickly makes the pulses more visible.)

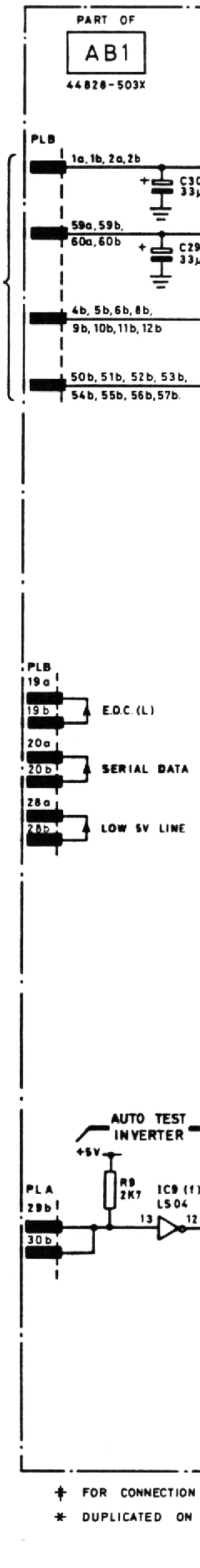
2. Check that no pulses are produced by rotating REF FREQ clockwise.

Waveforms for AB1

Fig. 6A

May 86





Component layout AB1

Fig. 6
May 86

PART OF

AB1

44828-503X

PLB

1a, 1b, 2a, 2b

C30 33µ

+5V

59a, 59b, 60a, 60b

C29 33µ

FROM ‡ ACO

4b, 5b, 6b, 8b, 9b, 10b, 11b, 12b

50b, 51b, 52b, 53b, 54b, 55b, 56b, 57b.

SUPPLY LINE TABLE					
IC	+5 V	GROUND	IC	+5 V	GROUND
IC1	14	7	IC13	16	8
IC2	16	8	IC14	14	7
IC3	16	8	IC15	14	7
IC4	40	20	IC16	16	8
IC5	20	10	IC17	16	8
IC6	28	14	IC18	16	8
IC7	14	7	IC19	26	4
IC8	16	8	IC20	20	10
IC9	14	7	IC21	20	10
IC10	14	7	IC22	20	10
IC11	5	10	IC23	20	10
IC12	16	8	IC24	20	10

ALL IC'S DECOUPLED AT +5V PIN TO GROUND RAIL WITH 10n CAPACITOR.

TO AF1 PLC 1,2,3,4 6,7,8,9

FROM AF1 X51 10 11 12 13 KD5 KD4 KD3

FROM AF1 X51 14 15 16 KD2 KD1 KD0

KEY PRESSED (L)

+5V

IC24 LS374 CLK LATCH OE D7 D0

QUIET

IC14 (a) LS 86

1 PLAA

KEY DEBOUNCE CIRCUITRY

'MAKE' DEBOUNCE MONO

'BREAK' DEBOUNCE MONO

IC1 (a) LS74

IC1(b) LS74

2 PLAB

R14 6K8 C28 1µ0 IC16 (a) LS221

R13 33K C27 1µ0 IC16(b) LS221

IC14(d) LS86

PLB 19a 19b E.O.C. (L)

20a 20b SERIAL DATA

28a 28b LOW 5V LINE

FROM AB3 PLB 18a 16a 17a 18b 16b 17b

AZ1

44828-523J

SHAFT

SEE DIAGRAM

AUTO TEST INVERTER

PLA 29b 30b R9 2K7 IC9 (f) LS04

AUTO TEST INPUT

R19 2K2

PLC 5

PLB 49a*

RESET

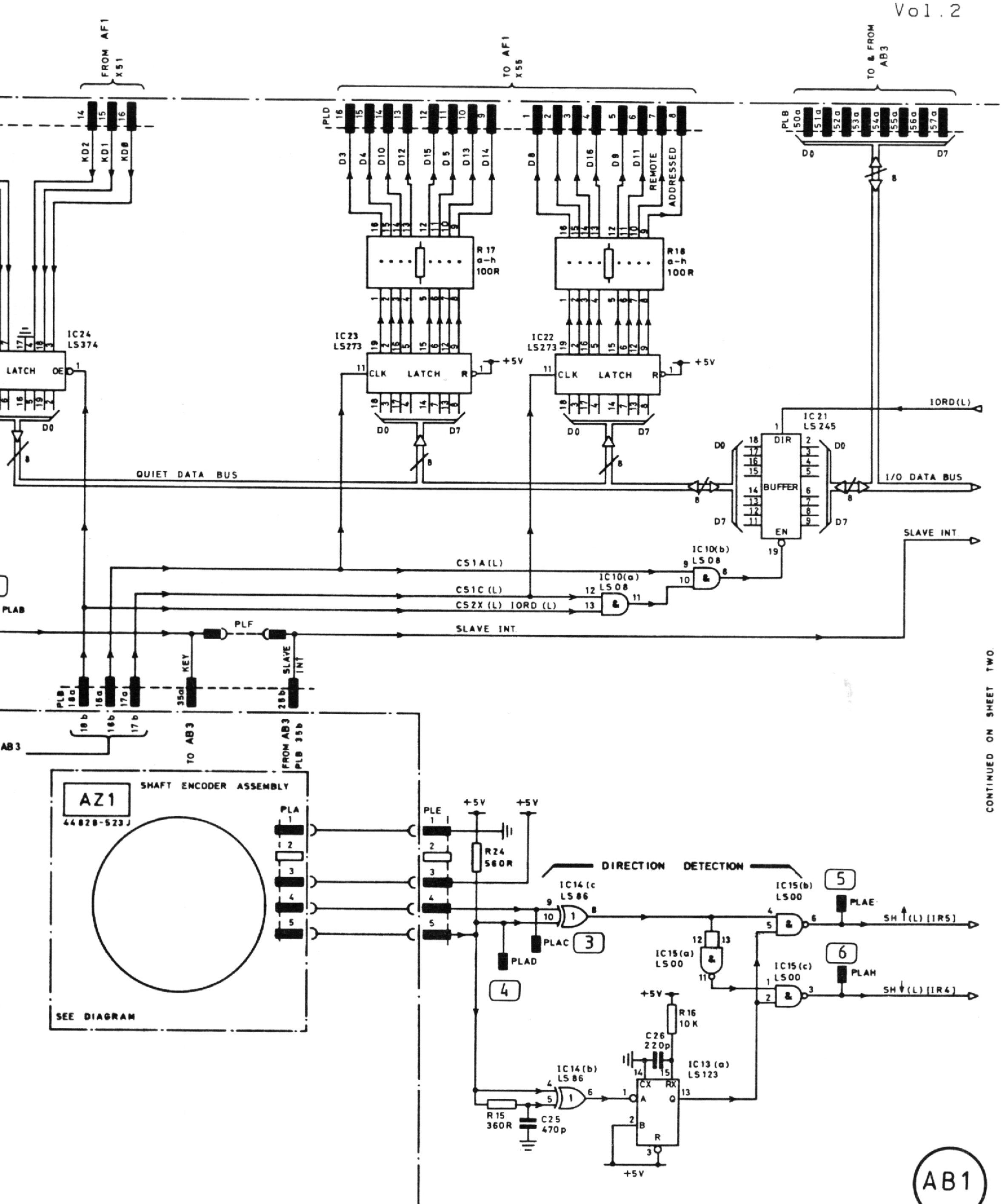
FROM AB3 PLB 49a

‡ FOR CONNECTION DETAILS SEE CIRCUIT ACO.

* DUPLICATED ON THIS DIAGRAM FOR CLARITY.

Drg.No. Z52380-900E
Sh.4 Iss.1

AB1 : I/O & Keyboard


FROM AF1 X51
TO AF1 X55
TO & FROM AB3
PLD
PLB
KD2
KD1
KD0
D3
D4
D10
D12
D15
D5
D13
D14
D8
D16
D9
D11
REMOTE
ADDRESSED
D0
D7
R 17 a-h 100R
R18 a-h 100R
IC24 LS374
IC23 LS273
IC22 LS273
LATCH
OE
CLK
R
+5V
IC21 LS245
DIR
BUFFER
EN
IORD(L)
I/O DATA BUS
QUIET DATA BUS
IC10(b) LS08
IC10(a) LS08
CS1A(L)
CS1C(L)
CS2X(L) IORD(L)
SLAVE INT
PLAB
PLF
KEY
SLAVE INT
AB3
TO AB3
FROM AB3 PLB 35b
AZ1
SHAFT ENCODER ASSEMBLY
44828-523J
SEE DIAGRAM
PLA
PLE
R24 560R
DIRECTION DETECTION
IC14(c LS86
IC15(b) LS00
IC15(a) LS00
IC15(c) LS00
PLAE
PLAH
PLAC
PLAD
SH↑(L) [IR5]
SH↓(L) [IR4]
R16 10K
C26 220p
IC14(b) LS86
IC13(a) LS123
R15 360R
C25 470p
CX
RX
A
B
Q
R
CONTINUED ON SHEET TWO
AB1

BOARD : AB1
KEY OF FUNCTIONS (concluded)

7 125 kHz - TTL WAVEFORM CLOCK
8 BAUD RATE CLOCK (TTL)
9 RECEIVED DATA - FROM LOWER UNIT - AT 9600 BAUD
10 TRANSMITTED DATA (TO LOWER UNIT) - AT 9600 BAUD
11 PCLK - 2.083 MHz TTL CLOCK (480 ns PERIOD) INPUT CLOCK TO GPIB CONTROLLER

---

7 BOARD : AB1

FUNCTION : 125 kHz - TTL WAVEFORM CLOCK.

TEST POINT : PLAJ
GROUND POINT : C13 (end adjacent to C12)
SCOPE SETTING
MAIN TIMEBASE : 1 ms/DIV

PROCEDURE :

1 Check for : TTL clock, period = 8 µs
clock LOW time = 1.6 µs
(clock HIGH time = 6.4 µs).

---

8 BOARD : AB1

FUNCTION : BAUD RATE CLOCK (TTL).

TEST POINT : PLAK
GROUND POINT : C24 (end adjacent to PLAK)
SCOPE SETTING
MAIN TIMEBASE : 1 µs/DIV

PROCEDURE :

1. Check for : TTL clock period = 6.4 µs
HIGH, LOW clock time = 3.2 µs.

---

9 BOARD : AB1

FUNCTION : RECEIVED DATA - FROM LOWER UNIT

TEST POINT : PLAL
GROUND POINT : C8 (end adjacent to C7)
SCOPE SETTING
MAIN TIMEBASE : 500 µs/DIV

PROCEDURE :

1. Check for a TTL pulse train (lasting 4
The intervening periods should be (TTL

---

10 BOARD : AB1

FUNCTION : TRANSMITTED DATA (TO LOWER UNIT)

TEST POINT : PLAM
GROUND POINT : C8 (end adjacent to C7)
SCOPE SETTING
MAIN TIMEBASE : 500 µs/DIV

PROCEDURE :

1. Check for a TTL pulse train (lasting 4
The intervening periods should be (TTL

---

11 BOARD : AB1

FUNCTION : PCLK - 2.083 MHz TTL CLOCK (480 n
GPIB CONTROLLER.

TEST POINT : PLAS
GROUND POINT : C24 (end adjacent to PLAK)
SCOPE SETTING
MAIN TIMEBASE : 100 ns/DIV

PROCEDURE :

1. Check for : TTL clock period = 480 ns
HIGH, LOW clock time = 240 ns.

- AT 9600 BAUD
) - AT 9600 BAUD
ns PERIOD) INPUT CLOCK TO

9 BOARD : AB1

FUNCTION : RECEIVED DATA - FROM LOWER UNIT - AT 9600 BAUD.

TEST POINT : PLAL
GROUND POINT : C8 (end adjacent to C7)
SCOPE SETTING
MAIN TIMEBASE : 500 µs/DIV

PROCEDURE :

1. Check for a TTL pulse train (lasting 4 ms), repeating 2 or 3 times/second. The intervening periods should be (TTL) HIGH.

OCK.

C12)

8 µs
1.6 µs
6.4 µs).

10 BOARD : AB1

FUNCTION : TRANSMITTED DATA (TO LOWER UNIT) - AT 9600 BAUD

TEST POINT : PLAM
GROUND POINT : C8 (end adjacent to C7)
SCOPE SETTING
MAIN TIMEBASE : 500 µs/DIV

PROCEDURE :

1. Check for a TTL pulse train (lasting 4 ms), repeating 2 or 3 times/second. The intervening periods should be (TTL) HIGH.

LAK)

.4 µs
.2 µs.

11 BOARD : AB1

FUNCTION : PCLK - 2.083 MHz TTL CLOCK (480 ns PERIOD) INPUT CLOCK TO GPIB CONTROLLER.

TEST POINT : PLAS
GROUND POINT : C24 (end adjacent to PLAK)
SCOPE SETTING
MAIN TIMEBASE : 100 ns/DIV

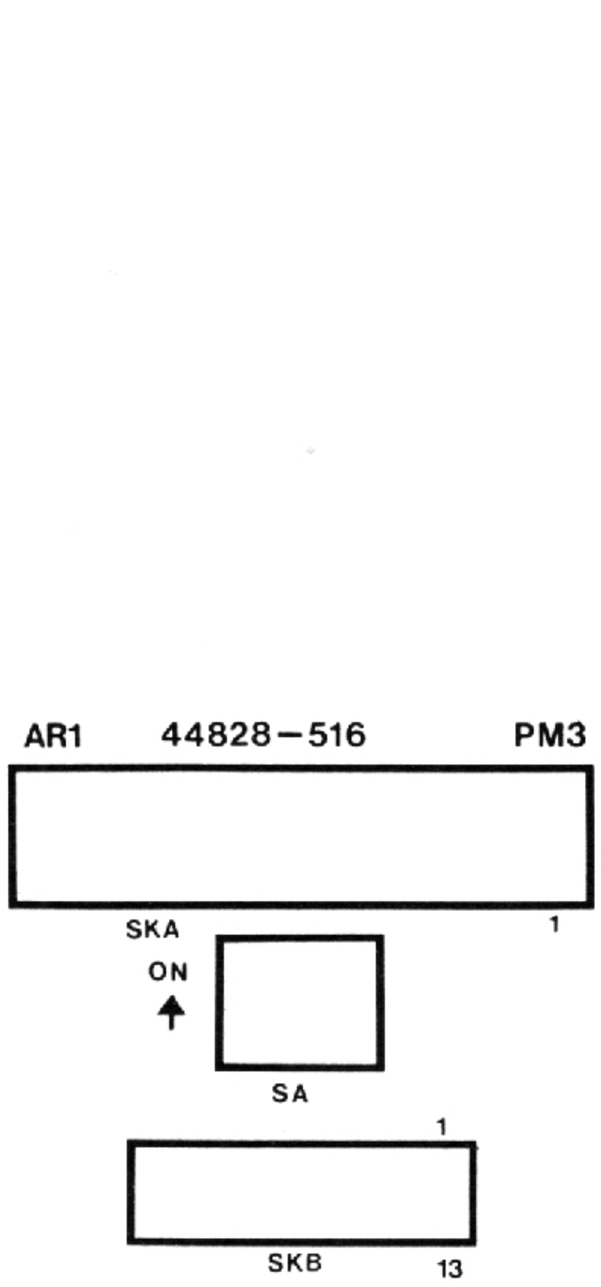
PROCEDURE :

1. Check for : TTL clock period = 480 ns
HIGH, LOW clock time = 240 ns.

Waveforms for AB1

Fig. 7A

May 86



Switch & sockets underside layout AR1

Fig. 7
May 86

DISPLAY ENABLE

IC7(a) LS32

IC20 LS273

DISPLAY ENABLE (L)

CHAR ON

÷10

IC12(a) IC12(b) LS390

6·25MHz

÷5

IC15(d) LS00

125 KHz

PLAJ

BAUD RATE GENERATOR ÷4

IC11 LS390

PLAK

AUTO TEST LEAD

AUTO TEST LEAD

AUTO TEST LEAD

RESET

PCLK

BREAK

INTER-UNIT BUS UART

IC19 8251A

RXD

CTS

TXD

RXC

TXC

RX RDY

TX RDY

RESET

C/D

CS IORD IOWR

[IR1]

[IR0]

A0

IORD (L)

I/O DATA BUS

INTERRUPT CONTROLLER

IC6 8259A

SLAVE INT [IR6]

R22 4k7

R23 4k7

R21 4k7

R8 4k7

IR0 IR1 IR2 IR3 IR4 IR5 IR6 IR7

INT

INTA

CAS0 CAS1 CAS2

A0

CONTINUED FROM SHEET ONE

SH↑ (L) [IR5]

SH↓ (L) [IR4]

[IR3]

END OF SWEEP

CLOCKTICK

INT

INTA (L)

CAS0

CAS1

CAS2

A0

2-4 LINE CHIP SELECT DECODERS

8 BYTE BOUNDARY

IC8(a) LS139

A3

CS0X (L)

A1

A2

CS00 (L)

2 BYTE BOUNDARY

IC8(b) LS139

CS0E (L)

CS08 (L)

CS0A (L)

CS0C (L)

IORD(L)

IOWR(L)

TO AB8

FROM AB3 PLB

FROM AB2 PLB 23b

FROM AB2 PLB 24b

TO AB3

FROM AB3 PLB 27b

TO AB3

TO AB3

TO AB3

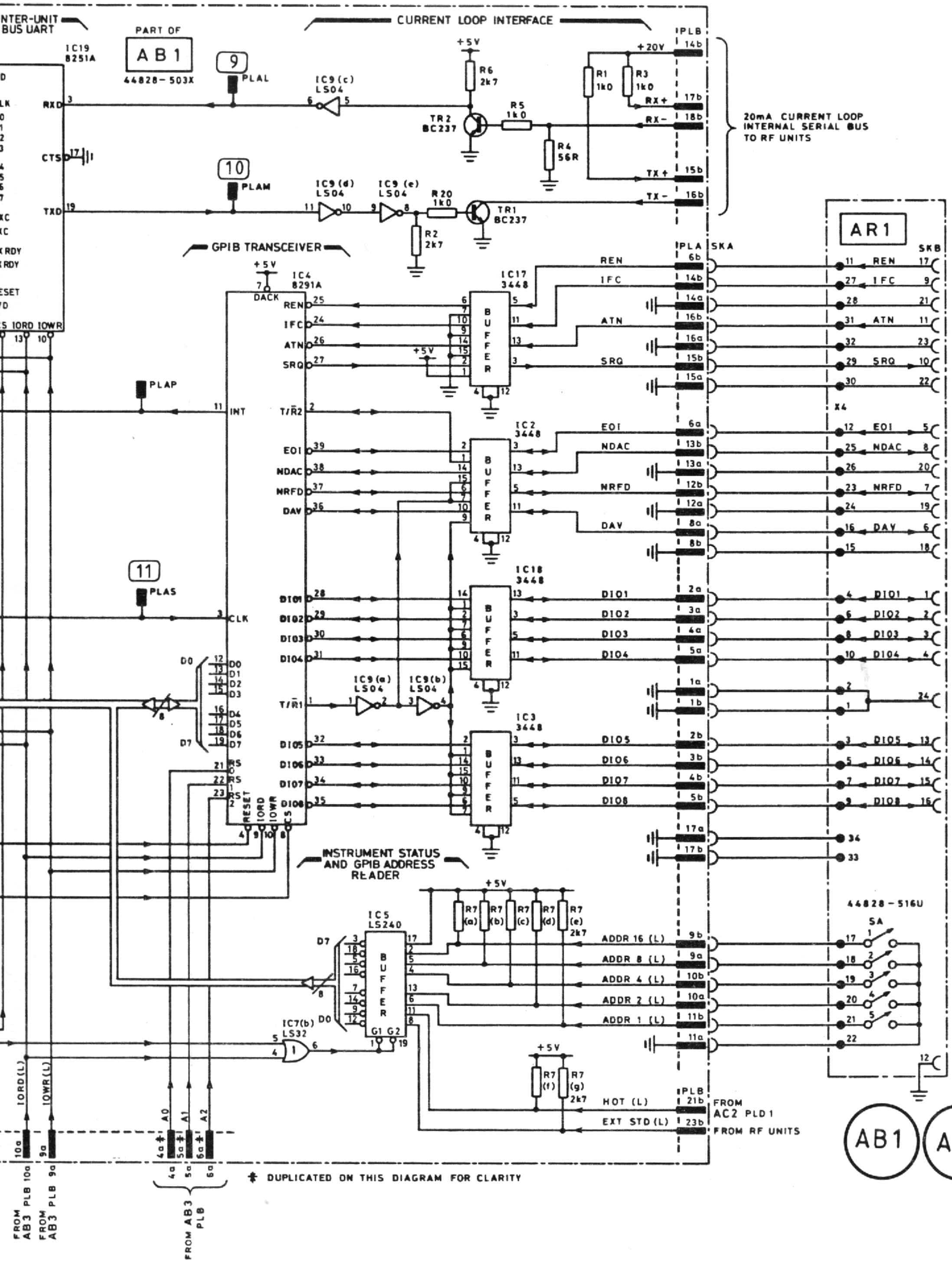
FROM AB3 PLB 4a

FROM AB3 PLB 10a

FROM AB3 PLB 9a

Drg.No. Z52380-900E
Sh.5 Iss.1

AB1 : I/O & Keyboard
AR1 : GPIB Connector



I/O & Keyboard communication
GPIB Connector

BOARD : AB2
KEY OF FUNCTIONS

1 12.5 MHz CLOCK
2 SYNCHRONIZED 'END OF CONVERSION'
3 PLAC - OUTPUT FROM CHANNEL 1 OF AMD 9513 COUNTER (IC20)
4 STROBED 2.5 MHz-CLOCK
5 AVERAGER CLOCK COUNTER OUTPUT (VIDEO BANDWIDTH CONTROL)
6 GATED 2.5 MHz CLOCK FOR SERIAL TO PARALLEL CONVERTER AND AVERAGER
7 OUTPUT OF AVERAGER CLOCK COUNTER
8 SERIAL INPUT DATA
9 SUM OUTPUT FROM ONE BIT FULL ADDER
10 SERIAL RUNNING AVERAGE
11 CLOCK TICK (10 ms) [IR7]
12 PLAS - OUTPUT OF CHANNEL 3 OF COUNTER
13 END OF SWEEP [IR3]
14 CS16(L) CHIP SELECT FOR AMD 9513 COUNTER CHIP

continued opposite Fig. 9

1 BOARD : AB2

FUNCTION : 12.5 MHz CLOCK.

TEST POINT : PLAA
GROUND POINT : C15 (end adjacent to PCB edge)
SCOPE SETTING
MAIN TIMEBASE : 20 ns/DIV

PROCEDURE :

1. Check for clock period = 80 ns.

2 BOARD : AB2

FUNCTION : SYNCHRONIZED 'END OF CONVERSION'.

TEST POINT : PLAB
GROUND POINT : C15 (end of adjacent to PCB edge)
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE : 2 µs/DIV

PROCEDURE :

1. Press [PRESET].
Press 'horizontal sweep time [↑]' to select 2 sec/DIV sweep.
Check for pulse rep rate/period = 100 kHz/10 µs
pulse HIGH time = 800 ns
(pulse LOW time = 9.2 µs)
} During an active sweep.
Check for LOW (TTL) state if no sweep is taking place.

3 BOARD : AB2

FUNCTION : PLAC - OUTPUT FROM CH

TEST POINT : PLAC
GROUND POINT : C15 (end adjacent
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE : 2 µs/DIV

PROCEDURE :

1. Press [PRESET].
Press 'horizontal sweep tim
Check for : pulse rep rate/
pulse LO
(pulse HIG
Check for HIGH (TTL) state

2. Press 'horizontal sweep tim
Change scope main timebase
Check for : pulse rep rate/
HIGH, LOW puls

3. Press 'horizontal sweep tim
Check for pulse rep rate/pe
pulse LOW
pulse HIGH

4 BOARD : AB2

FUNCTION : STROBED 2.5 MHz-CLOC

TEST POINT : PLAD
GROUND POINT : C15 (end adjacent
SCOPE SETTING
CH2 : 2 V/DIV ON PLAB
TRIGGER : -ve, CH2

PROCEDURE :

1. Press [PRESET].
Press 'horizontal sweep tim
Check for a sequence of 23
10 µs, where pulse HIGH tim

Fig. 8A
Chap. 7
Page 18

e Fig. 9

3 BOARD : AB2

FUNCTION : PLAC - OUTPUT FROM CHANNEL 1 OF AMD 9513 COUNTER (IC20).

TEST POINT : PLAC
GROUND POINT : C15 (end adjacent to PCB edge)
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE : 2 µs/DIV

PROCEDURE :

1. Press [PRESET].
Press 'horizontal sweep time [↑]' to select 2 sec/DIV sweep.
Check for : pulse rep rate/period = 100 kHz/10 µs
pulse LOW time = 800 ns
(pulse HIGH time = 9.2 µs)
} During an active sweep.
Check for HIGH (TTL) state if no sweep in progress.

2. Press 'horizontal sweep time [↑]' to select 10 sec/DIV sweep.
Change scope main timebase to 5 µs/DIV.
Check for : pulse rep rate/period = 50 kHz/20 µs
HIGH, LOW pulse time = 10 µs.

3. Press 'horizontal sweep time [↑]' to select 20 sec/DIV sweep.
Check for pulse rep rate/period = 25 kHz/40 µs
pulse LOW time = 30 µs
pulse HIGH time = 10 µs.

5 BOARD : AB2

FUNCTION : AVERAGER CLOCK COUNTER OUTPUT

TEST POINT : PLAE
GROUND POINT : C12 (end adjacent to C11)
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET].
Press 'horizontal sweep time [↑]' t
Check for (TTL) pulse rep time = 5
pulse LOW time = 1.

6 BOARD : AB2

FUNCTION : GATED 2.5 MHz CLOCK FOR SERIAL

TEST POINT : PLAH
GROUND POINT : C15 (end adjacent to PCB e
SCOPE SETTING
CH2 : 2 V/DIV on PLAE
TRIGGER : -ve, CH2
MAIN TIMEBASE : 1 µs/DIV

PROCEDURE :

1. Press [PRESET].
Press 'horizontal video bandwidth [↑
After an intial (TTL) LOW period of
13 (HIGH) pulses.

4 BOARD : AB2

FUNCTION : STROBED 2.5 MHz-CLOCK.

TEST POINT : PLAD
GROUND POINT : C15 (end adjacent to PCB edge)
SCOPE SETTING
CH2 : 2 V/DIV ON PLAB
TRIGGER : -ve, CH2

PROCEDURE :

1. Press [PRESET].
Press 'horizontal sweep time [↑]' to select 2 s/DIV sweep.
Check for a sequence of 23 HIGH/LOW (TTL) pulses, which repeats every
10 µs, where pulse HIGH times = 200 ns.

7 BOARD : AB2

FUNCTION : OUTPUT OF AVERAGER CLOCK COUNT

TEST POINT : PLAJ
GROUND POINT : C15 (end adjacent to PCB e
SCOPE SETTING
CH2 : 2 V/DIV on PLAH
MAIN TIMEBASE : 1 µs/DIV

PROCEDURE :

1. Press [PRESET].
Press 'horizontal video bandwidth [↑
In the first 5 µs, CH1 (PLAJ) should
CH2 (PLAH) should
In the next 5 µs, CH1 (PLAJ) should
CH2 (PLAH) should
(That is, the counter controlling PL

UTPUT (VIDEO BANDWIDTH CONTROL).

C11)

tl' to select 2 s/DIV sweep.
= 5 ms
= 1.55 µsec.

ERIAL TO PARALLEL CONVERTER AND AVERAGER.

PCB edge)

dth [↑]' to select 50 kHz video bandwidth.
od of 5 µs, there should be a sequence of

COUNTER.

PCB edge)

ith [↑]' to select 50 kHz video bandwidth.
should be HIGH (TTL),
should be LOW (TTL).
ould be LOW (TTL),
ould have a sequence of 13 HIGH (TTL) pulses.
ng PLAJ is dividing by 13).

8 BOARD : AB2

FUNCTION : SERIAL INPUT DATA

TEST POINT : PLAK
EARTH POINT : C15 (end adjacent to PLB edge)
SCOPE SETTING
CH2 : 2 V/DIV ON PLAB
TRIGGER : -ve, CH2
MAIN TIMEBASE : 1 µs/DIV

PROCEDURE :

1. Press [PRESET]. Connect RF input to TG and press [TRACK GEN].
Press 'horizontal [METER]'.
Check for TTL pulse sequence repeating every 10 µs.

NOTE. It will not be possible to resolve the first 2 or 3 bits of each sequence, as these are the least significant bits of a 13 bit quantity coming from an A/D converter.

9 BOARD : AB2

FUNCTION : SUM OUTPUT FROM ONE BIT FULL ADDER.

TEST POINT : PLAL
GROUND POINT : C15 (end adjacent to PCB edge)
SCOPE SETTING
CH2 : 2V/DIV on PLAJ
TRIGGER : +ve, CH2
MAIN TIMEBASE : 1 µs/DIV

PROCEDURE :

1. Press [PRESET]. Press [TRACK GEN] (to activate tracking generator).
Connect tracking generator output to RF input. Press [ZERO SPAN].
On scope CH1 there should be a LOW (TTL) period of 5 µs, followed by a pulse sequence for 5 µs (each pulse 400 ns long).

NOTE. The first pulses will appear unresolved, as these are the least significant bits of a 13 bit A/D quantity.

10 BOARD : AB2

FUNCTION : SERIAL RUNNING AVERAGE.

TEST POINT : PLAM
GROUND POINT : C15 (end adjacent to PCB edge)
SCOPE SETTING
CH2 : 2V/DIV on PLAJ
TRIGGER : CH2
MAIN TIMEBASE : 2 µs/DIV

PROCEDURE :

1. Press [PRESET]. Connect tracking generator output to RF input.
Press '(horizontal video bandwidth [↑]' to select 25 kHz video bandwidth.
Press [TRACK GEN]. Press 'horizontal [METER]'.
Scope CH1 (PLAM) should show an initial LOW (TTL) period of 15 µs, followed by a serial pulse sequence for 5 µs.

NOTE. It will not be possible to resolve the first bits of the sequence, as these are the least significant bits of 13 A/D quantity.

11 BOARD : AB2

FUNCTION : CLOCK TICK (10 ms) [IR7].

TEST POINT : PLAP
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE : 1 ms/DIV

PROCEDURE :

1. Check for a LOW (TTL) pulse (length 800 ns) every 10 ms.

every 10 ms.

12 BOARD : AB2

FUNCTION : PLAS - OUTPUT OF CHANNEL 3 OF COUNTER.

TEST POINT : PLAS
GROUND POINT : C19 (end adjacent to C18)
SCOPE SETTING
MAIN TIMEBASE : 20 µs/DIV

PROCEDURE :

1. Press [PRESET].
Check for HIGH (TTL) pulses (10 µs long) occurring every 200 µs.

2. Press 'horizontal sweep time [t]' to select 20 ms/DIV. The pulses described above should now be occurring every 400 µs.

13 BOARD : AB2

FUNCTION : END OF SWEEP [IR3].

TEST POINT : PLAT
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
TRIGGER : -ve, manual, CH1
MAIN TIMEBASE : 50 µs/DIV

PROCEDURE :

1. Press [PRESET].
Check for LOW (TTL) pulses (200 µs long) every 180 ms (approx.).

14 BOARD : AB2

FUNCTION : CS16(L) CHIP SELECT FOR AMD 9513 COUNTER CHIP.

TEST POINT : PLBP
GROUND POINT : C40 (end adjacent to C39)
SCOPE SETTING
TRIGGER : -ve, manual, dc
MAIN TIMEBASE : 200 ns/DIV

NOTE. Use scope hood or storage scope.

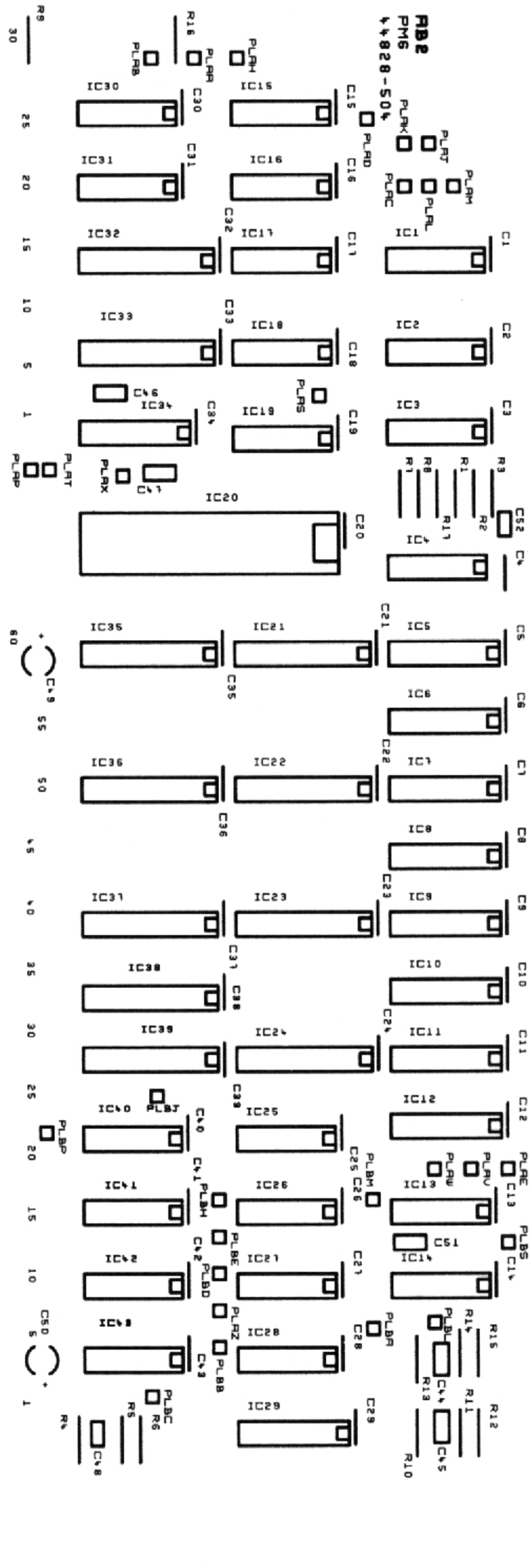
PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain scope display.
(If this is difficult, put CH1 probe on PLAB to adjust trigger level.)
Check for LOW (TTL) pulses, approx. 500 ns long.

Waveforms for AB2

Fig. 8B

May 86



Component layout for AB2

Fig. 8
May 86

PART OF AB 2 44828-504M

FROM RF UNITS AA1 PLA 6

PLB 20b

SERIAL INPUT DATA

8 PLAK

ONE BIT FULL ADDER

IC1(a) LS86

IC1(b) LS86

SUM

PLAL 9

SERIAL-TO-PARALL

IC3(a) LS08

IC2(b) LS32

IC18(b) LS74

+5V

IC17 LS164

D12

D5

IC2(a) LS32

IC3(d) LS08

CARRY OUT

CARRY IN

SERIAL RUNNING AVERAGE

FROM * AC0

1a, 1b, 2a, 2b

C50 33 µ

+5V

59a, 59b, 60a, 60b

C49 33 µ

4b, 5b, 6b, 8b

9b, 10b, 11b, 12b

50b, 51b, 52b, 53b

54b, 55b, 56b, 57b

ALL IC'S DECOUPLED AT +5V PIN TO GROUND RAIL WITH 10n CAPACITOR

SUPPLY LINE TABLE					
IC	+5V	GROUND	IC	+5V	GROUND
IC1	14	7	IC22	20	10
IC2	14	7	IC23	20	10
IC3	14	7	IC24	20	10
IC4	14	7	IC25	14	7
IC5	16	8	IC26	14	7
IC6	16	8	IC27	14	7
IC7	16	8	IC28	14	7
IC8	16	8	IC29	16	8
IC9	16	8	IC30	5	10
IC10	16	8	IC31	5	10
IC11	16	8	IC32	20	10
IC12	16	8	IC33	20	10
IC13	14	7	IC34	16	8
IC14	14	7	IC35	20	10
IC15	14	7	IC36	20	10
IC16	14	7	IC37	20	10
IC17	14	7	IC38	20	10
IC18	14	7	IC39	20	10
IC19	14	7	IC40	14	7
IC20	1	21	IC41	14	7
IC21	20	10	IC42	14	7
			IC43	14	7

SERIAL DATA STROBE GEN ÷5

1 PLAA

2 PLAB

IC30 LS90

STROBED 2·5MHz

4 PLAD

IC3(c) LS08

PLAC 3

INPUT WORD RATE DIVIDER

IC19(b) LS74

IC20 9513

IC2(b) LS32

IC18(a) LS74

IC3(b) LS08

AB7 PLB 12a

12·5MHz CLOCK

AVERAGER CLOCK COUNTER ÷D

7 PLAJ

IC20 9513

IN OUT

6 PLAH

IC4(a) LS04

R2 2k2

R1 2k2

5 PLAE

C52 470p

R3 8k2

FROM S

FORCE EOC

IC42(c) LS32

FROM RF UNITS AA1 PLA 5

PLB 19b

IC4(c) LS04

END OF CONVERSION

÷10 ÷5 ÷2

µP REAL TIME CLOCK GEN.

11

IC31 LS90

12·5MHz

1·25MHz

IC20 9513

PLAP

R16 2k2

IC20 9513

X2 IN OUT GATE

R7 2k

PLA 12

÷2

IC29 LS112

6·25MHz CLOCK

CLOCK TICK (10mS) [1R7]

IC25(a) LS74

R5 2k2

R4 2k2

C48 470p

R6 8k2

PLB 11a

24b

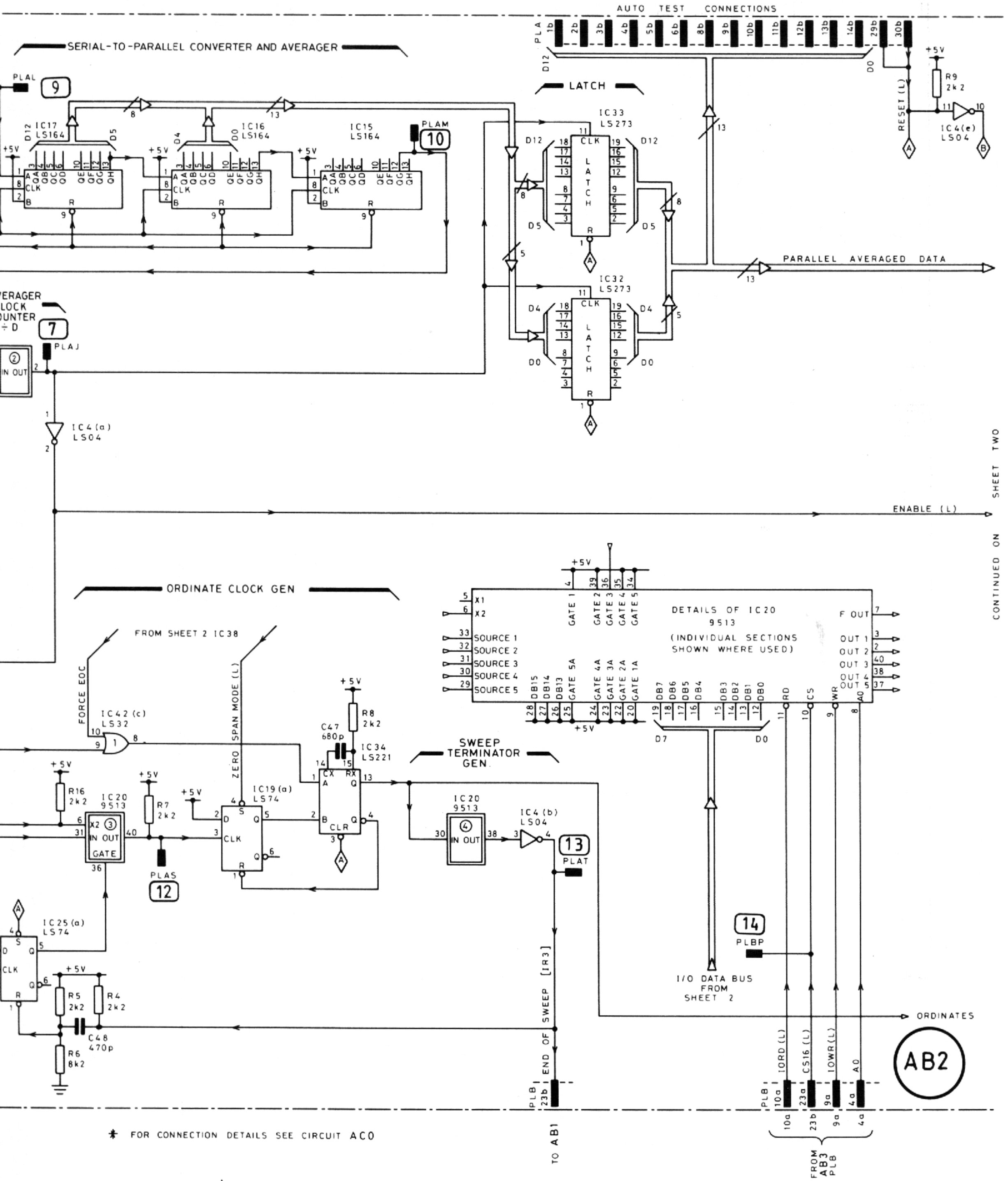
TO AB1

TO AB1

* FOR CON

Drg. No. Z44828-504M
Sh. 1 Iss. 2

AB2: Input signal data proc



gnal data processing

BOARD : AB2
KEY OF FUNCTIONS (concluded)

15 MAX DATA LATCHES CLOCK CONTROL (OF DISPLAY DETECTOR BLOCK)
16 MIN DATA LATCHES CLOCK CONTROL (OF DISPLAY DETECTOR BLOCK)
17 CLOCK INPUT TO DISPLAY DETECTORS
18 OUTPUT OF DETECTOR MAX LATCH
19 OUTPUT OF DETECTOR MIN LATCH
20 OUTPUT OF DETECTOR MIN LATCH
21 OUTPUT OF DETECTOR MIN LATCH
22 OUTPUT OF DETECTOR MIN LATCH
23 DACKØ(L). IORD(L) - DMA READ PULSES WHICH TRANSFER DATA FROM DISPLAY DETECTOR TO SCREEN MEMORY
24 DRQØ - DMA REQUEST FOR DISPLAY UPDATE
25 SELECT HIGH BYTE (L) (FOR DMA FROM DISPLAY DETECTOR TO SCREEN MEMORY)
26 SELECT LOW BYTE (L) (FOR DMA FROM DISPLAY DETECTOR TO SCREEN MEMORY)
27 'NEW MAXIMUM DETECT' CONTROL (IN DISPLAY DETECTOR)
28 'NEW MINIMUM DETECT' CONTROL (IN DISPLAY DETECTOR)
29 PART OF MAX DATA LATCH INITIALIZATION LOGIC OF DISPLAY DETECTOR BLOCK
30 CSIE(L)

15 BOARD : AB2

FUNCTION : MAX DATA LATCHES CLOCK CONTROL (OF DISPLAY DETECTOR BLOCK).

TEST POINT : PLAV
GROUND POINT : C12 (end adjacent to C11)
SCOPE SETTING
CH2 : 2 V/DIV on IC41 pin 8
TRIGGER : +ve, CH2, manual, dc
MAIN TIMEBASE : 200 ns/DIV
MODE : CH1 only

NOTE. Use a scope hood, or else a storage scope.

PROCEDURE :

1. Press [PRESET]. Use controls to select video bandwidth = 50 kHz, filter bandwidth = 100 Hz and sweep time = 2s/DIV. (This should give a very noisy spectrum display.)
Adjust the scope trigger level to get a scope display (if this is difficult, temporarily put CH2 scope probe on PLAB for trigger level adjust).
Check for a HIGH (TTL) pulse (length approx. 100ns) occurring 1 µs after the trigger.

2. Move CH2 scope probe to PLBM. Check CH1 for a HIGH (TTL) pulse (length approx. 80 ns) occurring within 100 µs of the trigger.

16 BOARD : AB2

FUNCTION : MIN DATA LATCHES CLOCK

TEST POINT : PLAW
GROUND POINT: C12 (end adjacent to
SCOPE SETTING
CH2 : 2 V/DIV on PLBH
TRIGGER : -ve, CH2, manual, d
MAIN TIMEBASE : 200 ns/DIV
MODE : CH1 only

NOTE. Use a scope hood, or

PROCEDURE :

1. Press [PRESET]. Use control
filter bandwidth = 100 Hz, sw
(This should give a very 'noi
Adjust the scope trigger leve
temporarily put CH2 probe on
Check for a HIGH (TTL) pulse
the trigger.

2. Move CH2 scope probe to PLBL.
occurring within 100 ns of th

17 BOARD : AB2

FUNCTION : CLOCK INPUT TO DISPLAY

TEST POINT : PLAX
GROUND POINT : C34 (end adjacent t
SCOPE SETTING
CH2 : 2V/DIV on PLBH
TRIGGER : -ve, CH2, manual, d
MAIN TIMEBASE : 500 ns/DIV

NOTE. Use a scope head or s

PROCEDURE :

1. Press [PRESET]. Use control
filter bandwidth = 100 Hz, sw
a very 'noisy' display.)
Adjust the scope trigger leve
difficult, temporarily put CH
Check for a LOW (TTL) pulse (
trigger.

16 BOARD : AB2

FUNCTION : MIN DATA LATCHES CLOCK CONTROL (OF DISPLAY DETECTOR BLOCK).

TEST POINT : PLAW
GROUND POINT: C12 (end adjacent to C11)
SCOPE SETTING
CH2 : 2 V/DIV on PLBH
TRIGGER : -ve, CH2, manual, dc
MAIN TIMEBASE : 200 ns/DIV
MODE : CH1 only

NOTE. Use a scope hood, or storage scope.

PROCEDURE :

1. Press [PRESET]. Use controls to select video bandwidth = 50 kHz, filter bandwidth = 100 Hz, sweep time = 2 s/DIV. (This should give a very 'noisy' spectrum display.) Adjust the scope trigger level to get a scope display (if this is difficult, temporarily put CH2 probe on PLAB for setting trigger level). Check for a HIGH (TTL) pulse (length approx. 100 ns) occurring 1 µs after the trigger.

2. Move CH2 scope probe to PLBL. Check CH1 for a HIGH (TTL) pulse (80 ns long) occurring within 100 ns of the trigger.

17 BOARD : AB2

FUNCTION : CLOCK INPUT TO DISPLAY DETECTORS.

TEST POINT : PLAX
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2V/DIV on PLBH
TRIGGER : -ve, CH2, manual, dc
MAIN TIMEBASE : 500 ns/DIV

NOTE. Use a scope head or storage scope.

PROCEDURE :

1. Press [PRESET]. Use controls to select video bandwidth = 50 kHz, filter bandwidth = 100 Hz, sweep time = 2 s/DIV. (This should give a very 'noisy' display.) Adjust the scope trigger level to get a scope display (if this is difficult, temporarily put CH2 probe on PLAB to set trigger level). Check for a LOW (TTL) pulse (200 ns long) occurring 1 µs after the trigger.

18 BOARD : AB2

FUNCTION : OUTPUT OF DETECTOR MAX LATCH.

TEST POINT : PLAZ
GROUND POINT : C42 (end adjacent to C41)
SCOPE SETTING
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Press 'horizontal s
Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access' (for upp
Select [1] 'enter upper unit I/O port
'Enter port number [HEX] =' [1 E] [-]
'Enter port value [BIN] =' [0 0 0 0 0

2. Check for scope CH1 giving random TTL
Press 'horizontal sweep mode [START].
Press [-] ('minus' key).

3. Check that scope CH1 now remains (TTL
next sweep.

19 BOARD : AB2

FUNCTION : OUTPUT OF DETECTOR MIN LATCH.

TEST POINT : PLBA
GROUND POINT : C28 (end adjacent to C27)
SCOPE SETTING
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Press 'horizontal s
Enter DEBUG OPERATIONS mode.
Select [1] - 'I/O port access' (for u
select [1] - 'enter upper unit I/O po
'Enter port number [HEX] =' [1 E] [-]
'Enter port value [BIN] =' [0 0 0 0

2. Check for scope CH1 giving random TTL
Press 'horizontal sweep mode [START]'
Press [-] ('minus' key).

3. Check that scope CH1 now remains LOW
next sweep.

TCH.

C41)

ntal sweep time [↑]' to select 5 s/DIV.

or upper unit).
O port parameters'.
E] [-].
0 0 0 0 1 0].

om TTL HIGHS and LOWS.
TART].

s (TTL) HIGH until the beginning of the

20 BOARD : AB2

FUNCTION : OUTPUT OF DETECTOR MIN LATCH.

TEST POINT : IC26 pin 1
GROUND POINT : C26 (end adjacent to C25)
SCOPE SETTING
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Press 'horizontal sweep time [↑]' to select 5s/DIV.
Enter DEBUG OPERATIONS mode.
Select [1] - 'I/O port access' (for upper & lower units), then
select [1] - 'enter upper unit I/O port parameters'.
'Enter port number [HEX] =' [1 E] [-].
'Enter port value [BIN] =' [0 0 0 0 0 0 1 0].

2. Check for scope CH1 giving random TTL HIGH and LOW states.
Press 'horizontal sweep mode [START]'.
Press [-] ('minus' key).

3. Check that scope CH1 now remains LOW (TTL) until the beginning of the next sweep.

TCH.

C27)

tal sweep time [↑]'to select 5 s/DIV.

for upper & lower units) , then
I/O port parameters'.
E] [-].
0 0 0 0 1 0].

m TTL HIGH and LOW states.
ART]'.

LOW (TTL) until the beginning of the

21 BOARD : AB2

FUNCTION : OUTPUT OF DETECTOR MIN LATCH.

TEST POINT : PLBB
GROUND POINT : C43 (end adjacent to C42)
SCOPE SETTING
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Press 'horizontal sweep time [↑]' to select 5 s/DIV.
Enter DEBUG OPERATIONS mode.
Select [1] - 'I/O port access' (for upper & lower units), then
select [1] - 'enter upper unit I/O port parameters'.
'Enter port number [HEX] =' [1 E] [-].
'Enter port value [BIN] =' [0 0 0 0 0 0 1 0].

2. Check for scope CH1 giving random TTL HIGH and LOW states.
Press 'horizontal sweep mode [START]'.
Press [-] ('minus' key).

3. Check that scope CH1 now remains LOW (TTL) until the beginning of the next sweep.

Fig. 9A

May 86

22 BOARD : AB2

FUNCTION : OUTPUT OF DETECTOR MIN LATCH

TEST POINT : PLBC
GROUND POINT : C43 (end adjacent to C42)
SCOPE SETTING
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Press 'horizontal sweep time [↑]' to select 5 s/DIV.
Enter DEBUG OPERATIONS mode.
Select [1] - 'I/O port access' (for upper & lower units), then
select [1] - 'enter upper unit I/O port parameters'.
'Enter port number [HEX] =' [1 E] [-].
'Enter port value [BIN] =' [0 0 0 0 0 0 1 0].

2. Check for scope CH1 giving random TTL HIGH and LOW states.
Press 'horizontal sweep mode [START].
Press [-] ('minus' key).

3. Check that scope CG1 now remains HIGH (TTL) until the beginning of the next sweep.

23 BOARD : AB2

FUNCTION : DACKØ(L). IORD(L) - DATA READ PULSES WHICH TRANSFER DATA FROM DISPLAY DETECTOR TO SCREEN MEMORY.

TEST POINT : PLBD
GROUND POINT : C43 (end adjacent to C42)
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for two LOW (TTL) pulses paired together.
Pulse LOW time = 900 ns (±100 ns)
Inter-pulse separation = 500 ns (±100 ns).

24 BOARD : AB2

FUNCTION : DRQØ - DMA REQUEST FOR DISPLAY UP

TEST POINT : PLBE
GROUND POINT : C42 (end adjacent to C41)
SCOPE SETTING [DEFAULT]

PROCEDURE :

1. Press [PRESET]. Press 'horizontal swe
Check for a HIGH (TTL) pulse occurring
pulse will vary between 2 µs and approx

25 BOARD : AB2

FUNCTION : SELECT HIGH BYTE (L) (FOR DMA FRO

TEST POINT : PLBH
GROUND POINT : C41 (end adjacent to C40)
SCOPE SETTING
CH2 : 2 V/DIV on PLBD
TRIGGER : -ve, manual, CH2
MAIN TIMEBASE : 500 ns/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger
Check CH1 (scope) for LOW (TTL) pulse (
the trigger.

26 BOARD : AB2

FUNCTION : SELECT LOW BYTE (L) (FOR DMA FROM

TEST POINT : PLBJ
GROUND POINT : C40 (end adjacent to C39)
SCOPE SETTING
CH2 : 2 V/DIV on PLBD
TRIGGER : -ve, manual, CH2
MAIN TIMEBASE : 500 ns/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger
Check CH1 (scope) for LOW (TTL) pulse (
after the trigger.

Fig. 9B
Chap. 7
Page 24/23

24 BOARD : AB2

FUNCTION : DRQϕ - DMA REQUEST FOR DISPLAY UPDATE.

TEST POINT : PLBE
GROUND POINT : C42 (end adjacent to C41)
SCOPE SETTING [DEFAULT]

PROCEDURE :

1. Press [PRESET]. Press 'horizontal sweep time [↑]' to select 500 ms/DIV. Check for a HIGH (TTL) pulse occurring every 10 ms; the length of the pulse will vary between 2 µs and approx. 7 µs.

25 BOARD : AB2

FUNCTION : SELECT HIGH BYTE (L) (FOR DMA FROM DISPLAY DETECTOR TO SCREEN MEMORY).

TEST POINT : PLBH
GROUND POINT : C41 (end adjacent to C40)
SCOPE SETTING
CH2 : 2 V/DIV on PLBD
TRIGGER : -ve, manual, CH2
MAIN TIMEBASE : 500 ns/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain scope display. Check CH1 (scope) for LOW (TTL) pulse (900 ns long) occurs 1.5 µs after the trigger.

26 BOARD : AB2

FUNCTION : SELECT LOW BYTE (L) (FOR DMA FROM DIAPLAY DETECTOR TO SCREEN MEMORY).

TEST POINT : PLBJ
GROUND POINT : C40 (end adjacent to C39)
SCOPE SETTING
CH2 : 2 V/DIV on PLBD
TRIGGER : -ve, manual, CH2
MAIN TIMEBASE : 500 ns/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain display. Check CH1 (scope) for LOW (TTL) pulse (900 ns long), occurring 1.5 µs after the trigger.

27 BOARD : AB2

FUNCTION : 'NEW MAXIMUM DETECT' CONTROL (IN DISPLAY D

TEST POINT : PLBM
GROUND POINT : C26 (end adjacent to C25)
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 200 µs/DIV

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to
Check for LOW (TTL) pulses (80 ns long ±30 ns).

2. Connect RF input to tracking generator, and pres
Press 'vertical [↓]'to obtain -80 dBm at top of

NOTE. Spectrum display should be compressed in
top of display.

Check that pulses described above are no longer
checked by setting scope to single sweep, and wa
status indicator to see if it finds a pulse to t

28 BOARD : AB2

FUNCTION : 'NEW MINIMUM DETECT' CONTROL (IN DISPLAY D

TEST POINT : PLBL
GROUND POINT : C28 (end adjacent to C27)
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 200 ns/DIV

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to
Check for LOW (TTL) pulses (80 ns long, ±30 ns).

2. Connect RF input to tracking generator, and pres
Press 'vertical [↓]' to obtain -80 dBm at top of

NOTE. Spectrum should be compressed into a str

Check that pulses described above are no longer
checked by setting scope to single sweep, and wa
status indicator to see if it finds a trigger pu

PLAY DETECTOR).

el to obtain display.
ns).

d press [TRACK GEN].
op of display.

sed into a straight line at

onger present. (This may be
and watching the scope sweep
e to trigger from.)

29 BOARD : AB2

FUNCTION : PART OF MAX DATA LATCH INITIALIZATION LOGIC OF DISPLAY DETECTOR BLOCK.

TEST POINT : IC41 pin 8.
GROUND POINT : C41 (end adjacent to C40)
SCOPE SETTING
CH2 : 2 V/DIV on IC39 pin 1
TRIGGER : -ve, CH2, manual, dc
MAIN TIMEBASE : 200 ns/DIV
MODE : CH1 only

NOTE. You will need a scope hood, or else a storage scope.

PROCEDURE :

1. Press [PRESET]. Use controls to select video bandwidth = 50 kHz, filter bandwidth = 100 Hz and sweep time = 2 s/DIV, which should give a very 'noisy' spectrum display.

2. Adjust scope trigger level to get a scope display (if this is difficult, temporarily put CH2 probe on PLAB and then adjust trigger level).

3. Check for a HIGH (TTL) pulse (length approx. 1 μs).

4. Press 'horizontal [ZERO SPAN]', and the pulse should disappear, leaving CH1 at a (TTL) HIGH state.

PLAY DETECTOR).

el to obtain display.
0 ns).

d press [TRACK GEN].
top of display.

a straight line at top of display.

onger present (this may be
and watching the scope sweep
ger pulse).

30 BOARD : AB2

FUNCTION : CSIE(L)

TEST POINT : PLBS
GROUND POINT : C14 (end adjacent to C13)
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 200 ns/DIV

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Set scope trigger level to obtain display.
(If this is difficult, put scope CH1 probe on PLAB to set trigger level.)
Check for LOW (TTL) pulses on PLBS (500 ns long).

PART OF
AB 2
44828 - 504M

MAX DATA IDENTIFY
IC13(a) LS00
27 PLBM
DISPLAY DETECTOR FORCE MAX (L)
IC12 LS85
IC11 LS85
IC10 LS85
IC9 LS85
IC8 LS85
IC7 LS85
IC6 LS85
IC5 LS85
+5V
D12
D0
PARALLEL AVERAGED DATA
SHEET ONE
CONTINUED FROM
ENABLE (L)
MIN DATA IDENTIFY
IC13(d) LS00
IC13(b) LS00
IC13(c) LS00
PLAV
15
MAX DATA LATCHES
IC24 LS273
IC23 LS273
IC22 LS273
IC21 LS273
CLK
LATCH
R12 8k2
R11 2k2
R10 2k2
C45 180p
IC41(c) LS00
ZERO SPAN MODE (L)
TO SHEET 1 IC19 PIN 4
29
IC26(c) LS04
IC27(c) LS08
DETECTOR MAX LATCH
18
IC14(a) LS74
PLAZ
MAX/MIN LATCH SE
IC27(a) LS08
IC26(a) LS04
20
19
PLBA
IC29(a) LS112
IC27(b) LS08
28 PLBL
C51 68p
R14 2k2
R13 2k2
C44 180p
R15 8k2
IC26(f) LS04
C46 120p
IC34a LS221 6
R17 2k2
DETECTOR MIN LATCH
IC14(b) LS74
PLAX
17
HIGH/LOW BY
23
PLBD
16 PLAW
IC41(b) LS00
IC25(b) LS74
IC26(b) LS04
'ORDINATES' FROM SHEET 1
MIN LATCH BUS
IC4(f) LS04
PLB 20a DACK 0 (L) IORD (L)
FROM AB3 PLB 20b

Drg. No. Z44828-504M
Sh. 2 Iss. 1

AB2 : Input signal data processing

FROM AB3 PLB 24b

IPLB 24a

CS1E (L)

PLBS 30

IC38 LS273

MAX/MIN LATCH SELECT LOGIC

IC26 (a) LS04

20

IC28 (d) LS32

IC29 (a) LS112

IC27 (b) LS08

PLBB 21

+5V

IC43 (a) LS74

IC40 (b) LS32

IC40 (a) LS32

MAX OUTPUT LATCHES

IC39 LS374

IC37 LS374

IC36 LS374

IC35 LS374

FORCE EOC

TO SHEET 1 IC42 PIN 10

I/O DATA BUS

MAX LATCH BUS

PLBJ 26

PLBH 25

PLBC 22

HIGH/LOW BYTE SELECT GEN

23

PLBD

IC43 (b) LS74

IC42 (a) LS32

SELECT LOW BYTE (L)

IC42 (b)

SELECT HIGH BYTE (L)

DRQ LATCH

IC41 (a) LS00

IC41 (b) LS00

IC41 (d) LS00

IC25 (b) LS74

IC40 (c) LS32

IC40 (d) LS32

I/O DATA BUS TO SHEET 1

MIN OUTPUT LATCHES

PLBE 24

IC4 (f) LS04

MISS FIRST ORDINATE

DACK 0 (L) IORD (L)

DRQ 0

PLB 20a

PLB 19a

FROM AB3 PLB 20b

TO AB3

PLB 57a 56a 55a 54a 53a 52a 61a 50a

TO AB3

CS10 (L) 15a 15b

CS1A (L) 16a 16b

CS1C (L) 17a 17b

CS2 (L) 18a 18b

LOW 5V LINE (L) 21a 21b

CS0X (L) 25a 25b

INT 26a 26b

INTA (L) 27a 27b

SPARE 1 28a 28b

BREAK 29a 29b

PCLK 30a 30b

AB2

BOARD : AB3
KEY OF FUNCTIONS

1 PCLK - 2.83 MHz TTL CLOCK
2 WR(L) - WRITE CONTROL SIGNAL
3 RD(L) - READ CONTROL SIGNAL
4 ALE - ADDRESS LATCH ENABLE
5 IO/$\overline{M}$
6 INTA(L) - INTERRUPT ACKNOWLEDGE
7 RESET
8 HOLDA - HOLD BUS ACKNOWLEDGE
9 MWR(L).MRD(L) - TTL BUFFER CONTROL (goes low for a memory read or write)
10 IOEN(L) - I/O ENABLE, GOES LOW FOR ANY I/O ACCESS
11 +AEN - ACCESS ENABLE FOR DMA

+ printed alongside Fig. 11

1 BOARD : AB3

FUNCTION : PCLK - 2.83 MHz TTL CLOCK.

TEST POINT : PLX1
GROUND POINT : C16 (end adjacent to PLX1)
SCOPE SETTING
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET].
Check for TTL clock, period = 480 ns,
clock HIGH = clock LOW = 240 ns.

2 BOARD : AB3

FUNCTION : WR(L) - WRITE CONTROL SIGNAL.

TEST POINT : PLX3
GROUND POINT : C16 (end adjacent to PLX1)
SCOPE SETTING
CH2 : 2 V/DIV on PLG link (keep link on)
TRIGGER : -ve
MAIN TIMEBASE : 200 ns/DIV

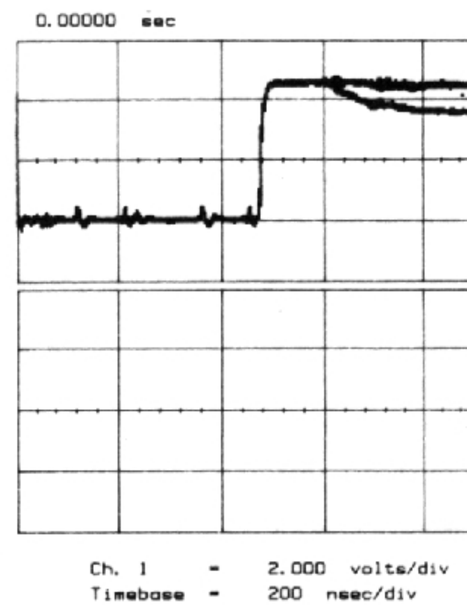
PROCEDURE :

1. Press [PRESET]. Check for LOW (TTL) pulses 480 ns long.
Time between pulses is irregular, but always an integral number of 480 ns periods (similar to AB3/PLX2 waveform diagram).

2. Change SCOPE TRIGGER to CH2, +ve. Check CH1 waveform stays (TTL) HIGH for at least 3 µs from trigger.

3 BOARD : AB3

FUNCTION : RD(L) - READ CONTROL SI



TEST POINT : PLX2
GROUND POINT : C16 (end adjacent t
SCOPE SETTING
CH2 : 2 V/DIV on PLG link or
TRIGGER : -ve, CH1
MAIN TIMEBASE : 200 ns/DIV
MODE : CH1 only

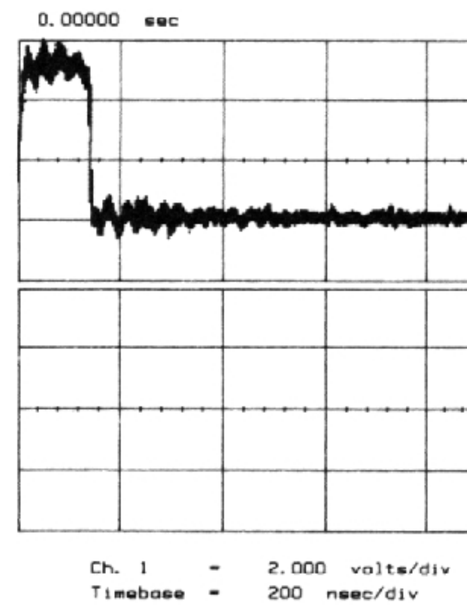
PROCEDURE :

1. Press [PRESET]. Check for
Pulse spacing is an integral
(this varies from one pulse

2. Change SCOPE TRIGGER to +ve,
CH1 waveform is (TTL) HIGH fo

4 BOARD : AB3

FUNCTION : ALE - ADDRESS LATCH ENA



TEST POINT : PLC link (keep link o
GROUND POINT : C16 (end adjacent t
SCOPE SETTING
CH2 : 2 V/DIV on PLG link (ke
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for H
repetition is irregular, but
(minimum 960 ns) - see wavefo

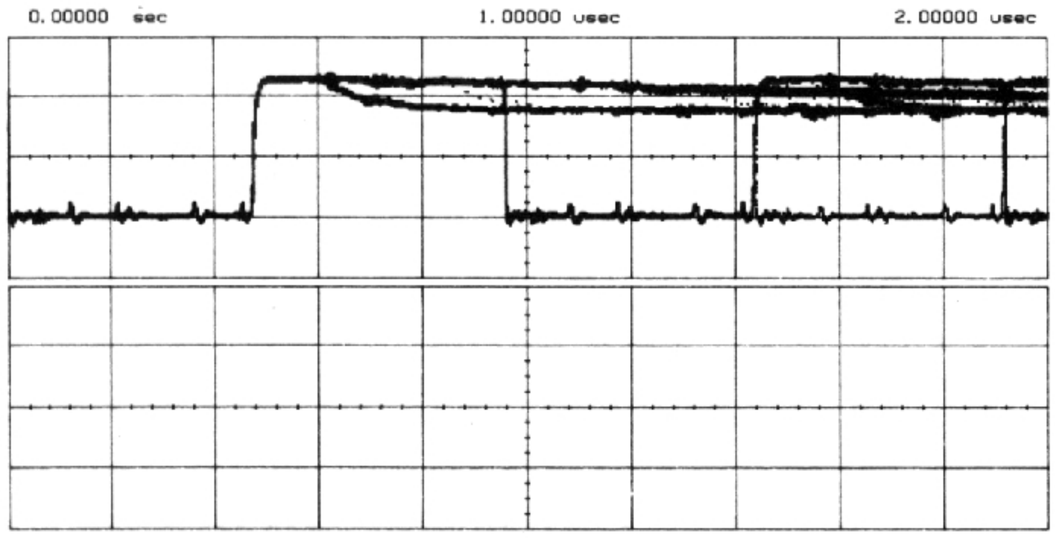
2. Change SCOPE TRIGGER to CH2,
Check CH1 waveform is (TTL) L

Fig. 10A
Chap. 7
Page 26

te)

3 BOARD : AB3

FUNCTION : RD(L) - READ CONTROL SIGNAL.



TEST POINT : PLX2
GROUND POINT : C16 (end adjacent to PLX1)
SCOPE SETTING
CH2 : 2 V/DIV on PLG link or IC15 pin 30 (keep link on)
TRIGGER : -ve, CH1
MAIN TIMEBASE : 200 ns/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Check for multiple LOW (TTL) pulses, length 480 ns. Pulse spacing is an integral number of 480 ns periods (minimum 480 ns) (this varies from one pulse to the next - see waveform diagram CH2).
2. Change SCOPE TRIGGER to +ve, CH2, MAIN TIMEBASE to 500 ns/DIV, check that CH1 waveform is (TTL) HIGH for at least 3 µs after the trigger.

5 BOARD : AB3

FUNCTION : IO/$\overline{M}$.

TEST POINT : PLX5
GROUND POINT : C16 (end adjacent to PLX1)
SCOPE SETTING
CH2 : 2 V/DIV on PLG link (keep link
MAIN TIMEBASE : 200 ns/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Check that CH1 show LOW states.
2. Change SCOPE TRIGGER to CH2. Check for at least 3 µs from the trigger.

6 BOARD : AB3

FUNCTION : INTA(L) - INTERRUPT ACKNOWLEDGE

TEST POINT : PLX6
GROUND POINT : C16 (end adjacent to PLX1)
SCOPE SETTING
TRIGGER : -ve, manual, dc
MAIN TIMEBASE : 200 ns/DIV

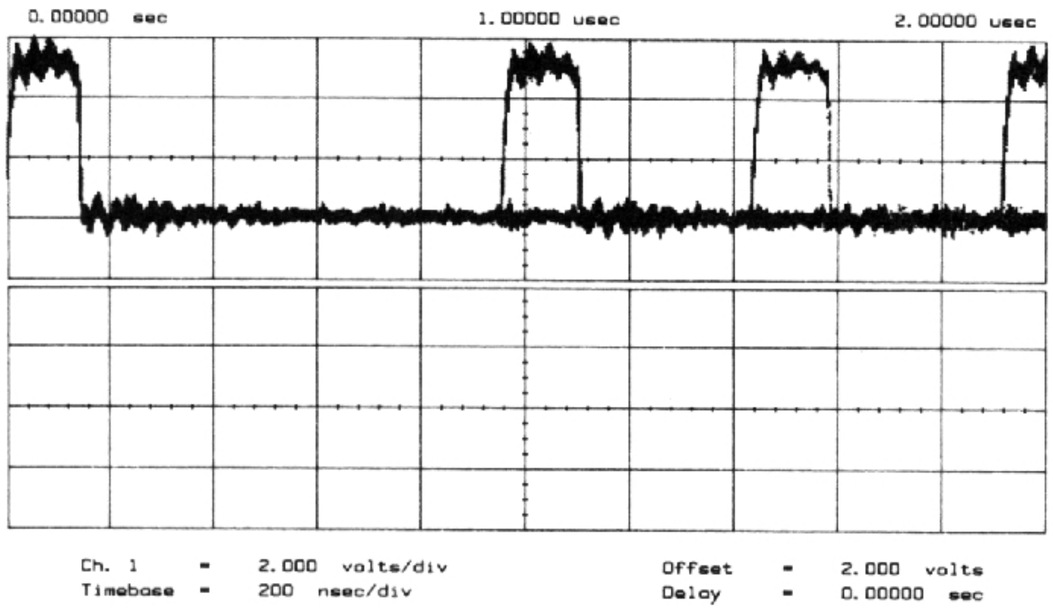
NOTE. Use scope hood or storage sc

PROCEDURE :

1. Press [PRESET]. Adjust scope trigge difficult move CH1 probe to PLX1 to s Check for 2 LOW (TTL) pulses on PLX6, pulse LOW time = 480 ns, pulse pair spacing = 480 ns.

4 BOARD : AB3

FUNCTION : ALE - ADDRESS LATCH ENABLE.



TEST POINT : PLC link (keep link on) (or IC23 pin 11)
GROUND POINT : C16 (end adjacent to PLX1)
SCOPE SETTING
CH2 : 2 V/DIV on PLG link (keep link on)
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for HIGH (TTL) pulses 160 ns long. Pulse repetition is irregular, but always an integral number of 480 ns periods (minimum 960 ns) - see waveform diagram.
2. Change SCOPE TRIGGER to CH2, MAIN TIMEBASE to 500 ns/DIV. Check CH1 waveform is (TTL) LOW for at least 3 µs after the trigger.

7 BOARD : AB3

FUNCTION : RESET.

TEST POINT : PLX4
GROUND POINT : C16 (end adjacent to PLX1)
SCOPE SETTING
MAIN TIMEBASE : 1 ms/DIV

PROCEDURE :

1. Observe scope CH1 display as the 238 a momentary HIGH (TTL) pulse just af repeated when the unit is switched o

PLX1)

link on)

shows a random series of (TTL) HIGH and

Check that scope CH1 waveform is (TTL) HIGH
ger.

LEDGE.

PLX1)

ge scope.

trigger to obtain display (if this is
to set trigger level).
PLX6,
,
.

PLX1)

e 2380 is switched on. There should be
st after switching on. (This pulse is
hed off.)

8 BOARD : AB3

FUNCTION : HOLDA - HOLD BUS ACKNOWLEDGE.

TEST POINT : PLG link
GROUND POINT : C16 (end adjacent to PLX1)
SCOPE SETTING
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for HIGH (TTL) pulses, at least 2.88 µs long (length will vary from one pulse to the next).

9 BOARD : AB3

FUNCTION : MWR(L).MRD(L) - TTL BUFFER CONTROL
(goes low for a memory read or write).

TEST POINT : PLL
GROUND POINT : C25 (end nearest IC24)
SCOPE SETTING
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET].
Check for 'random' TTL HIGH and LOW pulses.

10 BOARD : AB3

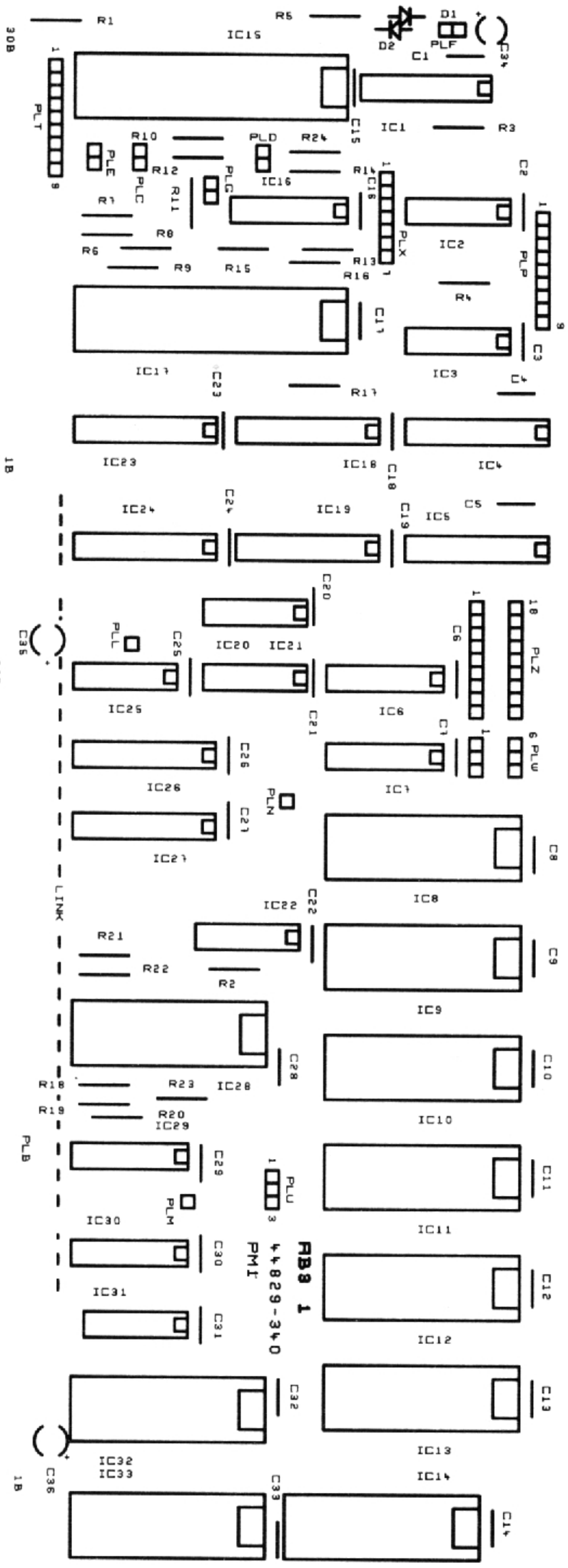
FUNCTION : IOEN(L) - I/O ENABLE, GOES LOW FOR ANY I/O ACCESS.

TEST POINT : PLM
GROUND POINT : C30 (end adjacent to C29)
SCOPE SETTING
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET].
Check for a random TTL pulse train of HIGH and LOW states.

Fig. 10A



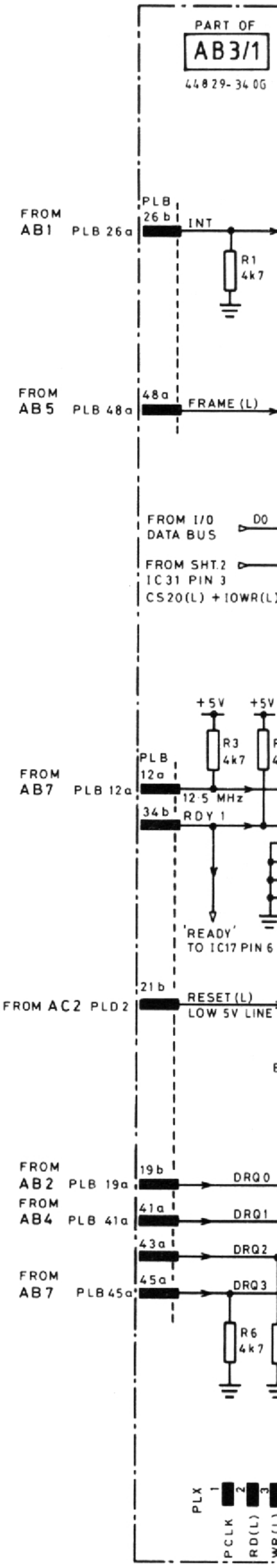


Fig. 10
May 86

Component layout for AB3/1

PART OF
AB3/1
44829-340G

MICROPROCESSOR
IC15
8088

NMI CONTROL

DMA
CONTROLLER

ADDRESS BUS (HIGH BYTE)

'READY'
TO IC17 PIN 6

'READY' FR
IC1 PIN 4

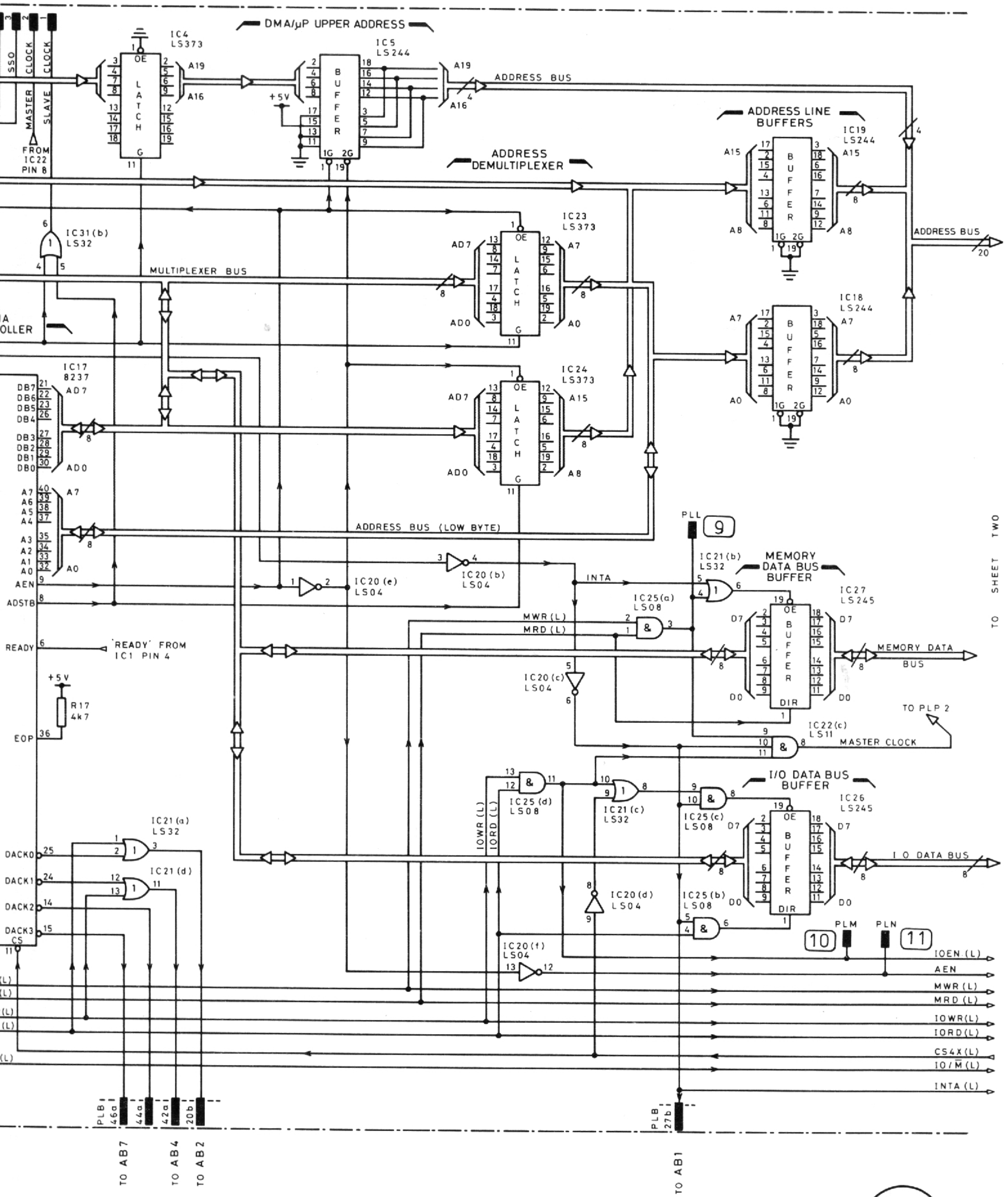
MUL

TO AB1

TO AB7

Drg. No. Z 44829-340G
Sh. 1 Iss. 1

AB3/1 : Processor mem



: Processor memory & chip select

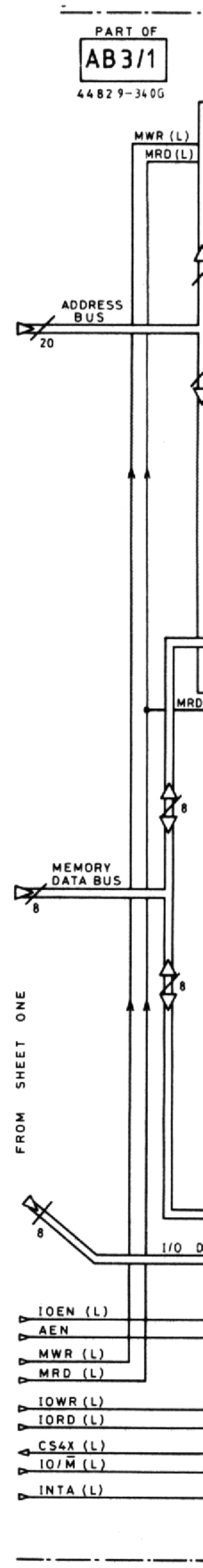
11 BOARD : AB3

FUNCTION : AEN - ACCESS ENABLE FOR DMA.

TEST POINT : PLN
GROUND POINT : C27 (end adjacent to C26)
SCOPE SETTING
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for HIGH (TTL) pulses, at least 2 µs long (pulse length will vary from pulse to pulse).



Waveform for AB3

(Relates to Fig. 10)

Fig. 11
May 86

PART OF
AB3/1
44829-340G

MEMORY CHIP SELECT DECODING

MWR (L)
MRD (L)
ADDRESS BUS
20
A18 A16 A15 A14 A13
IC8 IC9
OE WE
8K X8
CS2
+5V
R A M
A0
A12
D0 D7
CS1
IC6 LS138
G1 A B C G2A G2B
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
PLZ
A15 A8 A16 A0 A7
PLW
PLU

SUPPLY LINE TABLE						
IC	+5V	GROUND	CAP	IC	+5V	GROUND
IC1	18	9	C1	IC17	31	20
IC2	14	7	C2	IC18	20	10
IC3	14	7	C3	IC19	20	10
IC4	20	10	C4	IC20	14	7
IC5	20	10	C5	IC21	14	7
IC6	16	8	C6	IC22	14	7
IC7	16	8	C7	IC23	20	10
IC8	28	14	C8	IC24	20	10
IC9	28	14	C9	IC25	14	7
IC10	28	14	C10	IC26	20	10
IC11	28	14	C11	IC27	20	10
IC12	28	14	C12	IC28	28	14
IC13	28	14	C13	IC29	16	8
IC14	28	14	C14	IC30	16	8
IC15	40	1, 20	C15	IC31	14	7
IC16	16	8	C16	IC32	28	14
				IC33	28	14

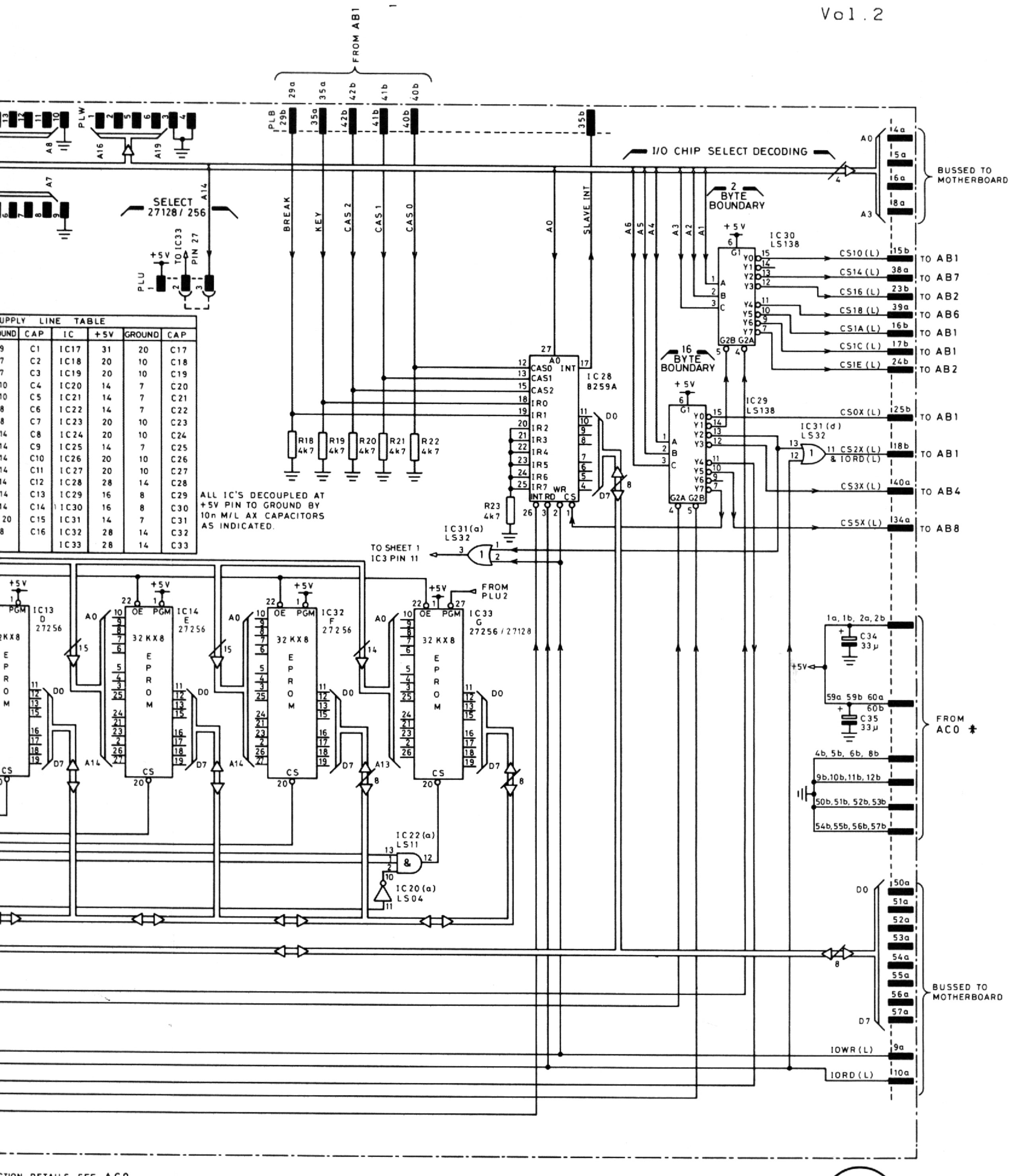
MRD (L)
A19 A18 A17 A16 A15
IC10 A 27256
IC11 B 27256
IC12 C 27256
IC13 D 27256
32KX8 EPROM
OE PGM
CS
IC7 LS138
MEMORY DATA BUS
FROM SHEET ONE
I/O DATA BUS

IOEN (L)
AEN
MWR (L)
MRD (L)
IOWR (L)
IORD (L)
CS4X (L)
IO/M̄ (L)
INTA (L)

* FOR CONNECTION DETAILS SEE AC0

Drg. No. Z 44829-340G
Sh. 2 Iss. 1

AB3/1:Processor memory &



SUPPLY LINE TABLE					
OUND	CAP	IC	+5V	GROUND	CAP
9	C1	IC17	31	20	C17
7	C2	IC18	20	10	C18
7	C3	IC19	20	10	C19
10	C4	IC20	14	7	C20
10	C5	IC21	14	7	C21
8	C6	IC22	14	7	C22
8	C7	IC23	20	10	C23
14	C8	IC24	20	10	C24
14	C9	IC25	14	7	C25
14	C10	IC26	20	10	C26
14	C11	IC27	20	10	C27
14	C12	IC28	28	14	C28
14	C13	IC29	16	8	C29
14	C14	IC30	16	8	C30
20	C15	IC31	14	7	C31
8	C16	IC32	28	14	C32
		IC33	28	14	C33

CTION DETAILS SEE AC0

sor memory & chip select

AB3/1

Fig. 11
Chap. 7
Page 29

BOARD : AB4
KEY OF FUNCTIONS

1 DACK1(L) + IOWR(L)
2 WD(L)
3 FRAME (L)
4 DRQ1 - DMA REQUEST FOR SCREEN UPDATE
5 CLOCK CONTROL FOR B TRACE INPUT DATA LATCHES
6 CLOCK CONTROL FOR B INPUT DATA LATCHES
7 CLOCK CONTROL FOR A INPUT DATA LATCHES
8 CLOCK FOR A INPUT DATA LATCHES
9 A OR A-B SEL (L)
10 A SEL (L)
11 A-B SEL (L)

continued opposite Fig. 13

1 BOARD : AB4

FUNCTION : DACK(L) + IOWR(L).

TEST POINT : PLAA
GROUND POINT : C37 (end adjacent to C36)
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE : 1 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check for 5 LOW (TTL) pulses in sequence.
Pulse LOW time = 400 ns
Pulse repetition time (in sequence) = 1.4 µs
Sequence repetition time = 64 µs (±20 ns variations).

2 BOARD : AB4

FUNCTION : WD(L).

TEST POINT : PLAB
GROUND POINT : C36 (end adjacent to C35)
SCOPE SETTING
CH2 : 2 V/DIV on PLAC
MAIN TIMEBASE : 20 µs/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Check for 2 LOW TTL pulses, 17 µs long, as follows :

Trigger to CH1↓ = 44 µs
CH1↑ to CH1↓ = 32 µs (pulse spacing)

3 BOARD : AB4

FUNCTION : FRAME (L).

TEST POINT : PLAC
GROUND POINT : C36 (end adjacent
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 5 ms/DIV

PROCEDURE :

1. Press [PRESET]. Adjust sc
Check for LOW (TTL) pulses,

4 BOARD : AB4

FUNCTION : DRQ1 - DMA REQUEST FOR

TEST POINT : PLAD
GROUND POINT : C36 (end adjacent
SCOPE SETTING
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check for
always greater than 7 µs, re

5 BOARD : AB4

FUNCTION : CLOCK CONTROL FOR B TR

TEST POINT : PLAE
GROUND POINT : C36 (end adjacent
SCOPE SETTING
CH2 : 2 V/DIV on PLAA
TRIGGER : -ve, CH2
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for
after trigger point.

NOTE. There will be some f

Fig. 12A
Chap. 7
Page 30

e Fig. 13

3 BOARD : AB4

FUNCTION : FRAME (L).

TEST POINT : PLAC
GROUND POINT : C36 (end adjacent to C35)
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 5 ms/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain display. Check for LOW (TTL) pulses, 1.6 ms long, occurring every 41 ms.

6 BOARD : AB4

FUNCTION : CLOCK CONTROL FOR B INPUT DATA

TEST POINT : PLAH
EARTH POINT : C22 (end adjacent to C21)
SCOPE SETTING
CH2 : 2 V/DIV on PLAE
TRIGGER : CH2
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for a single
starting simultaneously with the scop

4 BOARD : AB4

FUNCTION : DRQ1 - DMA REQUEST FOR SCREEN UPDATE.

TEST POINT : PLAD
GROUND POINT : C36 (end adjacent to C35)
SCOPE SETTING
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check for HIGH (TTL) pulses, length variable but always greater than 7 µs, repeating every 64 µs.

7 BOARD : AB4

FUNCTION : CLOCK CONTROL FOR A INPUT DATA

TEST POINT : PLAJ
GROUND POINT : C22 (end adjacent to C21)
SCOPE SETTING
CH2 : 2 V/DIV on PLAH
TRIGGER : CH2
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for a single
starting simultaneously with the scop

5 BOARD : AB4

FUNCTION : CLOCK CONTROL FOR B TRACE INPUT DATA LATCHES.

TEST POINT : PLAE
GROUND POINT : C36 (end adjacent to C35)
SCOPE SETTING
CH2 : 2 V/DIV on PLAA
TRIGGER : -ve, CH2
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for CH1 waveform going (TTL) HIGH 450 ns (±50 ns) after trigger point.

NOTE. There will be some faint background traces also - ignore these).

8 BOARD : AB4

FUNCTION : CLOCK FOR A INPUT DATA LATCHES.

TEST POINT : PLAK
GROUND POINT : C19 (end adjacent to C18)
SCOPE SETTING
CH2 : 2 V/DIV on PLAJ
TRIGGER : CH2
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for a single
starting simultaneously with the scop

Waveforms for AB4

DATA LATCHES.

1)

ngle LOW (TTL) pulse (1.4 µs long)
scope trigger.

DATA LATCHES.

21)

ngle LOW (TTL) pulse (1.4 µs long)
scope trigger.

TCHES.

18)

ngle LOW (TTL) pulse (1.4 µs long)
e scope trigger.

9 BOARD : AB4

FUNCTION : A OR A-B SEL (L).

TEST POINT : PLAL
GROUND POINT : C47 (end adjacent to C46)
SCOPE SETTING
CH2 : 2 V/DIV on PLAK
TRIGGER : CH2
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for a single LOW (TTL) pulse (1.4 µs long) starting simultaneously with scope trigger.

10 BOARD : AB4

FUNCTION : A SEL (L).

TEST POINT : PLAM
EARTH POINT : C37 (end adjacent to C36)
SCOPE SETTING
CH2 : 2 V/DIV on PLAL
TRIGGER : CH2, -ve, manual
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Adjust trigger level for scope display. Check for LOW TTL pulse (1.4 µs long) starting simultaneously with scope trigger.

2. Press 'display [A-B]'. Check that the pulses, described above, are replaced by a steady HIGH (TTL).

11 BOARD : AB4

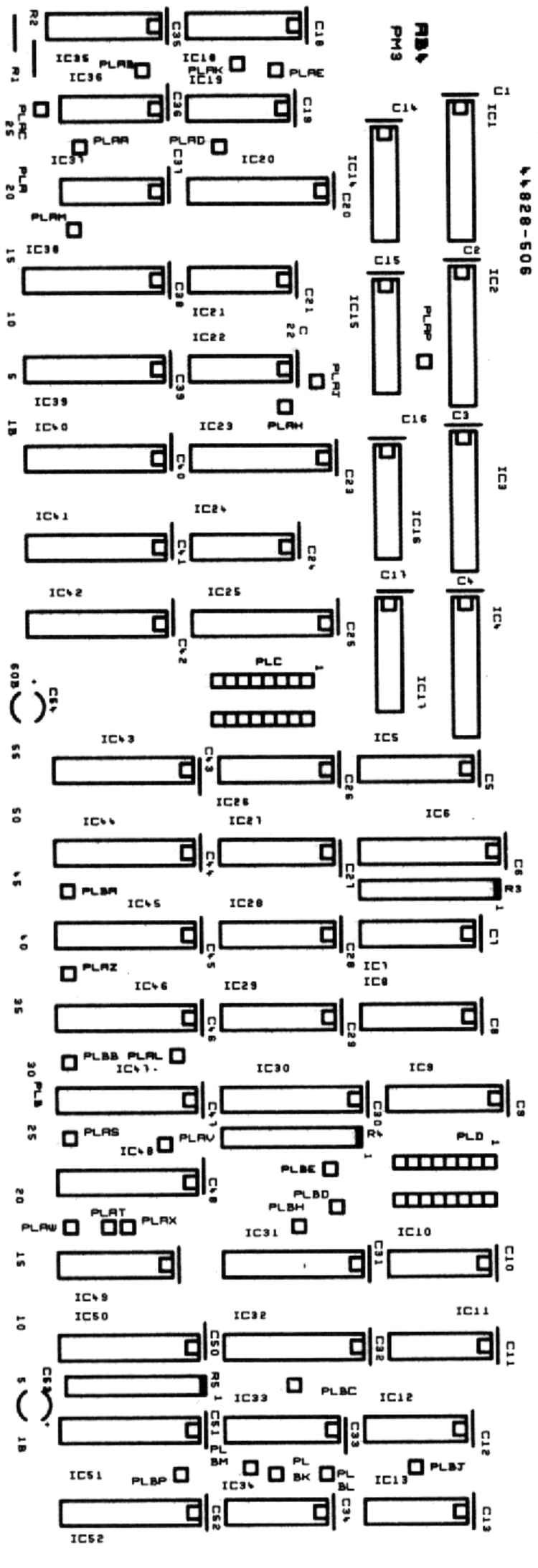
FUNCTION : A-B SEL (L).

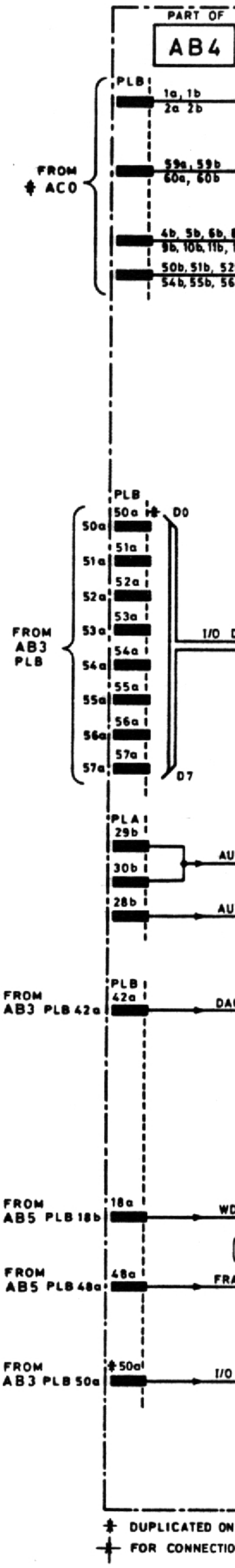
TEST POINT : PLAP
GROUND POINT : C15 (end adjacent C21)
SCOPE SETTING
CH2 : 2 V/DIV on PLAL
TRIGGER : -ve, CH2, manual

PROCEDURE :

1. Press [PRESET], 'display [A-B]'. Adjust trigger level for scope display. Check for LOW (TTL) pulse (1.4 µs long) starting simultaneously with scope trigger.

2. Press [PRESET]. Check that pulse described above is replaced by a steady (TTL) HIGH.





Component layout for AB4

Fig. 12
May 86

PART OF

AB4 44828-506R

PLB

FROM ‡ AC0

1a, 1b
2a 2b

C53 33µ +

+5V

59a, 59b
60a, 60b

C54 33µ +

4b, 5b, 6b, 8b,
9b, 10b, 11b, 12b

50b, 51b, 52b, 53b,
54b, 55b, 56b, 57b

SUPPLY LINE TABLE					
IC	+5V	GROUND	IC	+5V	GROUND
IC1	20	10	IC28	16	8
IC2	20	10	IC29	16	8
IC3	20	10	IC30	20	10
IC4	20	10	IC31	20	10
IC5	16	8	IC32	20	10
IC6	20	10	IC33	16	8
IC7	16	8	IC34	14	7
IC8	16	8	IC35	16	8
IC9	16	8	IC36	14	7
IC10	14	7	IC37	14	7
IC11	14	7	IC38	20	10
IC12	14	7	IC39	20	10
IC13	14	7	IC40	20	10
IC14	16	8	IC41	20	10
IC15	16	8	IC42	20	10
IC16	16	8	IC43	20	10
IC17	16	8	IC44	20	10
IC18	16	8	IC45	20	10
IC19	14	7	IC46	20	10
IC20	20	10	IC47	20	10
IC21	14	7	IC48	20	10
IC22	14	7	IC49	16	8
IC23	20	10	IC50	20	10
IC24	14	7	IC51	20	10
IC25	20	10	IC52	20	10
IC26	16	8			
IC27	16	8			

ALL IC'S DECOUPLED AT +5V PIN TO GROUND RAIL WITH 10n CAPACITOR

B INPUT LATCHES

IC39 LS273

D0 … D7 … D14

IC23 LS273

IC41 LS273

PLB

50a ‡ D0 … D7

FROM AB3 PLB

I/O DATA BUS

8

TO SHEET TWO

6 PLAH

5 PLAE

7 PLAJ

PLA

29b AUTOTEST CLEAR (L)

30b

28b AUTOTEST PRESET (L)

+5V R1 2k2

+5V R2 2k2

DMA BYTE COUNTER

IC35 LS161

1 PLAA

FROM AB3 PLB 42a — PLB 42a — DACK 1 (L) + IOWR (L)

2 PLAB

FROM AB5 PLB 18b — 18a — WD (L)

3 PLAC

FROM AB5 PLB 48a — 48a — FRAME (L)

IC24(d) LS04

IC37(c) LS32

IC36(a) LS08

B.A. GRAT DEMUX DECODER

IC18 LS138

DMA REQ LATCH

4 PLAD

IC19(a) LS74

A/A-B SELECT LATCH

IC19(b) LS74

FROM AB3 PLB 50a — ‡50a — I/O DATA BUS D0

CS36 (L)

FROM IC49 PIN 9 SHEET 2

DRQ1

A INPUT LATCHES

IC38 LS273

8 PLAK

IC40 LS273

9 PLAL

A OR A-B SEL (L)

B SEL (L)

IC37(d) LS32

A SEL (L)

IC37 LS32

A-B SEL (L)

IC37(a) LS32

PLB 41a — TO AB3

20a — TO AB5

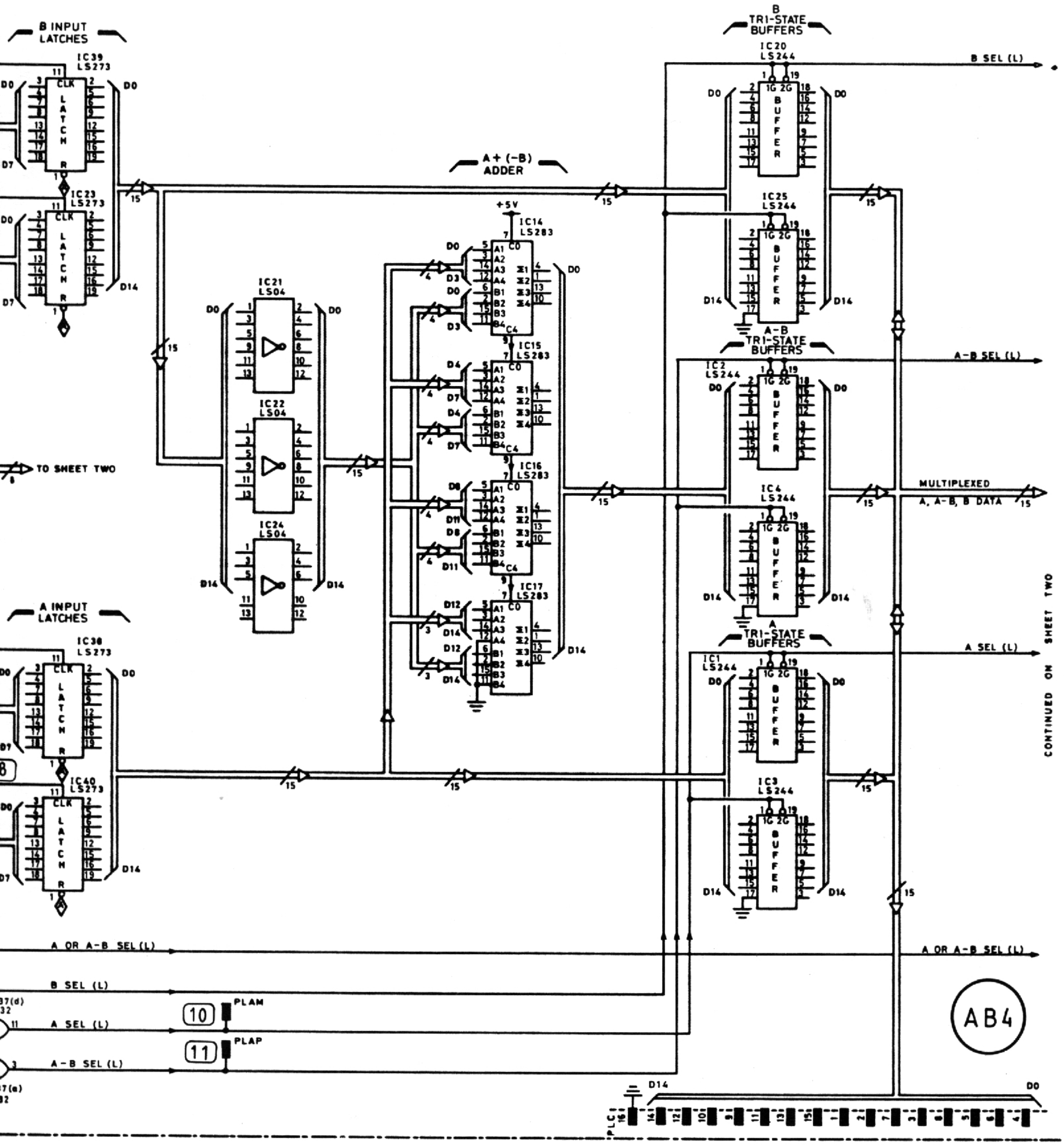
19a — TO AB6

‡ DUPLICATED ON THIS CIRCUIT FOR CLARITY

╪ FOR CONNECTION DETAILS SEE CIRCUIT AC0

Drg. No. Z52380-900E
Sh. 6 Iss. 1

AB4 : Mathematics opera


B INPUT LATCHES
IC39 LS273
IC23 LS273
IC38 LS273
IC40 LS273
A INPUT LATCHES
CLK
LATCH
D0
D7
D14
15
A+(-B) ADDER
IC21 LS04
IC22 LS04
IC24 LS04
IC14 LS283
IC15 LS283
IC16 LS283
IC17 LS283
+5V
C0
C4
A1
A2
A3
A4
B1
B2
B3
B4
Σ1
Σ2
Σ3
Σ4
D3
D4
D7
D8
D11
D12
D14
B TRI-STATE BUFFERS
IC20 LS244
IC25 LS244
IC2 LS244
IC4 LS244
IC1 LS244
IC3 LS244
1G 2G
BUFFER
B SEL (L)
A-B TRI-STATE BUFFERS
A-B SEL (L)
MULTIPLEXED
A, A-B, B DATA
A TRI-STATE BUFFERS
A SEL (L)
A OR A-B SEL (L)
B SEL (L)
A SEL (L)
A-B SEL (L)
PLAM
PLAP
10
11
TO SHEET TWO
CONTINUED ON SHEET TWO
AB4
PLC
D14
D0

BOARD : AB4
KEY OF FUNCTIONS (continued)

12 CS36(L)
13 UNDERRANGE SIGNAL FROM SHIFT ADDER
14 CS36(L)
15 CS36(L)
16 CS36(L)
17 CS36(L)
18 CS36(L)
19 CS36(L)
20 DIV L
21 DIV L
22 DIV L
23 CS36(L)

continued opposite Fig. 14

12 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLAS
GROUND POINT : C48 (end adjacent to C47)
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily put CH1 scope probe on PLAA and adjust scope trigger to obtain display. With scope probe on PLAS, put scope into single sweep mode and 'reset' (or 'rearm') scope trigger. Check from scope trigger indicator that no trigger has been detected.

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper & lower units)'.
Select [1] 'enter upper unit I/O parameters'.
Enter 'port number [HEX]' = [3 6 -]
Enter 'port value [BIN]' = [-]
Check that the scope triggers when the last [-] key is pressed, by observing the scope trigger indicator.

13 BOARD : AB4

FUNCTION : UNDERRANGE SIGNAL FROM SHIFT ADDER.

TEST POINT : PLBH
GROUND POINT : C31 (end adjacent to PLBD)
SCOPE SETTING
CH2 : 2 V/DIV on PLAL
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Rotate SPAN/DIV to select 10 MHz/DIV.
Adjust scope trigger level to obtain display. In the period 200 ns - 1400 ns from scope trigger, check that PLBH (scope CH1) is LOW (TTL).

2. Press 'vertical dB/DIVISION [1]'. (The displayed spectrum should be compressed into a straight line at the bottom of the screen). In the period 200 ns - 1400 ns from scope trigger point, check that PLBH (scope CH1) waveform is HIGH (TTL).

14 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLAV
GROUND POINT : C48 (end adjacent
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily
scope trigger to obtain disp
single sweep mode, and 'rese
scope trigger indicator that

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access
Select [1] 'enter upper unit
Enter 'port number [HEX]'= [
Enter 'port value [BIN]'= [-
Check that the scope trigger
observing the scope trigger

15 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLAW
GROUND POINT : C48 (end adjacent
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporaril
scope trigger to obtain disp
into single sweep mode and '
from scope trigger indicator

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access
Select [1] 'enter upper unit
Enter 'port number [HEX]'= [
Enter 'port value [BIN]'= [-
Check that the scope trigger
observing the scope trigger

Fig. 13A
Chap. 7
Page 32

14 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLAV
GROUND POINT : C48 (end adjacent to C47)
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily put CH1 scope probe on PLAA, and adjust scope trigger to obtain display. With scope probe on PLAS, put scope into single sweep mode, and 'reset' (or 'rearm') scope trigger. Check from scope trigger indicator that no trigger has been detected.

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper & lower units)'.
Select [1] 'enter upper unit I/O parameters'.
Enter 'port number [HEX]'= [3 0 -].
Enter 'port value [BIN]'= [-].
Check that the scope triggers when the last [-] key is pressed, by observing the scope trigger indicator.

16 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLAX
GROUND POINT : C48 (end adjacent to C47)
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily put CH
scope trigger to obtain display. W
into single sweep mode, and 'reset'
Check from scope trigger indicator th

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper &
Select [1] 'enter upper unit I/O para
Enter 'port number [HEX]'= [3 2 -].
Enter 'port value [BIN]'= [-].
Check that the scope triggers when th
observing trigger indicator.

15 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLAW
GROUND POINT : C48 (end adjacent to C47)
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily put CH1 scope probe on PLAA and adjust scope trigger to obtain display. With scope probe on PLAS, put scope into single sweep mode and 'reset' (or 'rearm') scope trigger. Check from scope trigger indicator that no trigger has been detected.

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper & lower units)'.
Select [1] 'enter upper unit I/O parameters'.
Enter 'port number [HEX]'= [3 1 -].
Enter 'port value [BIN]'= [-].
Check that the scope triggers when the last [-] key is pressed, by observing the scope trigger indicator.

17 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLAZ
GROUND POINT : C48 (end adjacent to C47)
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily put CH
scope trigger to obtain display. W
into single sweep mode, and 'reset'
Check from scope trigger indicator th

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper &
Select [1] 'enter upper unit I/O para
Enter 'port number [HEX]'= [3 3 -].
Enter 'port value [BIN]'= [-].
Check that the scope triggers when th
observing the scope trigger indicator

Fig. 14

OW (TTL).

e
ope CH1)

C47)

ut CH1 scope probe on PLAA and adjust
. With scope probe on PLAS, put scope
set' (or 'rearm') scope trigger.
tor that no trigger has been detected.

per & lower units)'.
0 parameters'.
-].

hen the last [-] key is pressed by

18 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLBA
GROUND POINT : C48 (end adjacent to C47)
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily put CH1 scope probe on PLAA and adjust scope trigger to obtain display. With scope probe on PLAS, put scope into single sweep mode, and 'reset' (or 'rearm') scope trigger. Check from scope trigger indicator that no trigger has been detected.

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper & lower units)'.
Select [1] 'enter upper unit I/O parameters'.
Enter 'port number [HEX]'= [3 4 -].
Enter 'port value [BIN]'= [-].
Check that the scope triggers when the last [-] key is pressed by observing the scope trigger indicator.

C47)

ut CH1 scope probe on PLAA and adjust
. With scope probe on PLAS, put scope
set' (or 'rearm') scope trigger.
tor that no trigger has been detected.

per & lower units)'.
0 parameters'.
-].

hen the last [-] key is pressed, by
icator.

19 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLBB
GROUND POINT : C48 (end adjacent to C47)
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily put CH1 probe on PLAA and adjust scope trigger to obtain display. With scope probe on PLAS, put scope into single sweep mode, and 'reset' (or 'rearm') scope trigger. Check from scope trigger indicator that no trigger has been detected.

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper & lower units)'.
Select [1] 'enter upper unit I/O parameters'.
Enter 'port number [HEX]'= [3 5 -].
Enter 'port value [BIN]'= [-].
Check that the scope triggers when the last [-] key is pressed, by observing the scope trigger indicator.

Fig. 13A

May 86

20 BOARD : AB4

FUNCTION : DIV L.

TEST POINT : PLBC
GROUND POINT : C33 (end adjacent to C32)
SCOPE SETTING
CH2 : 2V/DIV on PLAJ
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain display.
Check for scope CH1 being LOW (TTL) for 1.4 µs from scope trigger.*

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper & lower units)'.
Select [1] 'enter upper unit I/O port parameters'.
Enter 'port number [HEX]'= [3 6 -].

3. Enter 'port value [BIN]' = [0 0 0 0 0 1 0 0] [-].
Check for scope CH1 being HIGH (TTL) for 1.4 µs from scope trigger.*

4. Move scope CH2 probe to PLAL.

5. Repeat (1), (2) above.

6. Enter 'port value [BIN]' = [0 0 1 0 0 0 0 0] [-].
Check for scope CH1 being HIGH (TTL) for 1.4 µs from trigger.*

* Outside the defined time limits, the signals will not necessarily be TTL levels, as they are tristated.

21 BOARD : AB4

FUNCTION : DIV L.

TEST POINT : PLBD
GROUND POINT : C33 (end adjacent to C32)
SCOPE SETTING
CH2 : 2 V/DIV on PLAJ
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain display.
Check for scope CH1 being LOW (TTL) for 1.4 µs from scope trigger.*

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper & lower units)'.
Select [1] 'enter upper unit I/O port parameters'.
Enter 'port number [HEX]' = [3 6 -].

3. Enter 'port value [BIN]' = [0 0 0 0 1 0 0 0] [-].
Check for scope CH1 being HIGH (TTL) for 1.4 µs from scope trigger.*

4. Move scope CH2 probe to PLAL.

5. Repeat (1), (2) above.

6. Enter 'port value [BIN]' = [0 1 0 0 0 0 0 0] [-].
Check for scope CH1 being HIGH (TTL) for 1.4 µs from trigger.*

* Outside the defined time limits, the signals will not necessarily be TTL levels, as they are tristated.

22 BOARD : AB4

FUNCTION : DIV L.

TEST POINT : PLBE
GROUND POINT : C33 (end adjacent to C
SCOPE SETTING
CH2 : 2 V/DIV on PLAJ
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope t
Check for scope CH1 being LOW (T

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upp
Select [1] 'enter upper unit I/O
Enter 'port number [HEX]' = [3 6

3. Enter 'port value [BIN]' = [0 0
Check for scope CH1 being HIGH (

4. Move scope CH2 probe to PLAL.

5. Repeat (1), (2) above.

6. Enter 'port value [BIN]' = [0 0
Check for scope CH1 being HIGH (

* Outside the defined time limits, th
TTL levels, as they are tristated.

23 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLAT
GROUND POINT : C48 (end adjacent to C
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily pu
scope trigger to obtain display.
into single sweep mode and 'rese
from scope trigger indicator tha

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upp
Select [1] 'enter upper unit I/O
Enter 'port number [HEX]'= [3 6
Enter 'port value [BIN]'= [-].
Check that the scope triggers wh
observing the scope trigger indi

el to obtain display.
4 µs from scope trigger.*

units)'.
meters'.

0] [-].
.4 µs from scope trigger.*

0] [-].
.4 µs from trigger.*

will not necessarily be

22 BOARD : AB4

FUNCTION : DIV L.

TEST POINT : PLBE
GROUND POINT : C33 (end adjacent to C32)
SCOPE SETTING
CH2 : 2 V/DIV on PLAJ
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain display.
Check for scope CH1 being LOW (TTL) for 1.4 µs from scope trigger.*

2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper & lower units)'.
Select [1] 'enter upper unit I/O port parameters'.
Enter 'port number [HEX]' = [3 6 -].

3. Enter 'port value [BIN]' = [0 0 0 0 0 0 1 0] [-].
Check for scope CH1 being HIGH (TTL) for 1.4 µs from scope trigger.*

4. Move scope CH2 probe to PLAL.

5. Repeat (1), (2) above.

6. Enter 'port value [BIN]' = [0 0 0 1 0 0 0 0] [-].
Check for scope CH1 being HIGH (TTL) for 1.4 µs from trigger.*

* Outside the defined time limits, the signals will not necessarily be TTL levels, as they are tristated.

el to obtain display.
4 µs from scope trigger.*

units)'.
meters'.

0] [-].
.4 µs from scope trigger.*

0] [-].
.4 µs from trigger.*

will not necessarily be

23 BOARD : AB4

FUNCTION : CS36(L).

TEST POINT : PLAT
GROUND POINT : C48 (end adjacent to C47)
SCOPE SETTING
TRIGGER : manual, dc
MAIN TIMEBASE : 100 ms/DIV

PROCEDURE :

1. Press [PRESET]. Temporarily put CH1 scope probe on PLAA and adjust scope trigger to obtain display. With scope probe on PLAS, put scope into single sweep mode and 'reset' (or 'rearm') scope trigger. Check from scope trigger indicator that no trigger has been detected.

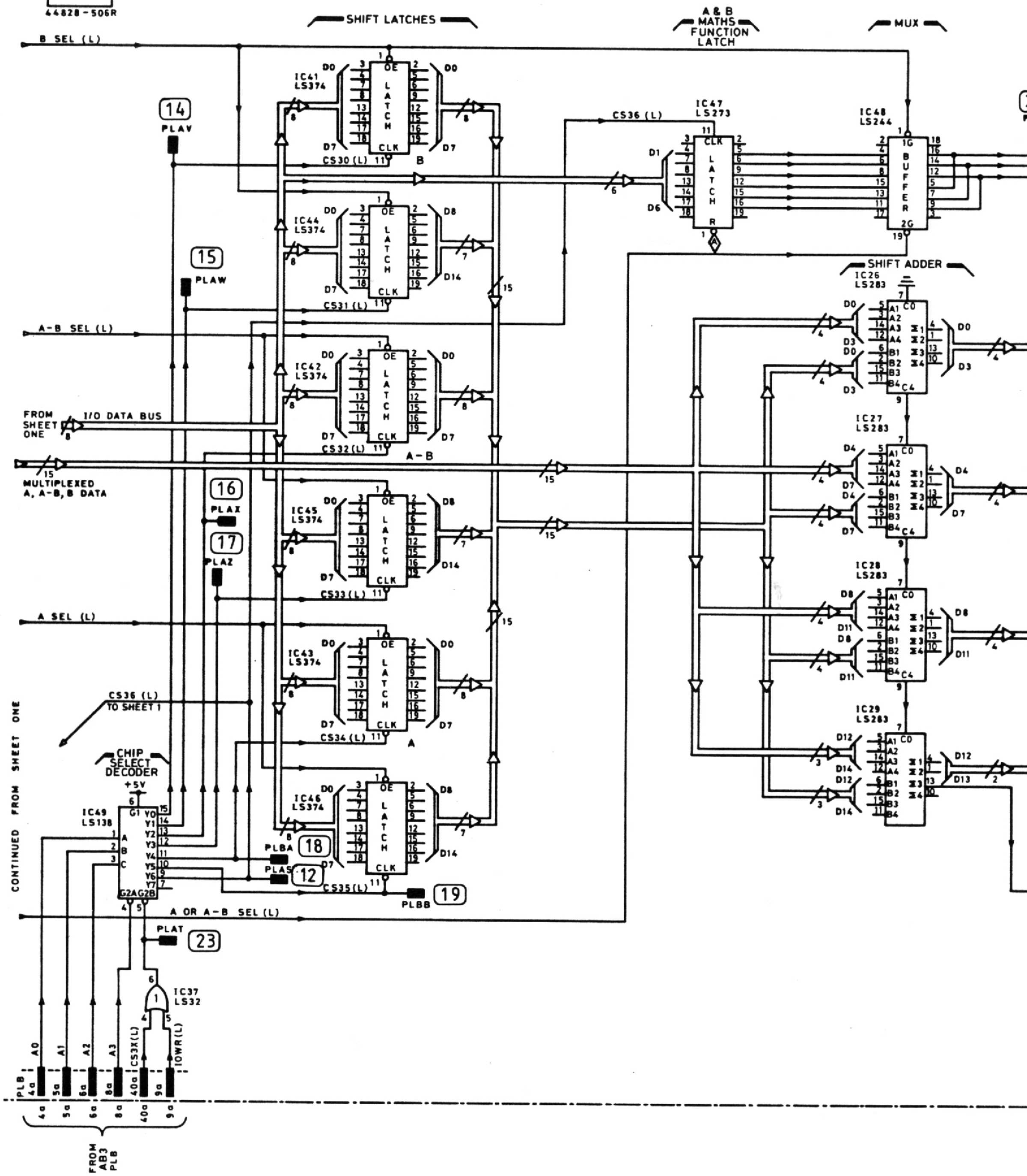
2. Enter DEBUG OPERATIONS mode.
Select [1] 'I/O port access (upper & lower units)'.
Select [1] 'enter upper unit I/O parameters'.
Enter 'port number [HEX]'= [3 6 -]
Enter 'port value [BIN]'= [-].
Check that the scope triggers when the last [-] key is pressed by observing the scope trigger indicator.

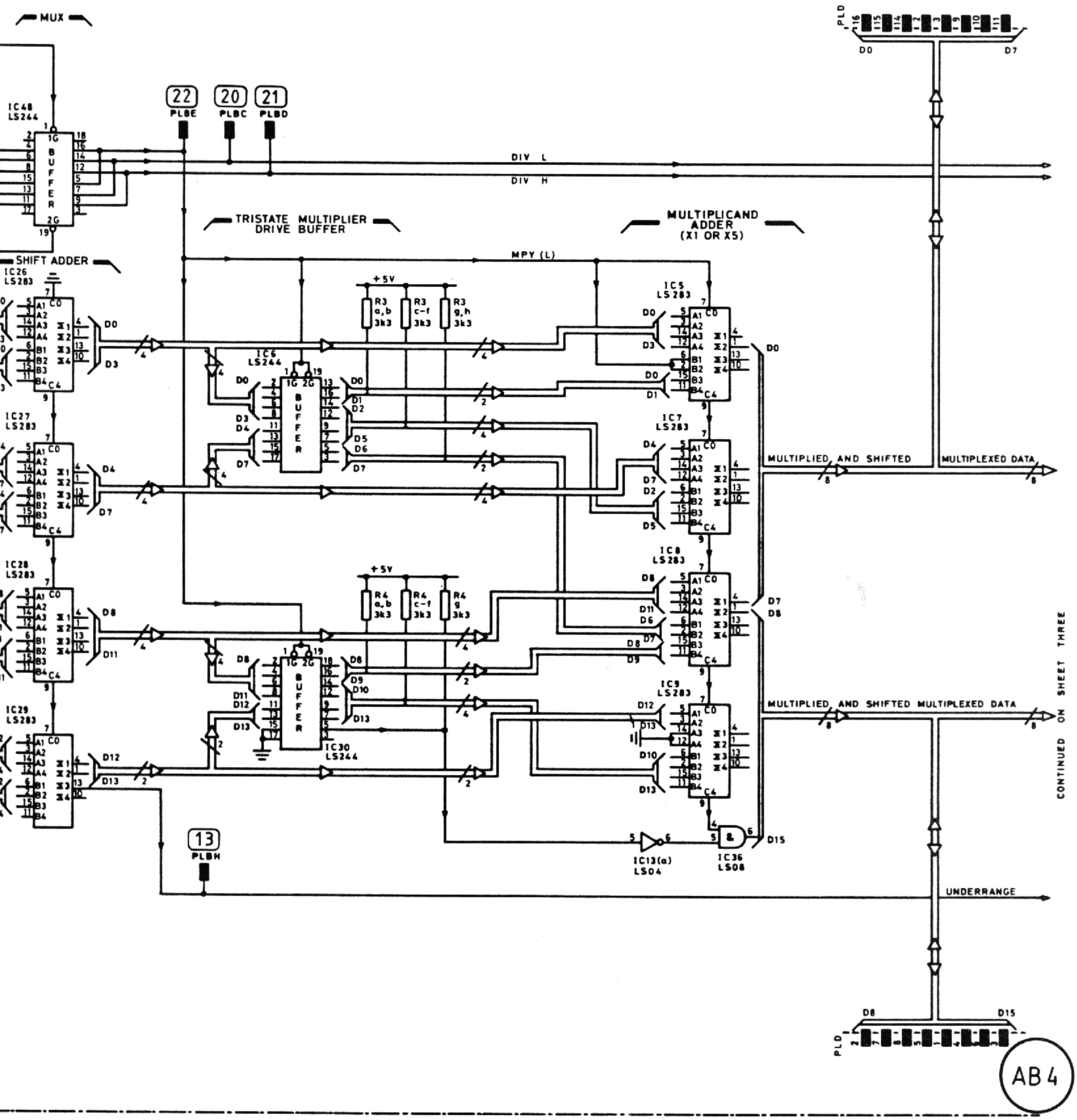
Waveforms for AB4

Fig. 13B

May 86

PART OF
AB4
44828-506R




MUX
IC48 LS244
BUFFER
22 PLBE
20 PLBC
21 PLBD
DIV L
DIV H
TRISTATE MULTIPLIER DRIVE BUFFER
MULTIPLICAND ADDER (X1 OR X5)
PLD
D0
D7
SHIFT ADDER
IC26 LS283
IC27 LS283
IC28 LS283
IC29 LS283
MPY (L)
+5V
R3 a,b 3k3
R3 c-f 3k3
R3 g,h 3k3
R4 a,b 3k3
R4 c-f 3k3
R4 g 3k3
IC6 LS244
IC30 LS244
IC5 LS283
IC7 LS283
IC8 LS283
IC9 LS283
MULTIPLIED AND SHIFTED
MULTIPLEXED DATA
MULTIPLIED AND SHIFTED MULTIPLEXED DATA
CONTINUED ON SHEET THREE
13 PLBH
IC13(a) LS04
IC36 LS08
UNDERRANGE
D8
D15
AB 4

KEY OF FUNCTIONS (concluded)

24 OVERRANGE
25 SELECTOR FOR ÷2 BIT SHIFT DIVIDER
26 SELECTOR FOR ÷4 BIT SHIFT DIVIDER
27 SELECTOR FOR ÷8 BIT SHIFT DIVIDER
28 SELECTOR FOR ÷16 BIT SHIFT DIVIDER

24 BOARD : AB4

FUNCTION : OVERRANGE.

TEST POINT : PLBJ
GROUND POINT : C13 (end adjacent to C12)
SCOPE SETTING
CH2 : 2V/DIV on PLAL.
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger to obtain display.
Rotate '[SPAN/DIV]' to select 10 MHz/DIV. Check for a LOW (TTL) pulse, 1.4 µs long (±200 ns) occurring within 200 ns of scope trigger.

2. Press 'vertical [÷]' to select most sensitive range. Check that pulse described above is replaced by a steady (TTL) HIGH.

25 BOARD : AB4

FUNCTION : SELECTOR FOR ÷2 BIT SHIFT DIVIDER.

TEST POINT : PLBK
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2 V/DIV on PLAL
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET], [TRACK GEN], 'vertical [÷]' to obtain -10 dBm at top of 2380 screen. Select 10 MHz/DIV. Adjust scope trigger level to obtain display. Connect tracking generator output to RF input on 2382.

2. Check that scope CH1 is TTL HIGH in the period 200 ns - 1400 ns after the scope trigger. Press 'vertical [VOLTS/DIV]'. Check that scope CH1 waveform is TTL LOW in the period defined above.

3. Press 'dB/DIVISION [10]'. Press 'vertical [A B SELECT]'.
Move scope CH2 probe to PLAJ, and repeat (2) above.

26 BOARD : AB4

FUNCTION : SELECTOR FOR ÷4 BIT SHIFT DIVIDER.

TEST POINT : PLBL
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2 V/DIV on PLAL
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET], [TRACK GEN], 'vertical [÷]'
2380 screen. Select 10 MHz/DIV. Adjust
display. Connect tracking generator outpu

2. Check that scope CH1 is TTL HIGH in the per
scope trigger. Press 'vertical dB/DIVISIO
waveform is TTL LOW in the period defined a

3. Press 'vertical dB/DIVISION [10]'. Press
Move scope CH2 probe to PLAJ and repeat (2)

27 BOARD : AB4

FUNCTION : SELECTOR FOR ÷8 BIT SHIFT DIVIDER.

TEST POINT : PLBM
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2V/DIV on PLAL
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET], [TRACK GEN], 'vertical [÷]'
2380 screen. Select 10 MHz/DIV. Adjust
display. Connect tracking generator outpu

2. Check that scope CH1 is TTL HIGH in the per
scope trigger. Press 'vertical dB/DIVISIO
waveform is TTL LOW in the period defined a

3. Press 'vertical dB/DIVISION [10]'. Press
Move scope CH2 probe to PLAJ and repeat (2)

28 BOARD : AB4

FUNCTION : SELECTOR FOR ÷16 BIT SHIFT DIVIDER.

TEST POINT : PLBP
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2 V/DIV on PLAL
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET], [TRACK GEN], 'vertical [÷]'
2380 screen. Select 10 MHz/DIV. Adjust
display. Connect tracking generator outpu

2. Check that scope CH1 is TTL LOW in the peri
scope trigger. Press 'vertical dB/DIVISIO
waveform is TTL HIGH in the period defined

3. Press 'vertical dB/DIVISION [10]'. Press
Move scope CH2 probe to PLAJ, and repeat (2

DER
DER
DER
IDER

C12)

trigger to obtain display.
0 MHz/DIV. Check for a LOW (TTL) pulse,
within 200 ns of scope trigger.

most sensitive range. Check that pulse
a steady (TTL) HIGH.

DIVIDER.

C33)

ertical [+]' to obtain -10 dBm at top of
V. Adjust scope trigger level to obtain
erator output to RF input on 2382.

l in the period 200 ns - 1400 ns after the
l [VOLTS/DIV]'. Check that scope CH1
od defined above.

ss 'vertical [A B SELECT]'.
nd repeat (2) above.

26 BOARD : AB4

FUNCTION : SELECTOR FOR ÷4 BIT SHIFT DIVIDER.

TEST POINT : PLBL
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2 V/DIV on PLAL
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET], [TRACK GEN], 'vertical [+]' to obtain -10 dBm at top of 2380 screen. Select 10 MHz/DIV. Adjust scope trigger level to obtain display. Connect tracking generator output to RF input on 2382.

2. Check that scope CH1 is TTL HIGH in the period 200 ns - 1400 ns after the scope trigger. Press 'vertical dB/DIVISION [0.5]'. Check that scope CH1 waveform is TTL LOW in the period defined above.

3. Press 'vertical dB/DIVISION [10]'. Press 'vertical [A B SELECT]'. Move scope CH2 probe to PLAJ and repeat (2) above.

27 BOARD : AB4

FUNCTION : SELECTOR FOR ÷8 BIT SHIFT DIVIDER.

TEST POINT : PLBM
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2V/DIV on PLAL
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET], [TRACK GEN], 'vertical [+]' to obtain -10 dBm at top of 2380 screen. Select 10 MHz/DIV. Adjust scope trigger level to obtain display. Connect tracking generator output to RF input on 2382.

2. Check that scope CH1 is TTL HIGH in the period 200 ns - 1400 ns after the scope trigger. Press 'vertical dB/DIVISION [5]'. Check that scope CH1 waveform is TTL LOW in the period defined above.

3. Press 'vertical dB/DIVISION [10]'. Press 'vertical [A-B SELECT]'. Move scope CH2 probe to PLAJ and repeat (2) above.

28 BOARD : AB4

FUNCTION : SELECTOR FOR ÷16 BIT SHIFT DIVIDER.

TEST POINT : PLBP
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2 V/DIV on PLAL
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET], [TRACK GEN], 'vertical [+]' to obtain -10 dBm at top of 2380 screen. Select 10 MHz/DIV. Adjust scope trigger level to obtain display. Connect tracking generator output to RF input on 2382.

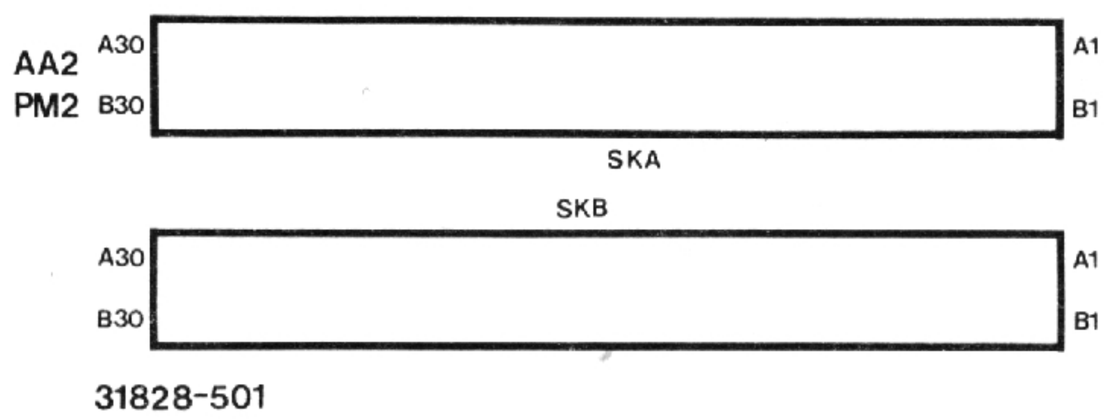
2. Check that scope CH1 is TTL LOW in the period 200 ns - 1400 ns after the scope trigger. Press 'vertical dB/DIVISION [5]'. Check that scope CH1 waveform is TTL HIGH in the period defined above.

3. Press 'vertical dB/DIVISION [10]'. Press 'vertical [A B SELECT]'. Move scope CH2 probe to PLAJ, and repeat (2) above.

Waveforms for AB4

Fig. 14A

May 86



31828-501

44828-501

PART OF

AB4

44828-50

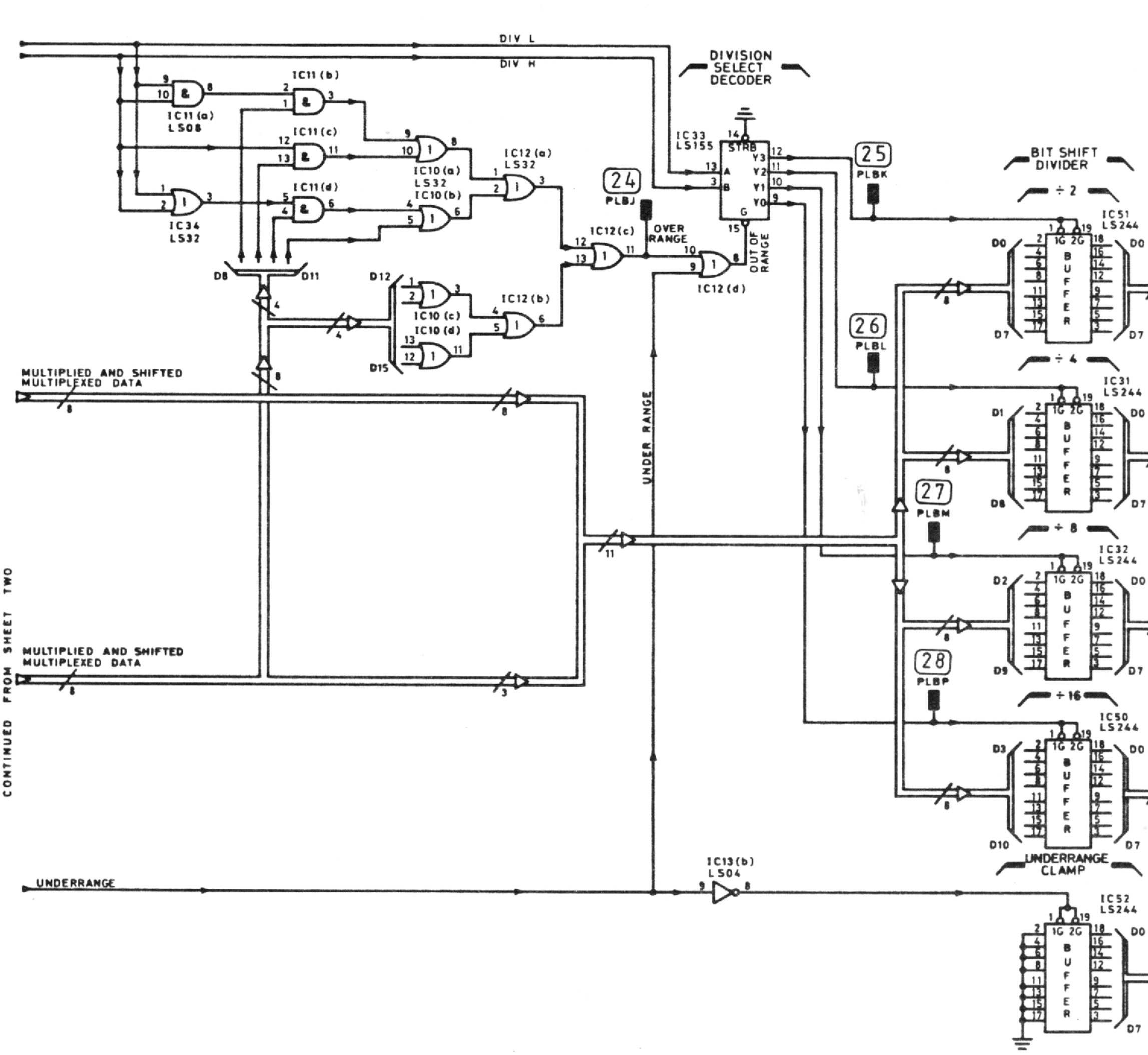
CONTINUED FROM SHEET TWO

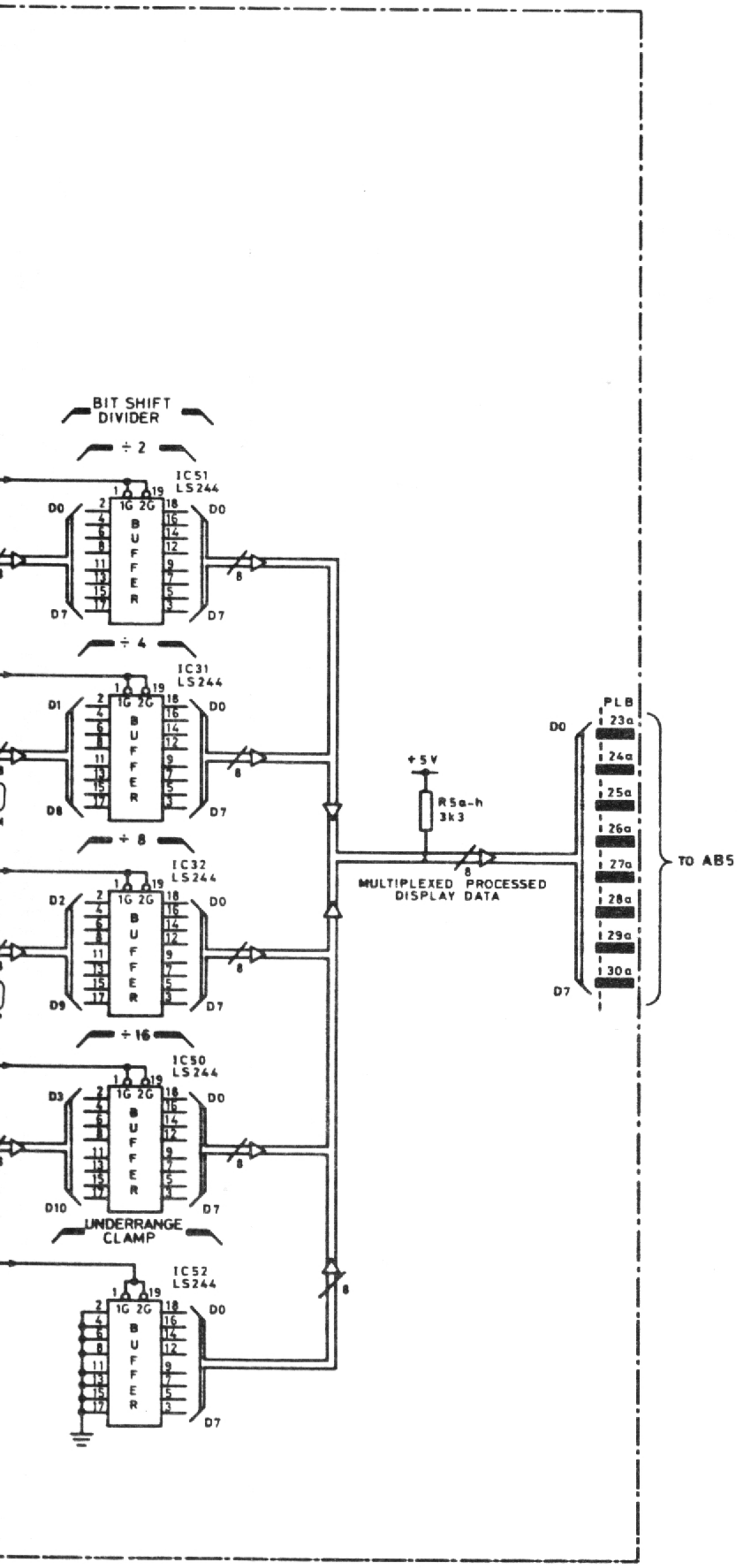
Sockets underside layout AA2

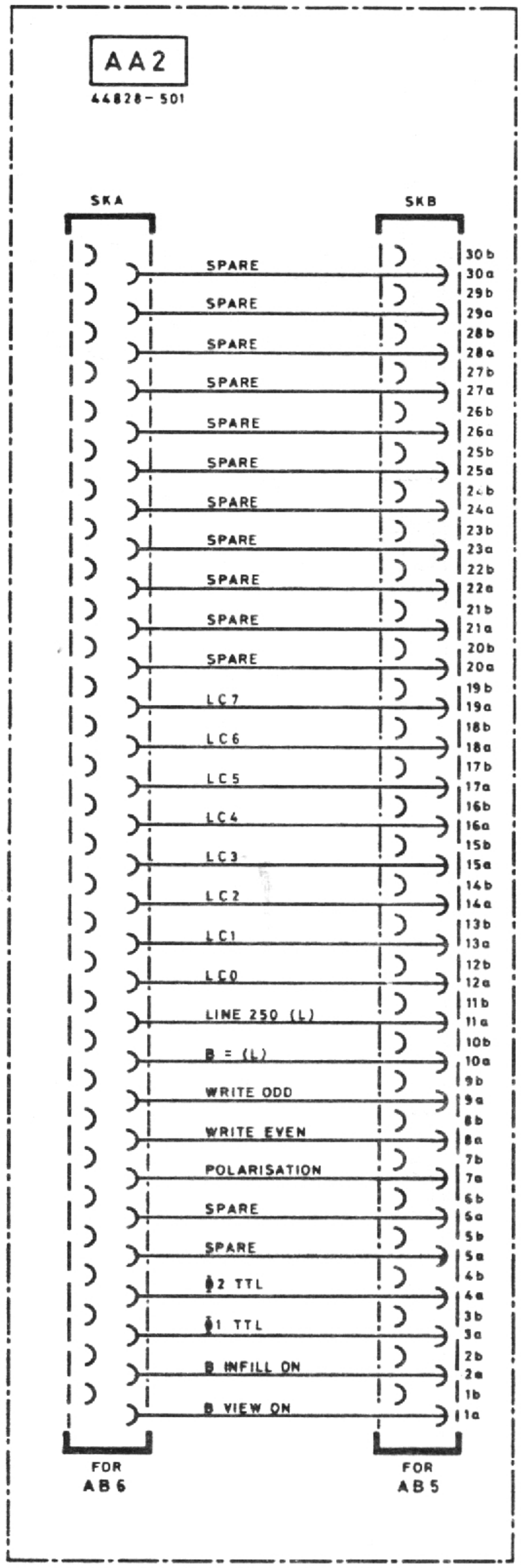
Fig. 14
May 86

PART OF
AB4
44828-506R

OVERRANGE DETECTOR







AB4
AA2

thematics operations
xiliary connector

Fig. 14
Chap. 7
Page 37

BOARD : AB5
KEY OF FUNCTIONS

1 B SEL (L)
2 12.5 MHz CLOCK (PHASED)
3 X VIDEN
4 CLOCK EN(L)
5 HRTC(L)
6 6.25 MHz SHIFT REGISTER GATED CLOCK
7 Φ_1 TTL ROOT CLOCK FOR SHIFT REGISTERS
8 Φ_2 TTL ROOT CLOCK FOR SHIFT REGISTERS
9 Φ_{1a} - SHIFT REGISTER CLOCK
10 Φ_{2a} - SHIFT REGISTER CLOCK
11 Φ_{1b} - SHIFT REGISTER CLOCK
12 Φ_{2b} - SHIFT REGISTER CLOCK
13 EVEN/ODD DISCRIMINATOR IN ODD/EVEN DATA BYTE WRITE PULSE GENERATOR FOR DISPLAY DYNAMIC STORES
14 DRQ1 - DMA REQUEST FOR UPDATING DISPLAY DYNAMIC STORES
15 WD(L) - WRITE DATA CONTROL
16 WO - WRITE ODD BYTE INTO DISPLAY DYNAMIC STORE
17 WE - WRITE EVEN BYTE CONTROL FOR DISPLAY

continued opposite Fig. 16

1 BOARD : AB5

FUNCTION : B SEL (L).

TEST POINT : PLAA
GROUND POINT : C45 (end adjacent to C54)
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for LOW (TTL) pulses, 1.4 µs long, occurring approx. every 64 µs (±15 µs).

2 BOARD : AB5

FUNCTION : 12.5 MHz CLOCK (PHASED).

TEST POINT : PLAB
GROUND POINT : C30 (end adjacent to PLBS)
SCOPE SETTING
MAIN TIMEBASE : 20 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for symmetrical TTL clock, period 80 ns.

3 BOARD : AB5

FUNCTION : X VIDEN.

TEST POINT : PLAC
GROUND POINT : C14 (end adjacent to
SCOPE SETTING
CH2 : 2 V/DIV on PLAE
TRIGGER : ext, +ve, manual, on
MAIN TIMEBASE : 10 µs/DIV
MODE : CH1, CH2 alternate

PROCEDURE :

1. Press [PRESET]. Adjust scope
on CH1, CH2 with the following
CH2↑
CH1↑
CH1↑

4 BOARD : AB5

FUNCTION : CLOCK EN(L).

TEST POINT : PLAD
GROUND POINT : C47 (end adjacent to
SCOPE SETTING
CH2 : 2 V/DIV on PLAE
TRIGGER : ext, +ve, manual, on
MAIN TIMEBASE : 10 µs/DIV
MODE : CH1, CH2 alternate

PROCEDURE :

1. Press [PRESET]. Adjust scope
on CH1, CH2 with the following
CH2↑
CH1↓
CH1↓

5 BOARD : AB5

FUNCTION : HRTC(L).

TEST POINT : PLAE
GROUND POINT : C40 (end adjacent to
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check for (T
Pulse length = 4.3 µs (±0.
Pulse repetition = 64 µs

Fig. 15A
Chap. 7
Page 38

g. 16

3 BOARD : AB5

FUNCTION : X VIDEN.

TEST POINT : PLAC
GROUND POINT : C14 (end adjacent to R7)
SCOPE SETTING
CH2 : 2 V/DIV on PLAE
TRIGGER : ext, +ve, manual, on PLBA
MAIN TIMEBASE : 10 µs/DIV
MODE : CH1, CH2 alternate

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger for display check for TTL signals on CH1, CH2 with the following timings :
CH2↑ to CH1↑ = 12 µs
CH1↑ to CH1↓ = 40 µs
CH1↑ to CH1↑ = 64 µs

4 BOARD : AB5

FUNCTION : CLOCK EN(L).

TEST POINT : PLAD
GROUND POINT : C47 (end adjacent to C46)
SCOPE SETTING
CH2 : 2 V/DIV on PLAE
TRIGGER : ext, +ve, manual, on PLBA
MAIN TIMEBASE : 10 µs/DIV
MODE : CH1, CH2 alternate

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger for display check for TTL signals on CH1, CH2 with the following timings :
CH2↑ to CH1↓ = 12 µs
CH1↓ to CH1↑ = 42 µs
CH1↓ to CH1↓ = 64 µs

5 BOARD : AB5

FUNCTION : HRTC(L).

TEST POINT : PLAE
GROUND POINT : C40 (end adjacent to PLAX)
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check for (TTL) LOW pulses
Pulse length = 4.3 µs (±0.5 µs)
Pulse repetition = 64 µs

6 BOARD : AB5

FUNCTION : 6.25 MHz SHIFT REGISTER GATED CL

TEST POINT : PLAH
GROUND POINT : C14 (end adjacent to R7)
SCOPE SETTING
CH2 : 2 V/DIV on PLAD
TRIGGER : CH2, -ve
MAIN TIMEBASE : 50 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for symmetrica
with period 160 ns.

2. Change scope trigger to +ve slope. C
LOW (TTL) state.

7 BOARD : AB5

FUNCTION : Φ_1 TTL ROOT CLOCK FOR SHIFT REGIS

TEST POINT : PLAJ
GROUND POINT : C44 (end adjacent to C43)
SCOPE SETTING
CH2 : 2 V/DIV on PLAD
TRIGGER : CH2, -ve
MAIN TIMEBASE : 500 ns/DIV
DELAY TIMEBASE : 100 ns/DIV
MODE :
Set delay to minimum (zero)
'B' (or 'delay') timebase only
Delay trigger : manual, CH1, +ve

PROCEDURE :

1. Press [PRESET]. Adjust delay trigger
Check for (TTL) HIGH pulses on CH1.
Pulse HIGH time = 80 ns (±10 ns)
Pulse repetition time = 320 ns

8 BOARD : AB5

FUNCTION : Φ_2 TTL ROOT CLOCK FOR SHIFT REGIS

TEST POINT : PLAK
GROUND POINT : C45 (end adjacent to C54)
SCOPE SETTING
CH2 : 2 V/DIV on PLAD
TRIGGER : CH2, -ve
MAIN TIMEBASE : 500 ns/DIV
DELAY TIMEBASE : 100 ns/DIV
MODE :
Set delay to minimum (zero)
'B' (or 'delay') timebase only
Delay trigger : manual, CH1, +ve

PROCEDURE :

1. Press [PRESET]. Adjust delay trigger
Check for (TTL) HIGH pulses on CH1.
Pulse HIGH time = 80 ns (±10 ns)
Pulse repetition time = 320 ns

TED CLOCK.

7)

etrical clock (TTL) on scope CH1,

e. Check that CH1 now shows

T REGISTERS.

3)

ly
+ve

igger level to obtain scope display.
1.
0 ns)

REGISTERS.

4)

ly
+ve

igger level to obtain scope display.
1.
10 ns)

9 BOARD : AB5

FUNCTION : Φ_{1a} - SHIFT REGISTER CLOCK.

TEST POINT : PLAL
GROUND POINT : C28 (end adjacent to C27)
SCOPE SETTING
CH1 : 5V/DIV
CH2 : 2V/DIV on PLAD
TRIGGER : CH2, -ve
MAIN TIMEBASE : 500 ns/DIV
DELAY TIMEBASE : 100 ns/DIV
MODE :
Set 'delay' to zero on scope.
Select delay timebase (or 'B' timebase) only
Set delay trigger : manual, CH1, -ve

PROCEDURE :

1. Press [PRESET]. Adjust delay trigger to obtain scope display.
Check for (TTL) LOW pulses on CH1.
Pulse HIGH time = 80 ns (±10 ns)
Pulse repetition time = 320 ns

10 BOARD : AB5

FUNCTION : Φ_{2a} - SHIFT REGISTER CLOCK.

TEST POINT : PLAM
GROUND POINT : C27 (end adjacent to C26)
SCOPE SETTING
CH1 : 5 V/DIV
CH2 : 2 V/DIV on PLAD
TRIGGER : CH2, -ve
MAIN TIMEBASE : 500 ns/DIV
DELAY TIMEBASE : 100 ns/DIV
MODE :
Set 'delay' to zero on scope
Select delay timebase (or 'B' timebase) only
Set delay trigger : manual, CH1, -ve

PROCEDURE :

1. Press [PRESET]. Adjust delay trigger to obtain scope display.
Check for (TTL) LOW pulses on CH1.
Pulse LOW TIME = 80 ns (±10 ns)
Pulse repetition time = 320 ns

11 BOARD : AB5

FUNCTION : Φ_{1b} - SHIFT REGISTER CLOCK.

TEST POINT : PLBV
GROUND POINT : C27 (end adjacent to C26)
SCOPE SETTING
CH1 : 5 V/DIV
CH2 : 2 V/DIV on PLAD
TRIGGER : CH2, -ve
MAIN TIMEBASE : 500 ns/DIV
DELAY TIMEBASE : 100 ns/DIV
MODE :
Set 'delay' to zero on scope
Select delay timebase (or 'B' timebase) only
Set delay trigger : manual, CH1, -ve

PROCEDURE :

1. Press [PRESET]. Adjust delay trigger to obtain scope display.
Check for (TTL) LOW pulses on CH1.
Pulse LOW time = 80 ns (±10 ns)
Pulse repetition time = 320 ns

12 BOARD : AB5

FUNCTION : Φ_{2b} - SHIFT REGISTER CLOCK.

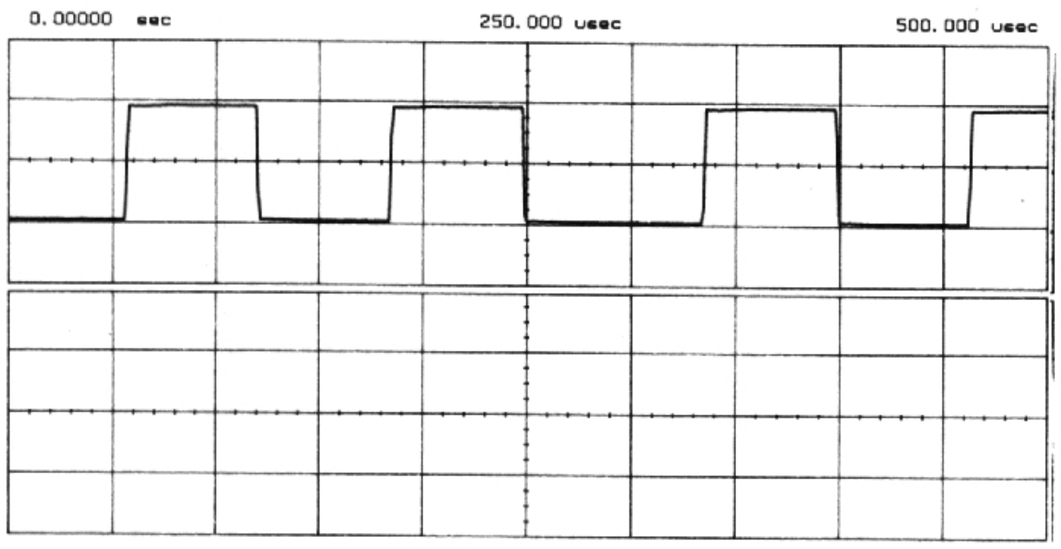
TEST POINT : PLAP
GROUND POINT : C29 (end adjacent to R5)
SCOPE SETTING
CH1 : 5 V/DIV
CH2 : 2 V/DIV on PLAD
TRIGGER : CH2, -ve
MAIN TIMEBASE : 500 ns/DIV
DELAY TIMEBASE : 100 ns/DIV
MODE :
Set 'delay' to zero on scope
Select delay timebase (or 'B' timebase) only
Set delay trigger : manual, CH1, -ve

PROCEDURE :

1. Press [PRESET]. Adjust delay trigger to obtain scope display.
Check for (TTL) LOW pulses on CH1.
Pulse LOW time = 80 ns (±10 ns)
Pulse repetition time = 320 ns

13 BOARD : AB5

FUNCTION : EVEN/ODD DISCRIMINATOR IN ODD/EVEN DATA BYTE WRITE PULSE GENERATOR FOR DISPLAY DYNAMIC STORES.



TEST POINT : PLAS
GROUND POINT : C18 (end adjacent to IC1)
SCOPE SETTING
CH2 : 2 V/DIV on PLAZ
TRIGGER : +ve, CH2, manual
MAIN TIMEBASE : 50 µs/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain display. Check for a series of HIGH (TTL) pulses, 64 µs long, spaced apart as follows :
Trigger to CH1↑ = 56 µs
CH1↓ to CH1↑ = 64 µs first interval
CH1↓ to CH1↑ = 84 µs 2nd interval
CH1↓ to CH1↑ = 64 µs 3rd interval
CH1↓ to CH1↑ = 64 µs all subsequent intervals

14 BOARD : AB5

FUNCTION : DRQ1 - DMA REQUEST FOR UPDATING DISPLAY

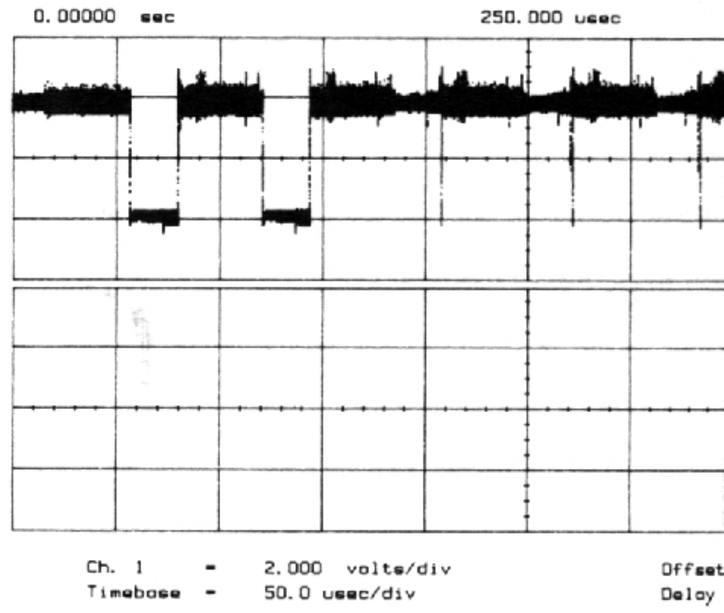
TEST POINT : PLAT
GROUND POINT : C34 (end adjacent to PLAZ)
SCOPE SETTING
CH2 : 2 V/DIV on PLAZ
TRIGGER : CH2, +ve, manual
MAIN TIMEBASE : 20 µs/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger for di
Check for HIGH (TTL) pulses (length variable
CH2↑ to CH1↑ = 64 µs
CH1↑ to CH1↑ = 64 µs

15 BOARD : AB5

FUNCTION : WD(L) - WRITE DATA CONTROL
(from AB5, odd/even byte write pulse g



TEST POINT : PLAV
GROUND POINT : C35 (end adjacent to C34)
SCOPE SETTING
CH2 : 2 V/DIV on PLAZ
TRIGGER : CH2, +ve, manual, dc
MAIN TIMEBASE : 50 µs/DIV
DELAY TIMEBASE : 200 ns/DIV
MODE : CH1 only, use scope hood.
Delay timebase trigger on CH1, -ve, dc,
Mode (a) main timebase only ('A' T/B).
(b) main timebase intensified by d
('A' intensified by 'B').
(c) Delay timebase only.

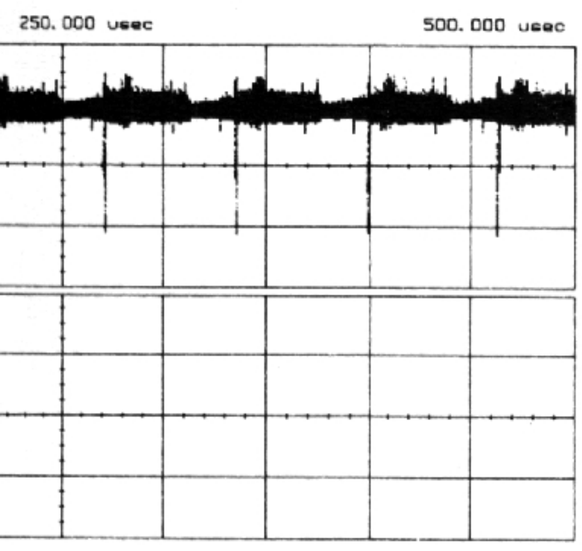
Waveforms for

UPDATING DISPLAY DYNAMIC STORES.

o PLAZ)

e trigger for display.
length variable between 5 and 12 µs).
H1↑ = 64 µs
H1↑ = 64 µs

TROL
te write pulse generator).



to C34)

lc

od.
n CH1, -ve, dc, manual.
nly ('A' T/B).
ntensified by delay timebase
d by 'B').
only.

15 BOARD : AB5

PROCEDURE :

1. Press [PRESET]. Scope in mode (a) (see waveform diagram).
   Adjust main timebase trigger level until a display is obtained.
   Check for 2 LOW (TTL) pulses, 23 µs long, 40 µs apart, occurring 56 µs after scope trigger.

2. Set delay control on scope to minimum and adjust delay trigger level until there appears a bright spot on the scope display, positioned at the beginning of the first pulse (described above). (It may be necessary to reduce the display intensity to distinguish the spot from the waveform).
   Rotate the delay control on the scope, and the bright spot should 'hop' to the start of the second pulse. Rotate the control still further until the spot leaves the 2nd pulse. It should hop to a position approx. 80 µs from the start of the 2nd pulse.
   Select mode (c) above, check for a LOW (TTL) pulse approx. 150 ns long (see waveform diagram).

16 BOARD : AB5

FUNCTION : WO - WRITE ODD BYTE INTO DISPLAY DYNAMIC STORE.

TEST POINT : PLAW
GROUND POINT : C38 (end adjacent to C37)
SCOPE SETTING
CH2 : 2 V/DIV on PLAZ
TRIGGER : CH2, manual, +ve

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger to obtain display.
   Check for HIGH (TTL) pulse (on scope CH1), length 23 µs, occurring 120 µs after scope trigger.

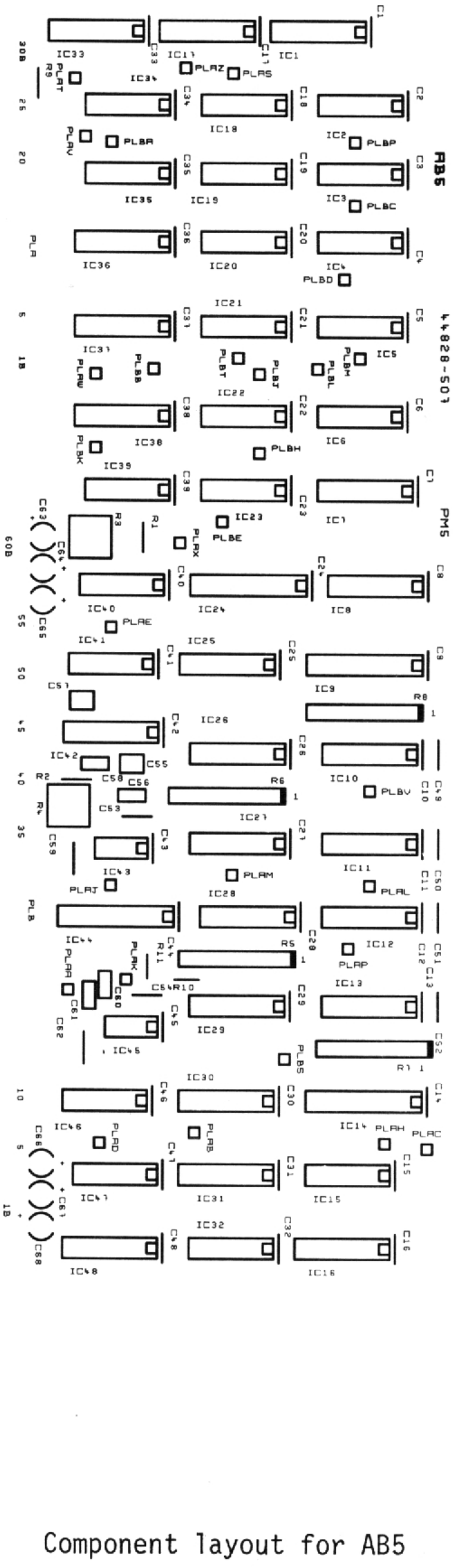
17 BOARD : AB5

FUNCTION : WE - WRITE EVEN BYTE CONTROL FOR DISPLAY DYNAMIC STORES.

TEST POINT : PLAX
GROUND POINT : C40 (end adjacent to PLAX)
SCOPE SETTING
CH2 : 2 V/DIV on PLAZ
TRIGGER : CH2, manual
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain display.
   Check for a HIGH (TTL) pulse, 23 µs long, occurring 115 µs after the trigger.



Component layout for AB5

Fig. 15
May 86

PART OF
AB5
44828-507B

FROM AB4 PLB 20a

PLB 19a, 19b, 20b, 23a, 23b, 24a, 24b, 25a, 25b, 26a, 26b, 27a, 27b, 28a, 28b, 29a, 29b, 30a, 30b

A OR A-B SEL (L)

B SEL (L)

FROM AB4 PLB

D0 ... D7

B DEMUX LATCH

IC44 LS273

MULTIPLEXED PROCESSED DISPLAY DATA

PLAA 1

TO AB6

PLA 3a, 4a

Φ1 TTL, Φ2 TTL

DUAL 2 PHASE CLOCK DRIVER

+5V

R2 3k3, R4 10k

SET Φ1 PULSE WIDTH

C57 10p

IC42(a) LS221

PLAJ 7

C56 180p

IC43 0026

PLAL 9

Φ1a

C58 180p

Φ2a

PLAM 10

R1 3k3, R3 10k

SET Φ2 PULSE WIDTH

C55 10p

IC42(b) LS221

TWO PHASE GEN. +5V

IC41 LS74

C61 180p

IC45 0026

R10 22R, R11 22R

PLBV 11

Φ1b

Φ2b

C60 180p

PLAK 8

PLAP 12

12·5 MHz PHASED CLOCK TO SHEET 2

SHIFT REGISTER GATED CLOCK GENERATOR AND HORIZONTAL MASK GENERATOR

AUTOTEST INVERTER

PLA 29b, 30b

ATR (L)

R9 2k2

IC18(d) LS04

PLAB 2

DETECT 502 CLOCKS AFTER START

IC15(a) LS74

XVIDEN TO SHEET 2

PLAC 3

IC32 LS30

IC15(b) LS74

6·25 MHz SHIFT REGIST

IC46(a) (f) (e)

PLAD 4

IC25(b) LS00

IC47(a) LS32

DETECT 514 CLOCKS AFTER START

FROM AB7 PLB 32b

PLB 32a

PHASED 12·5 MHz CLOCK

IC4(b) LS04

IC48 S161

IC31 LS161

IC16 LS161

CLOCK EN (L)

C69 330p

IC40(a) LS74

IC47(b) LS32

PLAE 5

HRTC (L) TO SHEET 2

6·25 MHz PHASED CLOCK

SR CLK

COUNTERS IC16, IC31, IC48 PRELOADED TO B38H (2572D)

PLB 37a

PLB 31a

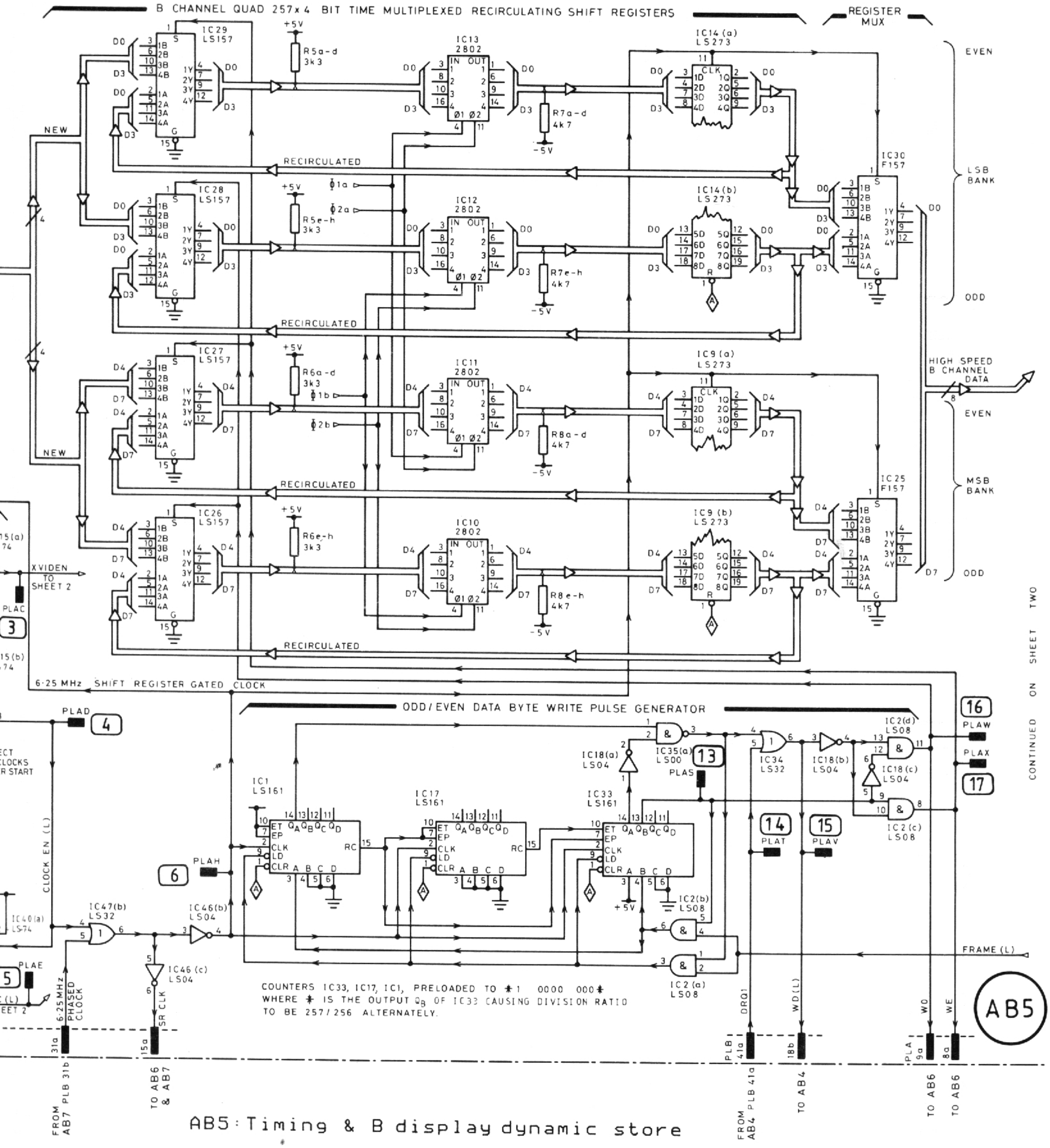
PLB 15a

FROM AB7 PLB 37a

FROM AB7 PLB 31b

TO AB6 & AB7

Drg. No. Z44828-507B
Sh. 1 Iss. 2



AB5 : Timing & B display dynamic store

BOARD : AB5
KEY OF FUNCTIONS (concluded)

18 FRAME(L)
19 VRTC(L)
20 Y VIDEN
21 BOX(L)
22 TOTAL DDM(L)
23 OUTPUT FROM B DATA/LINE COUNT COMPARATOR
24 OUTPUT FROM B DATA/LINE COUNT COMPARATOR
25 PART OF B DISPLAY AMPLITUDE LIMITER CIRCUIT
26 B=(L)
27 B VIEW ON
28 B INFILL VID
29 B LINE VID
30 B INFILL ON

---

18 BOARD : AB5

FUNCTION : FRAME(L).

TEST POINT : PLAZ
GROUND POINT : C34 (end adjacent to PLAZ)
SCOPE SETTING
    TRIGGER : manual, -ve
    MAIN TIMEBASE : 200 µs/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger for display.
   Check for LOW (TTL) pulse, length 1.6 ms, occurring every 41.6 ms.

---

19 BOARD : AB5

FUNCTION : VRTC(L).

TEST POINT : PLBA
GROUND POINT : C35 (end adjacent to C34)
SCOPE SETTING
    TRIGGER : -ve, CH1, manual

PROCEDURE :

1. Press [PRESET]. Adjust trigger level for display.
   Check for LOW (TTL) pulses (1.6 ms long) occurring every 20.8 ms.

---

20 BOARD : AB5

FUNCTION : Y VIDEN.

TEST POINT : PLBB
GROUND POINT : C38 (end adjacent to
SCOPE SETTING
    CH2 : 2 V/DIV on PLBA
    TRIGGER : CH2, manual
    MODE : CH1, CH2 CHOP

PROCEDURE :

1. Press [PRESET]. Adjust scope
   Check for TTL waveform (on scop

   CH2↑ (trigger) t
   CH1↑ t
   CH1↓ t

---

21 BOARD : AB5

FUNCTION : BOX(L).

TEST POINT : PLBC
GROUND POINT : C20 (end adjacent to
SCOPE SETTING
    CH2 : 2 V/DIV on PLAZ
    TRIGGER : CH2, manual

PROCEDURE :

1. Press [PRESET]. Adjust scope
   Check for a series of TTL pulse

2. Press [2ND FUNCT], [ANNOT GRAT]
   Scope CH1 should now show a ste

Fig. 16A
Chap. 7
Page 42

20 BOARD : AB5

FUNCTION : Y VIDEN.

TEST POINT : PLBB
GROUND POINT : C38 (end adjacent to C37)
SCOPE SETTING
    CH2 : 2 V/DIV on PLBA
    TRIGGER : CH2, manual
    MODE : CH1, CH2 CHOP

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level to obtain display.
   Check for TTL waveform (on scope CH1) with the following timings :

CH2↑ (trigger)	to CH1↑	= 1.4 ms
CH1↑	to CH1↓	= 1.6 ms
CH1↓	to CH2↓	= 1.7 ms

21 BOARD : AB5

FUNCTION : BOX(L).

TEST POINT : PLBC
GROUND POINT : C20 (end adjacent to C19)
SCOPE SETTING
    CH2 : 2 V/DIV on PLAZ
    TRIGGER : CH2, manual

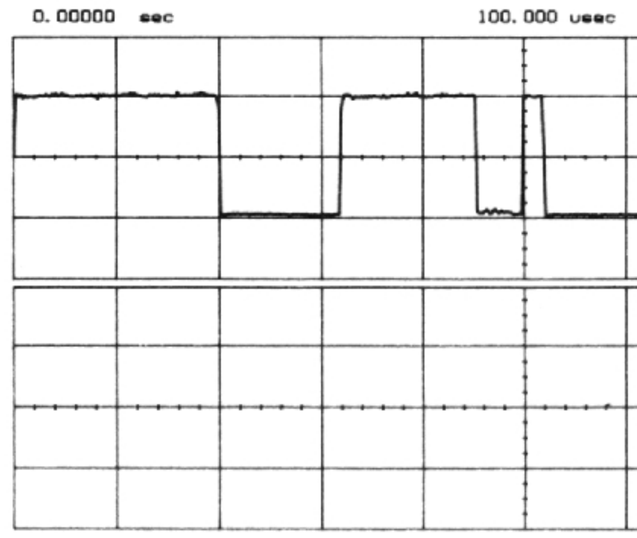
PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level for display.
   Check for a series of TTL pulses, of various lengths.

2. Press [2ND FUNCT], [ANNOT GRAT] (to remove annotation).
   Scope CH1 should now show a steady (TTL) HIGH.

22 BOARD : AB5

FUNCTION : TOTAL DDM(L).



TEST POINT : PLBD
GROUND POINT : C5 (end adjacent to C4)
SCOPE SETTING
    CH2 : 2 V/DIV on PLBA
    TRIGGER : manual, CH2
    MAIN TIMEBASE : 200 µs/DIV
    MODE : CH1 only

PROCEDURE :

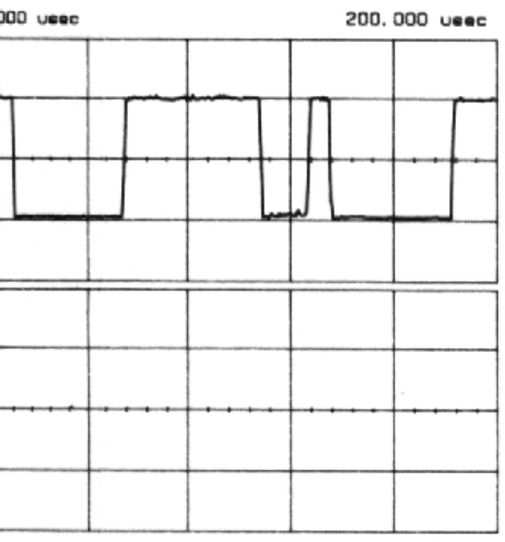
1. Press [PRESET]. Adjust scope trigger l
   Check for a series of HIGH (TTL) pulses
2. Select 'x10 sweep' facility, and adjust
   on the beginning of the pulse series (ab
   every 64 µs.

22 continued

3. Press 'display [CAL]' and wait for it t
   beginning of the displayed pulse series
   examine each pulse in turn.

First 4	HIGH pulse
5th	HIGH pulse
6th	HIGH pulse

See waveform diagram.



)

igger level control to obtain display.
pulses starting 1.4 ms after scope trigger.

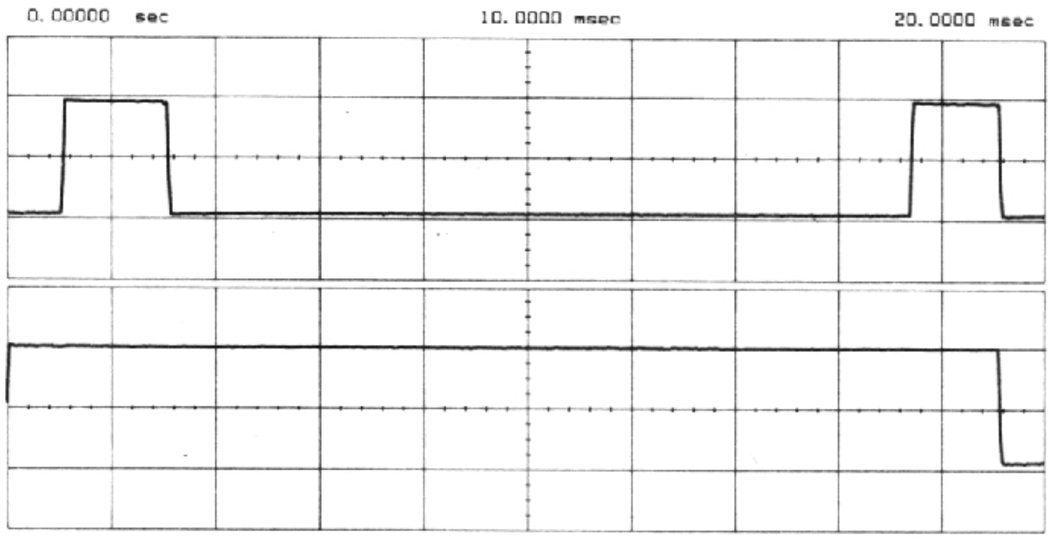
adjust 'x position' control to 'zoom in'
ies (above). Pulses should be 40 μs high

r it to finish (50 s). Starting at the
series, use the 'x position' control to

pulses = 40 μs long
pulse = 26 μs long
pulse = 4 μs long

23 BOARD : AB5

FUNCTION : OUTPUT FROM B DATA/LINE COUNT COMPARATOR.



TEST POINT : PLBE
GROUND POINT : C24 (end adjacent to C23)
SCOPE SETTING
CH2 : 2 V/DIV on PLBA
TRIGGER : manual, +ve, CH2
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1, CH2 CHOP

23 continued

PROCEDURE :

1. Press [PRESET]. Connect track generator output to RF input.
Press 'display A [VIEW]'.
Press 'display B [VIEW]'.
Press '[TRACK GEN]'.
Rotate [SPAN DIV] to select 10 Hz/DIV.
Adjust scope trigger to obtain display. Check scope display for two HIGH (TTL) pulses on CH1 during the period that CH2 is (TTL) HIGH.

CH2↑ to CH1↑ = 1.1 ms	1st pulse	All times ±0.2 ms
CH1↑ to CH1↓ = 1.9 ms		
CH1↓ to CH1↑ = 14.6 ms	2nd pulse	
CH1↑ to CH1↓ = 1.7 ms		

See waveform diagram.

Fig. 16A

May 86

24 BOARD : AB5

FUNCTION : OUTPUT FROM B DATA/LINE COUNT COMPARATOR.

TEST POINT : PLBH
GROUND POINT : C22 (end adjacent to C21)
SCOPE SETTING
CH2 : 2 V/DIV on PLBA
TRIGGER : manual, +ve, CH2
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1, CH2 CHOP

PROCEDURE :

1. Press [PRESET]. Connect tracking generator output to RF input.
Press 'display A [VIEW]'.
Press 'display B [VIEW]'.
Press '[TRACK GEN]'.
Rotate [SPAN DIV] to select 10 Hz/DIV.
Adjust scope trigger to obtain display. Check scope display for two LOW (TTL) pulses on CH1 during the period that CH2 is (TTL) HIGH.

CH2↑ to CH1↓ = 1.1 ms } 1st pulse
CH1↓ to CH1↑ = 1.9 ms }
CH1↑ to CH1↓ = 14.6 ms } 2nd pulse
CH1↓ to CH1↑ = 1.7 ms }
} All times ±0.2 ms

See waveform diagram 23

25 BOARD : AB5

FUNCTION : PART OF B DISPLAY AMPLITUDE LIMITE

TEST POINT : PLBL
GROUND POINT : C22 (end adjacent to C21)
SCOPE SETTING
CH2 : 2 V/DIV on PLBK
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 1 ms/DIV
DELAY TIMEBASE : 10 µs/DIV
MODE : CH1 only
Delay trigger : manual, +ve, CH1
Delay set to minimum
Sweep 'A' intensified by 'B'

NOTE. Use a scope hood or storage scope.

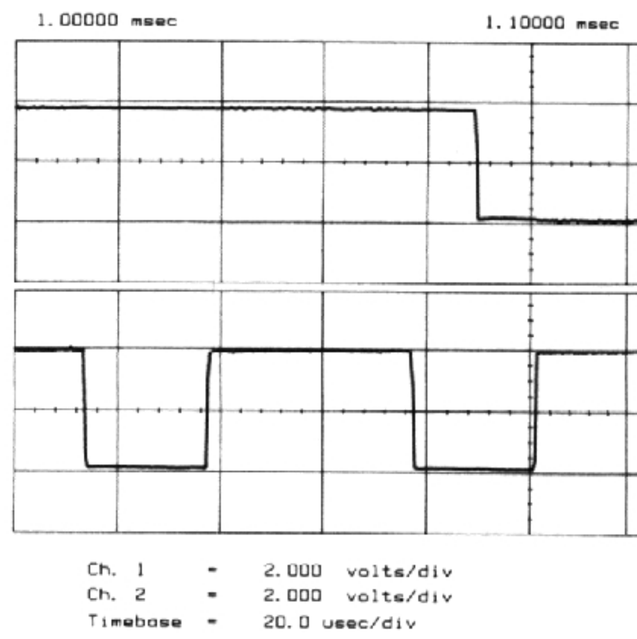
PROCEDURE :

1. Press [PRESET].
Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [2] 'enter data display and linear
Adjust main trigger level to obtain displ
level so that the delay sweep (intensifie
pulse, approx. 35 µs from start of sweep.
to 200 ns/DIV, change scope to 'B' sweep
check the HIGH (TTL) pulse to be 80 ns lo

2. Increase scope delay slowly and observe t
80 ns (that is 80, 160, 240, 320 ... ns).

26 BOARD : AB5

FUNCTION : B = (L).



TEST POINT : PLBJ
GROUND POINT : C22 (end adjacent to C21)
SCOPE SETTING
CH2 : 2 V/DIV on PLAC
TRIGGER : manual, +ve, external on PLEA
MAIN TIMEBASE : 1 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1, CH2 ALT
DELAY TRIGGER : 'B sweep after A'

Fig. 16B
Chap. 7
Page 44/43

DISPLAY AMPLITUDE LIMITER CIRCUIT.

nd adjacent to C21)

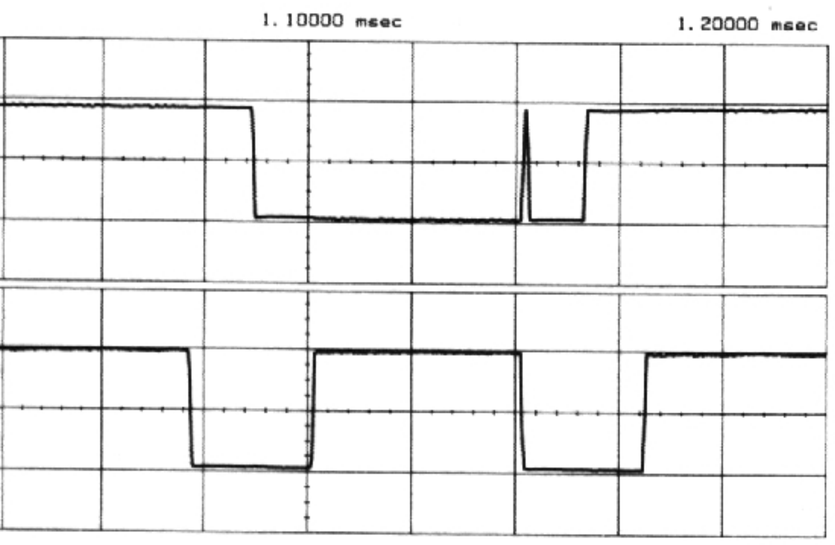
PLBK
, -ve, CH2
1 ms/DIV
10 µs/DIV

er : manual, +ve, CH1
o minimum
ntensified by 'B'

ood or storage scope.

ATIONS mode.
r unit confidence tests'.
r data display and linearity tests'.
ger level to obtain display. Adjust delay trigger
e delay sweep (intensified) starts on a narrow HIGH (TTL)
5 µs from start of sweep. Change scope delay timebase
hange scope to 'B' sweep only (delay timebase only) and
TTL) pulse to be 80 ns long.

elay slowly and observe the pulse widen by increments of
0, 160, 240, 320 ... ns).



nd adjacent to C21)

PLAC
, +ve, external on PLEA
ms/DIV
20 µs/DIV
ALT
IGGER : 'B sweep after A'

26 continued

PROCEDURE :

1. Press [PRESET]. Connect tracking generator output to RF input. With main timebase only, adjust main trigger level for display. Press [TRACK GEN] 'display A [VIEW]', 'display B [VIEW]'. Press 'vertical [+]'to select -30 dBm at the top of the 2380 display. Check for one short LOW (TTL) pulse, approx. 1.1 ms after trigger.

2. Switch scope to 'A sweep intensified by B sweep'. Adjust scope intensity (brilliance) to observe the (intensified) delay sweep, and adjust delay to align delayed sweep with pulse on CH1. Switch scope to 'delay sweep only'. Check that there is only one HIGH (TTL) pulse on CH2 during which CH1 is LOW, as shown on the waveform diagram.

27 BOARD : AB5

FUNCTION : B VIEW ON.

TEST POINT : PLBM
GROUND POINT : C6 (end adjacent to C5)
SCOPE SETTING
MAIN TIMEBASE : 10 ms/DIV

PROCEDURE

1. Press [PRESET]. Check for steady (TTL) LOW.

2. Press 'display B [VIEW]'. Check for steady (TTL) HIGH.

Waveforms for AB5

tracking generator output to RF input.
adjust main trigger level for display.
y A [VIEW]', 'display B [VIEW]'.
lect -30 dBm at the top of the 2380 display.
TTL) pulse, approx. 1.1 ms after trigger.

intensified by B sweep'. Adjust scope
observe the (intensified) delay sweep,
delayed sweep with pulse on CH1.
eep only'. Check that there is only
H2 during which CH1 is LOW, as shown on

to C5)

r steady (TTL) LOW.

Check for steady (TTL) HIGH.

28 BOARD : AB5

FUNCTION : B INFILL VID.

TEST POINT : PLBP
GROUND POINT : C3 (end adjacent to C2)
SCOPE SETTING
CH2 : 2 V/DIV on PLBK
TRIGGER : -ve, manual, CH2
MAIN TIMEBASE : 2 ms/DIV

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [2] 'enter data display & linearity tests'.
Adjust scope trigger to obtain display. Check for a TTL pulse sequence, starting from the scope trigger, ending after 16 ms, where the pulses (HIGH,TTL) increase in length from 80 ns (at the start) to 40 µs (at the end).

29 BOARD : AB5

FUNCTION : B LINE VID.

TEST POINT : PLBS
GROUND POINT : C30 (end adjacent to PLBS)
SCOPE SETTING
CH2 : 2 V/DIV on PLBK
TRIGGER : +ve, manual, CH2
MAIN TIMEBASE : 2 ms/DIV

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [2] 'enter data display & linearity tests'.
Press [2ND FUNCT], 'display B [VIEW]'.
Adjust scope trigger to obtain display. Check for a TTL pulse sequence, starting from the scope trigger, ending after 16 ms, where the pulses (HIGH,TTL) are 160 ns long, and 64 µs apart.

30 BOARD : AB5

FUNCTION : B INFILL ON.

TEST POINT : PLBT
GROUND POINT : C21 (end adjacent to C20)
SCOPE SETTING
MAIN TIMEBASE : 1 ms/DIV

PROCEDURE :

1. Press [PRESET], 'display B [VIEW]'. Check for steady (TTL) LOW.

2. Press [2ND FUNCT], 'display B [VIEW]'. Check for steady (TTL) HIGH.

PART OF AB5
44828-507B

TO AB6
12a 13a 14a 15a 16a 17u 18a 19a
PLA 12a 13a 14a 15a 16a 17a 18a 19a
D0 D7

B DATA STROBE
+5V
IC7 S85
IC8 S85
D0 D3 D4 D7
LINE COUNT BUS
8
HIGH SPEED 8 CHANNEL DATA
FROM SHEET 1

12·5MHz PHASED CLOCK FROM SHEET 1

X VIDEN FROM SHEET 1

TO AB6
IPLA 10a
11a
B = (L)
LINE 250 (L)

26
B LINE DRAW AND B INFILL BRIGHT UP GEN.
PLBJ
IC6(a) LS00
IC19 LS08
IC21(a) LS02

CURRENT ORDINATE LATCHES
PREVIOUS ORDINATE LATCHES
IC23(a) LS74
IC22(a) LS74
PLBH
24
IC6(b) LS00
IC5(a) LS10
25
PLBL
23
PLBE
IC23(b) LS74
IC22(b) LS74
IC6(c) LS00
PLBK

LINE DOWN COUNTER AND VERTICAL DISPLAY MASK GEN.
IC20 LS30
IC39(a) LS32
IC39(b) LS32
IC39(c) LS32
VERTICAL MASK LATCH
IC40(b) LS74
LINE 250(L)
LINE 0
HRTC(L) FROM SHEET 1
IC37 LS193
IC36 LS193
IC38 LS193
LSB
MSB
PLB

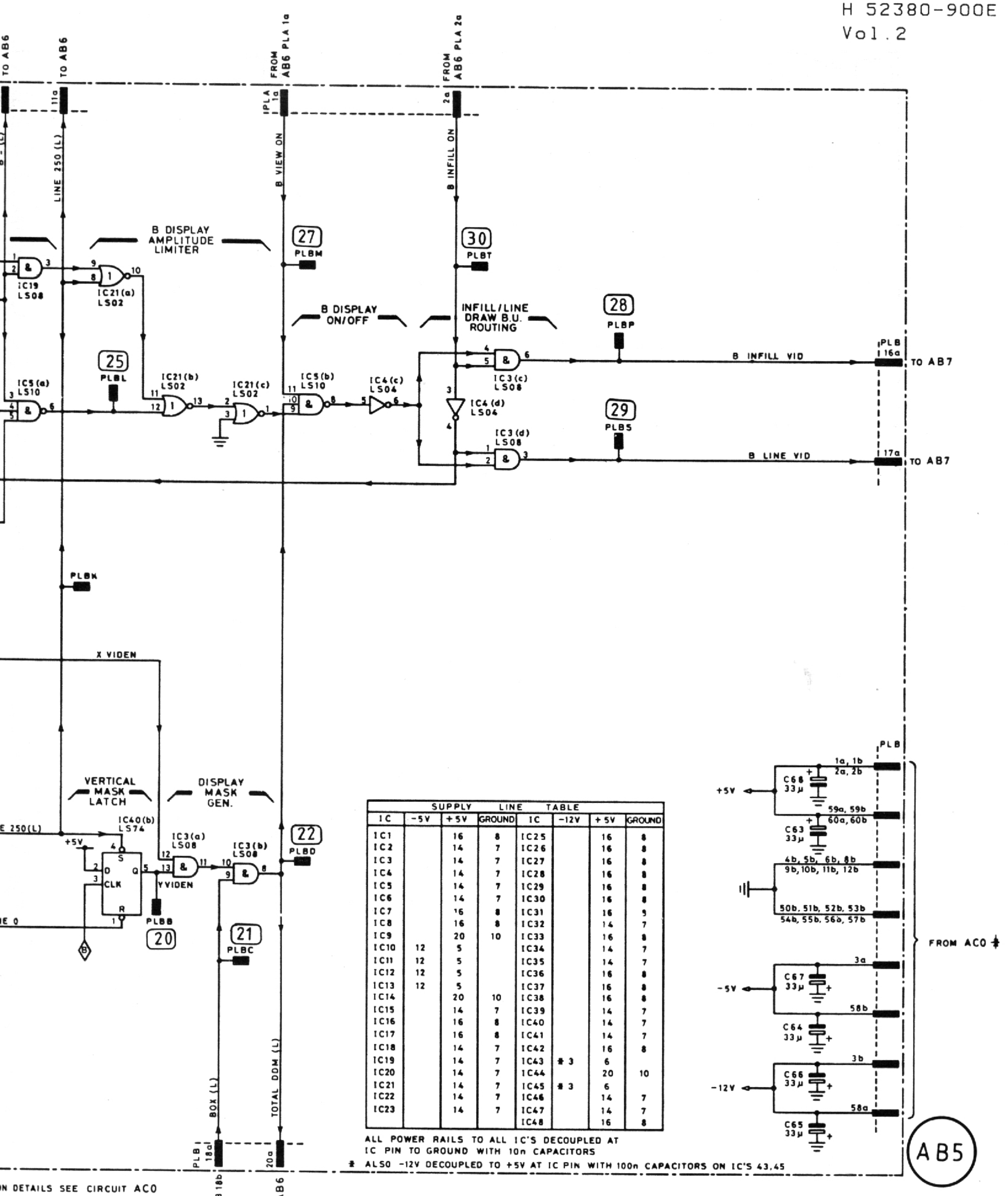
CONTINUED FROM SHEET ONE

18
PLAZ
IC34 LS32
IC41(b) LS74
COUNTERS IC38, IC36, IC37 PRELOADED TO 0111H (273)
PLBA
19
FRAME(L)
VRTC(L)
PLB 48a
PLB 36a
TO AB4 & AB3
FROM AB7 PLB 36a

FOR CONNECTION DETAILS SEE CIRCUIT AC0

Drg.No. Z44828-507B
Sh.2 Iss.1

AB5: Timing & B display dynar



SUPPLY LINE TABLE							
IC	-5V	+5V	GROUND	IC	-12V	+5V	GROUND
IC1		16	8	IC25		16	8
IC2		14	7	IC26		16	8
IC3		14	7	IC27		16	8
IC4		14	7	IC28		16	8
IC5		14	7	IC29		16	8
IC6		14	7	IC30		16	8
IC7		16	8	IC31		16	5
IC8		16	8	IC32		14	7
IC9		20	10	IC33		16	8
IC10	12	5		IC34		14	7
IC11	12	5		IC35		14	7
IC12	12	5		IC36		16	8
IC13	12	5		IC37		16	8
IC14		20	10	IC38		16	8
IC15		14	7	IC39		14	7
IC16		16	8	IC40		14	7
IC17		16	8	IC41		14	7
IC18		14	7	IC42		16	8
IC19		14	7	IC43	# 3	6	
IC20		14	7	IC44		20	10
IC21		14	7	IC45	# 3	6	
IC22		14	7	IC46		14	7
IC23		14	7	IC47		14	7
				IC48		16	8

ALL POWER RAILS TO ALL IC'S DECOUPLED AT IC PIN TO GROUND WITH 10n CAPACITORS

ALSO -12V DECOUPLED TO +5V AT IC PIN WITH 100n CAPACITORS ON IC'S 43,45

BOARD : AB6
KEY OF FUNCTIONS

1 A OR A-B SEL (L)
2 3.125 MHz SHIFT REGISTER GATED CLOCK - Φ_2 TTL
3 3.125 MHz SHIFT REGISTER GATED CLOCK - Φ_2 TTL
4 Φ_{1a} - MOS† SHIFT REGISTER GATED CLOCK
5 Φ_{1b} - MOS† SHIFT REGISTER GATED CLOCK
6 Φ_{2a} - MOS† SHIFT REGISTER GATED CLOCK
7 Φ_{2b} - MOS† SHIFT REGISTER GATED CLOCK
8 WO
9 WE
10 SR CLOCK (6.25 MHz)
11 MOS† SHIFT REGISTER GATED CLOCK
12 MOS† SHIFT REGISTER GATED CLOCK
13 Φ_1 TTL ROOT CLOCK FOR SHIFT REGISTERS
14 Φ_2 TTL ROOT CLOCK FOR SHIFT REGISTERS

continued opposite Fig. 18

1 BOARD : AB6

FUNCTION : A OR A-B SEL (L).

TEST POINT : PLAA
GROUND POINT : C41 (end adjacent to C40)
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE ; 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for LOW (TTL) pulses, 1.4 µs long, occurring approx. every 64 µs (±15 µs).

2 BOARD : AB6

FUNCTION : 3.125 MHz SHIFT REGISTE

TEST POINT : PLAB
GROUND POINT : C35 (end adjacent t
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual,
Delay set to minimum

NOTE. Use scope hood or storage

PROCEDURE :

1. Press [PRESET]. Check scope
times refer to trigger point)
From 0 - 16 µs - st
From 16 µs - 56 µs - TT
From 56 µs - 80 µs - st
From 80 µs - 120 µs - TT
From 120 µs - 144 µs - st

2. *To examine the 3.125 MHz clock
and adjust delay trigger level
timebase to 200 ns/DIV. Chec

3 BOARD : AB6

FUNCTION : 3.125 MHz SHIFT REGISTE

TEST POINT : PLAC
GROUND POINT : C35 (end adjacent to
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual,
Delay set to minimum

NOTE. Use scope hood or storage

PROCEDURE :

1. Press [PRESET]. Check scope
times refer to trigger point)
From 0 - 16 µs - st
From 16 µs - 56 µs - T
From 56 µs - 80 µs - st
From 80 µs - 120 µs - T
From 120 µs - 144 µs - st

2. *To examine the 3.125 MHz clock
and adjust delay trigger level
timebase to 200 ns/DIV. Chec

Fig. 17A
Chap. 7
Page 46

Fig. 18

2 BOARD : AB6

FUNCTION : 3.125 MHz SHIFT REGISTER GATED CLOCK - Φ_2 TTL.

TEST POINT : PLAB
GROUND POINT : C35 (end adjacent to PLAB)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1, +ve
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Check scope CH1 waveform for the following (assume times refer to trigger point) :

From 0 - 16 µs - steady TTL state (HIGH or LOW).
From 16 µs - 56 µs - TTL clock at 3.125 MHz.*
From 56 µs - 80 µs - steady TTL state (LOW or HIGH).
From 80 µs - 120 µs - TTL clock at 3.125 MHz.*
From 120 µs - 144 µs - steady TTL state (HIGH or LOW).

2. *To examine the 3.125 MHz clock in detail, set scope to delayed sweep and adjust delay trigger level to obtain display, then turn down delay timebase to 200 ns/DIV. Check for symmetrical TTL clock, period 0 320 ns.

4 BOARD : AB6

FUNCTION : Φ_{1a} - MOS† SHIFT REGISTER GATED

TEST POINT : PLAD
GROUND POINT : C35 (end adjacent to PLAB)
SCOPE SETTING
CH1 : 5 V/DIV
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1, +ve
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Check scope CH1 wav
times refer to trigger point):

From 0 - 16 µs - steady m.
From 16 µs - 56 µs - m.o.s. cl
From 56 µs - 80 µs - steady m.
From 80 µs - 120 µs - m.o.s. cl
From 120 µs - 144 µs - steady m.

2. *To examine the 3.125 MHz clock in det
and adjust delay trigger level to obt
timebase to 200 ns/DIV. Check for L
(±20 ns), period = 320 ns.

†MOS levels are HIGH = 5 volts, LOW =

3 BOARD : AB6

FUNCTION : 3.125 MHz SHIFT REGISTER GATED CLOCK - Φ_2 TTL.

TEST POINT : PLAC
GROUND POINT : C35 (end adjacent to PLAB)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1, +ve
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Check scope CH1 waveform for the following (assume times refer to trigger point):

From 0 - 16 µs - steady TTL state (HIGH or LOW).
From 16 µs - 56 µs - TTL clock at 3.125 MHz.*
From 56 µs - 80 µs - steady TTL state (LOW or HIGH).
From 80 µs - 120 µs - TTL clock at 3.125 MHz.*
From 120 µs - 144 µs - steady TTL state (HIGH or LOW).

2. *To examine the 3.125 MHz clock in detail, set scope to delayed sweep and adjust delay trigger level to obtain display, then turn down delay timebase to 200 ns/DIV. Check for symmetrical TTL clock period = 320 ns.

5 BOARD : AB6

FUNCTION : Φ_{1b} - MOS† SHIFT REGISTER GATE

TEST POINT : PLAE
GROUND POINT : C35 (end adjacent to PLAB)
SCOPE SETTING
CH1 : 5 V/DIV
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Check scope CH1 wav
times refer to trigger point):

From 0 - 16 µs - steady m.o
From 16 µs - 56 µs - m.o.s. clo
From 56 µs - 80 µs - steady m.o
From 80 µs - 120 µs - m.o.s. clo
From 120µs - 144 µs - steady m.o

2. *To examine the 3.125 MHz clock in det
and adjust delay trigger level to obt
timebase to 200 ns/DIV. Check for L
(±20 ns), period = 320 ns.

†MOS levels are HIGH = 5 volts, LOW =

Waveforms for AB6

GATED CLOCK.

LAB)

, +ve

pe.

l waveform for the following (assume

dy m.o.s. state (HIGH).
s. clock at 3.125 MHz.*
dy m.o.s. state (HIGH).
s. clock at 3.125 MHz.*
dy m.o.s. state (HIGH).

n detail, set scope to delayed sweep
o obtain display, then turn down delay
for LOW (m.o.s.) pulses, length = 100 ns

OW = -12 volts.

6 BOARD : AB6

FUNCTION : Φ_{2a} - MOS† SHIFT REGISTER GATED CLOCK.

TEST POINT : PLAH
GROUND POINT : C35 (end adjacent to PLAB)
SCOPE SETTING
CH1 : 5 V/DIV
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1, +ve
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Check scope CH1 waveform for the following (assume times refer to trigger point):

From 0 - 16 µs - steady m.o.s. state (HIGH).
From 16 µs - 56 µs - m.o.s. clock at 3.125 MHz.*
From 56 µs - 80 µs - steady m.o.s. state (HIGH)
From 80 µs - 120 µs - m.o.s. clock at 3.125 MHz.*
From 120 µs - 144 µs - steady m.o.s. state (HIGH).

2. *To examine the 3.125 MHz clock in detail, set scope to delayed sweep and adjust delay trigger level to obtain display, then turn down delay timebase to 200 ns/DIV. Check for LOW (m.o.s.) pulses, length = 100 ns (±20 ns), period = 320 ns.

†MOS levels are HIGH = +5 volts, LOW = -12 volts.

GATED CLOCK.

LAB)

pe.

l waveform for the following (assume

y m.o.s. state (HIGH).
. clock at 3.125 MHz.*
y m.o.s. state (HIGH).
. clock at 3.125 MHz.*
y m.o.s. state (HIGH).

n detail, set scope to delayed sweep
o obtain display, then turn down delay
for LOW (m.o.s.) pulses, length = 100 ns

OW = -12 volts.

7 BOARD : AB6

FUNCTION : Φ_{2b} - MOS† SHIFT REGISTER GATED CLOCK.

TEST POINT : PLAJ
GROUND POINT : C35 (end adjacent to PLAB)
SCOPE SETTING
CH1 : 5 V/ DIV
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1, +ve
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Check scope CH1 waveform for the following (assume times refer to trigger point):

From 0 - 16 µs - steady m.o.s. state (HIGH)
From 16 µs - 56 µs - m.o.s. clock at 3.125 MHz.*
From 56 µs - 80 µs - steady m.o.s. state (HIGH).
From 80 µs - 120 µs - m.o.s. clock at 3.125 MHz.*
From 120 µs - 144 µs - steady m.o.s. state (HIGH).

2. *To examine the 3.125 MHz clock in detail, set scope to delayed sweep and adjust delay trigger level to obtain display, then turn down delay timebase to 200 ns/DIV. Check for LOW(m.o.s.) pulses, length = 100 ns (±20 ns), period = 320 ns.

†MOS levels are HIGH = +5 volts, LOW = -12 volts.

Fig. 17A

May 86

8 BOARD : AB6

FUNCTION : WO.

TEST POINT : PLAK
GROUND POINT : C36 (end adjacent to PLAK)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2
MAIN TIMEBASE : 5 ms/DIV
MODE : CH1, CH2, ALT

PROCEDURE :

1. Press [PRESET]. Check for a HIGH (TTL) pulse on CH1, occurring on alternate rising (+ve) edges on CH2.

2. Select the appropriate edge of CH2 on the scope trigger, and turn the main timebase to 20 µs/DIV. Check the HIGH (TTL) pulse timings.

Trigger to CH1↑ = 120 µs
CH1↑ to CH1↓ = 23 µs

NOTE.

There will also be much shorter HIGH (TTL) pulses on CH1, but these should be invisible at these scope settings.

9 BOARD : AB6

FUNCTION : WE.

TEST POINT : PLAL
GROUND POINT : C6 (end adjacent to C5)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2
MAIN TIMEBASE : 5 ms/DIV
MODE : CH1, CH2, ALT

PROCEDURE :

1. Press [PRESET]. Check for a HIGH (TT
after alternate +ve edges on CH2.

2. Select the appropriate edge of CH2 on
main timebase to 20 µs/DIV. Check th

Trigger to CH1↑ =
CH1↑ to CH1↓ =

NOTE.

There will also be much shorter HIGH (
should be invisible at these scope set

10 BOARD : AB6

FUNCTION : SR CLOCK (6.25 MHz).

TEST POINT : PLAM
GROUND POINT : C42 (end adjacent to C52)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
MAIN TIMEBASE : 20 µs/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Check for a TTL wavel

From 0 - 16 µs - LOW (TTL) st
*16 µs - 56 µs - TTL clock (s
56 µs - 80 µs - LOW (TTL) st
*80 µs - 120 µs - TTL clock

2. *To check the period of the 6.25 MHz cl
and main timebase to 50 ns per box.

end adjacent to C5)

on IC8 pin 14

: 5 ms/DIV
2, ALT

. Check for a HIGH (TTL) pulse on CH1, occurring just
e +ve edges on CH2.

ropriate edge of CH2 on the scope trigger, and turn the
to 20 µs/DIV. Check the HIGH (TTL) pulse timings.

Trigger to CH1↑ = 57 µs
CH1↑ to CH1↓ = 23 µs

o be much shorter HIGH (TTL) pulses on CH1, but these
sible at these scope settings.

(6.25 MHz).

(end adjacent to C52)

on IC8 pin 14
: 20 µs/DIV
y

. Check for a TTL waveform as follows :

- 16 µs - LOW (TTL) state
s - 56 µs - TTL clock (symmetrical) at 6.25 MHz
s - 80 µs - LOW (TTL) state
s - 120 µs - TTL clock (symmetrical) at 6.25 MHz

eriod of the 6.25 MHz clock, change scope trigger to CH1, +ve,
ase to 50 ns per box. Period should be 160 ns.

11 BOARD : AB6

FUNCTION : MOS† SHIFT REGISTER GATED CLOCK.

TEST POINT : PLBS
GROUND POINT : C35 (end adjacent to PLAB)
SCOPE SETTING
CH1 : 5 V/DIV
CH2 : 2 V/DIV on IC8 pin 1
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1, +ve
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Check scope CH1 waveform for the following (assume times refer to trigger point).

From 0 - 80 µs - steady m.o.s. state (HIGH)
From 80 µs - 120 µs - m.o.s. clock at 3.125 MHz*
From 120 µs - 144 µs - steady m.o.s. state (HIGH)
From 144 µs - 184 µs - m.o.s. clock at 3.125 MHz*
From 184 µs - 208 µs - steady m.o.s. state (HIGH)

2. *To examine the 3.125 MHz clock in detail, set scope to delayed sweep and adjust delay trigger level to obtain display, then turn down delay timebase to 200 ns/DIV. Check for LOW (m.o.s.) pulses, length = 100 ns (±20 ns), period = 320 ns.

†MOS levels are HIGH = 5 volts, LOW = -12 volts.

12 BOARD : AB6

FUNCTION : MOS† SHIFT REGISTER GATED CLOCK.

TEST POINT : PLBT
GROUND POINT : C35 (end adjacent to PLAB)
SCOPE SETTING
CH1 : 5 V/DIV
CH2 : 2 V/DIV on IC8 pin 1
TRIGGER : CH2, +ve
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1, +ve
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Check scope CH1 waveform for the following (assume times refer to trigger point):

From 0 - 80 µs - steady m.o.s. state (HIGH)
From 80 µs - 120 µs - m.o.s. clock at 3.125 MHz*
From 120 µs - 144 µs - steady m.o.s. state (HIGH)
From 144 µs - 184 µs - m.o.s. clock at 3.125 MHz*
From 184 µs - 208 µs - steady m.o.s. state (HIGH)

2. *To examine the 3.125 MHz clock in detail, set scope to delayed sweep and adjust delay trigger level to obtain display, then turn down delay timebase to 200 ns/DIV. Check for LOW (m.o.s. pulses, length = 100 ns (±20 ns) , period = 320 ns.

†MOS levels are HIGH = 5 volts, LOW = -12 volts.

Waveforms for AB6

GATED CLOCK.

nt to PLAB)

1

al, CH1, +ve

age scope.

cope CH1 waveform for the following (assume
int).

- steady m.o.s. state (HIGH)
- m.o.s. clock at 3.125 MHz*
- steady m.o.s. state (HIGH)
- m.o.s. clock at 3.125 MHz*
- steady m.o.s. state (HIGH)

clock in detail, set scope to delayed sweep
level to obtain display, then turn down delay
Check for LOW (m.o.s.) pulses, length = 100 ns
s.

olts, LOW = -12 volts.

13 BOARD : AB6

FUNCTION : Φ_1 TTL ROOT CLOCK FOR SHIFT REGISTERS.

TEST POINT : PLBV
GROUND POINT : C37 (end adjacent to C36)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve, manual
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1, +ve
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Check scope CH1 waveform for the following (times are referred to trigger point):

0	-	16 µs	- steady (TTL) high
16 µs	-	56 µs	- TTL clock at 3.125 MHz
56 µs	-	80 µs	- steady (TTL) HIGH
80 µs	-	120 µs	- TTL clock at 3.125 MHz

2. To check the 3.125 MHz clock in detail set scope to delayed sweep and adjust delay trigger to obtain display, then turn down delay timebase to 200 ns/DIV. Check for HIGH (TTL) pulses, 80 - 90 ns long every 320 ns.

GATED CLOCK.

t to PLAB)

1

al, CH1, +ve

age scope.

cope CH1 waveform for the following (assume
int):

- steady m.o.s. state (HIGH)
- m.o.s. clock at 3.125 MHz*
- steady m.o.s. state (HIGH)
- m.o.s. clock at 3.125 MHz*
- steady m.o.s. state (HIGH)

lock in detail, set scope to delayed sweep
evel to obtain display, then turn down delay
Check for LOW (m.o.s. pulses, length = 100 ns
.

lts, LOW = -12 volts.

14 BOARD : AB6

FUNCTION : Φ_2 TTL ROOT CLOCK FOR SHIFT REGISTERS.

TEST POINT : PLBW
GROUND POINT : C39 (end adjacent to C38)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : CH2, +ve, manual
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Main timebase only
Delay trigger : manual, CH1, +ve
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

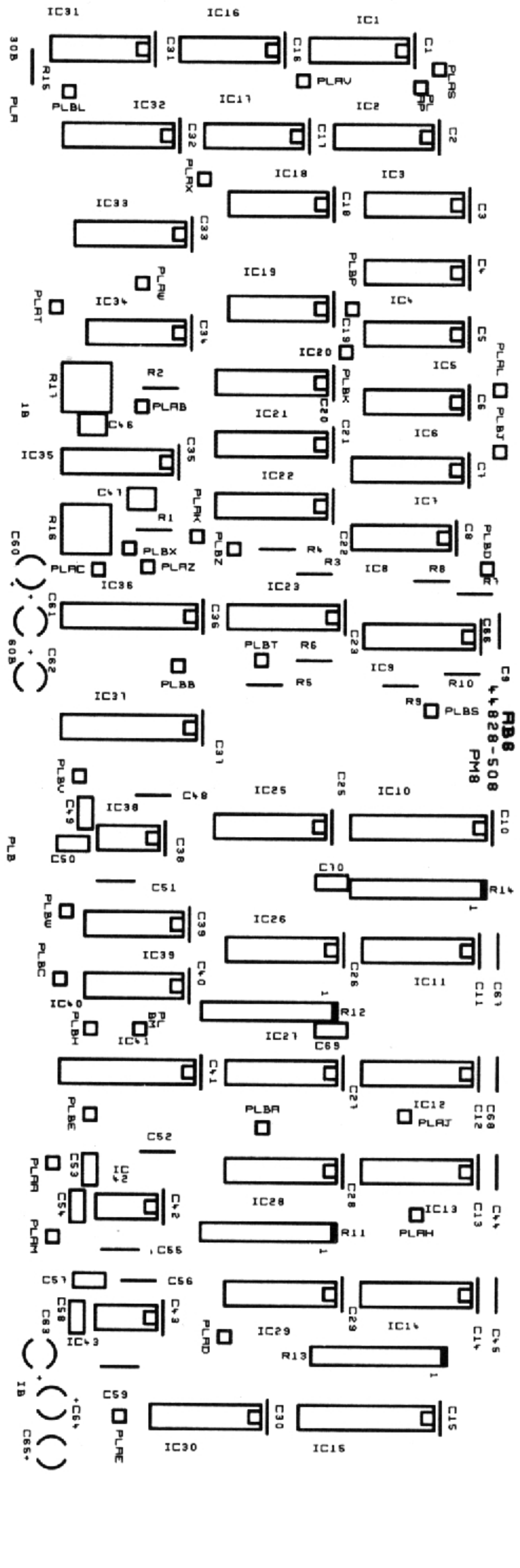
1. Press [PRESET]. Check scope CH1 waveform for the following (times are referred to trigger point):

0	-	16 µs	- steady (TTL) HIGH
16 µs	-	56 µs	- TTL clock at 3.125 MHz
56 µs	-	80 µs	- steady (TTL) HIGH
80 µs	-	120 µs	- TTL clock at 3.125 MHz

2. To check the 3.125 MHz clock in detail, set scope to delayed sweep and adjust delay trigger to obtain display, then turn down delay timebase to 200 ns/DIV. Check for HIGH (TTL) pulses, 80 - 90 ns long every 320 ns.

Fig. 17B

May 86



Component layout for AB6

Fig. 17
May 86

PART OF
AB6
44828-508K

FROM AB5 PLA 4a
FROM AB5 PLA 3a
PLA 4a
3a
2TTL
1TTL

DUAL 2 PHASE CLOCK DRIVER

+5V
R2 3k3
R17 10k
SET #1 PULSE WIDTH
C46 10p
IC35(a) LS221
CX RX 2A 2Q 2B R
PLBV
C57 180p
C58 180p
IC43 0026
IN A OUT A IN B OUT B
PLAD
PLAE
#1a
#2a

IC29 LS157
D0 D3 1B 2B 3B 4B 1A 2A 3A 4A 1Y 2Y 3Y 4Y S G

NEW

IC28 LS157
IC27 LS157
IC26 LS157

A DEMUX LATCH

FROM AB4 PLB 19a
PLB 19b
A OR A-B SEL (L)
PLAA
IC41 LS273
CLK LATCH CLR
MULTIPLEXED PROCESSED DISPLAY DATA
FROM AB4 PLB
23b 24b 25b 26b 27b 28b 29b 30b
23a 24a 25a 26a 27a 28a 29a 30a
D0 D7

+5V
R1 3k3
R16 10k
SET #2 PULSE WIDTH
C47 10p
IC35(b) LS221
PLBW
C53 180p
C54 180p
IC42 0026
PLAH
PLAJ
#1b
#2b

AUTOTEST INVERTER
+5V
R15 2k2
PLA 29b
30b
ATR (L)
IC31(d) LS04
A
B

GRAT. INPUT LATCH
IC37 LS273
IC23 LS157

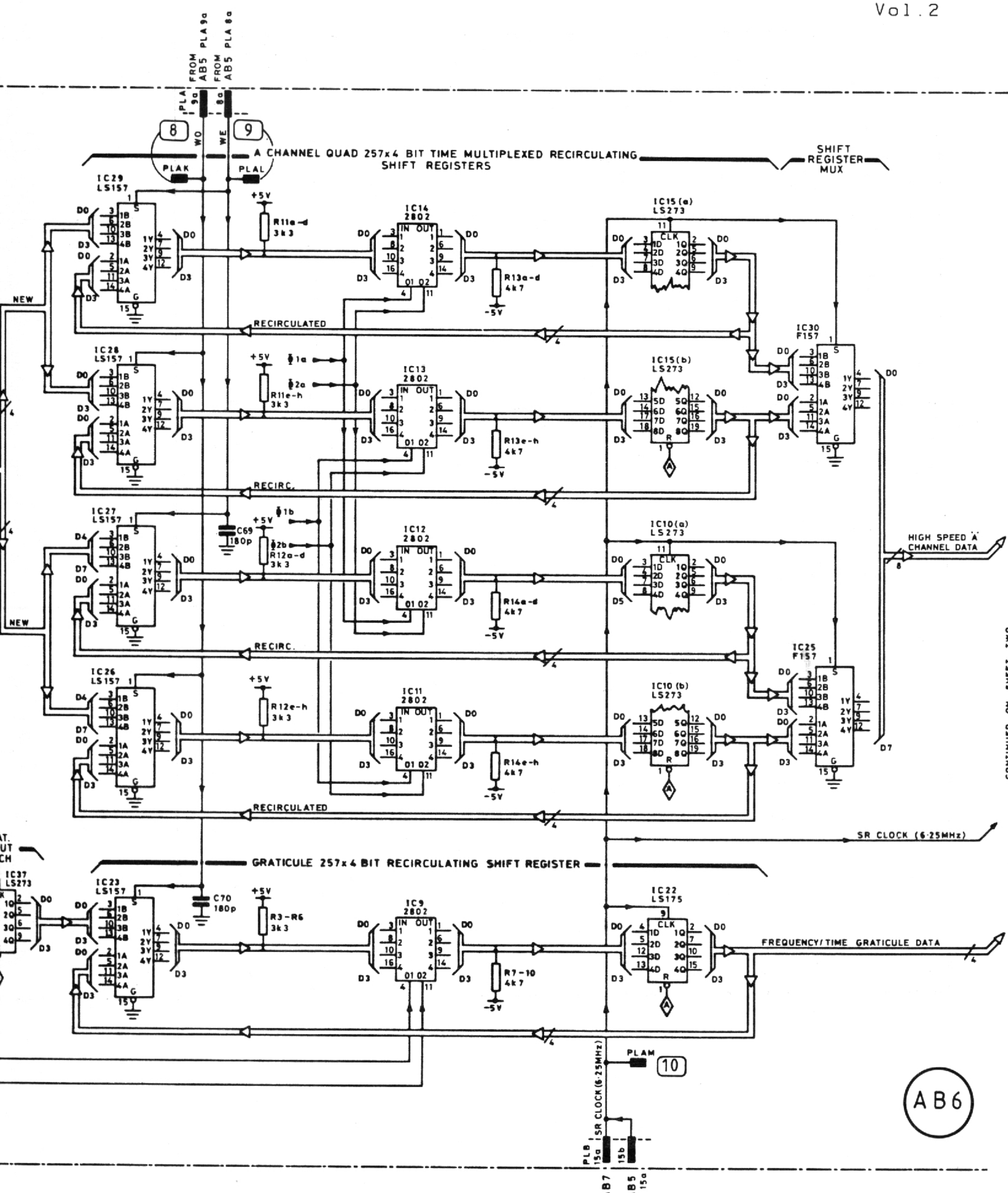
FROM AB3 PLB
PLB 50a 51a 52a 53a 54a 55a 56a 57a
50a 51a 52a 53a 54a 55a 56a 57a
D0 D7

I/O DATA BUS TO SHEET 2

PLBT
PLBS
IC38 0026
C49 180p
C50 180p

Drg.No. Z44828-508K
Sh.1 Iss.1

AB6: Graticule & A displa


FROM AB5 PLA 9a
FROM AB5 PLA 8a
PLA 9a
8a
8
WO
WE
9
A CHANNEL QUAD 257x4 BIT TIME MULTIPLEXED RECIRCULATING SHIFT REGISTERS
SHIFT REGISTER MUX
PLAK
PLAL
IC29 LS157
+5V
R11a-d 3k3
IC14 2802
IC15(a) LS273
R13a-d 4k7
-5V
NEW
RECIRCULATED
IC28 LS157
R11e-h 3k3
IC13 2802
IC15(b) LS273
R13e-h 4k7
IC30 F157
RECIRC.
IC27 LS157
C69 180p
1b
2b
R12a-d 3k3
IC12 2802
IC10(a) LS273
R14a-d 4k7
HIGH SPEED A CHANNEL DATA
IC26 LS157
R12e-h 3k3
IC11 2802
IC10 (b) LS273
R14e-h 4k7
IC25 F157
CONTINUED ON SHEET TWO
SR CLOCK (6·25MHz)
GRATICULE 257x4 BIT RECIRCULATING SHIFT REGISTER
IC37 LS273
IC23 LS157
C70 180p
R3-R6 3k3
IC9 2802
IC22 LS175
R7-10 4k7
FREQUENCY/TIME GRATICULE DATA
PLAM
10
PLB 15a
SR CLOCK (6·25MHz)
15b
TO AB7
FROM AB5 PLB 15a
AB6

BOARD : AB6
KEY OF FUNCTIONS (concluded)

15 OUTPUT FROM A DATA/LINE COUNT COMPARATOR
16 OUTPUT FROM A DATA/LINE COUNT COMPARATOR
17 A = (L)
18 LINE 250 (L)
19 A VIEW ON
20 TOTAL DDM (L)
21 GATED OUTPUT OF A DATA/LINE COUNT COMPARATOR
22 A INFILL VID
23 A LINE VID
24 MAJOR VERTICAL GRATICULE
25 MINOR VERTICAL GRATICULE
26 A INFILL ON
27 FLASH RATE
28 ODD/EVEN(L) FLASHING MARKERS
29 MARKER
30 MARKER
31 B = (L)
32 MKR VIDEO
33 CLOCK CONTROL FOR IC36
34 12.5 MHz CLOCK (PHASED)

15 BOARD : AB6

FUNCTION : OUTPUT FROM A DATA/LINE COUNT COMPARATOR.

TEST POINT : PLAS
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : manual, +ve, CH2
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1, CH2 CHOP

PROCEDURE :

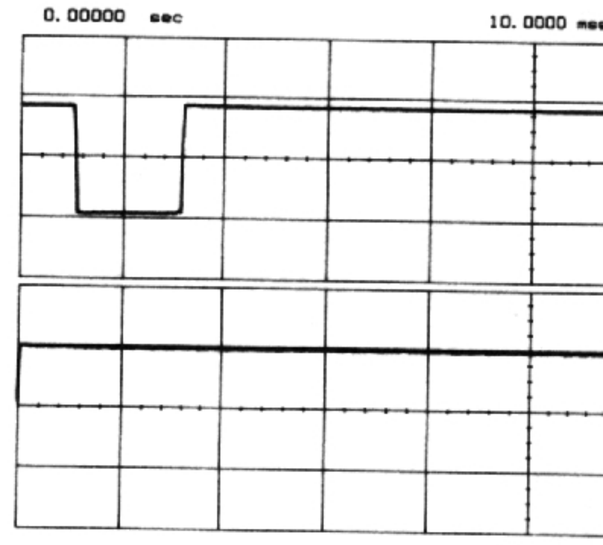
1. Press [PRESET]. Connect tracking generator output to RF input.
Press [TRACK GEN].
Rotate SPAN/DIV to select 10 Hz/DIV.
Adjust scope trigger to obtain display.
Check scope display for two HIGH (TTL) pulses on CH1 during the period that CH2 is (TTL) HIGH.

CH2↑ to CH1↑ = 1.1 ms		All times ±0.2 ms
CH1↑ to CH1↓ = 2.0 ms	1st pulse	
CH1↓ to CH1↑ = 14.6 ms		
CH1↑ to CH1↓ = 1.7 ms	2nd pulse	

See waveform diagram Fig. 15.

16 BOARD : AB6

FUNCTION : OUTPUT FROM A DATA/LINE COUN



TEST POINT : PLAP
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : manual, +ve, CH2
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1, CH2 CHOP

16 continued

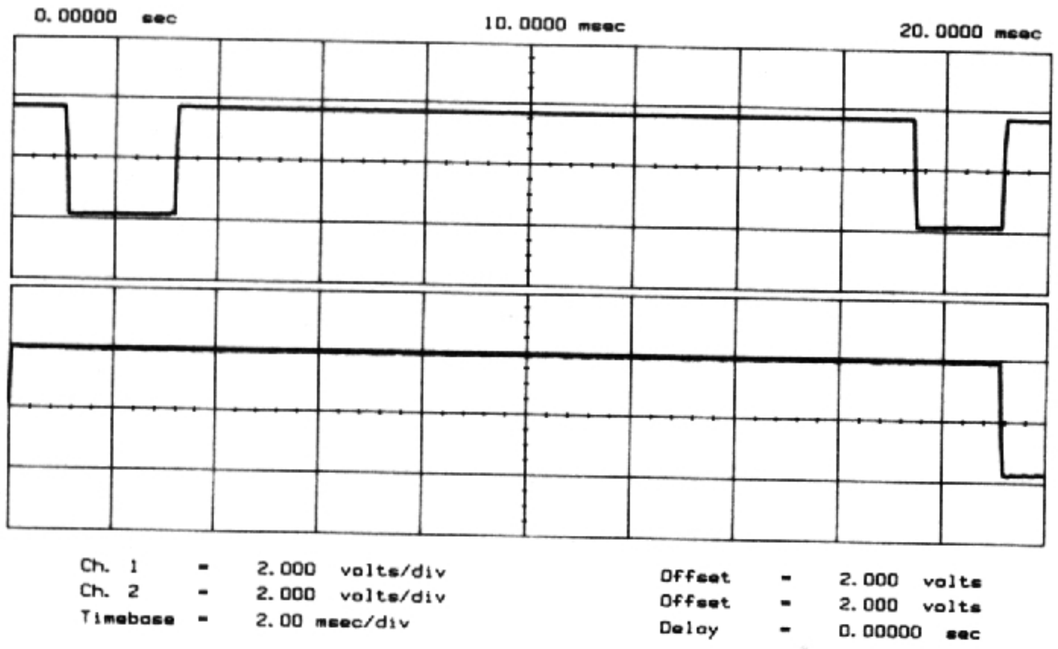
PROCEDURE :

1. Press [PRESET]. Connect tracking
Press [TRACK GEN].
Rotate SPAN/DIV to select 10 Hz/DIV
Adjust scope trigger to obtain disp
Check scope display for two LOW (TT
that CH2 is (TTL) HIGH:

CH2↑ to CH1↓ = 1.1 ms	
CH1↓ to CH1↑ = 2.0 ms	1st
CH1↑ to CH1↓ = 14.6 ms	
CH1↓ to CH1↑ = 1.7 ms	2nd

16 BOARD : AB6

FUNCTION : OUTPUT FROM A DATA/LINE COUNT COMPARATOR.



TEST POINT : PLAP
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : manual, +ve, CH2
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1, CH2 CHOP

16 continued

PROCEDURE :

1. Press [PRESET]. Connect tracking generator output to RF input.
Press [TRACK GEN].
Rotate SPAN/DIV to select 10 Hz/DIV.
Adjust scope trigger to obtain display.
Check scope display for two LOW (TTL) pulses on CH1 during the period that CH2 is (TTL) HIGH:

CH2↑ to CH1↓ = 1.1 ms		All times ±0.2 ms
CH1↓ to CH1↑ = 2.0 ms	1st pulse	
CH1↑ to CH1↓ = 14.6 ms		
CH1↓ to CH1↑ = 1.7 ms	2nd pulse	

17 BOARD : AB6

FUNCTION : A = (L).

TEST POINT : PLAV
GROUND POINT : C2 (end adjacent to PLAS)
SCOPE SETTING
CH2 : 2 V/DIV on PLBA
TRIGGER : manual, +ve, external on IC8 p
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 10 µs/DIV
MODE : CH1, CH2 ALT
Delay trigger : manual, CH2, +ve, D
Delay set to minimum (zero)

PROCEDURE :

1. Press [PRESET]. Connect tracking genera
With main timebase only, adjust main trig
Press [TRACK GEN] 'vertical dB/DIVISION
'delayed sweep only' and adjust delay tri
Adjust scope delay to obtain delayed swee
on CH2. Check that, for the duration of
(40 µs), CH1 is LOW (TTL).

18 BOARD : AB6

FUNCTION : LINE 250 (L).

TEST POINT : PLAT
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 1
TRIGGER : manual, +ve, CH2
MAIN TIMEBASE : 200 µs/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger fo
Check for LOW (TTL) pulse, 64 µs long, oc
(Use x10 sweep facility to check pulse le

19 BOARD : AB6

FUNCTION : A VIEW ON.

TEST POINT : PLAX
GROUND POINT : C33 (end adjacent to C32)
SCOPE SETTING
MAIN TIMEBASE : 10 ms/DIV

PROCEDURE :

1. Press [PRESET]. Check for steady (TTL)

3. Press 'display A [VIEW]'. Check for stea

IC8 pin 14

ve, DC

generator output to RF input.
n trigger level for display.
SION [0.5]'. Select (scope)
ay trigger level to obtain display.
d sweep starting on the last +ve pulse
ion of the HIGH (TTL) pulse on CH2

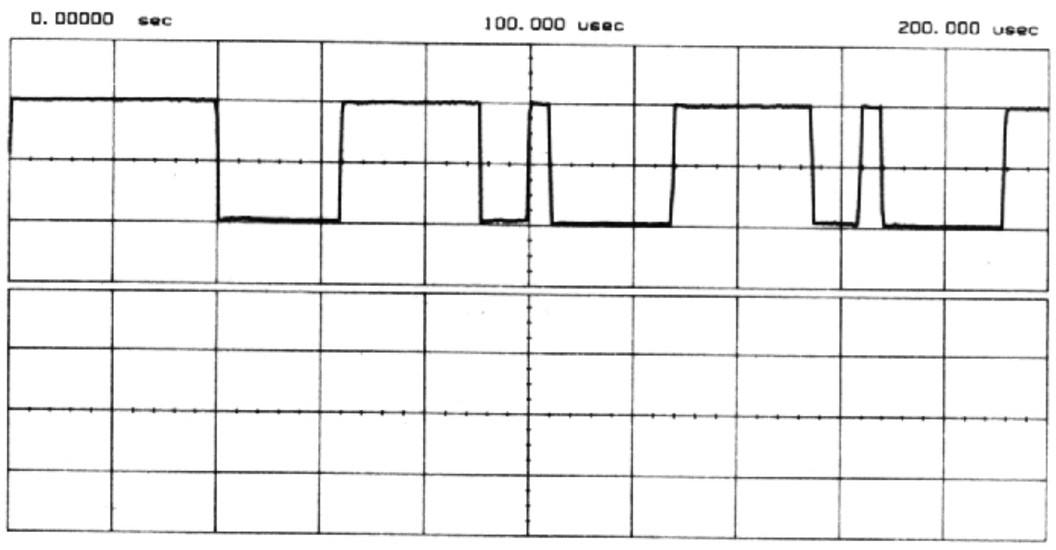
er for display.
g, occurring 1.4 ms after trigger.
se length.)

TTL) HIGH.

steady (TTL) LOW.

20 BOARD : AB6

FUNCTION : TOTAL DDM(L).



TEST POINT : PLBA
GROUND POINT : C28 (end adjacent to C27)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 1
TRIGGER : manual, CH2
MAIN TIMEBASE : 500 µs/DIV
DELAY TIMEBASE : 10 µs/DIV
MODE : CH1 only
Delay trigger : CH1, manual, DC, +ve
Delay set to minimum

20 continued

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger level control to obtain display. Check for a series of HIGH (TTL) pulses starting 2.9 ms after scope trigger.

2. Select delayed sweep facility, and adjust delay trigger level to trigger on the beginning of the pulse series (above). Pulses should be 40 µs HIGH every 64 µs.

3. Press 'display [CAL]' and wait for it to finish (approx. 1 min.). Starting at the beginning of the displayed pulse series, use the 'X position' control to examine each pulse in turn.

First 4 HIGH pulses = 40 µs long
5th HIGH pulse = 27 µs long
6th HIGH pulse = 4 µs long

21 BOARD : AB6

FUNCTION : GATED OUTPUT OF A DATA/LINE COUNT COMPARATOR.

TEST POINT : PLAW
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2 V/DIV on PLAT
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 1 ms/DIV
DELAY TIMEBASE : 10 µs/DIV
MODE : CH1 only
Delay trigger : manual, +ve, CH1, DC
Delay set to minimum
Sweep 'A' intensified by 'B'

PROCEDURE :

1. Press [PRESET].
Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [2] 'enter data display and linearity tests'.
Adjust main trigger level to obtain display.
Adjust delay trigger level so that the delay sweep (intensified) starts on the first HIGH (TTL) pulse.
Switch scope to delay timebase ('B sweep only').
Check for HIGH (TTL) pulses, 25 µs long, occurring every 64 µs.

2. Increase the scope delay from minimum through to maximum and check that the HIGH (TTL) pulses increase in length from 25 µs to 55 µs.

22 BOARD : AB6

FUNCTION : A INFILL VID.

TEST POINT : PLBC
GROUND POINT : C40 (end adjacent to C39)
SCOPE SETTING
CH2 : 2 V/DIV on PLAT
TRIGGER : +ve, manual, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 200 ns/DIV
MODE : CH1 only
Delay trigger : CH1, +ve, DC, manual
Delay set to minimum

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [2] 'enter data display & linearity tests'.
Adjust scope trigger to obtain display.
Check for a TTL pulse sequence, starting rrom the scope trigger, ending after 16 ms, where the pulses (HIGH TTL) increase in length from 320 ns (at the start) to 40 µs (at the end).*

2. *To examine these pulses in detail, switch scope to delay timebase and adjust delay trigger level to obtain display (it will be very dim). Increase delay from minimum and check that the pulses go from 320 ns to 40 µs (max).

23 BOARD : AB6

FUNCTION : A LINE VID.

TEST POINT : PLBB
GROUND POINT : C37 (end adjacent to C36)
SCOPE SETTING
CH2 : 2 V/DIV on PLAT
TRIGGER : +ve, manual, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 50 ns/DIV
MODE :
Delay trigger : CH1, +ve, DC, manua
Delay set to minimum

NOTE. Use a scope hood.

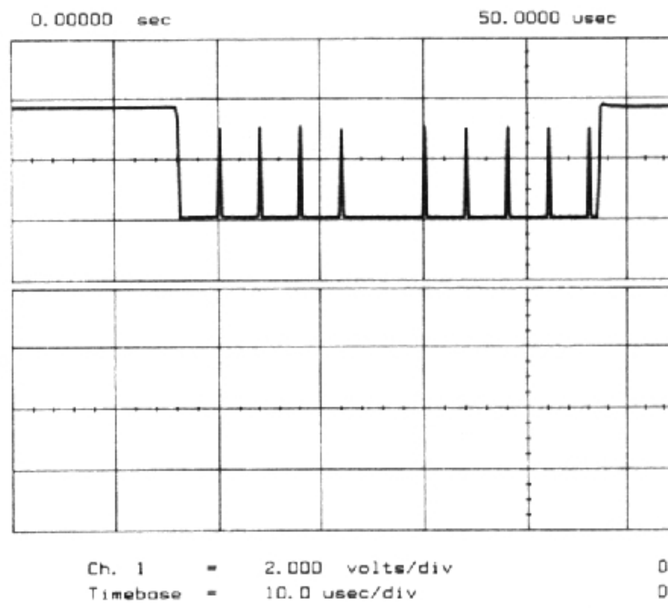
PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS
Select [2] 'upper unit confidence tests'
Select [2] 'enter data display & linear
Press [2ND FUNCT], 'display A [VIEW]'.
Adjust scope trigger to obtain display.
Check for a TTL pulse sequence, starting
ending after 16 ms, where the pulses (H
and 64 µs apart.*

2. *To check the length of these pulses, swi
and adjust delay trigger level to obtain

24 BOARD : AB6

FUNCTION : MAJOR VERTICAL GRATICULE.



TEST POINT : PLBH
GROUND POINT : C41 (end adjacent to C40)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : +ve, CH2, manual
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger f
Check for a repeating sequence of 10 HIG
is 23 µs long, the others are 160 ns lon

Fig. 18B
Chap. 7
Page 52/51

d adjacent to C36)

PLAT
nual, CH2
2 ms/DIV
50 ns/DIV

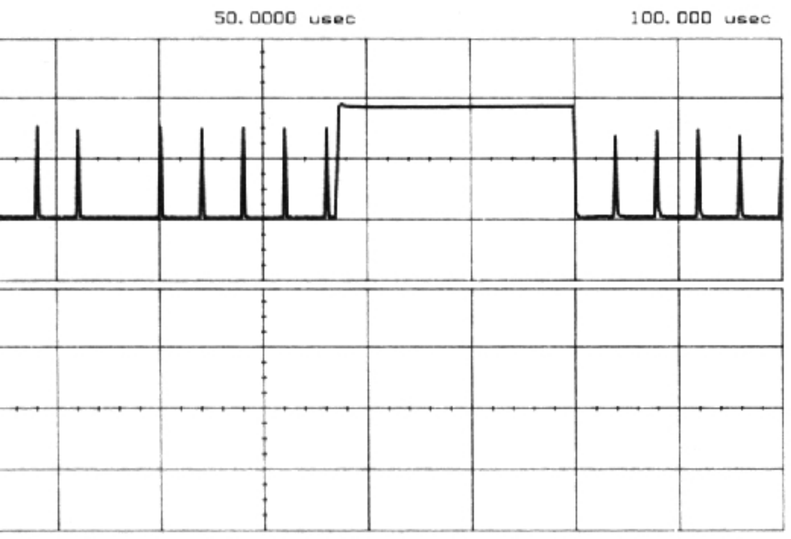
er : CH1, +ve, DC, manual
o minimum

ood.

Enter DEBUG OPERATIONS mode.
r unit confidence tests'.
r data display & linearity tests'.
], 'display A [VIEW]'.
gger to obtain display.
pulse sequence, starting from the scope trigger,
ns, where the pulses (HIGH TTL) are 160 ns long,
*

gth of these pulses, switch to delay timebase,
trigger level to obtain display (it will be very dim).

ICAL GRATICULE.



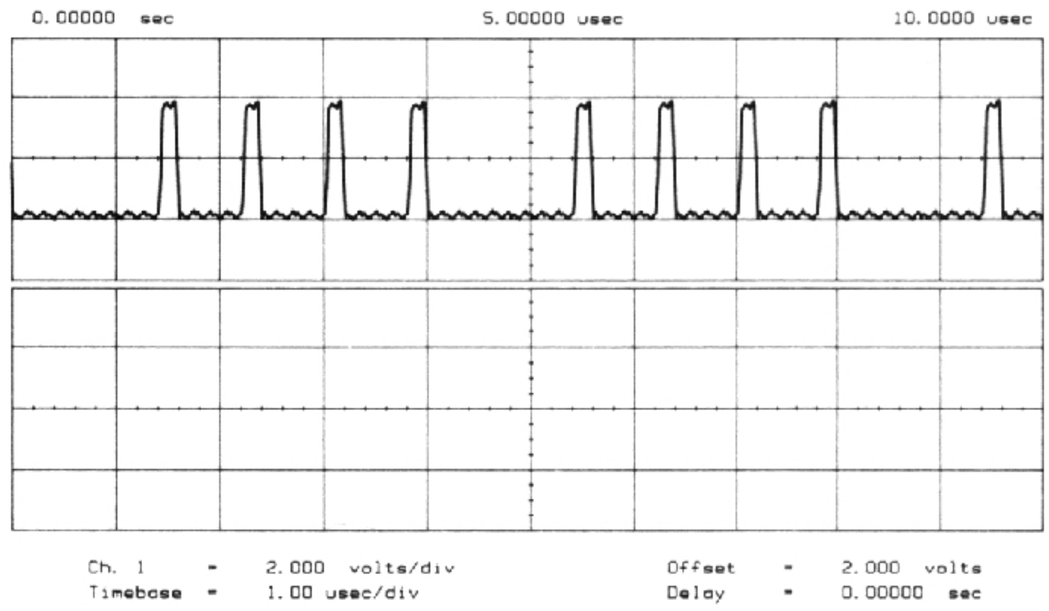
d adjacent to C40)

IC8 pin 14
2, manual
0 µs/DIV

Adjust scope trigger for display.
ting sequence of 10 HIGH (TTL) pulses, where one pulse
e others are 160 ns long.

25 BOARD : AB6

FUNCTION : MINOR VERTICAL GRATICULE.



TEST POINT PLBE
GROUND POINT : C41 (end adjacent to C40)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 14
TRIGGER : +ve, CH2
MAIN TIMEBASE : 5 µs/DIV
DELAY TIMEBASE : 1 µs/DIV
MODE :
Delay trigger : +ve, CH1, manual
Delay set to minimum
Set to 'A intensified by B'

NOTE. Use scope hood or storage scope.

25 continued

PROCEDURE :

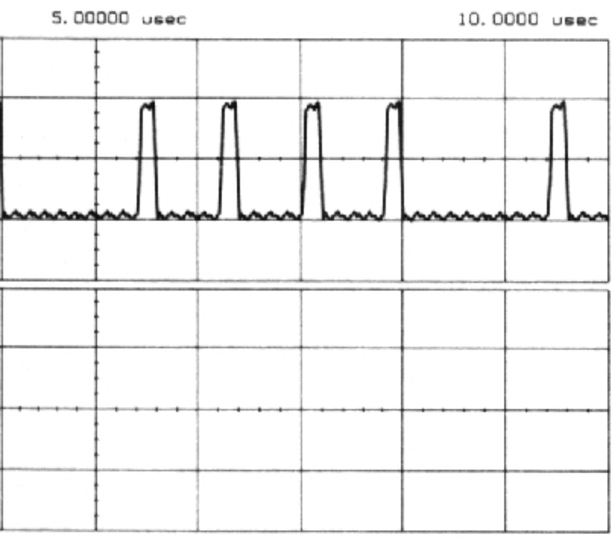
1. Press [PRESET]. Adjust scope trigger to obtain display.
Check for HIGH (TTL) pulses occurring 17 µs after scope trigger.

2. Set scope to B sweep ('delay timebase') only.
Adjust scope delay trigger to obtain display.
Check for repeating sequences of 4 (TTL HIGH) pulses (see waveform dia

3. Change delay timebase to 200 ns/DIV to check HIGH pulse width at 160 ns
pulse spacing (within group of 4 pulses) at 640 ns, and spaces between
pulse groups of 1.6 µs.

Waveforms for AB6

CULE.



: to C40)

CH1, manual

'by B'

ge scope.

cope trigger to obtain display.
s occurring 17 µs after scope trigger.

ay timebase') only.
to obtain display.
nces of 4 (TTL HIGH) pulses (see waveform diagram).

00 ns/DIV to check HIGH pulse width at 160 ns,
p of 4 pulses) at 640 ns, and spaces between

26 BOARD : AB6

FUNCTION : A INFILL ON.

TEST POINT : PLAZ
GROUND POINT : C36 (end adjacent to C35)
SCOPE SETTING
MAIN TIMEBASE : 1 ms/DIV

PROCEDURE :

1. Press [PRESET]. Check for steady (TTL) HIGH.

2. Press '[2ND FUNCT]', 'display A [VIEW]'. Check for steady (TTL) LOW.

27 BOARD : AB6

FUNCTION : FLASH RATE.

TEST POINT : PLBD
GROUND POINT : C9 (end adjacent to PLBD)
SCOPE SETTING
MAIN TIMEBASE : 10 ms/DIV

PROCEDURE :

1. Press [PRESET]. Check for TTL symmetrical clock, period 83 ms.

28 BOARD : AB6

FUNCTION : ODD/EVEN (L) FLASHING MARKERS.

TEST POINT : PLBJ
GROUND POINT : C7 (end adjacent to C6).
SCOPE SETTING
MAIN TIMEBASE : 1 ms/DIV

PROCEDURE :

1. Press [PRESET]. Press 'markers [MKR 1]' and 'markers [1 2 MOVE]'. Check for a steady TTL LOW.

2. Very slowly rotate 'markers MOVE' and check that scope CH1 waveform changes state (should change state 100 times/revolution).

Fig. 18B

May 86

29 BOARD : AB6

FUNCTION : MARKER.

TEST POINT : PLBK
GROUND POINT : C20 (end adjacent to C19)
SCOPE SETTING
CH2 : 2 V/DIV on PLBA
TRIGGER : external on IC8 pin 14, +ve, manual
MAIN TIMEBASE : 200 µs/DIV
DELAY TIMEBASE : 200 ns/DIV
MODE : CH1 only
Delay trigger : CH2, +ve, manual
Delay set to zero

NOTE. Use scope hood.

PROCEDURE :

1. Press [PRESET]. With 'main timebase sweep only' on scope, adjust main scope trigger to obtain display. Set scope to 'delay sweep only' and adjust delay trigger to obtain display (it will be very dim).

30 BOARD : AB6

FUNCTION : MARKER.

TEST POINT : PLBK
GROUND POINT : C20 (end adjacent to C19)
SCOPE SETTING
CH2 : 2 V/DIV on PLBA
TRIGGER : +ve, manual, external on IC8 pin 14
MAIN TIMEBASE : 200 µs/DIV
DELAY TIMEBASE : 5 µs/DIV
MODE : CH1 only
Set delay to zero (minimum)
Delay trigger to : +ve, CH2, manual

PROCEDURE :

1. Press [PRESET]. Press 'markers [MKR 1]'.
With main timebase sweep selected, adjust main trigger level for display.
Change to delay timebase sweep, and adjust delay trigger level for display.
Check scope CH1 for very narrow (TTL) pulse occurring approx. 20 µs after start of sweep (scope).

2. Press 'markers [1 2 MOVE]' and rotate 'markers MOVE' approx. 1 turn.
Check that pulse moves correspondingly.

3. To check pulse width, rotate 'markers MOVE' counter-clockwise (5 turns or so) to move the marker to the left-hand edge of the display. Change scope delay timebase to 200 ns/DIV and pulse (HIGH) should be seen to be 100 ns (±20 ns) long.

31 BOARD : AB6

FUNCTION : B = (L).

TEST POINT : PLBL
GROUND POINT : C32 (end adjacent to C31)
SCOPE SETTING
CH2 : 2 V/DIV on PLBA
TRIGGER : manual, +ve, external on IC8 pin 1
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 10 µs/DIV
MODE : CH1, CH2 alt
Delay trigger : manual, CH2, +ve, DC
Delay set to minimum (zero)

PROCEDURE :

1. Press [PRESET]. Connect tracking generator
With main timebase only, adjust main trigger
Press [TRACK GEN] 'vertical [A B SELECT]', '
'display A [VIEW]', 'display B [VIEW]'.
Select (scope) 'delayed sweep only' and adju
obtain display. Adjust scope delay to obta
on the last +ve pulse on CH2.
Check that, for the duration of the HIGH (TT
CH1 is LOW (TTL).

32 BOARD : AB6

FUNCTION : MKR VIDEO.

TEST POINT : PLBM
GROUND POINT : C40 (end adjacent to C39)
SCOPE SETTING
CH2 : 2 V/DIV on PLBA
TRIGGER : manual, +ve, external on IC8 pin 1
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 10 µs/DIV
MODE : CH1, CH2 alt
Delay trigger : manual, CH1, +ve, DC
Delay set to minimum (zero)

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mo
Select [2] 'upper unit confidence tests'.
Select [2] 'enter data display and linearity
Press 'markers [MKR 1]', 'markers [1 2 MOVE]
Adjust scope trigger level to obtain scope
timebase sweep only'. Select 'delay sweep
delay trigger level to obtain display. Che
trigger to CH2↓ = 20 µs.

2. Rotate 'markers MOVE', and check that this p
change in the time interval defined above.

t to C31)

ernal on IC8 pin 14

l, CH2, +ve, DC
(zero)

tracking generator output to r.f. input.
djust main trigger level for display.
l [A B SELECT]', 'vertical dB/DIVISION [0.5]',
ay B [VIEW]'.
eep only' and adjust delay trigger level to
cope delay to obtain delayed sweep starting
H2.
on of the HIGH (TTL) pulse on CH2 (40 µs),

t to C39)

ernal on IC8 pin 14

l, CH1, +ve, DC
(zero)

BUG OPERATIONS mode.
fidence tests'.
play and linearity tests'.
markers [1 2 MOVE]'.
to obtain scope display, with 'main
lect 'delay sweep only', and adjust
ain display. Check the time interval -

check that this produces a corresponding
l defined above.

33 BOARD : AB6

FUNCTION : CLOCK CONTROL FOR IC36.

TEST POINT : PLBP
GROUND POINT : C20 (end adjacent to C19)
SCOPE SETTING
TRIGGER : -ve, manual, CH
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for TTL LOW pulses, 450 ns long (±80 ns) (occurrence asynchronous, but at least 10 per second).

34 BOARD : AB6

FUNCTION : 12.5 MHz CLOCK (PHASED).

TEST POINT : PLBZ
GROUND POINT : C22 (end adjacent to C19)
SCOPE SETTING
MAIN TIMEBASE : 20 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for symmetrical TTL clock, period 80 ns.

rms for AB6

Fig. 18C

May 86

PART OF
AB6
44828-508K

FROM AB5 PLB 12a 13a 14a 15a 16a 17a 18a 19a

PLA 12a 13a 14a 15a 16a 17a 18a 19a

D0 D7

+5V

IC33 S85

IC32 S85

D0 D3 D4 D7

LINE COUNT BUS

HIGH SPEED A CHANNEL DATA

FROM AB5 PLB 11a

PLA 11a

LINE 250(L)

A LINE DRAW AND A INFILL BRIGHT UP GENERATION

IC18(d) LS08

IC2(a) LS00

CURRENT ORDINATE LATCHES

PREVIOUS ORDINATE LATCHES

16 PLAP

IC1(a) LS74

IC3(a) LS74

IC2(b)

IC17(a) LS10

15 PLAS

IC1(b) LS74

IC3(b)

IC2(c)

1(D2)

MARKER DECODER

A=(L)

PLAV 17

SR CLOCK (6·25MHz)

IC31(b) LS04

IC6(a) LS32

IC31(e) LS04

IC6(d)

IC7 LS155

IC6(b)

IC6(c)

IC4(b) LS32

IC4(d)

IC5 LS30

29 30 PLBK

MARKER

PLBX

D0 D1 FLASH RATE

CONTINUED FROM SHEET ONE

FREQUENCY / TIME GRATICULE DATA

IC21 LS175

PLBJ 28

ODD / EVEN (L) FLASHING MARKERS

A/B MKRS

GRATICULE DECODER

IC19(d) LS04

IC18(a) LS08

DASHED MAJOR GRAT

IC20 LS155

IC19(c)

MAJOR GRAT

IC4(a) LS32

PLBH 24

IC36 LS273

I/O DATA BUS FROM SHEET 1

PLBZ 34

TO IC40 PIN 3

IC19(a) LS04

FLASH RATE DIVIDER

IC19(b)

PLBE 25

IC4(c)

33 PLBP

IC8 LS93

PLBD 27

PHASED 12·5MHz CLOCK

VRTC(L)

MINOR VERT. GRAT.

MAJOR VERT. GRAT.

CS1B (L)

A0

READ-IN BRIGHT UP ON

GRAT. ON

B INFILL ON

B VIEW ON

PLB1 32a 32b 36a 24a 25a 39a 4a 21a 19a PLB 1a 2a

FROM AB7 PLB 32b

TO AB5

FROM AB7 PLB 36a

TO AB7

TO AB7

FROM AB3 PLB 39a

FROM AB3 PLB 4a

TO AB7

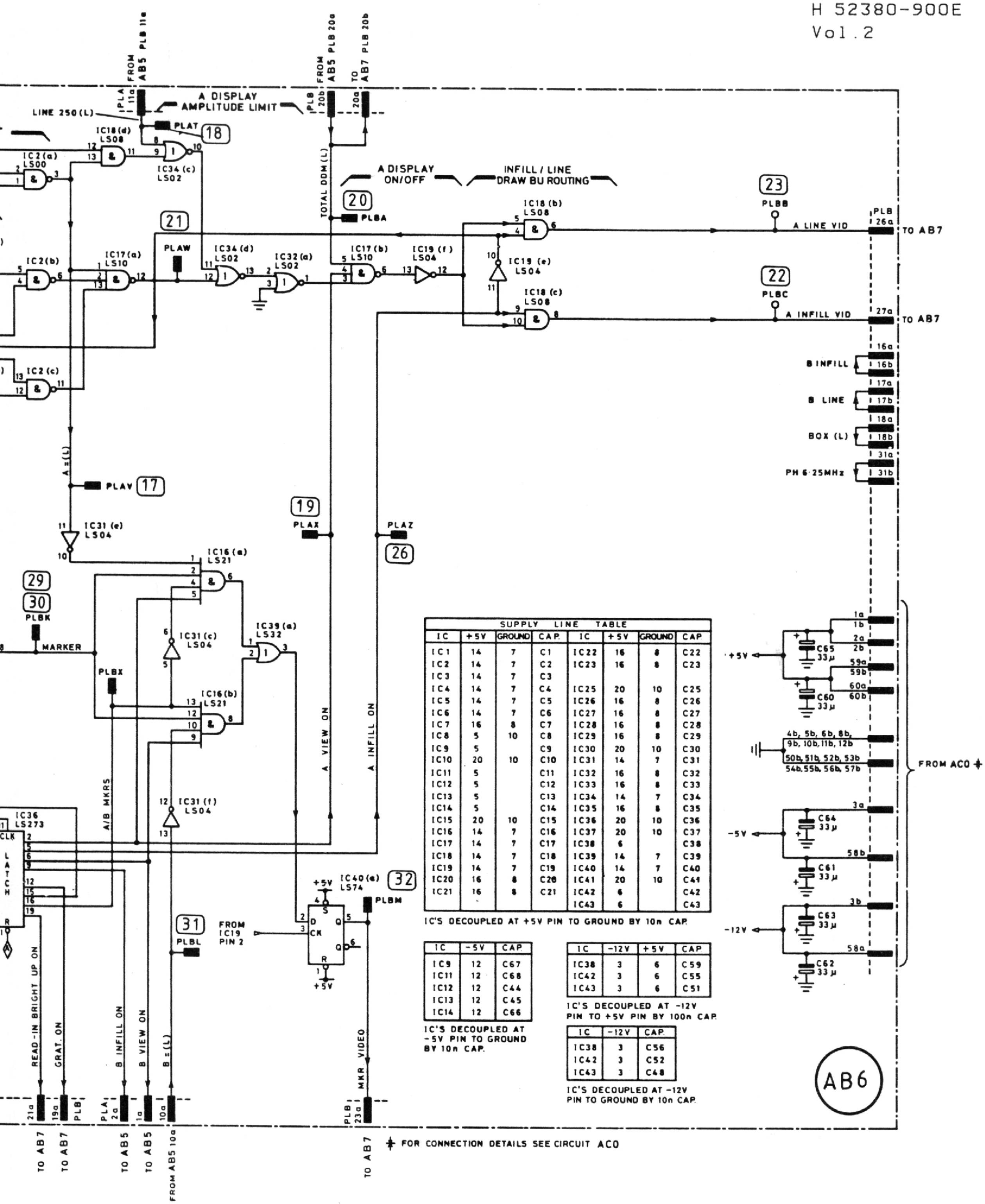
TO AB7

TO AB5

TO AB5

Drg. No. Z44828-508K
Sh. 2 Iss. 1

AB6: Graticule & A display d



SUPPLY LINE TABLE

IC	+5V	GROUND	CAP.	IC	+5V	GROUND	CAP.
IC1	14	7	C1	IC22	16	8	C22
IC2	14	7	C2	IC23	16	8	C23
IC3	14	7	C3				
IC4	14	7	C4	IC25	20	10	C25
IC5	14	7	C5	IC26	16	8	C26
IC6	14	7	C6	IC27	16	8	C27
IC7	16	8	C7	IC28	16	8	C28
IC8	5	10	C8	IC29	16	8	C29
IC9	5		C9	IC30	20	10	C30
IC10	20	10	C10	IC31	14	7	C31
IC11	5		C11	IC32	16	8	C32
IC12	5		C12	IC33	16	8	C33
IC13	5		C13	IC34	14	7	C34
IC14	5		C14	IC35	16	8	C35
IC15	20	10	C15	IC36	20	10	C36
IC16	14	7	C16	IC37	20	10	C37
IC17	14	7	C17	IC38	6		C38
IC18	14	7	C18	IC39	14	7	C39
IC19	14	7	C19	IC40	14	7	C40
IC20	16	8	C20	IC41	20	10	C41
IC21	16	8	C21	IC42	6		C42
				IC43	6		C43

IC'S DECOUPLED AT +5V PIN TO GROUND BY 10n CAP.

IC	-5V	CAP.
IC9	12	C67
IC11	12	C68
IC12	12	C44
IC13	12	C45
IC14	12	C66

IC'S DECOUPLED AT -5V PIN TO GROUND BY 10n CAP.

IC	-12V	+5V	CAP.
IC38	3	6	C59
IC42	3	6	C55
IC43	3	6	C51

IC'S DECOUPLED AT -12V PIN TO +5V PIN BY 100n CAP.

IC	-12V	CAP.
IC38	3	C56
IC42	3	C52
IC43	3	C48

IC'S DECOUPLED AT -12V PIN TO GROUND BY 10n CAP.

& A display dynamic store

BOARD : AB7
KEY OF FUNCTIONS

1 INVERTED 5 MHz SYNC CLOCK FROM LOWER UNIT
2 PHASE ERROR SIGNAL ON PLL 25 MHz OSCILLATOR
3 VARACTOR BIAS VOLTAGE FOR 25 MHz PLL OSCILLATOR
4 25 MHz OSCILLATOR OUTPUT
5 BUFFERED 25 MHz CLOCK
6 5 MHz PHASING CLOCK FOR 25 MHz PLL OSCILLATOR
7 REGULATED 12 V RAIL

continued opposite Fig. 20

1 BOARD : AB7

FUNCTION : INVERTED 5 MHz SYNC CLOCK FROM LOWER UNIT.

TEST POINT : PLAA.
GROUND POINT : C7 (end adjacent to C6)
SCOPE SETTING
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Observe 5 MHz TTL square wave.

2. Remove upper/lower data link connector from rear panel socket and check for (TTL) LOW.

3. Reconnect upper/lower data link. Check 5 MHz TTL signal for accuracy - 5 MHz ±50 Hz (use digital frequency meter).

2 BOARD : AB7

FUNCTION : PHASE ERROR SIGNAL IN PLL 25 MHz OSCILLATOR.

TEST POINT : PLAB
GROUND POINT : C82 (end adjacent to IC42)
SCOPE SETTING
CH1 : 0.5 V/DIV
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for 1.5 V (±0.5 V).

2. Switch off unit, remove data link connector (rear panel), switch on. Check for 1.7 (±0.2 V). Replace data link connector.

NOTE. This depends on C43 being correctly set for 25 MHz.

3 BOARD : AB7

FUNCTION : VARACTOR BIAS VOLTAGE FOR 25 MHz PLL O

TEST POINT : PLAC
GROUND POINT : C82 (end adjacent to IC42)
SCOPE SETTING
MAIN TIMEBASE : 20 ns/DIV

PROCEDURE :

1. Unplug upper/lower data link connector from Switch on, press [PRESET] and observe 25 MHz with a DC offset of 5 V (±0.5 V).

2. Switch off, clip IC10 pin 1 to IC10 pin 7. sine wave superimposed on a 1 Hz waveform va 11 V (±1 V).

3. Switch off, remove clip, replace upper/lower Switch on and observe 25 MHz* sine wave 1 V of 5 V* (±1.5 V).

*These values depend on C43 being set for 25

4 BOARD : AB7

FUNCTION : 25 MHz OSCILLATOR OUTPUT.

TEST POINT : PLAD
GROUND POINT : C82 (end adjacent to IC42)
SCOPE SETTING
MAIN TIMEBASE : 20 ns/DIV

PROCEDURE :

1. Press [PRESET] and observe 25 MHz sine wave, with a DC offset of 6 V (±1 V).

LTAGE FOR 25 MHz PLL OSCILLATOR.

acent to IC42)

DIV

a link connector from rear panel.
ET] and observe 25 MHz sine wave, 1 V (±0.5 V) p-p,
V (±0.5 V).

pin 1 to IC10 pin 7. Switch on and observe 25 MHz*
on a 1 Hz waveform varying between 0 V (±1 V) and

p, replace upper/lower data link connector.
25 MHz* sine wave 1 V (±0.5 V) with a DC offset

C43 being set for 25 MHz.

R OUTPUT.

acent to IC42)

DIV

erve 25 MHz sine wave, 4 V p-p (±1 V),
(±1 V).

5 BOARD : AB7

FUNCTION : BUFFERED 25 MHz CLOCK.

TEST POINT : PLAE
GROUND POINT : D21 (end adjacent to IC1)
SCOPE SETTING
MAIN TIMEBASE : 20 ns/DIV

PROCEDURE :

1. Press [PRESET], observe 25 MHz TTL signal. Check frequency with a digital frequency meter for 25 MHz ±250 Hz.

6 BOARD : AB7

FUNCTION : 5 MHz PHASING CLOCK FOR 25 MHz PLL OSCILLATOR.

TEST POINT : PLAH
GROUND POINT : D21 (end adjacent to IC1)
SCOPE SETTING
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET] and observe* 5 MHz (TTL) signal, HIGH for 80 ns (±10 ns), LOW for 120 ns (±10 ns).

*Observed times will be subject to scope performance.

7 BOARD : AB7

FUNCTION : REGULATED 12 V RAIL.

TEST POINT : PLCH
GROUND POINT : C82 (end adjacent to IC42)

SCOPE SETTING
MAIN TIMEBASE : 50 ms/DIV

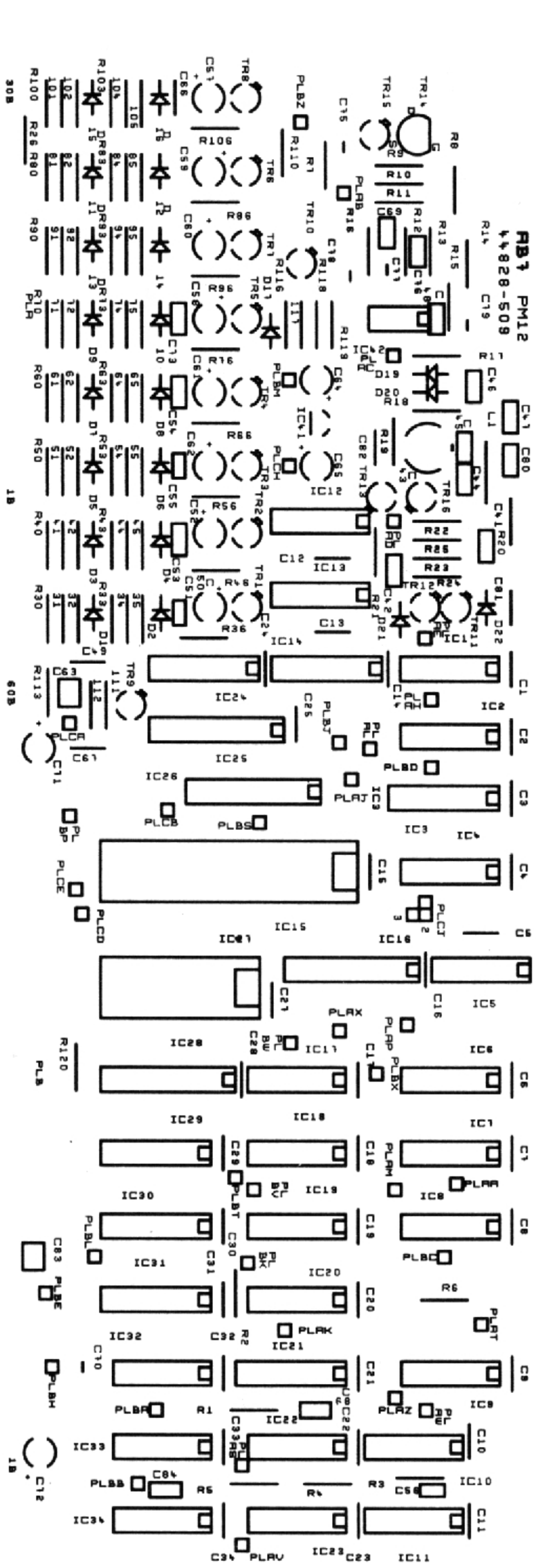
PROCEDURE :

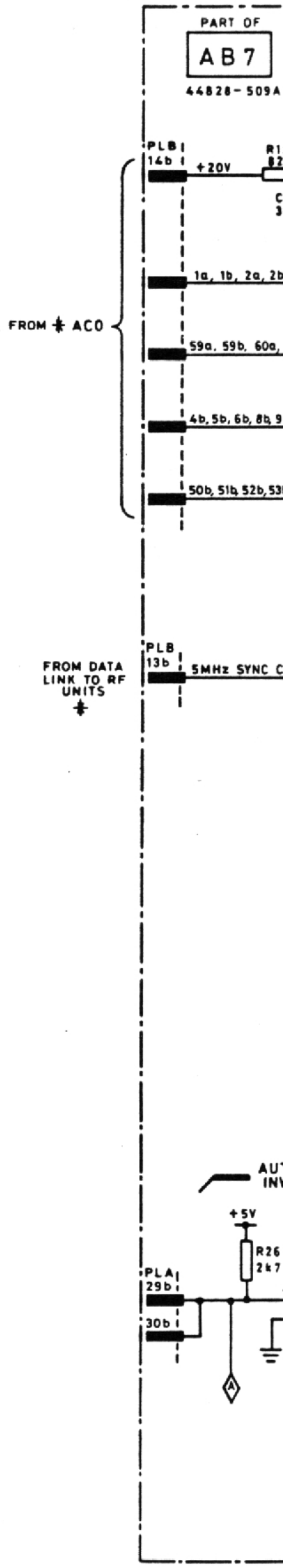
1. Press [PRESET], check for ±12 V DC (±0.5 V).

Waveforms for AB7

Fig. 19A

May 86





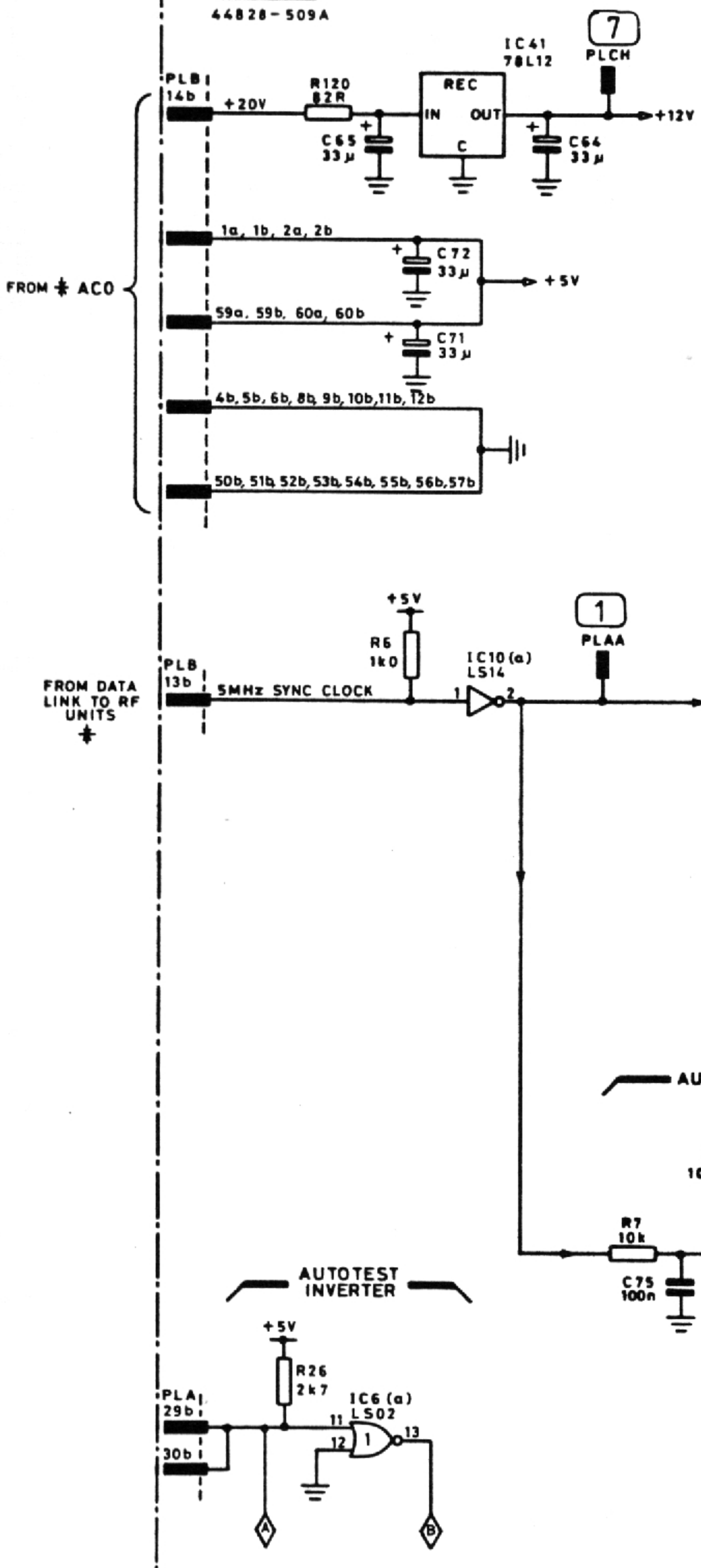
Component layout for AB7

Fig. 19
May 86

PART OF

AB7

44828-509A

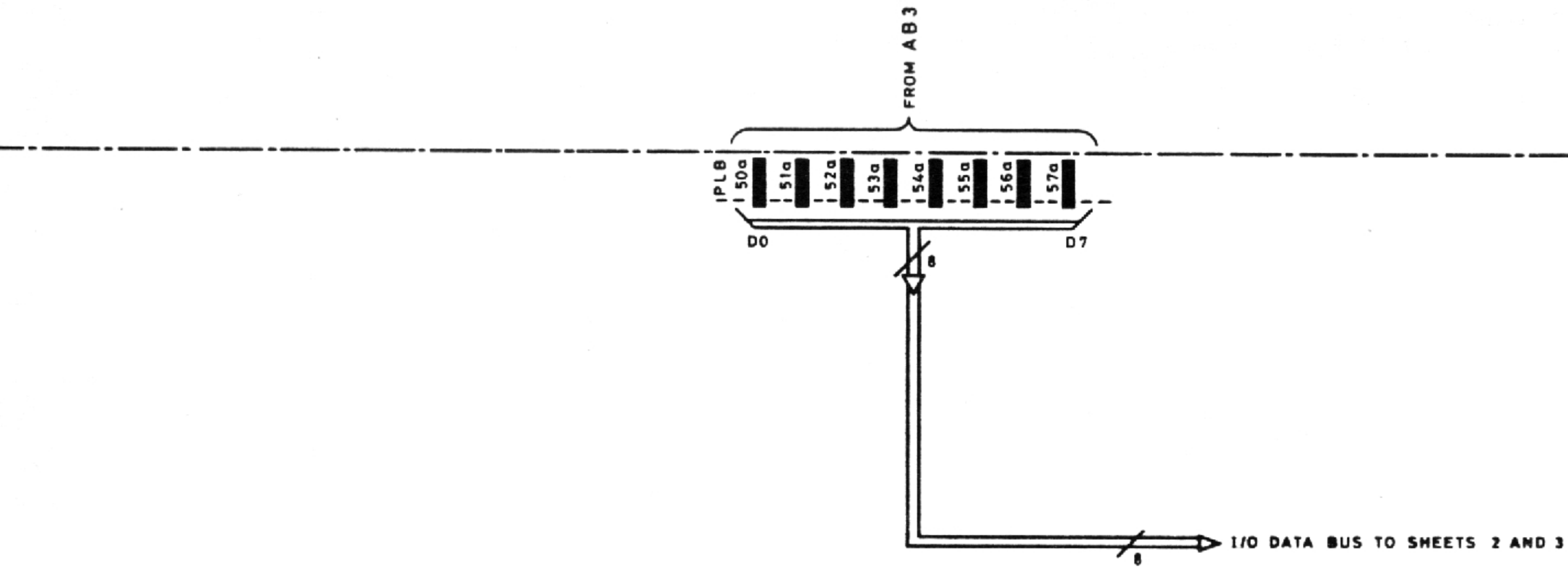


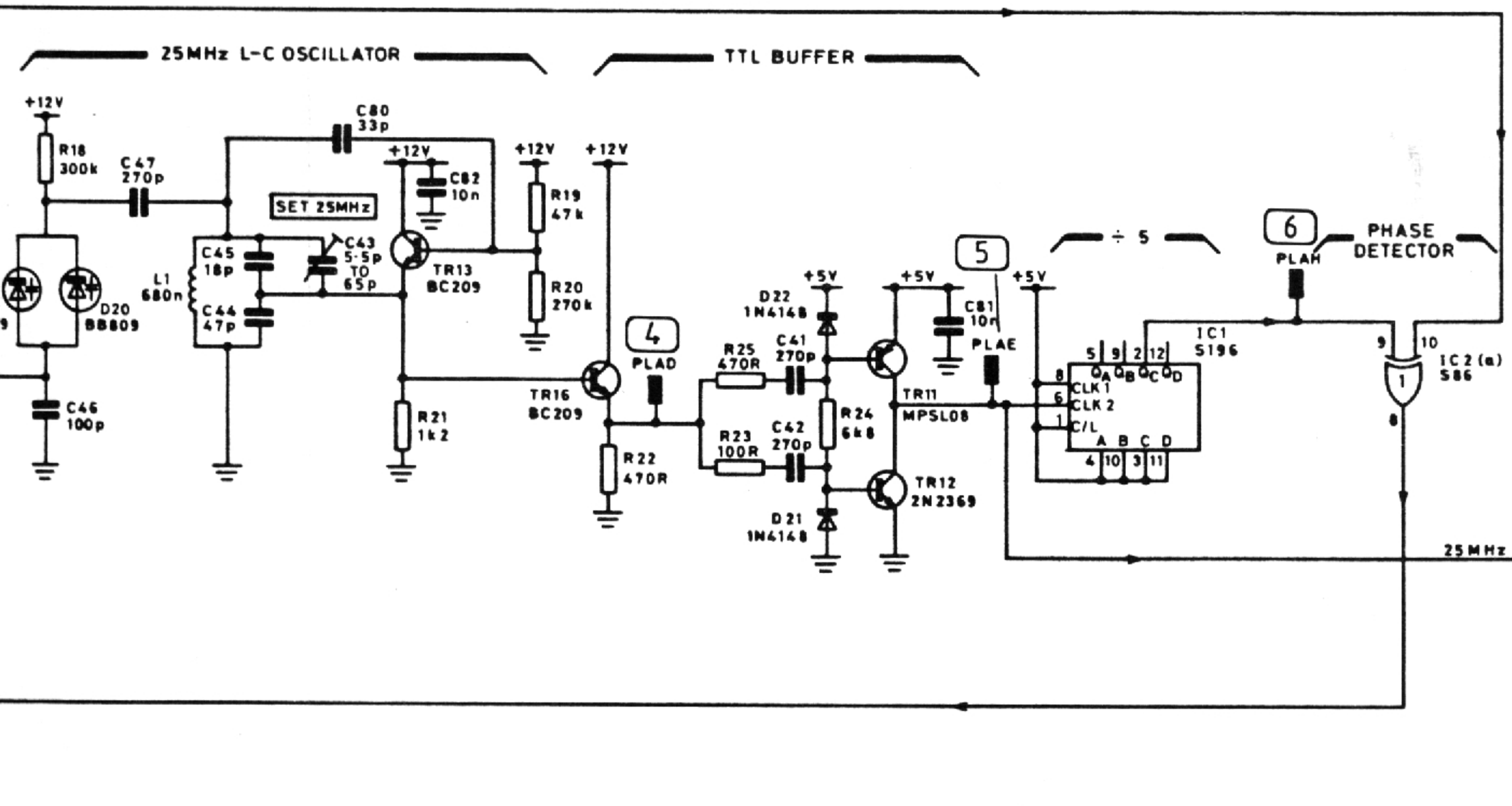
SUPPLY LINE TABLE

IC	+5V	GROUND	IC	+5V	GROUND
IC1	14	7	IC18	14	7
IC2	14	7	IC19	14	7
IC3	16	8	IC20	14	7
IC4	14	7	IC21	16	8
IC5	14	7	IC22	14	7
IC6	14	7	IC23	14	7
IC7	14	7	IC24	16	8
IC8	14	7	IC25	20	10
IC9	14	7	IC26	20	10
IC10	14	7	IC27	24	12
IC11	14	7	IC28	20	10
IC12	14	7	IC29	16	8
IC13	14	7	IC30	16	8
IC14	16	8	IC31	16	8
IC15	40	20	IC32	14	7
IC16	20	10	IC33	14	7
IC17	14	7	IC34	14	7

ALL IC'S DECOUPLED AT +5V PIN TO GROUND WITH 10n CAPACITOR (EXCEPT IC26)

✱ FOR CONNECTION DETAILS SEE CIRCUIT AC0


FROM AB3
IPL8
50a
51a
52a
53a
54a
55a
56a
57a
D0
D7
8
8
I/O DATA BUS TO SHEETS 2 AND 3


25MHz L-C OSCILLATOR
TTL BUFFER
+12V
R18
300k
C47
270p
C80
33p
SET 25MHz
C45
18p
C44
47p
C43
5-5p
TO
65p
L1
680n
D20
BB809
C46
100p
TR13
BC209
C82
10n
R19
47k
R20
270k
R21
1k2
TR16
BC209
R22
470R
4
PLAD
R25
470R
R23
100R
C41
270p
C42
270p
R24
6k8
D22
1N4148
D21
1N4148
TR11
MPSL08
TR12
2N2369
C81
10n
PLAE
5
÷ 5
IC1
S196
6
PLAH
PHASE
DETECTOR
IC2(a)
S86
25MHz CLOCK
CONTINUED ON SHEET TWO

AB7

BOARD : AB7
KEY OF FUNCTIONS (continued)

8 12.5 MHz CLOCK
9 PHASED 12.5 MHz CLOCK
10 PHASED 6.25 MHz CLOCK
11 HRTCS - HORIZONTAL RETRACE (SYNCHRONIZED)
12 CHARACTER CLOCK
13 VRTCS - VERTICAL RETRACE (SYNCHRONIZED)
14 EXTRA LINE (L)
15 EXTRA SYNC (L)
16 LC3
17 DREQ3
18 HRTC - HORIZONTAL RETRACE CONTROL
19 BOX (L)
20 PLBB - TTL SIGNAL - MINOR GRATICULE LINES
21 PLBC - TTL SIGNAL - MAJOR GRATICULE LINES
22 CHAR DOTS
23 C514(L)
24 DACK3(L) - DMA ACKNOWLEDGE

continued opposite Fig. 21

8 BOARD : AB7

FUNCTION : 12.5 MHz CLOCK

TEST POINT : PLAJ
GROUND POINT : C3 (end adjacent to C2)
SCOPE SETTING
MAIN TIMEBASE : 50 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for TTL square wave of 12.5 MHz (80 ns period).

9 BOARD : AB7

FUNCTION : PHASED 12.5 MHz CLOCK.

TEST POINT : PLAK
GROUND POINT : C20 (end adjacent to C19)
SCOPE SETTING
CH2 : 2 V/DIV on PLAJ
MAIN TIMEBASE : 20 ns/DIV
MODE : CHOP CH1, CH2

PROCEDURE :

1. Press [PRESET]. Check for TTL square wave, 12.5 MHz (80 ns period).

2. Put CH2 probe on PLAJ and display both waveforms on scope together. CH2 should also have a 12.5 MHz TTL square wave; inspect PLCJ option link. If link is in position 1-2, then CH1 waveform (PLAK) will lag CH2 waveform (PLAJ) by approx. 10 ns. If link is in position 2-3, then CH1 waveform (PLAK) will lead CH2 waveform (PLAJ) by approx. 30 ns.

NOTE. Do not change the option link.

10 BOARD : AB7

FUNCTION : PHASED 6.25 MHz CLOCK.

TEST POINT : PLAL
GROUND POINT : C2 (end adjacent to
SCOPE SETTING
CH2 : 2 V/DIV on test point
MAIN TIMEBASE : 20 ns/DIV
MODE : CHOP CH1, CH2

PROCEDURE :

1. Press [PRESET]. Observe PLA
The logic transitions should
sitions of CH2 waveform (PLA

11 BOARD : AB7

FUNCTION : HRTCS - HORIZONTAL RET

TEST POINT : PLAM
GROUND POINT : C7 (end adjacent t
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : auto, -ve, CH2
MAIN TIMEBASE : 0.2 ms/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET] and observe C
repeating sequence of 24 HIG
Use the scope 'x10' facility
The first pulse in each sequ
23 pulses being 8.4 µs.

12 BOARD : AB7

FUNCTION : CHARACTER CLOCK.

TEST POINT : PLAS
GROUND POINT : C23 (end adjacent
SCOPE SETTING
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for
Pulse LOW = 80 ns, pulse HIG

Fig. 20A
Chap. 7
Page 58

10 BOARD : AB7

FUNCTION : PHASED 6.25 MHz CLOCK.

TEST POINT : PLAL
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH2 : 2 V/DIV on test point PLAK
MAIN TIMEBASE : 20 ns/DIV
MODE : CHOP CH1, CH2

PROCEDURE :

1. Press [PRESET]. Observe PLAL for 6.25 MHz TTL square wave (160 ns period). The logic transitions should occur within 10 ns of the HIGH to LOW transitions of CH2 waveform (PLAK).

Fig. 21

11 BOARD : AB7

FUNCTION : HRTCS - HORIZONTAL RETRACE (SYNCHRONIZED) FROM CRT CONTROLLER.

TEST POINT : PLAM
GROUND POINT : C7 (end adjacent to C6)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : auto, -ve, CH2
MAIN TIMEBASE : 0.2 ms/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET] and observe CH1 waveform (PLAM). This should be a repeating sequence of 24 HIGH (TTL) pulses, repeating every 1.60 ms. Use the scope 'x10' facility for checking the width of the pulses. The first pulse in each sequence should be 72 µs, the remaining 23 pulses being 8.4 µs.

12 BOARD : AB7

FUNCTION : CHARACTER CLOCK.

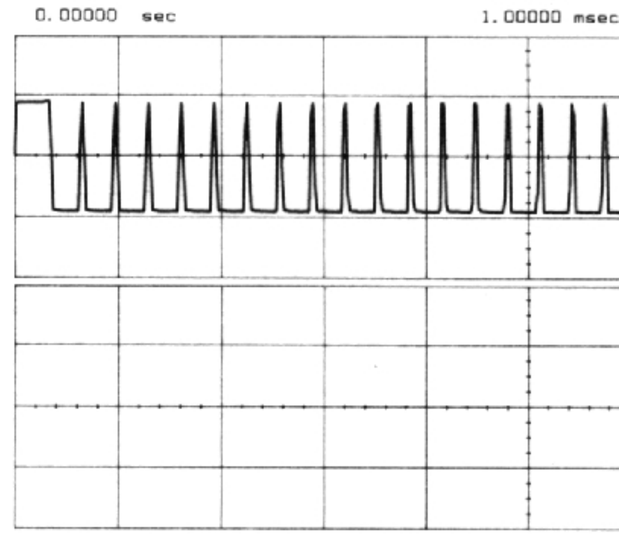
TEST POINT : PLAS
GROUND POINT : C23 (end adjacent to C22)
SCOPE SETTING
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for TTL pulse waveform, period 120 ns (8.3 MHz). Pulse LOW = 80 ns, pulse HIGH = 40 ns.

13 BOARD : AB7

FUNCTION : VRTCS - VERTICAL RETRACE (SYNC



TEST POINT : PLAP
GROUND POINT : C7 (end adjacent to C6)
SCOPE SETTING
MAIN TIMEBASE : 5 ms/DIV

PROCEDURE :

1. Press [PRESET]. Check for HIGH (TT (± 0.3 ms) repeating every 20.8 ms.

14 BOARD : AB7

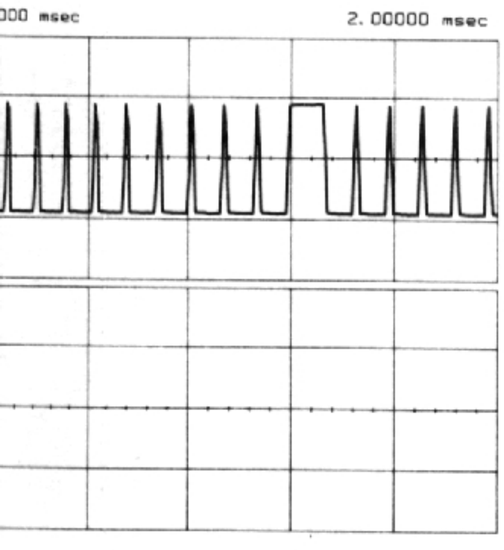
FUNCTION : EXTRA LINE (L). (Used to add after each pair of character r

TEST POINT : PLAT
GROUND POINT : C9 (end adjacent to PLAT)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 10 µs/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Check for 12 LOW (spaced 1.6 ms apart.

(SYNCHRONIZED) FROM CRT CONTROLLER.



6)

H (TTL) pulses, lasting approx. 1.5 ms
ms.

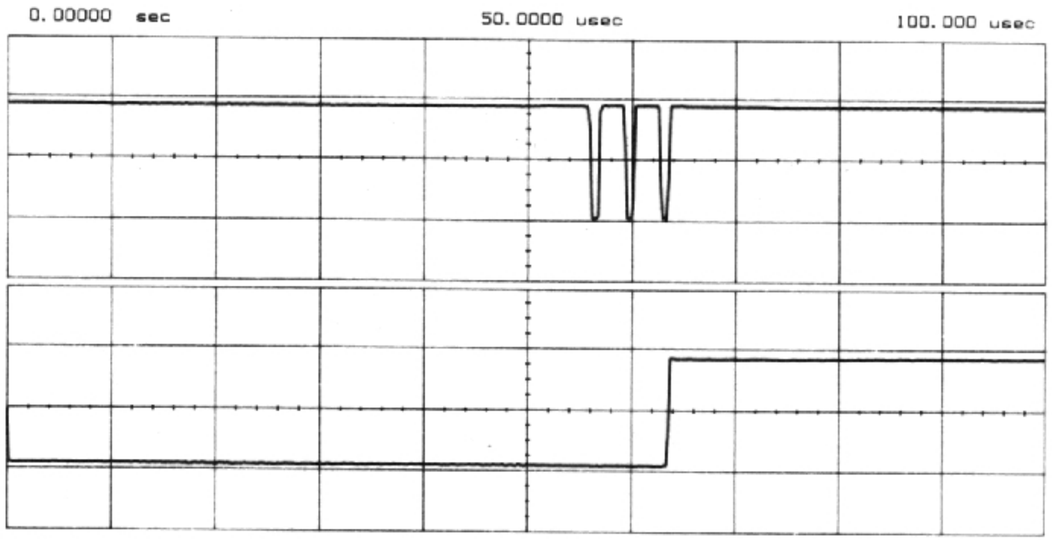
o add one extra horizontal c.r.t. scan
ter rows, to align graticule with chars.)

LAT)

LOW (TTL) pulses each lasting 64 µs,

15 BOARD : AB7

FUNCTION : EXTRA SYNC (L).



TEST POINT : PLAV
GROUND POINT : C34 (end adjacent to C33)
SCOPE SETTING
CH2 : 2 V/DIV on PLAT
TRIGGER : -ve, CH2
MAIN TIMEBASE : 10 µs/DIV
MODE : CH1, CH2, ALT

PROCEDURE :

1. Press [PRESET]. Check CH1 for 3 LOW (TTL) pulses, each lasting 840 ns, spaced 2.52 µs apart. The beginning of the first pulse should occur 55.4 µs after the negative edge (TTL) of CH2 waveform (PLAT). The end of the third pulse should coincide with the positive edge (TTL) of CH2 waveform (PLAT)

16 BOARD : AB7

FUNCTION : LC3 (Line Count 3).

TEST POINT : PLAW
GROUND POINT : C10 (end adjacent to IC9)
SCOPE SETTING
CH2 : 2V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 100 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check CH1 for HIGH (TTL) pulses, lasting 256 µs, spaced apart by LOW periods of 512 µs and 576 µs (alternately) (The first space after the trigger is 576 µs).

17 BOARD : AB7

FUNCTION : DREQ 3

TEST POINT : PLAX
GROUND POINT : C17 (end adjacent to PLAX)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : +ve, CH2
MAIN TIMEBASE : 2 ms/DIV

PROCEDURE :

1. Press [PRESET]. CH1 should show a sequence of 24 (TTL) HIGH pulses, where the whole sequence lasts 1.54 ms and repeats every 1.6 ms.

2. Change trigger to CH2, -ve. Change timebase to 100 µs. It should be seen that the positive edges of the pulses are stable, while the trailing (negative) edges are not. The pulse repetition rate is 768 µs.

3. With a good scope it should be possible to identify 7 very brief LOW (TTL) pulses (400 ns) within the longer HIGH pulses on CH1 (PLAX), but these will not appear to be synchronous.

18 BOARD : AB7

FUNCTION : HRTC - HORIZ RETRACE CONTROL (from c.r.t. controller).

TEST POINT : PLAZ
GROUND POINT : C9 (end adjacent to PLAT)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : AUTO, -ve, CH2
MAIN TIMEBASE : 200 µs/DIV
DELAY TIMEBASE : 10 µs/DIV, starts after main timebase
MODE : CH1, only, and
(a) main timebase only
(b) delay timebase only

PROCEDURE :

1. Press [PRESET]. Use scope in mode (a) above. Check for a repeating sequence of 24 HIGH (TTL) pulses. Sequence length 1.60 ms.

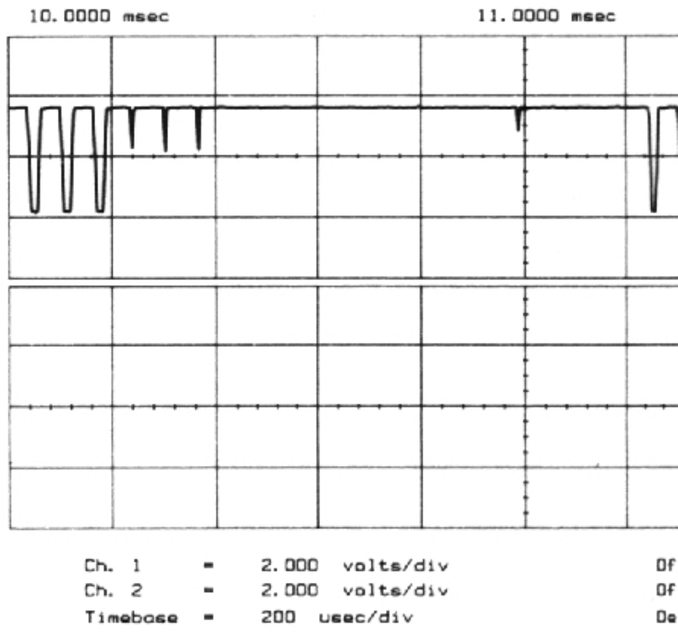
2. Change scope to mode (b) above. Check for :

Pulse rep. rate : 15.625 kHz/64 µs
Pulse (HIGH) width : 8.4 µs, except for
1st pulse width : 72 µs

See waveform diagram (11).

19 BOARD : AB7

FUNCTION : BOX (L) (TTL signal identifies the b
is to be displayed, and is used to



TEST POINT : PLBA
GROUND POINT : C33 (end adjacent to C32)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : CH2, -ve
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 200 µs/DIV
MODE : CH1 only
Set delay to ~ halfway ('500' on most scop
Delay trigger : auto ('B' sweeps after 'A

19 continued

PROCEDURE :

1. Press [PRESET] and 'display A [VIEW]' so t
the graticule and 'Marconi 2382' identifie
TTL signal which is HIGH except for LOW pu

2. Press 'display A [VIEW]','display [OPTNS]
a sequence of LOW (TTL) pulses superimpose

20 BOARD : AB7

FUNCTION : PLBB - TTL SIGNAL - MINOR GRATICULE
of each horizontal row. Used to ge

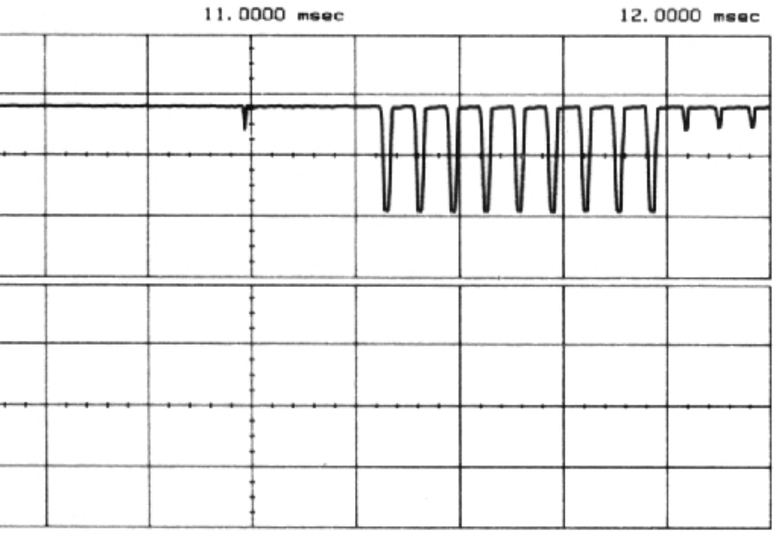
TEST POINT : PLBB
GROUND POINT : C33 (end adjacent to C32)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Check for a repeating se
Sequence length : 16.4 ms; sequence start

2. Change scope main timebase to 50 µs/DIV.
Change scope trigger to +ve, CH1.
Check for :
Pulse rep. rate : 31.25 kHz/320 µs
Pulse (HIGH) width : 55 µs

signal identifies the box within which a character
played, and is used to 'cut' a box out of the graticule).



adjacent to C32)

V
/DIV

fway ('500' on most scopes)
to ('B' sweeps after 'A' sweep ends)

'display A [VIEW]' so that the 2380 screen shows only
'Marconi 2382' identifier. Scope CH1 should show a
s HIGH except for LOW pulses (840 ns long) every 1.6 ms.

VIEW]','display [OPTNS]'. The scope CH1 should show
(TTL) pulses superimposed on the waveform above.

IGNAL - MINOR GRATICULE LINES (updated at beginning
zontal row. Used to generate minor graticule lines).

adjacent to C32)

LAP

ms/DIV

Check for a repeating sequence of 50 HIGH (TTL) pulses.
16.4 ms; sequence starts 1.4 ms after trigger.

timebase to 50 µs/DIV.
er to +ve, CH1.

te : 31.25 kHz/320 µs
width : 55 µs

21 BOARD : AB7

FUNCTION : PLBC - TTL SIGNAL - MAJOR GRATICULE LINES (updated at start of each horizontal row. Used to generate major graticule lines).

TEST POINT : PLBC
GROUND POINT : C8 (end adjacent to C7)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 100 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check for a sequence of 9 HIGH (TTL) pulses, each 55 µs wide, spaced 9 µs apart. Trigger to 1st pulse = 72 µs.

2. Change scope main timebase to 2 ms/DIV. This should reveal a further 11 HIGH (TTL) pulses, width 55 µs, and spaced 1.55 ms apart.

22 BOARD : AB7

FUNCTION : CHAR DOTS (serial character information, at 120 ns/bit).

TEST POINT : PLBD
GROUND POINT : C3 (end adjacent to C2)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 200 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check for a very long sequence of pulses (sequence repeats every 20.8 ms, pulses only 120 ns long). It should be possible to see the sequence change when 'display A [VIEW]' is pressed.

Waveforms for AB7

NES (updated at start of each
or graticule lines).

HIGH (TTL) pulses, each
1st pulse = 72 µs.

is should reveal a further
d 1.55 ms apart.

n, at 120 ns/bit).

ence of pulses (sequence
ng). It should be possible
VIEW]' is pressed.

23 BOARD : AB7

FUNCTION : C514(L) - CHIP SELECT FOR CRT CONTROLLER.

TEST POINT : PLCD
GROUND POINT : C15 (end adjacent to PLAJ)
SCOPE SETTING
TRIGGER : -ve, DC
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check that scope CH1 shows a steady (TTL) HIGH state.

2. Change scope trigger from auto to manual level setting. Adjust scope trigger level to obtain a steady display when CH1 scope probe is temporarily put on PLAS (near C33). With scope CH1 probe back on PLCD, put scope into single sweep mode, and reset the scope single sweep trigger. (Check scope single sweep indicator is lit.) Press [PRESET] and check that the single sweep indicator is now off, indicating that a LOW (TTL) pulse was received on PLCD.

NOTE. To actually see the pulses on PLCD requires a storage scope. (The pulses (LOW) are 480 ns long.)

24 BOARD : AB7

FUNCTION : DACK 3(L) - DMA ACKNOWLEDGE (from c.p.u. to c.r.t. controller).

TEST POINT : PLCE
GROUND POINT : C15 (end adjacent to PLAJ)
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for LOW (TTL) pulses, length 1.4 µs.

PART OF AB7
44828-509A

TO AB3 | PLB 45a | DREQ 3 | PLAX 17

FROM AB3 PLB: 46a, 4a*, 38a, 10a, 9a

PLCE 24 | PLCD 23

IC8(a) LS08

IC15 8275: DREQ, DACK, A0, CS, RD, WR, LC0-LC3, CC0-CC6

CRT CONTROLLER: HRTC, VRTC, HGLT, GPA0, GPA1, VSP, RVV, LTEN, CLK

IC22(a) LS08

I/O DATA BUS FROM SHEET 1 | D0-D7

TO AB8 | PLB 28a | 29a | GPA0S | GPA1S

CHARACTER GEN PROM

+5V | IC27 2716: VPP, A0-A10, O0-O7, OE, CS | LC0, LC3, CC0, CC6

IC16 LS273 LATCH: CLR, CLK | HRTCS, VRTCS, VSPS, RVVS, LTENS

11 PLAM | PLAP 13

EXTRA LINE (L)

CONTINUED FROM SHEET ONE

25MHz CLOCK

DATA DISPLAY PHASED CLOCK GENERATOR

IC5(a) S74: VRTC, CHAR CLOCK (L)

SELECT PHASE ÷2

IC4(b) S74 | PLCJ 1 | IC3(b) S112 | IC5(b) S74 | IC2(c) S86 | 10 PLAL

÷2 | IC3(a) S112 | PLAJ 8 | IC2(b) S86 | IC20(a) S00 | IC20(b) S00 | 9 PLAK

12.5MHz CLOCK | PHASED 12.5MHz CLOCK | PHASED 6.25MHz CLOCK

IC10(c) LS14 | PLAW 16 | IC10(d) LS14

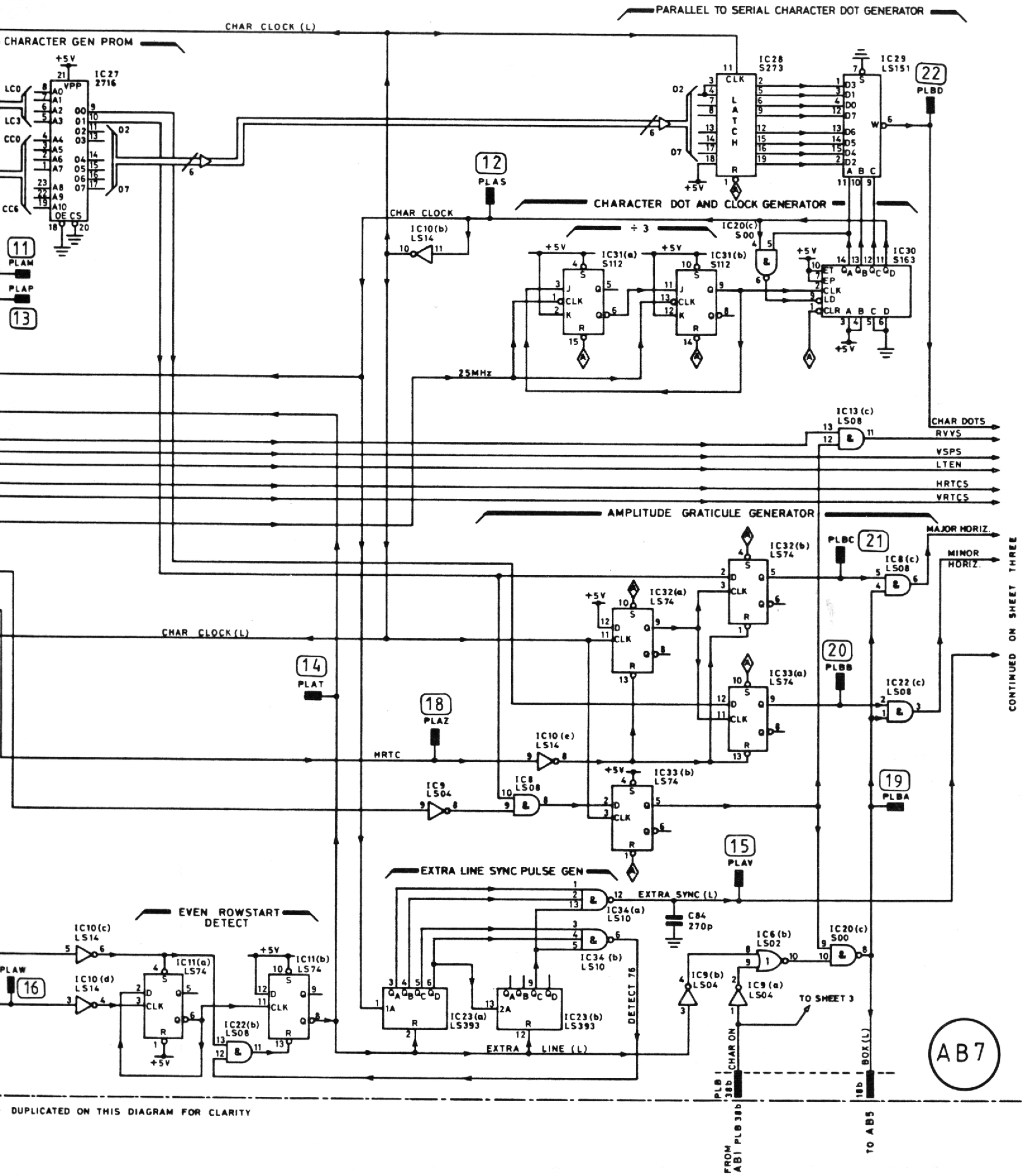
PLB 12a | PLB 32b | PLB 31b

TO AB2 & AB3 | TO AB5 & AB6 | TO AB5 & AB6

* DUPLICATED ON THIS DIAGRAM

Drg.No. 44828-509A
Sh.2 Iss.1

AB7: CRT Control, clock &


PARALLEL TO SERIAL CHARACTER DOT GENERATOR
CHAR CLOCK (L)
CHARACTER GEN PROM
+5V
IC27
2716
VPP
LC0
LC3
CC0
CC6
OE CS
02
07
6
11
PLAM
PLAP
13
IC28
S273
CLK
LATCH
R
IC29
LS151
S
W
22
PLBD
12
PLAS
CHARACTER DOT AND CLOCK GENERATOR
CHAR CLOCK
IC10(b)
LS14
÷ 3
IC20(c)
S00
IC31(a)
S112
IC31(b)
S112
IC30
S163
ET
EP
CLK
LD
CLR
25MHz
IC13(c)
LS08
CHAR DOTS
RVVS
VSPS
LTEN
HRTCS
VRTCS
AMPLITUDE GRATICULE GENERATOR
MAJOR HORIZ.
MINOR HORIZ.
PLBC
21
IC8(c)
LS08
IC32(b)
LS74
IC32(a)
LS74
IC33(a)
LS74
IC33(b)
LS74
20
PLBB
IC22(c)
LS08
19
PLBA
CHAR CLOCK (L)
14
PLAT
18
PLAZ
HRTC
IC10(e)
LS14
IC9
LS04
IC8
LS08
15
PLAV
EXTRA LINE SYNC PULSE GEN
EXTRA SYNC (L)
IC34(a)
LS10
C84
270p
IC34(b)
LS10
IC23(a)
LS393
IC23(b)
LS393
DETECT 76
EXTRA LINE (L)
IC6(b)
LS02
IC20(c)
S00
IC9(b)
LS04
IC9(a)
LS04
TO SHEET 3
EVEN ROWSTART DETECT
IC10(c)
LS14
IC10(d)
LS14
PLAW
16
IC11(a)
LS74
IC11(b)
LS74
IC22(b)
LS08
CHAR ON
BOX (L)
PLB 38b
18b
FROM AB1 PLB 38b
TO AB5
CONTINUED ON SHEET THREE
AB7
DUPLICATED ON THIS DIAGRAM FOR CLARITY

BOARD : AB7
KEY OF FUNCTIONS (concluded)

25 V SYNC - VERTICAL SYNC SIGNAL
26 H SYNC - HORIZONTAL SYNC SIGNAL
27 DDM - DISPLAY DIVISIONS MASK
28 B INFILL VID
29 B LINE VID
30 READ-IN BRIGHT UP
31 'CHAR' - CHARACTER DOT INFORMATION
32 MAJOR - MAJOR GRATICULE DOT INFORMATION
33 MINOR - MINOR GRATICULE INFORMATION
34 'MARKER' DOT INFORMATION INTO VIDEO MIXER
35 'A INFILL' - INPUT TO VIDEO MIXER
36 'A LINE VIDEO' - INPUT TO VIDEO MIXER
37 PLBZ - MIXED VIDEO SIGNAL (UNBUFFERED)
38 PLCB - CLOCKS READ-IN BRIGHT UP POSITION
39 VIDEO OUTPUT (BUFFERED)

25 BOARD : AB7

FUNCTION : V SYNC - VERTICAL SYNC SIGNAL (active HIGH TTL used on display drive board AD1).

TEST POINT : PLBE
GROUND POINT : C32 (end adjacent to C31)
SCOPE SETTING
MAIN TIMEBASE : 20 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check for a HIGH (TTL) pulse, width 120 µs (±12 µs) occurring every 20.8 ms.

26 BOARD : AB7

FUNCTION : H SYNC - HORIZONTAL SYNC SIGNAL (active HIGH TTL used on display drive board AD1).

TEST POINT : PLBH
GROUND POINT : C32 (end adjacent to C31)
SCOPE SETTING
MAIN TIMEBASE : 500 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for a HIGH (TTL) pulse, width 4.3 µs (±0.5 µs), occurring every 64 µs.

27 BOARD : AB7

FUNCTION : DDM - DISPLAY DIVISIONS M
centre area of screen, le

TEST POINT : PLBJ
GROUND POINT : C25 (end adjacent to
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 200 µs/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Check for a (
initial LOW (TTL) period of 1.4

2. Change the main timebase to 5 µ
scope should show the HIGH (TTL

28 BOARD : AB7

FUNCTION : B INFILL VID (input to vi

TEST POINT : PLBK
GROUND POINT : C31 (end adjacent to
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 0.2 ms/DIV

PROCEDURE :

1. Press [PRESET]. Press 'vertica
into an unbroken horizontal line
Press 'display A [VIEW]' (to eli
Press 'display B [VIEW]' (to obt
Press '[2ND FUNCT]', 'display B
Scope CH1 should display a pulse
period of 1.4 ms, with pulses HI
every 64 µs.

2. Select scope main timebase of 1
the displayed spectrum down the
ing reduction in the number of p

Fig. 21A
Chap. 7
Page 62

27 BOARD : AB7

FUNCTION : DDM - DISPLAY DIVISIONS MASK (signal (TTL) limits graticule to centre area of screen, leaves 'boxes' for characters).

TEST POINT : PLBJ
GROUND POINT : C25 (end adjacent to IC14)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 200 µs/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Check for a (TTL) pulse train, starting after an initial LOW (TTL) period of 1.4 ms.

2. Change the main timebase to 5 µs/DIV, trigger to +ve, CH1. The scope should show the HIGH (TTL) pulse width to be 40 µs.

28 BOARD : AB7

FUNCTION : B INFILL VID (input to video mixer block for infilled B displays).

TEST POINT : PLBK
GROUND POINT : C31 (end adjacent to C30)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 0.2 ms/DIV

PROCEDURE :

1. Press [PRESET]. Press 'vertical [↓]' repeatedly until waveform limits into an unbroken horizontal line at the top of the display.
Press 'display A [VIEW]' (to eliminate 'A' display).
Press 'display B [VIEW]' (to obtain 'B' display).
Press '[2ND FUNCT]', 'display B [VIEW]' (to infill display 'B').
Scope CH1 should display a pulse sequence, after an initial LOW (TTL) period of 1.4 ms, with pulses HIGH (TTL) of width 40 µs, repeating every 64 µs.

2. Select scope main timebase of 1 ms/DIV. Press 'vertical [↑]' to bring the displayed spectrum down the screen, and there should be a corresponing reduction in the number of pulses seen on the scope.

29 BOARD : AB7

FUNCTION : B LINE VID (input to video mixer

TEST POINT : PLBL
GROUND POINT : C31 (end adjacent to C30)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 0.2 ms/DIV

PROCEDURE :

1. Press [PRESET]. Press 'vertical [↓]'
pressed into a straight line at top of
Press 'display A [VIEW]' (to eliminate
Press 'display B [VIEW]' (to select 'B
Scope CH1 should display a HIGH (TTL)
after the scope trigger.

2. Select scope main timebase of 1 ms/DIV.
the displayed spectrum down the screen,
ing movement of the pulse position on t
band noise of the measured spectrum wil
rising and falling edges of the pulse s

30 BOARD : AB7

FUNCTION : READ-IN BRIGHT UP (input to vide
screen data updates).

TEST POINT : PLBM
GROUND POINT : C82 (end adjacent to IC42)
SCOPE SETTING
MAIN TIMEBASE : 5 µs/DIV

PROCEDURE :

1. Press [PRESET]. Select 10 Hz/DIV by
[SPAN/DIV]', [1 0], [Hz].

2. The scope should show a HIGH (TTL) pul
nothing to 40 µs over a period of appr
correspond to the screen update (indic
being highlighted in comparison to the
across the screen.

to video mixer block for line B displays).

ent to C30)

IV

'vertical [↓]'repeatedly until spectrum is com-
line at top of screen.
(to eliminate 'A' display).
(to select 'B' display).
a HIGH (TTL) pulse, 40 µs wide, occurring 1.4 ms

se of 1 ms/DIV. Press 'vertical [↑]' to bring
own the screen, and there should be a correspond-
e position on the scope. (Note that the base-
ed spectrum will produce a fuzzy effect on the
of the pulse seen on the scope.)

(input to video mixer block for indicating
s).

ent to IC42)

10 Hz/DIV by pressing 'function/data
.

HIGH (TTL) pulse, growing in width from
period of approx. 5 seconds. This should
update (indicated by the new information
parison to the old data) as the sweep scans

31 BOARD : AB7

FUNCTION : 'CHAR' - CHARACTER DOT INFORMATION (with reverse video, etc. incorporated. Input to video mixer).

TEST POINT : PLBP
GROUND POINT : C67 (end adjacent to C71)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 100 µs/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Check for a stable (but apparently random) train of HIGH (TTL) pulses. Press [2ND FUNCT], [ANNOT GRAT] to eliminate all screen characters, and CH1 waveform should now be permanently LOW (TTL).

2. Press [PRESET] to restore characters.

32 BOARD : AB7

FUNCTION : MAJOR - MAJOR GRATICULE DOT INFORMATION (input to video mixer block).

TEST POINT : PLBS
GROUND POINT : C15 (end adjacent to PLAJ)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. CH1 should show a (TTL) pulse sequence, with a pattern, length 1.6 ms, that repeats 10 times every 20.8 ms.

2. Press [2ND FUNCT], 'vertical [LOG]' and the scope CH1 waveform will change to a different pattern of HIGH (TTL) pulses.

3. Press 'display [GRAT]' and the pulse sequence will be replaced by a TTL LOW.

33 BOARD : AB7

FUNCTION : MINOR - MINOR GRATICULE DOT INFORMATION INPUT TO VIDEO MIXER BLOCK.

TEST POINT : PLBT
GROUND POINT : C30 (end adjacent to C29)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. CH1 should show a (TTL) pulse sequence, (1.4 ms from trigger) with a pattern (length 320 µs) that repeats 51 times every 20.8 ms.

2. Press [2ND FUNCT], 'display A [SAVE]' and the pulses should disappear, leaving the signal at TTL LOW.

3. Press [PRESET]. Press 'display [GRAT]' and the pulse sequence should be replaced by a TTL LOW.

Fig. 21A

May 86

34 BOARD : AB7

FUNCTION : 'MARKER' DOT INFORMATION INTO VIDEO MIXER.

TEST POINT : PLBV
GROUND POINT : C29 (end adjacent to C28)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 200 µs/DIV
MODE : CH1 only
Delay set to minimum
Delay trigger : manual, DC, CH1, +ve
Set mode : A intensified by B

NOTE. Use a scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [2] 'enter data display & linearity tests'.

2. Press 'markers [MKR]'. Check for a HIGH TTL pulse occurring 9.4 ms after scope trigger, by adjusting the delay trigger level to find it.

3. Temporarily change scope settings to delay timebase = 200 ns, with B sweep only, to check pulse width = 80 ns (±20 ns).

4. Press 'markers [1 2 MOVE]', rotate 'markers [MOVE]' and the pulse seen on the scope will move corresponding in an interval 1.4 ms - 17.6 ms after trigger.

5. Press 'markers [MKR 2]' and repeat (2),(4) above.

35 BOARD : AB7

FUNCTION : 'A INFILL' - INPUT TO VIDEO MIXER.

TEST POINT : PLBW
GROUND POINT : C28 (end adjacent to C27)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 10 µs/DIV
MODE : CH1 only
Delay trigger : auto (B sweeps after A sweep ends)
Delay set to ~ halfway (500 on most scopes)
'A intensified by B' mode

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [2] 'enter data display & linearity tests'.
Check for a train of HIGH (TTL) pulses, which starts 1.4 ms after the trigger, and lasts 16 ms.

2. Rotate [REF FREQ] clockwise about 10 times. Measure the length of the pulses in the pulse train by using 'delay sweep only' mode, check for pulse cycle = 64 µs, pulse high time = 40 µs.

3. Press [2ND FUNCT], 'display A [VIEW[' and the pulses should disappear.

36 BOARD : AB7

FUNCTION : 'A LINE VIDEO' - INPUT TO VIDEO MIXER.

TEST POINT : PLBX
GROUND POINT : C17 (end adjacent to PLAX)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode
Select [2] 'upper unit confidence tests'.
Select [2] 'enter data display & linearity te
Press '[2ND FUNCT]', 'display 'A' [VIEW].

2. Measure the length of the pulses in the pulse
timebase to 200 ns/DIV, main trigger to CH1.
pulse high time = 160 ns.

3. Press [2ND FUNCT], 'display A [VIEW]' and the

37 BOARD : AB7

FUNCTION : PLBZ - MIXED VIDEO SIGNAL (UNBUFFERED).

TEST POINT : PLBZ
GROUND POINT : C82 (end adjacent to IC42)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 500 µs/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Turn all 3 front panel inte
(counter-clockwise). Check that scope CH1 s

2. Turn graticule intensity to maximum (clockwis
0.5 V/DIV, a.c. coupled, and check for LOW (n
from baseline).

38 BOARD : AB7

FUNCTION : PLCB - CLOCKS READ-IN BRIGHT UP POSITIO
into IC25).

TEST POINT : PLCB
GROUND POINT : C25 (end adjacent to IC14).
SCOPE SETTING
TRIGGER : -ve, manual setting
MAIN TIMEBASE : 500 ns/DIV

NOTE. Turn brilliance to full, use scope hood.

PROCEDURE :

1. Press [PRESET]. Press 'horizontal sweep tim
Set scope main timebase to 50 µs/DIV and rota
trol until a trace is obtained. Turn scope
with full brilliance, and check for a LOW (TT
350 ns, on PLCB.

2. Press [PRESET] on 2382. Put scope into sing
sweep trigger and check that the sweep is new
there are now no pulses on PLCB).

- INPUT TO VIDEO MIXER.

djacent to PLAX)

DIV

er DEBUG OPERATIONS mode.
t confidence tests'.
a display & linearity tests'.
'display 'A' [VIEW].

the pulses in the pulse train by changing main
V, main trigger to CH1. Pulse cycle = 64 µs,
ns.

display A [VIEW]' and the pulses should disappear.

IDEO SIGNAL (UNBUFFERED).

djacent to IC42)

s/DIV

n all 3 front panel intensity controls to minimum
Check that scope CH1 shows +10 V d.c. (±1 V).

ity to maximum (clockwise). Change scope CH1 to
ed, and check for LOW (not TTL) pulses (<1 volt

EAD-IN BRIGHT UP POSITION (information from c.p.u.

jacent to IC14).

setting
s/DIV

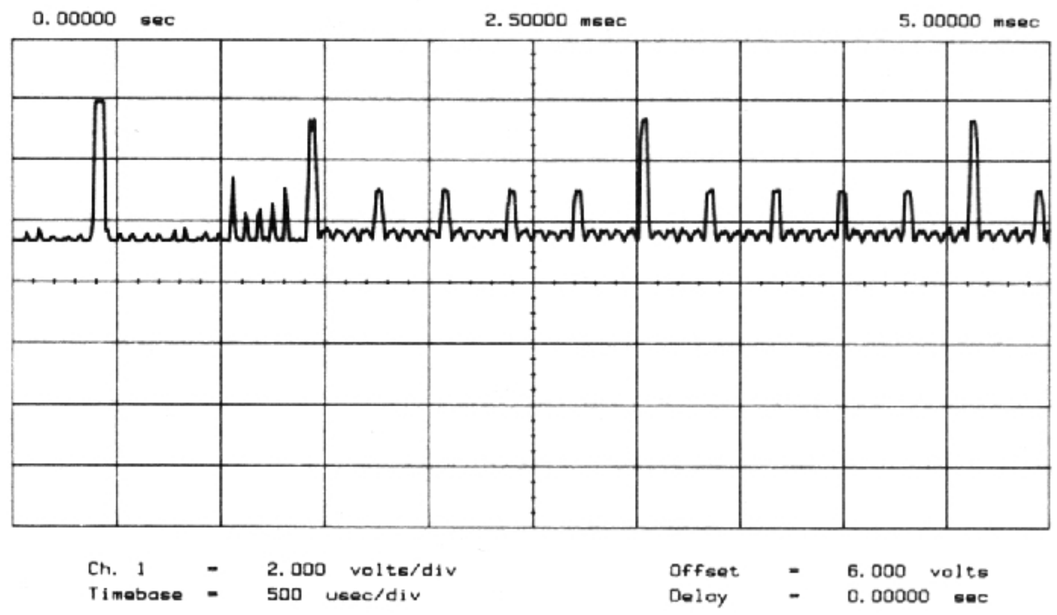
full, use scope hood.

ss 'horizontal sweep time [↑]' to obtain 200 ms/DIV.
se to 50 µs/DIV and rotate scope trigger level con-
obtained. Turn scope main timebase to 200 ns/DIV,
and check for a LOW (TTL) pulse, length approx.

2. Put scope into single sweep mode, re-arm single
ck that the sweep is never triggered (indicates that
es on PLCB).

39 BOARD : AB7

FUNCTION : VIDEO OUTPUT (BUFFERED).



TEST POINT : PLCA
GROUND POINT : C67 (end adjacent to C71)
SCOPE SETTING
CH2 : 2 V/DIV on PLAP
TRIGGER : -ve, CH2
MAIN TIMEBASE : 500 µs/DIV
MODE : CH1 only

39 continued

PROCEDURE :

1. Press [PRESET]. Turn all 3 intensity controls fully counter-clockwise. Check scope CH1 for steady d.c. voltage +7 V (±1 V).

2. Turn graticule intensity to maximum, check for :
(major graticule) pulses = +4 V above baseline (±0.4 V)
(minor graticule) pulses = +2 V above baseline (±0.4 V)
Ref. waveform diagram :

3. Turn down grat intensity to minimum. Turn A intensity to maximum. Enter DEBUG OPERATIONS mode, select [2] 'upper unit confidence tests'. Select [2] 'enter display data & linearity tests'.

4. Rotate 'function/data REF FREQ' clockwise (10 turns). Check that pulses on scope CH1 are +4 V (±0.4 V) over the baseline voltage.

5. Press display B [SAVE], turn A intensity to minimum, and B intensity to maximum and repeat (4) above.
See waveform diagram :

PART OF
AB7
44828-509A

FROM AB3 PLB 4a
FROM AB3 PLB 39a
FROM AB5 PLB 15a
TO AB8

PLB 14a
PLB 39a
PLB 15b
PLB 30a

A0
CS18 (L)
SR CLOCK (6·2MHz)
READ IN BRIGHT-UP

READ-IN SWEEP POSITION
READ-IN BRIGHT UP POSITION DOWN COUNTER

IC6 (c) LS02
IC18 (a) LS32
PLCB
38

IC14 LS193
IC24 LS193
IC12 (b) LS74
IC13 (b) LS08
+5V

IC25 LS273
I/O DATA BUS FROM SHEET 1
D0
D7
CLK
LATCH
CLR

IC13 (a) LS08
27
PLBJ

IC2 (d) S86
IC6 (d) LS02
IC7 (d) LS32
CHAR DOTS
RVVS
VSPS
LTEN

IC8 (d) LS08
CHAR ON FROM SHEET 2

IC18 (b) LS32
IC17 (a) LS11

HRTCS
VRTCS
MAJOR HORIZ.
MINOR HORIZ.
CONTINUED FROM SHEET TWO

SYNC. PULSE GENERATORS

IC19 (a) LS74
IC19 (b) LS74
IC7 (d) LS32
IC21 (a) LS221
R1 6k8
C68 1n0
EXTRA SYNC (L)

IC18 (c) LS32
IC17 (b) LS11
IC17 (c) LS11

26
PLBH

IC22 (d) LS08

IC9 (c) LS04
IC9 (d) LS04
R3 2k2
R4 2k2
C56 470p
R5 8k2

R2 2k2
C70 100n
IC21 (b) LS221
25
PLBE

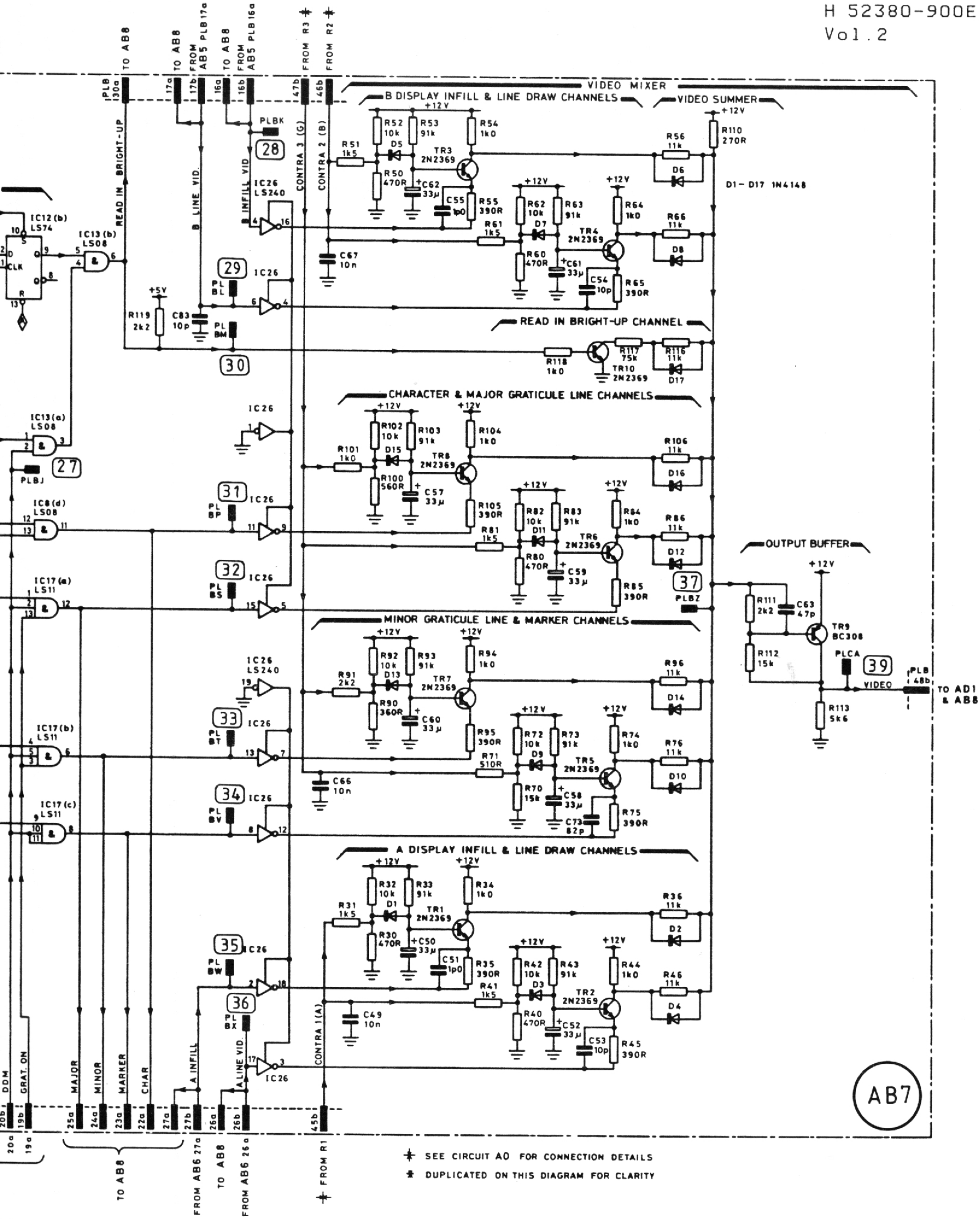
VRTCS
HRTCS
V SYNC
VRTC (L)
H SYNC
HRTC (L)

MAJOR VERT. GRAT.
MINOR VERT. GRAT.
MARKER VID.
READ IN BRIGHT UP ON
DDM
GRAT. ON
MAJOR
MINOR
MARKER
CHAR

TO AD1
TO AB5
TO AB5
TO AD1
FROM AB6 PLB
TO AB8

Drg. No. 44828-509A
Sh. 3 Iss. 1

AB7: CRT Control, clock & vi



l, clock & video mixer

Fig. 21
Chap. 7
Page 65

BOARD : AB8
KEY OF FUNCTIONS

1 PEN RECORDER DRIVE VOLTAGE REFERENCE
2 RECORDER PENLIFT CONTROL
3 BLEEPER DRIVE VOLTAGE
4 TRANSISTOR BASE DRIVE FOR RECORDER X CHANNEL
5 TRANSISTOR BASE DRIVE FOR RECORDER Y CHANNEL

continued opposite Fig. 23

1 BOARD : AB8

FUNCTION : PEN RECORDER DRIVE VOLTAGE REFERENCE.

TEST POINT : PLAA
GROUND POINT : C5 (end adjacent to p.c.b. edge)

Use DVM.

PROCEDURE :

1. Press [PRESET]. Check voltage to be 10 V (±200 mV) (DC) using AC volts range. Check PLAA <5 mV (AC).

2 BOARD : AB8

FUNCTION : RECORDER PENLIFT CONTROL.

TEST POINT : PLAB
GROUND POINT : C9 (end adjacent to IC9)
SCOPE SETTING
MAIN TIMEBASE : 1 ms/DIV

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [1] 'upper & lower unit I/O tests'.
Select [1] 'enter upper unit I/O tests'.
'Enter I/O port number [HEX] =' [5 9 -].
'Enter I/O port value [BIN] =' [0 -].
Check that PLAB is now a steady LOW (TTL).
Select [1] 'enter upper unit I/O port parameters'.
'Enter I/O port number [HEX] =' [5 9 -].
'Enter I/O port value [BIN] =' [0 0 1 0 0 0 0 0] [-].
Now check PLAB is a steady HIGH (TTL).

3 BOARD : AB8

FUNCTION : BLEEPER DRIVE VOLTAGE.

TEST POINT : PLAC
GROUND POINT : C10 (end adjacent to C18)
SCOPE SETTING

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS m
Select [2] 'upper unit confidence tests'.
Select [5] 'options board tests'.
Select [1] 'Beeper'.
Select [3] <<continuous beep>>.
Check for HIGH TTL pulses, 150 µs long, ev

2. Select [4] <<continuous beep, lower pitch>
Check for HIGH TTL pulses, 270 µs long, ev

4 BOARD : AB8

FUNCTION : TRANSISTOR BASE DRIVE FOR RECORDER X

TEST POINT : PLAD
GROUND POINT : C9 (end adjacent to IC9)
SCOPE SETTING

Alternatively, a DVM may be used in the procedu

PROCEDURE :

1. Press [PRESET]. Check that PLAD has a st
Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [5] 'options board tests'.
Select [3] 'pen plot'.
Select [2] 'set graticule top right'.
Check voltage on PLAD is now steady 6.7 vo

NOTE. It will take approx. 10 seconds af

5 BOARD : AB8

FUNCTION : TRANSISTOR BASE DRIVE FOR RECORDER Y

TEST POINT : PLAE
GROUND POINT : C9 (end adjacent to IC9)
SCOPE SETTING

Alternatively, a DVM may be used in the procedu

PROCEDURE :

1. Press [PRESET]. Check that PLAE has a ste
Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [5] 'options board tests'.
Select [3] 'pen plot'.
Select [2] 'set graticule top right'.
Check voltage on PLAD is now steady 6.7 vol

NOTE. It will take approx. 10 seconds aft

ENCE

ER X CHANNEL
ER Y CHANNEL

continued opposite Fig. 23

REFERENCE.

c.b. edge)

to be 10 V (±200 mV) (DC) using
mV (AC).

))

ERATIONS mode.
'O tests'.
tests'.
[5 9 -].
) -].
LOW (TTL).
port parameters'.
[5 9 -].
) 0 1 0 0 0 0 0] [-].
(TTL).

3 BOARD : AB8

FUNCTION : BLEEPER DRIVE VOLTAGE.

TEST POINT : PLAC
GROUND POINT : C10 (end adjacent to C18)
SCOPE SETTING

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
   Select [2] 'upper unit confidence tests'.
   Select [5] 'options board tests'.
   Select [1] 'Beeper'.
   Select [3] <<continuous beep>>.
   Check for HIGH TTL pulses, 150 µs long, every 270 µs.

2. Select [4] <<continuous beep, lower pitch>>.
   Check for HIGH TTL pulses, 270 µs long, every 400 µs.

4 BOARD : AB8

FUNCTION : TRANSISTOR BASE DRIVE FOR RECORDER X CHANNEL.

TEST POINT : PLAD
GROUND POINT : C9 (end adjacent to IC9)
SCOPE SETTING

Alternatively, a DVM may be used in the procedure below.

PROCEDURE :

1. Press [PRESET]. Check that PLAD has a steady d.c. offset of 500 mV.
   Enter DEBUG OPERATIONS mode.
   Select [2] 'upper unit confidence tests'.
   Select [5] 'options board tests'.
   Select [3] 'pen plot'.
   Select [2] 'set graticule top right'.
   Check voltage on PLAD is now steady 6.7 volts.

   NOTE. It will take approx. 10 seconds after pressing the last button.

5 BOARD : AB8

FUNCTION : TRANSISTOR BASE DRIVE FOR RECORDER Y CHANNEL.

TEST POINT : PLAE
GROUND POINT : C9 (end adjacent to IC9)
SCOPE SETTING

Alternatively, a DVM may be used in the procedure below.

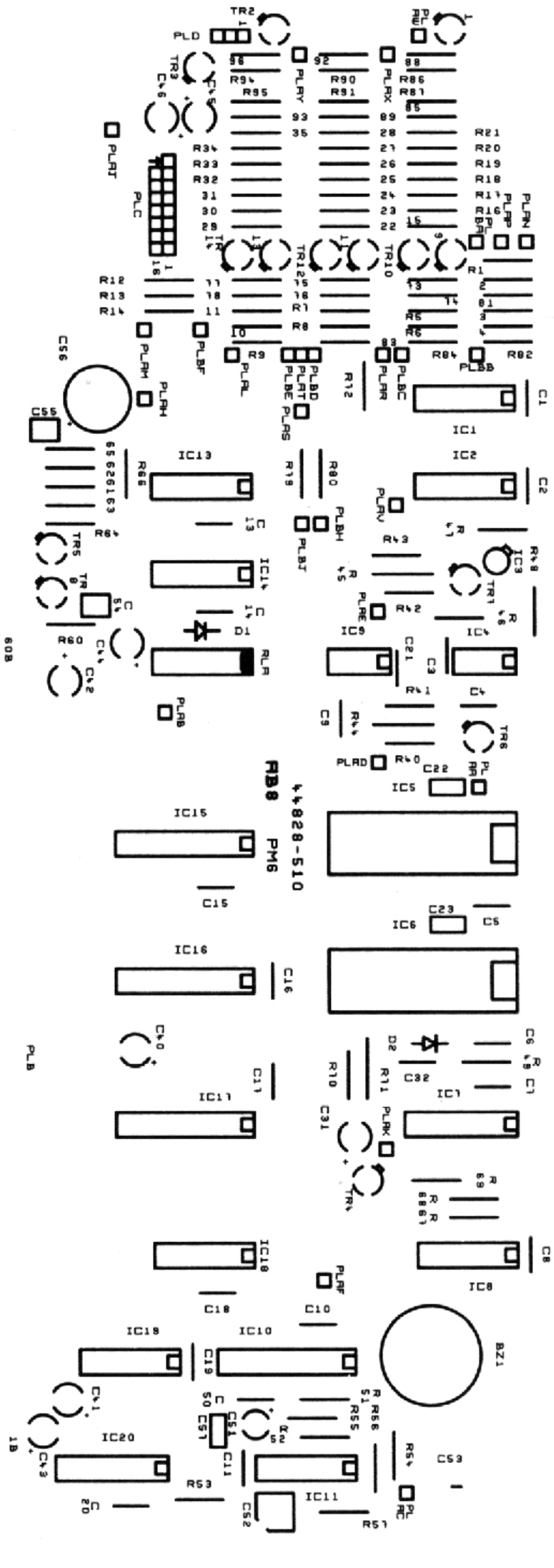
PROCEDURE :

1. Press [PRESET]. Check that PLAE has a steady d.c. offset of 500 mV.
   Enter DEBUG OPERATIONS mode.
   Select [2] 'upper unit confidence tests'.
   Select [5] 'options board tests'.
   Select [3] 'pen plot'.
   Select [2] 'set graticule top right'.
   Check voltage on PLAD is now steady 6.7 volts.

   NOTE. It will take approx. 10 seconds after pressing the last button.

Waveforms for AB8

Fig. 22A



Component layout for AB8

Fig. 22
May 86

PART OF
AB8
44828-510B

INSTALLED OPTIONS INDICATOR

DATA BYTE LATCH

IC17 LS244
BUFFER
+5V
CS5f (L)
D0
D7

IC15 LS273
CS58 (L)
CLK
LATCH
OE
+5V

REF VOLT GENERATOR
IC3 ZN404
2·45V ZENER REF
R46 2k2
-12V
IC4 (a) TL072
+14·5V
C4 10n
C3 10n
R48 51k
R47 16k
1
PLAA
IC4 (b) TL072

FROM AB3 PLB
50a
51a
52a
53a
54a
55a
56a
57a
I/O DATA BUS

LATCH SELECTOR
IC20 LS138
G1
G2A G2B
A
B
C
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

FROM AB3 PLB
8a A3
4a A0
5a A1
6a A2
34a CS5X (L)
9a IOWR (L)
10a IORD (L)
IC18 (d) LS08

D-A CONTROL BYTE LATCH
CS59 (L)
IC16 LS374
CLK
OE

33a +14·5V
C40 33µ
1a, 1b, 2a, 2b +5V
C43 33µ
59a,59b,60a,60b
C44 33µ
C45 33µ
FROM AC0
4b, 5b, 6b, 8b, 9b
10b, 11b, 12b
50b,51b,52b,53b
54b,55b,56b,57b
3a -5V
C46 33µ
3b -12V
C41 33µ
58a
C42 33µ

SUPPLY LINE TABLE			
IC	+14·5V	+5V	GROUND
IC1		14	7
IC2		14	7
IC5	1		8,28
IC6	1		8,28
IC7		16	8
IC8		14	7
IC10		20	10
IC11		14	7
IC13		14	7
IC14		14	7
IC15		20	10
IC16		20	10
IC17		20	10
IC18		14	7
IC19		14	7
IC20		16	8

ICS DECOUPLED AT +V TO GROUND BY 10n CAPACITOR

CS5b (L) → TO SHEET 2 IC14 PIN 3

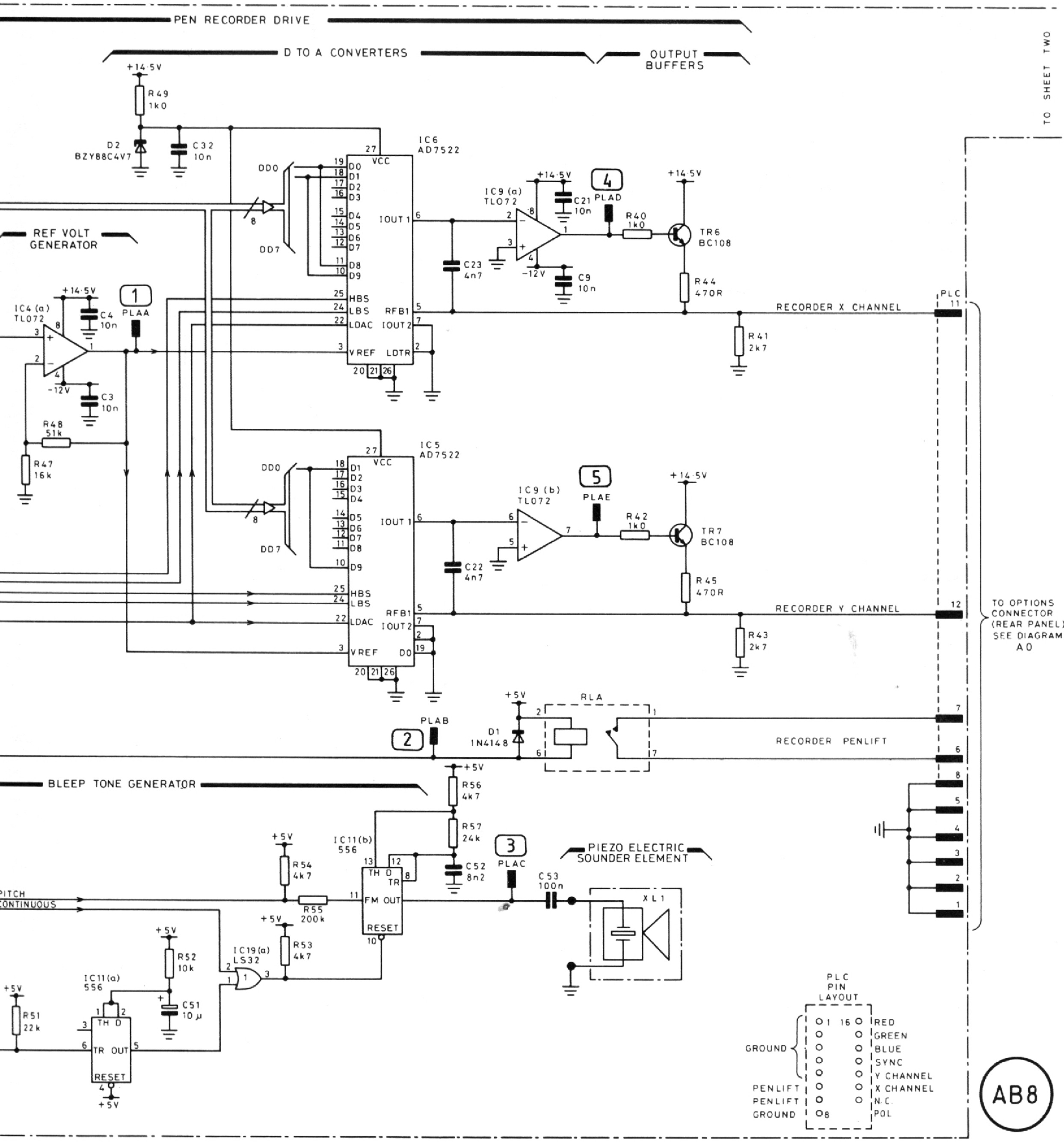
BLEEP TONE GENERA

BLEEP CONTROL LATCH
CS5A (L)
C57 150p
IC10 LS273
PITCH
CONTINUOUS
BLEEP TRIG
IC2 (f) LS04
RESET
PLB 49a
FROM AB3 PLB 49a
C50 10n
R51 22k
IC11(a) 556
TH D
TR OUT
RESET

✶ FOR CONNECTION DETAILS SEE CI

Drg.No. Z44828-510B
Sh.1 Iss.3

AB8 : Penp



R CONNECTION DETAILS SEE CIRCUIT AC0

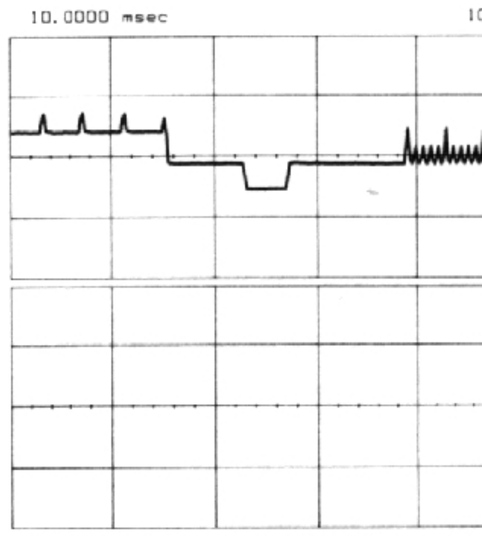
AB8: Penplot & R,G,B video

BOARD : AB8
KEY OF FUNCTIONS (concluded)

6	SYNC AMPLIFIER OUTPUT
7	COMPOSITE VIDEO OUTPUT
8	COMPOSITE SYNCS
9	MINOR GRATICULE INFORMATION (L)
10	MAJOR GRATICULE INFORMATION (L)
11	A LINE (L)
12	A INFILL (L)
13	B INFILL (L)
14	B LINE (L)
15	READ IN BRIGHT UP (L)
16	MARKER CHANNEL OVERDRIVE
17/18	RED VIDEO
19/20	GREEN VIDEO
21/22	BLUE VIDEO
23	A CHANNEL STRONG HUE
24	A CHANNEL NORMAL HUE
25	B CHANNEL STRONG HUE
26	B CHANNEL NORMAL HUE
27	GRAT CHANNEL STRONG HUE
28	GRAT CHANNEL NORMAL HUE
29	STRONG HUE CONTROL
30	NORMAL HUE CONTROL

7 BOARD : AB8

FUNCTION : COMPOSITE VIDEO OUTPUT



TEST POINT : PLAH
GROUND POINT : R66 (end adjacent to
SCOPE SETTING
CH1 : 200 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : CH2, manual
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 10 µs/DIV
MODE : CH1 only
Main timebase only
Set main trigger level fo

6 BOARD : AB8

FUNCTION : SYNC AMPLIFIER OUTPUT.

TEST POINT : PLAK
GROUND POINT : C7 (end adjacent to PLAK)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : CH2, manual
MAIN TIMEBASE : 20 µs/DIV

PROCEDURE :

1. Press [PRESET]. Check for a waveform similar to that on PLAF except that the LOW states are +8 volts, and HIGH states at +10 volts.

7 continued

PROCEDURE :

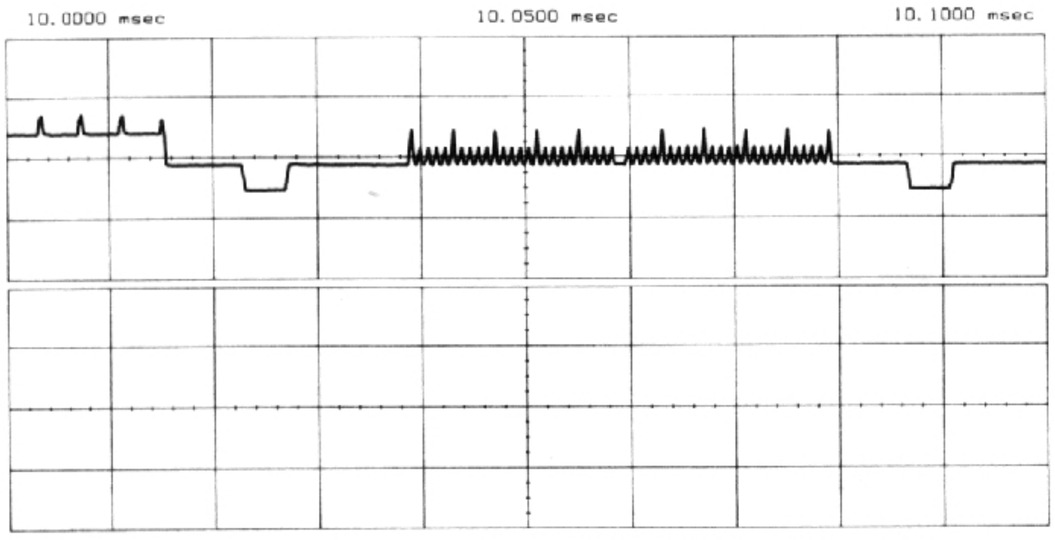
1. Press [PRESET]. Set GRATICUL
Check for a waveform similar t
except that the signal size is
of 10, and is a.c. coupled (no

2. Change timebase to 2 ms/DIV an
by B' with delay trigger set t
Adjust the delay (scope) to ge
10 ms after the scope trigger.
Select 'B' sweep only ('delaye
Check for a waveform similar t
sync and video components.

Fig. 23A
Chap. 7
Page 68

7 BOARD : AB8

FUNCTION : COMPOSITE VIDEO OUTPUT



TEST POINT : PLAH
GROUND POINT : R66 (end adjacent to R64)
SCOPE SETTING
CH1 : 200 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : CH2, manual
MAIN TIMEBASE : 20 µs/DIV
DELAY TIMEBASE : 10 µs/DIV
MODE : CH1 only
Main timebase only
Set main trigger level for display

7 continued

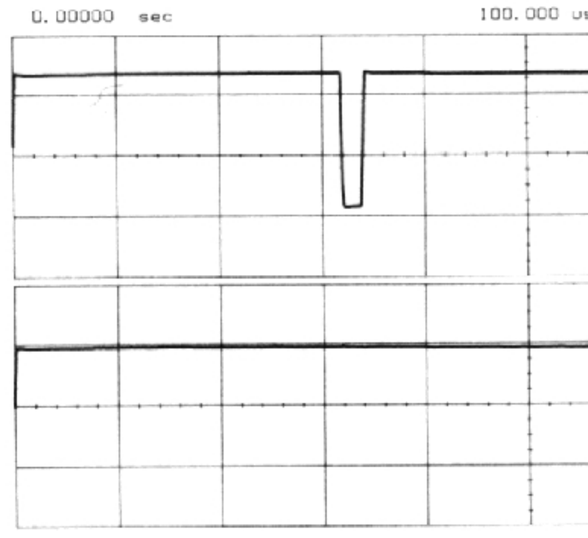
PROCEDURE :

1. Press [PRESET]. Set GRATICULE INTENSITY to max.
Check for a waveform similar to that found on PLAF,
except that the signal size is scaled down by a factor
of 10, and is a.c. coupled (not referenced to ground).

2. Change timebase to 2 ms/DIV and sweep to 'A intensified
by B' with delay trigger set to AUTO (or 'B sweep after A).
Adjust the delay (scope) to get the delayed sweep occurring
10 ms after the scope trigger.
Select 'B' sweep only ('delayed sweep').
Check for a waveform similar to waveform diagram, showing
sync and video components.

8 BOARD : AB8

FUNCTION : COMPOSITE SYNCS



TEST POINT : PLAF
GROUND POINT : C10 (end adjacent to C19)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER: CH2, manual
MAIN TIMEBASE : 20 µs/DIV
MODE : CH1, CH2 alt

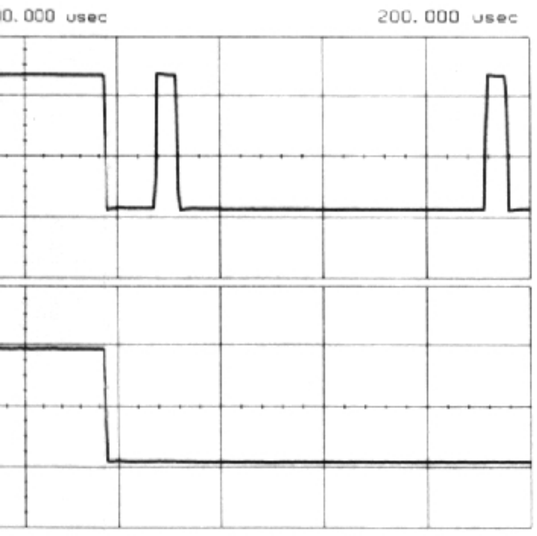
8 continued

PROCEDURE :

1. Press [PRESET]. Adjust scope trigge
Check for the following on scope CH1

0 - 64 µs TTL HIGH
64 - 68 µs TTL LOW
68 - 118 µs TTL HIGH } Point corre
118 - 128 µs TTL LOW }
128 - 132 µs TTL HIGH
132 - 192 µs TTL LOW

Waveforms for AB8



19)

rigger to obtain display.
CH1 :

corresponds with scope CH2

9 BOARD : AB8

FUNCTION : MINOR GRATICULE INFORMATION (L).

TEST POINT : PLAL
GROUND POINT : R66 (end adjacent to R14)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Adjust trigger level to obtain display.
Check for the following :

0	-	2.8 ms	- TTL HIGH
2.8	-	19 ms	- TTL LOW pulses*
19	-	20.8 ms	- TTL HIGH

*These LOW pulses will be too narrow to view accurately on this board. If a fault is suspected in this area, it should be investigated on board AB7.

10 BOARD : AB8

FUNCTION : MAJOR GRATICULE INFORMATION (L).

TEST POINT : PLAM
GROUND POINT : R66 (end adjacent to R64)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : -ve, CH2, manual
MAIN TIMEBASE : 2 ms/DIV
MODE : CH1 only

PROCEDURE :

1. Press [PRESET]. Adjust trigger level to obtain display.
Check for the following :

0	-	2.8 ms	- TTL HIGH
2.8	-	19 ms	- TTL LOW pulses*
19	-	20.8 ms	- TTL HIGH

*These low pulses will be too narrow to view accurately on this board. If a fault is suspected in this area, it should be investigated on board AB7.

(See Fig.23 for waveform 12)

11 BOARD : AB8

FUNCTION : A LINE (L)

TEST POINT : PLAP
GROUND POINT : C2 (end adjacent to R48)
SCOPE SETTING
TRIGGER : manual -ve,
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. Press [PRESET]. Check for LOW TTL pulses, mostly 100 ns long.

NOTE. It is impractical to investigate thoroughly on this board; thorough investigation should be done on AB6.

13 BOARD : AB8

FUNCTION : B INFILL (L).

TEST POINT : PLAR
GROUND POINT : C2 (end adjacent to R48)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : CH2, -ve, manual

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger for display.
Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [2] 'enter display data & linearity tests'.
Check scope CH1 for the following :

0 - 3 ms - TTL HIGH
3 - 19 ms - TTL pulses (LOW)*, 600 ns long
19 - 20.8 ms - TTL HIGH

*These low pulses will be too narrow and infrequent to view accurately here. If a fault is suspected, investigate on AB5.

14 BOARD : AB8

FUNCTION : B LINE (L).

TEST POINT : PLAS
GROUND POINT : C2 (end adjacent to R48)
SCOPE SETTING
TRIGGER : manual, -ve
MAIN TIMEBASE : 200 ns/DIV

PROCEDURE :

1. PRESS [PRESET], 'display B [VIEW]'.
Check for LOW TTL pulses, mostly 100 ns long.

*It is impractical to investigate thoroughly on this board.
Thorough investigation should be done on AB5.

15 BOARD : AB8

FUNCTION : READ IN BRIGHT UP (L).

TEST POINT : PLAT
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
TRIGGER : -ve
MAIN TIMEBASE : 10 µs/DIV

PROCEDURE :

1. Press [PRESET]. Press 'horizontal sw
Check scope CH1 for LOW (TTL) pulses,
increase in length from zero to 40 µs
(50 seconds).

16 BOARD : AB8

FUNCTION : MARKER CHANNEL OVERDRIVE.

TEST POINT : PLAV
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
TRIGGER : -ve, manual
MAIN TIMEBASE : 200 ns/DIV

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Press 'markers [MKR
Adjust scope trigger for display.
Check for LOW (TTL) pulses, approx. 16
occurring approx. every 21 ms.

Fig. 23B
Chap. 7
Page 70/69

BRIGHT UP (L).

end adjacent to C1)

: 10 µs/DIV

. Press 'horizontal sweep time [↑]' to select 5 s/DIV.
1 for LOW (TTL) pulses, occurring every 64 µs, which
ngth from zero to 40 µs over the 2380 sweep period

HANNEL OVERDRIVE.

end adjacent to C1)

manual
: 200 ns/DIV

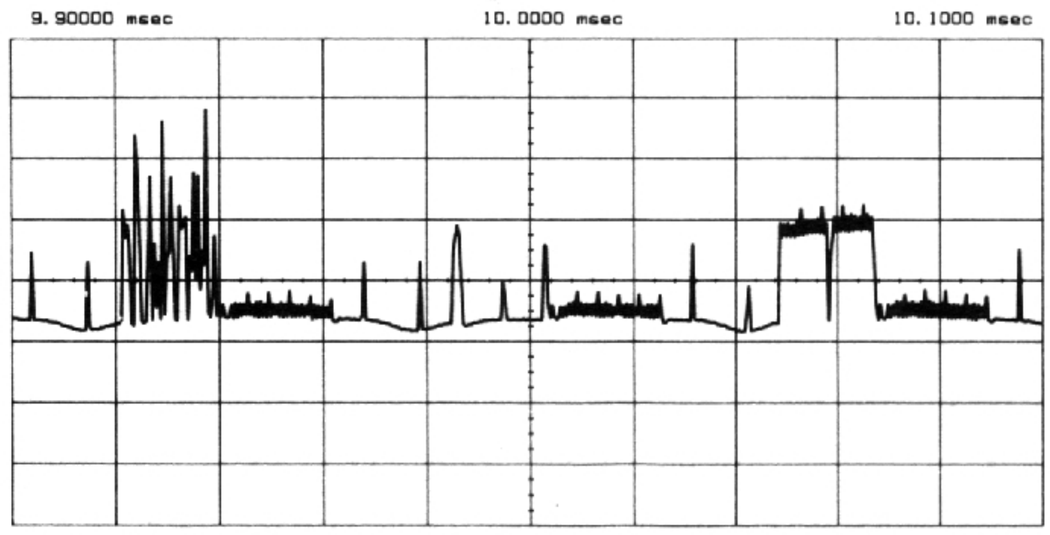
ood or storage scope.

. Press 'markers [MKR 1]'.
rigger for display.
(TTL) pulses, approx. 160 ns long
ox. every 21 ms.

17 BOARD : AB8

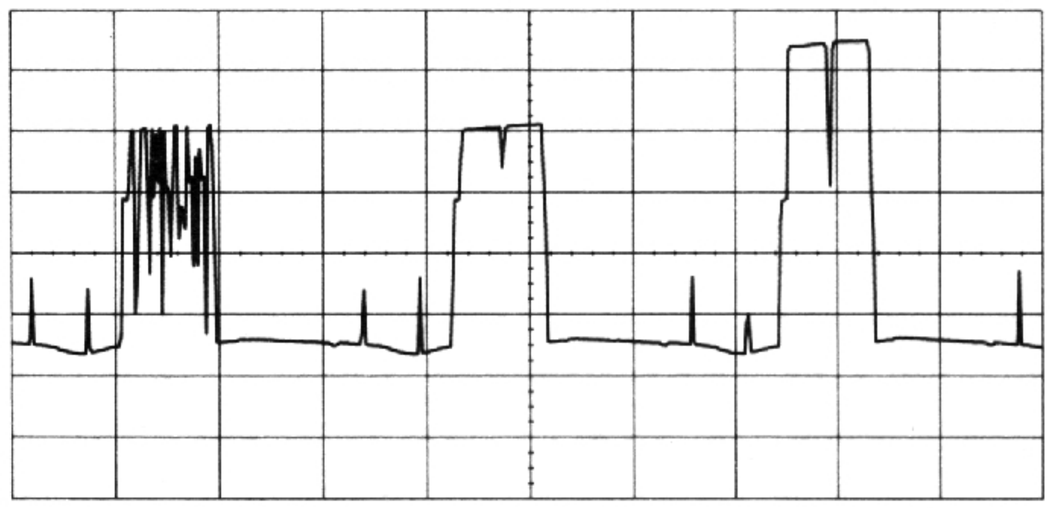
18 FUNCTION : RED VIDEO.

17



Ch. 1 - 500.0 mvolts/div
Timebase - 20.0 usec/div
Offset - 0.000 volts
Delay - 10.0000 msec

18



Ch. 1 - 500.0 mvolts/div
Timebase - 20.0 usec/div
Offset - 0.000 volts
Delay - 10.0000 msec

17 BOARD : AB8 continued

18

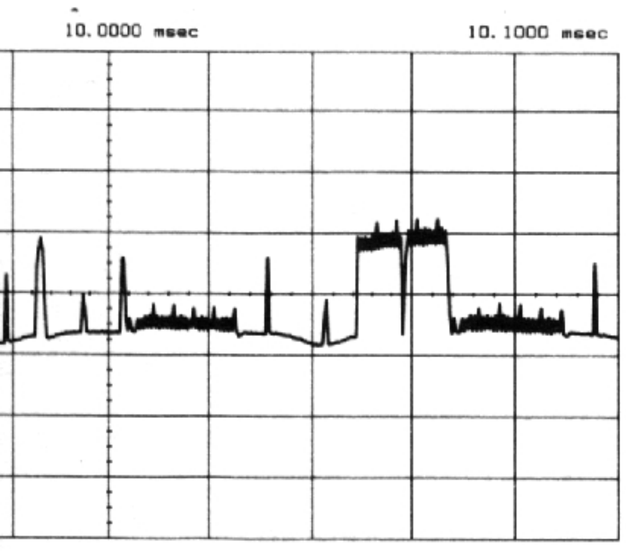
TEST POINT : PLAW
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH1 : 200 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1 only
Delay set to ~ halfway (500 on most scopes) (10 ms)
'B' sweep (delayed sweep) only
Delay trigger : auto ('B' sweeps after end of 'A' sweep)

NOTE. Use scope hood or storage scope.

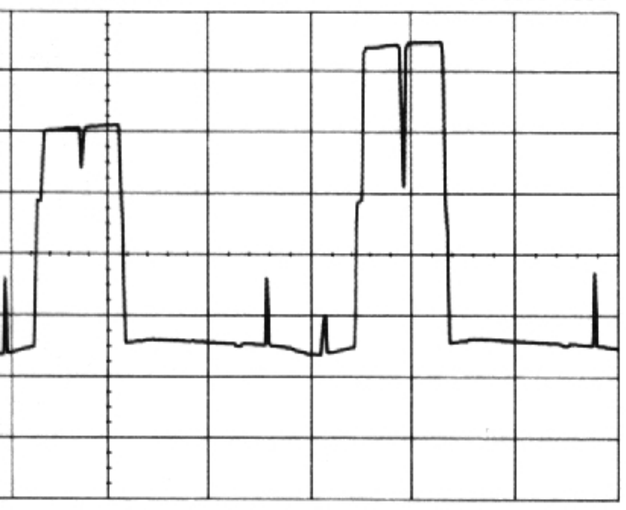
PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [5] 'enter option board tests'.
Adjust main trigger to obtain display.
Check for waveform similar to waveform diagram 17.

2. Select [2] 'colour palette'.
Select [2] 'strong colours'.
Check for waveform similar to waveform diagram 18.



/div — Offset - 0.000 volts
Delay - 10.0000 msec



/div — Offset - 0.000 volts
Delay - 10.0000 msec

to C1)

(500 on most scopes) (10 ms)
ep) only
'B' sweeps after end of 'A' sweep)

e scope.

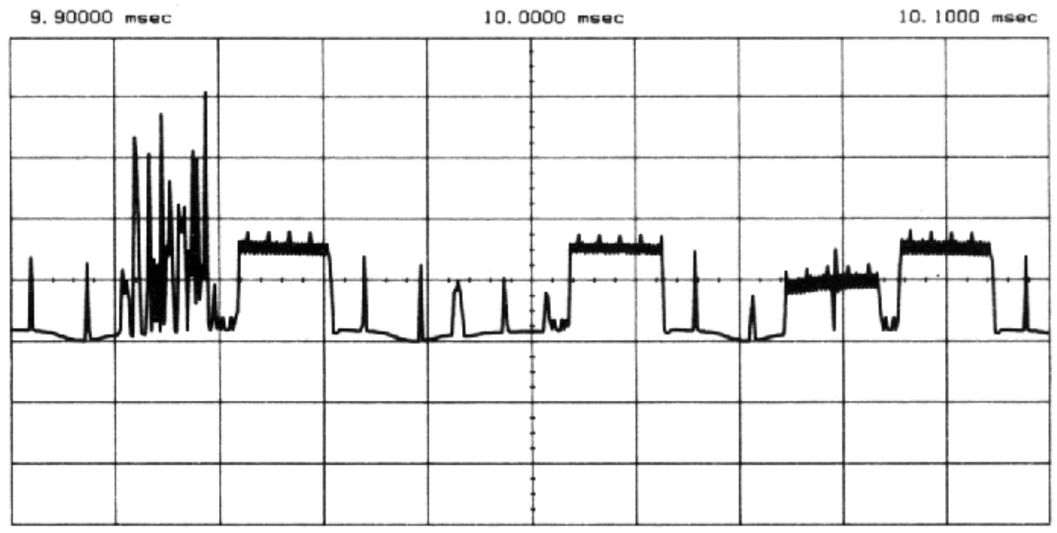
UG OPERATIONS mode.
idence tests'.
ard tests'.
in display.
to waveform diagram 17.

.
.
to waveform diagram 18.

19 BOARD : AB8

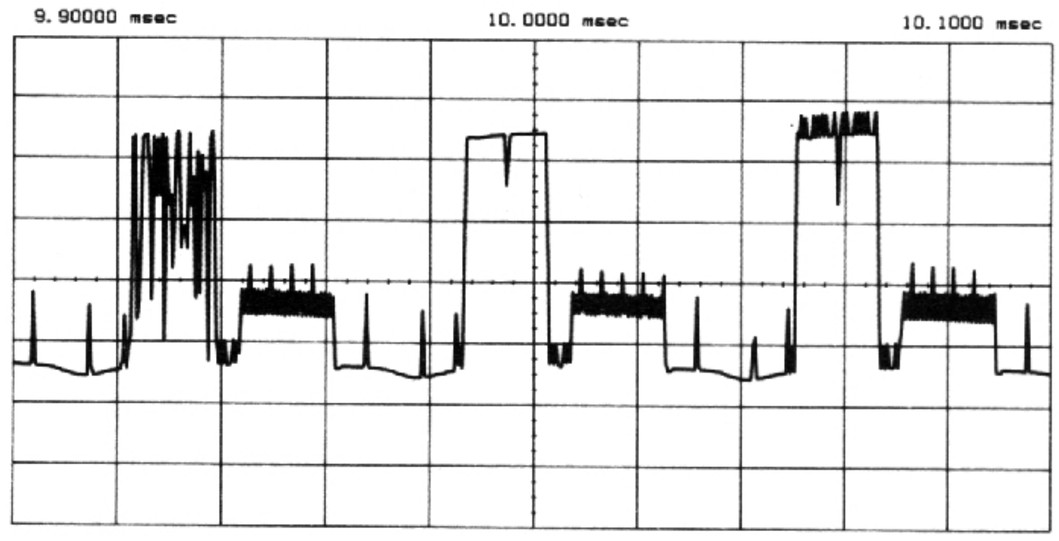
20 FUNCTION : GREEN VIDEO.

19



Ch. 1 - 500.0 mvolts/div — Offset - 0.000 volts
Timebase - 20.0 usec/div — Delay - 10.0000 msec

20



Ch. 1 - 500.0 mvolts/div — Offset - 0.000 volts
Timebase - 20.0 usec/div — Delay - 10.0000 msec

19 BOARD : AB8 continued

20

TEST POINT : PLAX
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH1 : 200 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1 only
Delay set to ~ halfway (500 on most scopes) (10 ms)
'B' sweep (delayed sweep) only
Delay trigger : auto ('B' sweeps after end of 'A' sweep)

NOTE. Use scope hood or storage scope.

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [5] 'enter option board tests'.
Adjust main trigger to obtain display.
Check for waveform similar to waveform diagram 19.

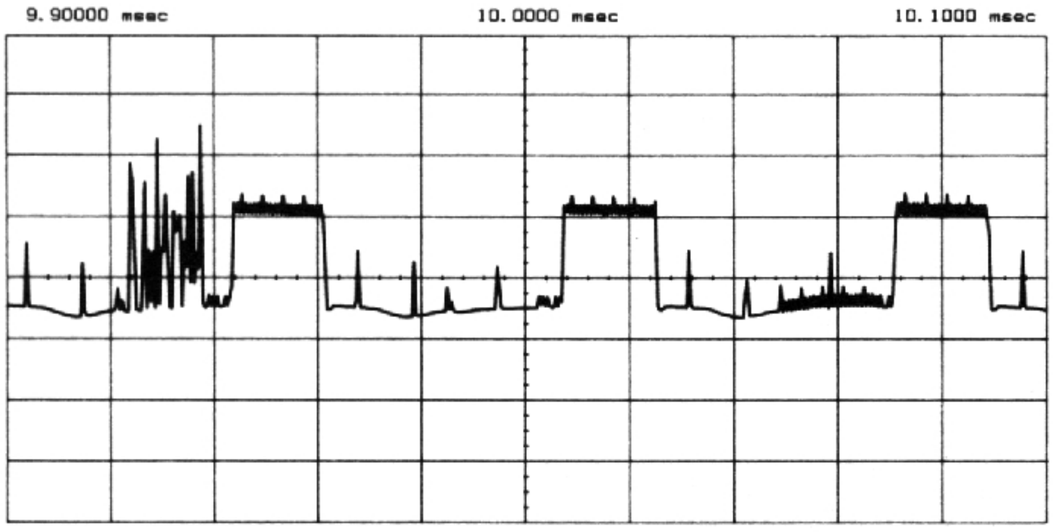
2. Select [2] 'colour palette'.
Select [2] 'strong colours'.
Check for waveform similar to waveform diagram 20.

Fig. 23B

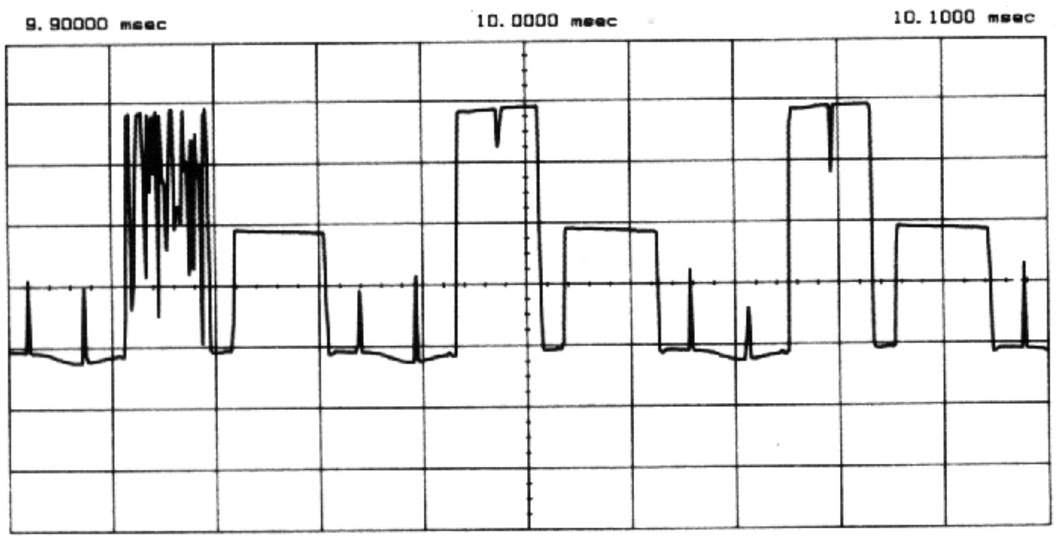
May 86

21 BOARD : AB8

22 FUNCTION : BLUE VIDEO.



Ch. 1 - 500.0 mvolts/div
Timebase - 20.0 usec/div
Offset - 0.000 volts
Delay - 10.0000 msec



Ch. 1 - 500.0 mvolts/div
Timebase - 20.0 usec/div
Offset - 0.000 volts
Delay - 10.0000 msec

21 BOARD : AB8 continued

22

TEST POINT : PLAY
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH1 : 200 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1 only
Delay set to ~ halfway (500 on most scopes) (10 ms)
'B' sweep (delayed sweep) only
Delay trigger : auto ('B' sweeps after end of 'A' sweep)

NOTE. Use scope hood or storage scope.

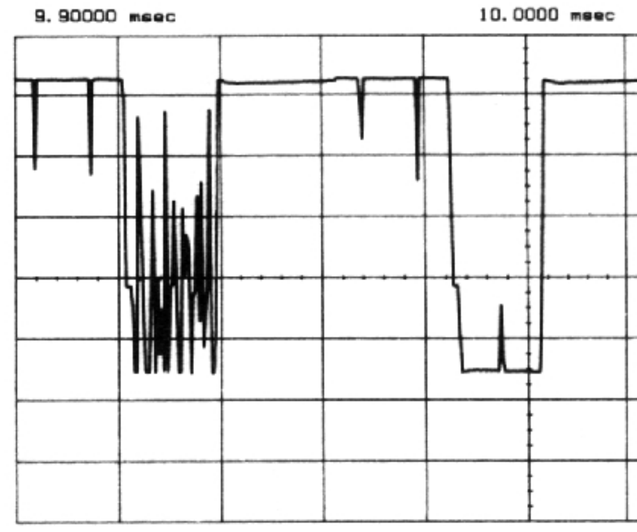
PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [5] 'enter option board tests'.
Adjust main trigger to obtain display.
Check for waveform similar to waveform diagram 21.

2. Select [2] 'colour palette'.
Select [2] 'strong colours'.
Check for waveform similar to waveform diagram 22.

23 BOARD : AB8

FUNCTION : A CHANNEL STRONG HUE.



Ch. 1 - 500.0 mvolts/div
Timebase - 20.0 usec/div

TEST POINT : PLBA
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH1 : 500 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1 only
Delay set to ~ halfway (500 on mos
Delay trigger : auto (sweep 'B' af

NOTE. Use scope hood or storage scope.

23 BOARD : AB8 continued

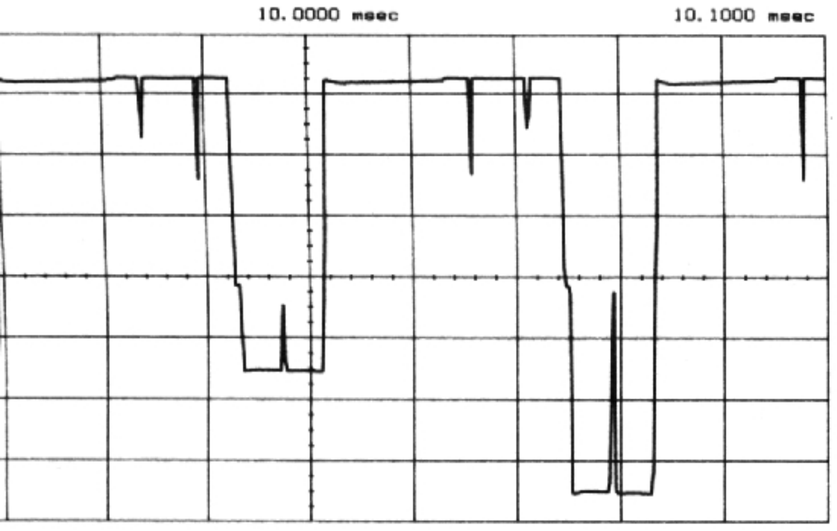
PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATION
Select [2] 'upper unit confidence tests
Select [5] 'enter options board tests'.
Select [2] 'colour palette'.
Select [2] 'strong colours'.
Manually adjust scope trigger level for
Check for display similar to waveform d

2. Select [1] 'normal colours'.
Check scope CH1 now stays at +5 V (±0.2

Fig. 23C
Chap. 7
Page 72/71

STRONG HUE.



- 500.0 mvolts/div Offset - 3.000 volts
- 20.0 usec/div Delay - 10.0000 msec

nd adjacent to C1)

V
n IC8 pin 13
l, -ve, CH2
2 ms/DIV
: 20 µs/DIV

to ~ halfway (500 on most scopes) (10 ms)
ger : auto (sweep 'B' after end of sweep 'A')

od or storage scope.

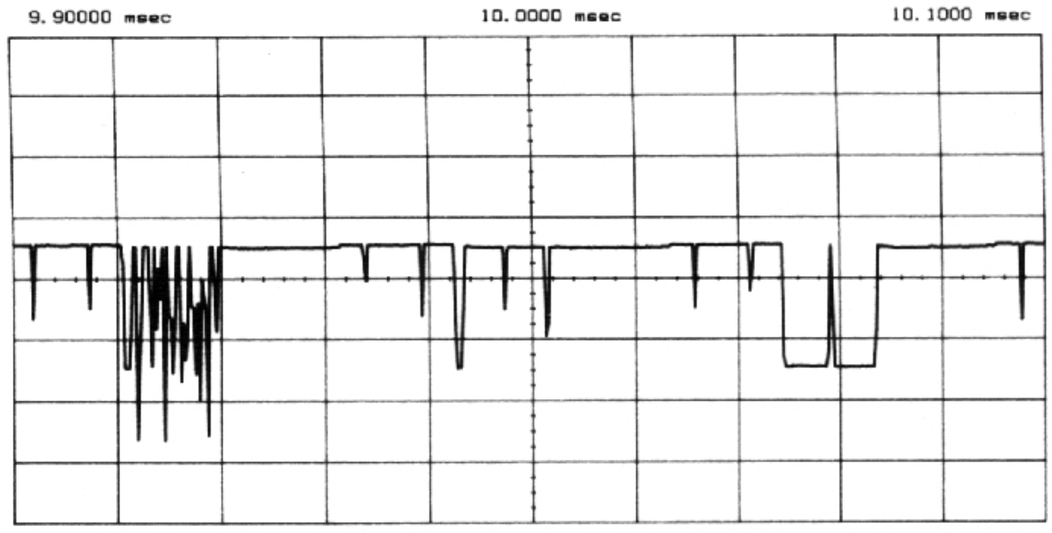
tinued

Enter DEBUG OPERATIONS mode.
er unit confidence tests'.
er options board tests'.
our palette'.
ong colours'.
scope trigger level for display.
ay similar to waveform diagram.

mal colours'.
now stays at +5 V (±0.2 V).

24 BOARD : AB8

FUNCTION : A CHANNEL NORMAL HUE.



Ch. 1 - 500.0 mvolts/div Offset - 4.000 volts
Timebase - 20.0 usec/div Delay - 10.0000 msec

TEST POINT : PLBB
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH1 : 500 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1 only
Delay set to ~ halfway (500 on most scopes) (10 ms)
Delay trigger : auto (sweep 'B' after end of sweep 'A')

NOTE. Use scope hood or storage scope.

24 BOARD : AB8 continued

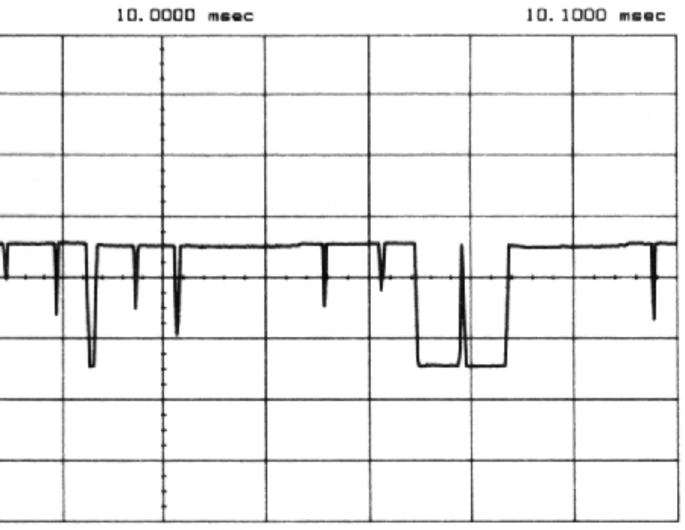
PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [5] 'enter options board tests'.
Select [2] 'colour palette'.
Select [1] 'normal colours'.
Manually adjust scope trigger level for display.
Check for display similar to waveform diagram.

2. Select [2] 'strong colours'.
Check scope CH1 now stays at +5 V (±0.2 V).

Waveforms for AB8

UE.



volts/div — Offset - 4.000 volts
c/div — Delay - 10.0000 msec

nt to C1)

13
H2
IV

way (500 on most scopes) (10 ms)
o (sweep 'B' after end of sweep 'A')

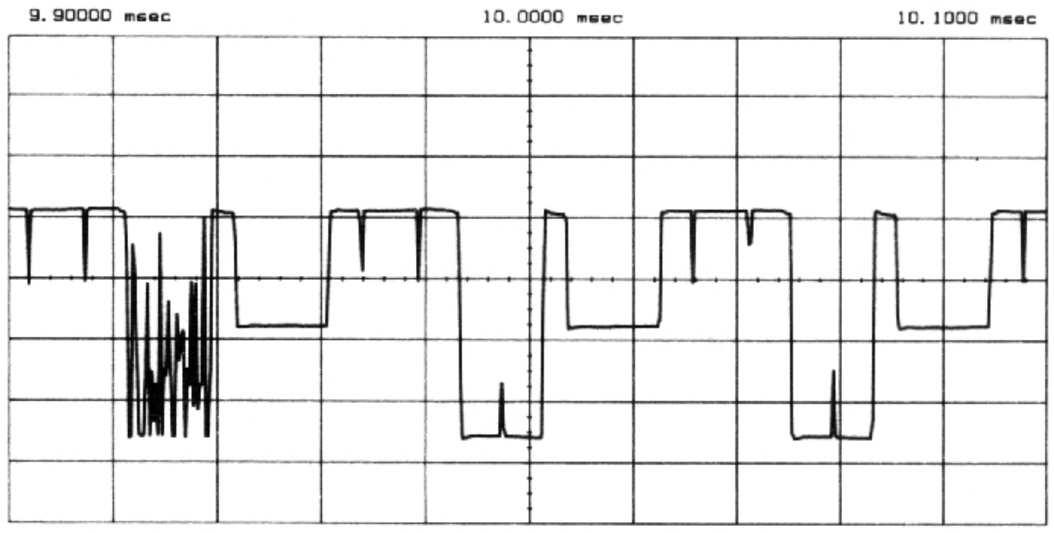
rage scope.

DEBUG OPERATIONS mode.
onfidence tests'.
s board tests'.
te'.
rs'.
igger level for display.
r to waveform diagram.

rs'.
s at +5 V (±0.2 V).

25 BOARD : AB8

FUNCTION : B CHANNEL STRONG HUE.



Ch. 1 - 500.0 mvolts/div — Offset - 4.000 volts
Timebase - 20.0 usec/div — Delay - 10.0000 msec

TEST POINT : PLBC
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH1 : 500 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1 only
Delay set to ~ halfway (500 on most scopes) (10 ms)
Delay trigger : auto (sweep 'B' after end of sweep 'A')

NOTE. Use scope hood or storage scope.

25 BOARD : AB8 continued

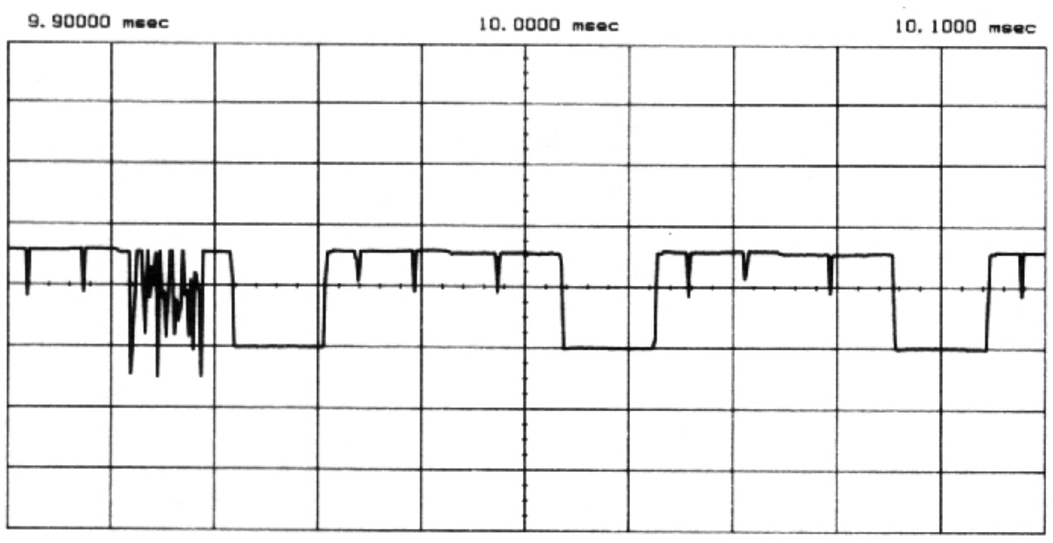
PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [5] 'enter options board tests'.
Select [2] 'colour palette'.
Select [2] 'strong colours'
Manually adjust scope trigger level for display.
Check for display similar to waveform diagram.

2. Select [1] 'normal colours'.
Check scope CH1 now stays at +5 V (±0.2 V).

26 BOARD : AB8

FUNCTION : B CHANNEL NORMAL HUE.



Ch. 1 = 500.0 mvolts/div
Timebase = 20.0 usec/div
Offset = 4.000 volts
Delay = 10.0000 msec

TEST POINT : PLBD
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH1 : 500 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1 only
Delay set to ~ halfway (500 on most scopes) (10 ms)
Delay trigger : auto (sweep 'B' after end of sweep 'A')

NOTE. Use scope hood or storage scope.

26 BOARD : AB8 continued

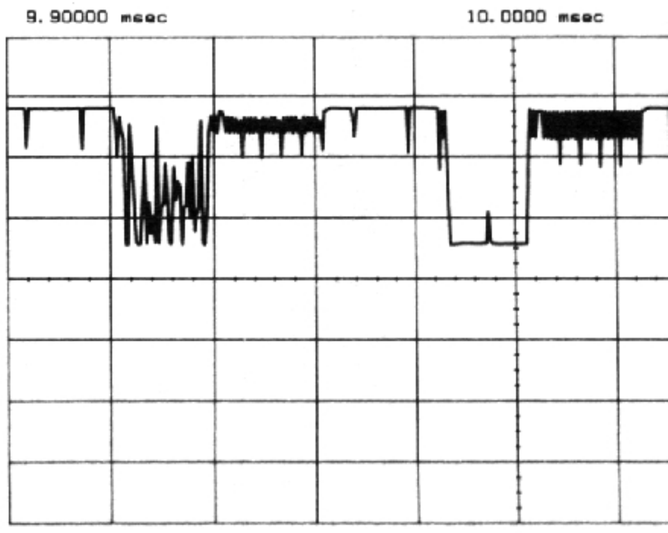
PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [5] 'enter options board tests'.
Select [2] 'colour palette'.
Select [1] 'normal colours'.
Manually adjust scope trigger level for display.
Check for display similar to waveform diagram.

2. Select [2] 'strong colours'.
Check scope CH1 now stays at +5 V (±0.2 V).

27 BOARD : AB8

FUNCTION : GRAT CHANNEL STRONG HUE.



Ch. 1 = 500.0 mvolts/div
Timebase = 20.0 usec/div

TEST POINT : PLBE
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH1 : 500 mV/DIV
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1 only
Delay set to ~ halfway (500 on most
Delay trigger : auto (sweep 'B' afte

NOTE. Use scope hood or storage scope.

27 BOARD : AB8 continued

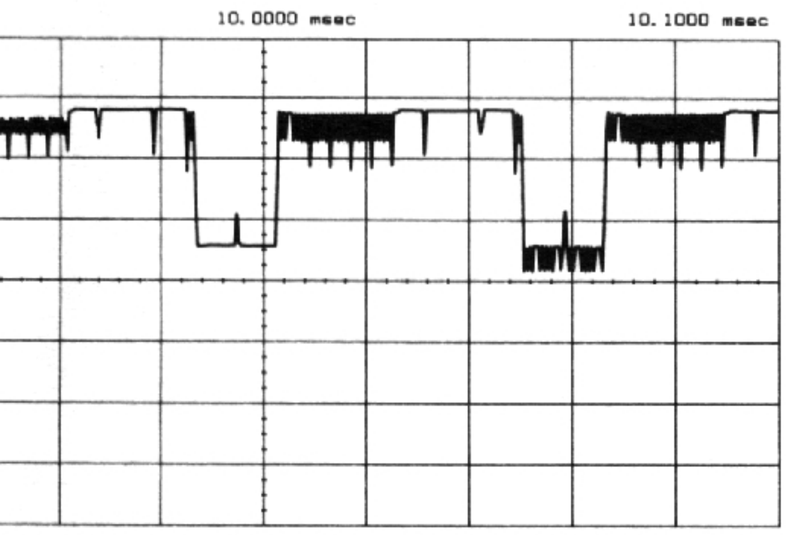
PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS
Select [2] 'upper unit confidence tests'
Select [5] 'enter options board tests'.
Select [2] 'colour palette'.
Select [2] 'strong colours'.
Manually adjust scope trigger level for
Check for display similar to waveform di

2. Select [1] 'normal colours'.
Check scope CH1 now stays at +5 V (±0.2

Fig. 23D
Chap. 7
Page 74/73

L STRONG HUE.



500.0 mvolts/div — Offset - 3.000 volts
20.0 usec/div — Delay - 10.0000 msec

adjacent to C1)

IC8 pin 13
-ve, CH2
ms/DIV
20 µs/DIV

~ halfway (500 on most scopes) (10 ms)
r : auto (sweep 'B' after end of sweep 'A')

or storage scope.

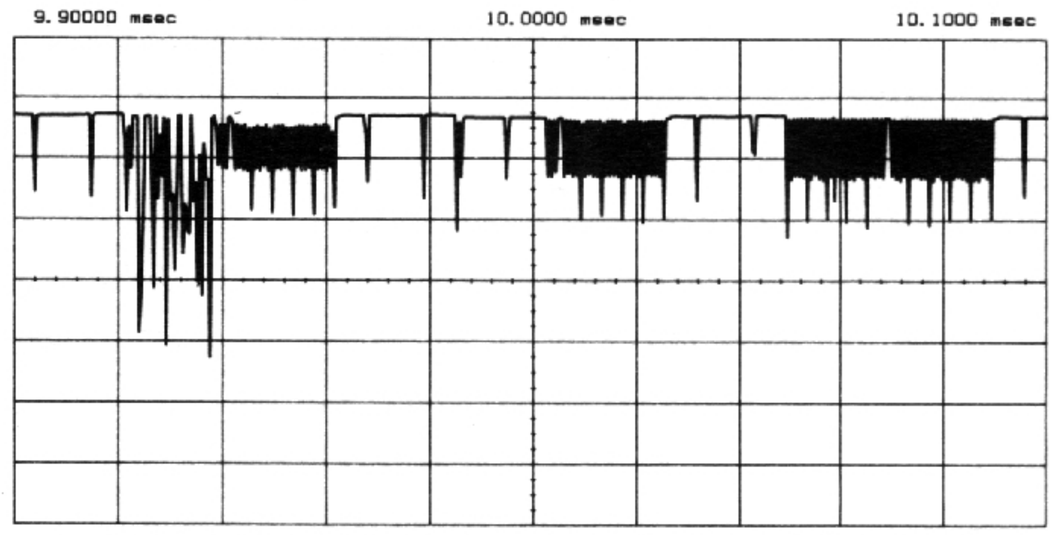
inued

Enter DEBUG OPERATIONS mode.
r unit confidence tests'.
r options board tests'.
ur palette'.
ng colours'.
scope trigger level for display.
y similar to waveform diagram.

al colours'.
now stays at +5 V (±0.2 V).

28 BOARD : AB8

FUNCTION : GRAT CHANNEL NORMAL HUE.



Ch. 1 - 500.0 mvolts/div — Offset - 3.000 volts
Timebase - 20.0 usec/div — Delay - 10.0000 msec

TEST POINT : PLBF
GROUND POINT : C2 (end adjacent to C1)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : manual, -ve, CH2
MAIN TIMEBASE : 2 ms/DIV
DELAY TIMEBASE : 20 µs/DIV
MODE : CH1 only
Delay set to ~ halfway (500 on most scopes) (10 ms)
Delay trigger : auto (sweep 'B' after end of sweep 'A')

NOTE. Use scope hood or storage scope.

28 BOARD : AB8 continued

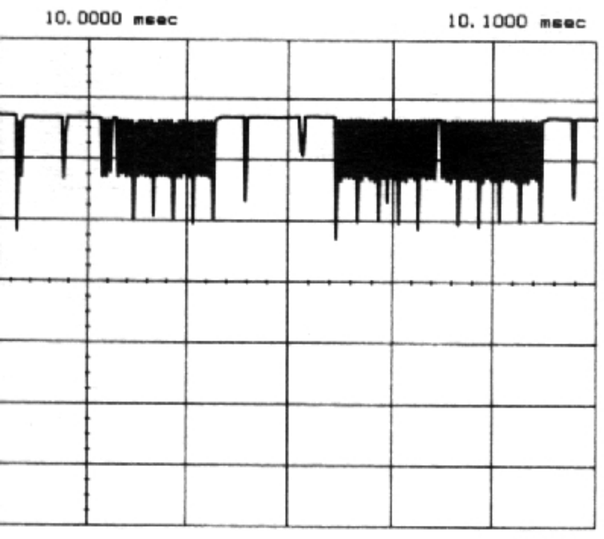
PROCEDURE :

1. PRESS [PRESET]. Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [5] 'enter options board tests'.
Select [2] 'colour palette'.
Select [1] 'normal colours'.
Manually adjust scope trigger level for display.
Check for display similar to waveform diagram.

2. Select [2] 'strong colours'.
Check scope CH1 now stays at +5 V (±0.2 V).

Waveforms for AB8

HUE.



to C1)

3

y (500 on most scopes) (10 ms)
(sweep 'B' after end of sweep 'A')

ge scope.

EBUG OPERATIONS mode.
nfidence tests'.
board tests'.
'.
'.
gger level for display.
to waveform diagram.

'.
at +5 V (±0.2 V).

29 BOARD : AB8

FUNCTION : STRONG HUE CONTROL.

TEST POINT : PLBH
GROUND POINT : C13 (end nearest to R64)
SCOPE SETTING : [DEFAULT]

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
   Select [2] 'upper unit confidence tests'.
   Select [2] 'enter options board tests'.
   Select [2] 'colour palette'.
   Select [2] 'strong colours'.
   Check that scope CH1 shows (TTL) HIGH state.

2. Select [1] 'normal colours'.
   Check that scope CH1 shows (TTL) LOW state.

30 BOARD : AB8

FUNCTION : NORMAL HUE CONTROL.

TEST POINT : PLBJ
GROUND POINT : C13 (end nearest R64)
SCOPE SETTING : [DEFAULT]

PROCEDURE :

1. Press [PRESET]. Enter DEBUG OPERATIONS mode.
   Select [2] 'upper unit confidence tests'.
   Select [2] 'enter options board tests'.
   Select [2] 'colour palette'.
   Select [2] 'strong colours'.
   Check that scope CH1 shows (TTL) LOW state.

2. Select [1] 'normal colours'.
   Check that scope CH1 shows (TTL) HIGH state.

Fig. 23D

May 86

12 BOARD : AB8

FUNCTION : A INFILL (L).

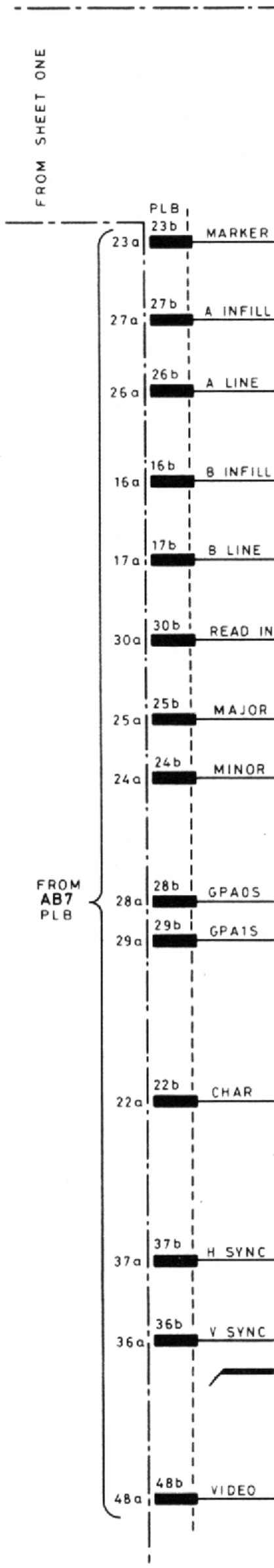
TEST POINT : PLAN
GROUND POINT : C2 (end adjacent to R48)
SCOPE SETTING
CH2 : 2 V/DIV on IC8 pin 13
TRIGGER : CH2, -ve, manual

PROCEDURE :

1. Press [PRESET]. Adjust scope trigger for display.
Enter DEBUG OPERATIONS mode.
Select [2] 'upper unit confidence tests'.
Select [2] 'enter display data & linearity tests'.
Check scope CH1 for the following :

0 - 3 ms - TTL HIGH
3 - 19 ms - TTL pulses (LOW)*, 600 ns long
19 - 20.8 ms - TTL HIGH

*These low pulses will be too narrow and infrequent to view accurately here. If a fault is suspected, investigate on board AB6.



Drg
Sh.

Waveform for AB8

Fig. 23
May 86

PART OF
AB8
44828-510B

FROM SHEET ONE

PLB
23b 23a MARKER
27b 27a A INFILL
26b 26a A LINE
16b 16a B INFILL
17b 17a B LINE
30b 30a READ IN BRIGHT UP
25b 25a MAJOR
24b 24a MINOR

FROM AB7 PLB
28b 28a GPA0S
29b 29a GPA1S
22b 22a CHAR

CHARACTER COLOUR SELECT
+5V
IC7 LS138
G1 G2A G2B A B C Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
IC8(b) LS86
IC8(c)
IC8(a)
IC18(b) LS08
IC18(c)
IC18(a)

SYNC COMBINER
37b 37a H SYNC
36b 36a V SYNC
IC8(d) LS86
8 PLAF
COMPOSITE SYNCS
+5V
R67 2k7
R68 2k2

SYNC AMPLIFIER
+14·5V
R71 220R
R70 1kΩ
6 PLAK
TR4 BC108
C31 33µ
R69 3k3
R72 75R
+5V

MONOCHROME COMPOSITE VIDEO OUTPUT
48b 48a VIDEO
C54 10p
R60 2k4
R64 6k8
R63 2k4
R62 680R
R61 4k7
TR5 2N2369
TR8 BC108
C55 10p
R65 130R
C56 470µ
R66 180R
7 PLAH PLAJ
COMPOSITE VIDEO O/P
PLD 1
2
3
PLC 13

MARKER CHANNEL
IC2(d) LS04
PLAV 16
MARKER

A CHANNEL
PLAN 12
IC2(b)
R1 1k8
R2 750R
A CHANN
IC13(b) LS27
PLAP 11
R3 1k8
R4 750R
A CHAN
IC1(a)
IC1(

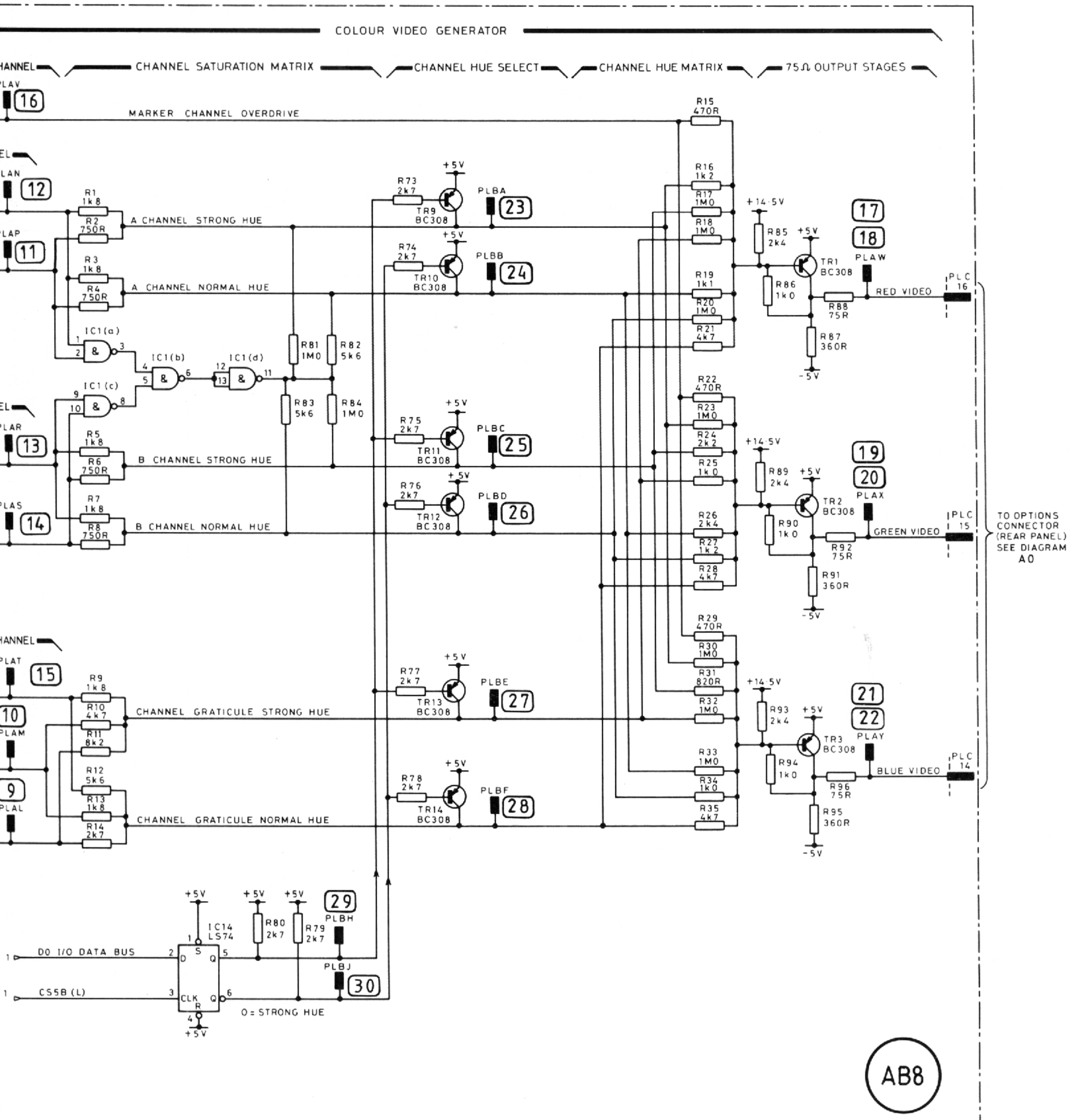
B CHANNEL
IC1(c)
PLAR 13
IC2(a)
R5 1k8
R6 750R
B CHA
PLAS 14
IC13(a)
R7 1k8
R8 750R
B CHAN

GRATICULE CHANNEL
PLAT 15
IC2(e)
R9 1k8
R10 4k7
R11 8k2
R12 5k6
R13 1k8
R14 2k7
CHANN
10 PLAM
IC13(c)
9 PLAL
IC2(c)
CHANN

FROM SHEET 1 D0 I/O DATA BUS 2
FROM SHEET 1 IC20 PIN 12 CS5B (L) 3

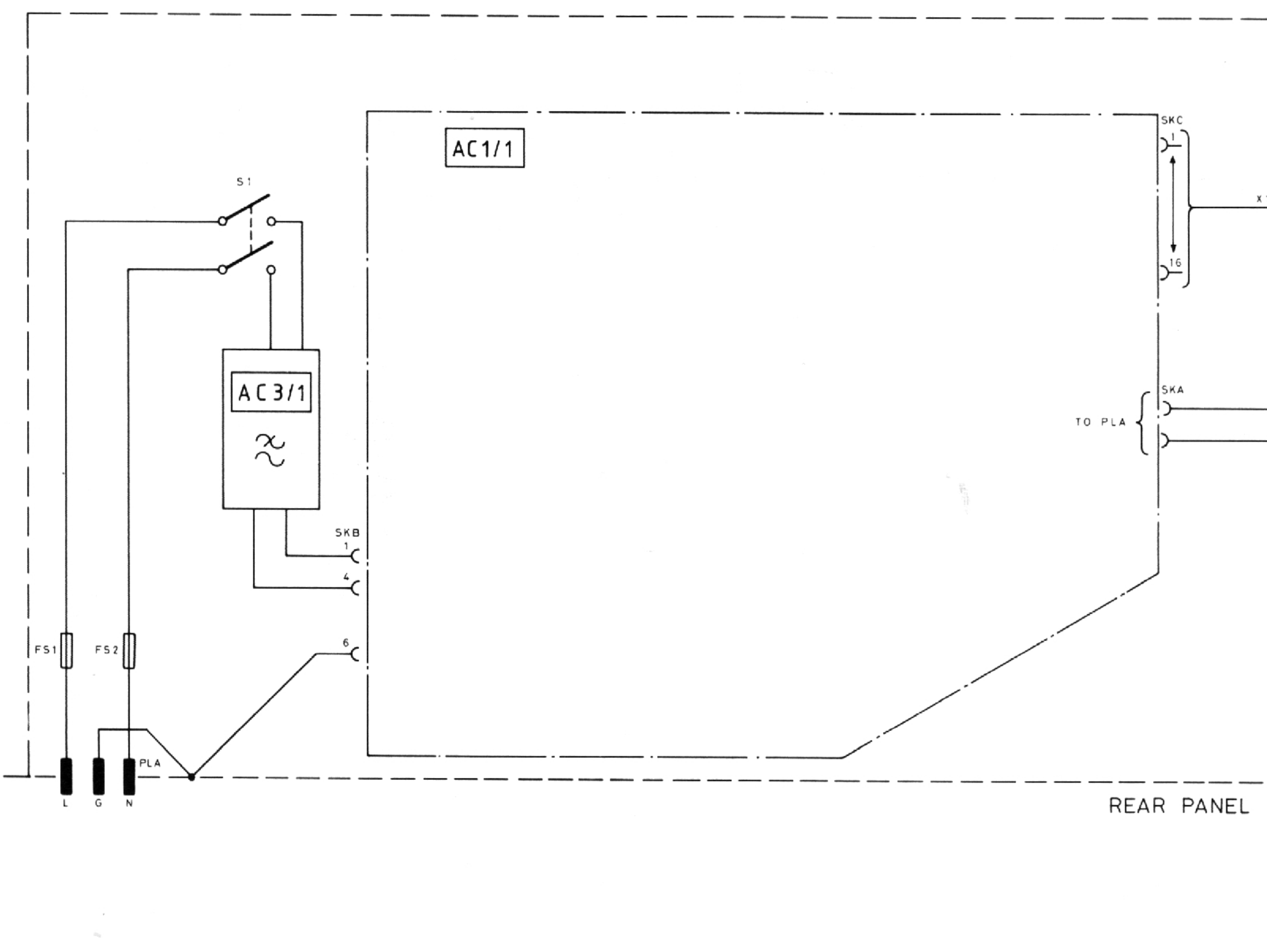
Drg.No. Z44828-510B
Sh.2 Iss.2

AB8: Red, green



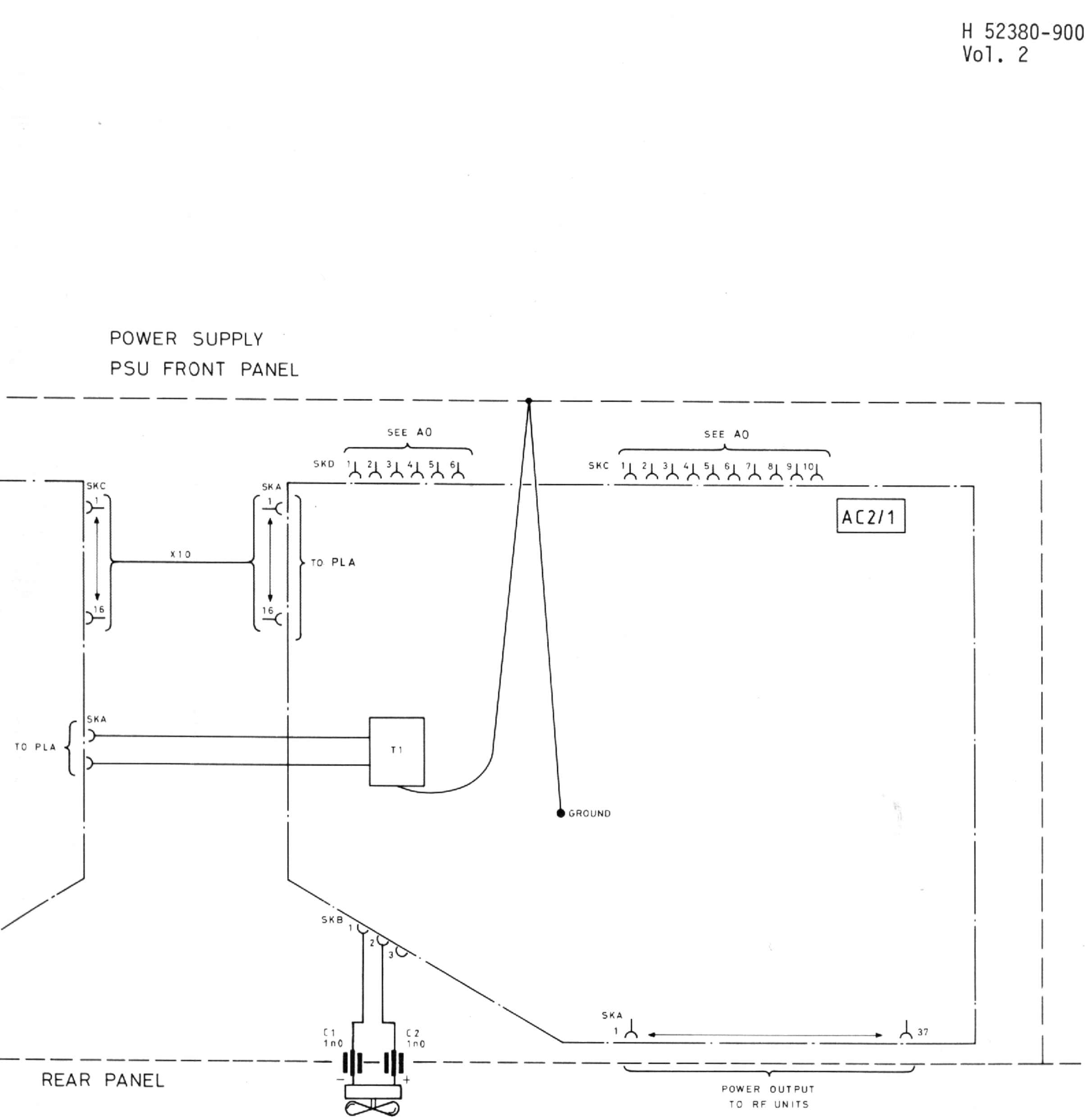
B8: Red, green, blue video

POWER
PSU FR



Drg.No. Z44990-449G
Sh.1 Iss.1

AC0/1 :



AC0/1

AC0/1 : SMPS interconnections

BOARD : AC1/1
KEY OF FUNCTIONS :

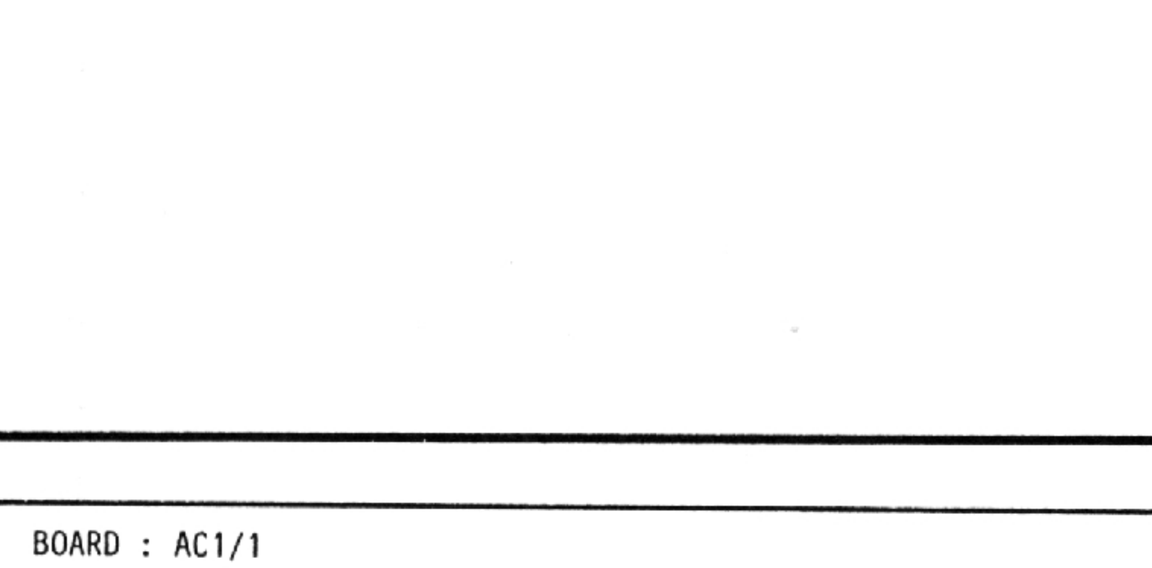
1
2 PRIMARY CURRENT WAVEFORM
3 125 kHz SYNC
4 SYNC
5
6
7 125 kHz SYNC
8
9 125 kHz SYNC
10

---

1 BOARD : AC1/1

2

TEST POINT : TP9 Ch.1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AC1 or AC1/1)

FUNCTION [2] : PRIMARY CURRENT WAVEFORM

TEST POINT : lead from T_3A for Ch. 2

CH. 2 Use a current probe and read screen legend as amps/div in place of volts/div.

---

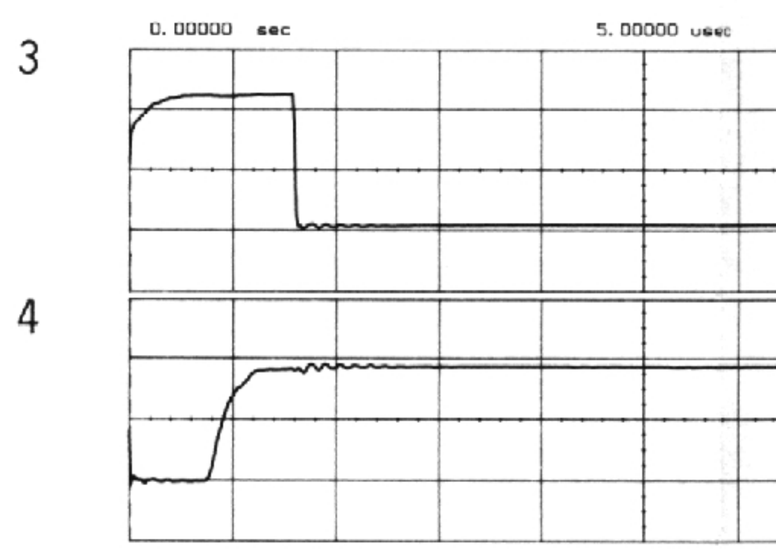
3 BOARD : AC1/1

4

FUNCTION : 125 kHz SYNC.

TEST POINT : TP12 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]

PLE LINK : Ensure that PLE link on board bridge



(AC1 or AC1/1)

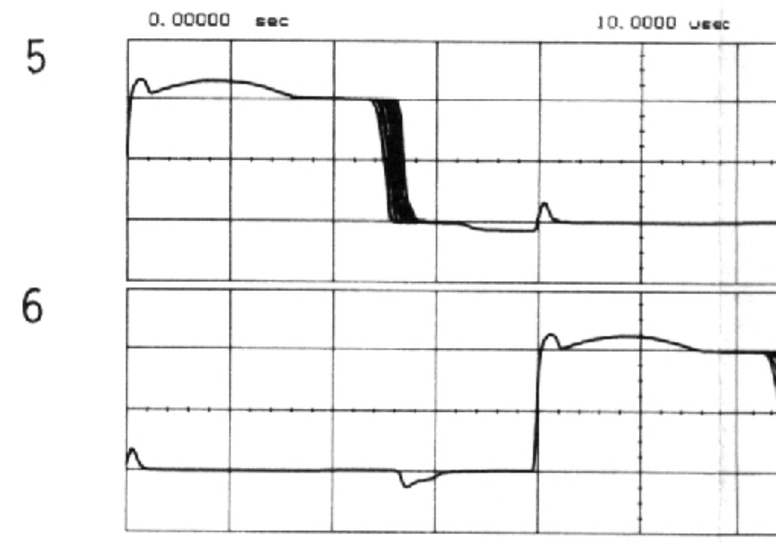
TEST POINT : TP13 for Ch. 2.

---

5 BOARD : AC1/1

6

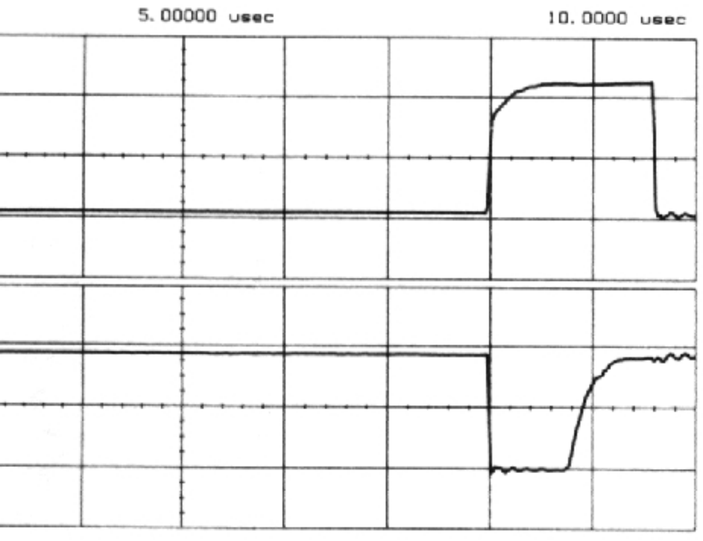
TEST POINT : TP8 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AC1 or AC1/1)

TEST POINT : TP9 for Ch. 2.

ink on board bridges 1-2.



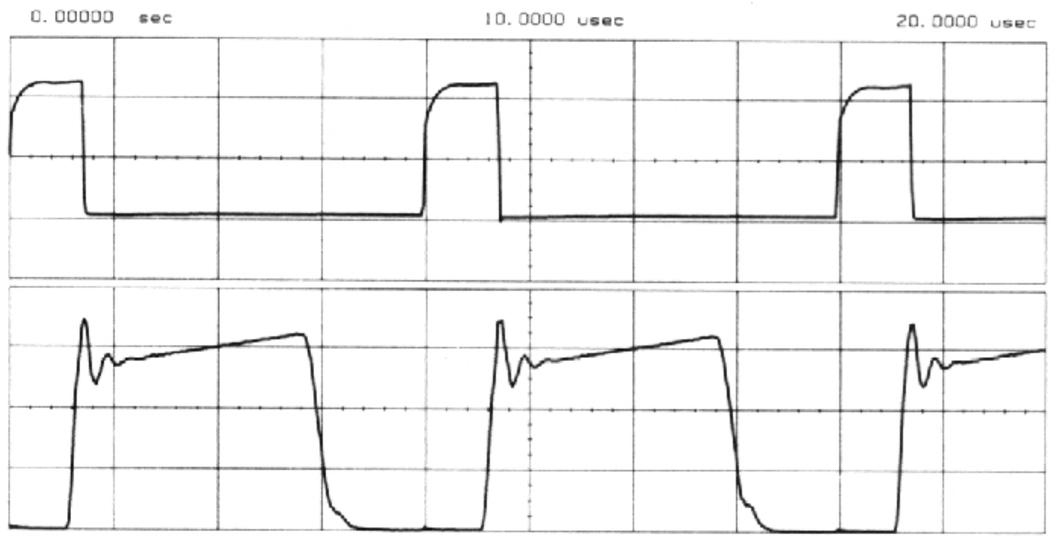
volts/div	Offset	=	2.000 volts
volts/div	Offset	=	1.000 volts
sec/div	Delay	=	0.00000 sec
0 usec			
0 sec	Stop	=	8.00000 usec

7 BOARD : AC1/1

8

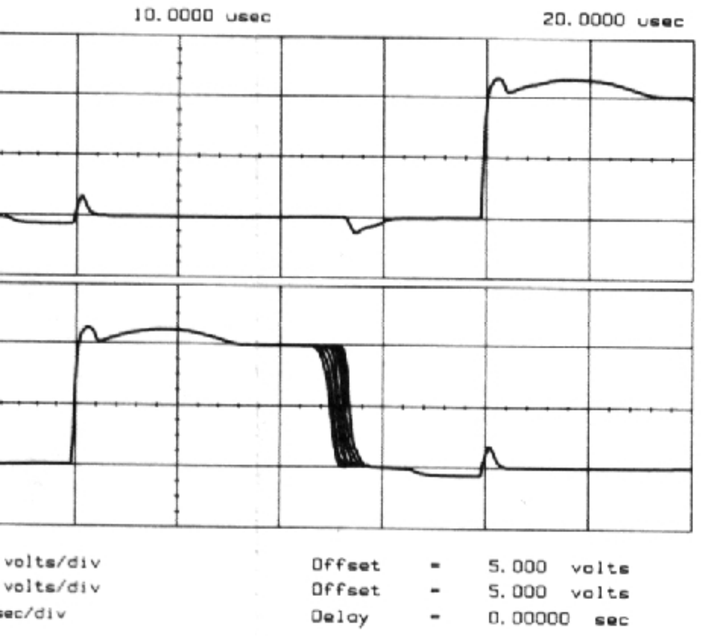
TEST POINT : TP12 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]

7
8



Ch. 1	=	2.000 volts/div		Offset	=	2.000 volts
Ch. 2	=	1.000 volts/div		Offset	=	2.000 volts
Timebase	=	2.00 usec/div		Delay	=	0.00000 sec

(AC1 or AC1/1)
TEST POINT : TP24 for Ch. 2.



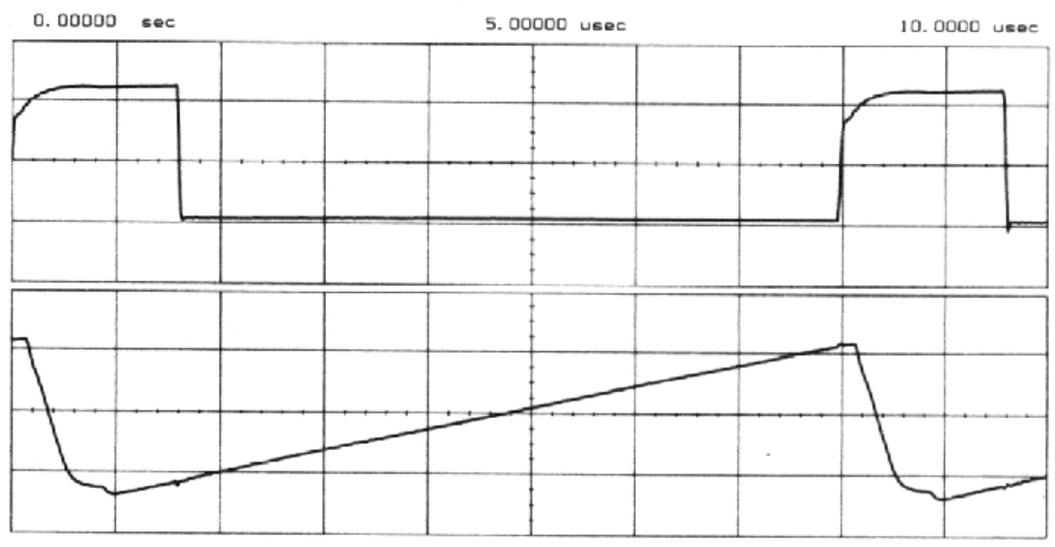
volts/div	Offset	=	5.000 volts
volts/div	Offset	=	5.000 volts
sec/div	Delay	=	0.00000 sec

9 BOARD : AC1/1

10

TEST POINT : TP12 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]

9
10



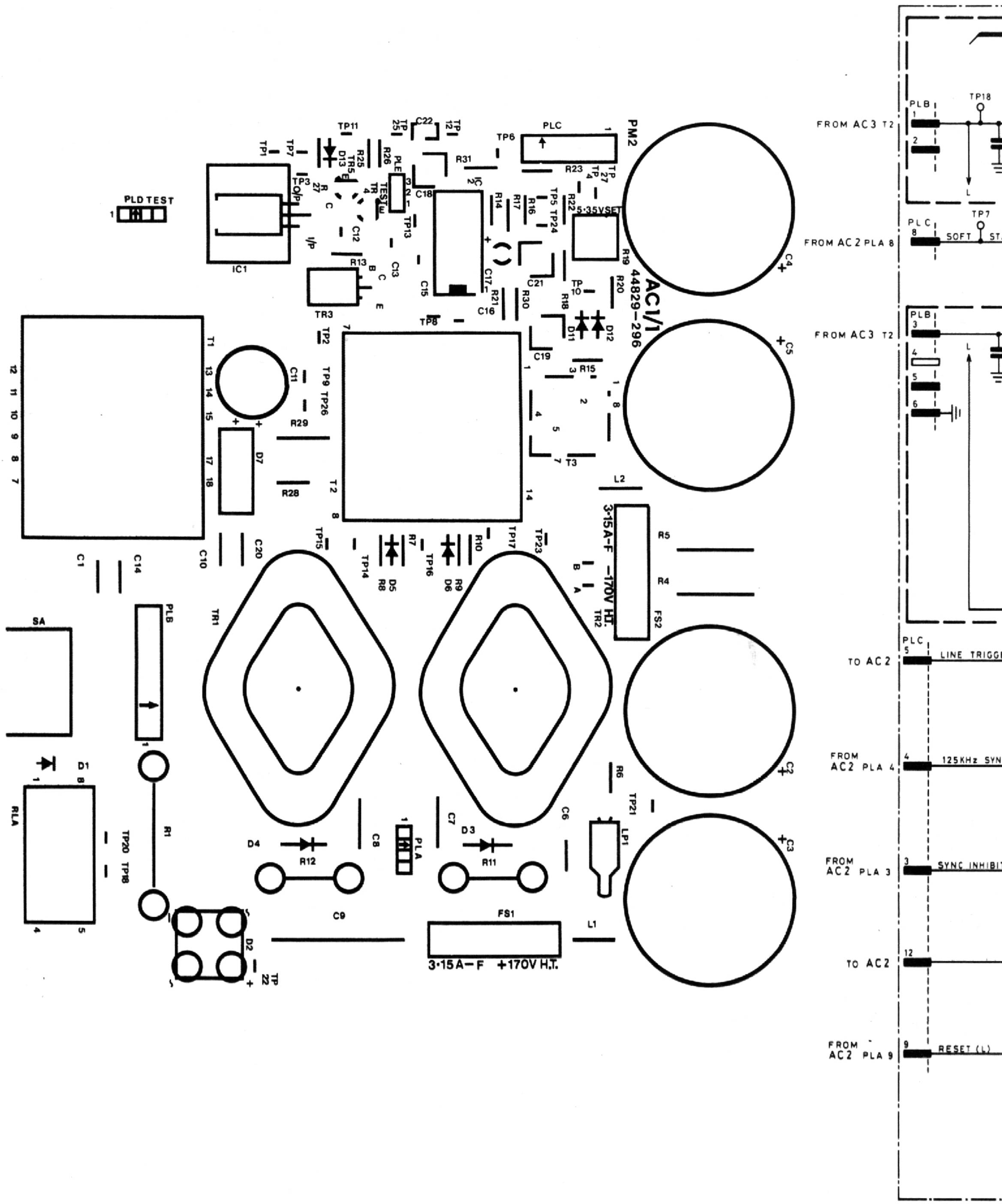
Ch. 1	=	2.000 volts/div		Offset	=	2.000 volts
Ch. 2	=	1.000 volts/div		Offset	=	2.000 volts
Timebase	=	1.00 usec/div		Delay	=	0.00000 sec

(AC1 or AC1/1)
TEST POINT : TP25 for Ch. 2 (IC2 pin 10 on AC1).

or AC1/1

Fig. 25A

May 86



Component layout for AC1/1

Fig. 25
May 86

SOFT START CIRCUIT

RECTIFIER AND RESERVOIRS

PHASE SPLITTER OUTPUT

AUXILIARY POWER SUPPLY

SYNC PULSE SHAPING AND GATE

FROM AC3 T2

PLB

TP18

R1 100R

TP20

C1 2n2

C14 2n2

RLA STC-5V

L

PLC

TP7

FROM AC2 PLA 8

SOFT START

+5V

D1 1N4004

C4 +

D2 KBPG608

TP22

+170V

D3 1·5KE220A

C3 470µ

C2 470µ

R4 56k

T2

L1

PLB

FROM AC3 T2

S1 (a)

230V

115V

TP21

C10 2n2

C20 2n2

C6 220n

LP1 50V

C5 +

D4 1·5KE220A

C4 470µ

C5 470µ

R5 56k

R6 10M

TP23

-170V

L2

DANGER!

AREA WITHIN DASHED LINES IS AT SUPPLY VOLTAGE

T1

S1 (b)

R28 1k0

TP2

IC1 7812

+22V

+12V

D7 2KBB20R

C11 1m0

C12 1µ0

C16 220n

TP1

R29 1k0

TP26

PLC

TO AC2

LINE TRIGGER

PLD TEST

PLE TEST

TP8

TP9

IC2 SG3526 SMPS CONTROLLER

C17 4µ7

R31 1k0

TP12

C22 150p

FROM AC2 PLA 4

125KHz SYNC

R27 1k0

D13 1N4148

R26 220R

TR4 BC209

TP13

TP25

C18 1n2

R14 10k

TP11

R25 10k

TR5 BC209

FROM AC2 PLA 3

SYNC INHIBIT

R22 10k

TP5

TO AC2

SYNC

CT

RT

OSC.

SOFT START

OUTPUT

V REF

SHUT-DOWN

TP6

FROM AC2 PLA 9

RESET (L)

RESET

GND

R23 2k2

R30 10k

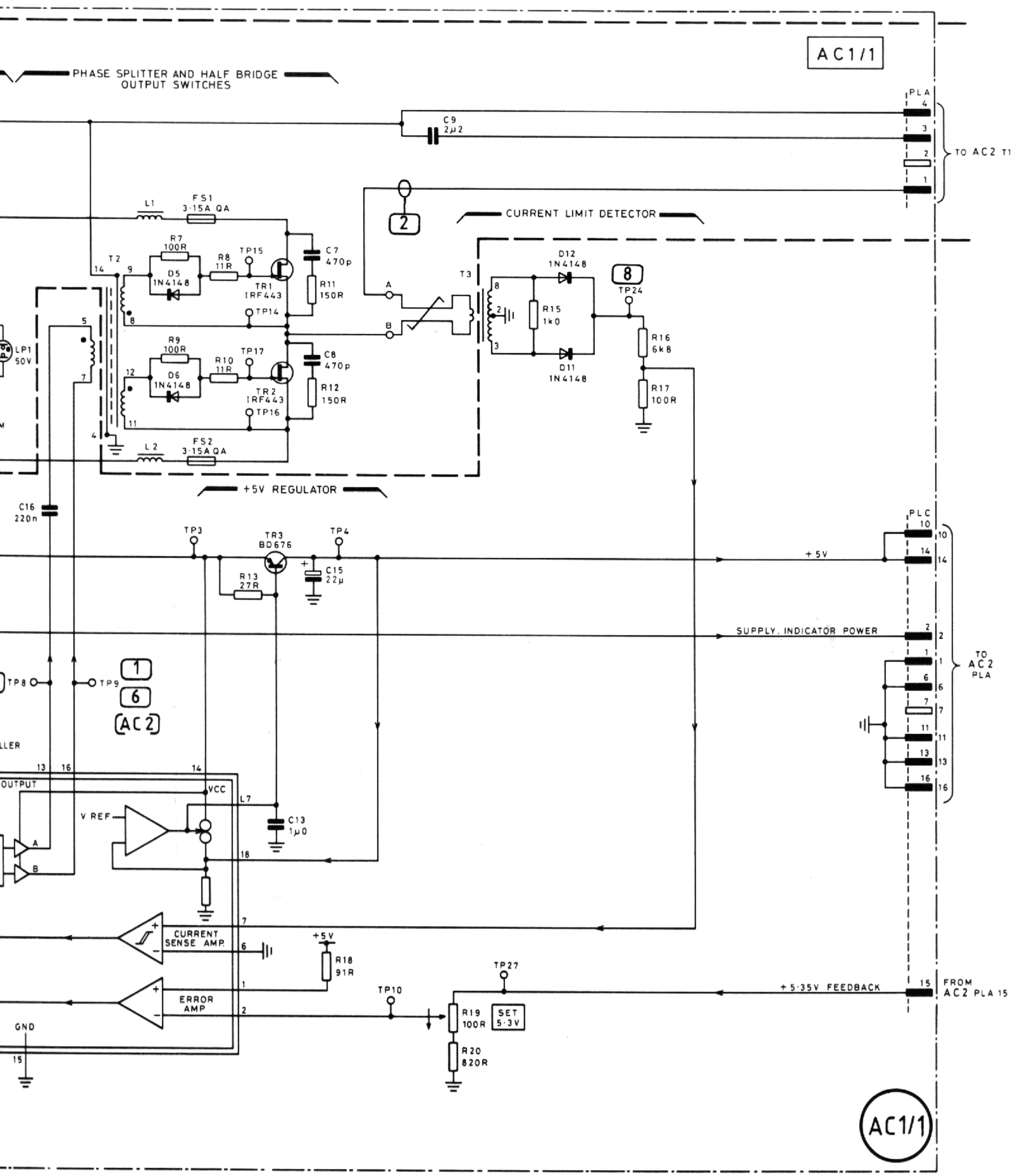
C19 4n7

R21 100k

C21 4n7

Drg.No. Z44828-514H
Sh.1 Iss.2

AC1/1 : Input & cont



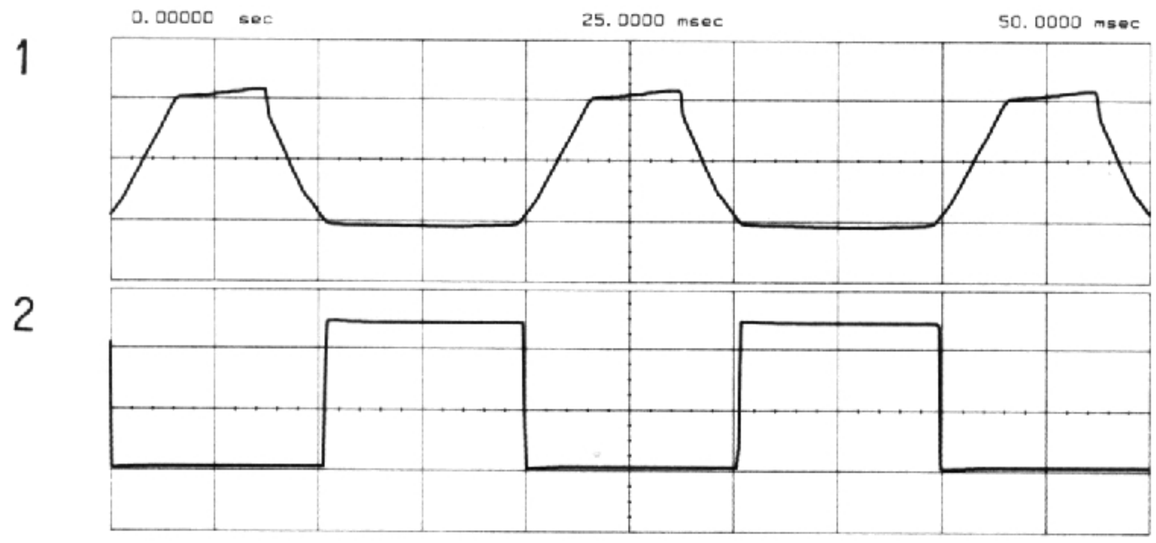
/1 : Input & control of SMPS

1

2

BOARD : AC2/1
FUNCTION : 50 Hz LINE INPUT FREQUENCY.

TEST POINT : TP4 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AC2 or AC2/1)

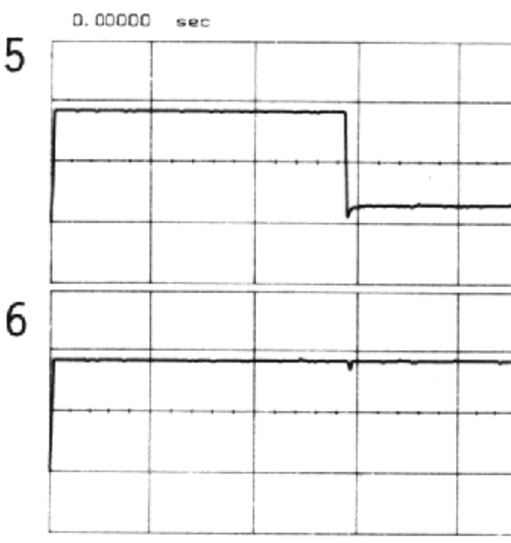
TEST POINT : TP5 for Ch. 2

5

6

BOARD : AC2/1

TEST POINT : TP6 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]
TRIGGER : D18 anode +ve edge, 1 V



(AC2 or AC2/1)

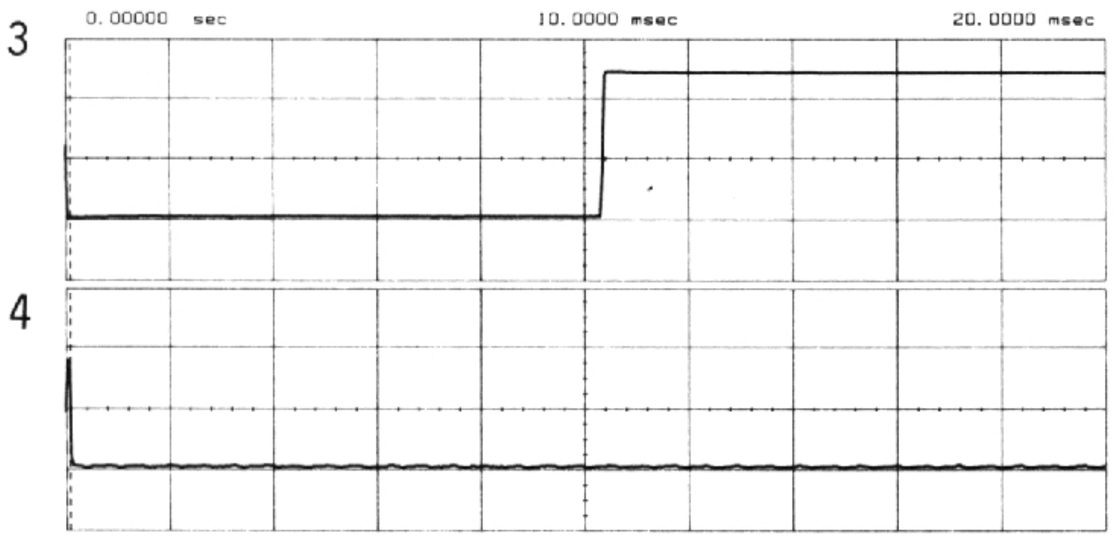
TEST POINT : TP7 for Ch. 2

3

4

BOARD : AC2/1

TEST POINT : TP5 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AC2 or AC2/1)

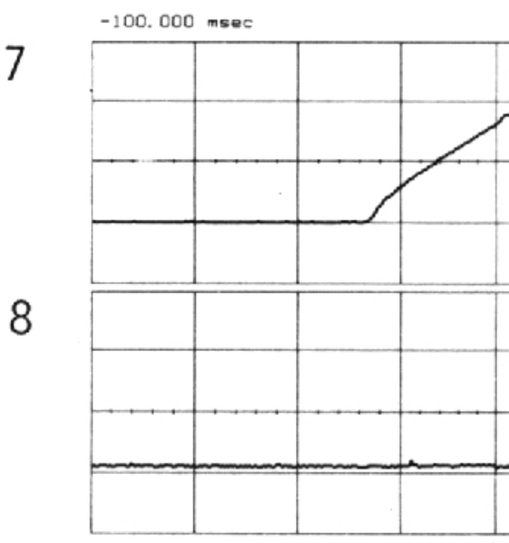
TEST POINT : TP15 for Ch. 2

7

8

BOARD : AC2/1
FUNCTION : POWER UP CONDITION.

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AC2 or AC2/1)

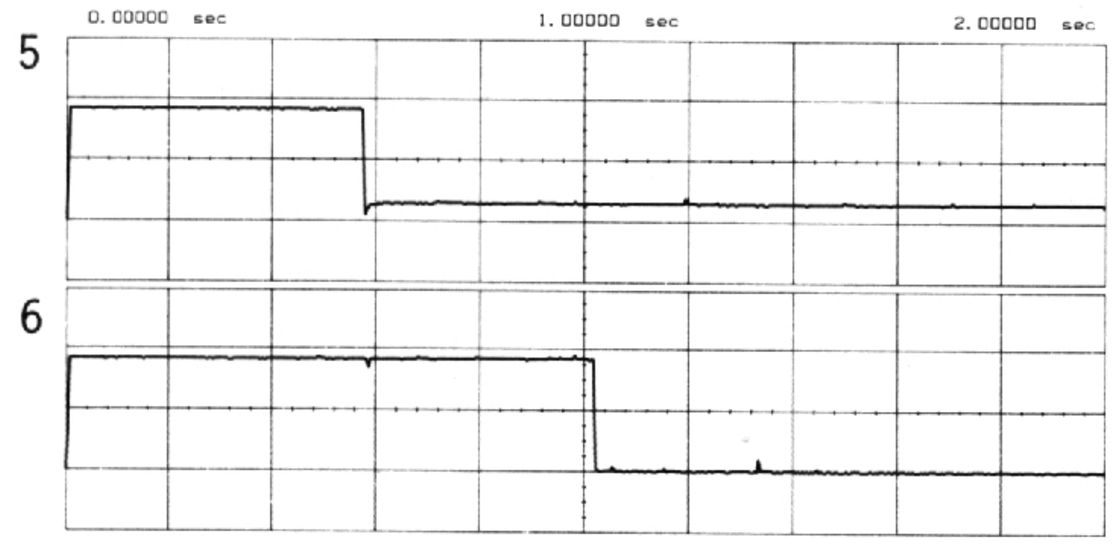
TEST POINT : TP10 for Ch. 2

Fig. 26A
Chap. 7
Page 80

5 BOARD : AC2/1

6

TEST POINT : TP6 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]
TRIGGER : D18 anode +ve edge, 1 V



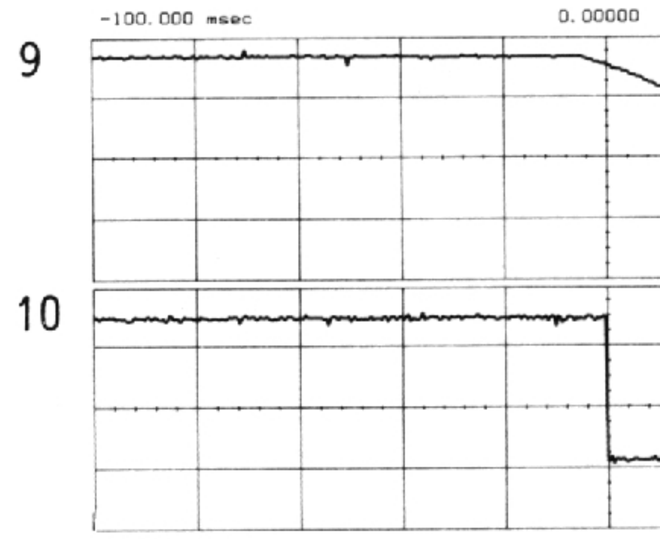
(AC2 or AC2/1)

TEST POINT : TP7 for Ch. 2

9 BOARD : AC2/1

10 FUNCTION : POWER DOWN CONDITION.

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



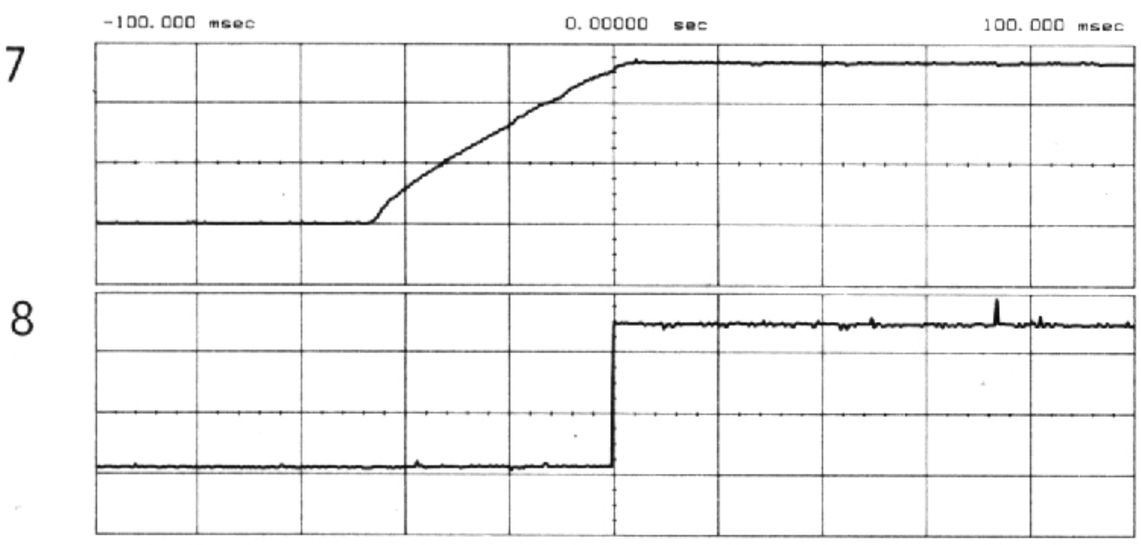
(AC2 or AC2/1)

TEST POINT : TP10 for Ch. 2

7 BOARD : AC2/1

8 FUNCTION : POWER UP CONDITION.

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



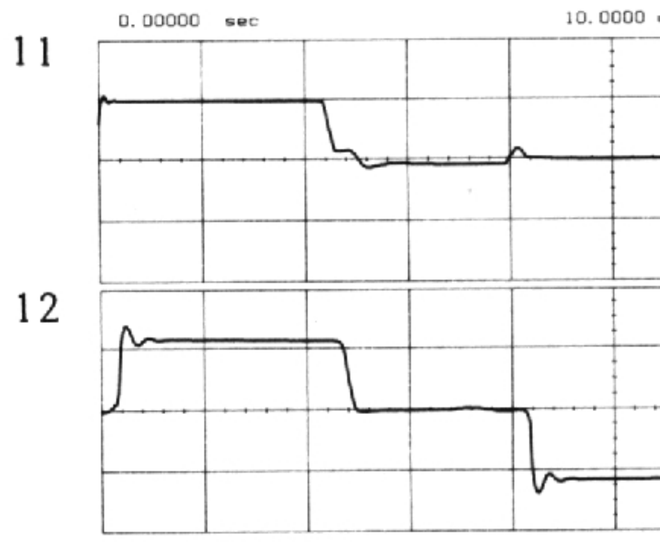
(AC2 or AC2/1)

TEST POINT : TP10 for Ch. 2

11 BOARD : AC2/1

12

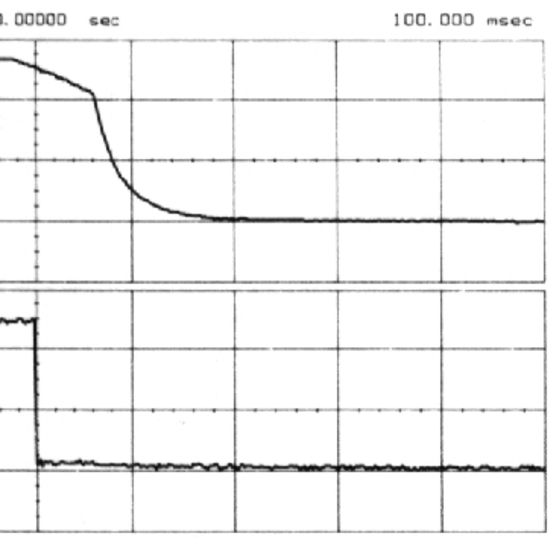
TEST POINT : AC1 TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AC2 or AC2/1)

TEST POINT : *A($D1_b$ anode) for Ch. 2

Waveforms for AC2/1

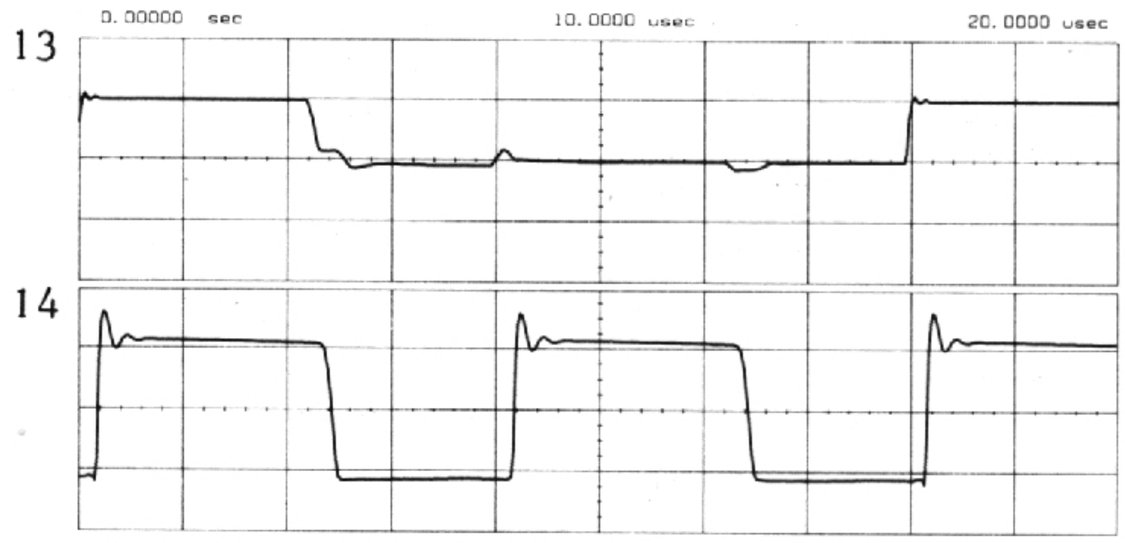


Offset = 2.000 volts
Offset = 2.000 volts
Delay = 0.00000 sec

13 BOARD : AC2/1

14

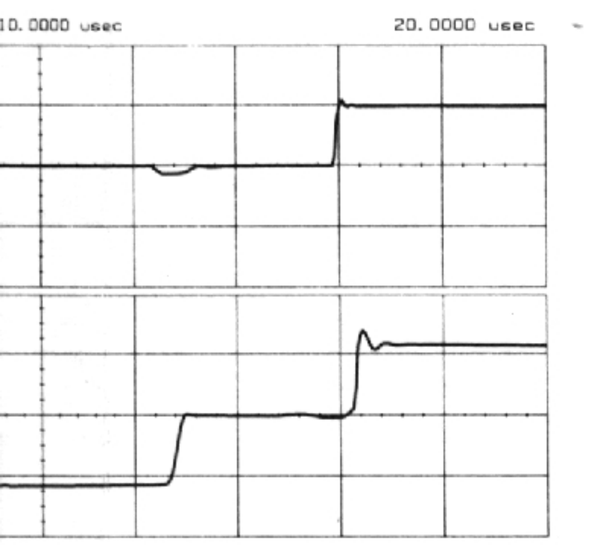
TEST POINT : AC1 TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



Ch. 1 = 10.00 volts/div
Ch. 2 = 5.000 volts/div
Timebase = 2.00 usec/div

Offset = 0.000 volts
Offset = 5.000 volts
Delay = 0.00000 sec

(AC2 or AC2/1)
TEST POINT : $D1_{A \text{ or } B}$ cathode for Ch. 2

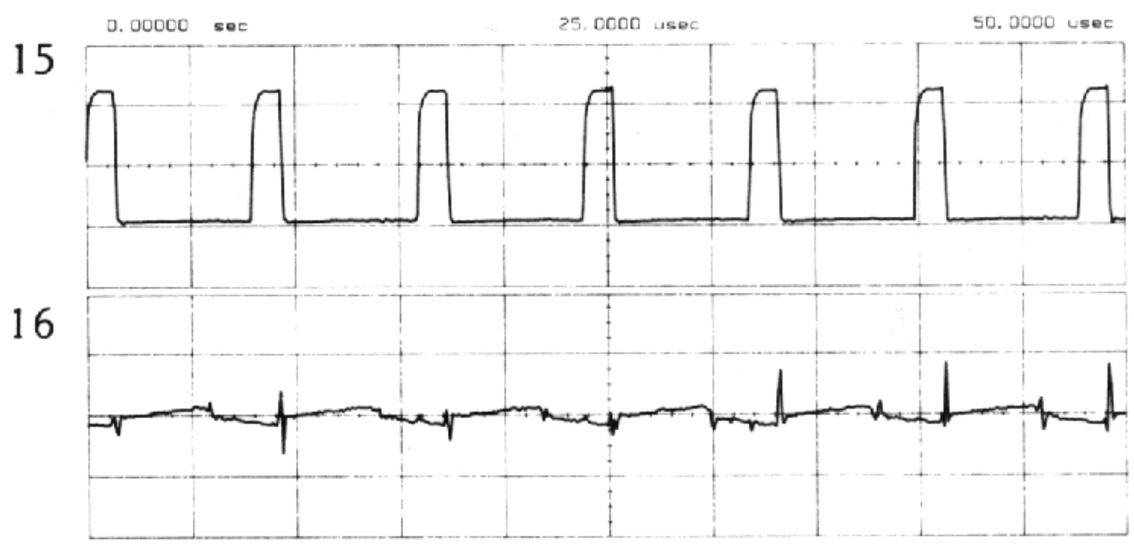


Offset = 0.000 volts
Offset = 0.000 volts
Delay = 0.00000 sec

15 BOARD : AC2/1

16

TEST POINT : *B or AC1 TP12 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



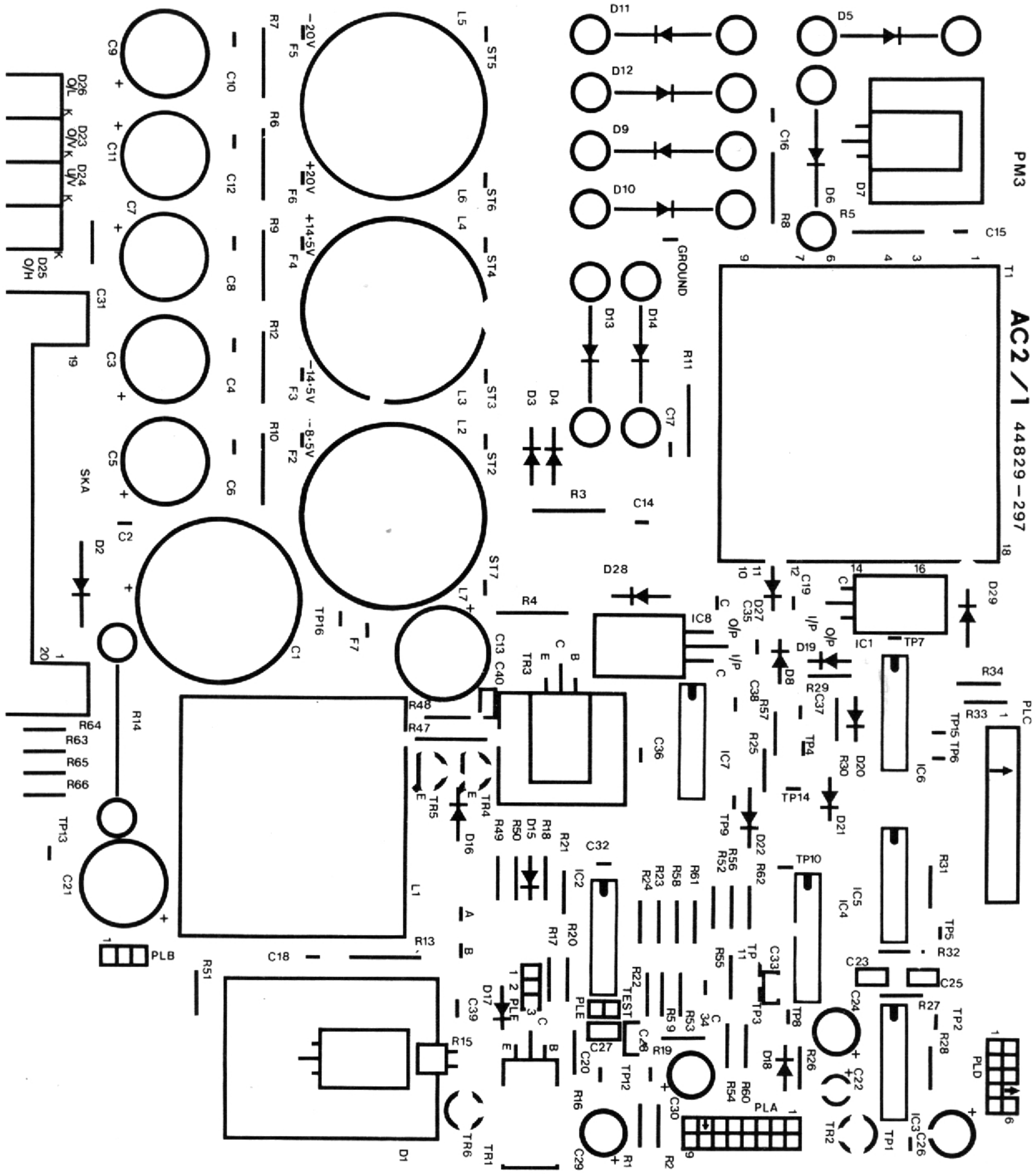
Ch. 1 = 2.000 volts/div
Ch. 2 = 200.0 mvolts/div
Timebase = 5.00 usec/div

Offset = 2.000 volts
Offset = 5.350 volts
Delay = 0.00000 sec

(AC2 or AC2/1)
TEST POINT : TP9 for Ch. 2

Fig. 26A

May 86



Component layout for AC2/1

Fig. 26
May 86

PM3

AC2/1 44829-297

DANGER!
AREA WITHIN DASHED LINES IS AT SUPPLY VOLTAGE

FROM AC1 PLA — OR — OR — RD/GN

T1 — D3 BA159 — D4 BA159 — L7 1·5m — R3 100R — C14 220p — ST7 — F7 — C13 33µ

D5, D6 = BYV28-100
D7 = BYV32-100
D9-D14 = BYV28-100
D1 = 20CTQ45

TR3 TIP112 — R4 10k — R47 5R6 — R48 10R — TR5 BC209 — TR4 BC449 — C40 1n0 — D16 BZX79C24 — R49 22k — C31 100n — R50 10k

L6 350µ — ST6 — F6 — R5 220R — C15 220p — D7(a) — D7(b) — D5 — C11 1m0 — C12 100n — R6 1k8

L5 350µ — ST5 — F5 — C9 1m0 — C10 100n — R7 1k8

IC8 7912 — C35 100n — D28 1N5401 — D8 1N4004

L4 350µ — ST4 — F4 — R8 100R — C16 220p — D9 — D10 — D11 — D12 — C7 1m0 — C8 100n — R9 1k2

L3 350µ — ST3 — F3 — C5 1m0 — C6 100n — R10 1k2

IC1 7905 — C19 100n — D29 1N5401 — D27 1N4004 — R51 4k7

L2 350µ — ST2 — F2 — R11 10R — C17 220p — D13 — D14 — C3 1m0 — C4 100n — R12 820R

L2 36µ — R13 10R — C18 10n — D1(a) — D1(b) — C1 10m0 — C2 100n — R14 47R — D2 ICT5 — R15 300k — R16 120k

TO R52, R58 — 7 9 16

FAN CONTROL — TEMP STATUS COMPARATORS

TR6 BC209 — D15 1N4148 — C39 100n

PLF — TR1 TIP112 — D17 1N4004 — C21 1m0 — C20 100n — R17 4k7 — R18 1k0

R19 680R — R20 100k — R21 1k0 — IC2(a) LM339 — C34 100n

R24 100k — R22 270R — IC2(c) LM339 — R25 1k0 — R23 1k5

FROM AC1 PLC 10 — FROM AC1 PLC 14 — C29 10µ — R1 100R 0·5% — C32 100n — R2 100R 0·5% — C30 10µ — TP2 — TP3 — GROUND

TO AA1 — PLD 8 10 9 — +20V — −12V — −5V

TO AA1 — PLC 6 5 4 3 2 1 — +14·5V — +5·3V — TP16 +80V

SKA

5V LINE

+20V — 13 31
−20V — 15 33
+14·5V — 9 27
−14·5V — 11 29
RF UNIT CONNECTED (−14·5V) — 28
−8·5V — 17 35
+5·3V — 2 3 4 20 21 22

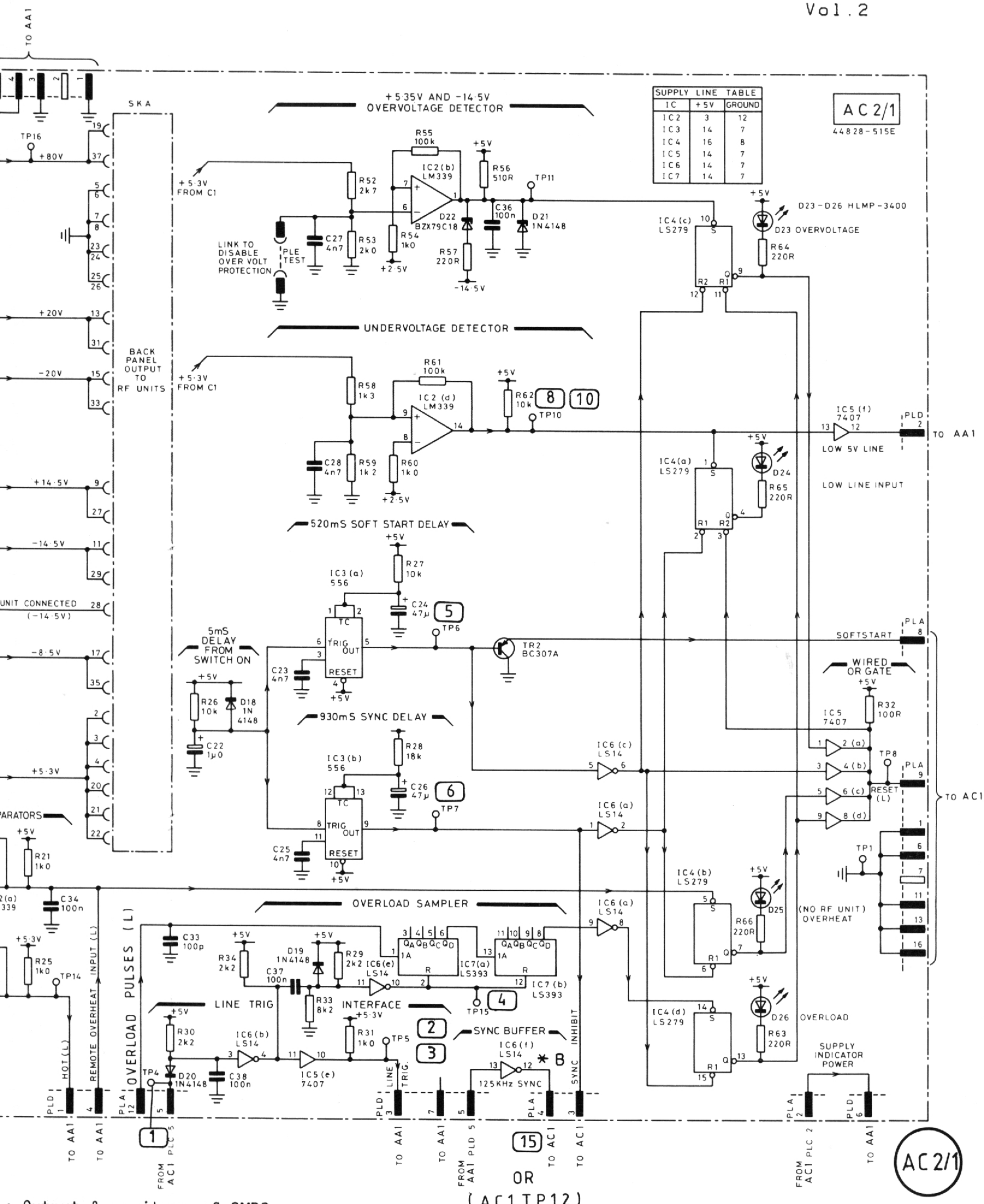
BACK PANEL OUTPUT TO RF UNIT

HOT(L) — REMOTE OVERHEAT INPUT (L) — OVERLOAD PULSES (L) — TP4

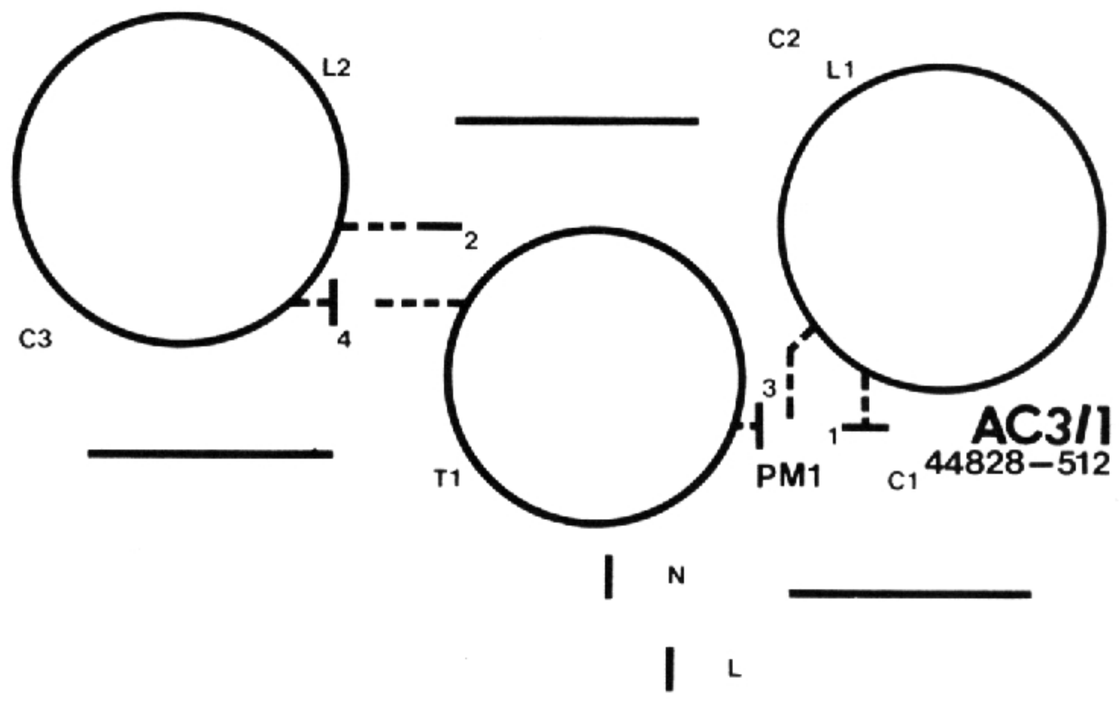
PLB 1 2 3 — TO FAN
PLA 15 +5·3V FEEDBACK — TO AC1
PLD 1 — TO AA1
PLD 4 — TO AA1
PLA 12 — 1

Drg.No. Z44828-515E
Sh.1 Iss.2

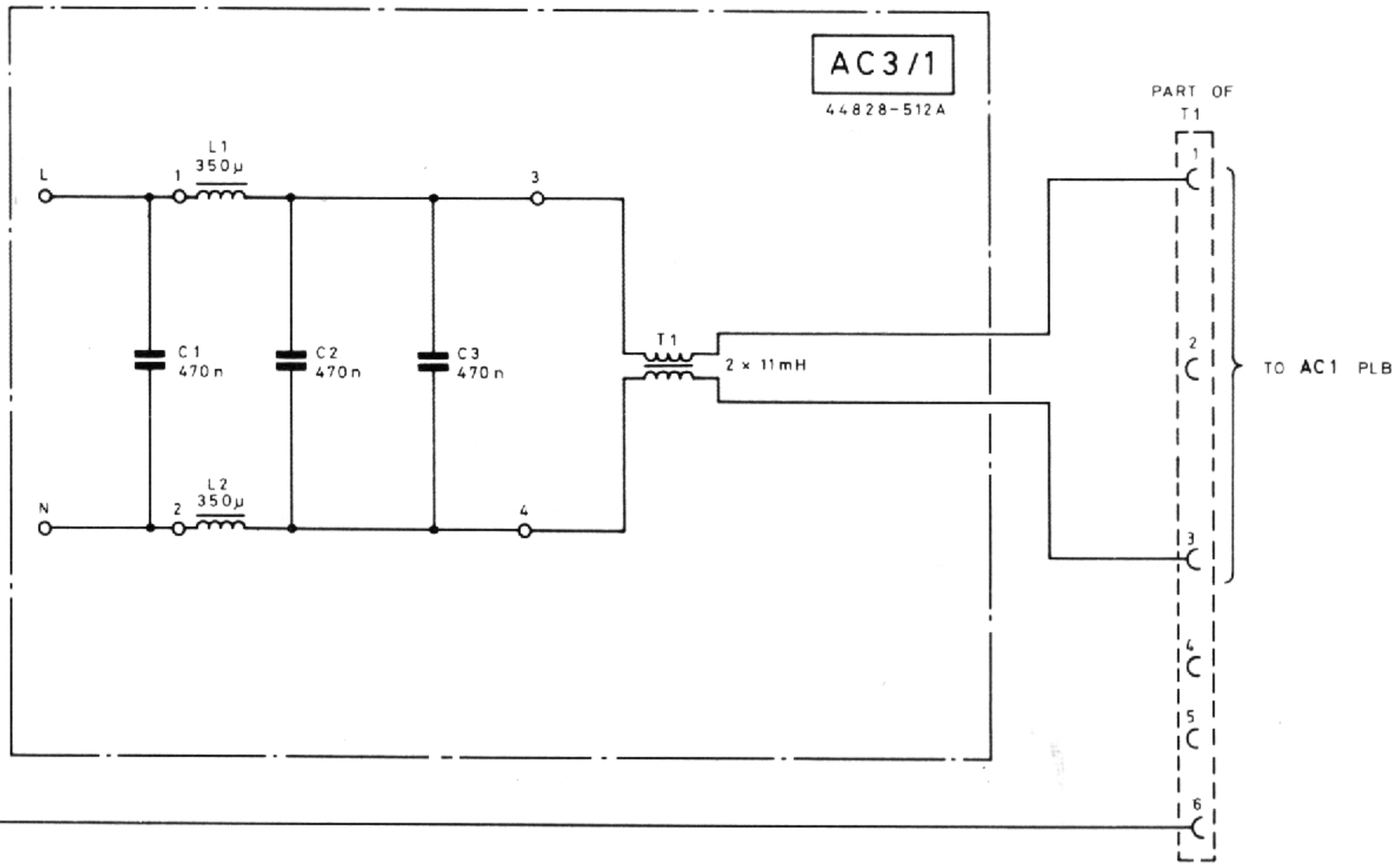
AC2/1 : Output & monit



: Output & monitors of SMPS



Component layout for AC3/1



Drg.No. Z44828-517Y
Sh.1 Iss.1

AC3/1

AC3/1 : Supply filter

BOARD : AD1/1
KEY OF FUNCTIONS :

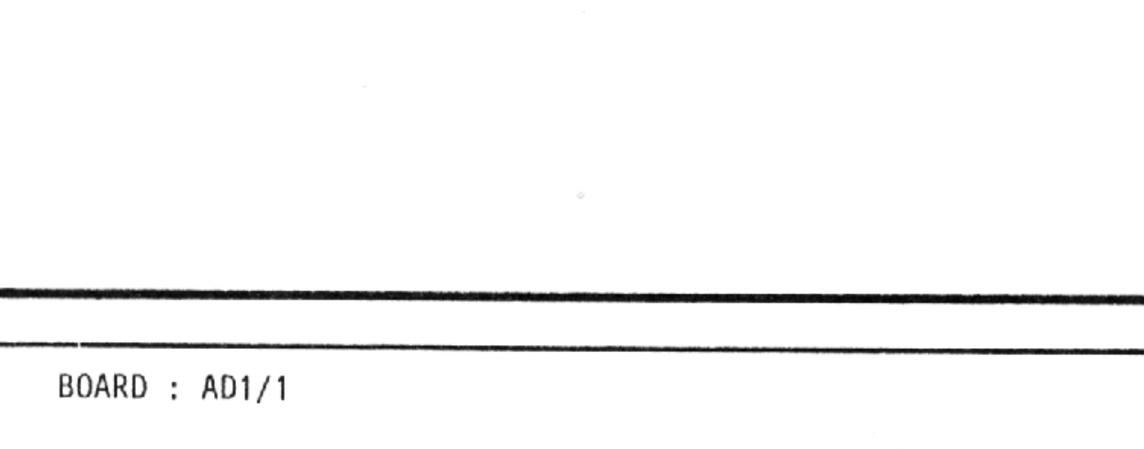
1
2
3
4 I HORIZ.

---

1 BOARD : AD1/1

2

TEST POINT : TP17 for Ch. 1 (TP10 on AD1)
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]
TRIGGER : TP9 +ve edge



(AD1 or AD1/1)

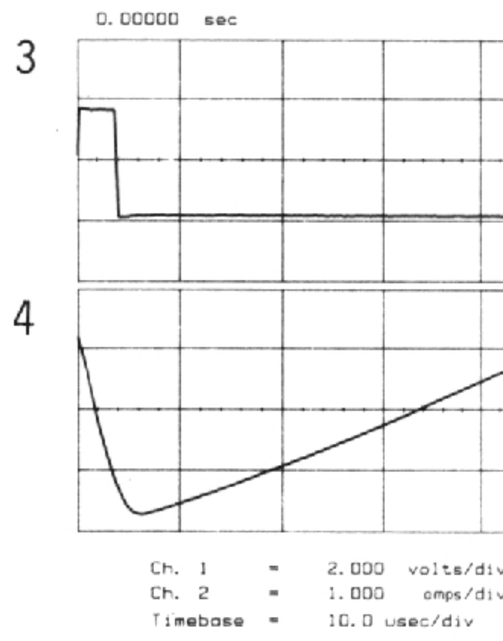
TEST POINT : TP18 for Ch. 2 (TP11 on AD1) offset AD1/1 = 60.00 V (AD1 = 40.00 V)

---

3 BOARD : AD1/1

4

TEST POINT : TP11 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AD1/1)

FUNCTION : I HORIZ
TEST POINT : *A for Ch. 2

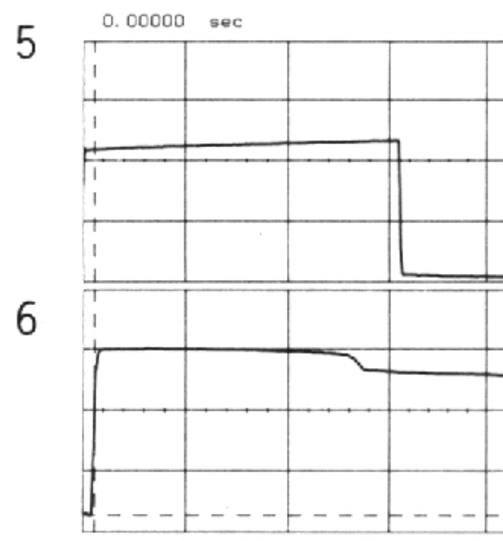
Ch. 2 Use a current probe and re
screen legend.

---

5 BOARD : AD1/1

6

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AD1/1)

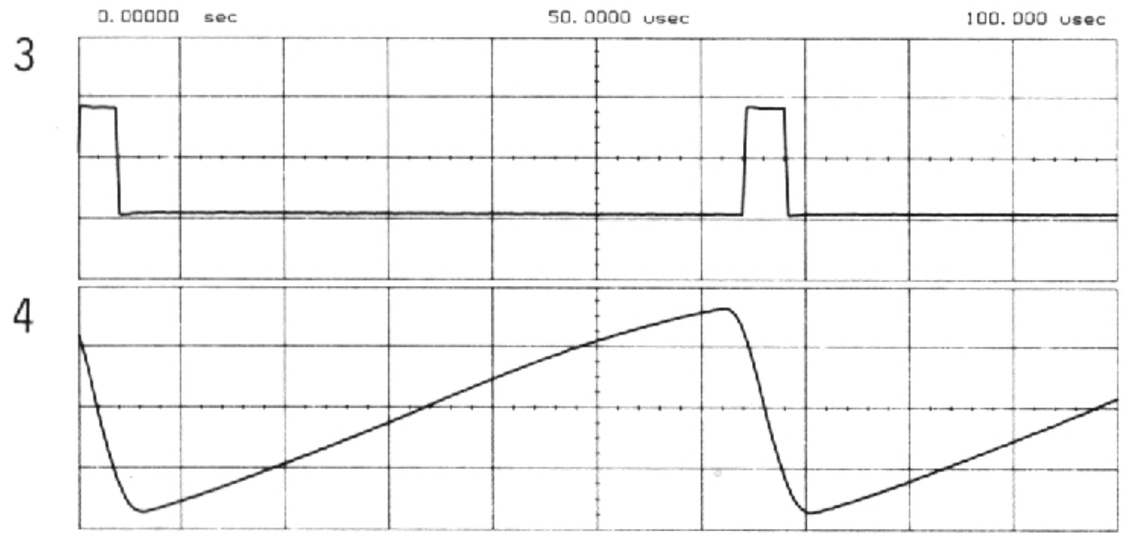
TEST POINT : TP10 for Ch. 2

Fig. 28A
Chap. 7
Page 84

3 BOARD : AD1/1

4

TEST POINT : TP11 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AD1/1)

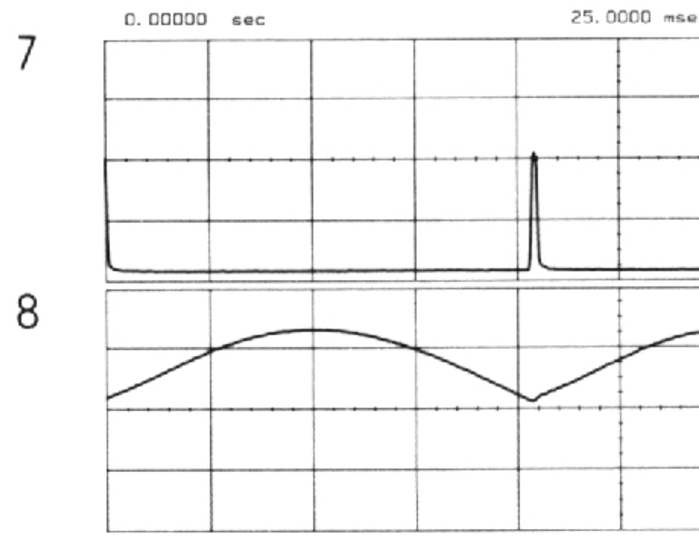
FUNCTION : I HORIZ
TEST POINT : *A for Ch. 2

Ch. 2 Use a current probe and read amps/div in place of volts/div on the screen legend.

7 BOARD : AD1/1

8

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



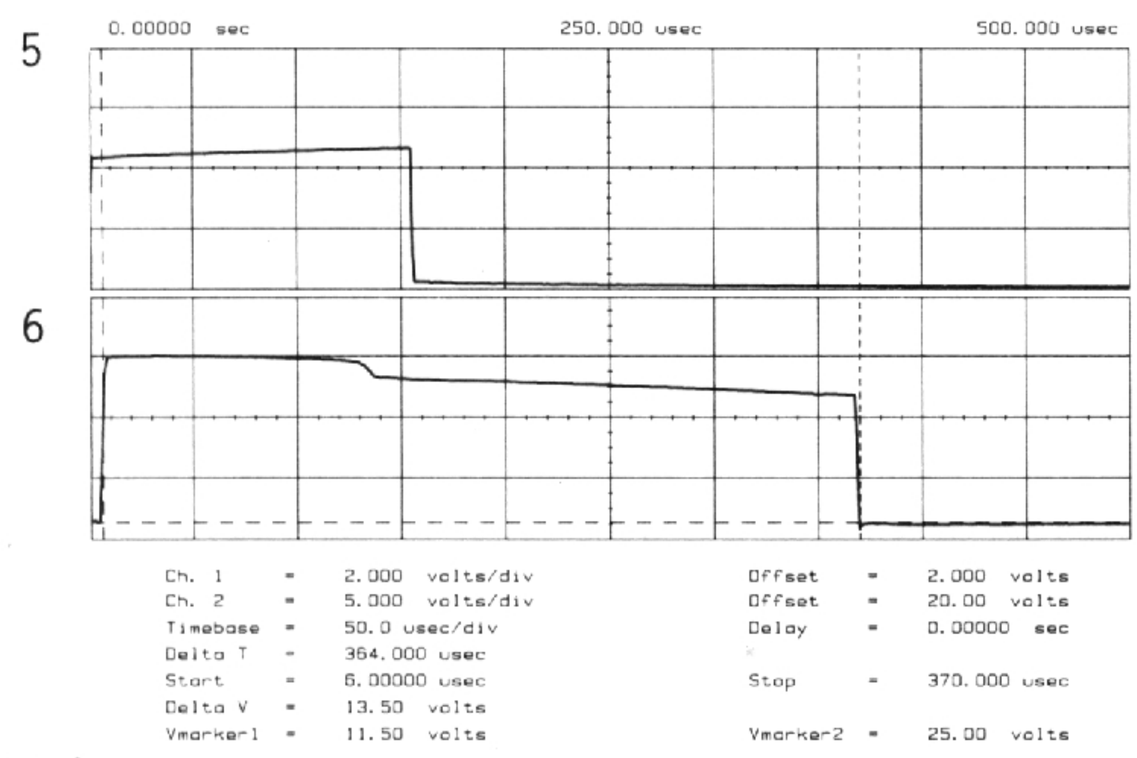
(AD1/1)

TEST POINT : *C (TR6 collector) for Ch. 2.

5 BOARD : AD1/1

6

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



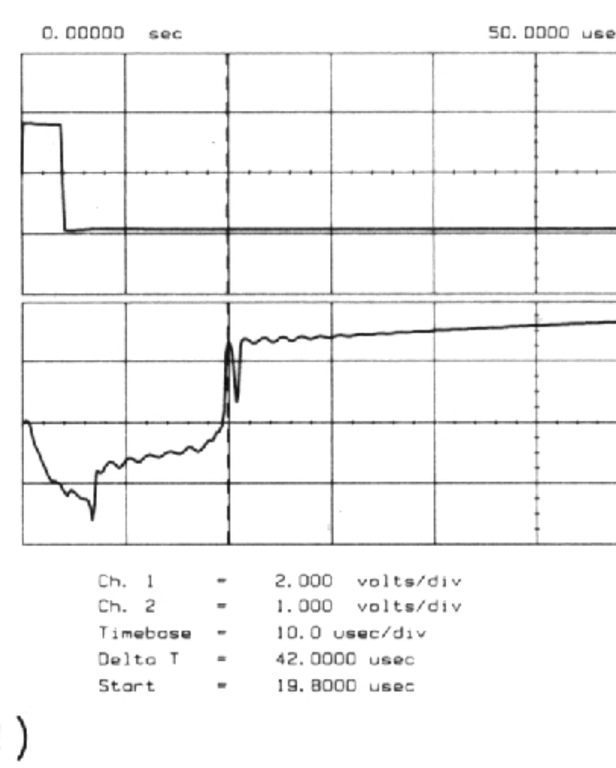
(AD1/1)

TEST POINT : TP10 for Ch. 2

9 BOARD : AD1/1

10

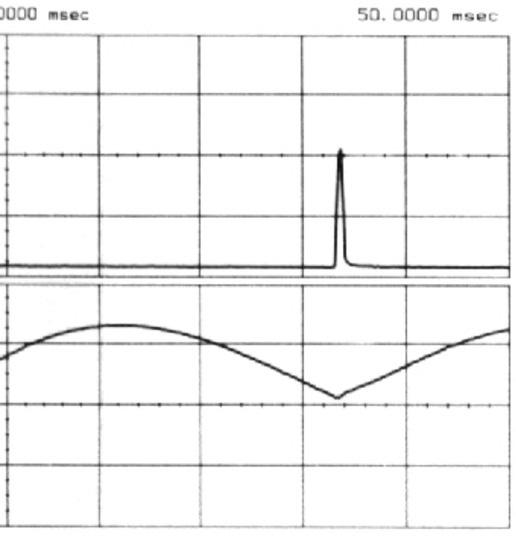
TEST POINT : TP11 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



(AD1/1)

TEST POINT : *B (TR11 base) for Ch. 2

Waveforms for AD1/1



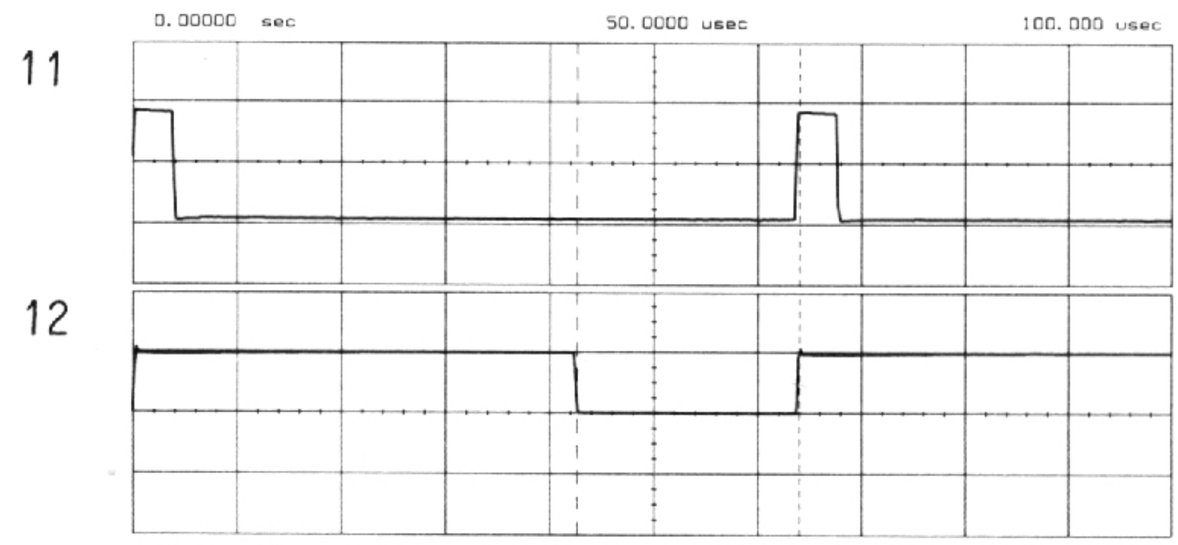
Offset = 2.000 volts
Offset = 5.000 volts
Delay = 0.00000 sec

h. 2.

11 BOARD : AD1/1

12

TEST POINT : TP11 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



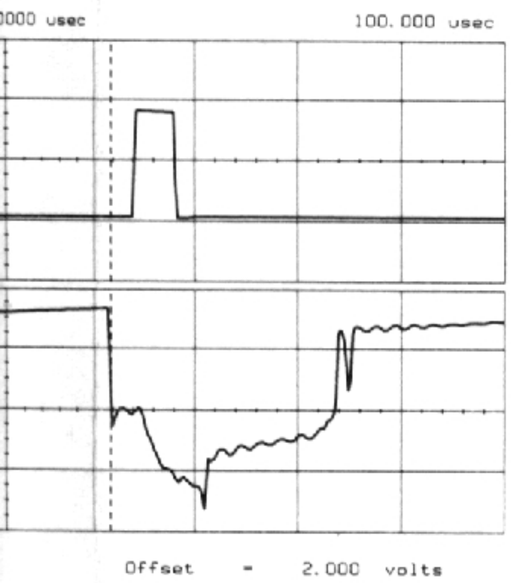
Ch. 1 = 2.000 volts/div
Ch. 2 = 10.00 volts/div
Timebase = 10.0 usec/div
Delta T = 21.4000 usec
Start = 42.6000 usec

Offset = 2.000 volts
Offset = 0.000 volts
Delay = 0.00000 sec

Stop = 64.0000 usec

(AD1/1)

TEST POINT : *D (IC3 pin 3) for Ch. 2



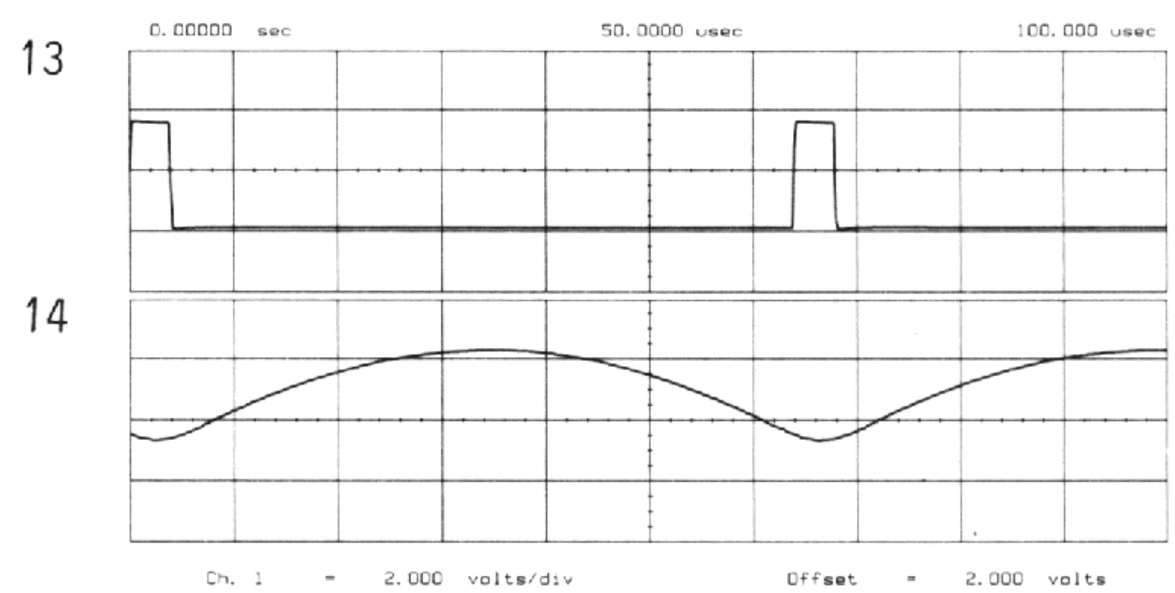
Offset = 2.000 volts
Offset = 0.000 volts
Delay = 0.00000 sec

Stop = 61.8000 usec

13 BOARD : AD1/1

14

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



Ch. 1 = 2.000 volts/div
Ch. 2 = 10.00 volts/div
Timebase = 10.0 usec/div

Offset = 2.000 volts
Offset = 20.00 volts
Delay = 0.00000 sec

(AD1/1)

TEST POINT : TP14 for Ch. 2

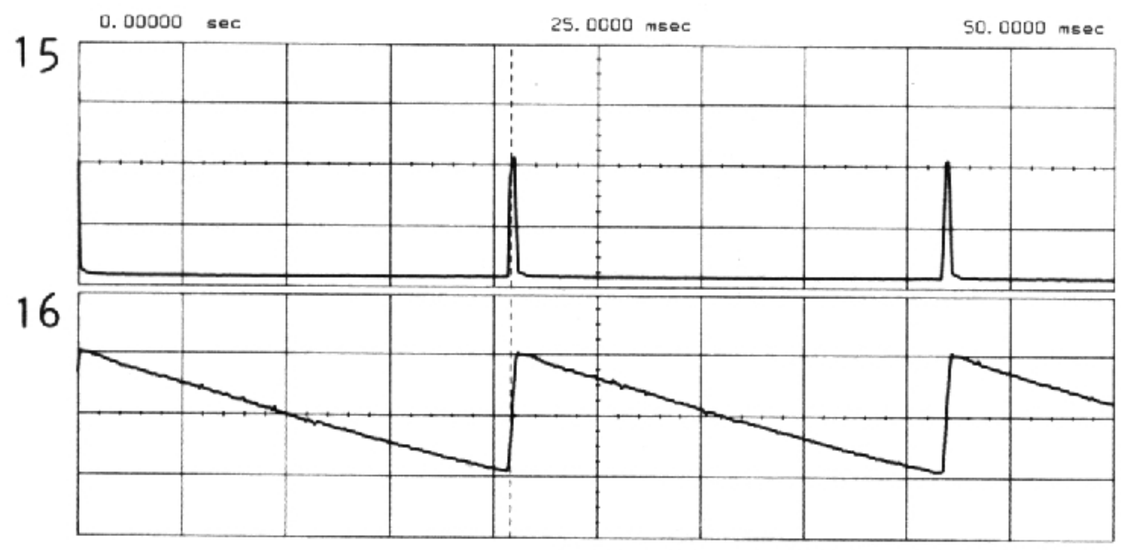
Fig. 28A

May 86

15 BOARD : AD1/1

16

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



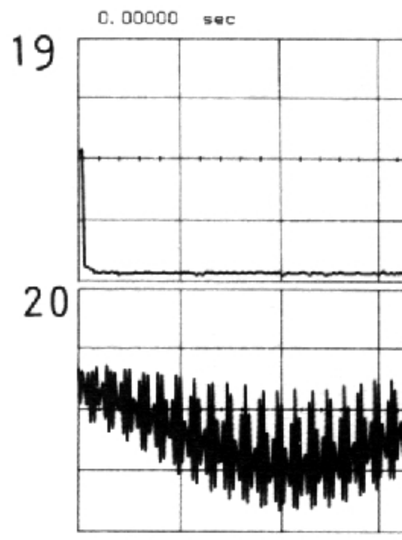
Ch. 1	=	2.000 volts/div	Offset	=	2.000 volts
Ch. 2	=	200.0 mvolts/div	Offset	=	0.000 volts
Timebase	=	5.00 msec/div	Delay	=	0.00000 sec
Delta T	=	20.8000 msec			
Start	=	0.00000 sec	Stop	=	20.8000 msec

TEST POINT : TP13 for Ch. 2

19 BOARD : AD1/1

20

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



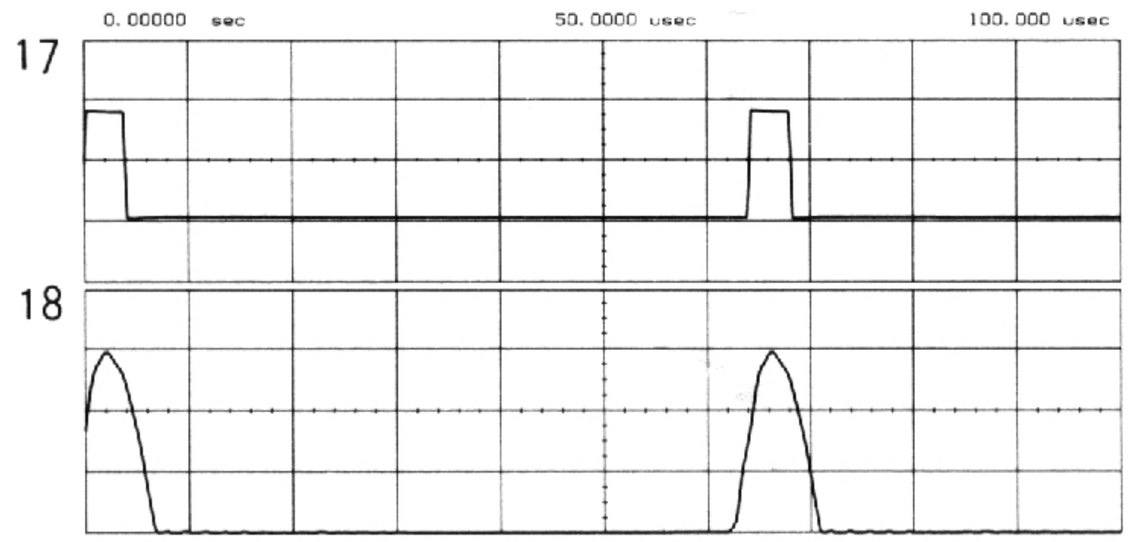
Ch. 1	=	2.000
Ch. 2	=	100.0
Timebase	=	5.00 ms

TEST POINT : TP15 for Ch. 2

17 BOARD : AD1/1

18

TEST POINT : TP11 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



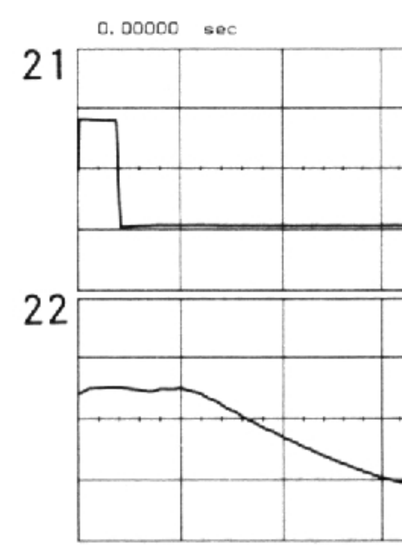
Ch. 1	=	2.000 volts/div	Offset	=	2.000 volts
Ch. 2	=	100.0 volts/div	Offset	=	200.0 volts
Timebase	=	10.0 usec/div	Delay	=	0.00000 sec

TEST POINT : *E (TR11 collector) for Ch. 2

21 BOARD : AD1/1

22

TEST POINT : TP11 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]

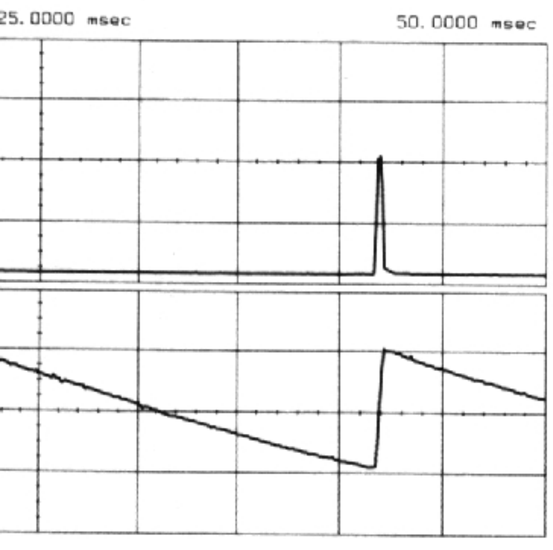


Ch. 1	=	2.000
Ch. 2	=	100.0
Timebase	=	10.0 us

TEST POINT : TP15 for Ch. 2

Waveforms for AD1/1

25.0000 msec 50.0000 msec



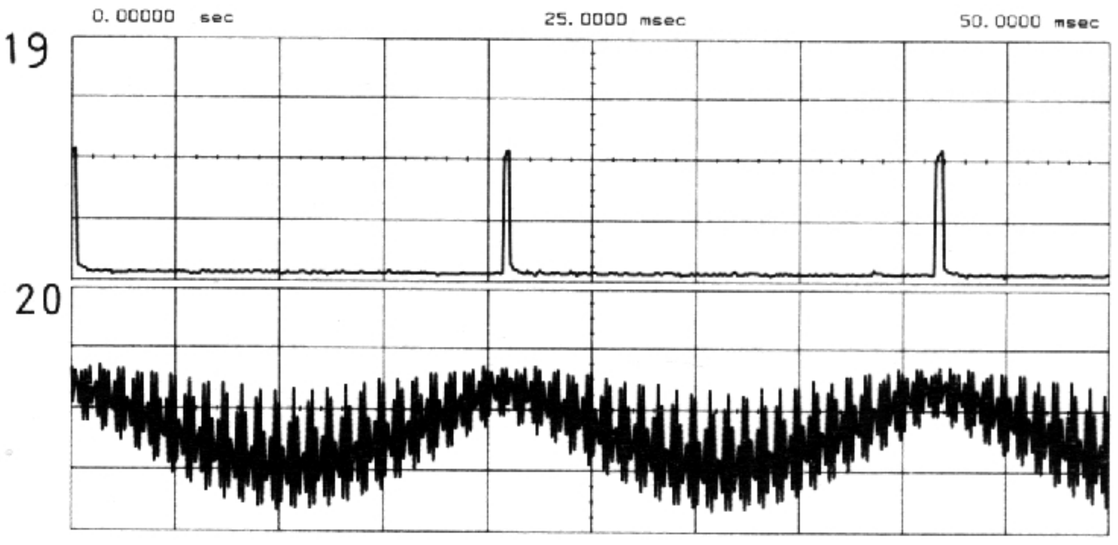
Offset = 2.000 volts
Offset = 0.000 volts
Delay = 0.00000 sec

Stop = 20.8000 msec

19 BOARD : AD1/1

20

TEST POINT : TP9 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]

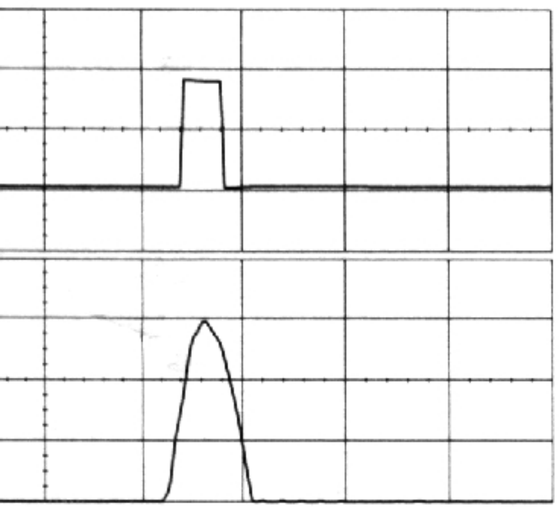


Ch. 1 = 2.000 volts/div
Ch. 2 = 100.0 volts/div
Timebase = 5.00 msec/div

Offset = 2.000 volts
Offset = 200.0 volts
Delay = 0.00000 sec

TEST POINT : TP15 for Ch. 2

50.0000 usec 100.000 usec



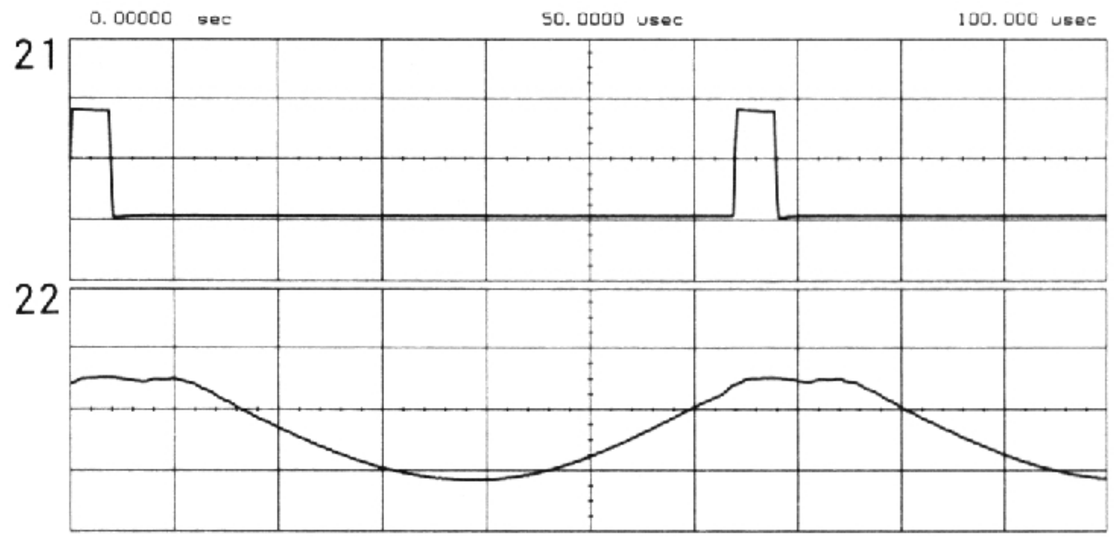
Offset = 2.000 volts
Offset = 200.0 volts
Delay = 0.00000 sec

Ch. 2

21 BOARD : AD1/1

22

TEST POINT : TP11 for Ch. 1
GROUND POINT : TP1
SCOPE SETTING [DEFAULT]



Ch. 1 = 2.000 volts/div
Ch. 2 = 100.0 volts/div
Timebase = 10.0 usec/div

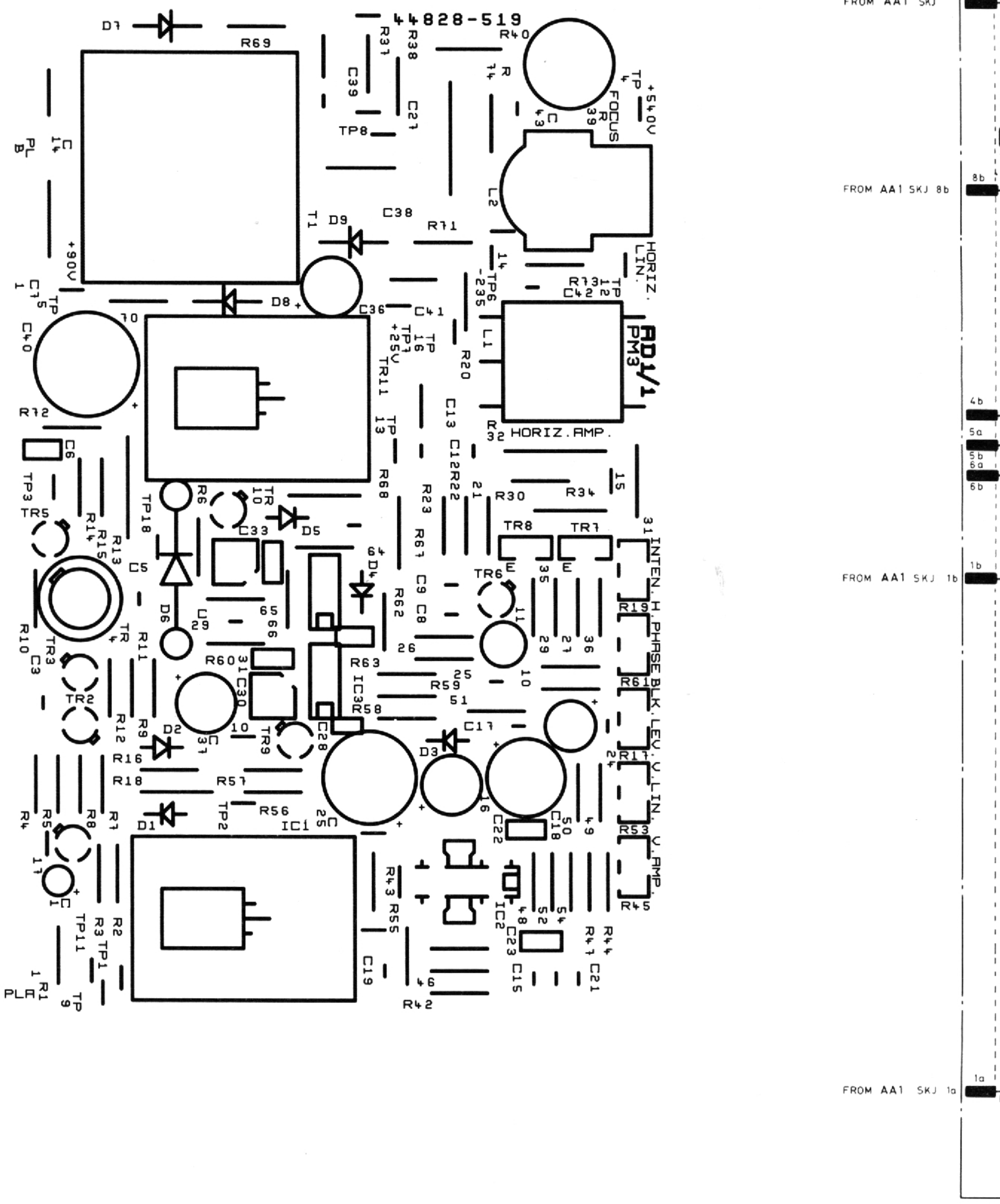
Offset = 2.000 volts
Offset = 200.0 volts
Delay = 0.00000 sec

TEST POINT : TP15 for Ch. 2

Waveforms for AD1/1

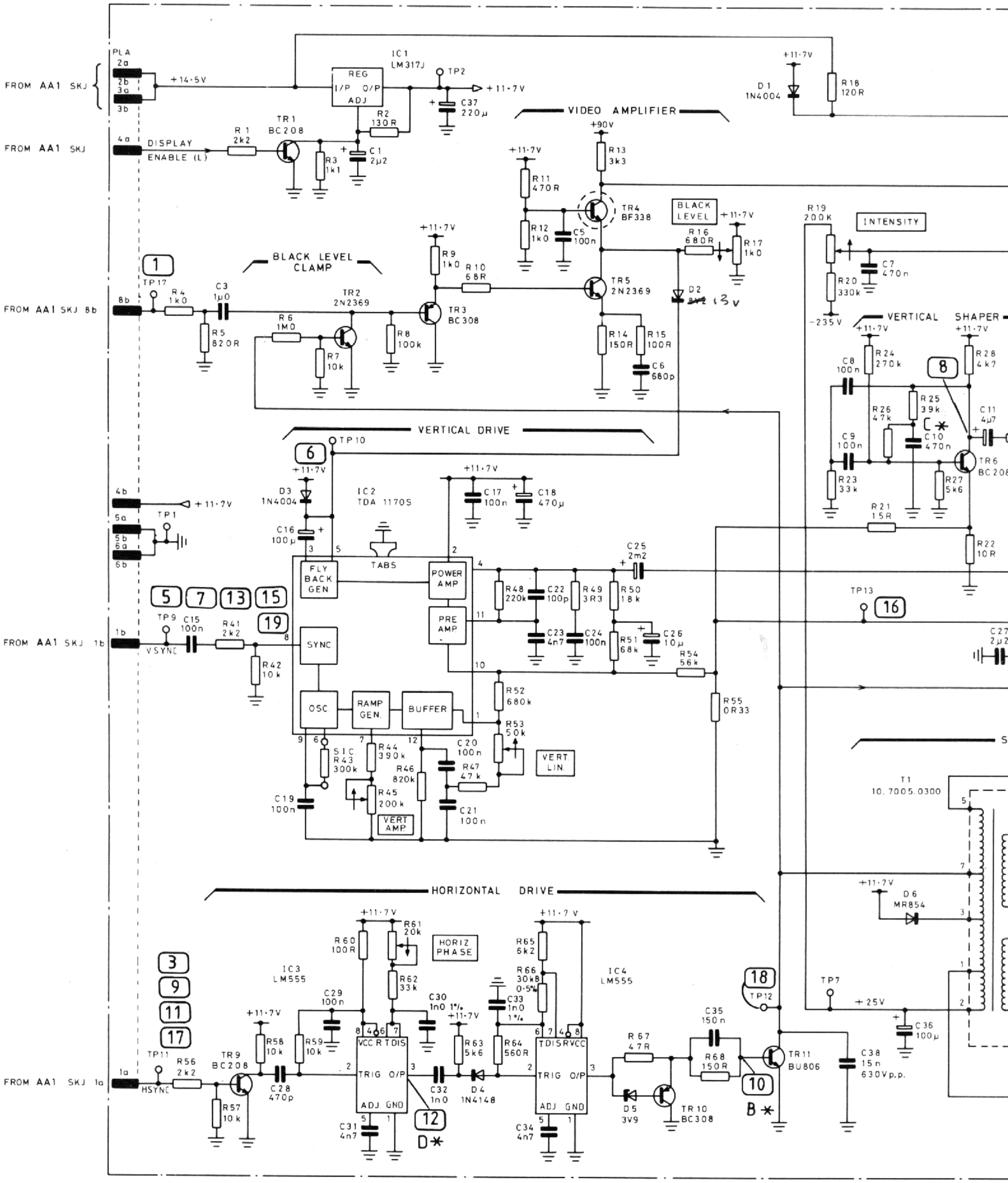
Fig. 28B

May 86



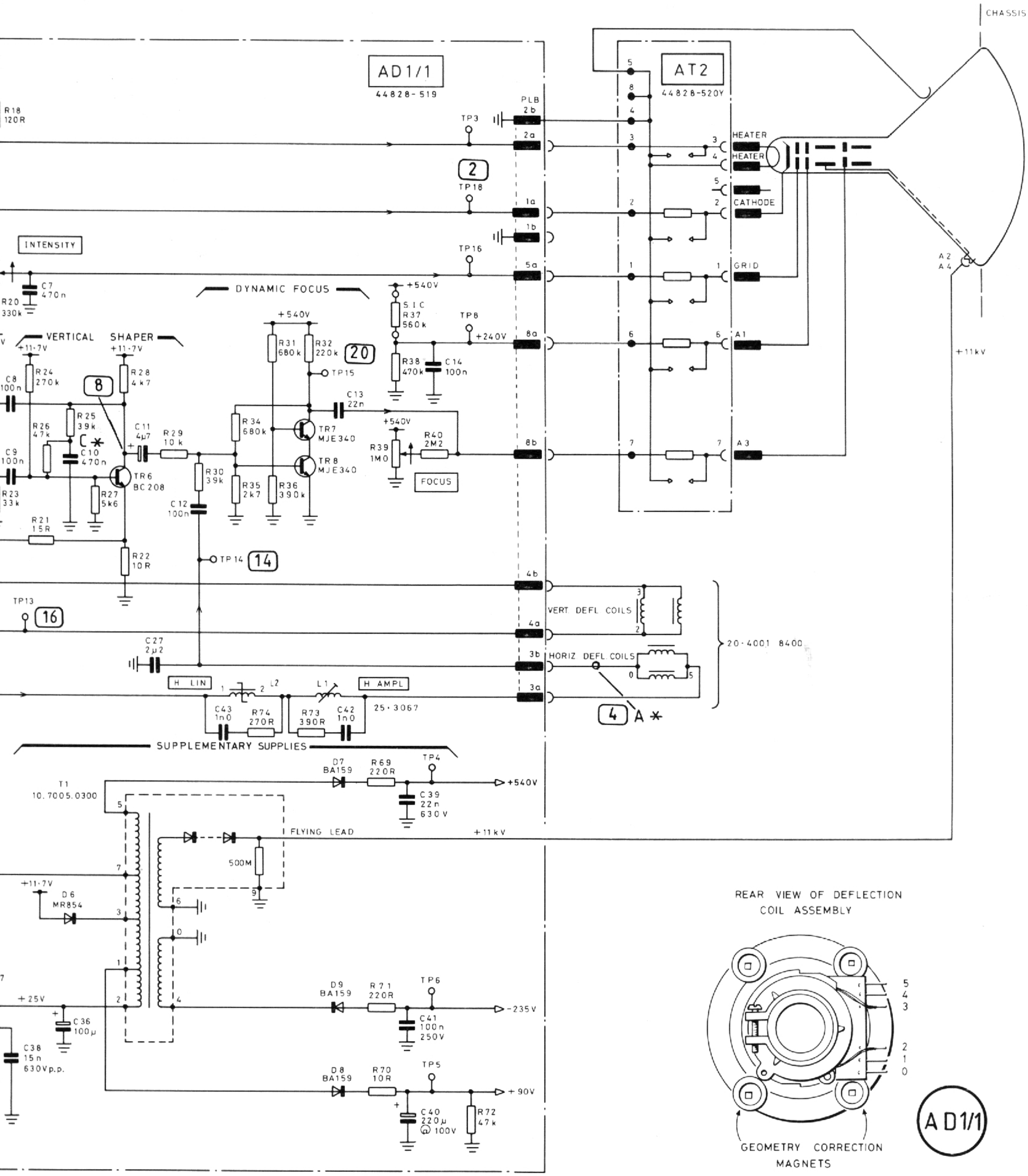
Component layout for AD1/1

Fig. 28
May 86



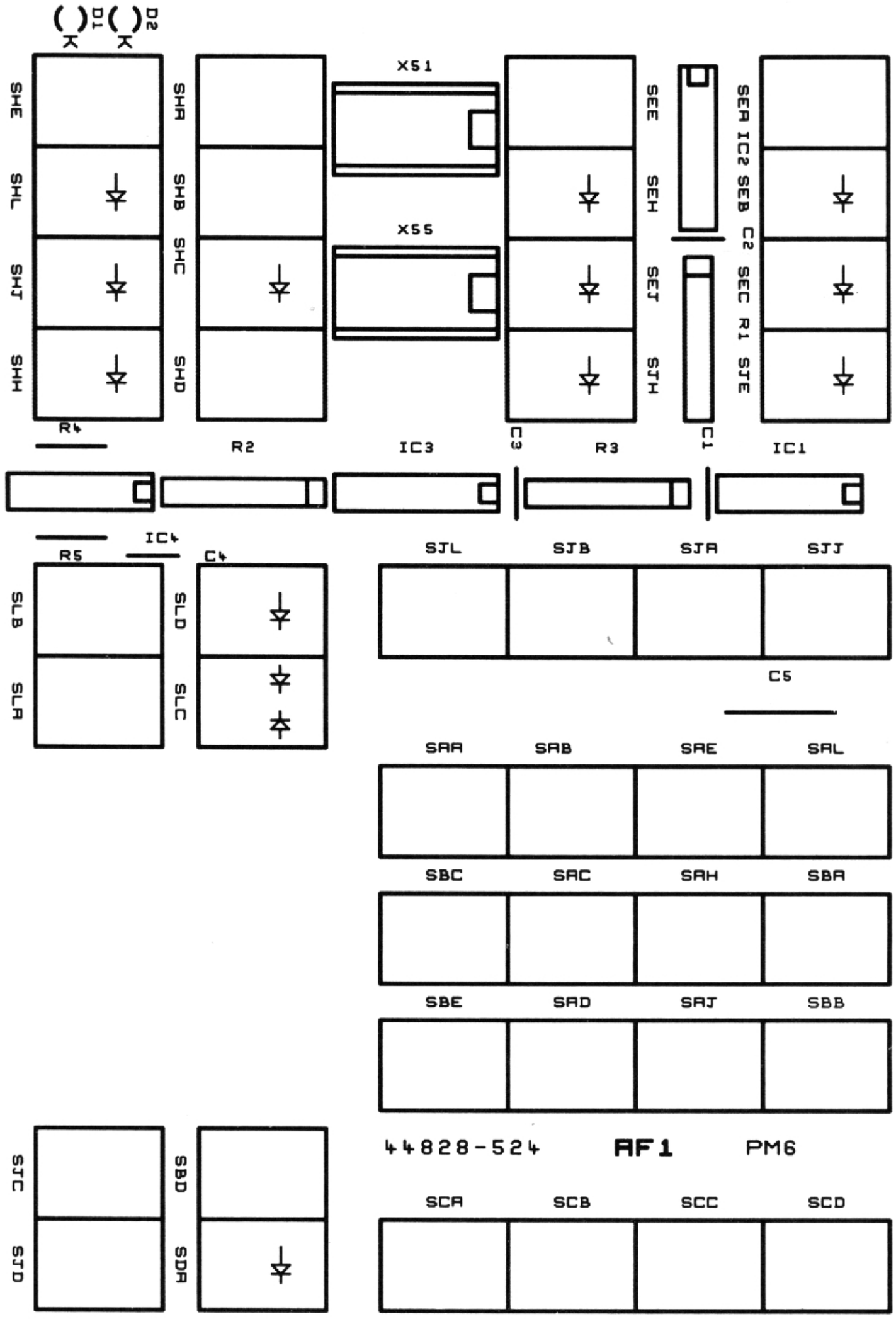
Org. No. Z52380-900E
Sh. 9 Iss. 1

AD



AD1/1 : Display drive

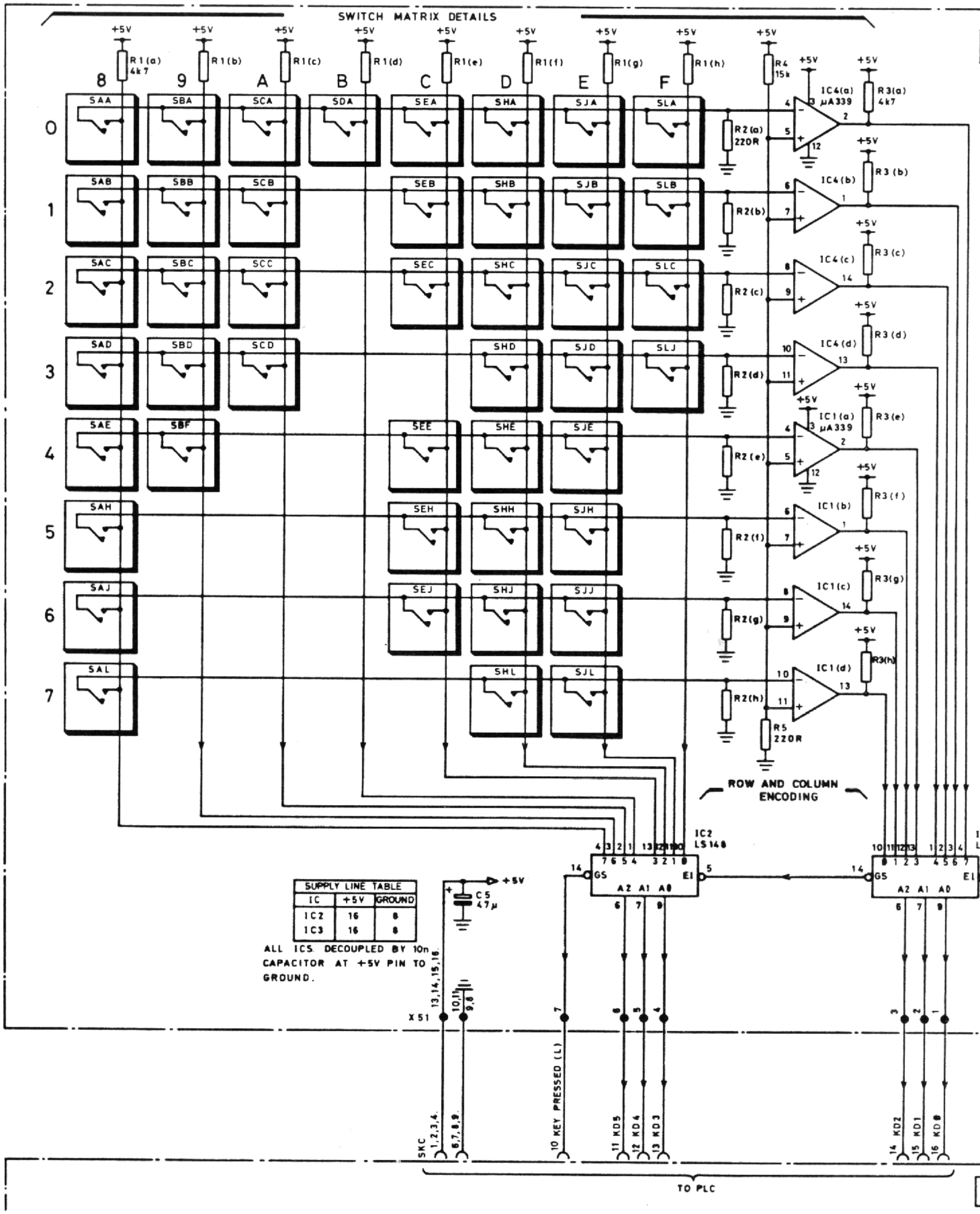
REAR VIEW OF DEFLECTION COIL ASSEMBLY



Component layout for AF1

Fig. 29
May 86

SWITCH MATRIX DETAILS

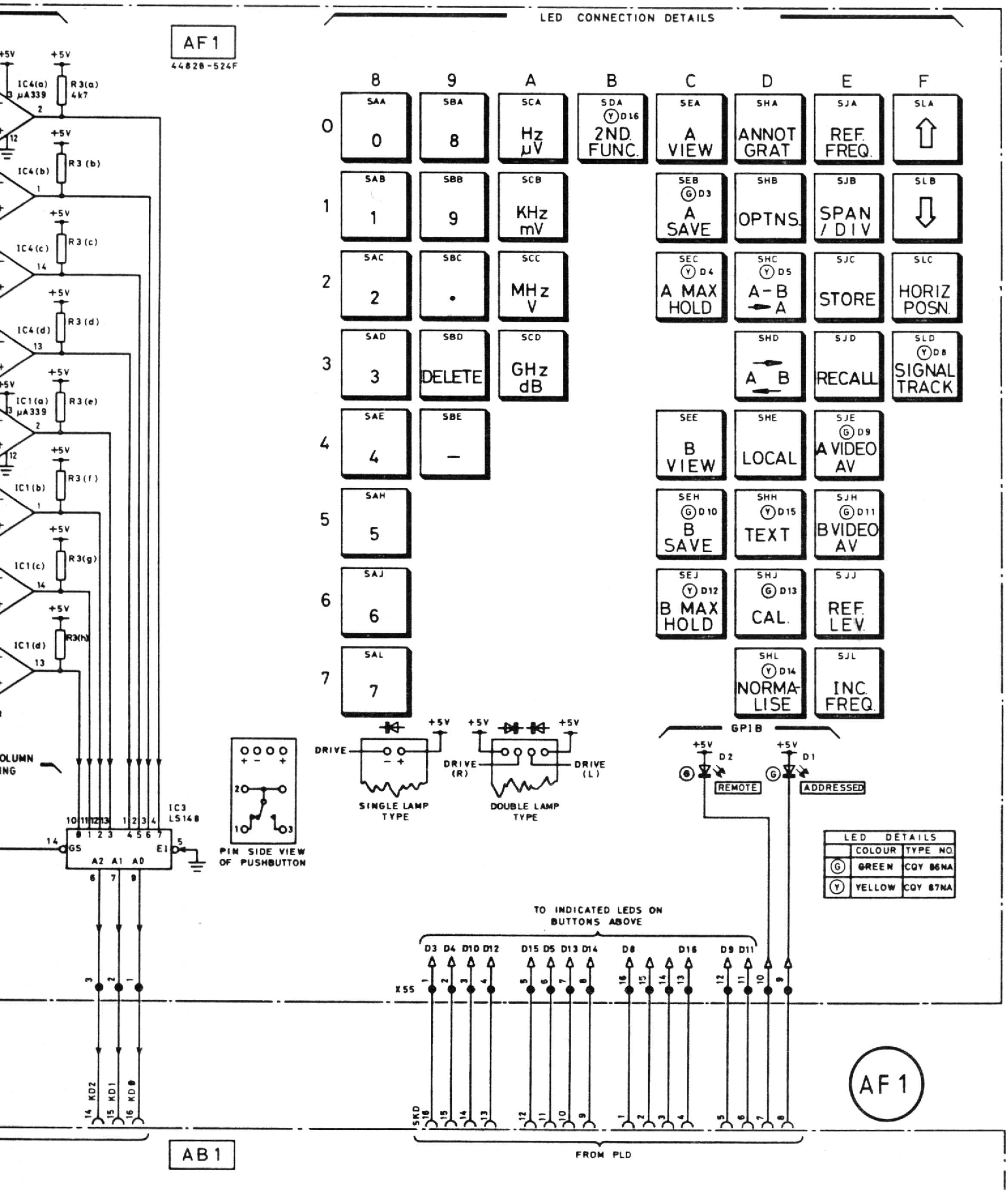


SUPPLY LINE TABLE		
IC	+5V	GROUND
IC2	16	8
IC3	16	8

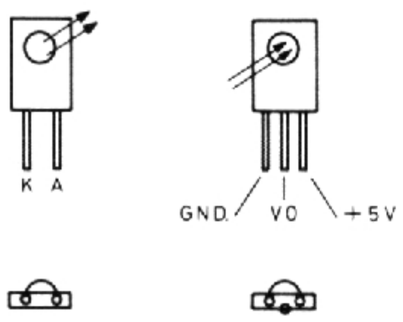
ALL ICS. DECOUPLED BY 10n CAPACITOR AT +5V PIN TO GROUND.

Drg.No. Z44828-524F
Sh.1 Iss.1

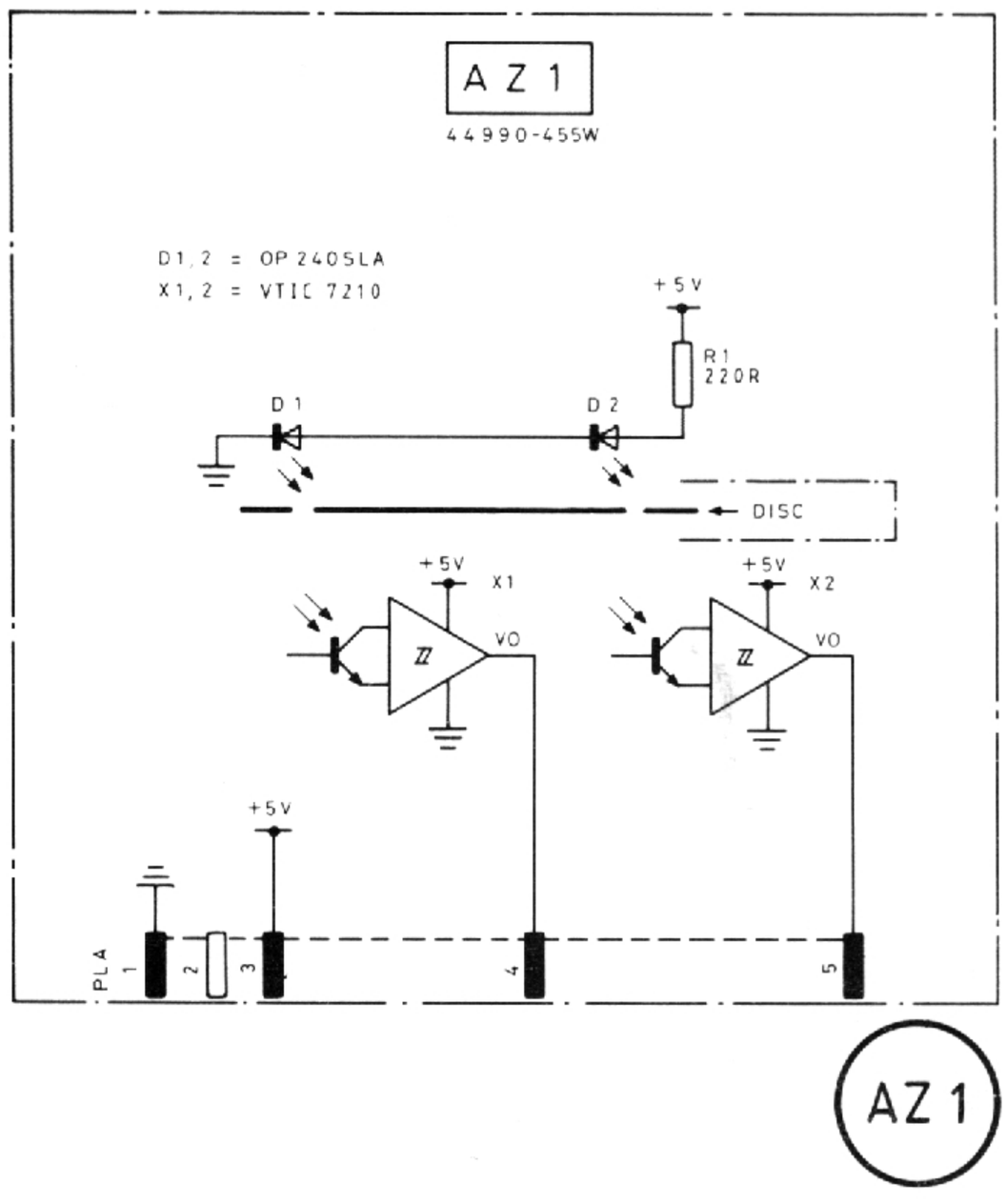
AF1: Keyboard matrix & enco



matrix & encoding



Drg.No. Z44990-455W
Sh.1 Iss.3



AZ1 Optical encoder

Fig. 30
Chap. 7
Fig. 91/92

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11 85