Model 2002 Multimeter

Repair Manual

Contains Servicing Information

KEITHLEY

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Keithley Instruments, Inc. warrants the following items for 90 days from the date of shipment: probes, cables, rechargeable batteries, diskettes, and documentation.

During the warranty period, we will, at our option, either repair or replace any product that proves to be defective.

To exercise this warranty, write or call your local Keithley representative, or contact Keithley headquarters in Cleveland, Ohio. You will be given prompt assistance and return instructions. Send the product, transportation prepaid, to the indicated service facility. Repairs will be made and the product returned, transportation prepaid. Repaired or replaced products are warranted for the balance of the original warranty period, or at least 90 days.

LIMITATION OF WARRANTY

This warranty does not apply to defects resulting from product modification without Keithley's express written consent, or misuse of any product or part. This warranty also does not apply to fuses, software, non-rechargeable batteries, damage from battery leakage, or problems arising from normal wear or failure to follow instructions.

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KEITHLEY

Keithley Instruments, Inc. • 28775 Aurora Road • Cleveland, OH 44139 • 440-248-0400 • Fax: 440-248-6168 • http://www.keithley.com

CHINA:	**Keithley Instruments China** • Yuan Chen Xin Building, Room 705 • 12 Yumin Road, Dewai, Madian • Beijing 100029 • 8610-62022886 • Fax: 8610-62022892
FRANCE:	**Keithley Instruments SARL** • BP 60 • 3 Allée des Garays • 91122 Palaiseau Cédex • 33-1-60-11-51-55 • Fax: 33-1-60-11-77-26
GERMANY:	**Keithley Instruments GmbH** • Landsberger Strasse 65 • D-82110 Germering, Munich • 49-89-8493070 • Fax: 49-89-84930759
GREAT BRITAIN:	**Keithley Instruments, Ltd.** • The Minster • 58 Portman Road • Reading, Berkshire, England RG3 1EA • 44-1189-596469 • Fax: 44-1189-575666
ITALY:	**Keithley Instruments SRL** • Viale S. Gimignano 38 • 20146 Milano • 39-2-48303008 • Fax: 39-2-48302274
NETHERLANDS:	**Keithley Instruments BV** • Avelingen West 49 • 4202 MS Gorinchem • 31-(0)183-635333 • Fax: 31-(0)183-630821
SWITZERLAND:	**Keithley Instruments SA** • Kriesbachstrasse 4 • 8600 Dübendorf • 41-1-8219444 • Fax: 41-1-8203081
TAIWAN:	**Keithley Instruments Taiwan** • 1FL., 85 Po Ai Street • Hsinchu, Taiwan • 886-3-572-9077 • Fax: 886-3-572-9031

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Manual Print History

The print history shown below lists the printing dates of all Revisions and Addenda created for this manual. The Revision Level letter increases alphabetically as the manual undergoes subsequent updates. Addenda, which are released between Revisions, contain important change information that the user should incorporate immediately into the manual. Addenda are numbered sequentially. When a new Revision is created, all Addenda associated with the previous Revision of the manual are incorporated into the new Revision of the manual. Each new Revision includes a revised copy of this print history page.

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Safety Precautions

The following safety precautions should be observed before using this product and any associated instrumentation. Although some instruments and accessories would normally be used with non-hazardous voltages, there are situations where hazardous conditions may be present.

This product is intended for use by qualified personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read the operating information carefully before using the product.

The types of product users are:

Responsible body is the individual or group responsible for the use and maintenance of equipment, and for ensuring that operators are adequately trained.

Operators use the product for its intended function. They must be trained in electrical safety procedures and proper use of the instrument. They must be protected from electric shock and contact with hazardous live circuits.

Maintenance personnel perform routine procedures on the product to keep it operating, for example, setting the line voltage or replacing consumable materials. Maintenance procedures are described in the manual. The procedures explicitly state if the operator may perform them. Otherwise, they should be performed only by service personnel.

Service personnel are trained to work on live circuits, and perform safe installations and repairs of products. Only properly trained service personnel may perform installation and service procedures.

Exercise extreme caution when a shock hazard is present. Lethal voltage may be present on cable connector jacks or test fixtures. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS, 42.4V peak, or 60VDC are present. **A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.**

Users of this product must be protected from electric shock at all times. The responsible body must ensure that users are prevented access and/or insulated from every connection point. In some cases, connections must be exposed to potential human contact. Product users in these circumstances must be trained to protect themselves from the risk of electric shock. If the circuit is capable of operating at or above 1000 volts, **no conductive part of the circuit may be exposed.**

As described in the International Electrotechnical Commission (IEC) Standard IEC 664, digital multimeter measuring circuits (e.g., Keithley Models 175A, 199, 2000, 2001, 2002, and 2010) measuring circuits are Installation Category II. All other instruments' signal terminals are Installation Category I and must not be connected to mains.

Do not connect switching cards directly to unlimited power circuits. They are intended to be used with impedance limited sources. NEVER connect switching cards directly to AC mains. When connecting sources to switching cards, install protective devices to limit fault current and voltage to the card.

Before operating an instrument, make sure the line cord is connected to a properly grounded power receptacle. Inspect the connecting cables, test leads, and jumpers for possible wear, cracks, or breaks before each use.

For maximum safety, do not touch the product, test cables, or any other instruments while power is applied to the circuit under test. ALWAYS remove power from the entire test system and discharge any capacitors before: connecting or disconnecting cables or jumpers, installing or removing switching cards, or making internal changes, such as installing or removing jumpers.

Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

Do not exceed the maximum signal levels of the instruments and accessories, as defined in the specifications and operating information, and as shown on the instrument or test fixture panels, or switching card.

When fuses are used in a product, replace with same type and rating for continued protection against fire hazard.

Chassis connections must only be used as shield connections for measuring circuits, NOT as safety earth ground connections.

If you are using a test fixture, keep the lid closed while power is applied to the device under test. Safe operation requires the use of a lid interlock.

If a  screw is present, connect it to safety earth ground using the wire recommended in the user documentation.

The  symbol on an instrument indicates that the user should refer to the operating instructions located in the manual.

The  symbol on an instrument shows that it can source or measure 1000 volts or more, including the combined effect of normal and common mode voltages. Use standard safety precautions to avoid personal contact with these voltages.

The **WARNING** heading in a manual explains dangers that might result in personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

The **CAUTION** heading in a manual explains hazards that could damage the instrument. Such damage may invalidate the warranty.

Instrumentation and accessories shall not be connected to humans.

Before performing any maintenance, disconnect the line cord and all test cables.

To maintain protection from electric shock and fire, replacement components in mains circuits, including the power transformer, test leads, and input jacks, must be purchased from Keithley Instruments. Standard fuses, with applicable national safety approvals, may be used if the rating and type are the same. Other components that are not safety related may be purchased from other suppliers as long as they are equivalent to the original component. (Note that selected parts should be purchased only through Keithley Instruments to maintain accuracy and functionality of the product.) If you are unsure about the applicability of a replacement component, call a Keithley Instruments office for information.

To clean the instrument, use a damp cloth or mild, water based cleaner. Clean the exterior of the instrument only. Do not apply cleaner directly to the instrument or allow liquids to enter or spill on the instrument.

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1
Routine Maintenance

1.1 Introduction

The information in this section deals with routine type maintenance that can be performed by the operator. This information is arranged as follows:

1.2 Line fuse replacement: Explains how to replace a blown line power fuse.

1.3 Current fuse replacement: Explains how to replace a blown current fuse.

1.4 Fan filter cleaning: Explains how to remove and clean the filter element for the cooling fan.

1.5 Firmware updates: Recommends a course of action for firmware updates provided by Keithley.

1.2 Line fuse replacement

WARNING

Disconnect the line cord at the rear panel and remove all test leads connected to the instrument (front and rear) before replacing the line fuse.

The power line fuse is accessible from the rear panel, just below the AC power receptacle (see Figure 1-1). Perform the following steps to replace the line fuse:

1. Insert a bladed screwdriver into the slot of the fuse carrier.
2. While pushing in, turn the screwdriver counter-clockwise until the spring-loaded fuse carrier releases from the fuse holder.
3. Pull out the fuse carrier and replace the fuse with the type specified in Table 1-1.

CAUTION

To prevent instrument damage, use only the fuse type specified in Table 1-1.

4. Re-install the fuse carrier.

NOTE

If the power line fuse continues to blow, a circuit malfunction exists and must be corrected. Refer to the troubleshooting section of this manual for additional information.

Table 1-1
Power line fuse

Size	Rating	Keithley Part No.
5 × 20mm	250V, ½A, Slo-Blo	FU-71

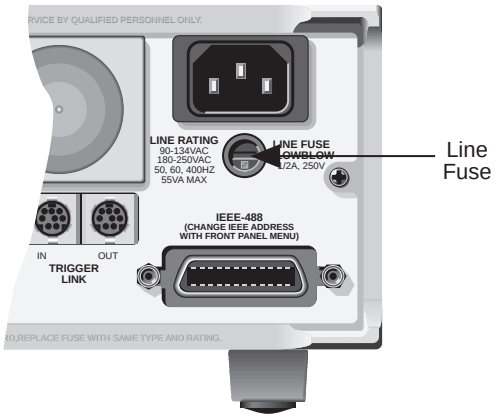

Figure 1-1
Line fuse location

1.3 Current fuse replacement

Each AMPS input (front and rear) has its own current fuse. When replacing a current fuse, use the type specified in Table 1-2.

Table 1-2
Power line fuse

Size	Rating	Keithley Part No.
5 × 20mm	250V, 2A, Slo-Blo	FU-48

WARNING

Disconnect the instrument from the power line and remove all test leads (front and rear) before replacing the AMPS fuses.

1.3.1 Front AMPS input fuse

The front panel AMPS jack functions as the AMPS input terminal and as the carrier for the AMPS fuse (see Figure 1-2). Perform the following steps to replace the fuse:

1. Push in the AMPS input jack and turn counter-clockwise until the spring-loaded fuse carrier releases from the fuse holder.
2. Pull out the fuse carrier and replace the fuse with the type specified in Table 1-2.

CAUTION

To prevent instrument damage, use only the type specified in Table 1-2.

3. Re-install the fuse carrier.

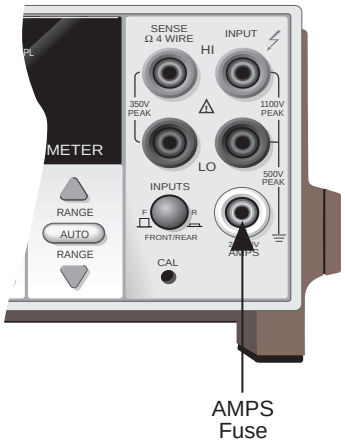

Figure 1-2
Front AMPS input fuse location

1.3.2 Rear AMPS input fuse

The rear AMPS input fuse is located just below the AMPS input jack (see Figure 1-3). Perform the following steps to replace the fuse:

1. Insert a bladed screwdriver into the slot of the fuse carrier.
2. While pushing in, turn the screwdriver counter-clockwise until the spring loaded fuse carrier releases from the fuse holder.
3. Pull out the fuse carrier and replace the fuse with the type specified in Table 1-2.

CAUTION

To prevent instrument damage, use only the fuse type specified in Table 1-2.

4. Re-install the fuse carrier.

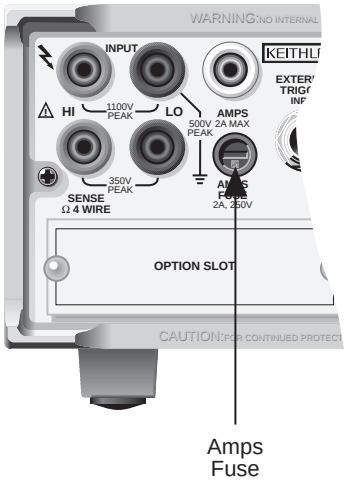

Figure 1-3
Rear AMPS input fuse location

1.4 Fan filter cleaning

The filter for the cooling fan requires periodic cleaning to maintain proper ventilation. The fan filter is accessible from the rear panel. Perform the following steps to remove the filter for cleaning:

1. While facing the rear panel, locate the lower right-hand corner of the filter cover plate.
2. At this corner, place a thin-bladed screwdriver between the cover plate and the rear panel, and gently pry the filter assembly away from the chassis.

The filter element is permanently fixed to the cover plate. Do not attempt to remove the filter element from the cover plate.

WARNING

Exercise care when handling the filter assembly. The filter element is a metal screen with sharp edges that could cause injury if not handled carefully.

The filter element is made of a rugged metal screen allowing the use of any type cleaning solution to clean it. A small metal brush can be used to remove dirt and debris. After cleaning the filter, rinse thoroughly with water. Make sure the filter assembly is completely dry before re-installing it.

1.5 Firmware updates

It is possible that you may receive a firmware update from Keithley to enhance operation and/or fix “bugs”. The firmware for the main microprocessor is contained in two EPROMS installed in sockets on the PC board to make replacement relatively easy.

The replacement procedure requires that the case cover be removed, and these static-sensitive devices require special handling. As a result, the firmware update procedure should be performed only by qualified service personnel. The procedure to replace the firmware EPROMS is contained in paragraph 3.8.

2
Troubleshooting

WARNING

The information in this section is intended for qualified service personnel. Some of these procedures may expose you to hazardous voltages. Do not perform these hazardous procedures unless you are qualified to do so.

2.1 Introduction

This section of the manual will assist you in troubleshooting the Model 2002. Included are self-tests, test procedures, troubleshooting tables, and circuit descriptions. It is left to the discretion of the repair technician to select the appropriate tests and documentation needed to troubleshoot the instrument.

This section is arranged as follows:

2.2 Repair considerations: Covers some considerations that should be noted before making any repairs to the Model 2002.

2.3 Power-on test: Describes the tests that are performed on its memory elements each time the instrument is turned on.

2.4 Front panel tests: Provides the procedures to test the functionality of the front panel keys and the display.

2.5 Diagnostics: Explains how to use the Diagnostics test mode of the Model 2002. In general, Diagnostics locks-up the instrument in various states of operation. With the instrument in a static state, you can then check the state of the various logic levels on the control registers and signal trace through the unit.

2.6 Control register bit patterns: Provides shift register bit patterns for the basic measurement functions and ranges.

2.7 Display board checks: Provides display board checks that can be made if Front Panel Tests fail.

2.8 Power supply checks: Provides power supply checks that can be made if the integrity of the power supply is questionable.

2.9 Principles of operation: Provides support documentation for the various troubleshooting tests and procedures. Included is some basic circuit theory for the display board and power supply, and support documentation for Built-in tests.

2.10 Built-in test overview: Summarizes the Built-in tests, which can be used to test and exercise the various circuits on the digital board, analog board and A/D converter boards.

2.11 Built-in test documentation: Provides a detailed analysis of each Built-in test.

2.2 Repair considerations

Before making any repairs to the Model 2002, be sure to read the following considerations.

CAUTION

The PC-boards are built using surface mount techniques and require specialized equipment and skills for repair. If you are not equipped and/or qualified, it is strongly recommended that you send the unit back to the factory for repairs or limit repairs to the PC-board replacement level (see following NOTE). Without proper equipment and training, you could damage a PC-board beyond repair.

NOTE

For units that are out of warranty, completely assembled PC-boards can be ordered from Keithley to facilitate repairs.

1. Repairs will require various degrees of disassembly. However, it is recommended that the Front Panel Tests (paragraph 2.4) and Built-In-Test (paragraph 2.10) be performed prior to any disassembly. The disassembly instructions for the Model 2002 are contained in Section 3 of this manual.
2. Do not make repairs to surface mount PC-boards unless equipped and qualified to do so (see previous CAUTION).
3. When working inside the unit and replacing parts, be sure to adhere to the handling precautions and cleaning procedures explained in paragraph 3.2.
4. Many CMOS devices are installed in the Model 2002. These static-sensitive devices require special handling as explained in paragraph 3.3.
5. Anytime a circuit board is removed or a component is replaced, the Model 2002 must be recalibrated.

2.3 Power-on test

During the power-on sequence, the Model 2002 will perform a checksum test on its EPROM (U637 and U638) and test its RAM (U608, U635, and U636). If one of these tests fail the instrument will lock up.

2.4 Front panel tests

There are two Front Panel Tests; one to test the functionality of the front panel keys and one to test the display. In the event of a test failure, refer to paragraph 2.7 for details on troubleshooting the display board.

2.4.1 KEYS test

The KEYS test allows you to check the functionality of each front panel key. Perform the following steps to run the KEYS test.

1. Display the MAIN MENU by pressing the MENU key.
2. Select TEST, and press ENTER to display the SELF-TEST MENU.
3. Select FRONT-PANEL-TESTS, and press ENTER to display the following menu:

   FRONT PANEL TESTS
   KEYS DISPLAY-PATTERNS CHAR-SET

4. Select KEYS, and press ENTER to start the test. When a key is pressed, the label name for that key will be displayed to indicate that it is functioning properly. When the key is released, the message “No keys pressed” is displayed.
5. Pressing EXIT tests the EXIT key. However, the second consecutive press of EXIT aborts the test and returns the instrument to the SELF-TEST MENU. Continue pressing EXIT to back out of the menu structure.

2.4.2 DISPLAY PATTERNS test

The display test allows you to verify that each pixel and annunciator in the vacuum fluorescent display is working properly. Perform the following steps to run the display test:

1. Display the MAIN MENU by pressing the MENU key.
2. Select TEST, and press ENTER to display the SELF-TEST MENU.
3. Select FRONT-PANEL-TESTS, and press ENTER to display the following menu:

   FRONT PANEL TESTS
   KEYS DISPLAY-PATTERNS CHAR-SET

4. Select DISPLAY-PATTERNS, and press ENTER to start the display test. There are five parts to the display test. Each time a front panel key (except EXIT) is pressed, the next part of the test sequence is selected. The five parts of the test sequence are as follows:
   A. Checkerboard pattern (alternate pixels on) and all annunciators.

B. Checkerboard pattern and the annunciators that are on during normal operation.
C. Horizontal lines (pixels) of the first digit are sequenced.
D. Vertical lines (pixels) of the first digit are sequenced.
E. Each digit (and adjacent annunciator) is sequenced. All the pixels of the selected digit are on.

5. When finished, abort the display test by pressing EXIT. The instrument returns to the SELF-TEST MENU. Continue pressing EXIT to back out of the menu structure.

2.4.3 Character set test

You can also display the character set as follows:

1. Display the MAIN MENU by pressing the MENU key.
2. Select TEST, and press ENTER to display the SELF-TEST MENU.
3. Select FRONT-PANEL-TESTS, and press ENTER to display the following menu:

   FRONT PANEL TESTS
   KEYS DISPLAY-PATTERNS CHAR-SET

4. Select CHAR-SET, and press ENTER to display the character set. Press EXIT to abort the test.

2.5 Diagnostics

The Model 2002 has diagnostic test modes that allow you to "freeze" instrument operation letting you check logic levels on the various control registers. The known bit pattern at these registers can then be used for signal tracing through the unit.

Perform the following steps to use DIAGNOSTICS:

1. Display the MAIN MENU by pressing the MENU key.
2. Select TEST, and press ENTER to display the SELF-TEST MENU.
3. Place the cursor on DIAGNOSTICS, and press ENTER.
4. Use the range keys to scroll through the various diagnostics phases summarized in Table 2-1.
5. To view A/D counts, press the right arrow key.
6. When finished, press EXIT three times to back out of the menu structure and return to the normal measurement mode of operation.

Table 2-1
Diagnostic bit patterns

Mode	Register IC*	
	U206	**U207**
Zero X1	01110000	00001111
Zero X5	10110000	00001111
Zero X50	11010000	00001111
Sense Zero X1	01110000	00011011
Sense Zero X5	10110000	00011011
Sense Zero X50	11010000	00011011
2V Reference	10110000	01010111
7V Reference	01110000	00110111
20V Zero	01110100	01101111
20V Reference low	01110001	01101111
20V Reference high	01110010	01101111

*Bits associated with register IC terminals as follows:
Q Q Q Q
87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.6 Control register bit patterns

2.6.1 Control register ICs

The four control registers are made up of the following ICs:

AD_STB: U811, U810, U809
MUX_STB: U206, U207
R1_STB: U203, U222, U224
R2_STB: U400, U406, U411, U432

2.6.2 Normal operation bit patterns

Table 2-2, Table 2-3, and Table 2-4 are provided to allow you to check logic levels on the R1_STB, R2_STB, and MUX_STB shift registers for each basic measurement function (DCV, ACV, DCI, ACI, Ω2 and Ω4) and range. The known bit pattern at these registers can then be used for signal tracing through the unit.

To use these tables, simply place the instrument in the designated function and range and check the output of the shift registers for the indicated bit pattern. The bit patterns in these tables assume the following conditions:

NPLC > 0.01
AC Type = RMS or Average
Offset Compensated Ohms = Off
Current Measurement Mode = Normal (No In-Circuit I)

Table 2-2
R1_STB register control bits

Range and function	Register IC*		
	U224	**U203**	**U221**
200mV-20V DC	10011111	01110000	11101001
200V, 1000V DC	10011111	00000110	11101001
200µA DC	00010111	00000110	11101001
2mA DC	00001111	00000110	11101001
20mA DC	00111111	00000110	11101001
200mA DC	01011111	00000110	11101001
2A DC	10011111	00000110	11101001
20Ω 2-wire	10011111	11110000	01110111
200Ω 2-wire	10011111	11110000	10110111
2kΩ 2-wire	10011111	11110000	10110111
20kΩ 2-wire	10011111	11110000	11010111
200kΩ 2-wire	10011111	11110000	11100111
2MΩ 2-wire	10011111	11110000	11101011
20MΩ 2-wire	10011111	01110100	11101000
200MΩ 2-wire	10011111	01110100	11101000
1GΩ 2-wire	10011111	01110100	11101000
20Ω 4-wire	10011111	10100001	01110111
200Ω 4-wire	10011111	10100001	10110111
2kΩ 4-wire	10011111	10100001	10110111
20kΩ 4-wire	10011111	10100001	11010111
200kΩ 4-wire	10011111	10100001	11100111
2MΩ 4-wire	10011111	10100001	11101011
200mV -750V AC	10011111	00001110	11101001
200µA AC	00010011	00000110	11101001
2mA AC	00001011	00000110	11101001
20mA AC	00111011	00000110	11101001
200mA AC	01011011	00000110	11101001
2A AC	10011011	00000110	11101001

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q
87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Table 2-3
R2_STB register control bits

Range and function	Register IC*			
	U400	**U432**	**U411**	**U406**
200mV-1000V DC	01101010	00000000	10100011	00000111
200µA-2A DC	01101010	00000000	10100011	00000111
20Ω-1GΩ 2-wire	01101010	00000000	10100011	00000111
20Ω-2MΩ 4-wire	01101010	00000000	10100011	00000111
200mV AC	01110001	10000000	11101101	10011111
2V AC	01110001	10000000	11101001	10011111
20V AC	01110001	10000000	11101111	00011110
200V AC	01110001	10000000	11101011	00011110
750V AC	01110001	10000000	11101010	00011110
200µA-2A AC	01110001	10000000	11101111	01001111

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Table 2-4
MUX_STB register control bits

Range and function	Register IC*	
	U206	**U207**
200mV DC	11000000	00001111
2V DC	10100000	00001111
20V DC	01111000	01101111
200V DC	10100000	00011110
1000V DC	01100000	00011110
200µA-2A DC	11010000	10101111
20Ω-200Ω 2-wire	11000000	00001111
2kΩ-200kΩ 2-wire	10100000	00001111
2MΩ-20MΩ 2-wire	01100000	00001111
200MΩ-1GΩ 2-wire	01111000	01101111
20Ω-200Ω 4-wire	11000000	00011101
2kΩ-200kΩ 4-wire	10100000	00011101
2MΩ 4-wire	01100000	00011101
2V-750V AC	10110000	11001111
200µA-2A AC	10110000	11001111

*Bits associated with register IC terminals as follows:
Q Q Q Q
87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.7 Display board checks

If the FRONT PANEL TESTS (paragraph 2.4) indicate that there is a problem on the display board, use Table 2-5. Circuit theory for the display is provided in paragraph 2.9.1.

Drawing reference: Display Board; 2002-110

2.8 Power supply checks

Power supply problems can be checked out using Table 2-6.

Drawing reference: Analog Board; 2002-100

Table 2-5
Display board checks

Step	Item/component	Required conditions	Remarks
1	FRONT PANEL TESTS	Verify that all pixels operate	Use SELF-TEST MENU selection
2	P1033, pin 5	+5V, ±5%	Digital +5V supply
3	CR902 cathode	+60V, ±10%	VFD +60V supply
4	P1033, pin 12	Goes low briefly on power-up, then goes high	Microcontroller RESET line
5	U902, pin 43	4MHz square wave	Controller 4MHz clock
6	P1033, pin 8	Pulse train every 1msec	Control from main processor
7	P1033, pin 10	Brief pulse train when front panel key pressed.	Key down data sent to main processor.

Table 2-6
Display board checks

Step	Item/component	Required conditions	Remarks
1	F101 line fuse	Check continuity	Remove to check
2	Line power	Plugged into live receptacle, power on	Check for correct power-up sequence
3	U108, pin 3	+5V, ±5%	Referenced to Common 3
4	U110, pin 3	+5V, ±5%	Referenced to digital common
5	U109, pin 3	+15V, ±0.75V	Referenced to COM
6	U107, pin 3	-15V, ±0.75V	Referenced to COM
7	CR114, +BS	+34V to +38V	Referenced to Common 3
8	CR115, -BS	-34V to -38V	Referenced to Common 3
9	U105, pin 3	≈+18V	Referenced to Isolated Common
10	U105, pin 2	+8V	Referenced to Isolated Common
11	U619, +5VC	+5V, ±5%	Referenced to Digital Common
12	U629, pin 3	+5V, ±5%	Referenced to Digital Common

2.9 Principles of operation

The following information is provided to support the troubleshooting tests and procedures previously covered in this section of the manual. Most circuits in the Model 2002 are tested and/or exercised by Built-in Test, which is described in detail in paragraphs 2.10 and 2.11. Since the display board and the power supply are not tested by Built-in Test, some basic theory is provided for these circuits in paragraphs 2.9.2 and 2.9.3.

2.9.1 Block diagrams

Figure 2-1 provides an overall block diagram of the Model 2002, while Figures 2-2 through 2-5 show block diagrams of the power supply, display board, digital board, and analog board respectively.

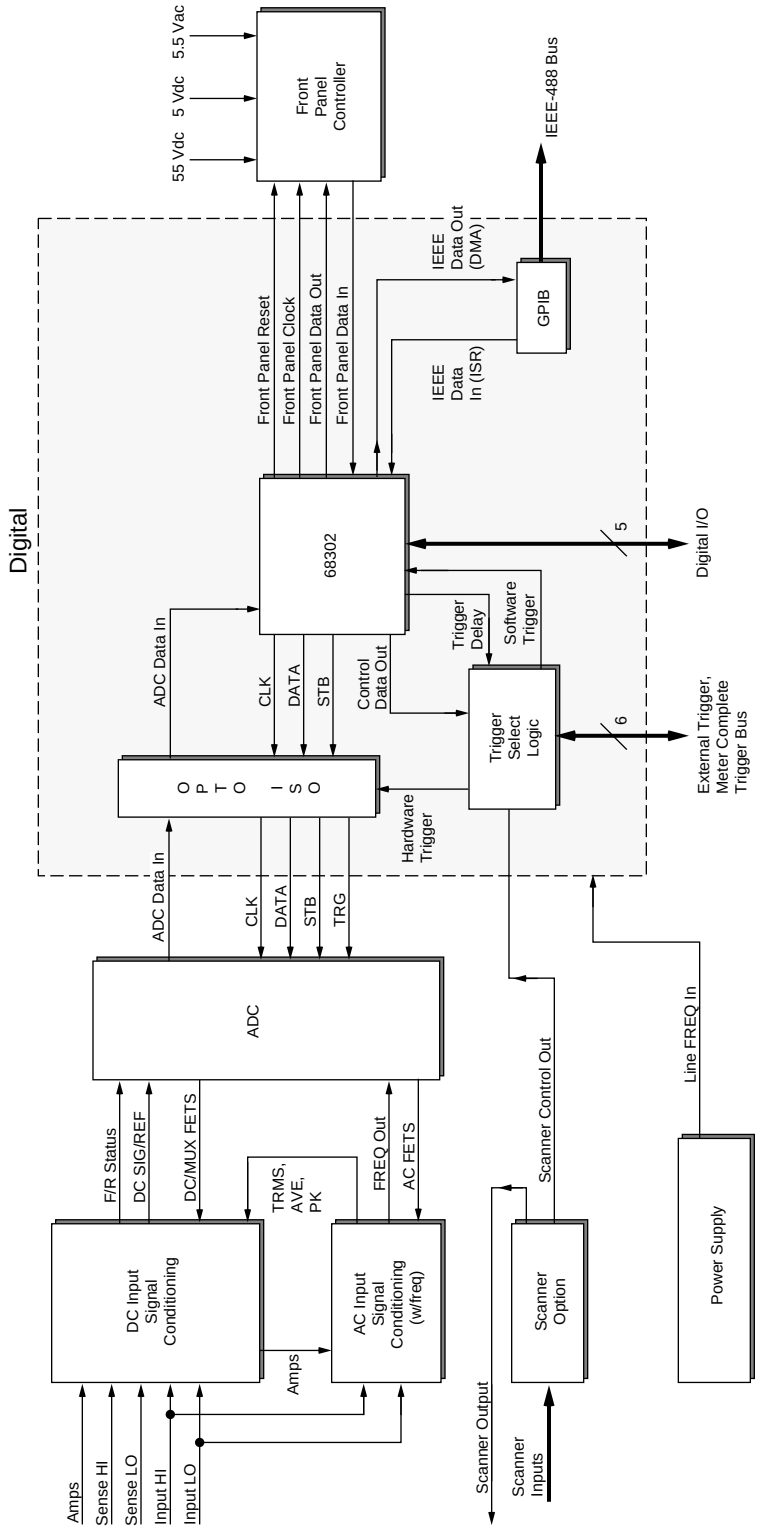

Figure 2-1
Model 2002 overall block diagram

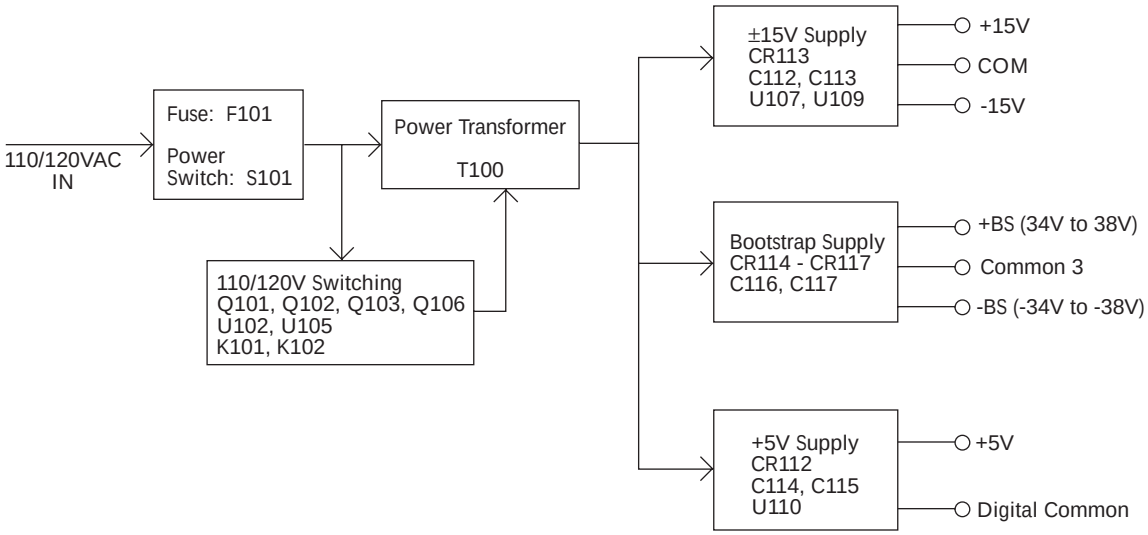

Figure 2-2
Power supply block diagram

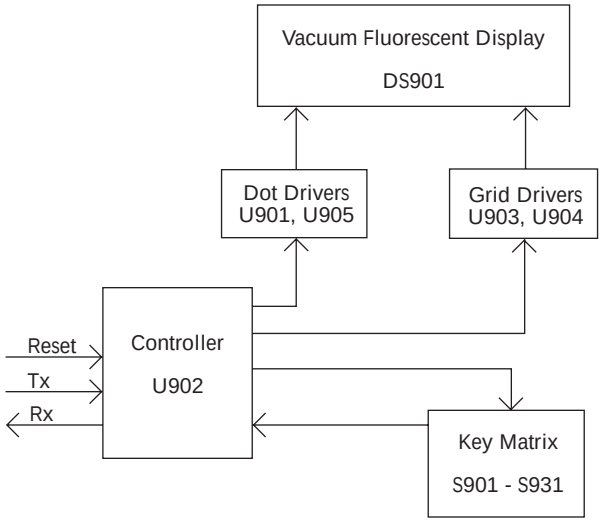

Figure 2-3
Display board block diagram

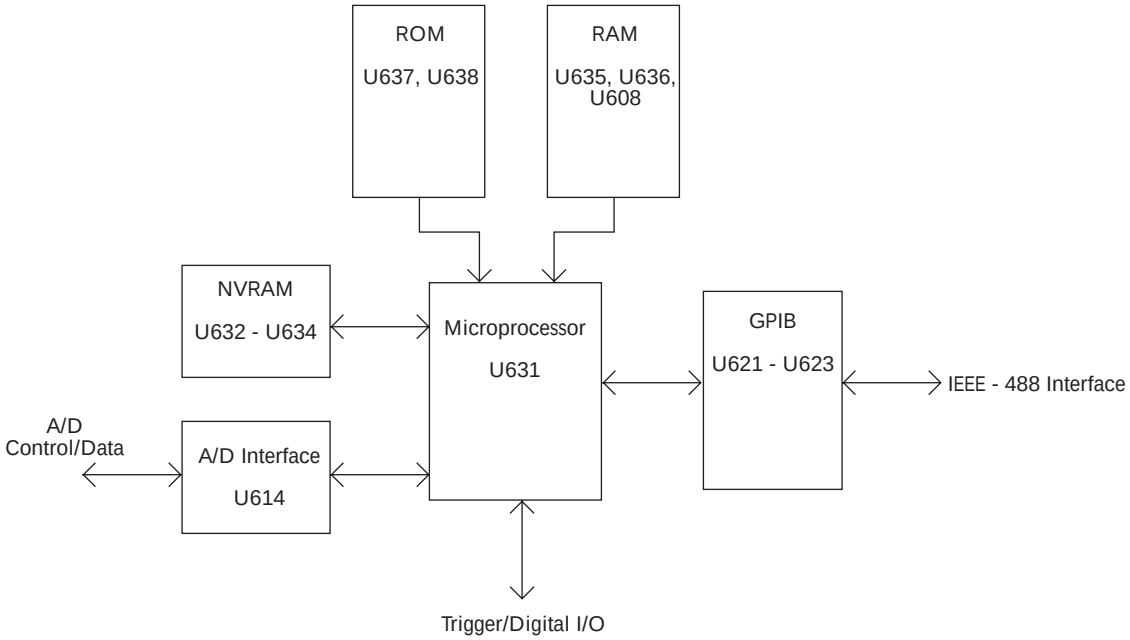

Figure 2-4
Digital board block diagram

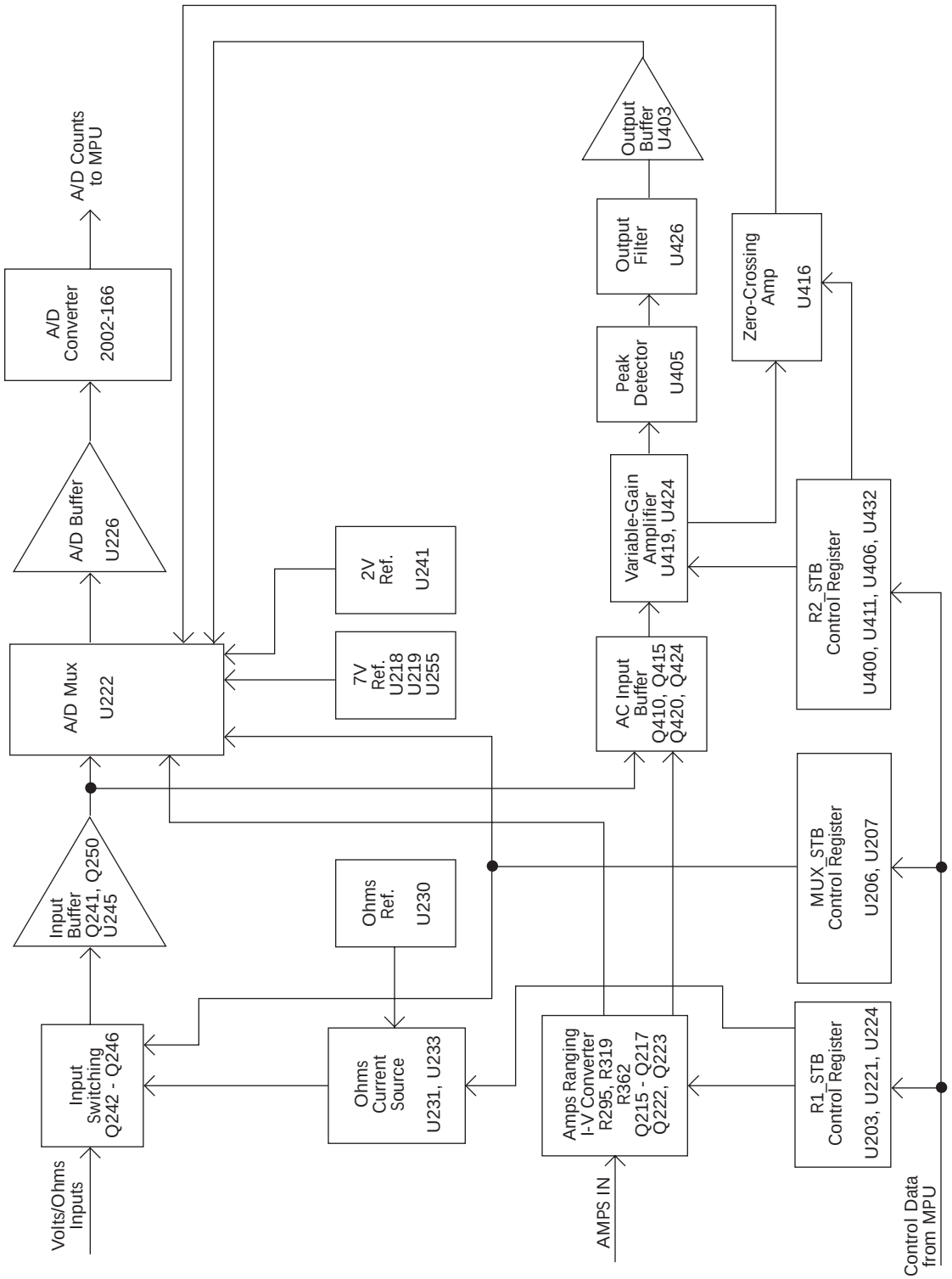

Figure 2-5
Analog board block diagram

2.9.2 Display board circuit theory

The following information provides some basic circuit theory that can be used as an aid to troubleshoot the display and keyboard.

Display microcontroller

U902 is the display microcontroller that controls the VFD (vacuum fluorescent display) and interprets key data. The microcontroller has four peripheral I/O ports that are used for the various control and read functions.

Display data is serially transmitted to the microcontroller from the digital board via the TXB line to the microcontroller PD0 terminal. In a similar manner, key data is serially sent back to the digital board through the RXB line via PD1. The 4MHz clock for the microcontroller is generated on the digital board.

Vacuum fluorescent display

DS901 is the VFD (vacuum fluorescent display) module, which can display up to 49 characters. Each character is organized as a 5×7 matrix of dots or pixels and includes a long under-bar segment to act as a cursor.

The display uses a common multiplexing scheme with each character refreshed in sequence. U903 and U904 are the grid drivers, while U901 and U905 are the dot drivers. Note that dot driver and grid driver data is serially transmitted from the microcontroller (PD3 and PC1).

The VFD requires both +60VDC and 5VAC for the filaments. These VFD voltages are supplied by U625, which is located on the digital board.

Key matrix

The front panel keys (S901-S931) are organized into a row-column matrix to minimize the number of microcontroller peripheral lines required to read the keyboard. A key is read by strobing the columns and reading all rows for each strobed column. Key down data is interpreted by the display microcontroller and sent back to the main microprocessor using proprietary encoding schemes.

2.9.3 Power supply circuit theory

The following information provides some basic circuit theory that can be used as an aide to troubleshoot the power supply.

Pre-regulator circuit

The pre-regulator circuit regulates power to the transformer. When power is applied to the instrument, a power transformer secondary voltage (pins 12 and 13) is rectified (CR622), doubled (C624, C630, CR624 and CR625) and applied to U619, which is a +5V regulator. This +5V (+5VC) is used for the pre-regulator circuit.

The pre-regulator circuit monitors the voltage level on C611 using an integrator (U627). The voltage on C611 (typically around 7.5V) is divided by three through R712 and R713 and applied to the inverting input (pin 2) of the integrator. The +5V (+5VC) is divided by two through R706 and R708. This 2.5V reference is applied to the non-inverting input (pin 3) of the integrator.

When the voltage on the inverting input of the integrator is less than the 2.5V reference on the non-inverting input, the integrator output ramps in the positive direction. This positive ramp turns on Q608, which pulls the CONT line low to digital common. With CONT connected to common, current flows through the photodiode of U100 and generates a positive voltage at the gate of FET Q528. As Q528 turns on, the 470Ω resistor (R100) becomes shunted and results in less effective resistance to the transformer. The resultant increase in current (power) will increase the voltage on C611.

Conversely, when the voltage on the inverting input of the integrator is more than the 2.5V reference, the integrator output ramps in the negative direction and begins to turn Q608 off. This will decrease current through U100, decrease the positive voltage on Q528 and thus, increase the effective resistance to the transformer. The resultant decrease in current (power) will decrease the voltage of C611.

This constant regulation of effective resistance in series with the transformer regulates the power delivered to the instrument.

Line voltage (110V/220V) selection circuit

This circuit automatically selects the proper power line voltage setting for the instrument. The line selection circuit derives its power from the AC1 and AC2 lines on the primary side of the transformer. Rectifier CR104 applies approximately +18V to regulator U105. The output of U105 provides the +8V for the line voltage selection circuit and the HI/LO voltage control circuit.

U102 is a comparator that has a +4V reference (via voltage divider R111 and R112) applied to its non-inverting input. The inverting input monitors the voltage on C103. When the voltage at the inverting input is greater than 4V, the output of U102 goes low and turns on FET Q106. With Q106 on, +8V

will be applied to the +RELAY1 line, which energizes relay K101 to select the 110V setting. Conversely, when the voltage at the inverting input is less than 4V, the output of U102 goes high and turns off Q106. With Q106 off, the +8V is removed from K101 and thus, the line voltage setting defaults to 220V.

The AC power line is tied to C103 through CR102, R113 and R114 via control line ACL. When the AC power line voltage is less than approximately 135VAC, sufficient charge remains on C103 to keep the inverting input of U102 above 4V to ultimately energize K101 (110V setting). When the AC power line voltage is greater than approximately 18VAC, charge will be pulled from C103 dropping the voltage at the inverting input of the comparator to less than 4V. This will de-energize K101 (220V setting).

HI/LO voltage control circuit

This circuit automatically selects the appropriate HI/LO setting for the available power line voltage. During power-up, the line voltage is rectified (CR101), divided (R105 and R107, or R104 and R107) and applied to the base of Q102.

If the voltage level at the base of Q102 is high (above zener VR101), the transistor will turn on and apply power to the ISO1+ and ISO1- lines. With power applied to ISO1+ and ISO1-, U103 will turn on and allow Q105 to be forward biased. With U103 and Q105 on, TRIG of U106 will be pulled low and allow its output (OUT) to latch at +8V which will turn on FET Q104. With Q104 on, the -RELAY2 line will be connected to common, and thus energize K101 (HI setting).

If the power line voltage decreases to a low level, U103 will turn off, but the output of U106 will remain latched at +8V. However, the low line will be driven low turning on U104. With U104 and Q105 on, +8V will be applied to THR of U106 forcing its output (OUT) to reset to low. With the gate of Q104 low, the FET will turn off and open the relay coil circuit for K101 (LO setting).

The low line is controlled by comparator U628. The inverting input of the comparator is connected to the 2.5V reference. The non-inverting input monitors (via divider R709 and R711) C611. As previously explained, the typical power line voltage level will apply around 7.5V to C611. However, if the line voltage decreases such that the voltage on C611 becomes less than 6V, the voltage level on the non-inverting input of the comparator will drop below 2.5V causing its output (low line) to go low.

2.10 Built-in test overview

BUILT-IN TEST is used to test and exercise various circuits and components on the digital board, analog board and A/D converter board. The Built-in tests are listed in Table 2-7. Many of the tests are actual pass/fail type tests, while others are circuit exercises that are used for subsequent tests. Each Built-in test can be run manually. After a test is manually run, operation is "frozen" to allow the technician to troubleshoot the circuit. Detailed troubleshooting documentation for each Built-in test is provided in paragraph 2.11.

Table 2-7
Built-in test summary

Test	Circuit tested/exercised
100 Series	
100.1	Memory: EPROM
101 Series	
101.1	Memory: RAM
102 Series	
102.1	Memory: E^2PROM
103 Series	Digital I/O:
103.1 - 103.4	Digital Output Bits 1-4
103.5	Digital Input
104 Series	IEEE-488 Bus:
104.1	Handshake
104.2	Data
105 Series	Triggers:
105.1 - 105.6	System Trigger Bus
105.7	External Trigger /Voltmeter Complete
105.8	Group Execute Trigger (GET)
105.11 - 105.18	Trigger Shorts
200 Series	A/D Converter:
200.1	A/D Communication
200.2	A/D Noise
201 Series	Calibration:
201.1	Test Cal Zero
201.2	7V Reference
201.3	1.75V Reference

Table 2-7(cont.)
Built-in test summary

Test	Circuit tested/exercised
202 Series	Integration:
202.1	Baseline (for test 202.2)
202.2	Integration Period Bit I15
202.3	Baseline (for test 202.4)
202.4	Integration Period Bit I14
202.5	Baseline (for test 202.6)
202.6	Integration Period Bit I13
202.7	Baseline (for test 202.8)
202.8	Integration Period Bit I12
202.9	Baseline (for test 202.10)
202.10	Integration Period Bit I11
202.11	Baseline (for Test 202.12)
202.12	Integration Period Bit I10
202.13	Baseline (for test 202.13)
202.14	Integration Period Bit I9
202.15	Baseline (for test 202.16)
202.16	Integration Period Bit I8
202.17	Baseline (for test 202.18)
202.18	Integration Period Bit I7
202.19	Baseline (for test 202.20)
202.20	Integration Period Bit I6
202.21	Baseline (for test 202.22)
202.22	Integration Period Bit I5
202.23	Baseline (for test 202.24)
202.24	Integration Period Bit I4
202.25	Baseline (for test 202.26)
202.26	Integration Period Bit I3
202.27	Baseline (for test 202.27)
202.28	Integration Period Bit I2
202.29	Baseline (for test 202.30)
202.30	Integration Period Bit I1
202.31	Baseline (for test 202.32)
202.32	Integration Period Bit I0
300 Series	A/D Multiplexer (MUX), A/D Buffer:
300.1	7V Reference, X1 Gain
300.2	1.75V Reference, X5 Gain
300.3	0V Reference, X50 Gain
301 Series	Temperature Sensor:
301.1	Temperature Sensor
302 Series	A/D Ground Multiplexer:
302.1	Signal Zero to A/D Ground
302.2	Reference LO to A/D Ground
302.3	Ohms LO to A/D Ground
302.4	Divider LO to A/D Ground

Table 2-7(cont.)
Built-in test summary

Test	Circuit tested/exercised
303 Series	Input Buffer:
303.1	Input Buffer
304 Series	Open-circuit Ohms:
304.1	Open-circuit Ohms
304.2	2MΩ Open-circuit Ohms
305 Series	20V Range Multiplexer:
305.1	20V Range MUX Reference HI
305.2	20V Range MUX Reference LO
305.3	20V Range MUX Zero
305.4	20V Range MUX Signal
306 Series	Ohms:
306.1	9.6μA Ohms Source
306.2	1.92μA Ohms Source
306.3	High Ohms Voltage Source
307 Series	100:1 Input Divider:
307.1	/100 Input Divider
308 Seres	Overload:
308.1	Overload HI
308.2	Overload Ohms
308.3	2MΩ Overload Ohms
400 Series	Calibration/Frequency Compensation DAC:
400.1	-4.36V DAC Output
400.2	-2.15V DAC Output
400.3	0V DAC Output
400.4	+2.33V DAC Output
400.5	+4.48V DAC Output
401 Series	Regulator:
401.1	Regulator
402 Series	Switching:
402.1	Frequency Switch
403 Series	Signal Switching:
403.1	Ground Switch
404 Series	Absolute Value (X1 Gain):
404.1	-Full Scale DAC Output
404.2	-Half Scale DAC Output
404.3	Zero DAC Output
404.4	+Half Scale DAC Output
404.5	+Full Scale DAC Output

Table 2-7(cont.)
Built-in test summary

Test	Circuit tested/exercised
405 Series	Absolute Value (X10 Gain):
405.1	Gain Comparison (Large +DAC Output)
405.2	Gain Comparison (Non-inverting)
405.3	Gain Comparison (Small +DAC Output)
405.4	Gain Comparison (Non-inverting)
405.5	Gain Comparison (Small -DAC Output)
405.6	Gain Comparison (Inverting)
405.7	Gain Comparison (Large -DAC Output)
405.8	Gain Comparison (Inverting)
406 Series	Sample and Hold Circuit:
406.1	Measure DAC Output (for test 406.3)
406.2	Sample and Hold Output (-1.13V)
406.3	Read Sample and Hold (for test 406.6)
406.4	Read DAC Output (for test 406.6)
406.5	Sample and Hold Output (-0.01V)
406.6	Sample and Hold Voltage Comparisons
407 Series	Front End X1, /100, /500:
407.1	2V Range
407.2	200V Range
407.3	750V Range
408 Series	/200 Frequency Compensation:
408.1	Circuit Setup (for test 408.2)
408.2	Step Response (for test 408.3)
408.3	Setup (for test 408.5) and Step Reading (for test 408.6)
408.4	Same as Test 408.3 but no measurement.
408.5	Step Response (for test 408.6)
408.6	/200 Frequency Compensation
409 Series	/750 Frequency Compensation:
409.1	Circuit Setup (for test 409.2)
409.2	Step Response (for test 409.3)
409.3	Setup (for test 409.5) and Step Reading (for test 409.6)
409.4	Same as Test 409.3 but no measurement.
409.5	Step Response (for test 409.6)
409.6	/750 Frequency Compensation

Table 2-7(cont.)
Built-in test summary

Test	Circuit tested/exercised
410 Series	True RMS Converter:
410.1	True RMS Converter
411 Series	Filters:
411.1	True RMS Filter
411.2	Full-wave Rectifier Filter
412 Series	Frequency:
412.1	Frequency, Phase 1
412.2	Frequency, Phase 2
412.3	Frequency, Phase 3
412.4	Frequency, Phase 4
412.5	Frequency, Phase 5
412.6	Frequency, Phase 6
412.7	Frequency, Phase 7
412.8	Frequency, Phase 8
412.9	Frequency, Phase 9
412.10	Frequency, Phase 10
500 Series	Amps/LO Ohms:
500.1	96µA Ohms/200µA DCA Range
500.2	960µA Ohms/2mA DCA Range
500.3	7.2mA Ohms/2mA DCA Range
500.4	20mA DCA Range
500.5	Baseline Reading (for tests 500.6 and 500.7)
500.6	200mA DCA Range
500.7	2A DCA Range
501 Series	Amps Protection:
501.1	Amps Protection
501.2	Amps Bootstrap
502 Series	ACA Switch
502.1	AC Amps Switch
600 Series	Ohms Sense:
600.1	Ohms Sense HI
600.2	Ohms Sense LO

2.10.1 Using Built-In Test

There are several ways to run the Built-In Test, including:

1. Run the AUTOMATIC Built-In-Test as explained in paragraph 2.10.2, and note the first (lowest numbered) test that has failed. Always address the lowest numbered test failure first because that failure could cause subsequent tests to fail.
2. Familiarize yourself with the failed circuit. Documentation for the Built-In Tests is provided in paragraph 2.11. Be sure to read the documentation for the complete series. For example, if test 202.4 fails, read the documentation for all 202 series tests.
3. Manually run the test that failed as explained in paragraph 2.10.3. Keep in mind that many of the pass/fail type tests require that one or more circuit exercise tests be run first. Using the manual step looping mode will "freeze" instrument operation after a test is run.
4. After manually running the test, use the test documentation and your troubleshooting expertise to locate the problem.
5. After repairing the instrument, start again at step 1 to check the integrity of the repair and to see if there are any other failures.

2.10.2 AUTOMATIC Testing

1. Display the MAIN MENU by pressing the MENU key.
2. Select TEST, and press ENTER to display the SELF-TEST MENU.
3. Place the cursor on BUILT-IN-TEST, and press ENTER to display the following menu:

   BUILT-IN TEST
   AUTOMATIC MANUAL

4. Place the cursor on AUTOMATIC, and press ENTER. The following prompt is displayed:

   TEST BANK
   FULL OPEN-INPUTS HI-TO-AMPS

   Select FULL then YES or NO repeat mode.

   In the non-repeat mode (NO), the testing process stops after all tests have been performed one time. In the continuous repeat mode (YES), the testing process loops around and repeats indefinitely until the EXIT key is pressed to stop the tests.

5. Place the cursor on the desired repeat mode selection (NO or YES), and press ENTER to start the testing process. The instrument displays the number of the test being run to the right, and the number to the left is the measured value. If a failure occurs, an asterisk (*) appears at the right hand end of the display and remains on for the remainder of the tests.
6. If the non-repeat mode is selected, the testing process automatically stops when all the tests have been performed. If the continuous repeat mode is selected, you will have to manually stop the testing process by pressing EXIT. When EXIT is pressed, all the tests in a series already started will be allowed to finish.

   When the testing process stops, the following message is displayed:

   All tests complete *
   Press ENTER to review or EXIT

   The asterisk (*) is only displayed if a failure occurs.

7. If all the tests passed (no asterisk displayed), use the EXIT key to back out of the menu structure. Otherwise, press ENTER to display the test number of the first failure. You can display any additional failures by using the left and right arrow keys. With a failed test displayed, pressing the INFO key provides an abbreviated description of the failure. Paragraph 2.11 provides detailed documentation for troubleshooting the defective circuit. When finished, use EXIT to back out of the menu structure.

2.10.3 MANUAL Testing

1. Display the MAIN MENU by pressing the MENU key.
2. Select TEST, and press ENTER to display the SELF-TEST MENU.
3. Place the cursor on BUILT-IN-TEST, and press ENTER to display the following menu:

   BUILT-IN TEST
   AUTOMATIC MANUAL

4. Select MANUAL, and press ENTER to display the currently selected test series number, for example:

   Test number: 100

   This test number indicates that the 100 series tests can be performed. In this case there is only one test, test 100.1.

5. Use the left or right arrow keys to display the desired test series number. For example, if you wish to run test 202.5, display the series 202 test number.

   Test number: 202

6. With the desired test series number displayed, press ENTER. The following menu displayed:

   SELECT LOOPING
   SINGLE CONTINUOUS STEP

7. Place the cursor on the desired looping selection, and press ENTER.

A. SINGLE looping performs all the tests in the specified series. The instrument displays the number of the test being run. If a failure occurs, an asterisk (*) appears at the right-hand end of the display and remains on for the remainder of the tests in the series. This testing process automatically stops after the last test in the series is completed. This test process can also be stopped by pressing EXIT. When EXIT is pressed, any test in process will be allowed to finish before aborting the testing process.

B. CONTINUOUS looping continuously repeats all the tests in the specified series until the testing process is manually stopped. If a failure occurs, an asterisk (*) appears at the right-hand end of the display and remains on for the remainder of the tests in the series. This test process can be stopped by pressing EXIT. When EXIT is pressed, any test in process will be allowed to finish before aborting the testing process.

C. STEP looping is used to perform one test at a time. Each press of the ENTER key performs the displayed test. If a failure occurs, an asterisk (*) appears at the right hand end of the display and remains on for the remainder of the tests in the series. The instrument automatically aborts the testing process after the last test in the series is run. If you do not wish to run all the tests in the series, simply press EXIT after the desired test is run. Again, the number to the left is the measured value, and the number to the right is the test number.

8. After the testing process is stopped, the following message is displayed:

   All tests complete *
   Press ENTER to review or EXIT

   The asterisk (*) is displayed only if a failure occurs.

9. In the event of no test failures, press any key to return to the BUILT-IN TEST menu. If you wish to run more tests, repeat steps 4 through 8.

   In the event of a failure, press ENTER to display the first test that failed. Other test failures can be displayed by using the left and right arrow keys. The INFO key can be used to provide a brief summary of each displayed test failure. Paragraph 2.11 provides detailed documentation for troubleshooting the defective circuit. When finished, press EXIT to return to the BUILT-IN TEST menu. If you wish to run more tests, repeat steps 4 through 8.

10. When finished with BUILT-IN TEST, use the EXIT key to back out of the menu structure.

2.11 Built-In test documentation

The following paragraphs provide a detailed description of each Built-In Test. Refer to paragraph 2.10 for basic information on how to use the Built-In Tests. The following documentation is provided for each Built-In Test:

1. Test Type: Some tests are pass/fail type tests while others are circuit exercises that are used for subsequent tests.
2. Fault Message: For pass/fail type tests, a message is provided to explain the cause of the failure. The fault message may be displayed during test failure analysis by pressing the INFO key.
3. Description: Provides a description of the circuit being tested.
4. Drawing Reference: Identifies the component layout drawing associated with the described circuitry. Component layout drawings are located at the end of Section 4.
5. Components: When appropriate, possible defective components and/or circuits are listed. It is left to the expertise of the repair technician to pin-point the problem.
6. Shift Register Bit Patterns: For tests starting with 200.1, the logic states for the R1_STB, R2_STB, MUX_STB, and AD_STB control shift registers are provided. After one of these tests is manually run, you can check the registers for the correct logic levels. Functional descriptions for the register bits are provided where applicable.

2.11.1 Memory element tests

These tests check the EPROM, RAM, and EEPROM memory circuits of the Model 2002.

Test 100.1 — EPROM

Type Pass/fail

Fault message `Checksum error`

Description All ROM bytes (except checksum bytes) are read, a checksum is calculated and compared to the stored checksum. Failure of this test indicates that one or more ROM locations cannot be read properly.

Components U637, U638 and associated logic.

Test 101.1 — RAM

Type Pass/Fail

Fault message `Address bus open/short`

Description This is an abbreviated version of power-on RAM testing. Memory locations are written to and then read back. It is highly unlikely that this built-in-test will fail. A unit with faulty memory will probably fail the power-on memory test or will lock up intermittently.

Drawing reference Digital Board; 2002-140

Components U635, U636 and associated logic.

Test 101.2 — RAM

Type Pass/Fail

Fault message `Pattern test failure`

Description A pattern of bits is written to each RAM location and then read back. This test performs a more rigorous check of RAM elements.

Components U635, U636, and associated logic.

Test 102.1 — EEPROM

Type Pass/Fail

Fault message `Read/write EEPROM failure`

Description An attempt is made to read a byte of information from the 24164 configuration EEPROM (U632, U633, U634), and an acknowledgment signal is verified. This is a hardware test only, and it does not verify the validity of configuration information stored in EEPROM.

Drawing reference Digital Board; 2002-140

Components U632, U633, U634, and associated circuitry.

2.11.2 Digital I/O tests

The Digital I/O port on the Model 2002 consists of four open collector outputs and one TTL-level input. Outputs originate from Port A of the 68302 microprocessor (U631), lines PA4 through PA7. PA4 drives Output #1, PA5 drives Output #2, PA6 drives Output #3 and PA7 drives Output #4. These signals are buffered by a 2596A open collector driver (U612).

The following table summarizes how the lines of Port A of the microprocessor and the IN/OUT designations of the 2596A driver correspond to the digital output lines:

Digital Output	68302 (U631) Port A	2596A (U612) IN, OUT
Output #1	PA4	IN4, OUT4
Output #2	PA5	IN3, OUT3
Output #3	PA6	IN1, OUT1
Output #4	PA7	IN2, OUT2

The single Digital Input is buffered by protection circuitry (CR619, CR626, R610, R733) and read by the 68302 at PB8.

NOTE

Digital I/O tests may or may not fail depending on the firmware revision of the instrument.

Test 103.1 through 103.4 — Digital output

Type Pass/Fail

Fault message `Output <n> open/short failure` (<n> = 1 to 4)

Description These tests make use of the fact that the 68302 MPU (U631) Port A registers are bidirectional even though in normal use they are programmed only as outputs.

Diodes and resistors are connected around U612 so that OUT1 feeds back to PA5, OUT2 feeds back to PA6, OUT3 to PA7 and OUT4 to PA4. (Note that signal numbers are scrambled at the 2596 open collector driver, U612. The numbers in the above description refer to the Digital output signal numbers, not to the numbers on U612.)

During test 103.1, PA4 and PA6 are programmed as outputs, and PA5 and PA7 are programmed as inputs. As PA4 (OUT1) is toggled high and low, the signal is verified at PA5.

During test 103.2, PA5 and PA7 are programmed as outputs, and PA4 and PA6 are programmed as inputs. As PA5 (OUT2) is toggled high and low, the signal is verified at PA6.

Tests 103.3 and 103.4 test OUT3 and OUT4 in a manner similar to the above.

Drawing reference Digital Board; 2002-140

Components U631 PA4-PA7, U612, and associated components.

Test 103.5 — Digital input

Type Pass/Fail

Fault message `Input continuity failure`

Description This test only verifies that the digital input signal is pulled high at PB8 of the microprocessor (U631). Success of this test does not guarantee complete functionality of the input port.

Drawing reference Digital Board; 2002-140

Components U631 PB8 and associated circuitry.

2.11.3 IEEE-488 bus tests

The IEEE-488 interface in the Model 2002 consists of the 9914 GPIA chip (U622) and the 75160 (U621) and 75161 (U623) bus drivers. The 75160 buffers the data lines (DIO1-DIO8), and the 75161 buffers the bus handshake lines and other control signals. The circuitry to test these components is contained in the 5064 ASIC (U618).

Test 104.1 — Handshake

Type Pass/Fail

Fault message `IEEE-488 handshake failure`

Description Circuitry in the 5064 (U618) is set up to simulate an IEEE-488 handshake. Bytes are written to the 9914 (U622) Data Out register, and the interrupt status register is checked to verify that a Byte-Out handshake is completed.

These tests verify the basic functionality of the 9914, 75161 and the handshake portion of the ASIC (Signals BNRFD, BNDAC, and BDAV).

Drawing reference Digital Board; 2002-140

Components U618, U622 and U623.

Test 104.2 — Data

Type Pass/Fail

Fault message `IEEE-488 data failure`

Description For this test, bytes are written to the 9914 Data Out register (U622) to drive and release bus line DIO1. The state of this signal is verified at the 68302 (U631) through PB0 (BITB1). This test verifies the basic functionality of the 9914 and 75160 (U621).

Drawing reference Digital Board; 2002-140

Components U612 and U622

2.11.4 Triggers tests

Triggers are controlled by the 5064 ASIC (U618). This component has seven trigger outputs (STO1-STO7) and eight trigger inputs (STI1-STI8). Lines STI1-STI6 and STO1-STO6 are used to control the system trigger bus, line STO7 is used for Meter Complete, and line STI7 is used for External Trigger. STI8 is connected to the Group Execute Trigger signal (GET) of the 9914 IEEE-488 bus controller (U622).

Test 105.1 through 105.6 — System trigger bus

Type Pass/Fail

Fault message `Trig link channel <n> open` (<n> = 1 to 6)

Description System trigger inputs are normally pulled up to 5V through the protection diodes and 5.1kΩ resistors (CR611-CR616, R648-R650 and R655-R657). The Model 2002 can generate a trigger on any of the six trigger bus inputs by turning on the appropriate FET (Q602-Q607). These FETs are controlled by system trigger outputs (STO1-STO6) of the 5064 ASIC (U618).

In test 105.1, STI1 is set up as the trigger input. The trigger 1 FET (Q606) is then turned on and off through STO1, and it is verified that this trips the trigger circuitry in the ASIC. This test is then repeated for trigger 2 through 6 for tests 105.2 through 105.6. Success indicates proper operation of the trigger bus.

Drawing reference Digital Board; 2002-140

Components ASIC (U618), FETs (Q602-Q607), diodes (CR611-CR616), and 5.1kΩ components resistors (R648-R650, R655-R657).

Test 105.7 — External Trigger/Meter Complete

Type Pass/Fail

Fault message `Shorted VMC/EXT trigger`

Description This test is similar to System Trigger tests 105.1 through 105.6 except that there is no internal connection between External Trigger and Meter Complete. Consequently, the meaning of a failure is reversed from that of the previous trigger tests. A failure is registered if a trigger does occur. A failure indicates that a short exists between External Trigger and Meter Complete.

An alternate way to test these triggers is to externally connect a BNC cable from External Trigger to Meter Complete. When test 105.7 is run, the short should cause the test to fail. If it does not, a problem in the signal path exists.

Drawing reference Digital Board; 2002-140

Components External Trigger/Meter Complete signal paths.

Test 105.8 — Group Execute Trigger (GET)

Type Pass/Fail

Fault message `Open IEEE-488 GET`

Description Trigger 8 (STI8) is set up as an input, and the 9914 (U622) is then programmed to generate a GET signal.

Drawing reference Digital Board; 2002-140

Components U618 and U622.

Test 105.11 through 105.18 — Trigger shorts

Type Pass/Fail

Fault message None

Description In test 105.11, STI1 is programmed as the trigger input. Each of the other triggers (STI2 through STI7 and GET) is programmed to toggle in sequence. If a trigger is detected at STI1, a short is indicated and the test fails. The test is repeated for STI2 through STI8 in tests 105.12 through 105.18.

Ordinarily, Built-In-Tests should be run with no external connections. However, the Trigger Shorts tests may be used to verify proper operation at the external trigger bus connector (J1029, J1030). For example, by shorting pins 1 and 2, tests 105.11 and 105.12 should fail, indicating that the short was detected between system trigger 1 and system trigger 2.

Drawing reference Digital Board; 2002-140

Components J1029, J1030, and associated circuitry.

2.11.5 A/D converter tests

Control registers

There are four data words used to configure and control the instrument. The AD_STB and MUX_STB data words are used to control the A/D converter, multiplexing, and the input gain configuration. The R1_STB data word is used to control the DCV and ohms configuration, and the R2_STB data word is used to control the ACV configuration. Each data word is generated in the digital section and is passed to the four sets of control shift registers.

The four control registers are made up of the following ICs:

AD_STB:	U811, U810, U809
MUX_STB:	U206, U207
R1_STB:	U203, U222, U224
R2_STB:	U400, U406, U411, U432

The description of each test provides a summary of bit patterns for each of the registers and identifies IC terminals.

Test 200.1 — A/D converter communication

Type Pass/Fail

Fault message `No A/D communication`

Description The instrument is set up in default condition as described in the note above. U222 is set up to switch common through R259 and S1 pin 4 input to the A/D buffer, U226. U226 is set up for X1 gain through U227 pin 2 to 3 with /X1 pin 1 low. Also, common is switched through R312 and U242 pins 2 to 3, through R311 and to pin 3 of U253. U253 is the buffer for ADGND. ADGND is routed to A/D in through the parallel combination of R285 and R286. Common is the input to A/D_IN. The A/D is triggered until the CB (Charge Balance) counts from triggered readings are the same value, the value is stored and compared to a zero by design CB value. FS (Final Slope) counts are also stored. The counts that are used for the limits are derived from input signal levels, current values to the integrator, integration time, and the clock for U816. The count values are raw counts and are required for the 200 series tests. Once proper operation of the A/D can be determined, the software will convert the counts into voltage values.

If the A/D cannot make this measurement, all BIT tests will fail.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components U816, analog-to-digital conversion circuitry.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00010111	—U809— 01101111	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 200.2 — A/D noise

Type Pass/Fail

Fault message `Signal conditioning noisy`

Description This test uses the same circuit setup as test 200.1. The A/D is triggered for 10 readings and a minimum/maximum comparison is done for 50 counts or less. Failing this test indicates A/D buffer noise or A/D converter circuit noise.

Drawing reference Analog Board; 2002-140
A/D Converter; 2002-160

Components A/D buffer or converter noise, power supply or reference supply noise.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00010111	—U809— 01101111	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 201.1 — Test cal zero

Type Pass/Fail

Fault message None

Description U222 is set up to switch common through R259 and S1 pin 4 input to the A/D buffer U226. U226 is set up for X1 gain through U227 pin 2 to 3 with /X1 pin 1 low. Also, common is switched through R312 and U242 pins 2 to 3, through R311 and to pin 3 of U253. U253 is the buffer for ADGND. ADGND is routed to A/D_IN through the parallel combination of R285 and R286. Common is the input to A/D_IN. Zero reading is acquired and stored for Testcal.

This test is performed by measuring for 0V at A/D_IN.

Drawing reference Analog Board; 2002-100

Components Switching paths for signals and A/D converter.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00010111	—U809— 01101111	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 201.2 — 7 Volt reference

Type Pass/Fail

Fault message Cannot measure 7V at A/D

Description The 7V reference REFHI generated by U219 and associated circuitry is connected to buffer U255 to generate REFBUF signal. REFBUF is switched through R263 and U222 pin 5 to U226. U226 is set up for X1 gain through U227 pin 2 to 3 with /X1 pin 1 low. R274 is the feedback path of U226. REFLO is switched through R310 and U242 pins 7 to 6, through R311, and to pin 3 of U253. U253 is the buffer for ADGND. ADGND buffer with REFLO signal is connected to the bottom of the parallel combination of R285 and R286. A/D_IN will be the difference voltage of REFHI (REFBUF) and REFLO (ADGND). The A/D is triggered and the REFHI reading in counts is acquired and stored for Testcal. REFHI counts are compared to a by design value of counts.

Drawing reference Analog Board; 2002-100

Components Reference circuit, A/D converter, and the switching paths for the signals.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00010111	—U809— 01101111	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 201.3 — 1.75 Volt Reference

Type Pass/Fail

Fault message `Cannot measure 1.75V at A/D`

Description The 7V reference REFHI generated by U219 and associated circuitry is connected to buffer U254. The output of U254 is connected to U230. The 7V reference is switched at 600Hz through U230. U235 and buffer U241 along with the 25% duty cycle of the 600Hz clock signal, generate the 1.75 volt reference (2VREF). 2VREF is switched through R260 and U222 pin 6 to U226. U226 is set up for X1 gain through U227 pin 2 to 3 with /X1 pin 1 low. REFLO is switched through R310 and U242 pins 7 to 6, through R311, and to pin 3 of U253. U253 is the buffer for ADGND. ADGND buffer with REFLO signal is connected to the bottom of the parallel combination of R285 and R286. A/D_IN will be the difference voltage of 2VREF and REFLO (ADGND). The A/D is triggered and the 2VREF reading in counts is acquired. A calculation is made with the values stored in 201.1, 201.2 to determine the proper operation and linearity of the A/D converter.

Drawing reference Analog Board; 2002-100

Components Reference circuit, the A/D converter, or the signal paths routing the values to components the A/D.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00010111	—U809— 01101111	AD_STB
		—U206— 01110000	—U207— 01010111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.6 Integration tests

The 202 Integration series of tests check the selectable integration times of the ASIC U816. This test is accomplished by loading the shift registers U809 and U810 with data words that will select the I15 through I0 inputs to U816 one at a time. The I15 through I0 inputs to U816 control the length of the integration time. The exception is that the I0 input will always be set high due to internal component requirements. A zero level is applied to the A/D and integrated for each integration time for a baseline value. Zero baseline values are acquired during the odd-numbered tests, and the values are used for a comparison in the even-number tests. The 7V reference is applied to the A/D and integrated for each integration time during the even-numbered tests. The 7V reference is compared to the zero, and the result is a number of counts that is relative to the length of the integration time. Each test will have an integration time that is smaller due to selecting a lower order I, and the counts will then be a division of the first value acquired. The circuit setup for zero and 7V reference will be in tests 202.1 and 202.2. The remaining tests will refer to the first two tests. HIGH and LOW logic levels refer to +5V and 0V respectively.

Test 202.1 — Baseline for test 202.2

Type Circuit Exercise

Fault message None

Description Integration time is set up with I15 and I0 high (longest integration time), all other I lines low. U222 is set up to switch common through R259 and S1 pin 4 input to the A/D buffer U226. U226 is set up for X1 gain through U227 pin 2 to 3 with /X1 pin 1 low. Also, common is switched through R312 and U242 pins 2 to 3, through R311 and to pin 3 of U253. U253 is the buffer for ADGND. ADGND is routed to A/D_IN through the parallel combination of R285 and R286. Common is the input to A/D_IN. A zero reading is acquired and stored as baseline value for test 202.2.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 10000000	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

202.2 — Integration period bit I15

Type Pass/Fail

Fault message `Integration period bit I15`

Description Integration time is set up with I15 and I0 high (longest integration time) and all other I lines low. The 7 volt reference REFHI generated by U219 and associated circuitry is connected to buffer U255 to generate REFBUF signal. REFBUF is switched through R263 and U222 pin 5 to U226. U226 is set up for X1 gain through U227 pin 2 to 3 with /X1 pin 1 low. R274 is the feedback path of U226. REFLO is switched through R310 and U242 pins 7 to 6, through R311, and to pin 3 of U253. U253 is the buffer for ADGND. ADGND buffer with REFLO signal is connected to the bottom of the parallel combination of R285 and R286. A/D_IN will be the difference voltage of REFHI (REFBUF) and REFLO (ADGND). The A/D is triggered and the REFHI reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines, or components U816.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	10000000	00000001	
		—U206—	—U207—	MUX_STB
		01110000	00110111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.3 — Baseline for test 202.4

Type Circuit Exercise

Fault message None

Description Integration time is set up with I14 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.4.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	01000000	00000001	
		—U206—	—U207—	MUX_STB
		01110000	00001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.4 — Integration period bit I14

Type Pass/Fail

Fault message `Integration period bit I14`

Description Integration time is set up with I14 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Components Shift registers that set up the I15 through I0 levels, open or shorted lines components associated with the I lines, or U816.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	01000000	00000001	
		—U206—	—U207—	MUX_STB
		01110000	00110111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.5 — Baseline for test 202.6

Type Circuit Exercise

Fault message None

Description Integration time is set up with I13 and I0 high and all other I lines low. This test used the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.6.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00100000	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.6 — Integration period bit I13

Type Pass/Fail

Fault message `Integration period bit I13`

Description Integration time is set up with I13 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines components associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00100000	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.7 — Baseline for test 202.8

Type Circuit Exercise

Fault message None

Description Integration time is set up with I12 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.8.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00010000	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.8 — Integration period bit I12

Type Pass/Fail

Fault message `Integration period bit I12`

Description Integration time is set up with I12 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines components associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00010000	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.9 — Baseline for test 202.10

Type Circuit Exercise

Fault message None

Description Integration time is set up with I11 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.10.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00001000	00000001	
		—U206—	—U207—	MUX_STB
		01110000	00001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.10 — Integration period bit I11

Type Pass/Fail

Fault message `Integration period bit I11`

Description Integration time is set up with I11 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines components associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00001000	00000001	
		—U206—	—U207—	MUX_STB
		01110000	00110111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.11 — Baseline for test 202.12

Type Circuit Exercise

Fault message None

Description Integration time is set up with I10 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.12.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000100	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.12 — Integration period bit I10

Type Pass/Fail

Fault message `Integration period bit I10`

Description Integration time is set up with I10 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000100	00000001	
		—U206—	—U207—	MUX_STB
		01110000	00110111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.13 — Baseline for test 202.14

Type Circuit Exercise

Fault message None

Description Integration time is set up with I9 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.14.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000010	00000001	
		—U206—	—U207—	MUX_STB
		01110000	00001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.14 — Integration period bit I9

Type Pass/Fail

Fault message `Integration period bit I9`

Description Integration time is set up with I9 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000100	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.15 — Baseline for test 202.16

Type Circuit Exercise

Fault message None

Description Integration time is set up with I8 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.16.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000001	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.16 — Integration period bit I8

Type Pass/Fail

Fault message `Integration period bit I8`

Description Integration time is set up with I8 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns .

Bit pattern*				Register
	—U811— 00001101	—U810— 00000001	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.17 — Baseline for test 202.18

Type Circuit Exercise

Fault message None

Description Integration time is set up with I7 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.18.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 10000001	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.18 — Integration period bit I7

Type Pass/Fail

Fault message `Integration period bit I7`

Description Integration time is set up with I7 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 10000001	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.19 — Baseline for test 202.20

Type Circuit Exercise

Fault message None

Description Integration time is set up with I6 and I0 high and all other I lines low. This test uses the same circuit setup as 202.1. Zero reading is acquired and stored as baseline value for test 202.20.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 01000001	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.20 — Integration period bit I6

Type Pass/Fail

Fault message `Integration period bit I6`

Description Integration time is set up with I6 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 01000001	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.21 — Baseline for test 202.22

Type Circuit Exercise

Fault message None

Description Integration time is set up with I5 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.22.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 00100001	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.22 — Integration period bit I5

Type Pass/Fail

Fault message `Integration period bit I5`

Description Integration time is set up with I5 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns .

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 00100001	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.23 — Baseline for test 202.24

Type Circuit Exercise

Fault message None

Description Integration time is set up with I4 and I0 high and all other I lines low. This test uses the same circuit setup as 202.1. A zero reading is acquired and stored as a baseline value for test 202.24.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 00010001	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1
7	6	5	4	3	2	1	0
6	5	4	3	2	1	0	1
5	4	3	2	1	0	1	2

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.24 — Integration period bit I4

Type Pass/Fail

Fault message `Integration period bit I4`

Description Integration time is set up with I4 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000000	00010001	
		—U206—	—U207—	MUX_STB
		01110000	00110111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.25 — Baseline for test 202.26

Type Circuit Exercise

Fault message None

Description Integration time is set up with I3 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.26.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000000	00001001	
		—U206—	—U207—	MUX_STB
		01110000	00001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.26 — Integration period bit I3

Type Pass/Fail

Fault message `Integration period bit I3`

Description Integration time is set up with I3 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 00001001	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.27 — Baseline for 202.28

Type Circuit Exercise

Fault message None

Description Integration time is set up with I2 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.28.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000000	00000101	
		—U206—	—U207—	MUX_STB
		01110000	00001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.28 — Integration period bit I2

Type Pass/Fail

Fault message `Integration period bit I2`

Description Integration time is set up with I2 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000000	00000101	
		—U206—	—U207—	MUX_STB
		01110000	00110111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.29 — Baseline for test 202.30

Type Circuit Exercise

Fault message None

Description Integration time is set up with I1 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.30.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 00000011	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.30 — Integration period bit I1

Type Pass/Fail

Fault message `Integration period bit I1`

Description Integration time is set up with I1 and I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Components Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000000	00000011	
		—U206—	—U207—	MUX_STB
		01110000	00001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.31 — Baseline for test 202.32

Type Circuit Exercise

Fault message None

Description Integration time is set up with I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A zero reading is acquired and stored as baseline value for test 202.32.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000000	00000001	
		—U206—	—U207—	MUX_STB
		01110000	00001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 202.32 — Integration period bit I0

Type Pass/Fail

Fault message `Integration period bit I0`

Description Integration time is set up with I0 high and all other I lines low. This test uses the same circuit setup as test 202.1. A reading is acquired and compared to a calculated value based on the previous reading.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Shift registers that set up the I15 through I0 levels, open or shorted lines associated with the I lines, or U816.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000000	—U809— 00000001	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.7 A/D multiplexer tests

Test 300.1 — A/D MUX 7V reference, X1 A/D MUX gain

Type Pass/Fail

Fault message `A/D MUX 7V ref., x1 gain`

Description The 7V reference REFHI generated by U219 and associated circuitry is connected to buffer U255 with output REFBUF. REFBUF is switched through R263 and U222 pin 5 to pin 3 of U226. The X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low. R274 is in the feedback path of U226. The typical reference voltage is actually 7.2V.

Components U219, U226, U227 and associated circuitry.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 00110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 300.2 — A/D MUX 1.75V reference, X5 A/D MUX gain

Type Pass/Fail

Fault message `A/D MUX 1.75V ref., x5 gain`

Description The 7V reference REFHI generated by U219 and associated circuitry is connected to buffer U254. The output of U254 is connected to U230. The 7V reference is switched at 600Hz through U230. U235 and buffer U241, along with the 25% duty cycle of the 600Hz clock signal, generates the 1.75V reference (2VREF). 2VREF is switched through R260 and U222 pin 6 to U226. U226 is set up for X5 gain through U227 pin 10 to 11 with /X5 pin 9 low. R285 provides the feedback for U226 X5 gain. REFLO is switched through R310 and U242 pins 7 to 6, through R311, and to pin 3 of U253. U253 is the buffer for ADGND. ADGND buffer with REFLO signal is connected to the bottom of the parallel combination of R285 and R286. A/D_IN will be the difference voltage of 2VREF and REFLO (ADGND).

Drawing reference Analog Board; 2002-100

Components U219, U226, U235, U241, U254, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		10110000	01010111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 300.3 — A/D MUX 0V reference, X50 A/D MUX gain

Type Pass/Fail

Fault message `A/D MUX 0V ref., x50 gain`

Description U222 is set up to switch common through R259 and S1 pin 4 input to the A/D buffer U226. U226 is set up for X50 gain through U227 pin 15 to 14 with /X50 pin 16 low. R286 provides the feedback for U226 X50 gain. Also, common is switched through R312 and U242 pins 2 to 3, through R311 and to pin 3 of U253. U253 is the buffer for ADGND. ADGND is routed to A/D_IN through the parallel combination of R285 and R286. Common is the input to A/D_IN. Common is switched through R259 and U222 pin 4 to pin 3 of U226.

Drawing reference Analog Board; 2002-100

Components U222, U226, U227, U253, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		11010000	00001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.8 Temperature sensor test

Test 301.1 — Temperature sensor

Type Pass/Fail

Fault message `Temperature sensor`

Description The temperature sensor is U205. Pin 1 of U205 is switched through U222 pin 12 to pin 3 of U226. The X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low. R274 is in the feedback path of U226. The output of U205 is approximately 10mV per degree Celsius. For example, if the ambient temperature is 25°C, the output would be 250mV. The measurement at the A/D converter is therefore dependent on the ambient temperature. For the purpose of this test, the limits of the measurement are 400mV ±400mV. These limits account for the entire specified range of operating environments.

Drawing reference Analog Board; 2002-100

Components U205 and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.9 A/D converter ground multiplexer tests

Test 302.1 — Signal zero to ADGND

Type Pass/Fail

Fault message `Signal zero to ADGND`

Description Common is switched through R312 and U242 pins 2 to 3, through R311 and to pin 3 of U253. U253 is the buffer for ADGND. ADGND is routed to A/D in through the parallel combination of R285 and R286. To ensure stability of the circuit, the X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low. R274 is in the feedback path of U226. Pin 3 of U226 is also pulled to common through U222 pin 4 and R259.

Drawing reference Analog Board; 2002-100

Components U226, U227, U242, U253 and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 302.2 — REFLO to ADGND

Type Pass/Fail

Fault message `REFLO to ADGND`

Description REFLO is switched through R310 and U242 pins 7 to 6, through R311, and to pin 3 of U253. U253 is the buffer for ADGND. ADGND buffer with REFLO signal is connected to the bottom of the parallel combination of R285 and R286. To ensure stability of the circuit, X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low. R274 is in the feedback path of U226, and pin 3 of U226 is also pulled to common through U222 pin 4 and R259.

Drawing reference Analog Board; 2002-100

Components U222, U226, U242, U253 and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 00010111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 302.3 — Ohms LO to ADGND

Type Pass/Fail

Fault message `Ohms LO to ADGND`

Description Common is switched through the parallel combination of R313 and R314 and U242 pins 10 to 11, through R311 and to pin 3 of U253. U253 is the buffer for ADGND. ADGND buffer with Ohms LO signal is connected to the bottom of the parallel combination of R285 and R286. To ensure stability of the circuit, X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low. R274 is in the feedback path of U226. Pin 3 of U226 is also pulled to common through U222 pin 4 and R259.

Drawing reference Analog Board; 2002-100

Components U222, U226,U227, U242, U253, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 00011011	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 302.4 — Divider LO to ADGND

Type Pass/Fail

Fault message `Divider LO to ADGND`

Description Common is switched through U244 pins 11 to 10, through Q226 and Q227, through R311 and to pin 3 of U253. U253 is the buffer for ADGND. ADGND buffer with Divider LO signal is connected to the bottom of the parallel combination of R285 and R286. To ensure stability of the circuit, X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low. R274 is in the feedback path of U226. Pin 3 of U226 is also pulled to common through U222 pin 4 and R259.

Drawing reference Analog Board; 2002-100

Components U226, U227, U244, U253, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 00011110	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.10 Input buffer tests

Test 303.1 — Input buffer

Type Pass/Fail

Fault message `Input buffer`

Description This is the first test in the series that actually takes a measurement from the BUFFIN line by using the R1_STB default condition described earlier (see the discussion on default state in paragraph 2.11.5). Common is switched through U244 pin 11 to 10, through Q226, the lower leg of the R335, R339, R341, R346 series parallel combination, through Q242 to BUFFIN. BUFFIN goes into the bootstrap supply and U245 input buffer (including the U249 servo). The input buffer output, BSCOM, goes through Q207 and Q208 to pin 3 of U226. The A/D MUX gain is X1.

Drawing reference Analog Board; 2002-100

Components U226, U244, U245, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01100000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.11 Open-circuit ohms tests

Test 304.1 —Open-circuit ohms

Type Pass/Fail

Fault message `Open circuit ohms`

Description This is the first test in the series that uses the ohms source. Most of the 300 and 500 series tests that follow also use the ohms circuit.

The 7V reference REFHI signal generated by U219 and associated circuitry is connected to buffer U254 and U255, and the outputs of U254 and U255 are connected to U230. The 7V reference value from U254 is switched at 600Hz through U230 to capacitor C234. REFBUF is connected to the bottom of C22, and the 7V from C234 is switched to the top of C227 to create a 14V reference at OHMREFHI. The OHMREFHI to REFBUF lines are the isolated reference signals used to generate the current for the ohms source. The ohms source is generated by OHMREFHI, buffered by U231 and Q251 and is switched in with the /OHMA line at U220 and U223 to U233 pin 2. REFBUF is connected to U233 pin 3 through U232 pins 2 and 3. This circuit setup applies 7.2V across R270, 1kΩ resistor to generate 7.2 mA. In this test, there is no path provided for current to flow outside of the ohms source. In normal operation, the current would flow out of the ohms current source from the parallel path of Q211 and Q212, through Q213, R322,CR217, K201, R334, R342, and out of input HI through the resistor being measured and back to common. Current flow in this setup with no resistor connected is downward through the parallel path of Q211 and Q212, through CR213, VR204, and Q214 to common. The voltage drop across the combination of VR204 and Q214 is sensed by the path that routes through Q213, R322, CR217, K201, R334 and R342. This point is the HI input terminal to the DMM. This signal is then switched through the Q246, Q245, Q244 path to BUFFIN and then to A/D_IN as in test 303.1.

Drawing reference Analog Board; 2002-100

Components U219, U220, U223, U233, U254, U255, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01100000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 11110100	—U221— 01110111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 304.2 — 2MΩ open-circuit ohms

Type Pass/Fail

Fault message `2M open circuit ohms`

Description This test uses the same setup as test 304.1 except that U232 pin 10 to 11 connects the ohms reference feedback to U233 pin 3. R276 is used as a voltage divider, but R276 is not an integral part of this test. Q214 is off, and the ohms current flows through CR214 to LO.

Drawing reference Analog Board; 2002-100

Components U219, U220, U223, U233, U254, U255, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01100000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 11110100	—U221— 01111011	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.12 20V range multiplexer tests

Test 305.1 — 20V range multiplexer REFHI

Type Pass/Fail

Fault message `20V range MUX REFHI`

Description Q201 is turned on, allowing 7.2V REFHI to be applied to the R240 divider. Q203 is always on because its gate and source are tied together by R241. Since R240 divides by 2, 3.6V appears at U217 pin 3. Because U217 is a unity-gain buffer, 3.6V also appears at R261, and U222 switches pin 7 to pin 3 of U226. X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low. R274 is in the feedback path of U226.

Drawing reference Analog Board; 2002-100

Components Q201, U217, U222, U226, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110010	—U207— 01110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7654321	8	7654321	8	7654321	8	7654321

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 305.2 — 20V range multiplexer REFLO

Type Pass/Fail

Fault message `20V range MUX REFLO`

Description Q206 is turned on, allowing the 0V REFLO to be applied to the R240 divider. Q203 is always on because its gate and source are tied together by R241, and 0V appears at U217 pin 3. Since U217 is a unity-gain buffer, 0V also appears at R261, and U222 switches pin 7 to pin 3 of U226. X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low, and R274 is in the feedback path of U226.

Drawing reference Analog Board; 2002-100

Components U217, U222, U226, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110001	—U207— 01110111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 305.3 — 20V range multiplexer zero

Type Pass/Fail

Fault message `20V range MUX zero`

Description Q202 is turned on, allowing the 0V common to be applied to the R240 divider. Q203 is always on because its gate and source are tied together by R241. 0V appears at U217 pin 3. Since U217 is a unity gain buffer, 0V also appears at R261, and U222 switches pin 7 to pin 3 of U226. X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low. R274 is in the feedback path of U226.

Drawing reference Analog Board; 2002-100

Components Q202, U217, U222, U226, U227, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110100	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 305.4 — 20V range multiplexer signal

Type Pass/Fail

Fault message `20V range MUX signal`

Description The ohms source is in the same configuration as test 304.1 to create 6V at input HI, which is the HI input terminal to the DMM. This signal is then switched through the Q246, Q245, Q244 path to BUFFIN. Q205 is turned on so that the signal reaches R240, and Q203 is always on because its gate and source are tied together by R241. 3V appears at U217 pin 3. Since U217 is a unity-gain buffer, 3V also appears at R261, and U222 switches pin 7 to pin 3 of U226. X1 gain is achieved by closing U227 pins 2 to 3 with /X1 low, and R274 is in the feedback path of U226.

Drawing reference Analog Board; 2002-100

Components Q205, U217, U222, U226, U227, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01111000	—U207— 01101111	MUX_STB
	—U224— 00010111	—U203— 11110100	—U221— 01110111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.13 Ohms tests

Test 306.1 — 9.6µA ohms source

Type Pass/Fail

Fault message `9.6uA ohms source`

Description The 9.6µA ohms source is switched in with the /OHMD line at U220 and U223. U232 pin 2 to 3 connects REFBUF to U233 pin 3. (For a more detailed circuit setup description, see test 304.1.) 7.2V appears across R277. The 9.6µA current will all flow through Q211 (9.6µA through R291 does not produce a high enough voltage drop to turn Q212 on), Q213, R322, CR217, K201, R334 and R342. This point is the HI input terminal to the DMM. Q246, Q245, Q244, and Q242 are all on, allowing the current to be shunted around the 9.9MΩ leg of the input divider. The current then flows through the 100kΩ leg through Q226 and U244 pin 11 to pin 10 to common. The voltage at BUFFIN is applied to the input buffer to BSCOM and to U226, which is configured for X1 gain.

Drawing reference Analog Board; 2002-100

Components U220, U223, U226, U232, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01100000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 11010110	—U221— 11100111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 306.2 — 1.92µA ohms source

Type Pass/Fail

Fault message `1.92uA ohms source`

Description The 1.92µA ohms source is switched in with the /OHMD line at U223 and U220. U232 pin 10 to 11 switches in R276, basically forming a 5:1 divider between buffered OHMREFHI and REFBUF. 5.76V (relative to REFBUF) or 12.96V relative to common 2 appears at U233 pin 3. 14.4V - 12.96 = 1.44V appears across R277. (For a more detailed circuit description, see test 304.1.) The 1.92µA current will all flow through Q211 (1.92µA through R291 does not produce a high enough voltage drop to turn Q212 on), Q213, R322, CR217, K201,R334 and R342. This point is the HI input terminal to the DMM. Q246, Q245, Q244, and Q242 are all on, allowing the current to be shunted around the 9.9MΩ leg of the input divider. The current then flows through the 100kΩ leg through Q226 and U244 pin 11 to pin 10 to common. The voltage at BUFFIN is applied to the input buffer to BSCOM and to the A/D MUX, which is configured for X1 gain.

Drawing reference Analog Board; 2002-100

Components U220, U223, U232, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01100000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 11010110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 306.3 — High ohms voltage source

Type Pass/Fail

Fault message `High ohms voltage source`

Description The HIOHMSRC line at pin 7 of U231 is approximately 14.4V. This voltage is generated by the Ohms Reference U230 switching OHMREFHI onto C227 that is relative to REFBUF. HIOHMSRC is then switched through U244 pin 6 to 7, through Q226, through the 100kΩ leg of the input divider, and through Q242 to BUFFIN. The 20V range MUX signal path is now used. Q205 is turned on so that the signal reaches R204. Q203 is always on because its gate and source are tied together by R241. 7.2V appears at U217 pin 3. Since U217 is a unity gain buffer, 7.2V also appears at U222 pin 7. The U222 control lines are configured to switch the pin 7 input to the U222 output and to the A/D buffer in the X1 configuration.

Drawing reference Analog Board; 2002-100

Components U222, U231, U244, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01111000	—U207— 01101111	MUX_STB
	—U224— 00010111	—U203— 10101110	—U221— 11111100	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.14 100:1 input divider test

Test 307.1 — /100 input divider

Type Pass/Fail

Fault message `/100 input divider`

Description The 7.2 mA ohms source is switched in with the /OHMA line at U223. U232 pin 2 to 3 connects REFBUF to U233 pin 3. 7.2V appears across R270. (For a more detailed description of the ohms source setup, see test 304.1.) In this test, a 10MΩ path is provided for current to flow outside of the ohms source; however a 7.2 mA current through 10MΩ would produce a high voltage in excess of the open circuit ohms clamp. The majority of current flow is downward through the parallel path of Q211 and Q212, through CR213, VR204, and Q214 to common. The voltage drop across the combination of VR204 and Q214 is sensed by the path that routes through Q213, R322, CR217, K201,R334 and R342. This point is the HI input terminal to the DMM. The 10MΩ value described above is the series/parallel combination of R335, R339, R341, and R346. The 6V open-circuit ohms voltage is divided by 100 and is sensed through Q242 to BUFFIN, through the input buffer then to A/D_IN. The A/D MUX is configured for X50 gain.

Drawing reference Analog Board; 2002-100

Components U223, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 11000000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 01110111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.15 Overload tests

Test 308.1 — Overload HI

Type Pass/Fail

Fault message `Overload HI`

Description 2VREF is switched through U222 to U226. The A/D MUX is configured for X50 gain. This condition saturates U226 at the positive rail of about 13V. R231, R230, R229, and R228 form a divider that outputs 11V to pin 9 of comparator U214 and -11V to pin 6 of U214. A/D_IN, which is about at 13V, at pin 8 of comparator U214 results in /OVLD_HI being pulled low at about -15V. All of the OVLD lines are latched by U202, parallel loaded into U201, and serially input to the A/D board at J1026 pin 15. There is no A/D measurement for this test. The pass/fail criteria is based on the value of the /OVLD_HI bit.

Drawing reference Analog Board; 2002-100

Components U214, U222, U226, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 11010000	—U207— 01001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 308.2 — Overload ohms

Type Pass/Fail

Fault message `Overload OHMS`

Description The 9.6µA ohms source is switched in with the /OHMD line at U223 and U220. U232 pin 2 to 3 connects REFBUF to U233 pin 3. 7.2V appears across R277. (For a more detailed description of the circuit setup, see test 304.1.) In this test, there is no path provided for current to flow outside of the ohms source. Current flow is downward through the parallel path of Q211 and Q212, through CR213, VR204, and Q214 to common. U238 sees the open-circuit ohms voltage of about 6V at pin 3. It is used in a unity-gain configuration, and its output, which is the COMPLIANCE signal, goes to comparator U215. The 2M control line is pulled flow, turning on U232 pin 15 to 14 and switching R288 in parallel with R234. Along with R235, this divider places pin 5 of U215 at 4.5V. Since the COMPLIANCE line at 6V is more positive than 4.5V, the /OVLD_OHM line is pulled low at about -15V. All of the OVLD lines are latched by U202, parallel loaded into U201, and serially input to the A/D board at J1026 pin 15. There is no A/D measurement for this test. The pass/fail criteria is based on the value of the /OVLD_OHM bit.

Drawing reference Analog Board; 2002-100

Components U220, U223, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10101010	—U221— 11100111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 308.3 — 2M overload ohms

Type Pass/Fail

Fault message `2M Overload OHMS`

Description The 9.6µA ohms source is switched in with the /OHMD line at U223 and U220. U232 pin 2 to 3 connects REFBUF to U233 pin 3, and 7.2V appears across R277. (For a more detailed description of the circuit setup, see test 304.1.) In this test, there is no path provided for current to flow outside of the ohms source. Current flow is downward through the parallel path of Q211 and Q212, through CR213, VR204, and CR214 to common. U238 sees the open-circuit ohms voltage of about 6.6V at pin 3. It is used in a unity-gain configuration, and its output, which is the COMPLIANCE signal, goes to comparator U215. U232 pin 15 to 14 is open, and the divider in this case is made up of R235 and R234. This divider places pin 5 of U215 at 5.7V. Since the COMPLIANCE line at 6.6V is more positive than the 5.7V on /OVLD_OHM, the line is pulled low at about -15V. All of the OVLD lines are latched by U202, parallel loaded into U201, and serially input to the A/D board at J1026 pin 15. There is no A/D measurement for this test. The pass/fail criteria is based on the value of the /OVLD_OHM bit.

Drawing reference Analog Board; 2002-100

Components U220, U223, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10101010	—U221— 11101011	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.16 Calibration/frequency compensation DAC tests

Test 400.1 — DAC output set to -4.36V

Type Pass/Fail

Fault message `DAC output not -4.36V`

Description U433 (DAC B) and corresponding circuitry around U430 is configured by programming the TRIG bits on the DAC to produce -4.36V at PRECOMP+ (pin 1 of U430). This signal is routed through R491and U412 (DAC control line pulled low). This line, now called ACF, is selected by multiplexer U414 and is routed out pin 8. It goes to buffer U403, through R462 (where the line is now called ACV/A), through A/D MUX U222 to the U226 A/D buffer, which is set up for X1 gain.

Drawing reference Analog Board; 2002-100

Components U403, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011011	—U432— 00010111	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 400.2 — DAC output set to -2.15V

Type Pass/Fail

Fault message `DAC output not -2.15V`

Description This test is the same as test 400.1 except that U433 (DAC B) is configured to output -2.15V.

Drawing reference Analog Board; 2002-100

Components U403, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011011	—U432— 10001100	—U411— 11111011	—U406— 00001100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 400.3 — DAC output set to 0V

Type Pass/Fail

Fault message `DAC output not 0.001V`

Description This test is the same as test 400.1 except that U433 (DAC B) is configured for 0V.

Drawing reference Analog Board; 2002-100

Components U403, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011011	—U432— 10000000	—U411— 11111011	—U406— 00001100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 400.4 — DAC output set to 2.33V

Type Pass/Fail

Fault message `DAC output not +2.33V`

Description This test is the same as test 400.1 except that U433 (DAC B) is configured for a 2.33V output.

Drawing reference Analog Board; 2002-100

Components U403, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011011	—U432— 10111000	—U411— 11111011	—U406— 00001100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 400.5 — DAC output set to 4.48V

Type Pass/Fail

Fault message `DAC output not +4.48V`

Description This test is the same as test 400.1 except that U433 (DAC B) is configured for a 4.48V output.

Drawing reference Analog Board; 2002-100

Components U403, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011011	—U432— 11101100	—U411— 11111011	—U406— 00001100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.17 Regulator and switching tests

Test 401.1 — Regulator

Type Pass/Fail

Fault message `Regulator`

Description COMMON is routed to the ACF line through U428 (SHORT control line is pulled low). ACF then goes to multiplexer U414 pin 8 and follows the same path to the A/D buffer as the 400 level tests. U226 is set up for X1 gain.

Drawing reference Analog Board; 2002-100

Components U403, U414, U418, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 00010111	—U411— 10111011	—U406— 00000101	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 402.1 — Frequency switch

Type Pass/Fail

Fault message `Frequency switch`

Description U433 (DAC B) is set up to output 4.48V at PRECOMP+, U430 pin 1. The operation of the frequency switch, U425 (FREQ control line pulled low), is verified by dividing the PRECOMP+ voltage by the ratio of R491 and R440. The on resistance of U425 (about 25Ω between pins 2 and 3 must also be added to R440 as this value is also part of the ratio). Again, as in the 400 level tests, this voltage is routed to the A/D buffer, and U226 is set up for X1 gain.

Drawing reference Analog Board; 2002-100

Components U403, U425, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01010011	—U432— 11101100	—U411— 11111011	—U406— 01001100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 403.1 — Ground switch

Type Pass/Fail

Fault message `Ground switch`

Description COMMON at pin 9 of U414 is multiplexed to pin 8 and measured as in the previous 400 level tests.

Drawing reference Analog Board; 2002-100

Components U414 and associated components

Bit patterns .

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01010111	—U432— 11101100	—U411— 11111011	—U406— 01001100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.18 Absolute value circuit X1 gain tests

Test 404.1 — Absolute value X1 gain, - full-scale DAC

Type Pass/Fail

Fault message `Absolute value gain = 1`

Description DAC U433 and op amp pair U430 are set up to generate -4.36 VDC at PRECOMP+ and tied to ACF through R491 and U412. ACF is tied to AMP IN through U428, Q422, and the ACV buffer. AMP IN is tied to the inverting and non-inverting paths of FWR. NETOUT from U417 in the non-inverting path is monitored by the ZERO CROSSING amp for positive or negative polarity of the input signal and generates the COMP- signal that is fed to comparator U408. The comparator selects the path that the AMP IN signal will follow through the FWR with switches U410. The minus AMP IN path is through the inverting path R452, U418, U410, Q404, and U419 to pin 12 of the U414 multiplexer. The output of the multiplexer is tied to the A/D through buffer U403, ACV/A input to U222, and the A/D buffer in the X1 gain configuration.

Drawing reference Analog Board; 2002-100

Components U403, U417, U418, U419, U428, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011100	—U432— 00010111	—U411— 11111011	—U406— 01001101	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 404.2 — Absolute value X1 gain, - half-scale DAC

Type Pass/Fail

Fault message `Absolute value gain = 1`

Description DAC U433 and op amp pair U430 are set up to generate -2.15 VDC at PRECOMP+. This signal follows the same path as test 404.1.

Drawing reference Analog Board; 2002-100

Components U403, U414, U417, U418, U419, U428, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01011100	01001100	11111011	01001100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 404.3 — Absolute value X1 gain, zero DAC

Type Pass/Fail

Fault message `Absolute value gain = 1`

Description DAC U433 and op amp pair U430 are set up to generate .001 VDC at PRECOMP+. This signal has the same path to FWR as test 404.1. In this test, AMP IN positive, NETOUT from U417, the ZERO CROSSING amp, and the COMP- signal that is tied to comparator U408 select the non-inverting path for the AMP IN signal. Also, the AMP IN path is through R452, Q412, Q411, U417, R453, U410, Q404, and U419 to pin 12 of multiplexer U414. The output of U414 is tied to the A/D through buffer U403, ACV/A input to U222, and the A/D buffer in X1 gain configuration.

Drawing reference Analog Board; 2002-100

Components U403, U414, U417, U419, U428, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01011100	10000000	11111011	01001101	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 404.4 — Absolute value X1 gain, +half-scale DAC

Type Pass/Fail

Fault message `Absolute value gain = 1`

Description DAC U433 and op amp pair U430 are set up to generate +2.33 VDC at PRECOMP+. This signal follows the same path as test 404.3.

Drawing reference Analog Board; 2002-100

Components U403, U414, U417, U419, U428, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011100	—U432— 10111000	—U411— 11111011	—U406— 01001101	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 404.5 — Absolute value X1 gain, +full-scale DAC

Type Pass/Fail

Fault message `Absolute value gain = 1`

Description DAC U433 and op amp pair U430 are set up to generate +4.48 VDC at PRECOMP+. This signal follows the same path as test 404.3.

Drawing reference Analog Board; 2002-100

Components U403, U414, U417, U419, U428, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011100	—U432— 11101100	—U411— 11111011	—U406— 01001101	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.19 Absolute value circuit, X10 gain tests

Test 405.1 — Large positive DAC V for X10 gain comparison

Type Circuit Exercise

Fault message None

Description DAC U433 and op amp pair U430 are set up to generate +0.51 VDC at PRECOMP+ and tied to ACF through R491and U412. ACF is tied to pin 7 of multiplexer U414. The output of the multiplexer is tied to the A/D through buffer U403, ACV/A input to U222, and A/D buffer gain is X1. The value of the DAC voltage is measured and stored. This value will also be applied to the FWR that will be set for X10 gain in test 405.2. In this manner, the applied value to the X10 FWR and the output value can be compared to check for FWR accuracy.

Components Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011011	—U432— 10001101	—U411— 11011111	—U406— 01001111	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 405.2 — Absolute value X10 gain (non-inverting)

Type Pass/Fail

Fault message `Absolute value gain = 10`

Description DAC U433 and op amp pair U430 are set up to generate +0.51 VDC at PRECOMP+ and tied to ACF through R491 and U412. ACF is tied to AMP IN through U428, Q422, and ACV buffer. AMP IN is tied to the inverting and non-inverting paths of the FWR. NETOUT from U417 in the non-inverting path is monitored by the ZERO CROSSING amp for either polarity of input signal and generates the COMP- signal that is tied to comparator U408. The comparator selects the path that the AMP IN signal will follow through the FWR with switches in U410. Plus AMP IN path with FWR X10 is through R452, Q413, Q411, U417, R453, U410, Q404, and U419 to pin 12 of multiplexer U414. The output of the multiplexer is tied to the A/D through buffer U403, ACV/A input to U222, and the A/D buffer in X1 gain configuration.

Drawing reference Analog Board; 2002-100

Components U403, U408, U412, U414, U417, U419, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011100	—U432— 10001101	—U411— 11111111	—U406— 01001111	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 405.3 — Small positive DAC V for X10 gain comparison

Type Circuit Exercise

Fault message None

Description DAC U433 and op amp pair U430 are set up to generate +0.190 VDC at PRECOMP+. This signal follows the same path as test 405.1. This test has the same purpose as test 405.1, but the new test value is used for test 405.4.

Components Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011011	—U432— 10000101	—U411— 11011111	—U406— 01001111	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 405.4 — Absolute value X10 gain (non-inverting)

Type Pass/Fail

Fault message `Absolute value gain = 10`

Description DAC U433 and op amp pair U430 are set up to generate +0.190 VDC at PRECOMP+. This signal follows the same path as test 405.2.

Drawing reference Analog Board; 2002-100

Components U403, U408, U412, U414, U417, U419, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011100	—U432— 10000101	—U411— 11111111	—U406— 01001111	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 405.5 — Small negative DAC V for X10 gain comparison

Type Circuit Exercise

Fault message None

Description DAC U433 and op amp pair U430 are set up to generate -0.210 VDC at PRECOMP+. This signal follows the same path as test 405.1. This test has the same purpose as test 405.1, but the new test value is used for test 405.6.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011011	—U432— 01111011	—U411— 11011111	—U406— 01001111	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 405.6 — Absolute value X10 gain (inverting)

Type Pass/Fail

Fault message `Absolute value gain = 10`

Description DAC U433 and op amp pair U430 are set up to generate -0.210 VDC at PRECOMP+. This signal has the same path to the FWR as test 405.2. However, in this test with AMP IN negative, NETOUT from U417, the ZERO CROSSING amp, and the COMP- signal that is tied to comparator U408 select the inverting path for the AMP IN signal. The minus AMP IN path with FWR X10 is through R452, U418, U410, Q404, and U419 to pin 12 of multiplexer U414. The output of the multiplexer is tied to the A/D through buffer U403, ACV/A input to U222, and the A/D buffer gain is X1.

Drawing reference Analog Board; 2002-100

Components U403, U408, U412, U414, U417, U419, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011100	—U432— 01111011	—U411— 11111111	—U406— 01001111	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 405.7 — Large negative DAC V for X10 gain comparison

Type Circuit Exercise

Fault message None

Description DAC U433 and op amp pair U430 are set up to generate -0.490 VDC at PRECOMP+. This signal follows the same path as test 405.1. This test has the same purpose as test 405.1, but the new test value is used for 405.8.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01011011	01110100	11011111	01001111	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 405.8 — Absolute value X10 gain (inverting)

Type Pass/Fail

Fault message `Absolute value gain = 10`

Description DAC U433 and op amp pair U430 are set up to generate -0.490 VDC at PRECOMP+. This signal follows the same path as test 405.6.

Drawing reference Analog Board; 2002-100

Components U403, U408, U412, U414, U417, U419, U430, U433, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01011100	01110100	11111111	01001111	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.20 Sample and hold tests

Test 406.1 — Read DAC V for sample and hold test 406.6

Type Circuit Exercise

Fault message None

Description DAC U433 and op amp pair U430 are set up to generate -1.13 VDC at PRECOMP+ and tied to ACF through R491 and U412. ACF is tied to pin 7 of multiplexer U414. The output of the multiplexer is tied to the A/D through buffer U403, ACV/A input to U222, and the A/D buffer in X1 gain configuration. The value of the DAC voltage is measured and stored. This value will also be applied to the circuit in tests 406.2 and 406.3. In this manner, the applied value to the circuit and the output value (SELFTEST OUT) can be compared to check for circuit accuracy in test phase 406.6.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011100	—U432— 01100100	—U411— 11111011	—U406— 01001111	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 406.2 — Sample and hold output (-1.13V)

Type Circuit Exercise

Fault message None

Description DAC U433 and op amp pair U430 are set up to generate -1.13 VDC at PRECOMP+ and tied to ACF through R491 and U412. ACF is buffered to AMP IN through U428, Q422, and ACV buffer. AMP IN is tied through U425, to inverting X5 gain U426, R466, and R465. The SELFTEST signal causes one-shot U402 to output a 5µs low pulse, turning U425 and Q414 ON for 5µs. The value from inverter U426 is stored on C439 and applied to buffer Q409. SELFTEST OUT is the value on C439 and the V_{GS} value of Q409. This signal is applied to multiplexer U414 pin 11. The multiplexer output is tied to the A/D through buffer U403, ACV/A input to U222, and the A/D buffer in X1 gain configuration.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01011101	01100100	11111011	01001101	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 406.3 — Read sample and hold for test 406.6 comparison

Type Circuit Exercise

Fault message None

Description This test is the same as test 406.2 except that the value is stored for use in comparison calculation in test phase 406.6.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01011101	01100100	11111011	01001101	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 406.4 — Read DAC V for sample and hold test 406.6

Type Circuit Exercise

Fault message None

Description DAC U433 and op amp pair U430 are set up to generate -0.01 VDC at PRECOMP+ and tied to ACF through R491 and U412. ACF is tied to pin 7 of multiplexer U414. The output of the multiplexer is tied to the A/D through buffer U403, ACV/A input to U222, and the A/D buffer in X1 gain configuration. The value of the DAC voltage is measured and stored. This value will also be applied to the circuit in tests 406.5 and 406.6. In this manner, the applied value to the circuit

and the output value (SELFTEST OUT) can be compared to check for circuit accuracy in test phase 406.6.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011011	—U432— 10000000	—U411— 11111011	—U406— 01001111	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 406.5 — Sample and hold output (-0.01V)

Type Circuit Exercise

Fault message None

Description DAC U433 and op amp pair U430 are set up to generate -0.01 VDC at PRECOMP+ and tied to ACF through R491 and U412. ACF is buffered to AMP IN through U428, Q422, and ACV buffer. AMP IN is tied through U425 to inverting X5 gain U426, R466, and R465. The SELFTEST signal causes one-shot U402 to output a 5µs low pulse, turning U425 and Q414 ON for 5µs. The value from inverter U426 is stored on C439 and applied to buffer Q409. SELFTEST OUT is the value on C439 and the V_{GS} value of Q409. This signal is applied to multiplexer U414 pin 11. The multiplexer output is tied to the A/D through buffer U403, ACV/A input to U222, and the A/D buffer in X1 gain configuration.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011101	—U432— 10000000	—U411— 11111011	—U406— 01001101	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 406.6 — Sample and hold circuit

Type Pass/Fail

Fault message `Sample and hold`

Description This test is the same as test 406.5, but the value is stored for use in comparison calculation in this test phase. The measurement compares the actual difference in the DAC voltages 406.1-406.4 with that found via the sample and hold circuit tests 406.3-406.6.

Drawing reference Analog Board; 2002-100

Components Q409, U402, U426, U428, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011101	—U432— 10000000	—U411— 11111011	—U406— 01001101	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.21 Front end X1, / 100, /500 tests

Test 407.1 — Front end 2V range

Type Pass/Fail

Fault message `Front end 2V range`

Description The REFHI line is buffered by U255 to create REFBUF and is tied to pin 1 of U420 and then buffered to form BUFF. BUFF is routed through R493, K403, K401, input protection, and Q421 is tied to the input buffer Q418 and U423. The buffered BUFF signal (AMP IN) is tied to the FWR, and, being positive, follows the non-inverting, X1 path R452, Q412, Q411, U417, R453, U410, Q404, and U419 to pin 12 of U414. The output of U414 is tied to the A/D buffer through buffer U403, R434, R462, and U222. The A/D buffer is configured for X1 gain.

Drawing reference Analog Board; 2002-100

Components Q418, U410, U417, U419, U420, U423, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01110100	—U432— 10000000	—U411— 11111000	—U406— 11101110	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 407.2 — Front end 200V range

Type Pass/Fail

Fault message `Front end 200V range`

Description The REFHI line is buffered by U255 to create REFBUF and tied to pin 1 of U420 and then buffered to form BUFF. BUFF through R493 is tied to NET1 pin 1 (R488). The divided voltage (/100) at R488 pin 4 is tied to the input buffer Q418 and U423 through U428 and Q422. The buffered signal AMP IN is tied to the FWR, and, being positive, follows the non-inverting, X10 path R452, Q413, Q411, U417, R453, U410, Q404, and U419 to pin 12 of U414. The output of U414 is tied to the A/D buffer through buffer U403, R434, R462, and U222. The A/D buffer is configured for X1 gain.

Drawing reference Analog Board; 2002-100

Components Q418, U410, U417, U419, U420, U423, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01110100	10000000	11111111	01101110	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 407.3 — Front end 750V range

Type Pass/Fail

Fault message `Front end 750V range`

Description REFHI is tied to pin 1 of U420 and buffered to form BUFF. BUFF through R493 is tied to NET1, pin 1 (R488). U428 connects R489 in parallel to the bottom leg of the NET1 divider. The divided voltage (/500), R488 pin 4 is tied to the input buffer Q418 and U423 through U428 and Q422. The buffered signal AMP IN is tied to the FWR, and, being positive, follows the non-inverting, X10 path R452, Q413, Q411, U417, R453, U410, Q404, and U419 to pin 12 of U414. The output of U414 is tied to the A/D buffer through buffer U403, R434, R462, and U222. The A/D buffer is configured for X1 gain.

Drawing reference Analog Board; 2002-100

Components Q418, U410, U417, U419, U420, U423, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01110100	10000000	11111110	01101110	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.22 /200 frequency compensation tests

Test 408.1 — Circuit setup for test 408.2

Type Circuit Exercise

Fault message None

Description In this series of tests, DAC A of U433 is used to exercise the frequency compensation capacitors C459 and C461 of NET1, R488 (/100). In this phase, DAC A is programmed with 1s (no compensation), and the pin 2 output is tied to C461. BUFF is applied to NET1 (R488) through R493. The divided voltage pin 4 is tied to AC buffer Q418 and U423 through U428 and Q422. The signal AMP IN is tied through U425, U426, to Q510. This phase sets up the conditions for the next phase; there is no measurement in this phase.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111101	—U432— 11111111	—U411— 00111011	—U406— 01101110	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7654321	8	7654321	8	7654321	8	7654321

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 408.2 — Signal stored for test 408.3

Type Circuit Exercise

Fault message None

Description The SELFTEST control line turns ON Q425 and forces the voltage on NET1 (R488) to ground. The response of R488 pin 4 is stored in C439. This test uses the same path as test 408.1 except as follows: when the SELFTEST control line forces the divider voltage to zero, it also generates a one-shot pulse 5ms after SELFTEST goes low. This pulse turns Q414 on and stores the voltage on C439. The 5ms delay that turns on Q414 comes from U402 and U425. Note that no measurement is made during this test phase.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111101	11111111	00111011	01101100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 408.3 — Setup for test 408.5 and A/D measurement for test 408.6

Type Circuit Exercise

Fault message None

Description In this phase, DAC A is programmed with 0s, and the output pin 2 is tied to C461. BUFF is applied to NET1 (R488) through R493. The divided voltage at pin 4 is tied to AC buffer Q418 and U423 through U428 and Q422. The signal AMP IN is tied to the circuit through U425, U426, to Q414. This phase sets up the conditions for the next phase. The voltage on C439 that is buffered by Q409 (SELFTEST OUT) is tied to U414 pin 11. The output of U414 is tied to the A/D buffer through buffer U403, R434, R462, and U222. The A/D buffer is configured in X1 gain. This measurement is saved and used in a comparison in test 408.6.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	00000000	00111011	01101110	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 408.4 — Correction factor

Type Circuit Exercise

Fault message None

Description This test is the same as test 408.3 except that no measurement is taken.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111101	—U432— 00000000	—U411— 00111011	—U406— 01101110	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 408.5 — Signal stored for test 408.6

Type Circuit Exercise

Fault message None

Description The SELFTEST control line turns ON Q425 and forces the voltage on NET1 (R488) to ground. The response of R488 pin 4 is stored in C439. This test uses the same path as test 408.1 except as follows: when the SELFTEST control line forces the divider voltage to zero, it also generates a one-shot pulse 5µs after SELFTEST goes low. This pulse turns Q414 on and stores the voltage on C439. The 5µs delay that controls U425 and Q414 is generated by U402. No measurement is made during this phase.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111101	—U432— 00000000	—U411— 00111011	—U406— 01101100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 408.6 — /200 frequency compensation

Type Pass/Fail

Fault message `200V range compensation`

Description Same as test 408.2. Measure the output at A/D IN.

Drawing reference Analog Board; 2002-100

Components C459, C461, Q418, Q422, U423, U425, U426, U433 and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 10001110	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111101	—U432— 00000000	—U411— 00111011	—U406— 01101110	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7654321	8	7654321	8	7654321	8	7654321

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.23 /750 frequency compensation tests

Test 409.1 — Circuit setup for test 409.2

Type Pass/Fail

Fault message None

Description In this series of tests, DAC A of U433 is used to exercise the frequency compensation capacitors C460 and C463 of NET1 (R488) and R489 (/500). In this phase, DAC A is programmed with 1s (no compensation), and the output at pin 2 is tied to C463. BUFF is applied to NET1 (R488) through R493. The voltage at pin 4 is tied to AC buffer Q418 and U423 through U428 and Q422. The signal AMP IN is tied to the circuit through U425, U426, to Q414. This phase sets up the conditions for the next phase; there is no measurement in this phase.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111101	11111111	00111010	01101110	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 409.2 — Signal stored for test 409.3

Type Circuit Exercise

Fault message None

Description The SELFTEST control line turns ON Q425 and forces the voltage on NET1 (R488) to ground. The response of R488 pin 4 is stored in C439. This test uses the same path as test 408.1 except as follows: when the SELFTEST control line forces the divider voltage to zero, it also generates a one-shot pulse 5µs after SELFTEST goes low. This pulse turns Q414 on and stores the voltage on C439. The 5µs delay that controls U425 and Q414 is generated by U402. No measurement is made during this phase.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111101	11111111	00111010	01101100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 409.3 — Setup for test 409.5 and A/D measurement for test 409.6

Type Circuit Exercise

Fault message None

Description In this phase, DAC A is programmed with 0s, and the output at pin 2 is tied to C463. The rest of this test is the same as Test 408.3.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111101	00000000	00111010	01101110	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 409.4 — Correction factor

Type Circuit Exercise

Fault message None

Description This test is the same as test 408.3 except that no measurement is taken.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111101	—U432— 00000000	—U411— 00111010	—U406— 01101110	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 409.5 — Signal stored for 409.6

Type Circuit Exercise

Fault message None

Description The SELFTEST control line turns on Q425 and forces the voltage on NET1 (R488) to ground. The response of R488 pin 4 is stored in C439. This test uses the same path as test 409.1 except as follows: when the SELFTEST control line forces the divider voltage to zero, it also generates a one-shot pulse 5µs after SELFTEST goes low. This pulse turns Q414 on and stores the voltage on C439. The 5µs delay that controls U425 and Q414 is generated by U402. No measurement is made during this phase.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111101	—U432— 00000000	—U411— 00111010	—U406— 01101100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 409.6 — Signal comparisons

Type Pass/Fail

Fault message `750V range compensation`

Description Same as Test 409.2. Measure the output as A/D IN.

Drawing reference Analog Board; 2002-100

Components C460, C463, Q418, Q422, U423, U425, U426, U420, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111101	—U432— 00000000	—U411— 00111010	—U406— 01101110	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7654321	8	7654321	8	7654321	8	7654321

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.24 True RMS converter and filter tests

Test 410.1 — True RMS converter

Type Pass/Fail

Fault message `TRMS`

Description The REFHI line is tied to pin 1 of U420 and buffered to form BUFF. BUFF is routed through R493, K403, K401, input protection, and Q421 is tied to the input buffer Q418 and U423. The buffered BUFF signal (AMP IN) is tied to the FWR, and, being positive, follows the non-inverting, X1 path R452, Q412, Q411, U417, R453, U410, Q404, and U419 to pin 15 of the TRMS converter U420. The output of U420 is tied to U414 pin 6 through R219, and the output of U414 is tied to the A/D buffer through buffer U403, R434, R462, and U222. The A/D buffer is configured for X1 gain.

Drawing reference Analog Board; 2002-100

Components U410, U417, U420, U423, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011010	—U432— 10000000	—U411— 10111001	—U406— 10101110	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 411.1 — True RMS filter

Type Pass/Fail

Fault message `TRMS filter`

Description REFHI is tied to pin 1 of U420 and buffered to form BUFF. BUFF is routed through R493, K403, K401, input protection, and Q421 is tied to the input buffer Q418 and U423. The buffered BUFF signal (AMP IN) is tied to the FWR, and, being positive, follows the non-inverting, X1 path R452, Q412, Q411, U417, R453, U410, Q404, and U419 to pin 15 of the TRMS converter U420. The output of U420 is tied to filter R435, R446, R447, C433, C434, C432, and U426 through U413. The output of the filter is tied to U414 pin 5, and the output of U414 is tied to the A/D buffer through buffer U403, R434, R462, and U222. The A/D buffer is configured for X1 gain.

Drawing reference Analog Board; 2002-100

Components U413, U417, U419, U420, U423, U426, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011001	—U432— 11000000	—U411— 10111001	—U406— 10101110	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 411.2 — Filter; variable gain amplifier

Type Pass/Fail

Fault message `Filter`

Description REFHI is tied to pin 1 of U420 and buffered to form BUFF. BUFF through R493, K403, K401, input protection, and Q421 is tied to the input buffer Q418 and U423. The buffered BUFF signal (AMP IN) is tied to the FWR, and, being positive, follows the non-inverting, X1 path R452, Q412, Q411, U417, R453, U410, Q404, and U419 to the filter through U412. Output of the filter R435, R446, R447, C433, C434, C432, and U426 is tied to U414 pin 5, and the output of U414 is tied to the A/D buffer through buffer U403, R434, R462, and U222. The A/D buffer is configured for X1 gain.

Drawing reference Analog Board; 2002-100

Components U410, U412, U417, U419, U420, U423, U426, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01011001	—U432— 10000000	—U411— 11111001	—U406— 10101110	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.25 Frequency tests

The 412 series is a 10-phase frequency test. The first three phases set up the ASIC U816 on the A/D board to internally read frequency. The setup of the ASIC is accomplished by data from shift register U811. The second two tests are iterative tests that occur 85 times to create a mock frequency for the ASIC to read. The remaining tests are intended to stop the ASIC from reading frequency, and to allow the internal counts to be acquired by the digital circuitry. Again, this is done by data from the shift register U811. There is only one error message at the end of the last phase of the Frequency test series. Most of the ACV circuitry that is used to generate this test has been tested in previous 400 series tests.

Test 412.1 — Frequency, phase 1

Type

Circuit Exercise

Fault message

None

Description

The shift registers U809, U810, and U811 on the A/D are set to all lows to begin to set up the U816 ASIC to read frequency. The reference (REFHI) is generated by U219 and associated circuitry and buffered by U255. The buffered output of U255 is REFBUF, which is connected to a buffer in U420 with output BUFF. BUFF is connected to R493, and depending on whether Q425 is on or off, BUFF or common will be connected to relay K403. The SELFTESTEN line to U415 arms the gate for the SELFTEST signal. When SELFTEST is changed from high to low, the output of U415 switches Q425 off and then on. The signal path for the resulting common or BUFF generated by Q425 switching is through K403, K401, protection Q410, 424, 420, 415, and connected to Q421. The SELFTEST control line is low in the first test so the signal will be common. ACLOW with a logic low turns Q421 ON, and the signal is connected to buffer Q418 with output AMP IN. AMP IN is monitored by the non-inverting X1 gain path through Q412 to Q411 and U417.

This section is only one-half of the non-inverting path, and NETOUT is the applied signal inverted. The output NETOUT is connected to the Zero Crossing circuit. The PRECOMP+ output from U433 and U430 is selected with the SEL line, and the output value is set by the TRIG lines. The value for this test is set at 2.25V positive and connects to the Zero Crossing circuit through U418 pin 14 to 15 with control line TRIGLEV low. The PRECOMP+ signal to the Zero Crossing circuit is an offset used to make the switching in the following tests look like the signal is crossing zero. U416 of the Zero Crossing circuit generates the COMP- signal depending on the input NETOUT polarity and the offset created by PRECOMP+. COMP- is connected to comparator U408 and the Q and NOT Q outputs configure the signal path of AMP IN. The NOT Q output is also connected to U409 pin 12. When the FREQ line is high, it arms gate U409. When the Zero Crossing circuit and comparator U408 change the NOT Q line due to the monitoring of the input signal at NETOUT, the FREQ_OUT line will change. FREQ_OUT is connected to the A/D, and the changing states are counted as a frequency.

The following tests are all set up the same except the SELFTEST line is toggled to switch to common. The remaining circuit path is put in the test for the ease of monitoring the signal switching. The A/D is not reading the A/D_IN line. The output is connected to pin 12 of U414 and switched to the input of buffer U403. Output of U403 is ACV/A and is connected to pin 10 of U222. U222 is set up to switch ACV/A input to the A/D buffer U226. U226 is set up for X1 gain through U227 pin 2 to 3 with /X1 pin 1 low.

Drawing reference

Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00000000	00000000	00000000	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01001100	11001010	10111000	11101100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 412.2 — Frequency, phase 2

Type Circuit Exercise

Fault message None

Description This test uses the same setup as test 412.1 except that shift register U811 on the A/D board is configured to set up the U816 ASIC to read frequency.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001010	00000000	00000000	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01001100	11001010	10111000	11101100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 412.3 — Frequency, phase 3

Type Circuit Exercise

Fault message None

Description This test uses the same setup as test 412.1 except that shift register U811 on the A/D sets up the U816 ASIC to read frequency.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001000	00000000	00000000	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01001100	11001010	10111000	11101100	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 412.4 — Frequency, phase 4

Type Circuit Exercise

Fault message None

Description This test uses the same setup as test 412.1 except that the SELFTEST line is toggled to make Q425 switch.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001000	00000000	00000000	
		—U206—	—U207—	MUX_STB
		01110000	11001111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	11101001	
—U400—	—U432—	—U411—	—U406—	R2_STB
01001100	11001010	10111000	11101110	

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 412.5 — Frequency, phase 5

Type Circuit Exercise

Fault message None

Description This test uses the same setup as test 412.1 except that the SELFTEST line is toggled to make Q425 switch. Tests 412.4 and 412.5 are repeated 85 times. The switching is read as a frequency.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001000	—U810— 00000000	—U809— 00000000	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01001100	—U432— 11001010	—U411— 10111000	—U406— 11101100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 412.6 — Frequency, phase 6

Type Circuit Exercise

Fault message None

Description This test uses the same setup as test 412.1 except that shift register U811 on the A/D board sets up the U816 ASIC to finish reading frequency.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001001	—U810— 00000000	—U809— 00000000	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01001100	—U432— 11001010	—U411— 10111100	—U406— 11101100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 412.7 — Frequency, phase 7

Type Circuit Exercise

Fault message None

Description This test uses the same setup as test 412.1 except that the SELFTEST line is toggled through one more iteration to finish the frequency measurement.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001001	—U810— 00000000	—U809— 00000000	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01001100	—U432— 11001010	—U411— 10111000	—U406— 11101110	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 412.8 — Frequency, phase 8

Type Circuit Exercise

Fault message None

Description This test uses the same setup as test 412.1 except that the SELFTEST line is toggled through one more iteration to finish the frequency measurement.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00001001	—U810— 00000000	—U809— 00000000	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01001100	—U432— 11001010	—U411— 10111000	—U406— 11101100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 412.9 — Frequency, phase 9

Type Pass/Fail

Fault message `Frequency counter circuit`

Description This test uses the same setup as test 412.1 except that shift register U811 on the A/D board sets up the U816 ASIC to finish reading frequency and transfer the internal counts to the digital board.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 00000000	—U810— 00000000	—U809— 00000000	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01001100	—U432— 11001010	—U411— 10111000	—U406— 11101100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 412.10 — Frequency, phase 10

Type Circuit Exercise

Fault message None

Description This test uses the same setup as test 412.1 except that shift register U811 on the A/D board sets up the U816 ASIC to finish reading frequency and transfer the internal counts to the digital board. The counts are compared to the value obtained when the circuit was switched.

Drawing reference Analog Board; 2002-100
A/D Converter; 2002-160

Bit patterns

Bit pattern*				Register
	—U811— 0000100	—U810— 00000000	—U809— 00000000	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01001100	—U432— 11001010	—U411— 10111100	—U406— 11101100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.26 Amps/low ohms tests

Test 500.1 — 96µA ohms/200µA DCA range

Type Pass/Fail

Fault message `96µA ohms/200µA DCA range`

Description The 96µA ohms source is switched in using the /OHMC control line at U223 and U220. U232 pin 2 to 3 connects REFBUF to U233 pin 3. The 96µA current divides through Q211 and Q212, then flows through Q213, R322, CR217, K201,R334 and R342. This point is the HI input terminal to the DMM. The HI to AMPS jumper routes the current to the AMPS line through the 200µA switch (U234 pin 7 to 6), through R295, R319, and R362 to common. 96µA through 1000Ω applies 0.096V to U225 pin 3. U225 is configured for unity gain so the same voltage is at DCA. DCA is switched through U222 to the A/D MUX U226, and the gain is X1.

NOTE: INPUT HI and AMPS must be externally jumpered together to run this test.

Drawing reference Analog Board; 2002-100

Components U220, U222, U223, U225, U226, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 10101111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11010111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7654321	8	7654321	8	7654321	8	7654321

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 500.2 — 960µA ohms/2mA DCA range

Type Pass/Fail

Fault message `960µA ohms/2mA DCA range`

Description The 960µA ohms source is switched in using the /OHMB control line at U223 and U220. U232 pin 2 to 3 connects the REFBUF to U233 pin 3. The 960µA current divides between Q211 and Q212, then flows through Q213, R322, CR217, K201, R334 and R342. This point is the HI input terminal to the DMM. The HI to AMPS jumper routes the current to the AMPS line through the 2mA switch (U234 pin 11 to 10), through part of R295, R319, and R362 to common. 960mA through 100Ω generates 0.096V at U225 pin 3. U225 is configured for unity gain so the same voltage is at DCA. DCA is switched through U222 to the A/D MUX U226, and the gain is X1.

NOTE: AMPS and INPUT HI must be externally jumpered to run this test.

Drawing reference Analog Board; 2002-100

Components U220, U222, U223, U225, U226, U232, U233,and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	10101111	
	—U224—	—U203—	—U221—	R1_STB
	00001111	10001110	10110111	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 500.3 — 7.2mA ohms/2mA DCA range

Type Pass/Fail

Fault message `7.2mA ohms/2mA DCA range`

Description The 7.2mA ohms source is switched in using the /OHMA control line at U223 and U220. U232 pin 2 to 3 connects the REFBUF to U233 pin 3. For a more detailed description of the circuit setup, see test 304.1. The 7.2mA current divides through Q211 and Q212, then flows through Q213, R322, CR217, K201,R334 and R342. This point is the HI input terminal to the DMM. The HI to AMPS jumper routes the current to the AMPS line through the 2mA switch (U234 pin 11 to 10), through part of R295, R319, and R362 to common. 7.2mA through 100Ω generates 0.72V at U225 pin 3. U225 is at unity gain so the same voltage is at DCA. DCA is switched through U222 to the A/D multiplexer U226, and the gain is X1.

NOTE: INPUT HI and AMPS must be externally jumpered to run this test.

Drawing reference Analog Board; 2002-100

Components U220, U222, U223, U225, U226, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	10101111	
	—U224—	—U203—	—U221—	R1_STB
	00001111	10001110	01110111	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 500.4 — 20mA DCA range

Type Pass/Fail

Fault message `20mA DCA range`

Description The 7.2mA ohms source is switched in using the /OHMA control line at U223 and U220. U232 pin 2 to 3 connects the REFBUF to U233 pin 3. The 7.2mA current divides between Q211 and Q212, then flows through Q213, R322, CR217, K201,R334 and R342. This point is the HI input terminal to the DMM. The HI to AMPS jumper routes the current to the AMPS line through the 20mA range (Q217 on), through part of R295, R319, and R362 to common. 7.2mA through 10Ω generates 0.072V at U225 pin 3. U225 is at unity gain so the same voltage is at DCA. DCA is switched through U222 to the A/D MUX U226, and the gain is X1.

NOTE: INPUT HI and AMPS must be externally jumpered to run this test.

Drawing reference Analog Board; 2002-100

Components U220, U222, U223, U225, U226, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 10101111	MUX_STB
	—U224— 00111111	—U203— 10001110	—U221— 01110111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 500.5 — Baseline reading for tests 500.6 and 500.7

Type Circuit Exercise

Fault message None

Description This test uses the same ohms source configuration as above. All amps range switches are open. Due to the small signals to be measured for tests 500.6.and 500.7, this test takes a baseline reading of any offsets and leakages and subtracts this reading from the readings of tests 500.6 and 500.7. A/D MUX gain is X50.

NOTE: INPUT HI and AMPS must be externally jumpered to run this test.

Drawing reference Analog Board; 2002-100

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 11010000	—U207— 10101111	MUX_STB
	—U224— 00001111	—U203— 10001110	—U221— 01110111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 500.6 — 200mA DCA range

Type Pass/Fail

Fault message `200mA DCA range`

Description The 7.2mA ohms source is switched in using the /OHMA control line at U223 and U220. U232 pin 2 to 3 connects the REFBUF to U233 pin 3. The 7.2mA current divides between Q211 and Q212, then flows through Q213, R322, CR217, K201,R334 and R342. This point is the HI input terminal to the DMM. The HI to AMPS jumper routes the current to the AMPS line through the 200mA range (Q222 and Q215 on), through R319, and R362 to common. 7.2mA through 1Ω generates 0.0072V at U225 pin 3. U225 is at unity gain so the same voltage is at DCA. DCA is switched through U222 to the A/D MUX U226, and the gain is X50.

NOTE: INPUT HI and AMPS must be externally jumpered to run this test.

Drawing reference Analog Board; 2002-100

Components U220, U222, U223, U225, U226, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 11010000	—U207— 10101111	MUX_STB
	—U224— 01011111	—U203— 10001110	—U221— 01110111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:
Q Q Q Q Q Q Q Q
87654321 87654321 87654321 87654321
IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 500.7 — 2A DCA range

Type Pass/Fail

Fault message `2A DCA range`

Description The 7.2mA ohms source is switched in using the /OHMA control line at U223 and U220. U232 pin 2 to 3 connects the REFBUF to U233 pin 3. The 7.2mA current divides through Q211 and Q212, then flows through Q213, R322, CR217, K201,R334 and R342. This point is the HI input terminal to the DMM. The HI to AMPS jumper routes the current to the AMPS line through the 200mA range (Q223 and Q216 on), through R362 to common. 7.2mA through 0.1Ω generates 0.72mV at U225 pin 3. U225 is at unity gain so the same voltage is at DCA. DCA is switched through U222 to the A/D MUX U226, and the gain is X50.

NOTE: INPUT LO and AMPS must be externally jumpered to run this test.

Drawing reference Analog Board; 2002-100

Components U220, U222, U223, U225, U226, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		11010000	10101111	
	—U224—	—U203—	—U221—	R1_STB
	10011111	10001110	01110111	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.27 Amps protection tests

Test 501.1 — Amps protection

Type Pass/Fail

Fault message `Amps protection`

Description The 7.2mA ohms source is switched in using the /OHMA control line at U223 and U220. U232 pin 2 to 3 connects the REFBUF to U233 pin 3. The 7.2mA current divides between Q211 and Q212, then flows through Q213, R322, CR217, K201, R334 and R342. This point is the HI input terminal to the DMM. The HI to AMPS jumper routes the current to the AMPS line. The 200µA range switch U234 pin 7 to 6 is closed. 7.2mA through 1000Ω would normally generate a large voltage at U225 pin 5; however the voltage is clamped at two diode drops (approximately 1.2V) by CR218. U225 is at unity gain so this voltage is at DCA. DCA is switched through U222 to the A/D MUX U226, and the gain is X1.

NOTE: INPUT HI and AMPS must be externally jumpered to run this test.

Drawing reference Analog Board; 2002-100

Components U220, U222, U223, U225, U226, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 10101111	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 01110111	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7654321	8	7654321	8	7654321	8	7654321

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 501.2 — Amps bootstrap

Type Pass/Fail

Fault message `Amps bootstrap`

Description The 7.2mA ohms source is switched in using the /OHMA line at U223 and U220. U232 pin 2 to 3 connects the REFBUF to U233 pin 3. The 7.2mA current divides between Q211 and Q212, then flows through Q213, R322, CR217, K201, R334 and R342. This point is the HI input terminal to the DMM. The HI to AMPS jumper routes the current to the AMPS line. All of the amps range switches are off. All current flows through CR218, and the voltage is clamped at two diode drops (approximately 1.2V) by CR218. This voltage is fed to U225 pin 3, which is at unity gain so this voltage is at the AMPBOOT line. AMPBOOT is switched through U222 to the A/D MUX U226, and the gain is X1.

NOTE: INPUT HI and AMPS must be externally jumpered to run this test.

Drawing reference Analog Board; 2002-100

Components U220, U222, U223, U225, U226, U232, U233, and associated components.

Bit patterns

Bit pattern*				Register
	—U811—	—U810—	—U809—	AD_STB
	00001101	00000011	11100111	
		—U206—	—U207—	MUX_STB
		01110000	11101111	
	—U224—	—U203—	—U221—	R1_STB
	00010111	10001110	01110111	
—U400—	—U432—	—U411—	—U406—	R2_STB
01111011	10000000	11111011	00000100	

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7654321	8	7654321	8	7654321	8	7654321

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.28 ACA switch test

Test 502.1 — AC amps switch

Type Pass/Fail

Fault message `AC amps switch`

Description The 7.2mA ohms source is switched in using the /OHMA line at U223 and U220. U232 pin 2 to 3 connects the REFBUF to U233 pin 3. The 7.2mA current divides between Q211 and Q212, then flows through Q213, R322, CR217, K201, R334 and R342. This point is the HI input terminal to the DMM. The HI to AMPS jumper routes the current to the AMPS line. The 200µA range switch U234 pin 7 to 6 is closed. 7.2mA through 1000Ω would normally generate a large voltage at U225 pin 5; however the voltage is clamped at two diode drops (approximately 1.2V) by CR218. U234 pin 2 to 3 is closed, which routes the 1.2V to the ACA line.

In the AC section, the REL3 and DCF control lines are set to route the ACA signal through U413 pin 6 to 7 and U428 pin 10 to 11 respectively. The ACLOW control line turns Q422 on, which routes the 1.2V ACA signal to the AC volts input buffer to the AMP IN line. AMP IN is tied to the inverting and noninverting paths of the FWR. NETOUT from U417 in the noninverting path is monitored by the ZERO CROSSING amp for either polarity of input signal and generates the COMP- signal that is tied to comparator U408. The comparator selects the path that AMP IN signal will follow through the FWR with switches in U410. The plus AMP IN path is through R452, Q412, Q411, U417, R453, U410, Q404, and U419 to pin 12 of U414 MUX. The output of the MUX is tied to the A/D through buffer U403, ACV/A input to U222, and the A/D buffer in X1 gain configuration.

NOTE: INPUT HI and AMPS must be externally jumpered to run this test.

Drawing reference Analog Board; 2002-100

Components U410, U411, U413, U414, U419, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11001111	MUX_STB
	—U224— 00010011	—U203— 10001110	—U221— 01110111	R1_STB
—U400— 01111100	—U432— 00000001	—U411— 10011011	—U406— 00001111	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

2.11.29 Ohms sense tests

Test 600.1 — Ohms sense HI

Type Pass/Fail

Fault message `Ohms sense HI`

Description A 4-wire short on the input lines applies LO through the path of Q232 and Q231 (turned on by control line 4WOHM), through Q243 to BUFFIN to the input buffer. BSCOM goes through Q207 and Q208 to the A/D MUX U226. The gain is X1.

NOTE: The INPUTS and SENSE jacks must be externally shorted together to run this test.

Drawing reference Analog Board; 2002-100

Components Q207, Q208, Q231, Q232, Q243, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01100000	—U207— 00001111	MUX_STB
	—U224— 00010111	—U203— 10101001	—U221— 11100101	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
8	7	6	5	4	3	2	1

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

Test 600.2 — Ohms sense LO

Type Pass/Fail

Fault message `Ohms sense LO`

Description A 4-wire short on the input lines applies LO through the SENSE_LO path of R360, U242 pins 15 to 14, to the ADGND MUX U253, then to the A/D MUX at U226. Common is routed through U222 S1 to U226 pin 3. A/D MUX gain is X1.

NOTE: The INPUTS and SENSE jacks must be externally shorted together to run this test.

Drawing reference Analog Board; 2002-100

Components R360, U242, and associated components.

Bit patterns

Bit pattern*				Register
	—U811— 00001101	—U810— 00000011	—U809— 11100111	AD_STB
		—U206— 01110000	—U207— 11111101	MUX_STB
	—U224— 00010111	—U203— 10001110	—U221— 11101001	R1_STB
—U400— 01111011	—U432— 10000000	—U411— 11111011	—U406— 00000100	R2_STB

*Bits associated with register IC terminals as follows:

Q	Q	Q	Q	Q	Q	Q	Q
87654321		87654321		87654321		87654321	

IC pins: Q8=11, Q7=12, Q6=13, Q5=14, Q4=7, Q3=6, Q2=5, Q1=4.

3
Disassembly

3.1 Introduction

The information in this section explains how to disassemble the Model 2002. Also discussed are handling and cleaning considerations as well as the procedure to change the main CPU firmware in the event of an upgrade. This section is organized as follows:

3.2 Handling and cleaning precautions: Covers general precautions to take when troubleshooting inside the unit, and cleaning procedures when replacing parts.

3.3 Static-sensitive devices: Explains handling procedures for static-sensitive devices.

3.4 Case cover and shield removal: Explains how to remove the case cover. Also covered is the removal of the top shield of the analog board to allow access to analog circuitry for troubleshooting.

3.5 PC-board removal: Provides the procedures for removing the digital board, A/D converter board and the analog board.

3.6 Front panel disassembly: Explains how to remove the display board and/or the front panel switch pad.

3.7 Cooling fan removal: Explains how to remove the cooling fan from the chassis.

3.8 Firmware replacement: Provides the procedure to change firmware.

3.9 Instrument re-assembly: Provides some general guidelines to follow when re-assembling the Model 2002.

3.10 Assembly drawings: Provides mechanical drawings to assist in the disassembly and re-assembly of the Model 2002.

3.2 Handling and cleaning precautions

When servicing the instrument, care should be taken not to indiscriminately touch PC board traces to avoid contaminating them with body oils or other foreign matter. Mother board areas covered by the shield have high-impedance devices or sensitive circuitry where contamination could cause degraded performance.

3.2.1 PC-board handling

Observe the following precautions when handling PC-boards:

- Wear clean cotton gloves.
- Handle PC-boards only by the edges and shields.
- Do not touch any board traces or components not associated with the repair.
- Do not touch areas adjacent to electrical contacts.
- Use dry nitrogen gas to clean dust off PC-boards.

3.2.2 Solder repairs

Observe the following precautions when it is necessary to use solder on a circuit board:

- Use an OA-based (organic activated) flux, and take care not to spread the flux to other areas of the circuit board.

- Remove the flux from the work areas when the repair has been completed. Use pure water along with clean foam-tipped swabs or a clean soft brush to remove the flux. Be sure not to flush the flux across PC-boards when removing flux or cleaning PC-boards with water.
- Once the flux has been removed, swab only the repaired area with methanol, then blow dry the board with dry nitrogen gas.
- After cleaning, the board should be allowed to dry in a 50°C low-humidity environment for several hours.

3.3 Special handling of static-sensitive devices

CMOS devices operate at very high impedance levels for low power consumption. As a result, any static that builds up on your person or clothing may be sufficient to destroy these devices, if they are not handled properly. Use the following precautions to avoid damaging them:

CAUTION

Many CMOS devices are installed in the Model 2002. In general, it is recommended that all semiconductor devices be handled as being static-sensitive.

1. ICs should be transported and handled only in containers specially designed to prevent static build-up. Typically, these parts will be received in anti-static containers of plastic or foam. Keep these devices in their original containers until ready for installation.
2. Remove the devices from their protective containers only at a properly grounded work station. Also, ground yourself with a suitable wrist strap.
3. Handle the devices only by the body; do not touch the pins.
4. Any printed circuit board into which the device is to be inserted must also be grounded to the bench or table.
5. Use only anti-static type solder sucker.
6. Use only grounded tip solder irons.
7. Once the device is installed in the PC board, it is normally adequately protected, and normal handling can resume.

3.4 Case cover and shield removal

If it is necessary to troubleshoot the instrument or to replace a component, use the following procedures as required. The first procedure removes the case cover, and the second procedure removes the top shield of the analog board, allowing access to analog circuitry.

3.4.1 Case cover removal

WARNING

Before removing the case cover, disconnect the line cord and any test leads from the instrument.

To remove the case cover, refer to drawing 2002-054 (at the end of this section), and perform the following steps:

1. **Remove Handle:** The handle serves as an adjustable tilt-bail. Its position is adjusted by gently pulling it away from the sides of the instrument case and swinging it up or down. To remove the handle, swing the handle below the bottom surface of the case and back until the orientation arrows on the handles line up with the orientation arrows on the mounting ears. With the arrows lined up, pull the ends of the handle out of the case.
2. **Remove Mounting Ears:** Each mounting ear is secured to the chassis with a single screw. Remove the two screws, and pull down and out on each mounting ear. Note: When re-installing the mounting ears, make sure to mount the right ear to the right side of the chassis, and the left ear to the left side of the chassis. Each ear is marked “RIGHT” or “LEFT” on its inside surface.
3. **Remove Rear Bezel:** The rear bezel is secured to the chassis by two captive screws. To remove the rear bezel, loosen the two screws, and pull the bezel away from the case.
4. **Remove Grounding Screw:** Remove the grounding screw for the case cover. This screw is located on the bottom side of the instrument at the rear.
5. **Remove Chassis:** Grasp the front bezel of the instrument and carefully slide the chassis forward, out of the metal case.

The internal PC-board assemblies are now accessible.

3.4.2 Analog board top shield removal

Most of the analog circuitry is located under the top shield for the analog board. The top shield (shown in drawing 2002-050) is secured to the analog board by a single screw. To remove the top shield, simply loosen the screw, and carefully lift the shield out of the chassis. You should remove the rear choice first and may have to remove the front choke as well to prevent damage.

3.5 PC-board removal

There are three PC-boards mounted in the chassis: the digital board, the A/D converter board, and the analog board. The removal of these three boards is covered in this paragraph. The display board is mounted in the front panel assembly. The removal of the display board is covered in paragraph 3.6.

Any one of the PC-boards can be removed without having to remove any of the other boards. Note that the A/D converter board plugs into the analog board and can be left installed when removing the analog board.

NOTE

Before performing any of the following procedures to remove a PC-board, remove the case cover as explained in paragraph 3.4.1.

3.5.1 Digital board

The digital board is removed through the bottom of the chassis (see drawing 2002-053). Note that the power switch pushrod need not be removed in order to remove the digital board.

Perform the following steps to remove the digital board:

1. **Unplug Cables:** Turn the chassis upside-down and unplug the following cables from the digital board:
   A. Unplug the display board ribbon cable from connector J1033.
   B. Unplug the transformer cable from connector J1032.
   C. Unplug the analog board ribbon cable from connector J1027. This cable connection is located under the power switch pushrod.
   D. Unplug the fan cable from connector J1037. This two-conductor cable connection is located at the rear of the digital board in front of the IEEE-488 connector.
2. **Unfasten PC-Board:** Remove the following screws and nuts to unfasten the digital board from the chassis:
   A. At the rear panel, remove the two nuts that secure the IEEE connector to the chassis.
   B. Remove the screw that connects ground of the +5V regulator (U629) to the chassis. The regulator is located at the front of the digital board behind the large electrolytic capacitor (C611).
   C. Remove the four screws that secure the digital board to the chassis. One screw is located at the rear of the digital board in front of the bank of 12 capacitors. Another screw is located next to the +5V regulator (U629). The other two screws are located near the connector for the option slot.
3. **Remove Digital Board:** The board is held in place by edge guides on each side. Slide the digital board forward until the board edges clear the guides, and then carefully pull the board out of the chassis.

3.5.2 A/D converter board

The A/D converter board is located under the analog board top shield (see drawing 2002-050).

Perform the following steps to remove the A/D converter board:

1. **Remove Analog Top Shield:** Position the chassis right-side-up. The top shield is secured to the analog board by a single screw. To remove the top shield, simply loosen the screw, and carefully lift the shield out of the chassis.
2. **Remove A/D Converter Board:** The A/D converter board is located near the front of the instrument and is plugged into the analog board at connector J1026. The board rests on three stand-offs. Each standoff has a retaining clip to hold the board securely in place. Gently pull each retaining clip away and lift the board up until it clears the clip. With the board clear of the three retaining clips, unplug the board, and pull it out of the chassis.

3.5.3 Analog board

The analog board is removed through the top of the chassis (see drawing 2002-051). Perform the following steps to remove the analog board:

1. **Remove Analog Top Shield:** The top shield is secured to the analog board by a single screw. To remove the top shield, simply loosen the screw, and carefully lift the shield out of the chassis.
2. **Remove Pushrods:** Remove the pushrods for the INPUTS switch and the POWER switch as follows:
   A. Using suitable pliers, grasp the INPUTS pushrod near the switch, and pull forward until it disengages from the switch shaft. Remove the pushrod from the chassis.
   B. Turn the chassis upside-down. Grasp the rear end of the POWER pushrod, and pull upward until it disengages from the switch shaft. Remove the pushrod from the chassis.
   C. Return the chassis to the up-right position.
3. **Remove Power Transformer:** Remove the power transformer (see drawing 2002-052) as follows:

A. Disconnect the transformer ground. A kep nut is used to connect this green ground wire to a threaded stud on the chassis.
B. Unplug the transformer. There are three plugs for the transformer. Two are located on the analog board at connectors J1024 and J1025, and the third is located on the digital board at connector J1032. Turn the chassis upside-down to gain access to the plug on the digital board. When finished, return the chassis to the up-right position.
C. The transformer is secured to the side of the chassis by a single screw. Remove this screw, and pull the transformer out of the chassis.

4. **Remove AC Power Receptacle:** Remove the AC power receptacle as follows:
   A. Disconnect the receptacle ground wire. A kep nut is used to connect this green ground wire to a threaded stud on the chassis.
   B. Unplug the AC power receptacle cable. The connector for this cable is located on the analog board next to the power receptacle.
   C. A spring clip on each side of the receptacle is used to secure it to the rear panel of the chassis. To remove it, press both clips inward and, at the same time, push the receptacle out of the access hole in the rear panel of the chassis.
5. **Unplug Cable to Digital Board:** On the left side of the analog board there is a ribbon cable going to the digital board. Turn the chassis upside-down, and unplug this cable at connector J1027 on the digital board. Return the chassis to the right-side-up position.
6. **Disconnect Input Terminals:** There are 10 input terminal connections (five for the front and five for the rear). Nine of these terminal wires are disconnected by simply pulling them off the pin connector on the input terminals. The front panel AMPS terminal wire must be unsoldered from the analog board. The solder connection for this white/blue wire is located next to the INPUTS switch.

Terminal wire color identification for re-assembly is as follows:

Terminal	Front	Rear
INPUT HI	Red	White/Red
INPUT LO	Black	White/Black
SENSE HI	Yellow	White/Yellow
SENSE LO	Grey	White/Grey
AMPS	White	White/Blue

7. **Remove Regulator Clip:** A metal clip is used to transfer heat from two power supply devices (R101 and Q528) to the chassis. The clip is located on the left side of the chassis towards the rear. The clip is removed by pulling it upward. You may need to use a small flat-bladed screwdriver to pry it up.

CAUTION

The regulator clip allows the chassis to serve as a heat sink for R101 and Q528. To prevent damage to these devices (due to overheating), be sure to install the clip when re-assembling the Model 2002.

8. **Unfasten Analog Board:** The analog board is secured to the chassis at the rear panel by the two BNC connectors (External Trigger and Meter Complete). At the rear panel, remove the nuts and lock washers for the BNC connectors. Also remove the chokes.
9. **Remove Analog Board:** The board is held in place by edge guides on each side of the chassis. Slide the analog board forward until the board edges clear the guides, and then carefully lift the board out of the chassis. The bottom shield on the analog board can be removed by simply pulling it off the board.

NOTE

With the analog board removed, the cooling fan can be removed as explained in paragraph 3.7.

3.6 Front panel disassembly

Use the following disassembly procedure to remove the display board and/or the pushbutton switch pad. Drawing 2002-052 shows how the front panel separates from the chassis, and drawing 2002-040 shows an exploded view of the front panel assembly.

NOTE

Before performing the following procedure to remove and disassemble the front panel, remove the case cover as explained in paragraph 3.4.1.

Perform the following steps to remove and disassemble the front panel:

1. **Unplug Display Cable:** Turn the chassis upside-down, and unplug the display cable from the digital board at connector J1033.

2. **Remove Front Panel Assembly:** The front panel assembly has four retaining clips that snap onto the chassis over four pem nut studs. Two retaining clips are located on each side of the front panel. Pull the retaining clips outward and, at the same time, pull the front panel assembly forward until it separates from the chassis.
3. **Remove Display Board:** The display board is held in place by a PC board stop. This stop is simply a plastic bar that runs along the bottom edge of the display board. Using a thin bladed screwdriver, pry the plastic bar upward until it separates from the casing of the front panel. Pull the display board out of the front panel.
4. **Remove Switch Pad:** The conductive rubber switch pad simply pulls out of the front panel.

3.7 Cooling fan removal

The cooling fan, which is mounted to the rear panel of the chassis, need not be removed in order to clean the filter. To clean the filter, refer to the procedure in paragraph 1.4. If, however, the fan must be removed, perform the following procedure.

NOTE

In order to remove the cooling fan, the case cover must be removed (see paragraph 3.4.1), and the analog board must be removed (see paragraph 3.5.3).

1. **Disconnect Fan Cable:** Turn the chassis upside-down, and unplug the fan cable from connector J1037. This two-conductor cable connection is located at the rear of the digital board in front of the IEEE-488 connector. Return the chassis to the right-side-up position.
2. **Remove Mounting Nuts:** The fan is secured to the chassis by two mounting nuts. Remove these nuts, and pull the fan out of the chassis.

3.8 Main CPU firmware replacement

Changing the firmware may be necessary as upgrades become available. The firmware revision level for the main CPU is displayed during the power-on sequence. The firmware for the main CPU is located in two EPROMS (U637 and U638) located on the digital board. (See the digital board component layout drawing 2002-140 at the end of Section 4.)

Perform the following steps to replace the CPU firmware:

WARNING

Disconnect the instrument from the power line and remove all test leads before changing the firmware.

1. Remove the case cover as explained in paragraph 3.4.1.
2. Turn the instrument upside down to gain access to the digital board.
3. Locate U637 and U638 (EPROMS) on the digital board. These two ICs are located near the center of the PC board.

CAUTION

EPROMS U637 and U638 are static-sensitive devices. Be sure to adhere to the handling precautions explained in paragraph 3.3 when replacing these devices.

4. Using an appropriate chip extractor, remove U637 and U638 from their sockets.
5. Install the new EPROMS in the appropriate sockets, making sure that pin 1 for each device is properly oriented.

NOTE

The odd-addressed EPROM must be installed at U637, and the even-addressed EPROM must be installed at U638. The instrument will not operate if the EPROMS are incorrectly installed.

3.9 Instrument re-assembly

The instrument can be re-assembled by reversing the previous disassembly procedures. Make sure that all parts are properly seated and secured, and that all connections are properly made. To ensure proper operation, shields must be replaced and fastened securely.

WARNING

To ensure continued protection against safety hazards, verify that power line ground (green wire attached to AC power receptacle) and the power transformer ground are connected to the chassis.

3.10 Assembly drawings

The following assembly drawings are provided to assist in disassembly and re-assembly of the instrument. Also, the Keithley part numbers for most mechanical parts are provided in these drawings.

- Front Panel Assembly; 2002-040
- Analog Shield Assembly; 2002-050
- Chassis Assembly (Analog Board); 2002-051
- Chassis Assembly (Front Panel and Miscellaneous); 2002-052
- Chassis Assembly (Digital Board); 2002-053
- Chassis Assembly (Case Cover and Handle); 2002-054
- Chassis Assembly (Rear Panel and Miscellaneous); 2002-055
- Final Inspection (Label Location); 2002-080

4
Replaceable Parts

4.1 Introduction

This section contains replacement parts information and component layout drawings for the Model 2002.

4.2 Parts lists

The following parts lists for the Model 2002 are shown in Tables 4-1 to 4-5. For part numbers to the various mechanical parts and assemblies, use the miscellaneous parts list (Table 4-5) and the assembly drawings provided at the end of Section 3.

4.3 Ordering information

To place an order, or to obtain information concerning replacement parts, contact your Keithley representative or the factory (see inside front cover for addresses). When ordering parts, be sure to include the following information:

- Instrument model number (Model 2002)
- Instrument serial number
- Part description
- Component designation (if applicable)
- Keithley part number

To facilitate repairs, complete circuit boards are available. Contact the Repair Department (see below) for pricing and availability.

4.4 Factory service

If the instrument is to be returned to Keithley Instruments for repair, perform the following:

1. Call the Repair Department at 1-800-552-1115 for a Return Material Authorization (RMA) number.
2. Complete the service form at the back of this manual, and include it with the instrument.
3. Carefully pack the instrument in the original packing carton.
4. Write ATTENTION REPAIR DEPARTMENT and the RMA number on the shipping label.

4.5 Component layouts

The component layouts are provided in the following pages:

A/D Converter Board: 2002-160
Display Board: 2002-110
Analog Board: 2002-100
Digital Board: 2002-140

Table 4-1
Model 2002 ADC board, parts list

Circuit desig.	Description	Keithley part number
C801-823	DIODE, ZENER, 6.2V, MMS26V2 SOD-123	DZ-97
C824-828	IC, QUAD 2 IN NOR, 74HCT02	IC-809
C829	IC, NCHAN LAT DMOS QUADFET, SD5400CY	IC-893
C830, 831	FERRITE CHIP 600 OHM BLM32A07	CH-62
C832, 833	CAP, 2200P, 10%, 100V CERAMIC	C-430-2200P
C834, 835	IC, 8 STAGE SHIFT/STORE, MC14094BD	IC-772
C836	IC, OP-AMP, AD847JR	IC-779
C837	IC, HI-SPEED BIFET OP-AMP, AD711JR	IC-894
CR801, 802	DIODE, DUAL HSM-2822T31	RF-95
L801-804	FERRITE CHIP 600 OHM BLM32A07	CH-62
P1026	CONNECTOR, FEMALE 25 PIN	CS-767-25
Q801-804	TRANS, N-MOSFET, UN0605T	TG-243
Q805	TRANS, P-CHAN, JFET MMBF5460	TG-272
Q806, 807	TRANS, N-CHAN J-FET, MMBF5457	TG-273
R801-804, 828-831	RES, 10, 5%, 125MW, METAL FILM	R-375-10
R805, 806, 808	RES, 100, 5%, 125MW, METAL FILM	R-375-100
R809-812	RES, 1K, 5%, 125MW, METAL FILM	R-375-1K
R813-815	RES, 10K, 5%, 125MW, METAL FILM	R-375-10K
R816	RES, 1.28M, .1%, 1/8W METAL FILM	R-176-1.28M
R817	RES, 150, 5%, 125MW, METAL FILM	R-375-150
R818	RES, 200K, 5%, 125MW, METAL FILM	R-375-200K
R819	RES, 2K, 5%, 125MW, METAL FILM	R-375-2K
R820, 822	RES, 470, 5%, 125MW, METAL FILM	R-375-470
R821	RES, 5.1K, 5%, 125MW, METAL FILM	R-375-5.1K
R823, 824	RES, 49.9K, 1%, 125MW, METAL FILM	R-391-49.9K
R825	RES, 82.5, 1%, 125MW, METAL FILM	R-391-82.5
R826	RES NET, 20K, .1%, 668A	TF-243-20K
R827	RES NET 5K, .1%, 668A	TF-243-5K
U801, 802	IC, OP-AMP, LOW NOISE, OP27GS	IC-914
U803	IC, 18V BIFET OP-AMP, AD744	IC-586
U804, 805	IC, OP-AMP, AD847JR	IC-779
U806, 807	IC, QUAD 2 IN NOR, 74HCT02	IC-809
U808	IC, HI-SPEED BIFET OP-AMP, AD711JR	IC-894
U809-811	IC, 8 STAGE SHIFT/STORE, MC14094BD	IC-772
U812	IC, NCHAN LAT DMOS QUADFET, SD5400CY	IC-893
U813, 815	IC, JFET OP-AMP, LF411	IC-453
U814	PROGRAMMED, IC, 160 MACROCELL CMOSEPLDEPM7160LC-84-3	2002-802-*
U816-818	IC, LO NOISE BIFET OP-AMP OPA776P	IC-954
U819	IC, GND-SENSE, 12NS COMPARATOR, LT1116	IC-908
U820	IC, QUAD D FLIP FLOP W/CLK, RESET 72HC175	IC-923
VR801, 802	DIODE, ZENER, 6.2V, MMS26V2 SOD-123	DZ-97
Y801	OSCILLATOR HIGH SPEED CMOS 12MHZ	CR-37

* Order revision level. For example: 2002-803-A03

Table 4-2
Model 2002 display board, parts list

Circuit desig.	Description	Keithley part number
	DISPLAY BOARD ASSEMBLY	2002-110
C901	CAP, 22UF, 20%, 6.3, TANTALUM	C-417-22
C902, 904, 907, 908, 910	CAP, .1UF, 20%, 100V, CERAMIC	C-436-.1
C903, 905, 906, 909, 911	CAP, .1UF, 20%, 50V, CERAMIC	C-418-.1
C912	CAP, 2.2UF, 20%, 100V ALUM ELEC	C-503-2.2
C913, 914	CAP, 100UF, 20%, 16V, TANTALUM	C-504-100
C915, 916	CAP, 33PF, 10%, 100V, CERAMIC	C-451-33p
CR901-904	DIODE, SWITCHING, 250MA, BAV103	RF-89
CR905, 906	DIODE, SWITCHING, MMBD914	RF-83
DS901	VACUUM FLUORESCENT DISPLAY	DD-51C
P1033	CABLE ASSEMBLY	CA-62-4A
Q901-902	TRANS, NPN GEN PURPOSE BC868	TG-293
R901	RES NET, 15K, 2%, 1.875W	TF-219-15K
R902	RES, 13K, 5%, 125MW, METAL FILM	R-375-13K
R903, 904	RES, 4.7K, 5%, 250MW, METAL FILM	R-376-4.7K
R905	RES, 1M, 5%, 125MW, METAL FILM	R-375-1M
R906	RES, 1K, 5%, 250MW, METAL FILM	R-376-1K
R907	RESISTOR	R-376-240
R908	RES, 10M, 5%, 125MW, METAL FILM	R-375-10M
T901	TRANSFORMER, TDK, ER14.5 SERIES	TR-300
U901, 904, 905	IC, LATCHED DRIVERS, UCN-5812EPF-1	IC-732
U902	PROGRAMMED, IC, 8-BIT MICROCON, MC68HC705C89	7001-800-*
U903	IC, 32-BIT, SERIAL UCN5818EPF-1	IC-830
VR901	DIODE, ZENER, 8.2V, MMBZ5237	DZ-92
Y901	CRYSTAL, 4MHZ	CR-36-4M

* Order revision level. For example 7001-800A02

Table 4-3
Model 2002 analog board parts list

Circuit desig.	Description	Keithley part number
	ANALOG ASSEMBLY	2002-100
	CONN, TEST POINT	CS-553
	CRIMP CONTACT ROUND	CS-760
	FUSE HOLDER (FOR F101, 102)	FH-32
C101, 103, 115, 402	CAP, 10UF, 20%, 25V, TANTALUM	C-440-10
C102	CAP, .01UF, 20%, 500V, CERAMIC	C-22-.01
C104	CAP, 1000UF, 20%, 50V, ALUM ELEC	C-469-1000
C105, 422	CAP, 1UF, 20%, 50V, TANTALUM	C-431-1
C106, 107, 201-205, 207-216, 218-223, 226, 229-232, 237, 239, 240, 243-245, 252, 254-257, 259, 264-267, 269, 276, 280-283, 288, 289, 293, 294, 401, 403, 405-411, 413, 421, 423-425, 428-431, 435, 442-447, 449, 451, 465-467	CAP., .1UF, 20%, 50V, CERAMIC	C-418-.1
C108	CAP, 1UF, 20%, 100V, CERAMIC	C-487-1
C109, 111, 273, 468	CAP, .1UF, 20%, 50V, CERAMIC	C-418-.1
C110	CAP, 2.2UF, 20%, 35V, TANTALUM	C-476-2.2
C112, 113	CAP, 2200UF, 20%, 35V, ALUM ELEC	C-468-2200
C114	CAP, 2200UF, 20%, 16V, ALUM ELEC	C-473-2200
C116, 117	CAP, 470UF, 20%, 63V, ALUM ELEC	C-477-470
C118, 119	CAP, 1000UF, 20%, 35V, ALUM ELEC	C-468-1000
C206	CAP, 100UF, 20%, 10V, ALUM ELEC	C-483-100
C217	CAP, .022UF, 10%, 50V, CERAMIC	C-491-.022
C224	CAP, 20PF, 5%, 500V, DIPPED MICA	C-236-20P
C225, 450, 452, 454	CAP., .01UF, 20%, 50V, CERAMIC	C-418-.01
C227, 234, 235, 238, 271, 272	CAP, 68UF, 20%, 50V, POLYESTER FILM	C-344-.68
C228, 263, 287	CAP, 220PF, 2.5%, 630V, POLYPROPYLENE	C-405-220P
C233, 241, 242, 404, 418, 456, 457	CAP, 1000PF, 20%, 50V, CERAMIC	C-418-1000P
C247, 250, 253	CAP, 22UF, 10%, 16V, ALUM ELEC	C-361-22
C248, 249, 260-262, 290, 291, 416, 437	CAP, 100PF, 5%, 100V, CERAMIC	C-465-100P
C251	CAP, .01UF, 10%, 1000V, CERAMIC	C-64-.01
C268, 284-286, 417	CAP., .15UF, 20%, 50V, CERAMIC	C-418-.15
C270, 274, 277, 278, 292, 412	CAP, 47PF, 10%, 100V, CERAMIC	C-451-47P
C275	CAP, 47PF, 10%, 100V, CERAMIC	C-451-47P
C279, 436	CAP, 33PF, 10%, 100V, CERAMIC	C-451-33P
C414	CAP, 4.7PF, 5%, 50V, MONO-CERAMIC	C-452-4.7P
C415	CAP, 2.2PF, 5%, 1500V, CERAMIC	C-308-2.2P
C419, 440	CAP, 100PF, 10%, 1000V, CERAMIC	C-64-100P
C420	CAP, 2.2UF, 20%, 63V, POLYCARB	C-480-2.2
C426	CAP, 10PF, 10%, 1000V, CERAMIC	C-64-10P
C427	CAP, 22PF, 10%, 1000V, CERAMIC	C-64-22P
C432-434	CAP, .33UF, 20%, 63V, POLYCARBONATE	C-482-.33
C438	CAP, 1000PF, 20%, 50V, CERAMIC	C-418-1000P
C439	CAP, 10000PF, 20%, 63V, POLY-FILM	C-471-10000P
C441	CAP, 2.7PF, .25PF TOL, 1000V, CERAMIC	C-367-2.7P
C448	CAP, 47PF, 10%, 1000V, CERAMIC	C-64-47P
C453, 462	CAP, 6.2PF, .25PF TOL, 1000V, CERAMIC	C-349-6.2P
C458	CAP, 10PF, 1%, 2KV, GLASS	C-485-10P
C459	CAP, 820PF, 1%, 300V, GLASS	C-486-820P
C460	CAP, 3600PF, 1%, 500V, MICA	C-278-3600P

Table 4-3
Model 2002 analog board parts list (cont.)

Circuit desig.	Description	Keithley part number
C461	CAP, 91PF, 1%, 300V, MICA	C-474-91P
C463	CAP, 270PF, 1%, 300V, MICA	C-462-270P
C464	CAP, .1UF, 20%, 1000V, MET POLYCARBONATE	C-490-.1
CR101	DIODE, BRIDGE, 5 AMP/400V, EDI-PE40	RF-88
CR102, 214, 219, 404, 410, 414, 415	DIODE, DUAL SWITCHING, BAV99L	RF-82
CR103, 105, 106, 108, 109	DIODE, SWITCHING, 250MA, BAV103	RF-89
CR104, 113	DIODE, BRIDGE, VM18	RF-52
CR107	DIODE, CONTROLLED AVALANCHE, BYD17GSOD-87	RF-91
CR110, 111, 118, 119, 204, 417-419	DIODE, SWITCHING, 250MA, BAV103	RF-89
CR112	DIODE, SILICON, W04M (CASE WM)	RF-46
CR114-117, 210, 211	DIODE, CONTROLLED AVALANCHE, BYD17GSOD-87	RF-91
CR201-203, 215, 216, 220, 401, 403, 406-408	DIODE, SWITCHING, MMBD914	RF-83
CR206-209, 212, 213, 411-413, 416	DIODE, IN3595 (D0-7)	RF-43
CR217, 223, 224	DIODE, HI-VOLTAGE, HV-15	RF-76
CR218	DIODE, BRIDGE PE05 (CASE KBU)	RF-48
CR225	DIODE (HP HSMS-2813)	RF-100
CR226	DIODE, SILICON, 5400 (267-01)	RF-34
CR402	DIODE, SILICON, IN4148 (D0-35)	RF-28
CR405, 409	DIODE, DUAL MIXER, MMBD352L	RF-86
DS201	PILOT LIG, HSMH-T400, LED	PL-92-1
E201	SURGE ARRESTOR SELECTED CG-3-1.52	SA-5
E295	RES NET, 900, 90, 9, 10%	TF-168-1
F101	FUSE, .5A, 250V	FU-71
F201	FUSE, 2A, 250V, FAST-BLO (5X20MM)	FU-48
J1002	CONN, MOLEX, 3-PIN	CS-772-3
J1022, 1023	CONN, BNC	CS-547
J1024, 1025	CONN, MALE, 5-PIN (MOLEX 42491)	CS-784-5
J1026	HEADER, DUAL BODY/STRAIGHT PIN	CS-765-25
K101	RELAY, MINIATURE, G6A-274P-ST-US-DC24	RL-160
K102	RELAY, MINIATURE, G6A-274P-ST-US-DC9	RL-159
K201	RELAY, REED HI VOLTAGE	RL-119
K401, 403, 404	RELAY, REED, HI-VOLT/ISOLATION, 848-1	RL-152
K402	RELAY, MINATURE (DPDT), DK1A1BE-6V	RL-153
L201	FERRITE CHIP 600 OHM BLM32A07	CH-62
L205	CHOKE	CH-61
L206	CHOKE, 100UH	CH-14
P1027	CABLE ASSEMBLY, 20 CONDUCTOR	CA-27-16C
Q101	TRANS, N-CHAN MOSFET 25K1451 (T03PML)	TG-291
Q102, 105, 220, 419	TRANS, NPN, MMBT3904	TG-238
Q103, 104, 209, 218, 221, 225, 403, 405-407	TRANS, N-MOSFET, VN0605T	TG-243
Q106	TRANS, P-CHAN, MOSFET, TP0610T	TG-259
Q107, 224, 229	TRANS, PNP, MMBT3906L	TG-244
Q201-203, 205, 206	TRANS, N-CHAN FET, 2MP4857A	TG-270
Q204, 251	TRANS, NPN SILICON, PXT 3904	TG-277
Q207	TRANS, N CHANNEL FET, 2N4392 (T0-92)	TG-128-1

Table 4-3
Model 2002 analog board parts list (cont.)

Circuit desig.	Description	Keithley part number
Q208	TRANS, N CHANNEL JFET (TO-92)	TG-225
Q210, 233, 239	TRANS, NPN COMP SILICON AMP, 2N5089	TG-62-1
Q211	TRANS, P-CHANNEL MOSFET, 3N163	TG-126
Q212	TRANS, PNP SILICON 2N3906 (T0-92)	TG-84
Q213	TRANS, N-CHAN MOSFET 25K1413 (T0-3PML)	TG-268
Q214, 402	TRANS, N-CHAN DMOS FET TN2504N8	TG-261
Q215, 216	TRANS, N-HEXFET, IRFR020 (D-PAK)	TG-239
Q217	TRANS, N CHANNEL JFET, 5432, (T0-92)	TG-198
Q219, 228	TRANS, PNP COMP SILICON AMP, MPS8599	TG-158
Q222, 223	TRANS, N-CHANNEL FET, BUZ71 (T0-220)	TG-196-1
Q226, 227, 242, 244	TRANS, SELECTED TG-128 (T0-92)	31841A
Q231, 232	TRANS, N-CHAN MOSFET, TN2540N8	TG-274
Q234, 238	TRANS, NPN SILICON, BC846BL	TG-278
Q240, 248	SELECTED, TG-167	2002-600A
Q241, 250	SELECTION, TG-225	182-600B
Q243	SELECTED TG-166	2001-601A
Q245, 246	TRANS, C-CHAN MOSFET, 2SK1412 (T0-220ML)	TG-276
Q247	TRANS, PNP BC 856BL	TG-287
Q252, 253	DIODE CURRENT REG CR200 (T0-46)	TG-218
Q401, 408	TRANS, P CHANNEL JFET, J270 (T0-92)	TG-166-1
Q404, 409, 411-413, 417, 421, 422	TRANS, N-CHAN JFET, SST4416	TG-241
Q410, 415	TRANS, N-CHANNEL FET, BUK 456-1000B (T0-220)	TG-247
Q414	TRANS, N-CHAN JFET, SST4391	TG-250
Q416	TRANS, CURRENT REGULATOR, CR430	TG-219
Q418	TRANS, N-CHAN, DUAL JFET, U441	TG-235
Q420, 424	TRANS, N-CHANNEL FET, J210 (T0-92)	TG-176
Q423	TRANS, N-CHAN JFET SMP4338	TG-257
Q425-427	TRANS, N-MOSFET, VN0605T	TG-243
Q428	TRANS, N-MOSFET, VN0605T	TG-243
R101	RES, 470, 5%, 10W, VERTICAL MOUNT	R-401-470
R102, 103, 128	RES, 20K, 5%, 250MW, METAL FILM	R-376-20K
R104, 235	RES, 243K, 1%, 125MW, METAL FILM	R-391-243K
R105, 229, 230	RES. 140K, 1%, 125MW, METAL FILM	R-391-140K
R106, 123, 126, 224, 227, 233, 484, 487	RES, 499K, 1%, 125MW, METAL FILM	R-391-499K
R107, 201-206, 212, 244, 253-257, 279, 293-300, 313, 321, 385, 394, 431, 474	RES, 100K, 1%, 125MW, METAL FILM	R-391-100K
R108, 111, 112, 116, 125, 416, 454, 463, 469-471, 479	RES, 10K, 5%, 125MW, METAL FILM	R-375-10K
R109	RES, 59K, 1%, 12,MW, METAL FILM	R-391-59K
R110	RES, 243K, 1%, 125MW, METAL FILM	R-391-243K
R113	RES, 1M, 5%, 1/2W, FLAME PROOF	R-394-1M
R114, 417, 418, 441, 448, 450, 459, 481	RES, 1K, 5%, 125MW, METAL FILM	R-375-1K
R115, 266, 278, 281, 414, 455, 467	RES, 4.7K, 5%, 125MW, METAL FILM	R-375-4.7K
R117, 322, 494	RES, 33, 5%, 250MW, METAL FILM	R-376-33
R118	RES, 1K, 5%, 250MW, METAL FILM	R-376-1K
R119	RES, 562K, 1%, 125MW, METAL FILM	R-391-562K
R120, 252	RES, 2.49K, 1%, 125MW, METAL FILM	R-391-2.49K
R121, 340, 348	RES, 475, 1%, 125MW, METAL FILM	R-391-475
R122, 124, 307, 309, 372	RES, 20K, 5%, 125MW, METAL FILM	R-375-20K
R127, 420	RES, 100K, 5%, 125MW, METAL FILM	R-375-100K

Table 4-3
Model 2002 analog board parts list (cont.)

Circuit desig.	Description	Keithley part number
R207-210, 249	RES, 270, 5%, 250MW, METAL FILM	R-376-270
R211, 245-248, 274, 284, 298, 317, 330, 351, 375, 378, 379, 383, 387, 389, 398, 466	RES, 1K, 1%, 125MW, METAL FILM	R-391-1K
R213, 223, 236, 241, 242, 292, 301-303, 305, 306, 308, 357, 358, 401, 403, 411, 422, 429, 475, 499, 500	RES, 1M, 5%, 125MW, METAL FILM	R-375-1M
R214, 219, 222, 228, 231, 304, 345, 354, 366, 464	RES, 49.9K, 1%, 125MW, METAL FILM	R-391-49.9K
R215-218, 220, 221, 234, 409	RES, 150K, 5%, 125MW, METAL FILM	R-375-150K
R225, 226, 232, 250, 291, 320, 343, 347, 370, 371, 373, 374, 404, 491	RES, 10K, 1%, 125MW, METAL FILM	R-391-10K
R237, 239, 399	RES, 182, 1%, 125MW, METAL FILM	R-391-182
R238, 363, 364	RES, 1M, 5%, 125MW, METAL FILM	R-375-1M
R240	RES NET, 100K, 100K, 0.1%, 100MW THINFILM	TF-237-1
R243, 384	RES, 499, 1%, 125MW, METAL FILM	R-391-499
R251, 381, 391	RES, 200K, 1%, 125MW, METAL FILM	R-391-200K
R258-263	RES, 220, 5%, 125MW, METAL FILM	R-375-220
R264, 265	RES, 68.1K, 0.1%, 1/8W METAL FILM	R-377-68.1K
R267, 280	RES, 13K, 5%, 125MW, METAL FILM	R-375-13K
R268	RES NET, 13.1K, 13.3K, 0.1%, 100MW, THINFILM	TF-237-3
R269	RES, 120, .1%, .25W, PRECISION WIREWOUND	R-421-120
R270	RES, 1K, 1%, .3W, 300V, METAL FOIL	R-412-1K
R271	RES, 7.5K, 1%, .3W, 300V, METAL FILM	R-412-7.5K
R272	RES, 75K, 1%, .3W, 300V, METAL FOIL	R-412-75K
R275, 390	RES, 1K, 1%, 125MW, METAL FILM	R-391-1K
R276, 285	RES NET, 3K, 12K, 0.1%, 100MW, THINFILM	TF-237-2
R277	RES, 750K, 1%, 1/8W, 300V, WIREWOUND	R-413-750K
R282, 283, 323, 329, 331, 352, 382	RES, 10, 5%, 125MW, METAL FILM	R-375-10
R286	RES NET, 500, 24.5K METAL FOIL	TF-244
R287, 296, 297, 318, 326, 327, 368	RES, 330, 5%, 125MW, METAL FILM	R-375-330
R288	RES, 357, 1%, 125MW, METAL FILM	R-391-357K
R289	RES, 2.15K, 5%, 250MW, METAL FILM	R-376-2.15K
R290, 316, 353, 421, 427, 437, 439	RES, 22K, 5%, 125MW, METAL FILM	R-375-22K
R310, 312	RES, 82.5, 1%, 125MW, METAL FILM	R-391-82.5
R311, 299, 349	RES, 100, 1%, 125MW, METAL FILM	R-391-100
R314, 465, 493	RES, 4.99K, 1%, 125MW, METAL FILM	R-391-4.99K
R315	RES, 2.2M, 10%, 1/2W, 1.5KV, METAL OXIDE	R-367-2.2M
R319	RES, .91, .1, 1/4W WIREWOUND	R-95-.91
R324, 325	RES, 2K, 1%, 125MW, METAL FILM	R-391-2K
R332, 395, 396, 405, 412, 461, 496	RES, 15K, 1%, 125MW, METAL FILM	R-391-15K
R334	RES, 273, .1%, 1/2W, 350V, METAL FILM	R-135-273
R335, 339, 341, 346	RESISTOR BOARD:	
	PC BOARD (QTY 1)	2002-192
	RESISTOR NETWORK (QTY 1)	TF-255
	CONNECTOR PIN (QTY 6)	CS-682

Table 4-3
Model 2002 analog board parts list (cont.)

Circuit desig.	Description	Keithley part number
R342	RES, 1.5K, 5%, 250MW, METAL FILM	R-376-1.5K
R350, 380	RES, 18.7, 1%, 125MW, METAL FILM	R-391-18.7
R359-361	RES, 5K, .1%, WIREWOUND	R-249-5K
R362	RES, .1, 1%, 2W, 4-TERMINAL MOLDED	R-342-.1
R365, 367	RES, 49.9K, 1%, 100MW, THICK FILM	R-418-49.9K
R376	RES, 909, 1%, 1W, THICK FILM	R-418-909
R377	RES, 768, 1%, 100MW, THICK FILM	R-418-768
R386, 440	RES, 49.9, 1%, 125MW, METAL FILM	R-391-49.9
R388	RES, 1.8M, 5%, 125MW, METAL FILM	R-375-1.8M
R392, 397, 443	RES, 665, 1%, 125MW, METAL FILM	R-391-665
R393, 456, 468	RES, 3.3K, 5%, 125MW, METAL FILM	R-375-3.3K
R402, 419, 442, 480	RES, 150, 5%, 125MW, METAL FILM	R-375-150
R406, 407, 425	RES, 470, 5%, 125MW, METAL FILM	R-375-470
R408, 436, 458	RES, 487K, 1%, 125MW, METAL FILM	R-391-487K
R410, 473, 498	RES, 33K, 5%, 125MW, METAL FILM	R-375-33K
R413	RES, 100, 5%, 125MW, METAL FILM	R-375-100
R415	RES, 10K, 5%, 125MW, METAL FILM	R-375-10K
R423	RES, 10M, 5%, 125MW, METAL FILM	R-375-10M
R424, 435, 446	RES, 120K, 5%, 125MW, METAL FILM	R-375-120K
R426, 462	RES, 2K, 5%, 125MW, METAL FILM	R-375-2K
R428	RES, 120K, 5%, 250MW, METAL FILM	R-376-120K
R430	RES, 39K, 5%, 250MW, METAL FILM	R-376-39K
R432	RES, 330, 5%, 125MW, METAL FILM	R-375-330
R433	RES, 620, 5%, 250MW, METAL FILM	R-376-620
R434, 449	RES, 68, 5%, 125MW, METAL FILM	R-375-68
R438	RES, 2.15K, 1%, 125MW, METAL FILM	R-391-2.15K
R444	RES, 1K, 5%, 125MW, METAL FILM	R-375-1K
R445, 451	RES, 7.5K, 5%, 125MW, METAL FILM	R-375-7.5K
R447, 485, 486	RES, 68K, 5%, 125MW, METAL FILM	R-375-68K
R452	RES NET, 250K, 9.34K, 1K, 10.233K, 15K, 7K	TF-226
R453	RES NET, 1K, 1K	TF-227
R457	RES, 3.3K, 5%, 125MW, METAL FILM	R-375-3.3K
R460, 476, 497	RES, 6.65K, 1%, 125MW, METAL FILM	R-391-6.65K
R472	RES, 15K, 1%, 125MW, METAL FILM	R-391-15K
R477, 483	RES, 1K, 1%, 1/2W FUSIBLE METAL FILM	R-370-1K
R478	RES, 90.9K, 1%, 125MW, METAL FILM	R-391-90.9K
R482	RES, 137, 1%, 125MW, METAL FILM	R-391-137
R488	RES NET, 1100K@ .990W, 11.111K@ .010W, 1%	TF-225
R489	RES, 2.74K, .1%, 1/10W, METAL FILM	R-263-2.74K
R490	RES, 11K, 1%, 125MW, METAL FILM	R-391-11K
R492	RES, 100K, 5%, 1/4W, COMPOSITION OR FILM	R-76-100K
R495	RES, 7.5K, 1%, 125MW, METAL FILM	R-391-7.5K
S101	SWITCH, PUSHBUTTON (6 POLE)	SW-466
S201	SWITCH, PUSHBUTTON, 8 POLE	SW-468

Table 4-3
Model 2002 analog board parts list (cont.)

Circuit desig.	Description	Keithley part number
U101, 237, 421	IC, MOSFET DRIVER, TLP590A	IC-812
U102, 405	IC, VOLT COMPARATOR, LM311M	IC-776
U103, 104	IC, OPTO-COUPLER, HIGH EMI, H11AV1A	IC-845
U105	IC, VOLTAGE REGULATOR, LM317T	IC-317
U106	IC, TIMING CIRCUIT, MC1455D	IC-847
U107	IC, NEG VOLTAGE REG -15V, 500MA, 79M15	IC-195
U108	IC, VAR POS VOLTAGE REG, 100MA, 78L05A	IC-223
U109	IC, POS VOLTAGE REG +15V, 500MA, 7815	IC-194
U110	IC, +5V VOLTAGE REGULATOR, LM2940CT	IC-576
U201	IC, CMOS QUAD R-S LATCH, MC14044BD	IC-915
U202	IC, OP-AMP, LOW NOISE, OP27GS	IC-914
U203, 206, 207, 221, 224, 400, 406, 411, 432	IC, 8 STAGE SHIFT/STORE, MC14094BD	IC-772
U204	IC, SUPPLY VOLT SUPERVISOR, TL7705A	IC-860
U205	IC, HI-SPEED BIFET OP-AMP, AD711JR	IC-894
U208-212	IC, OPTOCOUPLER, TLP582	IC-689
U213, 214, 229, 240, 429	IC, QUAD COMPARATOR, LM339D	IC-774
U215, 239, 407	IC, VOLT COMPARATOR, LM393D	IC-775
U216, 409, 415	IC, QUAD 2-INPUT NAND, 74HC00M	IC-781
U217, 233, 238	IC, OP-AMP, AD705JR	IC-814
U218	IC, DUAL SWITCHED CAP, LTC1043CS	IC-912
U219	IC, ULTRA PRECISION REF, LT21000A (PKG H8)	IC-858
U220, 234, 425	IC, CMOS ANAL. SWITCH, DG411DY	IC-785
U222, 414	IC, 8-CHAN ANA MULTIPLEXER, DG408DY	IC-844
U223, 232	IC, CENTRIGRADE TEMP SENSOR LN35DM	IC-906
U226	IC, 22V, OP-AMP, LT1007ACN8	IC-422
U227, 242, 244, 412, 413, 418, 423, 428	IC, CMOS ANAL SWITCH, DG444DY	IC-866
U228, 257, 404	IC, NCHAN LAT DMOS QUADFET, SD5400CY	IC-893
U230, 235	IC, PHOTO, DARLINGTON TRANS, PS2506L-1	IC-911
U231	IC, CMOS ANA SWITCH SPST MAX326CSE	IC-909
U236	IC, OP-AMP, DUAL PREC. LT1013DS8	IC-913
U241, 249, 427	OP-AMP, LTC1050CS8	IC-791
U245	IC, OP-AMP, LOW NOISE LT1007C58	IC-949
U246, 251, 252	IC, MOSFET DRIVER, TLP591B	IC-877
U247	MODULE, DC/DC CONVERTER, +/-12VDC, HPR116	MO-37
U248, 250	IC, DUAL PICOAMP OP-AMP AD706JR	IC-910
U253	IC, OP-AMP, AD707KR	IC-948
U254, 255	IC, 8-B, SER-OUT, SHIFT REG, 74HC165D	IC-916
U256	IC, BIFET, OP AMP, AD712JR	IC-834
U401	IC, -5V REGULATOR, 79L05ACM	IC-787
U402	IC, RETRIG., MULTIVIB, 74HC123AM	IC-788
U408	IC, VOLT. COMPARATOR, LT1016CS8	IC-797
U410	IC, OP-AMP LT1223C58	IC-873
U416, 431	IC, OP-AMP, AD847JR	IC-779
U417, 419	IC, OP-AMP, AD848JR	IC-784
U420	IC, TRMS TO DC CONVERTER, 637JR	IC-796
U426	IC, DUAL OP-AMP, LF353M	IC-842
U430	IC, DUAL OP-AMP, 1458	IC-811
U433	IC, DUAL 8-BIT DAC, MP7528JS	IC-810

Table 4-3
Model 2002 analog board parts list (cont.)

Circuit desig.	Description	Keithley part number
V243	IC, TRI-2CH MULTI-DEMUX, 4053	IC-770
V403, 422, 424, 425	IC, 20V OP-AMP, LT1097S8	IC-767
VR101	DIODE, ZENER 22V, BZX84C22	DZ-86
VR102, 104, 206, 211, 213	DIODE, ZENER 6.2V, BZX84B6V2	DZ-87
VR103	DIODE, ZENER, 39V, MLL4716	DZ-95
VR201, 202, 204	DIODE, ZENER 5.1V, BZX84C5V1	DZ-88
VR203, 208, 215, 404	DIODE, ZENER, 4.3V, BZX84C4V3	DZ-85
VR205, 207, 218, 219, 402	DIODE, ZENER, 8.2V, MMBZ5237	DZ-92
VR209, 210	DIODE, ZENER, 22V, BZV55C22	DZ-96
VR214	VAR, 576V METAL OXIDE	VR-5
VR216	DIODE, ZENER 10V MMSZ5240B	DZ-99
VR217	DIODE, ZENER 6.44V, IN4577AGED (D0-7)	DZ-58
VR401	DIODE, ZENER, 10V, IN5240C (D0-35)	DZ-93
VR403, 405	DIODE, ZENER 15V, 1N4744A (T0-41)	DZ-75

Table 4-4
Model 2002 digital board, parts list

Circuit desig.	Description	Keithley part number
	CONN, BERG	CS-339
	CONN, MALE 3 PIN	CS-612-1
	DIGITAL ASSEMBLY	2002-140
C602, 603, 605-607, 620, 636-640, 665-667	CAP, .1UF, 20%, 50V, CERAMIC	C-418-.1
C604, 661	CAP, .1UF, 20%, 50V, CERAMIC	C-418-.1
C609	CAP, .1UF, 20%, 100V, CERAMIC	C-436-.1
C611	CAP, 15000UF, 20%, 16V, ALUM ELEC	C-450-15000
C613, 619, 632	CAP, 10UF, 20%, 25V, TANTALUM	C-440-10
C617, 618	CAP, 33PF, 10%, 100V, CERAMIC	C-451-33P
C621-623, 626-628, 664	CAP, .01UF, 20%, 50V, CERAMIC	C-418-.01
C624, 630, 633	CAP, 1000UF, +/-20%, 16V, ALUMINUM	C-488-1000
C625	CAP, 47UF, 10%, 16V, ALUM ELEC	C-321-47
C631	CAP, 3.3UF, 20%, 50V, POLY-FILM	C-470-3.3
C641-659, 671, 672	CAP, 270PF, 20%, 100V, CERAMIC/FERRITE	C-386-270P
C668	CAP, .01UF, 20%, 50V, CERAMIC	C-418-.01
CR602-619, 626	DIODE, SWITCHING, 250MA, BAV103	RF-89
CR622	DIODE, BRIDGE PE05 (CASE KBU)	RF-48
CR624, 625	DIODE, SILICON, IN4006 (D0-41)	RF-38
CR627, 628	DIODE, ARRAY, MMAD1103	RF-80
J1027	CONN, HEADER STRAIGHT SOLDER PIN	CS-368-20
J1028	CONN, RIGHT ANGLE, 24PIN	CS-507
J1029, 1030	CONN, MICRODIN W/GND FINGERS	CS-792
J1031	CONN, RT ANGLE, MALE, 9 PIN	CS-761-9
J1032	CONN, RT ANGLE, MALE MOLEX .156	CS-715-4
J1033	CONN, HEADER STRAIGHT SOLDER PIN	CS-368-16
J1034	CONN, MALE RT ANGLE, 32-PIN	CS-456
L603-607	CHOKE, SHIELD BEAD	CH-52
Q602-607	TRANS, N CHAN MOSPOW FET, 2N7000 (T0-92)	TG-195
Q608	TRANS, N-CHANNEL FET, RN06L	TG-216
R601, 603-605, 610, 672	RES, 2K, 1%, 125MW, METAL FILM	R-391-2K
R616, 621, 625, 629, 631	RES, 10, 5%, 125MW, METAL FILM	R-375-10
R639	RES, 580K, 5%, 125MW, METAL FILM	R-375-680K
R644	RES NET, 4.7K, 2%, 1.875	TF-219-4.7K
R648-650, 655-657	RES, 5.1K, 5%, 125MW, METAL FILM	R-375-5.1K
R663, 677	RES, 4.7K, 5%, 125MW, METAL FILM	R-375-4.7K
R665	RES, 470, 5%, 125MW, METAL FILM	R-375-470
R667, 669	RES, 560, 5%, 250MW, METAL FILM	R-376-560
R668, 717, 720	RES, 10K, 5%, 250MW, METAL FILM	R-376-10K
R670, 675	RES, 100, 5%, 250MW, METAL FILM	R-376-100
R705	RES, 15K, 1%, 125MW, METAL FILM	R-391-15K
R706, 708, 711, 729	RES, 10K, 1%, 125MW, METAL FILM	R-391-10K
R707	RES, 150, 5%, 250MW, METAL FILM	R-376-150
R709	RES, 14K, 1%, 125MW, METAL FILM	R-391-14K
R710, 716	RES, 1M, 5%, 250MW, METAL FILM	R-376-1M

Table 4-4
Model 2002 digital board, parts list (cont.)

Circuit desig.	Description	Keithley part number
R712	RES, 100K, 1%, 125MW, METAL FILM	R-391-100K
R713	RES, 200K, 1%, 125MW, METAL FILM	R-391-200K
R714	RES, 4.7K, 5%, 250MW, METAL FILM	R-376-4.7K
R715, 743-748, 752-755, 757	RES, 100, 5%, 125MW, METAL FILM	R-375-100
R718, 719, 730	RES, 1K, 5%, 250MW, METAL FILM	R-376-1K
R721	RES, 2.15K, 5%, 250MW, METAL FILM	R-376-2.15K
R732-735, 737-742, 749, 771	RES, 10K, 5%, 125MW, METAL FILM	R-375-10K
R736	RES, 10K 5%, 125MW, METAL FILM	R-375-10K
R758-763	RES, 39, 5%, 125MW, METAL FILM	R-375-39
R768, 769	RES, 100, 5%, 125MW, METAL FILM	R-375-100
R772	RES, 47K, 5%, 125MW, METAL FILM	R-375-47K
TP601, 602, 603	CONN, TEST POINT	CS-553
U608	IC, (8KX8) HI SPEED STATI CMOS RAM, 6264	LSI-141
U612	IC, 350MA SATURATED SINL DRIVER UDN-2596A	IC-578
U614	IC, OCT BFR/LINE DRIVE, 74HCT244	IC-651
U615, 630	IC, QUAD 2 IN NOR, 74HCT02	IC-809
U616	IC, QUAD 2 INPUT OR, 74HCT32	IC-808
U618	PROGRAMMED, EPROM, EPM5064LC(PLCC)	2001-801-*
U619, 629	IC, +5V VOLTAGE REGULATOR, LM2940CT	IC-576
U620	IC, DUAL POWER-SUPPLY SUPER, TL7770-5	IC-805
U621	IC, OCTAL INTERFACE BUS, 75160	IC-646
U622	IC, GPIB ADAPTER, 9914A	LSI-123
U623	IC, OCTAL INTER BUS TRANS, 75161	IC-647
U627	IC, 18V OP-AMP, TLC 271	IC-347-1
U628	IC, VOLT COMPARATOR LM393D	IC-775
U631	IC, 16-BIT MICRO, MC68302FC	LSI-144
U633, 634	IC, SERIAL E EPROM, X24164 (8-PIN DIP)	IC-885
U635, 636	IC, 32KX8 STAT CMOS RAM, D43256C	LSI-93-100
U637	PROGRAMMED, IC, 4M, CMOS EPROM, AT27C040-15DC	2002-803-*
U638	PROGRAMMED, IC, 4M, CMOS EPROM, AT27C040-15DC	2002-804-*
VR602, 603	DIODE, ZENER 4.7V, IN4732A	DZ-67
W605, 606	CONN, 3 PIN	CS-339-3
W606	CONNECTOR, JUMPER	CS-476
Y602	CRYSTAL, 16MHZ	CR-30-16M

* Order correct firmware revision number. For example: 2002-803-A03

Table 4-5
Model 2002 miscellaneous, parts list

Circuit desig.	Description	Keithley part number
	1/4X1/4X.2 PAD, THERMAL	HS-46A
	BANANA JACK, PUSH-IN, BLACK	BJ-13-0
	BANANA JACK, PUSH-IN, RED	BJ-13-2
	BEZEL, REAR	428-303D
	CHASSIS	2001-303
	CHOKE	CH-58-1A
	COVER	2001-360C
	DISK PROGRAMMING	2002-DSK-81
	DISPLAY LENS	2002-305C
	DISPLAY SHIELD	2001-304
	FAN, DC BRUSHLESS, 12VDC, 100MA	FN-26
	FILTER, FAN	2001-353C
	FOOT	428-319A
	FOOT, EXTRUDED	FE-22A
	FOOT, RUBBER	FE-6
	FRONT/REAR SWITCH ROD	2001-322A
	FUSE, 2A, 250V, FAST-BLO(5X20MM)	FU-48
	HANDLE	428-329F
	LEXAN, ANALOG BOTTOM SHIELD	2001-340B
	LEXAN, SHIELD, CHASSIS-RIGHT	2001-336B
	MOUNTING EAR, LEFT	428-338B
	MOUNTING EAR, RIGHT	428-328E
	POWER ROD	2001-320A
	PRINTED, FRONT PANEL	2001-356C
	SHIELD	2002-325A
	SHIELDED, ANALOG BOTTOM SHIELD	2001-339C
	SHIELDED, ANALOG TOP SHIELD	2002-324A
	TRANSFORMER	TR-280D
J1001	CONN, AC RECEPTACLE (LINE FILTER)	LF-6-1
J1003, 1005, 1014, 1016	BANANA JACK, PUSH-IN, RED	BJ-13-2
J1004, 1006, 1013, 1015	BANANA JACK, PUSH-IN, BLACK	BJ-13-0
J1012	BANANA JACK, PUSH-IN, WHITE	BJ-13-9
P1002	CONN, MOLEX HEADER	CS-716-3
P1037	CONNECTOR, HOUSING	CS-638-3

A

Specifications

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KEITHLEY

Service Form

Model No. _____ **Serial No.** _____ **Date** _____

Name and Telephone No. _____

Company _____

List all control settings, describe problem and check boxes that apply to problem. _____

_____

_____

❑ Intermittent
❑ IEEE failure
❑ Front panel operational
❑ Analog output follows display
❑ Obvious problem on power-up
❑ All ranges or functions are bad
❑ Particular range or function bad; specify _____
❑ Batteries and fuses are OK
❑ Checked all cables

Display or output (check one)

❑ Drifts
❑ Unstable
❑ Overload
❑ Unable to zero
❑ Will not read applied input

❑ Calibration only
❑ Data required
❑ Certificate of calibration required

(attach any additional sheets as necessary)

Show a block diagram of your measurement system including all instruments connected (whether power is turned on or not). Also, describe signal source.

Where is the measurement being performed? (factory, controlled laboratory, out-of-doors, etc.)

_____

_____

What power line voltage is used? _____ Ambient temperature? _____ °F

Relative humidity? _____ Other? _____

Any additional information. (If special modifications have been made by the user, please describe.)

_____

_____

Be sure to include your name and phone number on this service form.