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In this Issue:

Regular readers may notice a new item in our table of contents this month. Author biographical sketches are now grouped in a special section instead of being spread around among the articles. We expect that the author section will be a regular feature.

Our cover subject this month is the elegantly simple magnetic card reader of the HP-75 Portable Computer. The entire card reader, which is also a recorder, consists of a magnetic head, a head fixture, a single integrated circuit, and a slot to guide the card. There's no motor; the user pulls the card through the reader manually, so one of the challenges in the design of the reader IC was to make it adapt to a wide range of pulling speeds.

The HP-75 is the first HP computer of its kind. Its design is discussed on pages 3 to 26 of this issue. About the size of a book, it's briefcase-portable and BASIC-programmable, runs on batteries, and retains programs and data when turned off. Along with it in that briefcase, a user can take a magnetic tape cassette drive for storing large amounts of data, a printer/plotter for hard copies of results, an acoustic modem for telephone access to a remote computer, and a video interface for displaying information on a television monitor. In other words, the HP-75 lets a traveling professional person turn a hotel room, an airline seat, or anyplace else into an office. There goes one more excuse for not working.

On pages 27 to 38, you'll find the design story of a trio of basic test instruments that are notable because they're all derived from the same three custom HP integrated circuits. One of the instruments is a pulse generator, and the other two are function generators that have enough pulse-generator capabilities to be given the name pulse/function generators. Their designers have exploited custom IC technology to lower costs and provide extra functions that let each of the instruments do a greater variety of jobs than other instruments in its class. It's the old IC story of more capability for less money, applied to a family of products.

-R. P. Dolan

A Portable Computer for Field, Office, or Bench Applications

This lightweight, battery-powered computer has features that make it an ideal tool for the traveling professional.

by Donald E. Morris, Anthony S. Ridolfo, and Donald L. Morris

ONLY A FEW PROFESSIONAL PEOPLE today are able to do their work effectively without some access to the many computation and information management tools provided by computer systems. Until recently, this access was limited to fixed-base installations where ac power is available.

To meet the growing need for computer capabilities that can be used anywhere, anytime, Hewlett-Packard has developed the HP-75 Portable Computer (Fig. 1). It weighs only 26 ounces and with other small HP battery-operated peripherals such as an acoustic modem, a digital cassette drive, and a printer/plotter, can fit easily into a briefcase to form a complete, yet portable information management system (see Fig. 2 on page 8). Some of the features contained in the HP-75's small 10×5×1.25-inch package are:

- Touch-type keyboard with extra keys for control and editing. There are 194 keycodes available and the keys can be redefined by user programs or ROM.
- Integral BASIC language system in a 48K-byte ROM that provides 50 functions, 6 time-mode commands, 43 statements, and 52 system commands (see Table I). A multiple file structure provides ready access to frequently used programs.
- Liquid-crystal display that shows up to thirty-two 5×8 dot-matrix characters. Lines can be up to 96 characters long and the display can be scrolled left or right to view any 32-character section of a line.
- 16K bytes of nonvolatile user memory, expandable to 24K bytes
- Three ROM ports that can hold up to 96K bytes of appli-

Fig. 1. *The HP-75 Portable Computer is battery-powered, has a nonvolatile memory, and provides a wide variety of computational and file handling features in a small package that can be taken with you to solve problems, collect and supply information, compile reports, and even remember appointments.*

cations modules
- Built-in magnetic card reader for low-cost program and data storage and input
- CMOS circuitry and a battery supply that allow up to a month of normal use without recharging
- Appointment mode with 10 different audible alarms that can serve as a calendar, appointment book, or alarm clock
- Built-in HP-IL (Hewlett-Packard Interface Loop)[1] interface for connection to a variety of HP-IL-compatible peripherals and instruments

Table I

HP-75 Command Set Summary

System Commands:

ALARM OFF	DELETE	PRINTER IS
ALARM ON	DISPLAY IS	PROTECT
ASSIGN IO	EDIT	PURGE
AUTO	ENDLINE	PWIDTH
BEEP OFF	FETCH	RENAME...TO
BEEP ON	FETCH KEY	RENUMBER
BYE	INITIALIZE	RESTORE IO
CAT	LIST	RUN
CAT ALL	LIST IO	STANDBY OFF
CAT CARD	LOCK	STANDBY ON
CLEAR LOOP	MARGIN	TRACE FLOW
CLEAR VARS	MERGE	TRACE OFF
CONT	NAME	TRACE VARS
COPY	OFF IO	TRANSFORM
DEFAULT ON	OPTION ANGLE DEGREES	UNPROTECT
DEFAULT OFF	OPTION ANGLE RADIANS	WIDTH
DEF KEY	PACK	
DELAY	PLIST	

BASIC Statements:

ASSIGN #	GOSUB	ON ERROR	READ
BEEP	GOTO	ON TIMER #	READ #
CALL	IF...THEN...ELSE	ON...GOSUB	REAL
DATA	IMAGE	ON...GOTO	REM
DEF FN	INPUT	OPTION BASE	RESTORE
DIM	INTEGER	POP	RESTORE #
DISP	LET	PRINT	RETURN
DISP USING	LET FN	PRINT #	SHORT
END	NEXT	PRINT USING	STOP
END DEF	OFF ERROR	PUT	WAIT
FOR...TO...STEP	OFF TIMER #	RANDOMIZE	

Numeric Functions:

ABS	COS	ERRL	INT	MEM	RAD	SIN
ACOS	COT	ERRN	IP	MIN	RES	SQR
ANGLE	CSC	EXP	LEN	MOD	RMD	TAN
ASIN	DATE	FLOOR	LOG	NUM	RND	TIME
ATN	DEG	FP	LOG10	PI	SEC	VAL
CEIL	EPS	INF	MAX	POS	SGN	

String Functions:

CAT$ CHR$ DATE$ KEY$ STR$ TIME$ UPRC$ VER$ TAB

Time Mode Commands:

ADJST EXACT EXTD RESET SET STATS

Arithmetic, Relational, and Logical Operators:

ARITHMETIC:	+, −, *, /, ^, DIV or \
RELATIONAL:	=, <> or #, >, >=, <, <=
LOGICAL:	AND, OR, EXOR, NOT

- Programmable (duration and frequency) beeper
- Real-time clock with perpetual calendar and timing functions.

Developing a Portable Computer

The development of the HP-75 Portable Computer presented many challenges for its designers. The engineering solutions required new and evolving technologies to support the innovations that came about in hardware, software, and machine concepts.

Two trends in the data processing field have helped determine the nature of the HP-75. The trend of longest duration is the decreasing cost for a given computational capability. At first glance, the HP-75 fits this category; it has the computational capability of HP's Series 80 Computers and uses the same internal software routines for less than one-third the price. However, the goal was not simply to lower the cost per function, but rather to develop a different machine. The other trend, increasing capability for the same price, began with the introduction of the HP-35 Calculator in 1972. This trend has led to a progression of new handheld calculators with ever-increasing capabilities. The latest models, such as the HP-41 Handheld Computer, have performance equal to that available only in computers of earlier times.

The desire to bring strong computational capability to both new users and new applications where portability is a key element shaped the musts and wants of the HP-75 project. To be portable, a machine should be small, battery powered, and have a long battery life. To meet the minimum definition of a computer, I/O, data communications, and peripheral support are required. Portability also requires that the minimum configuration be fully functional and appropriate for a large portion of the tasks encountered.

In the HP-75's minimum configuration, many features that would normally be optional and require additional pieces of hardware are built in. For instance, the minimum configuration contains the I/O interface, a mass data storage device, a line display, timing and calendar features, and software for a wide range of applications.

Because of the small size and weight requirements of the HP-75, the battery used in the HP-35 Handheld Calculator (1½ watt-hour) was chosen. This presented the challenge of creating a computer with high computational power that uses, on the average, less than 50 milliwatts of power. This constraint led to the design decision to use a liquid-crystal display, entirely CMOS circuitry, very low-power interface circuitry (HP-IL), and a high-efficiency switching power supply. The handpulled card reader also evolved as a result of the limited energy available.

The handpulled card reader presented a number of design challenges (see article on page 15 for the complete story). One of these was the magnetic head, which is required to read a clock track while writing the data. This requires a magnetic head with very strict crosstalk requirements. A second challenge was the design of the very high-speed digital circuitry required to decode the recorded data. Another was the design of analog card reader circuitry into a CMOS integrated circuit (see article on page 24).

The small size of the HP-75 dictates the use of high-

(continued on page 6)

A Telephone Interface for HP-IL Controllers

by Sidnee Snell and Brian G. Spreadbury

The ability to access remote data bases and programs via standard telephone lines greatly enhances the usefulness of a portable computer. This feature allows field sales personnel to access their office computer for the latest ordering information. Service personnel can download diagnostic programs from a remote central computer and run them locally to help solve problems in the field. Up-to-the-minute investment and other information is available from public or private data base services.

To provide this ability to access remote information, an acoustically coupled modem is required because direct-connection modems cannot be used with telephones in public booths and most hotel or motel rooms. This modem also must be portable and battery-powered. Although an answer mode capability might be useful in some instances, it is not, in general, a necessary feature for many remote applications.

With these requirements in mind, HP developed the 82168A Acoustic Coupler (Fig. 1), an acoustically coupled, full-duplex, originate-only modem with an HP-IL (Hewlett-Packard Interface Loop)[1] interface. Transmitting at 300 baud, it uses frequency-shift keying (FSK). The mark and space transmit frequencies are 1070 Hz and 1270 Hz, respectively. All current HP-IL controllers can be used with the 82168A. It implements the HP-IL's talker and listener functions and the auto address, accessory ID, and device ID functions.

A rechargeable nickel-cadmium battery pack provides power to the 82168A for approximately three hours. With the ac line recharger inserted, the unit can run indefinitely. Power on and off are software-controlled. Any activity on the HP-IL causes the 82168A to power up and remain on until receipt of an HP-IL power-down command, until 10 minutes have passed without any loop activity, or until a low-battery condition is detected. The activity timeout and power-down functions can be disabled with an HP-IL remote mode command. The modem will not power up with a low battery.

A two-segment liquid-crystal display (LCD) shows device status. The green segment indicates reception of a carrier from the telephone line. The red segment indicates power on, and when flashing, indicates a low-battery condition that will be followed shortly by loss of power.

Fig. 1. *The HP 82168A Acoustic Coupler can be used to connect any current HP-IL controller such as the HP-75 Portable Computer to a telephone line for transmission of data and programs to another controller or central computer system.*

Since reliable telephone line transmissions are limited to 300 baud, 40-byte input and output buffers are provided to prevent having to slow the HP-IL transmission rate to 300 bits per second. Input buffer overrun is avoided by handshaking with the remote computer. Output buffer overrun is prevented by using HP-IL protocol.

The 82168A has three handshake modes which allow the user to communicate with most computers. In the XON/XOFF mode, the modem responds to an XOFF character by suspending transmission until an XON character is received from the remote computer. The modem transmits an XOFF when the input buffer is almost full to prevent overruns that would result in lost data. When the input buffer becomes empty, an XON is sent to the remote computer to indicate readiness to receive data. In the ENQ/ACK mode, an ACK character is transmitted in response to an ENQ character from the remote computer as soon as the input buffer becomes empty. The third mode allows a user definition of a handshake.

Five parity modes are available for error detection. Like the handshake modes, parity modes are selected by the user via HP-IL remote mode commands. With even parity, the most-significant bit (MSB) in the data byte is set or cleared so that there are an even number of marks in a data byte. Odd parity causes the MSB to be set or cleared for an odd number of marks in every byte. For zero parity, the MSB is always cleared and for one parity, it is always set. The no-parity mode allows 8-bit data to be transmitted.

Electronics Operation

Fig. 2 shows a block diagram of the 82168A's electronics. At the heart of the 82168A design are a CMOS microcomputer and a modulator/demodulator IC. The microcomputer has 4K bytes of internal ROM, 128 bytes of RAM, and a universal asynchronous receiver-transmitter (UART). Eighty bytes of the RAM are used for the input and output buffers and the remaining bytes are used for the stack, flags and status.

The HP-IL interface converts the loop's 11-bit serial data to parallel form. The data is stored in the microcomputer's output buffer. The microcomputer's UART loads data from the output buffer and converts it to a 10-bit serial format suitable for modulation. The modulator has an internal filter and requires a minimum number of additional components for operation. It converts the serial binary data to an FSK-modulated sine wave and filters out harmonics generated in the modulation process. An additional amplifier drives the modem's speaker.

To receive data from the telephone lines, the amplified output of the modem's microphone is filtered to remove noise. The demodulated signal is in a serial binary format. The UART in the microcomputer converts the data to parallel format and stores it in the microcomputer's input buffer. The HP-IL interface then converts the buffered data to an 11-bit serial format for the interface loop.

The green segment of the LCD is controlled by the demodulator. When a carrier signal is received in the correct frequency and amplitude range, the green segment becomes dark. When the signal goes out of range, the segment turns pale, indicating carrier loss. The red segment of the LCD is under microcomputer control. When the microcomputer is powered, it turns the red segment dark. When a low-battery condition is

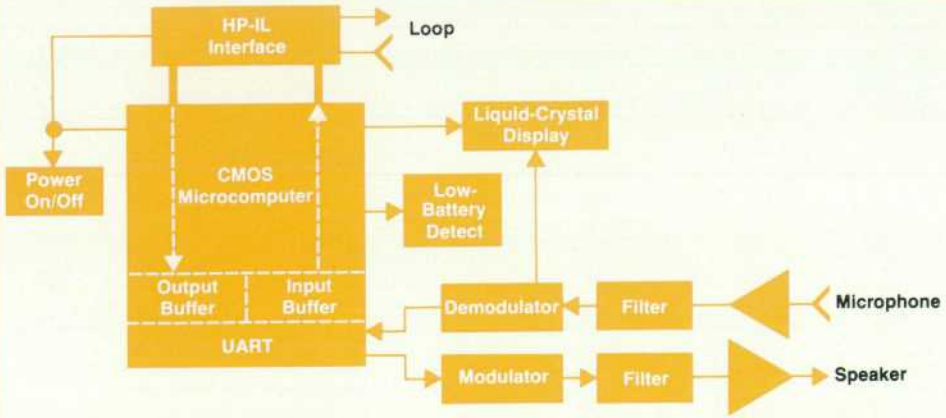

Fig. 2. *Block diagram of the electronics used in the 82168A Acoustic Coupler.*

detected, the microcomputer flashes the red segment at approximately 2 Hz.

The 82168A firmware is interrupt-driven using three service routines: monitoring, HP-IL, and serial interface. The monitoring routine takes advantage of the internal timer and counter. Every 53 ms, the microcomputer is interrupted to check the battery voltage, the carrier detect, and HP-IL activity. If appropriate, a power-down is executed. If no carrier is detected, telephone line transmission is suspended.

The HP-IL service routine handles all HP-IL interface overhead. It differentiates between the remote and local modes for data bytes. In the local mode, data bytes received from the loop are stored in the output buffer for transmission on the telephone line. In the remote mode, data bytes are parsed as 82168A commands to change parity or handshake modes, start and stop data breaks, or set up other software-controlled features.

In the serial interface service routine, the functions relating to telephone transmission are performed. For received data, handshaking is executed to prevent buffer overrun. The input buffer is loaded and all incoming data bytes are error checked. Output data is transferred from the microcomputer's output buffer to its UART. The parity is set or cleared if necessary and the byte is transmitted.

Mechanical Packaging

The main challenge in packaging the 82168A was the design of the rubber speaker and microphone housings (cups). They must effectively isolate the telephone handset from ambient noise and acoustically couple the handset to the 82168A's microphone and speaker. In addition, they should have an aesthetically pleasing low profile.

The rubber cups are located in the upper case by using the cling properties of rubber and an annular groove on three sides to prevent pull-out or push-in during telephone insertion and removal. The material selected for the cups is a chloroprene formulation, which has excellent tear and abrasion resistance, low compression set, and low-temperature flexibility.

The plastic case design is of orthodox construction with top and bottom cases held together by self-tapping screws. Trapped by these case halves are the end-panel plate and I/O plate used for HP-IL cable and battery recharger connections.

The bottom case locates the printed circuit board for the electronics. The top case houses the rubber cups, microphone, speaker, LCD indicator, and battery compartment. The cables from these parts can be quickly disconnected from the printed circuit board. The cables are also long enough to allow the top case to lie alongside the bottom case with a telephone handset installed. This simplifies troubleshooting and adjustment during assembly.

The speaker is a piezoelectric type, selected for its low power requirements, thin profile, and environmentally resistant construction.

The microphone is an electret type, selected for its small size and flat frequency response at the modem's operational frequencies.

The power and carrier indicators are segments of a single LCD, which was selected instead of light-emitting diodes to reduce power consumption. The LCD is of the twisted nematic variety with a reflective rear surface and red and green polarizers on the upper surface. The LCD pinouts are epoxy-bonded to the glass and edge traces, allowing simple attachment to a mass-termination connector for assembly to the printed circuit board.

Acknowledgments

Thanks to all the people who contributed to the 82168A project. Lee Collins was responsible for the firmware design. Gordon Margulieux and Ed Solari worked on the electronics. Dave Rohrer worked on mechanical design. The project manager was Rex Smith.

Reference:

1. R.D. Quick and S.L. Harper, "HP-IL: A Low-Cost Digital Interface for Portable Applications," Hewlett-Packard Journal, Vol. 34, no. 1, January 1983.

density packaging. The HP-75 uses both 44-pin and 60-pin flatpack integrated circuit packages. These packages are approximately 2 cm square and have leads on 0.8-mm spacing. The major design challenges in using flatpacks are process related. The first is to solder the 751 flatpack leads successfully in each HP-75 produced. The importance of this is emphasized by considering that the logic printed circuit board assembly, which has 13 integrated circuits and 513 flatpack leads, requires solder defects of less than one in ten thousand for a good assembly yield in the range of 95%. The second major problem of flatpacks is that the cleanliness of the printed circuit assemblies is crucial.

Both of these problems were resolved by the manufacturing and integrated circuit process teams and the result is the implementation of highly successful soldering and cleaning processes that make the HP-75 resistant to extremes of temperature and humidity.

The small size of the HP-75 required that we move away from our traditional "keep it out" approach to electrostatic discharge (ESD) protection. Because of the high density of

internal components in the HP-75, it was not possible to maintain the minimum 1-cm spark gap between the components and the user. The approach taken is to handle all discharges internally by the interconnection of external overlays, a single internal shield, and system ground. This approach brings all internal component potentials up simultaneously, and coupled with major reductions in integrated circuit susceptibility, results in the HP-75's high resistance to damage caused by electrostatic discharges.

Firmware Design

Traditionally, the design center for HP's personal computer products has been numerical computation. This is not only reflected in the handheld calculators, but also in the HP-85 Computer.[2] The HP-85 was designed for technical computation. Its BASIC language is a derivative of the HP BASIC found in the earlier HP 9800 Series Desktop Computers.[3] The HP-85 keyboard includes a numeric pad. The HP-85 has more built-in numeric functions than the HP-41 Handheld Computer. The HP-85's custom CPU can perform BCD (binary coded decimal) multibyte instructions, which makes numerical algorithms shorter and hence quicker, and return a higher number of accurate digits than other comparable microprocessors.

The HP-75 evolved from the HP-85, but because of the HP-75's personal, portable nature, the design center has subtle differences. The HP-75 was not designed to be a calculator, or even a number cruncher, but rather a tool on which one can develop programs—programs that, among other things, can do sophisticated numerical computations.

File System

Having 24K bytes of memory devoted to only one program is nice, but most of us would find it difficult to create such a large program at one sitting. Rather, most of us create smaller programs or collect small amounts of data and combine them to create larger programs or data bases. Having a CMOS memory means that whatever the user stores into the memory does not go away when the HP-75 is turned off. This feature gave the software design team the opportunity to create a nonvolatile internal file system. The result is a sophisticated multifile system controllable from either the keyboard or a user-written BASIC program.

Any BASIC program is a file. The user creates programs much the same as with any other computer system by entering lines from the keyboard. The HP-75 does syntax checking on the input of each line. To create another program or file, the user must either purge the current file or give it a name so the system can refer to it later. If the file is given a name, it remains in memory until purged.

Files can be manipulated by the user via a number of programmable commands, among which are RENAME, RENUMBER, PURGE, MERGE, LIST, TRANSFORM, EDIT, PLIST (send listing to a printer device), and COPY. The COPY command can make a duplicate copy of a file in RAM, onto magnetic cards, or on a digital cassette.

Not every file is a BASIC program. The clock keyboard chip contains a real-time clock for telling time. This clock is software-adjustable for changes in time zones and refinement of crystal accuracy. A time manager called the appointment mode is implemented in the firmware. The appointment file sets up interrupts that, when triggered, pass user commands or messages to the command interpreter. These commands can include any BASIC statement or statements including RUN filename. The appointment file can be renamed or copied to magnetic cards or cassette. The act of copying the file back into APPT merges the file with the current appointment file automatically and any past due appointment instructions (display message, run a program, etc.) are executed.

Another user-creatable file type is TEXT. This is simply a line-numbered ASCII character file. A text file can contain any string after the line number. These too can be manipulated by the user. In fact, BASIC programs can create TEXT files, read from them, write to them, copy them, merge them, list them, or transform them into BASIC programs. During this last process, lines that do not make syntactic sense are marked by the HP-75 by inserting the characters !? at the beginning of the line. Files can be transformed into LIF 1 files and stored on cards or cassette for transfer to other HP computers. Such files are called logical interchange files, and must be transformed into text or BASIC for editing.

To expand the system, HP offers language extension files (LEX files) on cards, cassettes, and plug-in ROMs. These files are assembly language files that can give the user new BASIC statements or even totally redefine the computer. Although these files are not editable, they can be copied like other files. LEX files offer third-party vendors opportunities to customize the HP-75 to their markets. New keywords can be added and distributed on magnetic media. An example is the I/O utilities card HPILCMDS. This 1300-byte file gives the HP-75 the ability to source or receive any HP-IL message, command, or data frame on the loop. Once read into the computer, the LEX file remains in the system until purged. BASIC programs can then use the keywords it defines to control instruments or other devices on the loop.

Two other capabilities of the file system are important. One is that any BASIC program can CALL any BASIC program, including itself. Parameter passage is through an auxiliary file. The other important capability is that the HP-75 runs BASIC programs in place. That is, a program does not have to be the file currently being edited, nor does it have to reside in RAM. It can reside in a plug-in ROM. Such programs (called BASIC in ROM) are not copied into RAM when executed. Only the variables of the program reside in RAM. The program itself remains in ROM with no speed penalty compared to RAM-based programs. The three plug-in slots in the front of the HP-75 can accommodate 32K bytes of ROM each. This increases the effective address space by 96K bytes. Third parties can create BASIC programs that reside in ROM, plug into the front of the computer, and are safe from unwanted duplication.

The hardware and software combine to give the user a powerful file system with a lot of flexibility and yet keep the number of commands relatively small and coherent. This file system was developed to take advantage of the CMOS memory, mass storage, and I/O capabilities built into the HP-75. One example is that when a text file is PLISTed to a printer, the line numbers are stripped off. Hence, memorandrums can be written on the HP-75 as text files and printed out as if typed.

HP-IL and the HP-75 Portable Computer

by Dennis C. York

The CMOS technology of the new HP-75 Portable Computer provides the capability associated with desktop personal computers in a more personal, highly portable, battery-operable configuration. The HP-75 can serve as a computer, an electronic notebook, and an electronic timepiece and secretary when used in the portable environment. When it is returned to its home base, or used in conjunction with highly portable peripherals, this new computer can function very much like traditional desktop computers. This implies access to hardcopy output devices, mass memory devices, video displays, instruments, and information contained in other computers.

Interfaces such as RS-232-C/V.24 and the HP-IB (IEEE 488) do not provide an adequate communication solution for this new type of computer. Today's battery technology can provide months of normal use for the CMOS circuitry of the computer, but an interface that would require a watt of power poses a severe design constraint. The Hewlett-Packard Interface Loop (HP-IL) provides an attractive solution to this problem.[1]

In the area of personal computation, the HP-IL provides access to several key peripherals for the HP-75 (Fig. 1). Since the display capabilities of the HP-75 are limited by the size of its package, the hardware occasionally needs access to more capable display and hardcopy output devices. Two HP-IL printers are currently available. The 24-character HP 82162A Printer/Plotter is battery-operated for portable applications and the 80-character HP 82905B Dot-Matrix Impact Printer with the HP-IL interface option provides full-page output for the office environment. A video interface for a television or CRT monitor is available to provide 32-

Fig. 2. *This HP-75 system features HP's 82168A Acoustic Modem, 82162A Thermal Printer/Plotter, and 82161A Digital Cassette Drive.*

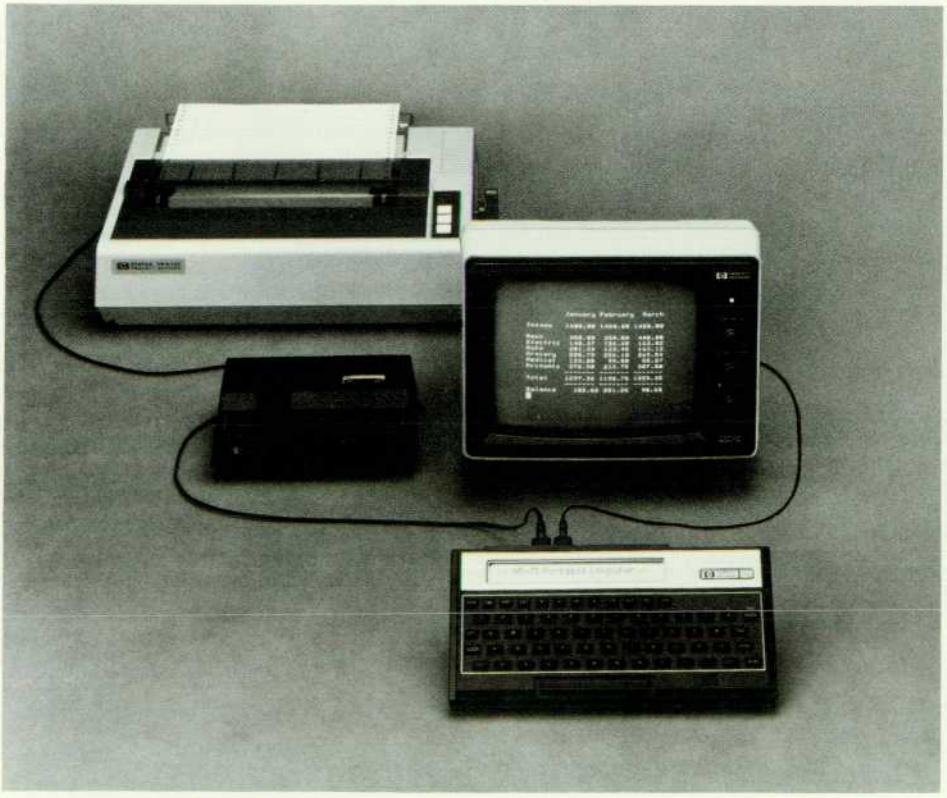

Fig. 1. *This HP-75 system features HP's 82161A Digital Cassette Drive, 82163A Video Interface (plus a video monitor) and 82905B Printer.*

character-by-16 line display capability. This secondary display capability is useful for editing, program development, soft-copy output of results, and group demonstration and instruction.

Personal computation implies access to programs and data. The HP 82161A Digital Cassette Drive[2] provides 128K bytes of mass memory. The HP-75 system firmware provides a capable file-by-name system to make information access simple and friendly. Since the 82161A is also battery-operated, it can accompany the HP-75 in applications requiring portability (Fig. 2).

Field sales and service representatives have been asking for a highly-capable portable computer for some time. They wish to use it as an electronic notebook to make quotes, take orders, account for time, supply reference information, write reports, do computation, and perform many other specialized applications. The HP-75 by itself provides the electronic notebook capability required for most of these applications. However, HP-IL communication will be required periodically to off-load collected information or to update the cache of programs and data in the HP-75's memory. Peripherals such as the HP 82168A Acoustic Modem (see box on page 5) or the HP 82164A HP-IL/RS-232-C Interface can provide the link between the HP-75 and the user's large factory computer.

References

1. R.D. Quick and S.L. Harper, "HP-IL: A Low-Cost Digital Interface for Portable Applications," Hewlett-Packard Journal, Vol. 34, no. 1, January 1983.
2. W.A. Buskirk, C.W. Gilson, and D.J. Shelley, "Compact Digital Cassette Drive for Low-Cost Mass Storage," Hewlett-Packard Journal, Vol. 34, no. 5, May 1983.

Character Editor and Display

The liquid-crystal display (LCD) and the file system interact through the editor. The LCD can be thought of as a 32-character-wide window on file lines of up to 96 characters. This window can be moved about by the →, ←, ↑, ↓ keys. The → key moves the cursor to the right until the right edge of the display is reached and then the whole window moves to the right. The ← key works similarly. Pressing the **SHIFT** → keys moves the window all the way to the right end of the line. The **SHIFT** ← keys move it all the way to the left end. The ↑ key moves the window all the way to the left and up towards the next lower-numbered line. (Think of the lines as listed on a sheet of paper, top to bottom, with the lowest numbered line at the top.) The ↓ key moves the window to the left and down one line, and the **SHIFT** ↑ and **SHIFT** ↓ keys move the window to the top and bottom of the file, respectively. In appointment mode, the appointments are stored in order of increasing time from the year 0000, top to bottom, so the →, ←, ↑, and ↓ keys move the display window through the appointments in the same manner.

There are several other editing keys: **CLR** to clear the LCD, **I/R** for inserting or replacing characters in a line, **BACK** for backspacing the cursor, **DEL** to delete a character, **SHIFT DEL** to delete from the cursor's position to the end of the line, and **FET**. The **FET** key is a typing aid for FETCH. It has many uses including fetching a line (FETCH linenumber), fetching a key definition (FETCH KEY), and fetching the next occurrence of a string in a text or BASIC file (FETCH "string").

All keys can be redefined to perform typing aids, executable strings, or system commands. These redefinitions are kept in a special text file called KEYS. This file can be manipulated like any other file in the system, including the EDIT and COPY operations. The redefinition can be done under program control as well. Thus programs can literally create their own keyboards.

The I/O control built into the HP-75 is all that is needed to control external printers, video interfaces and cassette drives. No extra software is needed. This part of the system interacts with the HP-IL hardware, the file system, and the character editor to give the user simple graphics, multiline displays, and mass storage backup of files.

Acknowledgments

A project as complex as the HP-75 is developed through the efforts of hundreds of individuals. Although not all can be acknowledged, the contribution of each person was essential and very much appreciated.

The pioneering efforts of the HP Laboratories team under the direction of Ted Laliotis spearheaded the initial development of the HP-75.

The management of the HP-75 project was organized as a tactical team chaired by the laboratory section manager. The team members, representing twenty-five separate areas of the division, are listed below. These individuals were responsible for the planning and coordination of efforts within their group and represented the many other people working behind the scenes on the HP-75.

The tactical team included Leonard Rosi, Ki Punches, Earl Ellis, John Van Santen, Bob Livengood, Rex Smith, Beth Brooks, Tom Arnold, Mark Warmann, Art Hart, John Smyth, Don Grant, Teri Wilson, Bruce Paris, Terry Yenchik, Larry Flory, Hans Lichtfuss, Bill Brown, Harry Griffin, Bob Wilson, Stan Hall, Jim Guynn, Jim Fremont, Nancy Lewis, Ravy Siuta, Robert Barkan, Mason Lakowske, Janet Placido, Jack Elward, Bill Wicks, Dave Conklin, Sherry Sisson, Roger Mullane, Pat Boyd, Steve Shepman, and Rob Horton.

The software design was done by Jack Applin IV, Seth Alford, Gary Cutler, Robert Heckendorn, Mary Jo Hornberger, Mark Rowe, and Raan Young.

The electrical design was done by Cindy Christensen, Al Benjaminson, Greg May, Tim Myers, David Lin, Ron Bilas, and Charles McCord.

The mechanical design was done by Cindy Bowline, Ken Hoecker, Tom Holden, Gary Lutnesky, Lee Mason, Ron Keil, and Roy Buck.

The IC design was done by Bill Thayer, Tom Arnold, Jim Schwartz, Dean Johnson, Bruce Schober, Mega Shyam, Loren Heisey, Liz Myers, and Les Moore.

The continued efforts and high standards of quality of all the people in the model and tool shops was much appreciated. Special thanks to Bernie Musch for continued support during some very tough times in the HP-75 development.

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High-Capability Electronics System for a Compact, Battery-Operated Computer

by Elizabeth Brooks, Robert J. Livengood, Rex C. Smith, and Timothy F. Myers

THE ELECTRONICS SYSTEM used in the HP-75 Portable Computer combines the processing capability of the HP-85 Personal Computer with the CMOS technology of the HP-41 Handheld Computer. Nine custom CMOS integrated circuits, a liquid-crystal display (LCD), commercially available CMOS static RAMs, an HP-IL (Hewlett-Packard Interface Loop[1]) interface, and a hand-pulled magnetic card reader form a complete computer system in a small, portable package.

A block diagram of the HP-75's electronics system is shown in Fig. 1. Using high-density plastic packages for the custom ICs, the HP-75 electronics can be mounted on three printed circuit boards. All of the custom ICs, excluding the display drivers, are located on the main logic board. The seven display drivers are located on a small board mounted with the LCD in the display assembly. The power supply circuitry and eight 2K×8 RAMs are on a third board sandwiched with the main logic board.

The HP-75 uses a CMOS version of the microprocessor developed for HP Series 80 Computers. This processor controls the 8-bit system bus that carries multiplexed data, instructions, and addresses to and from the other ICs in the system. The two-phase clocks on the bus are supplied by a clock generator on the CMOS 1LD2 chip. This IC was developed as the personality chip for the HP-75 and includes the clock generator, real-time clock, power supply controller, keyboard scanner, and programmable battery-detect circuitry.

The electronics system has three modes: deep sleep, light sleep, and awake. These modes are controlled by the 1LD2 integrated circuit.

In the awake mode the system clocks are operating at full speed (613 kHz). The system is in this mode whenever processing is being done, such as executing programs, storing or retrieving from memory, and executing HP-IL operations.

In the light sleep mode, the system is in an idle state (clocks operating at 4.68 kHz) awaiting the next key entry. The display is on in this mode. During keyboard entry, the system switches from the light sleep mode to the awake mode when a key is pressed. After the key is processed, the system reverts back to the light sleep mode.

The deep sleep mode is the off state for the HP-75 system. After the system has been in the light sleep mode for several minutes waiting for an entry, it goes to the deep sleep mode. Pressing the **SHIFT ATTN** keys also causes the system to go to the deep sleep mode. In this state, the power supply and display are off and battery power is applied directly to the 1LD2 IC, maintaining the real-time clock and allowing the **ATTN** key to be monitored. Battery power is also applied to the memory address, buffer, and RAM ICs in this mode.

Because of these three modes, maximum system speed can be attained while saving power.

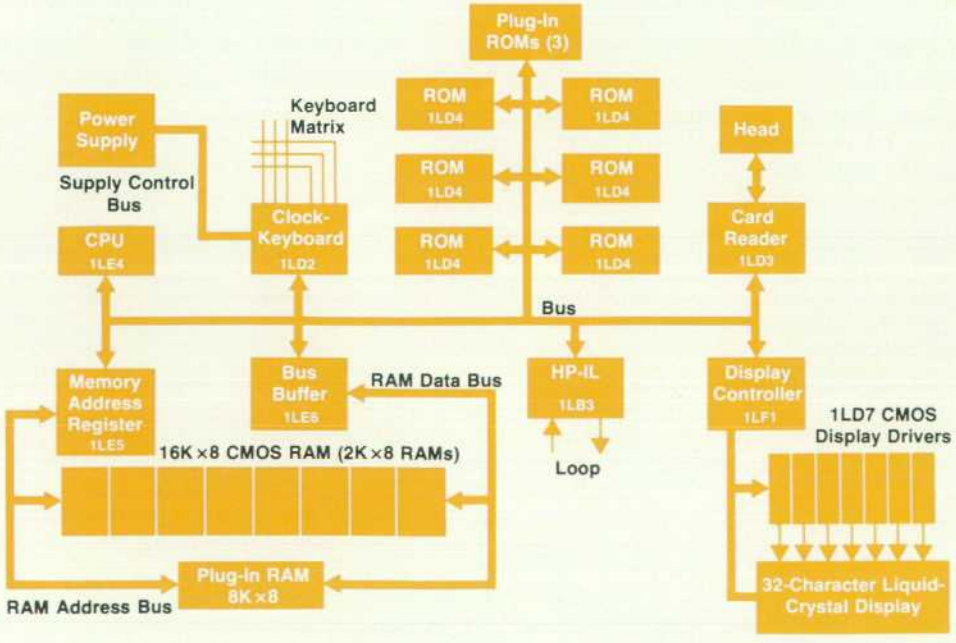

Fig. 1. *Block diagram of electronics system used in the HP-75 Portable Computer.*

Power Supply

The HP-75 power supply generates two primary output voltages. One provides power continuously to circuits such as the RAMs and the real-time clock. The other is a switchable supply line which shuts down when the system is in the deep sleep mode to eliminate unnecessary leakage current. The power supply's dc-to-dc converter is self-oscillating. It alternately stores energy in an inductor and dumps it into capacitors. The energy in the capacitors is used to supply power to the load while the switching circuit stores energy in the inductor. The converter is capable of providing 100 mA to a load at 5.5V with a minimum battery input voltage of 3.3V, and can provide up to 50 mA at 5.5V with an input voltage of only 2.5V.

Besides the dc-to-dc converter, the power supply printed circuit board includes a battery charger circuit, a generator of three temperature-compensated reference voltages for the LCD, an automatic reset circuit, a speaker driver circuit, and the external interfacing required for the HP-IL. There is also a battery-level detect circuit that sends a signal to a voltage comparator on the 1LD2 IC.

Timer

A 40-bit ripple counter serving as a real-time clock and a greater-than-or-equal-to comparator circuit are the only extra hardware required for the extensive time management features of the HP-75. The 32-kHz quartz crystal provides accuracy to within 3 minutes per month over worst-case operating temperatures. Accuracy can be improved to within 15 seconds per month by executing the proper software commands. This is made possible by a circuit on the 1LD2 IC that increments or decrements the real-time clock by 0.25 s on command from the processor.

Display

A 32-character liquid-crystal display is the primary output device of the HP-75. Each character position is represented by a 5×8 dot matrix where the eighth row of each matrix is reserved for underlining and descenders on lowercase letters. Also included on the LCD are four annunciators to indicate low battery voltage, a programming error, an appointment due, or that a program is running. The rows on the display are eight-way multiplexed so that only one row is displayed at a time.

Eight ICs drive and control the LCD. The display controller IC generates the voltage levels and timing waveforms necessary to multiplex the LCD, contains a character pattern ROM which translates ASCII character codes to the display's dot-on/dot-off code, and acts as the interface to the HP-75's processor. These features allow the display to operate independently of the processor except when the data in the display needs to be changed. To change the display, the processor writes two bytes of data to the display controller; the first byte indicates the position of the character on the display and the second byte is the character's ASCII code. Seven display driver ICs, each containing a 25-bit shift register, drive the column lines of the LCD. While one row is displayed, dot-on/dot-off data for the next row is shifted to the display drivers from the display controller.

Keyboard

The keyboard circuitry consists of an 8-column-by-10-row matrix. Keys are scanned by the column lines and the row lines are the receivers. There is a corresponding code for each row-column position in the matrix. This key code is read by the processor and is used as an entry address to service the key pressed.

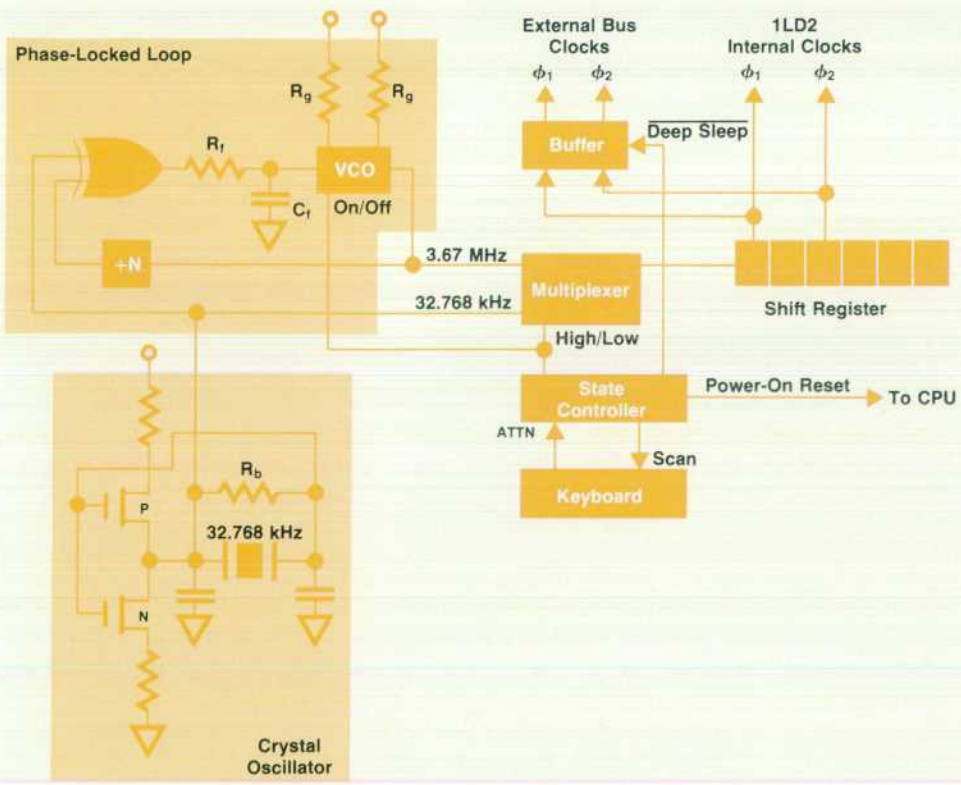

Fig. 2. *The clock system in the HP-75 Portable Computer uses a low-speed quartz crystal oscillator and a high-speed phase-locked loop to generate the system clocks.*

When the HP-75 system is in the awake or light sleep mode, the column lines are scanned continuously. In the deep sleep mode, the scanning is suspended and the column lines are held in a zero state. In this mode, any key closure on row 0 causes the HP-75 system to go to the awake mode and begin scanning the keyboard (the **ATTN** key is on row 0).

The keyboard has two-key rollover and features hardware key debouncing.

Card Reader

The magnetic card reader system (see article on page 15) consists of a custom IC, discrete components, and a magnetic head. Each magnetic card has two data tracks and two timing tracks, and stores a maximum of 1.3K bytes. Each track can only contain information from one file.

The need for a motor to pull the cards was eliminated by recording a timing track for each data track on a card. A variation in pull speed from 12.7 to 76.2 centimeters per

Packaging a Portable Computer

A major trend in personal computer design is to provide a more powerful machine in a smaller package. The HP-75 Portable Computer is a good example of this trend. Within its 10×5×1.25-inch dimensions are five major subassemblies: top case, display, logic printed circuit, power and memory printed circuit, and bottom case.

Top Case Assembly

The top case assembly consists of an aluminum overlay, an electroformed nameplate, a plastic top case, 65 keys, a rubber spacer, the keyboard printed circuit assembly, a stainless-steel ground plane, and a Mylar™ insulator. The aluminum overlay is bonded to the top case with pressure-sensitive adhesive. The overlay provides electrostatic discharge (ESD) protection as well as aesthetic appeal. The hinged keys are captured by ribbed details in the top case and a rubber spacer preloads the keys to prevent rattling. The keyboard printed circuit assembly is made up of a printed circuit board, 65 snap-disc switches, and two adhesive-backed Mylar sheets. The Mylar sheets serve three important purposes. First and foremost, they provide a barrier to dust and contamination. Second, they aid in protection against ESD, and third, they locate the switch discs with respect to the printed circuit board. The keyboard printed circuit assembly is heat-staked to the top case, retaining the keys and rubber spacer. Below the keyboard, pressure-sensitive adhesive holds the ground plane in place. The insulator below the ground plane prevents short circuits between components on the underlying logic board and the ground plane.

Display Assembly

The display assembly consists of the display printed circuit assembly, two elastomeric connectors, a liquid-crystal display (LCD), two silicone-rubber cushions, and an extruded aluminum retainer. The display printed circuit assembly has seven display driver ICs vapor-phase soldered to a 1×6-inch polyamide printed circuit board. The elastomeric connectors are compressed between the printed circuit assembly and the LCD to connect the driver ICs to the LCD. On top of the LCD are two silicone-rubber cushions enclosed in an aluminum retainer. An interference fit between the cushions and the retainer provides the proper compression for the elastomeric connectors and a good shock mount for the assembly. The display assembly fits into a recess in the top case.

Logic Assembly

The logic printed circuit assembly consists of 13 flatpack ICs, numerous discrete components, the logic printed circuit board, the card reader subassembly, and interconnects to the keyboard, display, and power and memory printed circuit assemblies. The ICs are vapor-phase soldered and the discrete components and connectors are wave soldered. The connectors are stamped beryllium-copper springs that extend perpendicularly from the logic printed circuit board. The connectors fit into corresponding holes in the interfacing printed circuit assemblies. The card reader subassembly is composed of a magnetic read/write head and a glass-reinforced plastic frame. The head is epoxied to the frame and the wires from the head are hand soldered to the logic printed circuit assembly. On the front edge of the logic printed circuit board are three extended ROM connectors which are accessible through ports in the front of the assembled product. The keyboard and display connectors position the printed circuit assembly with respect to the top case, and two screws secure it and the card reader frame to the top case.

Power and Memory Assembly

The power and memory printed circuit assembly consists of eight dual-inline-package ICs (RAM), discrete components, a speaker, and the I/O interface subassembly. Most of the components are wave soldered and the remainder are hand soldered. The I/O interface consists of the recharger connection, the HP-IL ports, an aluminum overlay, and a plastic backing plate. The interface is hand soldered to the power and memory printed circuit board and fits into grooves in the plastic case halves. On the power and memory printed circuit board is an extended RAM connection which is accessible through the battery compartment of the assembled product. The completed power and memory printed circuit assembly is aligned by the logic printed circuit assembly connectors and held to the top case by three screws. To minimize product thickness, the logic and power and memory printed circuit assemblies are mounted with their component sides away from each other. To prevent short circuits, a Mylar insulation sheet is placed between the boards.

Bottom Case Assembly

The bottom case assembly consists of the plastic bottom case, a steel magnetic shield, and an aluminum overlay. The magnetic shield fits within a recess in the bottom case and prevents the speaker in the HP-75 from accidentally erasing a magnetic card. The aluminum overlay is bonded to the bottom case with pressure-sensitive adhesive.

The three external aluminum overlays, the ground plane, the logic printed circuit assembly, and the power and memory printed circuit assembly have tabs which, once assembled, are connected to provide a common system ground. This connection is an interference fit and maintained by a screw through the bottom case. This common ground forms the primary ESD protection of the HP-75 (see box on page 14).

-Lee S. Mason
-Gary G. Lutnesky

second is allowed, providing a comfortable range for pulling a card by hand.

Limited security for card files is provided by using passwords and a private card option which allows a card file to be run, copied in, or purged, but not listed, edited, or duplicated. Each track can be protected from being overwritten. These protection options can be used separately or combined for various forms of security.

HP-IL

The HP-IL is supported directly from the HP-75 mainframe by the 1LB3 IC. This IC supports all of the hardware functions of the HP-IL, including timing, handshaking, transmitting and receiving on the loop, and partially decoding HP-IL frames. The HP-IL protocol is supported by firmware in the HP-75 operating system.

Clock System

The clock system in the HP-75 resides on the 1LD2 IC and supports the three system modes discussed earlier. This system (see Fig. 2) provides increased processing speed and power savings, accurate time-keeping capability, and an accurate system clock.

The system uses a low-speed quartz crystal oscillator that operates continuously in all three HP-75 system modes and a high-speed phase-locked loop. Both circuits are multiplexed into the two-phase clock generator input.

The crystal oscillator uses a single-stage CMOS amplifier with a 32.768-kHz quartz crystal. The only components external to the IC are the crystal and the bias resistor.

The phase-locked loop is a simple first-order loop. The only nonintegrated components are R_f, C_f, R_g, and R_b. These components are chosen judiciously to adjust capture, lock, and FM characteristics. The divide-by-N counter is mask-programmable on the 1LD2 IC's metal layer, enabling revision of clock speeds if necessary.

In the deep sleep mode, the crystal oscillator drives the two-phase clock generator. This generates the internal clocks that drive the real-time clock on the 1LD2 IC. Also in this mode, the two-phase clocks are inhibited from the system bus, the power supply is turned off, and the keyboard scanner is disabled.

In the light sleep mode, the crystal oscillator drives the clock generator. The clocks are enabled to output to the system bus, the power supply is on, the keyboard is scanned, and the HP-75 electronic system is operating at a 4.68-kHz clock rate.

In the awake mode, the phase-locked loop is enabled and selected to drive the clock generator. At this time, everything in the system is operating at a 613-kHz clock rate.

Typical operation of this circuitry is as follows. In its off state, the HP-75 is in the deep sleep mode. When the **ATTN** key is pressed, this activates the row 0 sensor in the keyboard circuitry and causes the state controller to enable the phase-locked loop, turn on the power supply, select the phase-locked loop to drive the clock generator, enable the clock generator to output to the system bus, enable the key scanner, and then allow the processor to execute its power-on sequence. The system is then in the awake mode.

When processing is completed in the awake mode, the processor instructs the state controller to go to the light sleep mode. The state controller in turn selects the crystal oscillator to drive the clock generator.

After several minutes of inactivity, the processor instructs the state controller to set up the deep sleep mode again. The state controller then disables the key scanner, turns off the power supply, and inhibits the clocks from outputting to the HP-75 bus.

Memory Organization

The HP-75's CPU has the capability of directly addressing 64K bytes of memory. This memory space is partitioned for various uses (see Fig. 3). The lower bytes (0000_{16} to 0011_{16}) are used for power-on and interrupt service routine vector addresses. The upper 256 bytes ($FFxx_{16}$) are reserved for use with I/O circuits.

The operating system for the HP-75 resides in 48K of ROM. This software determines the amount of RAM (4K to 24K) available for use. Since the I/O circuits are memory mapped into the physical address space of the CPU, the operating system is able to talk with each device directly. Data can be transferred in strings of one to eight bytes at a time, depending on the particular memory circuit's requirements.

One of the highlights of the HP-75 is its continuous memory. This feature allows the computer to maintain programs and data even when the machine is turned off. During the deep sleep mode, battery power is constantly applied to all RAM circuits. These ICs consist of eight 2K×8 RAM chips, a memory address register (MAR), and a data bus buffer (see Fig. 1).

The MAR decodes the address sent by the CPU and generates the chip-select signals needed to drive the RAM circuits. The MAR also determines whether the CPU is requesting a read or write and controls the direction of the buffer. The buffer isolates the load of the RAM bus from the CPU bus lines. If the RAM is not being accessed, the buffer latches the previous data. This technique conserves power by not charging and discharging large amounts of capacitance needlessly.

The ROM IC circuits in the HP-75 are organized in an 8K×8 structure. Each IC has its own circuitry to decode the multiplexed address sent by the CPU. The physical location of each ROM is programmed into the ROM's bit pattern.

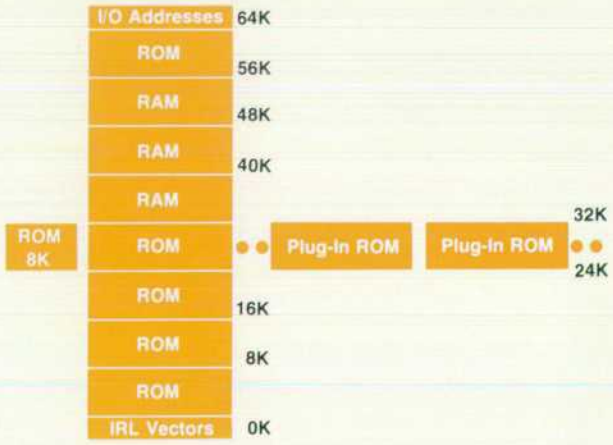

Fig. 3. *Memory organization in the HP-75 Portable Computer.*

One of the 8K ROM slots has the additional capability of being programmed to have its output bus drivers disabled. This action can be done on the ROM during bit pattern generation (for power-up enable and disabling) or by software via access of the I/O space.

The ability of the operating system to switch different ICs in and out of the same memory location gives the software the opportunity to address more commands, programs, and data than the CPU directly allows. With the addition of the plug-in module simulator software, the switchable bank need not be only ROM, but can be RAM as well. Although this RAM is not as completely accessible as the system RAM, programs can be loaded and then run. This allows saving the system RAM for data manipulation during program execution.

The HP-75 allows the user to interface easily with it. By the use of the I/O space, various methods of transferring information exist. Standard entry is by the keyboard. Normal output uses the 32-character LCD display. The operating system is also able to control the real-time clock, audio speaker, power supply, HP-IL interface, and handpulled card-reader circuits via the I/O addresses.

When the HP-75's CPU accesses the I/O space, the address is not incremented during consecutive reads or writes as done in the RAM and ROM circuits. Not all I/O addresses are used in the same manner. Some are used to set or read status and others are used to transfer data.

To allow the HP-75 to be customized for a particular application, the system bus is brought out to three ports in the front of the computer. The 8K, 16K, 24K, and 32K-byte plug-in modules are mapped into the switchable ROM bank. These ICs allow the system to have more functions

Electrostatic Discharge Protection for the HP-75

A major concern today in electronic product development is not only the sensitivity of individual CMOS devices, but also the increased sensitivity of the system to electrostatic discharge (ESD). Considerable time and effort is dedicated to developing functional and manufacturable protection to ensure that portable products can withstand greater-than-normal electrostatic discharges caused by human handling. The design effort in this regard for the HP-75 was first to develop adequate case protection and then to concentrate on the HP-IL.

Case Protection

Because the HP-75 is relatively quiet in terms of generating electromagnetic interference (EMI), it was not necessary to enclose the electronics completely in a metal box. However, careful design decisions had to be made to avoid ESD-related malfunctions, especially since portable devices have no earth ground connections. One thing was certain; a high-voltage transient to the electronics could be fatal to the HP-75 because of the large number of interconnected CMOS devices in the unit. Therefore, some type of protection is required to ensure that either the electronics is not exposed to ESD or that a discharge is directed to where it will do little or no harm.

The ESD protection for the HP-75 consists of three approximately parallel metal plates (the top overlay, the bottom overlay and the internal ground plane) that are tied to system ground at one common point near the I/O plate. The top overlay protects the key lines and display. The bottom overlay forms the other plate of a storage capacitor with respect to the reference ground plane. Therefore, the fields generated both during and after a transient charge exist outside of the electronics, avoiding the electrostatic field disturbances that would be present in a case if only the top overlay were used. The case seams are protected by the internal ground plane and the I/O plate overlay. With the ground planes extended to the external ROM ports, it is possible to protect the back side of the keyboard as well as the port connections from a direct discharge. This also provides an easy connection to any port-connected accessory that requires access to the HP-75's ground for ESD/EMI reasons.

HP-IL Protection

The objective is to maintain the integrity of each individual product's ESD protection when connected in the HP-IL. One weak device could take down the entire loop, especially if that device is the controller.

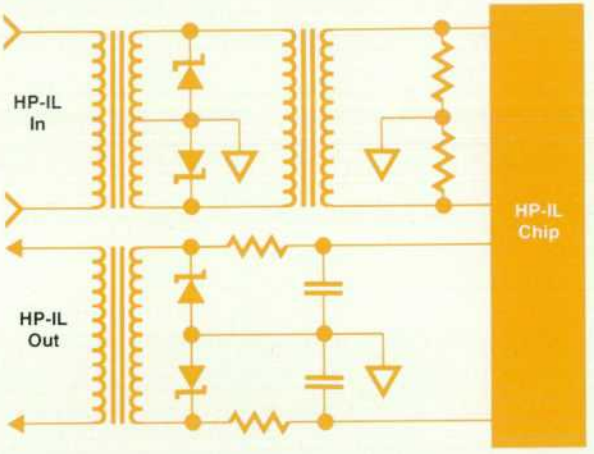

Fig. 1. *Simplified schematic of HP-IL interface showing components for ESD and EMI protection.*

Fig. 1 shows the basic HP-IL interface. While the transformers are used primarily for loop isolation and common-mode noise rejection, they also provide a significant ESD barrier. However, the small pulse transformers could not be designed to ensure that a breakdown would not occur across the transformers from device to device at high levels of ESD. Therefore, some sort of preconditioning of the transient signal had to be incorporated into the interface to prevent device damage. The Zener diodes greatly help in shaping the incoming transient and were chosen over transient suppressors because of their lower capacitance and cost. The remaining components represent normal line impedance matching and signal conditioning for EMI. For more details about HP-IL ESD/EMI protection, see reference 1.

Reference

1. C.J. Landsness, "The Electronics Interface for the Hewlett-Packard Interface Loop," Hewlett-Packard Journal, Vol. 34, no. 1, January 1983, pp. 14-16.

-Gregory J. May

and/or programs.

In addition to the system bus, the ports have control signals that allow external circuits to enhance the HP-75's capabilities by controlling interrupt routines, disabling memory circuits, or halting the CPU.

By using the I/O space in the CPU's address space, the memory of the HP-75 can be increased. The maximum amount of memory that the base computer will support is 200K bytes. This amount of memory, along with the ability to take control and modify the operating system, gives the HP-75 tremendous potential for use in many varying applications.

Acknowledgments

The people involved in the development of the HP-75 ICs were Megha Shyam, Liz Myers, Bruce Schober, Bill Thayer, Jim Schwartz, Dean Johnson, Tom Arnold, Bruce Schurmann, Loren Heisey, Charles McCord, and Peter Yu. The IC mask designers were Ed Guertin and Carolyn Bales. Those responsible for various aspects of the electronics system included Les Moore, Greg May, Al Benjaminson, David Lin, Eric Decker, and Cindy Christensen. Mechanical contributors were Ken Hoecker, Tom Holden, Gary Lutnesky, and Lee Mason. Project coordinators were Jerry Muravez and Teri Wilson. Many other people at Corvallis Division were directly or indirectly responsible for the development of the HP-75, but they are far too numerous to mention here.

A special thanks to the people at HP Laboratories for their support early in the project. Those included Ted Laliotis, Ken Peterson, Francé Rodé, Rich Wheeler, Rich Marconi, Clarence Studley, Hank Schade, and Dick Barth among others.

Reference

1. R.D. Quick and S.L. Harper, "HP-IL: A Low-Cost Digital Interface for Portable Applications," Hewlett-Packard Journal, Vol. 34, no. 1, January 1983.

Handpulled Magnetic Card, Mass Storage System for a Portable Computer

by Kenneth R. Hoecker, James R. Schwartz, Francis A. Young, and Dean R. Johnson

THE HP-75 PORTABLE COMPUTER features a built-in handpulled magnetic card reader/writer (Fig. 1) that can store 1.3K bytes of user data or programs per card. The cards are 10 inches long and 0.375 inch wide. Handpulled refers to the lack of a motor for transporting the cards past the head. Instead, this function is performed by the user. The user initiates a card operation with the appropriate command, inserts the card into the card reader, tells the HP-75 that the card is ready by pressing the **RTN** key, and then pulls the card through the card reader.

Card Format

There are four tracks on each card: two data tracks and two timing tracks (see Fig. 2). The timing tracks provide the speed information that allows cards to be pulled at an uneven rate without affecting the reading or writing of the card. The data tracks contain four fields of information.

Each field starts with a leader which has coding that cannot occur in the data to be written on the card. This leader provides the hardware with a signal that the start of a field has been encountered. In order, the fields are the card header (contains information on the format and size of the card), write protect (flag to indicate protected card), file header (contains information on filename, size, type, data, track number, number of tracks, etc.), and data (contains the user's data, up to 650 bytes).

Operation

The operation of the card reader is controlled by the user through BASIC commands. These commands allow copying of data to or from the HP-75 with options of privacy and/or password, cataloging the card to display its file

Fig. 1. *The HP-75 Portable Computer's internal mass storage system uses a handpulled magnetic card reader and recorder. This unit is located in the lower right corner of the HP-75. Each card can store up to 1300 bytes of data.*

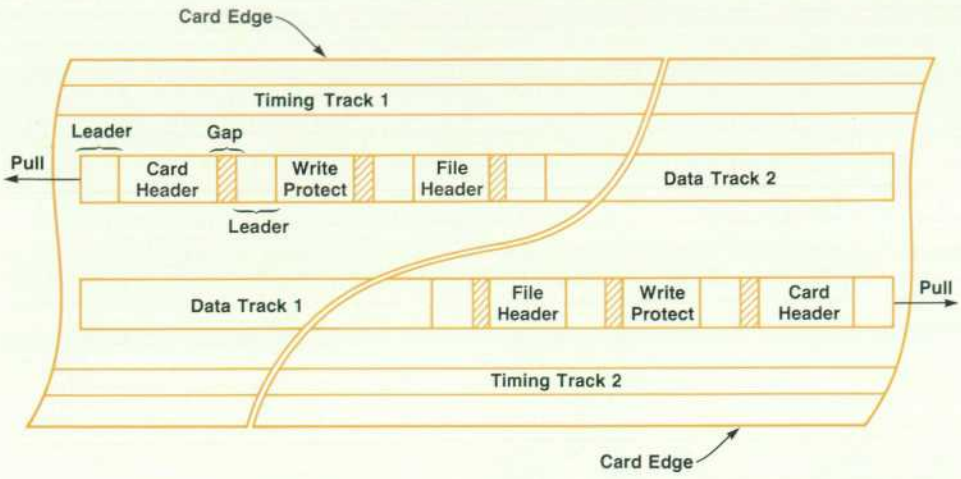

Fig. 2. *Magnetic card track and data field format.*

header, and protecting or unprotecting the card from overwriting. Privacy prevents any access to the file in the HP-75 except for running and purging. The password option prevents copying of the card if the password is not given. When a COPY TO CARD command is executed, the software automatically prompts the user to pull the card for verification after each track is written. The track is rewritten (by a third pull through the reader) if it does not verify. This ensures that a good copy is obtained at the end of the sequence.

If the card is pulled too slow or too fast, the hardware detects this and the user is asked to try again. Similarly, if the hardware detects an error other than speed, the user is informed and asked to try again. If the software does not receive anything from the hardware within seven seconds of the **RTN** key's being pressed after a pull prompt, it assumes that the card was not pulled or is damaged and asks the user to try again. If there is a delay of more than 0.25 second between data bytes from the hardware, the software also assumes a timeout.

The commands controlling the card reader are (in their general form):

```
COPY "filename" TO
  {CARD|"filename:{CARD|PCRD}[/password]"}
COPY {CARD|"filename:{CARD|PCRD} [/password]"} TO
  "filename"
CAT {CARD|":{CARD|PCRD}"}
PROTECT
UNPROTECT
```

where { }=choose one of the options separated by |, [ ]=optional parameter, lowercase = fill in value; UPPERCASE = use this keyword.

If the filename is specified in the COPY CARD command, the name on the card must match that name (if not, the user is asked to try again). Similarly, if the password is specified, it must match (a mismatch aborts the operation). If the name/password is specified on the COPY TO CARD command, that name/password will be used on the card. The PCRD option in either command causes the file on the target medium to be private (the user can only run or purge the file).

The card reader software attempts to be as friendly and forgiving as possible. Most errors will not abort the operation. Cards can be read in any order (or more than once), and the operation is kept simple. Verification of cards is done as part of the COPY TO CARD function, thereby assuring valid copies of the file. All card reader operations can be aborted at any time by pressing the **ATTN** key. If a COPY operation is aborted, the partial RAM file is purged. Identical copies of a file stored on cards can be mixed together without keeping the component cards together (the software checks each track to verify that it is part of the current file being read). Before writing on a card, the software checks the write protect flag and tells the user if the card is protected. If so, the write is not done.

Software/Hardware Interface

The interface between the software and hardware uses a two-byte I/O location. The first byte is data (from or to the hardware, depending on the read or write mode) and the second byte is the status. The status byte contains bits that allow the software to turn the hardware on or off, place it in the read or write mode, tell it to look for a field or reset itself, allow the hardware to report when it is ready with or for the next data byte, and report any errors such as speed and timing. The process of moving data between the hardware and software is simple: initialize hardware, wait for ready, loop (send byte, wait for ready) until done, stop hardware. This sequence is repeated once for each field on the card. One of the challenges of this project was designing the interface so that this process is symmetrical for read and write, thus enabling the same code to be used for both modes. While the software waits for the hardware to be ready, it counts down the contents of a timing register. The register is reset after every byte. If it counts down to 0, then a timeout is reported, and the operation is restarted.

Error Handling

Error handling was another interesting challenge. Since the software can be at any of a number of different places and/or many levels of subroutine nesting when an error occurs, it was necessary to devise a means of handling such errors and getting back to a known point without consuming vast amounts of code. Errors fall into two categories, those that cause the operation to restart (soft abort), and

those that abort the operation (hard abort). All top-level routines set a pointer to their restart address. When an error occurs, the top-level routine calls an abort routine, passing the error number and hard/soft flag. This routine restores the system stack pointer to the entry level, reports the error, and aborts or restarts the operation. Restart is done using the pointer set by the top-level routine. This method, while not structured, consumes only 50 bytes and removes the problem of backing out of the code after an error.

Extensions

The software allows for a potentially useful extension to the HP-75's functions. Volume purchasers can produce custom cards which can only be read with the aid of their custom ROM. This provides additional security because, without the ROM, the card will not be recognized.

Mechanical Design

The primary reasons for developing a handpulled card reader were that manufacturing cost and power demand are significantly lower than for motorized versions. It also requires less space in the product, and should have better long-term reliability because it has fewer moving parts (the only moving part is the card pulled through the slot).

One design objective was that the card reader must be easy and convenient to use. Some research was done to determine the range of speeds at which a person would naturally pull a card through a slot.* From the results, desirable and minimum acceptable speeds were determined. Each card must hold enough data to make it useful. Card life, card reader life, and reliability are also important considerations. All of the mechanical parts and the electronics had to be designed together as a system to achieve the objectives.

*This was done by using the HP-75 development system to record the time between each byte during the card pull, and then plotting the speed of the pull on a graphics terminal. The mechanism consisted of an assembly language program which ran on the HP-75 breadboard and used the HP-75's real-time clock to measure elapsed time between bytes. The data was recorded in RAM on the breadboard. After the pull, an ALGOL program on an HP-1000 Computer fetched the data from the breadboard RAM and plotted it on an HP 2648 Graphics Terminal, showing speed versus distance down the card.

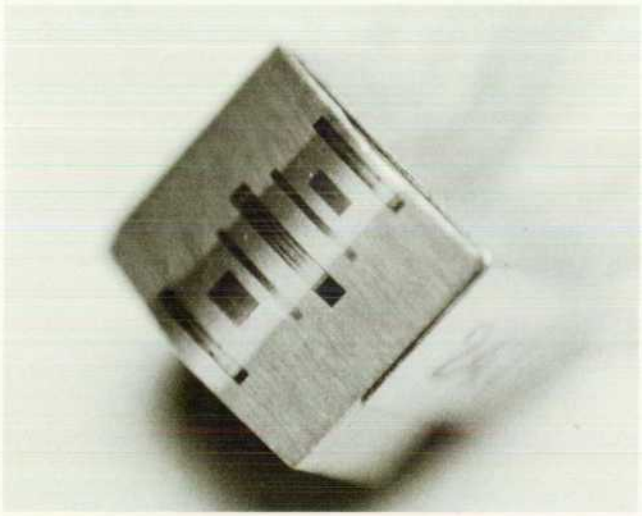

Fig. 3. *A common read-after-write head design locates the read and write gaps on opposite sides of the head's crown. The head used in the HP-75 has these gaps located on the crown as shown.*

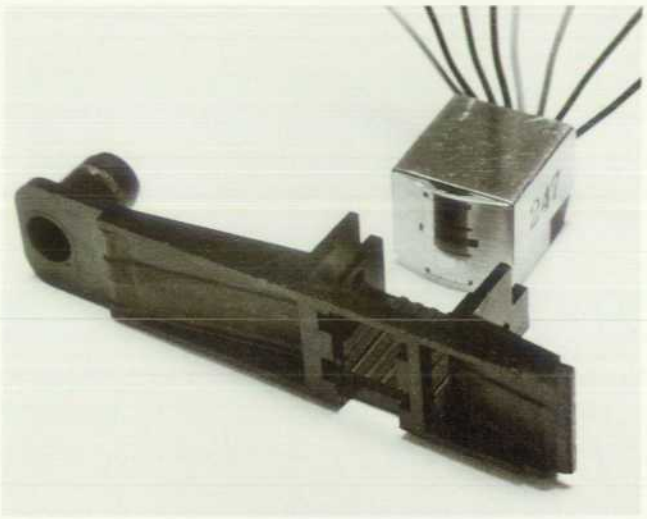

Fig. 4. *Base assembly for card reader.*

Magnetic Cards. The magnetic card material is critical to the overall performance of the card reader. The card performance requirements are somewhat different from those for previous HP card readers, so some different card materials and oxide coatings were tested, but none proved better overall than that used earlier in the card systems for the HP-67 Calculator, HP-97 Printing Caculator, and HP-41 Handheld Computer.

The cards are printed in sheet form and then punched into individual cards. All cards must then be passed through the production card recorder (see box on page 20), which records both timing tracks and data tracks on all cards. The blank cards have a specific bit pattern recorded on their data tracks and the application cards receive their appropriate programs and headers. All tracks are then read back to verify the quality of the cards and the recorder separates out the bad cards.

Magnetic Head. A special magnetic head (Fig. 3) had to be designed to satisfy the performance requirements of the card reader, taking into account the limitations of the card material. A prealigned design was chosen to reduce the cost and complexity of head alignment fixtures. Prealigned heads have their mounting surfaces machined and ground to tight tolerances with respect to their gaps at the factory. They are mounted to a frame made with comparably accurate surfaces by simply positioning the head against the appropriate frame surfaces and bonding it in place.

Without a motor to provide a constant card speed, some way of measuring card speed is necessary for recording a card. If the data is recorded using only a real-time reference, the data recorded will be compressed or stretched out, depending on whether the card is moving slower or faster than the nominal speed. Reading a timing track on the card was chosen as the easiest way to measure card speed.

With this system, the timing track must be read while writing a card. Since the write signal is much stronger than the read signal, crossfeed between the gaps was a problem. This was solved by separating the two gaps on the head as

much as possible and inserting extensive shielding between the gaps. Maximum separation of the gaps without widening the card was achieved by interlacing the tracks on the card as shown in Fig. 2. Also, the timing (read-only) gap on the head is made narrower than the data (read-write) gap because of their somewhat different performance requirements.

Card Reader Base. The card reader base (Fig. 4) is injection molded as one precision part to reduce assembly tolerances and cost. It is molded from 40% glass-filled PPS (polyphenylene sulfide) because of its low mold shrinkage and excellent dimensional stability. It was designed and the mold was built to very tight tolerances to achieve the required head-mounting and card-guidance accuracy.

The card track width is critical for controlling tracking error and card skew. Side springs are not used to position the card in the track. Instead, a minimal clearance is maintained between the track walls and the sides of the card. Clearance grooves are located in the bottom of the track coincident with the recorded portions of the card to prevent unnecessary wear of the oxide coating on the active portions of the card.

Another critical aspect of the card reader base is the card wrap detail. This feature must have low enough drag to allow the card to be easily pushed into the slot and not excessively wear the head, card, or plastic, and yet provide consistent intimate contact between the head and the card. The contact force is provided by small bumps on crossbars located before and after the head gaps and oriented perpendicular to the direction of card travel. These bars force the card to deflect slightly as it passes over the head. The member supporting the crossbars is used to control the amount the card is deflected. The area between the crossbars is exposed for easy head alignment inspection.

The head is located close to the slot exit to reduce the unusable card length required for gripping the card to pull it through the slot. The minimum distance is limited by the need for enough separation between the head and the slot to reduce the possibility of electrostatic discharges going into the head through the slot and damaging the sensitive electronics.

The head mounting pocket is the most critical aspect of the part. It has surfaces to control the six degrees of freedom of the head position with respect to the card track. All of these surfaces must be accurately maintained on the finished part if the card reader is to perform reliably and be able to read cards recorded on other HP-75 card readers.

Assembly. Card reader assembly is simple. The head is pushed to the upper left corner of the card reader base and bonded in place. A fast curing, but relatively weak adhesive is used to bond the sides of the head for a short fixturing time. The assembly is then inspected and functionally tested. If a problem is found with the mounting, the head can be removed without damaging it. If the assembly is good, the bottom surface of the head is then bonded with a high-strength epoxy.

After the epoxy cures, the card reader is assembled into the HP-75. The head wires are attached, and one end of the assembly is inserted into a notch. The other end drops over a boss and is secured by a screw.

Testing. Extensive testing was done throughout the development of the card reader to improve its performance and ensure its reliability. A machine that looped a card through the HP-75 every two seconds was built to life test the card readers. They were tested to 225,000 card passes (equal to over 100 cards per day for five years), after which they were still performing satisfactorily. Many tests were done recording cards on one card reader and then reading them on a different one to make sure the cards are interchangeable.

Bit densities as high as 3200 bits per inch (bpi) were tried during development of the card reader, but the cards were much more sensitive to dirt and damage at the higher densities. The final choice was to use 800 bpi, allowing 650 bytes of user data per track (1300 bytes per card) in addition to the header information.

Digital Design

The digital hardware is oriented around a PLA (programmed logic array) chip controller that functions according to an algorithm using qualifiers and commands. Changes to the algorithm entail only alteration in the orderly array structure of the PLA and so have minimum impact on the surrounding support circuitry. The state

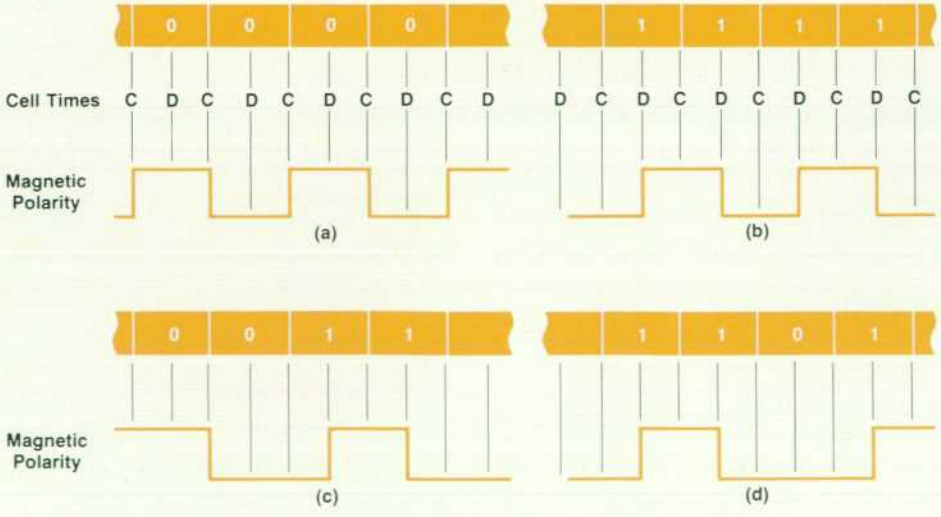

Fig. 5. *MFM code magnetic polarity distribution for (a) a string of zeros, (b) a string of ones, (c) a transition between zeros and ones, and (d) a single zero in a string of ones.*

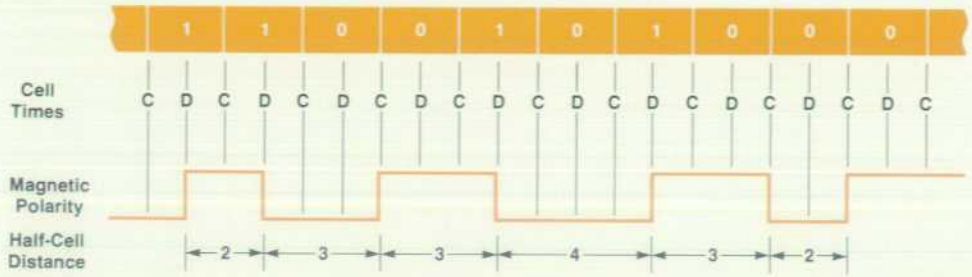

Fig. 6. *Example of a mixed data pattern in MFM code. Note the varying half-cell distances of two to four half-cell lengths.*

machine nature of the controller was a convenience during the breadboard stage because algorithm changes could be readily made using EPROMs.

The HP-75 CPU manipulates the card reader chip through the status byte passed back and forth. The CPU activates the chip, specifies read or write, start, and stop, and clears the ready flag.

The card reader chip encodes and decodes data for write and read operations, writes its own leader at the beginning of each field, decodes the leader on reads, and sets error bits for errors encountered in decoding and speed limit checks. The card reader chip also ensures that the proper physical gap is left between fields during write operations.

MFM Code. The MFM (modified frequency modulation) code was chosen for its overall rating for code efficiency, bandwidth, and circuit complexity (see Fig. 5).

Code efficiency. Measured as 100 divided by the number of flux reversals per bit. This figure is a minimum of 100 for MFM code for strings of ones or zeros. For typical mixed data streams, this figure is greater than 100. Some specific data sequences have an efficiency figure of 200.

Bandwidth. Keeping the bandwidth narrow reduces the spectrum of noise that can enter the system—the narrower the better. Also associated with the handpulled tape transport system is the presence of frequency variations that might be considered as flutter and rumble. Keeping the low end of the passband above these frequency disturbances is important. MFM provides this feature. Even with strings of continuous ones or zeros, flux reversals are present during the string.

Circuit complexity. Complex circuits are to be avoided, but performance tradeoffs start to improve with increased complexity of some codes. MFM decoding is not as simple as many codes, but the state machine PLA controller approach to the chip handles decoding nicely.

An area on the working surface of the medium devoted to defining a one or zero bit is called a cell. During motion of the medium, the point in time when a cell boundary passes through a planar extension of the magnetic head gap is defined as C time. The point in time when the cell center comes in alignment with the gap is called D time.

When writing a string of zeros (Fig. 5a) in MFM code, magnetic flux polarity reverses at C time. When writing a string of ones (Fig. 5b), flux reverses at D time. The rules change a little when ones and zeros are adjacent. Polarity still reverses at D time for ones, but the reversal at C time is omitted where a neighbor cell is a one (see Fig. 5c and 5d).

Fig. 6 shows a mixed data pattern. Note that we can break the cell time into halves and now speak of half-cells between flux reversals. This is a more convenient unit to use when discussing decoding and encoding processes for MFM.

Each magnetic card has two data tracks. Each data track has a factory-recorded timing track. Fig. 2 illustrates the magnetic card data track and timing track layout. Only one data track is written or read for each pull. Two pulls are required to access both tracks.

The write process uses the timing track for data registration and as a speedometer. The timing track consists of equally spaced flux reversals over the entire track length. The cell lengths are the same for the timing and data tracks.

Cells are registered during write by using the timing track flux reversal as C time. The digital circuitry generates D time for a cell by measuring the time lapse over the two previous timing track cells and adding a half-cell time beyond the last C time. The write circuitry now has C and D times defined in synchronism with the timing track (see Fig. 7).

Reading MFM code is a process of following the rules to define a zero or one. Based on what the last detected bit was and how many half-cells have passed, the decoder can define the present bit. On the HP-75 card reader chip, a circuit called a cell counter provides time windows (2W, 3W, and 4W) to tell the chip controller how many half-cells (2HC, 3HC, and 4HC) have passed. The PLA controller uses the half-cell count and knowledge of the previous bit to make the decision whether the present flux reversal represents a one or zero.

(continued on page 21)

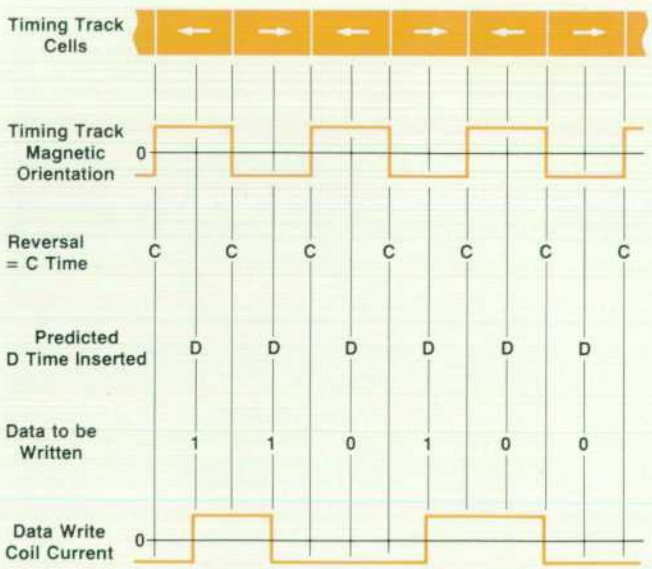

Fig. 7. *Write operation timing for HP-75 card recorder.*

The HP-75 Production Card Recorder

by David B. Patton

HP's manufacturing engineering group at Corvallis, Oregon developed a card recorder (Fig. 1) to meet the production needs for the HP-75's magnetic cards. Since even blank cards must have timing tracks and data tracks, every card sold must first go through this recorder. It can accept cards in any of four possible orientations and is capable of recording about 2500 cards per hour.

The operator interface to the recorder is an HP-85 Computer. After entering the program name, the card number, the number of cards, and the bin size for good cards, the operator inserts the raw cards into the input hopper and presses the ready softkey.

After each card is picked by the recorder, it is propelled through various card guides by 62 nylon-chain-driven rollers. The card guides are cast parts used to direct the cards through four read/write modules where they are recorded and verified. Each module records one of the four tracks. If the verification fails, the card is routed to the next bad bin. Cards are diverted into bad bins by a short burst of air which deflects the card into the set of card guides leading to the bad bin.

Synchronous ac motors with external rotors were chosen to run the drive rollers because a very stable, constant speed is required so that there is no buckling of cards as they pass from one roller to the next.

Cards that pass all four verification steps go into one of the two good bins. When this good bin is full, it is ejected and subsequent cards are directed to the other good bin. The operator removes the cards from the filled good bins and keeps the input hopper full of raw cards.

The HP-85 with a GPIO module and external disc drive controls the card recorder's distributed processing system containing ten 6802 microprocessor boards. The ten microprocessors control an input module, two timing track modules, two data track modules, and the pick and track modules. The HP-85 transfers data and sends commands to the modules over a bus connected to all of them.

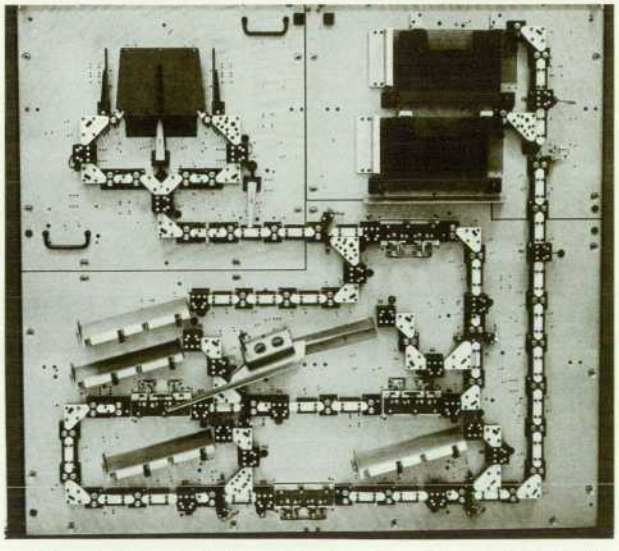

Fig. 1. *To record the timing tracks and programs on the magnetic cards for the HP-75 Portable Computer, this production system was designed and built. It accepts blank cards in any possible orientation, rejects bad cards, and can record 2500 cards per hour.*

Modules

The input, timing track (TT), and data track (DT) modules each contain an interface board that converts data bytes into bit streams and vice versa. The input module connects directly to an HP-75 card reader chip. The TT and DT modules connect to the read/write modules that the cards pass through. The DT modules each contain 6K bytes of RAM for the write data and 24K bytes of RAM for the verify data. Since the cards can travel through the recorder in either direction, both DT modules must be able to record either data track.

The read/write modules contain the magnetic heads, capstans, a read/write board, and two capstan motors (again ac synchronous). The magnetic heads are chrome-plated versions of the HP-75's head with a timing track write coil added to them (in the HP-75, the timing track is read only and its head therefore has no ability to write timing tracks). The read/write board contains the write head drivers and the analog circuitry for digitizing the read head signals.

Pick and Track Modules

The pick module controls the pick portion of the recorder (see Fig. 2). An HP 3050 Optical Wand detects which side of the card in the bottom of the hopper is down. It then picks the card to the left or right so that the card ends up with its painted side up at the next wand. The pick sequence is as follows: turn on the pick arm vacuum, raise the pick arm up to the card, pull the end of the card down by lowering the pick arm, lower a pinch roller onto another roller below the end of the card, and finally release the pinch roller and vacuum when the card is in the card guides.

The next wand reads and checks the tick marks on the card (the binary representation for the last seven digits of the card's part number and the revision letter) to ensure that the card and the data match. It also checks the direction that the card is traveling. If the tick code is wrong, the card is immediately ejected.

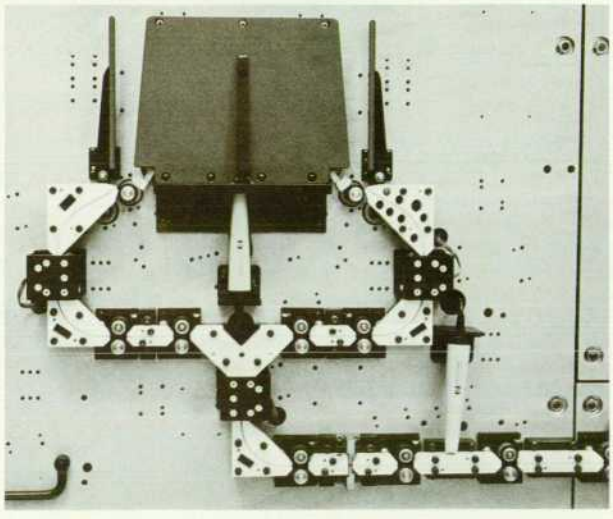

Fig. 2. *Card pick module for the production card recorder.*

The card is tracked through the recorder by the track module. This module is connected to the other modules, to 22 optical card sensors, and to valves, relays, and drive chain breakage sensors. As each card travels through the recorder, the track module tells the DT modules the card's direction, checks the TT and DT verification results, ejects bad cards, detects card jams, checks for broken drive chains, keeps count of the number of cards in the good bins, and controls the good bins.

Cards are tracked by giving each active card a status and position byte. A card becomes active when it is sensed at the first optical sensor. Active cards are updated every inch of travel. The status byte contains the following information: card direction, which good bin is active, and whether the card is good or bad. There are tasks associated with different positions of the card in the recorder. For example, when the card reaches position 108, data track 2 verification is checked and the status byte is updated. When the card is at position 109, the proper air jet is turned on to eject the card if it is bad. Other tasks include checking for a new card, turning off ejector air, setting a card's status to inactive, telling the pick module to stop picking, incrementing either good bin's number of cards, and ejecting good bin 1 or 2.

During the recording process, the track module informs the HP-85 controller of the occurrence of several conditions: the number of cards desired have been recorded, a drive chain has broken, there is a jam, or there is a checksum error in a TT or DT module. The jams are detected by using the position byte for each card. When a card is at position 45, the fourth optical card detector should sense the card. If it is not present after two checks in a row, then the card is considered to be jammed and the entire system is shut down by the track module and it tells the HP-85 where the jam was detected. This optical sensor checking is done for every inch of card travel.

The pick and track module software contains commands for exercising all of the valves and solenoids in the recorder, for reading the status of all of the sensors and switches, and for checking some of the intermodule wiring. An HP-85 program is used to access all of these commands for debug and maintenance of the recorder.

Acknowledgments

Contributors to the card recorder were Ralph Sebers, mechanical design, Ken Frazier, write/read module design, and Bob Conder, interface board design.

When writing the very first bit in a field, flux reverses at C time for a zero and at D time for a one. Likewise, when reading the very first bit in a field, the decoder follows this convention and decodes accordingly.

Functional Blocks. The card reader digital circuitry (Fig. 8) is composed of several major functional blocks:

- Cell counter. The cell counter is responsible for detecting the number of half-cell time periods that have occurred since the last flux reversal and providing time windows to the PLA controller. It also generates the signals 0MARK (C time) and 2MARK (D time) used for data registration during a write operation.

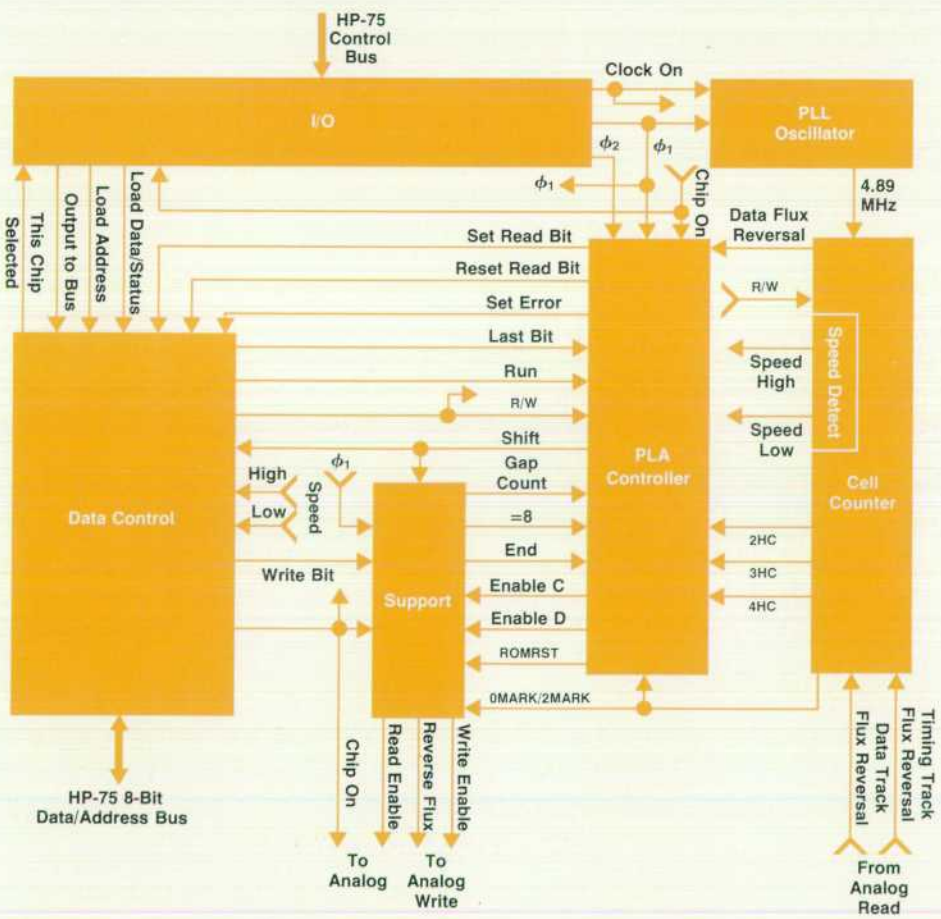

Fig. 8. *HP-75 card reader digital block diagram.*

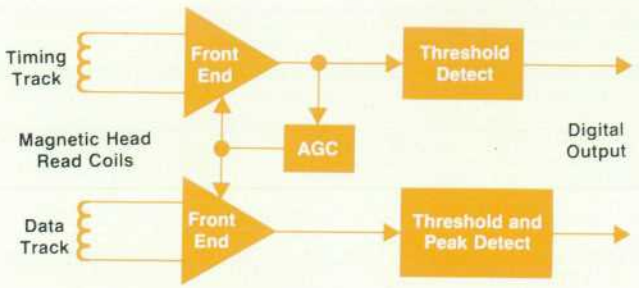

Fig. 9. *Block diagram of analog portion of the card reader electronics.*

- PLA controller. This controller guides the chip through the proper sequence of events for read and write with the aid of supporting circuitry that provides the necessary bus and analog interfacing and critical timing. The controller, guided by the MFM decoding rules, also performs the one or zero decisions and error detection during the read process.
- I/O. The card reader communicates with the HP-75's CPU via the I/O section. Data and status are passed back and forth on the HP-75's data/address bus in two-byte writes and reads.
- Phase-locked oscillator. The phase-locked loop circuit designed for the 1LD2 chip used in the HP-75 (see article on page 10) is also used on the card reader chip. One of the HP-75 system clocks is multiplied by eight by this circuit to provide the 4.89-MHz clock for the cell counter.
- Data control. This section contains the bus pad drivers, address decoder, data and status registers, and data shift register. The address decoder monitors the HP-75's data/address bus. Upon successful decoding of an address, the I/O section is allowed to generate the proper load or output signals to receive data via the bus from the CPU or to put data onto the bus for the CPU.
- Support circuitry. The support circuits handle the incidental tasks associated with reading and writing data. Some of these tasks are detection of proper gap length between data fields during write, providing the proper sequence of flux reversals for the leader at the beginning of each field written, and counting the number of bits read in or written out to initiate transfer of data bytes to and from the I/O section.

Analog to Digital Interface

In the design of the analog system for the HP-75 card reader, a number of problems had to be considered. The wide range of speeds encountered in the use of the unit requires gain control circuitry and circuitry that can accommodate a wide bandwidth. The increased density requirement forced the use of a peak-detect scheme with a wide usable frequency range. The unknowns associated with the CMOS operational amplifiers dictated a forgiving design which accommodates large offset voltages and extreme 1/f noise. To simplify manufacture, trimmer potentiometers were not allowed. Environmental noise from the digital circuitry and the magnetic head had to be minimized.

Dynamic Range. The analog circuitry must operate properly under a wide range of input amplitudes. The standard magnetic read head has an output amplitude proportional to card speed. Thus, a 6-to-1 variation in input amplitude is possible. Also, under the poor conditions the card is expected to survive, the circuitry has to read signals properly even with a 50% loss of amplitude from dropouts caused by contamination of the card surface.

Part of the solution to the dynamic range problem is seen in Fig. 9. An automatic gain control (AGC) circuit monitors the output of the timing track amplifier and feeds back a dc control voltage to set the gain of both input amplifiers. The timing track is continuous over the length of the card, but the data track is divided into records with gaps between. Because of the gaps in the data track, it cannot be easily used to provide suitable input to the AGC circuit. Thus, the magnetic head is specified to provide equal amplitudes from both read coils to allow this scheme to work.

The relatively long time constants associated with the AGC circuit were picked after much testing of the pulling styles of different people.

Frequency Response. The frequency response of the input circuitry was of concern for a number of reasons. A wide speed range requires a corresponding wide frequency range. The final product has a 5-to-30-inches-per-second speed range, or a 6-to-1 frequency range. Another important reason for using the MFM code scheme discussed earlier is the narrow frequency variation—a 2-to-1 variation. Thus a fundamental frequency range variation of 12 to 1 along with third-harmonic components must be replicated faithfully with minimal relative phase shift.

The 1/f noise normally associated with CMOS amplifiers required attenuation. The lack of total shielding of the head allows it to pick up ambient noise easily, so low-frequency limiting is necessary to ensure minimal noise susceptibility—particularly to 60-Hz noise.

In Fig. 10, we see the solution to the low-frequency problems. Amplifier A3 acts as an active filter to feed back the low-frequency components of the signal to amplifier A2, providing high-pass filtering. R1 and C1 are selected to minimize low-frequency noise while still reproducing the input signal with a minimum of phase distortion. This technique has the added advantage of nulling the accumulated offsets of amplifiers A1 and A2, leaving the output signal centered at V_{mid} with only the single offset of amplifier A3.

Detector Circuits. The density requirements of the system require a peak detect circuit for the data tracks as opposed to

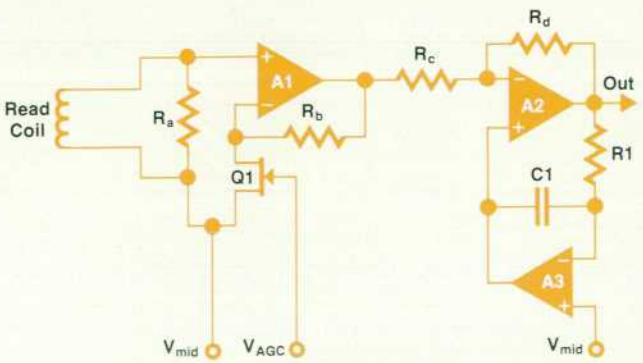

Fig. 10. *Analog front-end amplifier circuit.*

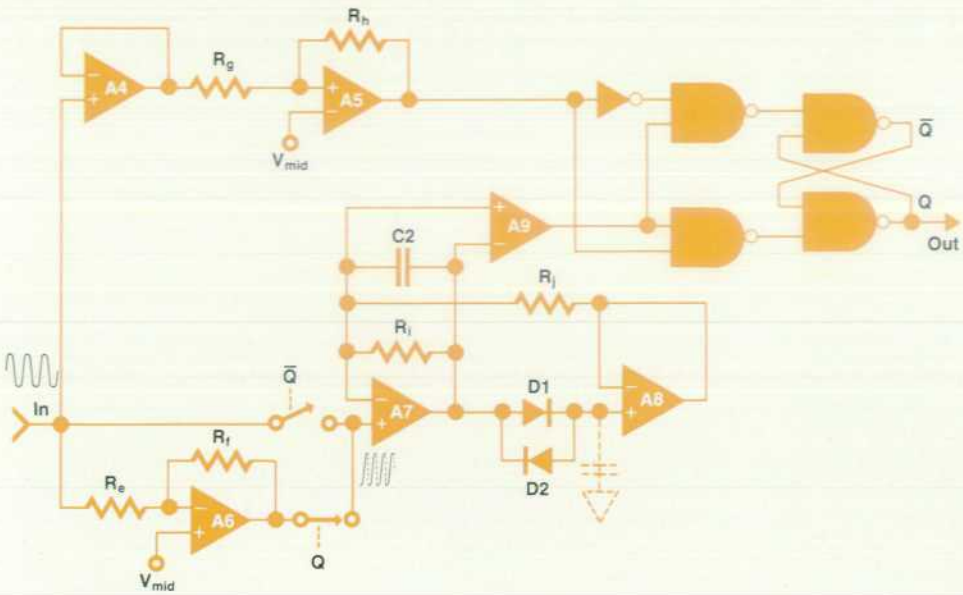

Fig. 11. *Detector circuits. Timing track detection uses only the threshold-detect circuit formed by A4 and A5. Data track detection uses both threshold-detect and peak-detect (A6, A7, A8, and A9) circuits.*

the threshold detect scheme used in HP's earlier card readers. The standard differentiate/zero-crossing scheme normally used for peak detection was unusable because of the wide frequency range required to handle the wide range of card pull speeds, and the limited dynamic range of the CMOS analog circuits.

The detection circuits are shown in Fig. 11. Amplifier A4 buffers the input to Schmitt trigger A5 to form the threshold detect path used for detecting the timing track.

The peak detect circuit consists of amplifiers A7 and A8 and comparator A9. The input to the peak detector comes either straight from the front-end circuitry or through A6, which is configured as a unity-gain inverter with $R_e=R_f$. The output switching logic, coupled with the input transmission switches, provides a positive-going signal to the peak detect circuit. The peak detector detects only positive peaks. This ensures that there is minimal phase shift between positive and negative peaks caused by offsets in the peak detector. The output logic is enabled by a threshold signal from A5 and then switches on the next peak signal from A9.

During the increase of the input signal, A7 is in a unity-gain configuration with its output a forward diode voltage drop above its negative input. This keeps the output of comparator A9 low. Diode D1 in Fig. 11 conducts and charges up the parasitic capacitance at the positive input to A8. When the input signal reaches a peak and starts coming down, D1 is cut off, A8 is held at the peak value, and A7 is now configured with a gain determined by the ratio of R_i and R_j. This ratio provides a noise margin. The output of A7 now follows its input with a high gain, quickly overcomes the diode drop difference at the input to comparator A9, which then switches, indicating a peak was detected. The parasitic capacitance at the positive input to A8 then discharges through diode D2 and the circuit is ready to detect the next peak.

Acknowledgments

Many people made significant contributions to the digital portion of the HP-75 card reader chip. Les Moore helped with breadboard development and debug and performed computer-aided logic testing on some of the more complex circuitry. Bill Thayer did the entire conversion from digital breadboard to CMOS silicon, both circuit design and layout. Bruce Schober was responsible for the chip PLA design. Tom Arnold, in addition to his analog efforts, invested considerable time in designing and building of test equipment to ensure quick evaluation of our first chips. Leonard Rosi was the driver behind quality assurance testing of the entire card reader system. Rex Smith contributed his CMOS phase-locked loop design to the card reader chip.

Tom Hender contributed to the mechanical design and Horst Irmscher was responsible for getting the plastic parts molded.

Thanks to Don L. Morris and Don E. Morris for creating the supportive atmosphere in which to do our work.

Integration of the HP-75's Handpulled Card Reader Electronics in CMOS

by Thomas J. Arnold and Billy E. Thayer

ONE OF THE ORIGINAL GOALS in the development of the HP-75 Portable Computer was to provide inexpensive mass storage capability. As described in the article on page 15, the decision was made to implement a handpulled magnetic card reader. Since the product was to be portable and operate on battery power, low-power CMOS technology was chosen to implement the HP-75's internal functions. This posed a real challenge to the HP-75 design team, because to implement the handpulled card reader circuit, some form of analog circuitry had to be designed using a standard digital CMOS process. Another constraint was that, to reduce cost, this analog circuitry had to be combined with digital circuitry on the same CMOS integrated circuit.

The approach taken in the development of the handpulled card reader IC was to design and lay out the digital circuit and analog circuit portions independently and then merge them into a single IC layout. This was possible since there are only five signals that must pass between the digital and analog functions. These signals consist of the timing and data track outputs of the analog portion and some control signals generated in the digital portion to turn off the analog circuits when the card reader is not in use.

Digital Circuit Design

The digital circuitry was simulated first with a breadboard design implemented with standard off-the-shelf TTL components. It was then necessary to convert this breadboard logic to CMOS circuitry for the IC. There were two main problems to overcome in the design of the digital circuitry, power consumption and circuit speed. The speed problem was the need for an internal 4.89-MHz clock to drive some high-speed counters used to decode data from the card. The power problem was the need to conserve power when the card reader is not in use.

Power consumption is held to a minimum by having a status bit that turns off the analog circuitry and all of the digital circuitry used in the reading and writing of the cards. The system software can read and write this status bit and thereby control power consumption. The only part of the chip that is always enabled is the input/output circuitry that monitors the status bits and accepts data and control information from the HP-75 system CPU.

When a card is read or written, the status information from the system CPU enables both the analog and the digital circuits. In the digital section, a VCO (voltage-controlled oscillator) is turned on and a phase-locked loop regulates the VCO to oscillate at a frequency of 4.89 MHz, eight times that of the system clock.

The high-frequency part of the chip is the half-cell counter section that uses the 4.89-MHz signal fed into two counters. One of these counters is a twelve-bit counter that determines card pull speed and divides the card's timing track period by eight for use in determining the relative time between flux reversals on the data track. The other counter is a nine-bit synchronous counter that starts at a timing track flux reversal and stops when the card's data track has a flux reversal. Special master-slave flip-flops had to be designed to operate at this speed. The IC layout of these flip-flops was done with great care to keep the connecting node capacitance to a minimum. They also must have a very low output impedance.

In the breadboard circuit, the logic control was done with a programmable ROM. This was converted to a programmable logic array (PLA) controlled by six state flip-flops and twelve other qualifier signals. There are sixteen output

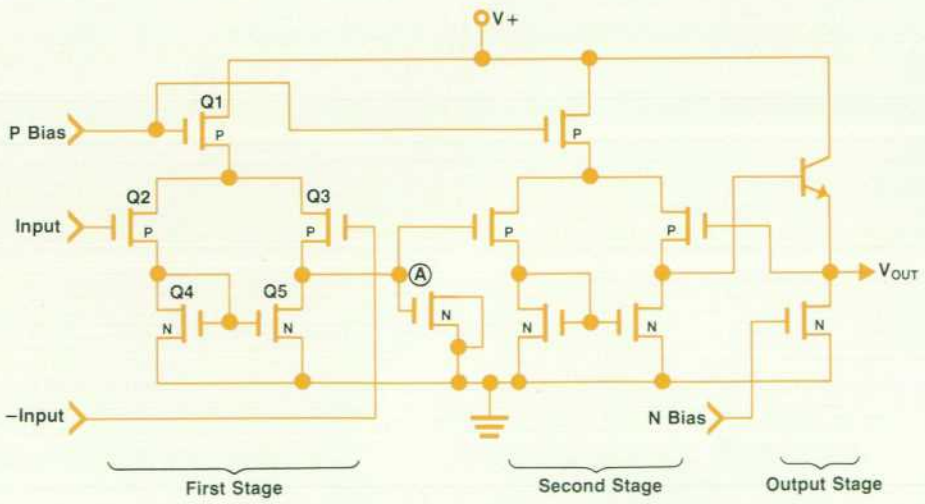

Fig. 1. *CMOS operational amplifier circuit.*

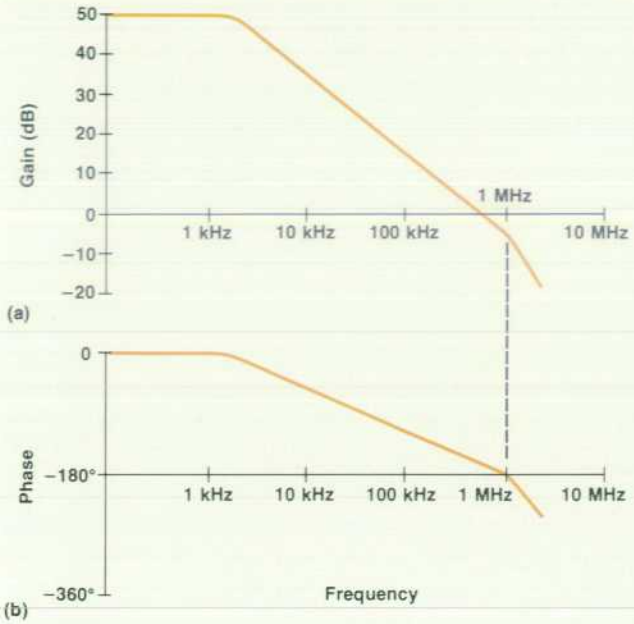

Fig. 2. *Gain (a) and phase (b) versus frequency for CMOS operational amplifier.*

signals; six of these are used to control the state flip-flops and the other ten are used to control the flow of data to and from the card and the HP-75 system memory.

Analog Circuit Design

The approach taken in the design of the analog portion of the card reader IC was very similar to the approach one would take when designing with off-the-shelf components. Because of development time constraints, the decision was made to try to copy the analog breadboard design as closely as possible. We therefore needed to design the operational amplifier circuit and use it as one would use an off-the-shelf operational amplifier. We could also use standard resistive feedback techniques by integrating resistors on the IC. One drawback to this design approach is that some external components must be used because very large resistors and capacitors cannot be integrated on the IC without taking up very large areas.

The operational amplifier has three stages (see Fig. 1). The first stage consists of a basic CMOS differential pair and provides the gain for the operational amplifier. The bias current is set by turning the p-channel transistor Q1 on with a gate voltage that is about 0.5 volts above threshold. This transistor acts as a current source since it is being operated in the saturation region with $V_{ds}>V_{gs}$. The inputs to the operational amplifier consist of two large p-channel transistors, Q2 and Q3. N-channel transistors Q4 and Q5 act as loads. Any small difference in voltage between the gates of the two input transistors causes a large voltage change at point A since there is a constant current that must be shared between both halves of the differential pair.

The second stage of the amplifier consists of another CMOS differential pair which buffers the output of the first stage. The output of the first stage requires buffering to keep the base current requirements of the bipolar transistor in the output stage from unbalancing the first-stage differential pair. The output of the operational amplifier is fed back into the negative input of the second-stage differential pair, forcing the pair to operate in a unity-gain configuration. The output stage consists of an npn bipolar transistor in an emitter-follower configuration. The collector current is limited by an n-channel transistor operated as a current source. The bipolar transistor is fabricated by making use of the substrate, p-well, and n-diffusion steps in the CMOS process.

One of the concerns in the design of the operational amplifier was 1/f noise, which is the noise generated by surface states or impurities in the surface of the silicon under the gate of a transistor. This noise can be quite large at low frequencies and its magnitude varies inversely with frequency. 1/f noise was minimized in the operational amplifier by using p-channel transistors for the differential stage inputs. Hewlett-Packard's CMOS process in Corvallis, Oregon uses n-type substrates and implanted p wells for fabricating the n-channel transistors.[1] The p-channel tran-

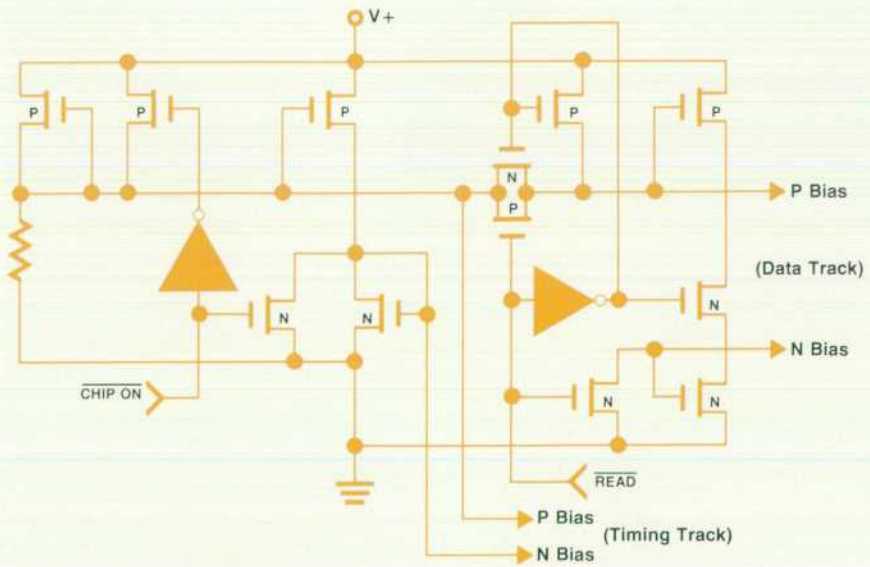

Fig. 3. *Bias generation circuitry of CMOS card reader IC.*

sistors are fabricated in the substrate and the substrate has much less crystal damage than the p wells since no implant is done under the gate of a p-channel transistor. This reduces 1/f noise in a p-channel transistor by an order of magnitude compared to an equivalent n-channel transistor fabricated in this process.

To reduce the input offset voltage for the operational amplifier, it was necessary to match the first-stage transistors as much as possible using circuit layout techniques. The gate of each first-stage input transistor is divided into two parts and drawn in an alternating fashion. This ensures that the input transistors are closely matched.

One final concern in the design was to compensate for high-frequency instabilities. These instabilities can be understood by looking at plots of gain and phase for the operational amplifier (Fig. 2). As the frequency of the input signal increases, the phase delay approaches 180 degrees. The amplifier is commonly used in a negative feedback mode, which means that the output signal is fed back into the negative input of the amplifier either directly (unity gain) or through some resistive network. This reduces the differential voltage between the positive and negative inputs of the operational amplifier and allows the voltage gain to be controlled. When the phase delay of the input signal is greater than 180 degrees, the amplifier enters a positive feedback mode and control of gain is lost. To solve this problem, we made sure that when the phase approached 180 degrees, the gain of the amplifier would be less than 1. This was accomplished by placing the gate capacitance of a large n-channel transistor between the output of the first-stage differential pair and ground. This reduces the gain-bandwidth product of the operational amplifier and prevents the high-frequency instabilities from affecting normal circuit operation.

Another circuit (Fig. 3) was needed to generate the bias voltages for the current-source transistors. This bias generation circuitry also generates a separate set of bias voltages for each of the sets of amplifiers in the read and data tracks and has the capability of shutting off the read and/or data tracks to conserve power when the card reader is not in use. To generate the bias voltages, an external resistor is used to set the current in a p-channel transistor whose gate and drain are connected together. The resistor was chosen such that the voltage at the gate and drain of the p-channel transistor is 0.5 volt above threshold. This voltage is used to set the current in the timing track operational amplifiers and is also fed through a transmission gate to generate the bias for the data track amplifiers. To shut off the timing track and data track operational amplifiers, a control signal from the digital portion of the IC pulls this bias voltage point to the supply voltage level.

The bias voltages for the n-channel current sources in the output stages of the operational amplifiers are generated by mirroring the current in the external resistor through an n-channel transistor whose gate and drain are tied together. This current mirror is repeated separately for the data track operational amplifiers and turned off by another control signal generated in the digital portion of the IC. This is done to turn off the data track operational amplifiers during a write operation.

Fig. 4, a picture of the card reader IC, shows how the analog circuitry is separated from the digital circuitry. The operational amplifiers are in two rows, with one row implementing the timing track read circuitry and the other row implementing the data track read circuitry. The amplifiers are connected by interconnect metal, polysilicon, and p-type resistor implants. A large, grounded p well is also used to isolate the analog circuitry from the digital circuitry.

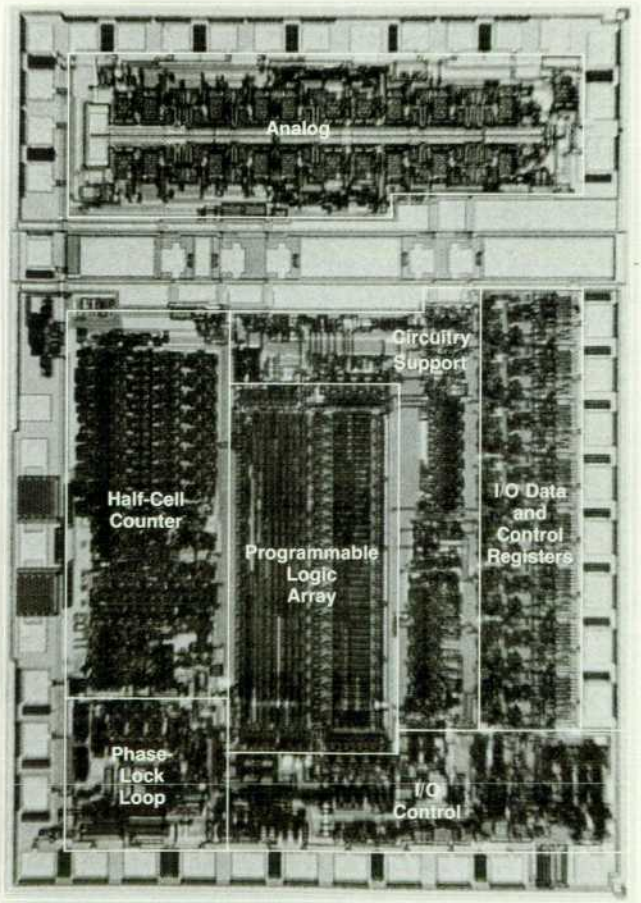

Fig. 4. *Photograph of card reader integrated circuit used in the HP-75 Portable Computer.*

Acknowledgments

Bob McCharles provided much guidance in the initial design of the operational amplifier. Ed Guertin provided valuable assistance in the IC layout and artwork generation. Doug Peck developed the program for production testing.

Reference

1. N.L. Johnson and V.J. Marathe, "Bulk CMOS Technology for the HP-41C," Hewlett-Packard Journal, Vol. 31, no. 3, March 1980.

A New Family of Pulse and Pulse/Function Generators

Here are three compact, easy-to-use instruments with the versatility needed for analog and digital applications over wide frequency and amplitude ranges.

by Michael Fleischer, Helmut Rossner, and Uwe Neumann

PULSE AND FUNCTION GENERATORS are basic measurement tools that provide controllable stimuli for stimulus/response testing of all kinds of analog and digital circuits. Two versatile new HP instruments now combine the capabilities of pulse generators and function generators in compact, low-cost packages. Designed to go beyond the performance range of existing function generators, both units offer a true pulse mode in addition to standard functions such as sine, triangle, square and haversine waveforms. Various trigger and modulation modes allow external control over all instrument functions. New operating concepts with error recognition make using all these capabilities a simple task.

Fully HP-IB (IEEE-488) programmable, the HP 8116A, Fig. 1, is a 50-MHz instrument for bench automation as well as for system integration. At lower cost, but with capabilities enhanced by a digital readout for all parameters, the 20-MHz HP 8111A, Fig. 2, is well suited for manual bench and service applications.

A third instrument in this family, Model 8112A Pulse Generator, Fig. 3, is an HP-IB programmable 50-MHz pulse generator that offers external modulation modes and other features. All three instruments have a basic accuracy of 5%. Table I compares their features.

Pulse/Function Generator Features

The 8116A Pulse/Function Generator operates over a wide 1-mHz-to-50-MHz frequency range and provides up to 32V peak-to-peak amplitude. Proper functioning is assured by automatic self-test and error recognition capabilities. Self-test and diagnosis are performed each time the instrument is turned on. Error recognition helps the operator recover from an incorrect front-panel or programming operation. Variable duty cycle makes it possible to generate constant-energy pulses and asymmetrical waveforms. Thus dc motor control, CRT deflection, material test, and servomechanisms are among the applications for this instrument. The 8116A has comprehensive trigger and gate capabilities including sweep (Option 001) and counted burst. In the latter case, the burst can be internally triggered because a second internal rate generator operates independently of the period generator. Combining trigger and modulation modes results in capabilities such as the generation of amplitude-modulated sine-wave bursts. These simulate transient responses or width-modulated pulse bursts similar to phase jitter in communication applica-

Fig. 1. *Model 8116A Pulse/Function Generator has standard function generator capabilities and a pulse mode suitable for testing CMOS and TTL logic. It is HP-IB programmable and operates over a frequency range of 1 mHz to 50 MHz. Logarithmic sweep is optional.*

Fig. 2. *Model 8111A Pulse/Function Generator is a low-cost 1-Hz-to-20-MHz unit for manual bench and service applications.*

Fig. 3. *Model 8112A Pulse Generator has all of the traditional pulse features for testing digital circuits, along with modulation capabilities useful for analog testing. It is HP-IB programmable and has a maximum repetition rate of 50 MHz.*

tions. The 8116A's pulse mode characteristics are suitable for testing many logic families such as CMOS and TTL. Transitions are faster than 6 nanoseconds and width can be programmed down to 10 nanoseconds. Programmable width also means that low-duty-cycle events can be simulated.

The low-cost 8111A Pulse/Function Generator offers a wide 1-Hz-to-20-MHz frequency range for all modes. Pulse width is variable down to 25 nanoseconds, and variable duty cycle is available for sine, triangle, and square waves. Therefore, ramps and sawtooth waveforms and constant-energy pulses can be generated. Small amplitudes down to 1.6 mV for sensitivity testing and large signals up to 16V into 50 ohms for stress and operational testing are available with variable offset.

Pulse Generator Features

The 8112A Pulse Generator has all the traditional pulse features for testing digital circuits, including delay, double-pulse, and variable slopes, plus unusual capabilities, such as modulation modes to test analog circuits like those in disc drives. All basic timing parameters such as period, delay, double-pulse spacing, and width can be modulated within a decade range by applying an external voltage to the control input of the 8112A. In addition, there is a high-level control mode in which the low level is programmable and the high level follows the voltage applied at the control input. These control modes can be accessed concurrently with the trigger capabilities (triggering is feasible on both slopes at the same time and the modes include counted burst and gate). There are two input connectors, one for trigger signals and one for control signals. Thus complex signals can be generated, such as pulse trains amplitude modulated with low-frequency noise. The 8112A can provide a cosine-shaped output for simulating bandwidth-limited signals or Gaussian transitions, in addition to variable linear transitions which allow triangular and trapezoidal waveforms to be generated.

Table I

Pulse and Pulse/Function Generator Features

		8112A	8111A	8116A
Timing	Maximum frequency (MHz)	50	20	50
	Transition time (ns)	≥5 (variable)	<10	<6
	Minimum width (ns)	10	25	10
	Square-wave duty cycle (%)	1-99	10-90	10-90
	Variable delay	yes	no	no
Output[1]	Amplitude (V)	32	32	32
	Offset/window (V)	±16/±16	±16/±16	±16/±16
	Formats (positive, negative, symmetrical, normal, and complement)	all	all	all
Operating Modes	Trigger	yes	yes	yes
	External width	yes	no	yes
	Gate	yes	yes	yes
	External burst	yes	option	option
	Internal burst	no	no	option
	Double pulse	yes	no	no
Control (modulation) Modes		yes	yes	yes
Waveforms	Sine (symmetry)		10-90%[2]	10-90%[3]
	Square (duty cycle)	1-99%	10-90%[2]	10-90%[3]
	(transitions)	≥5ns	<10 ns	<6 ns
	Triangle (symmetry)		10-90%[2]	10-90%[3]
	Haversine (symmetry)	5-95%	10-90%[2]	10-90%[3]
	Havertriangle (symmetry)	5-95%	10-90%[2]	10-90%[3]
	dc	±16V	±16V	±15.9V
HP-IB		yes	no	yes

Notes

1. Voltages shown are for high-impedance load. Divide by 2 for 50Ω load.
2. 10-50% above 1 MHz.
3. 20-80% above 1 MHz.

User-Friendly Operating Concept

Convenient operation with clear layout of the controls in a compact front panel were important design objectives of the 8112A Pulse Generator and the 8116A Pulse/Function Generator. Five (or, in the case of the 8116A Option 001, eight) operating modes are selected by just two pushbuttons, each of which accesses and rolls a list of modes. An illuminated LED shows the mode selected (Fig. 4).

Each parameter (frequency, amplitude, etc.) can be called into a three-digit display by a selector key. The selected parameter, which is indicated by the LED in the key, can be changed in value by means of rocker switches, one for each display digit. A fourth rocker selects the range. When the rockers are pressed at the top or bottom, the corresponding digit is stepped up or down.

With the 8116A's four waveforms (sine, triangle, square, and pulse) and eight operating modes, up to 13 parameters are selectable. Up to seven can be active at the same time in a

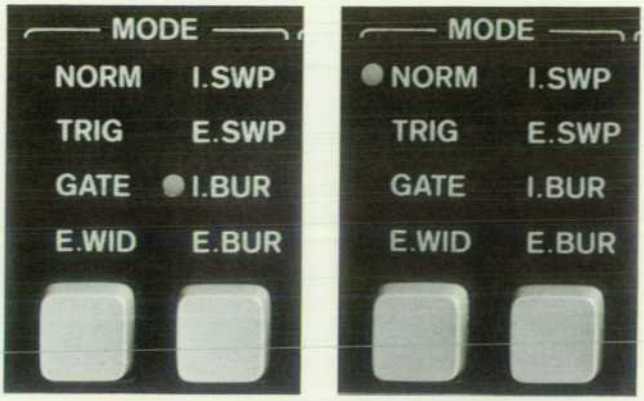

Fig. 4. *Two pushbuttons select the operating mode of the 8116A or 8112A. An illuminated light-emitting diode shows the mode selected.*

single operating mode. The 8116A's self-prompting menu relieves the user of the need to remember the applicable parameter combination. Automatic backlighting makes only the parameter mnemonics appropriate to the selected mode and waveform visible, so that an error-free choice can easily be made (Fig. 5).

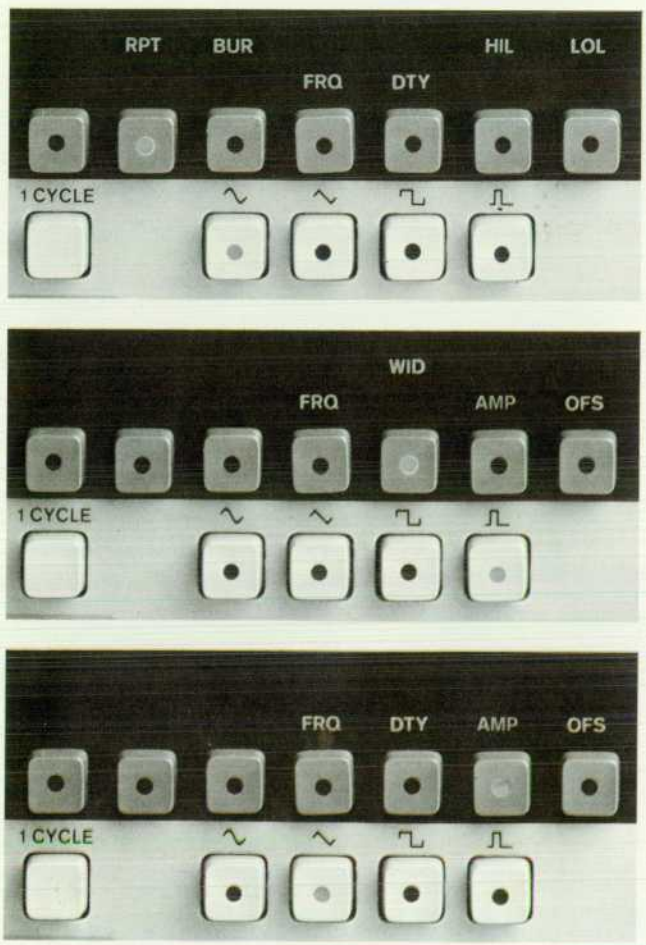

Fig. 5. *The 8116A prompts the user by backlighting only the parameter mnemonics appropriate to the selected mode and waveform.*

Pulse generators, as distinct from function generators, have a number of parameters such as delay, double-pulse spacing, width, and transition times (leading edge and trailing edge) that must harmonize with the period. These parameters can also be influenced by the external trigger and analog timing control voltages. Consequently, in the past, even an experienced user could easily select incompatible settings. This problem is eliminated by the 8112A's **SET** key. When this key is pressed, the internal microprocessor selects timing parameters compatible with the user-selected period and maintains the ratio of these parameters to the period as the period is varied. This simplifies operation by providing immediate recovery from an error condition, error-free setup for any desired period, and the ability to generate period-controlled "standard" pulses.

With the 8116A and the 8112A when the **SET** key is not used, incompatible states and operating conditions can occur. The instrument conforms as far as possible to the user's choices and errors are permitted but clearly indicated. The LEDs of mutually exclusive operating modes flash when their concurrent selection is attempted. Hardware detection of excessive delay or width (i.e., greater than the period minus 10 ns) ensures that the user can always exploit the full duty cycle capability (virtually 100%). Triangular waveforms can be set up on the 8112A because the transition times can be set greater than the width. An excessive-slope indication is displayed so that the user knows that the amplitude of the triangle is less than the set value.

The 8112A and 8116A feature a limit mode to safeguard devices under test. When the limit mode is activated, the existing HIL and LOL values become the limits for the output pulse. It is then no longer possible to set a larger output and devices are protected from inadvertent destruction.

A special feature of the 8116A is auto vernier. After pressing the **AUTO** key, any parameter can be selected for continuous incrementing. This continues until the range limit is reached, or until stopped by an external command. This provides the advantages of swept measurements. In manual operation, semiautomatic loops can be set up that allow the threshold value of various parameters to be measured and displayed. In automatic operation with an HP-IB controller, the 8116A needs only to be started. During the test, the controller is free for other tasks.

In the 8112A, to facilitate complex setups, up to nine complete user-defined instrument settings can be stored and recalled. An additional memory location contains standard settings. These settings are automatically implemented if the instrument is switched off in an error condition.

User-Friendly HP-IB Interface

One of the major objectives of the programmable 8112A and 8116A was simple front-panel and HP-IB operation.

For the HP-IB interface, we decided to accept a slower interpreter to get an easily understandable syntax for the parameter, mode, and special commands, which can be read directly from front-panel lettering. All parameter commands are constructed according to the following scheme:

PAR DATA EX UN

PAR = Parameter designator
DATA = Real or integer numbers
EX = Positive or negative exponent
UN = Unit

Examples:

FRQ 1.56 kHz (also programmable as FRQ 1.56 E+3 Hz)
HIL 4 V
AMP 10 mV (also AMP 10.0 E−3 V)

A useful feature in the remote state is background programming. This allows nonactive parameters (which cannot be changed locally) to be modified, ready for future use,

Feedback Amplifier Has Push-Pull Voltage Output Stage

The output amplifier for the 8116A and 8111A Pulse/Function Generators and the 8112A Pulse Generator had to fulfill many different requirements.

- Low distortion (<50 dB) for 8111A/8116A function generator capability
- High frequency range (dc to 50 MHz for the 8112A and 8116A)
- High slewing rate, especially for the 8112A (>5.12 kV/μs)
- Low power dissipation
- Easy interface to the Booster IC.

For low distortion, we decided to design a feedback amplifier with a voltage output stage, which requires only 25% of the power dissipated by a differential amplifier current-output stage.

Fig. 1 shows the Booster IC with a current mirror working into the amplifier's active current sink, which means a virtual ground at the inverting input of the output amplifier, caused by the feedback via R. The output amplifier consists of a low-offset low-frequency operational amplifier and a special high-frequency power amplifier (see Fig. 2). The low-frequency gain is determined by

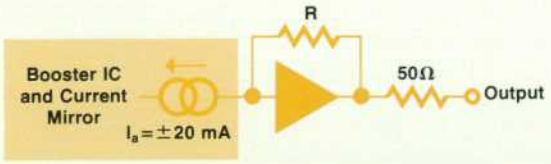

Fig. 1. *The Booster IC's current mirror works into the output amplifier's active current sink.*

R4/R3, and the high-frequency gain is determined by R2/R1. A second virtual ground is generated at the inverting input of the low-frequency amplifier, so that the offset signal I_b can be brought in on a lower level than the signal current from the Booster IC (±20 mA), i.e., less than 100 μA.

Fig. 3 shows the simplified schematic of the high-frequency amplifier.

Q5 and Q6 form the emitter-follower voltage output stage. Q3 and Q4 are a common-emitter stage needed to generate the necessary high open-loop gain. The ratio R_C/R_E determines the slewing rate and the transit frequency of the loop gain. This means that these resistors set the phase margin of the closed loop and therefore the frequency or pulse response. Lead compensation with C_E is possible to achieve stability. This is feasible even in the 8112A, which has the highest slewing rate and bandwidth of these three instruments.

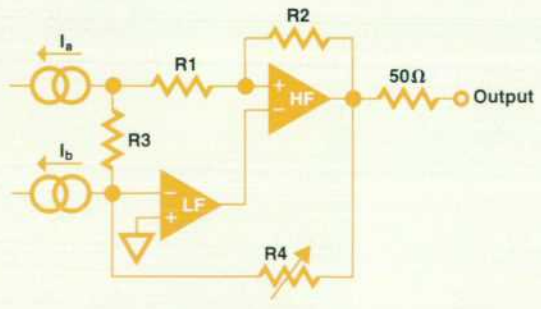

Fig. 2. *The output amplifier consists of a low-offset low-frequency operational amplifier and a special high-frequency power amplifier.*

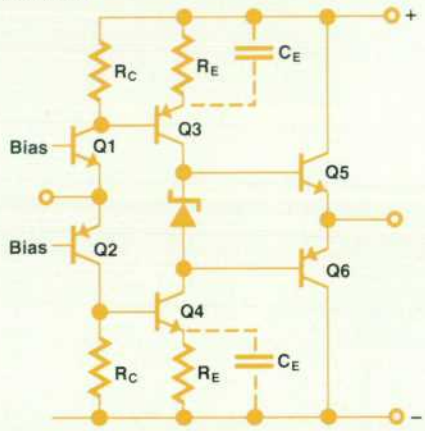

Fig. 3. *Simplified schematic of the high-frequency amplifier.*

Q1 and Q2 form the input stage, working in a common-base configuration with a low input impedance even without feedback. This approach instead of a differential amplifier stage with a high input impedance is rather unusual, but necessary for the following reason. Imagine the Booster IC switching from $I_a = +20$ mA to $I_a = -20$ mA. If the input stage of the amplifier of Fig. 1 were a differential amplifier, then for a time as long as the transition times of the amplifier (determined by slewing rate), the loop would be open and a rather large negative spike would appear at the inverting input of the amplifier because of its high input impedance. Even for medium ranges of the input impedance, this spike would drive the Booster current source into saturation (maximum allowed low level is about −0.7V). Therefore, a common-base stage with a low input impedance and, of course, better high-frequency performance was chosen.

This amplifier maintains its good pulse performance inside a large level window (±16V), regardless of the combination of amplitude (100 mV to 32V) and offset (±15.9V).

Acknowledgments

Special thanks to Stephen Bolz who had the original idea for this amplifier, and who did most of the design. He was also project leader of the 8111A. Many others from R&D and production contributed during the critical stages of introduction and the early production stages.

-Michael Fleischer

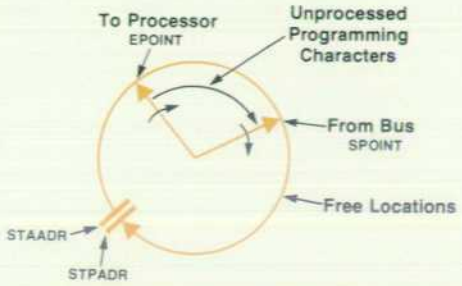

Fig. 6. *Structure of the HP-IB buffer in the 8116A and 8112A.*

without influencing the current operation. This means, for example, that start frequency, sweep time, and marker frequency can be modified in the normal mode without changing the output signal. All appropriate parameters are then implemented when the single command for activating the sweep mode is given.

The HP-IB implementation aims particularly at the applications field of the individual instrument. Thus, special accent is put on supporting the leading operating features such as the 8116A's auto vernier and the 8112A's recallable settings. The 8116A's auto vernier can be started from a selected parameter value via the HP-IB as well as the front panel. Because the vernier increments or decrements automatically until a stop signal is received at the external trigger input (or until a limit is reached), a software loop is not required. The 8112A's store/recall capability can also be implemented via the HP-IB. A single command is all that is needed to implement or store a complete set of instrument settings. Each of the nine store locations in the 8112A can be addressed from the controller.

Another contribution to the friendly human interface of the 8112A and the 8116A is that the HP-IB address is indicated in the display when the **LOCAL** key is held down. The address appearing in the display is automatically transferred to the HP-IB interface.

To simplify setup and documentation, both the pulse generator and the pulse/function generator have comprehensive talker capability. Upon command, the current values of all parameters, modes and special functions are transmitted in an ASCII string. This can be saved in the controller's mass storage memory, and can be retransmitted to the generator in exactly the same form. Also, any parameter required for modification or evaluation can be interrogated. The generator returns an ASCII string that contains the parameter's name, the value, and the unit (e.g., FRQ 1.00 MHz). If a service request (SRQ) occurs and the generator is interrogated with IERR, a detailed error message is output to the bus. For example, the incompatible setting of gate mode with 'trigger on both slopes' is depicted by the string "gate, both slopes." A status byte register offers a quick system overview by reporting when errors have occurred and on the general status. In addition, the 8112A has the ability to output stored parameter sets without changing the actual machine state.

A special HP-IB buffer lets the controller transmit at full speed without waiting for the 8112A or 8116A microprocessor to interpret and verify the commands. This buffer is like a FIFO register without shift operations. Its physical limits are the start address STAADR and the stop address STPADR (Fig. 6). The pointer SPOINT marks the next free memory location. A received character is stored into this location and then the pointer is incremented one step clockwise. After finishing the operation from the bus, the microprocessor interprets the commands in the segment indicated by EPOINT. The condition EPOINT−SPOINT=1 denotes a full buffer and SPOINT−EPOINT=1 an empty buffer. If the buffer is full and further characters are received, transmission on the bus is stopped until the next commands in the buffer are executed.

The advantages of this buffer structure are:

- The physical buffer area can easily be adapted to special

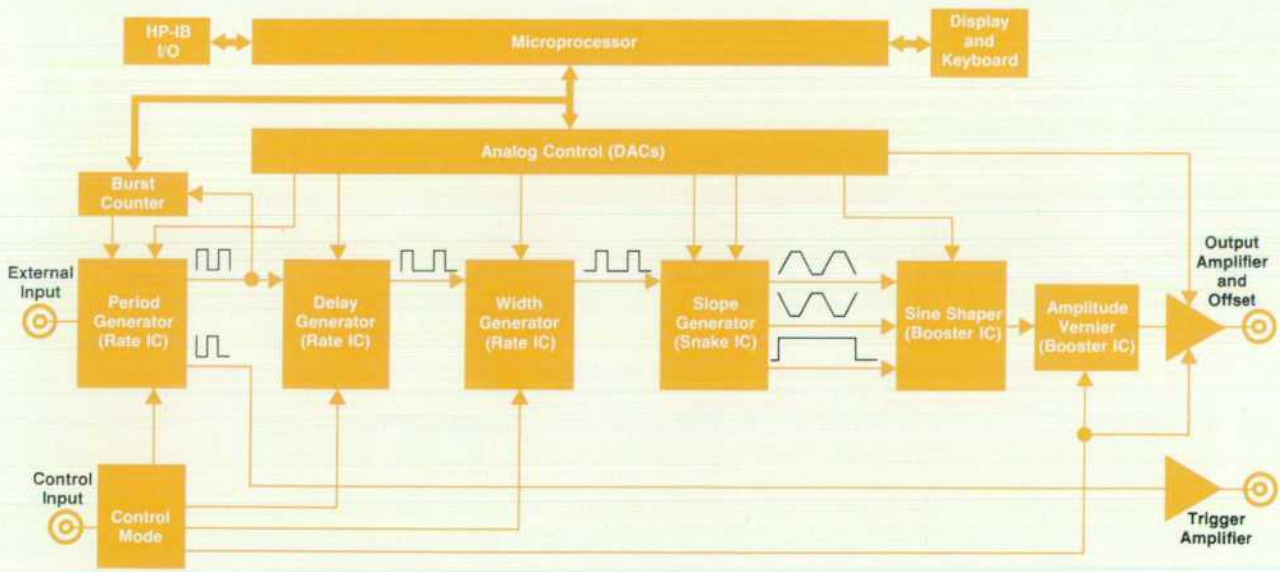

Fig. 7. *Block diagram of the 8112A Pulse Generator. Three custom integrated circuits (Rate, Snake, and Booster) are used in all three instruments in the family. The output amplifier is also common to all three instruments.*

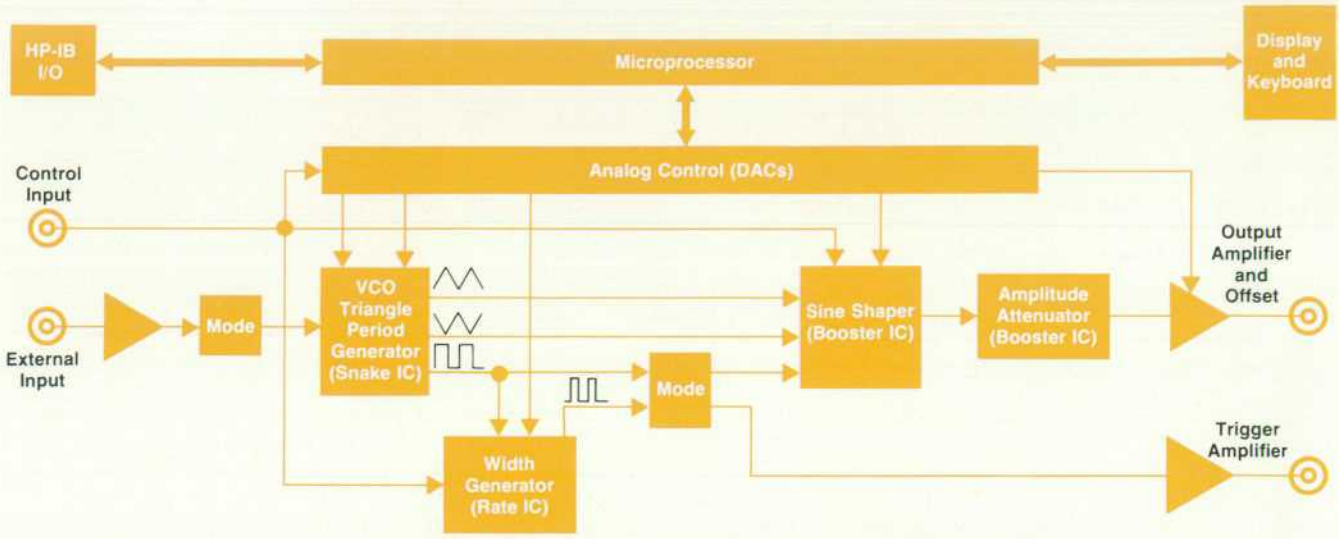

Fig. 8. *Block diagram of the 8116A Pulse/Function Generator.*

device specifications by shifting the start and stop addresses to the desired values.

- The rotating pointers avoid the time-intensive shift operations which would otherwise be necessary for buffer modification.

Custom IC Design

Figs. 7 and 8 are block diagrams of the 8112A Pulse Generator and the 8116A Pulse/Function Generator, respectively. Many functional blocks are similar in the two instruments. This led to the design of three large-scale integrated circuits.

- The Rate IC is an astable or monostable multivibrator. It serves as the repetition rate generator in the 8112A and as the width/double-pulse-delay generator in the 8111A, 8112A, and 8116A.
- The Snake IC is an integrator. It works as a slope generator in the 8112A and as a triangle repetition-rate generator in the 8111A and 8116A.
- The current-controlled amplifier and sine shaper Booster IC is used in all three instruments.

The many pulse features of the two pulse/function generators and the traditional function generator capabilities of the 8112A pulse generator were made feasible by these ICs. Detailed descriptions and a general overview of these ICs are presented in the following article.

The same output amplifier concept is used in all three instruments. Only details are changed for individual requirements. The concept is described in the box on page 30.

Acknowledgments

We want to thank section manager Werner Huettemann and project manager Peter Bruenner who defined the family of instruments and who helped out with ideas and advice during the projects. Werner Moehrle, Guenter Eckert, and 8116A project leader Rainer Plitschka contributed to the hardware and software design. Hartwig Bartl and Rudi Vosdecky did the mechanical design. Special thanks to Christian Hentschel and his section who designed the custom ICs.

Designing Bipolar Integrated Circuits for a Pulse/Function Generator Family

by Christian Hentschel, Adolf Leiter, Stephan Traub, Horst Schweikardt, and Volker Eberle

THE HEART of a pulse/function or pulse generator always consists of the same few functions. These functions are:

- A clocking generator, either square or triangle, synchronously startable as a special feature
- Time-segment-definition circuits to generate pulse width and delay
- Circuits for signal shaping, like sine shapers, slope generators for the generation of variable transition times, or amplifiers.

These functions are normally realized with conventional discrete circuits and have a very high component count.

For the 8111A/8112A/8116A Pulse/Function Generator IC program, these objectives were set:

- Drastically reduce the total number of components, thus also reduce the printed circuit board floor space
- Save costs by reducing material and labor
- No sacrifice in performance
- Improve reliability.

Three different circuits were thought to be the best compromise. For easy reference, they are called the Rate, Snake, and Booster ICs. HP's proprietary 1-GHz bipolar process was the best choice for the kind of complexity and the 50-to-100-MHz operation required. The characteristics of this process are:

Transit frequency: 600 to 1000 MHz
Base sheet resistance: 220 to 275 Ω/□
Forward current gain (npn): 50 to 200
Forward current gain (pnp): 15 to 50
Devices: npn, lateral pnp, base resistor, emitter resistor, Zener diodes, junction capacitors
Technology: diffusion process and dual-layer metallization system with selective anodization of the first metal layer
Complexity: up to 2000 transistors.

Because of the many possible errors and the high cost and long processing time of each modification, it is extremely important to verify any IC design thoroughly. All three ICs were simulated both with discrete hardware and the HP SPICE network analysis program. Another type of simulation was used to estimate voltage drops on power supply buses.

After mask design, mask making, wafer processing, packaging and testing, it is the designer's task to verify the performance and consistency of the circuit. This is most efficiently done with an automatic test system and a circuit analysis program, which we used extensively.

The Rate IC

The Rate IC (Fig. 1) is a monolithic timing circuit that produces triggerable and gateable repetition rate, pulse width, and pulse delay. Eight decades with analog control within each decade enable repetition rate settings from 1 Hz to 100 MHz and pulse width or pulse delay settings from 10 ns to 1 s without switching external range capacitors. An internal analog multiplier/divider allows frequency-proportional or period-proportional control of the current-controlled oscillator. The oscillator frequency is tunable from 10 MHz to 100 MHz in the fastest range (R1), and from 2 MHz to 20 MHz in range R2. Lower frequencies (or larger

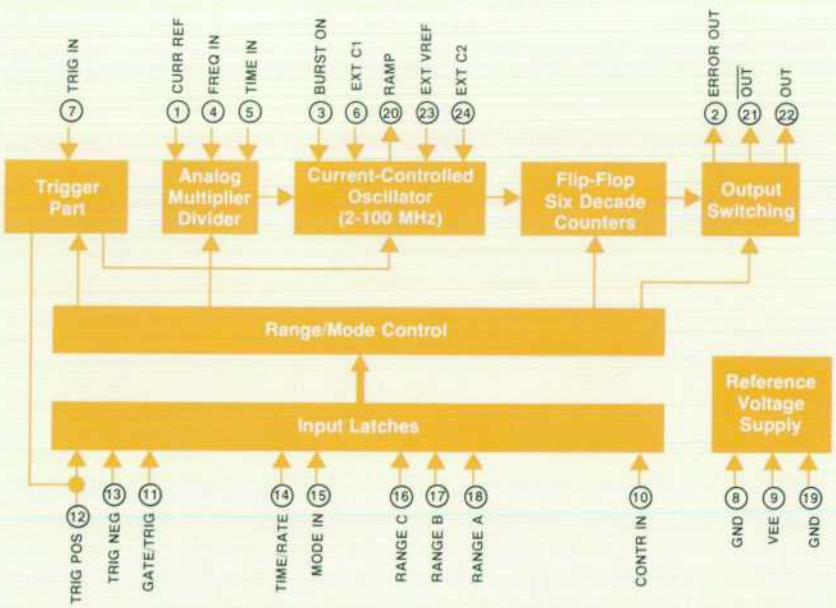

Fig. 1. *Block diagram of the Rate IC, a monolithic timing circuit.*

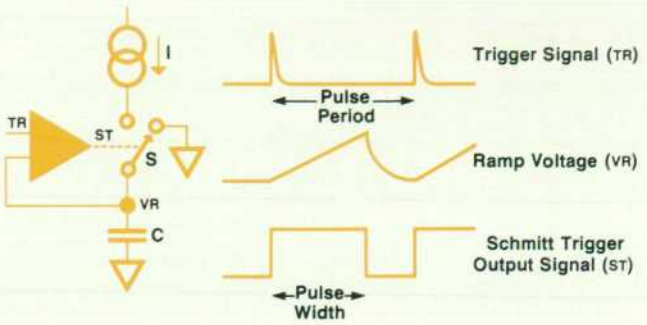

Fig. 2. *Simplified schematic and timing diagram of a conventional pulse width generator.*

width or delay) are achieved by an internal flip-flop and decade counters. A special feature of this circuit, the 100% retrigger capability, allows high duty cycles to be generated.

Various trigger and gate features are available, depending on the trigger mode setting. The trigger input has positive/negative trigger, double trigger, and positive/negative gate functions. The manual input has positive trigger and positive gate functions. In gate-through mode the circuit can be used for reshaping trigger input signals. In trigger-through mode a 3-ns spike is generated on each positive or negative slope or both slopes of the input signal. Generating a counted number of pulses is possible by triggering the trigger input and using a gate feedback signal from an external counter to the burst-on input. All digital mode and range select lines are TTL compatible. Input latches have been included so that the IC is also suitable for use in programmable instruments. A TTL positive slope at the control enable pin latches all digital information, and a negative level (−5.2V) sets the input latch in the through modes to enable direct access to all data inputs. The analog current-reference, frequency, and time inputs are virtual-ground current inputs. The outputs OUT, $\overline{\text{OUT}}$ and ERROR OUT are open-collector outputs.

The chip size of the Rate circuit is 3.7×3.5 mm, and the number of transistors is approximately 1400.

Conventional Pulse Width Generator

A typical approach to generating a variable pulse width in conventional pulse generators is shown in Fig. 2. After the generator has been started by a trigger signal, a capacitor is charged with a constant current until the ramp voltage reaches a certain level. The elapsed time between the trigger point and the ramp's reaching the Schmitt trigger level determines the pulse width. Switch S then changes position and connects the capacitor to ground. The capacitor has to be discharged to 0V before the next event can be started.

The capacitor cannot be discharged within an infinitely short time, and consequently the pulse width is less than the repetition time by the discharge time. Thus, the maximum duty cycle of conventional pulse generators is limited to about 50 to 90% at high frequencies. Also, since the frequency range is usually achieved by switching ramp capacitors, it is not possible to get close to a 100% duty cycle in low-frequency ranges either, because the ratio between charge and discharge times remains nearly the same.

IC Pulse Width Generator

The approach used in the Rate IC avoids this disadvantage. The circuit is shown in Fig. 3 and the timing diagram of the trigger mode is shown in Fig. 4. In the stationary condition, the output voltage of the RS flip-flop is low (this level is also the clamp reference voltage) and the Schmitt trigger output is high. Because the electronic switch is in position 1, the current through each diode equals I. Thus the voltage at capacitor C is clamped to the output voltage of the flip-flop.

When a trigger signal occurs, the flip-flop is set to its high level. This reverse-biases diode D2 so that the ramp capacitor charges with a constant current I. When the upper trigger level is reached, the Schmitt trigger switches to low, switch S changes to position 2, and the flip-flop is reset to its low level. Now diode D1 is reverse-biased so that the capacitor discharges with the difference current I−2I = −I until the lower Schmitt trigger level is reached. When this occurs, the Schmitt trigger output goes high and switch S reverts to position 1.

Since the low levels of the Schmitt trigger and the flip-flop are the same, the ramp voltage is clamped to the start level. As shown in Figs. 3 and 4, the OR combination of the

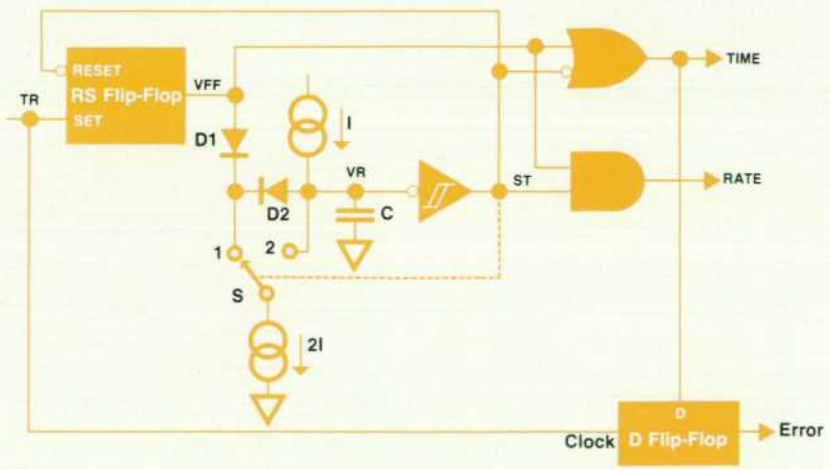

Fig. 3. *Schematic of the 100% retriggerable pulse width generator and error detector of the Rate IC. The circuit can be restarted immediately after being stopped.*

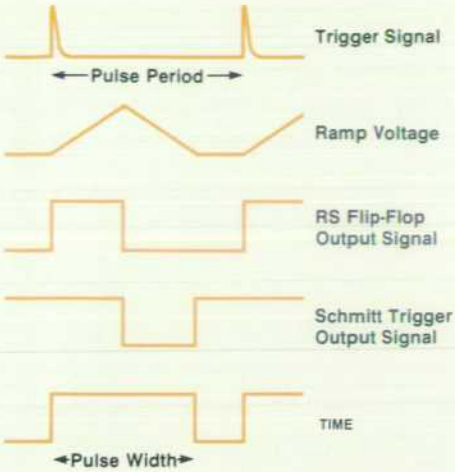

Fig. 4. *Timing diagram for Fig. 3 in trigger mode.*

flip-flop output with the inverted Schmitt trigger output produces a TIME signal that corresponds to the pulse width. Since the stop condition of the oscillator is the same as the start condition, the oscillator can be retriggered immediately. This is the big advantage of this circuit.

Fig. 5 shows the timing diagram in gate mode. Important for this mode is that the SET input of the flip-flop has higher priority than the RESET input. This means that the reset function is disabled as long as the SET input is high.

The start conditions are the same as in Fig. 4. The generator runs as long as the gate signal is high, and stops only when the current event is completed. The TIME output is a whole-number multiple of the width setting.

The AND combination of the flip-flop and the Schmitt trigger (RATE signal) provides a gated repetition-rate-generator function. This means the width of the external gate signal determines the number of pulses. Consequently, when the gate signal is delivered from an external counter, a counted number of pulses can be generated.

The Snake IC

The Snake IC performs two selectable functions: triangular waveform generation up to 50 MHz, in which it acts as a signal generator, or slope generation down to 4.5 ns, where it modifies an applied signal. It contains 350 transistors.

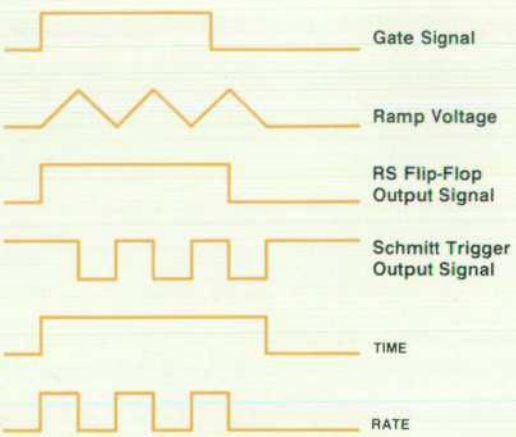

Fig. 5. *Timing diagram for Fig. 3 in gate mode.*

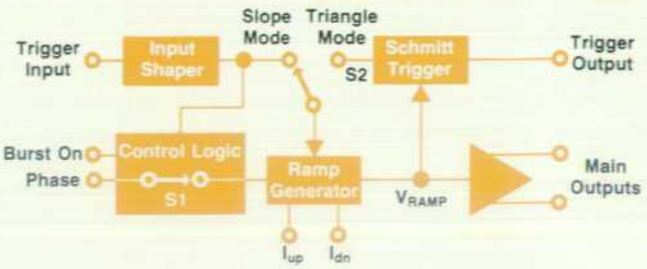

Fig. 6. *Simplified block diagram of the Snake IC in slope mode. This IC can act as a triangular waveform or slope generator.*

The chip area is 6.82 mm². It uses +5V and −5.2V power supplies and has a power consumption less than 1.5W.

The heart of this IC is the ramp generator (see block diagram. Fig. 6). It supplies two currents (I_{up} and I_{dn}) alternately to a ramp capacitor. Its function is similar to many conventional ramp generators, and allows continuously variable slopes to be generated. The selection of slope mode or triangle mode is made by switches S1 and S2.

In slope mode, a single transition is generated on each transition at the trigger input. Switch S1 is closed so that the upper level of the V_{RAMP} signal is defined by the voltage at the phase input. The lower level is at ground potential. Fig. 7 shows typical waveforms.

In triangle mode, a Schmitt trigger provides feedback so that the ramp generator oscillates. When S1 is opened, the triangle waveform starts synchronously with a positive transition, and the turning points are determined by the Schmitt trigger. If S1 is closed, oscillation will cease when a positive ramp transition reaches the voltage at the phase input. Consequently, the last cycle is always completed. This is termed gate operation, a submode of the triangle mode. Fig. 8 shows typical waveforms in triangle mode.

Triangle mode can also be modified by the trigger submode. Here, a single triangle is generated on each positive transition at the trigger input. This is achieved by differentiating the input pulse with a 5-ns delay line. The delay line is in the input shaper block and consists of ECL-like gates. A combination of the trigger and gate submodes allows counted bursts to be generated.

Electronic pnp

One of the interesting details in this IC is the circuit that selects one of two possible ramp voltages, V_{RAMP1} and V_{RAMP2}, to feed the Schmitt trigger and the output amplifier. The circuit consists of a diode bridge, two current sources I and I_1, and a selection voltage INT/EXT (Fig. 9).

For a balanced bridge, where $V_{RAMP}=V_{OUT}$, the currents through the diodes must be equal, i.e., $I_1=2I$.

The current source I is usually made with a single pnp transistor. However, there is a lack of good pnp transistors

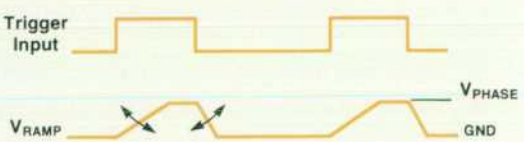

Fig. 7. *Snake IC ramp generator timing in slope mode.*

Fig. 8. *Snake IC ramp generator timing in triangle mode.*

in the IC process used (current gain and maximum current are low). Consequently, the electronic pnp in Fig. 9 was devised.

The current I generated by the network is given by:

$$I = (V_{B1} - V_{BIAS})/R - V_1/R_2 \quad (1)$$

Since the circuit's output current in equation 1 is not a function of V_{OUT}, it is apparent that the circuit is a current source and that the electronic pnp has been realized. Making $I = I_1/2$ to balance the bridge, equation 1 then gives the relation for the selection of resistors and voltages:

$$(V_{B1} - V_{BIAS})/V_1 = R/R_2 + R/2R_1 \quad (2)$$

If V_{BIAS} and V_1 are independent of temperature, equation 2 shows that the bridge balance can be made independent of temperature and V_{RAMP} by matching the values of R, R_1 and R_2.

The rated current of the electronic pnp is 4.33 mA. This is needed for speed and is much more than the pnp transistors of this process can handle.

The Booster IC

The Booster is a sine shaper, pulse shaper, amplitude modulator and vernier IC. It has 308 transistors, most of them very large, up to 16 times minimum size. The chip size is 2.85 by 2.85 mm.

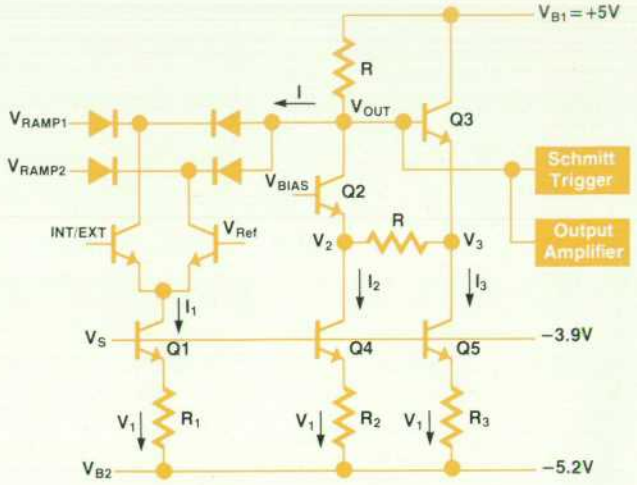

Fig. 9. *This circuit on the Snake IC selects one of two possible ramp voltages to feed the Schmitt trigger and output amplifier. The current source I is usually realized with a single pnp transistor, but since the IC process used does not have adequate pnp transistors, this electronic pnp implementation was devised.*

The main inputs are differential, linear current inputs at virtual ground potential leading to a waveforming stage (Fig. 10). This stage can be used as a linear feedthrough, as a triangle-to-sine converter, or as a shaper for generating pulses with rounded edges. There is also a voltage-controlled input for generating pulses with fast, fixed rise times. This input is EECL-compatible, i.e., −0.8V and 0V levels.* Waveform selection is made by two digital inputs which are TTL- as well as CMOS-compatible.

*EECL is an HP integrated circuit process that is similar to ECL (emitter coupled logic). EECL logic levels are 0 and −0.8 volts. ECL levels are −0.8 and −1.6 volts.

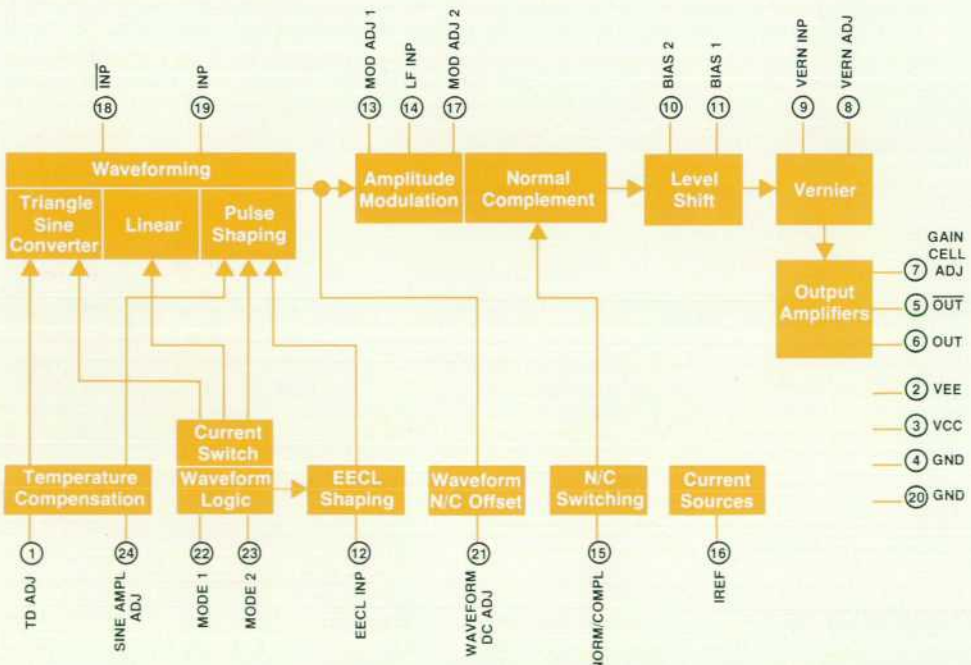

Fig. 10. *Block diagram of the Booster IC, a sine shaper, pulse shaper, amplitude modulator, and vernier.*

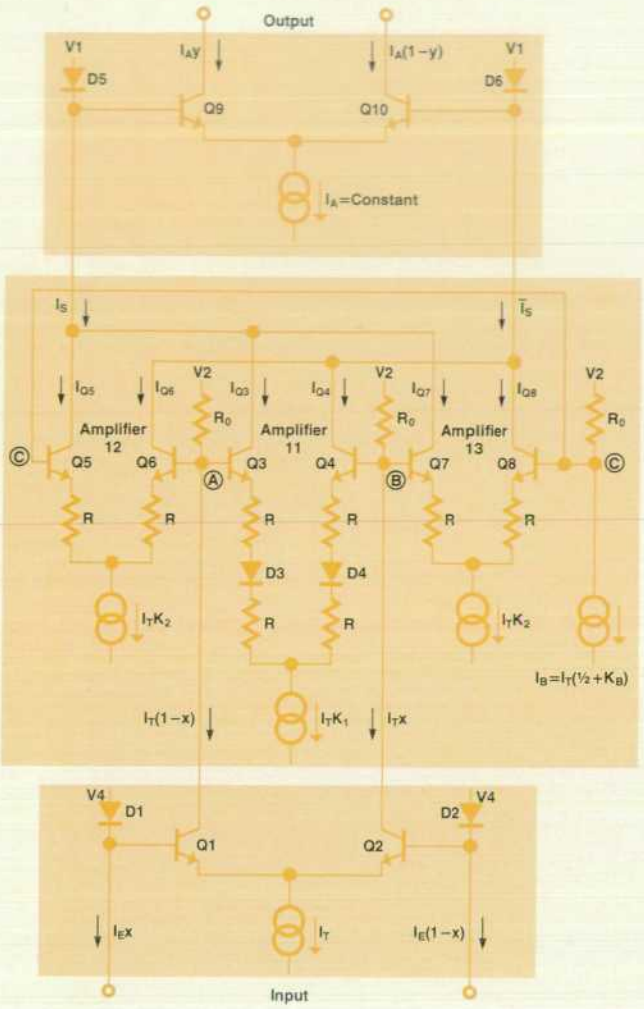

Fig. 11. *The Booster IC's triangle-to-sine converter uses a new technique that offers advantages over conventional methods. See text for details.*

The waveforming stage is followed by an amplitude modulator. An externally generated signal may be used to modulate all waveforms. Overmodulation up to suppressed carrier is possible. The LF input is a current input with a threshold of about 0.47 mA; for input currents less than this, the output signal is unmodulated. The last section of the modulator stage allows normal or complement phase of all waveforms to be selected by means of a TTL/CMOS-compatible digital input.

The next stage is a vernier attenuator controlled by a dc current. Since the voltage of the control input is held at virtual ground by an operational amplifier, a voltage source and a resistor may be used for controlling the attenuation. This stage does not effect the degree of modulation achieved by the modulator. The vernier input has no current threshold, zero current producing maximum gain. Increasing the current decreases the gain down to zero, and thereafter, the gain increases but with opposite phase.

Both modulator and vernier are stages of the same kind, namely Gilbert multipliers. These are four-quadrant multipliers with the big advantage of very good linearity. If the transistors of these stages are well matched, a nonlinearity as low as 0.2% is possible at an attenuation of 1:10.

The output stage is a gain cell with an amplification of 2. The differential outputs are current outputs with open collectors.

New Sine Shaper

One of the main parts of the Booster IC is the triangle-to-sine converter. This shaper uses a new technique which offers advantages over conventional methods.

One well known possibility to convert a triangular voltage into a sinusoid is to use a diode-resistor network or a transistor-resistor network. For a good approximation, however, a number of different sections are required, leading to a complicated network. Also, quite a large voltage swing is needed to drive these circuits.

Another possibility for a sine-shaping circuit is to use the nonlinear transfer characteristic of a transistor differential amplifier. Although this technique generates sinusoids with relatively low harmonic distortion, the waveform has bends at its maxima and minima. The reason for this effect is that the nonlinear transfer characteristic of the differential amplifier has a nonzero slope at its ends, since its slope approaches zero asymptotically.

The sine shaper in the Booster IC also uses the nonlinear transfer characteristics of a differential amplifier. However, two additional differential amplifiers are connected in parallel, their direction and operating points being chosen so that the resulting characteristic has zero slope at the amplitude extremities of the triangular signal.

As shown in Fig. 11, the sine shaper consists of three main parts: the three differential amplifiers which form the

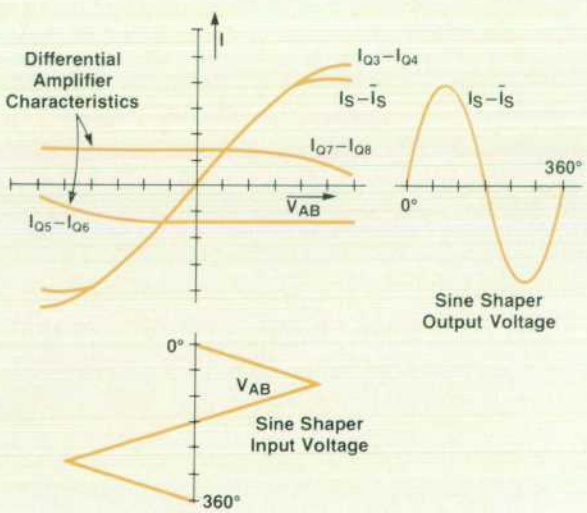

Fig. 12. *Linear superposition of two differential amplifier transfer characteristics results in the triangle-to-sine characteristic of the circuit of Fig. 11.*

shaper itself, an input multiplier, and an output amplifier. The multiplier's input terminals are fed with the current $I_E x$ and $I_E(1-x)$, respectively, where I_E is constant and x is the time-variable fraction of the input current, which is triangular in this case. The purpose of the input multiplier is to convert the temperature-independent input current into a temperature-dependent one and compensate the temperature dependency of the three sine-shaper differential amplifiers. The current source I_T is designed to deliver a current that is the required function of the absolute temperature, so that the output currents of the input multiplier are now $I_T(1-x)$ and $I_T x$, respectively. Thus the voltage drop between nodes A and B in the sine shaper is also a function of the absolute temperature.

Differential amplifier 11 is the main waveform shaper and differential amplifiers 12 and 13 correct the transfer characteristic as already mentioned. Currents I_S and $\bar{I}_S$ have the desired sinusoidal waveforms but are still dependent on temperature. The output amplifier eliminates this temperature dependence and produces the output currents $I_A y$ and $I_A(1-y)$.

Fig. 12 illustrates how the resulting characteristic of the sine shaper is generated. V_{AB} is the triangular input voltage of the sine shaper. $I_{Q3}-I_{Q4}$ indicates the transfer characteristic of differential amplifier 11. Zero slope for the circuit's transfer characteristic can be achieved by linear superposition of the transfer characteristics of differential amplifiers 12 and 13, $I_{Q7}-I_{Q8}$ and $I_{Q5}-I_{Q6}$.

The resulting transfer characteristic of the circuit is $I_S-\bar{I}_S$, also shown as a clean sinusoidal waveform in Fig. 12.

The maximum deviation from an ideal sine wave is ±0.22%. Harmonic distortions are about −60 dB. However, because of process tolerances, the mean value of the harmonic distortion observed in production is about −54 dB with a standard deviation of ±2 dB for a temperature range from 0°C to 55°C. Using the 1-GHz LSI process, the circuit is suitable for frequencies up to 100 MHz.

Acknowledgments

Thanks to many people within HP's Santa Clara Division. We particularly want to thank Santa Clara's mask designers and product engineers for their cooperation, and Jim Grace for many useful discussions.

Authors

June 1983

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Don Morris studied electrical engineering at the University of New Mexico (BSEE degree in 1967) and Oklahoma State University (MSEE degree in 1968 and PhD degree in 1970) before joining HP in 1970. He was project manager for the 9825A Computer (about which he coauthored an earlier HP Journal article), production engineering manager, and later R&D section manager before assuming his current responsibility as product assurance manager. Don has taught digital logic at Oregon State University and math and programming at local vocational education facilities. He has his own twin-engine airplane and flies it whenever he can. He is married, has two sons, and lives in Corvallis, Oregon.

Donald L. Morris

Don L. Morris received a BS degree in mechanical engineering in 1971 from Bradley University and a BS degree in electrical engineering in 1973 from the University of Illinois. After joining HP in 1973, he worked in both production and R&D. He worked on the 82143A Printer and coauthored an article about it in an earlier issue of the HP Journal. Don was the HP-75 production manager before leaving HP recently. A native of Lincoln, Illinois, he lives in Corvallis, Oregon, is married, and has two children.

Anthony S. Ridolfo

Born in Great Falls, Montana, Tony Ridolfo received his mathematics education at Wabash College (BA degree in 1966), Ohio University (MS degree in 1968), and Iowa State University (PhD degree in 1975). After teaching mathematics and computer science for a while as a college professor, he joined HP in 1976 and has programmed firmware for a number of HP's calculators. He was project manager for the HP-75 Computer's operating system before moving to marketing systems engineering. Tony is a member of the American Mathematical Society and the Society for Industrial and Applied Mathematics. He serves on a local math textbook adoption committee and is treasurer for a local Boy Scout troop when he is not busy refereeing youth soccer games, playing bridge or golf, or skiing. He is married, has three children, and lives in Philomath, Oregon.

Brian G. Spreadbury

Brian Spreadbury joined HP in 1976 with several years of experience in aviation system design. He has contributed to the mechanical design of the HP-85 Computer's tape drive (about which he coauthored an earlier HP Journal article), the 82163A Video Interface, and the 82168A Modem. Born in Aldershot, England, Brian studied mechanical engineering at Bournemouth College, England and received the H.N.C.-Mech degree in 1962. He enjoys cross-country skiing, fishing, canoeing, and hiking. Living in Corvallis, Oregon, he is married and has two sons.

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Sidnee Snell joined HP in 1979 after earning a BS degree in electrical engineering at the University of California at Davis. Besides her contributions to the 82168A Modem, she has worked on low-cost plotter hardware and firmware. Sidnee is vice president of the Oregon chapter of the Society of Women Engineers and lives in Corvallis, Oregon. She is married, owns two cats, and enjoys gourmet cooking.

Dennis C. York

Dennis York is a project manager for applications software at HP's Corvallis, Oregon facility. With HP since 1973, he was responsible for application software used in the HP-65, HP-67, and HP-41 Calculators, contributed to the HP-41's firmware, and was HP-IL product manager. Dennis has a BS degree in mechanical engineering awarded by Oregon State University in 1972. He is married, has three children, and lives in Corvallis. He enjoys playing softball and basketball when not checking out new computer programs.

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Born in Laramie, Wyoming, Beth Brooks grew up near Mt. Vernon, Virginia. She received a BA degree in electrical engineering from Rice University in 1975 and joined HP shortly after. While working as an R&D engineer at HP, Beth continued her studies and received an MS degree in electrical engineering from Stanford University in 1977. She was an R&D project manager for the HP-75 Computer, then a product engineering manager, and now is involved with increasing engineering productivity. She is married (her husband is a project manager at HP) and lives in Corvallis, Oregon.

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A native of Roseburg, Oregon, Rex Smith attended Oregon State University, earning a BSEE degree in 1973. He also has an MSEE degree from Stanford University awarded in 1976. Rex has been with HP since 1973 and has contributed to the design of the 4910G Open and Split Locator and the HP-01 Watch. He was project manager for the 82168A Modem and 82163A Video Interface and managed the initial architecture and IC development for the HP-75 Computer. He currently is managing portable data communications development. He served four years in the U.S. Navy (primarily on Orion aircraft) and is involved in church leadership. Married and the father of three children, he lives in Corvallis, Oregon. His interests include classical piano, watching college basketball, vacationing, and family activities.

Robert J. Livengood

With HP since 1969, Bob Livengood has contributed to a number of HP's products—frequency counters, digital multimeters, and portable computers such as the HP-75—in the areas of digital bipolar and MOS ICs. He is a project manager for portable computers at HP's Corvallis, Oregon facility. Bob is a graduate of the University of Missouri (a BSEE degree in 1969) and Colorado State University (an MSEE degree in 1974). He is married, has three sons, and when not involved with youth and church activities, spends his free time landscaping his yard. Born in Brush, Colorado, he now lives in Albany, Oregon.

Timothy F. Myers

Tim Myers joined HP in 1979 after receiving a BSEE degree from Montana State University. He worked on display and memory circuits for the HP-75 Computer with HP Laboratories personnel and now is production engineer for the HP-75 at HP's Corvallis, Oregon facility. He is married and has several interests—photography, holography, golf, softball, skiing, and exploring Oregon's back country. A native of Montana, he now lives in Corvallis.

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Raan Young was born in Pullman, Washington and earned his BSEE degree in 1979 at the University of Washington. He contributed to the HP-75 Computer's operating system and applications software and is an author of a paper on bar-code translation for the HP-41 Handheld Computer. Raan is a member of the IEEE. Living in Corvallis, Oregon, he is married and is interested in electronics, music, photography (including video techniques), and house remodeling.

Kenneth R. Hoecker

A graduate of Oregon State University with a BSME degree awarded in 1972, Ken Hoecker came to HP in 1977 after serving in the U.S. Army for two years and doing postgraduate study in mechanical engineering. He was a production engineer for the HP-01 Watch and joined R&D as part of the original design team for the HP-75 Computer. Born in Astoria, Oregon, Ken spent eight yearts of his childhood in Brazil. He is married, lives in Corvallis, Oregon, and enjoys basketball, water skiing, camping, foreign travel, and bridge playing.

Dean R. Johnson

Before joining HP in 1979, Dean Johnson did digital design of microprocessor-based products. At HP, he is concerned with implementing analog systems in CMOS technology. Raised in the Midwest, Dean attended the University of Minnesota where he earned a BEE degree in 1973 and an MSEE degree in 1979. He is a member of the IEEE and active in his community's Big Brother program. Living in Corvallis, Oregon, he enjoys mountain climbing, hiking, and playing racquetball.

James R. Schwartz

Jim Schwartz started at HP in 1971 after completing the requirements for a BSEE degree at San Jose State University. He left HP in 1973 and rejoined the company in 1977. He now is an R&D engineer for HP's Corvallis, Oregon facility. Raised in Chico, California, he lives in Corvallis with his wife and two soms. Until he was idled by an injury, his outside interests included tennis and fast-pitch softball.

David B. Patton

Dave Patton contributed to the design of several production tools for the HP-75, including the production card recorder, before assuming his current R&D position working on portable printers. He graduated from Purdue University in 1978 with a BS degree in electrical engineering technology and worked for Purdue's aerospace sciences laboratory before joining HP in 1980. Married, he lives in Corvallis, Oregon, and is interested in church activities, music, gardening, motorcycles, bicycling, and skiing.

Thomas J. Arnold

Born in Manitowoc, Wisconsin, Tom Arnold attended the University of Wisconsin at Madison where he received a BS degree in electrical engineering. He came to HP in 1979 as a product engineer and now is an R&D project manager. Tom is the author of a paper on CMOS latch-up and lives in Corvallis, Oregon. He is interested in home computers and motorcycles and enjoys downhill skiing and camping.

Billy E. Thayer

Bill Thayer began work at HP in 1964 after serving in the U.S. Air Force for ten years. He worked on some of HP's first transistorized instruments and the printed circuit boards in HP's first desktop calculator, the 9100A. Bill helped design the NMOS chip set used in the 9825A Computer before moving to HP's Corvallis, Oregon facility to design CMOS ICs. He designed parts of the keyboard/clock and card-reader chips for the HP-75 Computer. Born in Rushville, Nebraska, he now lives in Corvallis. He is an elder in the Presbyterian church, married, and has three sons. He enjoys water and downhill skiing and camping in the Oregon outdoors.

Michael Fleischer

A native of Essen, Michael Fleischer joined HP in Boeblingen in 1980 shortly after receiving his Engineering Diploma from the Ruhr University in Bochum. After working on several hardware problems, he joined the 8112A team and was responsible for completing the timing and slope sections and the output amplifier. Michael is lecturing in electronics at a Stuttgart college. He is single and likes to spend his spare time backpacking, traveling in his camper, and playing the guitar.

Helmut Rossner

Shortly after receiving his electronics engineering degree in 1969 at the Engineering School in Esslingen, Helmut Rossner joined the HP pulse generator design team at Boeblingen. His first projects were the 8012A and 8013A Pulse Generators. Later, he codesigned various programmable data generators and precision pulse generators. In the new series of pulse generators and pulse/function generators, he was project leader for the 8112A. Helmut is married and has two daughters. He is keen on all kinds of touring, whether by bicycle, on skis, or on foot, but most of all he is an enthusiastic mountaineer and is a member of the German Alpine Club.

Uwe Newmann

Uwe Neumann earned his Diplom Ingenieur (FH) at the Engineering School in Constance in 1978 and joined HP GmbH as an R&D engineer the same year. He worked on the 8161A's software and was later responsible for the software development of the 8112A Pulse Generator and 8116A Pulse/Function Generator. Uwe is married, has a daughter, and enjoys walking, traveling and cross-country skiing.

Christian Hentschel

Before joining HP in 1972, Christian Hentschel was involved at the Institute of Theoretical Electrotechnology, Aachen University, in research on thin-film, high-frequency lumped circuit elements, a topic of his doctoral dissertation. At HP's Boeblingen Instruments Division, he worked on the 8082A 250-MHz Pulse Generator, was project leader for the 8080A configurable 1-GHz/300-MHz Pulse/Data Generator, and subsequently became technology section manager. Christian is married and enjoys photography, tennis, sailing, windsurfing, and other sports.

Stefan Traub

Stefan Traub joined HP in 1969 with previous experience in R&D. He worked as a hardware development engineer on a variety of projects, including medical instrumentation and oscilloscopes. He was project leader for the 15239A Display Unit for medical monitoring and the 1222A Oscilloscope. He contributed to the design of the Snake IC and the Booster IC and was project leader for the Rate IC until 1979. His work has resulted in seven patents. Stefan is married and lives in Boeblingen. He has two sons, plays tennis and enjoys outdoor activities.

Adolf Leiter

Before joining HP, Adolf Leiter studied electrical engineering in Munich. He joined HP's Boeblingen Instruments Division in 1979 as an R&D engineer and took over the responsibility for the Rate IC design from Stefan Traub. He is presently working at HP Laboratories in California. Adolf is single and is living in Cupertino, California at the moment. He enjoys tennis and skiing and outdoor activities in general.

Horst Schweikardt

After finishing his electrotechnical studies at the University of Stuttgart, Horst Schweikardt joined HP GmbH in 1972. He was involved in the development of low-cost oscilloscopes, was project leader for the 1223A Storage Oscilloscope and 214B Pulse Generator, and then joined the IC team where he worked on the Rate and Snake designs. Horst is married, has a one-year-old daughter and enjoys bowling, photography, and mountain hiking.

Volker Eberle

Volker Eberle earned his Diplom Ingeniuer at the Technische Universität, Stuttgart in 1975. He then joined HP, starting on the 8092A Delay Generator, a module of the 8080A Configurable Pulse/Data Generator. During the final phase of the 8080A development, he became project leader, guiding the system into production. He then moved on to the Booster IC as project leader. Volker is married and has two daughters. His leisure activities are gardening, model railroading, and playing the accordion.

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