

A transition is now underway in the wireless communications industry, as wireless service providers embrace broadband communication standards such as LTE-Advanced and IEEE 802.11ac. In order to achieve Gb/s link-level throughput, these new formats use wider bandwidths, multiple-input multiple-output (MIMO) space-time coding, and higher order orthogonal frequency division multiplexing (OFDM) modulation formats. These requirements place new demands on linearity, bandwidth and power consumption in wireless components. For example, LTE-Advanced supports up to 100-MHz bandwidth to reach 1Gb/s and 500 Mb/s data rates for the downlink and uplink, respectively, IEEE 802,11ac will support 80-MHz and 160-MHz

bandwidths to achieve throughputs of at least 1 Gb/s for multi-station and 500 Mb/s maximum for a single link.

For the communications system architect and the RF power amplifier (PA) designer, these new formats introduce a number of challenges. Designers must determine the performance gap between their existing 3G designs and tomorrow's 4G operating environments, and whether these 3G designs will need to be redesigned, or a new vendor qualified. The hardware must also meet or exceed absolute performance metrics such as ACPR, EVM or throughput (e.g., BLER, BER and PER), while also meeting internal product design goals.

Because smart phones and other advanced wireless devices rely so heavily on battery power, getting the most efficiency out of a design is critical. The RF PA plays a particularly key role Choosing and designing the right PA to meet design goals is a significant challenge.

This application note outlines a broadband modeling approach that

- quickly characterizes broadband RF PA's,
- assesses "how linearizable" transceiver designs are, requiring typical wireless engineering skill sets and equipment; and
- helps estimate real-world 4G performance, prior to committing to intellectual property (IP), hardware or implementation details.



Problem

Power amplifiers are an essential component in the overall performance and throughput of wireless communications systems, and are inherently nonlinear. That nonlinearity generates spectral re-growth, which leads to adjacent channel interference and violations of the out-of-band emissions standards mandated by regulatory bodies. It also causes in-band distortion, which degrades the biterror-rate (BER) and data throughput of the communications system.



Figure 1. Multi-band integration in the digital baseband, with a single analog upconversion/transmit path.



Figure 2. Multi-band integration at the analog intermediate frequency (IF), with a common upconversion and RF PA.



Figure 3. Multi-band integration after upconversion, at the RF carrier, with a common RF PA.



Figure 4. Multi-band integration of multiple RF PA's, with further topologies possible to support MIMO, beamforming and operational redundancy.

Figures 1-4 illustrate various transmit architecture options, according to where the component carriers are combined, (e.g., at the digital baseband, in analog waveforms before the RF mixer, after the mixer but before the PA, or after the PA). While integrated RFIC SoCs, CMOS chipsets and base station architectures each achieve their design goals in different ways, Figures 1-4 show that they share a common challenge—the most common challenge for RF engineers—the broadband PA design.

The next challenge is the trade-off between the peak-to-average power ratio (PAPR, or crest factor) and power-added-efficiency (PAE). The newer OFDM transmission formats. The newer OFDM transmission formats, such as 3GPP LTE, LTE-Advanced, and 802.11ac, OFDM (e.g., such as 3GPP LTE and LTE-Advanced, 802.11ac), have high peak to average power. Infrequent intervals of higher peak power levels cause the PAs to clip harder and degrade the spectral mask compliance, EVM and BER for the entire waveform. Operating the PA at a lower power is one way to reduce this nonlinearity.

However, this means that the PA needs to be backed off well below its long-term saturated power level. In other words, for a large percentage of the time, the PA is operating with wasted capacity. This results in very low efficiencies, typically less than 10% (more than 90% of the DC power is lost and turns into heat). For a base station, this reduces the service area and increases both the capital and operating expenses of the service provider. For a mobile handset, this also reduces the quality of service (QoS) and battery life, leading to customer dissatisfaction and lower revenues. Linearization enables the PA to be operated in its high PAE region, near saturation and without significant signal distortion, thus reducing expenses.

Digital pre-distortion (DPD) is a cost-effective way to accomplish linearization. Today, turn-key, commercial off-the-shelf (COTS) chipsets and IP are available for 2G/3G formats to service this need. However, in many cases, these commercial DPD approaches fall short of the 4G requirements. Below is a summary of these and other challenges facing today's physical layer communications designers, with regard to DPD.

Commercial IP, Algorithms and Chipsets Challenges

- 4G Ready. May not yet support the bandwidth, dynamic range and performance needed for 4G.
- Closed IP. They do not allow internal algorithmic access, to enable proprietary studies and customization of Crest Factor Reduction (CFR), oversampling, filtering, DPD coefficient extraction and convergence, polynomial depth, memory effects, and other factors.
- Parts count. Add to the final Bill-of-Materials (BOM) and parts count. Would like to adds absorb DPD into existing baseband DSP without introducing external parts or cost.

Modeling Hardware Challenges

- **Bandwidth.** Existing test equipment platforms may not physically support the required hardware bandwidth of LTE-Advanced with carrier aggregation, or of 802.11ac, with the oversampling required for DPD.
- Not extendable. Ad hoc solutions with third-party demo boards may be uncalibrated, not repeatable, or not connected to an enterprise hardware design flow. They may also be difficult to automate.
- **Evolving Standards**. Need re-configurable, standardscompliant test vectors for emerging standards, but the standards are still evolving and may not be available in existing equipment. Or, personal algorithms for signal generation and measurement are not appropriate for working with external partners.

Modeling Team Challenges

- Platform. A team of highperformance Ph.D. modelers spends time writing simple code and "glue" in order to integrate general-purpose toolsets. They would like to use a better stimulus/response modeling platform to contribute higher engineering value.
- Skill-level. High skill level required for modeling and interpretation.
- Transportable IP. How to easily demonstrate a solution outside the lab environment to partners? How to remain vendor neutral? How to collaborate worldwide, with remote access to shared test equipment, device samples and use common toolsets, interoperability, and licenses?
- Current DPD methodologies are not predictive. Would like to virtualize the entire DPD/PA modeling process by connecting directly to RF EDA flows, for concurrent RF and baseband design.

Engineers migrating to 4G require a solution that makes implementing DPD fast and practical for 4G communications systems-one that can be used by engineers at all levels of expertise and requires minimal equipment. The tool set should be accurate, avoid dependence on a vendor-specific chipset or hardware implementation for the initial modeling, and able to absorb custom DPD into the rest of the baseband processing, preserving a lower BoM. Moreover, it must support connectivity with a range of other tools for hardware verification.

One solution that meets this criterion is Agilent Technologies' SystemVue platform with its add-on DPD personality—the W1716 DPD Builder. This utility features an easy, wizard-based user interface that helps users quickly model and correct common sources of 4G memory effects in both low and high-power PA's, as well as transceiver IC's, and even automatic gain control modules.

The W1716 DPD is aimed at early R&D architecture and component studies by wireless system architects using common, off-the-shelf test equipment already in a test lab. Whereas proprietary DPD solutions force a number of premature implementation decisions simply to perform a 4G feasibility study, by using the W1716 DPD, wireless architects can assess in minutes how "linearizable" a component will be. while still retaining ultimate hardware flexibility and full 4G measurement confidence. Agilent enables this thanks to several key advantages: the power and ease of the Agilent DPD algorithms; the open, vendor-neutral and technology-neutral approach taken to the DPD and PA hardware; the high performance and flexibility of the Agilent instruments; and the realistic, standards-compliant waveforms (such as LTE and LTE-Advanced with CFR) that are used for the characterizations.

CFR supplements and improves the effectiveness of DPD. In modern communication systems, spectrally efficient wideband RF signals have a peak-to-average power ratio (PAPR) as high as 13 dB. CFR preconditions the signal to reduce signal peaks without significant signal distortion. By reducing PAPR, CFR allows the PA to operate more efficiently at higher power levels, without impacting compliance with spectral mask and EVM specifications. CFR acts on the signal itself, whereas DPD corrects for the PA nonlinearity, allowing the signal to be run even higher.

Agilent PXI Modular Instruments for DPD

Unlike other approaches to DPD, Agilent's approach takes a designer's perspective by featuring flexible, builtin modeling and links to wideband, reconfigurable instruments, such as Agilent's Modular PXI family (Figure 5).



Figure 5. In this setup, the AWG with SystemVue for LTE-A and 802.11ac provides the standardbased signals required for component test, while the M9392A (running Agilent's vector signal analysis (VSA) software) captures the signal in order to measure the PA's nonlinearities. Using SystemVue with the M9330A andM9392A automates and controls the entire DPD design flow.

The M9392A PXI vector signal analyzer provides analysis bandwidths of up to 250 MHz in a frequency range from 2.25 GHz to 26.5 GHz, with full 89600B VSA software support. At the core of the M9392A vector signal analyzer is the M9202A wideband IF digitizer, with a 2 GSa/s sample rate and 12-bit resolution. With better than -65 dBc SFDR, the M9202A allows for up to 800-MHz bandwidth acquisitions. It also has full 89600B VSA software support, enabling configurations that support a wider bandwidth than the 250 MHz offered by the M9392A. The M9362AD01 4-channel 26.5-GHz downconverter module provides wider bandwidth analysis capability, up to 1.5 GHz.

The M9330A PXI AWG provides two synchronized outputs at 15-bit resolution. With a 1.25 GSa/s sample rate, the M9330A can be used to generate IQ signals to apply to an external IQ modulator such as the MXG or PXG signal generators with up to 1 GHz bandwidth. It can also be used to generate an IF waveform with up to 500 MHz bandwidth.

Figure 6 shows the architecture for the digital pre-distorter of memory polynomial. The first step is to understand the physical mechanisms behind the PA's behavior and extract DPD coefficients. The second step involves constructing a pre-distorter model to accurately capture both the static nonlinearity and the memory effects based on the first step. The feedback path labeled "Predistorter Training" (block A) has (n)/G as its input, where G is the intended PA small signal gain, and $z^{\gamma}(n)$ as its output. The actual pre-distorter is an exact copy of the feedback path (copy of A); it has x(n) as its input and z(n)as its output. Ideally, we would like (n) = Gx(n), which renders $z(n) = z^{n}(n)$ and the error term e(n) = 0. Given v(n) and z(n), this structure enables us to find the parameters of block A directly, which yields the pre-distorter. The algorithm converges when the error energy $||e(n)||^2$ is minimized.



Figure 6. The architecture for the digital pre-distorter.

Using the SystemVue W1716 DPD utility to characterize real PA hardware is a straightforward process that takes mere minutes, using the setup and measurement steps shown below (Figure 7). Note that the same procedure can also be used for simulation-based DPD extraction (not discussed in this application note).

Steps in the DPD modeling flow:

- 1. The DPD stimulus waveform (such as LTE-Advanced, 802.11ac or customized waveform) is calculated and downloaded into the M9330A AWG via the W1716 DPD wizard. The baseband AWG outputs I and Q analog voltages to drive the baseband inputs of the Agilent N5182 MXG source. The MXG then outputs a modulated RF waveform as the stimulus to the PA, with any flatness and calibrations applied. Note that for a large base station PA, an external preamp may be needed to drive the PA to approximately its 1-dB compression point.
- 2. Both the raw input signal and the PA's amplified response are captured using the M9392A vector signal analyzer, and brought back into SystemVue via the connectivity provided by the 89600 VSA software. Note that the PA output signal may need to be attenuated externally before entering the M9392A to avoid damaging or overloading the analyzer, or degrading its calibrated performance.
- 3. The W1716 DPD Builder time-aligns and compares the captured output waveform versus the linearly-scaled input waveform, to get an EVM history that is characteristic of the DUT. Based on this difference, the DPD model is extracted, and then verified in simulation. At this point, you also have a "dirty PA" model that can be used after your measurement hardware is disconnected.

- To verify in hardware, the original stimulus is now pre-distorted and downloaded a second time to the signal generator, to re-test the PA. The linearized DPD+PA response is captured using the same physical connection as Step 2.
- 5. The linearized DPD+PA response is now analyzed and plotted.



Figure 7. Flowchart of DPD hardware verification.

This 5-step measurement-based DPD modeling flow was used for a commercial PA, as shown in Figure 8. The laptop running SystemVue (Figure 8, top) controls the Agilent PXI Modular hardware (Figure 8, bottom), as was shown schematically in Figure 5, with the M9330A AWG being integrated physically into the same chassis with the M9392A. The external N5182 MXG RF source (Figure 8, middle) essentially upconverts the baseband signal from M9330A AWG into a modulated carrier.



Figure 8. Agilent PXI modular AWG and vector signal analyzer, with SystemVue W1716 DPD.

The result of using SystemVue DPD is shown in Figures 9 and 10. Figure 9 is the IEEE 802.11ac (80 MHz bandwidth) spectrum of a wireless PA output, with and without DPD. Note the use of oversampling for an actual measurement bandwidth that is wider than the original signal. Without this additional bandwidth to quantify the out-of-band energy (distortion products), it is not possible to correct for this spectral regrowth later.



Figure 9. DPD performance of IEEE 802.11ac (80 MHz). The PA input is displayed in green, the distorted PA output without DPD is displayed in blue, and the linearized DPD+PA output is shown in red.

Figure 10 shows an LTE-Advanced signal with 4x20 MHz carrier aggregation (80 MHz total signal bandwidth). The PA output spectrum is shown with and without DPD.



Figure 10. DPD performance of LTE-A with 4x20 contiguous carrier aggregation. The PA input is displayed in green, the distorted PA output without DPD is displayed in blue, and the linearized DPD+PA output is shown in red.

The Agilent SystemVue W1716 DPD provides the memory polynomial algorithm as a C++ dataflow model and the memoryless polynomial algorithm as a .m code (MATLAB format), which is visible to licensed users. Users can also take advantage of the SystemVue platform as a modeling tool and integrate their own digital pre-distortion algorithmic IP into the W1716 DPD wizard. As of SystemVue 2011.10, the W1716 DPD Builder graphical user interface (GUI) supports two families of Agilent instruments, as well as simulationbased extraction. This application note discusses integration with the Agilent PXI Modular series of instruments, as shown in the following section.

Support for the ESG/MXG family of sources and MXA/PXA family of signal analyzers is discussed in Application Notes http:// cp.literature.agilent.com/litweb/ pdf/5990-6534EN.pdf and http:// www.agilent.com/litweb/pdf/5990-7818EN.pdf. Simulation-based DPD based on co-simulation with Agilent Advanced Design System, Agilent GoldenGate, and X-parameter* devices is possible, but beyond the scope of this document.

Step 1: Create DPD Stimulus

The first step is to download a baseband waveform into the M9330A as DPD stimulus. The M9330A is an AWG and needs MXG as an external modulator. The values of FCarrier and RFPower in the GUI should be set manually in the MXG.

ate DPD Stimulus	2: Capture DUT Response	3: DUT Model Extracti	on 4: DPD Respons	e 5: Verify DPD Res	ponse
Current Iteration	1				
FCarrier	2.0e9 Hz 🗸		SamplingRate	34.66667e6	Hz 🐱
CFREnable		BandWidth	270.8333 KHz	 OverSampling 	Ratio 128
Clipping Paramete	rs				
ClippingThreshol	d 1		Maximum Order	300	
Pass Frequency	4.5e6	Hz 🗸	Pass Ripple	0.1	dB
Stop Frequency	5e6	Hz 🗸	Stop Ripple	50	dB
File Type	I/Q File	1			
IBranchBrowse	Jer\GSM_6Carriers_600	0K_new_I.txt	QBranchBrowse	er\GSM_6Carriers_600K	_new_Q.txt
Select Instrumen	t M9331A	~			
Oownload Parame	ter				
RFPower -7	dBm 🔽 Out	out Mode Single Ended	i 🔽 Instrument Ac	Idress PXI18::15::0::II	NSTR
TimeStart 0	ms v RFPowe	r should be set on MXG/E	SG manually TimeSto	p 40	ms 🗸
Customized Wa	veform	MXG			
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Con .			CCDF	PAPR 9.6	7580961687
SystemVue					

Figure 11. The graphical UI of step 1.

Step 2: Capture DUT Response

In this step, the PA input and output is captured from the M9392A using VSA software.



Figure 12. The GUI of step 2.

Step 3: Capture DUT Response

The next step, the most critical, is to extract the DPD coefficients for the memory polynomial and memoryless polynomial using the PA input and output waveform. Figure 13 shows the GUI by using the default memory polynomial algorithm.

1				🗐 🗆 🔀
1: Create DPD Stimulus	2: Capture DUT Response	3: DUT Model Extraction	4: DPD Response	5: Verify DPD Response
Ourrent Iteration	4			
NumOfEnputSamples	40000	Model Type	0: Memory Polynom	ntal 👻
MemoryOrder	4 Model	Identification Algorithm	0: LSE using QR	
NonlinearOrder	9			
<i>y</i> (<i>n</i>)		Use	Custom Model Extracto	orUse Custom Pre-Distorter
21	$\sum_{i=1}^{n} a_i \varphi(n) p(n) ^{-4}$	z(n)	tomized Model Extracto	Customized Pre-Distorter
21	a,pr(n-1)[r(n-1)] ⁻⁴		DPD Model Extraction	Show DPO Coefficients
how Results	$p(n-Q) r(n-Q) ^{-4}$			
Normalize				
PA AM-	AM DPD A	N-AM	A AM-PM	CPD AM-PM
Spectru	m Power Al	gnment 0.3706842751	46413 NMS	£ -45.2116900191479 dB

Figure 13. The GUI of step 3.

Figure 14 shows the GUI by using the MATLAB code of the memoryless polynomial algorithm when "Use Custom Model Extractor" and "Use Custom Pre-Distorter" are enabled.



Figure 14. The SystemVue DPD wizard (release 2011.10 and later) allows custom IP to be inserted for both the model extraction, and the actual pre-distorter.

After clicking the "Customized Model Extractor" item, the MATLAB code of the memoryless polynomial algorithm used to extract the coefficients of the predistorter is opened in the MathLang block (Figure 12). Customers can insert their own DPD algorithm's MATLAB code into this MathLang block to replace the Agilent memoryless polynomial algorithm.



Figure 15. Custom code for the model extractor can be inserted here. A simple memoryless polynomial nonlinearity is shown above, in MATLAB .m format.

To extract the coefficients for the digital pre-distorter, the digital pre-distorter structure should be changed to correspond to the change algorithm. After clicking the "Customized Pre-Distorter" item, the MATLAB code of the memoryless polynomial pre-distorter is shown in the MathLang block (Figure 16). Customers should insert their MATLAB code to match their own digital pre-distortion algorithm.

'DPD_PreDistort	er 1' Properties 🔀
Designator:	DPD_PreDistorter1
Desgription:	Math Language Block
Model:	MathLang@Data Flow Models
📔 Manage	Aodels Use Model 🛶
Equations I/O	Custom Parameters
4 5 6 7	<pre>DPD_Input_Q = imag(DPD_Input); DPD_Coef_I = real(DPD_Coef); DPD_Coef_Q = imag(DPD_Coef); setmatlabvariables('DPD_Input_I','DPD_Input_Q','DPD_Coef_I','DPD_Coef_(fmatlabvariables)</pre>
	N = NumOfInputSamples; n = NonlinearOrder;
13	<pre>y = DPD_Input_I + j * DPD_Input_Q; p = DPD_Coef_I + j * DPD_Coef_Q;</pre>
	R=zeros(N,n);
Advanc	d Options

Figure 16. MATLAB pre-distorter code, native within the SystemVue environment. Step-by-step debugging is provided within SystemVue, as well as optional direct invocation of the user's full MATLAB configuration.

Step 4: DPD Response

This fourth step is to generate a pre-distorted waveform using the memory polynomial coefficients extracted in step 3. The value of \mathbf{RF}_{Power} for the pre-distorted waveform in GUI should be set to MXG manually.



Figure 17. The GUI of step 4.

Step 5: Verify DPD Response

The fifth step is to verify DPD performances by comparing the spectrums of PA output with DPD and without DPD.



Figure 18. The GUI of step 5

	Required	Optional
Software	 W1461BP SystemVue W1716EP DPD Builder 89601B VSA, options 105, 200, 300 Agilent I/O Libraries, v16.0 or later 	 W1918EP LTE-Advanced library W1917EP WLAN library (w/802.11ac) VSA demodulation options" BHD (LTE FDD), BHE (LTE TDD), BHF (OFDM), BHG (LTE-A FDD), BHH (LTE-A TDD), BHJ (802.11ac)
Hardware Source	 Broadband signals > 60 MHz M9330A AWG, with option M16** (also requires M9018A PXI chassis) and N5182 MXG signal generator with the following helpful options: 506 (6 GHz range) 1EA (higher output power) UNV (extended dynamic range) 	Ultra Wideband signals > 1GHz • 81180A AWG, with options - 116 (1 chan., 4GSa/s, 16MSa depth) • or M8190A AWG (also requires M9502A AXIe chassis) • and E8267D PSG signal gen., w/options - 016 (wideband differential IQ inputs) - 520 (20 GHz range) - H18 (Modulation BW < 3.2 GHz)
Hardware Analyzer	 250 MHz Configuration M9018A PXI Chassis M9392A analyzer bundle, includes: M9302A 3-10 GHz local oscillator M9361A Downconverter M9360A Attenuator/Preselector M9202A IF Digitizer 	 Optional 800 MHz Configuration M9018A PXI Chassis M9202A IF Digitizer M9302A 3-10 GHz local oscillator M9362AD01 0.05-26.5 GHz Downconverter
Other integration pieces	 DC bias supply, and cables 10 MHz clock reference cable I, Q baseband cables RF DUT 2.5 mm coaxial cables LAN and PXIe cables 	 RF preamp (for PA input) RF attenuator (for PA output)

** for narrower bandwidth signals less than 60 MHz wide, the N5182A MXG signal generator provides internal baseband generation with options 654 (internal AWG) and 019 (deeper BB memory). An external M9330A would not be necessary for 2G/3G applications.

Summary

As engineers migrate to advanced wireless communication systems such as LTE-Advanced or 802.11ac, choosing and designing the right PA to meet design goals at the lowest possible cost becomes more difficult, both for base stations and mobile devices. Because DPD enables the PA to be operated with high efficiency, near saturation and without significant signal distortion, it allows engineers to address many base station/ mobile device PA design challenges. SystemVue with the W1716 DPD

option provides the algorithmic sophistication to work with 4G signals and formats, and interoperate with other trusted personalities like Agilent's 89600 VSA software. Agilent's PXI Modular instruments, such as the M9330A AWG and M9392A vector signal analyzer provide a calibrated, broadband measurement platform that's capable of DPD modeling up to 250 MHz today, and can accommodate future expansion to meet changing requirements.

A video demonstration of this configuration is available at http://www.youtube.com/watch?v=bocF6P74T9E

For more information about SystemVue, please visit us on the web:

SW Product information http://www.agilent.com/find/eesof-systemvue

HW Product information

http://www.agilent.com/find/modular

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