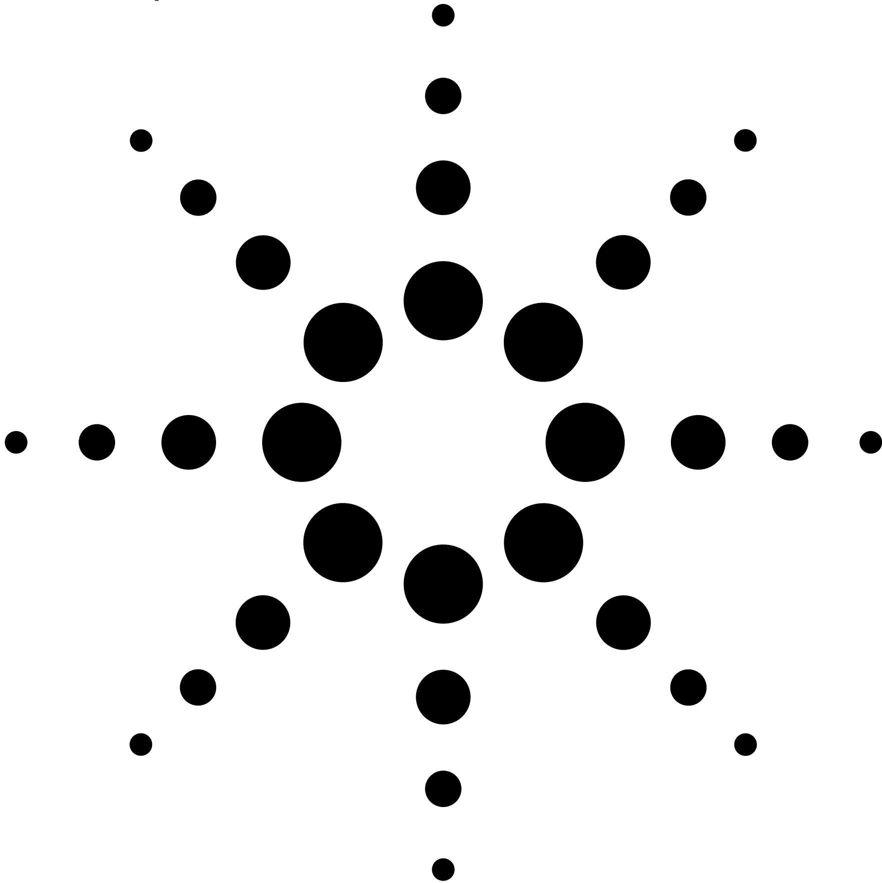
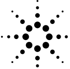
Backplane Differential Channel Microprobe Characterization in Time and Frequency Domains

White Paper





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Abstract

The chief difficulty with routine characterization of differential channel paths is the current requirement for SMA connectors to interface with the test equipment. With little extra space available on functional backplanes, and the problem of line loading produced by the SMA stubs, it is not practical to use SMA connectors. This means only specially designed test boards can be routinely characterized. This paper introduces a new methodology for testing the passive interconnects associated with a differential channel in a backplane assembly, which can be used for functional, populated backplane assemblies and shows how the pad layout can be optimized for routine probing without impacting the functional system performance.

Differential Channels Will Proliferate

We are in the beginning of a revolution in input/output formats. All high-speed interface specs are migrating toward the use of differential signals implemented with a differential pair of transmission lines. Figure 1 is a partial list of some of these high-speed serial link formats.

All Next Generation High Speed Serial Links will use Differential Signaling

Format	Rate	Format	Rate
Serial ATA	1.25 Gbps	XZUI	3.125 Gbps
Hypertransport	1.6 Gbps	PCI Express II	5.0 Gbps
AGP8x	2.1 Gbps	OC-192	9.953 Gbps
Infiniband	2.5 Gbps	10 GbE	10 Gbps
PCI Express	2.5 Gbps	OC-768	39.81 Gbps
Serial ATA II	2.5 Gbps		

Figure 1. Partial list of many new high speed serial link formats

In addition to being differential signals, they are all in excess of 1 Gbps. This translates to an analog bandwidth of at least 2 GHz. In the case of XAUI, this is in excess of a 5 GHz analog bandwidth. In order to verify the performance and the quality of models for use in system level simulation, measurements on the differential channel properties must be at least twice the application bandwidth, or up to a 10 GHz measurement bandwidth.

Characterizing a differential channel can be accomplished in two ways, either by building an equivalent circuit model based on a topology of ideal circuit elements that all simulators can understand, or with a physical layer characterization based on performance metrics. The model extracted from physical layer characterization is usually called a behavioral model, as it uses the direct measurements as the model itself. A behavioral model is often called a “black box” model because it cannot be determined what specific structures are inside.

A topology based model can be used in any simulator and provides useful design insight on what physical features influence which electrical features. It requires more work to construct and the effort usually increases exponentially with increasing bandwidth and complexity. Creating a model for a simple structure such as a balanced transmission line (microstrip or stripline) can be difficult at high speeds. Creating a topological model for a large backplane with multiple channels is daunting even for a team of experts.

The alternative characterization approach is to use the direct measurements as the characterization. This behavioral model can then be used directly in a system level simulation. Careful manipulation of the direct measurements can present the information in a format from which useful performance information can be directly extracted.

In this latter approach, there are a few metrics that describe the performance of the differential channel. They are:

- The insertion loss (quality of the transmitted differential signal)
- The return loss (the differential impedance profile)
- The conversion of differential to common signal
- The location in the interconnect where most of this conversion occurs
- The common impedance profile
- The cross talk between differential channels
- The eye diagram for a specific bit rate.

Each of the above figures-of-merit can be obtained with the Agilent Physical Layer Test System (PLTS) software using a 4-port measurement system, whether it is a 4-port vector network analyzer (VNA) or 4-channel time domain reflectometer (TDR). In theory, the measurements are simple. In practice, they are difficult and constrained by multiple factors such as the following: introduction of excess inductance of probe tips, excess capacitance of test fixture pads, instrument set-up, calibration, and deskewing of differential pairs. There are a myriad of other subtle process steps that can lead to poor results. The key step in using direct measurements for physical layer characterization is to minimize the artifacts introduced by the fixturing used to interface the test equipment with the differential channel under test. An example of a complete 4-port VNA-based measurement system is shown in Figure 2.

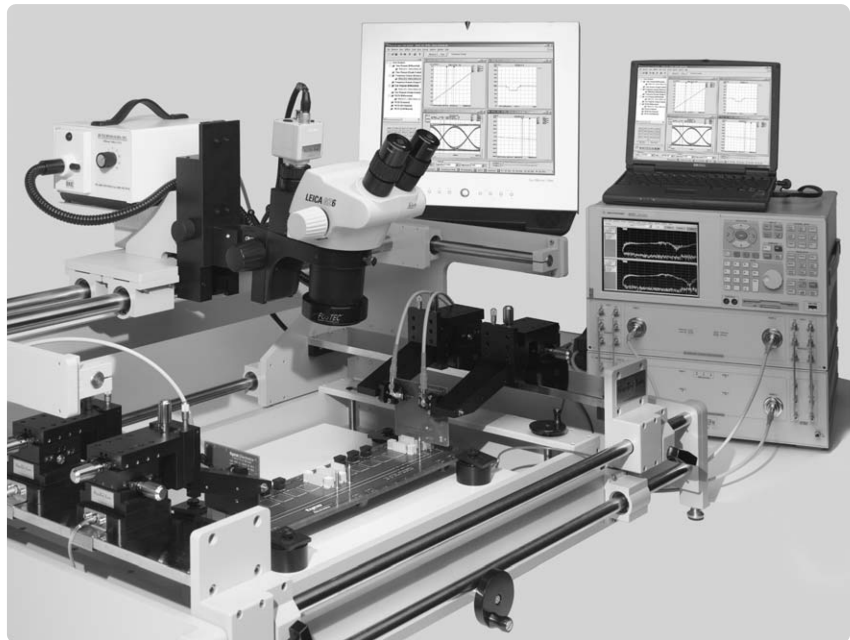

Figure 2. Complete four-port characterization system

The Bottle Neck of SMA’s

The most common technique of interfacing a backplane, for example, to a VNA is by designing the board for SMA connectors. An example of a test board instrumented with SMA’s is shown in Figure 3.

Typical SMA Fictured Test Board

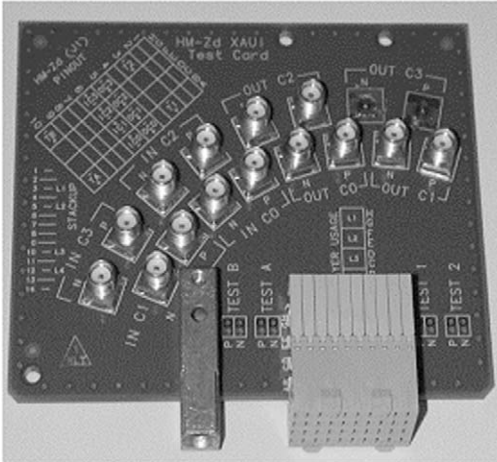

Figure 3. SMA connectors used to interface VNA to test board

The advantage of SMA’s is that they are easy to attach a precision 50 Ohm coax cable to and once attached, are robust. While SMA’s work, they have three significant drawbacks.

Though the bandwidth of an SMA connector itself maybe in excess of 10 GHz, the artifacts it introduces in the test board can often be seen at much lower frequency. This is usually due to the vias required in the board to plug in the SMA. If this structure is not optimized, the SMA can introduce either an inductive or capacitive artifact.

The SMA is physically large in size and with cable attached, there is a limit to how closely spaced they can be mounted to a board. The limit is roughly on a 0.75 inch pitch. This is a density of about 1.8 connections per square inch.

An SMA, in the best case, looks like a 50 Ohm stub about 0.5 inches long. When this is in series with the test line, it may be transparent to the signal. However, if it is placed on an active line, with a driver, it will load the line down and at Gbps rates, may cause the performance to degrade.

For these reasons, SMA's are typically used with special, custom characterization boards, rather than on the actual product. This is an expensive path and may not give an indication of the performance of the final product boards.

Advantages of Microprobing

Microprobes typically use precision 50 ohm micro coax cables with very small tips. They come in the form of coplanar or needle tips. Using a custom calibration substrate, they can be calibrated right down to the tip. The typical parasitics can be less than 100 pH and 100 fF. An example of a close up of a microprobe in contact with a test pad is shown in Figure 4.

Typical Microprobe Closeup

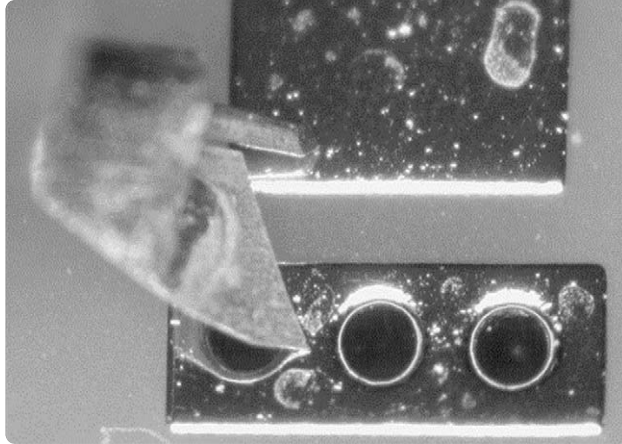

Figure 4. Typical signal-ground microprobe with 450 micron pitch

When the board is designed for microprobing, this approach eliminates the problems with SMA connections and can dramatically increase the value of characterization measurements.

The key to getting the most value from microprobes is to design the board with return paths adjacent to all signal paths. When there is an adjacent return connection to the signal line, the physical probe can be very small and its parasitics very low. This is true whether the probe is a 50 ohm controlled impedance probe or a high impedance active probe.

Design for Test

As more designs enter the gigahertz realm, designers should think about testability before the design is finished. All it takes to dramatically improve the high frequency testability of a board is to add a grounded copper fill in the vicinity of the signal vias. This is illustrated in Figure 5.

Design for Test (DFT)

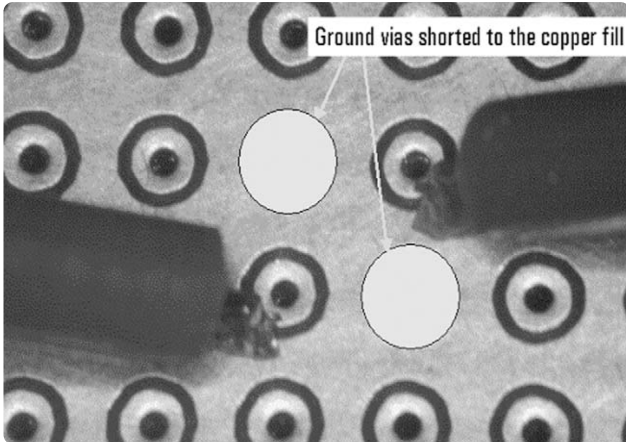

Figure 5. Pad geometry with copper fill adjacent to each signal via and the fill shorted to all ground vias

If this feature is added, a return path will be adjacent to each signal path and microprobe technology can be used. There is a slight increase in capacitance to the signal line, but this can be kept small, while still allowing all signal lines to be probed. With this approach, the density of probe points can increase almost 100 x over SMAs, and there is no loading of active signal lines. This approach will dramatically increase the value of instruments, both for passive, physical layer characterization and for active, signal monitoring.

Physical Layer Characterization

All the electrical performance information for a differential channel listed previously can be extracted using a four port VNA. It is actually the single ended S parameters that are measured in the frequency domain. Figure 6 shows the format for this information and the port labeling scheme for a differential channel that is measured as two single-ended channels.

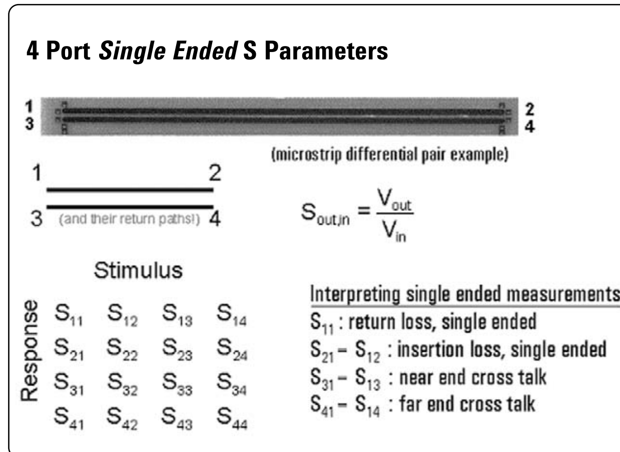

Figure 6. It is the four port singled ended S parameters that are measured and then transformed into other forms

These are mathematically transformed into the balanced, or mixed mode, or differential S parameters, also in the frequency domain. These parameters can be used directly to give information about the differential return or insertion loss, or can be transformed into the time domain to give information about the differential impedance profile of the channel or the location of the conversion of differential signal into common signal. The differential parameter matrix is shown in Figure 7.

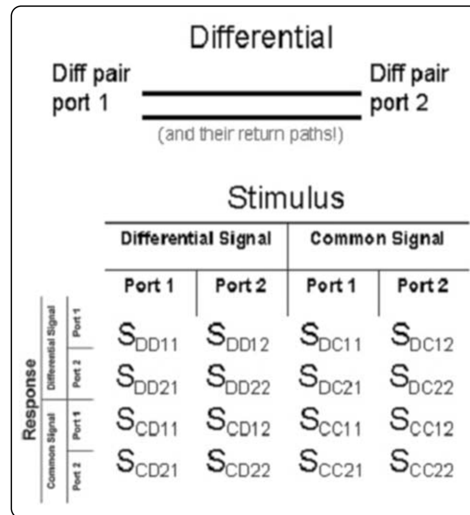

Figure 7. The result of the single ended to balanced S parameters transformation is a stimulus/response matrix of differential parameters

Understanding 4-port Mixed Mode Analysis

In order to interpret the large amount of data in the differential parameter matrix, it is helpful to analyze one quadrant at a time. The first quadrant is the upper left four parameters describing the differential stimulus and differential response characteristics of the device under test. This is the actual mode of operation for most high-speed differential interconnects, so it is typically the most useful quadrant that is analyzed first.

It includes the input differential return loss from both ends, SDD11 and SDD22, and the differential insertion loss, SDD21 and SDD12. Note the format of the parameter notation SXYba, where S stands for Scattering Parameter or S-Parameter, X is the response type (differential or common), Y is the stimulus type (differential or common), b is the output port and a is the input port. This is typical nomenclature for frequency domain scattering parameters. All sixteen differential S-Parameters can be transformed into the time domain by performing an Inverse Fast Fourier Transform (IFFT). The matrix representing the time domain will have similar notation, except the “S” will be replaced by a “T” (i.e. TDD11).

The second and third quadrants are the upper right and lower left four parameters, respectively. These are also referred to as the mixed mode quadrants. This is because they fully characterize any mode conversion occurring in the device under test, whether it is common-to-differential conversion (related to EMI susceptibility) or differential-to-common conversion (related to EMI radiation). Understanding the magnitude and location of mode conversion is very helpful when trying to optimize the design of interconnects for gigabit data throughput.

The fourth quadrant is the lower right four parameters and describes the performance characteristics of the common signal propagating through the device under test. For most differentially driven systems, the behavior of the common signals is not critically important. The information about how the channel affects common signals, the return and insertion losses, is contained in this quadrant. A summary of the four quadrants in the differential parameter matrix is shown in figure 8.

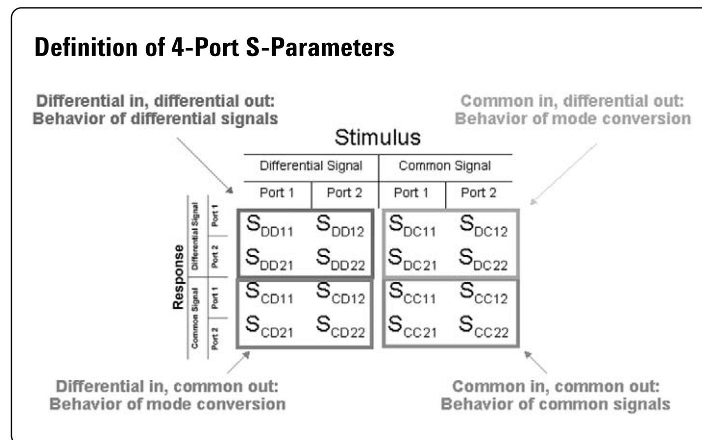

Figure 8. The result of the transformation is a stimulus/response matrix of differential parameters.

Design Case Study: XAUI Backplane

In order to demonstrate the proper measurement technique for characterizing a high-speed, linear, passive, interconnect, a popular industry standard XAUI backplane was utilized in a design case study. The expected serial data throughput of this device is a minimum of 3.125 Gbps. Daughter cards were used as test fixtures for analyzing the backplane and it’s connectors, since most test and measurement equipment has 3.5mm SMA connectors. A picture of the backplane is shown in Figure 9.

At a few selected locations, the SMA connectors were removed and microprobes were used to probe the differential channels. Because the via and pad design were optimized for SMA, and the performance is limited by the pad and vias, there was no improvement with microprobes. Both SMA measurements and microprobe measurements showed the same performance below 14 GHz.

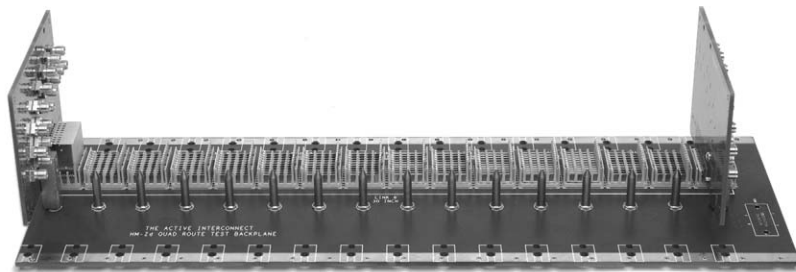

Figure 9. XAUI backplane used for Design Case Study (courtesy of John D’Ambrosia, Tyco Electronics)

Comparing Time Domain and Frequency Domain Data

Typically, the first step in analyzing the measurement data is to look at the reflected waveform. In the time domain, this is the differential impedance profile (TDD11). This intuitive waveform will quickly give the designer an idea of where the impedance mismatch of various structures (i.e. PCB trace, via, connector, etc) are causing reflections and degrading signal quality.

If a perfectly matched impedance environment is achieved, this waveform will be a flat horizontal line. Any deviation from this flat line can be interpreted as excess inductance (positive deflection from characteristic impedance) or excess capacitance (negative deflection from the characteristic impedance).

With the XAUI backplane, the individual features of the interconnect can be seen in Figure 10. From left to right, the first feature is excess inductance from the daughter card SMA connector, then the110 ohm daughter card differential transmission line, then the excess capacitance from the daughter card via field, then the excess capacitance from the backplane via field and then finally the 100 ohm differential backplane transmission line. The impedance profile of this complete differential channel can be easily seen in Figure 10.

Transforming the impedance profile into the frequency domain yields the input differential return loss (SDD11). Measured in decibels, return loss is a negative value that describes how the signal propagating through the device under test is reflected back as a function of frequency. Periodic negative deflections can be seen in this data that are a result of resonant structures within the device.

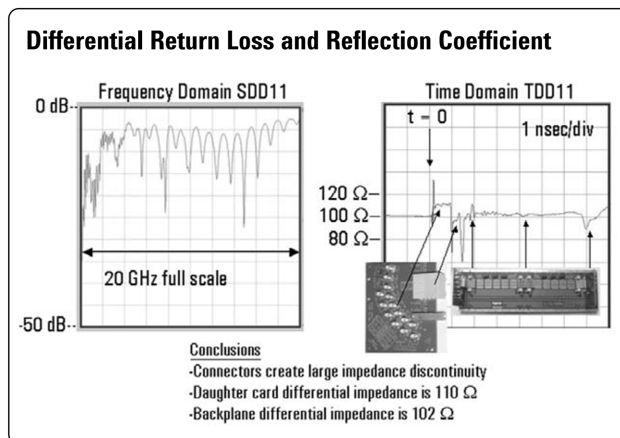

Figure 10. Analyzing both frequency and time domain data on XAUI backplane

Coupling Pulls Down Differential Impedance

In most single-ended high-speed digital interconnects, crosstalk between adjacent transmission lines is undesirable. This is not the case for differential transmission lines. The strong coupling of adjacent PCB traces that make up a differential pair is exactly what contributes to good common mode noise rejection. When targeting a specific differential impedance of 100 ohms, this coupling has to be taken into account.

An example of this can be seen in the impedance profiles in Figure 11. The single-ended TDR trace shows the daughter card and motherboard exhibiting around 55 to 56 ohms of single-ended impedance (only one line is driven, the other line is quiet and the impedance is measured from the driven line to ground).

The differential TDR trace shows the effect of coupling on the motherboard traces and yields about 100 to 101 ohms (both lines are driven with equal amplitude/opposite polarity steps and impedance is measured from line 1 to line 2). Notice that the daughter card differential impedance does not pull down to the target differential impedance of 100 ohms. This indicates weaker coupling on the differential traces due to larger spacing between daughter card traces.

Single-ended and Differential TDR

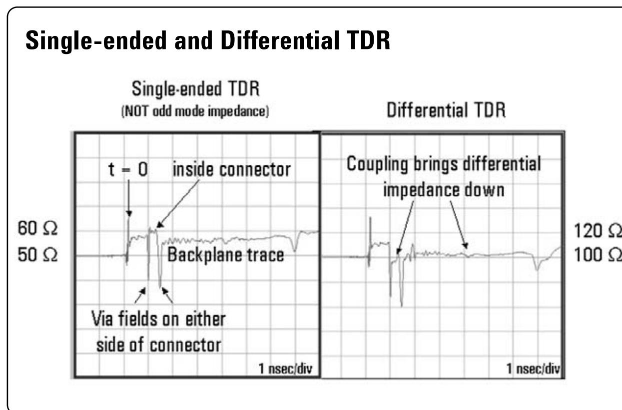

Figure 11. Comparing single-ended TDR and differential TDR indicates good coupling on backplane and in the connector

A figure-of-merit that has become important for characterizing high-speed differential channels is the input differential insertion loss (SDD21). This is the frequency response of the interconnect for a transmitted signal. It is often insightful to compare various length channels using SDD21. The two channels in Figure 12 are broadside-coupled stripline traces in a homogeneous dielectric system (both sides of copper embedded in dielectric). The 40-inch long channel has greater loss, as one would expect. Even though the measurement system had over 40GHz of bandwidth, it can be seen from Figure 12 that the device bandwidth falls off dramatically before 10GHz.

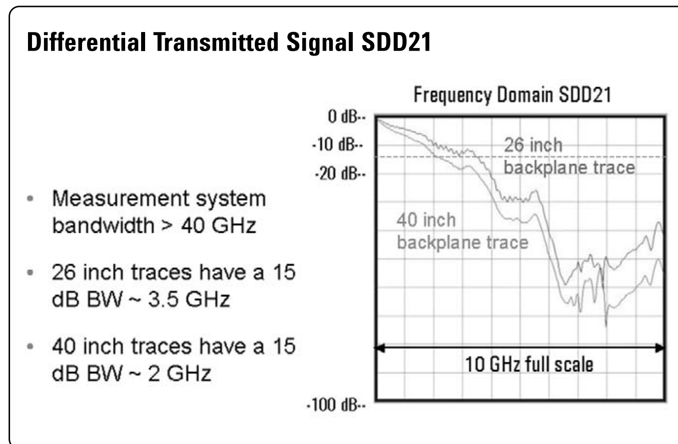

Figure 12. Differential insertion loss is a key figure-of-merit for backplane channels

Work performed by the High Speed Backplane Initiative (HSBI) includes the use of SDD21 to describe the relative amount of loss in multiple channels as a function of frequency. A typical compliance template would be used in a similar methodology to an eye diagram mask. A proposed SDD21 template is shown in Figure 13.

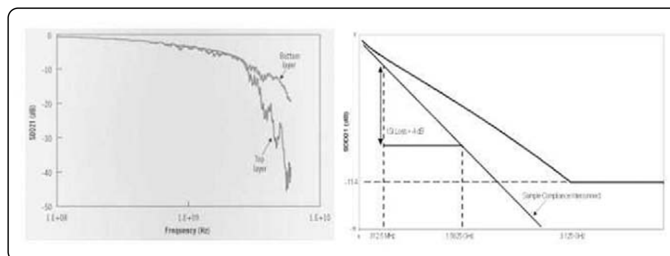

Figure 13. Example of SDD21 used as a compliance specification for 3.125 Gbps data transmission

Eye Diagram Simulation Using 4-port S Parameters

Most high-speed serializer-deserializer (SERDES) chipsets are verified to be compliant to standards by use of eye diagram analysis. A reference receiver used in conjunction with a high-bandwidth equivalent time sampling oscilloscope will display an eye diagram based upon the actual bit-stream output from the SERDES. The interconnect between the transmitter and receiver can be characterized using this test set up, also. Longer channel lengths between a SERDES chipset will exhibit eye diagrams that close with increasing length due to higher differential insertion loss. There is another way to obtain eye diagram information using S-Parameters.

The first step to achieve this simulated eye diagram is to obtain very accurate 4-port S-Parameters. This can be done using either a 4-port vector network analyzer or TDR with two differential-TDR modules (with PLTS software). Once the S-Parameters are obtained, the time domain impulse response of the channel can be derived. Using a Novel patent-pending algorithm, the impulse response can then be convolved with an arbitrary binary sequence. By changing the bit rate and risetime of the arbitrary binary sequence, a family of simulated eye diagrams can be developed as shown in Figure 14.

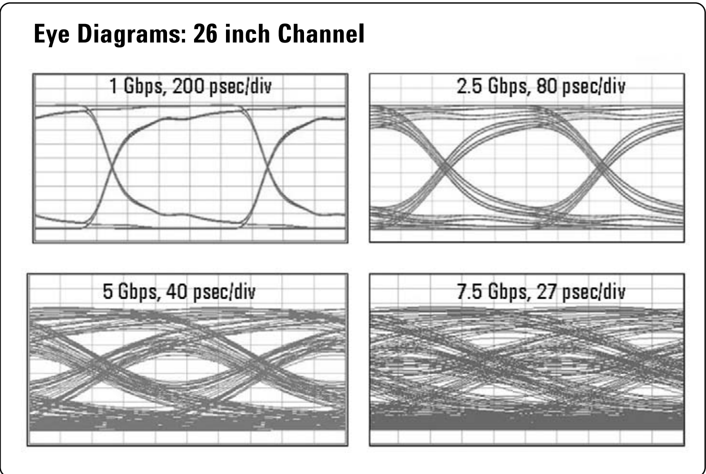

Figure 14. Eye diagrams derived from 4-port S-Parameters

Non-Ideal Differential Signaling (AKA Mode Conversion)

When a differential signal propagates through an ideal, symmetric, differential transmission line, no common signal will be generated. In other words, mode conversion should be zero for all frequencies (a flat, zero line). Any asymmetry between the lines that make up the differential pair can potentially convert some of the differential signal into a common signal. We generally call this effect, "mode conversion."

If no signals get out of the product enclosure, and there is sufficient common mode rejection ratio in the receivers, mode conversion may not be a problem. However, if a twisted pair connects to the end of the differential channel and any of this is converted to a common signal and gets out on the twisted pair, it will contribute to excessive radiated emissions.

Mode conversion can arise from asymmetries in the drivers and asymmetries in the interconnect. An example of active device mode conversion would be if a differential transmitter or amplifier had one drive signal different from the other supposedly complementary drive signal, either voltage, current, output impedance, or skew. An example of a passive device mode conversion would be if a differential connector had different characteristic impedance lines, different length pins, or different loading on each line such as jags, pads, or ground plane discontinuities. Mixed-mode analysis can be a powerful tool in locating obstacles that limit the highest possible data rate transmission in interconnects.

The differential-to-common signal conversion can be quantified as a percentage of amplitude by overlaying the time domain differential transmission waveform (TDD21) with the time domain differential to common transmission waveform (TCD21). As seen in Figure 15, the TDD21 waveform shows the propagation delay and risetime transition of the degraded differential signal at the output of the device under test.

Shown on a more sensitive scale, TCD21 is the amount of converted common signal coming out of the channel. This is the mode conversion waveform showing 7 percent of the original differential signal converted to common signal.

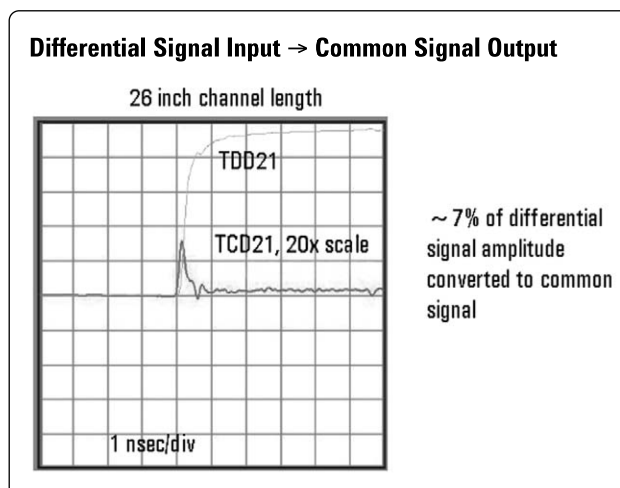

Figure 15. Overlaying mixed mode waveform TCD21 shows mode conversion of 7%

After determining that the mode conversion is present in the device under test, the next step is to locate the physical structure that is causing this undesirable effect. The easiest method for doing this is to view the input differential impedance profile (TDD11) and overlay the input time domain reflection mode conversion waveform (TCD11). Since TDD11 is roughly the impedance versus distance, this gives a physical reference to the structure of the daughter cards and backplane. The daughter card transmission line, daughter card via field, backplane connector, backplane via field, and backplane transmission lines are all clearly discernable from this impedance profile in Figure 16.

The corresponding location on the horizontal axis for the mode conversion waveform correlates exactly where the mode conversion is happening. This is how the mode conversion source is identified. The maximum deflection (positive or negative) in the mode conversion waveform is the structure that should be addressed first. Interestingly, the largest magnitude of mode conversion is not the backplane connector, but it is the via field layout on the daughter card and backplane.

In general, the greatest source of mode conversion is the asymmetry of the vias. As they generally represent the largest discontinuity, balancing this effect between both lines of the pair is difficult, if attention isn't paid to this. The conversion can be minimized if the via barrel and pads are optimized for 50 Ohms.

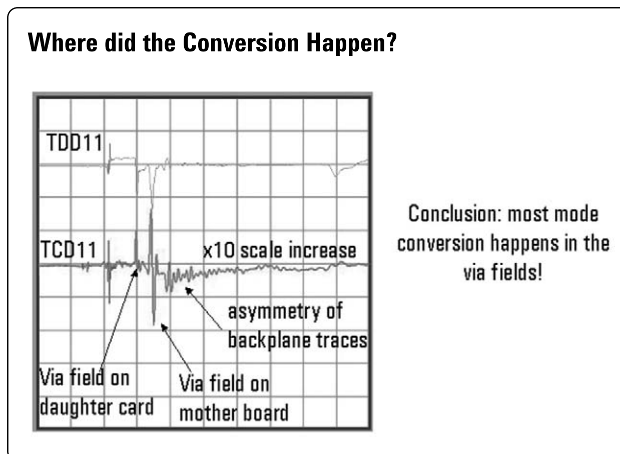

Figure 16. The location of mode conversion to be identified comparing the differential return loss to the common signal coming back to the source end.

Summary

Advanced design tools and test methodologies are now required to address the subtle signal integrity challenges created by microwave transmission line effects. Proper probing techniques are important to achieving fast design cycle improvements. In addition, complete measurement characterization of the physical layer in both the time domain and frequency domain is crucial to solving tomorrow's signal integrity problems.

References

Bogatin, Eric, *Signal Integrity-Simplified*, Prentice Hall, 2004.

Bogatin, Eric, *"Getting Your S (Parameters) Together"*, Printed Circuit Design and Manufacture, Feb. 2003.

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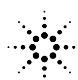

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