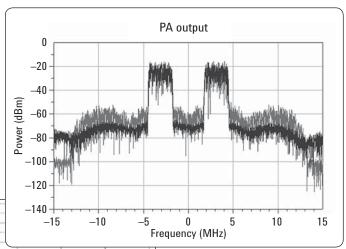# Linearization of a Multi-Carrier Power Amplifier using Digital Predistortion in ADS with the Linearization DesignGuide
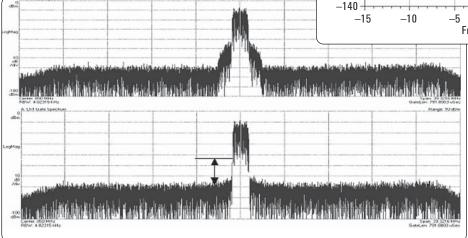
Connected Solutions
Application Bulletin 1476-3

Introduction

Modern wireless systems place extreme demands on base station power amplifiers when multiple carriers with high peak-to-average ratios are present. Linearization techniques must be applied to minimize spectral regrowth. One such technique is digital predistortion.

This application bulletin describes a method for using digital predistortion in ADS with the Linearization Design Guide to minimize spectral regrowth in wireless systems.

Agilent Technologies

Concept

In digital predistortion, a look-up table (LUT) containing optimized complex predistortion coefficients is dynamically addressed in proportion to the incoming signal envelope. These coefficients are multiplied with the signal ahead of the power amplifier. The coefficients model the inverse distortion characteristic of the DUT, as shown in Figures 1 and 2.
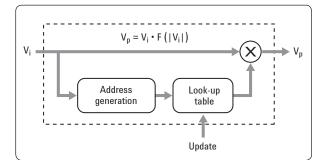

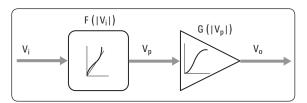**Figure 1. Addressing the lookup table.**

Figure 2. Predistortion applied to a non-linear power amplifier.

Advanced Design System (ADS) with the Linearization DesignGuide provides full implementation of digital predistortion for use with an actual Device Under Test (DUT). Menu-driven prompts control the initialization and updating of LUT coefficients, and provide access to pre-configured templates that provide connectivity to the ESG-C signal source and Vector Signal Analyzer (VSA).

Closed-loop Implementation

The closed-loop solution, shown in Figure 3, provides for optimization of the LUT coefficients by repeating the calculation of the coefficients with a feedback signal corresponding to the response of the PA DUT using the previous coefficients, until the difference between the feedback signal and the input signal is minimized to a defined tolerance.
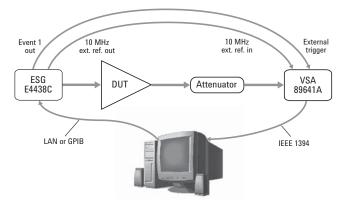

Figure 3. The closed-loop, ADS solution.

Training Signal

A training signal in the form of a linear ramp is inserted into the wireless signal. This signal is used by ADS to characterize the DUT's non-linear transfer characteristics. The ramp, shown in figure 4, occupies a small percentage of the total signal time, so it does not affect the inherent statistics of the wireless signal.
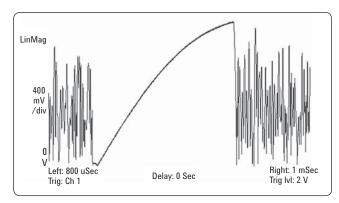

Figure 4. The response of the DUT to the training signal.

Using the Linearization DesignGuide for Digital Predistortion

The Linearization DesignGuide menu, shown in Figure 5, provides access to the Digital Predistortion functions and templates.
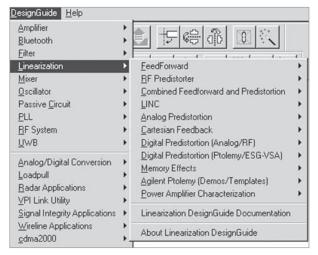

Figure 5. The Linearization DesignGuide menu.

To begin the process, the DUT is connected to the output of the ESG-C signal source and the VSA input, using an appropriate attenuator. The 10 MHz reference from the ESG-C is provided to the VSA hardware.
When using the 8905A input module, which does not have an external reference input as does the 8905B, the VSA's reference may be used to lock the ESG source. Finally, the Event1 trigger of the ESG-C is connected to the VSA hardware external trigger input and properly terminated.

There are two ADS templates provided with the Linearization DesignGuide to control the instruments and the predistortion process: the *ESG simulation* and the *VSA simulation*.

The DesignGuide menu provides step-by-step prompts, as shown in Figure 6.

Figure 6. The step-by-step menu for setting up the predistortion process.

Step 1: The LUT coefficients, which reside in a text file, are initialized to zero value. When the signal is downloaded to the ESG-C, no predistortion will be applied.

It is also important to note that the ESG component will normalize the signal to a peak magnitude of 1. The peak amplitude of the training signal at the output of the DUT will be different due to the DUT gain. A VSA scale factor is set to the inverse of this peak amplitude to calibrate the simulation.

Step 2: The ESG simulation is run to download the signal. The DUT should be connected and powered when running this simulation. At this point, the VSA may be run to observe the DUT output in both spectrum and time domains. The peak amplitude of the training signal can then be observed and the scale factor on the VSA simulation used in the next step may be set.

Step 3: The VSA simulation is run. Data from the ESG simulation input for reference, and data from the VSA is downloaded. ADS calculates the LUT coefficients and writes them to a data file in floating-point format.

Step 4: Update LUT coefficients. The LUT coefficients calculated in Step 3 are converted to fixed-point format and made available to the ESG simulation.

Step 5: Run the ESG simulation and record Power_Difference_dB, available from the ADS data display window. This value is the difference between the average output power with predistortion applied and the non-predistored power, due to gain expansion when pre-distortion is used. This value is noted and used in the next step.

Step 6: The value of Power_Difference_dB is subtracted from the original ESG output power to compensate for gain expansion, and the ESG simulation is run again to apply the first set of LUT coefficients to the DUT.

Step 7: Run VSA Simulation to calculate the 2nd set of LUT coefficients.

Step 8: Update LUT coefficients, similar to Step 4.

Step 9: Run ESG Simulation, similar to Steps 5 and 6.

This completes two iterations of LUT coefficient optimization. The process is repeated until little or no additional reduction of distortion products is observed.

Various ADS data displays such as the ones in Figure 7 are available to show the LUT coefficients and other signals helpful to understanding the process as it progresses.
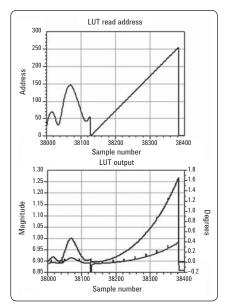

Figure 7. LUT Read Address and Complex Output

Summary

ADS and the Linearization DesignGuide provide an excellent method for using digital predistortion when designing power amplifiers for today's wireless systems. This closed-loop solution allows for faster, more accurate design. The prompt-driven DesignGuide makes it easy to create and update the digital predistortion lookup table.

Required Equipment/Software

E4438C Electronic Signal Generator (ESG) with arb (up to 6 GHz frequency range)
E89640 Vector Signal Analyzer (RF/IF to 2.7 GHz)

Advanced Design System (ADS)

E8900A Design Environment
E8901A Data Display
E8823A Ptolemy Simulator
E8822A Ptolemy Fixed Point Models
***E8857 CDMA Design Library**
***E8877 CDMA2000 Design Library**
***E8875 3GPP W-CDMA Design Library**

*Required for included pre-configured test benches but may be replaced with sources based on other Design Libraries

Agilent Technologies