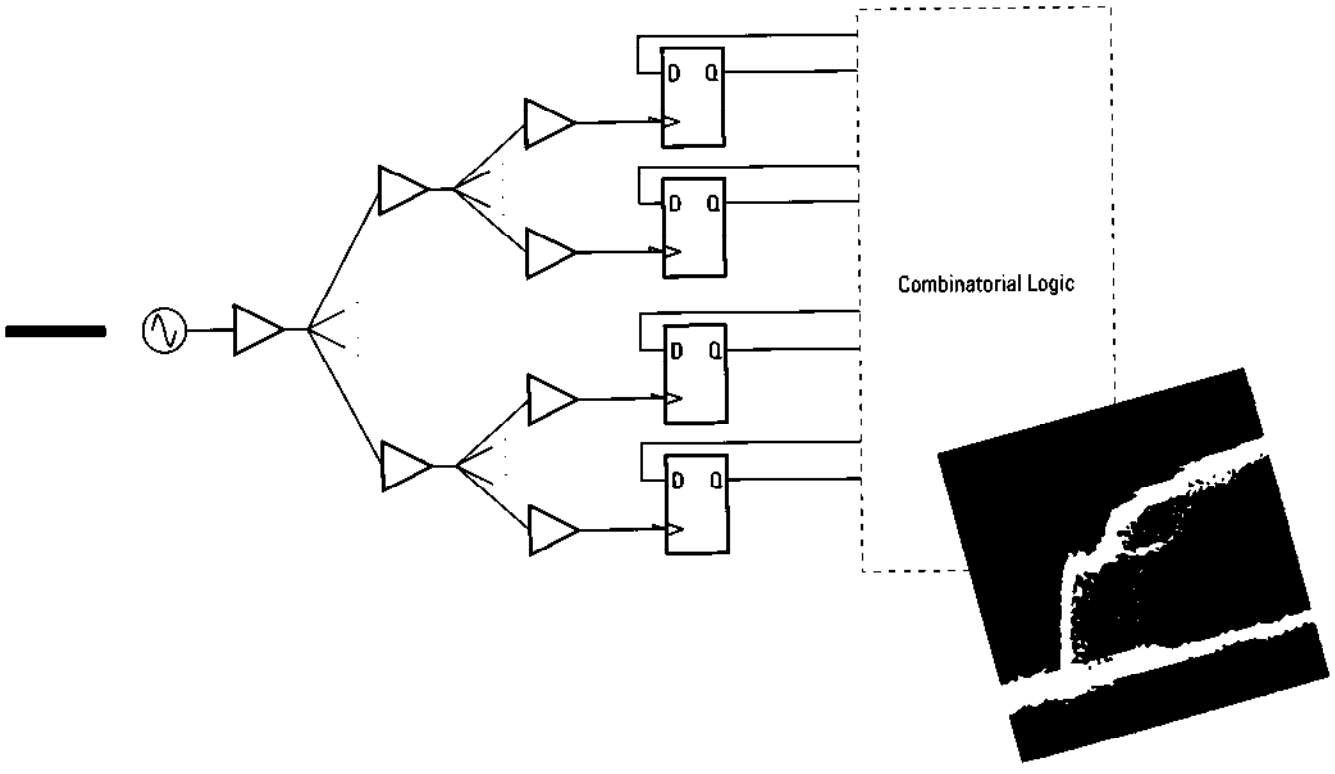
HEWLETT PACKARD

Timing Considerations in Clock Distribution Networks

Application Note 1210-10



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Introduction

The clock signal is the most important dynamic signal in a digital system. For proper system operation, a designer must make sure the timing environment is correct—or risk the product schedule and budget.

Figure 1 shows the timing environment of a digital system. The timing environment includes the clock generator, the clock distribution network (including buffering and system interconnects), and the memory elements. The computation environment includes the remaining logic in the system.

Consider the case of a large system of array processors using ECL 10KH131 flip-flops as the system state device, driven by a two-phase clock. The system ran correctly at 95% of full speed, but failed randomly at greater speeds. The failure location and symptoms differed for each occurrence. Analysis showed that some segment delays were slightly longer than the timing scheme and cycle time allowed. The problem was corrected by replacing the 10KH131 flip-flops with 10KH130 latches and widening the pulsewidth of both clock phases. Total delay in the prototype schedule: 11 weeks. Compare this to a situation where timing-environment design was well understood. A heavily-pipelined ECL system using a two-phase clock and latches for state devices had a clock cycle time of 22.5 ns with global clock skew of 3.5 ns. In each cycle, the data must propagate through 22.5 ns of logic. The prototype powered on and ran correctly at full speed because the designer addressed the timing environment and state architecture requirements. Thus, the system ran at 100% efficiency. Without proper design, the global skew would require a cycle time of 26.25 ns—wasting 17% of the cycle.

Information herein is provided by the courtesy of Michael K. Williams, Amherst Systems Associates.

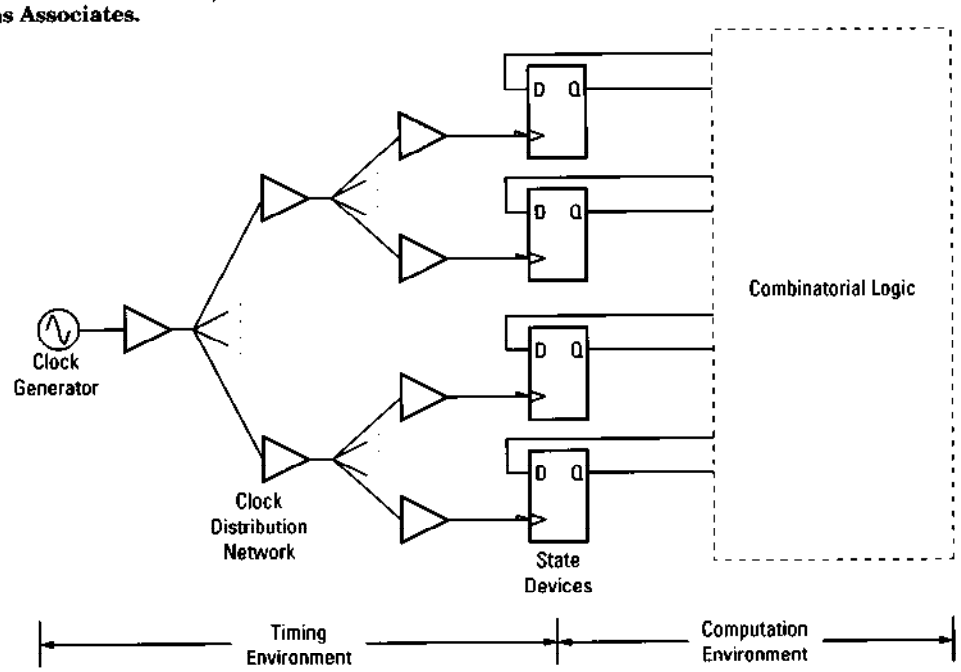


Figure 1. Timing Environment of a Digital System

Clock Signal Distortion

Four types of distortion can occur in the clock distribution network. First are problems with the signal integrity of the clock. These are typically the result of crosstalk, simultaneous switching noise, or other design oversights that degrade the fidelity of the signal. Second is jitter, which is a deviation in the arrival time of the clock edge. Jitter may be caused by variations in temperature or supply voltage at the oscillator or clock buffers. The third and fourth problems, which are clock skew and pulsewidth shrinkage and growth, are described in more detail in the remainder of this note.

Clock Skew

As the clock signal propagates through the distribution network, it is delayed by the devices in the network and by the interconnection paths. The total delay time to a particular level in the network is the clock path delay. Clock skew is the tolerance on the arrival time of the active edge to the inputs of state devices in the system. See figure 2. Skew is not the same as the clock path delay. Both the devices and the interconnects in the clock distribution network contribute to skew.

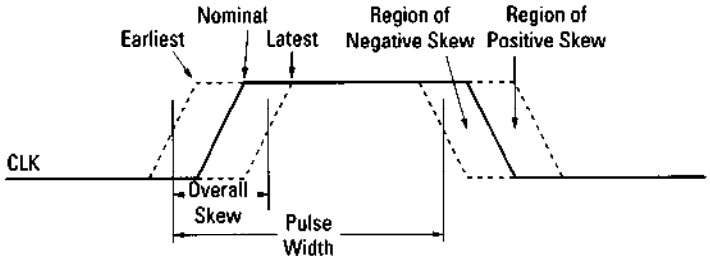


Figure 2. Clock Skew

Delay and skew in the network can be measured by observing the clock at several different leaves of the distribution tree. Figure 3 shows the delay between the clock (upper trace) and the output of three different paths through the distribution network. Note that the active edge of the distributed clock signal passes through the threshold at three distinctly different times, illustrating the skew problem. Figure 4 shows a closer look at the skew components of the system. Both figures were created using an Amherst Systems Associates clock

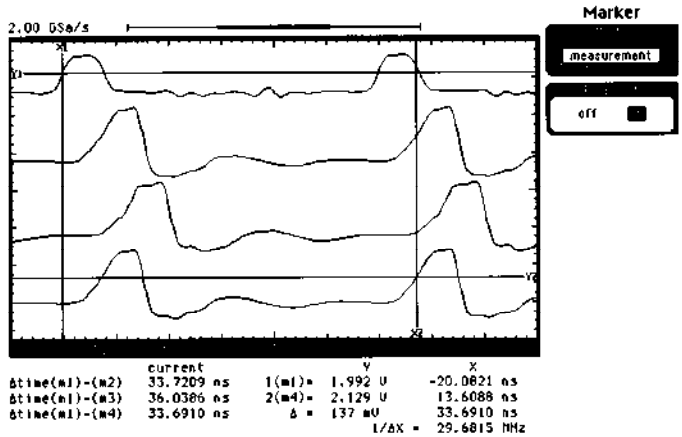


Figure 3. Path Delay in Clock Signal

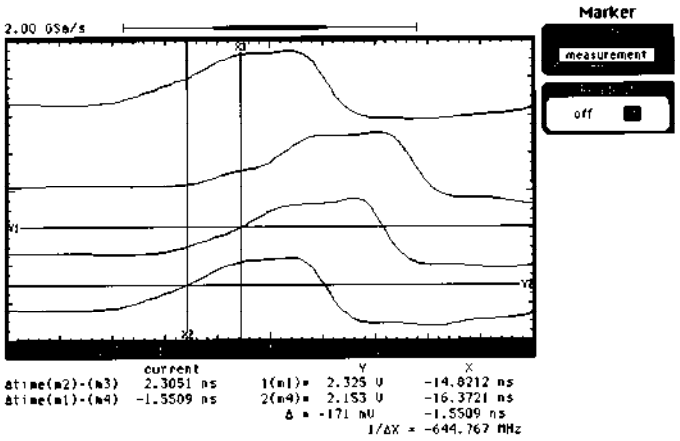


Figure 4. Skew in Clock Signal

distribution network testbed similar to figure 1. An HP 8133A pulse generator was used as the clock source and an HP 54720A digitizing oscilloscope recorded the waveforms.

Skew Introduced by Devices

Manufacturing tolerances in the buffers used in the clock distribution network account for one component of skew. These include propagation delay tolerances (which may vary for positive and negative edges), edge rate tolerances, and threshold voltage tolerances. For systems with very aggressive timing requirements, it is best to characterize individual devices and interconnecting components used to manufacture the system, then match parts with compatible characteristics.

Skew Introduced by the Interconnect

The interconnects that route the clock signal throughout the system also contribute to skew. As logic devices improve, these interconnects become a larger part of the skew problem. There are three components of interconnect-based skew. The first is the difference in capacitive loading between the clock trace and adjacent traces, vias, IC leads, and other signal and power planes. The second is the variation in propagation rate because of varying dielectric constants due to inconsistency in the board materials. Tolerances on board thickness and etch dimensions can affect propagation rate; also, if the clock signal passes both on the board surface and in internal layers, the changing propagation rate will affect the skew. The third is that variations in the etch geometry for clock traces will contribute to skew.

Structural Errors

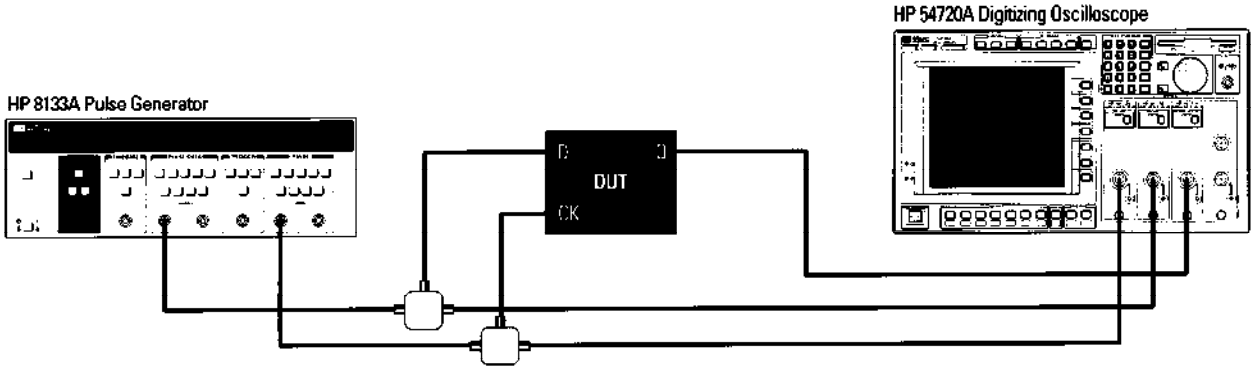
Various design errors can also contribute to skew. For example, extracting the clocks for a given set of state devices from different levels of the CDN means that each clock has different arrival time—though this can also be used to advantage in solving certain problems with unexpectedly long segment delays. Inconsistent use of inverting and noninverting buffer outputs, overloading the buffer outputs, and using fanout schemes other than lumped fanout can all adversely affect the clock skew.

Selecting Equipment for Clock Distribution Network Testing

Test equipment that can accurately resolve timing differences of picoseconds is needed to accurately measure skew and characterize device behavior in high-speed digital systems.

HP 8133A Pulse Generator
- 1-ps timing resolution
- Channel deskew
- 1.5-ps RMS typical jitter
- +15/–5 ns delay pulse/data mode
- 32-bit data channel w/pseudo-random bit sequences (PRBS)

HP 54720A Digitizing Oscilloscope
- 2 GSa/s sample rate on 4 channels
- Display update rate greater than 170 waveforms/s
- Channel deskew
- Automatic measurements
- User-defined measurement parameters



Test Setup for Characterizing a D Flip-Flop

Other Components of Skew

Jitter, or "phase noise," is the variation in the arrival time of a waveform event (such as the clock signal) relative to a particular point. Such noise may come from the power supply or other sources. Threshold voltage variations in the state devices also can contribute to skew; these are a component of the setup and hold time.

Pulsewidth Shrinkage and Growth (SAG)

While not as serious a problem as skew, pulsewidth shrinkage and growth (SAG) can contribute to timing failures. SAG is caused by asymmetrical leading and trailing edge propagation delays of the buffers in the clock distribution network.

Exceeding the maximum permitted pulsewidth in a multiphase system can create a race condition; in a single-phase system, faulty device triggering can occur. Violating minimum pulsewidth constraints (established by the device manufacturer or your own measurements) will create marginal conditions for triggering the device.

Skew in the clock distribution network may require that you widen the pulse. Also, the devices in the network may slow the edges of the pulse, requiring a wider pulse at the source so that the clock at the distribution points will meet device specifications. Another source of SAG is unequal threshold voltages for leading and trailing edges of a pulse (devices with Schmitt-trigger inputs).

Timing Failures

When skew and pulsewidth shrinkage and growth are not accounted for in the system design, the clock may arrive at the wrong time. If it arrives in the setup and hold time window, it is likely that the device may lose data, oscillate, or exhibit metastable behavior. The system may fail consistently, making the problem easy to locate, or it may fail only occasionally, in random locations.

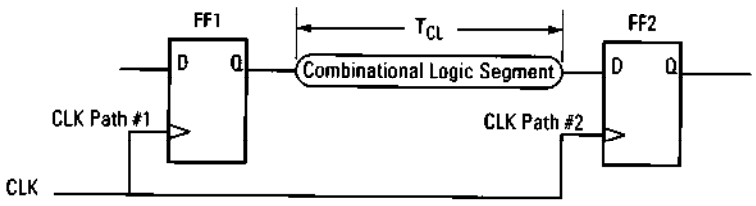


Figure 5. Circuit that may Exhibit Failures due to Timing Violations

Figure 5 shows a typical situation where skew will cause a problem. When this circuit works properly, a positive edge on CLK transfers data from D to Q on FF1. This data propagates through a logic segment and arrives at the D input of FF2 in time for the next positive edge of CLK. Suppose that CLK Path #1 is slower than nominal or that CLK Path #2 is faster than nominal. Then the setup time restriction for FF2 will be violated and the system will fail.

Metastable behavior is a common result of timing violations. The resolution time is a Gaussian random variable. With many forms of signal behavior, metastability can be difficult to capture and characterize. A digitizing oscilloscope, such as the HP 54720A, with time pattern triggering, high sample and update rates, and infinite persistence, can make it possible to capture and correctly characterize metastable behavior. Figure 6 shows a signal with both low-grade metastability (jitter-like behavior at the top of the rising edge), which may cause infrequent and unrepeatable failures. The figure also shows a single fully metastable trajectory that resolves incorrectly to a low.

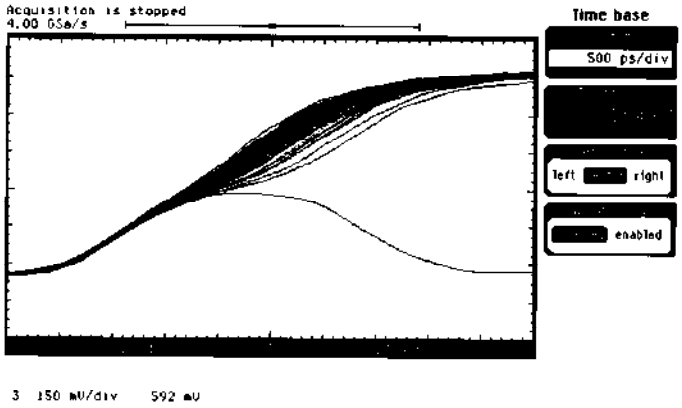


Figure 6. Metastability Resulting from Setup and Hold Time Violations

Timing Environment Design

The best strategy for avoiding timing environment problems is planning. An effective strategy is to use an accurate pulse generator and oscilloscope (such as the HP 8133A and HP 54720A) to characterize buffer and state devices used in the design. Also, be sure to carefully consider PCB design, including trace width, length, and routing. Finally, for very high-performance systems, more sophisticated timing schemes, such as multiple-clock, multiple-phase, polychronic, and tunable-delay, may be used to solve the problems caused by tolerance effects, most notably skew.

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