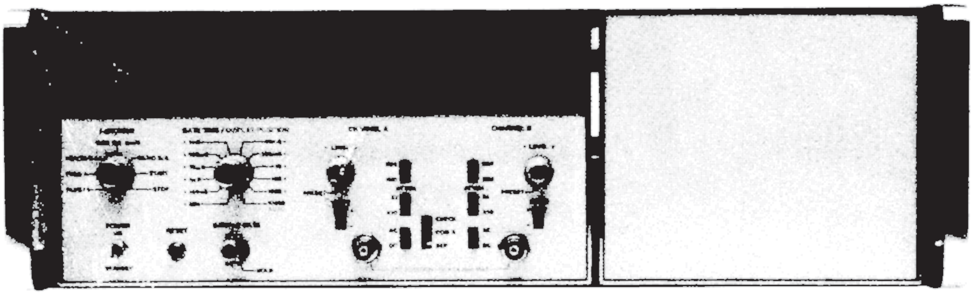
OPERATING AND SERVICE MANUAL

ELECTRONIC COUNTER

5345A



HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this instrument met its published specifications at the time of shipment from the factory. Hewlett-Packard Company further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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5345A
ELECTRONIC COUNTER

OPERATING AND SERVICE MANUAL

SERIAL PREFIX: 1708A

This manual applies directly to HP Model 5345A Electronic Counters having serial number prefix 1708A.

NEWER INSTRUMENTS

This manual, with enclosed "Manual Changes" sheet, applies to HP Model 5345A Electronic Counters having serial number prefixes as listed on the "Manual Changes" sheet.

OLDER INSTRUMENTS

For serial prefixes below 1708A; refer to Section VII for manual backdating.

MANUAL PART NUMBER 05345-90025
Microfiche Part Number 05345-90026
PRINTED IN U.S.A.
Printed: FEB. 1977

[illegible] STEVENS CREEK BLVD., SANTA CLARA, CALIF. 95050

HEWLETT
PACKARD

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SAFETY CONSIDERATIONS

GENERAL

This is a Safety Class I instrument. This instrument has been designed and tested according to IEC Publication 348, "Safety Requirements for Electronic Measuring Apparatus", and has been supplied in safe condition.

OPERATION

BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage and the correct fuse is installed (see Section II, Paragraph 2-6.) Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuseholders must be avoided.

SERVICE

Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to retain the instrument in safe condition. Service and adjustments should be performed only by qualified service personnel.

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Whenever it is likely that the protection has been impared, the instrument must be made inoperative and be secured against any unintended operation.

WARNING

IF THIS INSTRUMENT IS TO BE ENERGIZED VIA AN AUTOTRANSFORMER (FOR VOLTAGE REDUCTION) MAKE SURE THE COMMON TERMINAL IS CONNECTED TO THE EARTHED POLE OF THE POWER SOURCE.

WARNING

BEFORE SWITCHING ON THE INSTRUMENT, THE PROTECTIVE EARTH TERMINALS OF THE INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).

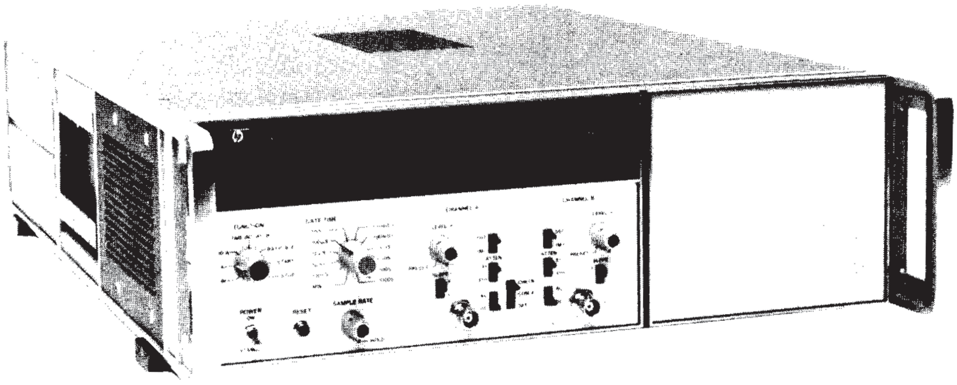
WARNING

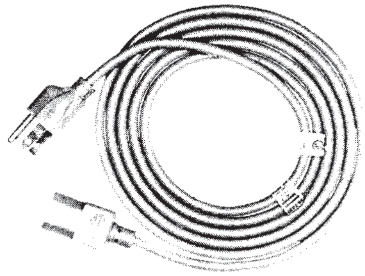
THE SERVICE INFORMATION FOUND IN THIS MANUAL IS OFTEN USED WITH POWER SUPPLIED AND PROTECTIVE COVERS REMOVED FROM THE INSTRUMENT. ENERGY AVAILABLE AT MANY POINTS MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

CAUTION

BEFORE SWITCHING ON THIS INSTRUMENT:

1. MAKE SURE THE INSTRUMENT IS SET TO THE VOLTAGE OF THE POWER SOURCE.
2. ENSURE THAT ALL DEVICES CONNECTED TO THIS INSTRUMENT ARE CONNECTED TO THE PROTECTIVE (EARTH) GROUND.
3. ENSURE THAT THE LINE POWER (MAINS) PLUG IS CONNECTED TO A THREE-CONDUCTOR LINE POWER OUTLET THAT HAS A PROTECTIVE (EARTH) GROUND. (GROUNDING ONE CONDUCTOR OF A TWO-CONDUCTOR OUTLET IS NOT SUFFICIENT.)
4. MAKE SURE THAT ONLY FUSES WITH THE REQUIRED RATED CURRENT AND OF THE SPECIFIED TYPE (NORMAL BLOW, TIME DELAY, ETC.) ARE USED FOR REPLACEMENT. THE USE OF REPAIRED FUSES AND THE SHORT-CIRCUITING OF FUSE HOLDERS MUST BE AVOIDED.





POWER CABLE HP NO. 8120-1378
U.S.A., Canada

Figure 1-1. Model 5345A Electronic Counter with Accessories Supplied

SECTION I
GENERAL INFORMATION

1-1. DESCRIPTION

1-2. The Hewlett-Packard Model 5345A Electronic Counter is a reciprocal counter capable of direct measurements to 500 MHz. The counter's ability to accept plug-in accessories extends its inherent capabilities and provides for a variety of additional measurements.

1-3. The instrument measures frequency, period, period average, single-shot time interval, time intervale average, and ratio. It also provides a totalize function, whereby two signals can be simultaneously totalized with the displayed result being the sum of difference in the total number of counts. Using the 5245 series of plug-ins (with 10590A Adapter) extends the frequency range to 18 GHz and adds other features, such as DVM capability.

1-4. INSTRUMENT IDENTIFICATION AND MANUAL CHANGES

1-5. Hewlett-Packard instruments have a 2-section, 10-character serial number (0000A00000), which is located on the rear panel. The 4-digit serial prefix identifies instrument changes. If the serial prefix of your instrument differs from that listed on the title page of this manual, there are differences between this manual and your instrument. Instruments having lower serial prefixes than that listed on the title page are documented in Section VII, and higher serial prefixes are covered with manual change sheets included with the manual. If the change sheet is missing, contact the nearest Hewlett-Packard Sales and Service Office listed on the inside rear cover of this manual.

1-6. OPTIONS

1-7. The following is a list of available options: Option 001, 10 MHz, Voltage Controlled Oscillator; Option 010, General Purpose Interface Output (Digital Output only, HP-IB format); Option 011, General Purpose Interface I/O (provides digital output and input control over all functions except input amplifier); Option 012, similar to Option 011 but includes slope and level control. Option 908 Rack Mounting Kit is available, at additional cost, when ordered at the same time as the instrument.

1-8. ACCESSORIES

1-9. Table 1-1 list equipment supplied and Table 1-2 list accessories available.

Table 1-1. Equipment Supplied

Description	HP Part No.
Detachable Power Cord 231 cm (7-½ feet long)	8120-1378

Table 1-2. Accessories Available

Description	HP Part Number
Automatic Frequency Converter (15 MHz to 4 GHz)	5345A
Rack Mounting Kit	5060-8740
Plug-In Adapter (for 5245 series plug-ins)	10590A
ASCII-to-Parallel Converter (Converts ASCII coded data to printer format)	59301A
Numeric Display (provides auxillary display)	59304A
Relay Actuator (relay switching controlled manually or by ASCII codes)	59306A
VHF Switch (allows two VHF signals to switch from one input to one of our outputs or vice versa. Controlled manually or by ASCII codes.)	59307A
Digital-to-Analog Converter	59303A
Marked Card Programmer (programs counter with marked sense cards)	3260A
I/O Card for 2100 Computer	59310A
Interface Cables (3, 6, and 12 feet, respectively)	10631A/B/C
Calculator (used as controller to program counter)	9820A or 9830A
Digital Recorder (provides printed copy of counter's data)	5050B or 5055A
Digital Recorder Interconnect Cable	562A-16C
Board Extender Kit	10595A
Replacement Board Kit	10597A
5245 Series Plug-Ins	
Frequency Converter (20-100 MHz, 50 mV rms sensitivity)	5251A
Prescaler (DC - 350 MHz, 100 mV rms sensitivity)	5252A
Frequency Converter (50-512 MHz, 50 mV rms sensitivity)	5253B
Frequency Converter (150 MHz - 3 GHz, 50 mV rms sensitivity)	5254C
Frequency Converter (3-12.4 GHz, 100 mV rms sensitivity)	5255A
Frequency Converter (8-18 GHz, 100 mV rms sensitivity)	5256A
Transfer Oscillator (.05-18 GHz, 100 mV rms; .05-15 GHz, 140 mV rms, 15-18 GHz)	5257A
Sensitive Prescaler (1-200 MHz, 1 mV rms sensitivity)	5258A
Video Amplifier (10 Hz - 50 MHz, 1 mV rms sensitivity)	5261A
Time Interval (1 μs - 2x10^4 sec, 0.1 μs resolution)	5262A
Digital Voltmeter (10V, 100V, 1000V fullscale; 100 μV resolution)	5265A
Time Interval (100 ns to 2x10^4 sec., 12 ns resolution)	5267A

Table 1-3. Specifications

FREQUENCY/FREQUENCY AVERAGE PERIOD/PERIOD AVERAGE MEASUREMENTS

Both frequency and period are measured by measuring the total elapsed time T, for an integral number of cycles, N, of the input waveform. Computation, involving the quantities of N and T, provides direct readout of either frequency or period.

Range: 50 μHz to 500 MHz; 2 nsec to 20,000 seconds

Measurement Time: Consists of GATE TIME plus the time required to reach the next STOP trigger level. When in MIN the GATE TIME is less than 50 nanoseconds. When in a decade step, the counter will reset if a stop trigger level is not reached within approximately 3.4 times the GATE TIME setting. Decade GATE TIME ranges from 100 nsec to 1000 sec.

When using EXT GATE the measurement time consists of the GATE TIME divided by the duty cycle of the EXT GATE signal plus the time required to reach the next STOP trigger level after the end of the last EXT GATE pulse.

Accuracy: Resolution is nine digits per second of measurement time. With DISPLAY POSITION switch in AUTO the least significant digit error is ±1 count if the most significant digit is 1 through 4, and ±2 counts if the most significant digit is 5 through 9. Accuracy is ± least significant digit (LSD) counts ± time base accuracy ± trigger error.*

TIME INTERVAL/TIME INTERVAL AVERAGE

Range: 10 nsec to 20,000 sec

Minimum Time Between Trigger Points: 10 nsec

Trigger Pulse Width: 1 nsec minimum width input at minimum voltage input.

Accuracy:

Time Interval: ± trigger error** ± 2 ns ± time base accuracy

Time Interval Averaging:

$$\pm \frac{\text{trigger error}^{**} \pm 2 \text{ nsec}}{\sqrt{\text{intervals averaged}}} \pm .7 \text{ nsec} \pm \text{time base accuracy}$$

Not affected by harmonics of clock frequency.

Resolution:

Time Interval: 2 nsec

Time Interval Average:

$$\pm \frac{2 \text{ nsec}}{\sqrt{\text{intervals averaged}}} \pm 2 \text{ picoseconds}$$

Measurement Time: For single time interval measurements the GATE TIME switch should be in MIN. Measurement time will be the displayed time interval.

When a decade GATE TIME is selected, the counter will be in the TIME INTERVAL AVERAGE mode. The GATE TIME selected should be greater than the displayed time interval. The measurement time is now the GATE TIME divided by the duty cycle of the time interval waveform plus the time required to reach the next trigger stop level after the total GATE TIME has been accumulated.

RATIO B/A

Range: Both channels accept dc to 500 MHz

Accuracy: ± LSD ± trigger error* (applies only to channel A). LSD is as described under FREQUENCY ACCURACY.

Measurement Time: Measurement time is equal to the GATE TIME selected times 500 MHz/frequency of Channel B input.

START/STOP

Range: Both inputs may have repetition rates from dc to 500 MHz.

Modes: A, A+B, and A–B is determined by a rear panel switch.

Resolution: Not affected by GATE TIME setting. Resolution is one count up to eleven digits.

Accuracy: Coincident pulses may be applied to both inputs. One count is required to initiate each input, i.e., in Mode A add one count to display, in Mode A+B add two counts to display, in Mode A–B add no counts to display.

SCALING

Range: dc to 500 MHz

Scaling Factor: Selectable by GATE TIME setting. As GATE TIME is varied from the 100 ns position to the 1000 s position, scaling factor increases from 10^2 to 10^{12}. Actual scaling factor equals GATE TIME setting ÷ 10^{-9} seconds.

Input: Input signal through Channel A.

Output: Output frequency equals input frequency divided by scaling factor. Rear panel BNC supplies 80% duty cycle TTL compatible pulses.

INPUT CHANNELS A AND B SEPARATE INPUTS

Range: DC coupled, 0 to 500 MHz
AC coupled, 1 MΩ 200 Hz to 500 MHz
50Ω 4 MHz to 500 MHz

Impedance: Switch selectable, 1 MΩ shunted by less than 30 pF or 50Ω nominal

Sensitivity: (preset)

X1	20 mV rms sine wave, 60 mV p-p pulse
X10	200 mV rms sine wave, 600 mV p-p pulse

Dynamic Range: (preset)

50Ω	X1	20 mV to 250 mV rms sine wave 60 mV to 750 mV p-p pulse
	X10	200 mV to 2.5V rms sine wave 600 mV to 7V p-p pulse
1 MΩ	X1	20 mV to 250 mV rms sine wave 60 mV to 750 mV p-p pulse
	X10	200 mV to 2.5V rms sine wave 600 mV to 7.5V p-p pulse

Linear Operating Range: –2.0 to +0.5 Vdc

Trigger Level: Continuously adjustable over ±1.3 Vdc. Adjustment is nonlinear with more settability around zero volts.

Preset: Centers trigger level about dc at 25°C

Drift: ±10 mV dc max., 0°C to 55°C

Output: CHAN A and CHAN B output trigger voltage (X ATTEN) is accurate to within ±15 mV (X ATTEN) of actual trigger point hysteresis center. Rear BNC connectors.

Slope: Independent selection of positive or negative slope.

---

*Trigger error for sine waves of 40 dB signal-to-noise amplitude ratio is < (±0.3% of one period + number of periods averaged). If peak noise amplitude is greater than 10 millivolts, additional miscounting may occur (this situation can arise when measuring high-level outputs of broadband synthesized signal sources).

**For any wave shape, trigger error is less than

$$\pm \frac{0.0025}{\text{signal slope in V}/\mu\text{s}} \mu\text{s (with 40 dB S/N) or}$$

$$\pm \frac{2 \times \text{peak noise voltage}}{\text{signal slope in V}/\mu\text{s}} \mu\text{s}$$

Table 1-3. Specifications (Continued)

Maximum Input: Damage may occur beyond specified level. For larger inputs voltage divider probes 10020A for 50Ω and 10004B for 1 MΩ are recommended.

50Ω	X1	±7V dc 7V rms below 5 MHz 3.5V rms (+24 dBm) above 5 MHz
	X10	±7V dc, 7V rms (+30 dBm)
1 MΩ	X1	±350V dc 250V rms to 20 kHz 3.5V rms to above 5 MHz
	X10	±350V dc 250V rms to 20 kHz 35V rms above 5 MHz

Cross Talk: No effects if inputs to Channel A and B are both above or below 100 MHz. With one signal above 100 MHz and the other below, there are no effects if the lower frequency signal has a slew rate of ⩾10V/μs.

COMMON INPUT

In this mode the signal is applied to Channel A through a power splitter which equalizes impedances and delays to the input amplifiers. Channel B input is disabled. Both input impedance switches should be in the same position. All specifications are the same as for separate operation with the following differences.

Range: DC coupled, 0 to 400 MHz
AC coupled, 1 MΩ 300 Hz to 400 MHz
50Ω 4 MHz to 400 MHz

Impedance: 1 MΩ becomes 500 kΩ shunted by <50 pF
50Ω no change

Sensitivity: (preset)

50Ω X1	40 mV rms sine wave, 120 mV p-p pulse
X10	400 mV rms sine wave, 1.2V p-p pulse
1 MΩ	no change

Dynamic Range: (preset)

50Ω X1	40 mV to 500 mV rms sine wave 120 mV to 1.5V p-p pulse
X10	400 mV to 5V rms sine wave, 1.2 to 5V p-p pulse
1 MΩ	no change

Maximum Input:

50Ω	±5.0V dc and 5V rms
1 MΩ	no change

Trigger Level: Continuously adjustable over the range of ±2.6 Vdc in 50Ω or ±1.3V dc in 1 MΩ multiplied by the attenuator setting.

Output: Rear BNC Connector

50Ω	Output voltage X2 (X ATTEN) is accurate to within ±15 mV X2 (X ATTEN) of actual trigger point.
1 MΩ	Same as in SEPARATE.

GENERAL

Display: 11 digit LED display and sign. Annunciator displays ksec to nsec, k to n, μHz to GHz. Decimal point is positioned with DISPLAY POSITION control or positioned after the first, second, or third most significant digit if DISPLAY POSITION is in AUTO. Leading zeros are suppressed.

Overflow: Asterisk is illuminated when display is overflowed or underflowed.

Sample Rate: Continuously variable from <0.1 sec to >5 sec with front panel control. In HOLD position the last reading is maintained until the counter is manually reset or an EXTERNAL ARM signal is applied. Number of readings per second will generally be limited by the output device, i.e., 5150A Printer or 9830A Calculator. In COMPUTER DUMP mode the counter can take up to several thousand readings per second.

External Arm Input: Arming will be initiated by -1.0V (-5.0 V max) into 50Ω rear BNC input for greater than 500 ns. Minimum time between EXT ARM and acceptance of start pulse is <1 μs.

External Gate Input: EXT GATE feature will respond to a 0.0V to -1.0V pulse into 50Ω with 50 ns or faster rise and fall time pulse edges. Maximum pulse height (damage level) is -5V. Minimum pulse width is 20 ns. Time delay of the leading edge of EXT GATE to the acceptance of input signal is less than 20 ns.

Gate Output: >1 volt into 50Ω.

Reset: Counter resets at initial turn on. Can be reset at any time with front panel pushbutton or through HP Interface Bus.

TIMEBASE

Standard High Stability Timebase: Crystal Frequency, 10 MHz Oven Oscillator (10544A). (See separate data sheet).

Stability:

Aging Rate:	<5 x 10^{-10}* per day
Short Term:	<1 x 10^{-11} for 1 s average
Temperature:	<7 x 10^{-9}, 0°C to 55°C
Line Voltage:	<1 x 10^{-10}**, ±10% from nominal

External Frequency Standard Input: 1, 2, 2.5, 5, or 10 MHz ± 5 x 10^{-8}. Input voltage ⩾ 1 V rms into 1 kΩ.

*For Oscillator off time less than 24 hours.
**15 minutes after change.

Option 001: Crystal Frequency, 10 MHz

Stability:

Aging Rate:	<3 x 10^{-7} per month
Short Term:	<2 x 10^{-9} rms for 1 s average
Temperature:	<2 x 10^{-6}, 25°C to 35°C <5 x 10^{-6}, 0°C to 55°C
Line Voltage:	<1 x 10^{-8}, ±10% from nominal

External Frequency Standard Input: 1, 2, 2.5, 5, or 10 MHz ±5 x 10^{-6}. Input voltage ⩾1 Vrms into 1 kΩ.

Frequency Standard Output: 10 MHz 1 Vrms high purity sine wave from 50Ω source.

Operating Temperature: 0°C to 55°C

Power Requirements: 100/120/220/240 Vrms +5% -10%, 48 to 66 Hz, maximum power 250 VA.

Weight: 37 lbs (17 kg) net

OPTIONS

Option 001: Room temperature time base (room temperature crystal).

Option 010: Digital Output only. HP Interface Bus format, useful with 5150A Printer or 59301A with 5050B Printer.

Option 011: Digital Input/Output. Full compatibility with HP Interface Bus. Provides digital output as well as input for control over all functions except input amplifier.

Option 012: Similar to Option 011 but includes slope and level control. Recommended for computer or dedicated calculator applications. Programming codes differ slightly from Option 011. See 5345A Option 012 Technical Data Sheet for full specifications.

Option 908: Rack Mounting Kit

Table 1-3. Specifications (Continued)

SELF-TEST

A 100 MHz is internally applied for testing all functions. Pushing RESET illuminates all segments of display digits. Seven internal diagnostic switches are provided for verifying the operation of the input amplifiers, digital front-end, processor, and plug-ins.

ACCESSORIES AVAILABLE

K13-59992A ASM Tester: Useful for troubleshooting Algorithmetic State Machine processor

10595A Board Extender Kit: Useful for troubleshooting plug-in boards while in operation.

10590A Plug-In Adapter: Increases usefulness of 5345A by providing interface to 5245L plug-ins. Except as noted, the plug-ins listed below operate in a manner as they do in the 5245L. Measurements taken with the plug-in adapter combination yield similar accuracy, and greater speed and resolution than is associated with the 5245 series counters. Compatible plug-ins: 5251A, 5252A (lower frequency limit 1 MHz), 5253B, 5254C, 5255A, 5256A, 5257A, 5258A, 5261A (lower frequency limit 1 MHz), 5262A, 5265A, 5257A.

10004B: 50Ω Probe Kit

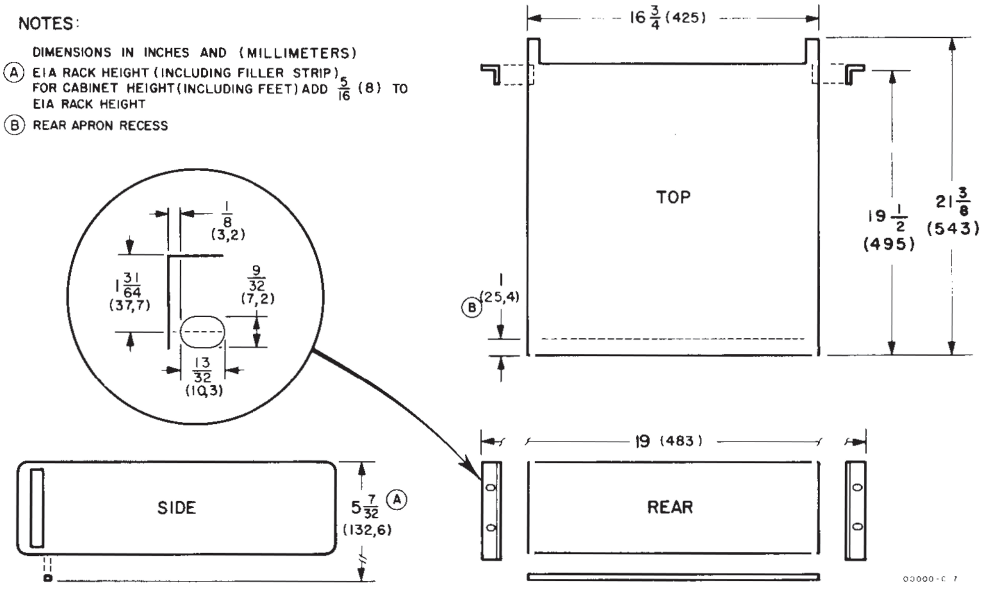
10020A: 10 MΩ Probe Kit

K15-59992A STANDBY POWER UNIT

Plug-in to maintain oscillator operation for prolonged periods without line voltage.

WEIGHT: 7.2 kg (3 lbs. 4 oz.) net

DIMENSIONS:



SECTION II

INSTALLATION AND REMOTE PROGRAMMING

2-1. INTRODUCTION

2-2. This section contains information for unpacking, inspection, storage, and installation. Also included in this section are the instructions for remote programming.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged, inspect the counter for visible damage (scratches, dents, etc.). If the counter is damaged, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (offices are listed at the back of this manual). Keep the shipping carton and packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

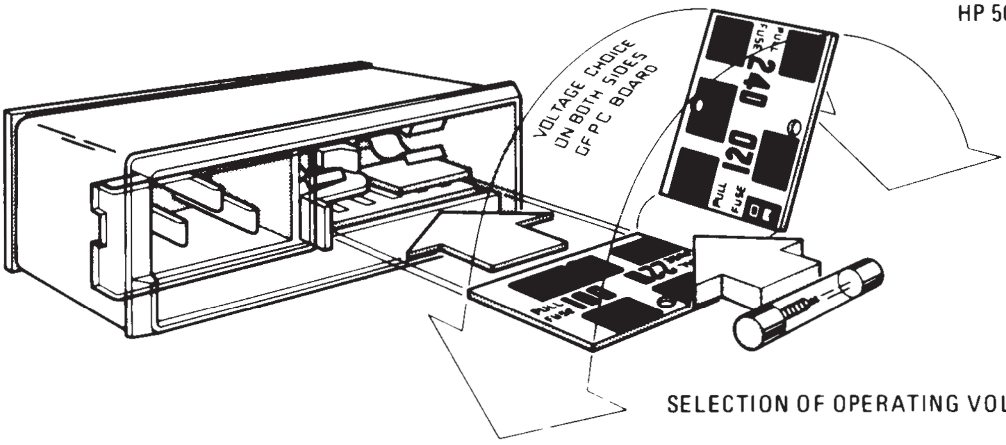
2-5. INSTALLATION REQUIREMENTS

CAUTION

BEFORE CONNECTING THE INSTRUMENT TO AC POWER LINES, BE SURE THAT THE VOLTAGE SELECTOR IS PROPERLY POSITIONED AS SHOWN IN THE FIGURE BELOW.

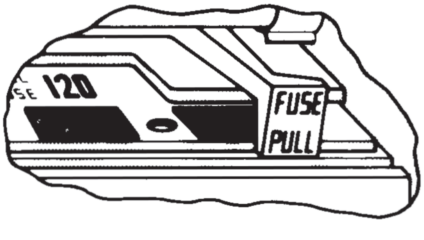
2-6. LINE VOLTAGE REQUIREMENTS. The 5345A is equipped with a printed-circuit line voltage selector to select 100, 120, 220, or 240-volt ac operation. Before applying power, the pc selector must be set to the correct position and the correct fuse must be installed as shown below. (Fuses are 100/120V, 2.5 AT; 220/240V, 1.25 AT.)

PC BOARD PART NUMBER IS
HP 5020-8122



SELECTION OF OPERATING VOLTAGE

Operating voltage is shown in module window.



1. Open cover door and rotate fuse-pull to left.
2. Select operating voltage by orienting PC board to position desired voltage on top-left side. Push board firmly into module slot.
3. Rotate fuse-pull back into normal position and re-insert fuse in holders, using cautions to select correct fuse value.

2-7. LINE FREQUENCY REQUIREMENTS. The counter operates at line frequencies between 48 Hz and 66 Hz.

2-8. THREE CONDUCTOR POWER CABLE. To protect the operator, the counter uses a grounded three-conductor detachable power cable. The male connector end is a NEMA type connector, and the female connector end is a C.E.E. type connector that mates with the 5345A rear panel power connector. Connect the power cable to a power source receptacle with a NEMA grounded third conductor. If the line power receptacle is a standard two-pin type instead of the NEMA three-pin receptacle, use a two-to-three pin adaptor (HP Part No. 1251-0048) and connect the green pigtail on the adaptor to ground.

2-9. REPACKING FOR SHIPMENT

2-10. If it becomes necessary to reship the counter, good commercial packing should be used. Contract packaging companies in many cities can provide dependable custom packaging on short notice. Instruments should be packed securely in a strong corrugated container (350 lb/sq. in bursting test) with suitable filler pads between the instrument and container. *The 4-corner support is not adequate, counter must also have center support.* Before returning instruments to Hewlett-Packard, contact the nearest Hewlett-Packard Sales and Service Office for instructions.

2-11. ENVIRONMENT DURING STORAGE AND SHIPMENT

2-12. Conditions during storage and shipment should normally be limited as follows:

a. Maximum altitude: 25,000 feet

b. Minimum temperature: -40°F (-40°C).

c. Maximum temperature: +167°F (+75°C).

2-13. REMOTE PROGRAMMING AND DIGITAL OUTPUT (OPTIONS 010 AND 011)

2-14. Option 011 adds remote programming and digital output capability to the 5345A Electronic Counter. Option 010 provides digital output capability only; no provision is made to program the front panel control functions. The following paragraphs apply to Option 011 and to Option 010 except for the remote programming codes, listen function and as specified. Programming is accomplished with a bi-directional bus, via a 24-pin connector on the rear panel. Associated with this connector are five slide switches used to address the instrument. A 5345A can be addressed to send output data (TALK) (Options 010 and 011) or to accept program information (LISTEN) (Option 011 only). Several HP-IB terms are defined as follows:

a. A TALKER sends information to the bus.

b. A LISTENER receives information from the bus.

c. A CONTROLLER is an instrument that has the responsibility of managing the instruments connected to the bus. It is capable of addressing other instruments on the bus as TALKERS or as LISTENERS. It is a TALKER and may be a LISTENER.

d. "High" or "0" level of a line or switch is the relatively more positive signal level (≥2.4 V).

e. "Low" or "1" level of a line or switch is the relatively less positive signal level (≤0.4 V).

2-15. Bus Description

2-16. The 15-line bus consists of 8 data lines, 3 transfer lines, plus 4 control and status lines. Addresses, program and output information are communicated on the *data* lines. These are based on a character-serial, seven-bit ASCII code set.

2-17. The 15 HP Interface Bus lines can be categorized into three groups by the job they perform.

a. **Data lines:** DIO1 through DIO8

Data lines (DIO1-DIO8) are used for transferring data from one instrument to another on the bus. They accommodate the 7 bits of the widely used ASCII code, leaving one bit that is not used. This line is permanently terminated in the 5345A.

b. **Transfer lines:** DAV = Data Valid. NDAC = Not Data Accepted. NRFD = Not Ready for Data.

Transfer lines DAV, NDAC, and NRFD must interact in the proper time sequence before complete communication between instruments is established. During the "three-wire transfer" a byte of data is transferred on the DIO lines.

c. **Control and Status lines:** ATN = Attention. REN = Remote Enable. IFC = Interface Clear. SRQ = Service Request.

Control and Status lines ATN, REN, and IFC are used by the controller to supervise and control the bus. Instruments on the bus use SRQ (Service Request) to inform the controller they have completed a measurement and are ready to output data.

2-18. Several 5345A's can be connected to a common bus. The exact number depends on the drive capability of the controller (see LINE CHARACTERISTICS). A specific 5345A is made to send output data (TALK) or accept program data (LISTEN) by addressing it to do so. Option 010 can be addressed to talk only.

2-19. All bus lines have been given names and mnemonic acronyms that convey the message being carried on that line. Each line is described below, followed by a table listing the relationship of the Attention and the three transfer lines. Also a figure is included showing the signal levels and timing relationship of the transfer and data lines. *ALL INSTRUMENTS CONNECTED TO THE BUS, INCLUDING THE CONTROLLER, MUST OBEY THESE DESCRIPTIONS.*

a. SERVICE REQUEST (SRQ)

For Option 011, when SRQ is set low the 5345A indicates to the controller that it has completed a measurement and is ready to output. It drives SRQ only if the 5345A output mode is programmed to "wait until address." When programmed in the other output mode "output ONLY IF addressed," the 5345A sets SRQ high at all times. When SRQ is high, service is not being requested. Option 010 has SRQ set high permanently.

Option 012 only. When enabled to Serial Poll, the 5345A will handshake out one status word. This word will be ASCII @ if the 5345A has enabled service request (SRQ) and will be an ASCII (NUL) if it has not enabled SRQ. This is the standard format for serial polling when SRQ is polled. The condition for removing SRQ is to:

1. Serial Poll.
2. Address the 5345A to Output.

For Option 011 and 012, if two or more 5345A's are connected to the bus and one of them sets SRQ low, the controller must go through a process of elimination to determine which one has requested service. It does this by sequentially addressing each one to TALK. Only the 5345A with output information will respond.

b. SERIAL POLLING

The 5345A responds to the universal commands Serial Poll Enable (SPE) and Serial Poll Disable (SPD). To serial poll the 5345A:

1. Send the Serial Poll Enable universal command ASCII (CAN).
2. Send the 5345A talk address that corresponds to the address switch setting."

c. REMOTE ENABLE (REN) (OPTION 011 ONLY)

REN can be used by a controller to select remote or local (front panel) control of the operation of a 5345A. It works in conjunction with the information stored in the local-remote program storage cell (see paragraph 2-48 and Table 2-3). When REN is low and the 5345A has been sent an ASCII "E8" it will operate according to the information previously stored in its remote-local program storage cells. It operates according to its front panel controls for all other combinations of these, i.e., REN is low and the remote-local storage cell contains an ASCII "E0" or when REN is high regardless of what is stored in the remote-local cell. ASCII "E0" is stored in the local-remote program storage cell when either the power is turned on or the RESET pushbutton is depressed.

d. INTERFACE CLEAR (IFC)

A controller uses IFC to clear the bus. When it sets IFC low, all 5345A's immediately stop driving the data lines (DIO1 through DIO7) and transfer lines (NRFD, NDAC, and DAV). IFC will not clear a 5345A's service request (SRQ). A controller may drive IFC low at any time. When IFC is high, it has no effect on the bus operation. The 5345A monitors IFC at all times.

e. ATTENTION (ATN)

ATN is used by a controller to address a 5345A. The 5345A monitors ATN at all times. When ATN is low, all 5345A's connected to the bus interpret the information on the data lines as an address.

When ATN is high, a 5345A that has been addressed to TALK will drive the data lines. Those that have been addressed to LISTEN will interpret the information on the data lines as data. Those that have not been addressed will not drive the data lines.

f. DATA LINES (EIGHT BITS DIO1, DIO2...DIO8)

DIO1 through DIO7 carry data between the 5345A and its controller. The 5345A drives these lines when it has been addressed to TALK. The 5345A receives information on the data lines when ATN is low and it has been addressed to LISTEN. DIO8 is permanently terminated in the 5345A.

When a DIO line is high, the data bit is a logic zero (0).

When a DIO line is low, the data bit is a logic one (1).

g. NOT READY FOR DATA (NRFD)

NRFD is the transfer line that indicates listeners are ready to accept information on the data lines. Its relationship to the other transfer lines and ATN is shown in Figure 2-1 and Table 2-1.

NRFD is driven by all listeners when ATN is low and those instruments addressed to listen when ATN is high. NRFD is sensed by talkers: the controller (talker) when ATN is low, and the instrument addressed to talk when ATN is high.

When NRFD is high, all listeners are unconditionally ready for data. The talker may then, at its own time, put a byte of information on the data lines and set DAV low. When NRFD is low, one or more listeners are not ready to data.

When the controller sets ATN low, all 5345A's will set NRFD high within 200 ns. When the controller sets ATN high, all 5345A's that have not been addressed to listen will not drive NRFD.

The listener must not set NRFD low until it senses DAV is low. It may do so before or at the same time that it sets NDAC high. It must not return NRFD high until it senses DAV is high and may do so before, or at the same time that it sets NDAC low.

h. NOT DATA ACCEPTED (NDAC)

NDAC is the transfer line that indicates the acceptance of information on the data lines. Its relationship to the other transfer lines and ATN is shown in Figure 2-1 and Table 2-1. NDAC is driven by all listeners when ATN is low and those instruments addressed to listen when ATN is high. It is sensed by talkers: the controller when ATN is low and the instrument addressed to talk when ATN is high.

When NDAC is high, all listeners have unconditionally accepted the byte of information on the data lines and no longer need it. The talker may then, at its own time, set DAV high, remove that byte of information and continue. When NDAC is low, one or more listeners have not accepted the information on the data lines.

DATA VALID (DAV)

DAV, a transfer line, indicates that an ASCII character already is placed on the data lines. Its relationship to the other transfer lines and ATN is shown in Figure 2-1 and Table 2-1.

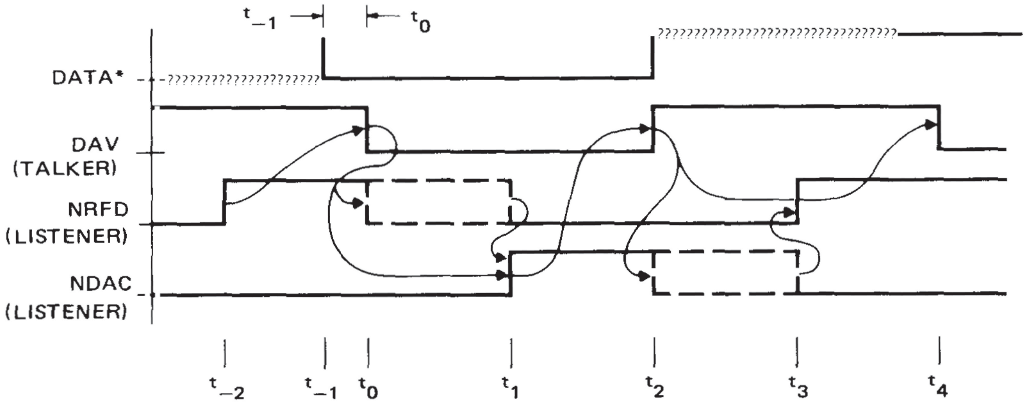
It is driven by talkers: the controller when ATN is low and by the instrument addressed to talk when ATN is high. It is sensed by listeners: all 5345A's if ATN is low and by the instruments addressed to listen when ATN is high.

When DAV is low, the states of data lines DIO1 through DIO7 are unconditionally valid and may be accepted by all listeners at their own time. DAV can be driven low only if NRFD and IFC are high. When DAV is high, the information on the data lines is not valid. DAV cannot be set high unless NDAC is high and NRFD is low.

Table 2-1. Relation of ATN and the Transfer Lines (NRFD, NDAC, DAV)

		NRFD		**NDAC**		**DAV**	
		LOW	HIGH	LOW	HIGH	LOW	HIGH
STATE OF ATTENTION (ATN) LINE	ADDRESS MODE LOW	One or more 5345A's not ready for data	All 5345A's are ready for data	One or more 5345A's has not accepted the data	All 5345A's have accepted the data	Controller has valid data on lines	Controller's data not valid
		(1) Driven by all 5345A's (2) Sensed by controller				(1) Driven by controller (2) Sensed by 5345A's	
	DATA MODE HIGH	One or more listeners are not ready for data	All addressed listeners are ready for data	One or more listeners have not accepted data	All addressed listeners have accepted the data	The addressed talker has valid data on lines	The addressed talker's data not valid
		(1) Driven by ALL instruments addressed to LISTEN (2) Sensed by the instrument addressed to TALK (3) All instruments not addressed will not drive				(1) Driven by the instruments addressed to TALK (2) Sensed by ALL instruments addressed to LISTEN	

SEQUENTIAL REQUIREMENTS OF THE THREE WIRE TRANSFER



EVENTS

t_{-2} : Listener becomes ready to accept data.

t_{-1} : Talker has put data on the lines.

t_0 : Indicates data is valid.

t_1 : Listener has accepted the data and no longer requires it held valid.

t_2 : Talker indicates the data is no longer valid and may change it.

t_3 : Listener indicates it is ready for new data.

t_4 : A new cycle begins (equivalent to t_0).

t_{-1} to t_0 : Time that data is put on lines before DAV is set low.

*A composite of the DIO1 through DIO7 lines for illustrative purposes.
(The curved lines indicate interlocked signal sequence.)

Figure 2-1. Transfer Timing

2-20. Data Transfer

2-21. Transfer of data on the bus is asynchronous. It places no restrictions on the data rates of instruments connected to the bus. The timing and levels required to transfer a byte of information on the data lines are shown in Figure 2-1. Transfer is under the control of three transfer lines DAV, NRFD, and NDAC. The talker (sender of data) drives DAV (Data Valid), and the listener (acceptor of data) drives both NRFD and NDAC.

2-22. The transfer of a byte is initiated by the listener, signifying it is ready for data by setting NRFD high. When the talker recognizes NRFD is high and has placed valid data on the data lines, it sets DAV low. When the listener senses that DAV is low and is finished using the data, it sets NDAC high. Since all instruments on the bus have their corresponding lines connected together (e.g., NRFD), all listeners must be in a high state before that lines goes high. This wire-AND situation allows a talker to recognize when the slowest listener has accepted a byte of data and is ready for the next byte.

2-23. What Can Be Programmed

2-24. For Option 011, all front and rear panel switch functions, except those on the input amplifier, are programmable. In addition, a controller can command the 5345A to make a measurement by sending a "Take a Measurement" instruction. The controller can elect to give control to the front panel controls (LOCAL) or have the 5345A operate according to the information stored in its remote program storage cells (REMOTE). These are listed in Table 2-3 along with their associated codes. Option 010 has no provision to remotely program the front panel functions.

2-25. Output Format

2-26. When addressed to output, the 5345A sends a space or minus, up to 11 digits of data, decimal point, the multiplier to make the reading (mHz, Hz, kHz, MHz, GHz, or ksec, sec, msec, μsec, nsec, and carriage return linefeed. These alpha-numeric characters are coded per the USA Standard code for Information Interchange (ASCII). When programming manual display all factitious (filler) digits are output as zeros (see paragraph 3-57).

2-27. Addressing the 5345A

2-28. Before a 5345A can send output data or accept program information it *MUST* be addressed to TALK or LISTEN. The method used to address it depends on the rear panel switch marked TALK ONLY — ADDRESSABLE (see Figure 2-2). When in the TALK ONLY position, the 5345A is addressed to TALK - it outputs ONLY. It operates according to the front panel controls and outputs each measurement. This position is intended for operation where there is no controller, e.g., with a digital recorder. When the rear panel switch is set to ADDRESSABLE, the 5345A can either be:

a. Sent program information by a controller and the measured results are observed visually, or

b. Both program and output information are passed on the bus, managed by a controller.

2-29. The thirty-one (31) LISTEN, sixteen (16) TALK, and fifteen (15) COMPUTER DUMP address characters and their signal levels are shown in Table 2-2. A unique character is selected for each 5345A with the four (4) slide switches on the rear panel marked ADDRESS (A5, A4, A3, A2). These switches may be set to either 0 or 1 (0 represents a high level and 1 a low level).

2-30. Two characters are reserved for the special function of clearing or removing a 5345A from the active state of an addressed talker or listener. The 5345A is cleared as a listener if it is sent an ASCII "?" while ATN is low. The 5345A is cleared as a talker if another instrument is addressed to talk or it is sent an ASCII "_" while ATN is low. It is cleared as either a talker or listener when IFC is low.

2-31. Addresses are communicated on the data lines. When the controller sets ATN low, all 5345A's interpret the information on data lines DIO1 through DIO5 as an address. During this time, the signal levels on DIO6 and DIO7 designate whether the addressed 5345A is to communicate as a talker or a listener.

DIO 7	DIO 6	DIO 5	DIO 4	DIO 3	DIO 2	DIO 1	
1	0	A_5	A_4	A_3	A_2	0	- TALK ADDRESS*
0	1	A_5	A_4	A_3	A_2	0	- LISTEN ADDRESS*
0	0	X	X	X	X	X	- Ignored by 5345A
1	1	X	X	X	X	X	when ATN is low

A_n - Address switches on rear panel

X - Don't care

* - The clear address characters (11111) not allowed.

NOTE

When the 5345A is addressed from a listener to a talker or talker to a listener, the appropriate clear codes ("?" or "_") must be issued. If underscore is not available, address a nonexistent talker.

2-32. Computer Dump

2-33. The 5345A has two discrete output modes. It has a talk mode and a computer dump mode. The computer dump output mode is used when it is desired to output 5345A readings (via Option 011) at extremely fast rates or to analyze raw measurement data. 5000 readings a second can be acquired in this mode. NOTE: Computer dump is not operatable with Option 010.

2-34. When the 5345A is addressed to output in this mode, it will output the contents of the denominator register and then output the numerator register contents. The processing and display cycles within the 5345A are bypassed with this mode. Computer dump is normally used when a computer is available with which to compute the measurement. The SAMPLE RATE (wait time between measurements) is <1μs in computer dump.

2-35. Computer Dump Format

2-36. A total of 32 ASCII digits are outputed in this mode with no CR (carriage return) or LF (line feed). Sixteen digits from the denominator register and 16 from the numerator. The counter outputs from the least to the most significant digits from the denominator followed with same order from the numerator. Contents for measurements are time for the numerator register and events for the denominator register. Count per unit time is equal to the internal clock frequency of 2 nsec.

2-37. Example: Denominator Register

MSD LSD
D D D D D D D D D D D D D D D D
————data flow————→

Numerator Register:

MSD LSD
D D D D D D D D D D D D D D D D
————data flow————→

2-38. The 5345A will continue to output in this mode each time a reading is taken until such time it is unaddressed.

2-39. Computer Dump Programming

2-40. Table 2-2 shows all talk and computer dump codes. Note that the computer dump program code is always one-bit greater than the talk code.

Example:

ASCII CODE							
TALK		ADDRESS					
B7	B6	B5	B4	B3	B2	B1	
1	0	X	X	X	X	0	- TALK OUTPUT MODE
1	0	X	X	X	X	1	- COMPUTER DUMP OUTPUT MODE

Table 2-2. Talk and Listen Addresses

USA STANDARD CODE FOR INFORMATION INTERCHANGE

BITS				b7 → b6 → b5 →	000	001	010	011	100	101	110	111
b4 ↓	b3 ↓	b2 ↓	b1 ↓	COLUMN → ↓ ROW	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	¦
1	1	0	1	13	CR	GS	–	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	—	o	DEL

LISTEN TALK

COMPUTER DUMP OUTPUT CODES ONLY.
CANNOT BE USED AS TALK OUTPUT CODES.

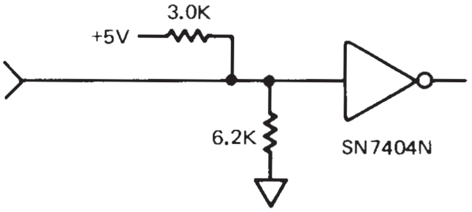
NOTES: ? = CLEAR LISTEN

— = CLEAR TALK

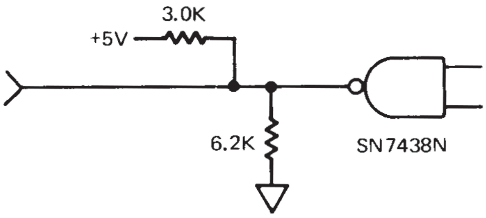
2-41. Line Characteristics

2-42. All 15 bus lines are designed to be compatible with TTL or DTL integrated circuits. Because wire-ANDing is used on some lines, the TTL line drivers must be either open collector or tri-state. Each line in the 5345A is terminated in a resistor divider consisting of a 3K connected to 5V and a 6.2K connected to ground. All receivers are hex inverters (SN 7404N or equivalent) and the drivers are open collector NAND gates (SN 7438N or equivalent). These may be put into four groups:

a. IFC, ATN, and REN are receivers only. They require -3.2 mA max. at 0.4V to drive.



b. SQR is output only: It is capable of sinking 45 mA at +0.4V.



c. Data lines (DIO1 through DIO7) and the transfer lines (NRFD, NDAC, and DAV) are bi-directional. They are a combination of a and b, i.e., when a talker, capable of sinking 45 mA at 0.4V; when a listener, requires -3.2 mA at 0.4V to drive.

d. DIO8 is connected to a similar divider and is always at 3.2V at 2K impedance.

2-43. Hardware

2-44. The 5345A digital INPUT/OUTPUT connector is on the rear panel (Figure 2-2). Pin connections to this Type 57 Microribbon connector are shown in Figure 2-3.

2-45. Cables of three different lengths are available for connecting a 5345A to a controller or another 5345A:

a. 3 feet long HP Part No. 10631A.
b. 6 feet long HP Part No. 10631B.
c. 12 feet long HP Part No. 10631C.

2-46. These have one overall shield to reduce susceptibility to external noise. The cables use a mixture of individual wires and twisted pairs to reduce crosstalk. Both ends are identical. They are terminated in two 24-pin piggy back connectors: one male and one female. This termination permits several cables to be connected to the same 5345A. Pin connections of these connectors are shown in Figure 2-4. There is a restriction of no more than 12-feet between the first two instruments in the system and 6-feet between the remaining instruments. The 5345A can drive a maximum of 50-feet of this cable.

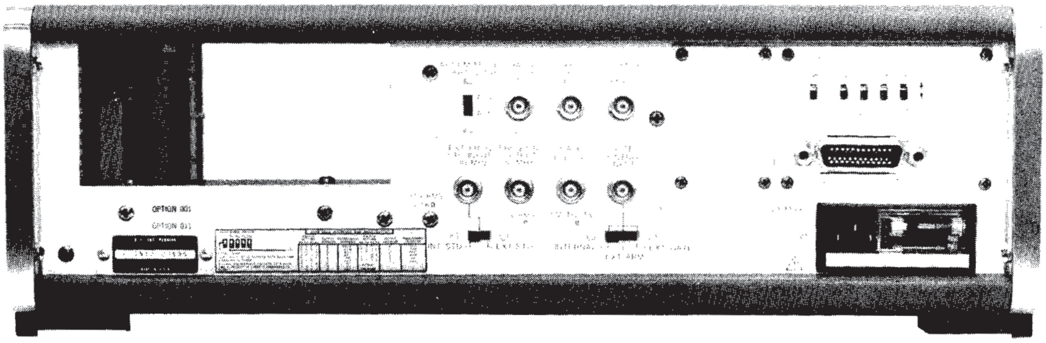


Figure 2-2. 5345A Rear Panel

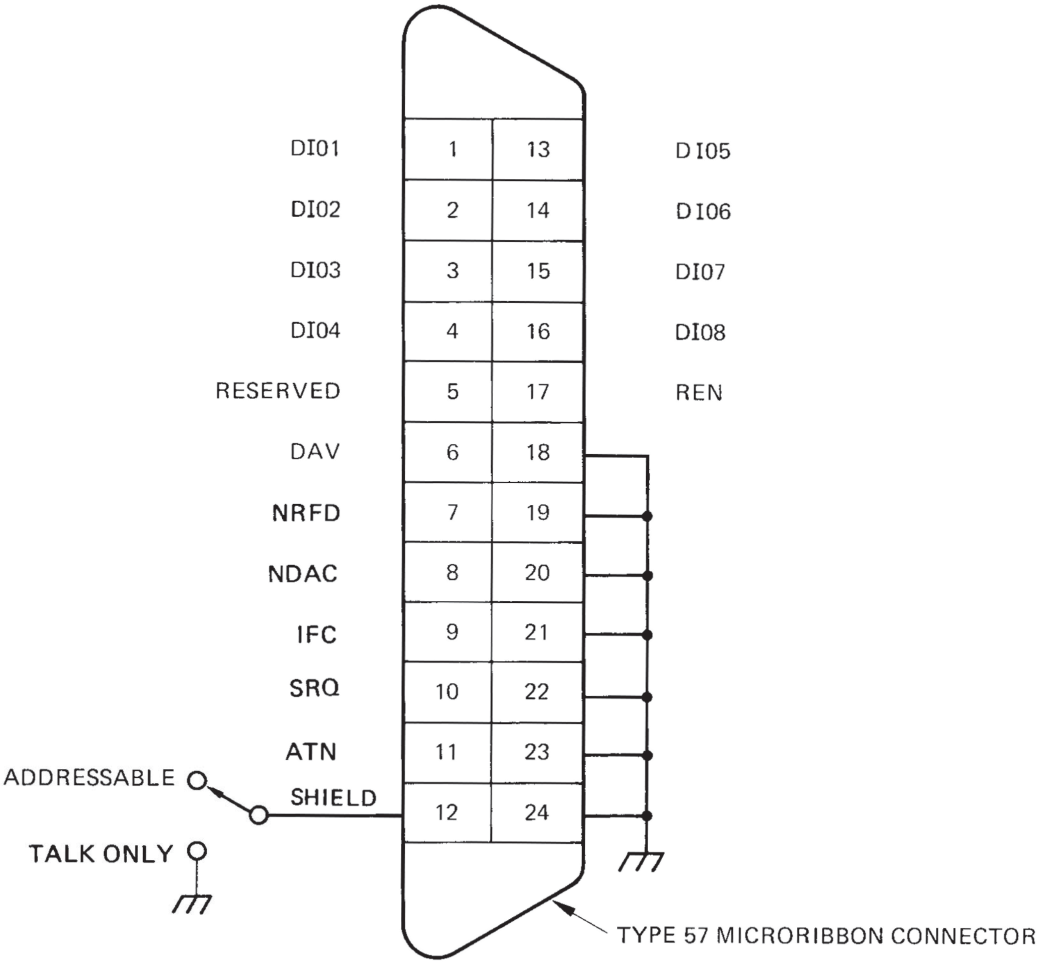
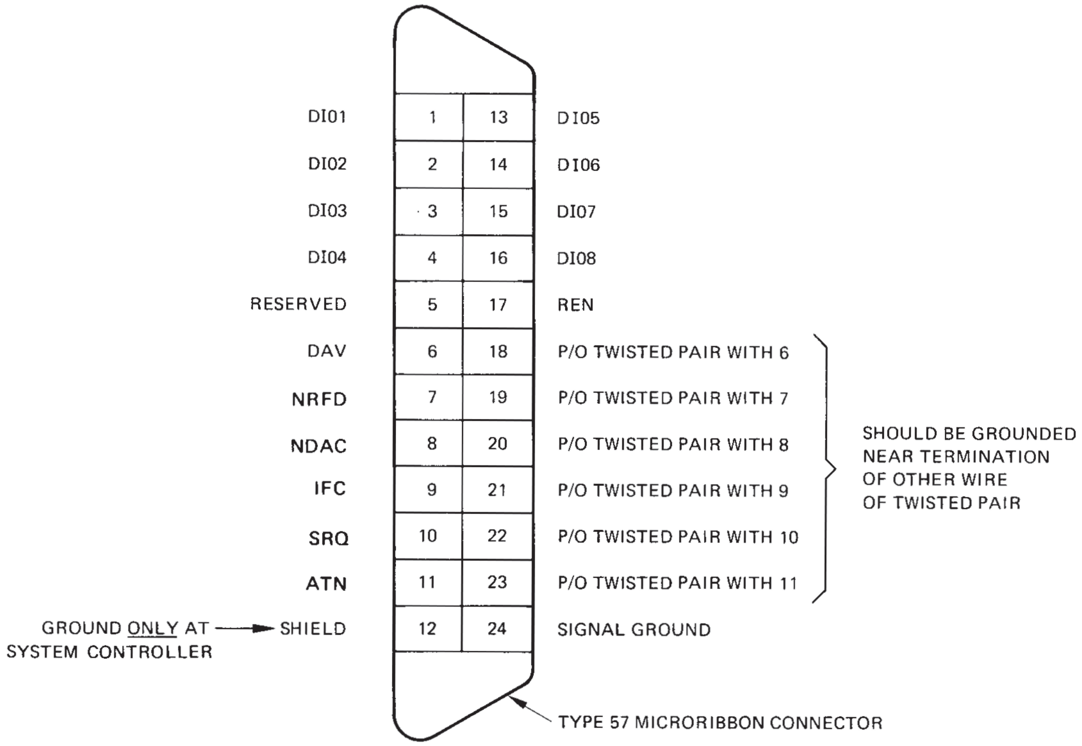


Figure 2-3. 5345A Digital Input/Output



NOTE 1: Pins 18 through 23 should be grounded near the termination of the other wire of its twisted pair. Pin 12 is grounded ONLY at the controller.

Figure 2-4. Pin Connections of the 10631A, B, C Cables

2-47. Programming the 5345A (Option 011 Only)

2-48. The 5345A has a group of storage cells that are used to store program information. They are used ONLY when a controller has the 5345A operating under remote control. The ASCII characters that can be stored in each cell and their relationship to the 5345A's operation are shown in Table 2-3. (Refer to Table 2-2 for signal levels.)

Table 2-3. Program Code Set, Option 011

1. **Function**	**ASCII**	**OCTAL***
a. Plug In	F2	106062
b. Frequency A	F0	106060
c. Period	F1	106061
d. Time Interval A to B	F3	106063
e. Ratio B/A	F5	106065
f. Start	F4	106064
g. Stop	F6	106066

2. **Accum Mode Start/Stop (If F4 or F6)**		
a. A+B	E=	105075
b. A-B	E5	105065

3. **Remote Gating**		
a. External Gate	E;	105073
b. Internal Gate	E3	105063

4. **Gate Time**		
a. 10000 sec	G4	107064
b. 1000 sec	G3	107063
c. 100 sec	G2	107062
d. 10 sec	G1	107061
e. 1 sec	G0	107060
f. 100 ms	G?	107077
g. 10 ms	G>	107076
h. 1 ms	G=	107075
i. 100 μs	G<	107074
j. 10 μs	G;	107073
k. 1 μs	G:	107072
l. 100 nsec	G9	107071
m. Min	G5	107065

5. **Input Amplifier Control**		
a. COM A or Separate	E7	105067
b. Check	E?	105077

6. **Sample Rate Selection**		
a. Maximum Sample Rate (~100 msec)	E1E4	105061 105064
b. Minimum Time (1-5 msec)	E1E<	105061 105074
c. HOLD	E9	105071

7. **Output Mode**	**ASCII**	**OCTAL***
a. ONLY IF Addressed	E2	105062
b. WAIT Until Addressed	E:	105072

(See NOTE following paragraph 2-50.h.2)

8. **Display Position**
(Digits from E in Data String)
(Digit Position Defined from Right to Left, Decimal Point on Right Side of Digit)

a. 0 Digits	D;	104073
b. 1 Digit	D:	104072
c. 2 Digits	D9	104071
d. 3 Digits	D8	104070
e. 4 Digits	D?	104077
f. 5 Digits	D>	104076
g. 6 Digits	D=	104075
h. 7 Digits	D<	104074
i. 8 Digits	D3	104063
j. 9 Digits	D2	104062
k. 10 Digits	D1	104061
l. Auto Position + Auto Suffix Multiplier	D0	104060

9. **Display Multiplier Suffix (If other than D0)**

FREQ.	**PERIOD/ TIME INTERVAL**	**START/ RATIO**	**ASCII**	**OCTAL***
GHz	nsec	G	C7	103067
MHz	μsec	M	C6	103066
kHz	msec	k	C5	103065
Hz	sec		C4	103064
mHz	ksec		C3	103063

	ASCII	**OCTAL***
10. **Remote Program Initialize**	I2	111062
11. **Local — Remote**		
a. Switch to Local	E0	105060
b. Switch to Remote	E8	105070
12. **Reset Command** (End of 100 ms reset pulse initiates measurement cycle)	I1	111061
13. **Sample Trigger Command (If E9)**	J1	112061

RESET PUSHBUTTON/POWER UP/I2 PROGRAM conditions are F0, G0, D0, E7, E0, E2, E3, E1, E4, E5

*The Octal listings are given to aid in troubleshooting.

2-49. The program storage cells are loaded with a predetermined set of conditions when either the front panel RESET pushbutton is depressed, power is turned on, or the special program code (Remote Program Initialize) I2 is issued. The initial conditions are listed in Table 2-3 under RESET PUSHBUTTON/POWER UP I2. Notice that each time either the RESET pushbutton is depressed, power is turned OFF - then ON, or program code I2 is issued, the 5345A operates according to its front panel controls.

2-50. Program Function Descriptions (Option 011 Only)

a. Function and Gate - Related directly to the front panel controls. For example, ASCII "F0" and ASCII "G0" select Frequency A function and 1 second gate time, respectively.

b. Display - The auto position (ASCII "D0") will normally be programmed. This positions the display's least-significant digit in the right most column with the correct Display Multiplier automically selected. Programming the display multiplier is not required in Auto Display. Manual display programming of 0 digits to 10 digits shifts the decimal point, hence the display, one place left for each programmed code. Manual requires a multiplier suffix to be programmed.

c. Display Multiplier Suffix - Used only when Manual Display has been programmed. Selects the correct unit of time or frequency.

d. RESET (I1) - The reset command causes the current measurement cycle to be terminated and a new cycle to begin (i.e., it also acts as a sample trigger). After sending any new programming codes, I1 must terminate the code string to ensure that a measurement cycle is begun using the new codes. If I1 is given when the counter is in the WAIT until addressed mode (E:), the counter will immediately go to an output cycle and output all zeros. Only when the output is complete and sample trigger occurs will a new measurement begin. Hence, under these conditions, the first reading into the calculator (consisting of all zeros) must be discarded.

e. Remote Program Initilize Instruction I2 - Sets the remote program storage cells to the initial conditions of instrument power up or front panel reset. The stored program is F0, G0, D0, E7, E0, E2, E3, E1, E4, E5. They are:

F0 - Frequency A
G0 - 1 sec gate time
D0 - Auto display position
E7 - COM A or Separate (depending on front panel position)
E0 - Local operation
E2 - Output only if addressed to talk
E3 - Internal gate
E1 - Sample rate not hold
E4 - Sample rate ≃ 50 msec time
E5 - A-B Start mode

When taking control of the 5345A it is necessary to change only those storage cells that are different from the above. For example, if the 5345A is to be used under remote control for a period measurement at 100 msec gate time it is only necessary to change the ASCII "F0" and "G0" to ASCII "F1" and "G?", respectively.

f. Input Amplifier Control

1. COM A or Separate (E7) - This programs the position of the COM A and SEP Switch on the front panel. Example: If program code E7 is issued and the Input Amplifier Control siwtch is set to COM A position, COM A will be selected. If, however, the front panel switch was set to SEP, then Separate is selected.

2. Check (E?) - This program selects the front panel check mode. The check mode is always selected regardless of Input Amplifier Control positions.

g. Local-Remote

1. Local - The 5345A operates according to its front panel controls.
2. Remote - Used in conjunction with the control line REN (Remote Enable) to have the 5345A operate according to the information in its program storage cells.

h. Output Modes - A 5345A outputs in one of two modes, providing it has been addressed to TALK.

1. ONLY IF addressed (ASCII "E2" stored in the program storage cell). The 5345A will output each measurement if it has been addressed to TALK. If not so addressed, it bypasses the entire output phase of its operating cycle.
2. WAIT until addressed (ASCII "E:" stored in the program storage cell). The 5345A will make a measurement, then wait in the output phase of its operating cycle until it is addressed to TALK. When waiting in the output phase, the 5345A display will be blank. As soon as it is so addressed, it will output and continue according to the information in its program storage cells.

NOTE

The output routine will be bypassed in the WAIT mode (ASCII characters E:) if the bus is in the DATA MODE with no listeners. This is a feature of the 5345A counter which prevents counter hang-up if the HP-IB cable is detached.

Notice that the 5345A ALWAYS outputs when it reaches the output phase of its operating cycle IF it has been addressed to TALK. When programmed ONLY IF, the 5345A continues to go through its operating cycle, bypassing the output phase until addressed to TALK. When programmed to WAIT, the 5345A will stop at its output phase and stay there until addressed to TALK.

i. Remote Gating

1. External Gate ("E;"). Selects EXT GATE position of Gate Control switch for control of gate circuits.
2. Internal ("E3"). Selects INTERNAL position of Gate Control switch, allowing normal operation of the counter.

j. Sample Rate Selection - The programmed sample rate determines the "wait time" between measurements. This is the time from the end of processing to the time the counter is armed for the next measurement.

1. Maximum Sample Rate (E1E4). Equivalent to selecting the maximum sample rate with the front panel sample rate control. This results in a wait time of 50 to 100 msec.
2. Minimum Time (E1E<). This results in the fastest repetitive measurement cycles possible since the sample rate portion of the measurement cycle is effectively bypassed. For normal talk mode, the wait time in this mode is <100 μsec plus the 1 to 5 msec processing time. For the unprocessed format talk mode (computer dump), the time is <1 μsec plus the output time of 107 μsec into an infinitely fast receiver.

NOTE

In Minimum mode, the counter display will be blank. If E1 has been previously programmed, only E4 or E< must be sent.

3. HOLD (E9). The counter will wait until a Sample Trigger Command (J1) occurs and then the measurement cycle begins.

k. ACCUM MODE START/STOP - Used when totalizing two input signals:

1. A+B (E=). Counts of each channel are added for the total displayed count.
2. A-B (E5). B counts are subtracted from Channel A counts.

2-50a. Program Codes and Universal Commands for Option 012

2-50b. Tables 2-4 and 2-5 list the program codes and universal commands for the Remote Programming Option 012.

Table 2-4. Program Code Set for 5345A Option 012

1. Function

		ASCII
a.	Plug-In	F2
b.	Frequency A	**F0**
c.	Period	F1
d.	Time Interval A to B	F3
e.	Ratio B/A	F5
f.	Start	F4
g.	Stop	F6

2. Gate Time

a.	10000 sec	G4
b.	1000 sec	G3
c.	100 sec	G2
d.	10 sec	G1
e.	1 sec	**G0**
f.	100 ms	G?
g.	10 ms	G>
h.	1 ms	G=
i.	100 μs	G< or G≤*
j.	10 μs	G;
k.	1 μs	G:
l.	100 nsec	G9
m.	Min	G5

3A. Display Position

(Digits from E in Data String) (Digit Position Defined from Right to Left, Decimal Point on Right Side of Digit)

a.	0 Digits	D;
b.	1 Digit	D:
c.	2 Digits	D9
d.	3 Digits	D8
e.	4 Digits	D?
f.	5 Digits	D>
g.	6 Digits	D=
h.	7 Digits	D< or D≤*
i.	8 Digits	D3
j.	9 Digits	D2
k.	10 Digits	D1
l.	Auto Position + Auto Suffix Multiplier	**D0**

3B. Display Multiplier Suffix

FREQ.	PERIOD TIME INTERVAL	START/ RATIO	ASCII
GHz	nsec	G	C7
MHz	μsec	M	C6
kHz	msec	k	C5
Hz	sec		C4
mHz	ksec		C3

4. Reset

a.	Machine reset	I1
b.	Remote Program Initialize	I2

5. Input Amplifier Control

a.	COM A or Separate	**E7**
b.	Check	E?

6. Local-Remote

Selects remote upon addressing provided the bus line REN is assertive.

7. Output Mode

a.	Output only if addressed to Talk; bypass if not addressed to Talk	**E2**
b.	Hold current measurement until addressed to Talk	E:

NOTE

The output routine will be bypassed in the wait mode (ASCE:) if the bus is in the DATA MODE with no listeners. This is the result of a 5345A feature which prevents hang-up of the 5345A in the event the HP-IB cable is disconnected.

8. Remote Gating

a.	Enable Rear Panel External Gate	E;
b.	Disable Rear Panel External Gate	**E3**

9. Sample Rate

(Wait Time Between Measurements)

a.	Not Hold	**E1**
	1. Min Time (1-5 msec)	E< or E≤*
	2. ≈50 msec time (Required for Start Function)	**E4**
b.	Hold	E9
	1. Take a measurement	J1

10. Accum Mode Start/Stop

A+B	E=
A–B	**E5**

11. Slope

Slope B +	**E0****
Slope B –	E8**
Slope A +	E6
Slope A –	E>

12. Trigger Levels

Level A	ADDD
Level B	BDDD

D=ASCII Digit 0-9

NOTE

On power up, these levels are random.

$$\text{Trigger Level in Voltage} = \frac{DDD}{250} - 2.000 \text{ for } 000 \leq DDD \leq 999$$

AND

A Chan A:00 = +2.000
B Chan B:00 = +2.000

NOTE

These codes are useful when calibrating the DAC.

*For 9820A/9821A Calculators
**Codes have different function for Option 011

RESET PUSHBUTTON/POWER UP/I2 PROGRAM conditions are **F0, G0, D0, E7, E0, E2, E3, E1, E4, E5**

Table 2-5. Universal Commands for Model 5345A Option 012*

ASCII CHARACTER	OCTAL CODE	REMARKS	5345A RESONSE
SOH	001	(GTL) Go To Local Included	Causes instrument to return to local if addressed to Listen
BS	010	(GET) Group Execute Trigger	Causes instruments on the bus (that are addressed to listen) to execute their function
DC1	021	(LLO) LOCAL Lockout	Disables the LOCAL pushbutton on the front panel
DC4	024	(DCL) Device Clear	Causes instrument to reset, same as instruction I1
CAN	030	(SPE) Serial Poll Enable	Controller places the bus in the serial polling mode
EM	031	(SPD) Serial Poll Disable	Controller terminates the serial polling mode.
?	077	(UNL) Unlisten	Clears or removes all addressed listeners from the active state of being addressed
— (underscore)	137	(UNT) Untalk	Underscore is used to clear the addressed talker from the active state of being addressed

NOTE: For additional information refer to User Guide manuals for 9820A, 9821A Calculators (HP 59300-90001) and 9830A Calculator (HP 59300-90002).

2-51. Output Process

2-52. When addressed to TALK, the 5345A outputs according to the program (Local or Remote), provided there is an addressed listener on the bus. The transfer routine, necessary for passing information on the data lines, cannot be started unless there is both an addressed listener and talker on the bus. The listener must be able to recognize LF (line feed) as the end of the 5345A's output data. As soon as the listener accepts LF (sets NDAC high) the 5345A leaves the output phase and continues through its operating cycle.

2-53. The output characters, their description, and the order in which they are outputted are shown in Table 2-6.

Table 2-6. 5345A Output Code Set

ORDER OUTPUTTED	CHARACTER	DESCRIPTION
1	( ) or (–)	Normally a space, minus when B is greater than A in start function.
2	0–9	0 to 11 digits may be outputted depending on Gate Time selection, most-significant-digit first.
3	.	Decimal Point.
4	E	Exponent Multiplier.
5	+ or –	Sign of Exponent Multiplier.
6	0, 3, 6, or 9	Multiplier.
7	CR	Carriage Return.
8	LF	Line Feed (used as a word terminator).

2-54. Modes of Operation (Option 011 Only)

2-55. The 5345A has several remote operating modes. They depend on the Sample Rate and Output modes and the method used to initiate a measurement procedure. This section includes a description of these modes and sample programs.

2-56. The two principal modes of remote operation, based on the Sample Rate and Output modes, are described in (a) and (b) below. Modes (c) and (d) are possible by selecting the remaining combinations of the Sample Rate and Output modes.

a. Sample Rate NOT HOLD (E1) and Output ONLY IF E2

   1. If not addressed to talk, the 5345A continuously makes measurements at a rate determined by program codes "E<" or "E4" 1-5 msec or ≈ 50 msec, respectively plus measurement time. It skips the output phase of its operating cycle.
   2. If 5345A is addressed to TALK, it no longer skips its output phase. The next and all subsequent measurements are outputted.

b. Sample Rate HOLD (E9) and output mode WAIT until addressed (E:) the 5345A sequence is:

   1. Addressed to LISTEN.
   2. Instructed to make a measurement.
   3. Makes a measurement and stops in its output phase.
   4. Addressed to TALK.
   5. Outputs and stops in its Sample Rate phase.
   6. Addressed to LISTEN.
   7. Instructed to make measurement, then repeats 3 through 6.

c. Sample Rate NOT HOLD (E1) with (E<) or (E4) programmed and WAIT until addressed (E:) the 5345A:

   1. Makes a measurement and stops in its output phase.
   2. Is addressed to TALK.
   3. Outputs, goes through its sample rate, and makes another measurement and if:
      (a) Still addressed to TALK, it repeats 3.
      (b) Not addressed to TALK, it stops in its output phase and waits until so addressed, then repeats 3.

d. Sample Rate HOLD (E9) and Output ONLY IF addressed (E2) the 5345A is:

   1. Addressed to LISTEN.
   2. Instructed to make a measurement.
   3. Makes the measurement and if:
      (a) Addressed to TALK by the end of the measurement phase, it outputs and stops in the Sample Rate phase until 1 and 2 are repeated.
      (b) Not addressed to TALK by the end of the measurement phase, it skips output and stops in the Sample Rate phase until 1 and 2 are repeated.

2-57. Starting a Measurement Procedure (Option 011 Only)

2-58. When operating the 5345A under remote control, a measurement procedure may be initiated by sending a Reset or Take a Measurement Instruction or by letting the sample rate time run out.

a. Sample Rate NOT HOLD (E1) - a measurement starts at the end of sample rate time.
b. Reset Instruction (I1):

   1. Can be given at any time during a 5345A's operating cycle.
   2. Does not change the information in the program storage cells.
   3. Clears the display.
   4. Arms the counter.
   5. Starts measurement phase of the 5345A's operating cycle.

c. Take a Measurement Instruction (J1):

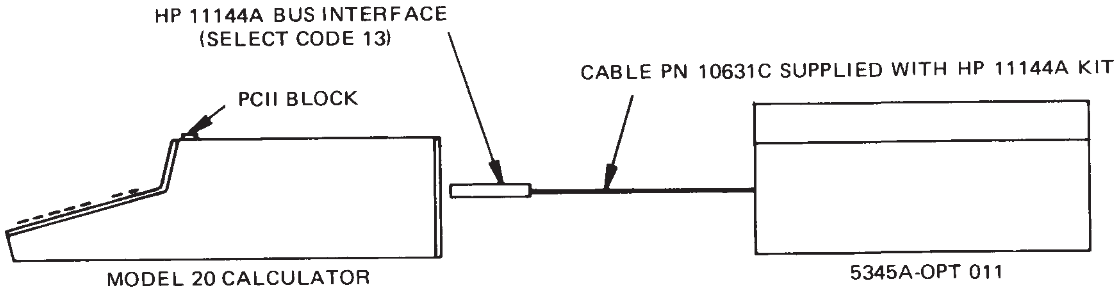
1. Can be given only if the 5345A is stopped in the Sample Rate phase of its operating cycle. If given at any other time it will be ignored by 5345A.
2. Does not change the information in the program storage cells.
3. Does not clear the display.
4. Starts the measurement phase of the 5345A's operating cycle.

2-59. Examples of Programming (Option 011 Only)

2-60. The following example shows 5345A and 9820A calculator programmed to instruct the counter to measure its 100 MHz check in a frequency mode at a 1-second gate time. The check frequency will also be recorded at 1-second intervals on the calculator printer.

Equipment Required:

Model 5345A Counter with Option 011.
Model 9820A Calculator with ASCII Bus Interface Model 11144A-020



NOTE

Set ASCII address switches on the rear panel of the 5345A to positions 1001. Set TALK ONLY/ADDRESSABLE switch to ADDRESSABLE.

2-61. LOADING THE PROGRAM. Prior to loading the program, push the END and EXECUTE keys. This positions the program counter to zero. Push the remaining keys in the program, as shown in the calculator key column of Table 2-7.

Table 2-7. Program Example

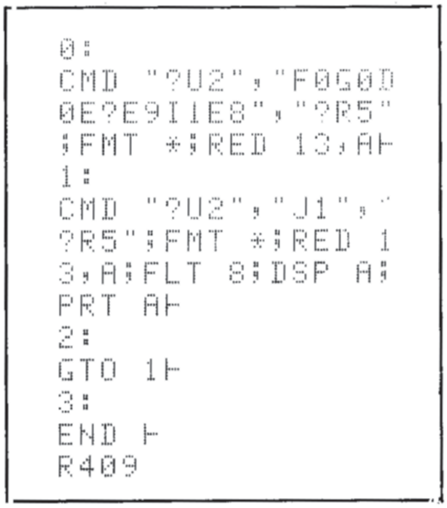
Program Line No.	Commands	Program Description (Function)	Calculator Key
0	CMD	Control statement. Refer to 11224A peripheral control II operating manual HP Part No. 09820-99024 Pg. 2-11.	Bus Command
0	"	First quotes following CMD statement specifies address mode.	"
0	?	Unaddresses all listeners on the Bus.	?
0	U	Calculator talker address.	U
0	2	5345A listen address, commands 5345A to listen.	2
0	"	Terminates address mode.	"
0	,	Delimiter between modes (address and data).	,
0	"	Second quote field specifies data program mode.	"
0	F0	Program code for frequency A (see 5345A program code sheet for all 5345A programming).	F 0
0	G0	Program for 1 sec gate time.	G 0
0	D0	Program for auto display position.	D 0
0	E?	Programs 100 MHz check.	E ?
0	E9	Programs sample rate to hold mode.	E 9
0	I1	Programs 5345A reset command. Resets previous reading, generates 100 ms reset pulse, and end of pulse initiates measurement cycle.	I 1

Table 2-7. Program Example (Continued)

Program Line No.	Commands	Program Description (Function)	Calculator Key
0	E8	Programs 5345A to remote mode.	E 8
0	"	Terminates data mode.	"
0	,	Delimiter between modes.	,
0	"	Specifies address mode.	"
0	?	Unaddresses all listeners on the bus.	?
0	R	5345A talk address commands 5345A to talk.	R
0	5	Calculator listen address commands, calculator to listen.	5
0	"	Terminates address mode.	"
0	;	End of statement delimiter which terminates bus command program.	;
0	FMT *	Defines free-field format, refer 11224A peripheral control II operating manual HP Part No. 09820-99024, Page 2-6.	Format *
0	;	End of statement delimiter.	;
0	RED 13,A	Reads data on the bus through the 11144A-020 calculator interface card to the "A" register in the calculator. See HP 11144A-020 manual for more information (the first reading due to I1 command is all zeros).	Read 1 3 , A
0	STORE	Stores program line 0 into calculator storage.	Store
1	CMD	Control statement. Refer to 11124A operating manual.	Bus Command
1	"	Specifies address mode.	"
1	?	Unaddress all listeners on the bus.	?
1	U	Calculator talker address commands calculator to talk.	U
1	2	5345A listen address, commands 5345A to listen.	2
1	"	Terminates address mode.	"
1	,	Delimiter between modes.	,
1	"	Specifies data program mode.	"
1	J1	Measure command to 5345A.	J 1
1	"	Terminates data mode.	"
1	,	Delimiter between modes.	,
1	"	Specifies address mode.	"
1	?	Unaddresses all listeners on the bus.	?
1	R	5345A talk address commands 5345A to talk.	R
1	5	Calculator listen address, commands calculator to listen.	5
1	"	Terminates address mode.	"
1	;	End of statement delimiter.	;
1	FMT *	Defines free-field format refer 11224A manual.	Format *
1	;	End of statement delimiter.	;
1	RED 13,A	Reads data on the bus through the 11224A-020 calculator interface card to the A register in the calculator (reads second and all successive readings to calculator A register).	Read 1 3 , A
1	;	End of statement delimiter.	;
1	FLT 8	Specifies eight digits to the right of the decimal point on the calculator display. (Refer to calculator operating and programming manual, HP Part 09820-99001, Page 5-11 for more information.)	Float N 8
1	;	End of statement delimiter.	;
1	DSP A	Places contents of "A" register into the display (in this example, 100 MHz check frequency).	Display A
1	;	End of statement delimiter.	;
1	PRT A	Prints contents of "A" register on calculator printer (100 MHz check).	Print A
1	STORE	Stores program line 1 into calculator storage.	Store
2	GO TO 1	Calculator program steps to program line 1 executes the program.	GO TO 1
2	STORE	Stores program line 2 into calculator storage.	Store
3	END	Ends program.	END
3	STORE	Stores program line 3 into calculator storage.	Store

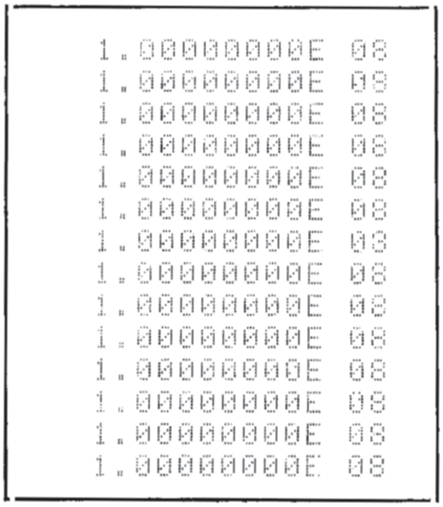
2-62. Calculator program with recorded output.

9820A Calculator Program Printer List



```
0:
CMD "?U2","F0G0D
0E?E9I1E8","?R5"
;FMT *;RED 13,A⊢
1:
CMD "?U2","J1","
?R5";FMT *;RED 1
3,A;FLT 8;DSP A;
PRT A⊢
2:
GTO 1⊢
3:
END ⊢
R409
```

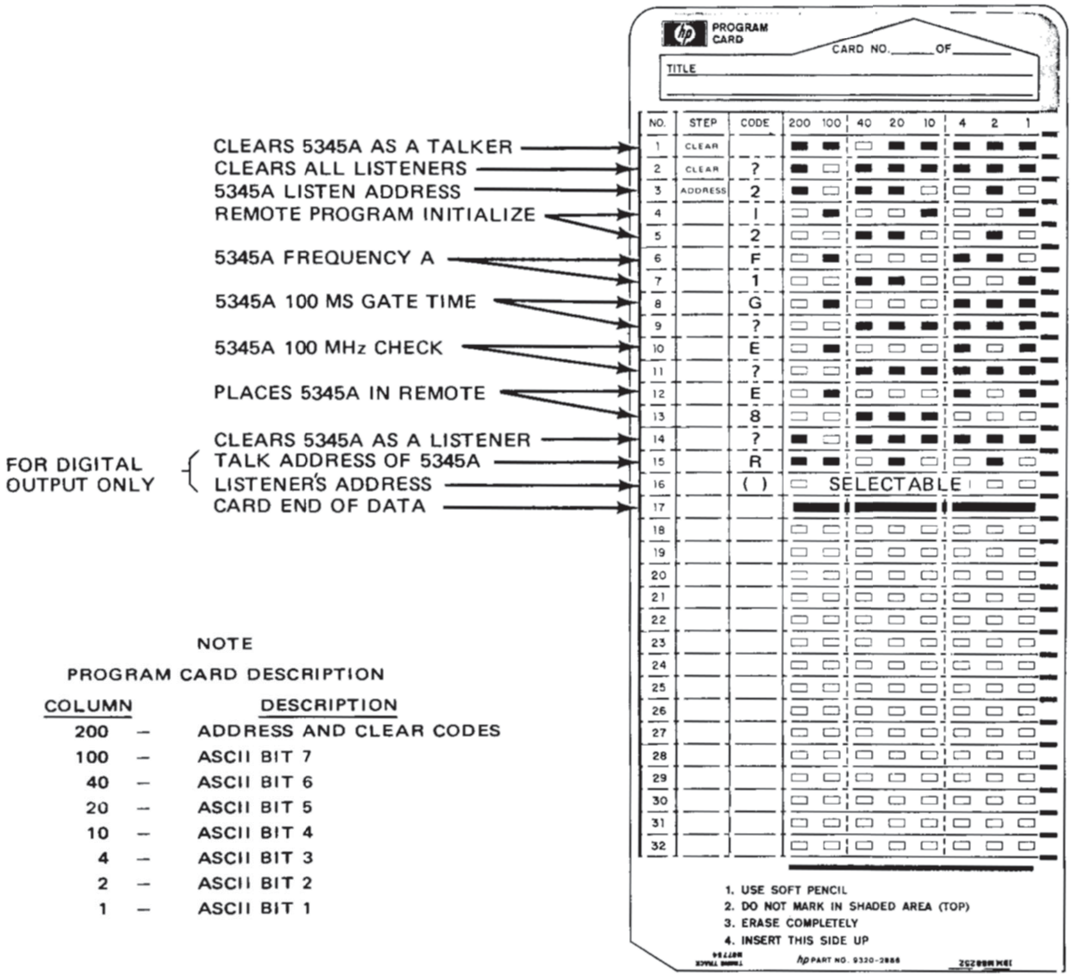
100 MHz Program Output



```
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
1.00000000E 08
```

2-63. VERIFYING THE PROGRAM. After the program has been loaded, push the END and LIST keys. This will run a printer list of the program. Check the list to verify that the program was entered correctly.

Example of Mark Sense Card Reader Program Card



NOTE

PROGRAM CARD DESCRIPTION

COLUMN		DESCRIPTION
200	–	ADDRESS AND CLEAR CODES
100	–	ASCII BIT 7
40	–	ASCII BIT 6
20	–	ASCII BIT 5
10	–	ASCII BIT 4
4	–	ASCII BIT 3
2	–	ASCII BIT 2
1	–	ASCII BIT 1

2-64. RUNNING THE PROGRAM. To run the program push the END and RUN PROGRAM keys. The program and printer continue to run until the STOP key is pushed. The printout should compare to the sample 100 MHz PROGRAM output shown above. This completes the test program.

2-65. Another example of programming is with a Hewlett-Packard Model 3260A Mark Sense Card Reader. Assume that it is desired to program a 5345A for a period measurement, 100 ms gate time, auto display position, and 100 MHz check. The Remote Program, Initialize Code I2 will be used in this example so only those program codes which differ from the initialize code will be issued. See previous page for example.

2-66. Option 012 Factory Installed Remote Programming

2-67. Option 012 provides all the features of Option 011, plus remote programming of the input amplifiers' slope and level controls. Option 012 also uses several universal commands, and responds and identifies to the serial polling.

2-68. Option 012 has two D/A converters that permit the reference voltage presented to the input amplifiers to be controlled in 4 mV steps from -2.0V to +1.3V. The input amplifier does *not* have a trigger accuracy of 4 mV with Option 012.

NOTE

Trigger level range is linear from -2.0V to +0.5V with 4 mV resolution.

2-69. Features

2-70. The following are special operating features of the Option 012:

a. Slope Control. The slope can be controlled externally.
b. Trigger Levels. The trigger levels are set sending a channel select code and three digits, as:
    ADDD
    or
    BDDD
    1. The actual trigger level will be:
    $$\frac{\text{DDD}}{250} - 2.000 \text{ volts}$$
    2. There is no defined power up state for the trigger levels.
    3. Trigger levels stabilize only when the last character is received from the Bus.
    4. Trigger level DAC's can be adjusted according to the procedure outlined in Table 5-6.
    5. A RESET code command (I1) should be sent to the counter after setting the DAC levels to prevent miscounts.

2-71. Special Programming Considerations (not in Option 011)

2-72. The following programming features must be considered when using Option 012:

a. SRQ Identified Serially.
b. Slope Controlled (must be Programmed).
c. Levels Controlled (must be Programmed).
d. LLO (Local-Lockout) Universal.
e. GTL (Go to Local) Universal Addressed.
f. DCL (Device Clear) Universal.
g. GET (Trigger) Universal Addressed.

h. All other codes same except E0, E8 which have different functions for Option 011.
i. Goes to Remote anytime the counter is addressed to listen.

NOTES

1. Counter should be RESET with I1 command anytime a program code is sent to the counter. The I1 command should be the last command sent, so as to prevent miscounts.
2. Slope and Trigger Level codes should be sent to the counter when first programming the counter after a power up of the counter.
3. Manual Trigger Level controls should be set to RESET position when in REMOTE control to prevent interference to the remote levels."

2-73. 5345A Option 011 with 9820A/21A Calculator Programming Summary

a. ADDRESS MODE SELECTION - Set the rear panel TALK ONLY—ADDRESSABLE switch as follows:
   1. To TALK ONLY if the 5345A is to operate according to its front panel controls and is to transfer measurement data to one or more listener devices on the bus.
   2. To ADDRESSABLE if the counter is to be addressed to talk or listen. In this mode, the counter can be remote programmed when addressed to listen and can send measurement data to the controller or other devices when addressed to talk.

b. ADDRESS ASSIGNMENT - In ADDRESSABLE, the counter's bus address is established by setting rear panel switches A5—A2 as shown in Table 2-8 on the next page. Each combination of switch positions results in a unique talk address, a unique unprocessed output format talk address (computer dump mode is the shaded talk address), and two listen addresses (the counter will respond to either one).

c. REMOTE OPERATION - To cause the counter to operate according to the program codes stored in the remote program cells, the bus must be in the Remote Enable state AND the counter must have been sent the ASCII code pair E8. To put the bus in the Remote Enable state, execute the statement: FMT Y3,Z; WRT 13. If the bus is in the Remote Disable state or if the ASCII local code E0 is stored in the counter, the counter will operate according to the front panel controls. To put the bus in the Remote Disable state, execute the statement: FMT Y4,Z; WRT 13. To switch to local if in remote, send the E0 code or push the reset button. (NOTE: The 9820A/9821A calculator powers up in the Remote Enable state.)

d. SETTING REMOTE PROGRAM CODES

Statement Format: CMD "ADDRESS STRING," "DATA STRING;"
Example: CMD "?U*," "I2E8E?G?I1"
Explanation: CMD is what the calculator displays when the BUS COMMAND key of PCII is pushed.

The first quote field defines the ADDRESS MODE of bus operation. The unlisten command (?) disables all listeners on the bus and should be first in the address string so as to avoid sending data to unwanted listeners which may have been previously addressed. The controller then designates itself as the talker (U) and designates the counter as the listener (*) (assuming counter address switches have been set for talk address of J, listen address of *). The calculator has a talk address of U and a listen address of 5 since the ASCII Bus Interface Card was preset to these codes before leaving the factory (see the ASCII Bus Interface Manual page 1-1). The second quote field defines the DATA MODE. One ASCII code pair from each of the 13 code groups shown in Table 2-3 may be selected. The ASCII characters are sent in a byte serial fashion from left to right in the statement. In the example, I2 causes the remote program initialize to be selected which causes the program storage cells of the counter to be initialized with the conditions: F0, G0, D0, E7, E0, E2, E3, E1, E4, E5. The codes after I2 make changes to the I2 conditions: E8 selects remote control, E? selects the check signal and G? selects a 100 msec gate time. Reset pulse I1 (100 ms) is sent to ensure start of a measurement cycle (at end of pulse) using the new program codes. Of course, the same result would have been obtained by sending "F0G?D0E?E8E2 E3E1E4E5I1."

e. SETTING REMOTE PROGRAM CODES USING 49 WRITE BYTE

Statement Format: CMD "ADDRESS STRING"; FMT Y2,Z; WRT 13; WTB 13, <register address>
Example: CMD "?U*; FMT Y2,Z; WRT 13; 70 → A; 49 → B; WTB 13, A; WTB 13, B
Explanation: It is sometimes useful to be able to send program codes which are the result of calculations in the program. This is most easily accomplished by using the WRITE BYTE key of PCII to send the decimal representation of an ASCII character. (Decimal equivalents of all the ASCII characters are given on page 2-8 of the PCII Operating Manual.) After the address information, the bus is put into the DATA MODE by executing FMT Y2,Z; WRT 13 (the bus may be put into the ADDRESS MODE by executing FMT Y1,Z; WRT 13). WTB 13,A writes out 70 (decimal equivalent to ASCII "F"). WTB 13, B writes out 49 (decimal equivalent to ASCII "1") onto the bus. The statements in the example are equivalent to performing CMD "?U*", "F1."

f. TAKING A MEASUREMENT

Statement Format: CMD "ADDRESS STRING", "J1"
Example: CMD "?U*", "J1"
Explanation: If the counter has been previously programmed for HOLD sample rate (E9), the Sample Trigger Command (J1) causes the counter to be armed thereby initiating a new measurement. In general, following the trigger command in the program are program statements to read the measurement into the calculator. To allow for the time lapse between the time of the sample trigger and the read statements, the counter should have been programmed for WAIT until addressed output mode (E:). Hence, before the J1 command, the counter should have been sent a sequence of ASCII codes which included the E9E: codes.

g. READING COUNTER MEASUREMENT INTO THE CALCULATOR

Statement Format: CMD "ADDRESS STRING"; FMT <format spec>; RED 13, <register address>
Example: CMD "?J5"; FMT*; RED 13, A;
Explanation: FMT and RED are displayed by the calculator when the FORMAT and READ keys on PCII are respectively pushed. These should not be confused with similarly labeled keys on PCI. The contents of the quote field after the CMD define the counter as the Talker (assuming that the counter address switches have been set for a talk address=J, listen address=*), and the calculator as the listener (listen address=5). The semicolon terminates the bus command statement. The FORMAT statement defines a free field format (see the

Table 2-8. Address Switches

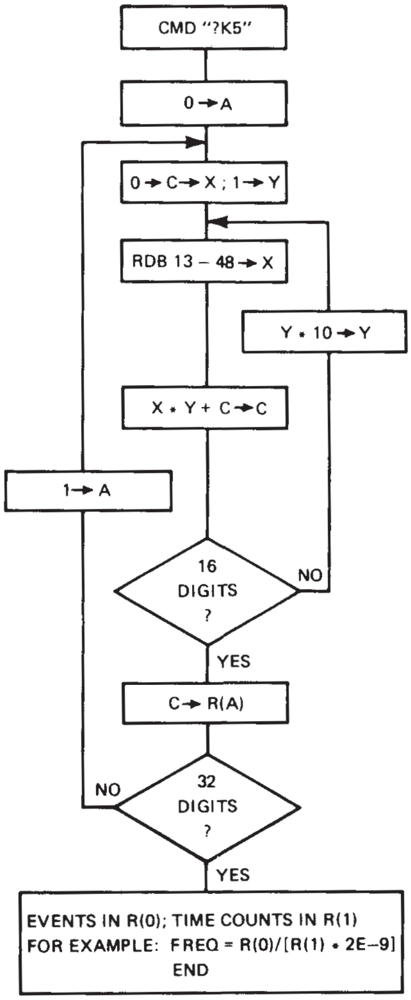
ADDRESS SWITCHES					
A_5	A_4	A_3	A_2	Listen** Address	Talk Address
0	0	0	0	SP !	@ **A**
0	0	0	1	" #	B **C**
0	0	1	0	$ %	D **E**
0	0	1	1	& '	F **G**
0	1	0	0	( )	H **I**
0	1	0	1	* +	J **K**
0	1	1	0	, -	L **M**
0	1	1	1	. /	N **O**
1	0	0	0	0 1	P **Q**
1	0	0	1	2 3	R **S**
1	0	1	0	4 5	T **U**
1	0	1	1	6 7	V **W**
1	1	0	0	8 9	X **Y**
1	1	0	1	: ;	Z **[**
1	1	1	0	< =	\ **]**

**either listen address may be used.
Shaded talk addresses are computer dump Talk codes only; cannot be used as Normal Talk Output codes.

PCII manual, pages 2-5 to 2-10). The READ statement specifies that data is to be read from the device with select code 13 (the ASCII Bus Interface card) and is to be placed in register A of the calculator (see the PCII manual, page 2-4).

h. READING COUNTER MEASUREMENTS INTO THE CALCULATOR USING UNPROCESSED FORMAT TALK MODE (COMPUTER DUMP)

Statement Format: CMD "ADDRESS STRING"; RDB 13 → <register>
Example: CMD "?K5"; RDB 13-48 → X
Explanation: This talk mode was not intended for use with the calculator. If, while in computer dump talk mode, the 5345A is unaddressed and another device is addressed, upon readdressing the 5345A to talk, one bit of data will be lost (this doesn't occur when using the computer). If this situation is avoided, computer dump talk may be used and is useful in obtaining constant 2x10^{-9} resolution from the counter. RDB is what the calculator displays when READ BYTE on PCII is pushed. If the counter address switches were set for a talk address of J and a listen address of *, the talk address for computer dump talk is K (always 1 bit greater than the normal talk code — see figure on the right). In the computer dump mode, 32 ASCII digits of information are output sequentially. Hence, the READ BYTE must be in a loop which is traversed 32 times. Each byte is read and converted to the decimal equivalent of the ASCII digit. In the above example, decimal 48 (decimal representation for 0 in ASCII) is subtraced from each byte, so that X contains a decimal number from 0 to 9. The 16 digits of the event scaler (from least significant to most significant) followed by the 16 digits of the time scaler (least significant to most significant) are output. The 5345A continues to output in this mode until it is unaddressed. The following figure on the right is a flowchart of a program which could be used to read the counter in computer dump output mode.



2-74. 5345A Implementation of Bus Features

a. UNIVERSAL COMMANDS - The 5345A Option 011 responds to the Untalk and Unlisten universal commands. It does NOT respond to the following universal commands: Local Lockout (LLO), Group Execute Trigger (GET), Device Clear (DCL), Serial Poll Enable (SPE), and Serial Poll Disable (SPD).

b. SERVICE REQUEST TESTING

Statement Format: If RDS 13 <1.9; GTO <STMT#>
Example: If RDS 13 <1.9; GTO 5
Explanation: RDS is what the calculator displays when the READ STATUS key of PCII is pushed. The 5345A pulls SRQ low (hence RDS 13 will be <1.9) after a measurement has been made only if it is in the "WAIT until address" output mode. The 5345A does NOT respond to serial polling. SRQ is cleared after the 5345A has been addressed to talk. If two or more 5345A's are connected to the bus and one of them sets SRQ low, the controller must sequentially address each to TALK. Only the 5345A with output information will respond.

2-75. 5345A Typical Output Speed

2-76. The following apply to both Option 011 and Option 010 (standard output format only).

Typical Through-put Rate:

a.	5345A—Superfast Computer	≈9 kHz
b.	5345A—Usual Computer I/O	≈1 kHz
c.	5345A/98XXA Calculator	≈25 Hz
c.	5345A/5150A Printer	≈3 Hz

The measurement cycle of the 5345A is the sum of several events.

a. Measurement time (Gate Time).
b. Process (compute) time.
c. Output time on the HP Interface bus.
d. Arming time to next measurement.

1. **Measurement time** for CW frequency signal can be from 20 ns to 20,000 s.

2. **Process time** for mainframe only (5345A), measurement will typically be 1 ms. For measurements involving plug-ins with complex arithmetic routine, the process time may be as long as 3 ms.

3. **Minimum output time** is a function the total number of digits outputted. Seven characters plus some number of displayed digits (1 to n) are outputted per measurement in (23 + 11n) μs.

4. **Arming Time** is variable from <1 μs to infinite (hold).

Output time occurs in parallel with arming time and measurement time. Thus, if the sum of arming time and measurement time exceeds output time, the effective output time is zero.

For the fastest possible measurement cycle rates: process, output, and arming are combined in the "computer dump" mode. **Total** minimum cycle time for the computer dump mode is

$$\text{Computer Dump Min.} \approx \text{Measurement Time} = 107\ \mu\text{s}$$

For the standard output mode

$$\text{Standard Output Time} \approx 1\ \text{ms}$$

Remember that the output time is timeshared with arming and measurement time. Thus, if the 5345A is EXT ARM for the <1 μs arming time and if GATE TIME is >1 ms, cycle time will equal to GATE TIME. NOTE: Plug-in measurement may add one or two more ms to the Standard Output Time.

Typically, system speed of outputting data from the 5345A is dictated by the receiver. DATA LISTENERS (receivers) are of two types:

a. Non-programmable, such as:

   1. 59303A Digital-to-Analog Converter.
   2. 59301A HP Interface Bus to Parallel Converter.
   3. 5150A Thermal Printer.

b. Programmable Data Receivers, such as:

1. 9820A Calculator.
2. 2105A Computer.

The data rate between the 5345A and type 1, non-programmable receivers is fixed for any given word length of "n" bytes. For any pair of sender-receiver on the bus, the rate of transmission is approximately equal to the rate of the slower machine. In fact, on the HP Interface Bus one may have several LISTENERS (Receivers). Of course, it is legal to have only one TALKER (sender). In this case the rate of information transmission is determined by the slowest instrument.

59301 Converter ≈200—400 μs (25 μs/byte)
5150A Terminal Printer Cycle Rate ≈300 ms

For programmable receivers, the input data rate is determined by three factors: the hardware constraint, system firmware, and the programmers software. Typically the software and system firmware (pre-programmed internal software) is much more restrictive. The following example with the 5345A minimum GATE TIME and minimum ARM TIME will illustrate this. Let 5345A talk address = J and listen address = *. Then:

a. 9820A — 5345A Operation

1. For reference: 5345A TALK, nobody LISTEN

```
CMD "J?"
```

Cycle time ≈1 ms (but useless because nobody listens)

2. 5345A TALK, 9820A LISTEN with no 9820A storage of data. 9820A storage of data. 9820A talk address = U, listen address = 5.

```
0:  CMD "J?5"
1:  RED 13,A; JMP 0
```

Cycle time ≈19 ms (useless)

The extra 18 ms represent firmware restriction of the 9820A.

3. 5345A TALK, 9820A LISTEN and STORE DATA POINTS a minimum length program.

```
0:  CMD "J?5", 1→C
1:  RED 13,R( )C; C+1→C
2:  IF C>300 GTO 4
3:  GTO 1
4:  STP
```

Cycle time ≈35 ms

This program stores 300 readings in 300 9820A storage locations. The incremental 15 ms represent 9820A program execution line.

b. 9830A—5345A Operation

5345A TALK, 9830A LISTEN with NO DATA STORAGE

```
10:  CMD "J?5"
20:  ENTER (13,*)A
30:  GO TO 20
```

Cycle time ≈18 ms (useless)

Program execution time for a useful program is similar to the 9820A (≈35 ms).

c. Even faster operation can be obtained with a calculator (9820A, 9821A, 9830A) with the following technique. Since the calculator spends much of its 35 ms in program execution time, it is possible to shorten this program loop and reduce input time by telling the calculator where to put the data instead of letting it figure it out itself.

```
0:  CMD "J?5"
1:  RED 13,R1
2:  RED 13,R2
3:  RED 13,R3
          .
          .
          .
300:  RED 13,R300
301:  STP
```

This program stores 300 readings in almost twice the speed but with a program length of 302 steps vs. 5 steps in a3, above.

d. 2100A, 59310A—5345A

1. 5345A Computer Dump Mode — DMA LISTEN program Cycle time ≈107 μs
2. 5345A Standard Output — variable computer software Cycle times 1—10 ms.

SECTION III

OPERATION

3-1. INTRODUCTION

3-2. Section III contains operating information that is helpful in realizing the best performance from the instrument. This includes a general description of the operating modes, the function of the controls and indicators, operator's maintenance, a self-check procedure, and setup procedures for making basic measurements.

3-3. MEASUREMENT TECHNIQUE

3-4. The counter uses a period average technique to make measurements. The counts (or pulses) that are generated from the input and time base signals are collected in separate scalers during the measurement time. The counter compares these pulses arithmetically and displays the result on the front panel.

3-5. OPERATING MODES

3-6. The following paragraphs describe the operating modes for frequency, period, time interval, ratio, and totalize measurements.

3-7. Frequency Mode

3-8. Channel A accepts input frequencies from 50 μHz to 500 MHz with a minimum level of 20 mV rms sine wave. These frequencies are counted directly with no prescaling techniques applied. Extended frequency capability is available with the use of plug-ins. The counter is capable of measuring pulsed RF in either a single burst or an average of several bursts. The measurement time within the burst may be varied in length and position for detecting frequency variations within a burst.

3-9. The measurement time is the selected gate time plus the time until the next trigger pulse occurs. For example, if the selected gate time is 1 ms, the event gate will close on the next trigger pulse after 1 ms has elapsed. If the input frequency were 20 kHz (.05 ms period), the measurement time would be 1 ms +.05 ms = 1.05 ms. The difference encountered does not affect the accuracy of the measurement.

3-10. Period Modes

3-11. Two modes of period measurements are available: single period and period average. These modes are described in the following paragraphs.

3-12. SINGLE PERIOD. Single period measurements are made with the GATE TIME switch set to MIN. In this position, the gate time is one period or 50 ns, whichever is greater. Therefore, the input frequency range for a single period measurement is 50 μHz to 20 MHz. Frequencies greater than 20 MHz may be applied, but they will be averaged during a 50 ns gate time.

3-13. PERIOD AVERAGE. When the GATE TIME switch is set to any other position than MIN, the counter averages multiple periods. Averaging increases the accuracy and resolution of the measurement. Input frequencies are in the 50 μHz to 500 MHz range. The actual gate time is determined in the same manner as that described under Frequency Mode.

3-14. <u>Number of Periods Averaged.</u> To determine the number of periods averaged during a measurement, divide the displayed answer into the selected gate time.

Example: $$\frac{\text{Gate Time setting (sec)}}{\text{Displayed Period (sec)}} = \frac{1\text{ ms}}{20.492\ \mu\text{s}} = 48.799 = 49\text{ periods}$$

The number of periods averaged will always be a whole number. Therefore, should the calculated answer contain any digits to the right of the decimal point, drop these digits and increment the remainder by one. This is due to the extended gate time. The answer for this example, then, is 49 periods averaged.

3-15. Time Interval Modes

3-16. The counter measures time intervals from Channel A to Channel B; that is, Channel A starts the measurement and Channel B stops the measurement. Time between points on a single waveform can be measured by connecting the input signal to CHANNEL A jack and placing the Input Amplifier Control switch to COM A. Under these conditions, the slope and level controls of Channel A and Channel B allow variable triggering on either the + or - slope. With the Input Amplifier Control switch set to SEP, measurements can be made between points on separate waveforms.

3-17. SINGLE TIME INTERVALS. Single time intervals down to 10 ns are measured with the GATE TIME switch set to MIN. The gate time is one time interval for repetition rates of less than 20 MHz. Thus, if two or more time intervals occur within 50 ns, they will be averaged.

3-18. TIME INTERVAL AVERAGE. The counter averages multiple time intervals when the GATE TIME switch is set to any position other than MIN. The maximum repetition rate is 50 MHz (10 ns time interval plus 10 ns deadtime = 20 ns period or 50 MHz). To average, the time interval must be less than the selected gate time.

NOTE

> If the time interval is greater than the gate time, but not more than 3.5 times greater, a single period will be measured. The MIN gate time position is preferred for single periods.

3-19. When averaging, white noise modulates the internal clock signal to prevent any harmonic relationship between the input signal and the clock. This increases the measurement accuracy. The noise is not generated when the GATE TIME switch is set to MIN.

3-20. INITIATING A MEASUREMENT. The front-panel ARM and GATE lights and the rear-panel dc trigger levels are helpful when setting up a time interval measurement. Place the GATE TIME switch to 100 μs. The ARM light is an indication that Channel A is not triggering, possibly due to insufficient signal amplitude or misadjusted front-panel controls. A flashing GATE light indicates that Channel A is triggering. If the counter is gating and *lamp test* (paragraph 3-63) is flashing or appears to be steady, the counter has gone into *excessive gate time* (paragraph 3-36). This means the counter has reset because Channel B was not triggered with a stop signal. This could be caused by the stop pulse failing to arrive until after the maximum allowable time, which is 3.5 times the selected gate time. In this case, increase the gate time. Other causes could be insufficient signal amplitude or misadjusted front-panel controls.

3-21. MEASUREMENT TIME. In time interval average, the time needed to complete a measurement may be much longer than the selected gate time. This is because the counter collects a *gate time's worth of time intervals*. The factors which would increase the measurement time are short time intervals and extended time between intervals (see Figure 3-1).

3-22. Occasionally, when increased resolution is needed, it may be convenient to estimate the total time of a measurement. To calculate this, use the equation below.

$$\text{Measurement Time} = \frac{\text{Gate Time (sec)}}{\text{Time Interval (sec) X Number of Time Intervals per sec}}$$

$$\text{Example:} \quad \frac{1 \text{ msec}}{100 \text{ ns X } 800/\text{sec}} = \frac{1 \text{ X } 10^{-3} \text{ sec}}{8 \text{ X } 10^{-5}} = 12.5 \text{ seconds}$$

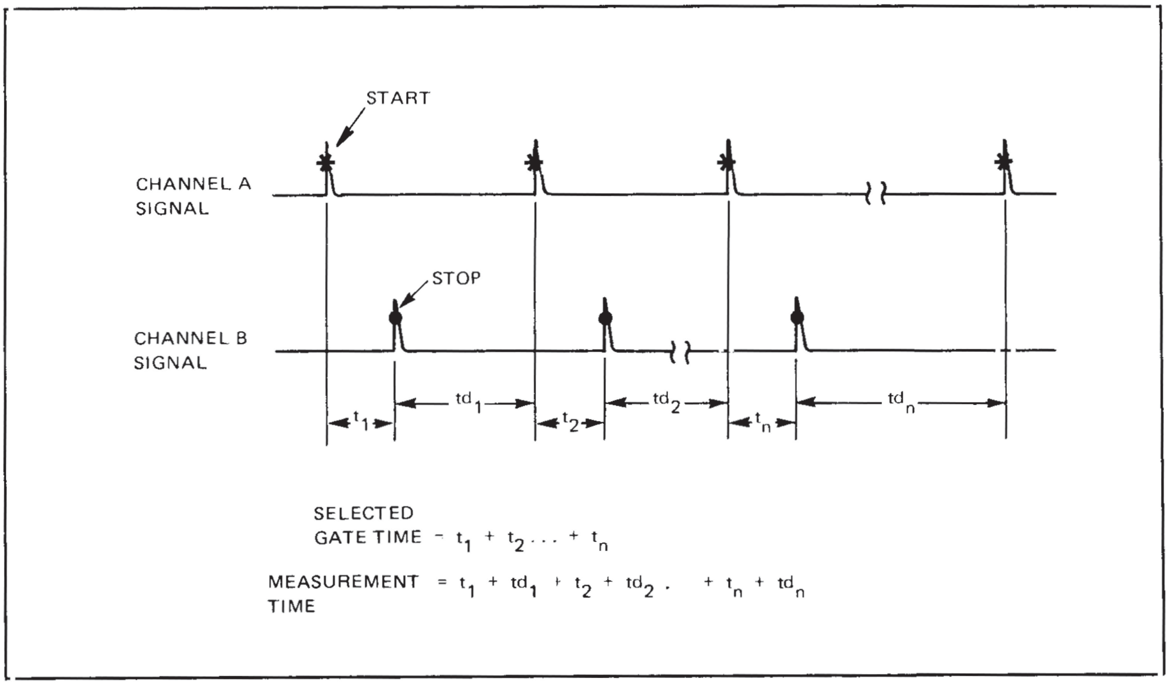

START
CHANNEL A SIGNAL
STOP
CHANNEL B SIGNAL
t_1
td_1
t_2
td_2
t_n
td_n
SELECTED GATE TIME = $t_1 + t_2 \ldots + t_n$
MEASUREMENT TIME = $t_1 + td_1 + t_2 + td_2 \ldots + t_n + td_n$

Figure 3-1. Measurement Time for Time Interval Average

3-23. If the time interval used in the equation is unknown, it can be obtained from the counter by selecting MIN. The number of time intervals per second can be taken from an oscilloscope reading. For most purposes, these figures need be only approximate to give a reasonable indication of the waiting time involved.

3-24. Ratio Measurements

3-25. The ratio between two frequencies (FB/FA) is measured by connecting one signal to Channel A and the other to Channel B. Both channels operate in the 50 μHz to 500 MHz range. If the higher frequency is connected to Channel B, the ratio will be greater than one. The answer for a ratio measurement is a unitless figure.

3-26. MEASUREMENT TIME. The difference between the selected gate time and the total measurement time depends on the frequency applied to Channel B. In the Ratio mode, the Channel B signal substitutes for the internal 500 MHz time base.

3-27. With the GATE TIME switch set to 1 s, for example, 5×10^8 time base counts are needed to end the measurement. When the 500 MHz internal time base is used, the 5×10^8 counts are accumulated in 1 second. If, for example, 70 MHz were applied to Channel B and used as the time base, it would take about 7 times as long (7.14 seconds) to accumulate the 5×10^8 counts needed to disarm the gate.

3-28. To estimate the measurement time, use the equation below.

$$\text{Measurement Time} = \frac{5 \times 10^8 \text{ Hz}}{\text{Channel B Freq.}} \times \text{Gate Time}$$

$$\text{Example:} \quad \frac{5 \times 10^8 \text{ Hz}}{25 \text{ MHz}} \times 1 \text{ ms} = \frac{5 \times 10^8}{2.5 \times 10^7} \times 1 \times 10^{-3} \text{ sec} = 20 \text{ ms}$$

3-29. Totalize Mode

3-30. The START and STOP positions on the FUNCTION switch allow manual opening and closing of the counter's main gate. The Input Amplifier Control switch must be placed in SEP. When the switch is in the START position, the counter totalizes the number of times the input signal passes through the Channel A trigger point. The GATE TIME switch does not affect the displayed result in any way.

3-31. BOTH CHANNELS TOTALIZED. When the Input Amplifier Control switch is set to SEP, Channel A and Channel B signals can be totalized simultaneously. The displayed result is a function of the ACCUM MODE START/STOP switch, located on the rear panel. The two signals are added (A+B) or subtracted (A-B), depending on the switch position. When the Input Amplifier Control switch is set to CHECK, the counter always selects A+B.

3-32. A minus sign on the display indicates that during a subtraction (A-B) the B events have outnumbered the A events. With the switch in A-B, the instrument functions like an up-down or reversible counter. That is, the counter will count down from a previously-given positive number. As an example of this, assume that the A frequency is greater than the B frequency and the switch is in A-B. The display accumulates positive numbers at a rate equal to the difference between the two input frequencies. If the frequency of B now becomes greater than A, the displayed count will decrease towards zero, again, at a rate equal to the difference between the two frequencies. Once the declining number passes through zero, the minus sign lights and the display continues to accumulate.

3-33. SCALED OUTPUT. With the FUNCTION switch set to START and SAMPLE RATE to HOLD, the counter scales (divides) the Channel A input frequency by powers of 10. This scaled signal is available on the rear-panel CHAN A SCALER OUTPUT jack. Although the display is not functioning, the counter is accumulating. The GATE TIME switch controls the division factor, as shown in Table 3-1.

Table 3-1. Scaler Output for Channel A

GATE TIME SETTING	SCALING FACTOR	SCALED OUTPUT (100 MHz IN OR CHECK)
100 ns	10^2	1 MHz
1 µs	10^3	100 kHz
10 µs	10^4	10 kHz
100 µs	10^5	1 kHz
1 ms	10^6	100 Hz
10 ms	10^7	10 Hz
100 ms	10^8	1 Hz
1 s	10^9	100 mHz
10 s	10^{10}	10 mHz
100 s	10^{11}	1 mHz
1000 s	10^{12}	100 µHz

3-34. INPUT TRIGGERING

3-35. The input circuits provide triggering over a range of -1.3V to +1.3V. The point at which triggering occurs is adjustable with the front-panel LEVEL control. Each input channel has a small amount of hysteresis (about 10 mV). If the SLOPE switch is set to "+," the trigger pulse occurs at the top of the hysteresis *window*. If the SLOPE switch is set to "-," the pulse occurs on the bottom line of the window. In other words, the signal must pass through the entire hysteresis window before a trigger pulse is generated (see Figure 3-2). The LEVEL control must be placed to allow at least a 1 ns pulse width for the Schmitt Trigger.

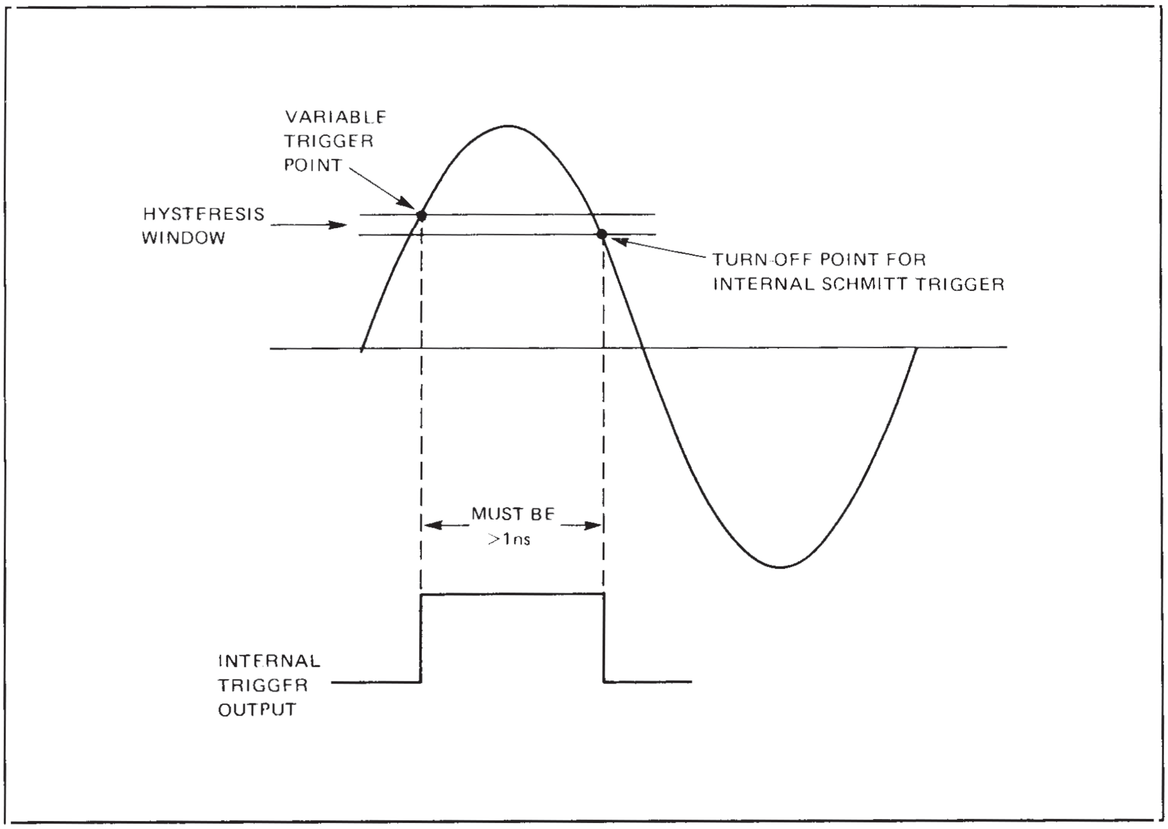


Figure 3-2. Internal Triggering

3-36. EXCESSIVE GATE TIME

3-37. In every measurement involving a gate time, the counter depends on the input signal to terminate the measurement. The measurement concludes one clock pulse after the next input pulse following the end of the gate time, not with the gate time itself. If the period of the input signal is much longer than the gate time or if the signal is interrupted sometime during the gate time, the excessive gate time circuits prevent the counter from waiting indefinitely for the terminating pulse. The counter will wait for about 3.5 times the selected gate time before resetting. At the end of excessive gate time, the display will flash instantaneously to lamp test before displaying all zeros. Excessive gate time is especially useful during the time interval measurement; see paragraph 3-20 for a further description.

3-38. EXTERNAL ARMING AND GATING

3-39. The GATE CONTROL INPUT jack (rear panel) allows the counter to be externally armed and gated. The jack works in conjunction with the Gate Control switch, located directly below the jack.

3-40. External Arming

3-41. When externally arming, set the Gate Control switch to EXT ARM and the SAMPLE RATE switch to HOLD. The counter will ARM when the instrument is first turned on because of the internal arming of the sample rate circuits. After the first measurement, however, the counter's arming circuits are fully controlled by the external source. The counter is armed within 1 μs of receiving the arm pulse (500 ns to dc at -1V). Once the counter is armed, the measurement begins with the first Channel A trigger pulse. The counter makes only one measurment for each arm pulse.

3-42. External Gating

3-43. When the Gate Control switch is set to EXT GATE, the counter's arming and gating is under full external control. The gating can be accomplished in two ways: single gating or multiple gating.

3-44. SINGLE PULSE GATING. Single gating is accomplished with a single, external gate pulse. The width of this pulse can be varied from 20 ns to 20,000 seconds. When using a single gate, set the GATE TIME switch to MIN. This assures the measurement will always take place during a single, external gate pulse. This will not be true for other settings of the GATE TIME switch.

3-45. MULTIPLE PULSE GATING. This method requires an arming pulse, which is automatically taken from the external gate pulse train. When the GATE TIME switch is in any position other than MIN, the counter accumulates as many external gate pulses as are needed to equal or exceed the gate time selected by the switch. As an example, assume a GATE TIME setting of 10 ms and external gate pulses of 4 ms. The counter requires three of these pulses before a measurement can be completed. The total gate time is 12 ms.

3-46. One of the uses of multiple gating is *frequency averaging*, i.e., an average of frequency measured over multiple bursts. Using the same values as above, Figure 3-3 shows the type of gating in frequency averaging.

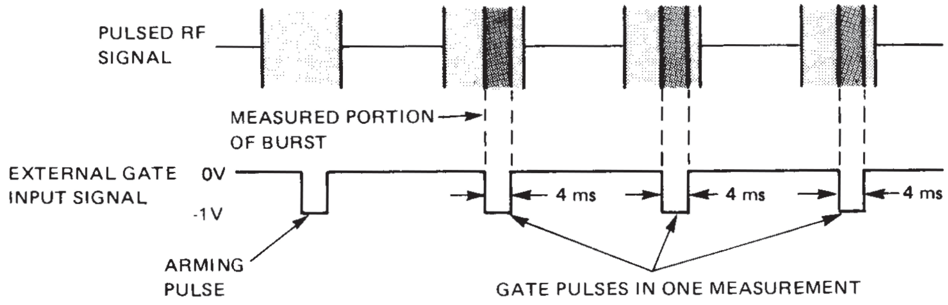


Figure 3-3. Multiple Gating

3-47. Time Interval Measurements

3-48. External gating is valuable when measuring the time between two events while ignoring the events occurring between them. The external gate signal must go low (-1 V) before the start pulse and return high (0 V) before the stop pulse.

3-49. SINGLE TIME INTERVALS. As previously mentioned for external gating, a measurement using a single external gate requires the GATE TIME switch to be set to MIN. The counter arms automatically and the external gate pulse provides a control over the time interval measurement. Varying the width of the pulse determines which time interval is measured, as can be seen in Figure 3-4.

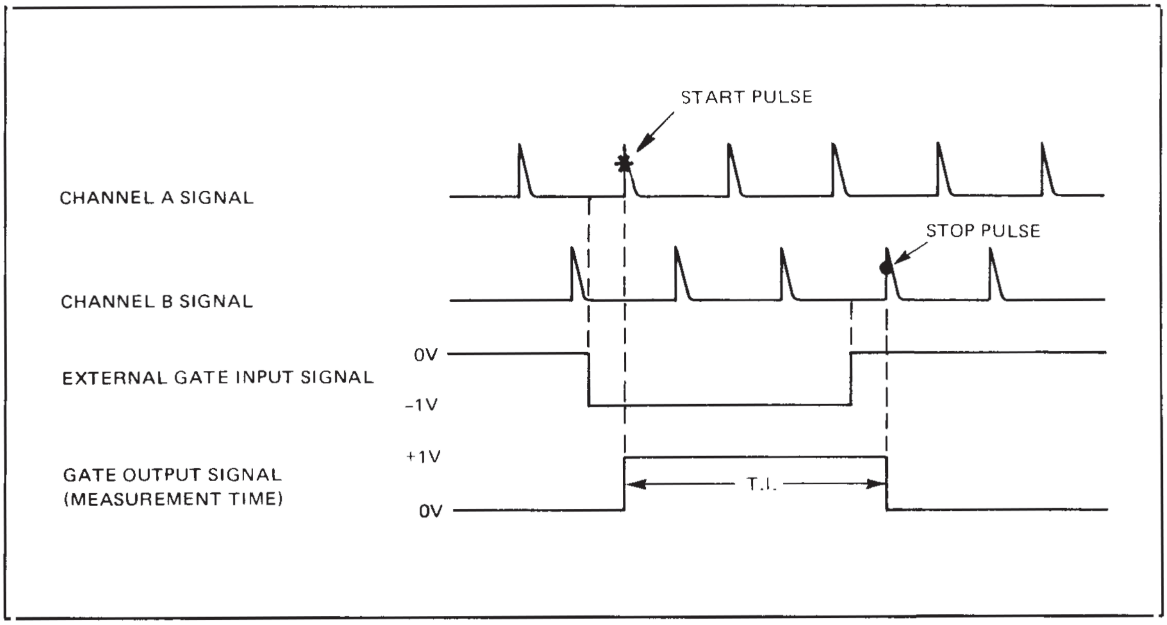


Figure 3-4. External Gating for Single Time Interval

3-50. MULTIPLE TIME INTERVALS. An average of time intervals can be measured using the external gating method. This method, as in single time intervals, allows certain pulses of the waveform to be ignored. The GATE TIME switch must be set to any other position than MIN. See Figure 3-5 for an example of time interval averaging. This method does require an arming pulse for each measurement cycle.

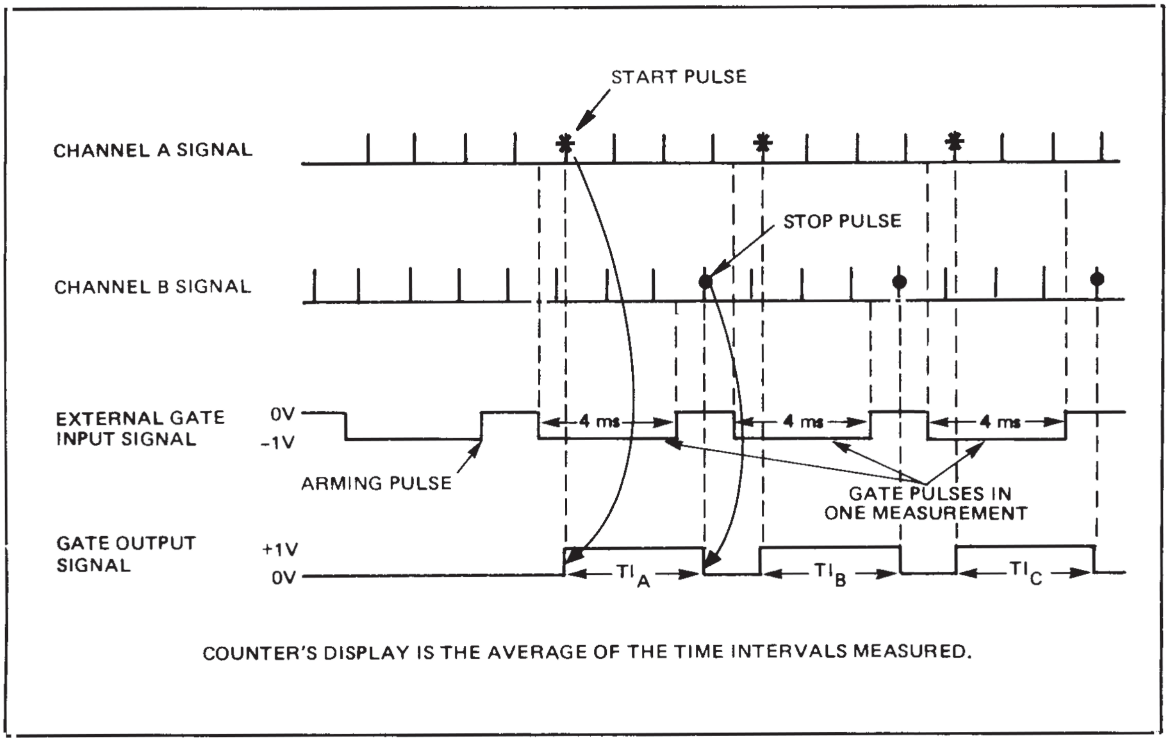

START PULSE
CHANNEL A SIGNAL
STOP PULSE
CHANNEL B SIGNAL
EXTERNAL GATE INPUT SIGNAL
0V
-1V
4 ms
4 ms
4 ms
ARMING PULSE
GATE PULSES IN ONE MEASUREMENT
GATE OUTPUT SIGNAL
+1V
0V
TI A
TI B
TI C
COUNTER'S DISPLAY IS THE AVERAGE OF THE TIME INTERVALS MEASURED.

Figure 3-5. External Gating for Time Interval Averaging

3-51. DISPLAY

3-52. The counter uses a 12-digit display: 11 digits of data and 1-digit for the minus sign. Unlike most counters, the number of digits displayed in a measurement is not a function of the input frequency and is not related to the FUNCTION switch. The number of digits is constant for each setting of the GATE TIME switch.

3-53. Display Position

3-54. When the DISPLAY POSITION switch is set to AUTO, the counter automatically positions the display's least-significant digit in the right-most column. Rotating the switch to each of its counterclockwise positions (blue dots) shifts the decimal point, hence the display, one place to the left. Once the switch is placed to any position other than AUTO, the annunciator (k, M, n, etc.) stays fixed, regardless of changing input frequency. The annunciator remains fixed until the RESET button is pushed or the FUNCTION switch setting is changed. Manually fixing the decimal point and the annunciator is convenient when collecting measurement data with a digital-to-analog converter. As an example, the DAC can continually record any 3 digits in a possible display of 11, regardless of changing input data.

3-55. Asterisk

3-56. The asterisk lamp will light under any one of four conditions: overflow, underflow, factitious zeros, or insuffucient oven temperature (standard only). Overflow occurs when the placement of the DISPLAY POSITION switch has positioned the display's most-significant digit(s) so far to the left that it is out of viewable range. Underflow occurs when the placement of the DISPLAY POSITION switch has positioned the display's least-significant digit(s) so far to the right that it is out of viewable range. If the counter is equipped with an oven-controlled oscillator (optional), the operating temperature of the oven must remain constant for the crystal to perform properly. Should the oven temperature drop below its normal operating range, the asterisk light will come on as an indication of this condition.

3-57. *Factitious* zeros occur when the settings of the GATE TIME switch and DISPLAY POSITION switch have been combined to give fewer significant digits than the DISPLAY POSITION demanded. In this combination, the display attempts to blank one or more of the significant digits located to left of decimal point. Instead of blanking the digit, the display substitutes an artificial and meaningless zero to keep that portion of the display filled.

3-58. Although the presence of factitious zeros is a rare occurrence, its appearance can be demonstrated with the counter set up as follows: FUNCTION to FREQ A, connect input signal of 125 MHz, turn DISPLAY POSITION switch out of AUTO to about mid-range, turn GATE TIME switch ccw until the display is 125 MHz. The next switch position changes the display to 120 MHz and lights the asterisk. The zero now displayed is a factitious or filler zero.

3-59. Arm Light

3-60. An illuminated ARM light indicates that Channel A is not triggering. The condition of this indicator should be observed when adjusting the front-panel controls for a first-time measurement. Insufficient amplitude of the input signal or improper setting of the input controls (LEVEL, ATTEN, etc.) are common causes for the failure of the GATE light to turn on.

3-61. Gate Light

3-62. Once Channel A triggers, the ARM light turns off and the GATE light turns on. The GATE indicator lights during the time the counter's event gate is open. For short-duration gate times, the GATE light circuits include a 40 ms one-shot MV to allow a visible flash of the light. The SAMPLE RATE control sets the time between flashes (or measurement cycles).

3-63. Lamp Test

3-64. To ensure that all segments of the display are capable of lighting, the counter provides a lamp test. The display should appear like the representation shown on the next page (Figure 3-6).

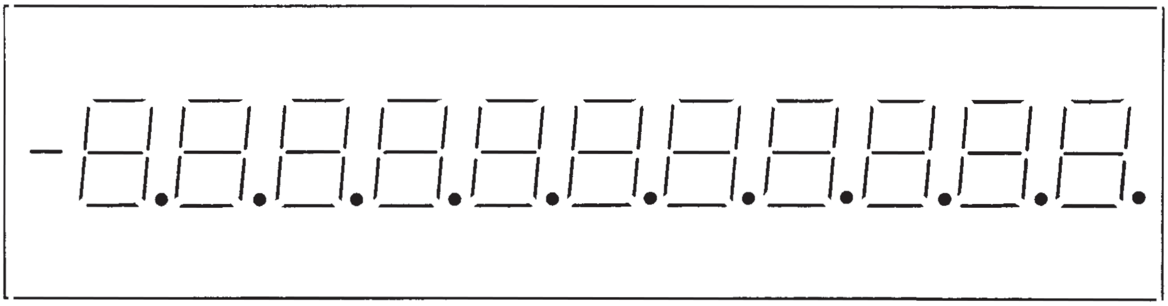


Figure 3-6. Lamp Test

3-65. Lamp test occurs under several conditions:

a. When the RESET button is pushed.

b. When the POWER switch is placed to ON, lamp test will light for about 2 seconds.

c. When switching between detent positions of the GATE TIME switch, FUNCTION switch, or DISPLAY POSITION switch.

d. When counter is attempting to phase lock the internal oscillator to an external standard.

e. When the counter has gone into excessive gate time.

f. When operating with an external frequency standard (rear panel INT STD-EXT STD set to EXT STD) and the external frequency is lost or disconnected.

3-66. COOLING

3-67. The counter's fan, located behind the display assembly, provides forced-air cooling to the electronic components throughout the instrument. The fan takes air in through the left side panel and bottom cover and exhausts it through the top cover and right side cover via the plug-in compartment.

NOTE

Check for proper air flow each time the instrument is turned on. If the unit is operated for extended periods of time without adequate cooling, the counter will automatically turn off.

3-68. AIR FILTER CLEANING

NOTE

Instruments with serial number 1708A02576 or higher are supplied less the air filters. Hewlett-Packard recommends removing the filters from all previous units. If desired to retain the filter protection, follow the step-by-step instructions below.

3-69. When the instrument is placed into service, the air filters should be inspected frequently to determine the rate at which they collect dirt in their particular environment. Under average conditions, the air filters should be cleaned about every 3 months. To remove these filters, proceed as follows:

a. Remove power cord at rear panel.

b. Remove the top and bottom covers (4 screws each).

c. Remove the 4 screws holding in display assembly (see Figure 3-7). Remove display assembly from mainframe and disconnect its power cable at bulkhead.

d. Remove left-front side cover (4 screws).

e. On left side frame, remove right-most top and bottom screws (1 ea.) and extract side air filter.

f. Remove the 4 screws holding the 2 internal brackets and extract bottom air filter.

Use the following procedure to clean the air filters.

a. Wash air filters with water.

b. Let stand until completely dry.

c. Recoat filters with *RP Super Filter Coat Adhesive*, Research Products Corporation.

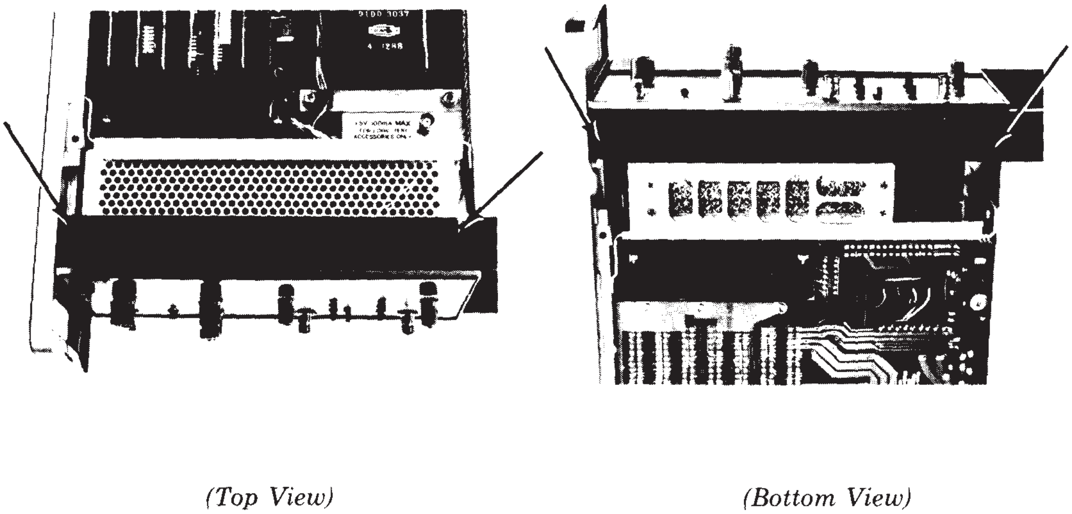


Figure 3-7. Location of Display Assembly Screws

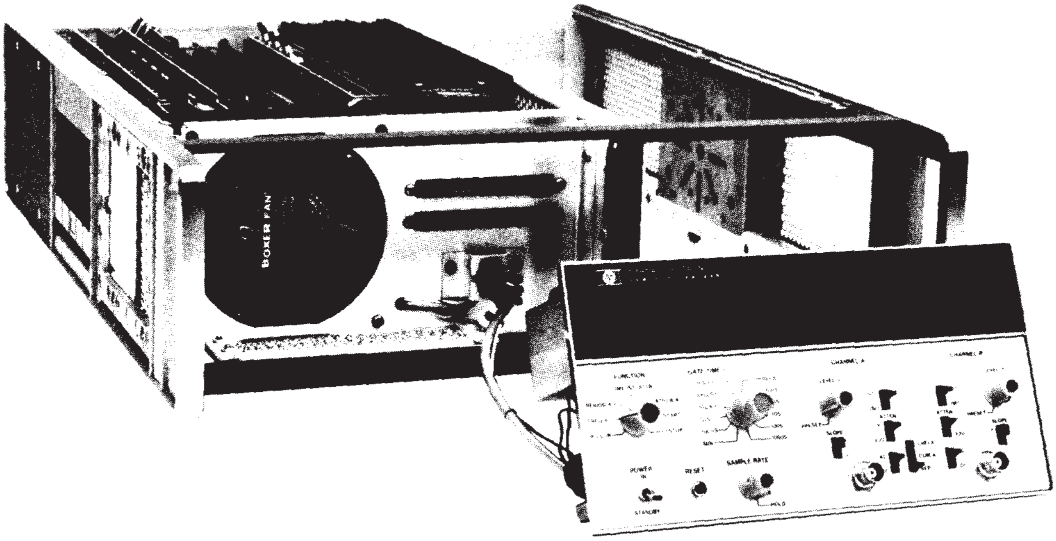


Figure 3-8. Removal of Display Assembly

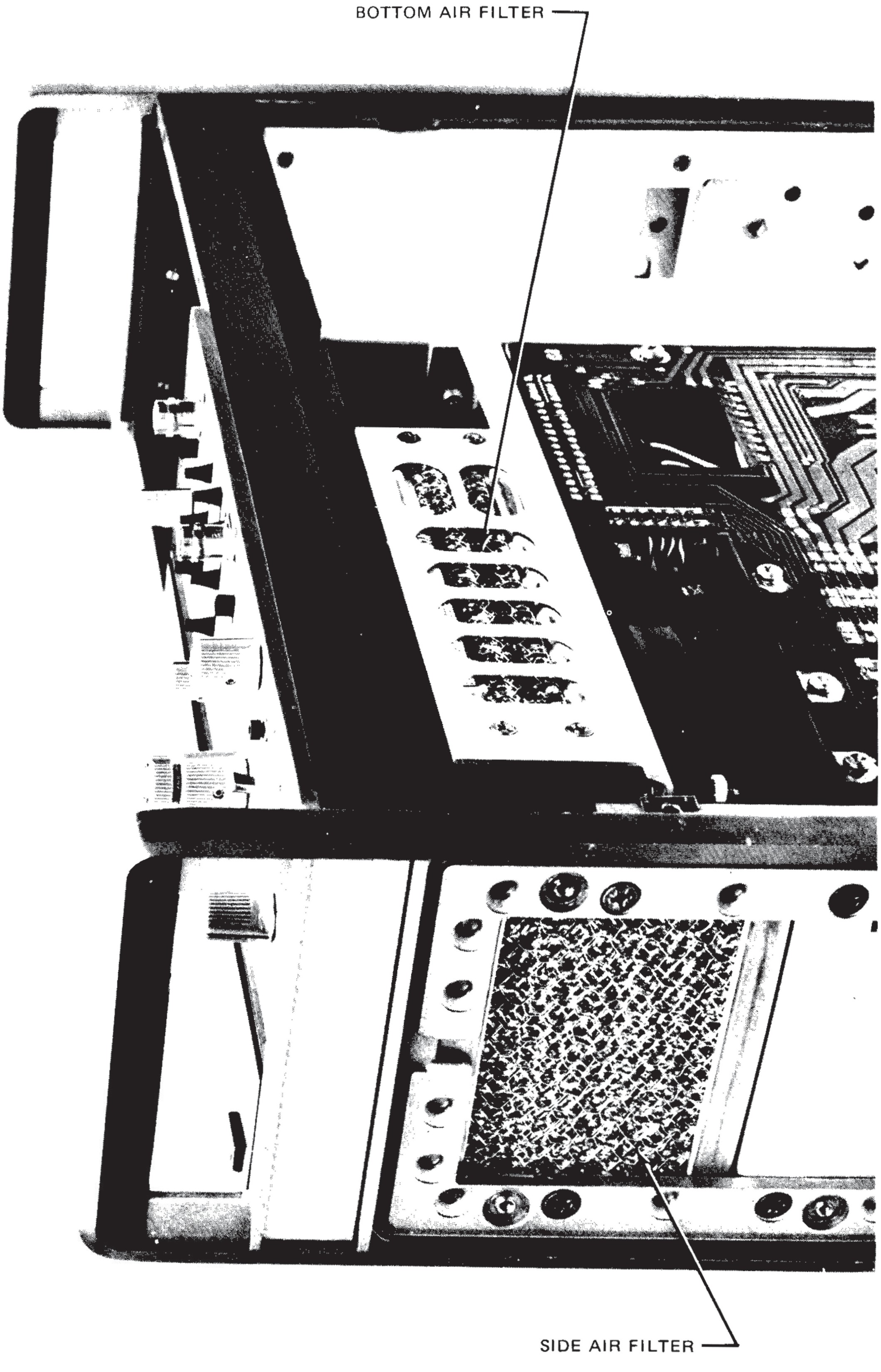
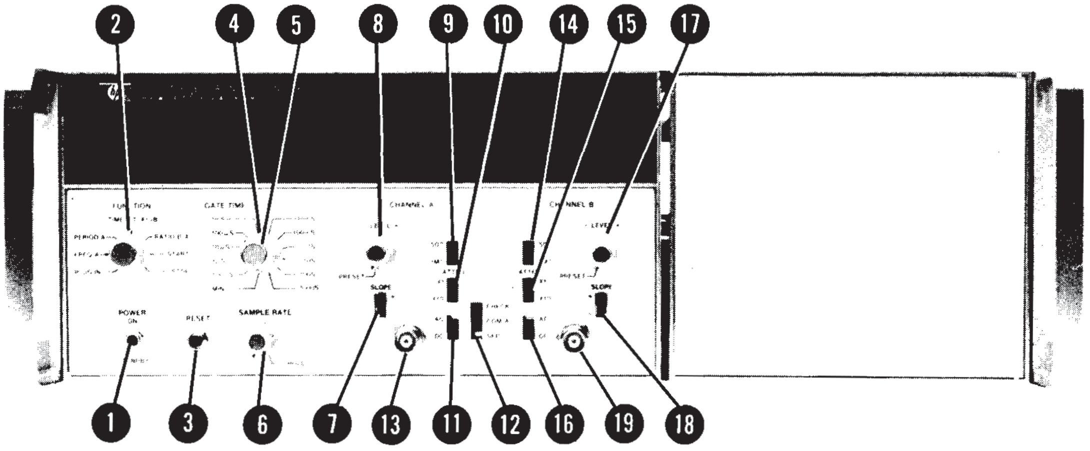


Figure 3-9. Location of Air Filters



1. POWER switch ①. In STANDBY position, supplies power to oscillator and oven (Option 001) to maintain a constant temperature for the crystal. In ON position, supplies normal operating power to remainder of instrument.

2. FUNCTION selector ②. Selects mode of operation.

    a. PLUG-IN — Enables plug-in to make measurement.

    b. FREQ A — Sets counter to measure frequency applied to CHANNEL A jack.

    c. PERIOD A — Sets counter to measure period or period average of signal applied to CHANNEL A jack.

    d. TIME INT. A to B — Sets counter to measure single time interval or time interval average. Channel A starts measurement and Channel B stops measurement.

    e. RATIO B/A — Sets counter to measure the ratio of Channel B frequency to Channel A frequency.

    f. START, STOP — Used for totalize mode to manually open and close counter's main gate and to turn scaled output on and off (SAMPLE RATE in HOLD).

3. RESET button ③. Resets display and internal count to zero and arms counter for new measurement. Generates lamp test.

4. GATE TIME switch ④. Selects total amount of time that the gate is open. MIN position opens main gate for one event or 50 ns, whichever is greater.

5. DISPLAY POSITION switch ⑤ (blue knob). In AUTO, counter displays least-significant digit in right-most column. Annunciators change with input frequency. Any other position manually fixes decimal point and annunciators.

6. SAMPLE RATE control ⑥. Varies time between measurements from <.1 sec to >5 sec. HOLD position holds display indefinitely.

7. SLOPE switch ⑦ ⑱. Permits triggering on positive or negative slope of input signal.

Figure 3-10. Front Panel Controls and Connectors

8. LEVEL control ⑧ ⑰ . Used in conjunction with ATTEN switch to select voltage at which triggering occurs. With X1 attenuator setting, level is variable ±1.3 V; on X10, ±13V.

9. Input Impedance Switch ⑨ ⑭ . Selects input impedance of 50Ω or 1 MΩ shunted by less than 30 pF.

10. ATTEN switch ⑩ ⑮ . Selects attenuation for input signal. Used in conjunction with LEVEL control to set trigger point. Input level is not affected in X1 position. Signal amplitude is reduced by factor of 10 in X10 position.

11. Coupling switch ⑪ ⑯ . Selects direct or capacitor coupling for input signal.

12. Input Amplifier Control switch ⑫ .

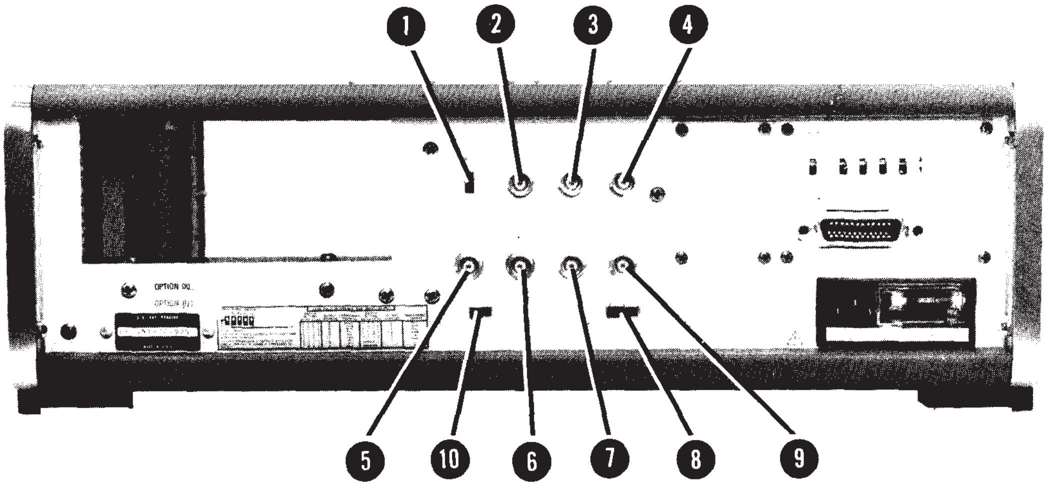
    a. CHECK — Checks that counter is functioning properly by connecting internal 100 MHz test signal to Channels A and B.

    b. COM A — Operationally connects A and B channels in parallel. Used for single source time interval measurements. Channel B jack is not active. Channel A and B Input Impedance switches must be set to same position.

    c. SEP — Allows independent operation of Channel A and B.

13. Input jacks ⑬ ⑲ . Inputs for Channel A and Channel B. Each input can accept signals from 50 μHz to 500 MHz.

Figure 3-10. Front Panel Controls and Connectors (Continued)



1. ACCUM MODE START/STOP switch ①. Used when totalizing two input signals. In A-B position, Channel B counts are subtracted from Channel A counts. In A+B position, the counts of each channel are added for the total displayed count.

2. CHAN A SCALER OUTPUT jack ②. With the FUNCTION switch set to START and the SAMPLE RATE control in HOLD, jack provides scaled output of Channel A input frequency or internal 100 MHz check signal.

3. CHAN A TRIG LEVEL jack ③. Output level corresponds to trigger point of Channel A. LEVEL control varies output ±1.3 Vdc.

4. CHAN B TRIG LEVEL jack ④. Output level corresponds to trigger point of Channel B. LEVEL control varies output ±1.3 Vdc.

5. EXT FREQ STD INPUT jack ⑤. Allows internal time base to phase lock to external frequency standard. Possible input frequencies =

$$\frac{10\text{ MHz}}{\text{any Integer from 1 to 10}} = 10\text{ MHz, } 5\text{ MHz, } 2.5\text{ MHz, } 2\text{ MHz, } 1\text{ MHz, etc.}$$

6. FREQ STD OUTPUT jack ⑥. Provides 10 MHz internal standard signal for external use. Amplitude is 1 Vrms into 50Ω.

7. GATE OUTPUT jack ⑦. Provides output pulses of counter's event gate.

8. GATE CONTROL INPUT jack ⑧. Allows counter's main-gate/arm circuits to be controlled from external source. Works with Gate Control switch. See paragraph 3-38.

9. Gate Control switch ⑨.
   a. INTERNAL — Allows normal operation of counter.
   b. EXT ARM — Allows counter to be armed from external source. SAMPLE RATE control must be set to HOLD. Counter will make only one measurement for each arm pulse. Measurement begins with first Channel A pulse after arm pulse.
   c. EXT GATE — Allows total control of gating circuits (see paragraph 3-42). Used in frequency average and in pulse selection for time interval and time interval average.

10. FREQUENCY STANDARD INT-EXT switch ⑩. Allows an external frequency standard connected to ⑤ EXT FREQ STD INPUT to be used in the counter for the time base. In the INT position, the EXT FREQ STD INPUT connector is not connected through to circuits in the counter.

Figure 3-11. Rear Panel Controls and Connectors

Table 3-2. Self Check

1. Set the counter controls as follows:

   Input Amplifier Control switch to CHECK.
   FUNCTION switch to PLUG-IN.
   GATE TIME switch to MIN.
   DISPLAY POSITION switch to AUTO.
   SAMPLE RATE control to maximum ccw.

2. Turn POWER switch to ON. Check that the counter displays a minus sign and eleven 7-segment symbols (8) with 11 decimal points. This display should last about 2 seconds before switching to 11 zeros with no decimal points.

3. Set FUNCTION switch to FREQ A. The GATE light should be flashing.

4. Set GATE TIME switch as shown in table below, and check for proper display.

GATE TIME	DISPLAY	ANNUNCIATOR
MIN	.1	G Hz
100 ns	.10	G Hz
1 μs	100.	M Hz
10 μs	100.0	M Hz
100 μs	100.00	M Hz
1 ms	100.000	M Hz
10 ms	100.0000	M Hz
100 ms	100.00000	M Hz
1 s	100.000000	M Hz
10 s	100.0000000	M Hz
100 s	100.00000000	M Hz
1000 s	00.000000000	M Hz*

5. Set FUNCTION switch to PERIOD A and then to TIME INT. A to B. Check for proper display, as shown in the table below.

GATE TIME	DISPLAY	ANNUNCIATOR
MIN	10.	n sec
100 ns	10.	n sec
1 μs	10.0	n sec
10 μs	10.00	n sec
100 μs	10.000	n sec
1 ms	10.0000	n sec
10 ms	10.00000	n sec
100 ms	10.000000	n sec
1 s	10.0000000	n sec
10 s	10.00000000	n sec
100 s	10.000000000	n sec
1000 s	0.0000000000	n sec*

6. Set FUNCTION switch to RATIO.

7. Set GATE TIME switch as shown in table below, and check for proper display.

Table 3-2. Self Check (Continued)

GATE TIME	DISPLAY
MIN	1.
100 ns	1.0
1 μs	1.00
10 μs	1.000
100 μs	1.0000
1 ms	1.00000
10 ms	1.000000
100 ms	1.0000000
1 s	1.00000000
10 s	1.000000000
100 s	1.0000000000
1000 s	.00000000000*

8. Set FUNCTION switch to START. Check that counter totalizes and that the GATE light is on.

9. Set FUNCTION switch to STOP. Check that GATE light goes out and the display is held.

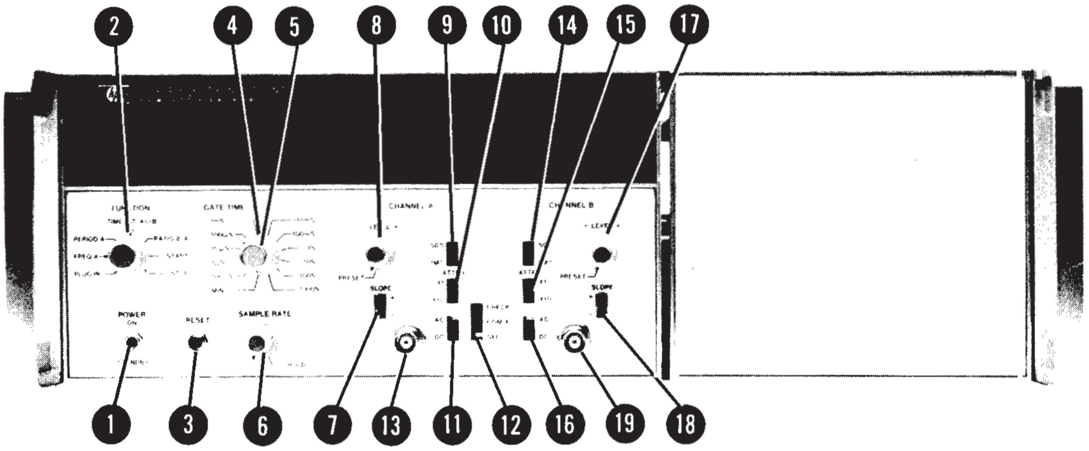
10. Set FUNCTION switch to START. The counter should begin totalizing from the previously held number.

11. Set FUNCTION switch to FREQ A and GATE TIME switch to 100 μs. Display is now 100.00 MHz.

12. Turn the DISPLAY POSITION switch (blue knob) through its positions and check for proper display, as shown in the table below.

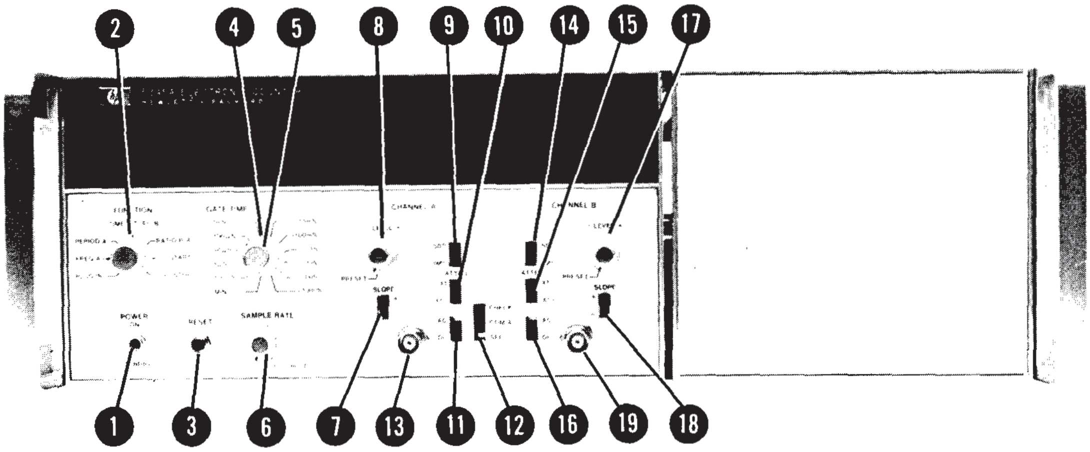
DISPLAY POSITION	DISPLAY (X = BLANK)	ANNUNCIATOR
AUTO	XXXXXX100.00	M Hz
100 s	XXXXXXXX100.	*M Hz
10 s	XXXXXXX100.0	*M Hz
1 s	XXXXXX100.00	M Hz
100 ms	XXXXX100.00X	M Hz
10 ms	XXXX100.00XX	M Hz
1 ms	XXX100.00XXX	M Hz
100 μs	XX100.00XXXX	M Hz
10 μs	X100.00XXXXX	M Hz
1 μs	100.00XXXXXX	M Hz
100 ns	00.00XXXXXXX	*M Hz
MIN	0.00XXXXXXXX	*M Hz

13. Push RESET button. Check that counter displays a minus sign and eleven 7-segment symbols (8) with 11 decimal points.



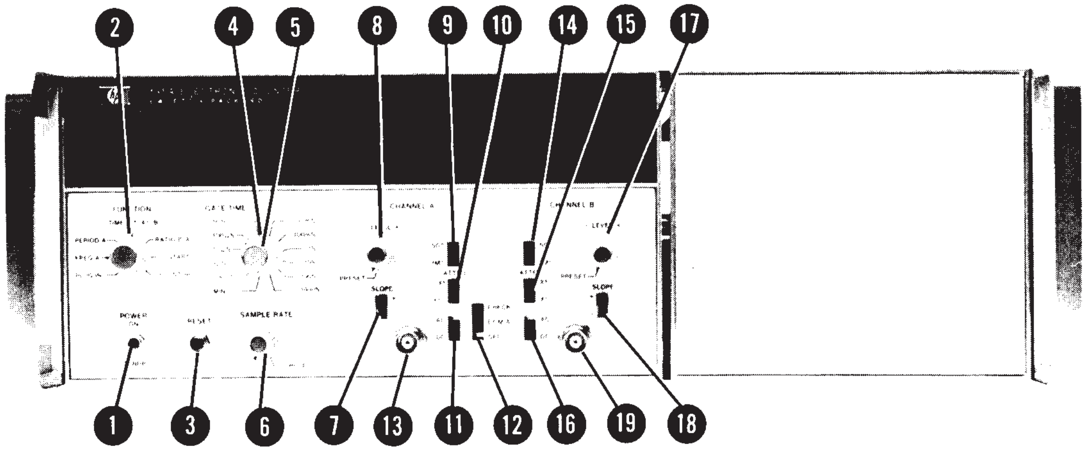
1. Set POWER switch ① to ON position.
2. Set FUNCTION switch ② to FREQ A.
3. Set DISPLAY POSITION switch ⑤ to AUTO.
4. Set GATE TIME switch ④ to give required integration time or desired resolution.
5. Set CHANNEL A Input Impedance switch ⑨ to desired position.
6. Set CHANNEL A ATTEN switch ⑩ to match input signal's amplitude; see Specifications Table 1-3 for maximum input levels.
7. Set CHANNEL A LEVEL control ⑧ to start measurement at desired voltage level. Use PRESET for sine waves.
8. Set CHANNEL A Coupling switch ⑪ to AC or DC; see Specifications in Table 1-3 for details.
9. Set Input Amplifier Control switch ⑫ to SEP.
10. Connect input signal to CHANNEL A input jack ⑬ .
11. Adjust SAMPLE RATE control ⑥ for a convenient interval between measurements.

Figure 3-12. Frequency Measurements



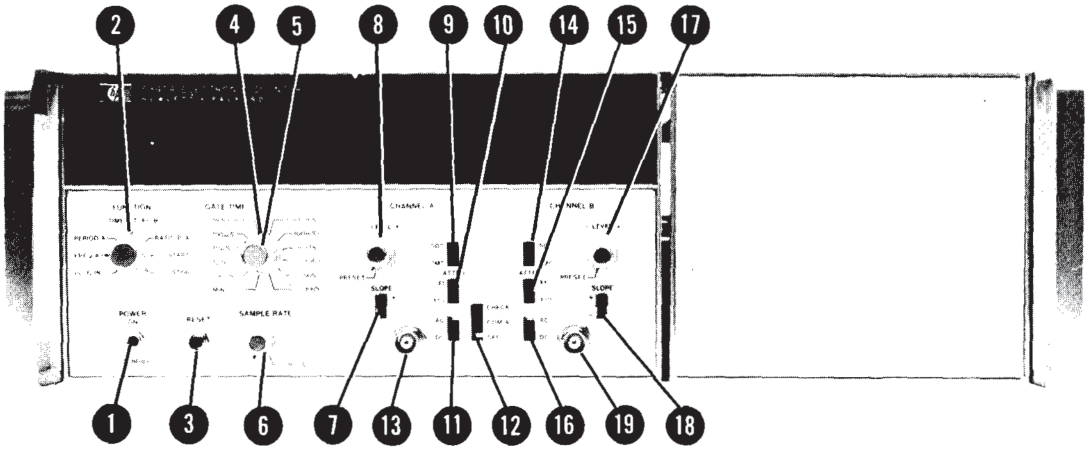
1. Set POWER switch ① to ON position.
2. Set FUNCTION switch ② to PERIOD A.
3. Set DISPLAY POSITION switch ⑤ to AUTO.
4. Set GATE TIME switch ④ to give required integration time or desired resolution.
5. Set CHANNEL A Input Impedance switch ⑨ to desired position.
6. Set CHANNEL A ATTEN switch ⑩ to match input signal's amplitude; see Specifications in Table 1-3 for maximum input levels.
7. Set CHANNEL A LEVEL control ⑧ to start measurement at desired voltage level. Use PRESET for sine waves.
8. Set CHANNEL A Coupling switch ⑪ to AC or DC; see Specifications in Table 1-3 for details.
9. Set Input Amplifier Control switch ⑫ to SEP.
10. Connect input signal to CHANNEL A input jack ⑬
11. Adjust SAMPLE RATE control ⑥ for a convenient interval between measurements.

Figure 3-13. Period Measurements



1. Set POWER switch ① to ON position.
2. Set FUNCTION switch ② to RATIO B/A.
3. Set DISPLAY POSITION switch ⑤ to AUTO.
4. Set GATE TIME switch ④ to give required integration time or desired resolution.
5. Set CHANNEL A Input Impedance switch ⑨ and CHANNEL B Input Impedance switch ⑭ to desired position. The switch positions may be selected independently.
6. Set CHANNEL A ATTEN switch ⑩ and CHANNEL B ATTEN switch ⑮ to match amplitude of respective input signal, see Specifications in Table 1-3 for maximum input levels.
7. Set CHANNEL A LEVEL control ⑧ and CHANNEL B LEVEL control ⑰ to desired trigger level or to PRESET for triggering at zero volts.
8. Set CHANNEL A Coupling switch ⑪ and CHANNEL B Coupling switch ⑯ to AC or DC, as required by the respective input signal. See Specifications in Table 1-3 for details.
9. Set Input Amplifier Control switch ⑫ to SEP.
10. Connect one signal to CHANNEL B jack ⑲ and comparator to CHANNEL A jack ⑬
11. Adjust SAMPLE RATE control ⑥ for a convenient measurement interval.

Figure 3-14. Ratio Measurements



1. Set POWER switch ① to ON position.

2. Set FUNCTION switch ② to TIME INT. A TO B.

3. Set DISPLAY POSITION switch ⑤ to AUTO.

4. Set GATE TIME switch ④ to MIN for single time interval or for desired resolution in time interval average.

5. Set CHANNEL A and CHANNEL B Input Impedance switches ⑨ ⑭ to desired position. The switches must be set to the same position.

6. Set CHANNEL A and CHANNEL B ATTEN switches ⑩ ⑮ to match input signal's amplitude; see Specifications in Table 1-3 for maximum input levels.

7. Set CHANNEL A Coupling switch ⑪ to AC or DC; see Specifications in Table 1-3 for details.

8. Set Input Amplifier Control switch ⑫ to COM A.

Continued on next page

Figure 3-15. One Source Time Interval Measurements

9. Connect input signal to CHANNEL A jack ⑬ .

10. Set CHANNEL A SLOPE switch ⑦ to + for triggering on positive slope or - for triggering on negative slope.

11. Set CHANNEL A LEVEL control ⑧ to start measurement at desired voltage level. Use CHAN A TRIG LEVEL output jack on rear panel to display starting point on an oscilloscope (if needed).

12. Set CHANNEL B SLOPE switch ⑱ to + for triggering on positive slope or - for triggering on negative slope.

13. Set CHANNEL B LEVEL control ⑰ to stop measurement at desired voltage level. Use CHAN B TRIG LEVEL output jack on rear panel to display stopping point on an oscilloscope (if needed).

14. Adjust SAMPLE RATE control ⑥ for convenient measurement interval.

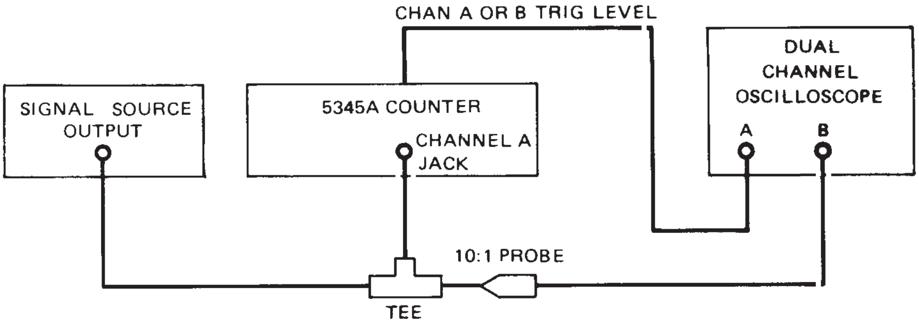
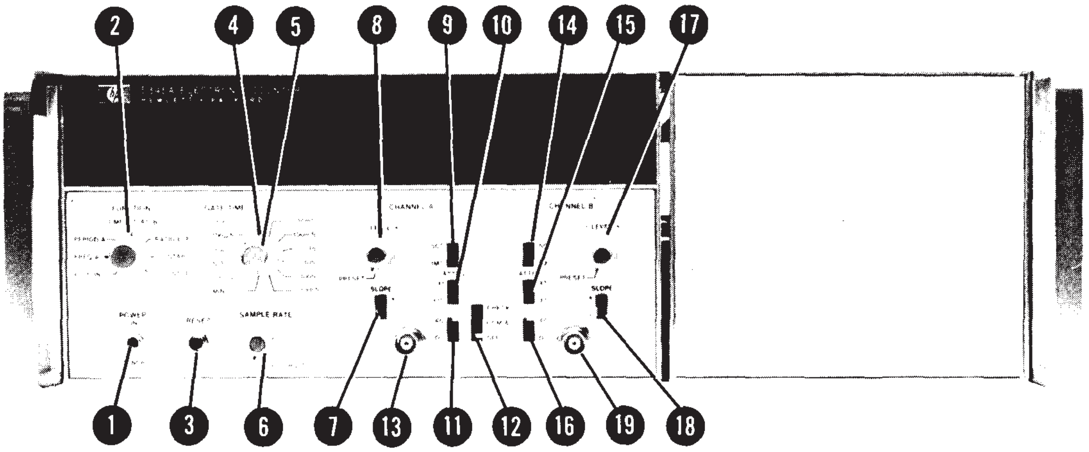


Figure 3-15. One Source Time Interval Measurements (Continued)



1. Set POWER switch ① to ON position.
2. Set FUNCTION switch ② to TIME INT A to B.
3. Set DISPLAY POSITION switch ⑤ to AUTO.
4. Set GATE TIME switch ④ to MIN for single time interval or for desired resolution in time interval average.
5. Set CHANNEL A Input Impedance switch ⑨ and CHANNEL B Input Impedance switch ⑭ to match impedance of respective signal source.
6. Set CHANNEL A ATTEN switch ⑩ and CHANNEL B ATTEN switch ⑮ to match amplitude of respective input signal; see Specifications in Table 1-3 for maximum input levels.
7. Set CHANNEL A Coupling switch ⑪ and CHANNEL B Coupling switch ⑯ to AC or DC, as required by the respective input signal. See Specifications in Table 1-3 for details.
8. Set Input Amplifier Control switch ⑫ to SEP.

Continued on next page

Figure 3-16. Two Source Time Interval Measurements

9. Connect start signal to CHANNEL A jack ⑬ and stop signal to CHANNEL B jack ⑲.

10. Set CHANNEL A SLOPE switch ⑦ to + for triggering on positive slope or to - for triggering on negative slope.

11. Set CHANNEL A LEVEL control ⑧ to start measurement at desired voltage level. Use CHAN A TRIG LEVEL output jack on rear panel to display starting point on an oscilloscope (if needed).

12. Set CHANNEL B SLOPE switch ⑱ to + for triggering on positive slope or - for triggering on negative slope.

13. Set CHANNEL B LEVEL control ⑰ to stop measurement at desired voltage level. Use CHAN B TRIG LEVEL output jack on rear panel to display stopping point on an oscilloscope (if needed).

14. Adjust SAMPLE RATE control ⑥ for a convenient measurement interval.

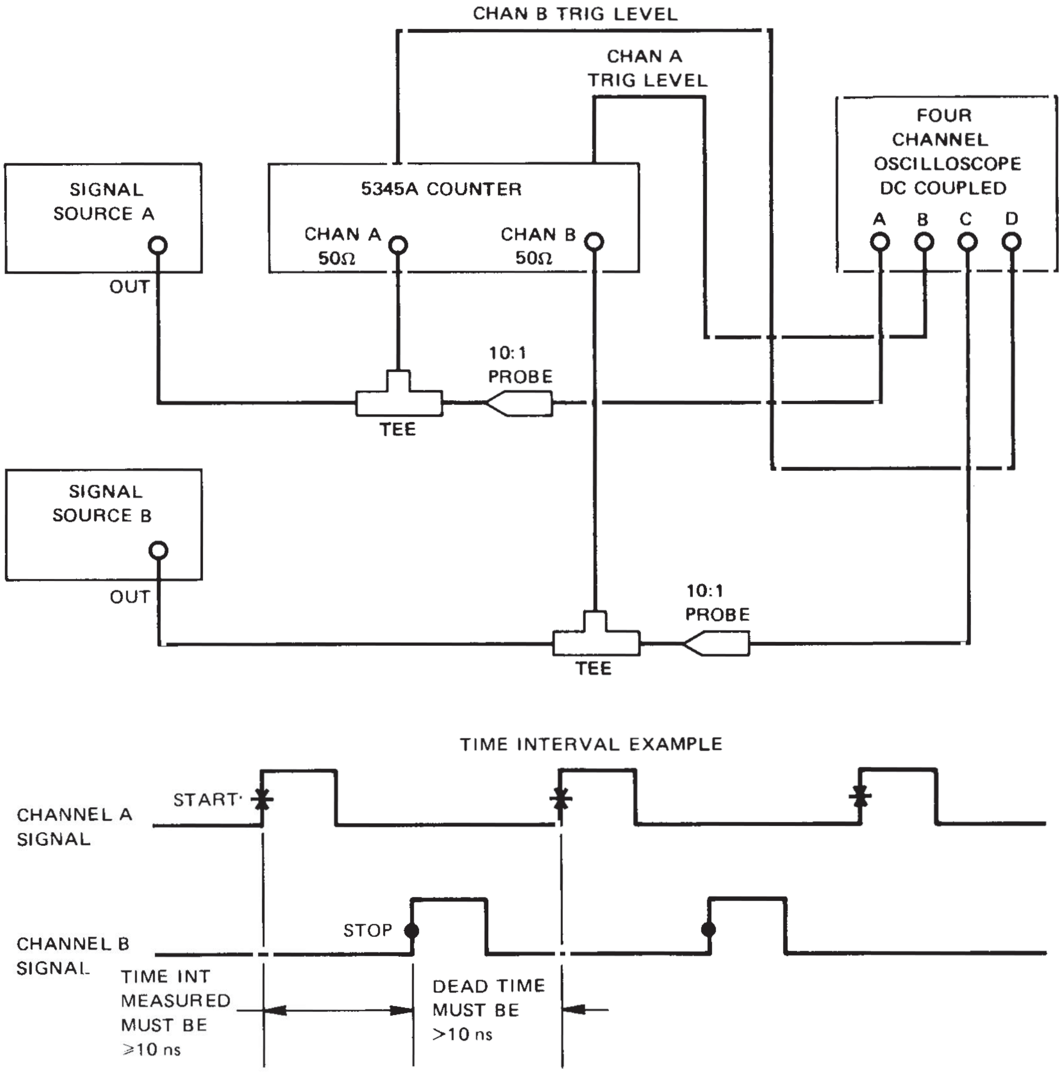
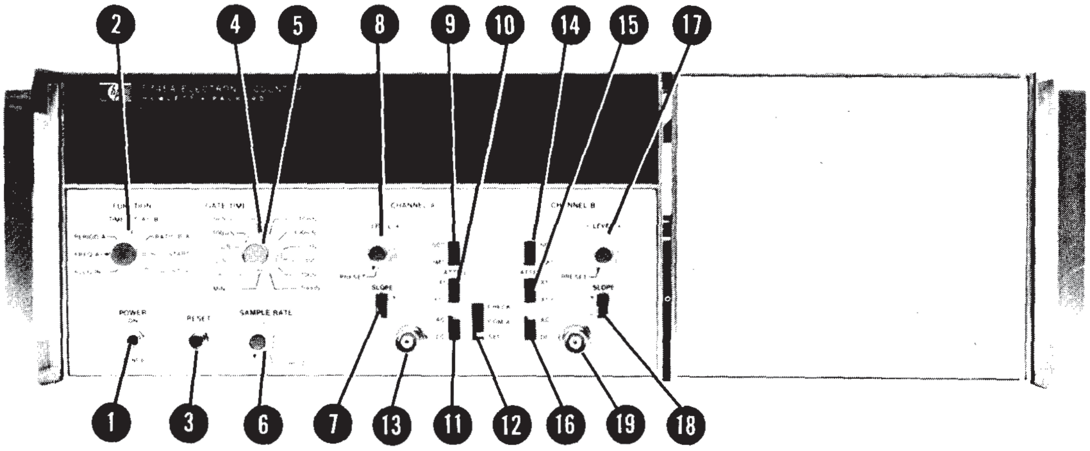


Figure 3-16. Two Source Time Interval Measurements (Continued)



1. Set POWER switch ① to ON position.
2. Set FUNCTION switch ② to STOP.
3. Set SAMPLE RATE control ⑥ full ccw.
4. Set DISPLAY POSITION switch ⑤ to AUTO.
5. Set CHANNEL A Input Impedance switch ⑨ and CHANNEL B Input Impedance switch ⑭ to desired positions.
6. Set CHANNEL A ATTEN switch ⑩ and CHANNEL B ATTEN switch ⑮ to match amplitude of respective input signal; see Specifications in Table 1-3 for maximum input levels.
7. Set CHANNEL A LEVEL control ⑧ to start measurement at desired voltage level.
8. Set CHANNEL A Coupling siwtch ⑪ to AC or DC, as required by the respective input signal. See Specification in Table 1-3 for details.
9. Set Input Amplifier Control switch ⑫ to SEP.
10. Connect one input signal to CHANNEL A jack ⑬ and the other to CHANNEL B jack ⑲ . If only one input signal is to be totalized, connect that signal to CHANNEL A jack ⑬ .
11. Set CHANNEL A LEVEL control ⑧ and CHANNEL B LEVEL control ⑰ to desired trigger level or to PRESET for triggering at zero volts.
12. Set the rear panel ACCUM MODE START/STOP switch to A+B to sum the two inputs or to A-B to totalize the difference.
13. Set FUNCTION switch ② to START.
14. A divided version of the CHANNEL A input frequency is available at the rear panel CHAN A SCALER OUTPUT jack if the SAMPLE RATE switch ⑥ is set to the HOLD position.

Figure 3-17. Totalize Measurements

SECTION IV

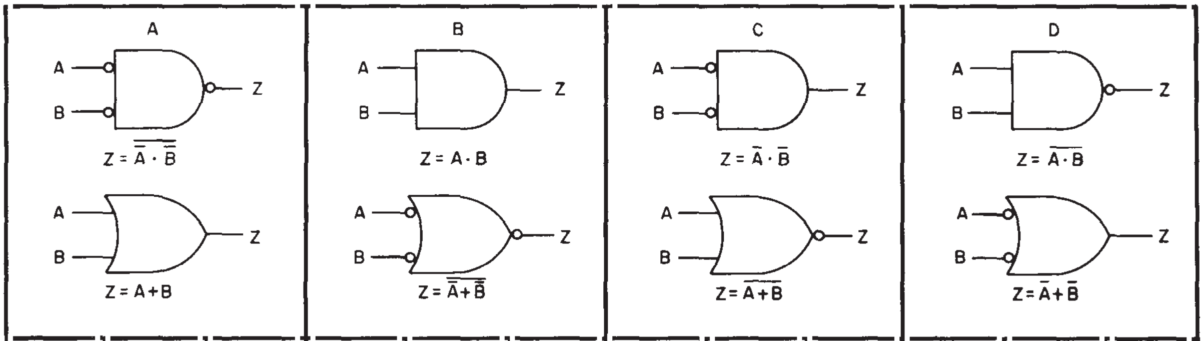
THEORY OF OPERATION

4-1. INTRODUCTION

4-2. This section describes the individual logic elements, overall counter operation, and theory of operation for each printed circuit assembly. The overall counter theory starts in Paragraph 4-44. The theory for each pc board starts in Paragraph 4-71.

4-3. LOGIC ELEMENTS

4-4. Two states exist in the binary system, 1 and 0. HIGH (H) and LOW (L) are used to represent the levels of 1 and 0. HIGH always represents the more positive level, whether it be positive or negative logic. Figure 4-1 shows four pairs of logic symbols that have the same truth tables and can be used interchangeably. The same function is perfomed by what appears to be two different logic symbols.


A
B
C
D
A
B
Z
$Z = \overline{\bar{A} \cdot \bar{B}}$
$Z = A \cdot B$
$Z = \bar{A} \cdot \bar{B}$
$Z = \overline{A \cdot B}$
$Z = A + B$
$Z = \overline{\bar{A} + \bar{B}}$
$Z = \overline{A + B}$
$Z = \bar{A} + \bar{B}$

A	B	Z	A	B	Z	A	B	Z	A	B	Z
L	L	L	L	L	L	L	L	H	L	L	H
L	H	H	L	H	L	L	H	L	L	H	H
H	L	H	H	L	L	H	L	L	H	L	H
H	H	H	H	H	H	H	H	L	H	H	L

Figure 4-1. Logic Comparison Diagrams

4-5. Logic Levels

4-6. This instrument uses three types of logic. They are:

1. Transistor-Transistor Logic (TTL)
2. Emitter-Coupled Logic (ECL)
3. Emitter-Emitter-Coupled Logic (EECL).

Digital signals have two logic states, referred to as High and Low. The voltage associated with the High or Low state is different for each logic type.

LOGIC STATE	TTL	ECL	EECL
Low	0 to +0.4V	approximately -1.5V	approximately -0.6V
High	2.4 to 5V	approximately -0.8V	approximately 0V

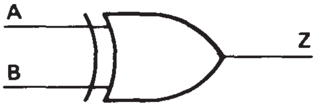
4-7. Wire-OR/Wire-AND Configuration

4-8. The wire-AND configuration applies to TTL type logic. (It may be commonly referred to as wire-OR.) In TTL, the output of an open-collector gate (one having no load resistor) can be paralleled with gates of the same type to perform this function. When the outputs are tied to the same line, any one of the gates can pull the line Low (.7V) without damaging itself. An external pull-up resistor is required.

4-9. The wire-OR configuration applies to ECL type logic. With ECL, an external resistor is not necessarily required. As with TTL, the gate outputs are connected together. In this case, however, any one of the gates can force the line High (-.7V).

4-10. Exclusive OR Gate

4-11. The output of the exclusive OR will be High if one, but not both, of the inputs is High. This can be seen in the truth table in Figure 4-2.



A	B	Z
L	L	L
L	H	H
H	L	H
H	H	L

Figure 4-2. Exclusive OR Gate

4-12. INTEGRATED CIRCUITS — THEORY OF OPERATION

4-13. Much of the circuitry used in this instrument is comprised of common logic elements: AND gates, D-Type flip-flops, JK's, etc. Other circuits may use devices that are not as familiar as those mentioned. The following paragraphs briefly describe the operation of these devices. Notice that these devices are shown functionally; i.e., they attempt to best describe the opertion of the device and may not reflect the nomenclature used by the manufacturer.

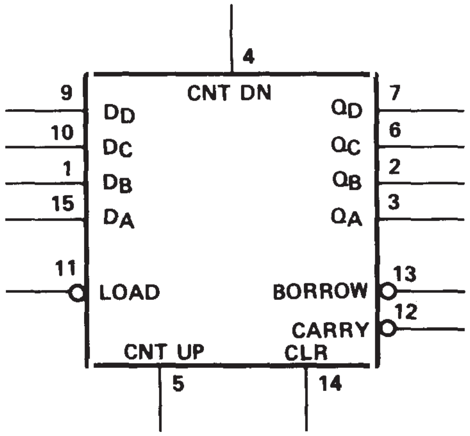
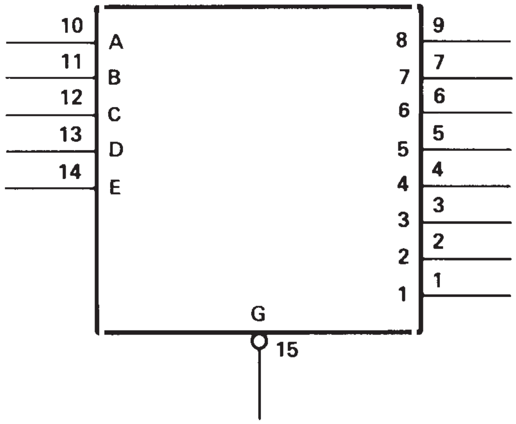


Figure 4-3. Synchronous 4-Bit Up/Down Counter, 1820-0233

4-14. Synchronous 4-Bit Up/Down Counter, 1820-0233

4-15. All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data on the data inputs while the LOAD input is Low. The output will change to agree with the data inputs. Once the Load condition is removed, the outputs can count down with each positive pulse on CNT DN or count up with each positive pulse on CNT UP. A High level on the CLR input forces all outputs Low. Borrow goes Low with an underflow condition, while CARRY goes Low with an overflow condition.



*Even through the *type* of ROMs used may be the same, the part numbers will differ with individual programs.

Figure 4-4. Read-Only Memory (ROM) 1820-0254*

4-16. Read-Only Memory (ROM) 1820-0254*

4-17. This device is a programmed, addressable memory. There are 32 storage locations, each of which is capable of storing an 8-bit character. The contents in each location is fixed. The contents of a location are placed on the output lines when the gate (G) is low and the location has been addressed with the proper input code (A,B,C,D,E lines).

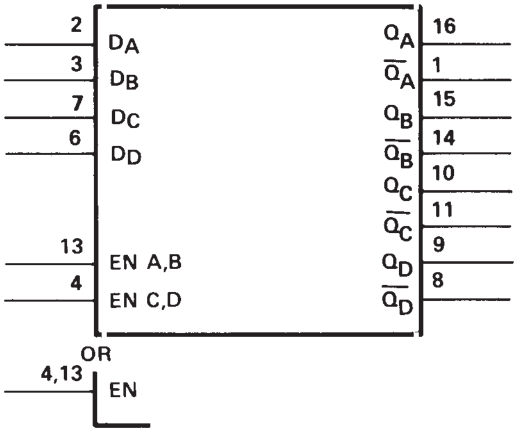


Figure 4-5. 4-Bit Bistable Latch 1820-0301

4-18. 4-Bit Bistable Latch 1820-0301

4-19. Information present at a data (D) input is transferred to the respective Q output when the enable line is High. The Q output will follow the data input as long as the enable line remains High. When the enable line goes Low, the information currently on the D inputs is retained (latched) on the Q output until the enable line returns High.

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*Even though the *type* of ROMs used may be the same, the part numbers will differ with individual programs.

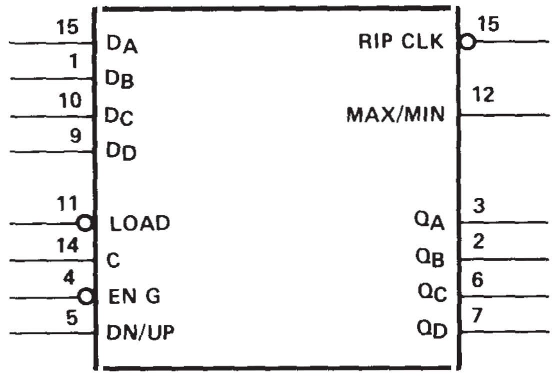
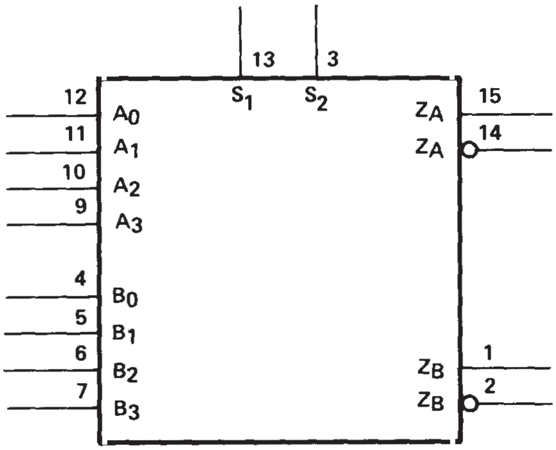


Figure 4-6. Synchronous Up/Down Counter 1820-0545

4-20. Synchronous Up/Down Counter 1820-0545

4-21. A Low on the EN G line enables the operation of this binary counter. While the LOAD input is Low, the counter can be preset to any number from 0 to 15. The Q outputs assume this number, and counting begins from that point. The state of DN/UP determines the direction of counting. If DN/UP is High, the counter counts down, when Low, it counts up. The MAX/MIN output produces a High level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The RIP CLK output produces a Low-level pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists.



S2	S1	Selects
0	0	A0 and B0
0	1	A1 and B1
1	0	A2 and B2
1	1	A3 and B3

The inputs are listed by data lines (ABCD). The schematics may show the inputs as C_0 C_1 C_2 C_3 and D_0 D_1 D_2 D_3.

Figure 4-7. Dual Four-Input Multiplexer 1820-0610

4-22. Dual Four-Input Multiplexer 1820-0610

4-23. This multiplexer selects one line from the four A inputs and one line from the four B inputs and transfers that data to the respective Z outputs. Each Z output (A or B) has an inverted and a noninverted line. The inputs to be transferred are selected by the code present on S1 and S2, as shown in the truth table of Figure 4-7.

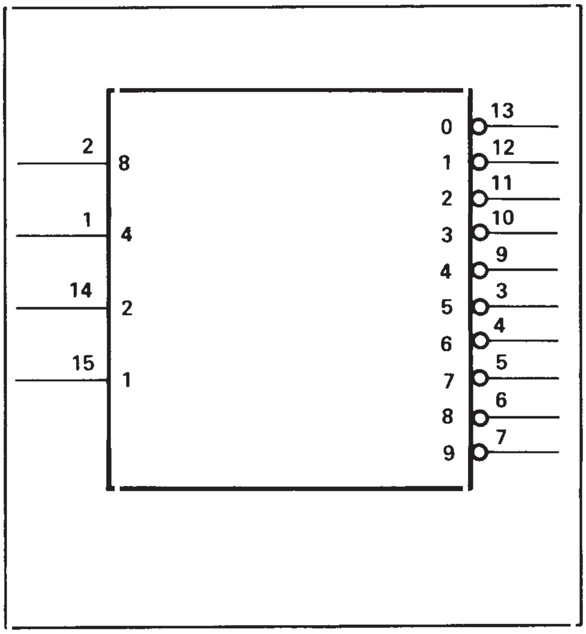


Figure 4-8. One-of-Ten Decoder 1820-0627

4-24. One-of-Ten Decoder 1820-0627

4-25. This IC converts a BCD code to a decimal equivalent. A code on the input lines (8,4,2,1) causes one of the output lines to Low. For example, a code of seven $(\frac{8421}{0111})$ pulls the "7" line Low.

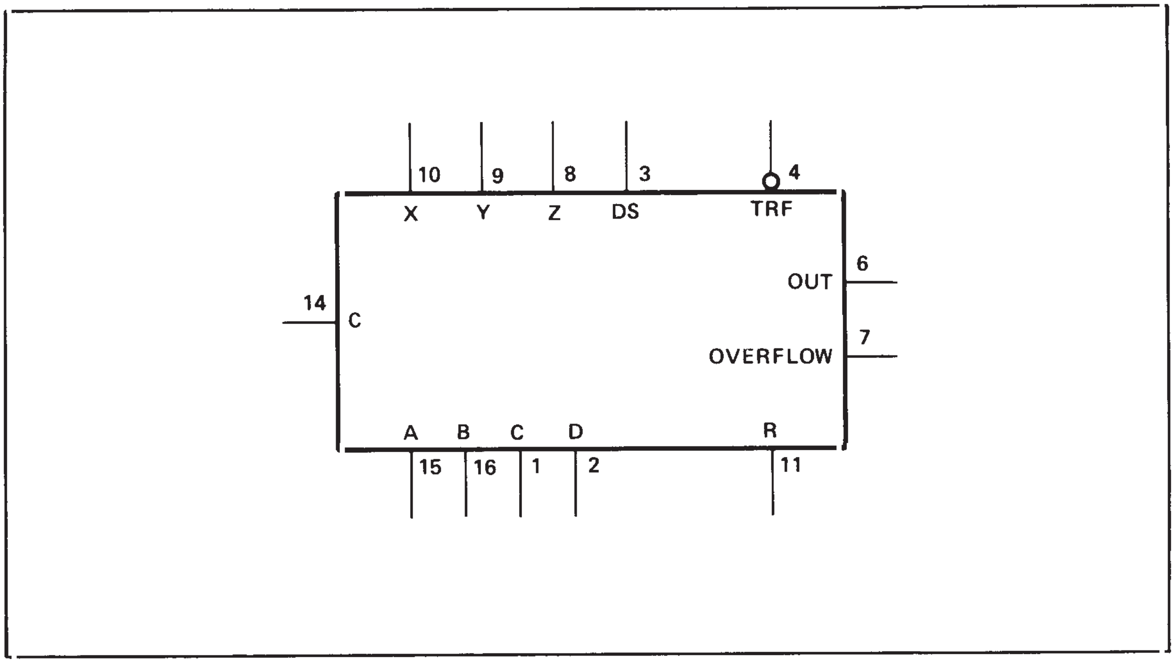


Figure 4-9. MOS Six Decade Counter 1820-0634

4-26. MOS Six Decade Counter 1820-0634

4-27. This is a 6-digit, ripple-through counter with buffer storage outputs for each decade. The circuit has one set of BCD outputs (ABCD) that may be switched from digit to digit, as determined by a decade select code (XYZ). For the counting operation, the device will advance its count on the positive going edge of the clock input (C). While counting is in progress, the decimal count of a selected decade (by means of XYZ lines) is transferred to the BCD outputs when the TRF line is held Low. The decade contents can be "scanned" and transmitted to the BCD outputs by sequentially changing the XYZ code. The High logic level is ⩾3.4V for all inputs.

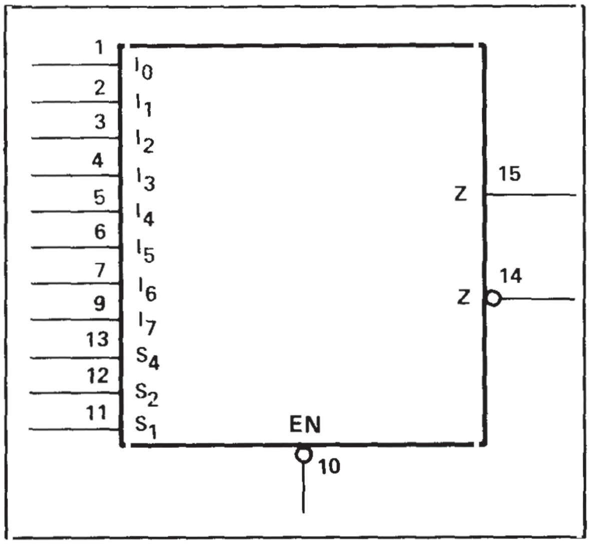


Figure 4-10. Eight-Input Multiplexer 1820-0658

4-28. Eight-Input Multiplexer 1820-0658

4-29. A Low on the EN line enables the operation of this multiplexer. A code on the select lines (S4, S2, S1) selects the corresponding input to transfer its data to the Z outputs. For example, a code of $\left(\frac{S4\;S2\;S1}{0\;\;\;1\;\;\;1}\right)$ selects the I_3 line, and the Z output (noninverted) assumes the state of I_3.

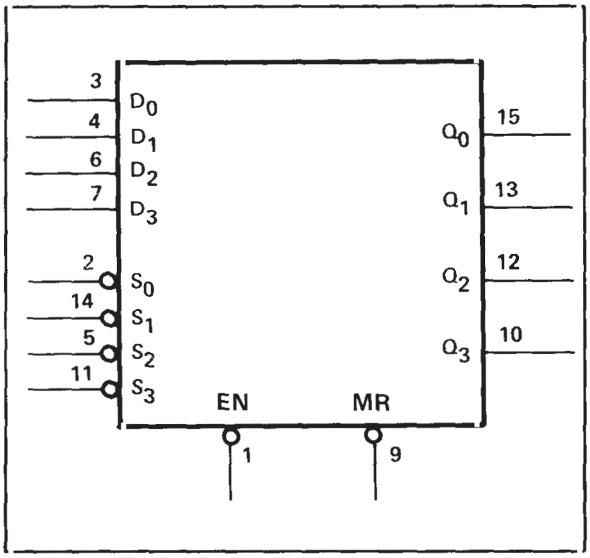


Figure 4-11. Quad Latch 1820-0701

4-30. Quad Latch 1820-0701

4-31. Information present at a data (D) input is transferred to the respective Q output when the enable line is Low and when the respective select (S) line is Low. The Q output will follow the data input as long as EN remains Low. When EN goes High the data currently on the D inputs is retained (latched) on the Q output until EN returns Low or the latch is reset (MR=Low). When the latch is reset, the Q outputs go Low.

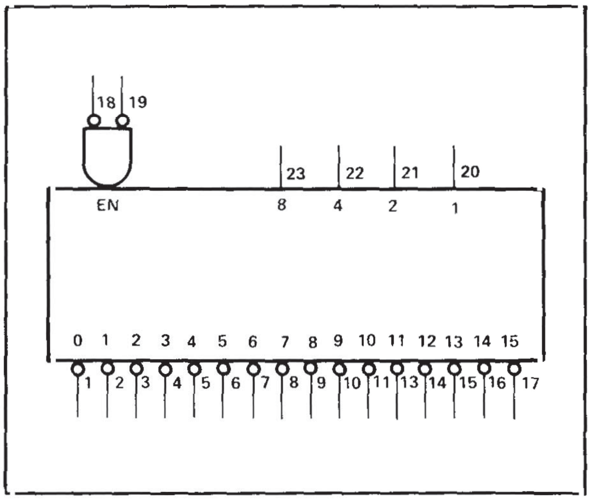


Figure 4-12. One-of-Sixteen Decoder
1820-0702

4-32. One-of-Sixteen Decoder 1820-0702

4-33. This IC converts a binary code to a decimal equivalent. When the device is enabled with two-low levels (pins 18 and 19), a code on the input lines (8,4,2,1) will pull one of the output lines Low. For example, a code of $12\left(\frac{8421}{1100}\right)$ pulls the "12" line Low.

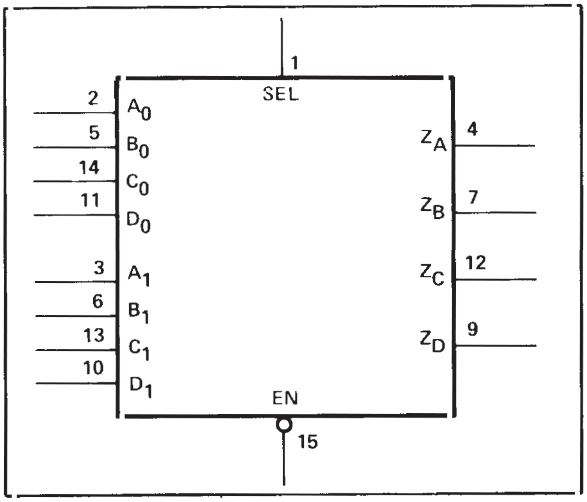


Figure 4-13. Quad Two-Input Multiplexer 1820-0710

4-34. Quad Two-Input Multiplexer 1820-0710

4-35. With the enable (EN) line Low, the multiplexer is enabled to transfer the data inputs (ABCD) directly to the output lines (Z). When SEL is a "0" (Low) the $A_0B_0C_0D_0$ inputs are selected; while the $A_1B_1C_1D_1$ inputs are selected with a "1" (High) on the SEL line.

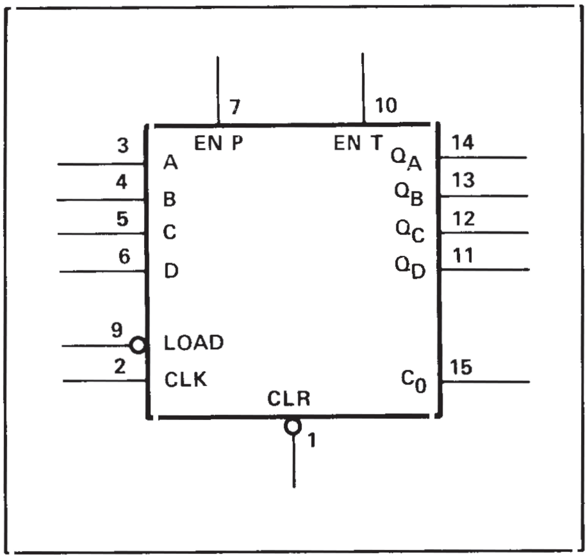


Figure 4-14. Synchronous 4-Bit Counter 1820-0716

4-36. Synchronous 4-Bit Counter 1820-0716

4-37. The two enable lines (EN P and EN T) must be High before the device can count. Each positive edge of the clock pulse advances the binary count on the Q outputs. The carry output (CO) goes High when the output reaches a count of 15 (a total of 16 clock pulses). The count can be preset to start counting from a given number. This is done by pulling the LOAD line Low and entering the desired number on the input lines (A,B,C,D).

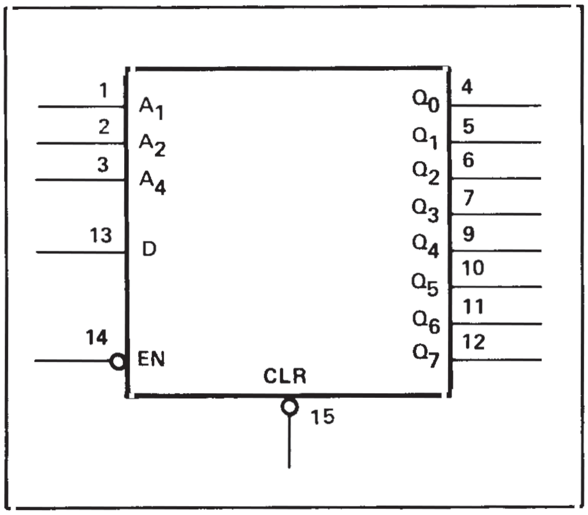


Figure 4-15. 8-Bit Addressable Latch 1820-0833

4-38. 8-Bit Addressable Latch 1820-0833

4-39. When the EN line is Low data (D) is written into the latch and will appear on only the Q that is selected by the address code. For example, an address code of 5 ($\frac{A4}{1}\frac{A2}{0}\frac{A1}{1}$) selects Q5. When EN is High, the latch is in the memory mode; i.e., all latches remain in their previous state and are unaffected by the data or address inputs.

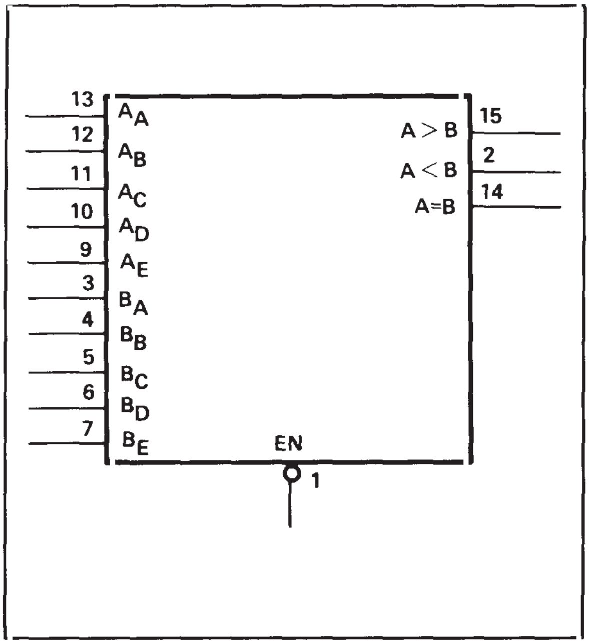


Figure 4-16. 5-Bit Comparator 1820-0904

4-40. 5-Bit Comparator 1820-0904

4-41. This IC performs a comparison between two 5-bit characters and provides three outputs to indicate the result of the comparison: less than, greater than, and equal to. A Low level on EN enables the device, and a High level forces all three outputs Low.

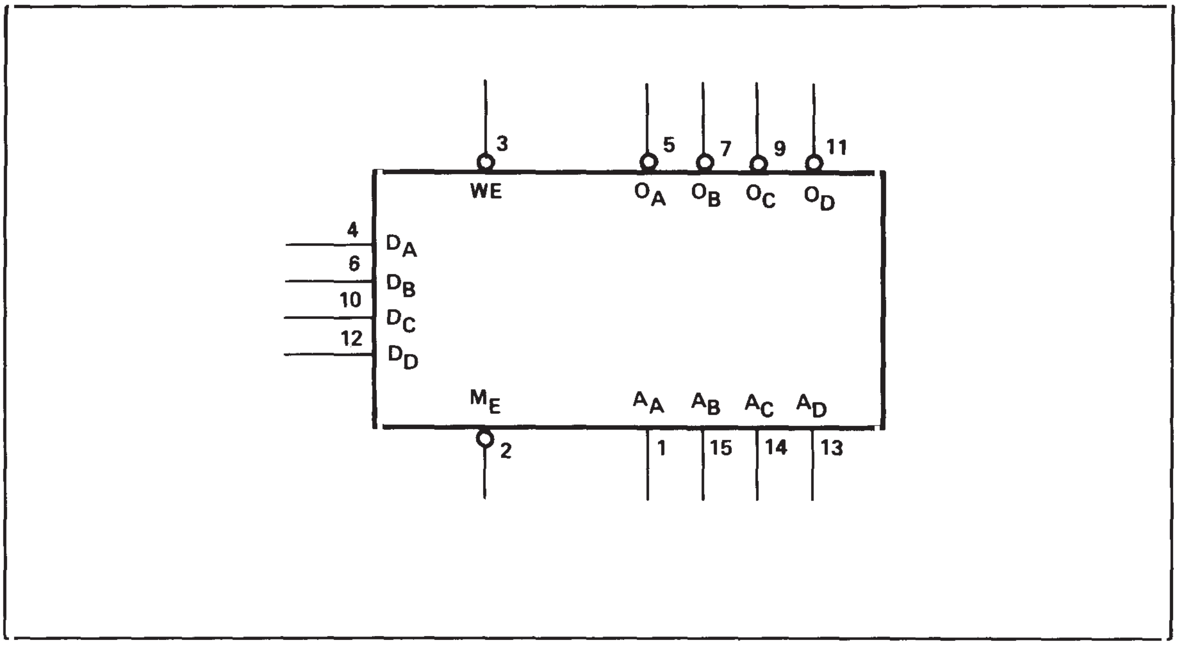


Figure 4-17. 64-Bit Read/Write Memory 1820-1028

4-42. 64-Bit Read/Write Memory 1820-1028

4-43. The memory is capable of storing 16 characters of 4-bits each. Information present at the data (D) inputs is written into the memory by addressing (A lines) the desired memory location and holding both memory enable (ME) and write enable (WE) low. The complement of the information that has been written into the memory is read out at the four output (O) lines. This is done by holding ME low, setting WE high, and addressing the desired location.

4-44. OVERALL THEORY OF OPERATION

4-45. The following paragraphs contain a general description of the counter's operation. A block diagram is provided in Section VIII for reference.

4-46. Input Assembly

4-47. The counter has two input channels, each having a frequency range of dc to 500 MHz. A two-position switch selects either X1 or X20 signal attenuation. The signal is amplified by two amplifiers: one on A3 and the other on A4. The sensitivity of the first amplifier is variable with the LEVEL pot. The second amplifier is a combination amplifier/Schmitt trigger. The outputs of the Schmitt triggers drive the gate board.

4-48. Gate

4-49. The main gate board (A9) uses three separate multiplex switches to select the proper signals for a particular measurement. Two of the switches select inputs from Channel A, Channel B, Plug-in A, Plug-in B, and 100 MHz test. These signals are termed *event counts*, where each pulse represents a count. The third switch selects the internal 500 MHz clock signal, the plug-in clock signal, or the output of the second multiplier for use in the RATIO or START Function. These signals constitute the *time counts*.

4-50. The main gate board also controls the gating of the input signal and clock signal. The main gate circuits are armed by the run down of sample rate or by the reset signal. The arming signal enables the gate to open on the next input cycle. During the time the main gate is open, the event signal and time signal are divided by 20 in the A9 scalers. The signal levels are shifted from EECL to T^2L before the signals are sent to the remainder of the scalers on A11.

4-51. Scalers

4-52. The scalers, or dividers, can be considered as a string of 13, individual, divide-by-10 stages. When the main gate opens, The Event Scaler begins accumulating event counts (e.g., Channel A pulses), and the Time Scaler begins accumulating time counts (e.g., internal 500 MHz pulses). Before the decades can output their data, the accumulation of counts must end with the conclusion of the gate time. A method for determining the end of the gate time is, therefore, needed.

4-53. The GATE TIME switch sends the A11 board a different 4-line code for each of its switch positions. The code is passed through a switch to a strobe coder, where it is decoded to a 16-line code. This code addresses one of the Time Scaler decades to output its data. The Time Scaler accumulates 500 MHz clock pulses until a "5" appears on the output of the addressed decade. Any division of 500 MHz by a power of 10 is also a division of 1 second by the same power. Therefore, when a "5" first appears on the output of the addressed decade, the elapsed time (gate time) is the selected multiple of 1 second. For example, if 5×10^8 counts accumulate in 1 second (500 MHz), 1 ms will accumulate 5×10^5 counts. Once a 5 is detected, the main gate closes on the next Channel A input pulse.

4-54. Each decade of the time and events scalers now contains one digit of information, which can be sent to the processor as a 4-line code. This is done by sequentially addressing each decade to output is stored data. The address codes are supplied to the A11 switch by a 16-bit counter: the Denominator Register Counter (DRC) located on the A13 board.

4-55. Arithmetic Processor

4-56. The data from the time and events scalers on A11 are strobed into the A13 board, where the data is manipulated in such a manner as to double the time data. The Adder/Subtracter circuits perform this operation by adding the time data to itself. This, in effect, produces a 1 GHz time base frequency. This results in keeeping the measurement in terms of events/nanosecond.

4-57. Once this is accomplished, the DRC again strobes events data into the A13 board. The events data is now located in the Denominator Register and the doubled time data is located in the Numerator Register. This sequence of events occurs in every frequency, period, or time interval measurement.

4-58. The arithemetic process consists of dividing the contents of the Denominator Register into the contents of the Numerator Register $\left(\frac{\text{NR}}{\text{DR}}\right)$. For mainframe measurements involving a gate time, the process is always a division. The contents of the registers, therefore, may have to be exchanged, depending on the type of measurement being made. For example, in a period measurements, the division needs to be $\frac{\text{time}}{\text{events}}$ $\left(\frac{1}{f} = \text{period}\right)$; therefore, no exchange is needed, since time data is in NR and events data is in DR. In a frequency measurement, however, the division needs to be $\frac{\text{events}}{\text{time}}$ (cycles/sec = frequency); therefore, the registers must exchange their data to perform the correct division.

4-59. Shifting data from one register to another involves "reading" the data out of each register, storing it in a latch, and then "writing" the data back into the other register. Once both groups of data are positioned in their correct register, the Adder/Subtracter Register accomplishes the division by performing a *series of successive subtractions.* Each time this register completes a successful subtraction, it increments the Quotient Multiplier Counter. Once this counter determines the total number of successful subtractions in a particular digit, it transfers that data into the Quotient Register and continues the subtraction process for the next significant digit. After all subtractions are complete, the Quotient Register shifts the data into the Denominator Register, where it can be distributed to the display or interface bus.

4-60. The Quotient Multiplier Storage circuit is used to determine the unit multiplier (K, M, n, etc.) of the result. The Digit Storage defines the number of significant digits to be computed. The digit counter (DC) is compared with Digit Storage (DS). When DS = DC, the division routine is complete. The Decimal Point Locator for the Result (DPLR) is a counter that keeps track of the decimal point location in the result. The Decimal Point Locator for K is also a counter and is used to keep track of decimal point information from the plug-in.

4-61. State Control Section

4-62. To this point, the counter has been described in terms of signal or data flow. To control the intricacies of the data flow, a hierarchy of commands and controls are needed. Depending on the operating mode being used, the counter uses a particular program which outputs the commands to the various assemblies in the counter. All possible program steps are contained in the ROMs (Read Only Memories), located on A15 (lower left of block diagram). The flow within the program is determined by generating a series of commands and then altering the program flow based on the results.

4-63. The ROMs output two sets of program codes: one set when the MSB address line is High and the other set when MSB is Low. The first set is chosen by address codes, which selects one out of 128 possible ROM address locations. The second set of program codes is chosen from a second set of ROM address locations. Each address location contains a specific program code.

4-64. The first set of program codes is stored in the Word Doubler Storage circuits (A14, A15) until the second set is received. The two sets are then fed to the Combinational Logic circuitry on A15 where the program codes combine to produce about 50 *command lines.* Some of these command lines come directly from the ROMs. As previously mentioned, the command lines control various assemblies to perform particular functions. The results of the function are carried on lines called *qualifier lines.* The A10, A11, A13, A14, and A15 boards contain combinational logic circuits which generate the qualifier signals that are sent to the Qualifier Select Logic. The Qualifier Select Logic examines only one qualifier line. The line it examines is determined by the 6-line output of Word Doubler Storage.

4-65. The Word Doubler Storage circuits provide 6 address lines from the previously addressed program codes. These 6 lines contain a two-digit octal code, which performs two functions: (1) it provides the two most significant digits of a 3-digit code, which will be used to address the ROMs to the next address in the program, and (2) it selects the specific qualifier line that the Qualifier Select Logic will output on the LSB (least significant bit) line. The LSB line is the third digit in the 3-digit ROM address code. Therefore, even though there is a definite arrangement of address codes in a particular program, the program flow can be modified by the state of the LSB line, which is the result of the last set of commands.

4-66. Oscillator Circuits

4-67. The internal time base for the counter is supplied by a 10 MHz, oven-controlled oscillator. The 10 MHz signal feeds through a pulse shaper and buffer to J2 on the rear panel and to the plug-in circuits. It also feeds into a times 50 multiplier circuit (X2, X5, X5). The result is a 500 MHz signal that is used as the counter's time base. Depending on the state of a status line, the 500 MHz clock may be jittered to provide true time interval averaging. A portion of the signal is tapped off after the X10 stage. This 100 MHz signal is used for self-check.

4-68. An external oscillator signal may be applied to J1, EXT FREQ STD INPUT. This signal is sent through a circuit that phase locks the internal oscillator to the external standard.

4-69. Power Supplies

4-70. The power supply circuits are contained on A6 and A7 assemblies. The suppplies are short-circuit proof and will automatically shut down if operated at too high a temperature. A sophisticated ground system requires that each supply line be measured to its own return line, e.g., +5V and +5V RET (return).

4-71. CIRCUIT BOARD THEORY

4-72. The following paragraphs describe the operation of each circuit board in the counter. Refer to the appropriate schematic in Section VIII while reading this material. If the reader's purpose is to learn the instrument's operation, rather than a specific part of the counter, it may be helpful to read the material in the suggested order: A3, A4, A9, A11, A10, A13, A15, A14, A1, and A2.

4-73. A1 and A2 Display Assemblies

4-74. Assemblies A1 and A2 combine the circuits necessary to display all measurement data, minus sign, and annunciators. The A1 board contains the digit LEDs, which are placed in sockets, and the annunciators, which are backlighted by incandescent lamps. A2 contains the character generator and its drivers, the decimal point decoder, and the digit enable circuit with its drivers. The annunciator decoding is shared between the two boards.

4-75. STROBING TECHNIQUE. The result of the measurement is displayed by using a strobing technique. That is, only one digit of the displayed number is on at any one time. One digit is displayed and then removed; then the next digit is displayed and removed. This process continues until all digits have been shown. The strobing process occurs at a faster rate than the eye can detect, so the display appears continuously lit. Character generator A2U6 controls the digit (numeric character) to be displayed, while A2U1 controls the placement of the digit in the display.

4-76. CHARACTER GENERATION. The BCD data lines (entitled DR A,B,C,D) carry the digit information from the DR RAM (A13) to the character generator, A2U6. The BCD lines are decoded by A2U6 into segment lines for the LEDs. Each segment line enables an individual segment (or diode) of the LED display; therefore, several of these output lines may be High when displaying a specific digit. Transistors A2Q1 through A2Q7 are used as drivers for the segment lines. A2Q8 drives the decimal point line (described later).

4-77. Since these lines connect to the same segment in each digit, the turn-on of these digits must also be controlled. The same counter codes that address the data from the DR RAM are also sent to A2U1. They are then decoded to turn on each digit, in sequence, from LSB to MSB. Eleven codes are needed to display all possible digits; therefore, the DRC codes are normally stepped from 0 to 10.

4-78. As the DR counter steps through its codes, the data lines (DR) and DRC lines change codes and each digit is displayed. The counter steps through all 11 codes, regardless of the number of digits displayed. A DR code of 15 will blank those columns that have no digits. If the measurement requires a minus sign, the DRC lines provide an additional code of 11. This causes A2U1(13) to go Low. This results in A2Q9 driving the anode of A1DS1 and, at the same time, enables A2U4B and A2Q7 to drive the cathode.

A1 and A2 Continued

4-79. When the $\overline{\text{LAMP TEST}}$ line goes Low, it forces all outputs of A2U1 to go High, which lights all segments of the display. This line also enables A2U4A to light the decimal points. During lamp test, the DRC lines step through all 16 codes (0-15).

4-80. ENABLE CIRCUITS FOR CHARACTER GENERATION. Before A2U1 can operate, both G1 and G2 inputs must be Low. Likewise, the RBO line of A2U6 must be High before the device can drive the segments. During the process cycle, the DISP CLK EN line is Low. This resets A2U7A and places a High on the G2 input of A2U1, thereby turning it off. When the display cycle begins, DISP CLK EN goes High and releases the reset position. Also, the DRC code returns to zero. This causes a High-to-Low transition on the DRC D line, which clocks A2U7A, a retriggerable one-shot multivibrator. The "time-out" for this one-shot is longer than the time required to strobe the display. If, for some reason, the DRC codes become inactive, the one-shot will time-out and turn off A2U1 by placing a High on G2.

4-81. A new digit is clocked out of the DR RAM with each negative transition of DISP CLK. When this line goes Low, however, it triggers A2U7B, a one-shot multivibrator. This produces a High on the Q output to turn off A2U1 via the G1 line. It also produces a Low on the $\overline{Q}$ output, which blanks A2U6 and forces its output lines Low. This same pulse also shuts off the decimal point by placing a Low on A2U3(3). The duration of these pulses is controlled by R26 and is in the order of about 5 to 50 μs. This provides enough time for the RAM circuits to settle after selecting another digit. Once the one-shot times out, the Q output of A2U7B returns Low to enable A2U1 and the $\overline{Q}$ output returns High to enable A2U6.

4-82. DECIMAL POINT GENERATION. As previously stated, each DRC code represents a specific position in the display. This is also true of the decimal point code, which is transferred on the DP A,B,C,D lines. The position of the decimal point in the display has been determined in the process cycle. The code is placed on the DP lines for the duration of the display cycle. These lines are connected to one side of four exclusive OR gates (A2U2), while the other side of these gates is connected to the DRC lines. When the two codes are equal, all inputs to A2U3B go Low. This enables A2U3A and A2U4A to turn on A2Q8 and light the decimal point.

4-83. ANNUNCIATOR CIRCUITS. The multipliers for the measurement (M, K, μ, etc.) are generated by a decoding network, comprised of A2U5A,B, and C, A1U2A and B, and A1U1. Since this counter can make period measurements in, say, kiloseconds or frequency measurements in terms of Micro Hertz, the decoding circuits must meet these criteria. Because, A1U1 is an open-collector 4-to-10 line decoder, its outputs can be wired together or to additional circuitry. A table is provided with the schematic to explain the functional decoding of this circuit. The other annunciators are driven directly or through individual buffers. NAND gate A2U4D ensures that the ARM light is on only when the GATE light is off.

4-84. A3 Input Attenuator

4-85. The Input Attenuator consists of two input channels. The channels are completely separate with each input having ac or dc coupling, an attenuator network, selectable 50Ω or 1MΩ impedance, level control, slope selection, and high frequency amplifier.

4-86. CIRCUIT THEORY. The circuit theory describes only channel A, since Channel B is analogous. The signal entering J2 is sent directly through S1 or through coupling capacitor C1, which blocks the signal's dc component. S4 selects R3 for 50 ohm input impedance and R4 and R5 for 1M ohm input impedance. When S3 is in the COM A position and S4 is set to 50Ω, the two channels are connected together and R1 helps maintain the 50 ohm input for each channel. In SEP, the inputs are isolated from each other, R1 is bypassed, and the impedance switches can be set separately. S5 ATTEN switch passes the signal directly in X1 or when in X10 attenuates the signal by 10 through divider network R4 and R5.

4-87. The signal is then routed to the amplifier through one of two paths, depending on the frequency. Frequencies below 10 MHz, including dc, pass through the FET impedance converter (source follower). Higher frequencies are bypassed around the FET through C9. The FET's input is protected at low frequencies by R1, CR1, and CR2. The amplifier U2 has differential inputs and outputs and has a gain (single ended) of about 3. One input accepts the signal and the other accepts the dc level (±1.3V) from the LEVEL pot (via A4U4). The amplifier is biased by 5 current sources: Q3,Q4, R51, and R56. R44 adjusts the amplifier bias (-70 mV at pin 15).

4-88. The counter may trigger on either slope of the input signal. The SLOPE switch, S8, determines this by controlling the output polarities of U2. If S8 is placed to +, the outputs of U2 will be 180° out of phase with their respective inputs. When S8 is placed to –, the outputs of U2 will be in phase with their respective inputs.

4-89. A4 Input Trigger

4-90. The Input Trigger assembly provides additional amplification of the input signals before they are sent to the counting circuits. The differential output of A3 enters the board on pin P1A(4) and P1A(7) and goes to the inputs of U2. R2 adjusts the trigger output of U2 for 50% duty cycle with a sine wave input. The amplifier has a gain of about 3.5 and contains a Schmitt trigger, which shapes the lower frequencies into fast rise time square waves. R15, 21, 20, 25, 28, 31, and 32 are current source resistors for U2, while R16 adjusts the bias.

4-91. The trigger output of U2(13) is a negative pulse about -0.7V in amplitude. Pulse width depends on the input signal and on the setting of R2. Pulse amplitude is controlled by the trigger current source at pin 14.

4-92. U4 is a buffer amplifier, which accepts dc levels from the front panel LEVEL control or the rear panel level inputs. R11 corrects for offset voltages in A3U2 when the SLOPE switch position is changed. The output of U4 also connects to U2's current source and turns off the amplifier when the signal level exceeds +3.5 Vdc.

4-93. A5 Front Panel Interconnect

4-94. This assembly provides an interconnection between the A4 Input Trigger Assembly and the A16 Motherboard Assembly. It also contains two coax cables for transferring the channel A and channel B signals to the A9 Main Gate Assembly.

4-95. A6 Switching Regulator

4-96. The A6 assembly provides +5V Display, +5V, and -5.2V for distribution throughout the instrument.

4-97. +5V DISPLAY SUPPLY. Rectifier diodes CR1 and CR2 receive 17V rms from the secondary of T1. C3 filters the resultant 8 Vdc. When the POWER switch is ON, P1B(7) is at ground potential. This causes CR4 to conduct and turn on Q2, which places 8V on U3's input. CR6 also conducts through R5, causing Q3 to turn off. U3 regulates the output voltage at +5V and provides fold back current protection. C7, C11, and C13 filter ac signals from U3. If the POWER switch is set to STANDBY or should S1 open, CR4 no longer conducts and Q2 turns off U3. With CR6 also turned off, Q3 is allowed to turn on through R5. This places a 100 ohm load on the 8V unregulated line, which helps keep the high line peak voltage within the voltage rating of C3.

4-98. THERMAL AND ELECTRONIC SHUTDOWN. S1 is a thermal switch that is mounted on U2. P1B(7) connects to the POWER switch and is at ground potential with the switch set to ON. When S1 is closed, there is .7V on the base of Q1, because of CR3. If the switch opens, due to high heat sink temperature, CR3 no longer conducts. This allows Q1 to turn on. Q1's collector voltage drops to a few tenths of a volt, which allows base current to flow in both Q5 and Q6 and causes them to turn on. Q6 turns on Q8. Q5 and Q8 turn on transistors inside U2 and U1, respectively, which turn off their internal current sources and shut off the two regulators. S1 shuts off the +5V DISPLAY supply by turning off CR4 and Q2. These three supplies are also turned off if the POWER switch is placed in STANDBY.

4-99. +5V REG SUPPLY. The +5V REG and -5.2V REG supplies receive power from the 22.3V rms secondary of T1. F1 and F2 provide protection for the rectifier circuits, while C1 and C2 prevent internally generated EMI from entering the power cord. CR5 rectifies the ac into +14 Vdc and -14 Vdc supplies. The voltages are filtered by C4-C6. U2 is connected as a switching type voltage regulator, whose output of +5V varies about 30 mV plus and minus at about 18 kHz. Output current is supplied through Q9 current boost.

A6 Continued

4-100. When U2 turns on, it draws current through R25. This produces a voltage drop across R25 and turns on Q9. The output of Q9 charges L1 and C16 and increases the voltage on the output. When the output voltage reaches about 30 mV above +5V, it is sensed at U2(5), via the short on the motherboard. U2 shuts off current through R25, thereby shutting off Q9. The field around L1 collapses and causes "catching" diode CR10 to conduct. C16 also discharges until the output voltage drops to about 30 mV below +5V. This voltage is again sensed at U2(5) and Q9 is again turned on. The values of L1 and C16 help determine the switching rate. Q11 limits the output current of U2 during Q9 turn on or should Q9 fail and the regulator attempts to output more current than it is capable of delivering. CR8 and CR9 serve as clamping diodes and prevent the internal circuits of U2 from saturating and causing a slower switching rate.

4-101. Bi-directional Crowbar. Should the output voltage become excessive due to a failure in the supply (e.g., Q9 shorted), the crowbar prevents damage to the counter by shorting the output line to common. This is done when the output voltage reaches +6.3V or is shorted to a negative voltage. In either case, CR16 and CR17 conduct and trigger triac CR14. This will probably cause F3 to open.

4-102. Sense Line Clamp. The power supply boards should not be removed with the power cord connected. If this occurs, the sense line is disconnected from the +5V output (short on motherboard). Even though the board is removed, power is supplied by the filter capacitors, C4 and C6; and the internal voltage tends to approach +14V, possibly causing damage. To prevent this, diode CR10 conducts and resembles the motherboard short. This regulates the supply at about +5.7V until the stored voltage bleeds off.

4-103. Current Limit. Q4 and Q7 form an equivalent SCR. If the output draws too much current (≈6A), the current sense resistor R7 developes a voltage drop sufficient to turn on Q4. Q4 turns on Q7, which causes Q4 to turn on even harder. The result is that the internal circuits of U2 are deprived of current and shut down the output of U2. Should Q5 turn on (POWER switch to STANDBY or S1 open), it causes the current to flow through Q5 instead of Q4 and Q7. Once this occurs, Q4 and Q7 can be considered "unlatched."

4-104. -5.2V REG SUPPLY. This supply is similar in operation to the +5V REG supply. The only differences being that R32 substitutes for Q11 and R34 as a peak current limiter, and CR7 substitutes for Q4 and Q7. As with the other supply, too much current through R12 triggers the SCR. This places -14V on CR7's anode, which draws current out of U2. The result is that U4's output and Q10 turn off. Should Q6 turn on (POWER switch to STANDBY or S1 open), it causes current to flow through Q8 instead of CR7. When the anode current of CR7 goes below its holding current (≈5 mA), the SCR unlatches. When Q8 turns off again, the time constant of C10 and R21, 22, and 24 slows the $\frac{dv}{dt}$ on CR7. This prevents the SCR from turning on with a sudden change in anode voltage.

4-105. A7 Linear Regulator

4-106. The A7 assembly provides +12V, +15V, and -15V for distribution throughout the instrument.

4-107. +12V OSCILLATOR SUPPLY. The 12V, 22V, and 11V supplies receive power from the 36V rms secondary of T1. F1 and F2 protect the rectifier circuits, while C1 and C2 prevent internally generated EMI from entering the power cord. CR2 rectifies the ac into +22 Vdc and -22 Vdc supplies. The voltages are filtered by C6–C9, while R6 and R7 serve as bleeder resistors. The +22V unregulated supply is sent out on P1A(10).

4-108. U2 is the 15V regulator whose output is filtered by C18 and C21. R21 and CR8 step the voltage down to +11V regulated and C14 filters the output.

4-109. Regulator U2 uses foldback current limiting and is thermal protected. Should the 12V output short to common, the voltage drops to zero and the current "folds back" to a safe value of current. If, in addition, the IC's temperature increases, the output shuts down completely, turning on again once the chip has cooled down. These actions prevent the supply from short-circuit damage. The +22V supply continues to supply power to the oscillator circuits with the POWER switch set to STANDBY or when the other supplies have shut down due to high temperature.

4-110. THERMAL AND ELECTRONIC SHUTDOWN. S1 is a thermal switch that is mounted on U4. P1B($\overline{6}$) connects to the POWER switch and is at ground potential with the switch set to ON. When S1 is closed, there is .7V on the base of Q3, because of CR3. If the switch opens, due to the high heat sink temperature, CR3 no longer conducts. This allow Q3 to turn on. Q3's collector voltage drops to a few tenths of a volt, which allows base current to flow in Q4 and causes it to turn on. Q4 and CR6 turn on transistors inside U1 and U4, respectively, which turn off their internal current sources and shuts off the two regulators. S1 shuts off the +20V REG supply by turning off Q2. These three supplies are also turned off if the POWER switch is placed in STANDBY.

4-111. +15V SUPPLY. The +22V line supplies input voltage to U1 pin 3. The +15 regulated output voltage is present at P1A(8,$\overline{8}$), via Q5 and R28. The motherboard sends this voltage back to P1A($\overline{7}$), where it is sent to U1(5) as the *sense* voltage.

4-112. Any voltage change on the sense line is compensated for by a subsequent change in output current in a direction necessary to counteract the change in output voltage. Since the regulated output of U1 is unable to supply high current to the +15V load, it is used as base drive for Q5 current boost. As the load increases, the base current increases, and Q5 draws more load current from the +22V supply. Should the load draw too much current, as in the case of a short, Q7 (normally off) conducts via R22. The collector of Q7 sinks current from the internal circuits in U1 that would normally drive Q5. Depriving Q5 of base current drops the output current to some nominal value, hence, foldback.

4-113. Sense Line Clamp. The power supply boards should not be removed with the power cord connected. If this occurs, the sense line is disconnected from the +15V output (short on motherboard). Even though the board is removed, power is supplied by the filter capacitors, C6 and C8; and the internal voltage tends to approach +22V, possibly causing damage. To prevent this, diode CR12 conducts and resembles the motherboard short. This regulates the supply at +15.7V until the stored voltage bleeds off.

4-114. -15V SUPPLY. The -15V supply is similar to the +15V supply; therefore, only the differences will be described. CR6 is used as the shutdown control for U4. With shutdown, U4's output turns off Q6.

4-115. +20V REG SUPPLY. Diode assembly CR1 rectifies the 22V rms voltage into 28 Vdc, which is filtered by C4. U3 is a +15V regulator whose common side is held at +5V. The result is a regulated +20V output. CR10 clamps the common terminal to the output in the event of a short to common. This prevents reverse biasing of circuits internal to U3, preventing damage to the IC.

4-116. A8 PLL Multiplier Noise Generator

4-117. The A8 assembly performs several processes, all of which pertain to the oscillator signal. The main function is to accept the internal 10 MHz oscillator signal and from it produce the 500 MHz time base signal. Other signals derived from the 10 MHz input are the 100 MHz test signal, used for the Check Mode; an amplified 10 MHz signal for the rear panel; and another amplified 10 MHz signal for the plug-in accessories. Another function of the board is to phase lock the internal oscillator signal to an external reference. At appropriate times, the board also places white noise on the time base signal, thereby preventing a harmonic relationship between the time base signal and input signal.

4-118. INPUT AND MULTIPLIER CIRCUITS. The 10 MHz oscillator signal enters differential amplifier U3, which serves as an isolation amplifier. This stage prevents changing load currents from affecting the oscillator, itself. One output of the amplifier, pin 6 (TP1), is decoupled by C15 and sets the bias of Q4, 5, and 6 at 8.5 to 9 Vdc. These three transistors form one side of a differential amplifier, while the other side, Q7, accepts the output signal from U3 pin 8 (TP2).

4-119. Output Amplifiers. The output of U3 is transferred from the emitter of Q7 to the emitters of the other three transistors, which constitutes a common base configuration for these stages. There are four outputs from these stages. Q7 provides 10 MHz to the rear panel through an impedance matching network, comprised of L7, C30, and C31 (TP5). Zener diode CR14 prevents the output signal from reaching too high of a level when J2 is not loaded with 50 ohms. Another stage, Q6, sends 10 MHz to the plug-in through a similar circuit, consisting of CR15, L8, and C32 (TP6). The remaining two signals are sent to the phase detector circuit and the multiplier circuits.

4-120. Multiplier Circuits. The 10 MHz signal from Q5 feeds into a tank circuit, consisting of L9-11, C24, C26, C29, and CR12. This circuit presents two signals, 180 degrees out of phase, to the bases of Q8 and Q9. The transistors form a full-wave rectifier circuit and have the effect of doubling the frequency, while providing current gain. The resultant 20 MHz signal (TP14) is smoothed by L12 and C39, before being amplified in U5. The output signal at U5(6) feeds into the tank circuit of C42, C43, and L13. It is then fed through coupling capacitor C46 (TP15) and into the X5 multiplier of U6B, C50, C52, and L14. The multiplier output is a current square wave, which are high in odd harmonics. Tuning capacitor C52 sets the tank circuit to select the 5th harmonic of the fundamental. The resultant 100 MHz output (TP16) is amplified and filtered by U6A, C56, C57, and L15. The gain of this stage can be varied by R81 (RA). Emitter follower Q17 sends the 100 MHz signal (TP17) off the board for use as a test signal during the check mode.

4-121. The collector of Q17 passes the signal to a phase shifter circuit, comprised of L17, L18, and C68. Adjusting C68 varies the phase relationship between the 100 MHz signal and the 500 MHz signal. The 100 MHz signal can be shifted ±36°, which is 360° with respect to 500 MHz (72° x 5 = 360°). This means a full period of adjustment for synchronization between the two signals. When in the Check Mode, the adjustment eliminates the ±2 ns error incurred in a time internal measurement.

4-122. The 100 MHz signal is amplified by U7B, which uses L19 as a load. The signal passes through coupling capacitor C74, before being further amplified in U7A. The gain of U7A is controlled by R99 (RB). The last stage switches current between output transistors and produces square waves of current, which are high in odd harmonics. A quarter wave length transmission line (etched on board) and C67 (CF) tune the 500 MHz output signal (TP18). Further filtering is provided by C65, L16, C60, and C61. The final stages of amplification are provided by Q19 and Q21.

4-123. During totalize, Channel C events, or a ratio measurement, A8 turns off the 500 MHz time base signal. When the $\overline{\text{500 MHz OFF}}$ line goes low (-2V from +2V), it turns on CR19 and CR20. The diodes sink collector current from Q18 and Q20. This turns off Q19 and Q21, since they no longer receive any base current.

4-124. NOISE GENERATOR. No noise is generated when the $\overline{\text{NOISE CONTROL}}$ line is High. At this time, both Q1 and Q2 are turned on. The collector of Q2 places -15V on the cathodes of CR5 and CR6, which results in biasing U8 and U9 out of their operating range.

4-125. Once the $\overline{\text{NOISE CONTROL}}$ line goes Low, it turns on CR1 and places the emitter of Q1 at about 0.7V. This turns off Q1 and Q2 and turns on U9 and U8. The noise generated from Zener diode CR2 is amplified by U9. The noise signal couples to U8 through C12 and C11 and is amplified by U8. The cathode of peak detector CR7 sits at about 2V. The noise, therefore, must be at least -2.7V for the diode to conduct. Any noise greater than this passes through the diode and is filtered into an average dc voltage by C20 (TP12). The higher the noise, the more negative this voltage becomes. An increase of negative voltage tends to turn off Q3, thereby increasing its drain resistance. This results in more of U9's output signal being fed back to its inverting input (pin 2) and causes a corresponding drop in output voltage. The output of U8, then, is constant, due to automatic gain control.

4-126. The output noise of U8 passes through R23, C21, and R41 to the cathode of the voltage variable capacitor, CR12. This capacitor is part of a 10 MHz tank circuit, comprised of C24, C26, C29, and L9-11. As the erratic changes in noise voltage affect CR12's capacitance, the phase of the 10 MHz signal shifts rapidly. The result is a 500 MHz time base signal that is phase modulated so rapidly and erratically that it cannot be harmonically related to any input signal.

4-127. PHASE LOCK LOOP. An external signal applied to the rear panel jack enters the board on J1. Limiting diodes CR3 and CR4 prevent excessive voltages from damaging the input circuits. The first two inverters, U2B and U2A, form a feedback trigger circuit and prevent noise from entering the circuits when no input is present. The output of U2A also feeds U2C and a delay circuit, formed by R21 and C17. The time difference between these two signals produces a positive voltage spike on U2D(15) and a negative voltage spike on U2D(9). These pulses are amplified and inverted in U1.

4-128. The phase detector circuit conducts during the time these pulses are present. During conduction, the circuit passes a small segment of the internal 10 MHz oscillator signal, which charges C33 to the value sampled. Each subsequent sample either adds to the previous charge or subtracts from it. A composite picture of many samples appears as a sine wave of the difference frequency.

4-129. When the difference frequency is too high or when the circuit is phase locked, the ac signal at TP10 is zero. At this time, Q14 and Q15 are turned on and force Q16 off. This places a High on the $\overline{\text{LAMP TEST}}$ line. The current drawn through Q14 turns on Q11, which results in shutting off Q10.

4-130. When the signal at TP10 is at a frequency that can be locked and the circuits are attempting to lock, the signal's amplitude is sufficient to drive the unlocked detector, Q12 and Q13. Diodes CR17 and CR18 pass only the positive going portions of the signal. C81 charges to a more positive level than before, which causes Q14 to turn off. Since no collector current is present, Q15 turns off, allowing Q16 to turn on and pull the $\overline{\text{LAMP TEST}}$ line Low. The gate of Q10 becomes more positive, since Q11 is also off, and allows the FET to pass the signal to the VCO on A18. Using this signal, the internal oscillator adjusts itself until it locks to the external standard.

4-131. Once the circuit locks, it opens FET Q10 and adds low pass filter R55, C45, C49, and R74 to the VCO signal line (TP11). This reduces any noise on the external standard line, connected to the back of the counter, and prevents miscounting. Rear panel switch S9 (FREQUENCY STANDARD INT-EXT) controls whether an external signal applied to the rear panel EXT FREQ STD input is used to control the counter. Q22 prevents the counter from operating off of the internal oscillator when in the EXT STD mode and the external frequency is lost or disconnected. When S9 is set to EXT, a ground is connected to Q22 emitter to enable a detector circuit composed of Q22, C84, CR21, and CR22. As long as the external frequency is present at U2D(15), Q22 is shut off. Loss of the external standard causes Q22 to conduct and initiate a front panel LAMP TEST display.

4-132. A9 Main Gate

4-133. This assembly contains 3 primary blocks: Input Selector, Main Gate, and Scaler. All input signals and reference signals (time base) are presented to the Input Selector circuits, which select only those signals needed to complete a given measurement. The Main Gate circuitry determines the precise moment these signals are passed to the scalers and, in addition, sets the timing requirements for a time interval measurement. The scalers count the input pulses of both the input signal (events) and reference signal (time) and, at the end of the gate time, outputs the stored data. Subsequent scalers are located on A11. A fourth block, Turn-off Control, controls the existence of the 500 MHz internal time base signal, as well as the Channel A and Channel B signals.

A9 Continued

4-134. FREQUENCY OR PERIOD MEASUREMENT. Assume a frequency measurement is being made from the front panel. (A period measurement is analogous.) The control lines (see Table 4-1) determine the signal path through the Input Selector circuits. With a Low on U14(11 and 12), the MF CH A signal is allowed to pass through U14D and A. If a signal is also connected to CHANNEL B jack, it will pass through the Channel B Multiplexer U15, but will be blocked by U12A and B (pins 6 and 14 are High). The disabled U6A (pin 8 = H) places a Low on U11(11), which enables U11C to pass the input signal to U5(13) and U10(15). At the same time, the Channel C Multiplexer U13 passes the 500 MHz clock signal to the clock input of the Time Gate F-F, U7(13). Now that both signals are present on their respective flip-flops, a set of conditions must be considered. Both gate flip-flops have been set (Q=H) by the GATE RST signal. U7(3) is High from the High outputs of U5(6) and U6B. The disabled U6A has set U5(1) Low, via U1B. The High outputs of U5 and U7 flip-flops prevent U4 and U2 from toggling. The TI+EVT line is Low and allows U10 to pass the input signal to the disabled U4(13).

Table 4-1. A9 Control Lines

Selected Input Signal	Control Lines (EECL)		
	Test	Ext AB	Ext C
100 MHz TEST	H	X	X
MF CH A AND CH B	L	L	X
PI CH A AND CH B	L	H	X
500 MHz CLK	X	X	L
PI CH C	X	X	H

Measurement Mode	Control Lines (EECL)	
	Ratio + ST	TI + EVT (P1B pin 14)
FREQ OR PERIOD	L	L
RATIO OR START/STOP	H	L
TI OR EVENTS	L	H

4-135. Noting the timing diagram of Figure 4-18, it is seen that once the GATE ARM line goes High (ECL), it places a Low (EECL) on U5(3). This allows the next input signal to toggle the Event Gate flip-flop. This does two things. (1) It places a Low on U4(14), which enables U4 and allows the next input pulse to enter the Event Scaler. (U4 is a binary of the scaler). (2) It places a Low on the D input of U7, which allows the next 500 MHz clock pulse to toggle the flip-flop and and enable U2 with a Low on C1. This allows the clock signal to enter the Time Scaler. Binaries U4 and U2 pass their divided (÷2) signals to U9 and U3, respectively, where the signals are further divided-by-10. The divide-by-20 input and clock signals are sent to the A11 Scaler board through emitter followers Q15-18.

4-136. The GATE ARM line goes Low once the total number of counts in the time scaler exceeds $\frac{\text{Gate Time}}{2\text{ns}}$. U5(6) goes High on next input pulse after GATE ARM goes Low. This disables U4 and shuts off the Event Scaler. On the next clock pulse after U7(3) goes High, U2 is disabled by a High on C1, which shuts off the Timer Scaler. Note that only integral (whole) periods are counted in the Event and Time Scalers. This is not true, however, in the totalize (start/stop) mode.

4-137. TOTALIZE MODE. The counter will totalize Channel A pulses for as long as the FUNCTION switch remains in the START position. In this position, the RATIO + ST line is High and causes Q2's collector to go High. This enables U13B and disables U13D from passing the 500 MHz clock signal. The Low on Q1's collector enables U12B to pass the Channel B signal (totalize can be A+B or A-B). The signal passes through U13B to the Time Gate F-F, while the Channel A signal follows the same path that it would in a frequency measurement. The GATE ARM signal is always High in totalize.

4-138. The measurement ends when the FUNCTION switch is placed to STOP. This causes the GATE RST line to go High and set the Event Gate and Time Gate flip-flops. Integral periods are not counted, since the measurement can be interrupted at any time.

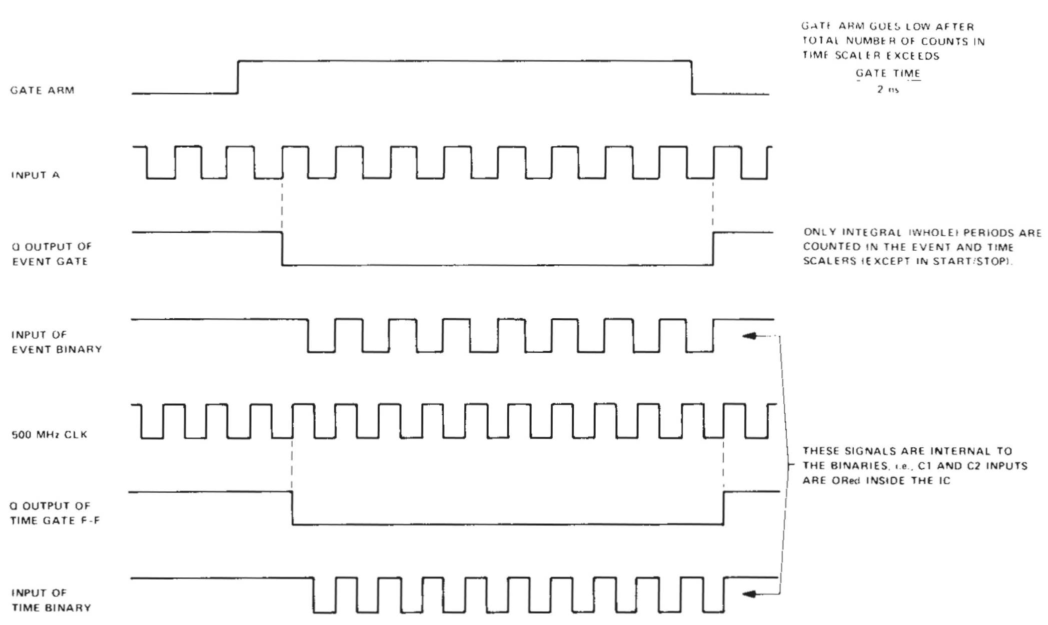

GATE ARM
INPUT A
Q OUTPUT OF EVENT GATE
INPUT OF EVENT BINARY
500 MHz CLK
Q OUTPUT OF TIME GATE F-F
INPUT OF TIME BINARY
GATE ARM GOES LOW AFTER TOTAL NUMBER OF COUNTS IN TIME SCALER EXCEEDS
GATE TIME
2 ns
ONLY INTEGRAL (WHOLE) PERIODS ARE COUNTED IN THE EVENT AND TIME SCALERS (EXCEPT IN START/STOP).
THESE SIGNALS ARE INTERNAL TO THE BINARIES, i.e., C1 AND C2 INPUTS ARE ORed INSIDE THE IC

Figure 4-18. A9 Timing Diagram for Frequency, Period, Ratio, and Start/Stop

4-139. RATIO MODE. The Ratio mode uses the same signal paths as the Totalize mode. That is, Channel A signal is sent to the Event Scaler and Channel B signal is sent to the Time Scaler. Unlike totalize, the Ratio measurement cycle is based on a selected gate time; therefore, it is dependent on GATE ARM. Since the Channel B signal is a direct replacement of the 500 MHz clock, the lower the frequency of Channel B, the longer the measurement time (see Section III).

4-140. TIME INTERVAL MODE. In this mode, the Time Scaler will count 500 MHz clock pulses only during the time between a Channel A pulse and a Channel B pulse. The two input channels regulate the switching of the clock signal by controlling the Event Gate F-F and Time Gate F-F. Refer to Figure 4-19.

4-141. The High on TI+EVT line causes U4(13) to stay Low, thereby enabling the binary to respond to the output of U5, only. Since U5 and U7 have been set (Q=H) by a High GATE RST, U6A is disabled, which results in a Low on U5(1) and causes U11C to be enabled. The first Channel A pulse to arrive after the GATE ARM line goes High clocks U5 and causes its output to go Low. This causes the output of U7 to go Low with the next clock pulse and enables U2 to pass 500 MHz clock pulses to the Time Scaler. The output of U5 also changes the output states of U6A, causing a High at U5(1) and allowing U11B to pass the next incoming Channel B pulse.

4-142. The Channel B pulse clocks the High on U5(1) onto the QA output. This clocks the C2 input of U4 to register that one time interval has occurred. On the next 500 MHz clock pulse, the High on U7(3) is clocked onto U2(13) and disables U2 from registering any more clock pulses.

4-143. TURN-OFF CONTROL LOGIC. To prevent possible cross talk of high frequency signals under certain conditions, it is necessary to turn off some of the unused internal signals. For example, the internal 500 MHz clock is turned off when using the external clock from the plug-in or when performing a ratio measurement.

A9 Continued

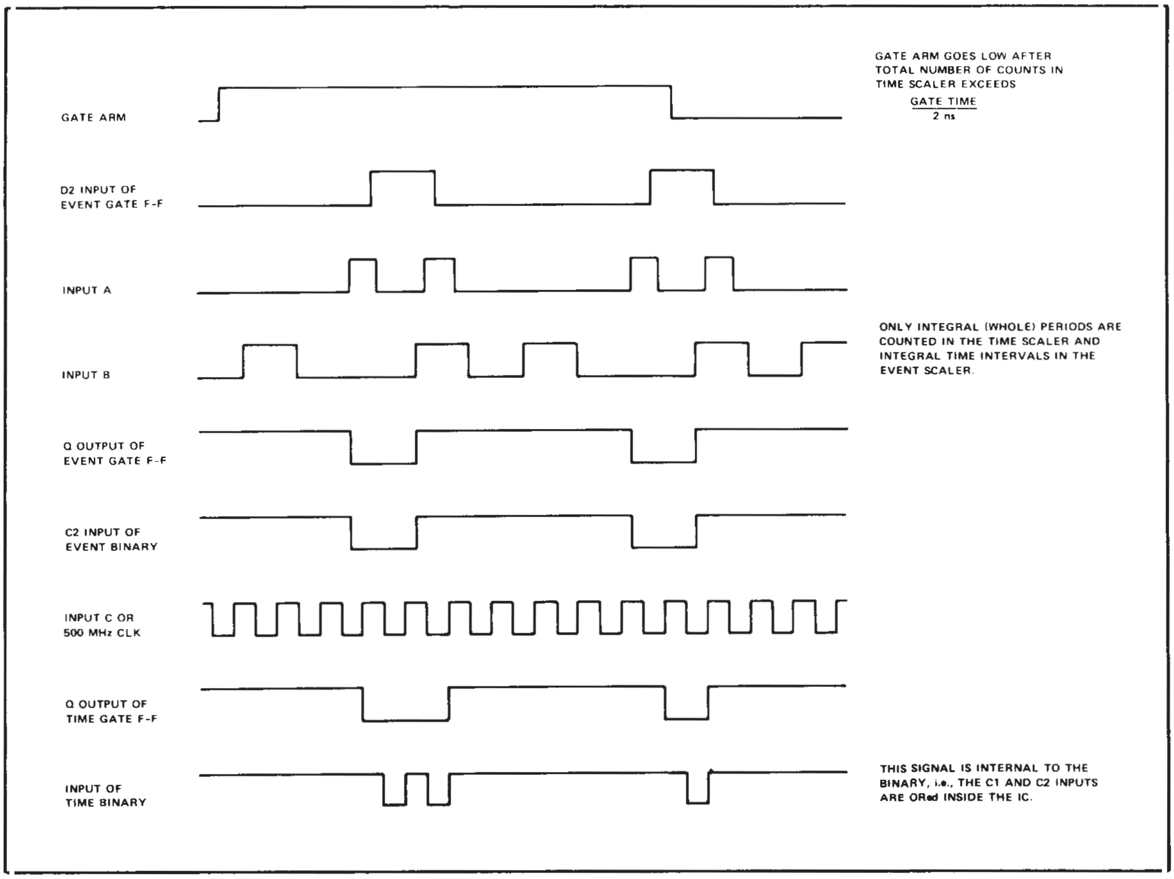

GATE ARM
D2 INPUT OF EVENT GATE F-F
INPUT A
INPUT B
Q OUTPUT OF EVENT GATE F-F
C2 INPUT OF EVENT BINARY
INPUT C OR 500 MHz CLK
Q OUTPUT OF TIME GATE F-F
INPUT OF TIME BINARY
GATE ARM GOES LOW AFTER TOTAL NUMBER OF COUNTS IN TIME SCALER EXCEEDS GATE TIME / 2 ns
ONLY INTEGRAL (WHOLE) PERIODS ARE COUNTED IN THE TIME SCALER AND INTEGRAL TIME INTERVALS IN THE EVENT SCALER.
THIS SIGNAL IS INTERNAL TO THE BINARY, i.e., THE C1 AND C2 INPUTS ARE ORed INSIDE THE IC.

Figure 4-19. A9 Timing Diagram for Time Interval

4-144. When the RATIO + ST line goes High, it turns on Q1 and turns off Q2. The High on Q2's collector turns on Q4, causing its collector to go Low. Q9, CR2, and R43 form an emitter follower, which level shifts the Low on the collector of Q4 to -2V on the 500 MHz control line. The Control line turns off the internal clock (+2V=ON). The same thing applies if the EXT C line goes High.

4-145. If the plug-in Channel A and Channel B signals are being used, the EXT AB line goes High and shuts off the mainframe's input triggers. The High on EXT AB turns on Q3, which saturates Q8 and Q10 and pulls the trigger line High. This turns off the Schmitt triggers on A4. R50 and R51 form a 10-to-1 divider network with two resistors on A4 (A4R22 and 24).

NOTE

Simplified flow diagrams for A9 are given in Figures 5-14 through 5-16.

4-146. A10 Gate Control

4-147. The A10 board is closely related in operation with the A9 Main Gate board. The board controls the various methods of arming the counter. Each of these methods must set the Arm F-F, which remains set throughout the measurement phase. The Resolution circuit detects a 5 code from the scalers and signals the end of the measurement. The board provides signals necessary to terminate the measurement, start the processing cycle, and reset the scalers. The function codes (front panel, remote, or plug-in) are decoded through switching and combinational gating and are sent out as control signals. These lines instruct the counter to perform unique functions for the selected mode.

4-148. CONVENTIONAL ARMING. The sequence of events for a frequency measurement, for example, would be sample rate arm, measure, process, display, and back to sample rate arm. At the end of the processing cycle, the sample rate circuit begins its rundown as the previously taken measurement is being displayed.

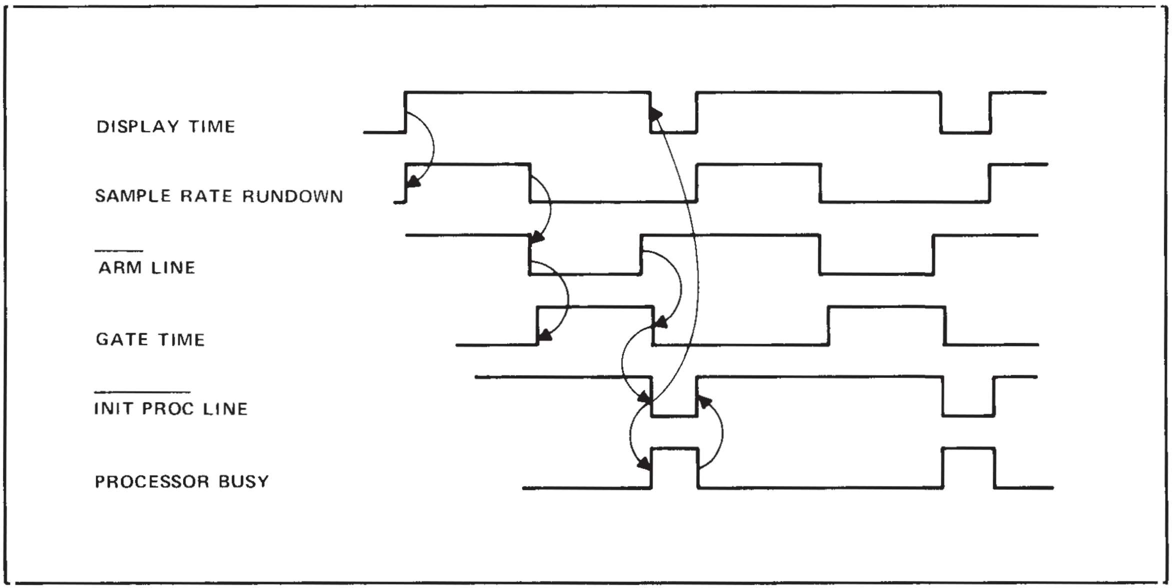


Figure 4-20. Measurement Timing Diagram

4-149. At the end of sample rate, the $\overline{\text{ARM}}$ line goes Low and sets the Arm F-F, U18A and B. If the rear panel GATE CONTROL switch is set to INTERNAL, the resultant $\overline{\text{ARMED}}$ signal turns on U17C, which enables the Event Gate F-F on A9. The complement signal, ARMED, passes through translator U20B and turns on the ARM light on A2. The next Channel A pulse sets the Event Gate F-F (A9) and drives the $\overline{\text{EVT GATE}}$ line low, which turns on the GATE light and turns off the ARM light. The ARMED line also places a High on the cathode of CR1, located in the Resolution circuit. Once the time scaler outputs a 5 code, a High is placed on each cathode of diodes CR1-4. This places a High on the J input of U22A and toggles the Q output High. The ECL High on U11B(4) and the ECL Low on U11C(9) reset the Arm F-F. The cathode of CR1 goes Low again, thereby preventing a 5 from toggling the Resolution F-F during the process phase when data is being read from the scalers. The reset state of the Arm F-F permits the Event Gate F-F on A9 to terminate the measurement on the next Channel A pulse. This is done when the disabled U17C forces the GATE ARM lines to their "false" states.

4-150. MAIN GATE STATUS. After arming, the first Channel A pulse sets the $\overline{\text{EVT GATE}}$ line Low, which causes U22B to set. The MEAS TIME line goes High and enables the Excessive Gate Time F-F on A11. Two nanoseconds later, the $\overline{\text{TIME GATE}}$ line goes Low, but has no effect on the MEAS TIME output until after a 5 code is detected and the Arm F-F resets. The Arm F-F resets U22B. At this time, the $\overline{\text{TIME GATE}}$ line holds the ECL wired-OR High, through U23C and U21C and D, until it also goes Low one time pulse after the Event Gate F-F resets.

4-151. During slow gate times, the GATE light is on for as long as the wired-OR line is High. With fast gate times, a 40 ms one-shot ensures that the GATE light is visible by keeping the $\overline{\text{GATE LITE}}$ line Low for 40 ms after the main gate closes.

4-152. INITIALIZE PROCESSOR CIRCUIT. The processing cycle begins when the measurement cycle is complete and the main gate closes. When the MEAS TIME line goes Low, it allows U12A to clock the Measurement Done F-F, U12B. The $\overline{\text{Q}}$ output goes Low and allows U13B and C to pull the $\overline{\text{INIT PROC}}$ line Low, thereby starting the process cycle. At near completion of the process cycle, the RST FRONT END line goes High and resets U12B via U10F and E.

4-153. ARMING AND PROCESSING IN TOTALIZE. During a totalize measurement, the process cycle is not controlled by the main gate. There is no gate time in an accumulating count and, therefore, no reasons to sample a 5 code. The scalers must be periodically scanned, however, to update the display. This is done by automatically fixing the sample rate at ≈80 ms when the FUNCTION switch is set to START and using this signal to control the process cycle. When SAMPLE RATE ARM signal from A11 goes High, it NANDs in U13A with the High output from U13D, caused by the Low $\overline{\text{ST+STP}}$ line. The output of U13A turns on U13B and C and pulls the $\overline{\text{INIT PROC}}$ line Low. The same type of processor start control can be done when using the $\overline{\text{PI DATA}}$ line.

A10 Continued

4-154. In totalize, the ARM F-F sets with the first sample rate rundown and remains set until the RESET button is pushed or the FUNCTION switch is set to some position other than START. With the switch set to STOP, U2C resets the ARM F-F via U5B and also causes the GATE RST line to go High. The $\overline{\text{ST+STP}}$ line also prevents a reset from the Resolution F-F by pulling the cathode of CR2 Low. When the FUNCTION switch is set to STOP, the ARM F-F resets and GATE RST goes High; however, the SCLR RST line does not go High to reset the scalers.

4-155. EXTERNAL ARMING. To externally arm the counter, the rear panel GATE CONTROL switch must be set to EXT ARM and the SAMPLE RATE control must be set to HOLD. This causes Q10, 11, and 12 to turn off and places a Low on U20D(13). The enabled gate can now provide a $\overline{\text{FORCED ARM}}$ signal when the GATE CONTROL jack receives an arm pulse. The $\overline{\text{FORCED ARM}}$ line causes the ARM line to set the Arm F-F. The remainder of the measurement proceeds in the normal manner.

4-156. EXTERNAL GATING. To externally gate the measurement, the rear panel GATE CONTROL switch must be set to EXT GATE. This setting requires both an arm pulse and a gate pulse. The switch position turns on Q10 and Q12 and disables U20D from providing a $\overline{\text{FORCED ARM}}$ signal. The switch also sets U7D(11) High, which places a Low on U17B(10). The first pulse in the GATE CONTROL jack is the arm pulse, assuming the GATE TIME switch is not in MIN. This pulse sets U11D(11) Low for at least 20 ns (depending on the external pulse width) and sets the Arm F-F with a Low on U11B(5). The resultant $\overline{\text{ARMED}}$ signal enables U17B to pass the forthcoming external gate pulse on U17B(9). This enables the Event Gate F-F on A9 with the GATE ARM lines.

4-157. In a time interval measurement, the counter "gates" on the next Channel A pulse after the $\overline{\text{GATE CONTROL}}$ line goes Low. The counter ignores Channel B pulses until the $\overline{\text{GATE CONTROL}}$ line returns High. After the line goes High, the next Channel B pulse toggles the Event Gate F-F (A9) and signals the end of the measurement. This is accomplished as follows.

4-158. With the GATE CONTROL switch set to EXT GATE, the High output of U7D(11) turns off Q7 and keeps the SCH-O line High. This line and the High on the GATE ARM line disable the Event Gate F-F during the time the $\overline{\text{GATE CONTROL}}$ line is Low. In remote operation, the same effect can be brought about by keeping the RMT GATE line High.

4-159. FUNCTION SELECTING AND DECODING. The counter works with a set of conditions given it by various control lines. The states of these lines are selected by the mode of operation being used. The function may originate from the front panel FUNCTION switch, from remote coding, or from the plug-in. The $\overline{\text{RMT}}$ line allows U14 to pass either remote codes or the FUNCTION switch codes. If plug-in is selected, the plug-in code sets U15A(12) Low and enables U8 to pass the plug-in code, rather than remote or function. The table below lists the function codes and the signal lines they activate.

FUNCTION	**CODE**	**ENABLES**
	CBA	
PERIOD A	000	$\overline{\text{SEC LITE}}$, PER+TI, NANO MULT
FREQ A	001	$\overline{\text{HZ LITE}}$
TIME INT AtoB	010	TI+EVT, $\overline{\text{TI+EVT}}$, $\overline{\text{NOISE CONTROL}}$ $\overline{\text{SEC LITE}}$, PER+TI, NANO MULT
PLUG-IN	011	$\overline{\text{PI SEL}}$
RATIO B/A	100	EVT+RAT+ST+STP, RATIO+ST
START	101	EVT+RAT+ST+STP, $\overline{\text{RATIO+ST}}$, $\overline{\text{ST+STP}}$
STOP	111	EVT+RAT+ST+STP, $\overline{\text{ST+STP}}$
EVENTS Not selectable from front panel. Can be from plug-in or remote. Intended for 3-channel time interval; i.e., indicate number of inputs on "C" between A and B.	110	TI+EVT, $\overline{\text{TI+EVT}}$, $\overline{\text{NOISE CONTROL}}$

A10 Continued

FUNCTION	CODE	
FREQ	001	Plug-in
FREQ X N	001	
TIME INT	010	
DVM	010	

4-160. NOISE CONTROL. A Low on the NOISE CONTROL line allows A8 to generate noise on the internal 500 MHz clock. This line is active when 1) function is time interval and gate time is *not* MIN, 2) in EXT GATE, any function is selected and gate time is *not* MIN, and 3) the GATE CONTROL switch is set to EXT GATE and function is Start or Stop (no time base signal is present, however). The conditions are controlled by gating of U5A and D and U2D. The NOISE CONTROL line is inactive when U2D(11) is Low, since the Noise Control F-F, U6A, clocks the Low to the Q output and disables U5C. The flip-flop examines the state of U2D each time the sample rate circuit pull the ARM line Low.

4-161. A11 Scaler

4-162. The scaler board accepts the incoming signal from the front panel and the time base signal and accumulates these counts in addressable decades. Once a 5 is detected in the time scaler, the measurement is stopped. Each decade in the scalers is addressed to output its data to the processor board. The A11 board also contains the sample rate, arming, and reset circuits for the instrument.

4-163. SCALERS. Once the Main Gate opens, it allows the Channel A signal and the time base signal to accumulate counts in their respective scalers. The A9 board contains a portion of the scalers, so the signals arriving at A11 have already been divided by 20. The Channel A signal connects to the bases of Q1 and Q2, which along with Q3 level shift it from ECL to TTL. U22A divides the signal by five before passing it to U17 and U16. These two ICs contain decade dividers, whose BCD data outputs are addressable. As the counts accumulate in the scalers, the decades internally store each changing digit, until the counting stops and the data can be addressed out. The time scaler accumulates time base counts in the same fashion.

4-164. The time scaler ends the measurement when a 5 is detected at its addressed output, since a 5 would be a division of 500 MHz and would correspond in time to a setting of the GATE TIME switch. While the count is accumulating, the PROC BUSY line is High. This places a code of "0" on the select lines (S1, S2) of U13 and U9, which allows the multiplexers to pass the BCD code on the FP GT lines to U4. The code from the GATE TIME switch, indicating a specific setting, is decoded in U4 and pulls one of the output lines Low. Output gates U11, 12, 3, and 10 supply a code to the address lines, which select one decade in the time scaler to output its most significant bit. When a 5 is placed on the output lines, it passes through the enabled 4-pole switch U26 to the TIME SCALER A and C lines. When the circuits on the A10 board receive the 5, they turn off the main gate circuit on A9, thereby stopping any further pulses from entering the scalers. The next step is to read the data out of the scalers and into the numerator and denominator registers on A13.

4-165. After the main gate closes, the PROC BUSY line goes Low and places a code of "3" on the S1 and S2 inputs of U13 and U9. This allows the two ICs to pass the states of the DRC A, B, C, D lines. These lines are the binary output of the 16-bit denominator register counter. As the counter steps through its sequence of codes, it addresses each decade (in both scalers) to output its data. The first decades to output are the ÷20s on the A9 board. The DRC code to U4 is "0000," which pulls pin 1 Low and enables U24 and U28 via U15C. The event code is passed through U23, an ECL to TTL converter, and inverted by U24 before being sent to U25. The time data is passed through converter U27 and inverter U28 and sent to U26. U25 and U26 are enabled by the Low output of U3C and select the "1" inputs because the SEL input is High. The data codes pass through these switches to the registers on A13.

4-166. The second DRC code (0001) causes the 1 line (U4 pin 2) to go Low and forces U25 and U26 to pass the data from U22A and U29A through the "0" outputs. As the DRC codes continue incrementing, each successive output of U4 goes Low and produces a 3-line code. The codes address the decades in U16-19 to output their stored data.

A11 Continued

4-167. When data is accumulating in the time scaler, one decade is always enabled, so that its output lines can send out a "5" to end the measurement. Because of the accumulating speed, the first bit in the first decade of U18 has difficulty outputting its state. A second binary, U29B, is used for this bit, instead. The first decade of U18 is addressed when U4(3) is Low. This disables U20D from passing the "A" bit of U18 and substitutes the output of U29B, instead. The B, C, and D lines of U18 output normally. When any other decade is addressed, U4 pin 3 is high. This enables U20D to pass U18's A bit and disables U20C from passing U29B's A bit.

4-168. EXECESSIVE GATE TIME When making a measurement, if the period is more than ≈3.5 times the GATE TIME setting, the counter will reset and flash lamp test on the display. This occurs through the following steps. When an 8 is detected on the input of U26, pin 7 returns High and clocks U22B, causing U3B pin 6 to go Low. With subsequent data entering U26, pin 7 stays High until just prior to three times the GATE TIME setting when it goes Low. When it returns High (at 3.6 times the switch setting), it clocks U22B's output Low and causes U3B(6) to go High. This causes U14A to set and the $\overline{\text{LAMP TEST}}$ line to go Low. U7D causes the $\overline{\text{RST}}$ line to also go Low, via U15A.

4-169. SAMPLE RATE AND ARMING. The sample rate circuit controls the arming of the counter. The counter is armed in one of five ways: 1) with the SAMPLE RATE pot circuit, 2) by the plug-in (P18 pin $\overline{19}$), 3) externally (P18 pin $\overline{21}$) from the rear panel (remote), 4) when in START/STOP, or 5) by resetting the counter.

4-170. When the measurement is ready to be displayed, the DISP CLK EN line goes High and causes the base of Q7 to go Low. This removes Q7's short from C5 and allows C5 to charge through R20 and the SAMPLE RATE pot. The time required for C5 to charge is the display time. When the charge on C5 reaches about 1.4V, it causes Q8 A and B to conduct and triggers a Low output from U2C. This arms the counter by pulling U5A(6) Low, via U5B. When the counter is in remote operation, the SAMPLE RATE line is shorted to +5V, and C5 charges through R20 in about 80 ms. If remote operation requires faster arming, the $\overline{\text{FORCED ARM}}$ lines sets the counter to a maximum sample rate of ≈5 ms. This line is also pulled Low through CR8 by the $\overline{\text{ST + STP}}$ line, which is Low during totalize.

4-171. The counter is also armed after a reset by the 1st cycle Arm flip-flop (U20A and B). When a reset is generated from U7D, it sets the output of U20A High. This sets U20B(6) Low, since U20B(5) is also High. U5B turns on and places a High on U5A(4). This does *not* set U5A's output Low, since U5A (1) is still held Low through CR11. Once the reset signal ends, pin 1 goes High and U5A arms the counter. The flip-flop resets when the PROC BUSY line goes Low.

4-172. Normally, processing the data begins when a 5 is detected in the time scalers. This is not possible for all measurements. During a plug-in measurement or a totalize measurement, U3A is used, instead, to initialize the processor. The SAMPLE RATE ARM lines goes High with the $\overline{\text{PI ARM}}$ line, a reset, or an output from the sample rate circuit. In totalize, the sample rate is about 80 ms. The SAMPLE RATE ARM line is ANDed on A10 with $\overline{\text{PI DATA}}$ or $\overline{\text{ST + STP}}$ to pull the $\overline{\text{INIT PROC}}$ line Low.

4-173. RESET. The counter uses several reset lines, and these are wire-ORed at U1A(1). When the counter is first turned on, C6 conducts rapidly and holds U1A(1) to a low state through CR9. The resultant Low on U7D(13) produces a reset by pulling the $\overline{\text{RST}}$ line Low via U15A. If the counter is not in remote operation, a reset will occur if the FUNCTION, GATE TIME, or DISPLAY POSITION switches change position or if the front panel RESET button is pushed. A reset can also be generated remotely ($\overline{\text{REM RESET}}$) or from the plug-in (PI RST). Excess gate time also resets the counter.

4-174. A reset signal also resets the Auto Single Cycle flip-flop, U14B. This pulls the $\overline{\text{AUT SC}}$ line Low, which instructs the counter that it should examine the measurement for a new annunciator. This is also done during the processing cycle. When $\overline{\text{LOAD MS}}$ clocks the High level on U14B(12), the annunciator has been selected.

4-175. MIN GATE TIME. This signal is developed on the board to allow a gate time for the duration of only one cycle of the measured frequency. This signal is developed when the GATE TIME switch is set to the "MIN" position. The GTS code of 13 is switched in the same manner as all other GT codes. The 4-to-16 line decoder (U4) decodes the 13 and inverts the output level in

U3C. The high output level is sent from the board via pin P1B($\overline{2}$). This High signal is also tied to the time scaler output switch U26, which disables the switch from passing the 5 code. This allows the MIN GATE signal to maintain full control of the gate.

4-176. A12 Option 010, General Purpose Interface Output

4-177. Option 010 allows the counter to make measurements in accordance with the front panel controls and to output the results of the measurements by means of a bus system. The system uses standard ASCII characters to communicate its data. There are two modes of operation: the address to talk mode for outputting data and the TALK ONLY mode. The circuits can be cleared from talking by supplying a Interface Clear (IFC) signal.

4-178. ADDRESSING TO TALK. The controller sets the ATN line Low, causing a High on U5A(1) and U5B(4) and a Low on U4B(5). At this time, the NRFD line from U5B is High, indicating to the controller that the counter can now accept an ASCII byte. The controller addresses the counter to talk $\begin{pmatrix} \text{DIO} & 7 & 6 & 5 & 4 & 3 & 2 & 1 \\ & 1 & 0 & A_5 & A_4 & A_3 & A_2 & 0 \end{pmatrix}$ and, at some time later, pulls the DAV line Low, indicating there is valid data on the bus.

4-179. If the 4-line address code equals the code selected by the rear panel ADDRESS switches, the A=B line of U7(14) goes High. The address code also allows U3D to enable U4C and D. The result of this gating is a High on the J input of the Talk F-F (U6) and a Low on the K input. The DAV line was set Low when the counter was addressed to talk; however, it was delayed 500 ns by R7, C4, and U1A to allow time for the address code to be gated. The delayed DAV line now produces a 500 ns pulse in U2C, U1C, and U3A. This pulse NANDs in U4B with ATN (still Low) and clocks the Talk F-F. Once the flip-flop is set, the controller causes ATN to return High, since it has accepted a high NDAC.

4-180. OUTPUT ROUTINE. The High output of the Talk F-F is sent to A19 and returns on the TALK ONLY line when the rear panel switch is set to ADDRESSABLE. The line is continuously High when the switch is set to TALK ONLY. This signal is inverted in U9C and becomes $\overline{\text{SER OUT}}$, which starts the output routine. TALK ONLY and the High of ATN also cause the output of U5D to go Low. This Low level switches the bus terminators from their *third state* (off or high impedance state) to their active state. Measurement data can now be placed on the bus.

4-181. Once data is placed on the bus, the counter waits until the listener requests information by sending NRFD High. This results in a GATED RFD signal from U10A, U10C, and U14A. The counter responds by setting the FLAG = H line High. Since the $\overline{\text{EXT OUT EN}}$ line is Low during the output routine, U8A and U5C cause the DAV line to go Low, indicating the valid data is on the line. Once the listener accepts the data, it responds with a high NDAC signal. This produces a GATE DAC signal to place new data on the bus and repeat the process. Gate U10A causes GATED DAC and GATED RFD to go High if the bus is disconnected. This causes the processor section of the counter to exit the serial output routine.

4-182. DATA TRANSFER. The DC SER OUT lines control the order of output data and the state of the ROMs (U16 and U17). Only one ROM is on at any given time. Three of the ROM's outputs (DIO7, 6, and 5) are sent to the Bus Drivers directly, while the remaining four lines are selected by four-pole switch U15. The ROMs convert the internal data codes to ASCII format. Since the counter is in its output routine, the $\overline{\text{EXT OUT EN}}$ line is Low. The FLAG = H lines goes High each time a new byte is ready for outputting on the bus. Table 4-2 shows the sequence of data flow to the ROMs, while Tables 4-3 and 4-4 list the ROM codes.

4-183. A12 Option 011, General Purpose Interface I/O

4-184. Option 011 allows the counter to be externally programmed to make measurements and to output the results of the measurements. The system uses standard ASCII characters for programming. The board can be divided into a few, basic sections. The Bus Communicator section determines the operating mode of the assembly by the use of combinational logic and three flip-flops.

A12 Option 011 Continued

These modes are talk, computer dump, and listen. When the counter is listening, the controller changes the basic program that is stored in the Data Steering Latch section. When the counter is talking, measurement data is sent to the bus through the Data Encoder ROMs and Bus Drivers.

4-185. When the counter is first turned on, the power up reset circuit of R7, C5, and U12C resets the mode flip-flops (U5A, U5B, and U6B) and the Data Steering Latches via U4D. For full communication with the bus, the rear panel TALK ONLY-ADDRESSABLE switch should be set to the ADDRESSABLE position. The following paragraphs describe the circuits as they might be used in a typical programming sequence.

4-186. ADDRESSING TO LISTEN. The controller sets the ATN line Low, causing U13D(11) to go High and set NDAC Low, via U2B. The NRFD line is High, indicating to the controller that the counter can now accept an ASCII byte. The controller addresses the counter to listen $\left(\begin{array}{cccccccc} \mathrm{DIO} & 7 & 6 & 5 & 4 & 3 & 2 & 1 \\ & 1 & 0 & A_5 & A_4 & A_3 & A_2 & 0 \end{array}\right)$ and, at some time later, pulls the DAV line Low, indicating there is valid data on the bus.

4-187. If the 4-line address code equals the code selected by the rear panel ADDRESS switches, the A=B line of U30(14) goes High. The High from U30 and the listen code (DIO7 and DIO6) are routed through the combinational gating of U23B, U22B, U23E, U9A, U21, and U23D. The result of this gating is a High on the J input of the Listen F-F (U6B) and a Low on the K input. The DAV line was set Low when the counter was addressed to listen; however, it was delayed 500 ns by R4, C3, and U12B to allow time for the address code to be gated. The DAV line now produces a 500 ns pulse in U3E, U12A, and U13B. This pulse NANDs in U4B with ATN (still Low) and clocks the three *mode* flip-flops (U5A, U5B, and U6B). Only the Listen F-F toggles. The Low from U12A(3) causes U2B to set the NDAC line High, indicating that the counter has been addressed. When DAV goes High, the NRFD line then goes High and signals the controller that the counter can receive new data.

4-188. CHANGING THE STORED PROGRAM. Once a reset has been generated from either power up reset, IFC, or PB reset, the data steering latches and their associated gates automatically set up a predetermined program. This program electrically sets all measurement controls to one setting, e.g., FUNCTION to frequency, GATE TIME to 1 second, etc. If the program is to be changed, it must be programmed to change. This is accomplished as follows.

4-189. Once the counter has been programmed to listen, the ATN line goes High and the Listen F-F remains set. Assume the function is to be changed from frequency to period (see Table 2-3). This requires an ASCII code of "F1" $\left(\mathrm{F} = \begin{array}{cccccccc} \mathrm{DIO} & 7 & 6 & 5 & 4 & 3 & 2 & 1 \\ & 1 & 0 & 0 & 0 & 1 & 1 & 0 \end{array} ;\ 1 = \begin{array}{cccccccc} \mathrm{DIO} & 7 & 6 & 5 & 4 & 3 & 2 & 1 \\ & 0 & 1 & 1 & 0 & 0 & 0 & 1 \end{array}\right)$, as shown in Table 2-2. The controller places the ASCII "F" on the bus and also set DAV Low, indicating the data is valid.

4-190. The incoming code is inverted by the Bus Terminators and is used as follows: DIO7 is not pulled Low; DIO6 and DIO5 disable U15B, which places a High on U15C(10); and DIO4 through DIO1 are placed on the input lines of U26. When the delayed DAV signal causes U13B to pulse Low, it enables U15C and allows U26 to transfer the data code to its output lines. As with every exchange of data, the transfer lines (NDAC, NRFD) perform their *handshake* operation.

4-191. The controller removes the "F" from the bus, replaces it with an ASCII "1", and pulls DAV Low. This code is used as follows: DIO7 is not pulled Low; DIO6 and DIO5 enable U15B; and DIO4 through DIO1 are placed on the inputs of the Data Steering Latches. When the delayed DAV signal pulses Low at U13B, it turns on U7C and causes U17 to accept the "F" code that was stored in U26. U17 uses this code to set one of its output lines Low; in this case, it is the 6 line (pin 7) and is used to enable U25 (the function latch). Once enabled, U25 transfers the "1" code to its output lines. Any further changes in the basic program are accomplished in the same manner.

ASCII CHAR	DATA STEERING LATCH
F	U25
G	U24
D	U32
C	U35
I	U5D, U8C
E	U16
J	U5A

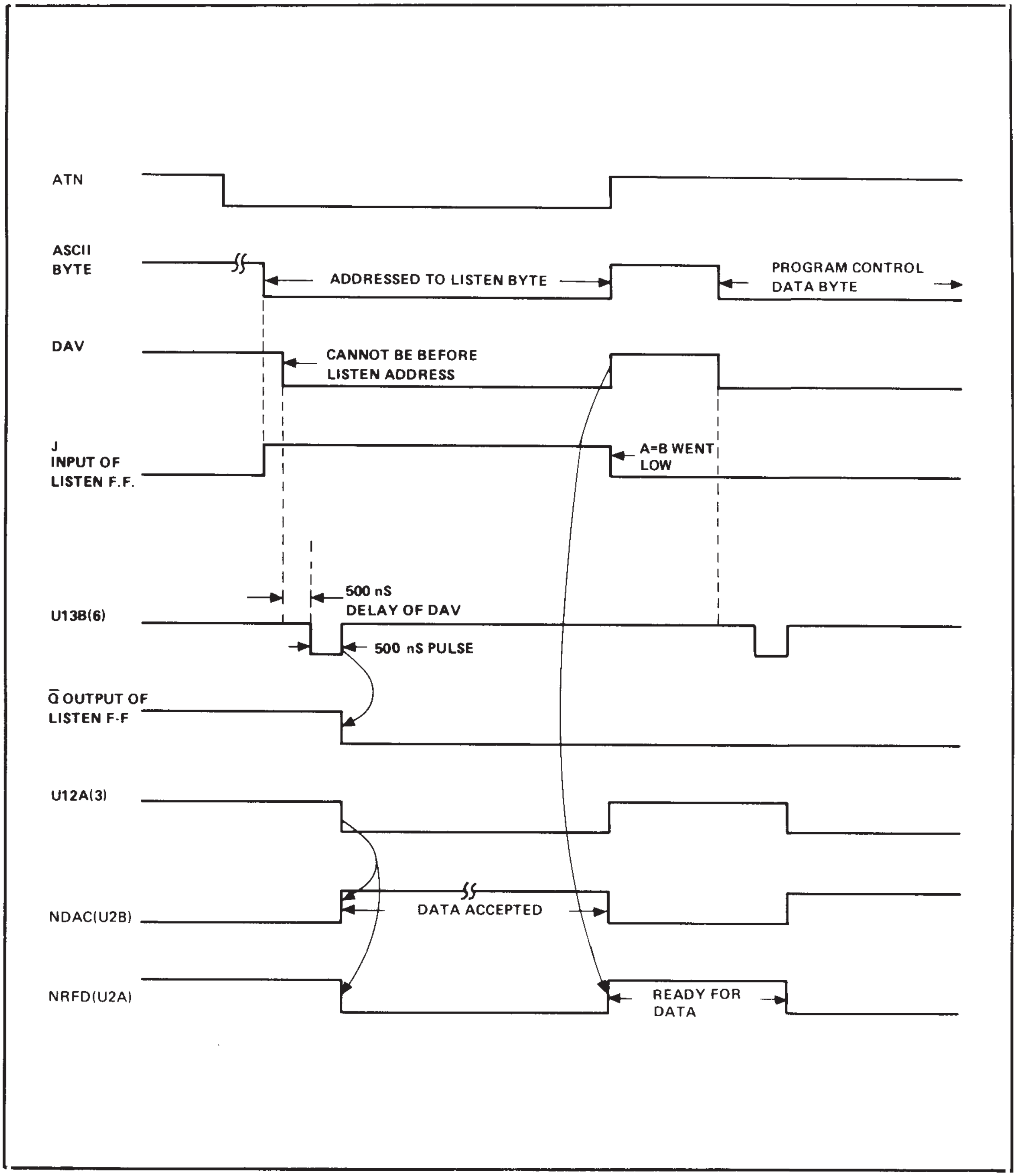


Figure 4-21. Address to Listen Timing Diagram

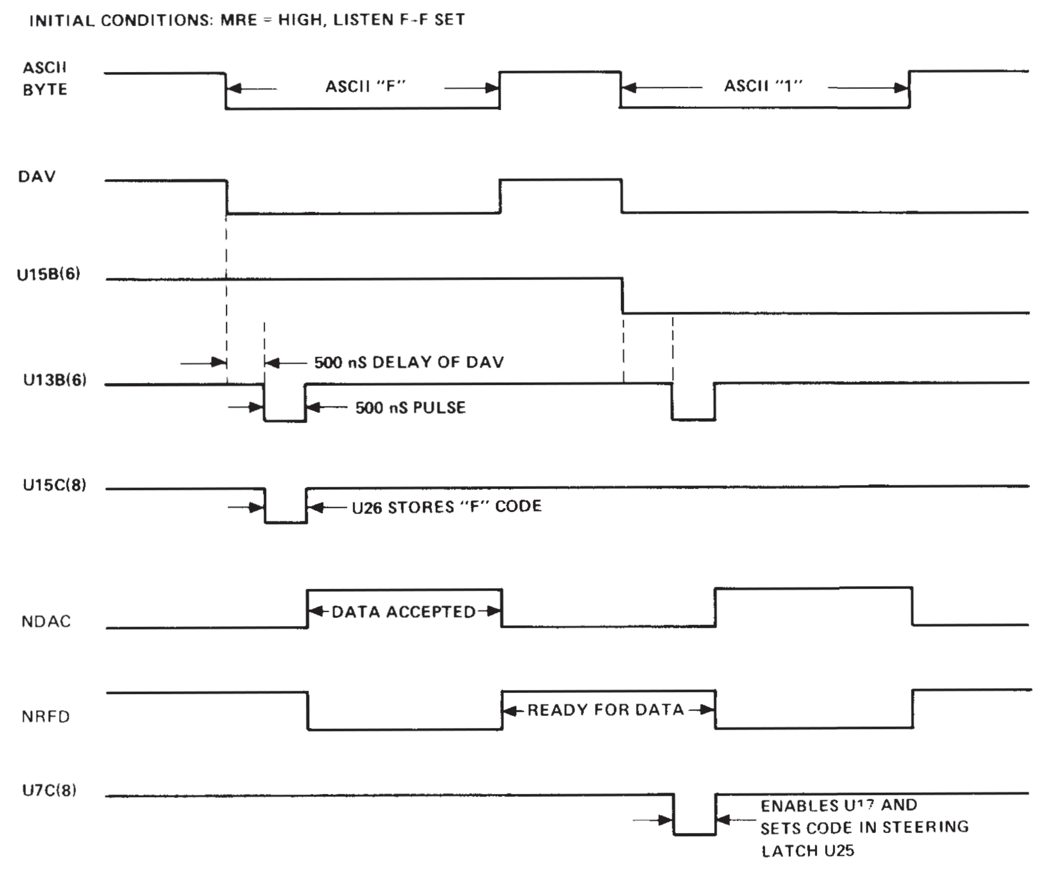


Figure 4-22. Remote Program Timing Diagram

4-192. SWITCHING TO REMOTE. Sometime before the counter makes a measurement, using the newly programmed control settings, it must be switched to remote operation. To do this, the controller sets the REN line Low and sends an ASCII "E8". The "E" enables U16, and the "8" causes U16(4) to go High. This output is NANDed in U8B with the inverted REN signal from U9C. This forces the RMT line Low and sets the counter to follow the remote instructions, instead of the counter's controls. The REN line must remain Low if the counter is to use the functions that were programmed.

4-193. ADDRESSING TO TALK. Before the counter can "talk", it must be cleared from listen. A code of "?" (DIO 7 6 5 4 3 2 1 / 0 1 1 1 1 1 1) enables U21 and disables U4A. When DAV clocks the three flip-flops, the Listen F-F (6B) returns to its reset state. The counter can now be addressed to "talk". When the Talk F-F sets, the TALK line causes TALK ONLY to go Low, via the switch circuit on A19. This disables U15D and enables U13C (ATN = HIGH). The Low output from U13C (TALK ENABLE), switches the bus terminators from their *third state* (off or high impedance state) to their active state. Measurement data can now be placed on the bus. U2C(8) sets the SRQ line High, indicating to the controller that the counter has data ready.

A12 Option 11 Continued

4-194. The DC SER OUT lines control the order of output data and the state of the ROMs (U29 and U27). Only one ROM is on at any given time. Three of the ROM's outputs (DIO7, 6, and 5) are sent to the Bus Drivers directly, while the remaining four lines are selected by four-pole switch U28. The ROMs convert the internal data codes to ASCII format. Since the counter is in its output routine, the EXT OUT EN line is Low. The FLAG = H line goes High each time a new byte is ready for outputting on the bus. These two lines NAND in U2D to generate a DAV signal. Table 4-2 shows the sequence of data flow to the ROMs, while Tables 4-3 and 4-4 list the ROM codes.

Table 4-2. ROM Sequence

DC SER OUT			DPLR<16	ENABLED ROM	BUS DATA
C	B	A			
0	0	0	L	U29	NONE. Counter is in process of deleting all leading blanks from measurement data before output cycle begins.
0	0	1	L	U29	DIGIT SIGN. ROM examines SIGN - line to determine polarity of measurement. No output if polarity is plus (line = H).
0	1	0	L	U29	DENOMINATOR REGISTER OUTPUT. U28 passes measurement digits contained on DR lines. Blank code (DR C & D=H) causes zero code on bus.
0	1	0	H	U29	DECIMAL POINT. DPLR<16 line may go High anytime during DR output to insert decimal point in output data.
0	1	1	L	U29	"E". Indicates that forthcoming data will be the exponent for power of 10 of measurement data.
1	0	0	L	U27	EXPONENT SIGN. Outputs minus sign to indicate a number smaller than one; e.g., 6=M, -6=μ
1	0	1	L	U27	EXPONENT DIGIT. Outputs digit to indicate magnitude of measurement data number.
1	1	0	L	U29	CARRIAGE RETURN. Used with teleprinter. Signals end of output. Provides ASCII code to generate teleprinter carriage return.
1	1	1	L	U29	LINE FEED. Used with teleprinter. Provides ASCII code to advance paper to next line.

4-195. COMPUTER DUMP. Computer Dump causes the Denominator Register and Numerator Register to output data directly from the scalers. When addressed to computer dump, U5B sets and forces the FORCED ARM line Low, via U33B. This line bypasses sample rate and forces the counter to make measurements at its fastest possible rate. The COMP DUMP line goes Low and prevents the counter from entering the arithmetic process.

Table 4-3. ROM Outputs, (1816-0254) U29

WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	8	7	6	5	4	3	2	1
0	L	L	L	L	L	L							L	
1	L	L	L	L	H	L							L	
2	L	L	L	H	L	L							L	
3	L	L	L	H	H	L							L	
4	L	L	H	L	L	L		L			L		L	L
5	L	L	H	L	H	L		L			L		L	L
6	L	L	H	H	L	L	L	L	L	L	L		L	L
7	L	L	H	H	H	L	L	L	L	L	L		L	L
8	L	H	L	L	L	L	L				L		L	L
9	L	H	L	L	H	L							L	
10	L	H	L	H	L	L	L				L		L	L
11	L	H	L	H	H	L							L	
12	L	H	H	L	L	L		L		L	L	L		L
13	L	H	H	L	H	L		L		L	L	L		L
14	L	H	H	H	L	L		L		L	L	L		L
15	L	H	H	H	H	L		L		L	L	L		L
16	H	L	L	L	L	L								
17	H	L	L	L	H	L								
18	H	L	L	H	L	L								
19	H	L	L	H	H	L								
20	H	L	H	L	L	L								
21	H	L	H	L	H	L								
22	H	L	H	H	L	L								
23	H	L	H	H	H	L								
24	H	H	L	L	L	L		L			L	L	L	L
25	H	H	L	L	H	L		L			L	L	L	L
26	H	H	L	H	L	L		L			L	L	L	L
27	H	H	L	H	H	L		L			L	L	L	L
28	H	H	H	L	L	L	L		L		L	L	L	L
29	H	H	H	L	H	L	L		L		L	L	L	L
30	H	H	H	H	L	L	L		L		L	L	L	L
31	H	H	H	H	H	L	L		L		L	L	L	L
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

Table 4-4. ROM Outputs, (1816-0255) U27

WORD	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	8	7	6	5	4	3	2	1
0	L	L	L	L	L	L			L		L		L	L
1	L	L	L	L	H	L			L		L		L	L
2	L	L	L	H	L	L			L		L		L	L
3	L	L	L	H	H	L			L		L		L	L
4	L	L	H	L	L	L		L			L		L	L
5	L	L	H	L	H	L		L			L		L	L
6	L	L	H	H	L	L		L			L		L	L
7	L	L	H	H	H	L								
8	L	H	L	L	L	L		L			L		L	L
9	L	H	L	L	H	L		L			L		L	L
10	L	H	L	H	L	L		L			L		L	L
11	L	H	L	H	H	L			L		L		L	L
12	L	H	H	L	L	L			L		L		L	L
13	L	H	H	L	H	L			L		L		L	L
14	L	H	H	H	L	L			L		L		L	L
15	L	H	H	H	H	L								
16	H	L	L	L	L	L		L	L				L	L
17	H	L	L	L	H	L	L			L			L	L
18	H	L	L	H	L	L			L	L			L	L
19	H	L	L	H	H	L	L	L	L	L			L	L
20	H	L	H	L	L	L			L	L			L	L
21	H	L	H	L	H	L	L			L			L	L
22	H	L	H	H	L	L		L	L				L	L
23	H	L	H	H	H	L								
24	H	H	L	L	L	L		L	L				L	L
25	H	H	L	L	H	L	L			L			L	L
26	H	H	L	H	L	L			L	L			L	L
27	H	H	L	H	H	L	L	L	L	L			L	L
28	H	H	H	L	L	L			L	L			L	L
29	H	H	H	L	H	L	L			L			L	L
30	H	H	H	H	L	L		L	L				L	L
31	H	H	H	H	H	L								
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

4-196. A13 Register, Adder/Subtracter

4-197. The A13 board performs an arithmetic process with the contents of the Event Scaler and Time Scaler. The result of this operation is displayed on the front panel. The board consists of three registers: Numerator, Denominator, and Quotient. Each register contains a Random Access Memory (RAM), having 16 addressable storage locations that are capable of storing 4-bits per location. Data from the Events and Time Scalers are sent to the Numerator and Denominator registers and are then arithmetically manipulated in the Adder/Subtracter circuitry. The Quotient Register (QR) stores the result, while the Quotient Multiplier Counter (QMC) and Multiplier Storage circuitry keep track of the annunciator. The QC also keeps track of the number of successful subtractions and sends this number to the QR.

4-198. The registers can shift data in the following manner.

Numerator Register

The Numerator register can *write* data *into* its RAM from the Time Scaler (A11), Denominator register, or Adder/Subtracter. It can *read* data *out* of the RAM into the Adder/Subtracter, Quotient register, or Denominator register.

Denominator Register

The Denominator register can *write* data *into* its RAM from the Events Scaler (A11), Quotient register, Numerator register, and Plug-in. It can *read* data *out* of the RAM to the plug-in, Adder/Subtracter, Numerator register, display, and output option board, A12.

Quotient Register

The Quotient register can *write* data *into* its RAM from the Numerator register, and Quotient Multiplier Counter (QMC). It can *read* data *out* of the RAM to the Denominator register, only.

4-199. REGISTER STORAGE OPERATION. The following description concerns an exchange of data between the Numerator Register (NR) and the Denominator Register (DR). The description serves an as explanation for the three registers in general. Each digit of Time Scaler data and Events Scaler data is represented as a 4-bit code. The RAMs are capable of storing 16 of these codes in separate locations (or addresses). The RAM counter that is enabled to count produces a new code with each negative transition of REG CLK. Each new code selects a different RAM location. Once the location is selected, data contained in the location can be read out while REG CLK is Low. If the data source code for the RAM is other than "READ", new data is written into the RAM when REG CLK goes High. Shifting data from one RAM to another requires switches to control the data flow and latches to store data during the write operation. Assuming data has been written into the RAMs from the scalers, a later ROM cycle exchanges data between NR and DR (a frequency measurement). This operation appears as follows.

4-200. The NR EN A and B code changes to "00", and the DR EN A, B, and C code changes to "101". NR CLK EN and DR CLK EN lines are High. This occurs at the start of a new process cycle. REG CLK is Low and data stored at the least-significant-digit (LSD) location appears on the RAM output lines, since the "WE" inputs are High (read mode). The data output of the NR RAM is sent to Latch U20, while the output of the DR RAM is sent to Latch U4 via U1.

4-201. When REG CLK goes High, the data in the latches is locked in, and the outputs of gates U27A and U12B to Low. This last condition forces the RAMs into the "write" mode. The NR RAM writes in the DR data (via (U30) that is stored in U4. The DR RAM writes in the NR data (via U17 and U26) that is stored in U20. When REG CLK goes Low again, U22 and U28 are clocked to a new location code. This process continues until all 16 words have been exchanged. The number of clock pulses (REG CLK) for this process was 16.

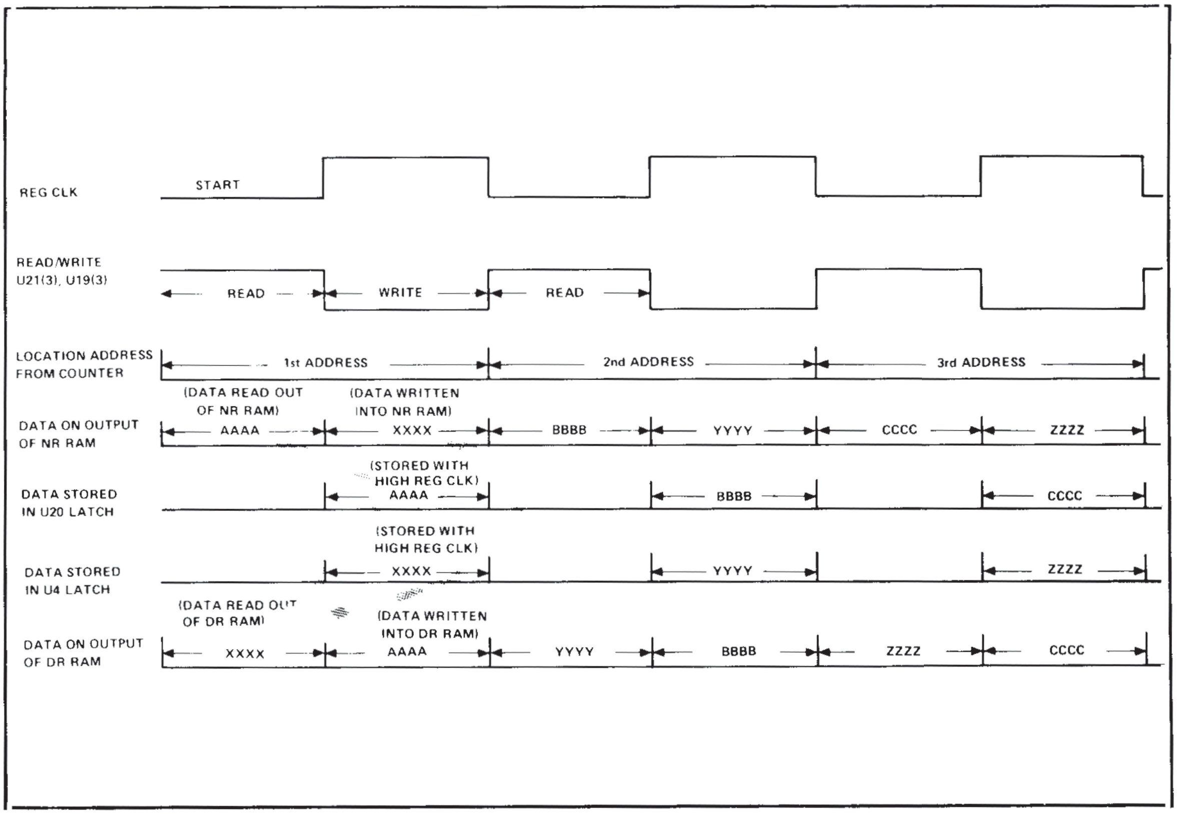


Figure 4-23. An Exchange of NR and DR Data

4-202. All data entering the registers from the scalers is written into the DR and NR with "LOAD EVENT SCR" and "LOAD TIME SCR" codes on the DR EN lines and NR EN lines, respectively. Data is sent to the Adder/Subtracter circuit during the "READ" portion of REG CLK (Low). The result of each digit subtraction is stored in U4 and in the NR during the "WRITE" portion of REG CLK with a "LOAD A/S" code on the NR EN lines.

4-203. ADD/SUBTRACT CIRCUITRY. This circuit performs an arithmetic operation between the Events Scaler's contents (E) and the contents of the Time Scaler (T). The operation is always a division, i.e., either $\frac{E}{2XT}$ for a frequency measurement or $\frac{2XT}{E}$ for a period measurement. The process of division is accomplished by performing a *series of subtractions.* Under certain conditions this circuit also performs addition (e.g., when the Numerator Register's content is added to itself to double the time count, to recover an overdraft of an unsuccessful subtraction, and during START OR STOP A+B).

4-204. Addition Mode (NR←NR+DR). At the beginning of the process cycle, the ADD line is High and WORD DBL CLK pulses High. Together, the two signals reset U6B via U27D. This sets the initial conditions for the addition: U3 does not receive a carry in (U3 pin 13).

4-205. Assume the circuit is to add 25 and 35. In this example, the registers would appear as:

$$\begin{array}{ccccc} \text{NR} & + & \text{DR} & \rightarrow & \text{NR} \\ \underbrace{[0000..\,.25]}_{16} & + & \underbrace{[0000..\,.35]}_{16} & = & \underbrace{[0000..\,.60]}_{16} \end{array}$$

The 5's are added first. Both 5's are in BCD form and are applied to the A and B inputs of U3 $\left({}^{A}_{0}\mathrm{D}\ {}^{A}_{1}\mathrm{C}\ {}^{A}_{0}\mathrm{B}\ {}^{A}_{1}\mathrm{A},\ {}^{B}_{0}\mathrm{D}\ {}^{B}_{1}\mathrm{C}\ {}^{B}_{0}\mathrm{B}\ {}^{B}_{1}\mathrm{A}\right)$. The Σ output data is the sum of these two numbers and is expressed in binary $\left({}^{\Sigma}_{1}\mathrm{D}\ {}^{\Sigma}_{0}\mathrm{C}\ {}^{\Sigma}_{1}\mathrm{B}\ {}^{\Sigma}_{0}\mathrm{A}\right)$. Since the counter circuits operate in BCD only, this code must be converted back to BCD. A second adder, U2, adds a zero when the sum is 0 to 9 and adds 6 when the sum is 10 to 18.

A13 Continued

4-206. U5A and B detect when numbers are from 10 to 15, while numbers from 16-18 are indicated by C4 going High (U3). The C4 line is a carry output. Any one of these sources will cause the output of U5C to go High. In the example, the result (10) is a Low output on U5. The High output of U5C applies "6" to the "A" inputs of U2 $\left(\underset{0}{A_D}\,\underset{1}{A_C}\,\underset{1}{A_B}\,\underset{0}{A_A}\right)$. It also places a High on the D input of U6B. When the 10 and 6 are added in U2, the result is a "0" and a carry. To this point, the entire addition appears as follows:

$$\begin{array}{rr} (5) & 0101 \\ (5) & +0101 \\ \hline (10) & 1010 \\ & \uparrow \\ & \text{Binary} \end{array} \nearrow \begin{array}{rl} (10) & 1010 \\ (6) & \underline{+0110} \leftarrow \text{conversion number} \\ 1 & 0000 \leftarrow \text{BCD} \\ \nwarrow & \text{carry in (CO)} \end{array}$$

4-207. The "0" output of U2 is stored in the Numerator register (with a LOAD A/S code on the NR EN lines), while the carry of 1 (output of U5C) is clocked from the D input of U6B into the CO input of U3. The next addition adds the next two numbers, plus the carry of 1, e.g.,

$$\begin{array}{rr} (2) & 0010 \\ (3) & +0011 \\ \hline (5) & 0101 \end{array} \nearrow \begin{array}{rl} (5) & 0101 \\ (1) & \underline{+0001} \leftarrow \text{CO} \\ (6) & 0110 \end{array}$$

The remaining 14 additions are 0+0 = 0, so that the final answer stored in NR is 60 $(\underbrace{000\,.\,.\,.60}_{16})$.

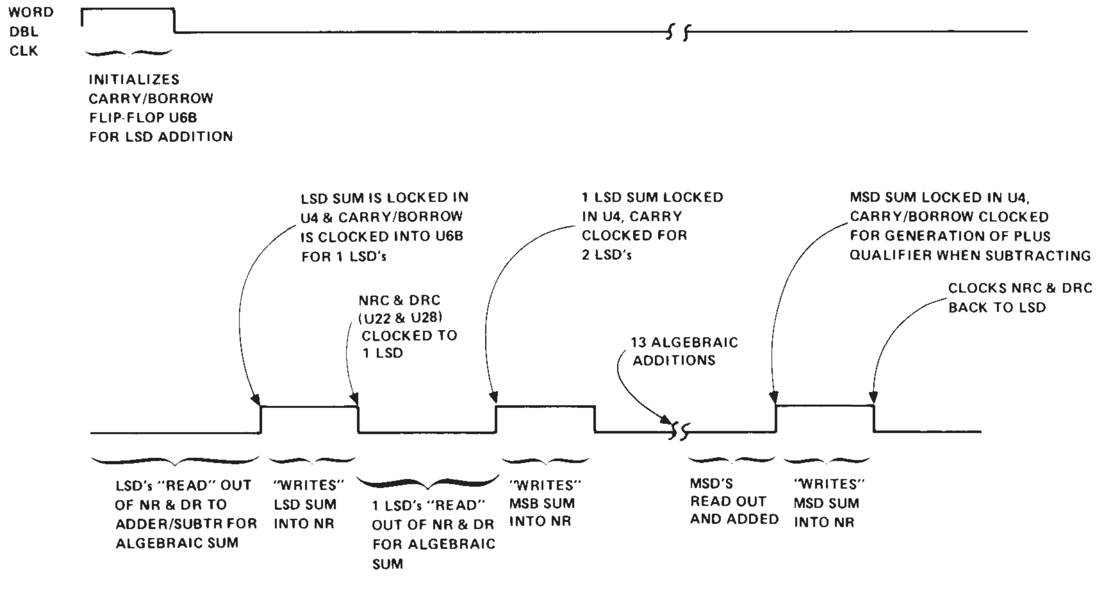

WORD
DBL
CLK
INITIALIZES CARRY/BORROW FLIP-FLOP U6B FOR LSD ADDITION
LSD SUM IS LOCKED IN U4 & CARRY/BORROW IS CLOCKED INTO U6B FOR 1 LSD's
NRC & DRC (U22 & U28) CLOCKED TO 1 LSD
1 LSD SUM LOCKED IN U4, CARRY CLOCKED FOR 2 LSD's
13 ALGEBRAIC ADDITIONS
MSD SUM LOCKED IN U4, CARRY/BORROW CLOCKED FOR GENERATION OF PLUS QUALIFIER WHEN SUBTRACTING
CLOCKS NRC & DRC BACK TO LSD
LSD's "READ" OUT OF NR & DR TO ADDER/SUBTR FOR ALGEBRAIC SUM
"WRITES" LSD SUM INTO NR
1 LSD's "READ" OUT OF NR & DR FOR ALGEBRAIC SUM
"WRITES" MSB SUM INTO NR
MSD'S READ OUT AND ADDED
"WRITES" MSD SUM INTO NR

Figure 4-24. Process Cycle Diagram of Addition

A13 Continued

4-208. Subtraction Mode (NR←NR-DR). During a subtraction, the ADD line is Low. The state of this line produces four important conditions: 1) It disables U5A and B from detecting numbers from 10-15, 2) It places a possible code of "10" or "0" on the A input of U2 $(\overset{A}{1}\,\overset{A}{0}\,\overset{A}{0}\,\overset{A}{1}$ + CO of 1 is effectively 10 and $\overset{A}{1}\,\overset{A}{1}\,\overset{A}{1}\,\overset{A}{1}$ + CO of 1 is effectively 0 when C4 from U2 is ignored), 3) WORD DBL CLK sets U6B via U27B, which causes a carry 1 in U3, and 4) It enables the exclusive OR gates of U11A, B, C, D. This last condition causes an inversion of the DR outputs and has the effect of taking a negative number and adding 15 to it (actually 16 with CO).

4-209. Assume that two sets of numbers are going to be subtracted: 7 minus 9 followed by 8 minus 5 or, seen differently, 87 minus 59. The exclusive OR gates invert the 9 code (1001) into a code of 6 (0110). This number is added in U3 to the NR number. One of the initial conditions was the setting of U6B. This places a High on the CO input and results in adding a 1 to the other two numbers. To this point, the addition process appears as follows:

$$\begin{array}{llll}
\text{NR(7) 0111} & (7)\ \ 0111 & \nearrow & (13)\ \ 1101 \\
\text{DR(9) 1001} \rightarrow \text{complement} \rightarrow & \underline{(6)\ +0110} & \text{CO} \rightarrow & \underline{(1)\ +0001} \\
 & (13)\ \ 1101 & & (14)\ \ 1110 \leftarrow \text{binary output of U3}
\end{array}$$

4-210. Since the sum is less than 16, the C4 output of U3 remains Low. The output of U5C is, therefore, Low. U5C and U7A place a code of 9 on the A inputs of U2 and supply a carry input to CO. The result of the addition in U2 is as follows:

$$\begin{array}{rlll}
(14)\ 1110 & \nearrow & (7)\ \ 0111 & \\
(9)\ \underline{+1001} & & (1)\ \underline{+0001} & \leftarrow \text{(CO), therefore 7-9 = 8.} \\
1\ \ 0111 & & (8)\ \ 1000 & \\
\uparrow\ \ \ \ \ \ \ \ & & & \\
\text{lost}\ \ \ \ \ & & &
\end{array}$$

4-211. When subtracting a larger number from a smaller number, as done here, a digit must be borrowed from the next higher column. This circuit accomplishes borrowing by *not* adding a 1 to the next set of numbers. When REG CLK goes High it clocks the Low on the D input of U6B into the CO input of U3. When REG clock goes Low, it clocks the next set of numbers onto U3's input lines. The next set of numbers in this example is 5 and 8. As before, the 5 is inverted in the exclusive OR gates and added with 8 in U3. This time, however, a 1 is not added in U3: the result of borrowing. The addition appears as follows:

$$\begin{array}{lrl}
\text{NR (8) 1000} & (8) & \ \ 1000 \\
\text{DR (5) 0101} \rightarrow \text{complement} \rightarrow & (10) & \underline{+1010} \\
 & (18)\ 1 & \ \ 0010\ \text{binary} \\
 & \uparrow & \\
 & \text{lost} &
\end{array}$$

4-212. Since the sum is greater than 15, the C4 output goes High. This causes a High on the output of U5C, which, along with U7A, produces a code of 15 on U2's A inputs and a High on the carry input, CO. Notice, also, the High on the D input of U6B, which will produce a carry in for U3 on the next positive edge of REG CLK. At the same time, the $\overline{Q}$ of U6B goes Low, causing a High output from U27C. This line supplies the plus qualifier to A14A(14). The addition in U2 appears as follows:

$$\begin{array}{rrlll}
(2) & 0010 & \nearrow & (1)\ \ 0001 & \\
(15) & \underline{+1111} & & (1)\ \underline{+0001} & \leftarrow \text{CO} \\
1 & 0001 & & (2)\ \ 0010 & \\
\uparrow & & & & \\
\text{lost} & & & &
\end{array}$$

For the next 14 digits, the operation is 0-0 = 0. The result of the two subtractions is stored in the Numerator register and appears as $\underbrace{(000\ldots28)}_{16}$ (87-59 = 28).

A13 Continued

4-213. DIVISION PROCESS, QMC, AND QR. The previous example of subtracting two numbers is only one portion of the arithmetic process. The process is a division, not a subtraction, and is accomplished by performing a *series of successful subtractions.* A successful subtraction is when all 16 digits in the DR have been subtracted (one time only) from all 16 digits in the NR. The two numbers in the previous example will serve to demonstrate the entire division.

4-214. The first subtraction gave a difference of 28, which was stored in the NR. At the end of the subtraction (all 16 digits), the A14 board examines the state of the PLUS line. If this line is High, the $\overline{\text{QMC CLK}}$ line pulses Low and then returns High and causes the QMC (U23) to increment by one, indicating a successful subtraction. Another subtraction can now be attempted; this one, however, is not successful.

$$\begin{array}{r} 0...00028 \\ -0...00059 \\ \hline 9...99969 \end{array}$$

After subtraction, the PLUS line is Low, and the QMC does not increment. Instead, a new set of commands is generated from A15. These commands cause the QR to accept the "1" stored in QMC; force the circuit to add

$$\begin{array}{r} 9...9969 \\ 0...0059 \\ \hline \underset{\substack{\uparrow \\ \text{lost}}}{1}\ \underbrace{0...0028}_{16} \end{array}$$

and place the answer in NR; and, once done, cause the NR contents to shift one place to the left. The last operation is done with a 15 pulse cycle. That is, 15 REG CLK pulses are applied to NRC (U22), causing the left most zero in the NR to become the least significant digit. This operation converts

$$\underbrace{000...28}_{16} \text{ to } \underbrace{00...280}_{16}.$$

4-215. The QMC is reset and another subtraction process continues, this time with the numbers

$$\begin{array}{r} 280 \leftarrow \text{shifted NR.} \\ \underline{-\ 59} \end{array}$$

The DR contents can be successfully subtracted four times before a negative answer appears. At that time, the 4 is also entered into the QR RAM. The entire process has produced an answer of 1.4.

$$\begin{array}{r} 1.4 \\ 59\overline{)87.00} \\ \underline{59} \\ 28\ 0 \\ \underline{23\ 6} \end{array}$$

The division process continues until QR has enough resolution.

4-216. Before the answer is sent to the display, the multiplier of the measurement (K, M, μ, etc.) must be determined. The QMC is used in the display formatting routine to keep track of the annunciator code. After formatting, the contents of QMC are read out of U23 and stored in the three D-type flip-flops, U15 A and B and U6A. The stored code is used to light the annunciator.

MULT STORAGE	(NANO MULT=L) ANNUNCIATOR	(NANO MULT=H) ANNUNCIATOR
000	G	n
001	M	μ
010	k	m
011	units	units
100	m	k
101	μ	M
110	n	G
111	not allowed	not allowed

A13 Continued

4-217. DISPLAY CYCLE. The DR RAM is used to output measurement readings to the display. When this occurs, the DRC requires 11 pulses to output all of the DR data; but it requires 12 pulses if a minus sign is to be displayed.

4-218. At the start of the display cycle, the DR CLK EN line goes High, and REG CLK begins clocking the DRC (U28). The DR outputs 11 words of data (0 to 10) and then a decision is made whether to light the hard-wired minus sign in the display. At this point the output code of DRC is 10 (1010). This code enables U18B, causing U28(9) to go Low. The DRC loads in the code on the ABCD lines. If the SIGN - line is High, U25A is disabled and places a "0" on the input lines. The next clock pulse returns the DRC count to zero. If SIGN - is Low, U25A is enabled and places an "11" on the DRC lines. This code turns on the hard-wired minus sign in the display. When lamp test is active DRC cycles through all 16 states.

4-219. A14 Qualifier

4-220. The A14 board selects the proper qualifier for each process cycle. It also stores the two most significant digits of the next ROM address code. Located on this board is the DPLR counter and DPLK counter. A comparison circuit is used to position the decimal point under certain conditions.

4-221. QUALIFIER CIRCUITS. Of all the returning qualifiers that are available for selection, only one is chosen and sent to A15. The selected qualifier is the output of U1 (far right of schematic) and is sent to A15 as SV7(T). This is the LSD in the octal code for the next ROM address. An example is helpful in understanding the principle of selecting the various ROM addresses. (A summary is included at the end of this description.)

4-222. Next State Address Storage. Assume the ROMs on A15 have just been addressed to location 211 (see Processor Flow Charts, Section V). The ROMs output a new set of commands. Part of these commands are used to generate the next ROM address; these are the six SV(T+1) lines (see smaller cutout in schematic). Shortly after this code appears on the input lines of U23, the code states are clocked into storage by WORD DBL CLK. In this example, the stored code is 15X, with X being the code's LSD and unknown at this time. Later, X will be replaced by the returning qualifier state (1 or 0).

4-223. Qualifier Selection. As the counter performs the operations asked for by the ROM commands, qualifiers are sent to A14, giving information on the result of these operations. However, at *this* ROM state, the counter is interested in only two qualifiers: PI Data and BKPT 6. These qualifiers are selected for examination, using the code stored in U23. The Q1, Q2, and Q3 outputs of U23 comprise the MSD of the stored next-state ROM address (001 is the 1 of 15X). These 3 lines are decoded in U24 to pull the "1" output Low (pin 12). This allows U16C and U17F to enable qualifier switch U8. The next most significant digit is on the Q4, Q5, and Q6 outputs of U23. This coded digit is 5 (101 is the 5 of 15X). These lines connect to the select lines (S1, S2, S4) of each qualifier switch; however, these lines affect only the enabled switch, U8. This code selects input I5. Tracing the source of input I5 reveals that this input connects to the PI DATA line and the S1-6 switch (BKPT-6): the two qualifiers shown in the flow chart. The qualifier state is inverted on the Z output and again in U1. It is then applied to the D input of U32A. When the next ROM cycle begins, ROM CLK clocks the qualifier to the Q output as SV7(T). The other SV(T) states are also clocked out of U31 with ROM CLK. If there is *not* plug-in data and break point 6 is *not* selected, the qualifier is "1" and the next ROM address is 151. If one of these qualifiers is true, the next ROM address is 150. The result of the qualifier, then, determines the direction of program flow, as shown in the flow charts.

4-224. Summary. The two most significant octal digits of the next ROM address are clocked into storage (U23) with WORD DBL CLK. U24 decodes the MSD to enable a qualifier switch. The enabled qualifier switch shares the same number as the value of the MSD in SV(T+1). The second most significant digit stored in U23 selects an input of the enabled qualifier switch. The switch passes the qualifier on that input to the inverted output, through U1, and onto U32A. The next ROM CLK pulse clocks U31 and U32A and places the address code onto the ROM's address lines. The input to the qualifier switch may be the result of combinational logic for several qualifiers.

A14 Continued

4-225. DPLR CIRCUIT. The abbreviation DPLR stands for "decimal point locator for the result." The circuit is a 6-bit counter comprised of up/down counter U29 and flip-flops U38A and U38B. The direction of counting is determined by the commands listed in the flow chart. Before counting begins, the circuits are *always* reset by the DPLR← - 1 command. This line resets U38A and B and loads a code of 15 into U29 (D inputs held High). The DPLR code is sent out of A14 via U20A, B, C, and D and U30A and B when the $\overline{\text{PI XMT}}$ line is High. When the $\overline{\text{PI XMT}}$ line is Low, the DP lines are high impedance to allow a plug-in to load decimal point data into DPLK.

4-226. Count Up Mode. In a "count up" operation, the flow chart command is DPLR ← DPLR+1. The purpose is to shift the decimal point one place to the left. The command places $\overline{\text{DPLR UP}}$ to a Low and pulses the $\overline{\text{DPLR CLK}}$ line Low. If the output code of U29 is 15 (as it is initially), a pulse is *always* produced at RIP CLK that will toggle flip-flop U38A through inverter U37B. The actual clocking occurs on the rising edge of RIP CLK when the code changes from 15 to 0. Flip-flop U38B will toggle at this same time *only* if U38A(13) is High (as it is initially), since this causes U37C(10) to be High.

4-227. Count Down Mode. In a "count down" operation, the flow chart command is DPLR←DPLR -1. The purpose is to shift the decimal point one place to the right. The command places $\overline{\text{DPLR UP}}$ to a High state and pulses the $\overline{\text{DPLR CLK}}$ line Low. This causes U29 to decrement its count by one. If the output code of U29 is zero, a pulse is *always* produced at RIP CLK that will toggle flip-flop U38A through inverter U37B. The actual clocking occurs on the rising edge of RIP CLK when the code changes from 0 to 15. Flip-flop U38B will toggle at this same time *only* if U38A(13) is Low, since this causes U37C(10) to be High.

4-228. Relating DPLR Code to D.P. Position. Each code of the DPLR relates to a specific placement of the decimal point in the display. Figure 4-25 shows the decimal point in the display and outside of the display. The ranges outside the display are possibly used during computation. Generally, the positive range codes are used in giga-unit arithmetic and negative range in nano-unit arithmetic. To determine the negative code, take the 2's complement of the positive code. For example, a code of -1 appears as follows:

DPLR:	-/+	E	D	C	B	A	
+1 code:	0	0	0	0	0	1	
Take complement:	1	1	1	1	1	0	
add one: (2's complement)	1	1	1	1	1	1	= -1 code

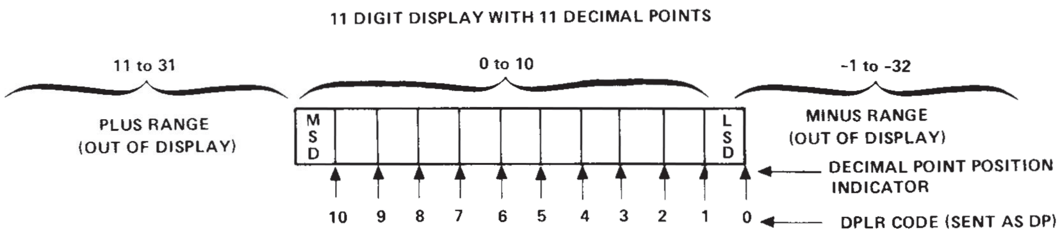


Figure 4-25. Relation of D.P. Codes to Display Position

4-229. DPLK CIRCUIT. The abbreviation DPLK stands for "decimal point locator for K". The K refers to K data from the plug-in. The counter is used in several operations. Briefly, it is used in computer dump to determine when all characters in the DR and NR have been strobed out; it recognizes when all 16 characters in NR have been examined for purposes of determining resolution; it stores the decimal point code for K data; it is used in the serial out routine to determine when all 16 characters have been examined; and, in general, it is the source of qualifier signals.

4-230. Resetting and Counting. The DPLK counter is *always* reset prior to use. Reset occurs when the $\overline{\text{DPLK} \leftarrow -1}$ line goes Low. This clears the 4-bit counter U13 via U5D and resets flip-flops U14A and U14B. This results in High output levels from U12B and D, U5B and C, and the $\overline{Q}$ outputs of U14A and B. These points are considered the output lines of the DPLK counter.

4-231. Even through U13 is connected for a count-up mode, using the inverters on the output lines and the $\overline{Q}$ outputs of U14A and B constitutes a count-down mode by forming the complement of the code. The reset code is equivalent to the first count-down from zero; therefore, all High output levels constitute a count of -1

$$\begin{pmatrix} -/+ & E & D & C & B & A \\ 1 & 1 & 1 & 1 & 1 & 1 \end{pmatrix}$$

Future count downs are accomplished with the $\overline{\text{DPLK CLK}}$ line. Each clock pulse decrements the counter by one count; for example, the next clock pulse sets the counter to -2

$$\begin{pmatrix} -/+ & E & D & C & B & C \\ 1 & 1 & 1 & 1 & 1 & 0 \end{pmatrix}$$

4-232. Loading Plug-In Decimal Point Data. When using K data from the plug-in, the $\overline{\text{DPLK} \leftarrow \text{DPLK PI}}$ command line goes Low to enter the decimal point code into DPLK storage. The LOAD input of U13 goes Low and allows the DP C, D, E, and F code to be entered into U13 storage. Entering the DP A and DP B states into U14A and B requires a different approach. Prior to loading from the plug-in, a $\overline{\text{DPLK} \leftarrow -1}$ command is generated. The $\overline{Q}$ outputs of U14A and B, therefore, are initially High. If DP A is Low, U21D, U21F, and U22D will cause U14A to *set* with the $\overline{\text{DPLK} \leftarrow \text{DPLK PI}}$ pulse. If DP B is Low, U21B, U21F, and U22C will cause U14B to *set* with the $\overline{\text{DPLK} \leftarrow \text{DPLK PI}}$ pulse. If neither of these conditions exists, the flip-flop will remain *reset*.

4-233. Generating Display Clock. The DISP CLK line is used to strobe the display at a much slower rate than REG CLK can normally provide. The DISP CLK line is a result of dividing the $\overline{\text{DPLK CLK}}$ signal by eight. This line continuously pulses Low during display. On the fourth Low-to-High transition of $\overline{\text{DPLK CLK}}$, the QA output of U13 goes High and on the eighth pulse it goes Low. The High-to-Low transition causes a new digit to be addressed and strobed and generates a blanking pulse for the display.

4-234. COMPARATOR DESCRIPTION. The comparator circuit compares the 6-bit DPLR code to one of four possible data sources. Selection of a data source is shown on the A14 schematic (table in large cutout). The result of comparison is a $\overline{\text{DPLR=}}$ qualifier or a DPLR≥ qualifier.

4-235. Switches U27 and U35 select the appropriate data code (ABCD) for comparison to the DPLR code. When a comparison is made to the DPLK code, two additional lines are compared. These are -/+ (from U12B) and E (from U12D). For any comparison other than DPLK, the FLAG=H line is High, forcing the outputs of U12B and U12D Low. The remaining 4-bits are provided by the display position A, B, C, D code.

4-236. Equality Comparison. When comparing DPLR to DPLK, the five code lines (A,B,C,D,E) are compared in U28, yielding a High output from A=B when the codes are the same. The sign (-/+) bits are compared in exclusive OR gate U37A, which yields a Low with equality. U37D inverts the sign comparison; therefore, when the A through E codes are equal, U30D output drives the $\overline{\text{DPLR=}}$ qualifier Low.

4-237. Magnitude Comparison. Switch U36B, C, and D determines whether DPLR is greater than the data being compared. The switch is controlled by U37A and inverter U37D. If the sign bits are *not* equal, U36B, C, and D passes the sign of the DPLR (from U38 pin 8). If the sign is positive (Low), then DPLR is greater, since the other sign had to be negative. This sets the

A14 Continued

DPLR> qualifier High through U36D. Conversely, a negative (High) sign sets U36(6) Low, indicating that DPLR is smaller. When the signs are equal, the U36B, C, D switch is capable of passing the A<B output of U28. If A<B is Low, the DPLR code is greater than the comparator's code and the output of U36D is High.

4-238. Example of Comparison: When the counter is operating out of the AUTO mode, the decimal point position on the display is fixed and the measured number is positioned around it. The DISPLAY POSITION switch controls the decimal point placement from the front panel. The placement can also be controlled remotely or from the plug-in. Since the code that positions the decimal point is derived from the DPLR, the DPLR must be made to agree with the display position code.

4-239. The states of the $\overline{\text{RMT}}$ and $\overline{\text{PI DISP POS/GT SEL}}$ lines determine which display position code is used (front panel, remote, or plug-in). The FLAG=H line is High when comparing for display position. Gates U22B, U6D, and U6C control the selection of input lines for U27 and U35. The selected outputs are sent to the B inputs of U28 where they are compared to the DPLR code on the A inputs.

4-240. If the DPLR code equals the display position code, the $\overline{\text{DPLR=}}$ qualifier will be Low. In this case, the measurement data is properly aligned around the selected decimal point position and no further action is required. When the two codes do not equal, the state of the DPLR> determines whether DPLR should be incremented or decremented, i.e., should the displayed digits be shifted to the left or to the right. This process ends when $\overline{\text{DPLR=}}$ becomes active.

4-241. A15 ROM

4-242. The A15 board contains four ROMs, used for generating the command lines. These lines control the counter's internal operation in accordance with the flow chart. Also present is the Multivibrator Clock: the source of all clock signals used in timing or in the shifting of data. Associated with this is the Processor Timing circuit which produces MSB, $\overline{\text{ROM CLK}}$, $\overline{\text{SINGLE PULSE}}$, and WORD DBL CLK pulses after a given number of REG CLK pulses. The remaining circuits are used in determining the resolution, decimal point placement in AUTO, and the status of the asterisk light.

4-243. ROMS AND COMMAND GENERATION. Each of the four ROMs on A15 are addressed by the eight lines entering the lower left of the schematic. As shown in the example below, seven of the input lines comprise an octal code; these codes are the *state address* numbers found throughout the flow chart. The remaining line is MSB. The ROMs output two sets of program codes: one set when MSB =1 and a second set when MSB =0. Each ROM contains 256 separate locations that store a 4-bit program code; an address from 128 to 255 is selected when MSB =1, while an address from 0-127 is selected when MSB =0. Example:

Octal State Address (261)	Binary Code	Signal Lines	ROM Inputs	ROM Address
	1	MSB	128	128
2	0	SV1(T)	64	
	1	SV2(T)	32	32
	0	SV3(T)	16	
6	1	SV4(T)	8	8
	1	SV5(T)	4	4
	0	SV6(T)	2	
1	1	SV7(T)	1	+1
				173

When MSB goes to 0, the ROM address becomes 32+8+4+1 = 45.

4-244. ROM CIRCUITS. The *program codes* (located in the ROMs) generate a group of *commands* by means of combinational logic and decoding devices or by simply using the lines as they appear at the ROM. Since both sets of program codes must generate commands, the first set of program codes are stored until the second set is generated. They are then converted to commands and sent out at the same time.

4-245. The first set of codes (MSB=1) is stored in U1 and U25A and in U17 on the negative transition to WORD DBL CLK. A14 stores the SV (T+1) codes on the positive transition of WORD DBL CLK. (These two transitions occur at the same time.) U18 decodes the output of U17 into separate command lines. The MSB line also goes Low at this time, and the ROMs output the second set of program codes. After a 350 ns delay, the SINGLE PULSE line pulses Low. This line pulses the D inputs and U9 and U33 and allows the two ICs to decode the ROM outputs. The new data on the outputs of U9 and U33 generate command lines but only for the duration of SINGLE PULSE. When SINGLE PULSE is High, U9 and U33 are effectively inhibited since they are 4 to 10 line decoders and a High on the D line (weighted 8) selects the upper eight codes (8 and 9 not used). With the D line Low, the remaining lines (A,B,C = 1,2,4) can select one of the output lines (0 to 7). Zero output is selected as a "do nothing" command. SINGLE PULSE and its inverse are also used to gate other commands (see "P" commands in Table 5-4).

4-246. NEW ADDRESS GENERATION. The address code for the next ROM cycle is a product of the current ROM cycle. While MSB equals 1, a portion of the ROM outputs (the SV(T+1) lines) are stored in A14. These lines are clocked into storage with the positive transition of WORD DBL CLK. See Figure 4-26. The lines then appear on the output of the first storage device. When the next ROM CLK pulses Low to High, these codes are shifted to the output of the second storage device; they are then used as the address code for the next ROM cycle.

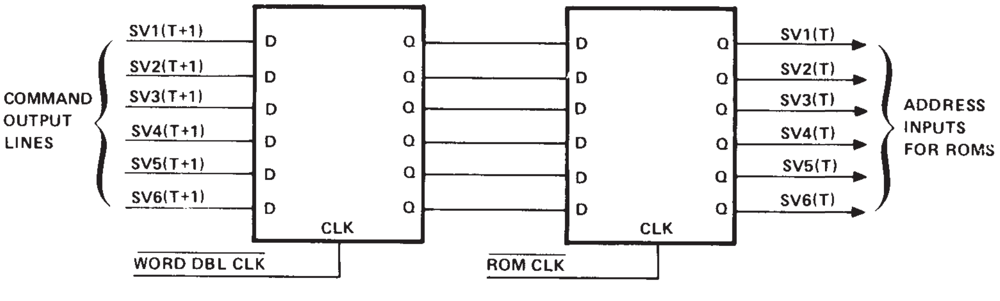


Figure 4-26. A14 ROM Address Storage

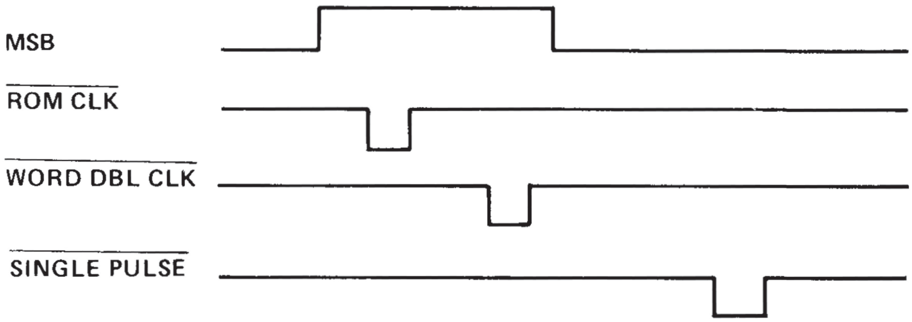
4-247. PROCESS TIMING CIRCUITS. The Multivibrator Clock circuit (U5A and B) generates a 4 MHz rectangular wave that produces all of the clock signals used in instrument timing. These signals include ROM CLK, WORD DBL CLK, REG CLK, PI CLK, MSB, and SINGLE PULSE. The signals are generated during one process cycle, which is defined as the time between two ROM CLK pulses.

4-248. The Processor Timing circuit operates in three basic modes by generating 1, 15, or 16 REG CLK pulses, according to the following chart. 1 PULSE COUNT, and 15 PULSE COUNT are ROM generated commands. These three modes are explained in more detail under Examples 1, 2, and 3 below. Examples 4 and 5 explain the effect on 15 and 16 pulse cylces during display and when loading the registers from the scalers.

Table 4-5. Commands for Processor Timing Modes

1 PULSE COUNT	15 PULSE COUNT	# of REG CLK PULSES GENERATED
L	---	1
H	H	15
H	L	16

4-249. The following timing diagram segment applies to this circuit, regardless of the circuit's operating mode.



4-250. *Example 1:* Assume the A13's NR and DR are to exchange all 16 characters of data. This requires 16 pulses of REG CLK between the two ROM CLK pulses. The description is related to the timing diagram, Figure 4-27 and the A15 schematic. The numbered circles in the text relate to those found in the timing diagram and on the schematics.

4-251. The output of MV CLK (TP8) clocks in the High on U39A(2). The resultant High on the Q output enables U31A to pass MV CLK (inverted through U6C) to the clock input of U23A ② (a divide by two). U22D changes the duty cycle of ③ by extracting every other Low-going pulse from ② and inverting it at ④. U22D is enabled to pass a pulse whenever ③ is Low. U14B inverts ④ to clock U15 with signal ⑤. The first time U15 is clocked, the carry output (CO) goes Low. When U15 has been clocked 16 times, the CO line ⑥ goes High. Each time U15 is clocked, a REG CLK pulse is also generated through U13E, U4C, and D, and U13F to clock the registers on A13.

4-252. The High from CO is inverted in U13D and disables U31C and D. The Low to High transition of U31D(6) clocks U39B, causing its Q output ⑦ to go High. This line is MSB. One clock pulse later (U38C pin 11), U38C is enabled and sets ROM CLK Low.

4-253. The output pulse of U22D ④ that occurs between the sixteenth pulse and the first pulse of the next process cycle performs two operations: 1) While the pulse is positive, it enables U14A to output WORD DBL CLK ⑨. 2) On its negative-going transition, it disables U31B and D to clock U39B back to its original reset state; and it disables U14A, both of which turn off WORD DBL CLK. Notice that the clock pulse ⑤ normally generated by U22D is inhibited by U14B during this time. When U39B is clocked back to its original state, MSB ⑦ goes Low, and a new timing cycle can begin.

4-254. *Example 2*: Assume an unsuccessful subtraction has occurred on A13. The NR contents must shift one place to the left. To do this, the contents are rotated 15 places to the right. Again, refer to Figure 4-27.

4-255. When MSB goes Low, a new set of commands are generated from the ROM circuits. One of the ROM lines, 15 PULSE COUNT, controls the number of clock pulses that U15 will accept before the CO lines goes High. The High of 15 PULSE COUNT enables U38B, which pulls the LOAD input of U15 Low. This inputs the High on U15(3), which has the effect of presetting the counter to a code of one with the first clock pulse ⑤. This pulse also causes CO ⑥ to go Low and disable U18B. When 15 clock pulses have occurred, the CO line returns High.

4-256. *Example 3*: Assume the QRC needs to be incremented by one (QRC←QRC+1). For the execution of this command, only one REG CLK pulse is sent to A13 while QRC CLK EN is active. The internal command that assures a process cycle of one REG CLK is 1 PULSE COUNT. Refer to Figure 4-28.

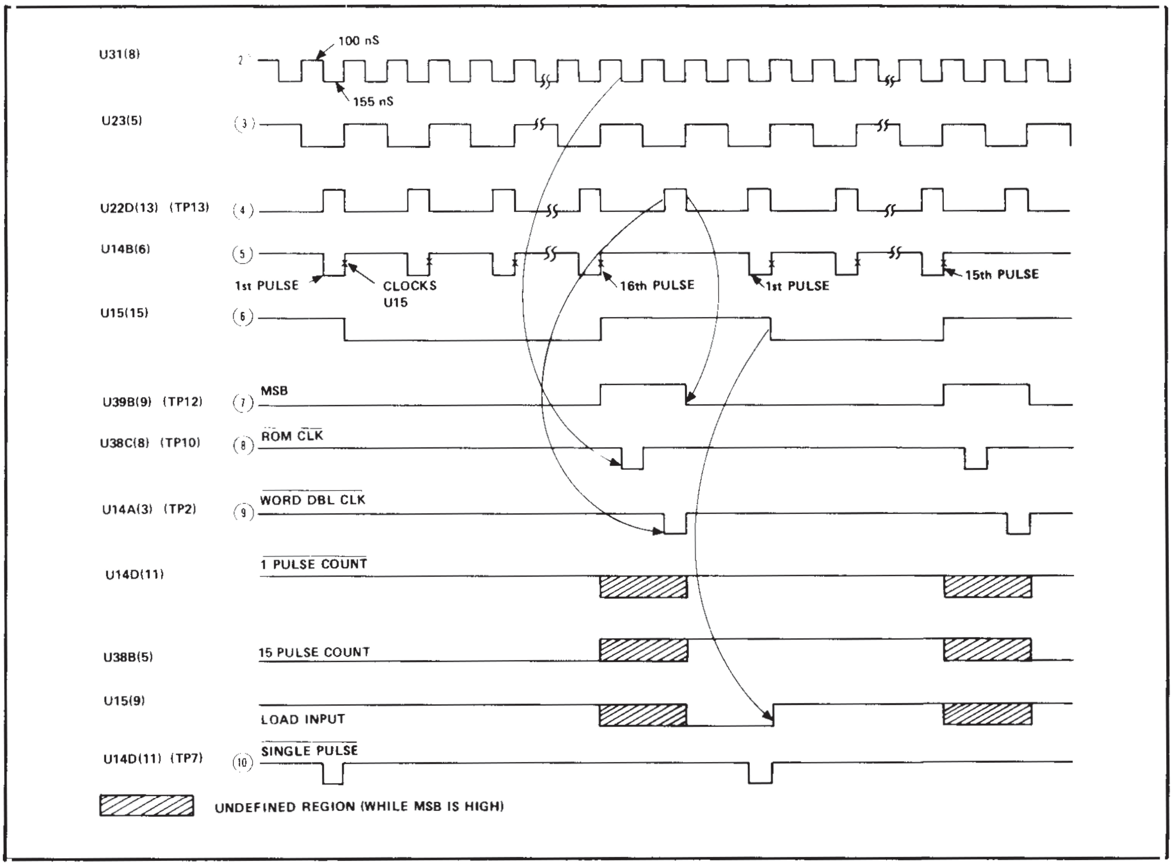


Figure 4-27. 16 and 15 Pulse Cycles

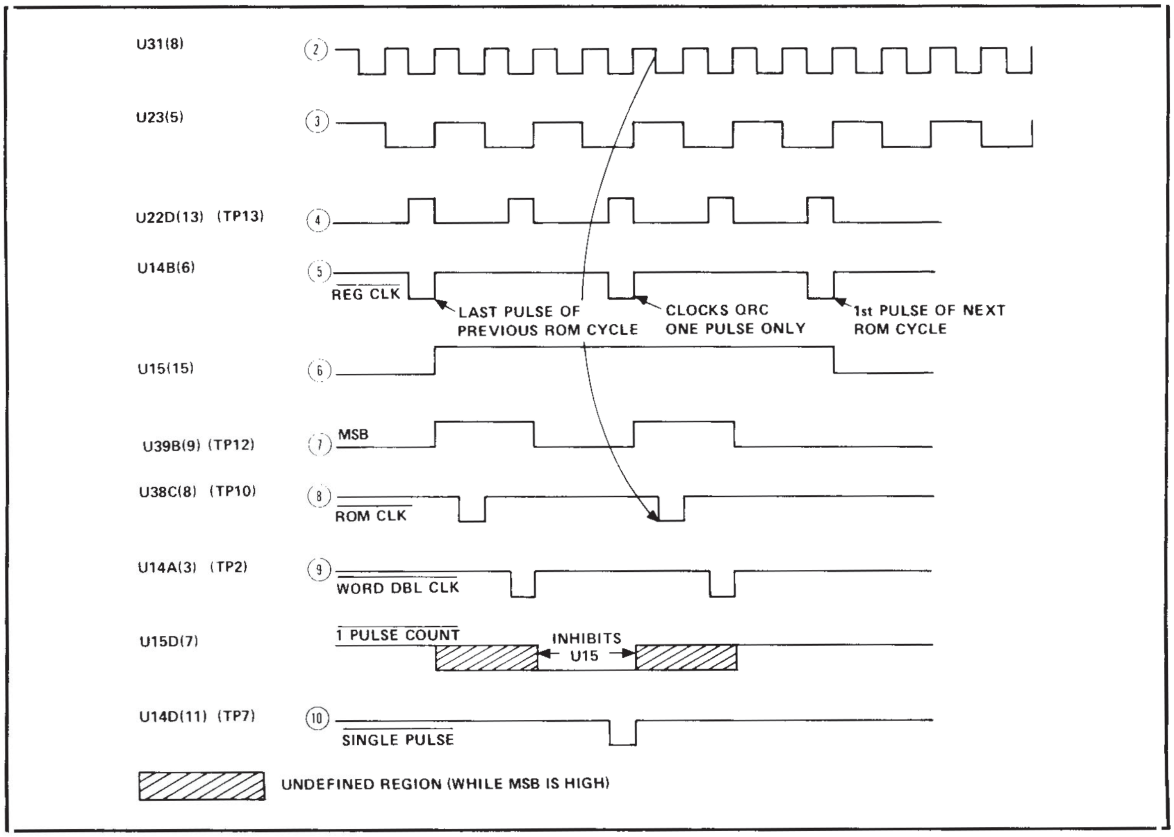


Figure 4-28. 1 Pulse Cycle

4-257. When MSB goes Low (MSB=0), ROM U24 generates $\overline{\text{1 PULSE COUNT}}$. This line inhibits U15 from operating by removing the enable signal (U15 Pin 7). While MSB remains Low, U14B is enabled by U39B. This allows U14B to pass one clock pulse ⑤ through U13E, U4C and D, and U13F. Once the pulse clocks QRC, the purpose of this ROM cycle is complete. What remains is to complete the rest of the timing cycle before continuing to the next.

4-258. The Low of $\overline{\text{1 PULSE COUNT}}$ causes the output of U7B to go High. Since this enables U31B, the Low-to-High transition of U15(15) is not needed to clock U39B. When the output of U22D ④ goes High and then Low, it causes a positive transition at U31(6). This clocks U39B(9) ⑦ High. The High on U39B's Q output combines with signals ② and ③ to produce a $\overline{\text{ROM CLK}}$ pulse ⑧ from U38C(8). This same ④ pulse that clocks U39B also produces REG CLK through U14B, U13E, U4C and D, and U13F. The $\overline{\text{ROM CLK}}$ signal and $\overline{\text{WORD DBL CLK}}$ initiate the process of generating a new set of commands for the next process cycle.

4-259. *Example 4*: Data is strobed from the Time or Events Scaler (A11) by the 4-bit binary output of $\overline{\text{DRC}}$ (A13). This counter is clocked by REG CLK; however, the clock signal's duty cycle is about 2 MHz, which is too fast for the scalers. Since no more than 13 decades of the scalers are ever used (a 10,000 second gate time), the A15 board divides the clock by two (1 MHz) for the first 13 places, then returns to its normal 2 MHz rate for the remaining three places. Refer to Figure 4-29.

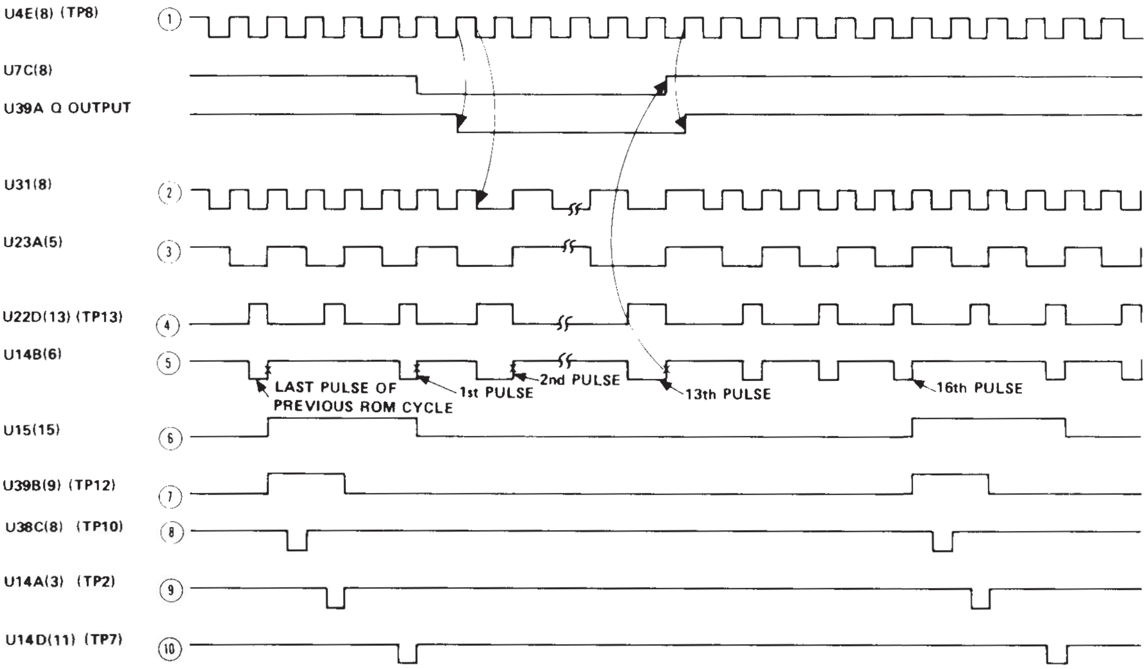


Figure 4-29. Timing for Scaler Strobing

4-260. The output of U7A is High when scaler data is being read into the DR (U3C and U11A) or into the NR (U7D). This High NANDs in U7C with the Low output of U14C. After the first REG CLK pulse, the output of U14C goes High. The next positive transition of MV CLK (TP8) ① clocks the Low on the D input of U39A to the Q output. This enables U22C to pass the Low pulses of MV CLK, which clock U23B (a ÷2 stage). The toggling of U39 also disables U31A and enables U31F, so that the output of U23B (the ÷2) is enabled to ②. As long as this condition exists, REG CLK will also be divided by two. Once U15 has been clocked 13 times, the QC and QD outputs of U15 go High (code of 12). This enables U14C and disables U7C. The next positive transition of MV CLK toggles U39A and allows the remaining pulses to go through U6C and U31A, thereby bypassing U23B.

4-261. *Example 5*: Assume that data is to be displayed. Strobing data into the display requires a much slower clock rate than REG CLK normally provides. During the display cycle, U20C(10) is commanded High. (On the schematic, U20C is located to the near left of the large cutout.) For every process cycle, the SINGLE PULSE line (U20C pin 9) goes High, once. The resultant Low output pulse is sent to A14 as $\overline{\text{DPLK CLK}}$. The A14 board divides these pulses by 8 and sends the A15 board a $\overline{\text{DISP CLK}}$ pulse. Therefore, for every ROM cycle there occurs one SINGLE PULSE, causing one $\overline{\text{DPLK CLK}}$ pulse; for every 8 $\overline{\text{DPLK CLK}}$ pulses there occurs one $\overline{\text{DISP CLK}}$ pulse. (On the schematic, $\overline{\text{DISP CLK}}$ is located in the lower right portion of the cutout.) Since DISP CLK EN is commanded High at this time, the slower $\overline{\text{DISP CLK}}$ signal is sent through U4B and D and U13F and leaves the A15 board as REG CLK.

4-262. DIGIT COUNTER, DIGIT STORAGE, AND ASSOCIATED CIRCUITS. Digit counter, U35, is a 4-bit binary counter. The counter's main function is to keep track of the number of digits that are resolved in a measurement. This is done by, first, counting the number of digits in the time scaler. In a frequency measurement having a 1-second gate time, for example, there will *always* be 9 digits in the time scaler. After the digits are counted, the ROMs issue a command (DS←DC) to store this count in Digit Storage (U34).

4-263. During the process cycle, Digit Counter increments by one each time the Quotient Register stores a calculated digit. When this count equals the count in Digit Storage, the division process has resolved enough digits for the particular gate time used.

4-264. The exclusive OR gates (U36A, B, C, D) compare the code in DC to the code in DS. U36C compares the "D" lines of the two codes; if equal, its output goes Low. Likewise, U36D(11) goes Low when the "B" lines are equal. The two gates combine to enable U29A. Since U36A and U36B are tied to the $\overline{Q}$ outputs of DS, their outputs will be High when the "A" lines are equal (U36A) and "C" lines are equal (U36B). When the two codes are equal, the output of U37A goes Low. This activates the qualifier line $\overline{\text{DC=DS}}$, which signals A14 that no further divisions are needed in the measurement.

4-265. In AUTO, the counter positions the decimal point behind one of the three most significant digits in the display. To do this, the code used to indicate the number of digits (DS) is subtracted from the code used to position the decimal point (DP lines). When DP minus DS gives a difference of -1 to -3, the decimal point is properly aligned. The $\overline{Q}$ outputs of DS provide the inverted code (for subtraction) to be added in U28 to the DP codes, along with a carry in of one (CO input). When the sum code equals 13 to 15 and C4 is Low, the decimal point is considered to be properly aligned. The output of U28 will then enable U21A, which, in turn, activates the $\overline{\text{AUT DP ALN}}$ line via U21B. Example: CHECK, FREQ A, 100 ms, AUTO. Measurement yields .10000000 GHz immediately after computation. At this point, DP=9 and DS=8. In Giga unit arithmetic, the DP is decremented by three each time DP-DS is out of the "aligned" range. Therefore, decrementing by three yields 100.00000 MHz. DP=6 and DS=8. DP-DS = -2, signifying that alignment has been achieved.

4-266. There are instances when the decimal point is not placed behind one of the first three digits, but the decimal point should, nevertheless, be considered aligned. For example, in a totalize measurement, the decimal point is continuously updated as the display accumulates counts. The display overflows when the number of digits exceeds 11.

¦ G M
(1X ¦XX.XXXXXXXXX).

The decimal point must remain fixed for the display to read in gigaunits (G is the highest annunciator). For 12 or greater numbers of resolved digits, the $\overline{\text{Q}}$ outputs of U34A and U34D go High when the display overflows. This enables U11B, U29C ($\overline{\text{ST+STP}}$ line is Low), and U21B, causing the decimal point to remain fixed (corresponding to G-units).

4-267. The decimal point is also considered aligned if U21B is enabled by U29D. This occurs when the number to be displayed is ≥10 G and contains less than 3 digits. In this case, the decimal point is initially positioned out of viewable range (DPLR=+ is Low). For example: $\overset{\text{QR}}{\boxed{\text{XX. . .X1}}}$ 2.G would satisfy the conditions to enable U29D. The display and decimal point would shift left one place and a facititious zero would be inserted in place of the 2 $\overset{\text{DISPLAY}}{\boxed{\text{XX. . .X10}}}$ G. The insertion of a factitious zero would also light the asterisk.

4-268. The $\overline{\text{QMC=6}}$ line goes Low after the QMC has stepped through all possible annunciator codes in an attempt to select the correct multiplier for the measurement's result. Each time the DP codes increment (or decrement) by three, the QMC is also incremented by one to change the multiplier code. The subtraction of DP and DS occurs in an attempt to satisfy the output of U21A (DPLR-DS= -1 to -3). When six attempts have been made to align the decimal point with the proper multiplier, the QMC has selected all available multipliers. The last annunciator is then used, regardless of the decimal point's position. The $\overline{\text{QMC=6}}$ line goes Low to enable U12B, which activates the $\overline{\text{AUT DP ALN}}$ line via U21B.

4-269. The last gate to control $\overline{\text{AUT DP ALN}}$ is U38A. Should a plug-in make time interval measurements in the sub-nanosecond range, U38A forces the decimal point alignment in terms of nanoseconds.

4-270. ASTERISK HARDWARE. The $\overline{\text{LOAD*S}}$ command clocks U25B. A High on the Q output causes the front panel asterisk lamp to light. The D input U25B(12) is High when the * Flip-Flop is "ON" (U10B(6) is Low making U37B(6) High) or when the DS contents are 0, 1, 2, 3, or 4 (U20A(3) or U37C(8) is Low). The asterisk lights under the following conditions:

Factitious zero — asterisk flip-flop is on.
Underflow — DS = 0
Overflow — DS = 0, 1, 2, 3, or 4

4-271. A16 Motherboard

4-272. The A16 assembly is the counter's largest interconnection board. It provides the main source of signal interconnection between the other board assemblies. It contains no electrical parts but does provide connection for several wiring harnesses plus a pressure connector that connects to A17. See motherboard wiring in Section VIII.

4-273. A17 Plug-In Interconnection

4-274. The A17 board is located behind the sheet metal at the rear of the plug-in compartment. The board connects to A16 by means of a pressure connector (P1) and to the plug-in via A17J1 (visible at rear of plug-in compartment).

4-275. A18 10 MHz Oscillator (Oven)

4-276. This unit is a 10 MHz crystal oscillator whose frequency stability is temperature regulated by an internal oven. The unit incorporates an AGC circuit and is also capable of phase locking to an external standard. Before phase locking can occur, however, the two signals must be within one cycle of each other. The specifications are listed in Table 1-3.

4-277. A18 Option 001 Oscillator

4-278. Option 001 is a voltage controlled 10 MHz oscillator. A separate power supply consisting of CR1, Q1, and associated components, provides a "cleaner" source of power. This helps to isolate the oscillator from the switching currents associated with other supplies.

4-279. U1A operates like an amplifier with positive feedback. The positive feedback path is from the noninverted output of U1A(6) through C9, C8, CR2, C4-C6, and crystal Y1. Negative feedback establishes the input bias for U1A. This path is through R5 and R2. The trimmer capacitors C4 and C5 provide frequency adjustment of the oscillator. Diode CR2 is a voltage variable capacitor. When this oscillator is phase locked to a external standard, a voltage from A8 assembly changes automatically to vary the capacitance of this diode. This change of value affects the feedback loop's phase and, therefore, the crystal's exact frequency.

4-280. The inverted output of U1A(5) is fed to buffer U1B(10). The buffer provides isolation between the oscillator and the output stage, Q2. The outputs of U1B(8) and (9) switch from about 4.0 to 4.75 volts. When one output is 4.0V, the other is 4.75V. Level shifter Q2 converts the output of U1B to an approximate TTL level.

4-281. A19, Option 010, 011, Interface Panel

4-282. The A19 assembly provides the interconnection between A12 (optional) and the interface bus. The A2 through A5 switches select the address code for the instrument. The remaining switch selects TALK ALWAYS or ADDRESSABLE.

SECTION V

MAINTENANCE AND SERVICE

5-1. INTRODUCTION

5-2. This section contains maintenance and service information. Included is a table of assemblies, a table of recommended test equipment, overall troubleshooting information and troubleshooting charts, processor flow charts, an in-cabinet performance check, and adjustment procedures.

5-3. ASSEMBLY DESIGNATIONS

5-4. Table 5-1 lists the designations, nomenclature, and Hewlett-Packard part number of assemblies used in the 5345A.

5-5. TEST EQUIPMENT

5-6. Table 5-2 lists test equipment recommended for maintaining the counter and for checking its performance. Test equipment having equivalent characteristics may be substituted for the equipment listed.

5-7. ADJUSTMENTS AND IN-CABINET PERFORMANCE CHECK

5-8. Table 5-6 contains adjustment procedures for the 5345A. Adjustments should be made when necessity is established by the performance test or when components are replaced that change the circuit's operating characteristics.

5-9. PERIODIC MAINTENANCE

5-10. Instrument cooling is accomplished by a fan that intakes air through two air filters. These filters *must* be periodically inspected and cleaned when dust buildup is apparent. This procedure is described in Section III under *AIR FILTER CLEANING.*

Table 5-1. Assembly Designations

Reference Designation	Description	HP Part No.
A1	Cathode Driver Display	05345-60001
A2	Anode Driver Display	05345-60027
A3	Input Attenuator	05345-60038
A3	Input Attenuator (Option 012)	05345-60039
A4	Input Trigger	05345-60004
A5	Interconnect	05345-60005
A6	Switching Regulator	05345-60006
A7	Linear Regulator	05345-60007
A8	PLL Multiplier Noise Generator	05345-60031
A9	Gate Control	05345-60009
A10	Main Gate	5345-60010
A11	Scaler	05345-60011
A12	General Purpose Interface Output (Option 010)	05345-60023
A12	General Purpose Interface I/O (Option 011)	05345-60018
A12	Interface I/O (Option 012)	05345-60021
A13	Adder/Subtracter	05345-60013
A14	Qualifier	05345-60044
A15	ROM	05345-60045
A16	Motherboard	05345-60016
A17	Plug-In Interconnection	05345-60017
A18	10 MHz Oscillator (Oven)	10544-60011
A18	Oscillator (Option 001)	05345-60069
A19	Interface Panel (Option 010)	05345-60024
A19	Interface Panel (Option 011)	05345-60019
A19	Interface Panel (Option 012)	05345-60022
A20	Filter (Option 012)	05345-60030

Table 5-2. Recommended Test Equipment

Instrument Type	Required Characteristics	Recommended Type
Oscilloscope	50 MHz Bandwidth	HP 180A
Vertical Plug-in	50 mV/div Sensitivity	HP 1801A
Time Base Plug-in	50 MHz Bandwidth	HP 1821A
Sampler	10 μs/div	HP 1810A
Test Oscillator	10 Hz to 10 MHz	HP 651B
Signal Generator	10 MHz to 500 MHz	HP 8640B*
Pulse Generator	10 ns pulse width, manual trigger	HP 8007B
DVM	0-25V	HP 3480A/3482A
AC VTVM	20 Hz to 1 MHz	HP 410C
Logic State Analyzer	ROM Test	HP 1601
5345A ASM Tester	ROM Test	HP K13-59992A
Logic Probe	Logic State Test	HP 10525T
Logic Pulser	State Activator	HP 10526T
Logic Comparator	IC Test	HP 10529A
Board Replacement Kit		HP 10597A
Extender Board Kit		HP 10595A

*See NOTE in Table 5-5, step 1.

5-11. OVERALL TROUBLESHOOTING

5-12. There are two methods of troubleshooting the 5345A to board level. The fastest and most efficient means of isolating problems is to use the board replacement kit. If this kit is not available, the trouble isolation method is recommended. This procedure makes use of troubleshooting charts and associated information. Both methods are described in the following paragraphs. In addition, see paragraph entitled *TROUBLESHOOTING AIDS.*

5-13. Board Replacement Method (Kit No. 10597A)

5-14. The board replacement method is the fastest means of isolating problems in the 5345A. Individual board substitution should be used until the defective board is located. Once this has been accomplished, the defective board should be repaired by consulting the circuit theory for that particular board and the signal line mnemonics in SECTION VIII. The *Trouble Isolation Method* can also help in locating the problem to general areas in the board assembly.

5-15. The boards should be substituted on the basis of suspected troubles. It is advisable, however, to ensure the 05345-60006 and 05345-60007 power supply assemblies are functioning properly before installing other board assemblies.

CAUTION

BE SURE TO REMOVE POWER CORD BEFORE REMOVING THE POWER SUPPLY BOARDS.

5-16. Trouble Isolation Method

5-17. The 5345A Overall Troubleshooting flow charts are intended to reveal any basic machine malfunctions. The tests verify the measurement and processor cycles; however, the input amplifiers are not tested. The internal 100 MHz test bypasses the amplifiers. Any suspected input amplifier problems should be tested separately.

5-18. The tests begin when the FUNCTION switch is set to START. This mode checks most of the basic operations during the measurement cycle. Much of the processing cycle is also verified in this mode. Upon successful completion of the Start mode, the frequency mode is set up. This test performs further and more complete testing of the processor.

5-19. Troubleshooting the instrument should be approached as described below. Refer back to this listing when progressing through the troubleshooting procedures.

a. Perform the operations that are outlined in the *Overall Troubleshooting Flow Chart*, Figure 5-1. The troubleshooting charts will isolate the problem to a specific board assembly or to a problem in the processor. When the problem is found to be on a board, consult the board theory in Section IV and the signal line mnemonics in Section VIII.

b. When the problem is in the processor, set up the available test equipment, as outlined in Figure 5-6 or Figure 5-7. Perform the described test while verifying results in Table 5-3, *Processor Flow Test Results*.

c. When an incorrect ROM address is detected, consult *Processor Troubleshooting Symptoms*, Figure 5-8, to determine the troubleshooting approach for the particular symptom.

5-20. TROUBLESHOOTING AIDS

5-21. In addition to the previously described troubleshooting methods, there are some devices unique to the 5345A that can aid in troubleshooting. These units are the 5345 ASM Tester, the Special Test Board, and the Extender Board Kit. These units are described in the following paragraphs.

5-22. 5345A ASM Tester (K13-59992A)

5-23. This tester is used to troubleshoot the processor section (A13, A14, and A15 assemblies) of the 5345A. Procedures for troubleshooting with this tester or with the HP LOGIC STATE ANALYZER are included in this section (Figures 5-6 and 5-7). The performance features of the ASM tester are outlined below. The operating procedures for these features are supplied with the K13-59992A 5345 ASM Tester.

a. Allows the contents of the NR, DR, and QR RAMs in the 5345A to be displayed by the tester. Can also display the inputs to these RAMs. The contents can be read at selected state addresses throughout the PROCESSOR FLOW CHARTS.

b. Aids in troubleshooting the timing circuits of the processor by providing state address advancement with lower-level processor clock signals.

c. Enables a properly operating 5345A to be dynamically compared to a defective 5345A.

5-24. Extender Board Kit (10595A)

5-25. This kit is required for servicing the 5345A Electronic Counter. It allows circuit boards and circuit assemblies to be extended from their plug-in connectors for monitoring signals with the appropriate test equipment. The kit includes the following extender assemblies:

a.	05345-60201 05345-60202	Extender boards for the A6, A7 power supplies, and A8 multiplier assembly.
b.	05345-60203	Extender board for the A9 Main Gate assembly only.
c.	05345-60204	Extender boards for the A10, A11, A12, A13, A14, and A15 assemblies.
d.	05345-60205	Front Panel Extender cable which allows troubleshooting the A1, A2 Display assemblies and A3, A4 Input Amplifier assemblies.

e.	1250-0831	Special adapter for BNC-to-subminiature connector. Used in calibrating the input amplifier assemblies.
f.	05345-60200	This is a special test board. See separate description.

5-26. Special Test Board (05345-60200)

5-27. Although included in the Extender Board Kit, this board provides some unique troubleshooting aids. The operations it can perform and methods for using it are outlined below.

FUNCTIONS PROVIDED

a. Extender board for A10, A11, A12, A13, A14, and A15 board assemblies.

b. Processor Tester. Transfers BCD data from the GATE TIME switch directly into the arithmetic processor. This provides known, good data to the processor, thereby isolating problems between the processor assemblies and data circuits on assemblies within the front end. Specific front end assemblies are A3, A4, A8, A9, and A11.

c. Front End Tester. This enables circuit tests to be made while the instrument is in the measurement phase. The processing phase is inhibited with the test board.

USING THE 05345-60200 TEST BOARD

a. When using as an extender board, install extender board with the two CINCH connectors up and install board to be tested.

b. When using the board to test the processor, follow the procedure below:

   1. Remove the A11 Scaler assembly.

   2. Install the test board, with the connectors marked XA11(A) and XA11(B) into the A11 position of the 5345A motherboard.

   3. Set the 5345A switches as described on the test board under FRONT PANEL FUNCTIONS.

   4. Set switches as outlined under A14 SWITCHES. The BKPT 1, 2, and 7 refer to the test switches located on the top of the A14 board.

NOTE

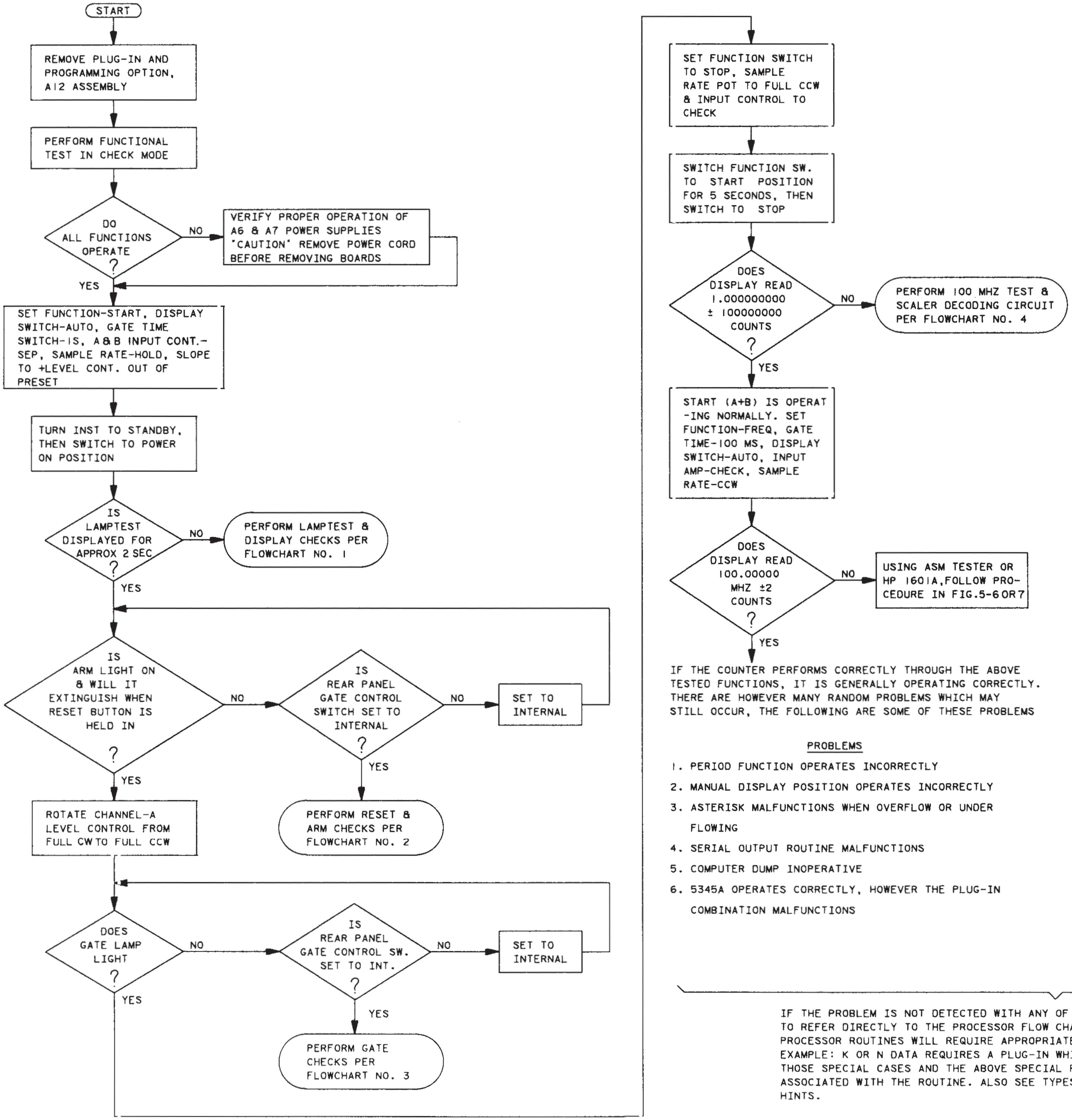
> BKPT-7 must be set and remain set while all tests are performed. Also, note the position of the SAMPLE RATE control when tests are performed.

c. When using the board to troubleshoot the FRONT END, use the following procedure:

   1. Remove the A15 RAM assembly.

   2. Install the test board, with the connectors marked XA15(A) and XA15(B) into the A15 position of the 5345A motherboard.

   3. Troubleshoot circuits associated with the measurement phase. The processor will remain inhibited during this time.


START
REMOVE PLUG-IN AND PROGRAMMING OPTION, A12 ASSEMBLY
PERFORM FUNCTIONAL TEST IN CHECK MODE
DO ALL FUNCTIONS OPERATE ?
NO
VERIFY PROPER OPERATION OF A6 & A7 POWER SUPPLIES 'CAUTION' REMOVE POWER CORD BEFORE REMOVING BOARDS
YES
SET FUNCTION-START, DISPLAY SWITCH-AUTO, GATE TIME SWITCH-1S, A & B INPUT CONT.-SEP, SAMPLE RATE-HOLD, SLOPE TO +LEVEL CONT. OUT OF PRESET
TURN INST TO STANDBY, THEN SWITCH TO POWER ON POSITION
IS LAMPTEST DISPLAYED FOR APPROX 2 SEC ?
NO
PERFORM LAMPTEST & DISPLAY CHECKS PER FLOWCHART NO. 1
YES
IS ARM LIGHT ON & WILL IT EXTINGUISH WHEN RESET BUTTON IS HELD IN ?
NO
IS REAR PANEL GATE CONTROL SWITCH SET TO INTERNAL ?
NO
SET TO INTERNAL
YES
PERFORM RESET & ARM CHECKS PER FLOWCHART NO. 2
YES
ROTATE CHANNEL-A LEVEL CONTROL FROM FULL CW TO FULL CCW
DOES GATE LAMP LIGHT ?
NO
IS REAR PANEL GATE CONTROL SW. SET TO INT. ?
NO
SET TO INTERNAL
YES
PERFORM GATE CHECKS PER FLOWCHART NO. 3
YES
SET FUNCTION SWITCH TO STOP, SAMPLE RATE POT TO FULL CCW & INPUT CONTROL TO CHECK
SWITCH FUNCTION SW. TO START POSITION FOR 5 SECONDS, THEN SWITCH TO STOP
DOES DISPLAY READ 1.000000000 ± 100000000 COUNTS ?
NO
PERFORM 100 MHZ TEST & SCALER DECODING CIRCUIT PER FLOWCHART NO. 4
YES
START (A+B) IS OPERAT-ING NORMALLY. SET FUNCTION-FREQ, GATE TIME-100 MS, DISPLAY SWITCH-AUTO, INPUT AMP-CHECK, SAMPLE RATE-CCW
DOES DISPLAY READ 100.00000 MHZ ±2 COUNTS ?
NO
USING ASM TESTER OR HP 1601A, FOLLOW PRO-CEDURE IN FIG. 5-6 OR 7
YES

IF THE COUNTER PERFORMS CORRECTLY THROUGH THE ABOVE TESTED FUNCTIONS, IT IS GENERALLY OPERATING CORRECTLY. THERE ARE HOWEVER MANY RANDOM PROBLEMS WHICH MAY STILL OCCUR, THE FOLLOWING ARE SOME OF THESE PROBLEMS

NOTE:

WHEN CHECKING FOR CORRECT ROM STATES OR COMMANDS AND QUALIFIERS, SET UP ASM TESTER OR HP 1601 AS OUTLINED IN PROCEDURE FIG. 5-6 OR 5-7

PROBLEMS	TEST
1. PERIOD FUNCTION OPERATES INCORRECTLY	1. ENSURE THAT THE PERIOD + TI QUALIFIER SELECTS STATE 531. ALSO THAT STATE 670 IS SELECTED IN THE DIVIDE ROUTINE
2. MANUAL DISPLAY POSITION OPERATES INCORRECTLY	2. THIS ROUTINE BEGINS AT STATE 510; CHECK COMMANDS AND QUALIFIERS IN THIS ROUTINE
3. ASTERISK MALFUNCTIONS WHEN OVERFLOW OR UNDER FLOWING	3. THIS ROUTINE BEGINS AT STATE 650; CHECK COMMANDS & QUALIFIERS THROUGH THIS ROUTINE
4. SERIAL OUTPUT ROUTINE MALFUNCTIONS	4. SWITCH REAR PANEL ASCII CODE SWITCHES TO THE 'TALK ALWAYS' POSITION; MONITOR STATES BEGINNING AT STATE 730.
5. COMPUTER DUMP INOPERATIVE	5. THIS ROUTINE BEGINS AT STATE 210; CHECK COMMANDS AND QUALIFIERS
6. 5345A OPERATES CORRECTLY, HOWEVER THE PLUG-IN COMBINATION MALFUNCTIONS	6. CHECK ROUTINES BEGINNING AT STATES 150, 170, 050 & 521

IF THE PROBLEM IS NOT DETECTED WITH ANY OF THE ROUTINES, IT WILL BE NECESSARY TO REFER DIRECTLY TO THE PROCESSOR FLOW CHARTS. (FIGURE 5-10) SOME OF THE PROCESSOR ROUTINES WILL REQUIRE APPROPRIATE PLUG-INS TO GET INTO THE ROUTINES EXAMPLE: K OR N DATA REQUIRES A PLUG-IN WHICH CAN PROVIDE K AND N DATA. FOR THOSE SPECIAL CASES AND THE ABOVE SPECIAL PROBLEMS, READ THE FLOWCHART THEORY ASSOCIATED WITH THE ROUTINE. ALSO SEE TYPES OF SYMPTOMS, UNDER TROUBLESHOOTING HINTS.

5345-D-20

Figure 5-1. Overall Troubleshooting Flow Chart

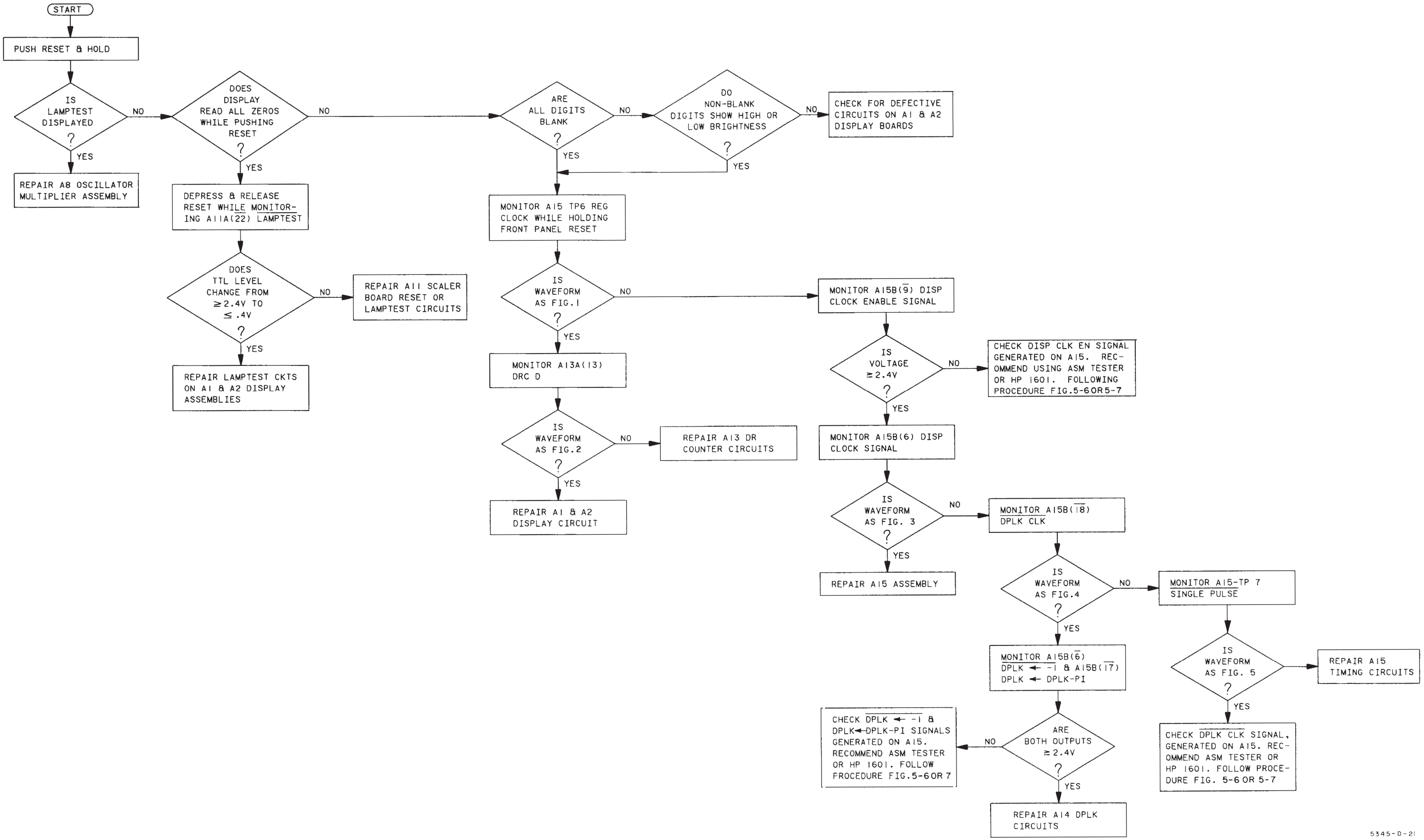

START
PUSH RESET & HOLD
IS LAMPTEST DISPLAYED ?
YES
REPAIR A8 OSCILLATOR MULTIPLIER ASSEMBLY
NO
DOES DISPLAY READ ALL ZEROS WHILE PUSHING RESET ?
YES
DEPRESS & RELEASE RESET WHILE MONITORING A11A(22) LAMPTEST
DOES TTL LEVEL CHANGE FROM ≥2.4V TO ≤.4V ?
NO
REPAIR A11 SCALER BOARD RESET OR LAMPTEST CIRCUITS
YES
REPAIR LAMPTEST CKTS ON A1 & A2 DISPLAY ASSEMBLIES
NO
ARE ALL DIGITS BLANK ?
NO
DO NON-BLANK DIGITS SHOW HIGH OR LOW BRIGHTNESS ?
NO
CHECK FOR DEFECTIVE CIRCUITS ON A1 & A2 DISPLAY BOARDS
YES
YES
MONITOR A15 TP6 REG CLOCK WHILE HOLDING FRONT PANEL RESET
IS WAVEFORM AS FIG.1 ?
YES
MONITOR A13A(13) DRC D
IS WAVEFORM AS FIG.2 ?
NO
REPAIR A13 DR COUNTER CIRCUITS
YES
REPAIR A1 & A2 DISPLAY CIRCUIT
NO
MONITOR A15B(9̄) DISP CLOCK ENABLE SIGNAL
IS VOLTAGE ≥2.4V ?
NO
CHECK DISP CLK EN SIGNAL GENERATED ON A15. RECOMMEND USING ASM TESTER OR HP 1601. FOLLOWING PROCEDURE FIG.5-6 OR 5-7
YES
MONITOR A15B(6) DISP CLOCK SIGNAL
IS WAVEFORM AS FIG. 3 ?
YES
REPAIR A15 ASSEMBLY
NO
MONITOR A15B(1̄8̄) DPLK CLK
IS WAVEFORM AS FIG.4 ?
NO
MONITOR A15-TP 7 SINGLE PULSE
IS WAVEFORM AS FIG. 5 ?
REPAIR A15 TIMING CIRCUITS
YES
CHECK DPLK CLK SIGNAL, GENERATED ON A15. RECOMMEND ASM TESTER OR HP 1601. FOLLOW PROCEDURE FIG. 5-6 OR 5-7
YES
MONITOR A15B(6̄) DPLK ← -1 & A15B(1̄7̄) DPLK ← DPLK-PI
ARE BOTH OUTPUTS ≥2.4V ?
NO
CHECK DPLK ← -1 & DPLK ← DPLK-PI SIGNALS GENERATED ON A15. RECOMMEND ASM TESTER OR HP 1601. FOLLOW PROCEDURE FIG.5-6 OR 7
YES
REPAIR A14 DPLK CIRCUITS
5345-D-21

Figure 5-2. Troubleshooting Flow Chart #1

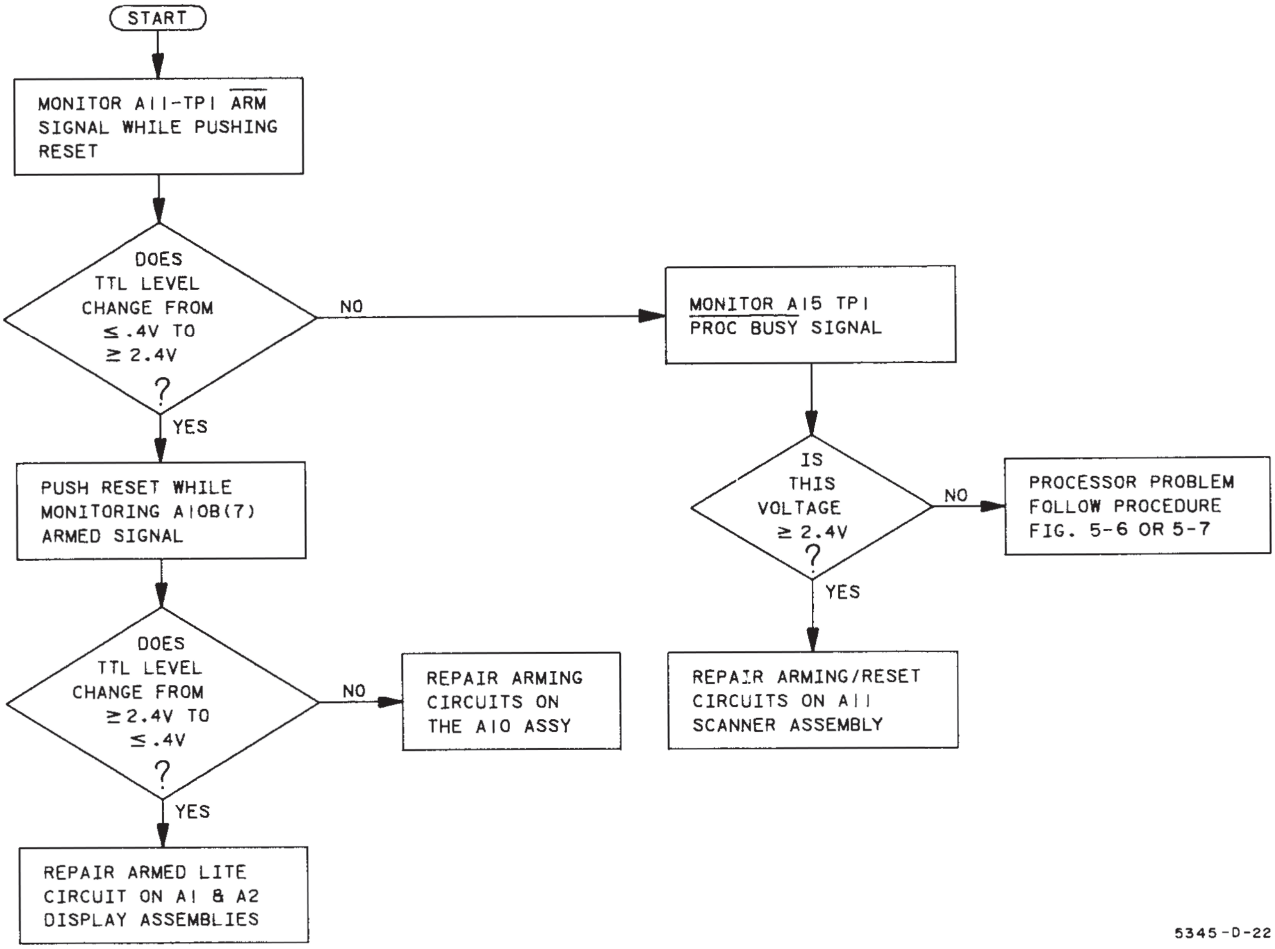
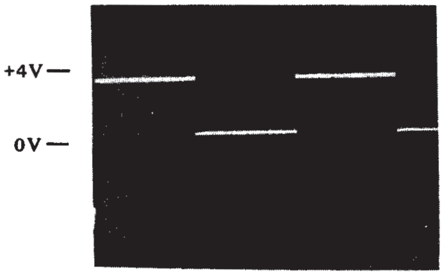

START
MONITOR A11-TP1 $\overline{\text{ARM}}$ SIGNAL WHILE PUSHING RESET
DOES TTL LEVEL CHANGE FROM ≤ .4V TO ≥ 2.4V ?
NO
YES
MONITOR A15 TP1 $\overline{\text{PROC BUSY}}$ SIGNAL
IS THIS VOLTAGE ≥ 2.4V ?
NO
YES
PROCESSOR PROBLEM FOLLOW PROCEDURE FIG. 5-6 OR 5-7
PUSH RESET WHILE MONITORING A10B(7) ARMED SIGNAL
DOES TTL LEVEL CHANGE FROM ≥ 2.4V TO ≤ .4V ?
NO
YES
REPAIR ARMING CIRCUITS ON THE A10 ASSY
REPAIR ARMING/RESET CIRCUITS ON A11 SCANNER ASSEMBLY
REPAIR ARMED LITE CIRCUIT ON A1 & A2 DISPLAY ASSEMBLIES
5345-D-22

Figure 5-3. Troubleshooting Flow Chart #2

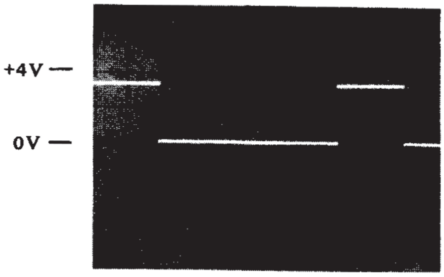
Equipment: 180A with 1801A/1821A and 100048 10:1 Probe

Figure 1. (REG CLK)



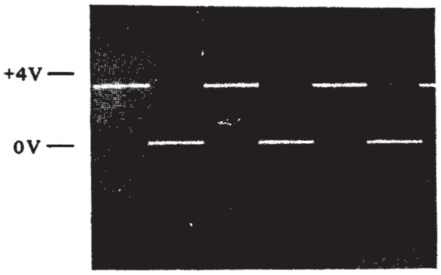
.2V/DIV, 20 μS/DIV,
+SLOPE, DC INPUT

Figure 2. (DRC D)



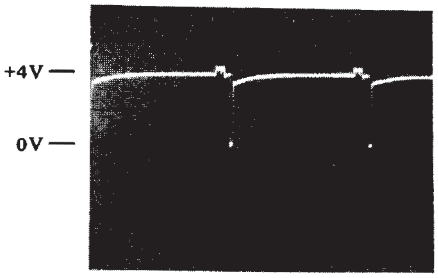
.2V/DIV, .1 mS/DIV,
+ SLOPE, DC INPUT

Figure 3. (DISP CLK)



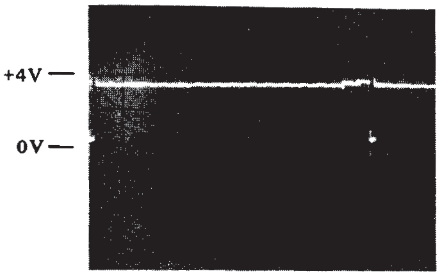
.2V/DIV, 20 μS/DIV,
+ SLOPE, DC INPUT

Figure 4. ($\overline{\text{DPLK CLK}}$)

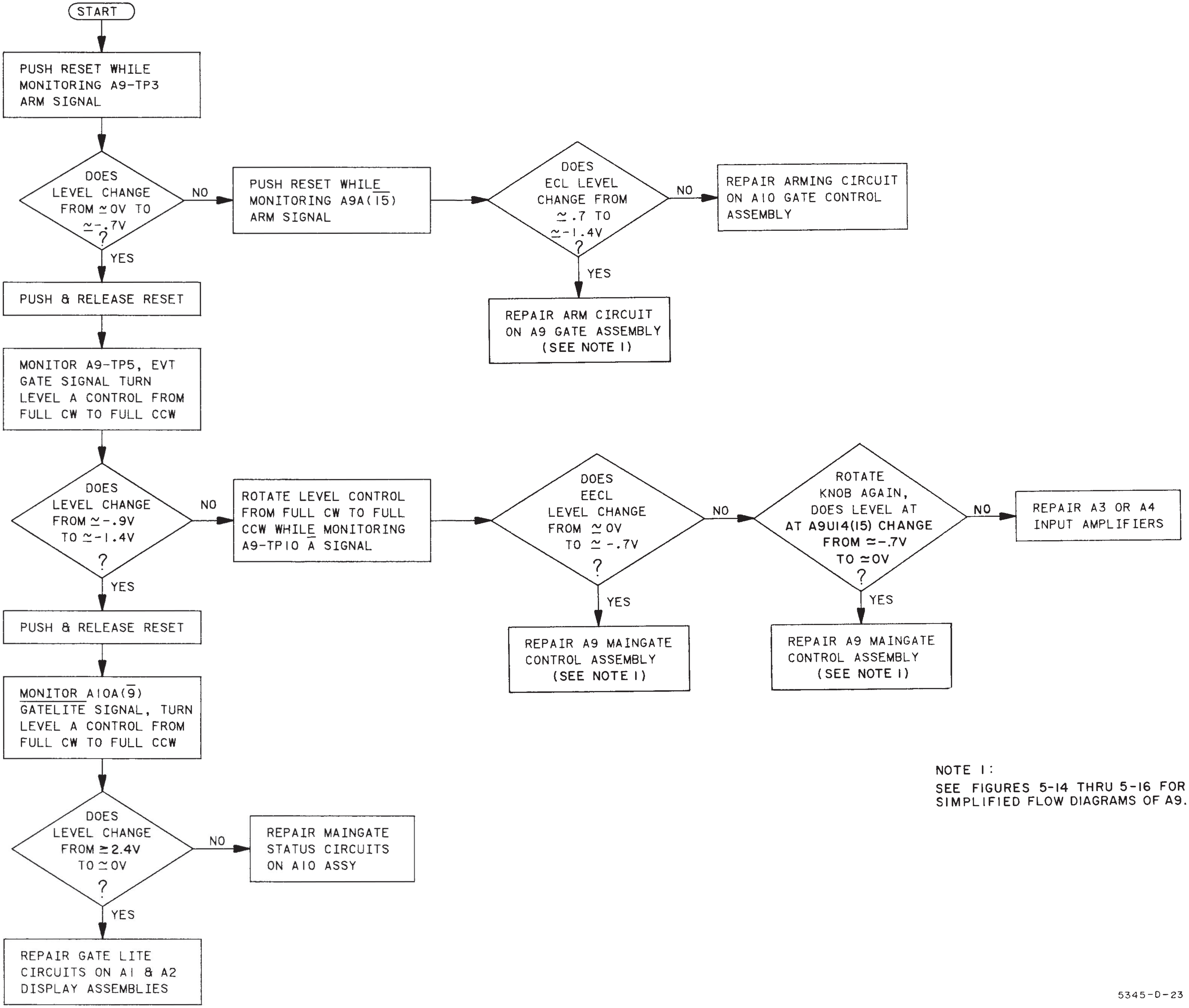


.2V/DIV, 2 μS/DIV,
- SLOPE, DC INPUT

Figure 5. ($\overline{\text{SINGLE PULSE}}$)

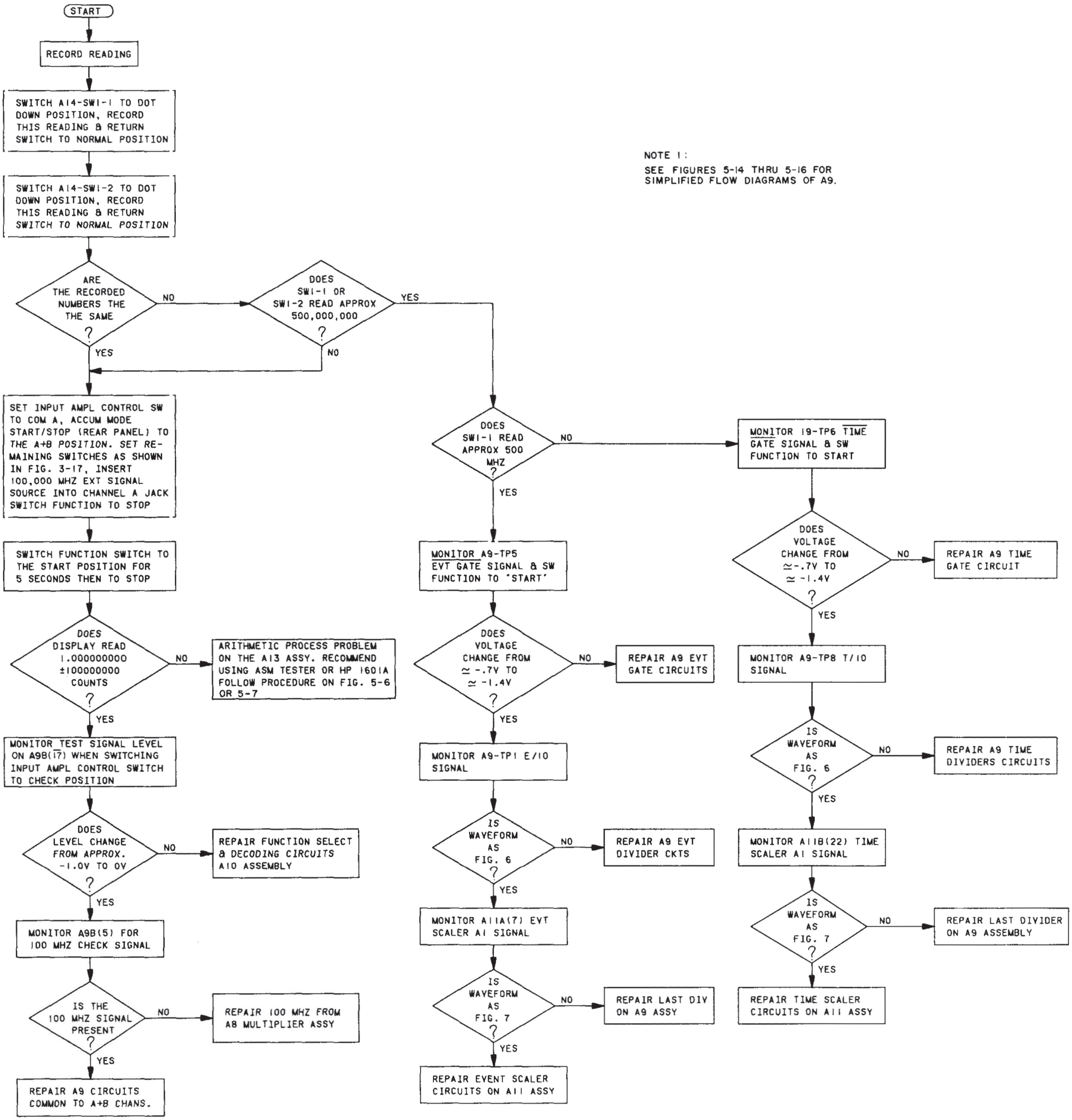


.2V/DIV, 1 μS/DIV,
- SLOPE, DC INPUT


START
PUSH RESET WHILE MONITORING A9-TP3 ARM SIGNAL
DOES LEVEL CHANGE FROM ≃0V TO ≃-.7V ?
NO
PUSH RESET WHILE MONITORING A9A(15) ARM SIGNAL
DOES ECL LEVEL CHANGE FROM ≃.7 TO ≃-1.4V ?
NO
REPAIR ARMING CIRCUIT ON A10 GATE CONTROL ASSEMBLY
YES
REPAIR ARM CIRCUIT ON A9 GATE ASSEMBLY (SEE NOTE 1)
YES
PUSH & RELEASE RESET
MONITOR A9-TP5, EVT GATE SIGNAL TURN LEVEL A CONTROL FROM FULL CW TO FULL CCW
DOES LEVEL CHANGE FROM ≃-.9V TO ≃-1.4V ?
NO
ROTATE LEVEL CONTROL FROM FULL CW TO FULL CCW WHILE MONITORING A9-TP10 A SIGNAL
DOES EECL LEVEL CHANGE FROM ≃0V TO ≃-.7V ?
NO
ROTATE KNOB AGAIN, DOES LEVEL AT AT A9U14(15) CHANGE FROM ≃-.7V TO ≃0V ?
NO
REPAIR A3 OR A4 INPUT AMPLIFIERS
YES
REPAIR A9 MAINGATE CONTROL ASSEMBLY (SEE NOTE 1)
YES
REPAIR A9 MAINGATE CONTROL ASSEMBLY (SEE NOTE 1)
YES
PUSH & RELEASE RESET
MONITOR A10A(9) GATELITE SIGNAL, TURN LEVEL A CONTROL FROM FULL CW TO FULL CCW
DOES LEVEL CHANGE FROM ≥2.4V TO ≃0V ?
NO
REPAIR MAINGATE STATUS CIRCUITS ON A10 ASSY
YES
REPAIR GATE LITE CIRCUITS ON A1 & A2 DISPLAY ASSEMBLIES
5345-D-23

NOTE 1:
SEE FIGURES 5-14 THRU 5-16 FOR SIMPLIFIED FLOW DIAGRAMS OF A9.

Figure 5-4. Troubleshooting Flow Chart #3

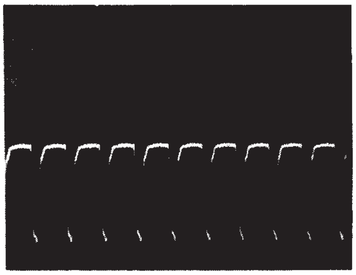

START
RECORD READING
SWITCH A14-SW1-1 TO DOT DOWN POSITION, RECORD THIS READING & RETURN SWITCH TO NORMAL POSITION
SWITCH A14-SW1-2 TO DOT DOWN POSITION, RECORD THIS READING & RETURN SWITCH TO NORMAL POSITION
ARE THE RECORDED NUMBERS THE SAME ?
NO
DOES SW1-1 OR SW1-2 READ APPROX 500,000,000 ?
YES
NO
YES
SET INPUT AMPL CONTROL SW TO COM A, ACCUM MODE START/STOP (REAR PANEL) TO THE A+B POSITION. SET REMAINING SWITCHES AS SHOWN IN FIG. 3-17, INSERT 100,000 MHZ EXT SIGNAL SOURCE INTO CHANNEL A JACK SWITCH FUNCTION TO STOP
SWITCH FUNCTION SWITCH TO THE START POSITION FOR 5 SECONDS THEN TO STOP
DOES DISPLAY READ 1.000000000 ±100000000 COUNTS ?
NO
ARITHMETIC PROCESS PROBLEM ON THE A13 ASSY. RECOMMEND USING ASM TESTER OR HP 1601A FOLLOW PROCEDURE ON FIG. 5-6 OR 5-7
YES
MONITOR TEST SIGNAL LEVEL ON A9B(17) WHEN SWITCHING INPUT AMPL CONTROL SWITCH TO CHECK POSITION
DOES LEVEL CHANGE FROM APPROX. -1.0V TO 0V ?
NO
REPAIR FUNCTION SELECT & DECODING CIRCUITS A10 ASSEMBLY
YES
MONITOR A9B(5) FOR 100 MHZ CHECK SIGNAL
IS THE 100 MHZ SIGNAL PRESENT ?
NO
REPAIR 100 MHZ FROM A8 MULTIPLIER ASSY
YES
REPAIR A9 CIRCUITS COMMON TO A+B CHANS.
DOES SW1-1 READ APPROX 500 MHZ ?
NO
MONITOR I9-TP6 TIME GATE SIGNAL & SW FUNCTION TO START
YES
MONITOR A9-TP5 EVT GATE SIGNAL & SW FUNCTION TO "START"
DOES VOLTAGE CHANGE FROM ≃ -.7V TO ≃ -1.4V ?
NO
REPAIR A9 EVT GATE CIRCUITS
YES
MONITOR A9-TP1 E/10 SIGNAL
IS WAVEFORM AS FIG. 6 ?
NO
REPAIR A9 EVT DIVIDER CKTS
YES
MONITOR A11A(7) EVT SCALER A1 SIGNAL
IS WAVEFORM AS FIG. 7 ?
NO
REPAIR LAST DIV ON A9 ASSY
YES
REPAIR EVENT SCALER CIRCUITS ON A11 ASSY
DOES VOLTAGE CHANGE FROM ≃-.7V TO ≃ -1.4V ?
NO
REPAIR A9 TIME GATE CIRCUIT
YES
MONITOR A9-TP8 T/10 SIGNAL
IS WAVEFORM AS FIG. 6 ?
NO
REPAIR A9 TIME DIVIDERS CIRCUITS
YES
MONITOR A11B(22) TIME SCALER A1 SIGNAL
IS WAVEFORM AS FIG. 7 ?
NO
REPAIR LAST DIVIDER ON A9 ASSEMBLY
YES
REPAIR TIME SCALER CIRCUITS ON A11 ASSY

NOTE 1:
SEE FIGURES 5-14 THRU 5-16 FOR SIMPLIFIED FLOW DIAGRAMS OF A9.

Figure 5-5. Troubleshooting Flow Chart #4

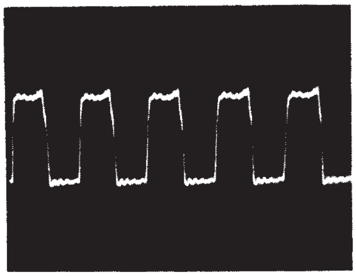
Equipment: 180A with 1801A/1821A and 100048 10:1 Probe

Figure 6.
(E/10 and T/10 Signal)

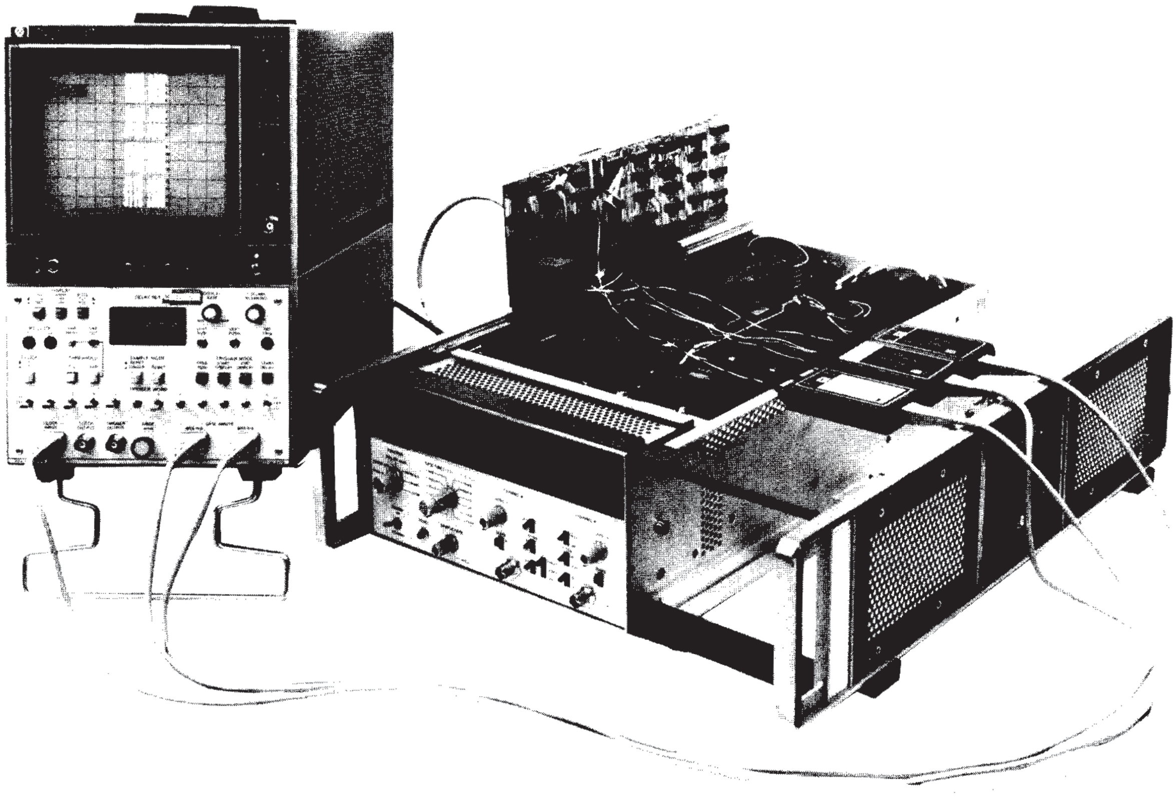


.02V/DIV, .1 μS/DIV,
+ SLOPE, DC INPUT

Figure 7.
(EVT SCLR and TIME SCLR A1)



.02V/DIV, .1 μS/DIV,
+ SLOPE, AC INPUT



EQUIPMENT REQUIRED:

A. 180 Oscilloscope.
B. 1601A Logic State Analyzer.

EQUIPMENT SETUP:

1. Remove 5345A Top Cover.
2. Place A15 on extender card (05345-60204 or 05345-60200).
3. Connect 10230A Clock Probe to A15 TP7 and common to A15 TP4.
4. Connect the 10231A Six Bit Probes to A15 as follows:

Bit 0 → U24(5)
Bit 1 → U24(6)
Bit 2 → U24(7)
Bit 3 → U24(4)
Bit 4 → U24(3)
Bit 5 → U24(2)
Bit 6 → U24(1)

Figure 5-6. Verifying Processor Flow With HP 1601A

EQUIPMENT SETTINGS:

5345A

FUNCTION	FREQ A
GATE TIME	100MS
Input Control	CHECK
SAMPLE RATE	HOLD

180/w 1601A

DISPLAY	PLUS, MARK-ON, BYTE BCD (this gives best pattern display)
CLOCK	POS
THRESHOLD	TTL
SAMPLE MODE	SINGLE
TRIGGER MODE	START DELAY
COLUMN BLANKING	To display seven bits
DISPLAY RATE	In single, it has no influence
TRIGGER WORD	Set to 570
	NOTE: Set all unused switches to OFF POSITION
DELAY SET	00000

OPERATING PROCEDURE:

1. Push SAMPLE MODE RESET button on the 1601A.
2. Push 5345A RESET.

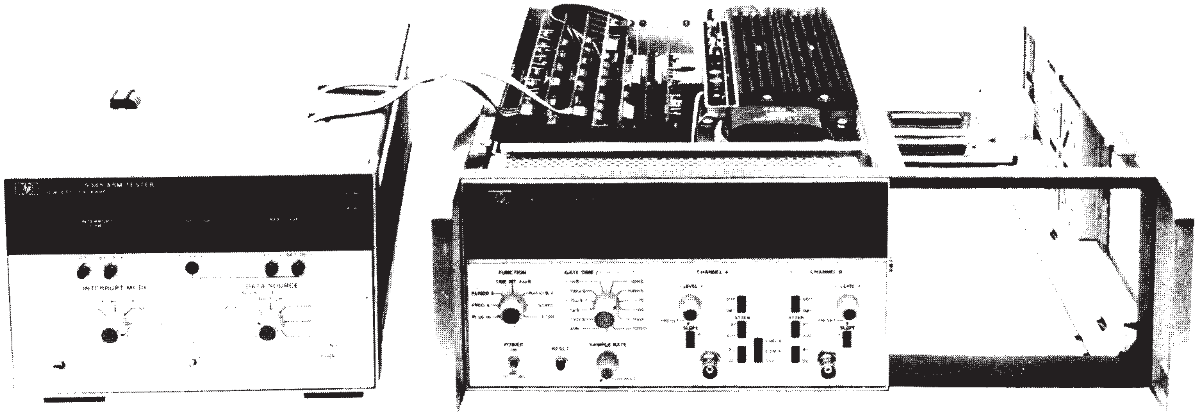
COMMENTS:

After the 5345A RESET is depressed and released, the ROM address of 570 should be displayed on the first word of the 1601A. $\begin{array}{ccc} 7654 & 321 & 0 \\ \underbrace{101}_{5} & \underbrace{111}_{7} & \underset{0}{0} \end{array}$

Table 5-3 shows the address which will be selected as the DELAY SET switch is incremented from the 570 trigger point. These addresses are correct only for the 5345A equipment settings above.

When verifying the selection of correct states, refer to *Processor Flow Test Results*, Table 5-3. ROM addresses can be quickly verified by setting the delay switches to mid points in the table. Any delayed states differing from those in the table indicate a failure. Also, all states *following* the incorrect state will usually differ from those in the table. When an incorrect state is found, refer to Figure 5-8, *Processor Symptoms and Troubleshooting*.

Figure 5-6. Verifying Processor Flow With HP 1601A (Continued)



EQUIPMENT REQUIRED:

1. K13-59992A 5345A ASM Tester.

EQUIPMENT SETUP:

1. Set 5345A POWER switch to STANDBY position.
2. Remove 5345A Top Cover.
3. Connect 5345A ASM Tester as follows:
   a. Test cable to A15 test socket J1. ((Note pin 1 placement.)
   b. Data cable to A13 test socket J1. (Note pin 1 placement.)

EQUIPMENT SETTINGS:

1. Set the 5345A the same as when using the HP 1601A.
2. Set the 5345A ASM Tester as follows:
   a. Switch the 5345A and ASM TESTER POWER switch to ON.
   b. Set the INTERRUPT MODE switch to the SEL STATE position.
   c. Set the SET 0-7 and SET 00-71 switches to 570 state address. The address will be displayed as the REF CODE.
   d. Set the INTERRUPT CTR to the number of times that the selected state is desired to match the REF CODE, before the 5345A is interrupted. The INTERRUPT CTR is normally set to 1.
   e. Push and HOLD RESET on the 5345A.
   f. Push and release CONTINUE. (Lamp test should be displayed on the 5345A and the TEST CODE will display state 001.)

Figure 5-7. Verifying Processor Flow With 5345A ASM Tester

g. Release RESET on the 5345A. The REF CODE and TEST CODE should now display the selected state address.

NOTE

> If there is a problem in the 5345A processor the TEST CODE may not be selected. In this case a new address should be tried. Check the PROCESSOR FLOW CHARTS to determine prior addresses.

h. Set INTERRUPT MODE switch to NEXT STATE.

OPERATING PROCEDURE:

Push CONTINUE. This will step the processor to the next ROM address, as listed in Table 5-3. This new address will be displayed as the Test Code. As CONTINUE is pushed, each sequential address that is listed in the table should be displayed as the Test Code. When an incorrect state is found, refer to Figure 5-8, *Processor Symptoms and Troubleshooting*.

NOTE

> The A13J1 connection enables the data to be monitored at selected states. For operating procedure, see *ASM TESTER* manual.

Figure 5-7. Verifying Processor Flow With 5345A ASM Tester (Continued)

Table 5-3. Processor Flow Test Results

Delay Switch	ROM Address	Processor Operation	Comment
00000	570	Initiate Processor	yes
00001	211	Computer dump	no
00002	151	PI Data	no
00003	361	Display TC	no
00004	440	DPLK=-17	no
00005	600	NR=0, 1st zero digit	yes
00006	440	DPLK=-17	no
00007	600	NR=0, 2nd zero digit	yes
00008	440	DPLK=-17	no
00009	600	NR=0, 3rd zero digit	yes
00010	440	DPLK=-17	no
00011	600	NR=0, 4th zero digit	yes
00012	440	DPLK=-17	no
00013	600	NR=0, 5th zero digit	yes
00014	440	DPLK=-17	no
00015	600	NR=0, 6th zero digit	yes
00016	440	DPLK=-17	no
00017	600	NR=0, 7th zero digit	yes
00018	440	DPLK=-17	no
00019	600	NR=0, 8th zero digit	yes
00020	440	DPLK=-17	no
00021	601	NR=$\overline{0}$, 1st nonzero digit	no
00022	400	Prepare to count 1st digit	yes
00023	440	DPLK=-17	no
00024	601	NR=$\overline{0}$, 2nd nonzero digit	no
00025	400	Prepare to count 2nd digit	yes
00026	440	DPLK=-17	no
00027	601	NR=$\overline{0}$, 3rd nonzero digit	no
00028	400	Prepare to count 3rd digit	yes
00029	440	DPLK=-17	no
00030	601	NR=$\overline{0}$, 4th nonzero digit	no
00031	400	Prepare to count 4th digit	yes
00032	440	DPLK=-17	no
00033	601	NR=$\overline{0}$, 5th nonzero digit	no
00034	400	Prepare to count 5th digit	yes
00035	440	DPLK=-17	no
00036	601	NR=$\overline{0}$, 6th nonzero digit	no
00037	400	Prepare to count 6th digit	yes
00038	440	DPLK=-17	no

Table 5-3. Processor Flow Test Results (Continued)

Delay Switch	ROM Address	Processor Operation	Comment
00039	601	NR=$\overline{0}$, 7th nonzero digit	no
00040	400	Prepare to count 7th digit	yes
00041	440	DPLK=-17	no
00042	601	NR=$\overline{0}$, 8th nonzero digit	no
00043	400	Prepare to count 8th digit	yes
00044	441	DPLK=-17	yes
00045	221	Period or TI	no
00046	451.	Flag = H	yes
00047	051	Plug-in	no
00048	420	Events, Ratio and Start or Stop	no
00049	530	Period or TI	no
00050	341	Display Time Count	no
00051	201	Start or Stop	no
00052	071	N Data	no
00053	671	Divide Routine	
00054	030	Divide Routine	
00055	310	Divide Routine	
00056	460	Divide Routine	MSB = 1
00057	540	Divide Routine	
00058	671	Divide Routine	
00059	031	Divide Routine	
00060	671	Divide Routine	
00061	030	Divide Routine	
00062	311	Divide Routine	
00063	460	Divide Routine	1st Remainder
00064	540	Divide Routine	
00065	671	Divide Routine	
00066	030	Divide Routine	
00067	311	Divide Routine	
00068	460	Divide Routine	2nd Remainder
00069	540	Divide Routine	
00070	671	Divide Routine	
00071	030	Divide Routine	
00072	311	Divide Routine	
00073	460	Divide Routine	3rd Remainder
00074	540	Divide Routine	
00075	671	Divide Routine	
00076	030	Divide Routine	
00077	311	Divide Routine	
00078	460	Divide Routine	4th Remainder
00079	540	Divide Routine	
00080	671	Divide Routine	
00081	030	Divide Routine	
00082	311	Divide Routine	

Table 5-3. Processor Flow Test Results (Continued)

Delay Switch	ROM Address	Processor Operation	Comment
00083	460	Divide Routine	5th Remainder
00084	540	Divide Routine	
00085	671	Divide Routine	
00086	030	Divide Routine	
00087	311	Divide Routine	
00088	460	Divide Routine	6th Remainder
00089	540	Divide Routine	
00090	671	Divide Routine	
00091	030	Divide Routine	
00092	311	Divide Routine	
00093	460	Divide Routine	7th Remainder
00094	540	Divide Routine	
00095	671	Divide Routine	
00096	030	Divide Routine	
00097	311	End Divide Routine	
00098	461	FLAG=H, LOAD RESULT to QR	yes
00099	121	K Data	no
00100	520	Start and Stop	no
00101	551		
00102	440	States 440 through 441 are repeated for a second time after the arithmetic routine. The purpose of the processor operations will vary during these operations. Consult flow chart theory 2A (440), if needed.	
00103	600		
00104	440		
00105	600		
00106	440		
00107	600		
00108	440		
00109	600		
00110	440		
00111	600		
00112	440		
00113	600		
00114	440		
00115	600		
00116	440		
00117	600		
00118	440		
00119	601		
00120	400		
00121	440		
00122	601		
00123	400		

Table 5-3. Processor Flow Test Results (Continued)

Delay Switch	ROM Address	Processor Operation	Comment
00124	440	Continued	
00125	601		
00126	400		
00127	440		
00128	601		
00129	400		
00130	440		
00131	601		
00132	400		
00133	440		
00134	601		
00135	400		
00136	440		
00137	601		
00138	400		
00139	440		
00140	601		
00141	400	↓	
00142	441	End of Count digits	
00143	221	Period or TI	no
00144	450	FLAG = H	no
00145	561	Display Storage	no
00146	510	DC = 0	no
00147	500	Determine Auto Multiplier	
00148	270	Determine Auto Multiplier	
00149	711	Determine Auto Multiplier	
00150	741	Determine Auto Multiplier	
00151	770	Determine Auto Multiplier	
00152	741	Determine Auto Multiplier	
00153	770	Determine Auto Multiplier	
00154	741	Determine Auto Multiplier	
00155	770	Determine Auto Multiplier	
00156	740	Determine Auto Multiplier	
00157	500	Determine Auto Multiplier	
00158	270	Determine Auto Multiplier	
00159	710	-1≥ DPLR-DS≥3	Mult. Selected
00160	640	Left justify result	
00161	651	Left justify result	
00162	660	Left justify result	

Table 5-3. Processor Flow Test Results (Continued)

Delay Switch	ROM Address	Processor Operation	Comment
00163	640	Left justify result	
00164	651	Left justify result	
00165	660	Left justify result	
00166	640	Left justity result	
00167	651	Left justify result	
00168	660	Left justify result	
00169	640	Left justify result	
00170	651	Left justify result	
00171	660	Left justify result	
00172	640	Left justify result	
00173	651	Left justify result	
00174	660	Left justify result	
00175	640	Left justify result	
00176	651	Left justify result	
00177	660	Left justify result	
00178	640	Left justify result	
00179	651	Left justify result	
00180	660	Left justify result	
00181	640	Left justify result	
00182	651	Left justify result	
00183	660	Left justify result	
00184	640	Left justify result	
00185	650	Left justify result	
00186	621	End of left justify	
00187	260	Auto Right justify	
00188	610	Auto Right justify	
00189	011	Auto Right justify	
00190	621	Auto Right justify	
00191	260	Auto Right justify	
00192	610	Auto Right justify	
00193	011	Auto Right justify	
00194	621	Auto Right justify	
00195	260	Auto Right justify	
00196	610	Auto Right justify	
00197	011	Auto Right justify	
00198	621	Auto Right justify	
00199	260	Auto Right justify	
00200	610	Auto Right justify	
00201	011	Auto Right justify	

Table 5-3. Processor Flow Test Results (Continued)

Delay Switch	ROM Address	Processor Operation	Comment
00202	621	Auto Right justify	
00203	260	Auto Right justify	
00204	610	Auto Right justify	
00205	011	Auto Right justify	
00206	621	Auto Right justify	
00207	260	Auto Right justify	
00208	610	Auto Right justify	
00209	011	Auto Right justify	
00210	621	Auto Right justify	
00211	260	Auto Right justify	
00212	610	Auto Right justify	
00213	011	Auto Right justify	
00214	621	Auto Right justify	
00215	260	Auto Right justify	
00216	610	Auto Right justify	
00217	011	Auto Right justify	
00218	620	Auto Right justify	
00219	731	Serial Output	no
00220	571	End of Test	

PROCESSOR SYMPTOMS AND TROUBLESHOOTING

A. The state address is off by one count in the LSD; e.g., Address 450 may be selected instead of 451.

B. The state address is off by several addresses; e.g., Address 440 follows 211 instead of 151.

HP 1601A EQUIPMENT SETUP

When using the HP 1601A Logic State analyzer, the equipment should be set up as shown in Figure 5-6. The additional Probe Bits can be used to monitor any of the commands or DC levels which make up the qualifiers. Note that many of these commands are active low outputs and will be displayed on the 1601A as zeros.

5345A ASM TESTER SETUP AND OPERATING PROCEDURE

When using the ASM Tester, the equipment should be set up as shown in Figure 5-7.

For checking output command states, the ASM Tester should be operated as follows:

1. Set the REF CODE to the last correct state.
2. Set the INTERRUPT MODE switch to SEL STATE.
3. Push CONTINUE. (Ref and test codes should now equal.)
4. Set the INTERRUPT MODE switch to NEXT STATE.
5. Using the 10525A Logic Probe, monitor the desired command.
6. Push CONTINUE. Note: When CONTINUE is pushed, the logic probe will display the active state of the selected command.

PROCESSOR PROBLEM A

mptom A is the result of a qualifier problem. Several things can cause this to occur.

1. Incorrect ROM command generation.
2. Associated circuits of the qualifier.
3. Defective circuits within the process arithmetic section.

TROUBLESHOOTING METHOD FOR A TYPE PROBLEMS

roubleshooting for A type problems should be done in the following manner.

1. First, locate the defective state on the flow charts. Refer to the command listings in Table 5-4. Find the letter code adjacent to the defective ROM address. Then, locate this letter code on the flow charts.
2. Determine which qualifier or part of the qualifier is responsible for selecting the *correct* ROM state. The particular qualifier may be obvious in some cases; however, familiarization with the flow charts will be required for detecting others. See flow chart theory.
3. Using the octal MSB digits of the defective state, locate the A14 qualifier switch and verify the proper closure of the switch. Must set TRIGGER WORD on 1601 to last correct state address while checking for proper switch closure. Refer to the A14 theory for a description of qualifier selection.
4. If the switch is operating properly, trace the qualifier signal back to its source. If it is a multiple qualifier, verify that the remaining qualifiers are inactive.
5. When the source of the qualifier has been identified, check previous ROM states in the flow charts and determine which ROM address executed the command or commands to satisfy the qualifier.
6. Monitor this new address and check the commands to ensure they are generated. If the commands are found to be defective, troubleshoot and repair the circuits. Some qualifiers will be generated by the result of a counter, comparator, or adder. For these qualifiers, the input commands should be checked first. If these commands are correct, the appropriate circuits should then be checked. An example of this type of qualifier is DRLK = -17. The input commands to this qualifier are DPLK ← -1 (Reset) and DPLK CLK (DPLK ← DPLK -1).

PROCESSOR PROBLEM B

The problem which caused symptom B will generally be a defective ROM or the next-state storage circuits (T+1) on the A14 qualifier assembly.

TROUBLESHOOTING METHOD FOR B TYPE PROBLEMS

NOTE

Connect 10230A Clock Probe to A15TP12 while monitoring SV1(T+1) -SV6(T+1).

Troubleshooting this problem should be done as follows:

1. Locate the defective state on the flow charts. Refer to the command listing table. Find the letter code adjacent to the defective ROM address. Then locate the letter code on the flow chart.
2. With the ASM Tester, step the processor to the last correct address. Use the operating procedure outlined in Figure 5-7. With the HP 1601A, trigger on the last correct address.
3. While at this address, check SV1(T+1) - SV6(T+1) states, located at pins 2, 7, 5, 10, 12, and 15, respectively, on the A14 Qualifier Assembly. Pins 2, 7, and 5 equal the Octal MSB, and pins 10, 12, and 15 equal the next MSB.
4. The output levels of these pins should reflect the octal address of the next state to be selected. If it is incorrect, tract the line back to its source and troubleshoot those circuits.

Figure 5-8. Processor Symptoms and Troubleshooting

Table 5-4. Command Source Listing

COMMAND SOURCE		A15-U10-6	A15-U10-3	A15-TP1	A15-U15-5	A15-$\overline{\text{A11}}$	A15-U35-2	A15-U35-14	A15-$\overline{\text{B9}}$	A15-$\overline{\text{B18}}$	A15-$\overline{\text{B17}}$	A15-$\overline{\text{B6}}$	A15-$\overline{\text{B15}}$	A15-B7	A15-B16	A15-A12	A15-$\overline{\text{A22}}$	A15-B21	A15-$\overline{\text{A8}}$	A15-$\overline{\text{A9}}$	A15-U34-4	A15-A9	A15-U2-5	A15-U2-1	A15-B5	A15-U25-11	A15-A12	A15-$\overline{\text{A7}}$	A15-$\overline{\text{B10}}$	A15-B8	A15-$\overline{\text{A6}}$	A14-$\overline{\text{A12}}$	A15-B10	A15-A21	A15-$\overline{\text{A15}}$	A15-A14	A15-A15	A15-$\overline{\text{A20}}$	A15-U10-9	A15-U10-13	A14-U23-2	A14-U23-7	A14-U23-5	A14-U23-10	A14-U23-12	A14-U23-15	A15-$\overline{\text{A10}}$	A15-U12-2
MSB		0	0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	1	1	1	1	1	1	0	0
PULSED COMMAND		P	P				P	P		P	P	P	P		P	P							P	P	P	P										P	P		P	P								P
LETTER CODES	COMMAND ADDRESSES	$\overline{*\leftarrow\text{ON}}$	$\overline{*\leftarrow\text{OFF}}$	$\overline{\text{1 PULSE CNT.}}$	15 PULSE CNT.	ADD	DC←0	DC CLK	DISP CLK EN	$\overline{\text{DPLK CLK}}$	$\overline{\text{DPLK}\leftarrow\text{DPLK-PI}}$	$\overline{\text{DPLK}\leftarrow -1}$	$\overline{\text{DPLR CLK}}$	$\overline{\text{DPLR UP}}$	$\overline{\text{DPLR}\leftarrow -1}$	$\overline{\text{DRC}\leftarrow 0}$	DR CLK EN	DR EN A	DR EN B	DR EN C	DS←DC	$\overline{\text{EXT OUT EN}}$	$\overline{\text{FLAG}\leftarrow\text{H}}$	$\overline{\text{FLAG}\leftarrow\text{L}}$	$\overline{\text{LOAD MS}}$	$\overline{\text{LOAD • STORAGE}}$	NR CLK EN	NR EN A	NR EN B	$\overline{\text{PROC BUSY}}$	$\overline{\text{PI CLK EN}}$	$\overline{\text{QR EN A/PI XMT}}$	QR EN B	QR EN C	QR EN CLK	$\overline{\text{QMC}\leftarrow 0}$	$\overline{\text{QMC CLK}}$	RST FRONT END	$\overline{\text{SIGN}\leftarrow -}$	$\overline{\text{SIGN}\leftarrow +}$	SV1 (T+1)	SV2 (T+1)	SV3 (T+1)	SV4 (T+1)	SV5 (T+1)	SV6 (T+1)	FLAG=H	$\overline{\text{RST PULSE CNT}}$
SHT 3P	000	H	H	H	L	H	H	L	L	H	H	H	H		H	H	H	H	L	H	H	H	H	H	H	H	H	L	H	L	H	H	L	H	H	H	H	L	H	H	H	L	H	H	L	H	L	H
RESET	001	H	H	L	L	H	H	L	H	L	H	H	H	H	L	H	H	L	H	L	L	H	L	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	L	H	L	L	L	H	L
SHT 2BB	010	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	L	H	L	H	H	H	H	H	H	H	H	L	L	H	L	H	H
SHT 2BB	011	H	H	L	H	H	L	L	L	L	H	H	H		H	H	L	H	L	L	L	H	H	H	H	H	H	L	H	L	H	L	L	H	H	H	H	H	H	H	H	H	L	L	H	L	H	H
SHT 3B	020	H	H	H	L	H	L	L	L	L	H	H	H	L	H	H	H	L	L	H	L	H	L	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H	L	L	L	H	H	H	H	H
SHT 3B	021	H	H	H	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H	L	H	H	L	H	H	H	L	L	L	L	L	L	H	L	H	H	L	H	H	L	L	L	H	H	H	L	H
SHT 3D	030	H	H	H	L	H	L	L	L	H	H	H	L	*	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L	L	H	H	L	L	L	H	H	L	H	H	L	H	H	L	L	H	*	H
SHT 3D	031	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	L	L	H	H	L	H	L	L	L	H	*	H
SHT 4J	040	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	L	H	H	H	H	L	L	H	H	H	L	H	H	L	H	H	L	H	H	L	L	L	H	L	L	H	H
SHT 4J	041	H	H	L	H	H	L	H	L	H	H	L	H	H	H	H	L	L	L	L	L	L	H	L	H	H	L	L	H	H	H	H	H	H	L	H	H	L	H	H	H	H	H	H	H	L	L	H
SHT 2F	050	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	L	H	L	L	H	H	H	H	H	H	L	H	L	H	L	H	L	H	H	H	L	H	H	H	H	L	H	H	H	H	H
SHT 2F	051	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	H	L	H	L	H	H	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	L	H	L	L	L	H	L	H	H
SHT 4H	060	H	H	L	H	H	L	L	L	H	H	L	H	H	H	H	L	L	L	L	L	L	H	L	H	H	L	L	H	H	H	L	H	H	L	H	H	L	H	H	L	L	L	H	H	L	L	H
SHT 4H	061	H	H	L	H	H	L	L	L	H	H	L	H	H	H	H	L	L	L	L	L	L	L	H	H	H	L	L	H	H	H	L	H	H	L	H	H	L	H	H	L	L	L	H	L	L	H	H
SHT 3A	070	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	L	L	H	H	L	L	L	L	H	L	*	H
SHT 3A	071	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	L	H	L	L	H	H	H	H	H	H	L	H	L	H	L	H	L	H	L	H	L	H	H	H	H	L	H	H	H	*	H
SHT 3K	100	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	L	L	H	H	H	L	H
SHT 1A	101	H	H	H	L	H	L	L	L	H	H	H	L	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	L	H	H	H	L	H	H	H	H
SHT 4F	110	H	H	L	L	H	L	L	L	H	H	H	H		L	H	L	L	L	L	L	L	H	H	H	H	L	H	L	H	H	H	H	H	L	H	H	L	H	H	L	H	H	H	L	H	H	H
SHT 4F	111	H	H	H	H	H	L	L	L	L	H	H	L	L	H	H	H	L	H	L	L	L	H	H	H	H	L	L	H	H	H	H	H	H	L	H	H	L	H	H	L	H	H	H	L	H	H	H
SHT 3G	120	H	H	H	L	H	L	L	L	H	H	H	L	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	L	H	L	L	H	H	H	H	L	H	L	H	L	L	H	L	H	L	H
SHT 3G	121	H	H	H	L	H	L	H	L	H	H	L	H		H	H	H	L	L	H	L	H	H	L	H	H	H	L	H	L	H	H	H	H	H	H	H	L	H	H	H	L	H	L	H	L	L	H
SHT 3N	130	H	H	H	L	H	L	L	L	H	H	H	H		H	H	H	L	H	L	L	H	H	H	H	H	H	H	L	L	H	L	H	H	L	H	H	L	L	H	H	L	L	H	H	H	L	H
SHT 3N	131	H	H	L	H	H	L	L	L	H	H	H	H		H	L	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	L	L	L	L	L	L	H
SHT 4E	140	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	L	L	H	H
SHT 4E	141	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	L	L	H	H	H
SHT 1H	150	H	H	H	L	H	L	L	L	H	L	H	H		H	H	H	H	H	H	L	H	H	H	H	H	H	H	L	L	L	L	H	H	L	H	H	L	H	L	L	H	L	L	H	H	L	H
SHT 1H	151	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	H	L	H	L	H	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	L	H	L	L	H	H	H	H	L	H	H
SHT 4D	160	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	H	L	L	H
SHT 4D	161	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	L	L	H	H
SHT 1L	170	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	H	H	H	L	H	L	H	H	H	H	L	L	L	L	L	L	H	L	H	H	L	H	H	H	L	L	H	L	L	H	H
SHT 1L	171	H	H	L	H	H	L	H	L	H	H	L	L	L	H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	H	H	H	L	H	H	L	H	H	H	L	H	L	H	L	L	H
SHT 2K	200	H	H	L	H	H	L	H	L	H	H	L	L	L	H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	L	L	H	H	H	H	H
SHT 2K	201	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	L	L	H	H	H	H	H
SHT 1D	210	H	L	H	L	H	L	L	L	H	H	H	H		H	H	H	L	H	H	L	H	H	L	H	H	H	H	H	L	H	L	H	H	H	H	H	L	H	H	L	H	H	L	L	L	L	H
SHT 1D	211	H	L	H	L	H	L	L	L	H	H	H	H		H	H	H	H	H	L	L	H	H	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	L	H	H	L	H	L	H
SHT 2D	220	H	L	L	H	H	L	H	L	H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	L	L	H	L	H	H	H
SHT 2D	221	H	L	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	L	L	H	L	H	L	H
SHT 1K	230	H	L	L	H	H	L	L	L	H	H	L	L	H	H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	H	H	H	L	L	H	L	H	H	L	L	H	H	H	H	L	H
SHT 1K	231	H	L	H	H	H	L	L	L	H	H	H	L	L	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	L	H	H	L	H	H	L	H	H	L	H	L	L	H	H	L	H
SHT 2M	240	H	L	H	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	L	H
SHT 2M	241	H	L	H	H	H	L	L	L	H	H	H	L	L	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	L	H	H	L	H	H	H	H	H	L	H	L	H	L	L	L	H
SHT 3J	250	H	L	L	H	H	L	L	L	L	H	H	H		H	H	H	L	H	H	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	L	L	H	L	L	L	L	H
SHT 3J	251	H	L	L	H	H	L	L	L	H	H	H	L	H	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	L	H	H	L	H	H	L	L	H	L	L	L	L	H
SHT 2Z	260	H	L	L	H	H	L	L	L	H	H	L	L	H	H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	L	L	L	H	H	H
SHT 2Z	261	H	L	H	H	H	L	L	L	H	H	H	L	L	H	H	L	H	L	L	L	H	H	H	H	H	L	L	H	L	H	L	L	H	L	H	H	H	H	H	H	H	L	L	H	L	H	H
SHT 2R	270	H	L	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	H	H	H	L	L	H	H	H
SHT 2R	271	H	L	H	H	H	L	H	L	H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	H	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	L	H	H	H	H	H
SHT 1D$_1$	300	H	H	H	L	H	L	L	L	H	H	L	H		H	H	L	H	L	H	L	H	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	L	L	H	H	L	H	L	L	H
SHT 1D$_1$	301	H	H	H	L	H	L	L	L	H	H	L	H		L	H	L	H	L	L	L	L	H	H	H	H	L	L	H	L	H	H	L	H	H	H	H	L	H	H	H	H	H	L	L	L	L	H
SHT 3E	310	H	H	L	H	H	L	L	L	L	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	L	H	L	L	H	H	L	*	H
SHT 3E	311	H	H	H	H	H	L	H	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	L	H	L	H	H	H	L	L	H	H	L	*	H
SHT 1D$_2$	320	H	H	L	L	H	L	L	L	H	H	L	H	H	L	H	L	H	L	L	L	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	L	H	H	H	H	L	H
SHT 1D$_2$	321	H	H	L	L	H	L	L	L	H	H	L	H	H	L	H	L	H	L	L	L	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	L	H	H	H	H	L	H
SHT 1G	330	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	H	L	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
SHT 1G	331	H	H	L	H	H	L	L	L	H	H	H	H		H	H	H	H	L	H	H	L	H	L	H	H	H	L	H	L	H	H	L	H	L	H	H	L	H	H	H	H	H	L	L	L	L	H
SHT 3R	340	H	H	L	H	H	L	L	H	L	H	H	H		H	H	H	L	H	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	L	L	H	H	L	H	H	H	L	L	*	H
SHT 3R	341	H	H	L	H	H	L	L	L	H	H	L	H		H	L	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	L	H	L	H	H	H	L	L	H	L	L	*	H
SHT 4G	350	H	H	L	H	H	L	H	L	H	H	L	L	L	H	H	L	L	L	L	L	L	H	H	H	H	L	L	H	H	H	L	H	H	L	H	H	L	H	H	L	L	L	H	H	L	H	H
SHT 4G	351	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	H	L	L	H
SHT 1J	360	H	H	L	H	H	L	L	H	L	H	H	L	H	H	H	H	L	H	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	H	H	L	H	H
SHT 1J	361	H	H	L	L	H	L	L	L	H	H	L	H		L	L	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	H	L	H	L	H	H	H	L	L	H	L	L	H	H
SHT 4C	370	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H
SHT 4C	371	H	H	L	H	H	L	H	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	H	L	L	H

NOTE:
* NORMALLY H, L WITH "N" DATA ROUTINE.
BLANK LOCATIONS = DON'T CARE STATES.
BOLD LETTERS = ACTIVE STATES.

Table 5-4. Command Source Listing (Continued)

COMMAND SOURCE		[illegible]	A15 U10 3	A15 TP1	[illegible]	[illegible]	A15 U35 2	A15 U35 4	A B9	A B7	A15 B1	A15 B6	A B1	A15 B	A15 B16	A15 A	A15 A	A15 B	A15 A8	A15 A9	A U 4 4	A15 A	A15 U	A15 U 1	A1 R	A15 11	A15 A1	A15 A7	A15 B1	A15 B8	A15 A6	A14 A12	A B1	A15 A	A15-A15	A15 A14	A15 A 5	A15 A2	A15 U10 9	A15 U10 13	A14 [illegible]	A14 U3	A14 U23 5	A14 U23-10	A 4 U 3 1	A15 15	A15 A10	A15 U12 2
MSB		0	0	0	1	1	0	1	1	1	0	1	0	0	0	0	1		0	1	1	1	0	0	1	0	0	0	0	1	1	1		1	1	0	1		0	0			1	1			0	0
PULSED COMMANDS		P	P				P	P		P	P	P	P		P	P							P	P	P											P	P		P	P								P
LETTER CODES	ADDRESSES	*-ON	*-OFF	1 PULSE CNT	1⁄5 PULSE CNT	ADD	DC-Ø	DC CLK	DISP CLK EN	DP K CLK	DPLK DPLK P	DPLK 1	DPLR CLK	DPLR UP	DPLR ÷1	DRC-Ø	DR CLK EN	DR EN A	DR EN B	DR EN C	DS DC	EXT OUT EN	FLAG-H	FLAG L	LOAD MS	OMD * S ORACE	NR CLK EN	NR EN A	NR EN B	PROC BUSY	PI CLK EN	QR EN A PI XMT	QR EN B	QR EN C	QR EN CLK	QMC-Ø	QMC CLK	RST FRONT END	SIGN--	SIGN-+	SV 1-1	SV2 1-1	SV3 (1-1)	SV4 (1-1)	SV5 1-1	SV6	FLAG H	RST PULSE CNT
SHT 2C	400	H	H	L	H	H	L	H	L	H	H	H	H		H	H		L	L	L	H	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	L	L	H	H	H	L	L	H	L	L	*	H
SHT 2C	401	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L		L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	L	L	H	H	H	L	L	H	L	L	H	H
SHT 2Q	410	H	H	L	H	H	L	L		H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	L	H	H	L	H	H		H	H	H	H	L	H			H	H
SHT 2Q	411	H	H	H	H	H	L	L	L	H	H	H	H		H	H	L		L	L	H	H	H	H	L	H	H	H	H	L	H	L	H	H	L	H	H		H	H	H	H	L	H	L	L	H	H
SHT 2C	420	H	H	H	L	H	L	L		H	H	H	H		H	H	H	L	H	H	L	H	H	H	H	H	H	H	L	L	H	H	H	H	L	H	H	L	H	H	H	L	H	L	H	H	*	H
SHT 2G	421	H	H	H	L	H	L	L	L	H	H	H	H		H	H	H		H	H	L	H	H	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H		H	L	L	L	L	*	H
SHT 3M	430	H	H	H	L	L	L	L		H	H	H	H		H	H	H	L	H	L		H	H	H	H	H	H	H	L	L	H	H	H	H	L	H	H	L	H	H	L		H	L	H	H	L	H
SHT 3M	431	H	H	H	L	H	L	L	L	H	H	H	H		H	H	H		H	L	L	H	H	H	H	H	H	H		L	H	H	H	H	L	H	H	L	H	H		L	H	L	H	H	L	H
SHT 2A	440	H	H	H	H	H	L	L	L	L	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	L	L	L	L	*	H
SHT 2A	441	H	H	L	H	H	L	L	L	H	H	H	H		H	H		L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	L	H	L	H	H	L	H	L	L	H	L	*	H
SHT 2E	450	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	H	L	H	H	H	L	L	H
SHT 2F	451	H	H	L	H	H	H	L	L	H	H	H	H		H	H		L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L		L	H	L	H	*	H
SHT 3F	460	H	H	H	H	H	L	L	H	L	H	H	H		H	H	L		L	L	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	H	L	H	L	H	L	H	H	L	L	*	H
SHT 3F	461	H	H	L	L	H	H	L	H	H	H	L	H		H	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H	L	H	H	L	L	H	L	H		*	H
SHT 3L	470	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	H	H	H	L	H	H	L	L	H	L	H	L	H	H	L	H	H		H	H	L	H	L	H		H	L	H
SHT 3L	471	H	H	H	L	H	L	L	L	H	H	H	H		H	H	H	H	L	H	H	H	H	L	H	H	H	L		L	H	L		H	L	H	H	L	H	H	H	L	L	L	H	H	L	H
SHT 2P	500	H	H	L	H	H	L	L	L	H	H	L	H		H	H		L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	L	H	H	H	H	H
SHT 2P	501	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	L	L	L	L	H	H	H
SHT 2N	510	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	L	H	H	L	H	H	H	L	H	L	L	L	H	H
SHT 2N	511	H	H	L	L	H	L	L	L	H	H	H	H		L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	L	L	H	L	L	L	H	H
SHT 3H	520	H	H	H	L	H	H	L	L	H	H	H	H		H	H	H	L	H	L	H	H	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H	L	H	H	H	L	H	H	L	H	L	H
SHT 3H	521	H	H	H	L	H	L	L	L	H	L	H	H		H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	L	L	L	L	H	L	H	H	H	H	H	H	L	L	H	H	H	L	H
SHT 2H	530	H	H	H	L	H	L	L	L	L	H	H	H		H	H	H	H	L	H		H	H	H	H	H	H	L		L	H	L	H	H	L	H	H	L	H	L	L	H	L	L	L	L	*	H
SHT 2H	531	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	L	L	H	L	L	L		*	H
SHT 3S	540	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L		L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	H	L	H	H	H	*	H
SHT 3S	541	H	H	L	L	H	L	L	L	H	H	H	H		L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	L	L	H	L	L	L	H	H
SHT 3Q	550	H	H	H	H	H	L	L	L	H	H	L	L	L	H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	L	L	H	H	H	L	H	H	L	H	L	H
SHT 3Q	551	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	H	H	L	L	H	H	H	H	H	H	L	H	L	L	H	L	H	H	L	H	L	H	H	L	H	H	H	L	L	L	H
SHT 2L	560	H	H	H	L	H	L	L	L	H	L	H	H		L	H	H	H	H	H	L	H	H	H	H	H	L	H	L	L	L	L	H	H	L	H	H	H	H	L	L	H	L	H	L	L	L	H
SHT 2L	561	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	L	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	H	L	H	L	L	H	H	H
SHT 1C	570	H	H	L	L	H	H	L	L	H	H	L	H		H	L	L	H	L	L	L	H	H	H	H	H	H	L	H	L	H	L	L	H	H	H	H	L	H	H	L	H	L	L	L	H	*	H
SHT 1C	571	H	H	L	H	H	L	L	H	L	H	H	H		H	H	H	L	H	L	L	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	L	H	H	H	H	*	H
SHT 2B	600	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	L	L	H	L	L	*	H
SHT 2B	601	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	H	L	L	H	H	H	H	H	H	L	L	H	L	H	L	L	L	L	H	H	L	H	H	H	L	L	L	L	L	*	H
SHT 2AA	610	H	H	L	H	H	L	H	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	L	L	L	L	H	H	H
SHT 2AA	611	H	H	L	H	H	H	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	L	L	L	L	H	H	H
SHT 2Y	620	H	H	H	L	H	L	L	L	H	H	H	H		H	H	H	L	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
SHT 2Y	621	H	H	H	H	H	L	L	L	L	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H	L	H	L	H	H	L	H	H
SHT 4A	630	H	H	H	H	H	L	L	L	L	H	H	L	L	H	H	H	L	H	L	L	H	H	H	H	H	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	H	H	H	H
SHT 4A	631	H	H	L	H	H	L	H	L	H	H	H	H		H	H	L	L	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L	H		L	H
SHT 2T	640	H	H	H	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	L	H	L	H	H	H
SHT 2T	641	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	H	H	H	H	L	L	H	H
SHT 2W	650	H	H	L	H	H	H	L	L	L	H	H	H		H	H		L	L	L	L	H	H	H	H	H	H	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	L	H	L	H	H
SHT 2W	651	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	H	L	H	H	L	H	H
SHT 2X	660	H	H	L	H	H	L	L	L	H	H	L	L	L	H	H	L	H	L	L	L	H	H	H	H	H	L	L	H	L	H	L	L	H	L	H	H	L	H	H	H	H	L	H	L	L	H	H
SHT 2X	661	L	H	L	H	H	L	L	L	H	H	L	L	L	H	H		L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	L	L	H	H	L	H	H	H	H	L	H	L		H	H
SHT 3C	670	H	H	H	H	H	L	L	L	H	H	L	L	*	H	H	H	L	H	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	L	H	L	H	H	L	L	L	L	H	H	*	H
SHT 3C	671	H	H	H	L	L	L	L	L	H	H	H	H		H	H	H	L	H	L	L	H	H	H	H	H	H	H	L	L	H	L	H	H	L	H	H	L	H	L		L	L	L	H	H	*	H
SHT 1E	700	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L		L	L	H	L	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	L	H	L	H
SHT 1E	701	H	H	L	H	H	L	L	L	L	H	H	H		H	H	L	L	L	L	L	L	L	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
SHT 2S	710	H	H	H	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	H	L	H	L		H	H
SHT 2S	711	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	H	H	H	H	L	L	H	H
SHT 4B	720	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L	H	L	L	H
SHT 4B	721	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H
SHT 1B	730	H	H	H	H	H	H	L	L	H	H	L	H		H	H	H	L	H	L	L	H	H	H	H	H	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H	L	L	H	H	H	H
SHT 1B	731	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
SHT 2L	740	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	L	L	H	H	H	L	H	L	L	L	H	H
SHT 2L	741	H	H	L	H	H	L	L	L	L	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H
SHT 1F	750	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	H	L	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	H	H	H	L	L	L	L	H
SHT 1F	751	H	H	H	L	H	L	L	L	H	H	L	H		L	H	H	L	L	H	L	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	L	H	H	H	H	L	H
SHT 4K	760	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	L	H	H	H	H	L	L	H	H	H	L	H	H	L	H	H	L	H	H	L		L	H	H	L	L	H
SHT 4K	761	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	H	H	H	H	H	L	H	H	L	H	H	H	L	H	H	H	H	L	H
SHT 2V	770	H	H	L	H	H	L	L	L	H	H	H	L	H	H	H	L	L	L	L	L	H	H	H	H	H	L	H	H	L	H	H	H	H	L	H	H	L	H	H	H	H	H	H	L	L	H	H
SHT 2V	771	H	H	L	H	H	L	L	L	H	H	H	L	L	H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	H	H	H	H	L	L	H	H

NOTE:
* NORMALLY H, L WITH ' N ' DATA ROUTINE
BLANK LOCATIONS DON'T CARE STATES
BOLD LETTERS ACTIVE STATES.

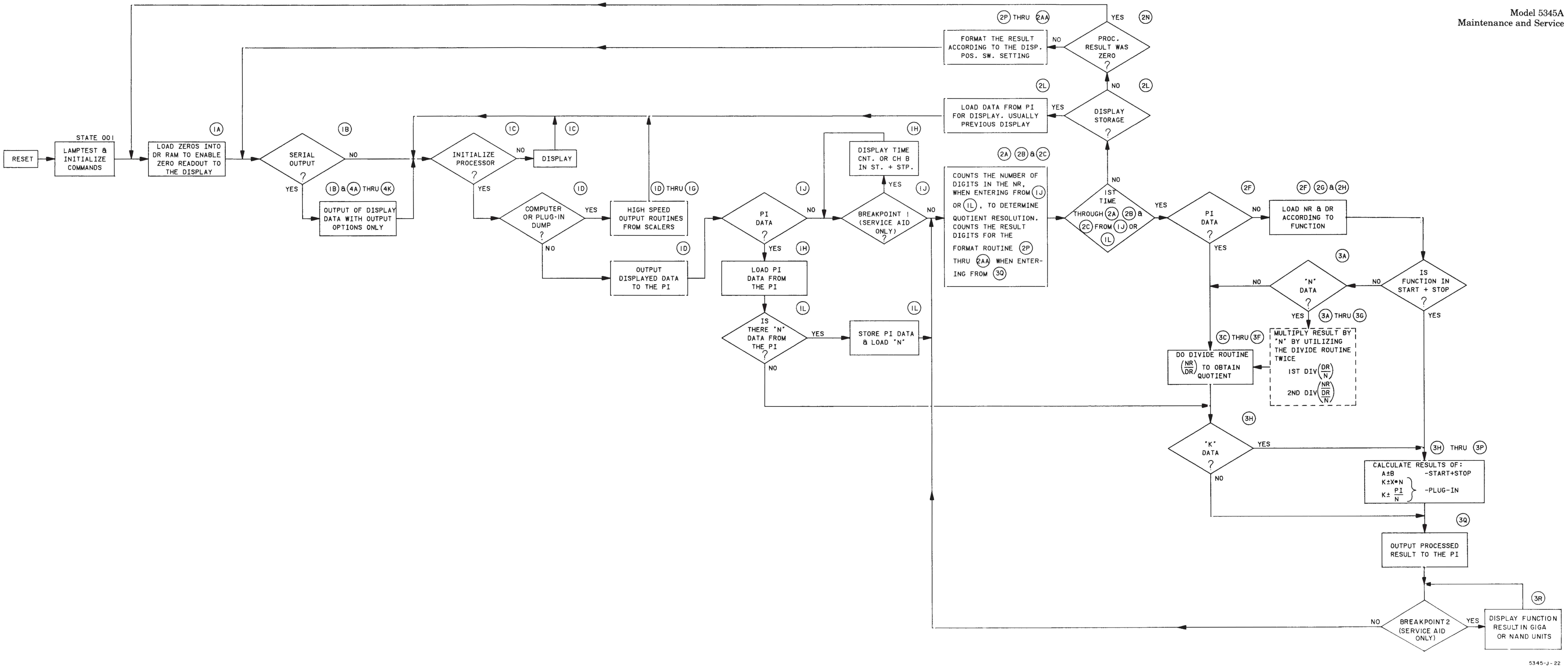

RESET
STATE 001
LAMPTEST & INITIALIZE COMMANDS
1A
LOAD ZEROS INTO DR RAM TO ENABLE ZERO READOUT TO THE DISPLAY
1B
SERIAL OUTPUT ?
NO
YES
1B & 4A THRU 4K
OUTPUT OF DISPLAY DATA WITH OUTPUT OPTIONS ONLY
1C
INITIALIZE PROCESSOR ?
NO
DISPLAY
1C
YES
1D
COMPUTER OR PLUG-IN DUMP ?
YES
NO
HIGH SPEED OUTPUT ROUTINES FROM SCALERS
1D THRU 1G
1D
OUTPUT DISPLAYED DATA TO THE PI
1J
PI DATA ?
NO
YES
1H
LOAD PI DATA FROM THE PI
1L
IS THERE "N" DATA FROM THE PI ?
YES
NO
1L
STORE PI DATA & LOAD "N"
1H
DISPLAY TIME CNT. OR CH B IN ST. + STP.
YES
1J
BREAKPOINT 1 (SERVICE AID ONLY) ?
NO
2A 2B & 2C
COUNTS THE NUMBER OF DIGITS IN THE NR, WHEN ENTERING FROM 1J OR 1L, TO DETERMINE QUOTIENT RESOLUTION. COUNTS THE RESULT DIGITS FOR THE FORMAT ROUTINE 2P THRU 2AA WHEN ENTERING FROM 3Q
1ST TIME THROUGH 2A 2B & 2C FROM 1J OR 1L
NO
YES
2L
LOAD DATA FROM PI FOR DISPLAY. USUALLY PREVIOUS DISPLAY
YES
DISPLAY STORAGE ?
NO
2L
2P THRU 2AA
FORMAT THE RESULT ACCORDING TO THE DISP. POS. SW. SETTING
NO
PROC. RESULT WAS ZERO ?
YES
2N
2F
PI DATA ?
NO
YES
2F 2G & 2H
LOAD NR & DR ACCORDING TO FUNCTION
3A
"N" DATA ?
NO
YES
3A THRU 3G
IS FUNCTION IN START + STOP ?
NO
YES
3C THRU 3F
DO DIVIDE ROUTINE (NR/DR) TO OBTAIN QUOTIENT
MULTIPLY RESULT BY "N" BY UTILIZING THE DIVIDE ROUTINE TWICE
1ST DIV (DR/N)
2ND DIV (NR/(DR/N))
3H
"K" DATA ?
YES
NO
3H THRU 3P
CALCULATE RESULTS OF:
A±B -START+STOP
K±X•N
K± PI/N
-PLUG-IN
3Q
OUTPUT PROCESSED RESULT TO THE PI
3R
BREAKPOINT 2 (SERVICE AID ONLY)
NO
YES
DISPLAY FUNCTION RESULT IN GIGA OR NAND UNITS
5345-J-22

Figure 5-9. Simplified Processor Flow Chart

SYMBOLOGY

←	reads "assign," e.g., DPLR←-1 reads "DPLR assign minus one."
+	reads "or" (will occasionally read "plus," e.g., DCR←DRC+1).
•	reads "and."
—	reads "not," e.g., qualifier 1E reads: "yes, the counter is ready for data and DPLK is not equal to minus 33."
ƀ	reads "blanks," e.g., QR←ƀ reads "QR assign blanks."
-	reads "minus."

RESET:

STATE 001

This state sets up the conditions prior to lamp test and the display of zeros. Lamp test is accomplished by the RESET and DISP CLK EN signals. The DPLK←DPLK-1 command clocks the DPLK counter. The DPLK output is then used as the display clock for the LED display. The RESET FRONT END command resets the scalers to zero.

Lamp test is displayed when enabled by DRC←DRC+1. The reset circuit enables the DRC←DRC+1 command repeatedly so the Denominator Register Counter is circulated through all 16 locations of the Denominator RAM. This causes lamp test display for approximately 50 msec during reset.

The decimal point is also positioned out of the visual range of the display by DPFR←-1. Plug-in data is inhibited by PI XMT BUS. The FLAG←H and DC←0 qualifiers are used later. PROC BUSY is inhibited until the end of the measurement phase.

1A QUALIFIER

The DIGIT COUNTER has just been set to 0, so command State 101 is selected.

STATE 101

This state sets the sign in the display to plus, continues to RESET FRONT END and inhibit PROC BUSY. Zeros are again loaded into the DR and also in the QR by DRC←DRC+16 and QRC←QRC+16. The decimal point is also shifted by the command DPLR←DPLR-1 for the serial output routine.

1B QUALIFIER

The SERIAL OUTPUT qualifier determines if the TALK ALWAYS switch is set or the serial output routine has been remotely programmed.

STATE 730

The command state resets the DPLK counter and digit counter. The DR and QR RAMs, which contain the data to be outputted, are shifted one RAM location by DRC←DRC+15 leading digits in the QR RAM. Digit counter is used by the programming option A12 to indicate the type of data to be outputted. See Table 4-2 A12 ROM sequence. After execution of this state, the DR and QR counters address the MSD in the RAM. The PROC BUSY is inhibited during the output routine.

STATE 731

This state continues to RESET FRONT END and inhibit PROC BUSY.

1C QUALIFIER

The INIT PROC qualifier remains false (N) until completion of the next measurement phase. Upon completion of TIME and EVENTS loaded into the scalers, the last measurement is displayed at State 571.

STATE 571

This state reads the DR contents to the display with commands DR←DR, DRC←DRC+1. If the display time is 12 μsec or more, the DRC will go through 11 states for a positive display of 11 digits; 12 states for a negative display of 11 digits and the - polarity sign. The display clock is generated by command DPLK←DPLK-1. The PI XMT BUS command inhibits PI DATA while DR data is read to the display. PROC BUSY is also inhibited until measurement phase is completed.

STATE 570

This state signifies the beginning of the process cycle. The DRC, DC, and DPLK counters are reset at this state.

1D QUALIFIER

The COMPUTER DUMP +PI DUMP qualifier remains false unless activated by the remote programming unit or the plug-in unit.

STATE 210

This state loads the TIME and EVENT counts into the NR and DR, respectively. The EVENT counts are transmitted through the DR to the plug-in unit. The number of digits (α) transferred out of the TIME AND EVENT scalers is 16 ($\alpha = 16$) for COMPUTER DUMP operation. For PI DUMP operation α is a variable from 1 to 16 ($\alpha = 1 - 16$). Refer to "Theory of Operation" in applicable manual for plug-in unit.

STATE 211

This command state enables the DR contents to be read to the plug-in when requested and also loads the time count from the A11 time scaler into the NR. The asterisk is also turned off. The following commands provide these operations.

DR←DR
DRC←DRC+16
	Rotate the contents of the DR onto the bus.

PI CLK EN	Enables 16 register clock pulses to the PI for data loading.

NR←TC
NRC←NRC+16
	Control the writing of the time count into the NR.

QR←ƀ
QRC←QRC+16
	Loads blank (ƀ) into the WR.

$\overline{\text{PI XMT BUS}}$	Inhibits plug-in data from being placed on the bus.
FLAG←L	This is a qualifier director used for the plug-in data routine.
*←OFF	Turns off the asterisk in the display block.

$1D_1$ QUALIFIER

The PI DUMP qualifier is determined by the plug-in unit when PI DUMP data is requested, otherwise the qualifier is false and COMPUTER DUMP data is assumed.

STATE 300

This state transfers TIME counts from NR through DR to the plug-in. The numbers of digits transferred (α) is determined by PI DUMP. See "Theory of Operation" in plug-in manual for added details. PI CLK EN provides clock pulses to the plug-in unit for data loading, RES FRONT END resets all scalers, and $\overline{\text{PI XMT BUS}}$ enables data input to the plug-in unit.

STATE 301

Blanks are loaded into the WR by QR←ƀ and QRC←QRC+16 commands to blank the display when COMPUTER DUMP is requested. The EXT OUT EN signal to A12 enables data outputting on the general purpose interface bus (HP-IB).

$1D_2$ QUALIFIER

This qualifier is true unconditionally and selects state 320.

STATE 320

Scalers in A11 reset by RES FRONT END command while $\overline{\text{PROC BUSY}}$ signals processing cycle is complete. Decimal point is set out of visual range for next display cycle by DPLR←-1 command.

STATE 321

This state occurs only if a qualifier malfunction occurs. State 321 is programmed identical to state 320 so counter operation is not affected.

1E QUALIFIER

The READY FOR DATA • $\overline{\text{DPLK=-33}}$ qualifier performs two main functions.

1. It causes the process to go into a wait loop (State 700 and State 750) until the READY for DATA (RFD) signal is received from the output recording device.
2. Causes the output to be terminated after all 32 characters have been outputted.

STATE 700

The EXT OUT EN signal is used to enable placing data on the general purpose interface bus. RES FRONT END resets the A11 scalers.

STATE 701

The EXT OUT EN signal is used to enable placing data on the general purpose interface bus (signal to A12). The FLAG←H causes the A12 DAV line to go Low, indicating the data is on the bus. PI DATA is inhibited from the A13 bidirectional bus and DPLK is decremented, indicating a character has been outputted.

1F QUALIFIER

The DPLK=-33 qualifier determines when all the characters have been outputted from the DR and NR RAMs. It is initialized to minus one at State 570 and each time a character is outputted, State 701 decrements the counter.

STATE 750

This state inhibits the plug-in from placing any data on A13A(7, 5, 6, and $\bar{6}$) bidirectional bus. The EXT OUT EN signal is used to enable placing data on the general purpose interface bus.

STATE 751

This state loads blanks into the DR for the display, sets the decimal point out of visual range by DPLR←-1, resets front end for next measurement, and disables the processor. The sign is also set to + for the display. This completes the computer dump routine.

1G QUALIFIER

The DATA ACCEPTED is a qualifier which originates from the recording device via the A12 assembly. If the data has not been accepted by the output device, State 330 is selected.

STATE 330

This state is a wait state which enables the data to be held on the output lines until the data is received by the recording device. PI XMT BUS is held inactive, thereby inhibiting PI DATA. EXT OUT EN allows the data to be held on the general purpose interface bus.

STATE 331

Once the data is accepted, the next character can now be readied for outputting. This is done by shifting the DR and NR RAMs by one place (DR←NR, DRC←DRC+1 and NR←NR, NRC←NRC+1). The EXT OUT EN remains enabled, however, the FLAG←L causes the DAC line on A12 to go High which indicates the data on the bus is no longer valid. PI XMT BUS remains inactive, inhibiting PI DATA.

Figure 5-9
SIMPLIFIED PROCESSOR FLOW CHART

(See Page 5-29)

1H QUALIFIER The PI DATA or BREAKPOINT 6 qualifier checks for PI DATA or the service switch setting A14S1-6. The 5354A uses this qualifier when sending its band frequency to the 5345A.

STATE 150 This state sets the sign to "+" and loads PI DATA to the DR RAM. The PI decimal point is also transferred to the DPLK counter. The PI XMT BUS enables the PI to transmit its data onto the A13 bidirectional data bus.

STATE 151 This state sets the sign to "+" and loads the time count from the NR to the DR in preparation for State 360. All data transferred to the display must be done via the DR RAM. The flag is also set High for future qualifiers 2C, 2D, and 2E.

1J QUALIFIER The BREAKPOINT 1 qualifier is generally used when servicing the 5345A. When it is enabled by switching A14S1-1, the contents of the NR is displayed via the DR RAM.

STATE 360 This state reads data from the DR RAM (time count) and into the display. The DPLK counter generates the DISP CLK. The DISP CLK EN enables the display and also causes the DRC on A13 to select a count 11 mode. DPLR is decremented, so its correct operation can be verified easily. This state also inhibits any PI DATA. The QR is also rotated with the DR RAM; however, this is done for purposes of servicing only.

STATE 361 This state reinitializes the DPLK, DPLR, QMC, and DRC counters. This is normally done after display states.

1K QUALIFIER The DPLR=DPLK qualifier essentially causes the contents of the DPLK counter to be loaded into the DPLR. The DPLR counter increments at State 231 until it equals the DPLK count. The flag must be low at this state to enable the comparison (see A14 Theory). The flag was set low at prior State 211.

STATE 231 This state causes DPLR to increment, so it can be equated with DPLK at the 1K qualifier.

STATE 230 This state resets DPLK; this can be done now because the contents were equated at the DPLK=DPLR qualifier. QMC is also reset for future use, and DPLR is decremented in the event "N" data is selected. "N" data causes the divide routine to be selected; where the result of the routine is accumulated in the QMC, therefore, the decimal point must be offset by one.

1L QUALIFIER The N DATA • $\overline{\text{BREAKPOINT 4}}$ (QMC=0) qualifier is active when N data is available from the PI. Many of the 5245 plug-ins send N data to the 5345A. Breakpoint 4 is a switch used to inhibit N data. This can be helpful when troubleshooting a mainframe that includes a plug-in with N data available.

STATE 171 With no N DATA, State 171 recovers the previous decimal point shift at State 230 with command DPLR←DPLR+1. The digit counter is incremented by DC←DC+1 in case the K DATA routine is selected. DC cannot be set to zero for K DATA.

NOTE

PI and K DATA must be in Giga or Nano units from the plugs-in.

STATE 170 This state sets the processor to divide PI DATA by N DATA. The previously loaded PI DATA is transferred from the DR RAM to the NR RAM by commands NR←DR, NRC←NRC+16, DRC←DRC+16. N DATA can now be loaded from the plug-in via the bidirectional bus to the A13 DR RAM. This is done with command DR←PI, PI CLK EN, and PI XMT BUS. The FLAG←H is used as a qualifier director to ensure State 2E (451) will be selected.

5957

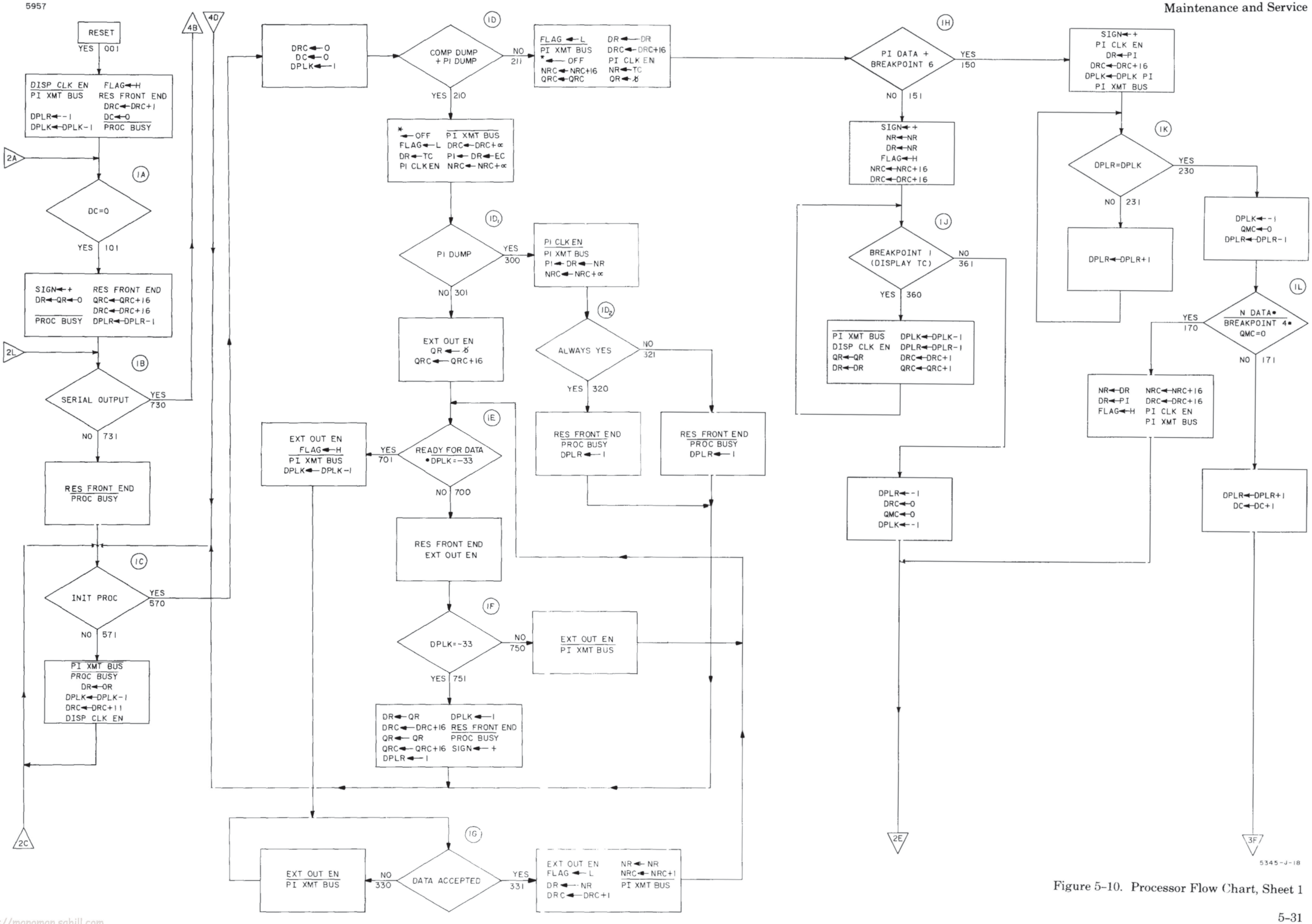


Figure 5-10. Processor Flow Chart, Sheet 1

2A QUALIFIER The DPLK=-17 qualifier is a routine consisting of commands and qualifiers 2A, 2B, and 2C. The commands and qualifiers in the loop are used to determine the number of significant digits desired in the algorithm. This loop looks at time data in the NR, beginning with the most significant digit, to determine the first nonzero digit. The NR is rotated until a nonzero is detected; then, the remaining digits in the RAM are counted.

STATE 441 This state resets QMC. This must be done because the 2A, 2B, and 2C routine could leave the counter at any value.

STATE 440 This state rotates the time data in the NR by one position with NR←NR and NRC←NRC+15 commands. DPLK is used as a loop counter and is decremented by DPLK←DPLK-1 each time it passes this state. The counter will be decremented until all 16 digits have been rotated through the RAM. The QR is also rotated by one position to allow loading of the next digit at State 2B(601) by QRC←QRC+15. This is required when the processor again enters this loop after the arithmetic routines. It maintains the alignment of the result and ensures that blanks remain in leading locations of QR. This must be done because QR is used as the working RAM during the format routine.

2B QUALIFIER The NR=0 • QMC=0 qualifier compares the NR MSD character with QMC. As long as they are both zero, State 600 is selected. When the first nonzero digit appears in the NR, a "noncompare" occurs and State 601 is selected.

STATE 600 This state causes the DPLK=-17 qualifier to be selected. The processor will continue to select State 440 and 600, rotating the NR and QR and decrementing DPLK until NR=0 is not zero at qualifier 2B.

STATE 601 This state loads the contents of the NR into the QR. Because the QR contents were all blanks prior to this state, the MSD zero digits in the NR will result as blank digits in the QR. The operation is not required when entering the 2A, 2B, and 2C loop from State 1J(361) or 1L(170). It is required, however, after the arithmetic routines when entering from State 3R(541) in preparation for the formatting routine.

2C QUALIFIER This qualifier is required to maintain the accuracy specification in MIN gate time when entering the qualifier from 1J(361) or 1L(170). MIN gate is the only gate position where this is required. During this first time through, State 400 is selected if the leading MSD is a 5 or greater. It it is less than 5, State 401 will be selected and the leading digit will not be counted. Events, Ratio, Start or Stop, and MIN always cause State 400 to be selected. The $\overline{\text{QMC=0}}$ ensures that for the remaining times through this loop State 2C(400) will be selected instead of 2C(401). $\overline{\text{FLAG=H}}$ causes State 2C(400) to always be selected when entering the 2A, 2B, and 2C loop from State 3R(541) instead of 1J(361) or 1L(170).

STATE 401 This state ensures two actions:

1. That State 601 will be selected for the remaining times through the loop, instead of State 600. This ensures that any remaining zero digits in the NR will be counted.
2. Causes the $\overline{\text{QMC=0}}$ to be true, thereby always forcing State 400 to be selected during the remaining times through the loop. This causes Digit Counter to count the remaining digits at State 2C(400).

STATE 400 If the 2C qualifier caused this state to be selected on the first pass through the loop, then QMC←QMC+1 performs the same action it did at State 401. DC←DC+1 is incremented and loaded into Digit Storage by DS←DC each time this state is encountered. This causes the digits in the NR to be counted by DC and stored in DS.

2D QUALIFIER This qualifier is also used to maintain the accuracy specification, as was qualifier 2C. When the 2D qualifier conditions are met, the result in the divide routine calculates one extra quotient digit. It does this because DS is incremented at State 220. The FLAG=H in this qualifier is true the first time this state is encountered because of State 1J(361). It will be false after the 2A, 2B, and 2C routine is encountered the second time from State 3R(541). In this case, it was set low after the divide routine at State 3G(121). This causes State 220 to be bypassed. The accuracy specification is checked only when the state is encountered for the first time.

STATE 220 Increments DC by one and places this into DS. This causes the quotient result in the divide routine to calculate one more digit when in MIN gate.

STATE 221 Causes State 220 to be bypassed.

Sheet 1

Figure 5-10
PROCESSOR FLOW CHART, SHEET 1

(See Page 5-31)

2E QUALIFIER	The first time this qualifier is encountered from 2A, 2B, and 2C, the flag will be high from 1L(170) or 1J(361); therefore, State 451 will be selected. The second time through this loop from 2A, 2B, and 2C, the flag is low and DPLK=-17 is false, so State 450 is selected. The DPLK=-17 is active when entering this state from sheet 3K after the result has been multiplied by "N". This was done in routine 3A through 3G. Selection of State 451 causes the divide routine to be repeated.
STATE 450	The DPLK counter is reset at this state.
STATE 451	Because the contents of DC are now stored in DS for divide routine, the counter is reset by command DC←0.
2F QUALIFIER	This qualifier checks for PI DATA or BREAKPOINT 6. BREAKPOINT 6 is a service switch, located on A14S1-5, which enables State 050 to be selected.
STATE 050	This state is selected for the division of PI DATA by "N". The QR is loaded with zeros in preparation for the divide routines 3C through 3F.
STATE 051	Time count from the scalers is loaded into the NR and also rotates into the DR. This is in preparation for doubling the time count to place reading in terms of Giga or Nano units.
2G QUALIFIER	This qualifier determines if the time count must be doubled. It is not doubled for C Channel Events + Ratio + Start + Stop.
STATE 421	When the time count is not doubled, the event count is loaded into the DR. DR←EC and DRC←DRC+16 perform this operation.
STATE 420	The NR and DR RAMs are rotated and the contents are added, thereby yielding the result of twice the time count. NR←NR+DR and DRC←DRC+16 and NRC←NRC+16 perform this. As the DR RAM is rotated, the event count is loaded into it.
2H QUALIFIER	This qualifier determines if the NR and DR contents must be rotated to yield the reciprocal. This operation must be done for a frequency measurement.
STATE 530	Rotates the NR and DR contents to enable calculation for frequency measurement.
STATE 531	No change in NR and DR contents is required. Causes qualifier 2J to be selected.
2K QUALIFIER	State 200 is selected when the counter's function is START or STOP.
STATE 200	This state sets the DC to one and also increments DPLR by one. DC is used as a qualifier director at State 000 (3P). It must not equal zero when going through this state. The decimal point for start or stop must be right justified in the display. The DPLR value prior to 2K was equal to -1; so by incrementing DPLR by one, it will now be equal to zero. This positions the decimal point to the extreme right in the display.
STATE 201	This state causes qualifier 3A to be selected.

2L QUALIFIER Some plug-ins have the capability of storing the old, or previously displayed data. When the plug-in requests a transfer of the old displayed data, the data is transferred from a plug-in RAM. When this occurs, State 560 is selected.

STATE 560 This state loads the old display contents into the DR RAM. This is done by DR←PIS, DRC←DRC+16, PI CLK EN, and by enabling the PI XMT BUS line. The decimal point data is transferred to the DPLK counter by DPLK←DPLK_PI. DPLR is reset in preparation for State 2M. Any data that was stored by the PI is assumed to be "+", so the sign is assigned "+". The plug-in can make data "-" by activating $\overline{\text{PI INV SIGN}}$. The RES FRONT END command is provided in preparation for the next measurement.

STATE 561 The FLAG←H command is required for the Auto/Manual routine (2P through 2AA).

2M QUALIFIER This qualifier looks for equality between DPLK and DPLR. When this occurs, their contents are the same. This means that, in effect, the contents of DPLK was loaded into DPLR.

STATE 241 When DPLK does not equal DPLR, the DPLR counter is incremented by 1 (DPLR←DPLR+1) and then rechecked for equality. This continues until they equal.

STATE 240 When equality occurs in the qualifier (2M), the DPLK counter is reset (DPLK←-1). This can be done because the DPLR counter now contains the same count as DPLK. The $\overline{\text{PROC BUSY}}$ line is disabled, so a new measurement cycle can occur. RES FRONT END also occurs in preparation for the new measurement cycle.

2N QUALIFIER Qualifier 2N checks if the DC equals zero. It will be zero if during the previous 2A, 2B, and 2C routine the NR contained all zeros. When this occurs, the Auto/Manual routine (2P through 2AA) is bypassed and the processor goes into the display routine to display or output zeros. Normally, the DC has something other than zero, so State 510(2P) is selected.

STATE 510 This state selects the Auto/Manual routine (2P).

STATE 511 The DPLR counter is set to -1, which sets the decimal point out of the viewable range of the display. RES FRONT END is done in preparation for a new measurement cycle.

2P QUALIFIER This qualifier determines if the front panel DISPLAY POSITION is set to AUTO or the DISPLAY POSITION has been set to a manual position for the first time (AUTO SC • LOCAL MUL) and RESET has been pressed.

STATE 501 This state selects the local multiplier qualifier (2Q).

STATE 500 This state selects the DS<3 qualifier (2R).

2Q QUALIFIER This qualifier determines if the multiplier is local or if it is programmed remotely. If it is being programmed remotely, then State 411 is selected and the remote multiplier is loaded into MS. If the multiplier is local, then MS contains what was loaded at State 710(2S) during the last AUTO processing cycle.

STATE 410 This state selects qualifier 2T.

STATE 411 This state loads the remote multiplier into MS.

2R QUALIFIER DS<3 digit qualifier is required when less than three digits are displayed; for example, MIN and CHECK display .1 GHz. In this case, the display remains unchanged. It does not shift the decimal point or change the multiplier and display to 1XX. MHz (XX equaling factitious zeros). To maintain the current decimal point location and multiplier when there is less than three digits, DC is incremented and stored in DS until the count equals three. It does this in the 271(2R) State. In the case of MIN and CHECK, qualifier 2S performs the DPLR(+1)-DS(+3) function. This qualifier is then satisfied because the difference between DPLR and DS is now -2. This causes State 710 to be selected.

STATE 271 This state increments Digit Counter and stores its contents into Digit Storage until the Digit Storage equals three.

STATE 270 The comparing of DPLR and DS at qualifier 2S requires that the DPLR data be placed on the bidirectional bus. This state, therefore, inhibits any plug-in data from the bus.

2S QUALIFIER This qualifier performs the comparison to determine if the result of the subtraction (DPLR-DS) is between -1 and -3. For example, assume a frequency measurement of the internal check signal is on 1 sec gate time mode. After the division routine at 3C through 3F, a reading of .100000000 GHz results. The AUTO decimal point position will cause a reading with the decimal point realigned to display 100.000000 MHz. This is accomplished as follows:

With .100000000 GHz, DPLR equals +9

With 1 sec gate time, there will be nine digits, so DS=+9. The qualifier compares DPLR with DS; the result is zero, so the -1 to -3 criterion is not met. State 711 is therefore selected. The next requirement is to shift the decimal point in increments of three and check for the -1 to -3 criterion each time. In frequency this causes the multiplier to shift from GHz to MHz to kHz, etc. This operation begins at State 711.

QMC is used to store the multiplier. It will count from 0 to 6, with each number representing a different mutliplier. If QMC reaches 6, it is necessary to ensure it is not incremented any further; therefore, the QMC=6 part of the qualifier causes the 2P, 2R, 2S, 2U, and 2V loop to be exited at State 710(2S). Another instance when this occurs is when a plug-in enables the processor to measure in the pico sec range. This case would cause nano sec to be selected; however, the criterion of DPLR and DS between -1 and -3 is not met. This would attempt to cause micro seconds to be selected and would only worsen the situation. The solution is to retain the nano multiplier. This is done by the qualifier DPLR-DS= + and nano. As an example, for .00XXXX nano sec., DPLR would be 6 and DS-4. The difference provides a + with nano, so the qualifier is now satisfied. State 710 will now be selected, and the nano multiplier and the decimal point position remain unchanged. A zero difference between DPLR and DS will also yield a + result. Another case occurs with an excessively large number in start or stop, such as 999 GHz. This case is covered by the qualifier Start + Stop • DS>12. 999 GHz would be 12 digits, again forcing the processor to 710 leaving the decimal point and annunciator unchanged. The last case occurs with large numbers caused by the Plug-in's multiply-by-N routine. This could cause DPLR to end up in the minus region. When this occurs, the processor again must leave the multiplier and decimal point unchanged. This is provided by the qualifier $\overline{\text{nano}} \bullet \overline{\text{DPLR+}}$.

STATE 710 This state loads the annunciator code from the QMC into the multiplier storage (MS).

STATE 711 This state selects the qualifier 2U.

2T QUALIFIER When entering from 2Q, this qualifier determines if the remote programmed or internal multiplier (MS) is equal to QMC. If not, State 641 will be selected. States 2U and 2V will change QMC and the decimal point until QMC equals MS. When this occurs, the correct multiplier has been selected and State 640 is selected. When entering from 710(2S) or 660(2X), State 640 is always selected.

STATE 641 Causes qualifier 2U to be selected.

STATE 640 This state moves the contents of the QR one location, so the most significant character (digit or blank) is in position for the next qualifier, 2W.

2U QUALIFIER The DPLK counter ensures that qualifier and States 2V are entered three times. DPLK is set to -1 prior to this state.

STATE 740 This state resets DPLK, since States 2V have been entered three times. QMC is also incremented, which represents the multiplier change.

STATE 741 This state causes the DPLK counter to be clocked, decrementing its value by one. This will continue each time this state is encountered until DPLK=-4.

2V QUALIFIER The nano qualifier determines if the measurement is Nano or Giga.

STATE 770 When State 770 is selected, the measurement unit was Giga. The multiplier change requires the decimal point be shifted three places to the display's right. Each shift is accomplished with DPLR←DPLR-1.

STATE 771 When State 771 is selected, the measurement unit was nano. The multiplier change requires the decimal point be shifted three places to the display's left due to 2U and 2V. Each shift is accomplished with DPLR←DPLR+1.

2W QUALIFIER This qualifier is the start of the 2W, 2X, and 2T loop, which is used to position the QR content to its most significant locations. The loop checks the decimal point location. When the decimal point is in the positive region, blanks are loaded in the LSD locations of the QR until there are no MSD blanks. When the decimal point is in the negative region, the QR is rotated one location, and the LSD position is loaded with a factitious zero at 640(2T). This qualifier continues to enter the 2W, 2X, and 2T loop, until the decimal point becomes positive and MSD location of the QR is not a blank.

STATE 650 This state resets digit counter (DC←0). This is required for future State 2AA. The RES FRONT END is activated in preparation for the next measurement. The QR is also repositioned one location. This was required because of previous State 2T(640). The one location change enables the least significant character of QR to be addressed for qualifier 2Y.

STATE 651 This state selects the 2X qualifier.

2X QUALIFIER This qualifier determines if the decimal point counter is in the positive or negative region. State 660 is selected when it is plus.

STATE 660 The blank at the QR location is preserved here with QR←b̸; this character will be in the least significant location after execution of 640(2T). When the contents are rotated at State 2T(640), the decimal point must also be moved. This is done at this state with DPLR←DPLR+1.

STATE 661 Because the decimal point is in the negative region, factitious zeros must be loaded into the least significant location of the QR RAM (QR←0). Because factitious zeros are loaded into the QR, the command *←ON enables the asterisk to be turned on. The QR contents were rotated at State 2T(640), so the decimal point must also remain aligned. This state performs this by incrementing the decimal point code (DPLR←DPLR+1).

2Y QUALIFIER This qualifier determines if the DISPLAY POSITION switch is in the AUTO or manual position; and if in manual, it checks the decimal point position relative to the manual DISPLAY POSITION switch setting. If the decimal point is not equal to the selected display position code, alignment is necessary, so State 621 is selected. Alignment is accomplished by shifting the result and decimal point position right or left until the decimal point code matches the display position code. If AUTO is selected, the result (QR) and decimal point are shifted right until no blanks are located in the right most location. State 621 is also selected for this.

STATE 621 This state changes the QRC code to address the most significant character in the QR. This is necessary in case State 2Z(261) is selected where blanks will be placed in the MSD position.

STATE 620 State 2Y(620) occurs under the two following conditions:

1. In Manual display, alignment is attained.
2. In Auto, the most right-justified digit is no longer a blank.

State 2Y(620) now loads the formatted result into the DR RAM in preparation for the display. The status of the asterisk is determined at this time. DS is loaded with the DC. The asterisk is displayed only if DS is less than five or if an *←ON command occurred. The RES FRONT END and disabling PROC BUSY is in preparation for the next measurement.

2Z QUALIFIER This qualifier determines if the AUTO or manual front panel display has been selected. If the DISPLAY POSITION switch is in manual, it checks if the decimal point position is greater than or equal to the value of the switch setting. If it is not, the MSD of the QR must be loaded with a blank code. The blank is loaded at State 261.

STATE 261 This state completes the "shift the result to the left" operation that was started at 621(2Y). The QR location, which now represents the least significant character of the display, is blanked and decimal point is shifted left one position. Execution of 261 means that an overflow occurs and the asterisk will be displayed, due to DC set to zero at State 650(2W). RES FRONT END is activated in preparation for the next measurement.

STATE 260 This state positions the QRC to address the LSD of the QR RAM (QR←QR and QRC←QRC+1) by cancelling 621(2Y). The decimal point is decremented in anticipation of a shift result (QR) right at 2BB.

2AA QUALIFIER This qualifier examines the LSD of the QR to determine if it is a blank. The QR will be shifted right one location at States 2BB. If the QR location (which will become the most significant character after 2BB) is a blank, DC will count it as a valid right shift (no underflow). If the QR location has a digit, then an underflow will occur (LSD(s)) will be lost. DC is reset to zero, so the asterisk will be displayed. At least five valid shifts are required to prevent an overflow condition. Less than five shifts will also display the asterisk (see A15 Theory).

STATE 610 This state increments DC by one each time the 2AA qualifier encounters a blank in the LSD position.

STATE 611 This state resets digit counter if a blank is not encountered at State 2AA. The state may be encountered only when the DISPLAY POSITION switch is set to manual.

2BB QUALIFIER Qualifier 2BB determines if the decimal point is away from the MSD in the result. If it is, then zeros must be inserted between the digits and the decimal point. When all the zeros have been inserted or if none were needed to begin with and further shift rights are required, blanks are inserted to cancel any possible underflowed digits.

Example: .000DDDDDDDD, 11 digit display with zeros. If the decimal point is less than 16, blanks are loaded in MSD locations.

Example: BBD.DDDDDDDD, the two MSDs are blank.

STATE 011 This state places blank codes in the LSD position of the QR RAM. QRC←QRC+1 positions the blank to the MSD position. RES FRONT END is used in preparation for the next measurement.

STATE 010 This state places zeros in the LSD position of the QR RAM. QRC←QRC+1 positions the blank to the MSD position. RES FRONT END is used in preparation for the next measurement.

3G QUALIFIER This qualifier determines if a second division is required. When it is required, State 120 is selected. Without "N" data, State 121 will always be selected. A second division occurs with a plug-in which supplies "N" data.

STATE 120 This state reloads time count into the NR and adjusts the decimal point position by incrementing DPLR. This state is required in anticipation of the second division where the NR will have measurement data and the DR, the quotient of the first division.

STATE 121 This state loads the result of the division routine from the QR to the DR. The flag is set Low for qualifier 3J and 3L. The digit counter is set to one for qualifiers 3F and 3P.

3H QUALIFIER This qualifier determines if the division result is to be added or subtracted from "K" data. State 521 can be selected only when there is a plug-in that can supply "K" data. BREAKPOINT 5, which is located on A14, can inhibit the "K" data routine even when the plug-in requests it.

STATE 520 This state loads the DR contents into the NR. This is done in preparation for future States 2A, 2B, and 2C. These states use the NR as the working RAM. Digit counter is also reset for the 2A, 2B, and 2C loop.

STATE 521 When the 3H qualifier has been entered from 1F, this state loads PI DATA from the DR into the NR. When the 3H qualifier has been entered from 121(3G) the division result in the DR is loaded into the NR. In either case, "K" data is loaded into the DR. This state also transfers the decimal point code for "K" data from the plug-in to the DPLK counter. PI CLK EN signal enables the transfer of data from the plug-in to the DR RAM. The RES FRONT END command resets the time and event scalers. The scalers will now be a source of zeros for "K" data States 250 and 251(3J). PI XMT BUS enables the plug-in on the bidirectional bus.

Sheet 2

Figure 5-11
PROCESSOR FLOW CHART, SHEET 2

(See Page 5-37)

to zero and providing the "ADD" command to force State 3D(031) to be selected, thereby incrementing QMC to one. When this state is encountered during the first division of the "N" data routine, the DPLR counter will be incremented. This occurs because State 3B(021) set the flag Low.

3D QUALIFIER This qualifier determines if the result of the subtraction at 3C(671) was positive. This is indicated by the plus qualifier from the adder/subtractor on the A13 assembly. If a successful subtraction occurred, the result yields a plus and QMC is incremented at State 031. This operation continues until a negative sign from the A13 adder/subtractor occurs. This indicates an unsuccessful subtraction, and State 030 is selected.

STATE 030 This state loads the subtraction result from QMC into the QR. This requires DPLR to be incremented (DPLR←DPLR+1), so the decimal point remains properly aligned with the data shift. The decimal point shift with "N" data will be decremented (DPLR←DPLR-1). This state also recovers the contents that were contained in the NR prior to the last unsuccessful subtraction. This is done by adding the unsuccessful result in the NR with the DR content. This yields the prior NR contents which are restored to the NR. Commands used for this operation are NR←NR+DR, NRC←NRC+16, DR←DR, and DRC←DRC+16. The MSD is now in the QR. Recovering and restoring the NR and DR are done in preparation of calculating the remaining digits.

STATE 031 This state increments the QMC each time a successful subtraction occurs at State 3C(671). It also increments QMC when a forced add from State 3C(670) occurs.

3E QUALIFIER This qualifier will cause State 311 to be bypassed until the first quotient digit has been calculated in the QMC. State 310 occurs as long as the NR magnitude is smaller than the DR.

STATE 310 This state causes qualifier 3F to be selected.

STATE 311 This state increments DC each time a digit is calculated. This will continue each time this state is encountered until all significant digits have been calculated. QMC is reset in preparation of calculating the next significant digit.

3F QUALIFIER This $\overline{\text{DC=DS}} \bullet \overline{\text{DISP STOR}}$ + FLAG=H part of the qualifier is used by the divide routine in determining if all significant digits have been calculated. State 460 is selected each time there is another significant digit to calculate. DS determines the number of digits in the result to resolve. When all the digits have been resolved, State 461 will be selected. The $(\text{DISP STOR} + \overline{\text{FLAG=H}}) \bullet \overline{\text{DC=14}}$ is used with some plug-in routines. When the flag is Low, as it will be when "N" data from the plug-in occurs, the intermediate result will be calculated to 14 digits. This is accomplished by this qualifier so no truncation error will occur when the final result is calculated. The DISP STOR $\bullet$ $\overline{\text{DC=14}}$ portion of the qualifier performs essentially the same operation as the $\overline{\text{FLAG=H}}$ part and is used when the plug-in enables DISP STOR. This could be done again when calculating the intermediate portion of the result.

STATE 460 This state positions the NR and QR contents one place to the left. The QR is shifted left in anticipation of the next quotient digit to be loaded at State 3D(030). The NR is shifted left to multiply it by 10 so the next quotient digit can be calculated.

STATE 461 This state reinitializes digit counter, DRC, and DPLK by resetting them. This is required for future states.

3A QUALIFIER This qualifier is active if there is an "N" value from the Plug-in. Many of the 5245 plug-ins supply "N". The operation that will be performed is the result times "N". The multiplication is performed by dividing the DR by "N" on the first time through the divide routine (3C through 3F). The second time through the divide routine (3C through 3F) the NR is divided by the first quotient. BREAKPOINT 4 of this qualifier will cause the 3A and 3B "N" routine to be by-passed even when there is "N" data. This is helpful when troubleshooting. QMC=0 is true the first time this qualifier is encountered.

STATE 070 This command increments QMC to one. This ensures that the 3A qualifier will be false after State 3B(021) is selected. This causes State 3A(071) selection.

STATE 071 This state resets QMC and loads zeros into the QR. The QR must contain zeros prior to the divide routine (3C through 3F), since it will be used to store the quotient. QMC was reset in case the "N" data routine was selected. Its value would have been set to one at State 3A(070).

3B QUALIFIER With "N" data, this qualifier is addressed twice, once for each division. The first time the flag will be high from State 1H(151) and State 021 will be executed. State 021 will set the flag low which causes 020 to be addressed the second time.

STATE 021 This state is selected in preparation of entering the divide routine (3C through 3F) for the first time. It loads the DR contents into the NR and the "N" data from the plug-in into the DR. The plug-in data transfer requires PI CLK EN and PI XMT BUS enable signals. The flag is set low for "reversed" decimal point shifts during the first division and selection of State 3G(120). State 120 will cause the divide routine to be selected a second time.

STATE 020 This state is selected prior to the second time through the divide routine. This state transfers the result of first divide routine (DR/"N") from the QR into the DR. The next time through the divide routine this result will be divided into the NR. These two divisions result in NR/(DR/"N"). This effectively multiplies a result times "N". The flag is assigned High to ensure State 3G(121) is selected. The flag set high also causes normal decimal point shifts during the second division.

3C QUALIFIER This qualifier is the beginning of the divide routine. A division is performed in the divide routine by a series of subtractions. The subtractions are accumulated in the quotient multiplier counter (A13). Each time a successful subtraction occurs, QMC is incremented by one. If the NR is 10 times greater than the DR, the quotient multiplier counter will reach 10. When this occurs State 3C(670) is selected.

STATE 671 This state effectively performs the division. This is done by subtracting the DR contents from the NR (NR←NR-DR). The DR contents remain the same and the result of the subtraction is placed into the NR.

STATE 670 QMC equaling 10 at qualifier 3C indicated that the NR is 10 times greater than the DR. This command state decrements the DPLR counter to indicate this is the case. The DR is multiplied by 10 with a shift left. The new value of the DR has been successfully subtracted from the NR once. Therefore, before starting the next set of subtractions QMC must be initialized to one. This is accomplished by setting QMC

3J QUALIFIER This qualifier determines whether DPLR is greater or smaller than DPLK. The possibility of DPLR equaling DPLK was eliminated by qualifier 3L.

STATE 251 This state decrements DPLR while shifting the result to the right. This causes the result's LSD to shift into the MSD position. The scaler, which contains zeros, now loads a zero in the MSD position. This action will continue until the decimal points are aligned.

STATE 250 This state decrements DPLK while shifting "K" data to the right. This causes the "K" data LSD to shift into the MSD position. The scalers, which contain zeros, now load a zero into the MSD position. This action will continue to occur until the decimal points are aligned.

3K QUALIFIER When entering this qualifier, digit counts should never be zero. This causes State 100 to be selected which selects qualifier 3L.

STATE 100 This state provides a delay from State 3J to qualifier 3L.

3L QUALIFIER This qualifier is selected when the START or STOP function is selected or when a plug-in supplies "K" data. For K data the DPLR=DPLK portion of the qualifier is active. The DPLR and DPLK counters, which contain decimal point codes for the result and "K" data, must be aligned prior to the addition or subtraction to "K" data. When the decimal point codes are not equal, State 470 is selected. The 3J and 3K states are selected until alignment is attained. When alignment occurs, State 471 is selected. The addition or subtraction will be performed in the START or STOP routine (3L, 3M, 3N, and 3P). When the START or STOP FUNCTION is selected, the (START + STOP) • $\overline{\text{PI DATA}}$ + $\overline{\text{BREAKPOINT 6}}$ part of the qualifier is used. In this case, only State 471 will be selected.

STATE 470 This state causes the 3J qualifier to be selected.

STATE 471 This state exchanges the contents of the NR and DR RAMs. In START + STOP this places A channel into the NR and B channel into the DR. With "K" data it places the result in the NR and "K" data in the DR. This is done in preparation for the A-B or A+B operation, in both cases at States 430(3M) and 431(3M) respectively. The flag is set Low for future State 550(3Q) and qualifier 2C. This causes the DPLR counter at State 550 to count up (+); and, at qualifier 2C, it always causes State 400(2C) to be selected. PI XMT BUS is also enabled. This is required so that the plug-in can transmit the sign status on the SIGN- line used in qualifier 3M. SIGN- determines whether the result is added or subtracted from "K".

3M QUALIFIER This is a three part qualifier. The first portion of the qualifier is PI • SIGN "-". This part is active when a result is added or subtracted to "K" data. If the sign is minus, the result will be subtracted from "K" data in State 430(3M); otherwise, it will be added at State 431(3M). The second part of the qualifier is $\overline{\text{PI}}$ • CHECK. This is used when in START + STOP and input control is in CHECK position. In this case, A+B is always performed, regardless of the switch setting of the ACCUM MODE START/STOP switch. This causes selection of State 431(3M). The third and final portion of the qualifier is $\overline{\text{PI}}$ • $\overline{\text{A-B SW}}$. When in START + STOP and not plug-in and the A-B switch is not in A-B position, the A+B State 431 is selected. When the ACCUM MODE START/STOP switch is set to A-B, State 430 is selected.

STATE 430 This state subtracts the contents of the DR from the contents of the NR and places the result in the NR. The DR maintains its original contents prior to the subtraction A-B or "K" data minus result.

STATE 431 This state adds the contents of the NR to the contents of the DR and places the result in the NR. A+B or result + "K" data is performed in this state.

3N QUALIFIER This qualifier checks the result of the NR+DR or NR-DR operations. When NR+DR was performed at State 431(3M), the qualifier always selects State 131 because the result will always equal plus. When NR-DR is performed at State 430(3M) a position or negative result will occur. When the NR was larger than the DR, a positive result occurs and State 131 is always selected. When the NR is smaller than the DR a negative result occurs. In this case, State 130(3N) is selected where it adds the negative result in the NR with B or "K" data in the DR. This recovers the original NR and DR contents prior to the subtraction at State 430(3M). The sign is also set to minus to indicate the final result will be negative. Upon completion of this operation, State 471 is again selected. This state again causes the NR and DR contents to be exchanged. When this occurs, the NR will now be larger than the

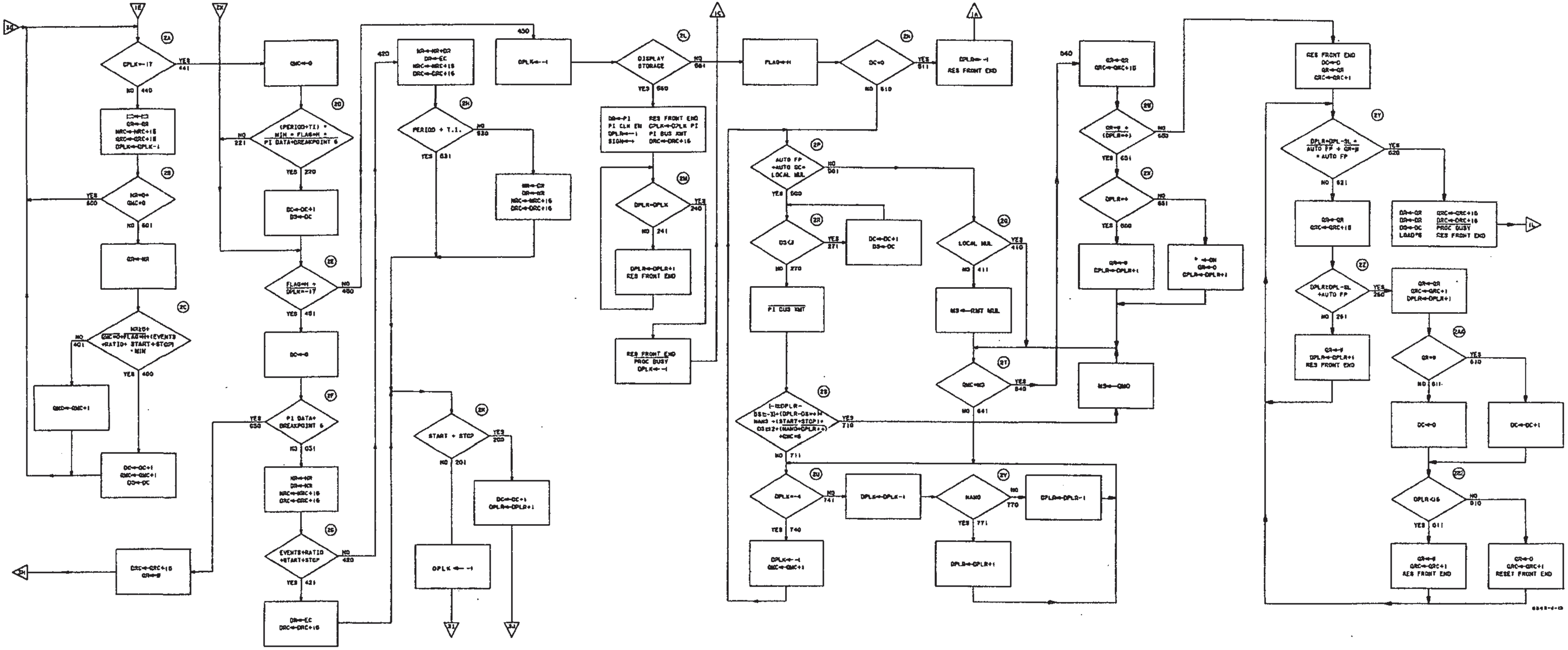


Figure 5-11. Processor Flow Chart, Sheet 2

DR. State 430(3M) is now selected and it will yield a positive result with the sign set to minus. This causes State 131 selection thereby completing A-B in START + STOP or "K" data minus the result.

STATE 130 This state recovers the original NR and DR contents prior to the A-B operation at State 430. This state is selected only when the 3N qualifier yielded a negative subtraction. The sign is set to minus, which indicates the final NR-DR result will be minus.

STATE 131 This state initializes the denominator register counter to zero and raises the 3P qualifier to be selected.

3P QUALIFIER Digit counter is always set at 1 when entering this qualifier. This causes State 000 to be selected.

STATE 000 This state positions the result from the START + STOP routine into the DR. This is done in the event it is desired to display the result with BREAKPOINT 3 at State 540(3R). DR is also reset to zero (or 2A, 2B, and 2C loop).

3Q QUALIFIER This qualifier is required to position the decimal point so it represents the result of Events, Ratio, Start, or Stop in Giga units. This is accomplished by State 550. QMC is incremented until it equals nine, each time the decimal point is shifted left. When the decimal point is shifted nine places (representing Giga) the qualifier is satisfied and State 551 is selected. Plug-in data or BREAKPOINT 6 will also cause State 551 selection. Any PI DATA at this point will already have the decimal point location selected according to Giga units.

STATE 550 This state decrements DPLR and increments QMC until the 3Q qualifier is satisfied.

STATE 551 This state performs the following functions.

1. Loads blank codes into the QR. This is required for the 2A, 2B, and 2C loop so the RAM locations prior to the MSD will contain blank codes.

2. The DR is circulated while PI XMT BUS is inhibited and PI CLK EN is enabled. This enables the DR result to be sent to the Plug-in. The QMC and DPLK counter are also reset at this state for future states.

3R QUALIFIER BREAKPOINT 2 is used for troubleshooting. It is located on the A14 qualifier assembly. When it is enabled, it allows the DR result to be displayed. This display is prior to the AUTO manual routine so the display result will not be formatted.

STATE 340 This state enables the DR contents to be read to the front panel display. The DPLK counter provides display clock and the DISP CLK EN signal enables the A1 and A2 display assembly. The DR contents are sent to the A1 and A2 assembly via the A13 bidirectional bus so the PI is inhibited from sending any data with PI XMT BUS line.

STATE 341 This state resets the DRC and DPLK counters. This must be done in case the display state at 541 was activated by BREAKPOINT 2.

3S QUALIFIER This qualifier detects when the search for the most significant quotient digit in the division routine has been executed 16 times. This is accomplished by subtracting one from the DPLK counter for each time through the search routine and detecting -17.

STATE 540 This state executes a branch to qualifier 3C.

STATE 541 This state will only be accessed when the search for the first quotient digit has been performed 16 times. This state is executed only when either the Numerator Register contents, and/or the Denominator Register contents are zero, and therefore a division cannot be performed. It will reset the front end so that a new measurement can be taken and set DPLR to -1 so that no decimal point will be displayed.

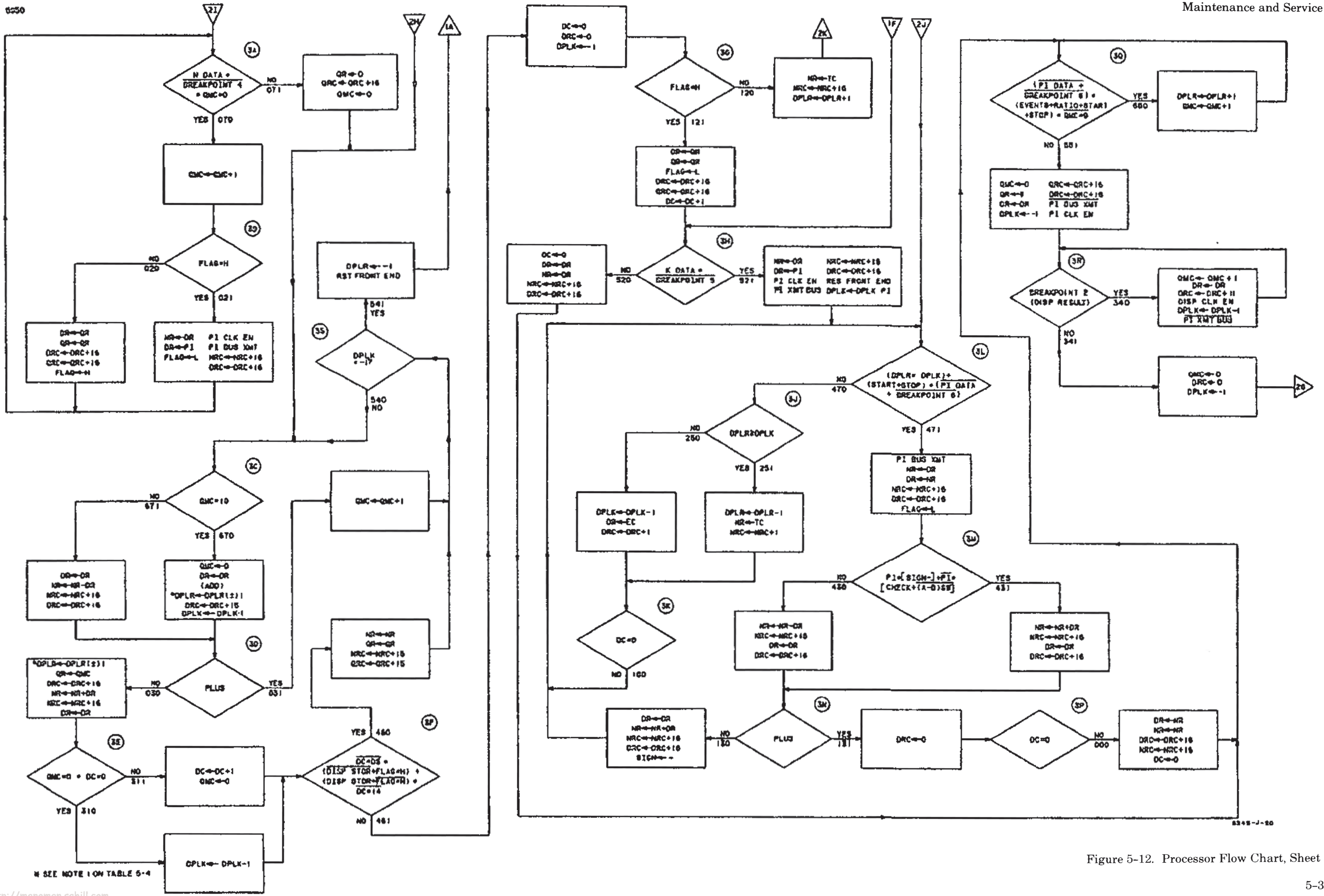


Figure 5-12. Processor Flow Chart, Sheet 3

4A QUALIFIER This qualifier ensures that 1) only 11 digits will be outputted (DPLK>-6), and 2) it will not output 11 digits if there are more than five leading blank codes (QR(QRC)=b̸ • DPLK=-17). The DPLK=-17 ensures that the processor does not continue to execute State 630 if all locations contained blank codes.

STATE 630 This state readjusts the decimal point with DPLR←DPLR+1, because of the shifting left of the DR and QR RAMs. The DPLK counter is also decremented, so the qualifier DPLK>-6 is satisfied when there are only 11 digits left in the RAM. The DPLK counter also records how many of the 16 characters in the DR have been scanned (characters are scanned from most to least significant). The processor busy is not active throughout the serial routine. This means if forced arm occurs, the measurement could begin during the serial out routine. Qualifier 4A and State 630 will continue to be selected until all the leading blanks are bypassed; then, State 631 is selected.

STATE 631 This state increments digit counter, setting its value to one. This enables the sign digit of the display to output (see output coding table). The PI XMT BUS line is also disabled, ensuring that PI DATA cannot get onto the bus. The flag is set low, alerting the A12 assembly that a character is ready to output. PROC BUSY remains inactive.

4B QUALIFIER This qualifier is generated by the device receiving the output data. When the output device enables the A12 output assembly RFD line, the "yes" state is selected and the character is outputted. Until this occurs, the qualifier and the "no" state continue to be selected.

STATE 720 This state serves as a wait loop until the NRFD line from the output device is activated. The state continues to inhibit any PI DATA and PROC BUSY. The EXT OUT EN signal enables the A12 board to output. This signal and the Flag signal cause data valid (DAV) to be generated; however, this doesn't occur until the qualifier is satisfied and the yes state is selected.

STATE 721 This state continues to inhibit PI DATA and PROC BUSY. The EXT OUT EN signal and Flag assigned high (FLAG←H) cause the data valid (DAV) to output to the recording device. This signal enables the character to be transferred.

4C QUALIFIER This qualifier is generated by the device receiving the output data. When the output device enables the data accept (NDAC) line, it indicates that the recording device has received the data. The "yes" state is selected when this occurs. The qualifier and the "no" state continue to be selected until this does occur.

STATE 370 This state continues to inhibit PI DATA and PROC BUSY. The EXT OUT EN line continues to remain active.

STATE 371 This state continues to inhibit PI DATA and PROC BUSY. EXT OUT EN remains enabled. The flag is assigned low and causes data valid (DAV) to become inactive. This is in preparation for outputting the next character. Digit counter is incremented by one (DC←DC+1). This causes its value to equal two, which now enables the DR contents to output. (See output coding table.)

4D QUALIFIER	See the 4B qualifier description. The qualifier operation is the same as for this qualifier.
STATE 160	See State 720(4B) description. The command operation is the same as for this state.
STATE 161	See State 721(4B) description. This command operation is the same as for this state.
4E QUALIFIER	See the 4C qualifier description. This qualifier operates the same as this state.
STATE 140	See State 370(4C) description. The command operation is the same as for this state.
STATE 141	See State 371(4C) description. This state differs only that digit counter is not incremented. Its value remains at two, thereby continuing to output each character in the denominator register in addition to outputting the decimal point once.

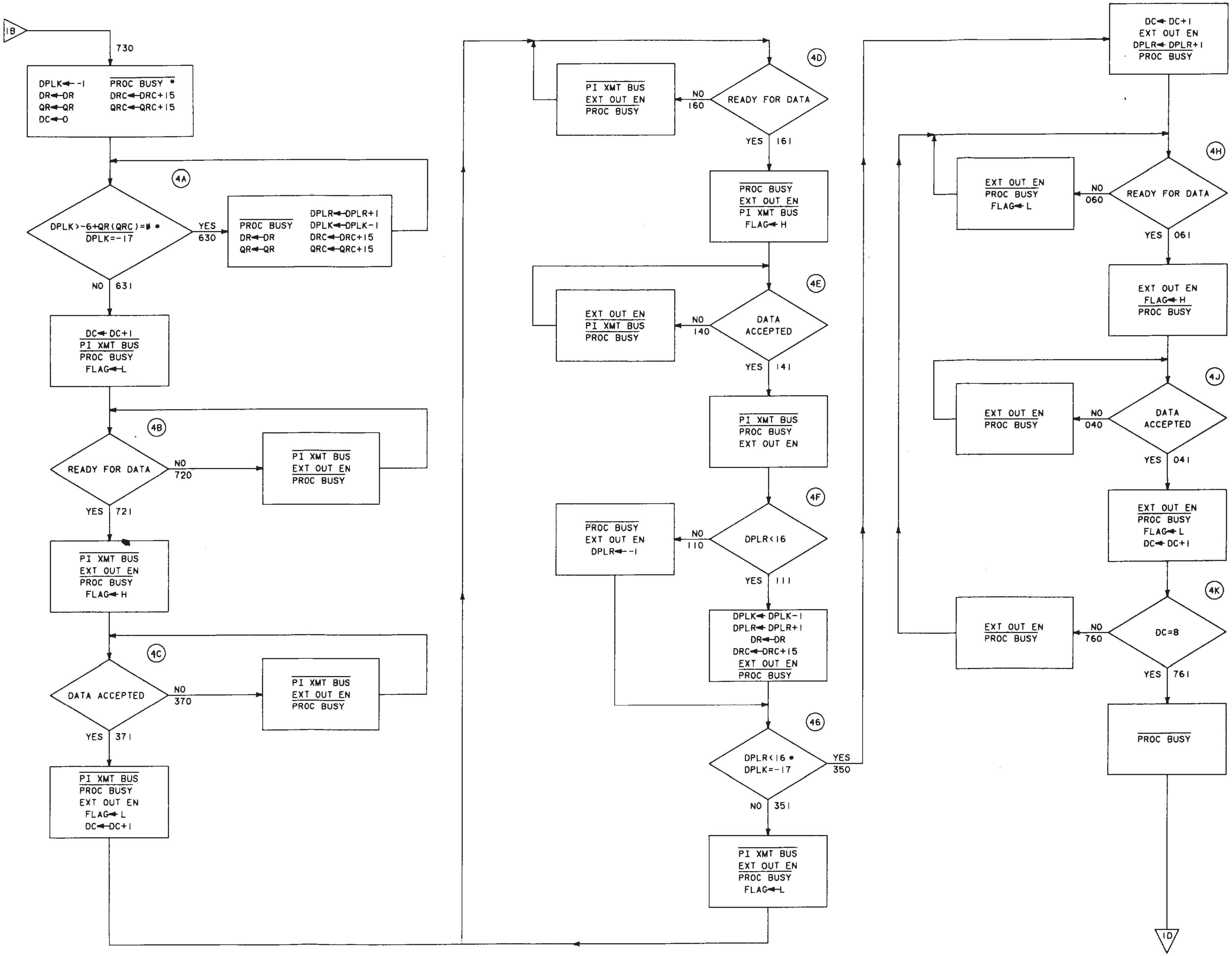
Sheet 3

Figure 5-12
PROCESSOR FLOW CHART, SHEET 3

(See Page 5-39)

4F QUALIFIER	This qualifier determines when the decimal point is ready to output. When DPLR is not less than 16, State 110 is selected. This also indicates that the decimal point has just been outputted. The digit counter is still equal to two; however, DPLR was 16. The output coding indicates Decimal Point.
STATE 110	This command state continues to enable EXT OUT EN and inhibit PROC BUSY. DPLR is reset to minus one from 16. This is done so the remaining denominator register digits to the right of the decimal point can be outputted. Note that DPLR no longer equals 16 on the output; however, Digit Counter still equals two.
STATE 111	This command state decrements the DPLK loop counter. This indicates that another RAM location has been outputted. The result is now shifted left so that the next digit can be outputted. DPLR is incremented to maintain the decimal point position in relation to the digits. EXT OUT EN remains enabled and PROC BUSY is still disabled.
4G QUALIFIER	This qualifier causes all 16 digits in the DR RAM to be observed. Digits are outputted by State 4D and 4E. This continues until this qualifier is satisfied and State 350 is selected. DPLR<16 causes 351 to be selected only in the special case of all blanks in DR with a decimal point at the right-most position.
STATE 351	This state sets the flag low, alerting the A12 assembly that a character is ready to output. The PI XMT BUS line disables any PI DATA and PROC BUSY also remains disabled. EXT OUT EN remains enabled.
STATE 350	Once all required characters output from the DR RAM, the digit counter is incremented to three. As per the output coding, this enables an ASCII "E" to be the next output character. DPLR is incremented by one to adjust for State 4F(110) (where DPLR was set from 16 to minus 1 — it should have been set to zero). PROC BUSY remains inactive and EXT OUT EN remains enabled.
4H QUALIFIER	See the 4B qualifier description. The qualifier operation is the same.
STATE 060	This command state and the qualifier will continue to be selected until the Ready for Data (NRFD High) signal is received from the recording device. The flag is set low in preparation of outputting the next character. PI XMT BUS is not inhibited at this state, as it was at States 4B and 4D, because the remaining characters are not being transmitted from the DR RAM onto the A13 bidirectional bus. EXT OUT EN remains enabled and PROC BUSY is disabled.
STATE 061	EXT OUT EN and Flag assigned high cause the data valid (DAV) line to transfer the character to the recording device. EXT OUT EN remains enabled and PROC BUSY is disabled.
4J QUALIFIER	See the 4C qualifier description. This qualifier operates in the same manner.
STATE 040	Because the output data is not sent from the DR RAM onto the bidirectional bus, it is not required to inhibit PI XMT BUS. The remaining description is the same as 4C(370).
STATE 041	Digit Counter is incremented each time this state is encountered. This enables the remaining characters as per the output coding, to output at States 4H and 4J. Flag is assigned low in preparation of the next character. EXT OUT EN remains enabled and PROC BUSY disabled.
4K QUALIFIER	When digit counter equals eight, all characters have been outputted per the rear panel output coding table. When this occurs State 761 is selected.
STATE 760	This state prepares the character to output by states 4H and 4J. EXT OUT EN is enabled and PROC BUSY remains inactive.
STATE 761	Maintains PROC BUSY inactive and returns the processor to the initialize processor qualifier 1D.

* MEASUREMENT STARTS AT 730 IF SAMPLE RATE IS BYPASSED. IF MEASUREMENT TERMINATES BEFORE COMPLETION OF OUTPUT ROUTINE, THEN THE DISPLAY (STATE 571) WILL BE BYPASSED.



REAR PANEL OUTPUT CODING

DC	DPLR	REAR PANEL DATA
010	16	DECIMAL POINT
000	$\overline{16}$	DENOM. REG. OUTPUT
001		DIGIT SIGN
010		DENOM. REG. OUTPUT
011		"E"
100		EXPONENT SIGN
101		EXPONENT DIGIT
110		CARRIAGE RETURN
111		LINE FEED

Figure 5-13. Processor Flowchart, Sheet 4

Table 5-5. In-Cabinet Performance Check

A. Set POWER switch to ON.

B. Push RESET. All segments of display, including decimal points should light.

C. Perform Self-Check, Table 3-2.

1. CHANNEL A FREQUENCY AND SENSITIVITY

Specifications:

Range: 20 Hz to 500 MHz
Sensitivity: 20 mV rms

Equipment:

Signal generators listed in Table 5-2.

NOTE

A very wide band source such as the HP Model 8660A/B Synthesizer with 86602A plug-in is not a recommended substitute for the fundamental oscillator type 8640B Signal Generator. With such a wideband source applied to the wideband counter, any instantaneous random event from the synthesizer broadband noise floor will be measured as a count if above the counter triggering threshold. If an 8660A/B is used to check the counter, the Synthesizer output level should be low (≈20 mV rms) so the noise floor will be below the counter trigger threshold.

a. Set counter controls as follows:

FUNCTION	FREQ A
GATE TIME	100 ms
DISPLAY POSITION	AUTO
SAMPLE RATE	full ccw
LEVEL	PRESET
ATTEN	X1
Input Impedance	50Ω
Input Amplifier Control	SEP
Input Coupling	DC

b. Adjust signal generator from 20 Hz to 500 MHz, maintaining 20 mV rms input amplitude. Counter should properly display all frequencies within this range. Record on test card.

Table 5-5. In-Cabinet Performance Check (Continued)

2. CHANNEL A ATTEN CONTROL

Specifications: ATTEN (sensitivity): 200 mV rms in X10

Equipment: Signal Generator: HP 651A

a. Set counter controls as follows:

FUNCTION	FREQ A
GATE TIME	100 ms
DISPLAY POSITION	AUTO
SAMPLE RATE	full ccw
LEVEL	PRESET
ATTEN	X10
Input Impedance	50Ω
Input Amplifier Control	SEP
Input Coupling	DC

b. Connect signal generator output to 5345A Channel A input. Set signal generator to 10 kHz at 0V rms.

c. Increase amplitude of input signal until counter displays a stable count of 10 kHz. Output level meter should read 200 mV or less. Record on test card.

3. TIME INTERVAL CHECK

Specifications:

10 ns single pulse time interval
120 mV p-p sensitivity

Equipment:

Pulse Generator: HP 8007B
Sampling Oscilloscope: HP 180A with HP 1810A
Attenuator: HP 355D

a. Set counter controls as follows:

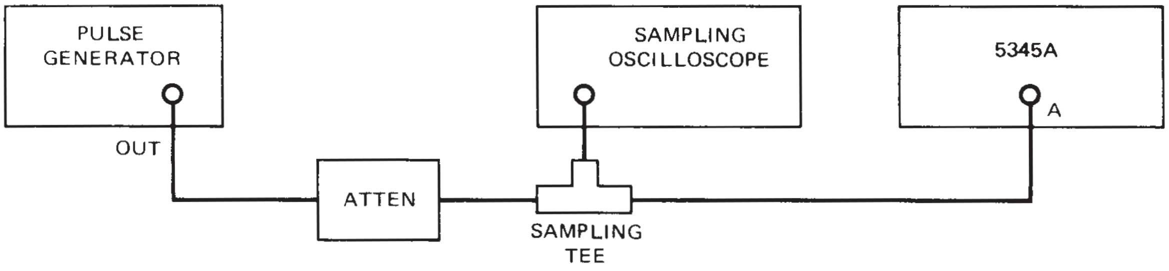
FUNCTION	TIME INT. A to B
GATE TIME	1 ms
DISPLAY POSITION	AUTO
SAMPLE RATE	full ccw
LEVEL (A&B)	PRESET
ATTEN (A&B)	X1
Input Impedance (A&B)	50Ω
Input Amplifier Control	COM A
Input Coupling	DC
SLOPE (Chan A)	+
SLOPE (Chan B)	–

b. Set pulse generator as follows:

TRANSITION TIME (s)	0.1μ - 2.5n; VERNIER full ccw
RATE (Hz)	10k - .3M; VERNIER Midrange
PULSE WIDTH (s)	5n - 50n; VERNIER Midrange
AMPLITUDE (V)	0.2 - 0.5; VERNIER ccw
PULSE POLARITY	+

c. Set output of pulse generator to give 10 ns pulses at 120 mV p-p, using external attenuator.

Table 5-5. In-Cabinet Performance Check (Continued)



d. Adjust CHANNEL A LEVEL control clockwise well into a region where the GATE light flashes.

e. Adjust CHANNEL B LEVEL control clockwise until the display becomes steady.

f. Adjust PULSE WIDTH control until display reads 10 ns or slightly below. Record on test card.

g. Set RATE (Hz) switch on pulse generator to MAN.

h. Set counter's GATE TIME switch to MIN.

i. Manually trigger the pulse generator, once.

j. The counter should display 10 ns ±2 ns. Record on test card.

---

4. CHANNEL B FREQUENCY AND SENSITIVITY

Specifications:

Range: 20 Hz to 400 MHz
Sensitivity: 20 mV rms

Equipment:

Signal generators listed in Table 5-2. NOTE: See NOTE in Table 5-5, step 1.

a. Set counter controls as follows:

FUNCTION	RATIO
GATE TIME	MIN
DISPLAY POSITION	AUTO
SAMPLE RATE	full ccw
LEVEL (A&B)	PRESET
ATTEN (Chan B)	X1
Input Impedance (A&B)	50Ω
Input Amplifier Control	COM
Input Coupling (A&B)	DC
SLOPE (Chan A&B)	−

b. Set signal generator to 20 Hz at 40 mV and connect signal to counter's CHANNEL A jack.

c. Adjust signal generator from 20 Hz to 400 MHz, maintaining 40 mV rms input amplitude. Counter should display a ratio of one throughout frequency range. As frequency is increased, adjust GATE TIME for more resolution. Record on test card.

Table 5-5. In-Cabinet Performance Check (Continued)

5. CHANNEL B ATTEN CONTROL

Specifications:

ATTEN (sensitivity): 200 mV rms in X10

Equipment:

Signal Generator: HP 651A

a. Set counter controls as follows:

FUNCTION	START
GATE TIME	1 ms
DISPLAY POSITION	AUTO
SAMPLE RATE	full ccw
LEVEL (A&B)	PRESET
ATTEN (Chan B)	X10
Input Impedance (Chan B)	50Ω
Input Amplifier Control	SEP
SLOPE (Chan A)	-

b. Connect signal generator output to 5345A CHANNEL B input. Set signal generator to to 10 kHz at 200 mV rms.

c. Turn CHANNEL A LEVEL control full clockwise. Counter should begin totalizing. Record on test card.

6. INPUT COUPLING, TOTALIZE MODE, AND SLOPE

Equipment:

Pulse Generator: HP 8007B
Oscilloscope: HP 180A with HP 1801A and HP 1820A

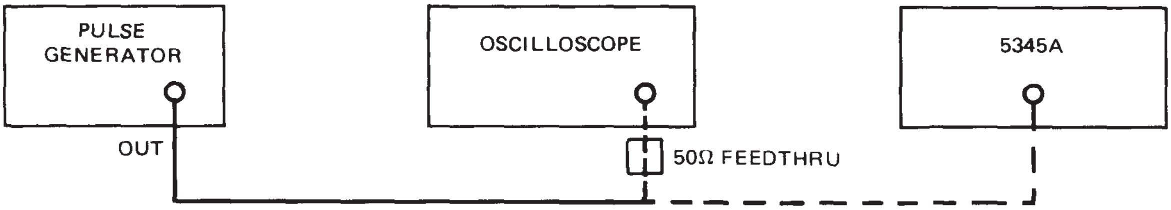
a. Set counter controls as follows:

FUNCTION	START
GATE TIME	MIN
DISPLAY POSITON	AUTO
SAMPLE RATE	full ccw
LEVEL (A&B)	≈10° ccw to -LEVEL
ATTEN (A&B)	X1
Input Impedance (A&B)	50Ω
Input Amplifier Control	SEP
Input Coupling	DC
SLOPE (A&B)	+
ACCUM MODE START/STOP	A+B

Table 5-5. In-Cabinet Performance Check (Continued)

b. Set pulse generator as follows:

TRANSITION TIME (s) ...... 0.1µ - 2.5n; VERNIER full ccw
RATE (Hz) .... .3k - 10k; VERNIER ccw
PULSE WIDTH (s) .... 50µ - 1.5m; VERNIER ccw
AMPLITUDE (V) .... 0.5 - 1
PULSE POLARITY .... +



c. Connect pulse generator to oscilloscope, using 50Ω feedthrough. Set pulse amplitude to 1V peak from zero volts.

d. Connect pulse generator to CHANNEL A jack, directly.

e. Set CHANNEL A Input Coupling switch to AC; counter should begin totalizing. Record on test card. Set SLOPE switch to - ; counter should continue totalizing. Record on test card.

f. Remove cable from CHANNEL A jack and connect to CHANNEL B jack. Counter should *not* totalize.

g. Set CHANNEL B Input Coupling switch to AC; counter should begin totalizing. Record on test card. Set SLOPE switch to - ; counter should continue totalizing. Record on test card.

h. Set ACCUM MODE START/STOP switch (rear panel) to A-B and push RESET.

i. Turn CHANNEL A LEVEL control full clockwise. Counter should begin totalizing and minus light should be on. Record on test card.

---

7. GATE OUTPUT, SAMPLE RATE, AND FREQUENCY STANDARD OUTPUT

Specifications:

Gate Output: 0 to >1V into 50Ω
Sample Rate: Continuously variable from <0.1 sec to >5 sec., also will hold display.
Frequency Standard Output: 10 MHz sine wave, >1V rms into 50Ω

Table 5-5. In-Cabinet Performance Check (Continued)

Equipment:

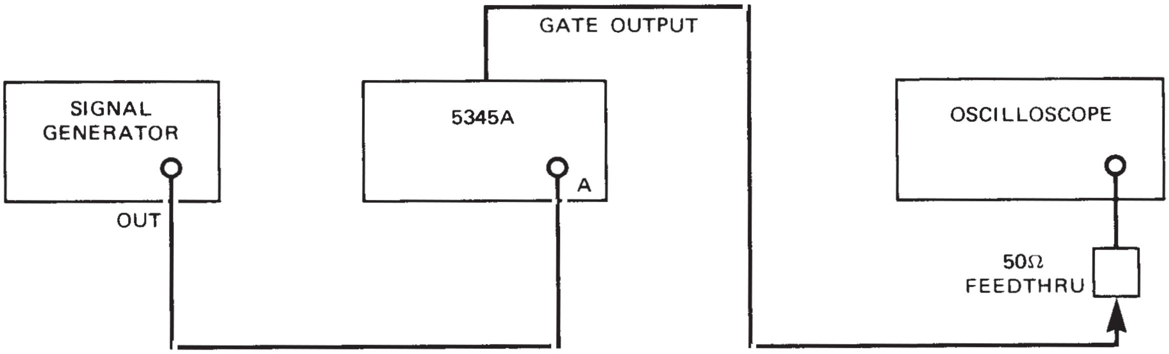
Signal Generator: HP 651A
Oscilloscope: HP 180A with HP 1801A and HP 1820A

a. Set counter controls as follows:

FUNCTION	FREQ A
GATE TIME	10 ms
DISPLAY POSITION	AUTO
SAMPLE RATE	full ccw
LEVEL	PRESET
ATTEN	X1
Input Impedance	50Ω
Input Amplifier Control	SEP
Input Coupling	AC

b. Set signal generator to 1 MHz at 20 mV rms.

c. Set oscilloscope's sweep time to 10 msec.



d. The positive pulses (about 10 ms wide) should be 0 to >1V. Record on test card.

e. The time between positive pulses should be <0.1 sec. Record on test card.

f. Slowly turn SAMPLE RATE control clockwise and observe increase in time between flashes of counter's GATE light.

g. At full clockwise position (not in HOLD) time between flashes should be >5 seconds. Record on test card.

h. Set SAMPLE RATE switch to HOLD. GATE light should *not* flash again. Record on test card.

FREQUENCY STANDARD OUTPUT

i. Remove cable from GATE OUTPUT jack and connect to FREQ STD OUTPUT jack. Oscilloscope should display a 10 MHz sine wave at >1V rms (>2.83V p-p). Record on test card.

---

8. EXTERNAL FREQUENCY STANDARD INPUT (Standard or Option 001)

Specification:

Counter must phase lock to external standard (±5 x 10^{-8} for standard oscillator, ±5 x 10^{-6} for Option 001).

Equipment:

Signal Generator: HP 651A

Table 5-5. In-Cabinet Performance Check (Continued)

a. Set counter controls as follows:

FUNCTION	FREQ A
GATE TIME	10 ms
DISPLAY POSITION	AUTO
SAMPLE RATE	full ccw
Input Amplifier Control	CHECK

b. Connect external standard to rear panel EXT FREQ STD INPUT jack. Set rear panel INT STD-EXT STD switch to EXT STD. Counter should display lamp test for about 2 seconds before again display 100 MHz. The internal time base is now phase locked to the external standard. Record on test card.

c. Set signal generator to 1V rms and connect to EXT FREQ STD INPUT jack.

d. Counter should continuously display lamp test, indicating that counter will *not* phase lock to external standard. Record on test card.

9. GATE CONTROL INPUT

Specification:

To ensure proper operation of Gate Control Input.

Equipment:

Pulse Generator: HP 8007B
Signal Generator: HP 651A
Oscilloscope: HP 180A with HP 1801A and HP 1820A

EXTERNAL ARM

a. Set counter controls as follows:

FUNCTION	FREQ A
GATE TIME	1 μs
DISPLAY POSITION	AUTO
SAMPLE RATE	HOLD
LEVEL	PRESET
ATTEN	X1
Input Impedance	50Ω
Input Amplifier Control	SEP
Input Coupling	DC
Gate Control (rear panel)	EXT ARM

b. Set pulse generator controls as follows:

RATE (Hz)	10K - .3M; VERNIER ccw
WIDTH (s)	1.5μ -50μ
PULSE POLARITY	-
AMPLITUDE (V)	0.5 - 1

c. Connect pulse generator to oscilloscope using 50Ω termination. Adjust pulse generator for 2.0 μs pulses at -1V peak. Disconnect setup.

d. Connect pulse generator to counter's GATE CONTROL INPUT jack.

e. Set pulse generator's RATE switch to MAN.

f. Set signal generator to 2 MHz to 20 mV rms and connect to counter's CHANNEL A jack. Counter should make measurement and display 2.00 MHz. Record on test card.

Table 5-5. In-Cabinet Performance Check (Continued)

EXTERNAL GATE

g. Set counter's GATE CONTROL switch (rear panel) to EXT GATE and SAMPLE RATE knob full ccw.

h. Set signal generator to 2.5 MHz and push counter's RESET button.

i. Push pulse generator's MAN button once; counter's ARM light should turn on. Record on test card.

j. Push MAN button once; ARM light should turn off, GATE light should flash on, and display should read 2.50 MHz. Record on test card.

---

10. CHANNEL A SCALER OUTPUT

Specification:

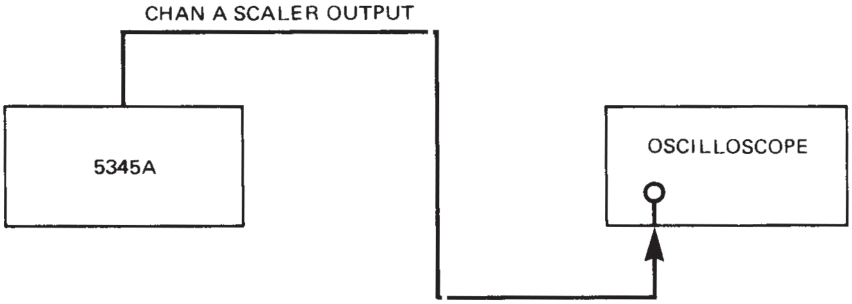
Divides Channel A frequencies by powers of 10.

Equipment:

Oscilloscope: HP 180A with HP 1801A and HP 1820A

a. Set counter controls as follows:

FUNCTION	START
GATE TIME	100 ns
DISPLAY POSITON	AUTO
SAMPLE RATE	HOLD
Input Amplifier Control	CHECK



b. Oscilloscope's display should be 80% duty cycle rectangular waveform, which is a divided version of the input signal. Record on test card.

Table 5-6. Adjustment Procedures

A2 ANODE DRIVER DISPLAY

Equipment:

HP 180A Oscilloscope with 1801A and 1820A. Adjustment A2R6 controls the width of the blanking pulses that are generated from A2U7B. These pulses are in the order of approximately 5 to 50 μs. The purpose of the pulses is to turn off the display when addressing a new digit. It also has the effect of controlling the intensity.

A3 INPUT ATTENUATOR

Equipment:

HP 3480A/3482A DVM
Extender Cable 05345-60205
HP 180A Oscilloscope with 1810A Sampler
HP 8640B Signal Generator

Setup:

1. Set LEVEL controls to PRESET.
2. Connect DVM between common and the cathode of diode A4CR1. Adjust A4R11 for an indication of 0 volts ±50 millivolts. Connect DVM between common and cathode of diode A4CR2. Adjust A4R13 for 0 volts ±50 millivolts.

NOTE

Allow a 5-minute warmup before performing adjustment procedure.

Bias Adjustment

1. Remove front panel display assembly, as outlined in Section III. Connect display assembly to counter, using extender cable. Place side of cable with "CINCH" on side of board with part number (05345-60004).
2. Connect DVM to U2 pin 15 (Channel B, U1 pin 15).
3. Adjust bias pot A4R44 (Channel B, A3R47) for a reading of 1.00V ±50 mV.

The following adjustments are done with the bottom cover and bottom air filter removed. The front panel display assembly is installed in the instrument.

Sensitivity Adjustment:

1. Set 5345A controls as follows:

Input Impedance	50Ω
ATTEN (A&B)	X1
Input Coupling	DC
Input Amplifier Control	SEP
SLOPE (A&B)	+
LEVEL Control	PRESET

2. Set 8640B Signal Generator output to 100 MHz at 100 mV rms into 50Ω.
3. Set 180A Oscilloscope controls as follows:

AC/DC	DC
MAGNIFIER	X1
DISPLAY	INT

PERFORMANCE CHECK TEST CARD

HEWLETT-PACKARD MODEL 5345A
ELECTRONIC COUNTER

Test Performed by ____________________
Date ____________________

SERIAL NO. ________________

DESCRIPTION	**CHECK**
1. CHANNEL A FREQUENCY AND SENSITIVITY	______________
2. CHANNEL A LEVEL AND ATTEN CONTROLS	
Attenuator Sensitivity: 200 mV	______________
3. TIME INTERVAL	
Time Interval: 10 ns at 60 mV p-p	______________
Single Shot Time Interval: 10 ns at 120 mV p-p	______________
4. CHANNEL B FREQUENCY AND SENSITIVITY	______________
5. CHANNEL B LEVEL AND ATTEN CONTROLS	
Attenuator Sensitivity: 200 mV	______________
6. INPUT COUPLING, TOTALIZE MODE, AND SLOPE	
Channel A Totalizes	______________
Channel B Totalizes	______________
A-B Model Totalizes	______________
+ and - Slope	______________
7. GATE OUTPUT, SAMPLE RATE, AND FREQ STD OUTPUT	
Gate Output: 0 to >1V	______________
Minimum Sample Rate: <0.1 s	______________
Maximum Sample Rate: >5 s	______________
Freq. Std. Output: 10 MHz at >1V rms	______________
8. EXTERNAL FREQ STD INPUT	
Phase Locks	______________
9. GATE CONTROL INPUT	
External Arm	______________
External Gate:	
Arm Light	______________
Gate Light	______________
10. CHANNEL A SCALER OUTPUT	______________

PERFORMANCE CHECK TEST CARD

HEWLETT-PACKARD MODEL 5345A
ELECTRONIC COUNTER

Test Performed by ____________________
Date ____________________

SERIAL NO. ________________

DESCRIPTION	**CHECK**
1. CHANNEL A FREQUENCY AND SENSITIVITY	____________
2. CHANNEL A LEVEL AND ATTEN CONTROLS	
Attenuator Sensitivity: 200 mV	____________
3. TIME INTERVAL	
Time Interval: 10 ns at 60 mV p-p	____________
Single Shot Time Interval: 10 ns at 120 mV p-p	____________
4. CHANNEL B FREQUENCY AND SENSITIVITY	____________
5. CHANNEL B LEVEL AND ATTEN CONTROLS	
Attenuator Sensitivity: 200 mV	____________
6. INPUT COUPLING, TOTALIZE MODE, AND SLOPE	
Channel A Totalizes	____________
Channel B Totalizes	____________
A-B Model Totalizes	____________
+ and - Slope	____________
7. GATE OUTPUT, SAMPLE RATE, AND FREQ STD OUTPUT	
Gate Output: 0 to >1V	____________
Minimum Sample Rate: <0.1 s	____________
Maximum Sample Rate: >5 s	____________
Freq. Std. Output: 10 MHz at >1V rms	____________
8. EXTERNAL FREQ STD INPUT	
Phase Locks	____________
9. GATE CONTROL INPUT	
External Arm	____________
External Gate:	
Arm Light	____________
Gate Light	____________
10. CHANNEL A SCALER OUTPUT	____________

Table 5-6. Adjustment Procedures (Continued)

4. Set 1810A Sampler controls as follows:

DISPLAY	FILTERED
MODE	A
POLARITY	+ UP
mV/DIV	200
TIME/DIV (outer knob)	10 nSEC
TIME/DIV (inner knob)	2 nSEC
CW SLOPE	+
SCAN	SWEEP
DIRECT/EXPANDED	EXPANDED
SCAN knob	almost fully cw

5. Disconnect the two white cables connected to the A9 board. Channel A output cable is the longer of the two. Connect these cables through an adapter connector (HP part number 1250-0831) to the oscilloscope's inputs.
6. Adjust A4R2 and A4R11 (Channel B, A4R5 and A4R13) for a signal on oscilloscope.
7. Adjust A4R11 (Channel B, A4R13) for no change in signal when SLOPE switch changes position.
8. Ajust A4R2 (Channel B, A4R45) for 50% duty cycle.
9. Set 8640B output to 20 mV rms.
10. Adjust A4R11 (Channel B, A4R13) for no change in signal when SLOPE switch changes position. Readjust A4R2 (Channel B, A4R5) for 50% duty cycle if required.

A4 INPUT TRIGGER

Equipment:

HP 3480A/3482A DVM
HP 180A Oscilloscope with 1810A Sampler
HP 8640B Signal Generator

NOTE

Allow a 5-minute warmup before performing adjustment procedure.

The following adjustments are done with the bottom cover and bottom air filter removed. The front panel display assembly is installed in the instrument. See Section III for removal of air filter.

Bias Adjustment:

1. Adjust A4R2 (Channel B, A4R5) offset pot to midpoint.
2. Connect 412A to A4U2 pin 3 (Channel B, A4U1 pin 3).
3. Adjust A4R16 (Channel B, A4R19) bias pot for a reading of +800 mV ±50 mV.

NOTE

NOTE — If A4U2 (Channel A) or A4U1 (Channel B) are replaced, the value of A4R15 (Channel A) or A4R18 (Channel B) may have to be increased in value to meet the 800 mV ±50 mV specifications. An increase of approximately 10Ω increases adjustment range of A4R16 or A4R19 approximately 100 mV.

Sensitivity Adjustment:

1. Set 5345A controls as follows:

Input Impedance	50Ω
ATTEN (A&B)	X1
Input Coupling	DC
Input Amplifier Control	SEP
SLOPE (A&B)	+
LEVEL Control	PRESET

Table 5-6. Adjustment Procedures (Continued)

2. Set 8640B Signal Generator output to 100 MHz at 100 mV rms into 50Ω.

3. Set 180A Oscilloscope controls as follows:

AC/DC	DC
MAGNIFIER	X1
DISPLAY	INT

4. Set 1810 Sampler controls as follows:

DISPLAY	FILTERED
MODE	A
POLARITY	+ UP
mV/DIV	200
TIME/DIV (outer knob)	10 nSEC
TIME/DIV (inner knob)	2 nSEC
CW SLOPE	+
SCAN	SWEEP
DIRECT/EXPANDED	EXPANDED
SCAN knob	almost fully cw

5. Disconnect the two white cables connected to the A9 board. Channel A output cable is the longer of the two. Connect these cables through an adapter connector (HP part number 1250-0831) to the oscilloscope's inputs.

6. Adjust A4R2 (Channel B, A4R5) for a signal on oscilloscope.

7. Adjust A4R11 (Channel B, A4R13) for no change in signal when SLOPE switch changes position.

8. Set 8640B output to 10 mV rms.

9. Adjust A4R2 (Channel B, A4R5) for 50% duty cycle.

10. Adjust A4R11 (Channel B, A4R13) for no change in signal when SLOPE switch changes position. Readjust A4R2 (Channel B, A4R5) for 50% duty cycle if required.

A6 and A7 POWER SUPPLIES

CAUTION

BEFORE REMOVING A POWER SUPPLY BOARD, ALWAYS DISCONNECT THE POWER CABLE AT REAR OF INSTRUMENT. TURNING THE POWER SWITCH TO STANDBY IS NOT SUFFICIENT TO PREVENT POSSIBLE COUNTER DAMAGE.

Adjust power supplies only when necessary. Use a quality DVM and place power supply boards on extender boards during adjustment.

+5V and -5.2V Adjustment:

1. Place A6 assembly (05345-60006) on extender boards.

2. Connect plus side of DVM to TP6 on board. Connect common side of DVM to "+5V RET" (+5V return) pin on board.

3. Adjust R19 until DVM reads +5V ±20 mV.

Table 5-6. Adjustment Procedures (Continued)

4. Connect plus side of DVM to TP3 on board. Connect common side of DVM to "-5.2V RET" pin on board.

5. Adjust R29 until DVM reads -5.2V ±20 mV. Return A6 to its connector.

+15V and -15V Adjustment:

1. Place A7 assembly (05345-60007) on extender boards.

2. Connect plus side of DVM to TP2 on board. Connect common side of DVM to "+15V RET" pin on board.

3. Adjust R18 until DVM reads +15V ±20 mV.

4. Connect plus side of DVM to TP7 on board. Connect common side of DVM to "-15V RET" on board.

5. Adjust R24 until DVM reads -15V ±20 mV.

A8 PPL MULTIPLIER NOISE GENERATOR

Equipment:

HP 180A with 1810A Sampler
HP 10020A Resistive Divider Kit

NOTE

TP15 through TP20 are probe sockets. A common socket is located next to each A8 test point for the probes common side. A good ground is essential for TP16-20, otherwise signal amplitude will vary.

1. Set counter's FUNCTION switch to FREQ A.

2. Set oscilloscope controls as shown under appropriate waveforms next to A8 schematic.

3. Connect the 20:1 probe divider from the 10020A kit to the oscilloscope probe.

4. Connect BNC cable from counter's FREQ STD OUTPUT 10 MHz jack (rear panel) to oscilloscope's EXT INPUT.

5. Place A8 on extender boards. (05345-60201 and 05345-60202).

6. Connect oscilloscope probe to TP14. Adjust C29 (labeled CA on the board) for maximum signal. The waveform is a full wave rectified 10 MHz yielding a 20 MHz period. Amplitude should be .75V to 2.0V p-p.

7. Connect oscilloscope probe to TP15. Adjust C43 (labeled CB on the board) 20 MHz signal for maximum. Amplitude should be 2V to 3V p-p.

8. Connect oscilloscope probe to TP16. Adjust C52 (labeled CC on the board) 100 MHz signal for maximum. Amplitude should be .075V to .125V p-p.

9. Connect oscilloscope probe to TP17. Adjust C57 (labeled CD on the board) 100 MHz signal for maximum. Adjust R81 (labeled RA on the board) for signal level of .6V to .7V p-p.

Table 5-6. Adjustment Procedures (Continued)

10. Connect oscilloscope probe to TP18. Adjust C67 (labeled CF on the board) for maximum 500 MHz signal. Amplitude should be .4V to .6V p-p.

11. Connect oscilloscope probe to TP19. Adjust C67 (labeled CF on the board) and C61 (labeled CG on the board) for maximum signal. Amplitude should be .3V to .5V p-p.

12. Connect oscilloscope probe to TP20. Adjust R99 (labeled RB on the board) for signal of ≈.85V. Check that 100 MHz modulation ripple on the top of waveform is <40 mV p-p.

13. Remove A8 from extender boards and reinstall A8 in motherboard. Set counter's FUNCTION switch to TIME INT A to B. Switch Input Control switch to CHECK position. Set GATE TIME switch to 100 ms position. Turn C68 (labeled CE on the board) phase adjust ccw until a stable 10 nsec reading is displayed on the 5345A display. Switch FUNCTION from PERIOD to TIME INT A to B position to ensure reliable reading. NOTE: Adjustment should be turned 360° before setting is selected.

A9 GATE CONTROL

The A9 adjustments were completed at the factory in accordance with the selected bias resistors for the particular ICs used. No attempt at adjustment should be made on this board. See further description adjacent to the A9 schematic.

A15 ROM

Equipment:

100048 10:1 Probe

1. Set counter controls as follows:

FUNCTION	TIME INT A TO B
GATE TIME	10 μs
DISPLAY POSITION	AUTO
LEVEL (A&B)	PRESET
SLOPE, Ch A	-
SLOPE, Ch B	+
Input Coupling (A&B)	AC
Input Impedance (A&B)	1 MΩ
Input Amplifier Control	COM A

2. Connect oscilloscope probe to A15 TP8 and BNC end of probe to CHANNEL A jack. The A15 board need not be placed on an extender board.

NOTE

If the 5345A is suspected faulty, connect BNC of probe to a separate counter (e.g., 5326A).

3. Adjust R5 (located between U4 and U5) to 155 ns.

4. Set FUNCTION switch to PERIOD A.

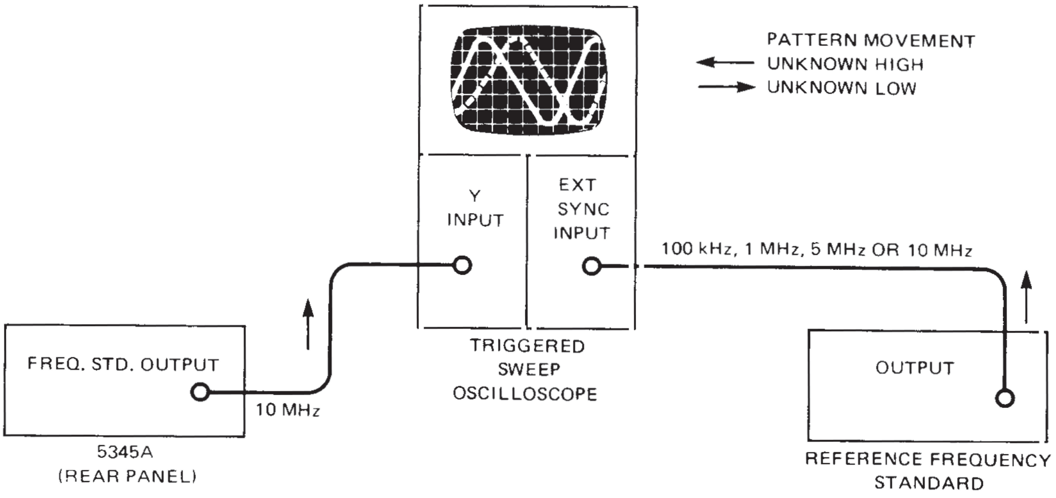
5. Adjust R4 to 255 ns.

6. Set FUNCTION switch back to TIME INT A to B and do steps 3 through 5 until both readings are correct.

Table 5-6. Adjustment Procedures (Continued)

A18 OSCILLATOR (STANDARD OR OPTION 001)

Every few months, the oscillator should be checked to a house standard. When adjustment is required, use the oscilloscope method shown below. Using the appropriate sweep speed, adjust the oscillator until the movement of the pattern is stopped or nearly stopped.



CALIBRATION

MOVEMENT	SWEEP SPEED			NOTES
	1µSEC/CM	0.1µSEC/CM	0.01µ SEC/CM	
1 CM/SEC	1 X 10^{-6}	1 X 10^{-7}	1 X 10^{-8}	TIME SCOPE TRACE MOVEMENT WITH SECOND HAND OF WATCH OR CLOCK
1 CM/10 SEC	1 X 10^{-7}	1 X 10^{-8}	1 X 10^{-9}	
1 CM/100 SEC	1 X 10^{-8}	1 X 10^{-9}	1 X 10^{-10}	

OPTION 001 SPECIAL ADJUSTMENT PROCEDURE

Under normal conditions, the oscillator can be adjusted by using the above procedure. Should the fine-tuning capacitor (accessible through hole in top of oscillator cover) fail to bring the oscillator frequency within range, a coarse adjustment must be made using A18C5. This adjustment is made at the factory to compensate for component value variances. The procedure is outlined as follows:

a. Remove rear panel power cord and remove oscillator from motherboard connector.

b. Remove metal cover from board by removing the four holding screws.

c. Turn adjustment screw of the 18-turn trimmer capacitor A18C4 (see component locator of A18 Option 001, Section VIII) full clockwise. The slot screw itself will not move in or out.

d. Turn C4 adjustment screw 7 turns ccw. This is the electrical center of the adjustment.

e. Place oscillator on extender board and insert extender board into the oscillator connector on 5345A motherboard.

f. Replace power cord, set FUNCTION to FREQ A, and GATE TIME to 100 ms.

g. Connect a 10 MHz frequency standard to CHANNEL A input.

h. Adjust A18C5 for a display of 10.000 018 MHz to 10.000 022 MHz. The 20 Hz offset compensates for cover capacity and warm-up in the counter.

i. Turn power off, mount metal cover to oscillator board, and insert oscillator board into instrument. Replace top cover and allow instrument to warm-up for 1/2 hour before performing oscillator adjustment using oscilloscope method outlined above.

Table 5-6. Adjustment Procedure (Continued)

A12 INTERFACE I/O (OPTION 012) CALIBRATION PROCEDURE

a. Allow instrument warmup of at least 30 minutes.
b. Connect DVM to rear-panel jacks for Channel A and B trigger levels.
c. Set Trigger Level manual controls to Preset position for Channel A and B.
d. Program Channel A to -2.000 volts (A000).
e. Adjust pot A (R69) to -2.0000 volts ±.0005 volt.
f. Program Channel A to +2.000 volts (A:00).
g. Adjust pot B (R74) to +2.0000 volts ±.0005 volt.
h. Program Channel B to -2.000 volts (B000).
i. Adjust pot D (R86) to -2.0000 volts ±.0005 volt.
j. Program Channel B to +2.000 volts (B:00.
k. Adjust pot C (R82) to +2.0000 volts ±.0005 volt.
l. Repeat steps 4 through 12 until DAC is within specified setting.

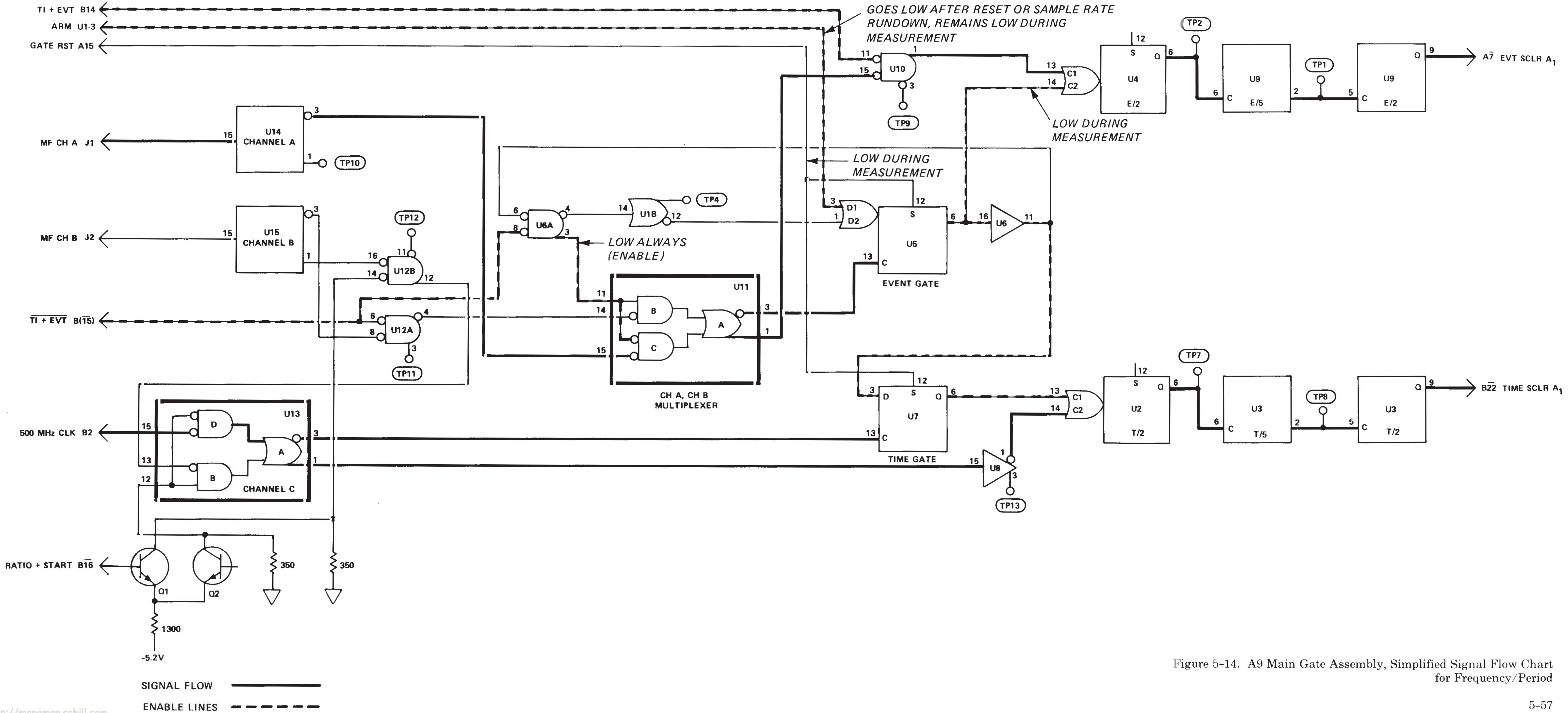


Figure 5-14. A9 Main Gate Assembly, Simplified Signal Flow Chart for Frequency/Period

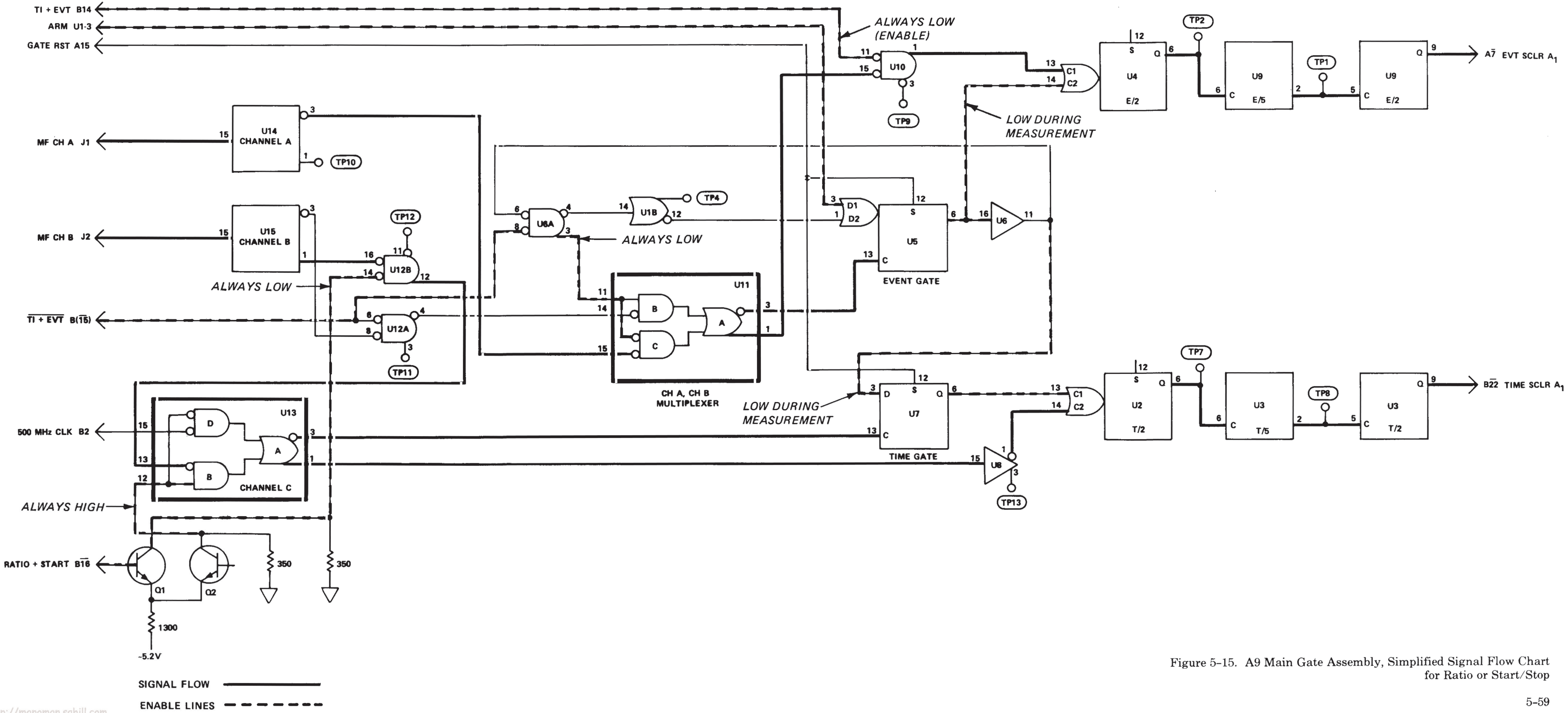


Figure 5-15. A9 Main Gate Assembly, Simplified Signal Flow Chart for Ratio or Start/Stop

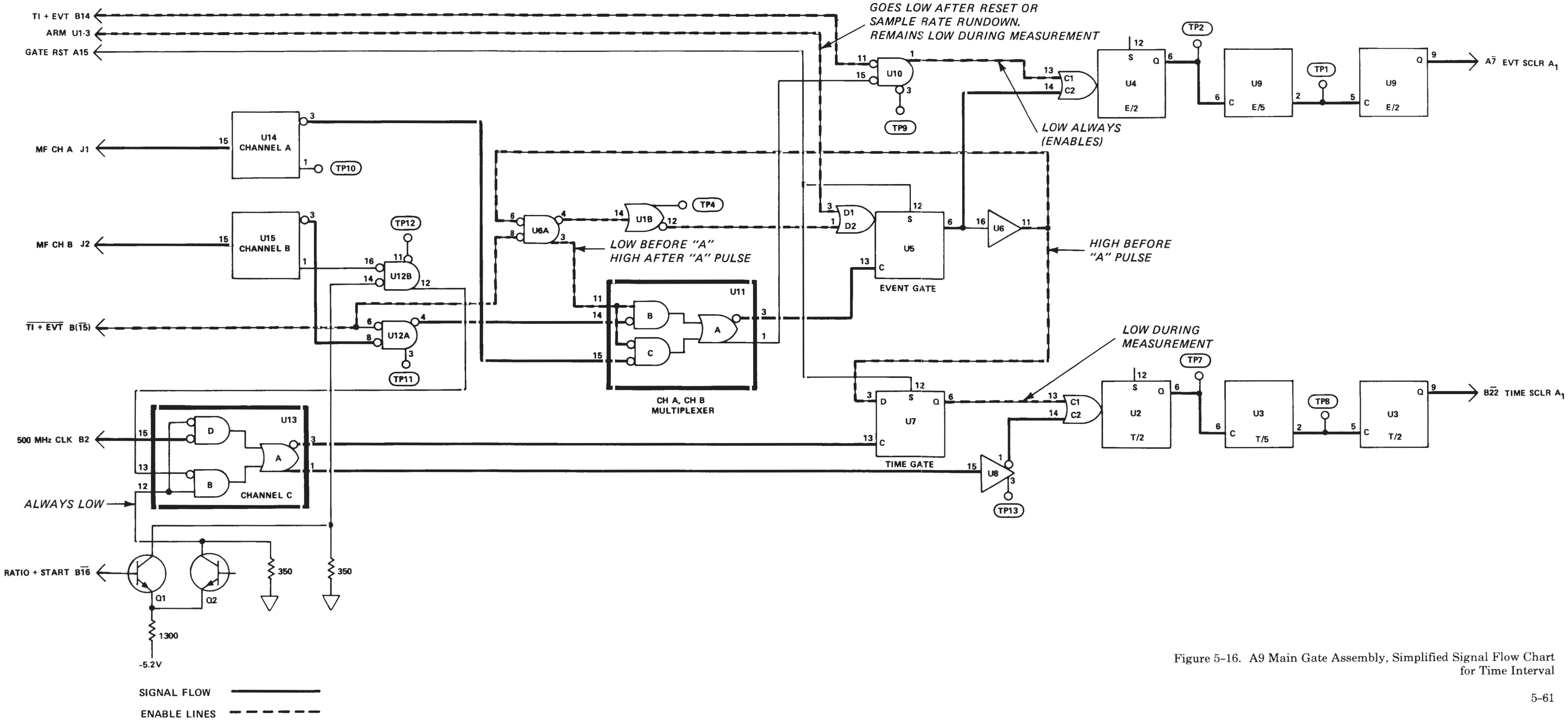


Figure 5-16. A9 Main Gate Assembly, Simplified Signal Flow Chart for Time Interval

SECTION VII

OPTIONS AND MANUAL CHANGES

7-1. INTRODUCTION

7-2. This section contains information necessary to adapt this manual to older instruments. Also included is information for available options. Refer to Section II for remote programming information.

7-3. OPTIONS

7-4. The following is a list of available options: Option 001, 10 MHz, Voltage Controlled Oscillator; Option 010, General Purpose Interface Output (Digital Output only, HP-IB format); Option 011, General Purpose Interface I/O (provides digital output and input control over all functions except input amplifier). Option 012 is similar to Option 011 but includes level and slope control. Correction of faults in Option 012 (05345-60021) board are accomplished under HP Blue Stripe program by board replacement. Order HP Part No. 05345-60521 assembly from nearest HP Sales and Service Office. (See Section II for full description and programming details.)

7-5. FIELD INSTALLATION OF OPTIONS

7-6. With the exception of Option 012, all options are field installable. Before installing Option 001, remove the instrument's bottom cover and remove the two screws that secure the standard oscillator. The optional oscillator can then be substituted for the standard unit. Order part number 05345-60069.

7-7. Options 010 and 011 are installed by removing the right-most patch panel on the counter's rear panel and substituting the A19 Interface Panel. Install the A12 board into the motherboard connectors marked XA12, and connect the A19 ribbon cable to the socket on A12. Note the position of pin one when performing this connection.

Option 010	A12 05345-60023 A19 05345-60024	}	May be ordered under a single number 05345-60208
Option 011	A12 05345-60018 A19 05345-60019	}	May be ordered under a single number 05345-60209

7-8. MANUAL CHANGES

7-9. This manual applies directly to Model 5345A Electronic Counters with serial prefix 1708A. Refer to paragraph 1-4 for a description of the serial prefix effectively.

7-10. Newer Instruments

7-11. As changes are made, newer instruments may have serial prefixes that are not listed in this manual. The manual for these instruments are supplied with a manual change sheet which contains the required updating information. If this sheet is missing, contact the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual.

7-12. Older Instruments

7-13. To adapt this manual to instruments having a serial prefix prior to 1708A, perform the backdating that applies to your instrument's serial prefix as listed in Table 7-1 below.

Table 7-1. Manual Backdating

If Your Instrument Has Serial Prefix	Make the Following Changes to Your Manual
1644A	1
1624A	1,2
1612A	1,2,3
1604A	1,2,3,4
1528A	1,2,3,4,5
1520A	1,2,3,4,5,6
1516A	1,2,3,4,5,6,7
1512A	1,2,3,4,5,6,7,8
1440A	1,2,3,4,5,6,7,8,9
1438A	1,2,3,4,5,6,7,8,9,10
1436A	1,2,3,4,5,6,7,8,9,10,11
1428A	1,2,3,4,5,6,7,8,9,10,11,12
1424A	1,2,3,4,5,6,7,8,9,10,11,12,13
1412A	1,2,3,4,5,6,7,8,9,10,11,12,13,14
1352A	1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
1340A	1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16

CHANGE 1 (1644A)

Page 6-21, Table 6-1:

Change part number of A14 from 05345-60044 to 05345-60034. Change series number from 1708 to 1624.

Page 6-22, Table 6-1:

Change part number of A15 from 05345-60045 to 05345-60035. Change series number from 1708 to 1624.
Change A15U8 from 1816-1018 to 1816-0824.
Change A15U16 from 1816-1019 to 1816-0825.
Change A15U24 from 1816-1020 to 1816-0826.
Change A15U32 from 1816-1021 to 1816-0827.

Page 8-53, Figure 8-18, A14 Qualifier Assembly:

Change schematic to delete jumper and terminals A,B,C near U2 and U7. The point that was terminal A connects directly to U7 pin 5. Also delete jumper and terminals D,E,F near U15. The terminals D and E are replaced with a straight thru connection so that U15(1) connects to U25A(3), R3, and P1A($\overline{16}$).

Page 5-27, Figure 5-11, Processor Flowchart, Sheet 2:

Near the center of the flowchart, delete the DPLK←-1 block between the START+STOP block and the 31 symbols.

Page 5-39, Figure 5-12, Processor Flowchart, Sheet 3:

Replace Figure 5-12 with Figure 7-1.

Page 5-26, Table 5-4, Command Source Listing:

Replace Table 5-4 with Table 7-2.

Page 5-27, Table 5-4, Command Source Listing:

Replace Table 5-4 with Table 7-3.

Page 5-19, Table 5-3, Processor Flow Test Results:

Replace part of Table 5-3 (starting with Delay Switch 00039 and ending with 00220) with Table 7-4 (5 pages).

Page 5-39, Figure 5-12, Processor Flowchart, Sheet 3:

Delete 3S QUALIFIER and change 3R QUALIFIER as follows:

3R QUALIFIER	BREAKPOINT 3 is used for troubleshooting. It is located on the A14 Qualifier assembly. When it is enabled, it allows the DR result to be displayed. This display is prior to the AUTO manual routine so the display result will not be formatted.
STATE 540	This state enables the DR contents to be read to the front panel display. The DPLK counter provides display clock and the DISP CLK EN signal enables the

A1 and A2 display assembly. The DR contents are sent to the A1 and A2 assembly via the A13 bidirectional bus so the PI is inhibited from sending any data with PI XMT BUS line.

STATE 541 This state resets the DRC and DPLK counters. This must be done in case the display state at 541 was activated by BREAKPOINT 3.

Page 5-4, Paragraph 5-27 (using the 05345-60200 Test Board) Step b(4):
Change second sentence to read "The BKPT 1, 2, 3, and 7 refers to test switches located on top of the A14 board.

Page 5-29, Figure 5-9, Simplified Processor Flowchart:
Change flowchart as indicated in partial diagram in Figure 7-2. In block 2A, 2B, and 2C, change last sentence to "....when entering from 3R."

Page 5-29, Figure 5-9, Simplified Processor Flowchart:
Change flowchart as shown in Figure 7-3a.
Page 5-37, Figure 5-11, Processor Flowchart, Sheet 2:
Change flowchart as shown in Figure 7-3b add accompanying 2J QUALIFIER test to page 5-32.

CHANGE 2 (1624A)

This change backdates the manual to cover instruments with CHANNEL A and CHANNEL B ATTEN controls with attenuations of X20 instead of X10.

Page 1-3, Table 1-3, Specifications:
Change first footnote to read "* Trigger error for sine waves is <[±0.3% of one period ÷ number of periods averaged] for signals with 40 dB or better signal-to-noise ratio."

Under INPUT CHANNELS A AND B SEPARATE INPUTS change as follows:

X1 (Same)
X20 400 mV rms sine wave 1.2V p-p pulse

Dynamic Range (preset)

50Ω X1	20 mV to 400 mV rms sine wave 60 mV to 1.2V p-p pulse	1MΩ X1	20 mV to 400 mV rms sine wave 60 mV to 1.2V p-p pulse
X20	400 mV to 7V rms sine wave 1.2V to 7V p-p pulse	X20	400 mV to 8V rms sine wave 1.2V to 24V p-p pulse

Page 1-4, Table 1-3, Specifications:
Change as follows:
Under maximum Input, change X10 to X20.
Change last spec in Maximum Input to 70V rms above 5 MHz.
Under COMMON INPUTS, change Sensitivity (preset) as follows:
Sensitivity: (preset)
50Ω X1 (same)
50Ω X20 800 mV rms sine wave, 2.4V p-p pulse.

Dynamic Range (preset)
50Ω X1 40 mV to 800 mV rms sine wave
120 mV to 2.4V p-p pulse
X20 .8 to 5V rms sine wave, 2.4 to 5V p-p pulse.

Page 5-1, Table 5-1, A3 Assembly:
Change A3 part number from 05345-60038 to 05345-60003.

Page 6-6, Table 6-1, Replaceable Parts for Standard Instruments:
Change A3 part number from 05345-60038 to 05345-60003 Series 1520.
Change A3C4 and A3C7 from 0160-4531 to 0160-0550 Capacitor-Fxd 10 pF ±5% 50WVDC CER, 28480, 0160-0550.
Change A3R4 and A3R7 from 0698-8881 to 0698-8383 Resistor 950K 5% .25W C TC=0+-150, 28480, 0698-8383.
Change A3R5 and A3R8 from 0698-8880 to 0698-8384 Resistor 50K 5% .15W C TC=0+-150, 28480, 0698-8384.

Page 6-24, Table 6-1, Replaceable Parts for Standard Instruments:
Change A3 part number in HP and Mfr Part Number columns from 05345-60038 to 05345-60003.

Page 6-26, Table 6-2, Mechanical Parts:
Change HP and Mfr Part Number for Front Panel MP 20 from 05345-00032 to 05345-00025.

Page 8-31, Figure 8-8, A3 Input Attenuator Schematic Diagram:
Change A3 part number and series number at top of diagram from 05345-60038 series 1644 to 05345-60003 series 1520A.
Change A3C4 and A3C7 from 2.2 pF to 10 pF.
Change A3R4 and A3R7 from 900K to 950K.
Change A3R5 and A3R8 from 100K to 50K.
Change "X10" markings for A3S5 and A3S7 attenuators to "X20".

CHANGE 3 (1612A)

Page 6-21, Table 6-1, A14 Replaceable Parts:
Change A14 from 05345-60034 to 05345-60014 in HP Part Number and Mfr Part Number columns.
Change A14 from "(SERIES 1624) to (SERIES 1612)".

Page 8-53, Figure 8-18, A14 Schematic Diagram:
Change the schematic diagram as shown in the partial diagram in Figure 7-3. The 05345-60034 and 05345-60014 circuit boards are **not** directly interchangeable.

Page 6-22, Table 6-1, A15 Replaceable Parts:
Change A15 from 05345-60035 to 05345-60015 in HP Part Number and Mfr Part Number columns.
Change A15 from SERIES 1624 to SERIES 1612.
Change A15U8 from 1816-0824 to 1816-0344, IC Digital, Memory, 50364, H620IN-5835.
Change A15U16 from 1816-0825 to 1816-0345, IC Digital, Memory, 50364, H620IN-5836.
Change A15U24 from 1816-0826 to 1816-0346, IC Digital, Memory, 50364, H620IN-5837.
Change A15U32 from 1816-0827 to 1816-0347, IC, Digital, Memory, 28480, 1816-0347.

NOTE

The 05345-60035 and 05345-60015 circuit boards are not directly interchangeable.

Page 5-29, Figure 5-9, Simplified Flowchart:
Change qualifier 1D from "COMPUTER OR PLUG-IN DUMP" to "COMPUTER DUMP."

Page 5-30, Flowchart States:
Change STATE 001 as follows:

RESET:

STATE 001 This state sets up the conditions prior to lamp test and the display of zeros. Lamp test is accomplished by the RESET and the DISP CLK EN signals. The DPLK←DPLK-1 command clocks the DPLK counter. The DPLK output is then used as the display clock for the LED display. The RESET FRONT END command resets the scalers to zero. This is in preparation for loading zero data into the DR by commands DR←EC and DRC←DRC+16. The decimal point is also positioned out of the visual range of the display by DPLR←-1. PI XMT BUS inhibits plug-in data. FLAG←H and DC←0 are qualifiers which are used later. PROC BUSY is inhibited until the end of the measurement phase.

Page 5-30, Flowchart States:
Change STATE 571 as follows:

STATE 571 This state reads the DR contents to the display with commands DR←DR, DRC←DRC+11 and DISP CLK EN. The display clock is generated by command DPLK←DPLK-1. PI XMT BUS inhibits any PI DATA while the DR data is read to the display. PROC BUSY is also inhibited until completion of the measurement phase.

Change STATE 570 under 1C QUALIFIER as follows:

STATE 570 This state signifies the beginning of the process cycle. Blanks are loaded into the QR by commands QR←b̸ and QRC←QRC+16. This is done to blank the display when COMPUTER DUMP is requested. The DRC, DC, and DPLK counters are reset at this state.

Change 1D QUALIFIER AND STATES 210 and 211 to the following:

1D QUALIFIER The COMPUTER DUMP qualifier remains false unless the remote programming unit requests that computer dump be outputted.

STATE 210 This state loads the TIME and EVENT counts into the NR and DR, respectively. The flag is set low, alerting the programming output option that the first digit is ready to output. The PI XMT BUS is inactive to ensure that no PI DATA can get onto the bus. The asterisk is also turned off during the blanked display.

STATE 211 This command state enables the DR contents to be read to the plug-in when requested and also loads the time count from the A11 time scaler into the NR. The asterisk is also turned off. The following commands provide these operations.

DR←DR
DRC←DRC+16
	Rotate the contents of the DR onto the bus.

PI CLK EN	Enables 16 register clock pulses to the PI for data loading.

NR←TC
NRC←NRC+16
	Control the writing of the time count into the NR.

$\overline{\text{PI XMT BUS}}$	Inhibits plug-in data from being placed on the bus.
FLAG←L	This is a qualifier director used for the plug-in data routine.
*←OFF	Turns off the asterisk in the display block.

Page 5-30, Flowchart States:
Delete QUALIFIER 1D$_1$, STATES 300 and 301, QUALIFIER 1D$_2$ and STATES 310 and 321.

Page 5-31, Figure 5-10, Processor Flowchart, Sheet 1:
Replace flowchart with Figure 7-4.

Page 5-37, Figure 5-11, Processor Flowchart, Sheet 2:
In STATE 340, change the second line to "DRC←DRC+11."

Page 5-39, Flowchart States:
In STATE 540 change second line to DRC←DRC+11.

Page 5-26 and 5-27, Table 5-4, Command Source Listing:
Replace Table 5-4 with Tables 7-5 and 7-6.

CHANGE 4 (1604A)

Page 6-8, Table 6-1, A4 (05345-60004) Replaceable Parts:
Change SERIES 1612 to 1512.
Delete A4CR3 and A4CR4.

Pages 6-21 and 6-22, Table 6-1, A14 (05345-60014) Replaceable Parts:
Change SERIES 1612 to 1340.
Delete A14R3.

Page 6-22, Table 6-1, A15 (05345-60015) Replaceable Parts:
Change SERIES 1612 to 1352.
Change A15U6 from 1820-1199 to 1820-0586 IC DM74L04N, 27014, DM74L04N.
Delete A15R7.

Page 6-25, Table 6-1, Replaceable Parts (Standard Instrument less Options):
Change W5 Part Number from 05345-60093 to 05345-60092 in "HP Part Number" and "Mfr Part Number" columns.

Page 8-31, Figure 8-8, A4 (05345-60004) Schematic Diagram:
Change series number at the top of A4 schematic from SERIES 1612 to 1512.
Delete diodes A4CR4 and A4CR3. Replace with straight thru connections. Also delete A4CR3 and A4CR4 from REFERENCE DESIGNATIONS.

Page 8-51, Figure 8-17, A13 (05345-60013) Schematic Diagram:
Change signal input to $\overline{\text{B13}}$ (left side of diagram) from $\overline{\text{NRC}\leftarrow 0}$ to $\overline{\text{INIT AUTEST}}$.

Page 8-53, Figure 8-18, A14 (05345-60014) Schematic Diagram:
Change series number at top of schematic from 1612 to 1340.
Change schematic diagram as shown in Figures 7-5 and 7-6.

Page 6-30, Table 6-3, A12 Option 011 Replaceable Parts:
Change A12 circuit board 05345-60018 from SERIES 1604 to 1340.
Change A12Q1 from 1854-0574 to 1854-0246.
Change A12R12 from 0683-3035 to 0683-8225 Resistor 8.2K, 5%, .25W, FCTC=400/+700, 01121, CB8225.

Page 8-49, Figure 8-16, A12 Option 011 Schematic:
Change SERIES 1604 to 1340.
Change diagram for A12Q1 to an NPN transistor.
Change A12R12 from 30K to 8200 ohms.

Page 8-55, Figure 8-19, A15 (05345-60015) Schematic Diagram:
Change SERIES number on top of schematic from 1612 to 1532.
Change A15 schematic as shown in Figure 7-7.

Page 8-65, Figure 8-24, W5J1 Wiring Diagram:
Delete brown wire connection to pin 1 of W5J1.
Delete red wire connection to pin 2 of W5J1.

CHANGE 5 (1528A)

Make note that a rack mount kit HP Part Number 5060-8740 was supplied with instruments serial prefixed 1528A and below.

Page 6-24, Table 6-1, Replaceable Parts:
Change FL1 part number from 0960-0444 to 5060-9422 in HP part number and Mfr part number columns.

Page 8-5, Figure 8-24, Power Wiring Diagram:
Change POWER MODULE from part number 0960-0444 to 5060-9422.

Pages 6-29 and 6-31, Table 6-3, A19 for Options 010, 011, and 012:
Change HP Part Number and Mfr Part Number for M/FEM HEX STANDOFF from 0380-0643 to 0380-1036.

Page 8-63, Figure 8-23, A19 for Options 010, 011, and 012:
Change SERIES number from 1604 to 1340.

Pages 6-12 and 6-15, Table 6-1, A8 Replaceable Parts:
Change A8 circuit board from SERIES 1604 to 1424.

NOTE

Heat sink 1205-0011 from A8U7 was not supplied for instruments prefixed 1528 and below but is recommended for all instruments.

CHANGE 6 (1520A)

Page 6-25, Table 6-1, Replaceable Parts for Standard Instruments without Options:
Change W5 part number from 05345-60092 to 05345-60075 in HP Part Number and Mfr Part Number columns.

Page 8-65, Figure 8-24, W5J1 Wiring Diagram:
On W5J1, delete yellow wire from pin 4.
On W5J1, delete blue wire from pin 6.

Page 6-26, Table 6-2, Mechanical Parts:
Delete MP47*, this was not supplied for instruments prefixed 1520 and below.

CHANGE 7 (1516A)

Page 6-15, Table 6-1, A9 Parts List:
Change series number of A9 to 1516A.

Page 6-18, Table 6-1, A9 Parts List:
Delete A9R114, A9R115, and A9R116.

Page 8-12, A9 Schematic Diagram:
Change series number at top of schematic to 1516A.
On component locator, delete A9R114, A9R115, and A9R116.
On schematic, replace A9R114, A9R115, and A9R116 with straight-through connections.

CHANGE 8 (1512A)

Page 6-6, Table 6-1, A3 Parts List:

Change A3C9 and A3C11 to 0160-4058, Capacitor-Fxd 39pF ±5% 400WVDC CER, 28480, 0160-4058.

Add A3C27; 0160-3879; Capacitor-Fxd 0.01μF ±20% 100WVDC CER; 28480; 0160-3879.

Change A3Q1 and A3Q2 to 1855-0050 in HP and Mfr Part number columns.

Change A3R38 and A3R40 from 0683-1635 (16KΩ) to 0683-1025; Resistor-Fxd 1000 ohm, 5% .25W FCTC=-400/+600; 01121, CB1025.

Change board series number to 1512A.

CHANGE 9 (1440A)

If the serial number of your instrument is between 1428A00451 and 1440A00950 and is not equipped with Option 001 make the changes in Table A. If your instrument is equipped with Option 001 and has a serial number between 1428A00451 and 1440A00950, make the changes given in Table B.

Table A. Changes for Standard Instrument (Serial Numbers 1428A00451 through 1440A00950)

Page 3-14, Figure 3-11, Rear Panel Controls and Connectors:

Delete FREQUENCY STANDARD INT-EXT switch and description.

Page 6-12, Table 6-1, A8 Parts List:

Change part number of A8 to 05345-60008 in HP amd Mrf part number columns.

Change A8C22 and A8C23 to 0140-0202, Capacitor-Fxd 15pF ±5% 500WVDC Mica, 72136 DM15C150J0500WV1CR.

Delete A8C83 and A8C84, A8CR21, A8CR22, A8Q22, and A8R107.

Page 6-24, Table 6-1, Chassis Parts:

Delete C6 and S9.

Change Figure 8-11, A8 Schematic Diagram as shown in the partial schematic in Figure 7-8. Replace A8 component locator with Figure 7-9.

Page 8-57, Figure 8-20, Motherboard Wiring:

Delete S9 and C6. Indicate that J1 connects directly to W8 (05345-60078).

Table B. Changes for Instruments Equipped with Option 001
(Serial Numbers 1428A00451 through 1440A00950)

Page 6-27, Table 6-3, Option 001 Parts:

Add A20 05345-60032, Int-Ext Freq Std Switch Assy, 28480, 05345-60032.

Add A20C1 0160-2055, Capacitor Fxd .01μFD 100V, 28480, 0160-2055.

Add A20S1 3101-0957, Switch, 28480, 3101-0957.

Add A20J1 1250-0829, Connector Coax RF, 28480, 1250-0829.

Add A20MP1 05345-00030, Plate Freq Std, 28480, 05345-00030.

Add A20MP2 05345-00031, Bracket-Connector, 28480, 05345-00031.

Add A20W1 05345-60078, Cable-Coax, 28480, 05345-60078.

Page 8-39, Figure 8-11, A8 PLL Multiplier Noise Generator Assembly:

Replace wiring of J1, S9, C6, and W8 with A20 circuitry as shown in Figure 7-10.

Page 6-12, Table 6-1, (Chassis Parts):

Delete S9 and C6.

Page 6-6, Table 6-1, A3 Parts List:

Change A3R14 and A3R16 to 0698-5174, Resistor 200 OHM 5% 1/8W CC Tubular, 01121, BB2015.

Change A3R19, A3R20, A3R28, and A3R29 to 0698-7964, Resistor 100K 5% 1/8W CC Tubular, 01121, BB1045.

Change A3R38 and A3R40 to 0757-0911, Resistor 300 OHM 2% 1/8W F Tubular, 24546, C4-1/8-TO-301-G.

Change A3R43 and A3R46 to 0675-1021, Resistor 1K 10% 1/8W CC Tubular, BB1021.

Change A4R45 to 0683-1025, Resistor 1K 5% 1/4W CC Tubular, 01121, CB1025.

Change A3R48 to 0675-1021, Resistor 1K 10% .125W CC Tubular, 01121, BB1021.

CHANGE 9 Cont'd.

Page 8-31, Figure 8-8, A3 Schematic Diagram:
Change the following resistor values:
A3R14, R16 to 200 OHMS.
A3R19, R20, R28, R29 to 100K.
A3R33, R40 to 300 OHMS.
A3R43, R46 to 1000 OHMS.
A3R45, R48 to 1000 OHMS.
Change A3 Series Number at top of Schematic to 1428A.

Page 6-8, Table 6-1, A4 Parts List:
Change A4R12, R14 to 0698-7178, Resistor-Fxd 2M OHM 5% 1/8W CC Tubular, 01121, BB2055.
Change A4R11, R13 to 2100-1738, Resistor-Var Trimmer 10K OHM 10% C, 19701, ET50W103.
Change A4R2, R5 to 2100-2061, Resistor-Var 200 OHM 10% C, 30983, ET50W201.

Page 8-31, Figure 8-8, A4 Schematic Diagram:
Change A4R2, R5 to 200 OHMS.
Change A4R12, R14 to 2M OHMS.
Change Series Number at top of Schematic to 1440A.

CHANGE 10 (1438A)

Page 6-8, Table 6-1 (A4 Parts List):
Change A4U1, U2 to 1826-0151.
Change Series number of board to 1340A.

Page 6-10, Table 6-1 (A7 Parts List):
Change A7C5 to 0160-0161, C:Fxd 0.01μ ±10% 200WVDC Polyester, 56289, 292P10392.
Change series number of board to 1436A.

Page 6-24, Table 6-1 (Chassis Parts):
Change FL1 to 5060-1189.
Change T1 to 9100-3037.
Change C3 to 0160-3043, Dual 5000PF ±20%, 28480, 0160-3043.
Delete C4.
Change W4 to 05345-60074.
Change W14 to 05345-60084.

Page 8-65, Figure 8-24 (Wiring Power Transformer):
Replace Power Wiring with **Figure 7-11.**

Page 2-1:
Delete illustration for pc board selector. Instruments with series prefix 1438A and below have a screwdriver-operated line voltage selector. Fuses are 2.5A for 115V operation or 1.25A for 230V operation.

CHANGE 11 (1436A)

Page 6-15, Table 6-1 (A9 Parts List):
Delete A9R112 and A9R113.
Change board series number to 1428A.

Page 8-41, Figure 8-12 (A9 Schematic Diagram):
Delete A9R112 and A9R113.

CHANGE 12 (1428A)

Page 6-10, Table 6-1 (A7 Parts List):
Replace A7 parts list with Table 7-5.

Page 6-18, Table 6-1 (A10 Parts List):
Change A10R45 and A10R46 to 0757-0440, Resistor Fxd 7.5K 1% 1/8W F Tubular, 24546, C4-1/8-TO-7501-F.

Page 8-35, Figure 8-10 (A7 Schematic Diagram):
Replace A7 schematic Diagram with Figure 7-12.
Replace A7 component locator with Figure 7-13.

Page 8-43, Figure 8-13 (A10 Schematic Diagram):
Change A10R45 to 7500 OHMS.
Change A10R46 to 2610 OHMS.

CHANGE 13 (1424A)

Page 6-6, Table 6-1 (A3 Parts List):
Change A3R10 and A3R12 to 0683-5625, Resistor Fxd 5.6K 5% 1/4W CC Tubular, 01121, CB2025.
Change A3 Series number to 1340A.

Page 6-15, Table 6-1 (A9 Parts List):
Delete A9R111.

Page 8-31, Figure 8-8 (A3 Schematic Diagram):
Change A3R10 and A3R12 to 5600 OHMS.
Change A3 series number to 1340A.

Page 8-41, Figure 8-12 (A9 Schematic Diagram):
Delete A9R111.
Change A9 series number to 1412A.

Page 1-4, Table 1-3 (Specifications):
Change specifications under INPUT CHANNELS A AND B

Sensitivity: X1, 10 mV rms sine wave and 30 mV peak-to-peak pulse. X20, 200 mV rms and 600 mV peak-to-peak pulse.

Dynamic Range: 30 dB
50Ω: X1, 10 mV to 350 mV rms sine wave and 30 mV to 1.0V peak-to-peak pulse. X20, 0.2 to 7.0V rms sine wave and 0.6V to 14V peak-to-peak pulse.

1 MΩ: X1, 10 mV to 350 mV rms sine wave and 30 mV to 1.0V peak-to-peak pulse. X20, 0.2 to 7.0V rms sine wave and 0.6V to 20V peak-to-peak pulse.

Delete linear operating range specification.

Trigger Level: Continuously adjustable to more than cover the DYNAMIC RANGE (±0.5 Vdc times the attenuator setting). Adjustment is nonlinear with more settability in the more sensitive region.

Page 1-5, Table 1-3:
Change specifications under INPUT CHANNELS A AND B.

Output: CHAN A and B trigger voltage (X ATTEN) is accurate to within ±15 mV (X ATTEN) of actual trigger point. Rear panel BNC connectors.

Under COMMON INPUT
Change to Sensitivity: (Preset)
50Ω: X1, 20 mV rms sine wave and 60 mV peak-to-peak pulse. X20, 400 mV rms sine wave and 1.2V peak-to-peak pulse.

Trigger Level: Continuously adjustable over the range of ±1 Vdc in 50Ω and 1 MΩ multiplied by the attenuator setting.

Page 3-1, Paragraph 3-8:
In first sentence, "change minimum level of 20 mV rms" to **10 mV** rms sine wave.

CHANGE 13 Cont'd.

Page 3-4, Paragraph 3-35:
In first sentence, change triggering range to **-0.5V to +0.5V.**

Page 3-13, Item 8:
Change level range in X1 setting to ±**0.5V.**
Change level range in X20 setting to ±**10V.**

Page 3-14, Item 3 and Item 4:
Change level control OUTPUT to ±**0.5V**.

Page 4-12, Paragraph 4-87:
In sixth sentence (6th line) change to read "accepts the dc level (±**0.5V**). . .".

Page 5-42, Step 1, Specifications:
Change sensitivity to **10 mV** rms.

Page 5-42, Step 1b:
Change to read, "Adjust signal generator from 20 Hz to 500 MHz", maintaining **10 mV** rms input amplitude.

Page 5-42, Step 2, Specifications:
Change Level Range to ±**0.5V**.
Change ATTEN (Sensitivity): to **200 mV** rms in X20.

Page 5-42, Step 2b:
Change to read "set signal generator to 10 kHz at **1V** rms".

Page 5-42, Step 2c:
Change 2nd sentence to read "dc voltmeter reading should vary from **-.5V** to **+.5V** with 0V at PRESET position".

Page 5-43, Step 2f:
Change 2nd sentence to read "OUTPUT level meter should read **200 mV** or less".

Page 5-43, Step 3, Specifications:
Change sensitivity spec to **60 mV** p-p.

Page 5-43, Step 3c:
Change pulse generator output to "10 ns pulses at **60 mV** p-p, ... ".

Page 5-44, Step 4, Specifications:
Change sensitivity spec to **10 mV** rms.

Page 5-44, Step 4b:
Change to read "set signal generator to 20 Hz at **20 mV** ... ".

Page 5-44, Step 4c:
In first sentence, change 40 mV to **20 mV**.

Page 5-45, Step 5, Specifications:
Change Level Range to ±0.5V
Change ATTEN (sensitivity) to **200 mV** rms in X20.

Page 5-45, Step 5b:
Change 1V rms to **1.5V** rms.

Page 5-45, Step 5d:
Change -1.3 to +1.3V to **-.5V to +.5V**.

Page 5-45, Step 5g:
Change 2nd sentence to read; "output level meter should read **200 mV** or less".

Page 5-50a, Performance Test Card:
Change Channel A and Channel B level spec to ±**0.5V**.
Change Channel A and Channel B Atten Sensitivity spec to **200 mV**.
Change time interval single shot time interval spec to 10 ns at **60 mV** p-p.

CHANGE 14 (1412A)

Page 6-9, Table 6-1 (A6 Parts List):
Change A6CR19 to 1902-3036.
Change series number to 1412A.

Page 8-33, Figure 8-9 (A6 Schematic Diagram):
Change A6CR19 to 3.16V.

CHANGE 15 (1352A)

Page 6-5, Table 6-1 (A1 Parts List):
Change A1DS1-12 to 1990-0452.
Change board series number to 1352A.

Page 6-9, Table 6-1 (A6 Parts List):
Change A6R4 to 0683-2035 Resistor, Fxd 20K 5% 1/4W CC Tubular, 01121, CB2035.

Page 8-33, Figure 8-9 (A6 Schematic Diagram):
Change A6R4 to 20K ohms.
Change board series to 1352A.

Page 6-15, Table 6-1 (A9 Parts List):
Delete A9R110.
Change A9R106 through A9R109 to 0698-3378, Resistor Fxd 51 Ohms 5% 1/4W, 01121, BB5105.
Change board series to 1352A.

Page 8-41, Figure 8-12 (A9 Schematic Diagram):
Delete A9R110.
Change A9R106 through R109 to 51 ohms.
Change board series to 1352A.
Replace component locator with **Figure 7-14.**

Page 6-19, Table 6-1 (A10 Parts List):
Change A10R51 to 0683-4715, Resistor Fxd 470 ohm 5% 1/4W CC Tubular, 01121,CB4715.
Change board series to 1340A.

Page 8-43, Figure 8-13 (A10 Schematic Diagram):
Change A10R51 to 470 Ohms.
Change baord series number to 1340A.

Page 6-24, Table 6-1 (Chassis Parts):
Delete R2 12K resistor.

Page 8-27, Figure 8-6 (Chassis Parts):
Delete R2.

Page 8-35, Figure 8-10 (A7 Schematic):
Delete top lead connection of A7R16 and connect it to junction of A7L1 and A7C9.
Change board series to 1340A.

CHANGE 16 (1340A)

Page 6-5, Table 6-1 (A1 Parts List):
Change A1R3 to 0683-1515, Resistor Fxd 150 ohm 5% 1/4W CC Tubular, 01121, CB1515.
Change board series number to 1340A.

Page 8-29, Figure 8-7 (A1 Schematic Diagram):
Change A1R3 to 150 ohms and board series number to 1340A.

Page 6-5, Table 6-1 and Page 8-29, Figure 8-7, (A2 Parts List and Schematic Diagram):
Change part number of A2 to 05345-60002, Series 1340A.

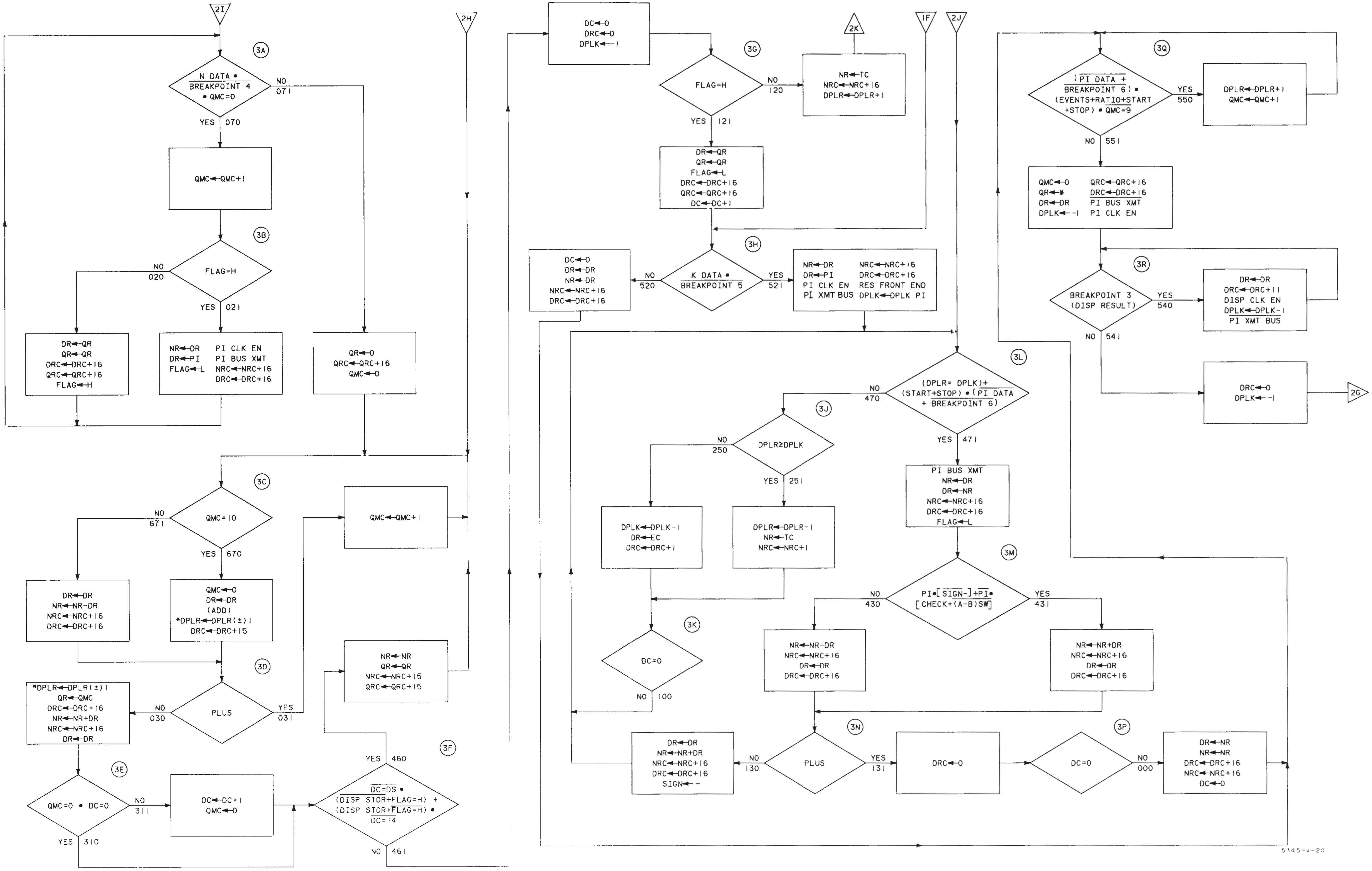
Page 6-9, Table 6-1 (A6 Parts List):
Change A6Q2 to 1853-0326.
Change A2 series number to 1340A.

Page 6-15, Table 6-1 and Page 8-41, Figure 8-12 (A9 Parts List and Schematic Diagram):
Delete A9R106 through A9R109.
Change A9 series number to 1340A.

Page 6-20, Table 6-1 and Page 8-45, Figure 8-14 (A11 Parts List and schematic diagram):
Delete A11Q9, Q10, R26, R27. On schematic, indicate a direct connection from U17 pin 6 to U16 pin 14. Also indicate a direct connection from U18 pin 6 to U19 pin 4.
Change A11 board series number to 1340A.

Page 6-22, Table 6-1 and Page 8-55, Figure 8-19 (A15 Parts List and Schematic Diagram):
Add A15R7, 0683-1325, 1300 Ohm 5% 1/4W CC Tubular, 01121, CB1325. On schematic, indicate resistor R7 in place of jumper A.
Change A2 assembly number to 1340A.

Page 6-24, Table 6-1 and Page 8-27, Figure 8-6 (Chassis Parts and Front Panel Switch Wiring):
Delete C4, insulator 0340-0797 and screw 0570-0130.



* SEE NOTE 1 ON TABLE 5-4

Figure 7-1. Processor Flowchart, Sheet 3, Series 1644A and Below

Table 7-2. Command Source Listing

COMMAND SOURCE		A1	A15 U10 3	A15 TP1	A1	A1 A̅T̅	A15 U3	A15 U15 14	A B̅T̅	A B̅T̅	A15 B̅T̅	A15 B̅6̅	A15 B̅	A B	A15 B16	A15 A12	A1 A̅	A	A15 A̅8̅	A15 A̅9̅	A15 4 1	A15 A1	A15 U2 5	A15 U2 1	A B	A1	A15 A1	A15 A̅7̅	A1 B̅7̅	A1 B8	A15 A̅6̅	A14 A̅1̅2̅	A B1	A15 A	A15 A̅1̅5̅	A15 A14	A1 A	A A̅	A15 U1 9	A1 U10 13	A14	A14	A14 U2 5	A14 U3 10	A14 1	A14	A15 A̅1̅0̅	A15 U12
MSB		0	0	0	0	1	0	1	1		0	1	0	0	0	0	1		0	1	1	1	0	0	0	0	0	0	0		1	1	1		0	0	0	1	0	0			1	1		1	0	0
PULSED COMMAND		P	P				P	P		P	P	P	P		P	P							P	P	P	P										P	P		P	P								P
LETTER CODES	ADDRESSES / COMMANDS	• ON	•←OFF	1 PULSE CNT	DSP SECNT	ADD	DC←0	DC CLK	DISP CLK EN	DFLK CK	DPLK←DPLK PI	DPLK←1	DPLR CK	DPLR UP	DPLR←1	DRC←0	DR CLK EN	DR EN A	DR EN B	DR EN C	DS·DC	EXT O TEN	FLAG←H	FLAG←L	LOAD MS	LOAD * STORAGE	NR CLK EN	NR EN A	NR EN B	PROC B SY	PI CLK EN	QR EN A PI XMT	QR EN B	QR EN C	QR EN CLK	QMC←0	QMC CLK	RST FRONT END	SIGN←	SIGN←+	SV1 T+1	SV2 T+1	SV3 (T+1)	SV4 (T+1)	SV5 T+1	SV6 T+1	FLAG H	RST PULSE CNT
SHT 3P	000	H	H	H		H	H	L	L	H	H	H	H		H	H	H	H	L	H	H	H	H	H	H	H	H	L	H	L	H	H	L	H	H	H	H	L	H	H	H	L	H	H	L	H	L	H
RESET	001	H	H	L		H	H	L	H	L	H	H	H	H	L	H	H	L	H	L	L	H	L	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L		H	L	L	L	H	L
SHT 2BB	010	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L		H	H	H	H	H	H	L	H	L	H	L	H	L	H	H	H	H	H	H	H	H	L	L	H	L	H	H
SHT 2BB	011	H	H	L	H	H	L	L		L	H	H	H		H	H		H	L	L	L	H	H	H	H	H	H	L	H	L	H	L	L	H	H	H	H	H	H	H	H	H	L	L	H		H	H
SHT 3B	020	H	H	H	L	H	L	L	L	L	H	H	H	L	H	H	H	L	L	H		H	L	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H	L		L	H	H	H	H	H
SHT 3B	021	H	H	H	L	H	L	L		H	H	L	H	H	H	H	H	H	H	H	L	H	H	L	H	H	H	L	L	L	L	L	L	H	L	H	H	L	H	H	L	L	L	H	H	H	L	H
SHT 3D	030	H	H	H	L	H	L	L		H	H	H	L	*	H	H	H	H	H	L		H	H	H	H	H	H	H	L	L	H	H	L	L	L	H	H	L	H	H		H	H	L	L	H	*	H
SHT 3D	031	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	L	L	H	H	H	H	L	H	H	H	*	H
SHT 4I	040	H	H	L	H	H	L	L		H	H	L	H		H	H	L	L	L	L		L	H	H	H	H	L	L	H	H	H	L	H	H	L	H	H	L	H	H	L		L	H	L	L	H	H
SHT 4I	041	H	H	L	H	H	L	H		H	H	L	H	H	H	H	L	L	L	L	L	L	H	L	H	H	L	L	H	H	H	H	H	H	L	H	H	L	H	H	H	H	H	H	H	L	L	H
SHT 2I	050	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	L	H	L	L	H	H	H	H	H	H	L	H	L	H	L	H	L	H	H	H	L	H	H	H	H	L	H	H	H	H	H
SHT 2I	051	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	H	L	H	L	H	H	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	L	H	L	L	L	H	L	H	H
SHT 4H	060	H	H	L	H	H	L	L	L	H	H	L	H	H	H	H	L	L	L	L	L	L	H	L	H	H	L	L	H	H	H	L	H	H	L	H	H	L	H	H		L	L	H	H	L	L	H
SHT 4H	061	H	H	L	H	H	L	L	L	H	H	L	H	H	H	H	L	L	L	L	L	L	L	H	H	H	L	L	H	H	H	L	H	H	L	H	H	L	H	H	L	L	L	H	L		H	H
SHT 3A	070	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	L	L	H	H	L	L	L	L	H		*	H
SHT 3A	071	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	L	H	L	L	H	H	H	H	H	H	L	H	L	H	L	H	L	H	L	H	L	H	H	H	H	L	H	H	H	*	H
SHT 3K	100	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	L	L	H	H	H	L	H
SHT 1A	101	H	H	H		H	L	L	L	H	H	H	L	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	L	H	H	H	L	H	H	H	H
SHT 4F	110	H	H	L	L	H	L	L	L	H	H	H	H		L	H	L	L	L	L	L	L	H	H	H	H	L	H	L	H	H	H	H	H	L	H	H	L	H	H	L	H	H	H	L	H	H	H
SHT 4F	111	H	H	H	H	H	L	L		L	H	H	L	L	H	H	H		H	L	L	L	H	H	H	H	L	L	H	H	H	H	H	H	L	H	H	L	H	H	L	H	H	H	L	H	H	H
SHT 3C	120	H	H	H	L	H	L	L	L	H	H	H	L	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	L	H	L	L	H	H	H	H	L	H	L	H	L	L	H	L	H	L	H
SHT 3G	121	H	H	H	L	H	L	H	L	H	H	L	H		H	H	H	L	L	H	L	H	H	L	H	H	H	L	H	L	H	H	H	H	H	H	H	L	H	H	H	L	H	L	H	L	L	H
SHT 3N	130	H	H	H	L	H	L	L	L	H	H	H	H		H	H	H	L	H	L	L	H	H	H	H	H	H	H	L	L	H	L	H	H	L	H	H	L	L	H	H	L	L	H	H	H	L	H
SHT 3N	131	H	H	L	H	H	L	L	L	H	H	H	H		H	L	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	L	L	L	.	L	L	H
SHT 4E	140	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	L	L	H	H
SHT 4E	141	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	L	L	H	H	H
SHT 1H	150	H	H	H	L	H	L	L	L	H	L	H	H		H	H	H	H	H	H	L	H	H	H	H	H	H	H	L	L	L	L	H	H	L	H	H	L	H	L	L	H	L	L	H	H	L	H
SHT 1H	151	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	H	L	H	L	H	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	L	H	L	L	H	H	H	H	L	H	H
SHT 4D	160	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	H	L	L	H
SHT 4D	161	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	L	L	H	H
SHT 1L	170	H	H	H	L	H	L	L	L	H	H	L	H		H	H	H	H	H	H	L	H	L	H	H	H	H	L	L	L	L	L	L	H	L	H	H	L	H	H	H	L	L	H	L	L	H	H
SHT 1L	171	H	H	L	H	H	L	H	L	H	H	L	L	L	H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	H	H	H	L	H	H	L	H	H	H	L	H	L	H	L	L	H
SHT 2K	200	H	H	L	H	H	L	H	L	H	H	L	L	L	H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	L	L	H	H	H	H	H
SHT 2K	201	H	H	L	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H		L	L	H	H	H	H	H
SHT 1D	210	H	L	H	L	H	L	L	L	H	H	H	H		H	H	H	L	H	H	L	H	H	L	H	H	H	H	H	L	H	L	H	H	H	H	H	L	H	H	L	H	H	L	L	L	L	H
SHT 1D	211	H	L	H	L	H	L	L	L	H	H	H	H		H	H	H	H	H	L	L	H	H	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	L	H	H	L	H	L	H
SHT 2D	220	H	L	L	H	H	L	H	L	H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	L	L	H	L	H	H	H
SHT 2D	221	H	L	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	H	L	L	H	L	H	L	H
SHT 1K	230	H	L	L	H	H	L	L	L	H	H	L	L	H	H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	H	H	H	L	L	H	L	H	H	L	L	H	H	H	H	L	H
SHT 1K	231	H	L	H	H	H	L	L	L	H	H	H	L	L	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	L	H	H	L	H	H	L	H	H	L	H	L	L	H	H	L	H
SHT 2M	240	H	L	H	H	H	L	L	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	L	H
SHT 2M	241	H	L	H	H	H	L	L	L	H	H	H	L	L	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	L	H	H	L	H	H	H	H	H	L	H	L	H	L	L	L	H
SHT 3	250	H	L	L	H	H	L	L	L	L	H	H	H		H	H	H	L	H	H	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	L		H	L	L	L	L	H
SHT 3	251	H	L	L	H	H	L	L	L	H	H	H	L	H	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	L	H	H	L	H	H	L	L	H	L	L	L	L	H
SHT 2Z	260	H	L	L	H	H	L	L	L	H	H	L	L	H	H	H	L	L	L	L	L	H	H	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	L	L	L	H	H	H
SHT 2Z	261	H	L	H	H	H	L	L	L	H	H	H	L	L	H	H	L	H	L	L	L	H	H	H	H	H	L	L	H	L	H	L	L	H	L	H	H	H	H	H	H	H	L	L	H	L	H	H
SHT 2R	270	H	L	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L		H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	L	H	H	H	H	H	L	L	H	H	H
SHT 2R	271	H	L	H	H	H	L	H	L	H	H	H	H		H	H	L	L	L	L	H	H	H	H	H	H	H	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	L	H	H	H	H	H
SHT 1D	300	H	H	H	L	H	L	L	L	H	H	L	H		H	H	L	H	L	H	L	H	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	L	L	H	H	L	H	L	L	H
SHT 1D	301	H	H	H		H	L	L	L	H	H	L	H		L	H	L	H	L	L	L	L	H	H	H	H	L	L	H	L	H	H	L	H	H	H	H	L	H	H	H	H	H	L	L	L	L	H
SHT 3E	310	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	H	H	L	H	L	H		L	H	H	L	*	H
SHT 3E	311	H	H	H	H	H	L	H	L	H	H	L	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	L	H	L	H	H	H	L	L	H	H	L	*	H
SHT 1D	320	H	H	L	L	H	L	L	L	H	H	L	H	H	L	H	L	H	L	L	L	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H		H	H	H	H	L	H
SHT 1D	321	H	H	L	L	H	L	L	L	H	H	L	H	H	L	H	L	H	L	L	L	H	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	L	H	H	H	H	L	H
SHT 1G	330	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	H	L	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H		H	H	L	H	H	L	H	H	H	H
SHT 1G	331	H	H	L	H	H	L	L	L	H	H	H	H		H	H	H	H	L	H	H	L	H	L	H	H	H	L	H	L	H	H	L	H	L	H	H		H	H	H	H	H	L	L	L	L	H
SHT 2J	340	H	H	L	H	H	L	L	H	L	H	H	H		H	H	H	L	H	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	L	L	H	H	L	H	H	H	L	L	*	H
SHT 2J	341	H	H	L	H	H	L	L		L	H	H	H		H	L	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	L	L	H	L	H	H	L	H	L	L	L	L	*	H
SHT 4G	350	H	H	L	H	H	L	H	L	H	H	L	L	L	H	H	L	L	L	L	L	L	H	H	H	H	L	L	H	H	H	L	H	H	L	H	H	L	H	H	L	L	L	H	H	L	H	H
SHT 4G	351	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	H	L	L	H
SHT 1J	360	H	H	L	H	H	L	L	H	L	H	H	L	H	H	H	H	L	H	L	L	H	H	H	H	H	L	L	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	H	H	L	H	H
SHT 1J	361	H	H	L	L	H	L	L		H	H	L	H		L	L	L	L	L	L	L	H	H	H	H	H	L	L	H	L	H	L	H	H	H	L	H	L	H	H	H	L	L	H	L	L	H	H
SHT 4C	370	H	H	L	H	H	L	L	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H
SHT 4C	371	H	H	L	H	H	L	H	L	H	H	H	H		H	H	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	L	L	H	H	H	L	L	H

NOTE
* NORMALLY H L WITH N' DATA ROUTINE
BLANK LOCATIONS DON'T CARE STATES
BOLD LETTERS ACTIVE STATES.

Table 7-3. Command Source Listing

LETTER CODES	ADDRESSES	* ON	* ← OFF	T PULSE CNT	T5 PULSE CNT	ADD	DC 0	DC CLK	DSP CLK EN	DPLK CLK	DPLK – DPLK PI	DPLK ← 1	DPLR CLK	DPLR P	DPLR 1	DRC · 0	DR CLK EN	DR EN A	DR EN B	DR EN C	DS DC	EXT OUT EN	FLAG · H	FLAG L	LOAD MS	LOAD • STORAGE	NR CLK EN	NR EN A	NR EN B	PROC B SY	PL CLK EN	QR EN A PI XMT	QR EN B	QR EN C	QR EN CLK	QMC 0	QMC CLK	RS TRON SD	SIGN	SIGN ·	SV1 1 1	SV2 1 1	SV3(T-1)	SV4(T-1)	SV5 1	SV6 1 1	* FLAG H	RST PULSE CNT
COMMAND SOURCE		A15-U10 6	A15-U10 3	A15-TP1	A15 U15 5	A15 A11	A15-U35 2	A15 U35-14	A15 B9	A15 B18	A15-B17	A15-B6	A15 B15	A15 B	A15 B16	A15-A12	A15 [illegible]	A15 B	A15 A8	A15-A9	A15 34 4	A15 A9	A15 U25	A15 U21	A15 B5	A15 U5 11	A15 A12	A15 A7	A15 B1	A15 B6	A15 A6	A14 A12	A15 B1	A15 A1	A15-A15	A15 A14	A15 A5	A15 A20	A15 U10 9	A15 U10-13	A14 U23 2	A14 3	A14-U23 5	A14-U23-10	A14 U23 12	A15 U23 15	A15 A10	A15-U12-2
MSB		0	0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	1	1	1			0	1			0	0			1	1	1		1	0
PULSED COMMANDS		P	P				P	P		P	P	P	P		P	P							P	P	P	P										P	P		P	P								P
SHT 2C	400	H	H	**L**	**H**	**H**	L	**H**	L	H	**H**	H	H		H	H	L	L	L	L	**H**	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	**L**		H	H	**H**	L	L	**H**			*	H
SHT 2C	401	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L		L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	**L**	**H**	**H**	L	H	**L**		H	H	**H**	L	L	**H**	L		H	H
SHT 2Q	410	H	H	**L**	**H**	**H**	L	L	L	H	H	**H**	H		H	H		L	L	L	**H**	H	H	H	H	H	**H**	**H**	**H**	**L**	H	L	**H**	**H**		H	H		H	H	**H**	**H**	L	**H**			H	H
SHT 2Q	411	H	H	H	**H**	**H**	L	L	L	H	H	H	H		H	H			L	L	**H**	H	H	H	**L**	H	**H**	**H**	**H**	L	H	L	**H**	**H**	L	H	H		H	H	**H**	**H**	L	**H**	L	L	H	H
SHT 2G	420	H	H	**H**	L	**H**	L	L	L	H	H	H	H		H	H	**H**	L	**H**	**H**		H	H	H	H	H	**H**	**H**		L	H	H	**H**	**H**	L	H	H		H	H	**H**	L	**H**	L	**H**	**H**	*	H
SHT 2G	421	H	H	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**		**H**	**H**	L		H	H	L	H	**H**	L	**H**	L	H	H	**H**	H	**H**	H	L		L	H		**H**	**H**	**H**			*	H
SHT 3M	430	H	H	H	L	L	L	L	L	H	H	H	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	**H**	**H**		**L**	H	H	**H**	**H**	L	H	H		H	H	L	L	**H**	L	**H**	**H**	L	H
SHT 3M	431	H	H	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	L	**H**	L	L	H	H	H	L	H	**H**	**H**	L	**L**	H	H	**H**	**H**	L	H	H		H	H			**H**	L	**H**	**H**	L	H
SHT 2A	440	H	H	H	**H**	**H**	L	L	L	**L**	H	H	H		H	H	L		L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	**H**	**H**	**H**	H	H	L	H	H	**H**	**H**	L	L		L	*	H
SHT 2A	441	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L		H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	**L**	H		H	H		**H**	L	L	**H**	L	*	H
SHT 2E	450	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L		L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	**H**	**H**	L	H	H		H	H	**H**	L	**H**	**H**	**H**	L	L	H
SHT 2E	451	H	H	**L**	**H**	**H**	**H**	L	L	H	H	H	H		H	H	L	L	L	L		H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	L	H	H	L	L	L	**H**		**H**	*	H
SHT 3F	460	H	H	**H**	**H**	**H**	L	L	L	**L**	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	**H**	**H**	**H**	H	H	L	H	**L**	**H**	**H**	L	**H**	**H**	**H**	*	H
SHT 3F	461	H	H	**L**	L	**H**	**H**	L	L	H	H	**L**	H		H	**L**	L	L	L	L	L	H	H	H	H	H	**H**	L	L	**L**	H	H	**H**	**H**	L	H	H		H	H		L	**H**	L	**H**	L	*	H
SHT 3L	470	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H		L	L	L	**H**	H	H	**L**	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H		H	H	L	**H**	L	**H**		**H**	L	H
SHT 3L	471	H	H	**H**	L	**H**	L	L	L	H	H	H	H		H	H	**H**	**H**	L	**H**	**H**	H	H	**L**	H	H	**H**	L	L	**L**	H	L	L	**H**	L	H	H		H	H	**H**		L	L	**H**	**H**	L	H
SHT 2P	500	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H		H	H		**H**	L	**H**	**H**	**H**	H	H
SHT 2P	501	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H		L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	L	H	H	**H**	L	L	L	L	**H**	H	H
SHT 2N	510	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	**H**	**H**	**L**	H	H	**H**	**H**	L	H	H	L	H	H	**H**	L	**H**	L	L	L	H	H
SHT 2N	511	H	H	**L**	L	**H**	L	L	L	H	H	H	H		**L**	H	**H**	**H**	**H**	**H**	**H**	H	H	H	H	H	L	**H**	**H**	**L**	H	H	L	**H**	**H**	H	H	**H**	H	H	L	L	**H**	L		L	H	H
SHT 3H	520	H	H	H	L	**H**	**H**	L	L	H	H	H	H		H	H	**H**		**H**	L	**H**	H	H	H	H	H	**H**	L	L	**L**	H	H	**H**	**H**	L	H	H		H	H	**H**	L	**H**	**H**	L	**H**	L	H
SHT 3H	521	H	H	H	L	**H**	L	L	L	H	**L**	H	H		H	H	**H**	**H**	**H**	**H**	**H**	H	H	H	H	H	**H**	L	**H**	L	**L**	L		**H**	L	H	H	**H**	H	H	**H**	L	L	**H**	**H**	**H**	L	H
SHT 2H	530	H	H	H	L	**H**	L	L		**L**	H	H	H		H	H	**H**	**H**	L	**H**	L	H	H	H	H	H	**H**	L	L	**L**	H	H	**H**	**H**	L	H	H		H	**L**	L	**H**	**H**	**H**			*	H
SHT 2H	531	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	L	H	H	**H**	**H**	L	H	H	L	H	**L**		**H**	**H**	**H**			*	H
SHT 3R	540	H	H	**L**	**H**	**H**	L	L	**H**	L	H	H	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	**H**	**H**	L	H	H		H	H	**H**	L	**H**	**H**		L	L	H
SHT 3R	541	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	**L**	L		L	L		H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	L	H	H	**H**	L	L	**H**			L	H
SHT 3Q	550	H	H	H	**H**	**H**	L	L		H	H	**L**	**L**	**L**	H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	**H**	**H**	L	H	**L**		H	H	**H**	L	**H**	**H**		**H**	L	H
SHT 3Q	551	H	H	H	L	**H**	L	L	L	H	H	**L**	H		H	H	**H**	**H**	**H**	L	L	H	H	H	H	H	**H**	L	**H**	**L**	**L**	H	L	**H**	**H**	**L**	H	L	H	H	**H**	L	**H**	**H**			L	H
SHT 2L	560	H	H	H	L	**H**	L	L	L	H	**L**	H	H		**L**	H	**H**	**H**	**H**	**H**	L	H	H	H	H	H	L	**H**	L	**L**	**L**	L	**H**	**H**	L	H	H	**H**	H	**L**	L	**H**	L	**H**	L	L	L	H
SHT 2L	561	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	**L**	H	H	H	L	L	**H**	**L**	H	H	**H**	**H**	L	H	H		H	H	**H**	L	**H**	L	L	**H**	H	H
SHT C	570	H	H	**L**	L	**H**	**H**	L	L	H	H	**L**	H		H	**L**	L	**H**	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	**H**	**H**	H	H	L	H	H		**H**	L	L	L	**H**	*	H
SHT 1C	571	H	H	**L**	**H**	**H**	L	L	**H**	**L**	H	H	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	H	H	H	**H**	**H**	**H**	H	H		H	H	**H**	L	**H**	**H**	**H**	**H**	*	H
SHT 2B	600	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H		L	L	L	**H**	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	L	H	H	**H**		L	**H**			*	H
SHT B	601	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	**H**	L	L	**H**	H	H	H	H	H	L	L	**H**	**L**	H	L	L		L	H	H		H	H	**H**	L	L	L			*	H
SHT 2AA	610	H	H	**L**	**H**	**H**	L	**H**	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	L	H	H	L		L	L		**H**	H	H
SHT 2AA	611	H	H	**L**	**H**	**H**	**H**	L	L	H	H	H	H		H	H		L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	L	H	H	L	L	L	L		**H**	H	H
SHT 2Y	620	H	H	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	L	L	**H**	**H**	H	H	H	H	**L**	**H**	L	**H**	H	H	H	**H**	**H**	**H**	H	H	**H**	H	H	**H**	**H**	**H**	L	**H**	**H**	H	H
SHT 2Y	621	H	H	H	**H**	**H**	L	L	L	**L**	H	H	H		H	H		L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	**H**	**H**	**H**	H	H	L	H	H		**H**	L	**H**	**H**		H	H
SHT 4X	630	H	H	H	**H**	**H**	L	L	L	**L**	H	H	**L**	**L**	H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	H	H	L	**H**	**H**	**H**	H	H		H	H	**H**	**H**	L	L	**H**	**H**	H	H
SHT 4X	631	H	H	**L**	**H**	**H**	L	**H**	L	H	H	H	H		H	H	L	L	L	L		H	H	**L**	H	H	L	**H**	**H**	H	H	H	**H**	**H**	L	H	H		H	H	**H**	**H**	**H**	L	**H**		L	H
SHT 2T	640	H	H	H	**H**	**H**	L	L	L	H	H	**L**	H		H	H		L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	**H**	**H**	**H**	H	H	L	H	H	**H**	**H**	L	**H**		**H**	H	H
SHT 2T	641	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L		L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	**H**	**H**	L	H	H	L	H	H	**H**	**H**	**H**	**H**	L		H	H
SHT 2W	650	H	H	**L**	**H**	**H**	**H**	L	L	**L**	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	**H**	**H**	**H**	H	H	**H**	H	H	**H**	**H**	L	L	**H**	L	H	H
SHT 2W	651	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	**H**		L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H		H	H	**H**	**H**	L	**H**	**H**	L	H	H
SHT 2X	660	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	**L**	**L**	H	H	L	**H**	L	L		H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H		H	H	**H**	**H**		**H**			H	H
SHT 2X	661	**L**	H	**L**	**H**	**H**	L	L	L	H	H	**L**	**L**	**L**	H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**		L	H			H	H	**H**	**H**		**H**			L	H
SHT 3C	670	H	H	H	**H**	**H**	L	L		H	H	**L**	**L**	•	H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	**L**	H		H	H			L	L	**H**	**H**	*	H
SHT 3C	[illegible]	H	H	H		L	L	L	L	H	H	H	H		H	H	**H**	L	**H**	L		H	H	H	H	H	**H**	**H**		**L**	H	L	**H**	**H**	L	H	H		H	**L**			L	L	**H**	**H**	*	H
SHT 1	00	H	H	L	**H**	**H**	L	L	L	H	H	H	H		H	H		L	L	L	**H**	**L**	H	H	H	H	L	L	**H**	L	H	H	**H**	**H**	L	H	H	**H**	H	H	**H**	**H**	**H**	**H**		**H**	L	H
SHT 1I	01	H	H	**L**	**H**	**H**	L	L	L	**L**	H	H	H		H	H	L		L	L		**L**	**L**	H	H	L	L	L	**H**	**L**	H	H	**H**	**H**	L	H	H		H	H		**H**	**H**	L	**H**	**H**	H	H
SHT 2S	0	H	H	H	**H**	**H**	L	L	L	H	H	**L**	H		H	**H**	L	L	L	L	L	H	H	H	**L**	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	L	H	H	**H**	**H**	L	**H**	L	L	H	H
SHT 2S	1	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H			L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	**H**	**H**	L	H	H		H	H	**H**	**H**	**H**	**H**			H	H
SHT 4B	[illegible]	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L		L	L		**L**	H	H	H	H	L	**H**	**H**	H	H	H	**H**	**H**	L	H	H	L	H	H	**H**	**H**	**H**	L	**H**	L		H
SHT 4B		H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	**L**	**L**	H	H	H	L	**H**	**H**	H	H	H	**H**	**H**	L	H	H	L	H	H		**H**	**H**	**H**	**H**	**H**	H	H
SHT 1E	30	H	H	H	**H**	**H**	**H**	L	L	H	H	**L**	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	H	H	L	**H**	**H**	**H**	H	H		H	H	**H**	**H**	L	L	**H**	**H**	H	H
S 1B		H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L		L	L		H	H	H	H	H	L	L	**H**	H	H	H	**H**	**H**	**H**	H		**H**	H	H	**H**	L	**H**	**H**	**H**	**H**	H	H
HT	740		H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H		L	L	**L**	L		H	H		H	L	L	**H**	**L**	H	H	**H**	**H**	L	H	**L**	L	H	H	**H**		**H**	L			H	H
SHT 2U	74	H	H	**L**	**H**	**H**	L	L		**L**	H	H	H		H	H			L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	**H**	**H**	L	H	H		H	H	**H**	**H**	**H**	**H**	**H**	**H**	H	H
SHT 1F	0	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	**L**	H	H	H	H	L		**H**	**L**	H	H	**H**	**H**	L	H	L	L	H	H	**H**	**H**	**H**		L		**L**	H
H 1F	1	H	H	H		**H**	L	L		H	H	**L**	H		**L**	H	**H**			**H**	L	H	H	H	L	H		L	**H**	H	H	H	**H**	**H**	**H**	H	H	**H**	H	**L**	**H**	L	**H**	**H**	**H**	**H**	L	H
SHT 4K	60	H	H	**L**	**H**	**H**		L	L	H	H	**L**	H		H	H			L			**L**	H	H	H	L		L	**H**		H		**H**	**H**	L	H	H		H	H			L	**H**	**H**			H
SHT 4K		H	H	**L**	**H**	**H**	L			H	H	**L**	H		H	H		L		L		H	H	H	H		L		**H**	H	H	H	**H**	**H**	L	H	H		H	H	**H**	L	**H**	**H**	**H**	**H**		H
SHT 2X	0	H	H	**L**	**H**	**H**		L		H	H	H	**L**	H	H	H						H	H	H		H		**H**	**H**	L		H	**H**	**H**		H	L			H	**H**	**H**	**H**	**H**			H	H
SHT X	1			**L**	**H**	**H**	L			L	H	L	**L**	**L**	H	H			L			H	H	H	H		L	L	**H**	**L**	H	L	**H**	**H**	L	H			H	H	**H**	**H**	**H**	**H**			H	H

NOTE
* NORMALLY H [illegible] DATA ROUTINE
BLANK LOCATIONS = DON'T CARE STATES
BOLD LETTERS = ACTIVE STATES.

Table 7-4. Processor Flow Test Results

Delay Switch	ROM Address	Processor Operation	Comment
00039	601	NR=$\overline{0}$, 7th nonzero digit	no
00040	400	Prepare to count 7th digit	yes
00041	440	DPLK=-17	no
00042	601	NR=$\overline{0}$, 8th nonzero digit	no
00043	400	Prepare to count 8th digit	yes
00044	441	DPLK=-17	yes
00045	221	Period or TI	no
00046	451	Flag = H	yes
00047	051	Plug-in	no
00048	420	Events, Ratio and Start or Stop	no
00049	530	Period or TI	no
00050	341	Display Time Count	no
00051	201	Start or Stop	no
00052	071	N Data	no
00053	671	Divide Routine	
00054	030	Divide Routine	
00055	310	Divide Routine	
00056	460	Divide Routine	
00057	671	Divide Routine	
00058	031	Divide Routine	MSB = 1
00059	671	Divide Routine	
00060	030	Divide Routine	
00061	311	Divide Routine	
00062	460	Divide Routine	1st Remainder
00063	671	Divide Routine	
00064	030	Divide Routine	
00065	311	Divide Routine	
00066	460	Divide Routine	2nd Remainder
00067	671	Divide Routine	
00068	030	Divide Routine	
00069	311	Divide Routine	
00070	460	Divide Routine	3rd Remainder
00071	671	Divide Routine	
00072	030	Divide Routine	
00073	311	Divide Routine	
00074	460	Divide Routine	4th Remainder
00075	671	Divide Routine	
00076	030	Divide Routine	
00077	311	Divide Routine	

Table 7-4. Processor Flow Test Results (Continued)

Delay Switch	ROM Address	Processor Operation	Comment
00078	460	Divide Routine	5th Remainder
00079	671	Divide Routine	
00080	030	Divide Routine	
00081	311	Divide Routine	
00082	460	Divide Routine	6th Remainder
00083	671	Divide Routine	
00084	030	Divide Routine	
00085	311	Divide Routine	
00086	460	Divide Routine	7th Remainder
00087	671	Divide Routine	
00088	030	Divide Routine	
00089	311	Divide Routine	
00090	461	End Divide Routine	
00091	121	FLAG=H, LOAD RESULT to QR	yes
00092	520	K Data	no
00093	551	Start and Stop	no
00094	541	Display Result	no
00095	440	States 440 through 441 are repeated for a second time after the arithmetic routine. The purpose of the processor operations will vary during these operations. Consult flow chart theory 2A (440), if needed.	
00096	600		
00097	440		
00098	600		
00099	440		
00100	600		
00101	440		
00102	600		
00103	440		
00104	600		
00105	440		
00106	600		
00107	440		
00108	600		
00109	440		
00110	600		
00111	440		
00112	601		
00113	400		
00114	440		
00115	601		
00116	400		

Table 7-4. Processor Flow Test Results (Continued)

Delay Switch	ROM Address	Processor Operation	Comment
00117	440	Continued	
00118	601	↓	
00119	400		
00120	440		
00121	601		
00122	400		
00123	440		
00124	601		
00125	400		
00126	440		
00127	601		
00128	400		
00129	440		
00130	601		
00131	400		
00132	440		
00133	601		
00134	400		
00135	441	End of Count digits	
00136	221	Period or TI	no
00137	450	FLAG = H	no
00138	561	Display Storage	no
00139	510	DC = 0	no
00140	500	Determine Auto Multiplier	
00141	270	Determine Auto Multiplier	
00142	711	Determine Auto Multiplier	
00143	741	Determine Auto Multiplier	
00144	770	Determine Auto Multiplier	
00145	741	Determine Auto Multiplier	
00146	770	Determine Auto Multiplier	
00147	741	Determine Auto Multiplier	
00148	770	Determine Auto Multiplier	
00149	740	Determine Auto Multiplier	
00150	500	Determine Auto Multiplier	
00151	270	Determine Auto Multiplier	
00152	710	-1≥ DPLR-DS≥3	Mult. Selected
00153	640	Left justify result	
00154	651	Left justify result	
00155	660	Left justify result	

Table 7-4. Processor Flow Test Results (Continued)

Delay Switch	ROM Address	Processor Operation	Comment
00156	640	Left justify result	
00157	651	Left justify result	
00158	660	Left justify result	
00159	640	Left justity result	
00160	651	Left justify result	
00161	660	Left justify result	
00162	640	Left justify result	
00163	651	Left justify result	
00164	660	Left justify result	
00165	640	Left justify result	
00166	651	Left justify result	
00167	660	Left justify result	
00168	640	Left justify result	
00169	651	Left justify result	
00170	660	Left justify result	
00171	640	Left justify result	
00172	651	Left justify result	
00173	660	Left justify result	
00174	640	Left justify result	
00175	651	Left justify result	
00176	660	Left justify result	
00177	640	Left justify result	
00178	650	Left justify result	
00179	621	End of left justify	
00180	260	Auto Right justify	
00181	610	Auto Right justify	
00182	011	Auto Right justify	
00183	621	Auto Right justify	
00184	260	Auto Right justify	
00185	610	Auto Right justify	
00186	011	Auto Right justify	
00187	621	Auto Right justify	
00188	260	Auto Right justify	
00189	610	Auto Right justify	
00190	011	Auto Right justify	
00191	621	Auto Right justify	
00192	260	Auto Right justify	
00193	610	Auto Right justify	
00194	011	Auto Right justify	

Table 7-4. Processor Flow Test Results (Continued)

Delay Switch	ROM Address	Processor Operation	Comment
00195	621	Auto Right justify	
00196	260	Auto Right justify	
00197	610	Auto Right justify	
00198	011	Auto Right justify	
00199	621	Auto Right justify	
00200	260	Auto Right justify	
00201	610	Auto Right justify	
00202	011	Auto Right justify	
00203	621	Auto Right justify	
00204	260	Auto Right justify	
00205	610	Auto Right justify	
00206	011	Auto Right justify	
00207	621	Auto Right justify	
00208	260	Auto Right justify	
00209	610	Auto Right justify	
00210	011	Auto Right justify	
00211	620	Auto Right justify	
00212	731	Serial Output	no
00213	571	End of Test	

Table 7-5. Command Source Listing

COMMAND SOURCE		A15-U10-6	A15-U10-3	A15-TP1	A15-U15-5	A15-A11	A15-U35-2	A15-U35-14	A15-B9	A15-B18	A15-B17	A15-B6	A15-B15	A15-B7	A15-B16	A15-A12	A15-A22	A15-B21	A15-A8	A15-A9	A15-U34-4	A15-A9	A15-U2-5	A15-U2-1	A15-B5	A15-U25-11	A15-A12	A15-A7	A15-B10	A15-B8	A15-A6	A14-A12	A15-B10	A15-A21	A15-A15	A15-A14	A15-A15	A15-A20	A15-U10-9	A15-U10-13	A14-U23-2	A14-U23-7	A14-U23-5	A14-U23-10	A14-U23-12	A14-U23-15	A15-A10
MSB		0	0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	1	1	1	1	1	1	0
PULSED COMMAND		P	P				P	P		P	P	P	P		P	P							P	P	P	P										P	P		P	P							
LETTER CODES	COMMANDS / ADDRESSES	*←ON	*←OFF	T PULSE CNT.	15 PULSE CNT.	ADD	DC←0	DC CLK	DISP CLK EN	DPLK CLK	DPLK←DPLK-PI	DPLK←-1	DPLR CLK	DPLR UP	DPLR←-1	DRC←0	DR CLK EN	DR EN A	DR EN B	DR EN C	DS←DC	EXT OUT EN	FLAG←H	FLAG←L	LOAD MS	LOAD * STORAGE	NR CLK EN	NR EN A	NR EN B	PROC BUSY	PI CLK EN	QR EN A/PI XMT	QR EN B	QR EN C	QR EN CLK	QMC←0	QMC CLK	RST FRONT END	SIGN←-	SIGN←+	SV1 (T+1)	SV2 (T+1)	SV3 (T+1)	SV4 (T+1)	SV5 (T+1)	SV6 (T+1)	FLAG=H
SHT 3P	000	H	H	H	L	**H**	**H**	L	L	H	H	H	H		H	H	**H**	**H**	L	**H**	**H**	H	H	H	H	H	**H**	L	**H**	**L**	H	H	**H**	**H**	**H**	H	H	L	H	H	**H**	L	**H**	**H**	L	**H**	L
RESET	001	H	H	H	L	**H**	**H**	L	**H**	**L**	H	H	H	H	**L**	H	**H**	L	**H**	**H**	L	H	**L**	H	H	H	L	L	**H**	H	H	H	L	**H**	**H**	H	H	**H**	H	H	L	L	**H**	L	L	L	H
SHT 2BB	010	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	L	**H**	H	H	**H**	H	H	**H**	**H**	L	L	**H**	L	H
SHT 2BB	011	H	H	**L**	**H**	**H**	L	L	L	**L**	H	H	H		H	H	L	**H**	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	**H**	**H**	**H**	H	H	**H**	H	H	**H**	**H**	L	L	**H**	L	H
SHT 3B	020	H	H	H	L	**H**	**L**	L	L	**L**	H	H	H	**L**	H	H	**H**	L	L	**H**	L	H	**L**	H	H	H	**H**	L	**H**	**L**	H	L	L	**H**	**H**	H	H	L	H	H	L	L	L	**H**	**H**	**H**	H
SHT 3B	021	H	H	H	L	**H**	L	L	L	H	H	**L**	H	H	H	H	**H**	**H**	**H**	**H**	L	H	H	**L**	H	H	**H**	L	L	**L**	**L**	L	**H**	**H**	L	H	H	L	H	H	L	L	L	**H**	**H**	**H**	L
SHT 3D	030	H	H	H	L	**H**	L	L	L	H	H	H	**L**	*	H	H	**H**	**H**	**H**	L	L	H	H	H	H	H	**H**	**H**	L	**L**	H	H	**H**	L	L	H	H	L	H	H	L	**H**	**H**	L	L	**H**	*
SHT 3D	031	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	**L**	L	H	H	**H**	**H**	L	**H**	**H**	**H**	*
SHT 4J	040	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	**L**	H	H	H	H	L	L	**H**	H	H	L	L	**H**	L	H	H	L	H	H	L	L	L	**H**	L	L	H
SHT 4J	041	H	H	**L**	**H**	**H**	L	**H**	L	H	H	**L**	H	H	H	H	L	L	L	L	L	**L**	H	**L**	H	H	L	L	**H**	H	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	**H**	**H**	L	L
SHT 2F	050	H	H	H	L	**H**	**L**	L	L	H	H	**L**	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	L	**H**	H	H	L	H	H	**H**	**H**	L	**H**	**H**	**H**	H
SHT 2F	051	H	H	H	L	**H**	L	L	L	H	H	**L**	H		H	H	**H**	**H**	L	**H**	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	**H**	**H**	**H**	H	H	L	H	**L**	**H**	L	L	L	**H**	L	H
SHT 4H	060	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H	H	H	H	L	L	L	L	L	**L**	H	**L**	H	H	L	L	**H**	H	H	L	L	**H**	L	H	H	L	H	H	L	L	L	**H**	**H**	L	L
SHT 4H	061	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H	H	H	H	L	L	L	L	L	**L**	**L**	H	H	H	L	L	**H**	H	H	L	L	**H**	L	H	H	L	H	H	L	L	L	**H**	L	L	H
SHT 3A	070	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	**L**	L	H	H	L	L	L	L	**H**	L	*
SHT 3A	071	H	H	H	L	**H**	L	L	L	H	H	**L**	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	L	**H**	**L**	H	L	H	H	**H**	**H**	L	**H**	**H**	**H**	*
SHT 3K	100	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	L	L	**H**	**H**	**H**	L
SHT 1A	101	H	H	H	L	**H**	L	L	L	H	H	H	**L**	H	H	H	**H**	L	L	**H**	**H**	H	H	H	H	H	**H**	**H**	**H**	H	H	H	**H**	L	**H**	H	H	**H**	H	**L**	**H**	**H**	**H**	L	**H**	**H**	H
SHT 4F	110	H	H	**L**	L	**H**	L	L	L	H	H	H	H		**L**	H	L	L	L	L	L	**L**	H	H	H	H	L	**H**	L	H	H	H	L	**H**	L	H	H	L	H	H	L	**H**	**H**	**H**	L	**H**	H
SHT 4F	111	H	H	H	**H**	**H**	L	L	L	**L**	H	H	**L**	**L**	H	H	**H**	L	**H**	L	L	**L**	H	H	H	H	L	L	**H**	H	H	H	L	**H**	L	H	H	L	H	H	L	**H**	**H**	**H**	L	**H**	H
SHT 3G	120	H	H	H	L	**H**	L	L	L	H	H	H	**L**	**L**	H	H	**H**	**H**	L	**H**	L	H	H	**H**	H	H	**H**	**H**	**H**	**L**	H	L	**H**	**H**	**H**	H	H	L	H	**L**	**H**	L	L	**H**	L	**H**	L
SHT 3G	121	H	H	H	L	**H**	L	**H**	L	H	H	H	H		H	H	**H**	L	L	**H**	L	H	H	**L**	H	H	**H**	L	**H**	**L**	H	H	L	**H**	**H**	H	H	L	H	H	**H**	L	**H**	L	**H**	L	L
SHT 3N	130	H	H	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	**H**	**H**	L	**L**	H	L	L	**H**	L	H	H	L	**L**	H	**H**	L	L	**H**	**H**	**H**	L
SHT 3N	131	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	**L**	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	L	L	L	L	L	L	L
SHT 4E	140	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	**L**	H	H	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	**H**	L	L	H
SHT 4E	141	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	**L**	H	H	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	L	L	**H**	H
SHT 1H	150	H	H	H	L	**H**	L	L	L	H	**L**	H	H		H	H	**H**	**H**	**H**	**H**	L	H	H	H	H	H	**H**	**H**	L	**L**	**L**	L	**H**	**H**	L	H	H	L	H	**L**	L	**H**	L	L	**H**	**H**	L
SHT 1H	151	H	H	H	L	**H**	L	L	L	H	H	**L**	H		H	H	**H**	**H**	L	**H**	L	H	**L**	H	H	H	**H**	L	**H**	**L**	H	H	**H**	**H**	**H**	H	H	L	H	**L**	L	**H**	**H**	**H**	**H**	L	H
SHT 4D	160	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	**L**	H	H	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	**H**	**H**	L	L
SHT 4D	161	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	**L**	**L**	H	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	**H**	L	L	H
SHT 1L	170	H	H	H	L	**H**	L	L	L	H	H	**L**	H		H	H	**H**	**H**	**H**	**H**	L	H	**L**	H	H	H	**H**	L	L	**L**	**L**	L	**H**	**H**	L	H	H	L	H	H	**H**	L	L	**H**	L	L	H
SHT 1L	171	H	H	**L**	**H**	**H**	L	**H**	L	H	H	**L**	**L**	**L**	H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	L	**H**	L	**H**	L	L
SHT 2K	200	H	H	**L**	**H**	**H**	L	**H**	L	H	H	**L**	**L**	**L**	H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	**H**	H	H	L	H	H	**H**	L	L	**H**	**H**	**H**	H
SHT 2K	201	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	L	L	L	**H**	**H**	**H**	H
SHT 1D	210	H	**L**	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	L	**H**	**H**	L	H	H	**L**	H	H	**H**	**H**	**H**	**L**	H	H	L	**H**	**H**	H	H	L	H	H	**H**	**H**	**H**	L	L	L	L
SHT 1D	211	H	**L**	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	**H**	**H**	L	L	H	H	**L**	H	H	**H**	**H**	**H**	**L**	**L**	H	**H**	**H**	**H**	H	H	L	H	H	L	L	**H**	**H**	L	**H**	L
SHT 2D	220	H	**L**	**L**	**H**	**H**	L	**H**	L	H	H	H	H		H	H	L	L	L	L	**H**	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	L	L	**H**	L	**H**	H
SHT 2D	221	H	**L**	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	L	L	**H**	L	**H**	L
SHT 1K	230	H	**L**	**L**	**H**	**H**	L	L	L	H	H	**L**	**L**	H	H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	H	L	**H**	L	**L**	H	L	H	H	L	L	**H**	**H**	**H**	**H**	L
SHT 1K	231	H	**L**	H	**H**	**H**	L	L	L	H	H	H	**L**	**L**	H	H	L	L	L	L	L	H	H	H	H	H	**H**	**H**	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	L	**H**	L	L	**H**	**H**	L
SHT 2M	240	H	**L**	H	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	H	H	H	L	**H**	**H**	H	H	**H**	H	H	**H**	L	**H**	**H**	**H**	**H**	L
SHT 2M	241	H	**L**	H	**H**	**H**	L	L	L	H	H	H	**L**	**L**	H	H	L	L	L	L	L	H	H	H	H	H	**H**	**H**	**H**	**L**	H	L	L	**H**	L	H	H	**H**	H	H	L	**H**	L	**H**	L	L	L
SHT 3J	250	H	**L**	**L**	**H**	**H**	L	L	L	**L**	H	H	H		H	H	**H**	L	**H**	**H**	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	L	L	L	L
SHT 3J	251	H	**L**	**L**	**H**	**H**	L	L	L	H	H	H	**L**	H	H	H	L	L	L	L	L	H	H	H	H	H	**H**	**H**	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	L	L	L	L
SHT 2Z	260	H	**L**	**L**	**H**	**H**	L	L	L	H	H	**L**	**L**	H	H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	**H**	**H**	H	H	L	H	H	**H**	**H**	L	L	L	**H**	H
SHT 2Z	261	H	**L**	H	**H**	**H**	L	L	L	H	H	H	**L**	**L**	H	H	L	**H**	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	**H**	H	H	**H**	**H**	L	L	**H**	L	H
SHT 2R	270	H	**L**	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	L	L	**H**	H
SHT 2R	271	H	**L**	H	**H**	**H**	L	**H**	L	H	H	H	H		H	H	L	L	L	L	**H**	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	L	**H**	L	**H**	**H**	**H**	H
	300																	STATES NOT USED																													
	301																			"						"				"																	
SHT 3E	310	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	L	H	**L**	**H**	L	L	**H**	**H**	L	*
SHT 3E	311	H	H	H	**H**	**H**	L	**H**	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	**L**	H	L	H	H	**H**	L	L	**H**	**H**	L	*
	320																	STATES NOT USED																													
	321																			"						"				"																	
SHT 1G	330	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	**L**	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	L	**H**	**H**	L	**H**	**H**	H
SHT 1G	331	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	**H**	**H**	L	**H**	**H**	**L**	H	**L**	H	H	**H**	L	**H**	**L**	H	H	**H**	**H**	L	H	H	L	H	H	**H**	**H**	**H**	L	L	L	L
SHT 2J	340	H	H	H	**H**	**H**	L	L	**H**	**L**	H	H	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	**L**	L	H	H	L	**H**	**H**	**H**	L	L	*
SHT 2J	341	H	H	**L**	**H**	**H**	L	L	L	**L**	H	H	H		H	**L**	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	**L**	H	L	H	H	L	**H**	L	L	L	L	*
SHT 4G	350	H	H	**L**	**H**	**H**	L	**H**	L	H	H	**L**	**L**	**L**	H	H	L	L	L	L	L	**L**	H	H	H	H	L	L	**H**	H	H	L	L	**H**	L	H	H	L	H	H	L	L	L	**H**	**H**	L	H
SHT 4G	351	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	**L**	H	**L**	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	**H**	**H**	L	L
SHT 1J	360	H	H	H	**H**	**H**	L	L	**H**	**L**	H	H	**L**	H	H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	**H**	H	H	L	H	H	L	**H**	**H**	**H**	**H**	L	H
SHT 1J	361	H	H	**L**	L	**H**	L	L	L	H	H	**L**	H		**L**	**L**	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	**H**	**L**	H	L	H	H	**H**	L	L	**H**	L	L	H
SHT 4C	370	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	**L**	H	H	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	L	**H**	**H**	**H**	**H**	**H**	H
SHT 4C	371	H	H	**L**	**H**	**H**	L	**H**	L	H	H	H	H		H	H	L	L	L	L	L	**L**	H	H	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	**H**	**H**	L	L

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NOTE:
* NORMALLY H, L WITH 'N' DATA ROUTINE.
BLANK LOCATIONS= DON'T CARE STATES

BOLD LETTERS= ACTIVE STATES

Table 7-6. Command Source Listing

LETTER CODES	ADDRESSES \ COMMANDS	*←ON	*←OFF	1 PULSE CNT	15 PULSE CNT	ADD	DC←0	DC CLK	DISP CLK EN	DPLK CLK	DPLK←DPLK-PI	DPLK←-	DPLR CLK	DPLR UP	DPLR←-1	DRC←0	DR CLK EN	DR EN A	DR EN B	DR EN C	DS←DC	EXT OUT EN	FLAG←H	FLAG←L	LOAD MS	LOAD * STORAGE	NR CLK EN	NR EN A	NR EN B	PROC BUSY	PI CLK EN	QR EN A/PI XMT	QR EN B	QR EN C	QR EN CLK	QMC←0	QMC CLK	RST FRONT END	SIGN←-	SIGN←+	SV1 (T+1)	SV2 (T+1)	SV3 (T+1)	SV4 (T+1)	SV5 (T+1)	SV6 (T+1)	FLAG=H
COMMAND SOURCE		A15-U10-6	A15-U10-3	A15-TP	A15-U15-5	A15-A11	A15-U35-2	A15-U35-4	A15-B9	A15-B18	A15-B17	A15-B6	A15-B5	A15-B7	A15-B16	A15-A12	A15-A22	A15-B21	A15-A8	A15-A9	A15-U34-4	A15-A9	A15-U2-5	A15-U2-1	A15-B5	A15-U25-11	A15-A12	A15-A7	A15-B10	A15-B8	A15-A6	A14-A12	A15-B10	A15-A21	A15-A15	A15-A14	A15-A5	A15-A20	A15-U10-9	A15-U10-3	A14-U23-2	A14-U23-7	A14-U23-5	A14-U23-10	A14-U23-12	A14-U23-15	A15-A10
MSB		0	0	0	0	1	0			1	0		0	0	0	0		0	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1	0	0	1	1	1	1	1	1	0
PULSED COMMAND		P	P				P	P		P	P	P	P		P	P							P	P	P	P										P	P		P	P							
SHT 2	400	H	H	**L**	**H**	**H**	L	**H**	L	H	H	H	H		H	H	L	L	L	L	**H**	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	**L**	L	H	H	**H**	L	L	**H**	L	L	*
SHT 2	40	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	**L**	L	H	H	**H**	L	L	**H**	L	L	H
SHT 2Q	4 0	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	H	H	H	H	H	**H**	**H**	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	**H**	L	**H**	L	L	H
SHT 2Q	4	H	H	H	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	H	H	H	**L**	H	**H**	**H**	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	**H**	L	**H**	L	L	H
SHT 2G	420	H	H	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	L	**H**	**H**	L	H	H	H	H	H	**H**	**H**	L	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	L	**H**	L	**H**	**H**	*
SHT 2G	42	H	H	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	L	**H**	**H**	L	H	H	H	H	H	**H**	L	**H**	**L**	H	H	L	**H**	**H**	H	H	L	H	H	L	**H**	**H**	**H**	L	L	*
SHT 3M	430	H	H	H	L	L	L	L	L	H	H	H	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	**H**	**H**	L	**L**	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	L	**H**	**H**	L
SHT 3M	43	H	H	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	**H**	**H**	L	**L**	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	L	**H**	**H**	L
SHT 2A	440	H	H	H	**H**	**H**	L	L	L	**L**	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	**H**	**H**	H	H	L	H	H	**H**	**H**	L	L	L	L	*
SHT 2A	44	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	**L**	H	L	H	H	L	**H**	L	L	**H**	L	*
SHT 2E	450	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	L	**H**	**H**	**H**	L	L
SHT 2E	451	H	H	**L**	**H**	**H**	**H**	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	L	L	L	**H**	L	**H**	*
SHT 3F	460	H	H	H	**H**	**H**	L	L	L	**L**	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	**H**	**H**	**H**	H	H	L	H	**L**	**H**	**H**	L	**H**	**H**	**H**	*
SHT 3F	461	H	H	**L**	L	**H**	**H**	L	L	H	H	**L**	H		H	**L**	L	L	L	L	L	H	H	H	H	H	**H**	L	L	**L**	H	H	L	**H**	L	H	H	L	H	H	L	L	**H**	L	**H**	L	*
SHT 3L	470	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	H	H	**L**	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	L	**H**	L	**H**	L	**H**	L
SHT 3	47	H	H	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	**H**	L	**H**	**H**	H	H	**L**	H	H	**H**	L	L	**L**	H	L	**H**	**H**	L	H	H	L	H	H	**H**	L	L	L	**H**	**H**	L
SHT 2P	500	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	L	**H**	L	**H**	**H**	**H**	H
SHT 2P	501	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	L	L	L	L	**H**	H
SHT 2N	5 0	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	**H**	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	L	**H**	L	L	L	H
SHT 2N	5 1	H	H	**L**	L	**H**	L	L	L	H	H	H	H		**L**	H	**H**	**H**	**H**	**H**	**H**	H	H	H	H	H	L	**H**	**H**	**L**	H	H	**H**	**H**	**H**	H	H	**H**	H	H	L	L	**H**	L	L	L	H
SHT 3H	520	H	H	H	L	**H**	**H**	L	L	H	H	H	H		H	H	**H**	L	**H**	L	**H**	H	H	H	H	H	**H**	L	L	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	L	**H**	**H**	L	**H**	L
SHT 3H	521	H	H	H	L	**H**	L	L	L	H	**L**	H	H		H	H	**H**	**H**	**H**	**H**	**H**	H	H	H	H	H	**H**	L	**H**	**L**	**L**	L	**H**	**H**	L	H	H	**H**	H	H	**H**	L	L	**H**	**H**	**H**	L
SHT 2H	530	H	H	H	L	**H**	L	L	L	H	H	**L**	H		H	H	**H**	**H**	L	**H**	L	H	H	H	H	H	**H**	L	L	**L**	H	H	**H**	**H**	L	H	H	L	H	**L**	L	**H**	**H**	**H**	L	L	*
SHT 2H	531	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	**H**	**H**	L	H	H	L	H	**L**	L	**H**	**H**	**H**	L	L	*
SHT 3R	540	H	H	H	**H**	**H**	L	L	**H**	**L**	H	**L**	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	L	**H**	**H**	L	L	L
SHT 3R	54	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	**L**	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	L	L	**H**	L	L	L
SHT 3Q	550	H	H	H	**H**	**H**	L	L	L	H	H	H	**L**	**L**	H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	**L**	L	H	H	**H**	L	**H**	**H**	L	**H**	L
SHT 3Q	55	H	H	H	L	**H**	L	L	L	H	H	**L**	H		H	H	**H**	**H**	**H**	L	L	H	H	H	H	H	**H**	L	**H**	**L**	**L**	H	**H**	**H**	**H**	**L**	H	L	H	H	**H**	L	**H**	**H**	L	L	L
SHT 2L	560	H	H	H	L	**H**	L	L	L	H	**L**	H	H		**L**	H	**H**	**H**	**H**	**H**	L	H	H	H	H	H	L	**H**	L	**L**	**L**	L	**H**	**H**	L	H	H	**H**	H	**L**	L	**H**	L	**H**	L	L	L
SHT 2L	56	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	**L**	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	L	**H**	L	L	**H**	H
SHT C	570	H	H	H	L	**H**	**H**	L	L	H	H	**L**	H		H	**L**	L	**H**	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	**H**	**H**	**H**	H	H	L	H	H	L	**H**	L	L	L	**H**	*
SHT C	571	H	H	H	**H**	**H**	L	L	**H**	**L**	H	**L**	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	H	H	H	L	**H**	**H**	H	H	L	H	H	**H**	L	**H**	**H**	**H**	**H**	*
SHT 2B	600	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	L	L	**H**	L	L	*
SHT 2B	601	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	**H**	L	L	**H**	H	H	H	H	H	L	L	**H**	**L**	H	L	L	L	L	H	H	L	H	H	**H**	L	L	L	L	L	*
SHT 2AA	610	H	H	**L**	**H**	**H**	L	**H**	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	L	L	L	L	L	**H**	H
SHT 2AA	611	H	H	**L**	**H**	**H**	**H**	L	L	H	H	H	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	L	L	L	L	L	**H**	H
SHT 2Y	620	H	H	H	L	**H**	L	L	L	H	H	H	H		H	H	**H**	L	L	**H**	**H**	H	H	H	H	H	**L**	**H**	L	**H**	H	H	L	**H**	**H**	H	H	**H**	H	H	**H**	**H**	**H**	L	**H**	**H**	H
SHT 2Y	62	H	H	H	**H**	**H**	L	L	L	**L**	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	**H**	**H**	H	H	L	H	H	L	**H**	L	**H**	**H**	L	H
SHT 4A	630	H	H	H	**H**	**H**	L	L	L	**L**	H	H	**L**	**L**	H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	H	H	L	L	**H**	**H**	H	H	L	H	H	**H**	**H**	L	L	**H**	**H**	H
SHT 4A	631	H	H	**L**	**H**	**H**	L	**H**	L	H	H	H	H		H	H	L	L	L	L	L	H	H	**L**	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	L	**H**	L	L
SHT 2T	640	H	H	H	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	**H**	**H**	H	H	L	H	H	**H**	**H**	L	**H**	L	**H**	H
SHT 2T	641	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	**H**	L	L	H
SHT 2W	650	H	H	**L**	**H**	**H**	**H**	L	L	**L**	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	**H**	L	**H**	**L**	H	L	L	**H**	**H**	H	H	**H**	H	H	**H**	**H**	L	L	**H**	L	H
SHT 2W	651	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	**H**	L	**H**	**H**	L	H
SHT 2X	660	H	H	**L**	**H**	**H**	L	L	L	H	H	H	**L**	**L**	H	H	L	**H**	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	**H**	**H**	L	H	H	L	H	H	**H**	**H**	L	**H**	L	L	H
SHT 2X	661	**L**	H	**L**	**H**	**H**	L	L	L	H	H	H	**L**	**L**	H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	L	L	H	H	L	H	H	**H**	**H**	L	**H**	L	L	H
SHT 3C	670	H	H	H	**H**	**H**	L	L	L	H	H	H	**L**	*	H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	**L**	H	L	L	**H**	L	**L**	H	L	H	H	L	L	L	L	**H**	**H**	*
SHT 3C	67	H	H	H	L	L	L	L	L	H	H	H	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	**H**	**H**	L	**L**	H	L	**H**	**H**	L	H	H	L	H	**L**	L	L	L	L	**H**	**H**	*
SHT E	700	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	**L**	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	**H**	H	H	**H**	**H**	**H**	**H**	L	**H**	L
SHT E	701	H	H	**L**	**H**	**H**	L	L	L	**L**	H	**L**	H		H	H	L	L	L	L	L	**L**	**L**	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	L	**H**	**H**	L	**H**	**H**	H
SHT 2S	7 0	H	H	H	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	**L**	H	L	L	**H**	**L**	H	L	L	**H**	L	H	H	L	H	H	**H**	**H**	L	**H**	L	L	H
SHT 2S	7 1	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	**H**	L	L	H
SHT 4B	720	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	**L**	H	H	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	L	**H**	L	L
SHT 4B	721	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	L	**L**	**L**	H	H	H	L	**H**	**H**	H	H	H	L	**H**	L	H	H	L	H	H	L	**H**	**H**	**H**	**H**	**H**	H
SHT B	730	H	H	H	**H**	**H**	**H**	L	L	H	H	**L**	H		H	H	**H**	L	**H**	L	L	H	H	H	H	H	L	L	**H**	H	H	L	L	**H**	**H**	H	H	L	H	H	**H**	**H**	L	L	**H**	**H**	H
SHT B	73	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	H	H	H	L	**H**	**H**	H	H	**H**	H	H	**H**	L	**H**	**H**	**H**	**H**	H
SHT 2U	740	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	**L**	L	H	H	**H**	L	**H**	L	L	L	H
SHT 2J	741	H	H	**L**	**H**	**H**	L	L	L	**L**	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	**H**	**H**	**H**	H
SHT F	750	H	H	**L**	**H**	**H**	L	L	L	H	H	H	H		H	H	L	L	L	L	**H**	**L**	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	L	L	L	L
SHT F	751	H	H	H	L	**H**	L	L	L	H	H	**L**	H		**L**	H	**H**	L	L	**H**	L	H	H	H	H	H	L	L	**H**	H	H	H	**H**	**H**	**H**	H	H	**H**	H	**L**	**H**	L	**H**	**H**	**H**	**H**	L
SHT 4K	760	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	**L**	H	H	H	H	L	L	**H**	H	H	L	L	**H**	L	H	H	L	H	H	L	L	L	**H**	**H**	L	L
SHT 4K	761	H	H	**L**	**H**	**H**	L	L	L	H	H	**L**	H		H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	H	H	H	L	**H**	L	H	H	L	H	H	**H**	L	**H**	**H**	**H**	**H**	L
SHT 2V	770	H	H	**L**	**H**	**H**	L	L	L	H	H	H	**L**	H	H	H	L	L	L	L	L	H	H	H	H	H	L	**H**	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	**H**	L	L	H
SHT 2V	771	H	H	**L**	**H**	**H**	L	L	L	H	H	H	**L**	**L**	H	H	L	L	L	L	L	H	H	H	H	H	L	L	**H**	**L**	H	H	L	**H**	L	H	H	L	H	H	**H**	**H**	**H**	**H**	L	L	H

NOTE:
* NORMALLY H, L WITH "N" DATA ROUTINE.
BLANK LOCATIONS = DON T CARE STATES.
BOLD LETTERS = ACTIVE STATES

5345 D 26

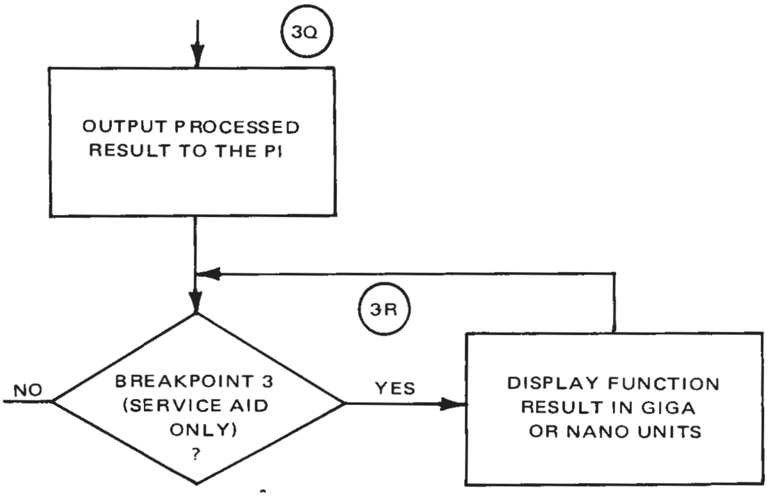
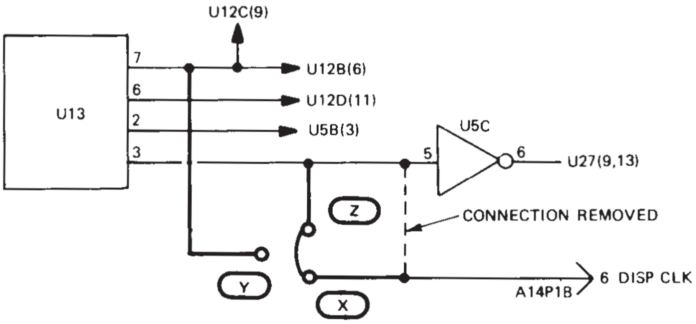

3Q
OUTPUT PROCESSED RESULT TO THE PI
3R
NO
BREAKPOINT 3 (SERVICE AID ONLY) ?
YES
DISPLAY FUNCTION RESULT IN GIGA OR NANO UNITS

Figure 7-2. Partial Flowchart for Backdating Figure 5-9.



Wiring for Jumper Connection

Figure 7-3. Partial Diagrams Showing Changes on A14 (05345-60014) for Series 1612

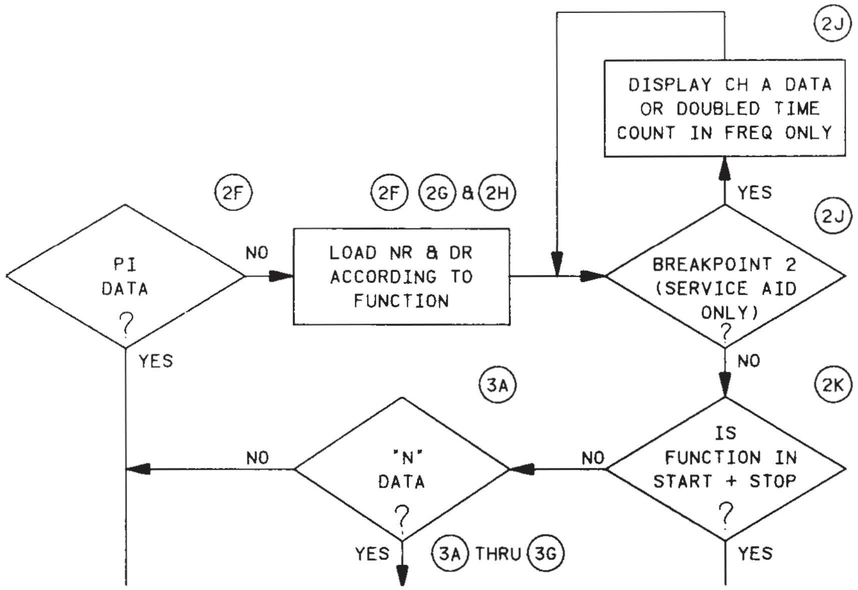

2J
DISPLAY CH A DATA OR DOUBLED TIME COUNT IN FREQ ONLY
2F
2F 2G & 2H
YES
2J
PI DATA ?
NO
LOAD NR & DR ACCORDING TO FUNCTION
BREAKPOINT 2 (SERVICE AID ONLY) ?
YES
NO
3A
2K
NO
"N" DATA ?
NO
IS FUNCTION IN START + STOP ?
YES
3A THRU 3G
YES

Figure 7-3A. Partial of Simplified Processor Flow Chart

2J QUALIFIER BREAKPOINT 2 is a service aid switch located on A14(S1-2). For frequency, it enables the counter to display the doubled time count. For functions other than frequency, it enables the counter to display the Channel A event counts. When the switch is enabled, State 340 is selected.

STATE 340 This state rotates the contents of the DR RAM to the display. DISP CLK EN enables the count 11 mode; DPLK←DPLK-1 clocks the DPLK counter to enable the display clock; and PI XMT BUS inhibits plug-in data from the A15 bidirectional bus. The QMC←QMC+1 causes the QMC to be clocked. This is done as a test function to enable its operation to be checked.

STATE 341 QMC←0 resets the QMC (A13) and DRC←0 resets the DRC (A13). This is done in the event the display state was enabled by BREAKPOINT 2 (2J). When counters are used during the display, the are always reset after use.

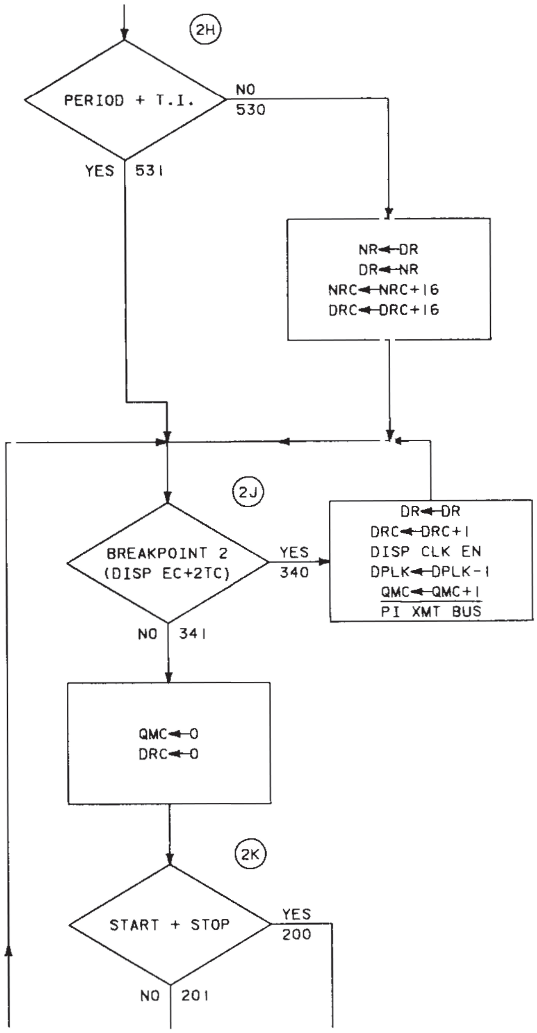


Figure 7-3B. Partial of Processor Flowchart, Sheet 2

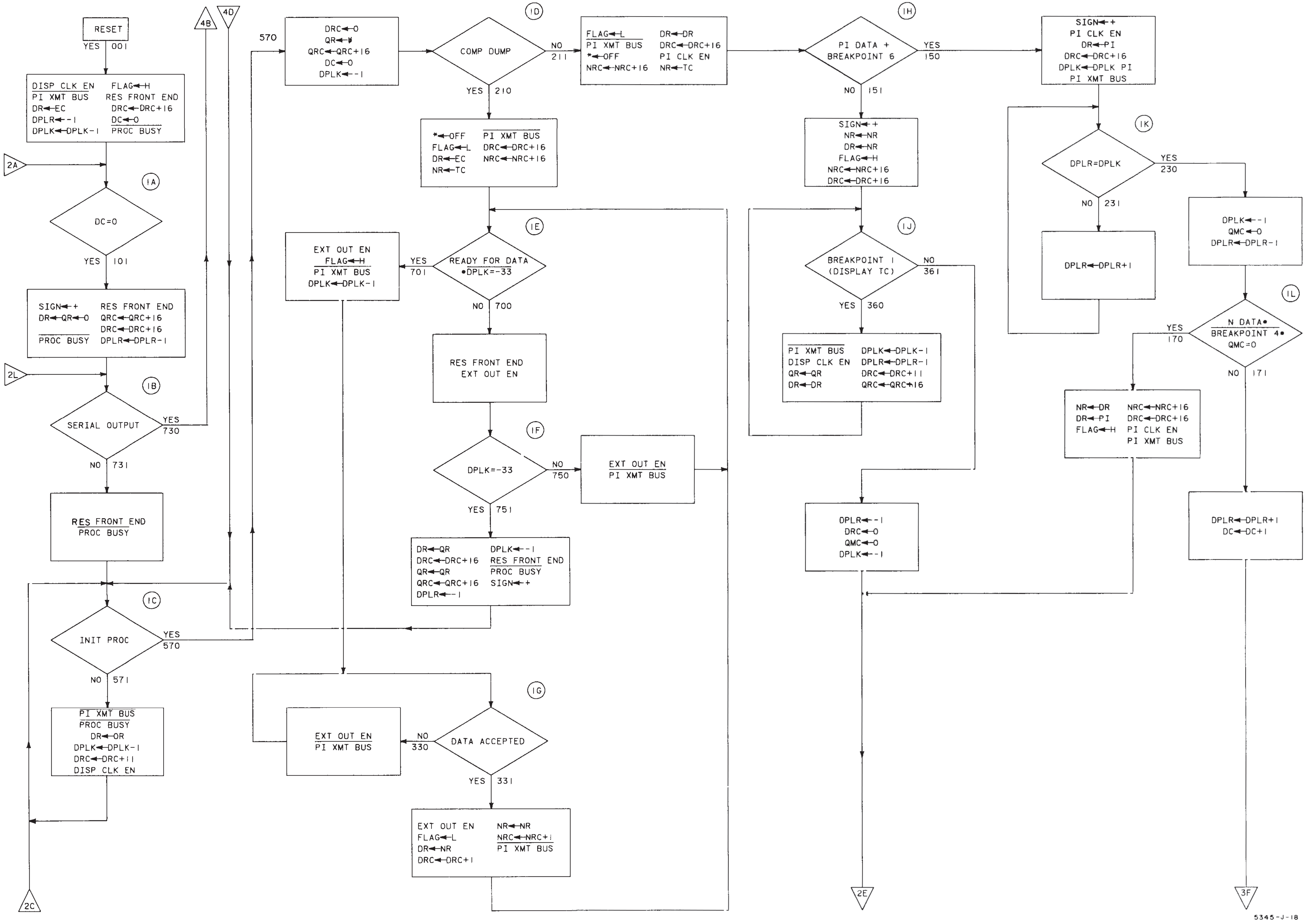


Figure 7-4. Processor Flowchart, Sheet 1, Series 1612A and Below

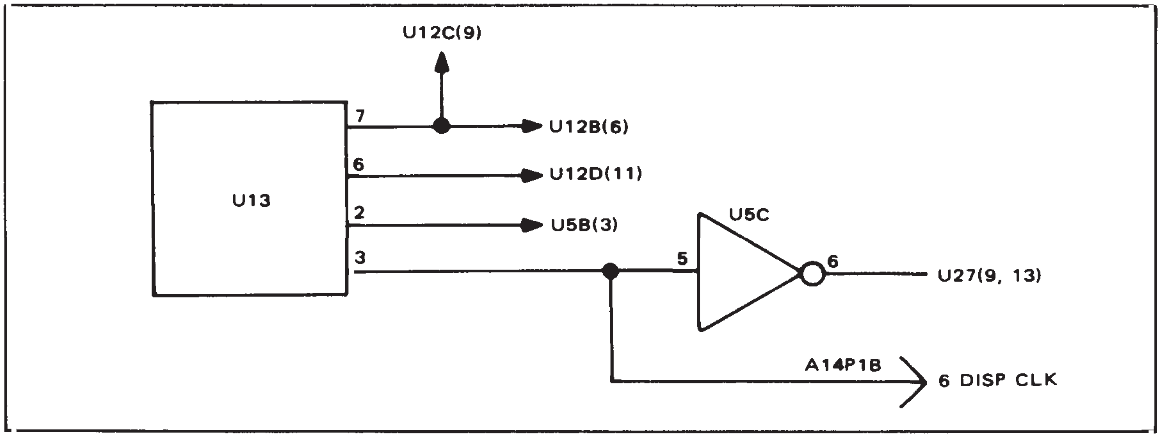


Figure 7-5. Wiring Changes for A14 Series 1604

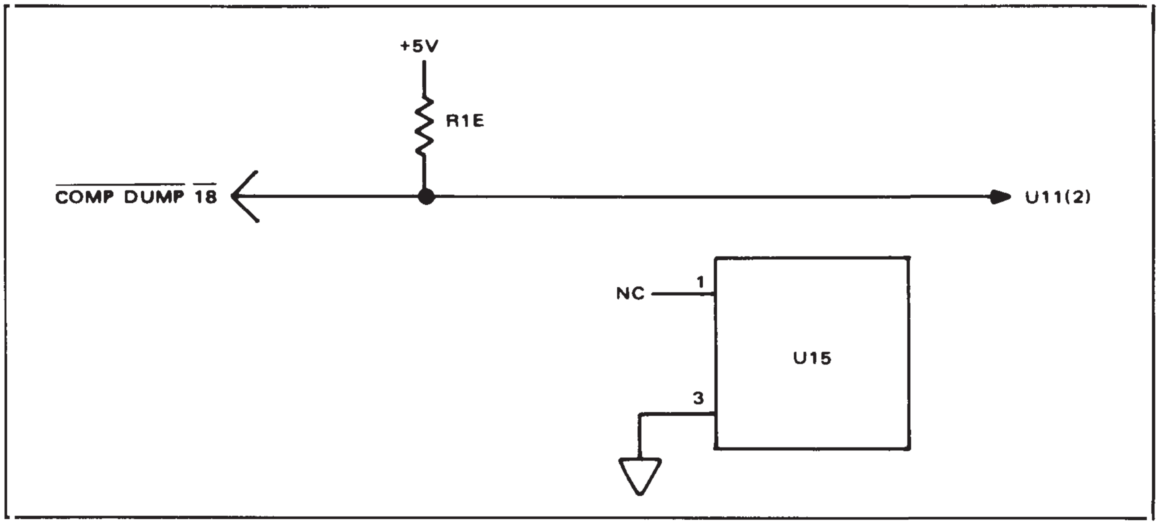


Figure 7-6. Wiring Change for A14 Series 1604

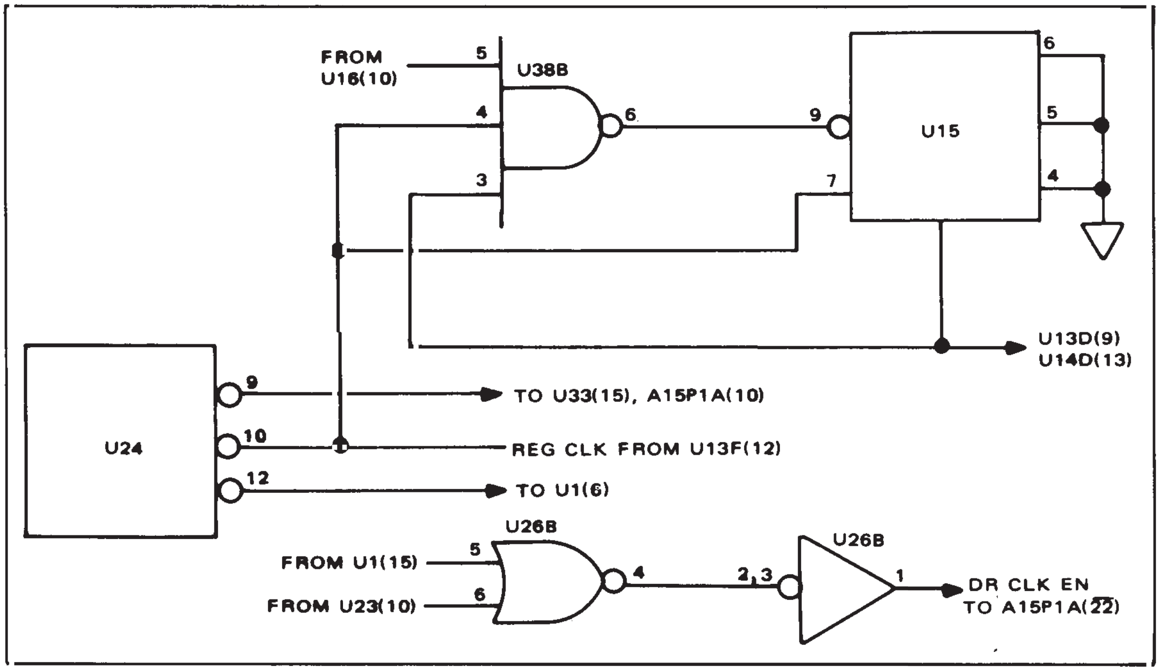


Figure 7-7. A15 Wiring Changes for Series 1604A

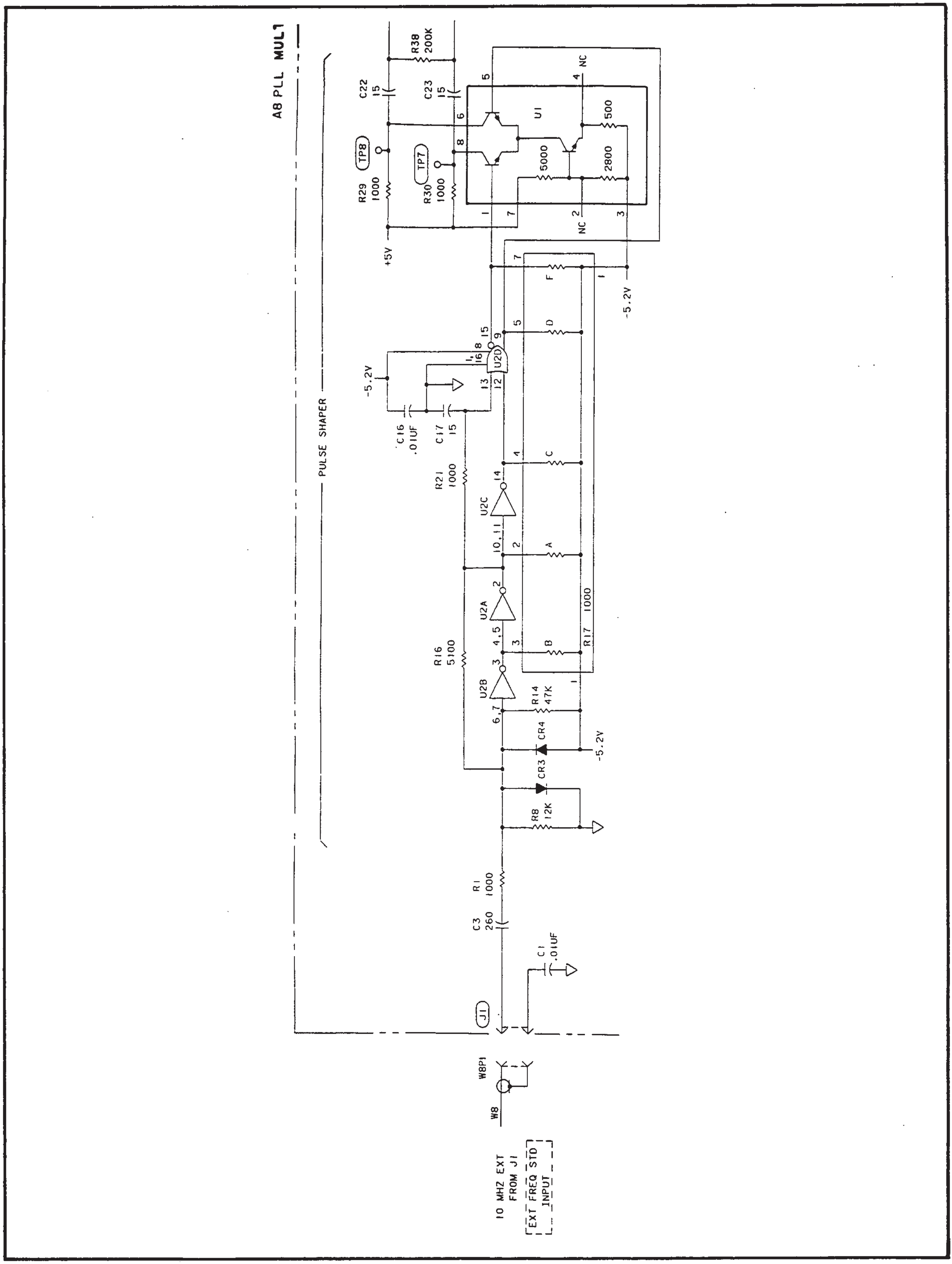


Figure 7-8. Partial Schematic of Circuit Changes for A8 Series 1340A

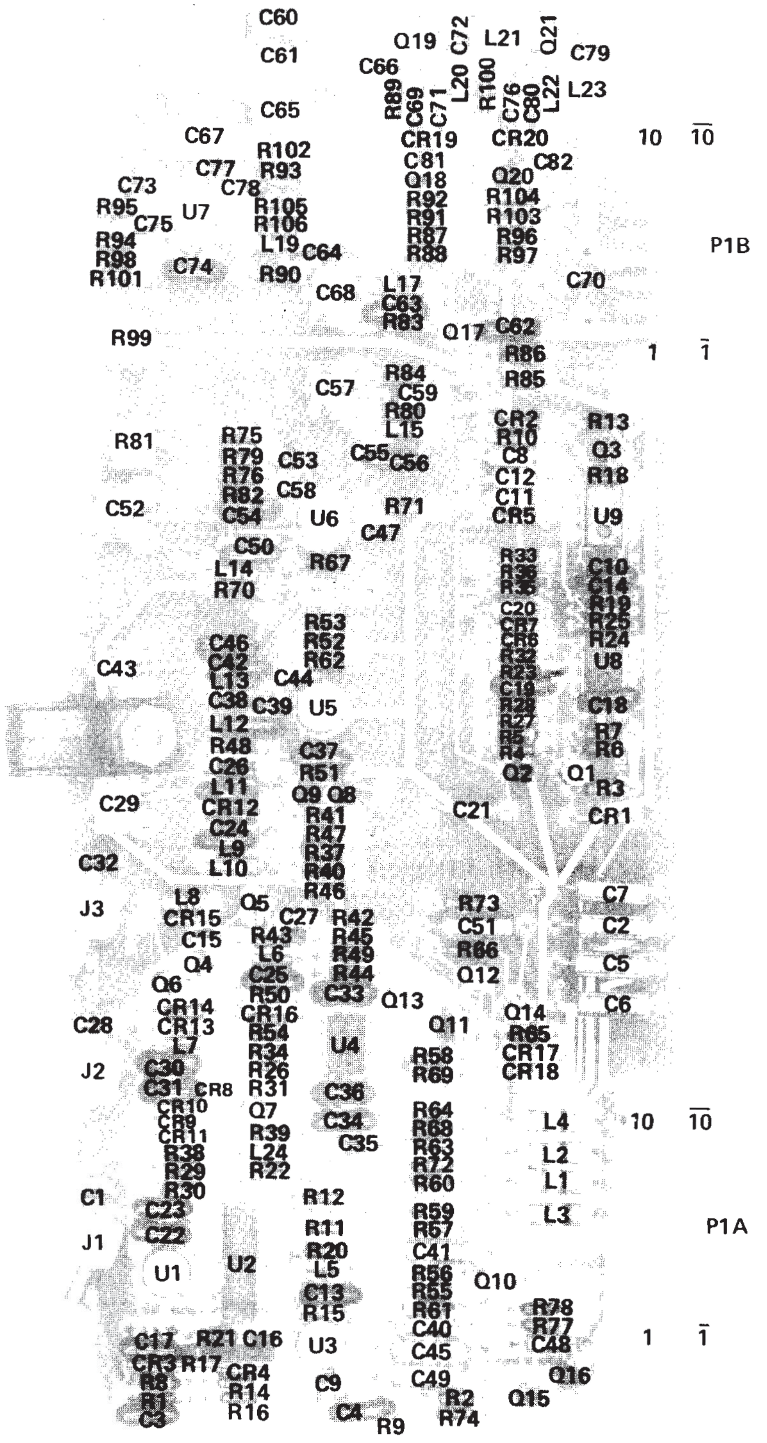


Figure 7-9. A8 Component Locator Series 1340A

A20 INT-EXT FREQUENCY STANDARD SWITCH (OPT. 001) (SERIAL 1428A00451 THRU 1440A00950)

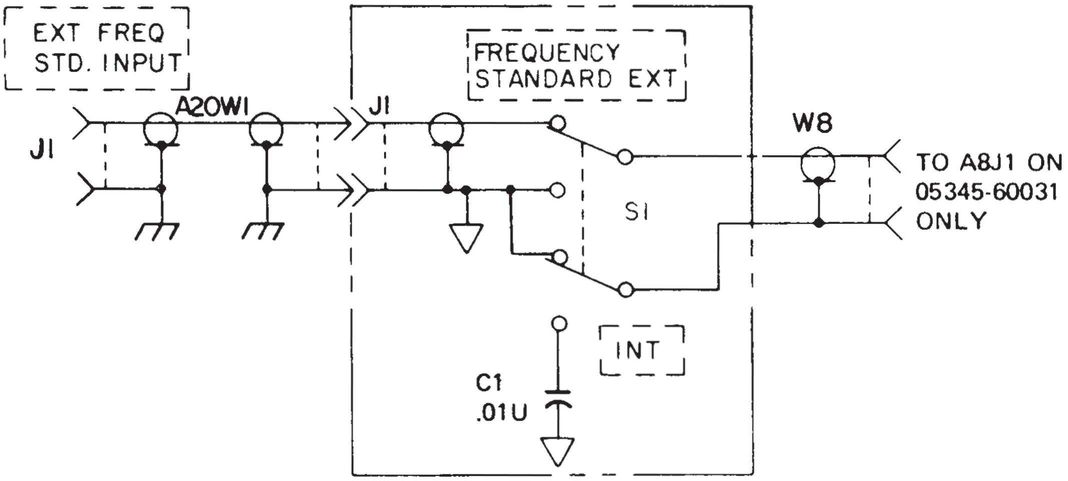


Figure 7-10. A20 INT-EXT FREQ STANDARD Switch Schematic Diagram for Option 001 Instrument With Serial Numbers 1428A00451 through 1440A00950

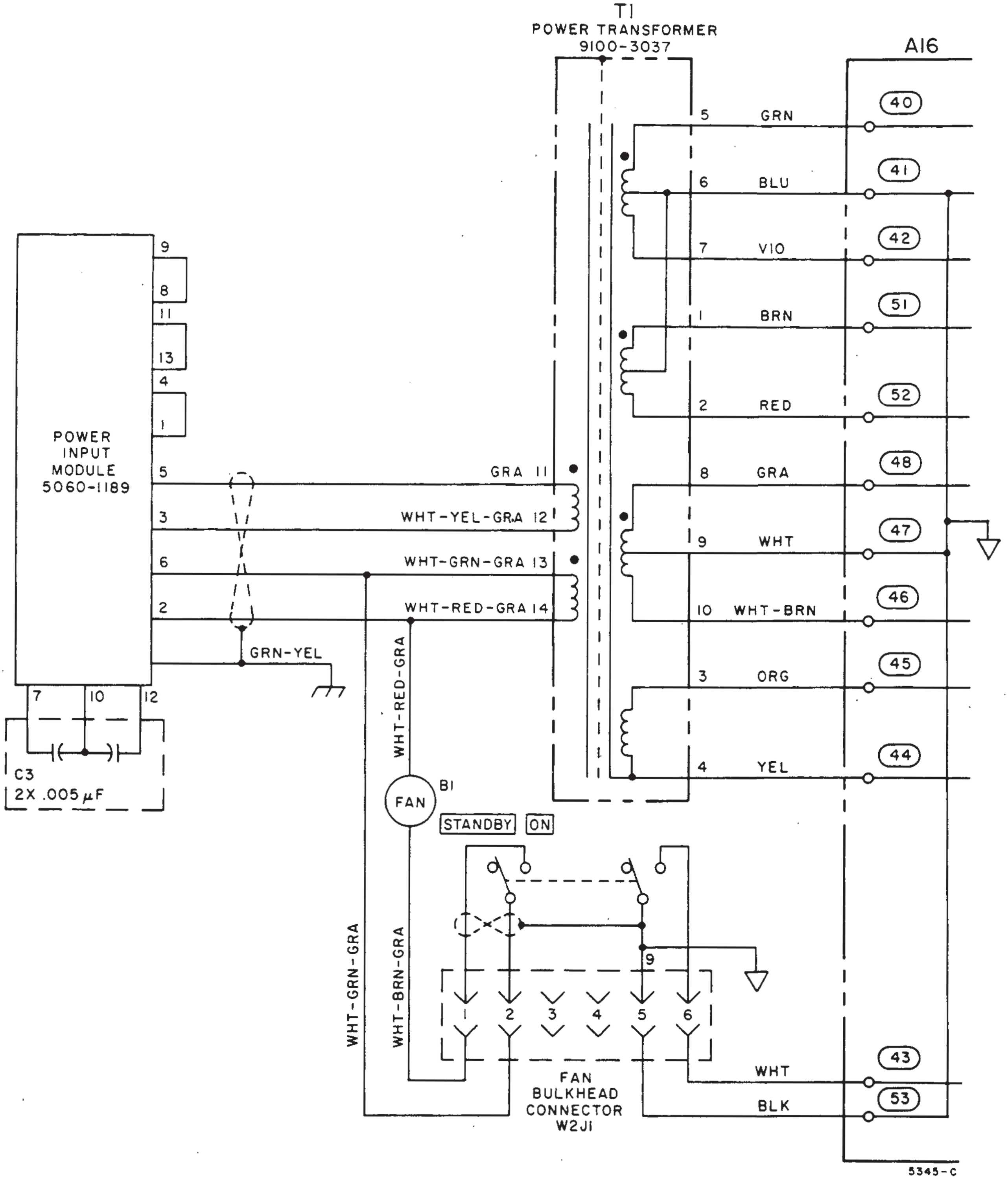


Figure 7-11. Wiring for Primary Power Circuit (Series 1340A through 1438A)

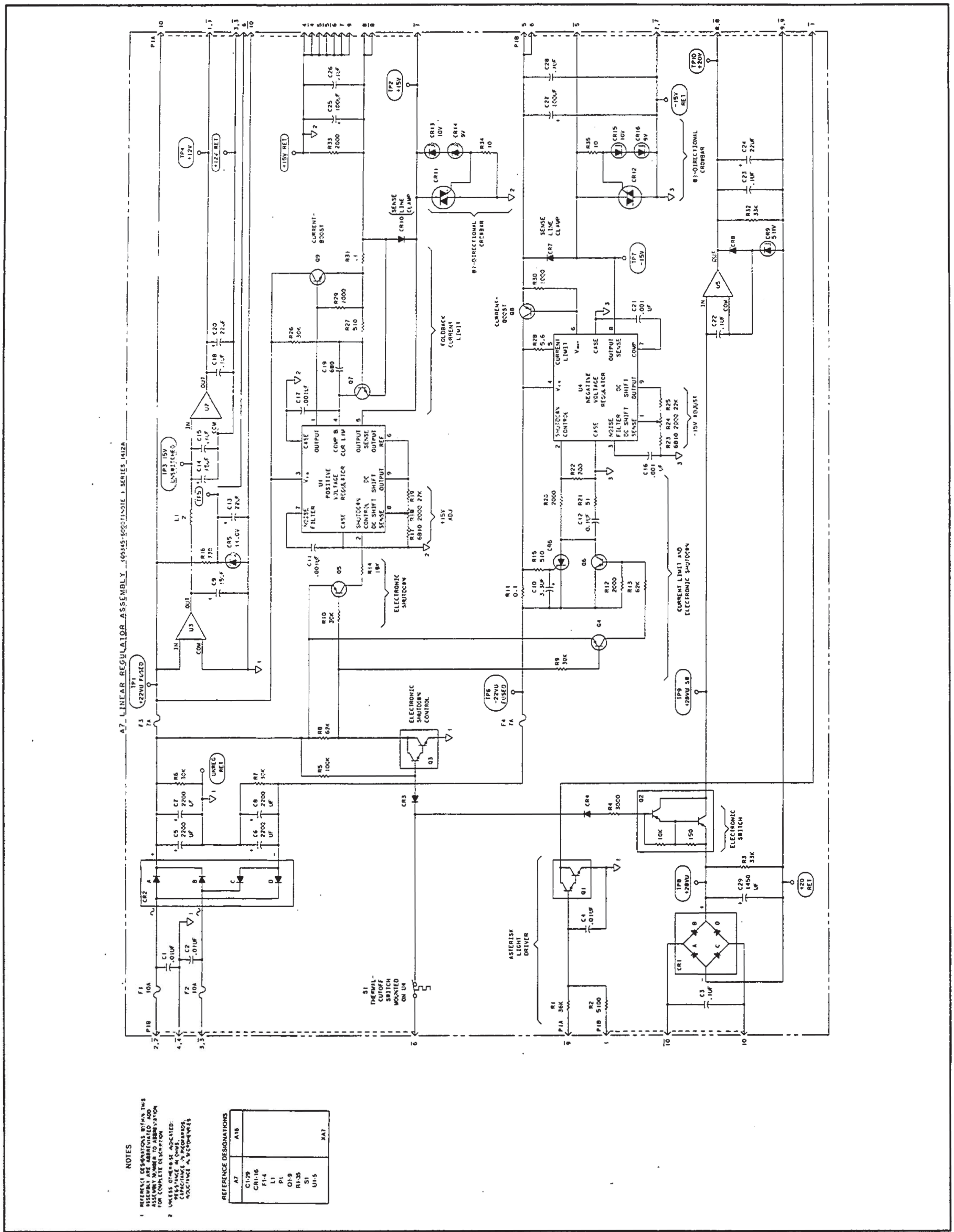

A7 LINEAR REGULATOR ASSEMBLY (05345-60021) SERIES 1412A
U1 POSITIVE VOLTAGE REGULATOR
U4 NEGATIVE VOLTAGE REGULATOR
FOLDBACK CURRENT LIMIT
ELECTRONIC SHUTDOWN
ELECTRONIC SHUTDOWN CONTROL
CURRENT LIMIT AND ELECTRONIC SHUTDOWN
BI-DIRECTIONAL CROWBAR
SENSE LINE CLAMP
CURRENT-BOOST
ELECTRONIC SWITCH
ASTERISK LIGHT DRIVER
S1 THERMAL-CUTOFF SWITCH MOUNTED ON U4
+15V ADJ
-15V ADJUST
TP1 +22VU FUSED
TP2 +15V
TP3 15V UNREGULATED
TP4 +12V
TP6 -22VU FUSED
TP7 -15V
TP8 +28VU
TP9 +28VU SB
TP10 +20V
+15V RET
+12V RET
-15V RET
UNREG RET
+20 RET
NOTES
1 REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION
2 UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN PICOFARADS, INDUCTANCE IN MICROHENRIES
REFERENCE DESIGNATIONS
A7
C1-29
CR1-16
F1-4
L1
P1
Q1-9
R1-35
S1
U1-5
A18
XA7

Figure 7-12. A7 Linear Regulator Assembly, Series 1412A

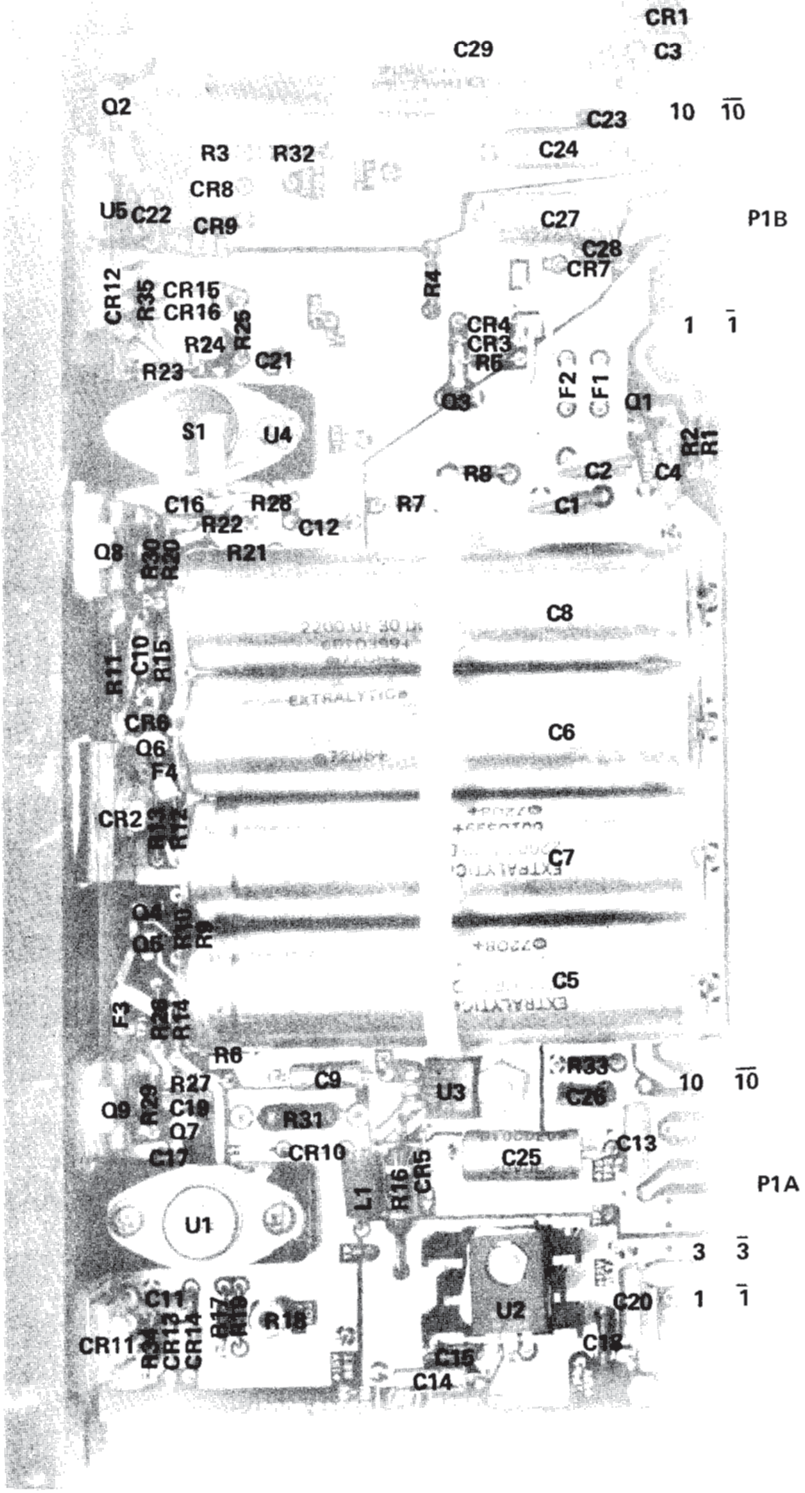


Figure 7-13. A7 Component Locator, Series 1412A

Table 7-7. A7 Replaceable Parts for Series 1428A and Below

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A7	05345-60007	1	LINEAR REGULATOR ASSY	28480	05345-60007
A7C1	0150-0012	2	CAPACITOR-FXD .01UF +-20% 1000WVDC CER	56289	C023A102J103MS38
A7C2	0150-0012		CAPACITOR-FXD .01UF +-20% 1000WVDC CER	56289	C023A102J103MS38
A7C3	0150-0084	3	CAPACITOR-FXD .1UF +80-20% 100WVDC CER	28480	0150-0084
A7C4	0160-0161	1	CAPACITOR-FXD .01UF +-10% 200WVDC POLYE	56289	292P10392
A7C5	0180-2470	4	CAPACITOR-FXD; 2200UF+75-10% 30VDC AL	56289	601D228G030GS4
A7C6	0180-2470		CAPACITOR-FXD; 2200UF+75-10% 30VDC AL	56289	601D228G030GS4
A7C7	0180-2470		CAPACITOR-FXD; 2200UF+75-10% 30VDC AL	56289	601D228G030GS4
A7C8	0180-2470		CAPACITOR-FXD; 2200UF+75-10% 30VDC AL	56289	601D228G030GS4
A7C9	0180-1746	5	CAPACITOR-FXD; 15UF+-10% 20VDC TA-SOLID	56289	150D156X9020B2
A7C10	0180-0210		CAPACITOR-FXD; 3.3UF+-20% 15VDC TA	56289	150D335X0015A2
A7C11	0150-0050	10	CAPACITOR-FXD 1000PF +80-20% 1000WVDC	28480	0150-0050
A7C12	0150-0084		CAPACITOR-FXD .1UF +80-20% 100WVDC CER	28480	0150-0084
A7C13	0180-0228	2	CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID	56289	150D226X9015B2
A7C14	0180-1746		CAPACITOR-FXD; 15UF+-10% 20VDC TA-SOLID	56289	150D156X9020B2
A7C15	0160-3060		CAPACITOR-FXD .1UF +-20% 25WVDC CER	28480	0160-3060
A7C16	0150-0050		CAPACITOR-FXD 1000PF +80-20% 1000WVDC	28480	0150-0050
A7C17	0160-3878		CAPACITOR-FXD 1000PF +-20% 100WVDC CER	28480	0160-3878
A7C18	0160-3060		CAPACITOR-FXD .1UF +-20% 25WVDC CER	28480	0160-3060
A7C19*	0160-2141	1	CAPACITOR-FXD 680PF +-20% 1000WVDC CER	28480	0160-2141
A7C20	0180-0228		CAPACITOR-FXD; 22UF+-10% 15VDC TA-SOLID	56289	150D226X9015B2
A7C21	0160-3878		CAPACITOR-FXD 1000PF +-20% 100WVDC CER	28480	0160-3878
A7C22	0150-0084		CAPACITOR-FXD .1UF +80-20% 100WVDC CER	28480	0150-0084
A7C23	0160-3060		CAPACITOR-FXD .1UF +-20% 25WVDC CER	28480	0160-3060
A7C24	0180-0160	1	CAPACITOR-FXD; 22UF+-20% 35VDC TA-SOLID	56289	150D226X0035R2
A7C25	0180-0098	2	CAPACITOR-FXD; 100UF+-20% 20VDC TA	56289	150D107X0020S2
A7C26	0160-3060		CAPACITOR-FXD .1UF +-20% 25WVDC CER	28480	0160-3060
A7C27	0180-0098		CAPACITOR-FXD; 100UF+-20% 20VDC TA	56289	150D107X0020S2
A7C28	0160-3060		CAPACITOR-FXD .1UF +-20% 25WVDC CER	28480	0160-3060
A7C29	0180-2472	1	CAPACITOR-FXD; 1450UF+75-10% 35VDC AL	28480	0180-2472
A7CR1	1906-0026	1	DIODE; MULT; FULL WAVE BRIDGE RECTIFIER	04713	MDA922-3
A7CR2	1901-0638		DIODE; MULT; FULL WAVE BRIDGE RECTIFIER	28480	1901-0638
A7CR3	1901-0519		DIODE-SWITCHING 50NS 200V	28480	1901-0519
A7CR4	1901-0519		DIODE-SWITCHING 50NS 200V	28480	1901-0519
A7CR5	1902-3171	1	DIODE-ZNR 11V 5% DO-7 PD=.4W TC=+.062%	04713	SZ 10939-194
A7CR6	1884-0201		THYRISTOR; SCR; JEDEC	04713	2N5061
A7CR7	1901-0519		DIODE-SWITCHING 50NS 200V	28480	1901-0519
A7CR8	1901-0519		DIODE-SWITCHING 50NS 200V	28480	1901-0519
A7CR9	1902-0041	2	DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=	04713	SZ 10939-98
A7CR10	1901-0519		DIODE-SWITCHING 50NS 200V	28480	1901-0519
A7CR11	1884-0217		THYRISTOR; SI TRIAC	28480	1884-0217
A7CR12	1884-0217		THYRISTOR; SI TRIAC	28480	1884-0217
A7CR13	1902-0025	2	DIODE-ZNR 10V 5% DO-7 PD=.4W TC=+.06%	04713	SZ 10939-182
A7CR14	1902-3149	2	DIODE-ZNR 9.09V 5% DO-7 PD=.4W	04713	SZ 10939-170
A7CR15	1902-0025		DIODE-ZNR 10V 5% DO-7 PD=.4W TC=+.06%	04713	SZ 10939-182
A7CR16	1902-3149		DIODE-ZNR 9.09V 5% DO-7 PD=.4W	04713	SZ 10939-170
A7F1	2110-0446		FUSE; 10A 125V	28480	2110-0446
A7F2	2110-0446		FUSE; 10A 125V	28480	2110-0446
A7F3	2110-0438	2	FUSE 7A 125V SLO-BLO	28480	2110-0438
A7F4	2110-0438		FUSE 7A 125V SLO-BLO	28480	2110-0438
A7L1	9100-1788		COIL; FXD; NON-MOLDED RF CHOKE; .75UH	02114	VK200-20/4B
A7Q1	1854-0574		TRANSISTOR NPN SI PD=500MW FT=125MHZ	28480	1854-0574
A7Q2	1853-0364	1	TRANSISTOR TC-22 PD=40W	04713	MJE-701
A7Q3	1854-0574		TRANSISTOR NPN SI PD=500MW FT=125MHZ	28480	1854-0574
A7Q4	1853-0317		TRANSISTOR PNP SI CHIP PD=625MW	28480	1853-0317
A7Q5	1853-0317		TRANSISTOR PNP SI CHIP PD=625MW	28480	1853-0317
A7Q6	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q7	1854-0071		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A7Q8	1853-0365	1	TRANSISTOR SI PD=90W	04713	MJE2901K
A7Q9	1854-0640	1	TRANSISTOR SI PD=90W	04713	MJE2801K
A7R1	0683-3635	1	RESISTOR 36K 5% .25W CC TUBULAR	01121	CB3635
A7R2	0683-5125	1	RESISTOR 5.1K 5% .25W CC TUBULAR	01121	CB5125
A7R3	0683-3335	2	RESISTOR 33K 5% .25W CC TUBULAR	01121	CB3335
A7R4	0683-3025	1	RESISTOR 3K 5% .25W CC TUBULAR	01121	CB3025
A7R5	0683-1045	1	RESISTOR 100K 5% .25W CC TUBULAR	01121	CB1045
A7R6	0683-3035	4	RESISTOR 30K 5% .25W CC TUBULAR	01121	CB3035
A7R7	0683-3035		RESISTOR 30K 5% .25W CC TUBULAR	01121	CB3035
A7R8	0683-6235	2	RESISTOR 62K 5% .25W CC TUBULAR	01121	CB6235
A7R9	0683-3035		RESISTOR 30K 5% .25W CC TUBULAR	01121	CB3035
A7R10	0683-3035		RESISTOR 30K 5% .25W CC TUBULAR	01121	CB3035
A7R11	0811-1827		RESISTOR .1 OHM 10% 3W PW TUBULAR	91637	CW2B-1
A7R12	0683-2025		RESISTOR 2K 5% .25W CC TUBULAR	01121	CB2025
A7R13	0683-6235		RESISTOR 62K 5% .25W CC TUBULAR	01121	CB6235
A7R14	0683-1835	1	RESISTOR 18K 5% .25W CC TUBULAR	01121	CB1835
A7R15	0757-0917		RESISTOR 510 OHM 2% .125W F TUBULAR	24546	C4-1/8-T0-511-G

See introduction to this section for ordering information

Table 7-7. A7 Replaceable Parts for Series 1428A and Below (Continued)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A7R16	0761-0054	1	RESISTOR 330 OHM 5% 1W MO TUBULAR	24546	FP32-1-T00-331-J
A7R17	0757-0439		RESISTOR 6.81K 1% .125W F TUBULAR	24546	C4-1/8-T0-6811-F
A7R18	2100-2457		RESISTOR; VAR; TRMR; 2KOHM 10% C	19701	ET50W202
A7R19	0757-0956	2	RESISTOR 22K 2% .125W F TUBULAR	24546	C4-1/8-T0-2202-G
A7R20	0683-2025		RESISTOR 2K 5% .25W CC TUBULAR	01121	CB2025
A7R21	0683-5105		RESISTOR 51 OHM 5% .25W CC TUBULAR	01121	CB5105
A7R22	0683-2015	7	RESISTOR 200 OHM 5% .25W CC TUBULAR	01121	CB2015
A7R23	0757-0439		RESISTOR 6.81K 1% .125W F TUBULAR	24546	C4-1/8-T0-6811-F
A7R24	2100-2457		RESISTOR; VAR; TRMR; 2KOHM 10% C	19701	ET50W202
A7R25	0757-0956		RESISTOR 22K 2% .125W F TUBULAR	24546	C4-1/8-T0-2202-G
A7R26	0757-0959	1	RESISTOR 30K 2% .125W F TUBULAR	24546	C4-1/8-T0-3002-G
A7R27	0757-0917		RESISTOR 510 OHM 2% .125W F TUBULAR	24546	C4-1/8-T0-511-G
A7R28	0683-0565	1	RESISTOR 5.6 OHM 5% .25W CC TUBULAR	01121	CB56G5
A7R29	0683-1025		RESISTOR 1K 5% .25W CC TUBULAR	01121	CB1025
A7R30	0683-1025		RESISTOR 1K 5% .25W CC TUBULAR	01121	CB1025
A7R31	0811-1827		RESISTOR .1 OHM 10% 3W PW TUBULAR	91637	CW2B-1
A7R32	0683-3335		RESISTOR 33K 5% .25W CC TUBULAR	01121	CB3335
A7R33	0683-2025		RESISTOR 2K 5% .25W CC TUBULAR	01121	CB2025
A7R34	0683-1005		RESISTOR 10 OHM 5% .25W CC TUBULAR	01121	CB1005
A7R35	0683-1005		RESISTOR 10 OHM 5% .25W CC TUBULAR	01121	CB1005
A7S1	3103-0032		SWITCH-THRM FXD 194F 3A OPN ON RISE	28480	3103-0032
A7U1	1826-0024		IC LIN MC 1469R REGULATOR	04713	MC1469R
A7U2	1826-0147	1	IC LIN REGULATOR	07263	7812UC
	1205-0219	1	HEAT-DISSIPATOR; SGL; SHUNT PKG	28480	1205-0219
A7U3	1826-0106	2	IC LIN REGULATOR	07263	7815UC
A7U4	1826-0032		IC LIN MC 1463R REGULATOR	04713	MC1463R
A7U5	1826-0106		IC LIN REGULATOR	07263	7815UC

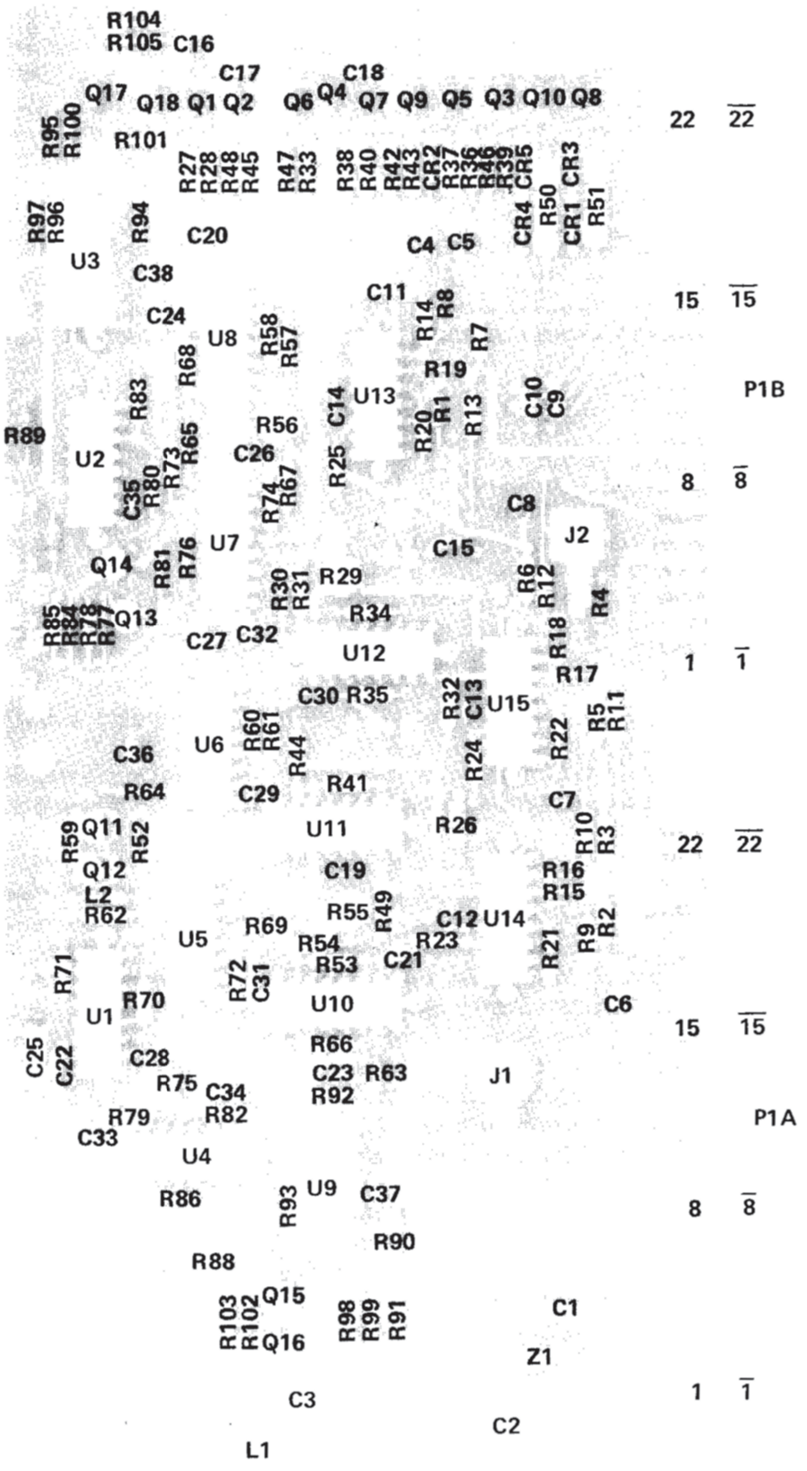


Figure 7-14. A9 Component Locator, Series 1332A

SECTION VIII

SCHEMATIC DIAGRAMS

8-1. SCHEMATIC DIAGRAMS

8-2. This section contains schematic diagrams, assembly and chassis part locators, component locators, block diagrams, waveforms, test points, and troubleshooting information. The schematics are presented in assembly number order A1 through A19. The component, chassis, and assembly locators show the location by reference designator. The block diagrams give a simplified block of the corresponding schematic diagram.

8-3. SCHEMATIC DIAGRAM NOTES, ASSEMBLY NUMBERS, AND REFERENCE DESIGNATORS

8-4. Figure 8-1 shows the symbols used on the schematic diagrams. The bottom of Figure 8-1 shows the method for assigning reference designators, assembly numbers, and subassembly numbers.

8-5. Reference Designations

8-6. Assemblies such as printed-circuit boards are assigned numbers in sequence, A1, A2, etc. As shown in Figure 8-1, subassemblies within an assembly are given a subordinate A number. For example, rectifier subassembly A1 has the complete designator of A25A1. For individual components, the complete designator is determined by adding the assembly number and subassembly number, if any. For example, CR1 on the rectifier assembly is designated A25A1CR1.

8-7. Identification Markings on Printed-Circuit Boards

8-8. HP printed-circuit boards (see Figure 8-1) have four identification numbers; an assembly part number, a series number, a revision letter, and a production code.

8-9. The assembly part number has 10 digits (such as 05345-60009) and is the primary identification. All assemblies with the same part number are interchangeable. When a production change is made on an assembly that makes it incompatible with previous assemblies, a change in part number is required. The series number (such as 1340A) is used to document minor electrical changes. As changes are made, the series number is incremented. When replacement boards are ordered, you may receive a replacement with a different series number. If there is a difference between the series number marked on the board and the schematic in this manual, a minor electrical difference exists. If the number on the printed-circuit board is lower than that on the schematic, refer to Section VII for backdating information. If it is higher, refer to the loose leaf manual change sheets for this manual. If the manual change sheets are missing, contact your local Hewlett-Packard Sales and Service Office. See the listing on the back cover of this manual.

8-10. Revision letters (A, B, etc.) denote changes in printed-circuit layout. For example, if a capacitor type is changed (electrical value may remain the same) and requires different spacing for its leads, the printed-circuit board layout is changed and the revision letter is incremented to the next letter. When a revision letter changes, the series number is also usually changed. The production code is the four-digit, seven-segment number used for production purposes.

Table 8-1. Signal Line Descriptions and Destinations

1. **Static Control Line (SCL).** Stays in one state throughout measurement or while controlled externally.
2. **Dynamic Control Line (DCL).** Changes state during some phase of measurement.
3. **Signal Line (SL).** Dynamic line changing state at some frequency. Directly used in measurement, e.g., Channel A input signal or a derivative, or Time Base signal or a derivative.
4. **Clock Line (CL).** Dynamic line changing state at some frequency. Initiates a sequence of events.
5. **Data Line (DL).** Code line carrying measurement information. Changes state with new data.

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
A-B SW	A12B(20), S8	A10A(14), A16(35)	A-B Switch (SCL-TTL). Used in START to totalize Channel A counts plus Channel B counts *or* Channel A counts minus Channel B counts. In remote operation, line is controlled by A12. When *not* in remote, line is controlled by S8. A+B mode forces line Low.
ADD	A15A($\overline{11}$)	A13A($\overline{11}$)	(DCL-TTL). Used during process cycle. Instructs Add/Subtract circuit on A13 to perform addition (High) or subtraction (Low).
$\overline{\text{ARM}}$	A11B(17)	A10B($\overline{17}$)	(DCL-TTL). Goes Low after rundown of sample rate to set Arm F-F (A10). Can be forced Low by $\overline{\text{PI ARM}}$, $\overline{\text{FORCED ARM}}$, $\overline{\text{ST+STP}}$, or a reset.
ARMED	A10B(7)	A2P1(7), A17J1(13) via A17J2(39), A16(13)	(DCL-TTL). Goes High when Arm F-F (A10) sets. Causes front panel ARM lamp to light. Instructs plug-in that counter is armed.
$\overline{\text{ASTERISK}}$	A7B($\overline{1}$)	A2P1($\overline{9}$)	(DCL-TTL). A result of the OSC HTR line (A18) going High to indicate that the oscillator oven temperature is too low. Also active from DIG ASTERISK line being set High by Asterisk F-F on A15.
$\overline{\text{AUT}}$	A14B(3)	A13B($\overline{3}$)	Automatic (SCL-TTL). When Low, used to select the multiplier from QMC in automatic routine. Goes High when a fixed display position code (manual mode) is selected for use.
$\overline{\text{AUT+AUT SC • LOC MUL}}$	A13A($\overline{13}$)	A14A(13)	Auto or Auto Single Cycle and Local Multiplier (DCL-TTL). Causes auto decimal point alignment routine when DISPLAY POSITION switch is set to AUTO. Causes a single auto decimal point alignment routine when switch is *not* in AUTO (manual) and a reset is generated.
$\overline{\text{AUT DP ALN}}$	A15B($\overline{1}$)	A14B($\overline{1}$)	Auto Decimal Point Align (DCL-TTL). A qualifier line that goes Low to indicate that the decimal point is properly aligned and the correct multiplier is selected during Auto display.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{AUT SC}}$	A11B(15)	A13B(15)	Auto Single Cycle (DCL-TTL). Generated on A11 when counter is reset while in manual mode and not remotely programmed. Forces one measurement in auto mode to align decimal point and multiplier. Causes generation of $\overline{\text{AUT+AUT SC}}$ • $\overline{\text{LOC MUL}}$ qualifier from A13.
$\overline{\text{COMP DUMP}}$	A12A(18)	A14A($\overline{18}$)	Computer Dump (DCL-TTL). An externally programmed condition. This line is a qualifier signal. It causes the DR to output 32 characters to A12 for the output routine. The first 16 characters are from the DR and the next 16 from the NR.
$\overline{\text{DC = DS}}$	A15A($\overline{17}$)	A14A($\overline{17}$)	Digit Counter Equals Digit Storage (DCL-TTL). Active Low qualifier line, indicating that sufficient divisions have occurred to produce proper resolution for gate time being used. DS contains number of digits that were in time scaler. DC increments with each digit that is resolved during division process.
DC SER OUT A	A15A($\overline{16}$)	A12A($\overline{15}$)	Digit Counter Serial Output (DCL-TTL). The three line code controls the order of output data from A12. See Table 4-2, A12 ROM Sequence.
DC SER OUT B	A15A($\overline{13}$)	A12A($\overline{13}$)	
DC SER OUT C	A15A($\overline{18}$)	A12A($\overline{12}$)	
DC = 0	A15A(17)	A14A(17)	Digit Counter Equals zero (DCL-TTL). Active High qualifier line. Sometimes used as qualifier director. Also used to determine value of other counters, e.g., QMC=0 • DC=0.
DC = 8	A15B(4)	A14B($\overline{3}$)	Digit Counter Equals Eight (DCL-TTL). Active High qualifier, indicating the digit counter serial output ROM sequence is complete and processor should return to main processor program.
DECADE RST	A10A($\overline{17}$)	A9A(17)	Decade Reset (DCL-TTL). Resets Time and Events scalers on A11. Goes High with $\overline{\text{SET AUT SC}}$ or RST FRONT END when $\overline{\text{ST+STP}}$ line is Low.
DIG ASTERISK	A15B($\overline{8}$)	A7B(1)	Digit Asterisk (DCL-TTL). A result of setting the Asterisk F-F on A15. Conditions for setting F-F are overflow, underflow, or factitious zeros.
DISP CLK	A14B(6)	A2P1($\overline{3}$), A15B(6)	Display Clock (CL-TTL). Used during display cycle to strobe time and events scalers and data from DR at a slower rate than normally available. The signal is a divided version of $\overline{\text{DPLK CLK}}$, which is, itself, derived from $\overline{\text{ROM CLK}}$. DISP CLK is sent to A15, where it is converted to REG CLK for use in the display cycle strobing.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
DISP CLK EN	A15B($\overline{9}$)	A2P1($\overline{14}$) via A16(54), A11B($\overline{12}$), A13B(8)	Display Clock Enable (DCL-TTL). At start of display cycle, goes High to enable anode driver circuit (A2). Turns on Sample Rate circuit (A11). Allows circuit on A13 to decide if it will output a twelfth DRC code to light the minus sign.
$\overline{\text{DISP STR}}/\overline{\text{INH PROC}}$	A17J1(15) via A17J2(35)	A10B(22), A14A($\overline{22}$)	Display Storage/Inhibit Processor (DCL-TTL). Time shared control line from processor. Active when plug-in is storing the mainframe display. Can cause processor to calculate a 14 digit quotient result when more than one division process is required. When Low, it also prevents a process cycle by keeping the $\overline{\text{INIT PROC}}$ line High.

DP A	A14B($\overline{14}$)
	A17J1(43) via A17J2(27)
		A2P1(15),
		A15B(14),
		A16(1)
			Decimal Point (DL-TTL). A2 assembly uses code to light decimal point in the display. A15 assembly uses code to help determine placement of decimal point and proper annunciator. The A14 assembly usually outputs the code on these lines, but can also accept a decimal point code from the plug-in on the same lines.

DP B	A14B($\overline{17}$)
	A17J1(7) via A17J2(51)
		A2P1(12),
		A15B(17),
		A16(3)	

DP C	A14B($\overline{18}$)
	A17J1(8) via A17J2(49)
		A2P1(16),
		A15B(18),
		A16(5)	

DP D	A14B($\overline{15}$)
	A17J1(20) via A17J2(29)
		A2P1(17),
		A15B(15),
		A16(2)	

DP E	A14B($\overline{13}$)
	A17J1(17) via A17J2(33)
		A15B(13)	

DP F	A14B($\overline{16}$)
	A17J1(6) via A17J2(53)		

$\overline{\text{DPLK CLK}}$	A15B($\overline{18}$)	A14B(18)	Decimal Point Locator for K, Clock (CL-TTL). In the display cycle, this line is divided by 8 and results as DISP CLK. When DPLR<DPLK, the line is used to decrement the DPLK counter until the decimal point codes are equal.
$\overline{\text{DPLR CLK}}$	A15B($\overline{15}$)	A14B(15)	Decimal Point Locator for Result, Clock (DCL-TTL). This line clocks the DPLR counter. Used in decimal point alignment.
$\overline{\text{DPLR UP}}$	A15B(7)	A14B($\overline{7}$)	Decimal Point Locator for Result Up (DCL-TTL). When High, allows each $\overline{\text{DPLR CLK}}$ pulse to decrement the DPLR counter (A14). When Low, allows each clock pulse to increment the counter.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS FROM	CONNECTOR AND PINS TO	DESCRIPTION
$\overline{\text{DPLK}\leftarrow\text{-1}}$	A15B($\overline{6}$)	A14B($\overline{6}$)	Decimal Point Locator for K Assign minus one (DCL-TTL). Used as a reset signal for the DPLK counter. Sets the counter's output lines (A,B,C, D,E, and -/+) High.
$\overline{\text{DPLK}\leftarrow\text{DPLK\_PI}}$	A15B($\overline{17}$)	A14B(17)	DPLK Assign DPLK with Plug-In (DCL-TTL). Active Low ROM command. Causes decimal point data from plug-in to be sent to mainframe DPLK counter (A14).
$\overline{\text{DPLR}\leftarrow\text{-1}}$	A15B(16)	A14B(16)	Decimal Point Locator for Result Assign minus one (DCL-TTL). Used as a reset signal for the DPLR counter. Sets all counter outputs High.
DPLR=+	A14B(22)	A15B(22)	Decimal Point Locator for Result Equals Plus (DCL-TTL). Goes High to indicate that decimal point is in viewable range. Combines with NANO MULT line (both Low) to force an auto decimal point align ($\overline{\text{AUTO DP ALN}}$ line).
DPLR<16	A14A(20)	A12A(21)	Decimal Point Locator for Result is less than 16 (DCL-TTL). Qualifier used to determine the direction the decimal point is away from the quotient's MSD. Also, used in determining when to output the decimal point in the output routine (A12).

DR A	A13A(7)
	A17J1(63) via A17J2(21)
		A2P1(4),
		A16(21)
			Denominator Register (DL-TTL). When the $\overline{\text{PI XMT}}$ line is High, the DR outputs its data on these lines to the display and the plug-in. When $\overline{\text{PI XMT}}$ is Low, the DR accepts data from the plug-in.

DR B	A13A(5)
	A17J1(57) via A17J2(19)
		A2P1($\overline{5}$),
		A16(19)	

DR C	A13A(6)
	A17J1(61) via A17J2(26)
		A2P1($\overline{4}$),
		A16(26)	

DR D	A13A($\overline{6}$)
	A17J1(59) via A17J2(27)
		A2P1(5),
		A16(27)	

$\overline{\text{DRC}\leftarrow\text{0}}$	A15A($\overline{12}$)	A13A(12)	Denominator Register Counter Assign Zero (DCL-TTL). Active Low ROM command. Resets the DR counter to zero. Required after every display state, since display state could leave counter at any location.
DR CLK EN	A15A($\overline{22}$)	A13B($\overline{21}$)	Denominator Register Clock Enable (DCL-TTL). When High, allows the DR counter outputs to increment with each REG CLK pulse.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS FROM	CONNECTOR AND PINS TO	DESCRIPTION
DR EN A	A15B(21)	A13B($\overline{21}$)	Denominator Register Enable (DCL-TTL). Presents a 3-line code to the DR (A13) that controls and directs the shifting of data to and from the register.
DR EN B	A15A($\overline{8}$)	A13A(8)	
DR EN C	A15A($\overline{9}$)	A13A($\overline{8}$)	
DRC A	A13A(19)	A2P1($\overline{15}$) via A16(23), A11A($\overline{19}$)	Denominator Register Counter (DCL-TTL). A 4-line code used to strobe data out of the scalers (A11). Also used to strobe measurment data out of the DR and enable the proper LED in the display for each DR digit.
DRC B	A13A(20)	A2P1($\overline{12}$) via A16(25), A11A($\overline{20}$)	
DRC C	A13A(21)	A2P1($\overline{16}$) via A16(10), A11A($\overline{21}$)	
DRC D	A13A(13)	A2P1($\overline{17}$) via A16(8), A11A(13)	
DS<3	A15A(20)	A14A($\overline{20}$)	Digit Storage Less Than Three (DCL-TTL). A qualifier line that, when High, indicates the resolution of measurement is less than three digits. Causes the decimal point and multiplier to remain in their current positions.
EFC	A8A(4, $\overline{4}$)	A18(6, $\overline{6}$)	Electronic Frequency Control. Used to control the frequency of the internal oscillator (A18) when using an external standard. Line varies from -10V to +5V and causes VCO on A18 to phase lock internal oscillator to external standard.
$\overline{\text{EVT GATE}}$	A9B($\overline{19}$)	A10B(19)	Event Gate (DCL-ECL). Goes Low when the Event Gate F-F sets. Causes front panel GATE lamp to light and MEAS TIME line to enable Excessive Gate Time F-F (A11). Starts process cycle when $\overline{\text{EVT GATE}}$ and $\overline{\text{TIME GATE}}$ go High to cause $\overline{\text{INIT PROC}}$ to go Low. Initiates signal for GATE OUTPUT jack.
EVT+RAT+ST+STP	A10B(4)	A14B(1)	Events or Ratio or Start or Stop (SCL-TTL). A result of decoding the FUNCTION switch code. Line is High in any of these modes. Used as a qualifier to indicate to the processor which function has been selected.
EVT SCLR A	A11A($\overline{16}$)	A13A(16)	Events Scaler (DL-TTL). At beginning of process cycle, these lines transfer Events Scaler data (in BCD) from A11.
EVT SCLR B	A11A($\overline{15}$)	A13A(15)	
EVT SCLR C	A11A(9)	A13A(9)	
EVT SCLR D	A11A($\overline{10}$)	A13A(10)	

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{EVT SCLR A}_0}$	A9A($\overline{5}$)	A11A(5)	Event Scaler (DL-EECL). A four-line code from a divide-by-10 stage in the events scaler (A9). At the end of the gate time, this decade holds the least significant digit in the event count.
$\overline{\text{EVT SCLR B}_0}$	A9A(6)	A11A($\overline{6}$)	
$\overline{\text{EVT SCLR C}_0}$	A9A(5)	A11A($\overline{5}$)	
$\overline{\text{EVT SCLR D}_0}$	A9A($\overline{8}$)	A11A(8)	
EVT SCLR A1	A9A($\overline{7}$)	A11A(7)	Events Scaler A1 (SL-ECL). Derivative of Channel A signal. Has been divided by 20 in scaler on A9 before being sent to remainder of scalers on A11. Complement of $\overline{\text{EVT SCLR A1}}$.
$\overline{\text{EVT SCLR A1}}$	A9A($\overline{6}$)	A11A(16)	Events Scaler A1 (SL-ECL). Derivative of Channel A signal. Has been divided by 20 in scaler on A9 before being sent to remainder of scalers on A11. Complement of EVT SCLR A1.
EXT AB	A10A(20)	A9A(16)	External AB (SCL-EECL). Controlled from plug-in by $\overline{\text{SEL A•B}}$. When $\overline{\text{SEL A•B}}$ is High, EXT AB is Low and allows the mainframe's channel A and B signals to be used. When $\overline{\text{SEL A•B}}$ is Low, EXT AB is High and allows the mainframe to use the plug-in's Channel A AND B signals. Also turns off Schmitt trigger circuits on A4, preventing front panel signals from entering control circuits on A9.
EXT C	A10B(14)	A9B($\overline{14}$)	External C (SCL-EECL). Controlled from plug-in by $\overline{\text{SEL C}}$ line. Used when measuring events of Channel C occurring between Channel A pulse and Channel B pulse. Causes Time Scaler to accept Channel C signal instead of Time Base signal.
$\overline{\text{EXT OUT EN}}$	A15A(9)	A12A($\overline{8}$)	External Out Enable (DCL-TTL). An active Low ROM command. Used with FLAG command on A12 to generate Data Valid (DAV) signal to the recording device.
$\overline{\text{FP CHK}}$	A4P2($\overline{18}$)	A10A(8, $\overline{8}$)	Front Panel Check (SCL-TTL). Combined on A10 with the FUNCTION switch codes. Operational only when using front panel controls. Forces selection of A+B, regardless of ACCUM MODE START/STOP switch position. Causes TEST line to select 100 MHz test signal for measurement and turn off front panel input trigger circuits.
FP DISP POS A	S5, A4J1($\overline{4}$), A4J2($\overline{12}$)	A14B($\overline{10}$)	Front Panel Display Position (SCL-TTL). The 4-line code fixes the decimal point position in the display. The DPLR counter is incremented or decremented until its code equals the FP DISP POS code.
FP DISP POS B	S5, A4J1($\overline{5}$), A4J2($\overline{11}$)	A14B($\overline{11}$)	
FP DISP POS C	S5, A4J1(3), A4J2($\overline{13}$)	A14B($\overline{9}$)	
FP DISP POS D	S5, A4J1(4), A4J2(11)	A14B($\overline{12}$)	

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS FROM	CONNECTOR AND PINS TO	DESCRIPTION
FP FUNC A	S1 via A4J1(9), A5(7)	A10A(6)	Front Panel Function (SCL-TTL). When using front panel controls, lines provide a 3-line code to program the desired operating mode (freq, period, TI, etc).* Code list is on the switch schematic. Codes are decoded on A10 to provide several static control lines. *These lines are selected for use when $\overline{\text{RMT}}$ is High.
FP FUNC B	S1 via A4J1(10), A5(6)	A10A(5)	
FP FUNC C	S1 via A4J1(8), A5($\overline{6}$)	A10A(4)	
FP GT A	S4 via A4J1($\overline{9}$), A5(5)	A11A(18)	Front Panel Gate Time (SCL-TTL). When using front panel controls, lines provide a 4-line code to program the desired gate time (1s, 1μs, etc.). These lines are selected for use when $\overline{\text{RMT}}$, $\overline{\text{PROC BUSY}}$, and $\overline{\text{PI DISP POS}}$/$\overline{\text{GT SEL}}$ lines are High. Code list is shown on switch schematic. Lines are decoded to enable one of the Time Scalers (A11) to output a 5 code.
FP GT B	S4 via A4J1(7), A5($\overline{8}$)	A11A(19)	
FP GT C	S4 via A4J1($\overline{6}$), A5(8)	A11A(20)	
FP GT D	S4 via A4J1($\overline{7}$), A5(8)	A11A(14)	
$\overline{\text{FORCED ARM}}$	A10B($\overline{21}$), A12B(21)	A11B($\overline{21}$)	(DCC-TTL) Causes counter to arm when EXT CONTROL jack receives an arm pulse with switch in EXT ARM position or in remote operation.
FUNC SW RST	S1 FUNC SW	A11A(21)	Function Switch Reset (DCL-TTL). A reset signal generated between switch positions of FUNCTION switch. Not active when in remote operation. Generates lamp test. Forces a single automatic measurement while in manual by activiating $\overline{\text{AUT SC}}$ and $\overline{\text{SET AUT SC}}$. Causes $\overline{\text{RST}}$ lines to go Low.
GATE ARM	A10A(15)	A9A($\overline{15}$)	(DCL-ECL) When High (-0.7V), enables Event Gate F-F (on A9) to set with next Channel A pulse. Complements $\overline{\text{GATE ARM}}$ line.
$\overline{\text{GATE ARM}}$	A10A(16)	A9A($\overline{16}$)	(DCL-ECL) When Low (-1.4V), enables Event Gate F-F (on A9) to set with next Channel A pulse. Complements GATE ARM line.
$\overline{\text{GATE CONTROL}}$	A10B(12)	J4 (rear panel)	Allows counter's main gate/arm circuits to be controlled from external source. Requires 0V to -1V pulse.
$\overline{\text{GATE LITE}}$	A10A(9, $\overline{9}$)	A2P1($\overline{7}$), A16(7)	Gate Light (DC-TTL). Used to light the GATE lamp on A1. Goes Low with first Channel A pulse after counter is armed. Line stays Low for 40 ms after main gate closes, then returns High to turn off light.
GATE RST	A10A(19)	A9A(15)	Gate Reset (DCL-ECL). Rests the Event Gate and Time Gate flip-flops on A9. Generated by $\overline{\text{SET AUT SC}}$ or RST FRONT END when $\overline{\text{ST+STP}}$ is High.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS FROM	CONNECTOR AND PINS TO	DESCRIPTION
GATED RFD	A12A(10)	A14A($\overline{9}$)	Gated Ready for Data (DCL-TTL). A qualifier that instructs the processor to output a character from A12 to the Interface Bus.
GATED DAC	A12A($\overline{20}$)	A14A($\overline{19}$)	Gated Data Accepted (DCL-TTL). A qualifier line that indicates to the processor that the recording device has received the character, hence the processor prepares to output the next character.
GT+DISP POS RST	S4, S5 via A5(10)	A10A(22)	Gate Time or Display Position Reset (SCL-TTL). A reset signal generated between switch positions of GATE TIME switch or DISPLAY POSITION switch. Causes $\overline{\text{RST}}$ and $\overline{\text{LAMP TEST}}$ lines to go Low, but does not produce a single auto measurement while in manual mode ($\overline{\text{AUT SC}}$ and $\overline{\text{SET AUT SC}}$ lines) as would the front panel RESET switch.
HOLD	A12A(9), SAMPLE RATE POT via A5($\overline{7}$) & A4($\overline{8}$)	A11A(12)	(SL-TTL) When High, causes counter to hold displayed measurement, indefinitely. Prevents sample rate circuit on A11 from turning on and prevents the counter from rearming (A10).
$\overline{\text{Hz LITE}}$	A10A(7)	A1J1($\overline{21}$), A2P1($\overline{8}$) via A5($\overline{7}$), A16(20)	Hertz Light (SCL-TTL). A result of decoding the function codes on A10. Goes Low to turn on the front panel Hz light for frequency measurements.
$\overline{\text{INIT PROC}}$	A10B($\overline{5}$)	A14B(5)	Initialize Processor (DCL-TTL). Signals the beginning of the process cycle. Goes Low when measurement cycle is complete and the main gate closes.
INP LEVEL A	A4P2(12) via A5(12)	A9B(17)	Input Level A. DC voltage that is variable from +0.5V to -0.5V with front panel LEVEL pot. Voltage determines trigger point. Line provides voltage to rear panel jack.
INP LEVEL B	A4P2(18) via A5(18)	A9B(16)	Input Level B. DC voltage that is variable from +0.5V to -0.5V with front panel LEVEL pot. Voltage determines trigger point. Line provides voltage to rear panel jack.
$\overline{\text{K DATA/PI INH ARM}}$	A17J1(40) via A17J2(36)	A11B($\overline{20}$), A14A($\overline{15}$)	K Data/Plug-In Inhibit Arm (DCL-TTL). Time shared control line from plug-in. $\overline{\text{K DATA}}$ indicates that K data is available from plug-in. Causes processor to select K data routine. $\overline{\text{PI INH ARM}}$ allows plug-in to control counter's measurement phase by inhibiting the arming.
$\overline{\text{LAMP TEST}}$	A8A(3, $\overline{3}$), A11A($\overline{22}$)	A2P1(3) via A16(9), A13A(22)	(DCL-TTL) When Low, causes lamp test condition. Activated by excessive gate time, a reset signal, or by attempt to lock an external frequency standard to internal oscillator.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
LOAD MS	A15B(5)	A11B($\overline{16}$), A13B($\overline{6}$)	Load Multiplier Storage (DCL-TTL). Clocks the annunciator code of QMC or the Remote Multiplier into the Multiplier Storage flip-flops (A13) during auto mode. Clocks Auto Single Cycle flip-flop (A11) after a manual reset to generate one auto measurement while in the manual mode.
$\overline{\text{LOC MULT}}$	A13B($\overline{5}$)	A14B($\overline{4}$)	Local Multiplier (SCL-TTL). Goes Low only when the RMT MULT lines are *not* being used. Indicates source of MULT code to qualifier board for purpose of altering internal program flow.
MEAS TIME	A10B($\overline{18}$)	A11B($\overline{18}$), A17J1(42) via A17J2(28)	Measurement Time (DCL-TTL). When Low, prevents Excessive Gate Time F-F from setting as scaler data is fed to processor. When High, enables the Excessive Gate Time F-F (A11). High for duration of actual measurement time. Signal indicates to plug-in that mainframe is in measurement phase.
MIN GATE TIME	A11B($\overline{2}$)	A10B($\overline{2}$), A14B(14)	Minimum Gate Time (SCL-TTL). Goes High when GATE TIME lines are decoded in A11 to detect MIN. Prevents $\overline{\text{NOISE CONTROL}}$ from going Low when not in START or STOP. Used to set Resolution F-F (A10) when $\overline{\text{TIME GATE}}$ goes Low to stop measurement on next channel A pulse. Used as qualifier to A14.
MSB	A15B($\overline{20}$)	A15B($\overline{19}$)	Most Significant Bit (DCL-TTL). Used in conjunction with state variable lines (SV1(T), etc.) to address ROMs. Used with one set of state variable codes to output two sets of ROM program codes. When MSB=1, addresses locations 128 to 256; when MSB=0, addresses locations 0 to 127.
MULT STR A	A13A(3)	A1J1(19), A2P1(11), A12A($\overline{3}$), A16(18)	Multiplier Storage (DCL-TTL). Stores the QMC code that represents the annunciator. Sends this code to A1 and A2 to display annunciator and to A12 when outputting measurement result.
MULT STR B	A13A($\overline{3}$)	A1J1(18), A2P1($\overline{11}$), A12A(3), A16(22)	
MULT STR C	A13A($\overline{4}$)	A1J1(17), A2P1(10), A12A(4), A16(24)	

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
MV EXT	External Source	A15B($\overline{16}$)	Multivibrator External (SCL–TTL). An externally applied signal used to step the counter through its timing sequence at a rate convenient for troubleshooting. Must be used with another external signal, $\overline{\text{MV EXT EN}}$. External signal must be TTL.
$\overline{\text{MV EXT EN}}$	External Source	A15B(11)	Multivibrator External Enable (SCL–TTL). When Low, it disables the MV from generating the processor timing and associated pulses; $\overline{\text{ROM CLK}}$, MSB, $\overline{\text{WORD DBL CLK}}$, etc. It allows substitution of an external signal on the MV EXT line to produce these timing pulses at a convenient rate for troubleshooting. External signal must be TTL.
NANO MULT	A10A($\overline{22}$)	A1J1($\overline{17}$), A2P1($\overline{10}$), A12A($\overline{22}$), A14A(22), A15A(22), A16(12)	Nano Multiplier (SCL–TTL). A result of decoding the function codes on A10. High for a period or time interval measurement. Used as a qualifier in A14 to determine whether DPLR should be incremented or decremented. Used in A15 to help force a decimal point alignment for sub-nanosecond T.I. measurements. Used in A1 and A2 to change annunciator coding. Used in A12 talk mode to indicate the exponent is >1 or <1, e.g., M or μ.
$\overline{\text{NOISE CONTROL}}$	A10B($\overline{15}$)	A8A(5, $\overline{5}$)	(SCL–TTL). Goes Low to turn on Noise Generator (A8) to noise modulate the time base signal. Goes Low when GATE TIME switch is *not* set to MIN while GATE CONTROL switch is set to EXT GATE or when FUNCTION switch is set to TIME INT A to B.
NR CLK EN	A15A(12)	A13A($\overline{10}$)	Numerator Register Clock Enable (DCL–TTL). Active during process cycle for purpose of shifting data. Each time it goes High, it enables the NR counter to be clocked by REG CLK.

NR EN A
NR EN B
	A15A($\overline{7}$)
	A15B($\overline{10}$)
		A13A($\overline{7}$)
		A13B($\overline{11}$)
			Numerator Register Enable (DCL–TTL). Presents a 2-line code to the NR (A13) that controls and directs the shifting of data to and from the register.

$\overline{\text{NR(NRC)=0 • QMC=0}}$	A13A($\overline{19}$)	A14A(19)	Numerator Register (NR Counter) Equals Zero and Quotient Multiplier Counter Equals Zero (DCL–TTL). Used in divide routine to determine when the first quotient digit has been calculated. When this occurs, QMC no longer equals zero and another routine is selected.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
NR(NRC) ⩾5	A13A($\overline{12}$)	A14A(12)	Numerator Register (NR Counter) Equal to or Greater than five (DCL–TTL). A qualifier signal used to ensure the ±2 count accuracy error is not exceeded. During Period (in MIN) and T.I. (in MIN), only.
$\overline{\text{PB RST}}$	S3 RESET SW	A11A($\overline{7}$) & A12A(14) via A4 & A5	Pushbutton Reset (SCL–TTL). Goes Low when front panel RESET switch is pushed. Not active when in remote operation. Generates lamp test. Forces a single automatic measurement while in manual by activating $\overline{\text{AUT SC}}$ and $\overline{\text{SET AUT SC}}$. Causes $\overline{\text{RST}}$ line to go Low.
PER + TI	A10A($\overline{11}$)	A14A(11)	Period or Time Interval (SCL–TTL). A result of decoding the FUNCTION switch code. Line is High if counter is in either mode. Used as a qualifier to indicate to the processor which function has been selected.
$\overline{\text{PI ARM}}$	A17J1(41) via A17J2(30)	A11B($\overline{19}$)	Plug-In Arm (DCL–TTL). Goes Low to allow plug-in to arm counter.
PI CH A	W5J1(2)	A16J3, A9A(18)	Plug-In Channel A (SL–EECL). Substitutes for mainframe Channel A signal as a measurement signal.
PI CH B	W5J1(5)	A16J2, A9A(21)	Plug-In Channel B (SL–EECL). Substitutes for mainframe Channel B signal as a measurement signal.
PI CH C	W5J1(21)	A16J1, A9B(8)	Plug-In Channel C (SL–EECL). Measurement signal from plug-in. Used for an events measurement, i.e., where PI CH C pulses accumulate in Events Scaler (A11) during time between Channel A pulse and Channel B pulse.
PI CLK	A15B(12)	A17J1(16) via A17J2(34)	Plug-in Clock (CL–TTL). Used to clock K DATA, N DATA, or plug-in data from the plug-in.
$\overline{\text{PI CLK EN}}$	A15A($\overline{6}$)	A17J1(21) via A17J2(26)	Plug-In Clock Enable (DCL–TTL). Enables plug-in's counter to clock K data, N data, or plug-in data from plug-in.
$\overline{\text{PI DATA}}$	A17J1(14) via A17J2(37)	A10B($\overline{8}$), A14B(7)	Plug-In Data (DCL–TTL). Goes Low to request 16 BCD digits and a decimal point code from the plug-in. Data is sent in Giga or Nano units.
$\overline{\text{PI DISP POS}}$/$\overline{\text{GT SEL}}$	A17J1(10) via A17J2(45)	A11B($\overline{3}$), A14B(20)	Plug-In Display Position/Gate Time Select (SCL–TTL). Enables counter to accept gate time codes or display position codes from plug-in.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
PI FUNC A	A17J1(36) via A17J2(44)	A10B(11)	Plug-In Function (SCL-TTL). Used on A10 to operate counter according to selected function of plug-in. Code is enabled for use when 5345 FUNCTION switch is set to PLUG-IN.
PI FUNC B	A17J1(11) via A17J2(43)	A10B(9)	
PI FUNC C	A17J1(12) via A17J2(41)	A10B(8)	
$\overline{\text{PI INH ANUN}}$	A17J1(35) via A17J2(46)	A10A($\overline{4}$)	Plug-In Inhibit Annunciator (DCL-TTL). Goes Low to blank Hz or SEC lamp during display.
$\overline{\text{PI INV SIGN}}$	A17J1(27) via A17J2(62)	A15B(20)	Plug-In Invert Sign (DCL-TTL). Allows plug-in to define sign of result data or displayed data being sent to mainframe.
PI GT/DISP POS A	A17J1(9) via A17J2(47)	A11B(5), A14B($\overline{19}$)	Plug-In Gate Time/Display Position (SCL-TTL). The 4-line code from the plug-in selects the counter's gate time in A11 when enabled by a Low $\overline{\text{PI DISP POS}}$/$\overline{\text{GT SEL}}$ signal. The code is used with the same enable signal to select the display position in A14. This code may or may not be used, depending on the selected qualifier.
PI GT/DISP POS B	A17J1(28) via A17J2(60)	A11B($\overline{6}$), A14B($\overline{20}$)	
PI GT/DISP POS C	A17J1(30) via A17J2(56)	A11B($\overline{9}$), A14B($\overline{22}$)	
PI GT/DISP POS D	A17J1(29) via A17J2(58)	A11B($\overline{11}$), A14B($\overline{21}$)	
$\overline{\text{PI RST}}$	A17J1(34) via A17J2(48)	A11B(20)	Plug-In Reset (SCL-TTL). Signal from the plug-in. Line goes Low to reset the 5345. Same type of reset as front panel pushbutton reset ($\overline{\text{PB RST}}$).
$\overline{\text{PI SEL}}$	A10A($\overline{21}$)	A17J1(39) via A17J2(38)	Plug-In Select (SCL-TTL). A result of decoding the FUNCTION switch code on A11 (PLUG-IN position code). Enables plug-in measurements to be made.
PI • [$\overline{\text{SIGN-}}$] + $\overline{\text{PI}}$ • [CHK + ($\overline{\text{A-B}}$) SW]	A10A($\overline{16}$)	A14A(16)	(SCL-TTL). See Sheet 3M of Processor Flow Chart theory for description.
$\overline{\text{PI XMT}}$	A14A($\overline{12}$)	A13A(18), A15A($\overline{19}$), A17J1(5) via A17J2(55)	Plug-In Transmit (DCL-TTL). Goes Low to allow the plug-in to transmit data and decimal point into the DR via the bidirectional bus. Allows counter to input minus sign from plug-in by turning off internal sign circuit on A15.
PLUS	A13A($\overline{14}$)	A14A(14)	(DCL-TTL). A14 examines state of this line after a subtraction (all 16 digits) in A13. If line is High, subtraction was successful and another subtraction is attempted. If line is Low, DR was greater than NR (unsuccessful); contents of NR must be shifted one place and subtraction tried again. When Low (after 16-digit subtraction) contents of QMC shift into QR.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{PROC BUSY}}$	A15B(8)	A11B($\overline{8}$), A17J1(32) via A17J2(52)	Processor Busy (DCL–TTL). Goes Low during process cycle. An indirect result of $\overline{\text{INIT PROC}}$. On A11, it causes circuits to select DRC codes for strobing data out of scalers. Inhibits plug-in from sending measurement data.
QMC CLK	A15A(15)	A13A($\overline{16}$)	Quotient Multiplier Counter Clock (CL–TTL). Goes High each time the Add/Subtract circuitry completes a successful subtraction (all 16 digits). The QMC totalizes these subtractions until an unsuccessful subtraction occurs. The count in QMC then shifts into the QR. Also pulses High to determine proper annunicator.
QR EN CLK	A15A($\overline{15}$)	A13A($\overline{17}$)	Quotient Register Enable Clock (DCL–TTL). Active during process cycle for purpose of entering each digit of measurement result into QR. Each time it goes High, it enables the QR counter to be clocked by REG CLK.
$\overline{\text{QMC = MULT STR}}$	A13A($\overline{15}$)	A14A(15)	Quotient Multiplier Counter Equals Multiplier Storage (DCL–TTL). Used when a remote multiplier (M, K, n, etc.) is programmed in the measurement. Even though the decimal point alignment may be correct, the decimal point may not be in the correct placement for the fixed multiplier. The decimal point is shifted and QMC is clocked until QMC equals MULT STR. When this occurs, this line goes Low and signifies that the decimal point and multiplier properly indicate the number's magnitude. The decimal point may be placed several digits away from the MSD.
$\overline{\text{QMC}\leftarrow 0}$	A15A(14)	A13A(14)	Quotient Multiplier Counter Assign Zero (DCL–TTL). Resets the QMC to a count of zero.
QMC = 0	A13A($\overline{21}$)	A14A(21)	Quotient Multiplier Counter Equals Zero (DCL–TTL). Active High qualifier used to determine when the QM counter equals zero.
$\overline{\text{QMC = 6}}$	A13B(19)	A15B(19)	Quotient Multiplier Counter Equals Six (DCL–TTL). Active Low qualifier used in the multiplier selected routine to indicate that all multipliers have been examined for possible use. Forces processor to accept the last available multiplier.
$\overline{\text{QMC = 9}}$	A13B($\overline{2}$)	A14B(2)	Quotient Multiplier Counter Equals Nine (DCL–TTL). Active Low qualifier used to place result of START + STOP, Events, or RATIO in Giga units.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{QMC = 10}}$	A13B($\overline{12}$)	A14B(12)	Quotient Multiplier Counter Equals 10 (DCL-TTL). An active Low qualifier in the divide routine. Indicates that NR contents are at least 10 times greater than DR contents. Causes the DR contents and decimal point to shift one place to the left.
QR EN A	A14A($\overline{12}$)	A13A(18), A15A($\overline{19}$), A17J1(5) via A17J2(55)	Quotient Register Enable (DCL-TTL). These lines carry a 3-line code used to control data transfer to and from the QR.
QR EN B	A15B(10)	A13B($\overline{10}$)	
QR EN C	A15A(21)	A13A($\overline{20}$)	
QR EN A/$\overline{\text{PI XMT}}$	A14A($\overline{12}$)	A13A(18), A15A($\overline{19}$), A17J1(5) via A17J2(55)	Functionally, this line is considered two separate lines. See individual descriptions for each portion of line name.
$\overline{\text{QR(QRC) = BLNK}}$	A13A($\overline{9}$)	A14A(9)	Quotient Register (QR Counter) Equals Blank (DCL-TTL). Active Low qualifier. As the QR outputs the contents of its locations, this line goes Low to indicate blank codes.
RATIO + ST	A10B(16)	A9B($\overline{16}$)	Ratio or Start (SCL-ECL). Result of decoded ratio or start function code. Controls turn off of 500 MHz output of A8. Allows Channel B signal to accumulate counts in Time Scaler (A11).
REG CLK	A15B($\overline{4}$)	A13B(4)	Register Clock (CL-TTL). Clocks the RAM counters on A13 to shift data during process cycle. For one ROM cycle, number of pulses may be 16, 15, or 1.
$\overline{\text{RMT}}$	A12B($\overline{19}$)	A10B($\overline{19}$), A11B(19), A14B(19), A17J1(31) via A17J2(54)	Remote (SCL-TTL). When Low, places counter operation under remote programming control. Line causes A10 to select remote function codes; causes A11 to select remote gate time codes; causes A14 to select remote display position codes. Disables front panel FUNCTION switch reset, GATE TIME switch reset, and push-button RESET switch.
$\overline{\text{RMT CHK}}$	A12A(8)	A10A($\overline{5}$)	Remote Check (SCL-TTL). Combined on A10 with the remote function codes. Operational only when using remote function codes. Forces selection of A+B, regardless of ACCUM MODE START/STOP switch position. Causes TEST line to select 100 MHz test signal for measurement and turn off front panel input trigger circuits.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS FROM	CONNECTOR AND PINS TO	DESCRIPTION

RMT DISP POS A
RMT DISP POS B
RMT DISP POS C
RMT DISP POS D
	A12B($\overline{11}$)
	A12B($\overline{12}$)
	A12B($\overline{8}$)
	A12B($\overline{13}$)
		A14B(10)
		A14B(11)
		A14B($\overline{8}$)
		A14B(13)
			Remote Display Position (SCL-TTL). When counter is remotely programmed, lines provide a 4-line code to select the desired display position.

RMT FUNC A
RMT FUNC B
RMT FUNC C
	A12B(12)
	A12B(11)
	A12B($\overline{10}$)
		A10B($\overline{12}$)
		A10B($\overline{11}$)
		A10B(10)
			Remote Function (SCL-TTL). When counter is being remotely programmed, lines provide a 3-line code to program the desired operation mode (freq, period, TI, etc.). These lines are selected for use when $\overline{\text{RMT}}$ is Low. Code list is same as for FP FUNC (see Switch Schematic). Codes are decoded on A10 to provide several static control lines.

RMT GATE	A12A(12)	A10A($\overline{12}$)	Remote Gate (SCL-TTL). A remote program operation. When High, allows counter's gate time to be controlled by pulses on the GATE CONTROL jack. Performs same function as having switch position in EXT GATE.

RMT GT A
RMT GT B
RMT GT C
RMT GT D
	A12B(4)
	A12B(5)
	A12B(9)
	A12B(10)
		A11B($\overline{4}$)
		A11B($\overline{5}$)
		A11B(9)
		A11B($\overline{10}$)
			Remote Gate Time (SCL-TTL). When counter is being remotely programmed, lines provide a 4-line code to program the desired gate time (1s, 1μs, etc.). These lines are selected for use when $\overline{\text{RMT}}$ is Low and $\overline{\text{PROC BUSY}}$ and $\overline{\text{PI DISP POS/GT SEL}}$ are High. Code list is same as for FP GT (see Switch Schematic). Lines are decoded on A11 to enable one of the Time Scalers to output a 5 code.

$\overline{\text{RMT INH ARM}}$	A12A(15)	A11B($\overline{14}$)	Remote Inhibit Arm (DCL-TTL). An externally controlled line that prevents the counter from arming. Prevents the $\overline{\text{ARM}}$ line from going Low.
$\overline{\text{RMT LITE}}$	A12B(3)	A2P1(8)	Remote Light (SCL-TTL). Used to light the display's RMT lamp. Goes Low with the RMT line.

$\overline{\text{RMT MULT A}}$
$\overline{\text{RMT MULT B}}$
$\overline{\text{RMT MULT C}}$
	A12B($\overline{21}$)
	A12B($\overline{22}$)
	A12B($\overline{20}$)
		A13B(21)
		A13B(22)
		A13B(20)
			Remote Multiplier (SCL-TTL). When counter is in remote operation, these lines provide a 4-line code to program the desired multiplier (K, M, n, etc.). These lines are selected for use when $\overline{\text{RMT}}$ is Low.

$\overline{\text{RMT RST}}$	A12B(13)	A11B($\overline{13}$)	Remote Reset (SCL-TTL). Externally programmed reset. When Low, provides same type of reset as the front panel RESET switch.
$\overline{\text{ROM CLK}}$	A15A(11)	A14A($\overline{11}$)	ROM Clock (DCL-TTL). Pulses Low to initiate a new ROM cycle. Causes the new ROM address codes stored in A14 to be shifted onto the ROM address lines (SV(T)).

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{RST}}$	A11B(4)	A14B(4), A17J1(38) via A14J2(40)	Reset (SCL-TTL). Goes Low with any type of manual reset, plug-in reset, or excessive gate time. Used to clear the present state ROM address codes on A14 and to set the address code to 001. Also, resets the plug-in circuits.
RST FRONT END	A15A($\overline{20}$)	A10A($\overline{20}$)	Reset Front End (DCL-TTL). A ROM command line generated near the end of the process cycle. Causes the scalers on A9 and A11 to reset and causes the Event Gate and Time Gate flip-flops to reset (A9). Line is not functional when counter is in START or STOP.
SAMPLE RATE	S6 via A4 & A5, A12A(11)	A11A(11)	This line connects the front panel SAMPLE RATE pot to the sample rate circuit on A11. This line can also be controlled remotely from A12. Controls the time between measurement cycles.
SAMPLE RATE ARM	A11A(10)	A10A($\overline{10}$)	(DCL-TTL). Used to initialize processor during totalize or when $\overline{\text{PI DATA}}$ is Low. Can be set High by rundown of sample rate, by $\overline{\text{PI ARM}}$, or by a reset.
SCH-O	A10A(13)	A9A($\overline{13}$)	Stop Channel Hold-Off (SCL-TTL). Used only in externally controlled time interval measurement to prevent Channel B pulses from stopping measurement. Controlled by $\overline{\text{GATE CONTROL}}$ signal when rear panel switch is set to EXT GATE. Controlled by RMT GATE line during remote operation.
SCLR RST	A10A(17)	A9A(14)	Scaler Reset (DCL-EECL). Resets Time and Events scalers on A9. Goes High with $\overline{\text{SET AUT SC}}$ line or RST FRONT END when $\overline{\text{ST+STP}}$ line is High.
$\overline{\text{SEC LITE}}$	A10A(10)	A2P1(9), A16(11)	Second Light (SCL-TTL). A result of decoding the FUNCTION switch codes on A10. Goes Low to light the display's SEC lamp.
$\overline{\text{SEL A • B}}$	A17J1(18) via A17J2(32)	A10B(6)	Select A and B (SCL-TTL). Pulled Low from plug-in. Line is level shifted to EECL and sent to A9 as EXT AB. This signal enables the counter to use the plug-in's A and B channels for a measurement and also shuts off the mainframe's input trigger circuits.
$\overline{\text{SEL C}}$	A17J1(33) via A17J2(50)	A10B(21)	Select C (SCL-TTL). Controls state of EXT C line. Used when measuring events of Channel C signal occurring between Channel A pulse and Channel B pulse. Causes Time Scaler to accept Channel C signal instead of Time Base signal.

Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{SER OUT}}$	A12A($\overline{4}$)	A14A(6)	Serial Out (SCL-TTL). A qualifier line that, when called upon, initiates the output data routine (a remote program operation). Set Low when counter is addressed to talk or when rear panel switch is set to TALK ALWAYS.
$\overline{\text{SET AUT SC}}$	A11B($\overline{17}$)	A10B(12), A13B($\overline{4}$), A15B($\overline{5}$)	Set Auto Single Cycle. Goes Low on 1) initial instrument turn-on, 2) with RESET switch when not in remote, 3) between settings of FUNCTION switch (except STOP/START) when not in remote, 4) with plug-in reset, or 5) with remote reset. Generates signals on A10 to reset the scalers on A9 and A11. Resets Noise Control F-F (A10), Asterisk Storage F-F (A15), Multiplier Storage flip-flops (A13), Measurement Done F-F (U12B), and the Event Gate and Time Gate flip-flops (A9) using the GATE RST line. Used to make a single automatic measurement while in manual mode, thereby recalculating the annunciator and decimal point.
$\overline{\text{SIGN-}}$	A15A(19)	A10A(18), A12A($\overline{17}$), A13A(17), A17J1(19) via A17J2(31)	Sign Minus (SCL-TTL). Combines with plug-in function code on A10 to indicate sign of plug-in data. Used in serial output routine of A12 to determine the sign of the data. When Low, instructs DR counter on A13 to supply additional DRC code to light display's minus sign.
$\overline{\text{ST+STP}}$	A10B($\overline{10}$)	A11B(10), A14B(9), A15B(9)	Start or Stop (SCL-TTL). Result of decoded start or stop function code. Permits oscillator noise to be generated in all functions when in EXT GATE. Bypasses Measurement Done F-F (A10) and allows sample rate to cause scaler scanning every 50 ms to update display.
SV1(T)	A14A($\overline{4}$)	A15A(4)	State Variable # (time) (DCL-TTL). Octal coded address lines for the ROMs (A15). Used with the MSB line and SV7(T). See A15 theory for further description.
SV2(T)	A14A(4)	A15A($\overline{4}$)	
SV3(T)	A14A(5)	A15A($\overline{5}$)	
SV4(T)	A14A($\overline{6}$)	A15A(6)	
SV5(T)	A14A(3)	A15A($\overline{3}$)	
SV6(T)	A14A($\overline{3}$)	A15A(3)	
SV7(T)	A14A($\overline{13}$)	A15A(13)	State Variable 7 (Time) (DCL-TTL). The state of this line is the result of the qualifier. Used as the LSB in the octal code that addresses the next ROM location. Determines the direction of the program flow, e.g., 740 or 741.
SV1(T+1)	A15A(10)	A14A($\overline{10}$)	State Variable # (Time plus one) (DCL-TTL). These lines are derived from the first group in each set of command lines (MSB=1). While MSB is still "1", the states of the lines are stored. The lines are coded in octal and are used to determine the *next* ROM location.
SV2(T+1)	A15A(7)	A14A($\overline{7}$)	
SV3(T+1)	A15A(5)	A14A($\overline{5}$)	
SV4(T+1)	A15A($\overline{8}$)	A14A(8)	
SV5(T+1)	A15A(8)	A14A($\overline{8}$)	
SV6(T+1)	A15A($\overline{7}$)	A14A($\overline{7}$)	

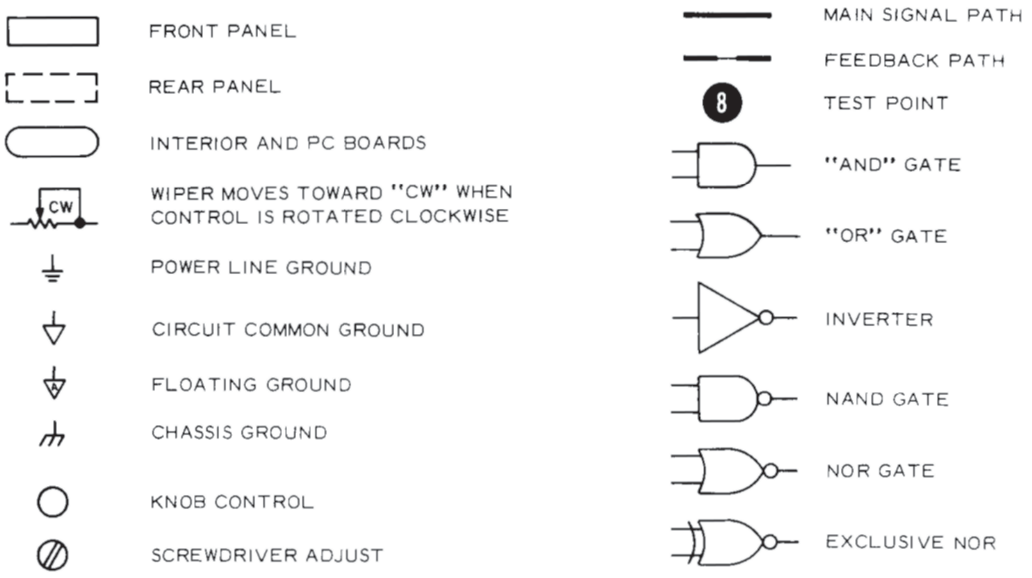
Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
SV4(T+1)/DR EN B	A15A($\overline{8}$)	A13A(8), A14A(8)	This line is considered SV4(T+1) when MSB is "1" and DR EN B when MSB is "0". See separate descriptions for each portion of line name.
SV6(T+1)/NR EN A	A15A($\overline{7}$)	A13A($\overline{7}$), A14A(7)	This line is considered SV6(T+1) when MSB is "1" and NR EN A when MSB is "0". See separate descriptions for each portion of line name.
TEST	A10B(17)	A10B($\overline{17}$)	(SCL-TTL). Controlled by front panel check or remote check. If check is selected, line goes High and causes Events Scaler to accumulate 100 MHz counts.
TI + EVT	A10B($\overline{13}$)	A9B(14)	Time Interval or Events (SCL-EECL). Result of decoded function codes. Goes High during time interval mode or C channel events.
$\overline{\text{TI + EVT}}$	A10B(15)	A9B($\overline{15}$)	Time Interval or Events (SCL-EECL). Result of decoded function codes. Goes Low during time interval mode. Allows passage of Channel B signal to Event Gate F-F (A9) for stopping time interval.
$\overline{\text{TIME GATE}}$	A9B($\overline{18}$)	A10B(18)	(DCL-ECL). Goes Low when Time Gate F-F sets (A9). When $\overline{\text{TIME GATE}}$ and $\overline{\text{EVT GATE}}$ go High, starts process cycle by pulling $\overline{\text{INIT PROC}}$ line Low. In MIN gate time, goes Low to set Resolution F-F (A10) and stop measurement cycle.
$\overline{\text{TIME SCLR A}}$	A11B(1)	A13B(1), A10B($\overline{1}$)	Time Scaler (DL-TTL). At beginning of process cycle, these lines transfer Time Scaler data (in BCD) from A11. During the measurement time, A10 monitors the $\overline{A}$ and $\overline{D}$ lines to detect a 5 code.
$\overline{\text{TIME SCLR B}}$	A11B($\overline{1}$)	A13B(1)	
$\overline{\text{TIME SCLR C}}$	A11B(3)	A13B(3)	
$\overline{\text{TIME SCLR D}}$	A11B(2)	A13B(2), A10B($\overline{3}$)	
$\overline{\text{TIME SCLR A}_0}$	A9B($\overline{10}$)	A11B(6)	Time Scaler (DL-EECL). A four-line code from a divide-by-10 stage in the time scaler (A9). At the end of the gate time, this decade contains the least significant digit in the time count.
$\overline{\text{TIME SCLR B}_0}$	A9B($\overline{12}$)	A11B(7)	
$\overline{\text{TIME SCLR C}_0}$	A9B($\overline{13}$)	A11B(8)	
$\overline{\text{TIME SCLR D}_0}$	A9B($\overline{11}$)	A11B($\overline{7}$)	
TIME SCLR A1	A9B($\overline{22}$)	A11B(22)	Time Scaler A1 (SL-ECL). A derivative of the 500 MHz clock signal, or plug-in Channel C signal, or Channel B signal (ratio or start). Has been divided-by-20 in A9 scaler before being sent to remainder of scalers on A11. Complement of $\overline{\text{TIME SCLR A1}}$.

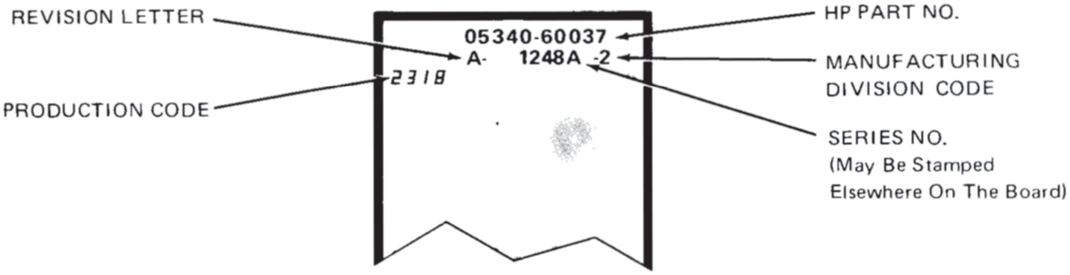
Table 8-1. Signal Line Descriptions and Destinations

MNEMONIC ABBREVIATIONS	CONNECTOR AND PINS		DESCRIPTION
	FROM	TO	
$\overline{\text{TIME SCLR A1}}$	A9B($\overline{21}$)	A11B(21)	Time Scaler (SL-ECL). A derivative of the 500 MHz clock signal, or plug-in Channel C signal, or Channel B signal (ratio or start). Has been divided by 20 in A9 scaler before being sent to remainder of scalers on A11. Complement of TIME SCLR A1.
$\overline{\text{TRANS MULT}}$	A17J1(37) via A17J2(42)	A10A($\overline{19}$)	Transpose Multiplier (DCL-TTL). When Low, causes the normal output multiplier to be changed. For data normally expressed in Giga units, the multiplier is changed to nano and vice-versa.
WORD DBL CLK	A15A($\overline{21}$)	A13A($\overline{18}$)	Word Doubling Clock (DCL-TTL). Used to store ROM program codes while MSB is equal to "1". Pulses High for each ROM cycle. Also used to set initial conditions of Add/Subtract circuit on A13.
$\overline{\text{WORD DBL CLK}}$	A15A(18)	A14A($\overline{21}$)	Word Doubling Clock (DCL-TTL). Used to store ROM program codes while MSB is equal to "1". Pulses Low during each ROM cycle. Used to clock newly generated SV(T+1) lines into storage (A14) for use in next ROM cycle.
$\overline{\text{XS GT RST INH}}$/$\overline{\text{N DATA}}$	A10B($\overline{22}$), A17J1(26) via A17J2(64)	A11B(18), A14B($\overline{2}$)	Excessive Gate Time Reset Inhibit/N Data (DCL-TTL). A time shared control line. First portion of line name is active when GATE CONTROL switch is set to EXT GATE. Inhibits counter from resetting itself under excessive gate time conditions. N DATA portion is active Low when plug-in is able to send an "N" to the mainframe.
10 MHz INT CLK	A18A(1, $\overline{1}$)	A8A(1, $\overline{1}$)	10 MHz Internal Clock (CL-TTL). A 10 MHz signal produced by A18 oscillator. Converted to 500 MHz in A8 for use as time base signal. Converted to 100 MHz in A8 for use as a test signal in the CHECK mode.
100 MHz TEST	A8B(2)	A9B(5)	(SL-EECL). Derived from 10 MHz oscillator signal. Used as test signal in the CHECK mode.
$\overline{\text{500 MHz OFF}}$	A9B(13)	A8B(4)	(SCL). Set Low by RATIO+ST line or EXT C line. Turns off 500 MHz oscillator output of A8 (on = +2V, off = -2V).

SYMBOLS



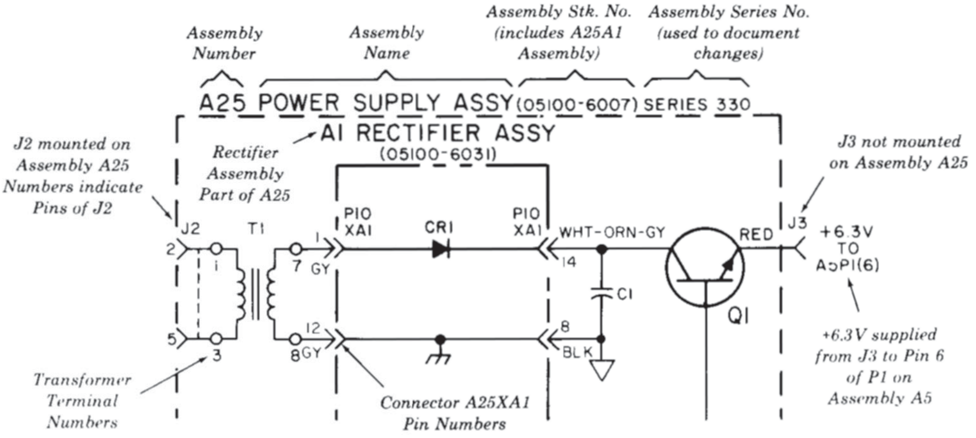
PRINTED CIRCUIT BOARD IDENTIFICATION



REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION. JACKS ARE THE STATIONARY CONNECTORS AND PLUGS ARE THE MORE MOVEABLE OF TWO CONNECTORS.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3


Assembly Number
Assembly Name
Assembly Stk. No. (includes A25A1 Assembly)
Assembly Series No. (used to document changes)
A25 POWER SUPPLY ASSY (05100-6007) SERIES 330
A1 RECTIFIER ASSY
(05100-6031)
J2 mounted on Assembly A25 Numbers indicate Pins of J2
Rectifier Assembly Part of A25
J3 not mounted on Assembly A25
J2
T1
P1O XA1
CR1
P1O XA1
WHT-ORN-GY
RED
J3
+6.3V TO A5P1(6)
7 GY
14
C1
Q1
8
12
8GY
BLK
2
5
3
1
Transformer Terminal Numbers
Connector A25XA1 Pin Numbers
+6.3V supplied from J3 to Pin 6 of P1 on Assembly A5

COMPONENT PLACEMENT

Δ OR □

IDENTIFIES:

Pin 1 of dip and flat-pack IC's.
Tab of TO cases.
+ side of electrolytic capacitors.
Pin 1 of resistor packs.
Cathode of diodes.
Section 1 of dip switches.

Figure 8-1. Schematic Diagram Notes

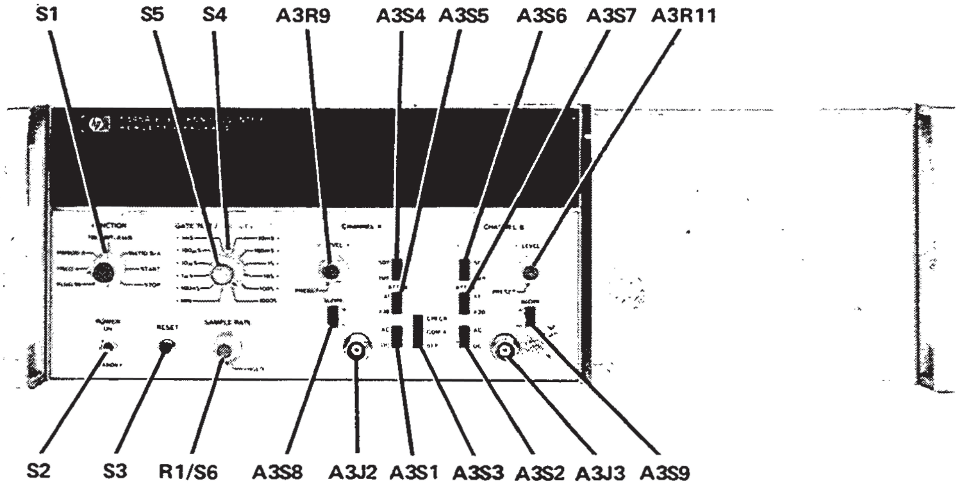


Figure 8-2. Front Panel Designations

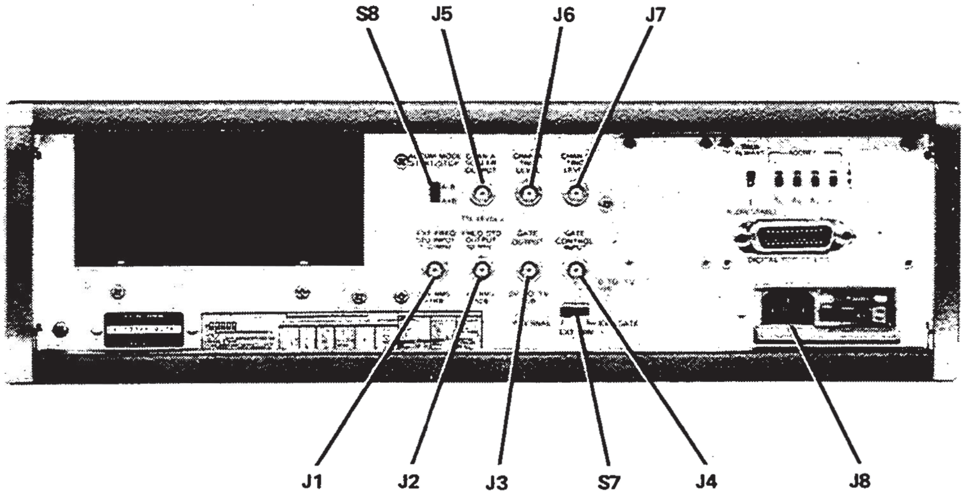


Figure 8-3. Rear Panel Designations

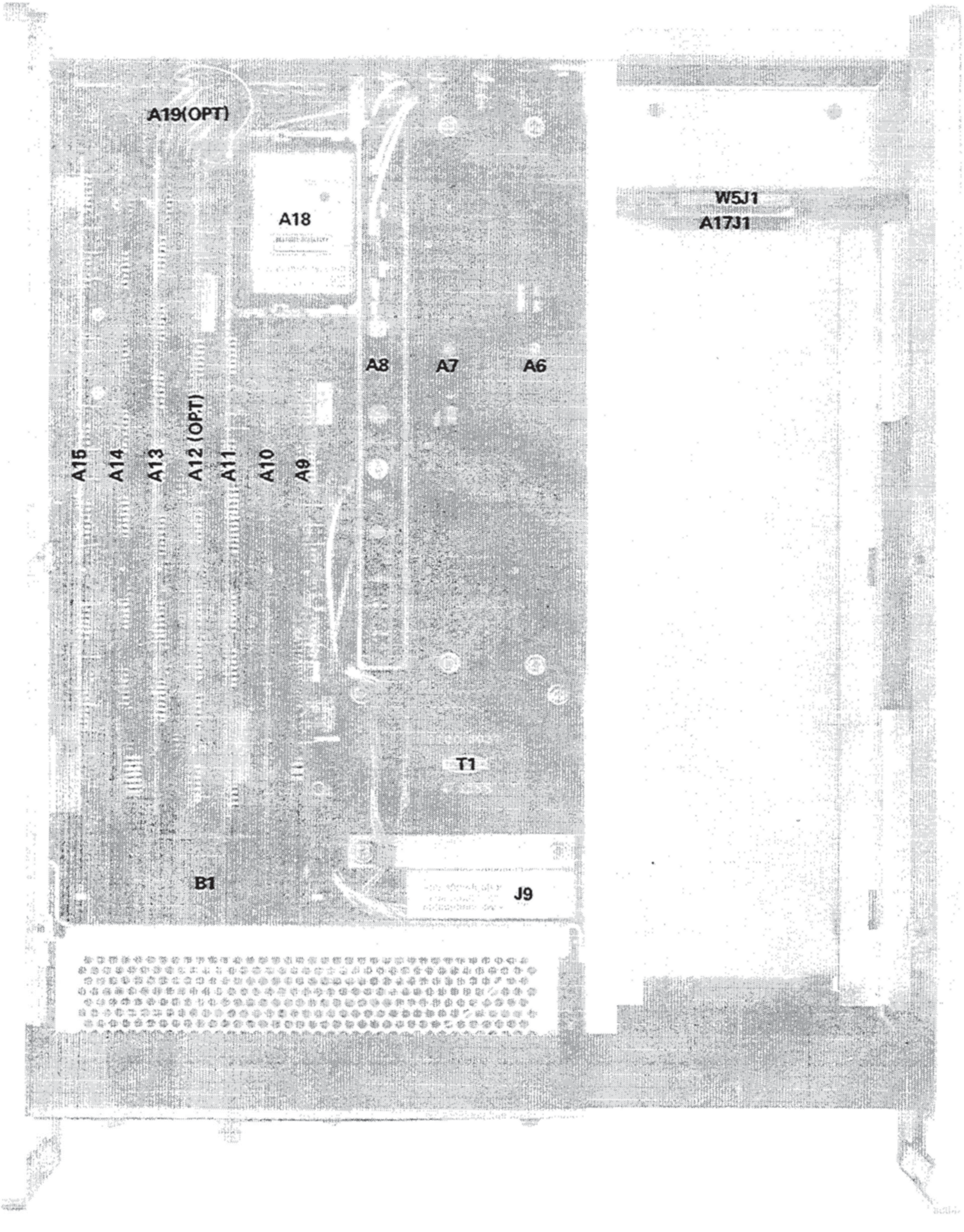


Figure 8-4. Top Internal View

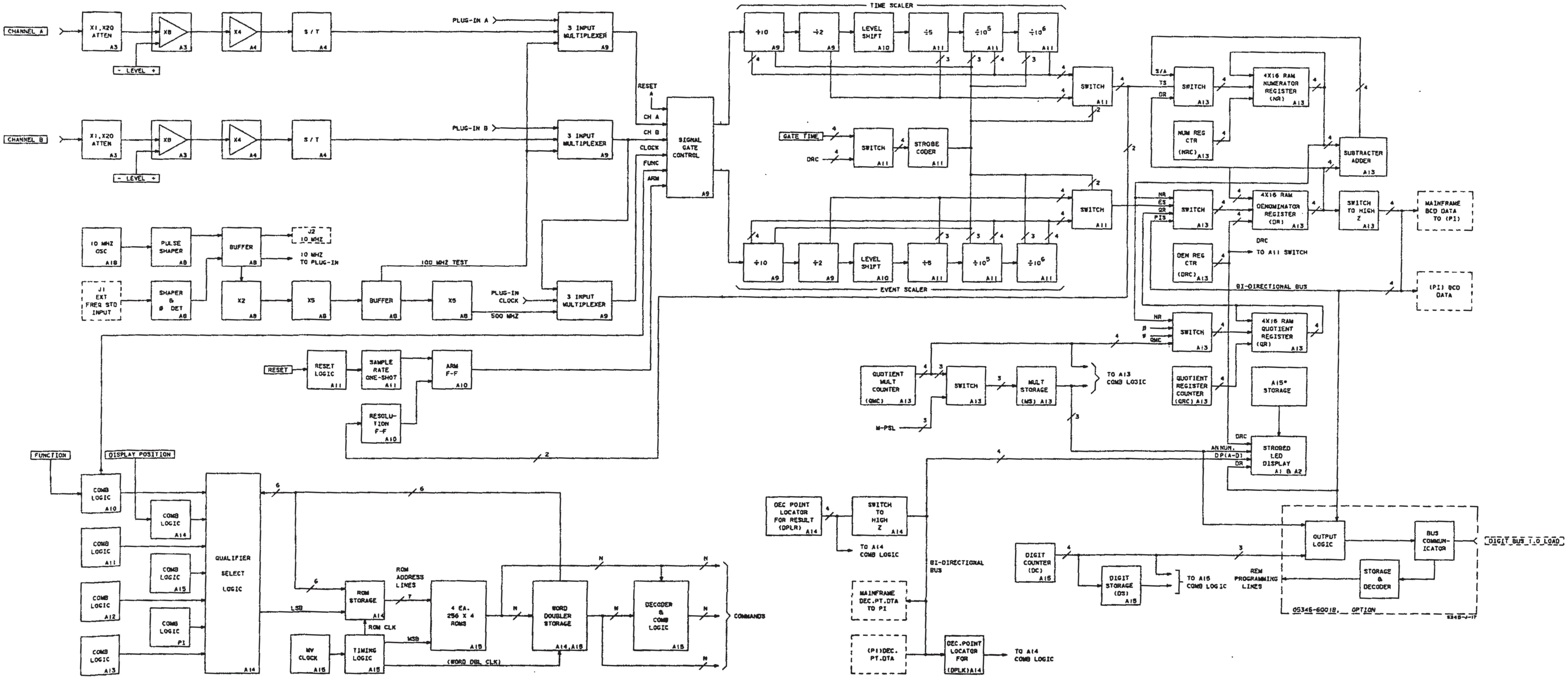
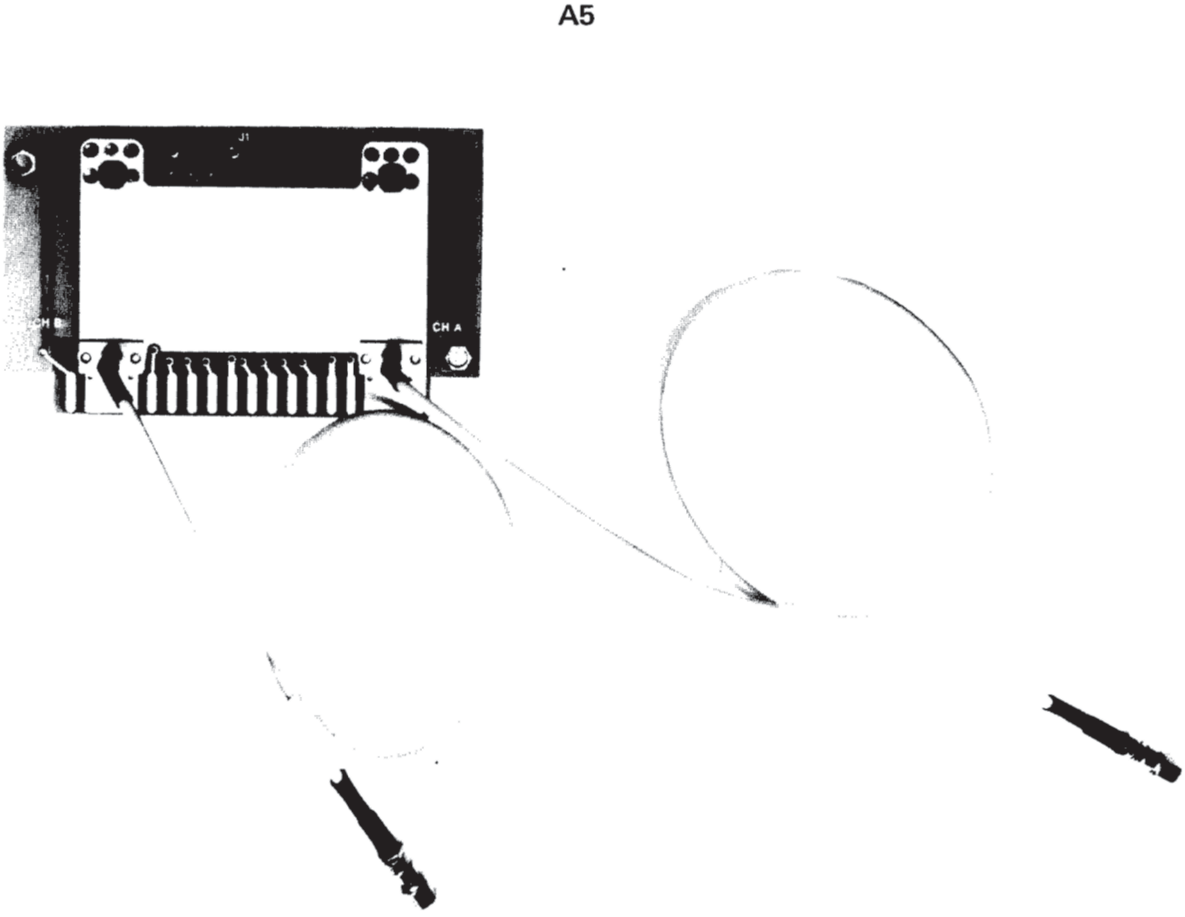
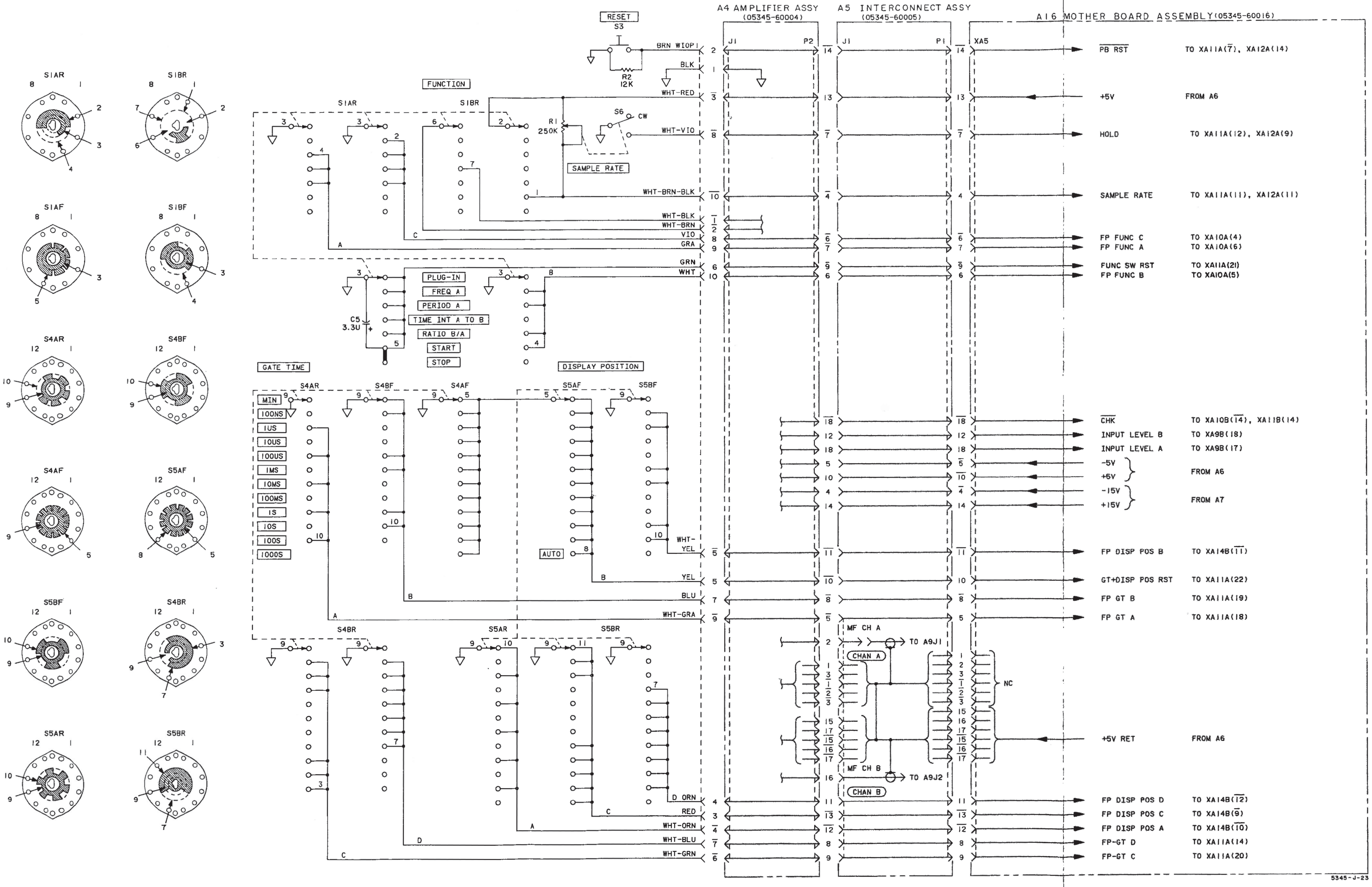


Figure 8–5. Overall Block Diagram



5345-A-31



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES.

3. ROTARY SWITCH WAFERS ARE SHOWN FROM FRONT PANEL VIEW.

4. SWITCH CODES ARE: 1≙ OPEN CIRCUIT AND 0≙ CONNECTION.

FUNCTION SWITCH

FUNCTION	CODE C B A
PLUG IN	0 1 1
FREQ A	0 0 1
PERIOD A	0 0 0
TIME INT A TO B	0 1 0
RATIO B/A	1 0 0
START	1 0 1
STOP	1 1 1
NOT SELECTABLE FROM FRONT PANEL-CAN BE FROM PLUG-IN OR REMOTE. INTENDED FOR 3-CHANNEL TIME INTERVALS; I.E., INDICATE NO. OF INPUTS ON "C" BETWEEN A & B	1 1 0

GATE TIME D C B A		DISPLAY POSITION D C B A
1 1 0 1	MIN	1 0 1 0
0 0 0 1	100 NS	1 0 0 1
0 0 1 0	1 US	1 0 0 0
0 0 1 1	10 US	0 1 1 1
0 1 0 0	100 US	0 1 1 0
0 1 0 1	1 MS	0 1 0 1
0 1 1 0	10 MS	0 1 0 0
0 1 1 1	100 MS	0 0 1 1
1 0 0 0	1 S	0 0 1 0
1 0 0 1	10 S	0 0 0 1
1 0 1 0	100 S	0 0 0 0
1 0 1 1	1000 S/AUTO	1 0 1 1

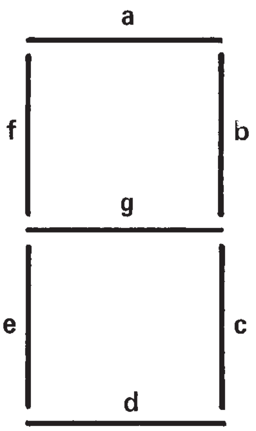
REFERENCE DESIGNATIONS
NO PREFIX
C5 R2 S1-6

Figure 8-6. Front Panel Switch Wiring Part of A4/A5/A16

A2U6
TRUTH TABLE

$\overline{\text{LT}}$	$\overline{\text{RB}}$ IN	A	B	C	D	a	b	c	d	e	f	g	$\overline{\text{RB}}$ OUT	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
	X	H	L	L	L	L	H	H	L	L	L	L	H	1
		L	H	L	L	H	H	L	H	H	L	H	H	2
		H	H	L	L	H	H	H	H	L	L	H	H	3
		L	L	H	L	L	H	H	L	L	L	H	H	4
		H	L	H	L	H	L	H	H	L	H	H	H	5
		L	H	H	L	H	L	H	H	H	H	H	H	6
		H	H	H	L	H	H	H	L	L	L	L	H	7
		L	L	L	H	H	H	H	H	H	H	H	H	8
		H	L	L	H	H	H	H	H	L	H	H	H	9
		L	H	L	H	L	L	L	H	H	L	H	H	10
		H	H	L	H	L	L	L	H	L	L	H	H	11
		L	L	H	H	L	H	H	L	L	H	H	H	12
		H	L	H	H	H	L	H	H	L	H	H	H	13
		L	H	H	H	L	L	L	H	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	H	15

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Voltage Level

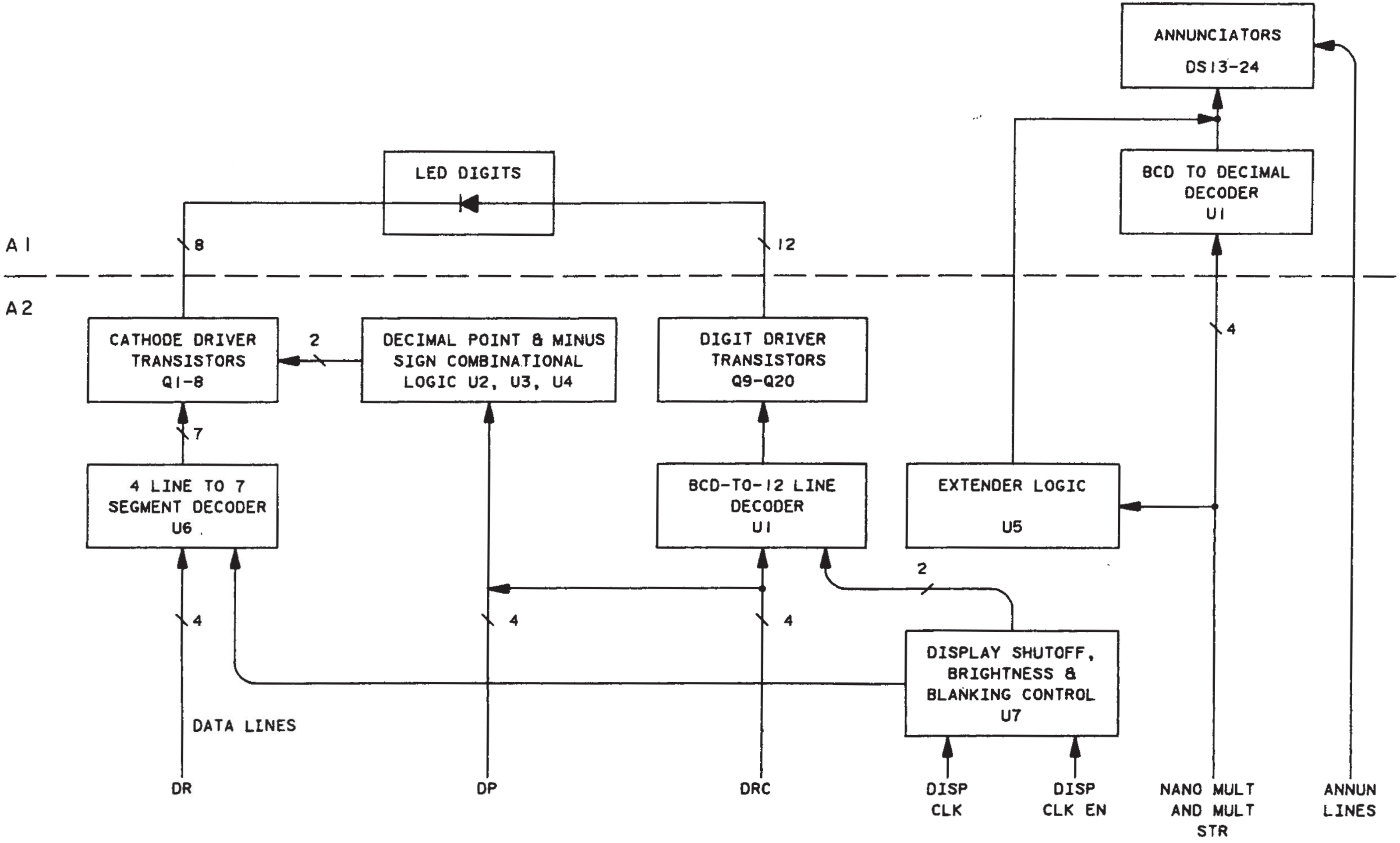


ANNUNCIATOR DECODING

A1U1 INPUTS →	A	B	C	D
SIGNAL LINES →	NANO MULT	MS C	MS B	MS A
ANNUNCIATORS				
G	0	0	0	0
M	0	0	0	1
K	0	0	1	0
BLANK	0	0	1	1
m	0	1	0	0
μ	0	1	0	1
n	0	1	1	0
μ	0	1	1	1
n	1	0	0	0
μ	1	0	0	1
m	1	0	1	0
BLANK	1	0	1	1
K	1	1	0	0
M	1	1	0	1
G	1	1	1	0
M	1	1	1	1

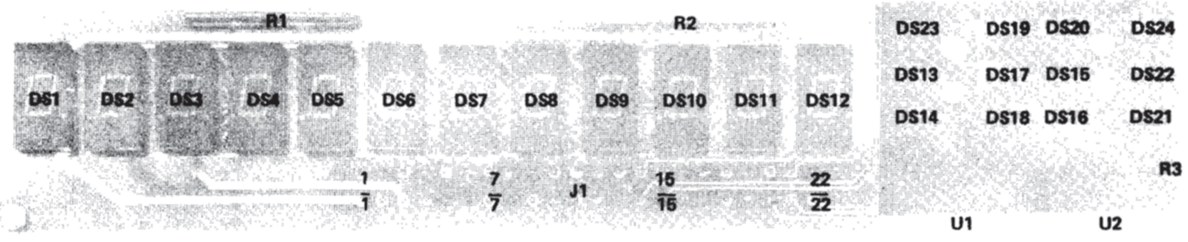
Figure 8-6
FRONT PANEL SWITCH WIRING

(See Page 8-27)

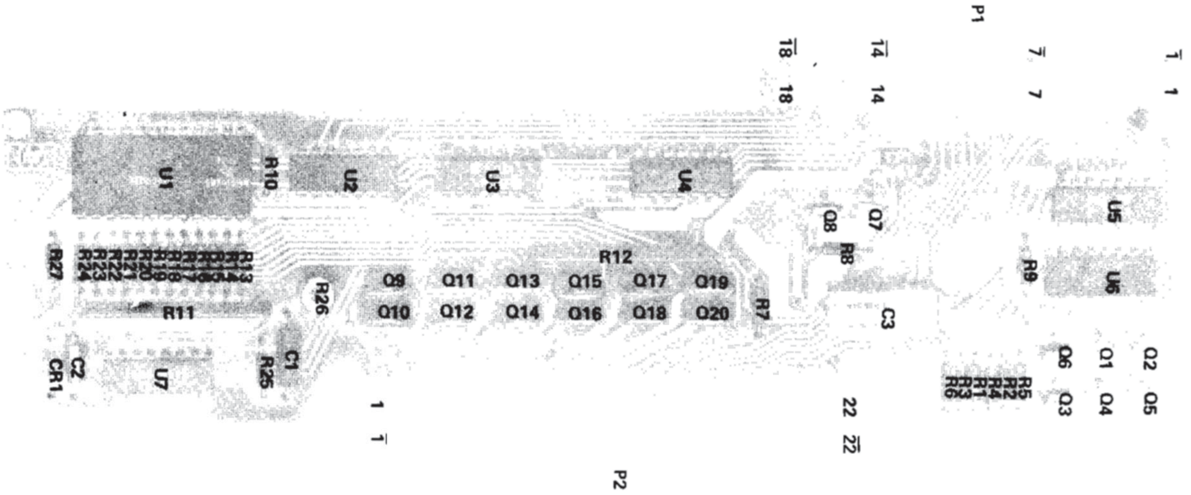

ANNUNCIATORS
DS13-24
LED DIGITS
BCD TO DECIMAL DECODER U1
A1
A2
8
12
4
CATHODE DRIVER TRANSISTORS Q1-8
2
DECIMAL POINT & MINUS SIGN COMBINATIONAL LOGIC U2, U3, U4
DIGIT DRIVER TRANSISTORS Q9-Q20
7
4 LINE TO 7 SEGMENT DECODER U6
BCD-TO-12 LINE DECODER U1
EXTENDER LOGIC
U5
2
4
4
4
DISPLAY SHUTOFF, BRIGHTNESS & BLANKING CONTROL U7
DATA LINES
DR
DP
DRC
DISP CLK
DISP CLK EN
NANO MULT AND MULT STR
ANNUN LINES

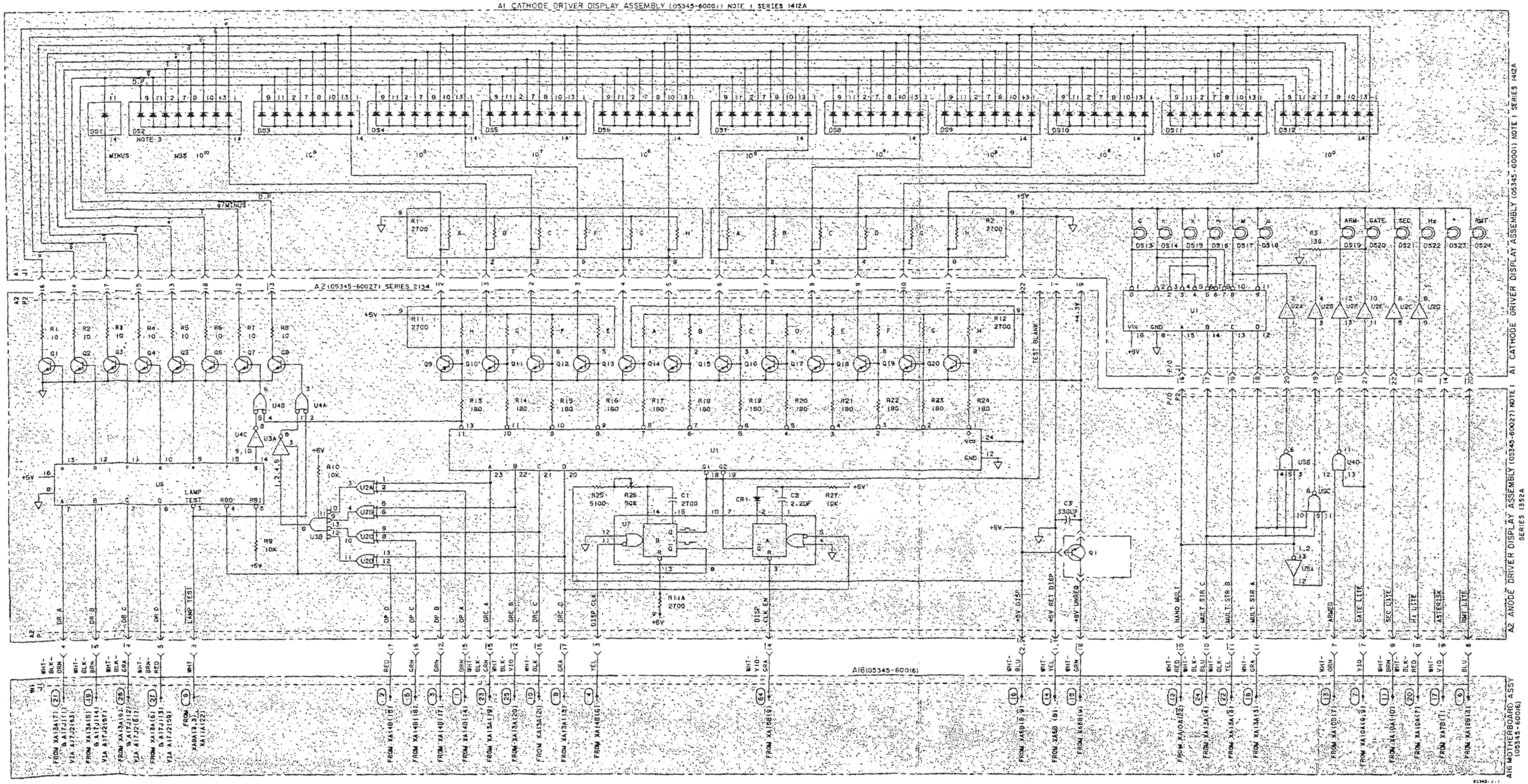
5345-D-5

A1


R1
R2
DS1
DS2
DS3
DS4
DS5
DS6
DS7
DS8
DS9
DS10
DS11
DS12
DS23
DS19
DS20
DS24
DS13
DS17
DS15
DS22
DS14
DS18
DS16
DS21
R3
1
1
7
7
J1
15
15
22
22
U1
U2

A2


P1
18
18
14
14
7
7
1
1
U1
R10
U2
U3
U4
U5
Q8
Q7
R8
R9
U6
R27
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R12
R26
Q9
Q11
Q13
Q15
Q17
Q19
R11
Q10
Q12
Q14
Q16
Q18
Q20
R7
C3
C2
CR1
U7
R25
C1
Q6
Q1
Q2
R5
R2
R4
R1
R3
R6
Q3
Q4
Q5
1
1
22
22
P2



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES.
3. DS1 THRU DS12 ARE LIGHT-EMITTING DIODES (1990-0437) AND ARE SOCKET MOUNTED.

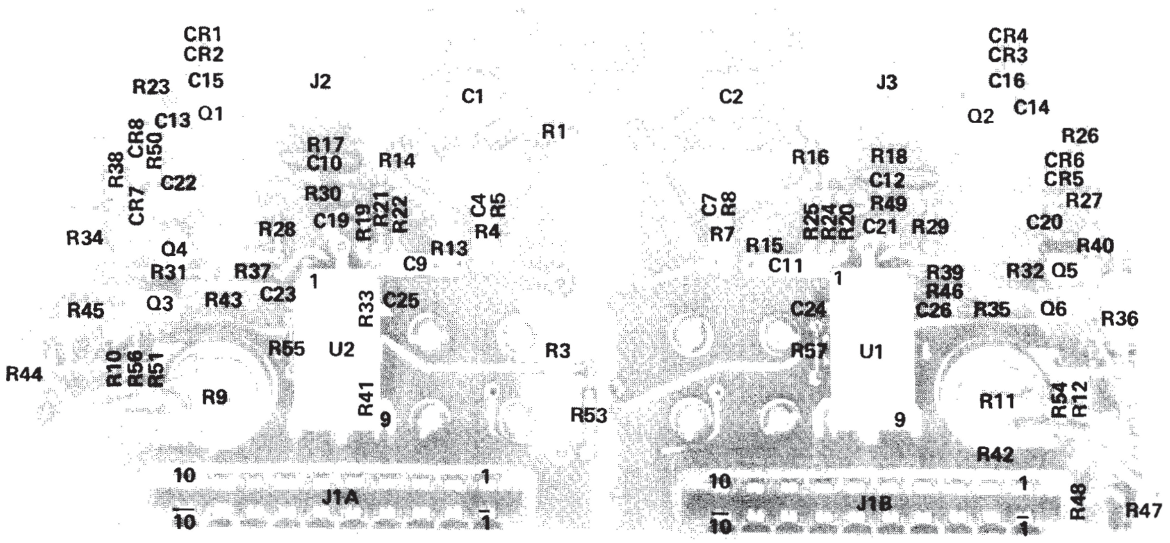
REFERENCE DESIGNATIONS

NO PREFIX	A1	A2	A16
Q1	DS1-24 J1 R1-3 U1,2	C1-3 CR1 Q1-20 R1-27 U1-7	W1J1

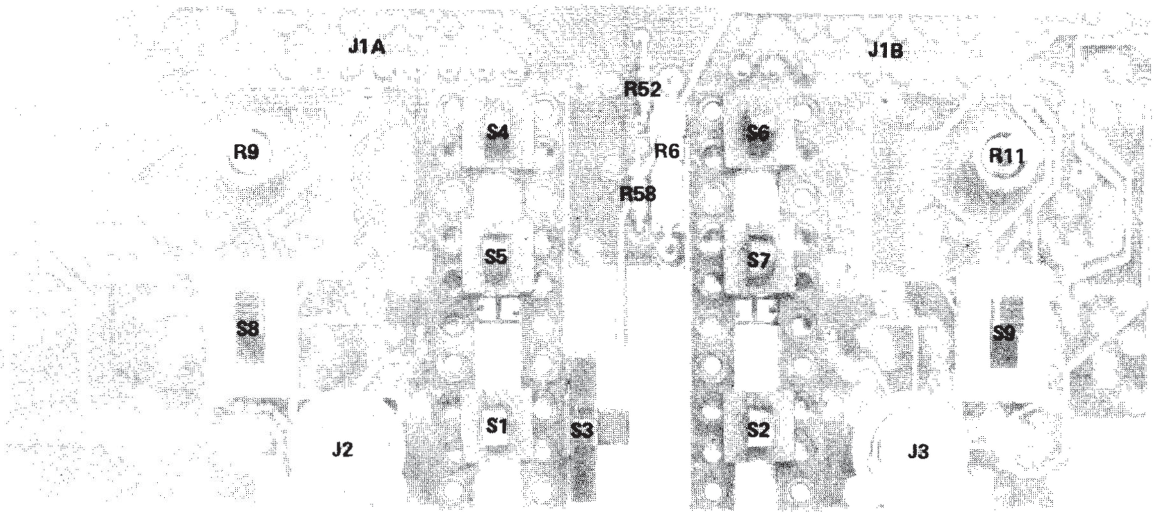
Figure 8-7. A1 Cathode Driver Display Assembly, A2 Cathode Driver Display Assembly

05345-J-1

A3 (Component Side)



A3 (Circuit Side)



Part of Figure 8-8. A3 Input Attenuator Assembly, A4 Input Trigger Assembly

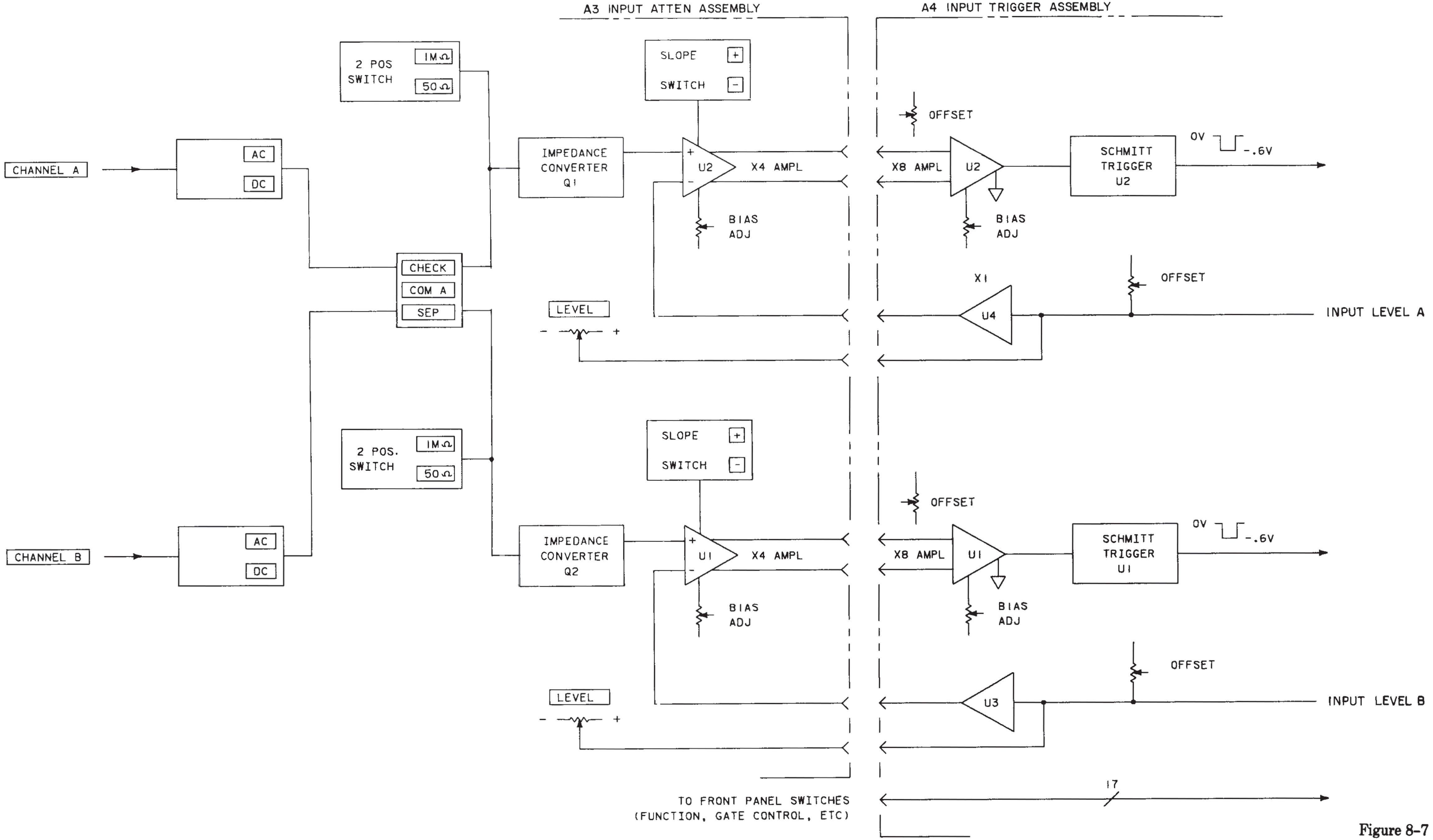
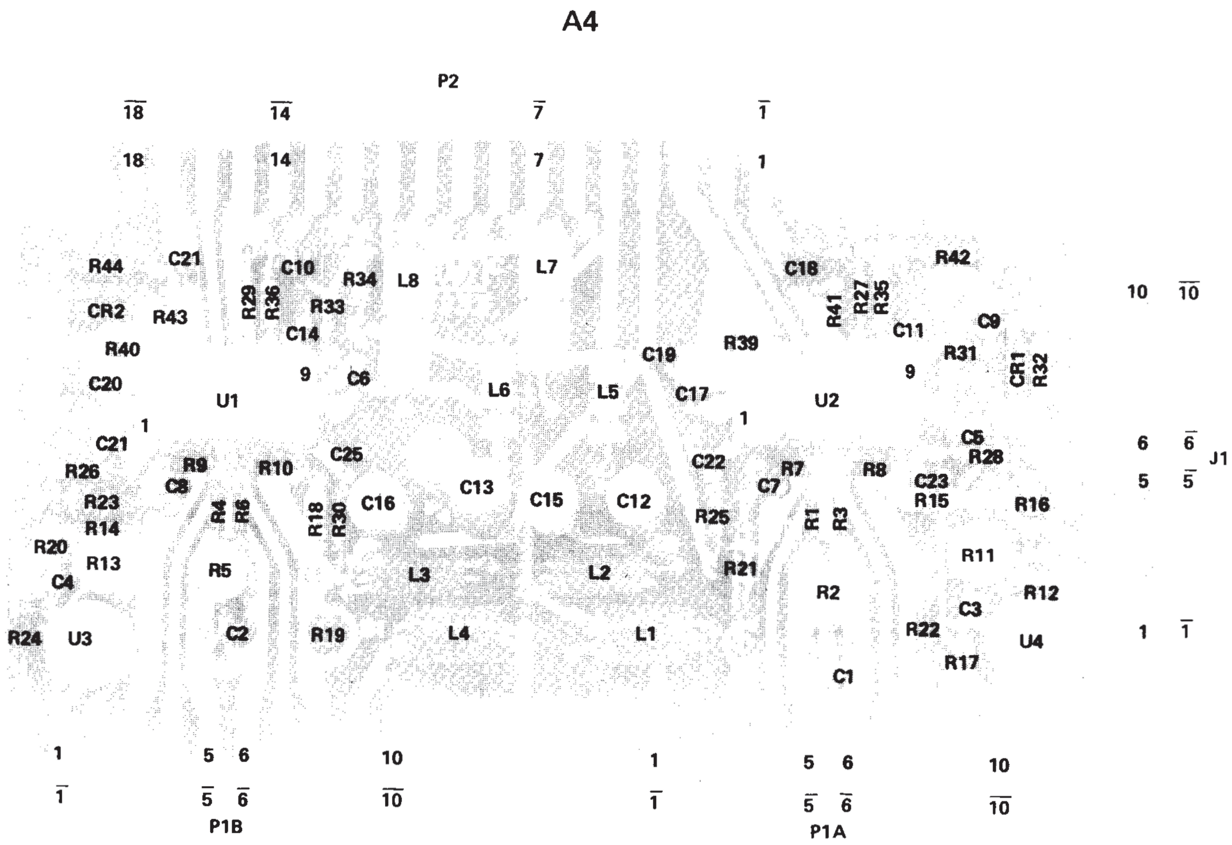


Figure 8-7
A1 ANODE DRIVER DISPLAY ASSEMBLY
A2 CATHODE DRIVER DISPLAY ASSEMBLY

(See Page 8-29)

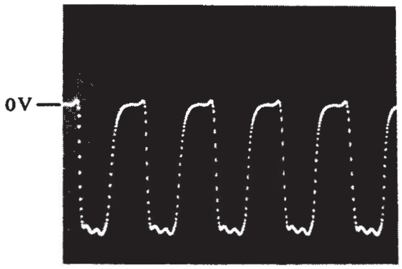

A4
P2
$\overline{18}$ $\overline{14}$ $\overline{7}$ $\overline{1}$
18 14 7 1
R44 C21 C10 R34 L8 L7 C18 R42
R29 R36 R33 R41 R27 R35
CR2 R43 C14 C11 C9 10 $\overline{10}$
R40 C19 R39 R31
C20 9 C6 L6 L5 C17 9 CR1 R32
U1 1 U2
1
C21 C5 6 $\overline{6}$
R26 R9 R10 C25 C22 R7 R8 R28 J1
C8 C7 C23 5 $\overline{5}$
R23 R4 R6 R18 R30 C16 C13 C15 C12 R25 R1 R3 R15 R16
R14
R20 R11
R13 R5 L3 L2 R21
C4 R2 R12
C3
R24 U3 C2 R19 L4 L1 R22 1 $\overline{1}$
U4
R17
C1
1 5 6 10 1 5 6 10
$\overline{1}$ $\overline{5}$ $\overline{6}$ $\overline{10}$ $\overline{1}$ $\overline{5}$ $\overline{6}$ $\overline{10}$
P1B P1A

5345-A-30

Equipment: 180A with 1810A

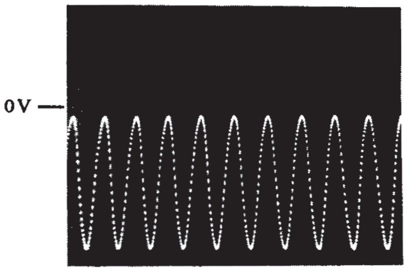
Schmitt trigger output taken from A5 cable, using BNC-to-subminature adaptor, part number 1250-0831.

Figure 1.
(100 MHz)

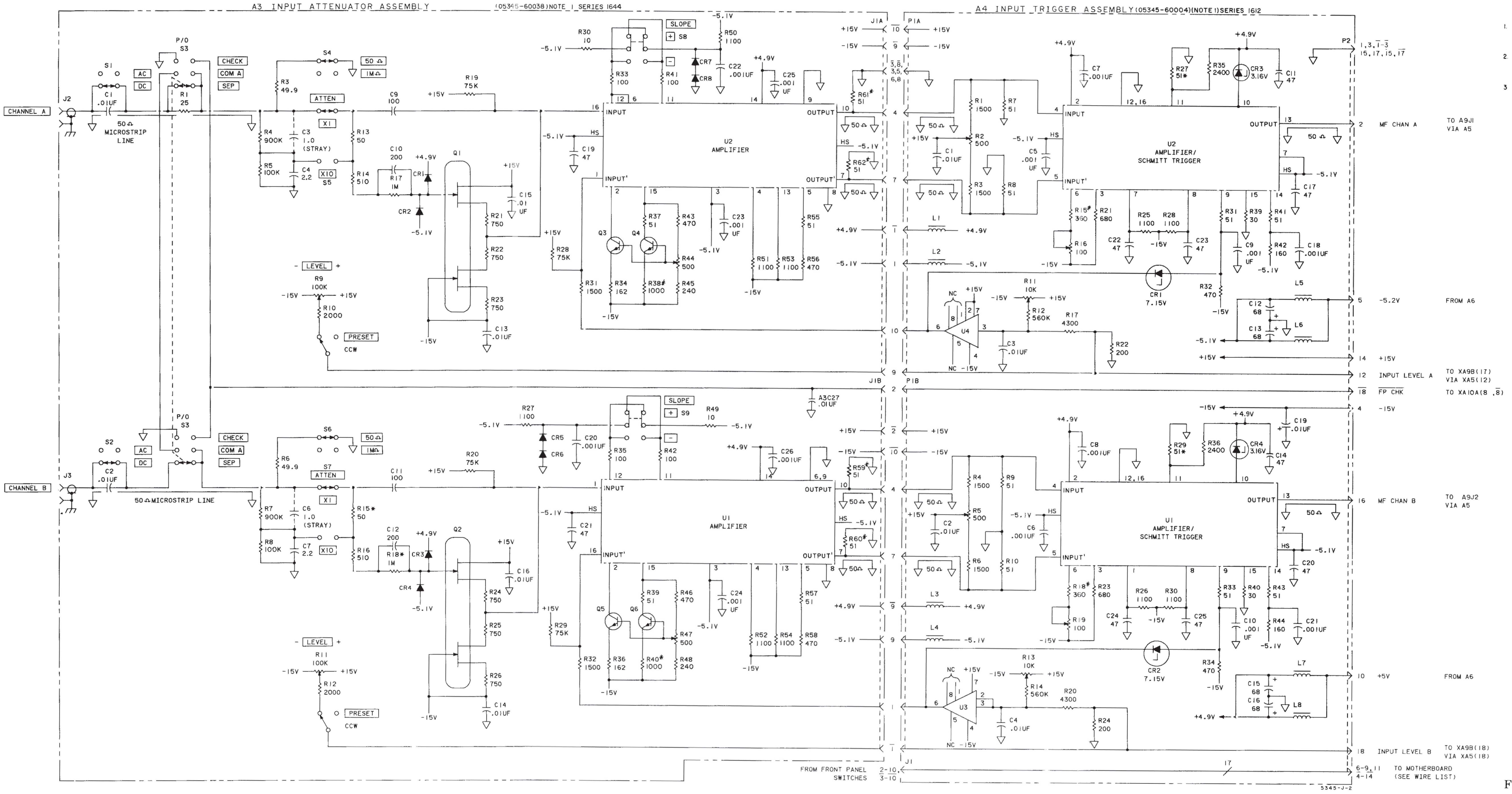


200 mV/DIV,
5 nS/DIV, + SLOPE,
EXPANDED

Figure 2.
(500 MHz)



200 mV/DIV,
2 nS/DIV, + SLOPE,
EXPANDED



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

REFERENCE DESIGNATIONS

A3	A4
C1-27	C1-25
CR1-8	CR1,4
J1-3	L1-8
Q1-6	P1,2
R1,R3-58	R1-44
S1-9	U1-4
U1,2	

NOTE

SEE FIGURE 8-8a, on next page, for A3 Option 012.

Figure 8-8. A3 Input Attenuator Assembly, A4 Input Trigger Assembly

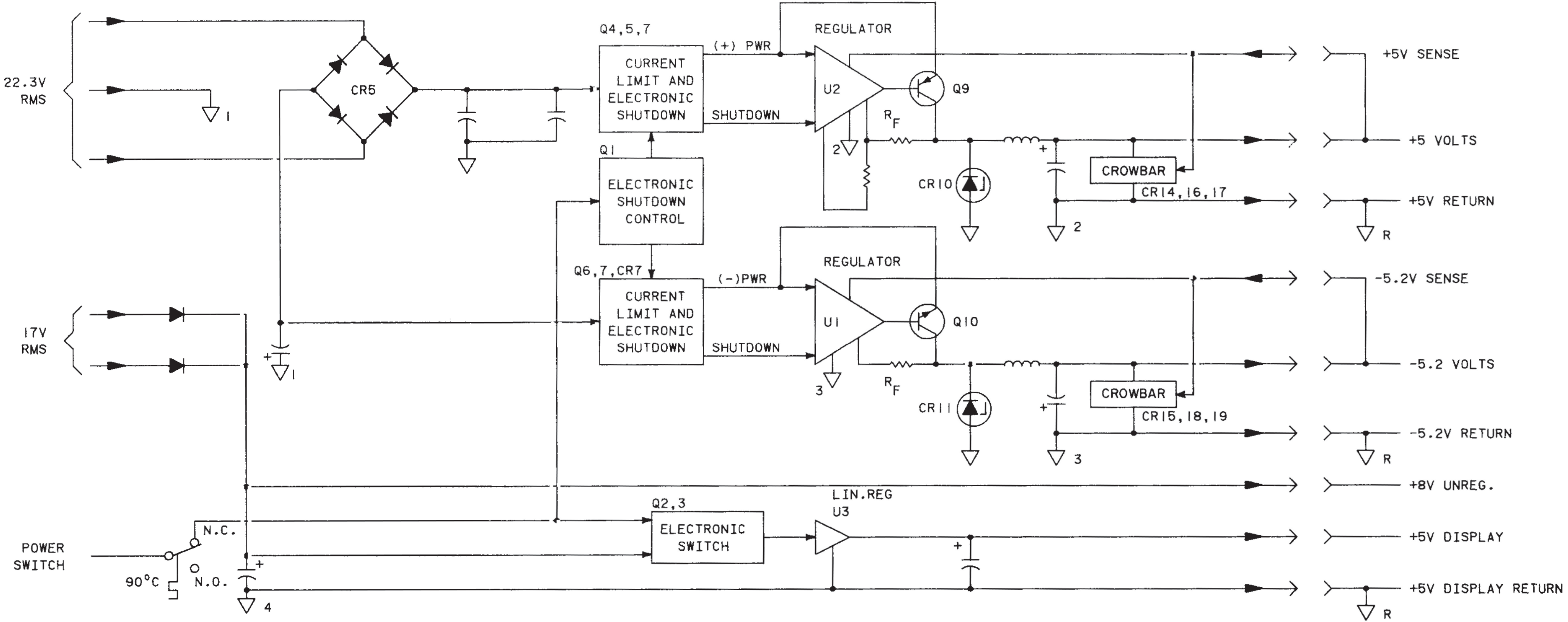


Figure 8-8

A3 INPUT ATTENUATOR ASSEMBLY,
A4 INRUT TRIGGER ASSEMBLY

(See Page 8-31)

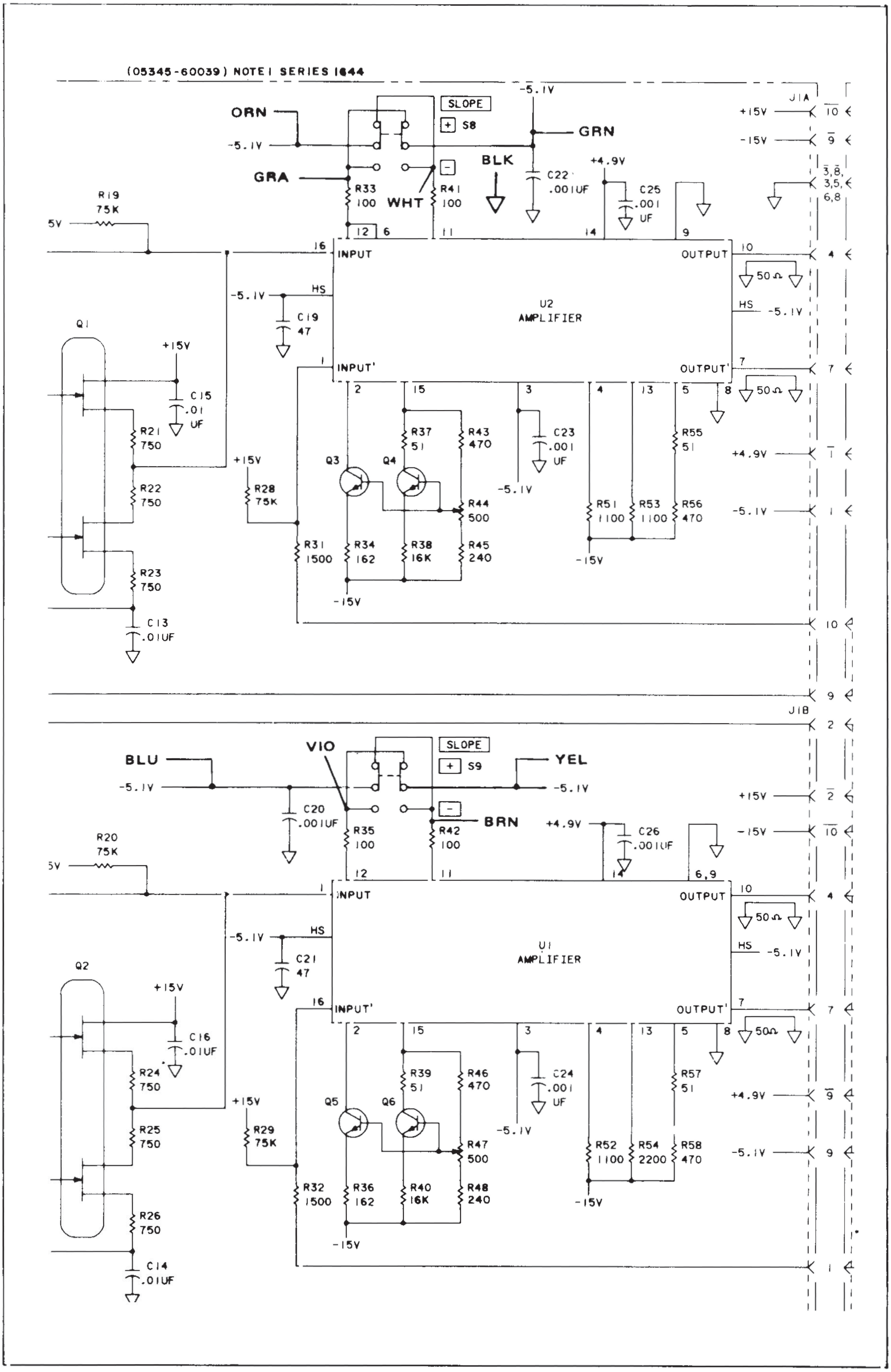
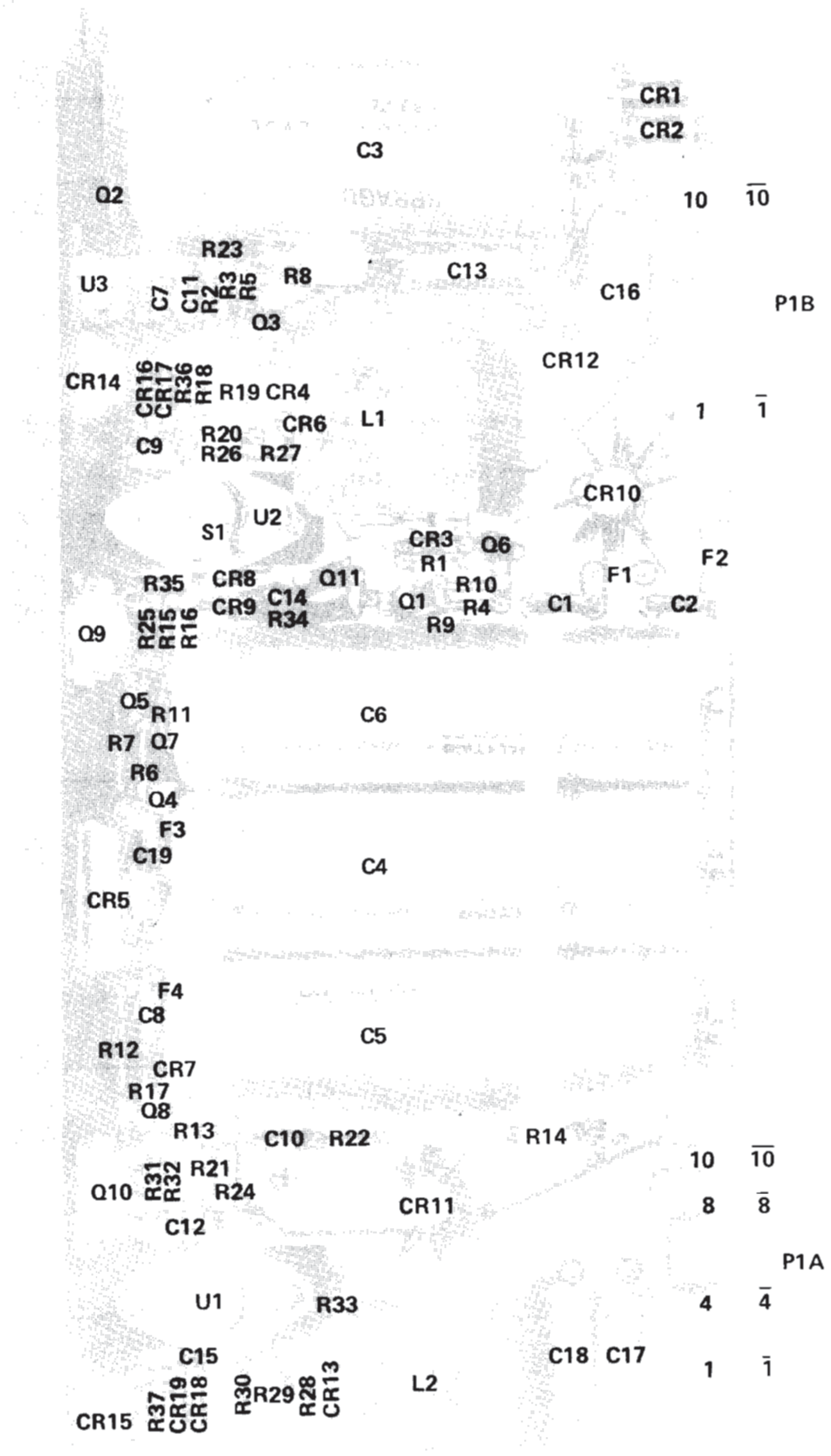
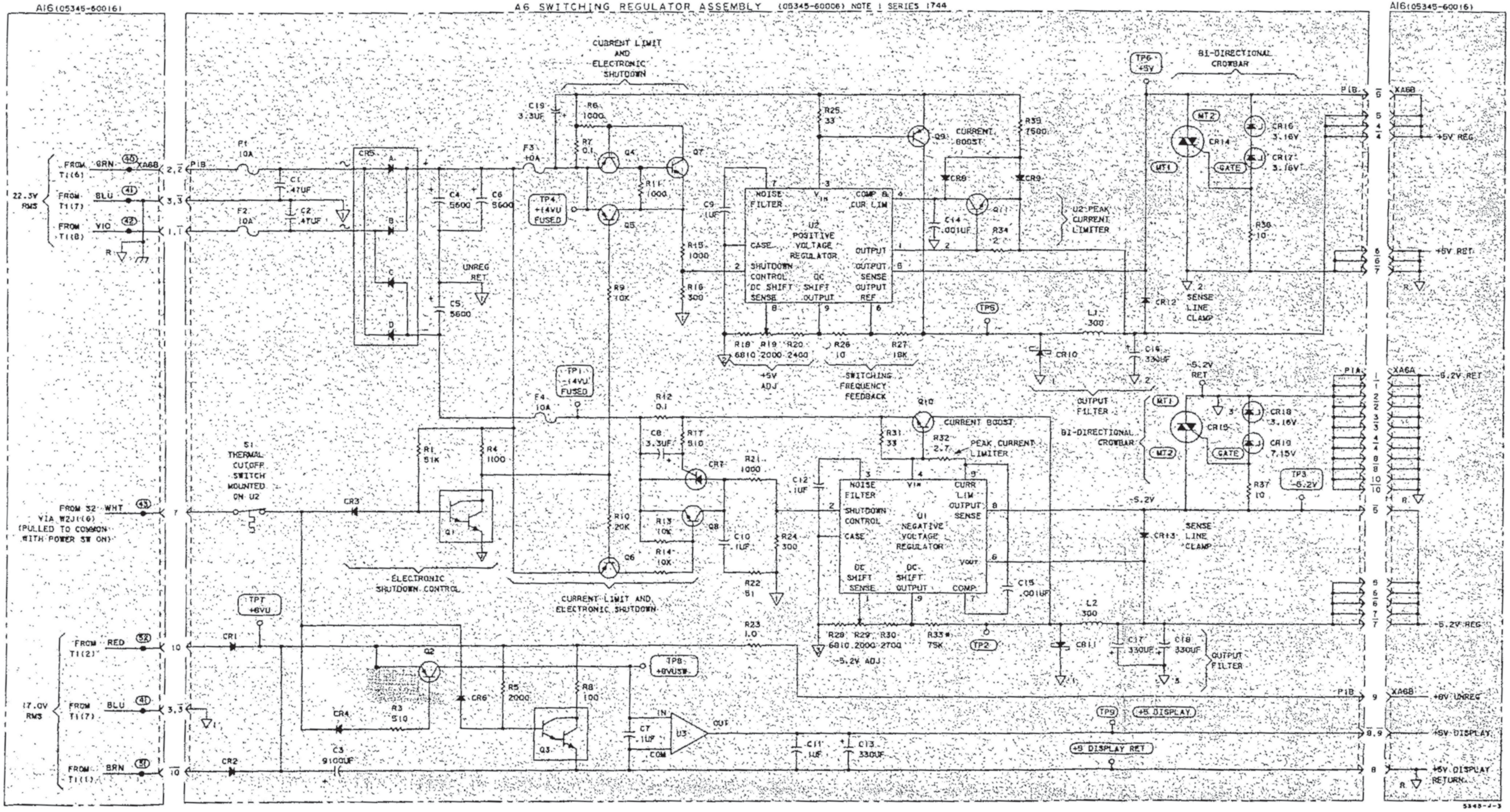


Figure 8-8A. Partial A3 Schematic (05345-60029 or 05345-60039) for Option 012


CR1
CR2
C3
Q2
10
$\overline{10}$
R23
U3
C7
C11
R2
R3
R5
R8
C13
C16
P1B
Q3
CR12
CR14
CR16
CR17
R36
R18
R19
CR4
1
$\overline{1}$
L1
CR6
C9
R20
R26
R27
CR10
U2
S1
CR3
Q6
R1
F2
F1
R35
CR8
Q11
R10
C14
Q1
R4
C1
C2
CR9
R34
R9
Q9
R25
R15
R16
Q5
R11
C6
R7
Q7
R6
Q4
F3
C19
C4
CR5
F4
C8
C5
R12
CR7
R17
Q8
R13
C10
R22
R14
10
$\overline{10}$
Q10
R31
R32
R21
R24
CR11
8
$\overline{8}$
C12
P1A
U1
R33
4
$\overline{4}$
C15
C18
C17
1
$\overline{1}$
R37
CR19
CR18
R30
R29
R28
CR13
L2
CR15

5345-A-32



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

REFERENCE DESIGNATIONS

A6	A16
C1-19	
CR1-19	
F1-4	
L1,2	
P1	
Q1-11	
R1-37	
S1	
U1-3	XA6

Figure 8-9. A6 Switching Regulator Assembly

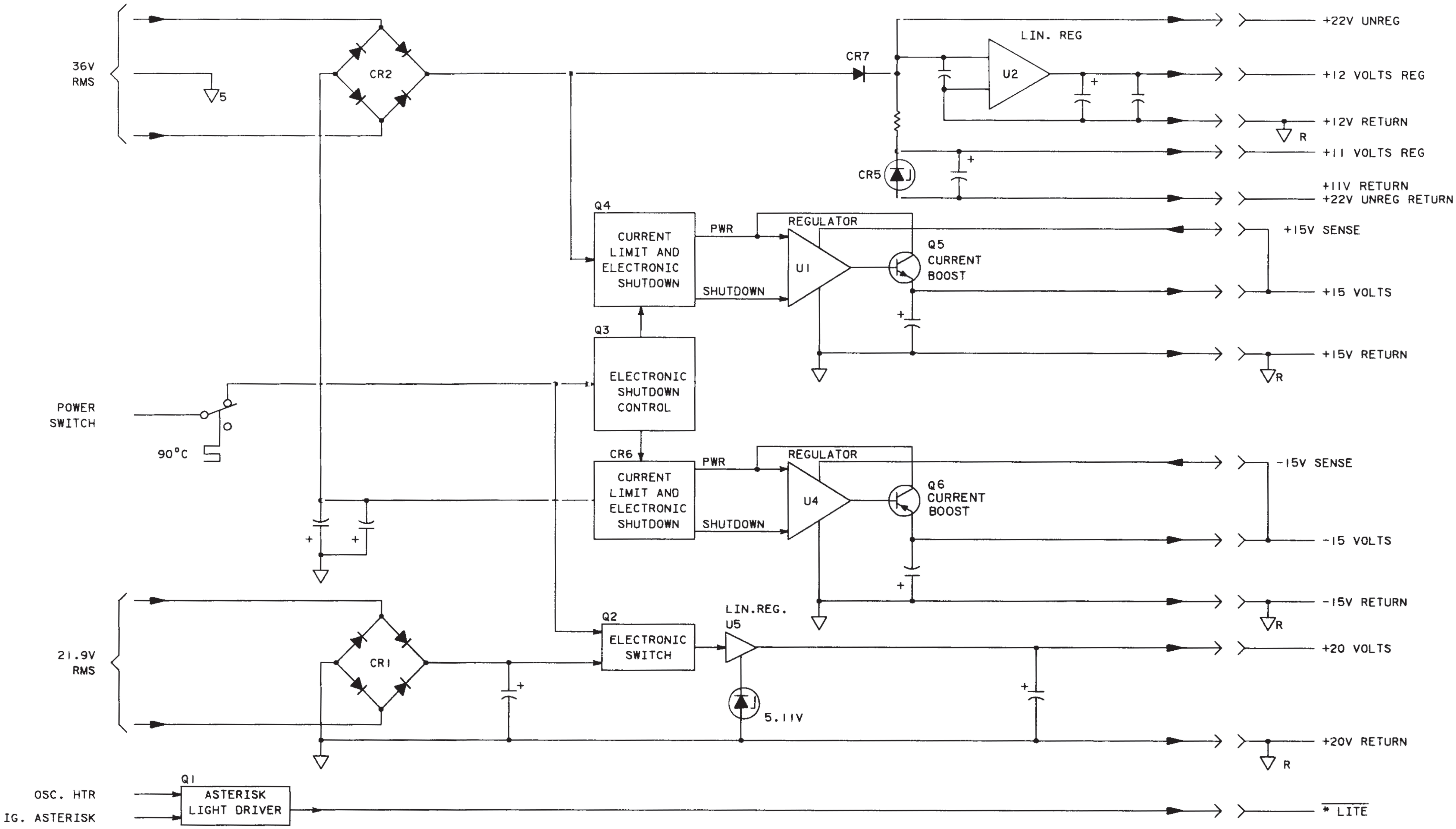
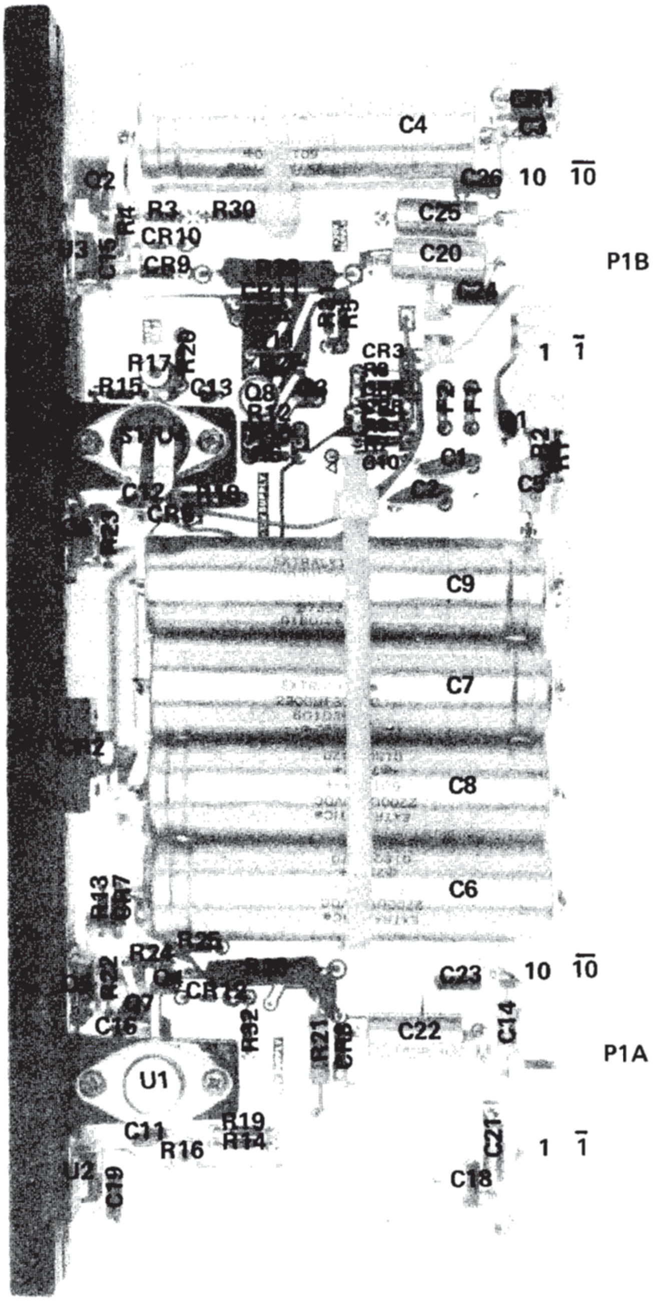
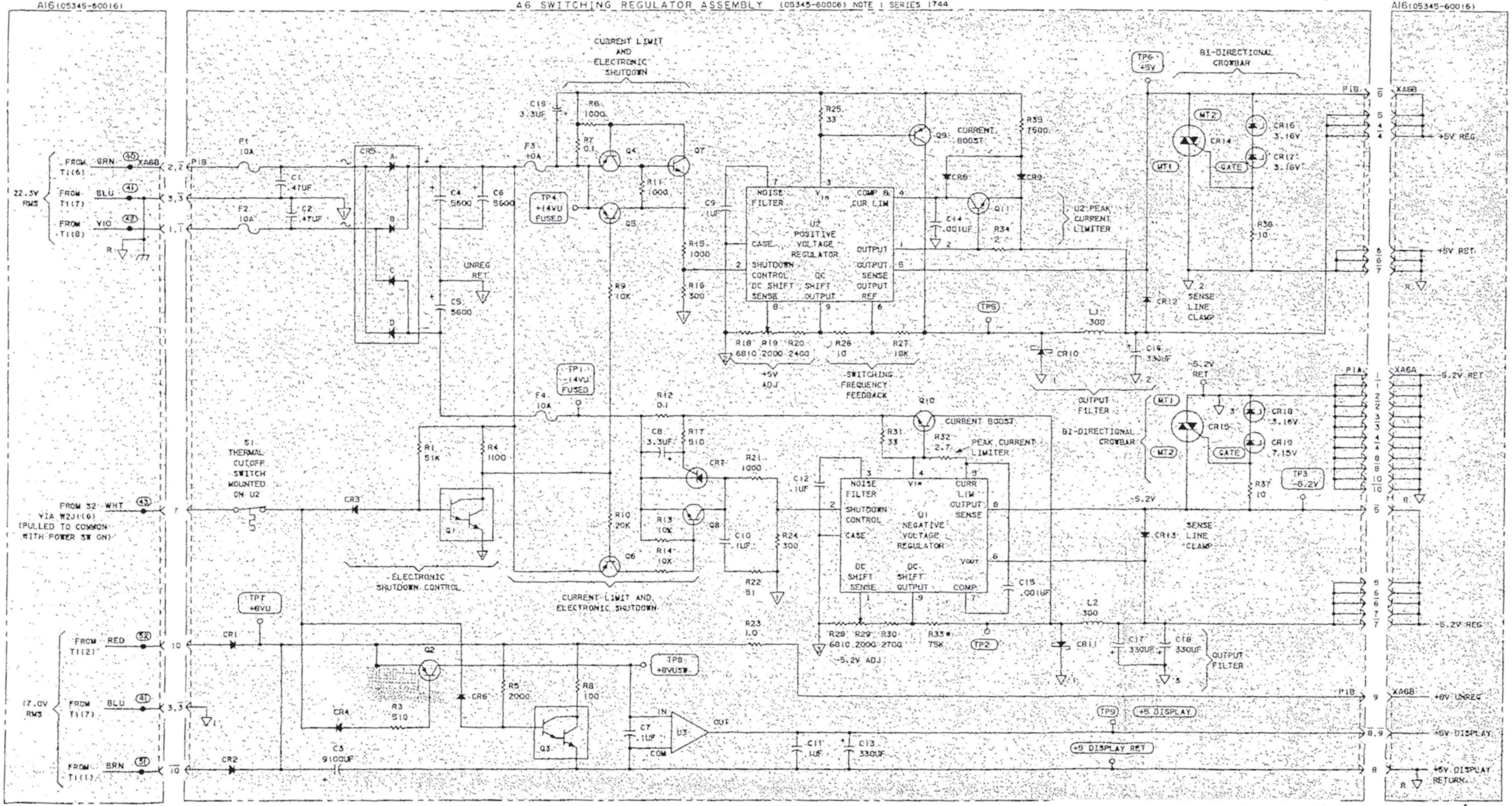


Figure 8-9
A6 SWITCHING REGULATOR ASSEMBLY

(See Page 8-33)


C4
Q2
C26
10
$\overline{10}$
R3
R30
C25
CR10
U3
C15
CR9
C20
P1B
CR3
1
$\overline{1}$
R17
R15
C13
Q8
C1
C5
C12
CR8
C9
C7
CR2
C8
R43
CR7
C6
R24
R25
C23
10
$\overline{10}$
R22
CR12
Q7
C16
R32
R21
C22
C14
P1A
U1
C11
R19
R16
R14
C21
1
$\overline{1}$
U2
C19
C18

5345-A -33



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

REFERENCE DESIGNATIONS

A6	A16
C1-19 CR1-19 F1-4 L1,2 P1 Q1-11 R1-37 S1 U1-3	XA6

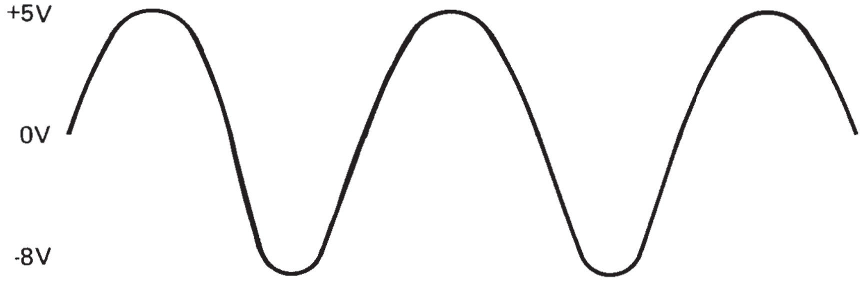
Figure 8-9. A6 Switching Regulator Assembly

Phase Lock Loop:

REPLACE:	606 — with 5 MHz House Standard (stable source necessary)
CONNECT:	Test Point 11 — to ground with Clip Lead (this unlocks oscillator)
OBSERVE:	DISPLAY — all readouts should be in LAMP TEST (all segments lit)

Continuing the Test Point Table:

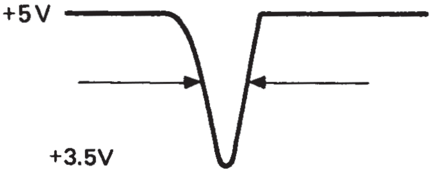
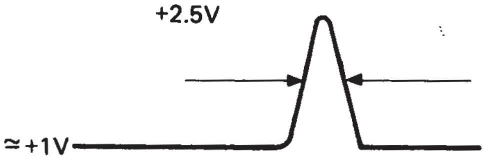
Test Points:	**Test Limit:**
9.	Low frequency Sine Wave ≃1 V P-P Sine Wave centered about +1 V (+0.5 V to +1.5 V).
10.	Distorted low frequency sine wave with positive peak between +4.5 and +6.0 volts and negative peak between -7.0 and -12.0 volts, with breaks at about +1.5 V.



REMOVE:	Clip Lead — from Test Point 11.
OBSERVE:	Test Point 10 — waveshape changes quickly to a DC Voltage between -5 V and +5 V. DISPLAY — LAMP TEST condition ceases in 3 sec. or less after clip lead is removed. Test Point 11 — has less noise than Test Point 10.

Test Points:

Connect 606A (10 MHz at 1.0V rms) to EXT STD INPUT thru 50Ω.

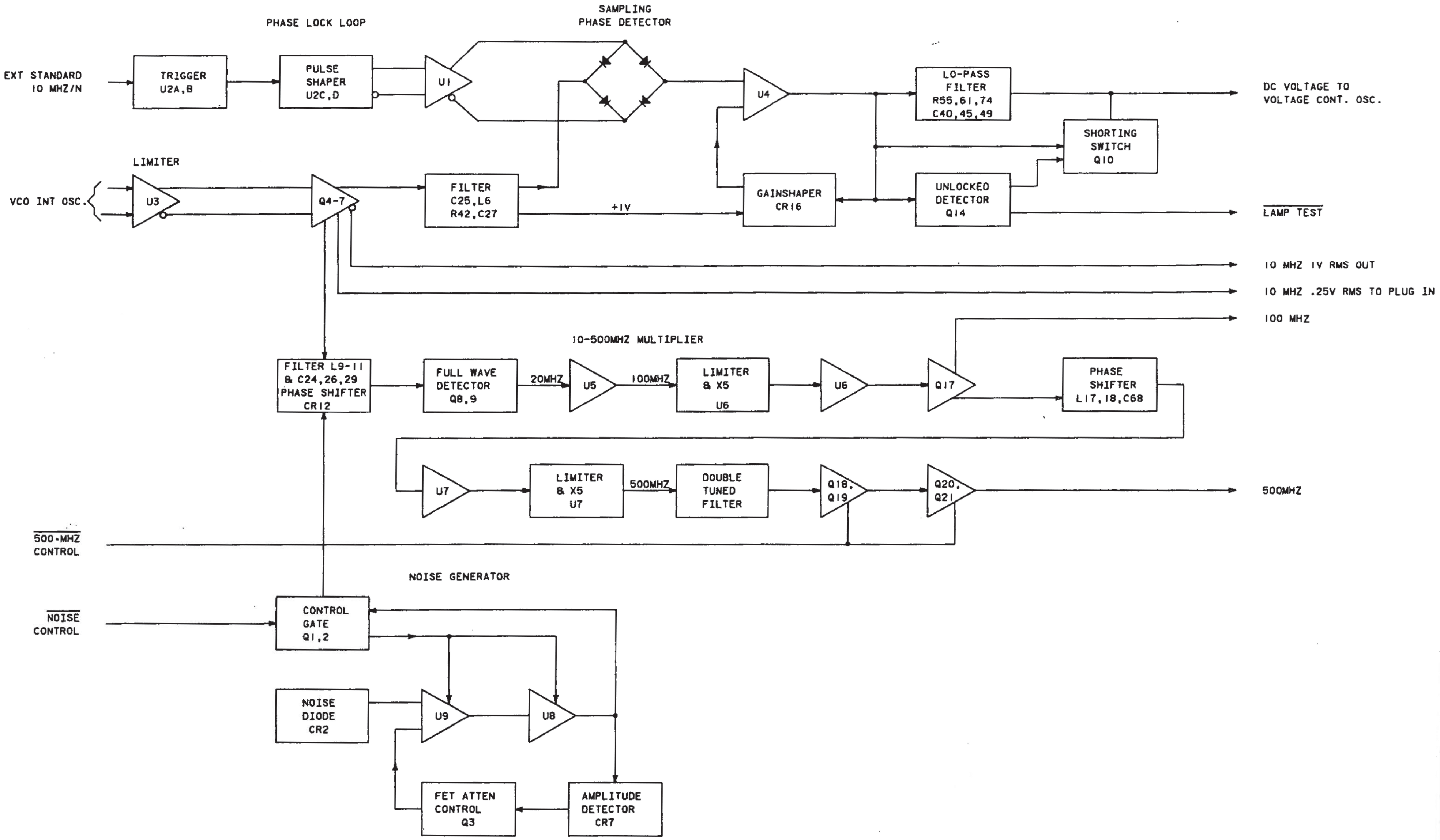
Test Points	**Test Limits**
1.	+8.5V to +9.5V DC
2.	10 MHz, 2 to 3 V P-P centered around the DC voltage at T.P. 1.
3.	+0.9V to +1.1V DC.
4.	10 MHz Sine Wave, 1.0 to 1.5 V P-P centered around the DC voltage at T.P. 3.
5.	10 MHz Sine Wave, 3 to 6 V P-P (>1 V rms).
6.	10 MHz Sine Wave, 0.7 to 2.5 V P-P (> .225 V rms).
7.	1 to 2 V Neg. Pulse 20 to 40 nS wide starting from +5V base line. 
8.	1 to 2 V Pos. Pulse 20 to 40 nS wide starting from ≃+1 V base line. 

Check the voltage level of 606 where the above waveform drops out.

TEST LIMIT: .25 to .5 V rms.

Figure 8-10
A7 LINEAR REGULATOR ASSEMBLY

(See page 8-35)


PHASE LOCK LOOP
SAMPLING PHASE DETECTOR
EXT STANDARD 10 MHZ/N
TRIGGER U2A,B
PULSE SHAPER U2C,D
U1
U4
LO-PASS FILTER R55,61,74 C40,45,49
DC VOLTAGE TO VOLTAGE CONT. OSC.
SHORTING SWITCH Q10
LIMITER
VCO INT OSC.
U3
Q4-7
FILTER C25,L6 R42,C27
+1V
GAINSHAPER CR16
UNLOCKED DETECTOR Q14
LAMP TEST
10 MHZ 1V RMS OUT
10 MHZ .25V RMS TO PLUG IN
100 MHZ
10-500MHZ MULTIPLIER
FILTER L9-11 & C24,26,29 PHASE SHIFTER CR12
FULL WAVE DETECTOR Q8,9
20MHZ
U5
100MHZ
LIMITER & X5 U6
U6
Q17
PHASE SHIFTER L17,18,C68
U7
LIMITER & X5 U7
500MHZ
DOUBLE TUNED FILTER
Q18, Q19
Q20, Q21
500MHZ
500-MHZ CONTROL
NOISE GENERATOR
NOISE CONTROL
CONTROL GATE Q1,2
NOISE DIODE CR2
U9
U8
FET ATTEN CONTROL Q3
AMPLITUDE DETECTOR CR7

Noise Generator:

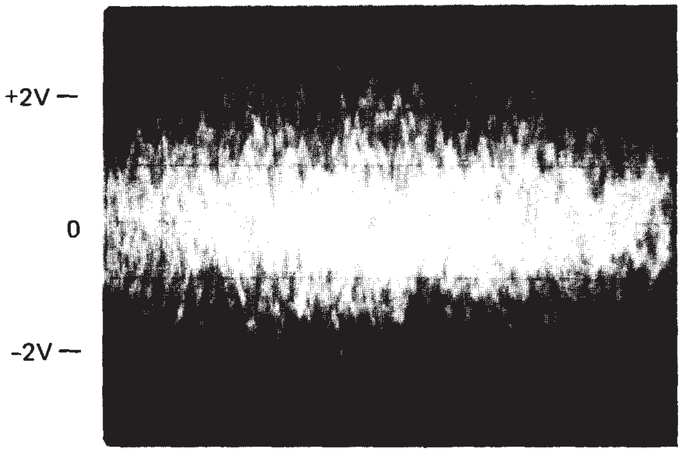
SET: 5345 FUNCTION — to T.I. position.

MEASURE: DC Voltage at Test Point 12 with scope probe

TEST LIMIT: Between -1.8 and -5 V DC.

CONNECT: Scope probe — to Test Point 13

SET: SCOPE —.1 mS/CM



SET: 5345 FUNCTION — to PERIOD

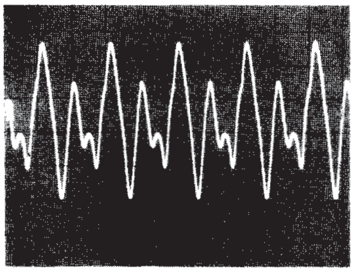
OBSERVE: Test Point 13 — -15 V and no noise with scope probe

NOTE:

Pin 5 XA8A Noise Control	Noise
0 to 1 V	ON
+2 to +5 V	OFF

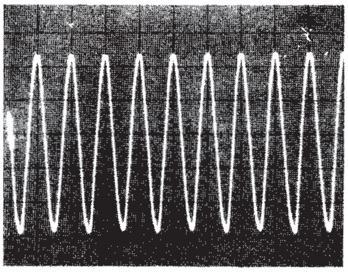
Equipment: 180A with 1810A and 10020A Probe

TP-14



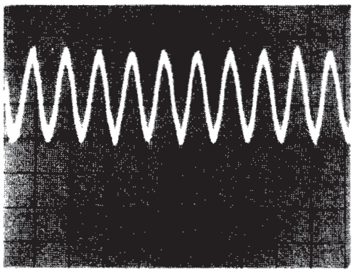
20 mV/div, EXPANDED, expanded to 50 nsec, direct to 50 nsec TRIGGER-EXT, NORM

TP-15



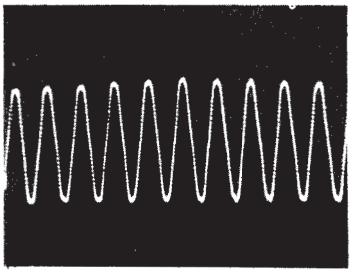
20 mV/div, EXPANDED, expanded to 50 nsec, direct to 50 nsec TRIGGER-EXT, NORM

TP-16



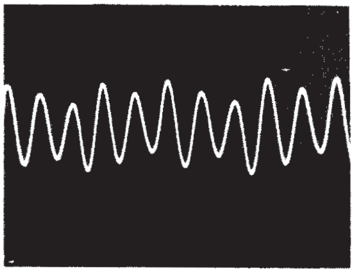
2 mV/div, EXPANDED to 10 nsec, direct to 10 nsec TRIGGER-EXT, NORM

TP-17



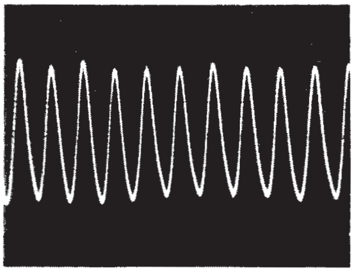
10 mV/div, EXPANDED to 10 nsec, direct to 10 nsec TRIGGER-EXT, NORM

TP-18



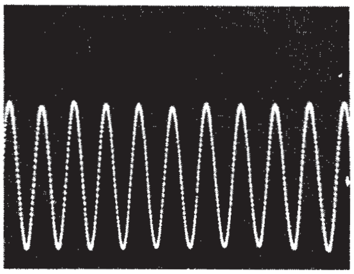
10 mV/div, EXPANDED to 2 nsec, direct to 10 nsec TRIGGER-EXT, NORM

TP-19



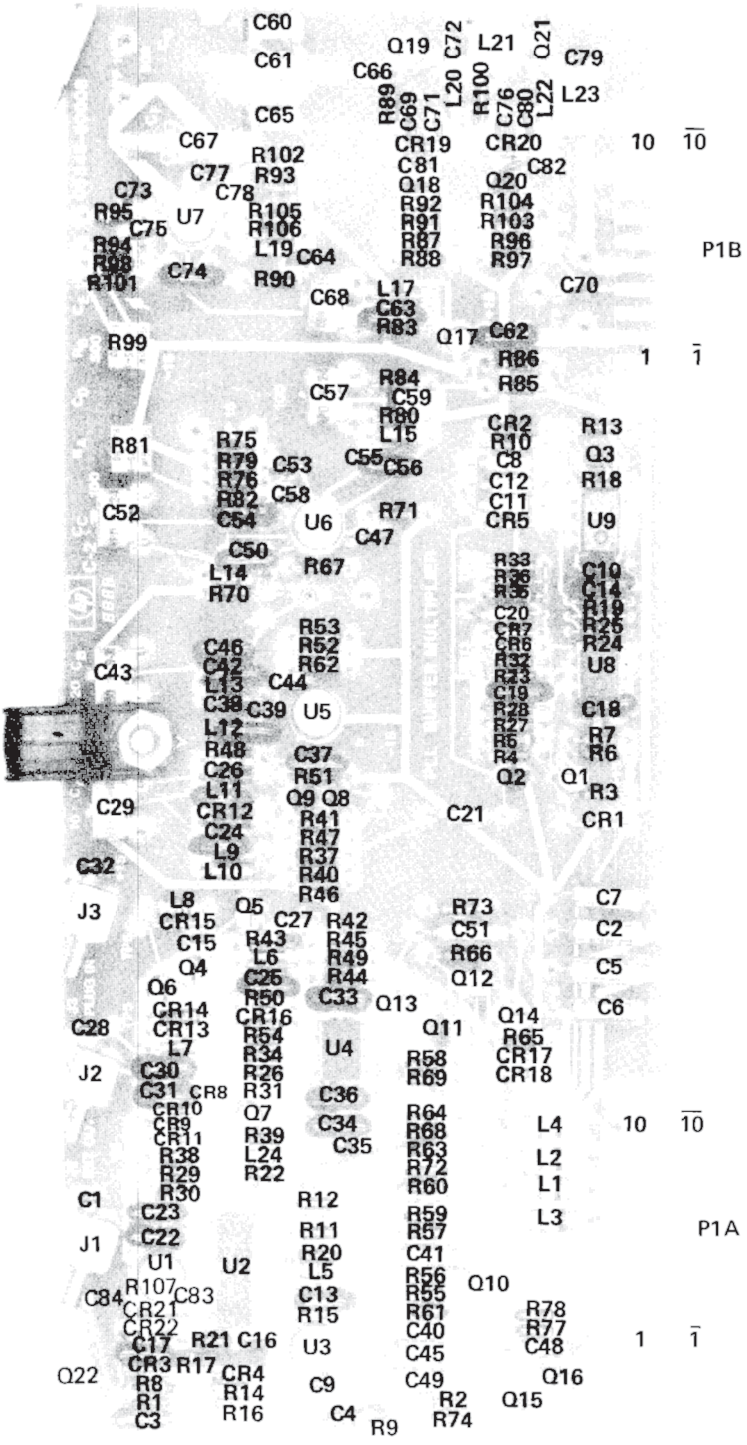
5 mV/div, EXPANDED to 2 ns, direct to 10 nsec TRIGGER-EXT, NORM

TP-20



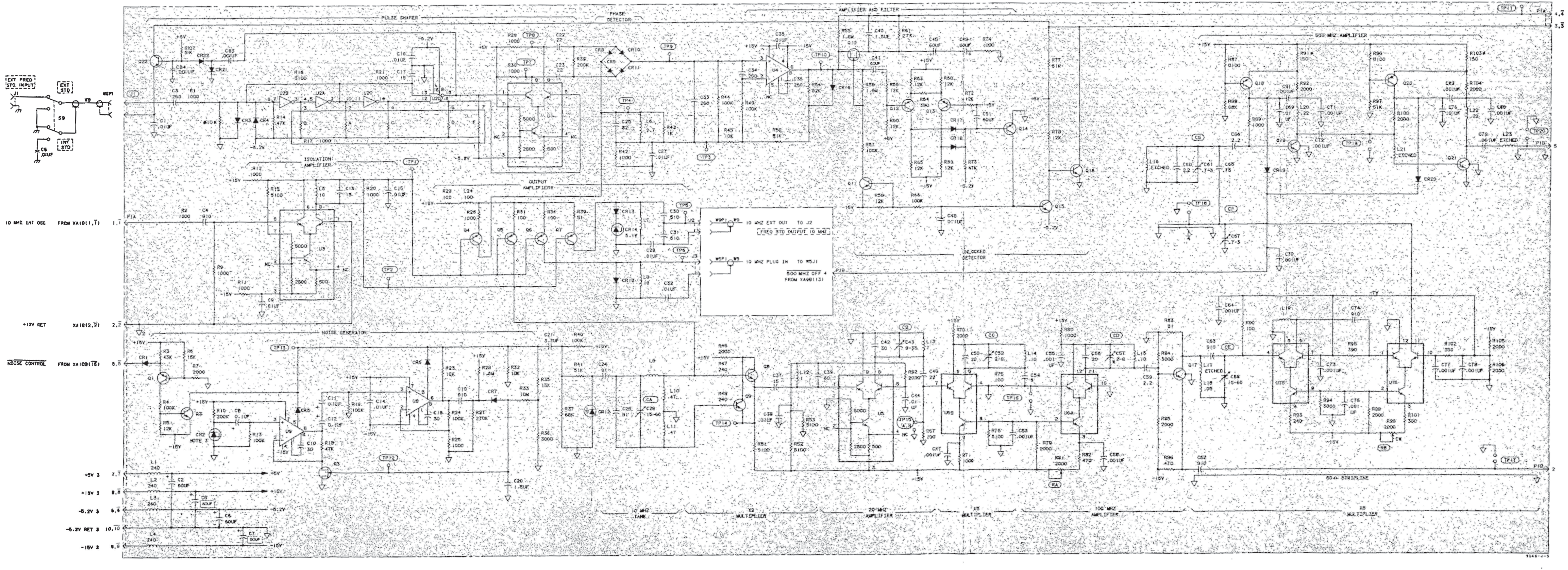
10 mV/div, other settings same as TP-19

Part of Figure 8-11. A8 PLL Multiplier Noise Generator Assembly


C60
C61
Q19
C72
L21
Q21
C79
C66
C65
R89
C69
C71
L20
R100
C76
C80
L22
L23
C67
CR19
CR20
10
10̄
R102
C81
C82
C77
R93
Q18
Q20
C73
C78
R92
R104
R95
C75
U7
R105
R106
R91
R103
R94
R98
R101
L19
C64
R87
R88
R96
R97
P1B
C74
R90
C68
L17
C63
R83
C70
Q17
C62
R99
R86
1
1̄
C57
R84
C59
R85
R80
L15
CR2
R10
R13
R81
R75
R79
C53
C55
C56
C8
Q3
R76
C12
R18
R82
C58
C11
C52
C54
U6
R71
CR5
U9
C47
C50
L14
R67
R33
R36
R35
C10
C14
R70
R19
C20
CR7
CR6
R25
R24
R53
R52
C46
C42
R62
C43
R32
R23
U8
L13
C44
C19
C38
C39
U5
R28
C18
L12
R27
R7
R5
R6
R48
C37
R4
C26
R51
Q2
Q1
R3
L11
Q9
Q8
C29
CR12
R41
C21
CR1
C24
R47
L9
R37
C32
L10
R40
R46
C7
L8
J3
CR15
Q5
C27
R42
R73
C2
C15
R43
R45
C51
L6
R49
R66
C5
Q4
C25
R44
Q12
Q6
R50
C33
Q13
C6
CR14
CR16
Q11
Q14
C28
CR13
R54
R65
L7
R34
U4
R58
CR17
J2
C30
R26
R69
CR18
C31
CR8
R31
C36
CR10
Q7
R64
CR9
C34
R68
L4
10
10̄
CR11
R39
R63
R38
L24
C35
L2
R29
R22
R72
R30
R60
L1
C1
R12
C23
R59
L3
J1
C22
R11
R57
P1A
U1
U2
R20
C41
L5
R56
Q10
C84
R107
C83
C13
R55
R78
CR21
R15
R61
R77
CR22
C40
C17
R21
C16
U3
C45
C48
1
1̄
CR3
R17
CR4
Q22
R8
R14
C9
C49
Q16
R1
R16
R2
Q15
C3
C4
R9
R74

5345-A-34

A8 PLL MULTIPLIER NOISE GENERATOR ASSEMBLY (05345-60031)(NOTE 1) SERIES 2128



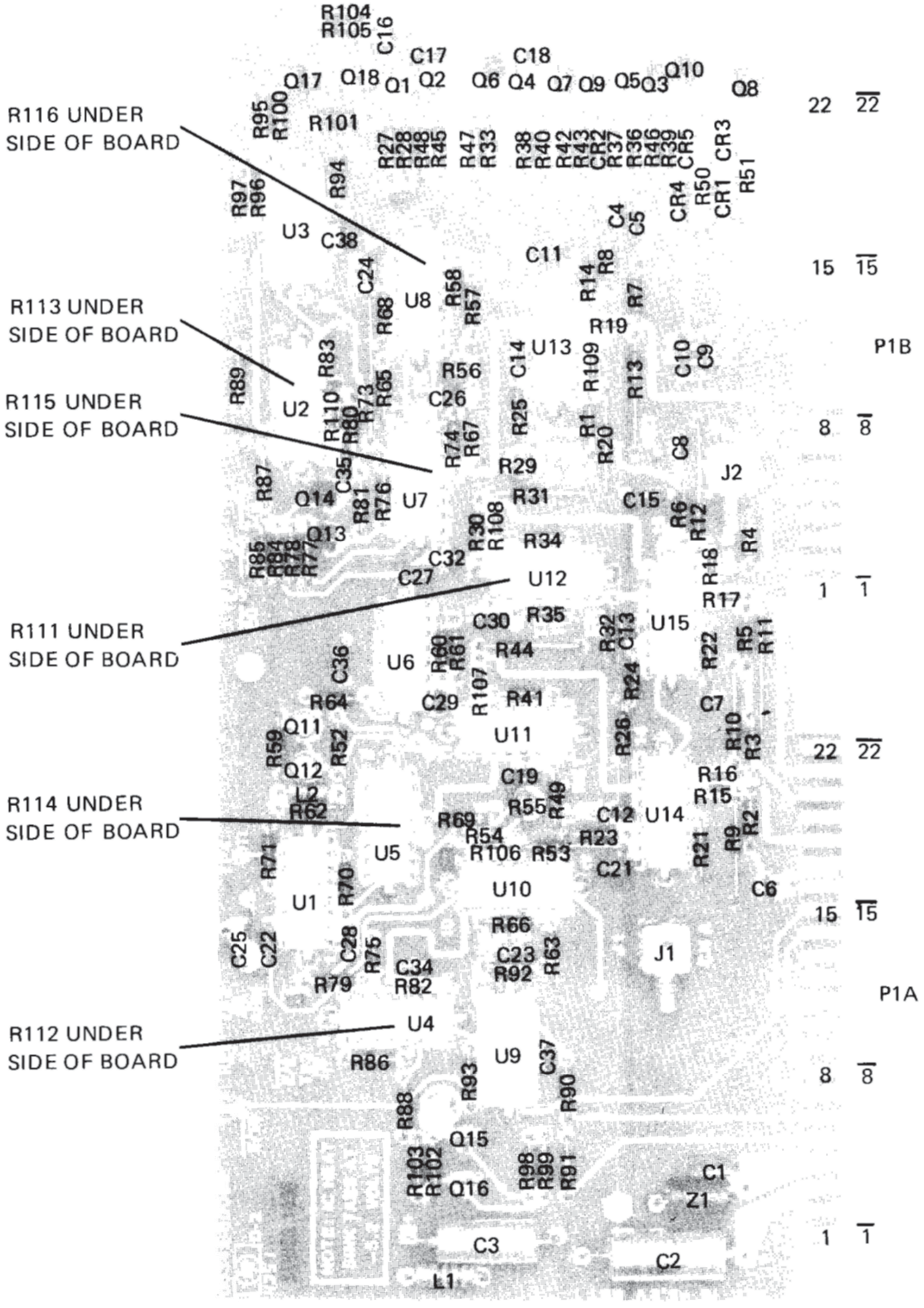
NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS,
   CAPACITANCE IN PICOFARADS,
   INDUCTANCE IN MICROHENRIES
3. CR2 IS FACTORY SELECTED FOR NOISE PROPERTIES AND MAY VARY IN BREAKDOWN VOLTAGE FROM 6 TO 10 VOLTS.
4. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN

REFERENCE DESIGNATIONS

NO PREFIX	A8
C6	C1-84
J1	CR1-22
S9	J1-3
W8	L1-24
	P1
	Q1-22
	R1-107
	U1-9

Figure 8-11. A8 PLL Multiplier Noise Generator Assembly



5345-A-35

Part of Figure 8-12. A9 Main Gate Assembly

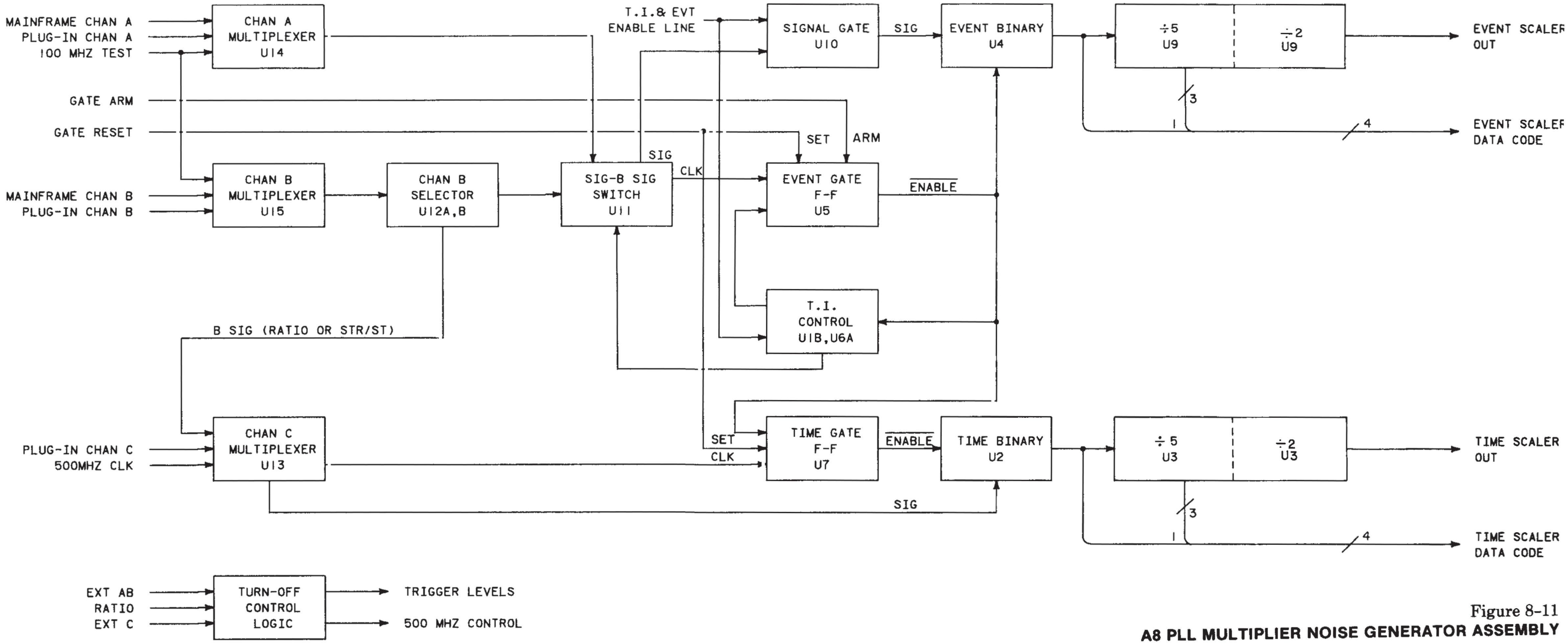


Figure 8-11
A8 PLL MULTIPLIER NOISE GENERATOR ASSEMBLY

(See Page 8-39)

IMPORTANT

A front panel bandwidth and input sensitivity check should be performed when a defective IC on A9 has been replaced. Proper plug-in operation should be confirmed with 5354A (checks Channel A) and 5353A (checks Channel C Ratio). If IC U8 or U10 through U15 has been replaced and the input specifications are not met, do *not* attempt any adjustments. Substitute another IC in its place and repeat the performance test. A replacement IC that meets the performance tests does not indicate that the previous IC was faulty, only that its characteristics were not in accordance with the factory selected bias resistors. If the counter continues to fail the bandwidth or sensitivity test, the board should be returned to the factory. Send the A9 board to your nearest Hewlett-Packard Sales and Service Office listed at the back of this manual.

Simplified Flow Diagrams of A9 are contained in Figures 5-14 through 5-16.

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES
3. ASTERISK (*) INDICATES SELECTED COMPONENT, AVERAGE VALUES SHOWN
4. SUPPLY VOLTAGE IS SELECTED AT FACTORY.

REFERENCE DESIGNATIONS

A9
C1-38
CR1-5
J1,2
L1,2
P1
Q1-18
R1-116
U1-15
Z1

5345-D-27

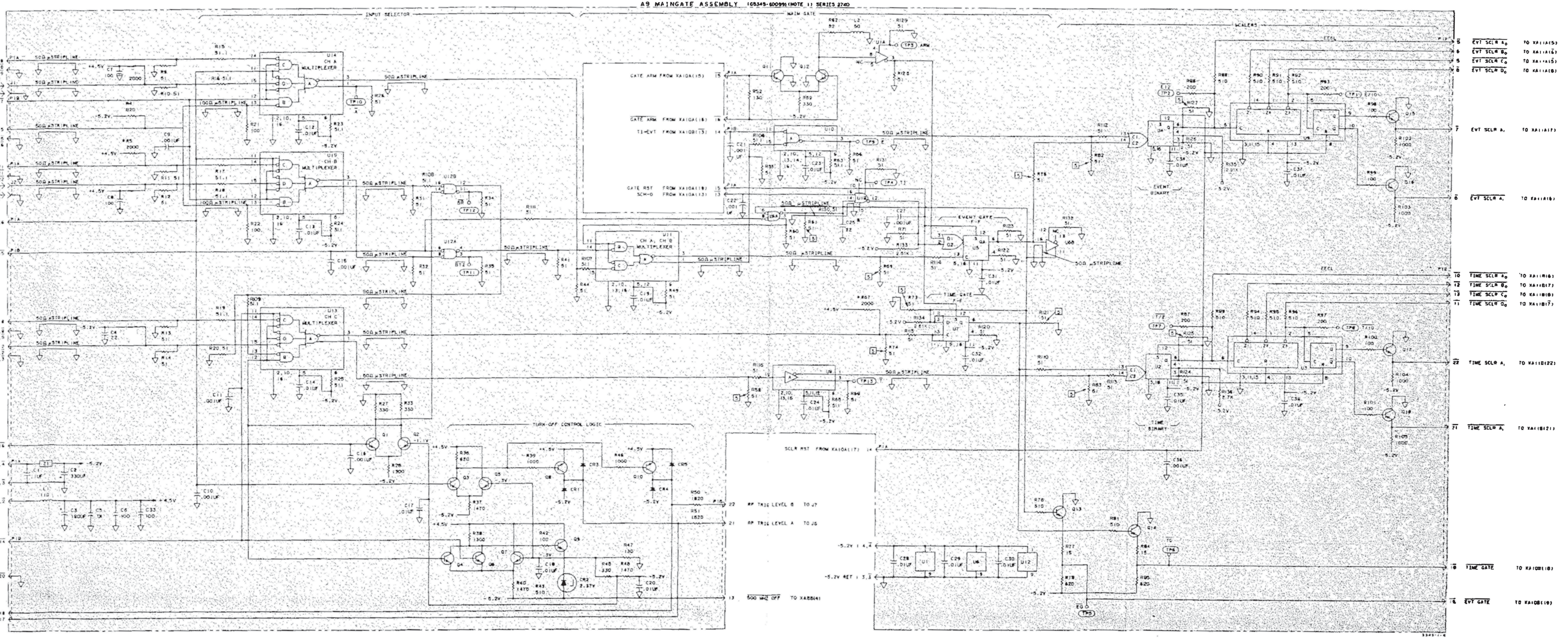
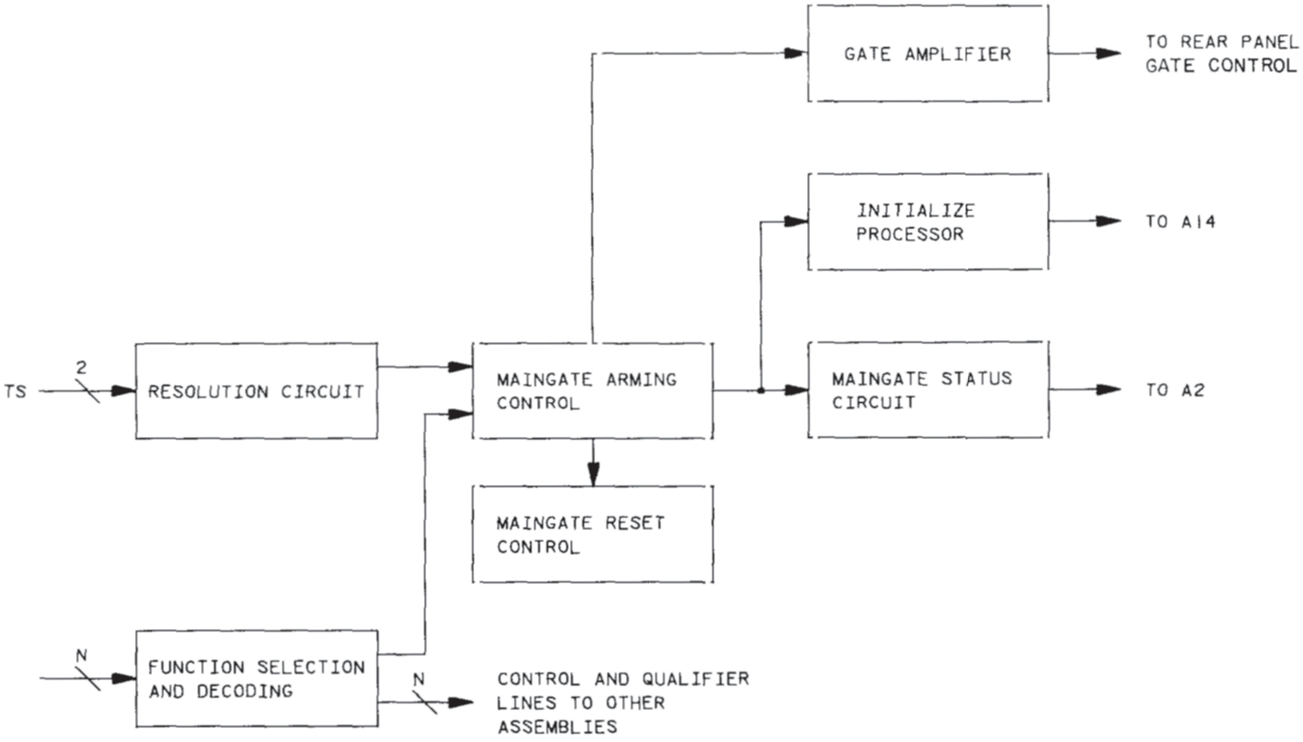
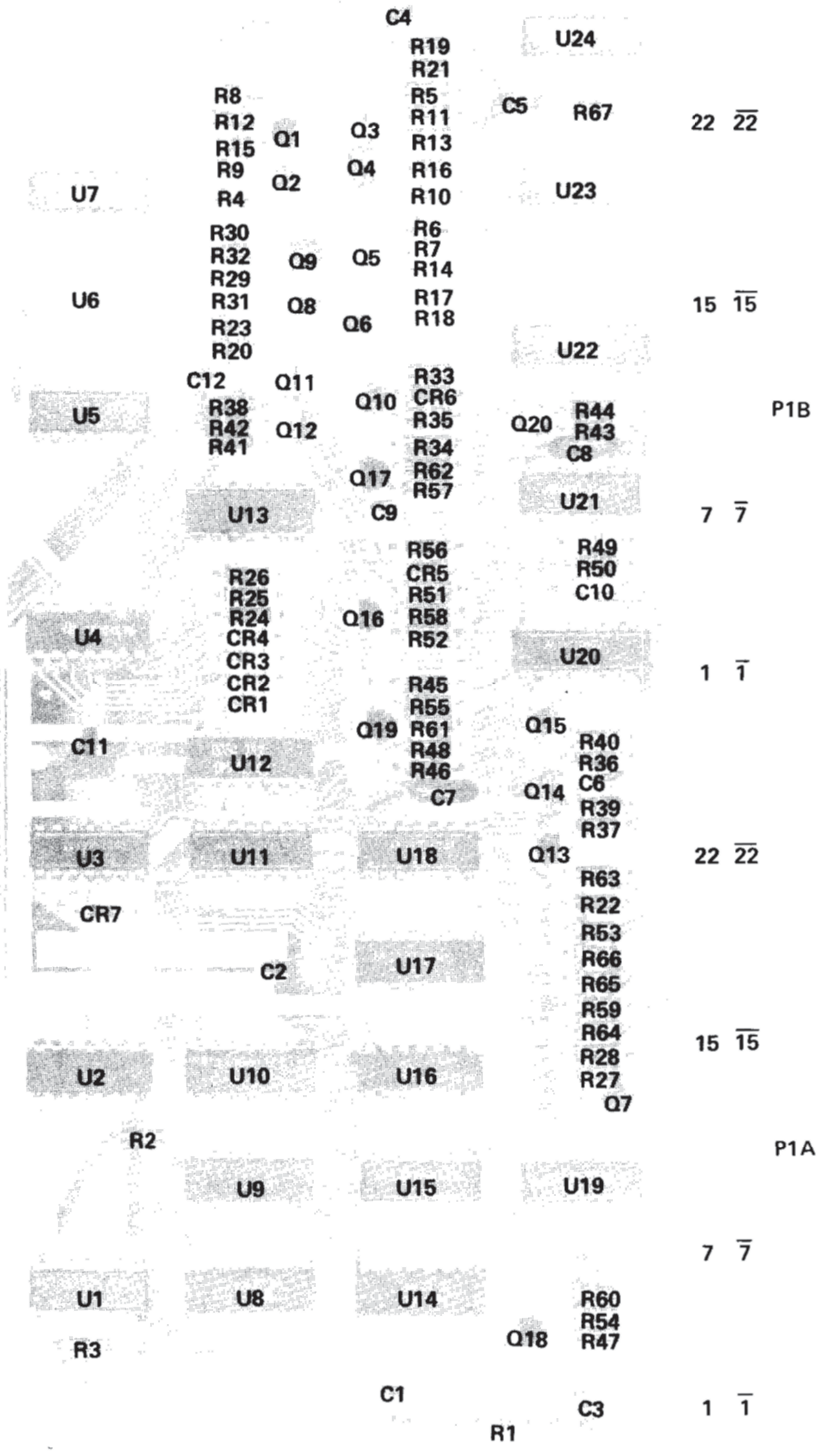
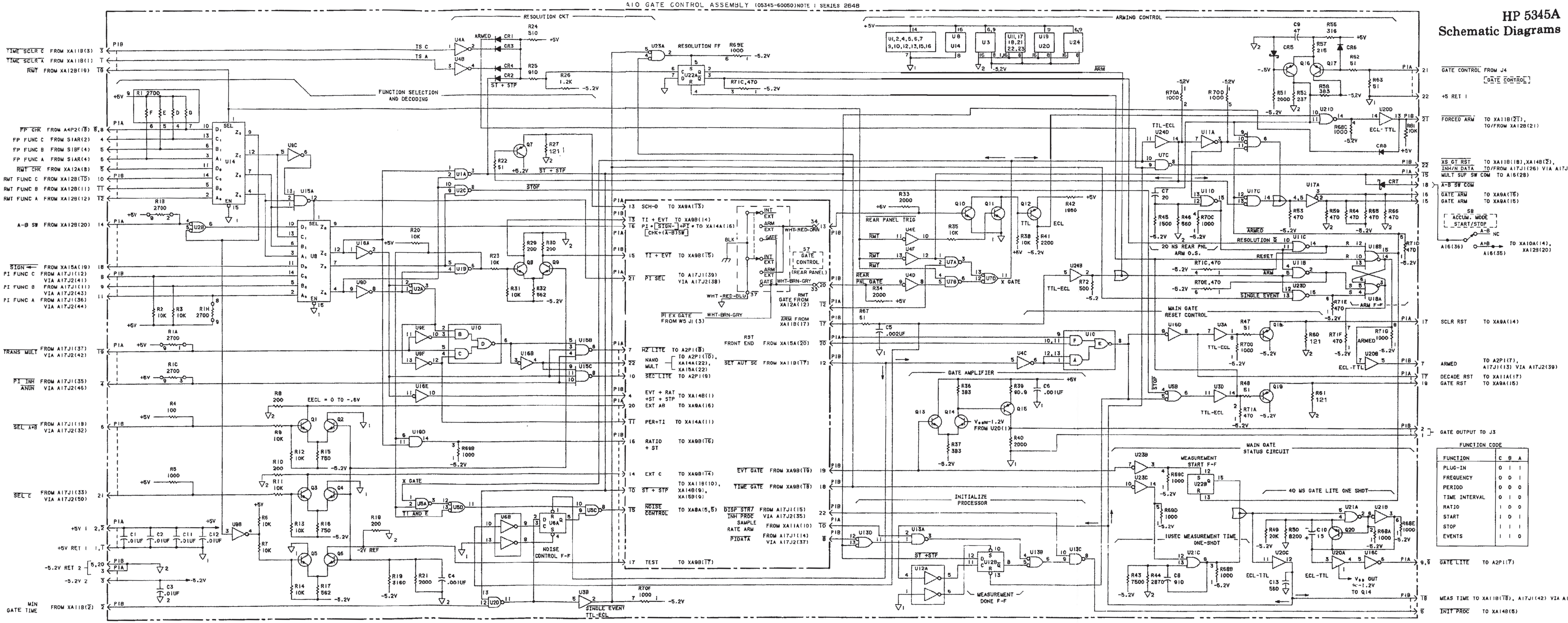


Figure 8-12. A9 Main Gate Assembly


GATE AMPLIFIER
TO REAR PANEL GATE CONTROL
INITIALIZE PROCESSOR
TO A14
TS
2
RESOLUTION CIRCUIT
MAINGATE ARMING CONTROL
MAINGATE STATUS CIRCUIT
TO A2
MAINGATE RESET CONTROL
N
FUNCTION SELECTION AND DECODING
N
CONTROL AND QUALIFIER LINES TO OTHER ASSEMBLIES


C4
R19
R21
U24
R8
R5
R12
R11
C5
R67
22 $\overline{22}$
R15
Q1
Q3
R13
R9
Q4
R16
U7
Q2
R4
R10
U23
R30
R6
R32
R7
Q9
Q5
R14
R29
U6
R31
R17
Q8
15 $\overline{15}$
R23
Q6
R18
R20
U22
C12
Q11
R33
Q10
CR6
U5
R38
R35
Q20
R44
P1B
R42
Q12
R43
R41
R34
C8
Q17
R62
R57
U21
U13
C9
7 $\overline{7}$
R56
R49
R26
CR5
R50
R25
R51
C10
R24
Q16
R58
U4
CR4
R52
U20
CR3
1 $\overline{1}$
CR2
R45
CR1
R55
Q19
R61
Q15
C11
R48
R40
U12
R46
R36
C7
Q14
C6
R39
R37
U3
U11
U18
Q13
22 $\overline{22}$
R63
CR7
R22
R53
U17
R66
C2
R65
R59
R64
15 $\overline{15}$
U2
U10
U16
R28
R27
Q7
R2
P1A
U9
U15
U19
7 $\overline{7}$
U1
U8
U14
R60
R54
Q18
R47
R3
C1
C3
1 $\overline{1}$
R1

5345-A-36


A10 GATE CONTROL ASSEMBLY (05345-60050)NOTE 1 SERIES 2648
RESOLUTION CKT
ARMING CONTROL
FUNCTION SELECTION AND DECODING
RESOLUTION FF
GATE AMPLIFIER
MAIN GATE RESET CONTROL
MAIN GATE STATUS CIRCUIT
MEASUREMENT START F-F
1USEC MEASUREMENT TIME ONE-SHOT
40 MS GATE LITE ONE SHOT
INITIALIZE PROCESSOR
MEASUREMENT DONE F-F
NOISE CONTROL F-F
SINGLE EVENT TTL-ECL
20 NS REAR PNL ARM O.S.
REAR PANEL TRIG
ARM F-F
EECL = 0 TO -.8V
-2V REF
S7 GATE CONTROL (REAR PANEL)
S8 ACCUM. MODE START/STOP
TIME SCLR C FROM XA11B(3)
TIME SCLR A FROM XA11B(1)
RMT FROM XA12B(19)
FP CHK FROM A4P2(18)
FP FUNC C FROM S1AR(2)
FP FUNC B FROM S1BF(4)
FP FUNC A FROM S1AR(4)
RMT CHK FROM XA12A(8)
RMT FUNC C FROM XA12B(15)
RMT FUNC B FROM XA12B(11)
RMT FUNC A FROM XA12B(12)
A-B SW FROM XA12B(20)
SIGN FROM XA15A(19)
PI FUNC C FROM A17J1(12) VIA A17J2(41)
PI FUNC B FROM A17J1(11) VIA A17J2(43)
PI FUNC A FROM A17J1(36) VIA A17J2(44)
TRANS MULT FROM A17J1(37) VIA A17J2(42)
PI INH ANUN FROM A17J1(35) VIA A17J2(46)
SEL A+B FROM A17J1(18) VIA A17J2(32)
SEL C FROM A17J1(33) VIA A17J2(50)
+5V 1
+5V RET 1
-5.2V RET 2
-5.2V 2
MIN GATE TIME FROM XA11B(2)
GATE CONTROL FROM J4
+5 RET 1
FORCED ARM TO XA11B(21), TO/FROM XA12B(21)
XS GT RST TO XA11B(18),XA14B(2), INH/N DATA TO/FROM A17J1(26) VIA A17J2(54)
MULT SUF SW COM TO A16(28)
A-B SW COM
GATE ARM TO XA9A(15)
GATE ARM TO XA9A(15)
SCLR RST TO XA9A(14)
ARMED TO A2P1(7), A17J1(13) VIA A17J2(39)
DECADE RST TO XA11A(17)
GATE RST TO XA9A(15)
GATE OUTPUT TO J3
GATE LITE TO A2P1(7)
MEAS TIME TO XA11B(18), A17J1(42) VIA A17J2(28)
INIT PROC TO XA14B(5)
SCH-O TO XA9A(13)
TI + EVT TO XA9B(14)
PI • SIGN • PI • TO XA14A(16)
TI + EVT TO XA9B(15)
PI SEL TO A17J1(39) VIA A17J2(38)
HZ LITE TO A2P1(8)
NANO MULT TO A2P1(10), XA14A(22), XA15A(22)
SEC LITE TO A2P1(9)
EVT + RAT +ST + STP TO XA14B(1)
EXT AB TO XA9A(16)
PER+TI TO XA14A(11)
RATIO + ST TO XA9B(16)
EXT C TO XA9B(14)
ST + STP TO XA11B(10), XA14B(9), XA15B(9)
NOISE CONTROL TO XA8A(5,5)
TEST TO XA9B(17)
RST FRONT END FROM XA15A(20)
SET AUT SC FROM XA11B(17)
RMT GATE FROM XA12A(12)
ARM FROM XA11B(17)
PI EX GATE FROM W5 J1(3)
EVT GATE FROM XA9B(19)
TIME GATE FROM XA9B(18)
DISP STR FROM A17J1(15)
INH PROC VIA A17J2(35)
SAMPLE RATE ARM FROM XA11A(10)
PIDATA FROM A17J1(14) VIA A17J2(37)
WHT-RED-BRN
WHT-BRN-GRY
WHT-RED-BLU
BLK
X GATE
TI AND E
ST + STP
STOP
ARMED
RESET
ARM
SINGLE EVENT
TTL-ECL
ECL-TTL

FUNCTION CODE

FUNCTION	C	B	A
PLUG-IN	0	1	1
FREQUENCY	0	0	1
PERIOD	0	0	0
TIME INTERVAL	0	1	0
RATIO	1	0	0
START	1	0	1
STOP	1	1	1
EVENTS	1	1	0

REFERENCE DESIGNATIONS

NO PREFIX	A10
	C1-12 CR1-7 P1 Q1-20 R1-67
S8	U1-24

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES

Figure 8-13. A10 Gate Control Assembly

5345-D-27

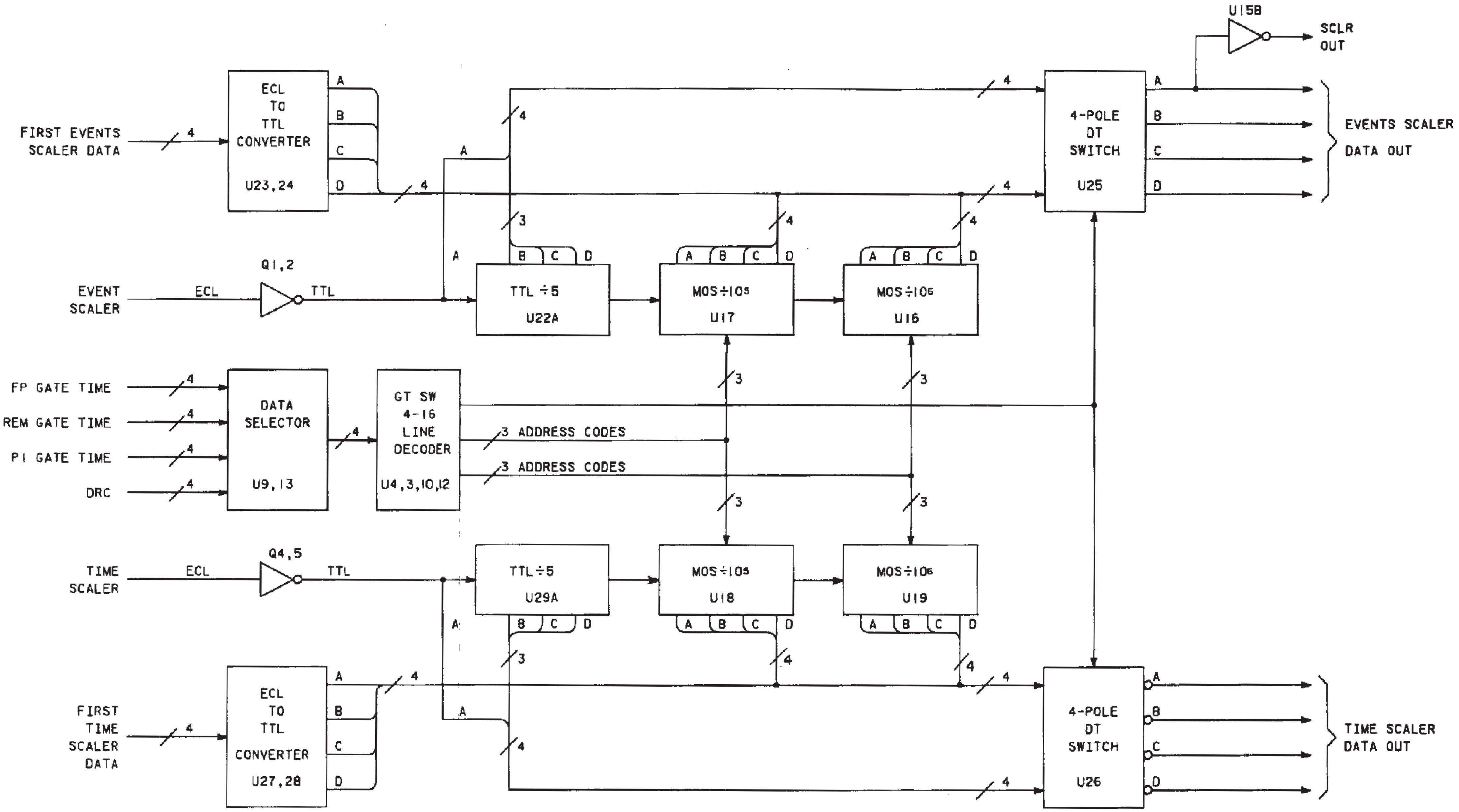


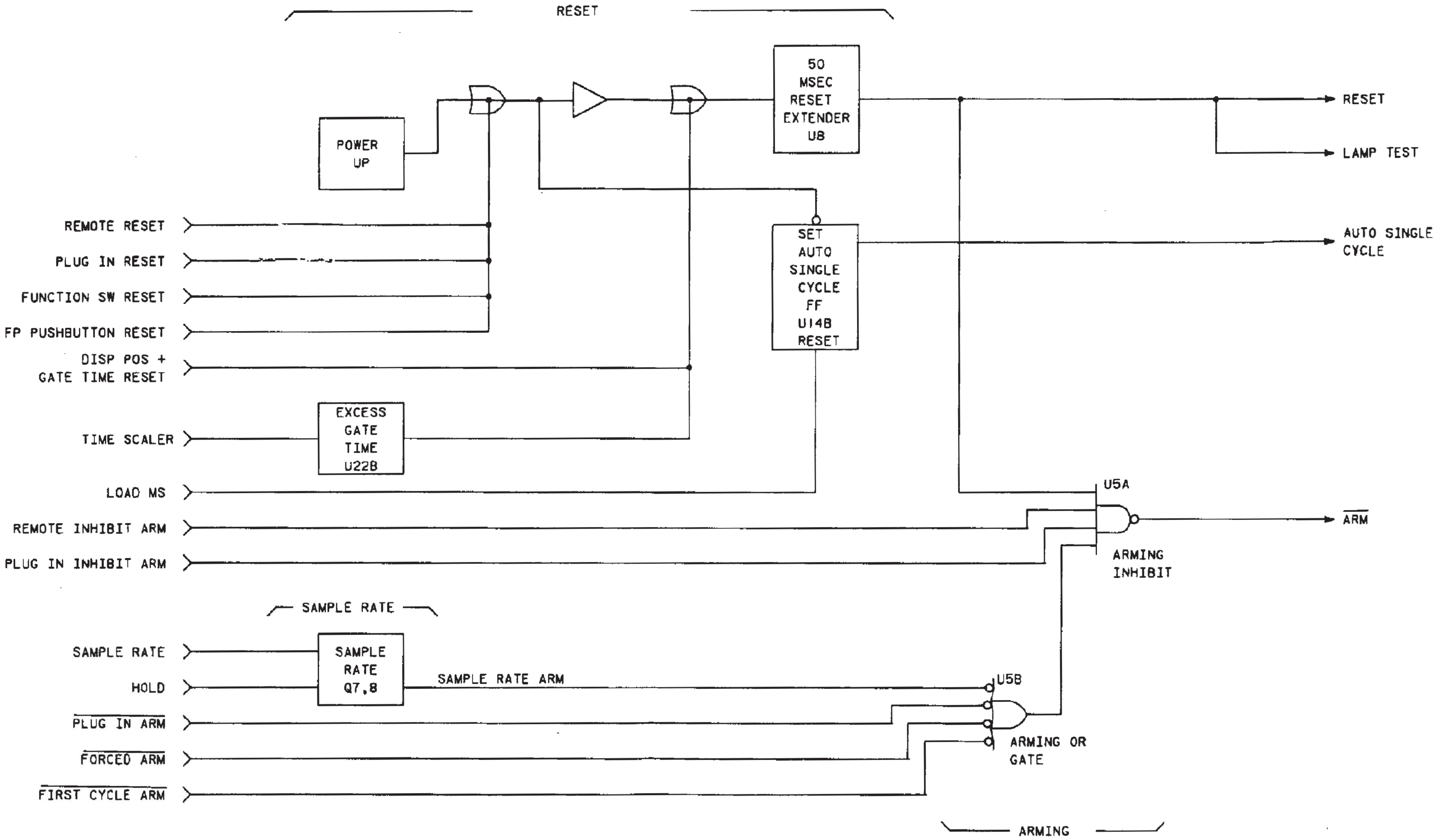
Figure 8-13
A10 GATE CONTROL ASSEMBLY

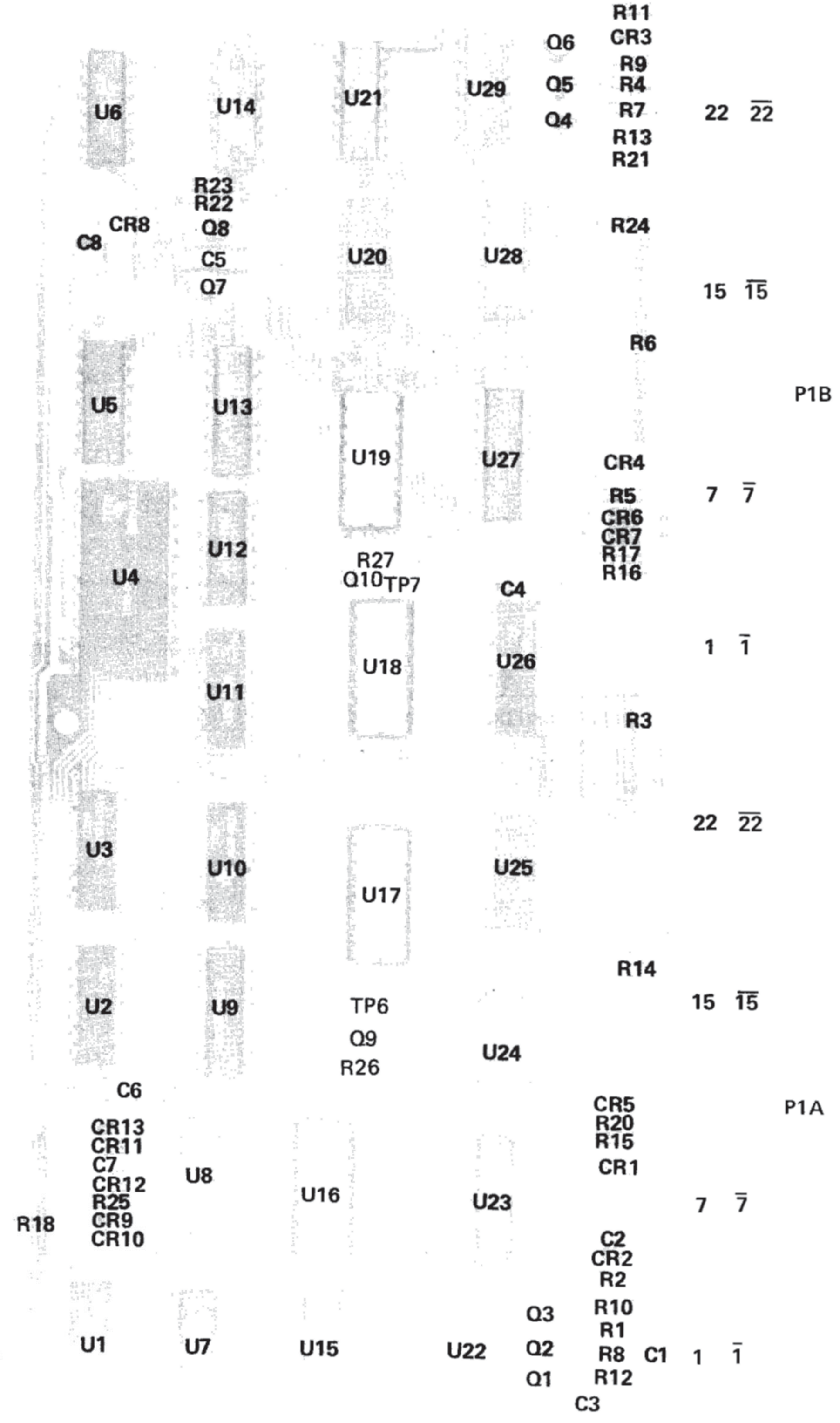
(See page 8-43)

TABLE 1

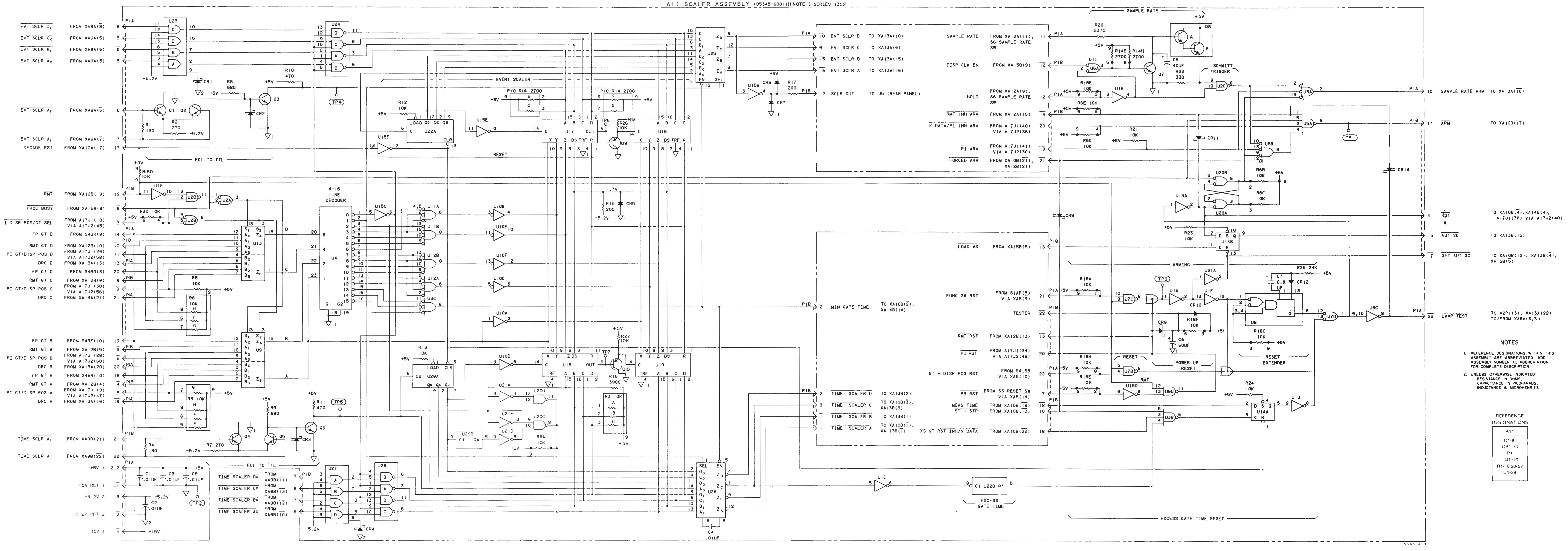
A11 05345-60011 SCALER ASSEMBLY

GATE TIME SETTING	U4 OUTPUT LINES	U17 AND U18			SELECTED BINARY	U16 AND U19			SELECTED BINARY
		X	Y	Z		X	Y	Z	
–	0	0	1	1	Open	1	1	1	Open
100 NS	1	1	1	1	Open	0	1	1	Open
1 μS	2	0	0	0	Decade 1	1	1	1	Open
10 μS	3	1	0	0	Decade 2	0	1	1	Open
100 μS	4	0	1	0	Decade 3	1	1	1	Open
1 MS	5	1	1	0	Decade 4	0	1	1	Open
10 MS	6	0	0	1	Decade 5	1	1	1	Open
100 MS	7	1	1	1	Open	0	0	0	Decade 1
1 S	8	0	1	1	Open	1	0	0	Decade 2
10 S	9	1	1	1	Open	0	1	0	Decade 3
100 S	10	0	1	1	Open	1	1	0	Decade 4
1000 S	11	1	1	1	Open	0	0	1	Decade 5
–	12	0	1	1	Open	1	1	1	Open
MIN	13	1	1	1	Open	0	1	1	Open
–	14	0	1	1	Open	1	1	1	Open
–	15	1	1	1	Open	0	1	1	Open


RESET
POWER UP
50 MSEC RESET EXTENDER U8
RESET
LAMP TEST
REMOTE RESET
PLUG IN RESET
FUNCTION SW RESET
FP PUSHBUTTON RESET
SET AUTO SINGLE CYCLE FF U14B RESET
AUTO SINGLE CYCLE
DISP POS + GATE TIME RESET
TIME SCALER
EXCESS GATE TIME U22B
LOAD MS
U5A
REMOTE INHIBIT ARM
ARM
PLUG IN INHIBIT ARM
ARMING INHIBIT
SAMPLE RATE
SAMPLE RATE
SAMPLE RATE Q7,8
HOLD
SAMPLE RATE ARM
U5B
PLUG IN ARM
FORCED ARM
ARMING OR GATE
FIRST CYCLE ARM
ARMING


R11
CR3
Q6
R9
Q5
R4
U6
U14
U21
U29
R7
Q4
22 $\overline{22}$
R13
R21
R23
R22
CR8
Q8
R24
C8
C5
U20
U28
Q7
15 $\overline{15}$
R6
P1B
U5
U13
U19
U27
CR4
R5
7 $\overline{7}$
CR6
CR7
U12
R17
R27
R16
U4
Q10
TP7
C4
1 $\overline{1}$
U18
U26
U11
R3
22 $\overline{22}$
U3
U10
U25
U17
R14
15 $\overline{15}$
U2
U9
TP6
Q9
U24
R26
C6
CR5
P1A
CR13
R20
CR11
R15
C7
CR1
U8
CR12
U16
U23
R25
7 $\overline{7}$
R18
CR9
CR10
C2
CR2
R2
Q3
R10
R1
U1
U7
U15
U22
Q2
R8
C1
1 $\overline{1}$
Q1
R12
C3

5345-A-37


A11 SCALER ASSEMBLY (05345-60011)(NOTE 1) SERIES 1352
EVT SCLR D0 FROM XA9A(8)
EVT SCLR C0 FROM XA9A(5)
EVT SCLR B0 FROM XA9A(6)
EVT SCLR A0 FROM XA9A(5)
EVT SCLR A1 FROM XA9A(6)
EVT SCLR A1 FROM XA9A(7)
DECADE RST FROM XA10A(17)
ECL TO TTL
EVENT SCALER
RESET
RMT FROM XA12B(19)
PROC BUSY FROM XA15B(8)
I DISP POS/GT SEL FROM A17J1(10) VIA A17J2(45)
FP GT D FROM S4BR(8)
RMT GT D FROM XA12B(10)
PI GT/DISP POS D FROM A17J1(29) VIA A17J2(58)
DRC D FROM XA13A(13)
FP GT C FROM S4BR(3)
RMT GT C FROM XA12B(9)
PI GT/DISP POS C FROM A17J1(30) VIA A17J2(56)
DRC C FROM XA13A(21)
FP GT B FROM S4BF(10)
RMT GT B FROM XA12B(5)
PI GT/DISP POS B FROM A17J1(28) VIA A17J2(60)
DRC B FROM XA13A(20)
FP GT A FROM S4AR(10)
RMT GT A FROM XA12B(4)
PI GT/DISP POS A FROM A17J1(9) VIA A17J2(47)
DRC A FROM XA13A(19)
4-16 LINE DECODER
TIME SCLR A1 FROM XA9B(21)
TIME SCLR A1 FROM XA9B(22)
+5V
+5V RET
-5.2V
-5.2V RET
-15V
TIME SCALER D0 FROM XA9B(11)
TIME SCALER C0 FROM XA9B(13)
TIME SCALER B0 FROM XA9B(12)
TIME SCALER A0 FROM XA9B(10)
EVT SCLR D TO XA13A(10)
EVT SCLR C TO XA13A(9)
EVT SCLR B TO XA13A(15)
EVT SCLR A TO XA13A(16)
SCLR OUT TO J5 (REAR PANEL)
SAMPLE RATE FROM XA12A(11), S6 SAMPLE RATE SW
DISP CLK EN FROM XA15B(9)
HOLD FROM XA12A(9), S6 SAMPLE RATE SW
RMT INH ARM FROM XA12A(15)
K DATA/PI INH ARM FROM A17J1(40) VIA A17J2(36)
PI ARM FROM A17J1(41) VIA A17J2(30)
FORCED ARM FROM XA10B(21), XA12B(21)
SAMPLE RATE
SCHMITT TRIGGER
SAMPLE RATE ARM TO XA10A(10)
ARM TO XA10B(17)
RST TO XA10B(4), XA14B(4), A17J1(38) VIA A17J2(40)
AUT SC TO XA13B(15)
SET AUT SC TO XA10B(12), XA13B(4), XA15B(5)
LOAD MS FROM XA15B(5)
ARMING
MIN GATE TIME TO XA10B(2), XA14B(14)
FUNC SW RST FROM S1AF(5) VIA XA5(9)
TESTER
RMT RST FROM XA12B(13)
PI RST FROM A17J1(34) VIA A17J2(48)
GT + DISP POS RST FROM S4,S5 VIA XA5(10)
PB RST FROM S3 RESET SW VIA XA5(14)
MEAS TIME FROM XA10B(18)
ST + STP FROM XA10B(10)
XS GT RST INH/N DATA FROM XA10B(22)
RESET
POWER UP RESET
RESET EXTENDER
LAMP TEST TO A2P1(3), XA13A(22) TO/FROM XABA(3,3)
TIME SCALER D TO XA13B(2)
TIME SCALER C TO XA10B(3), XA13B(3)
TIME SCALER B TO XA13B(1)
TIME SCALER A TO XA10B(1), XA13B(1)
EXCESS GATE TIME
EXCESS GATE TIME RESET
5345-J-8

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES

REFERENCE DESIGNATIONS

A11
C1-8
CR1-13
P1
Q1-10
R1-18,20-27
U1-29

Figure 8-14. A11 Scaler Assembly

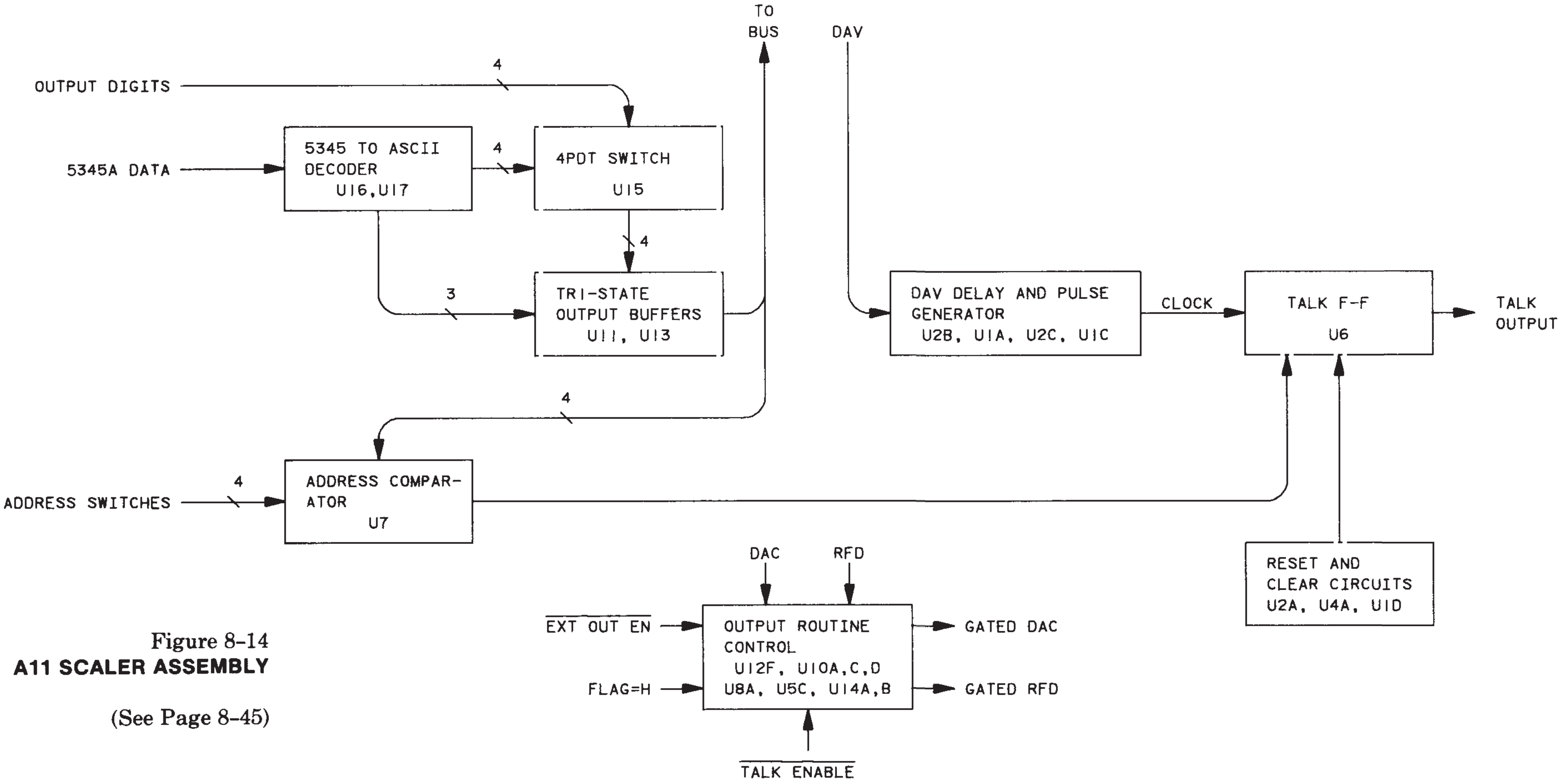
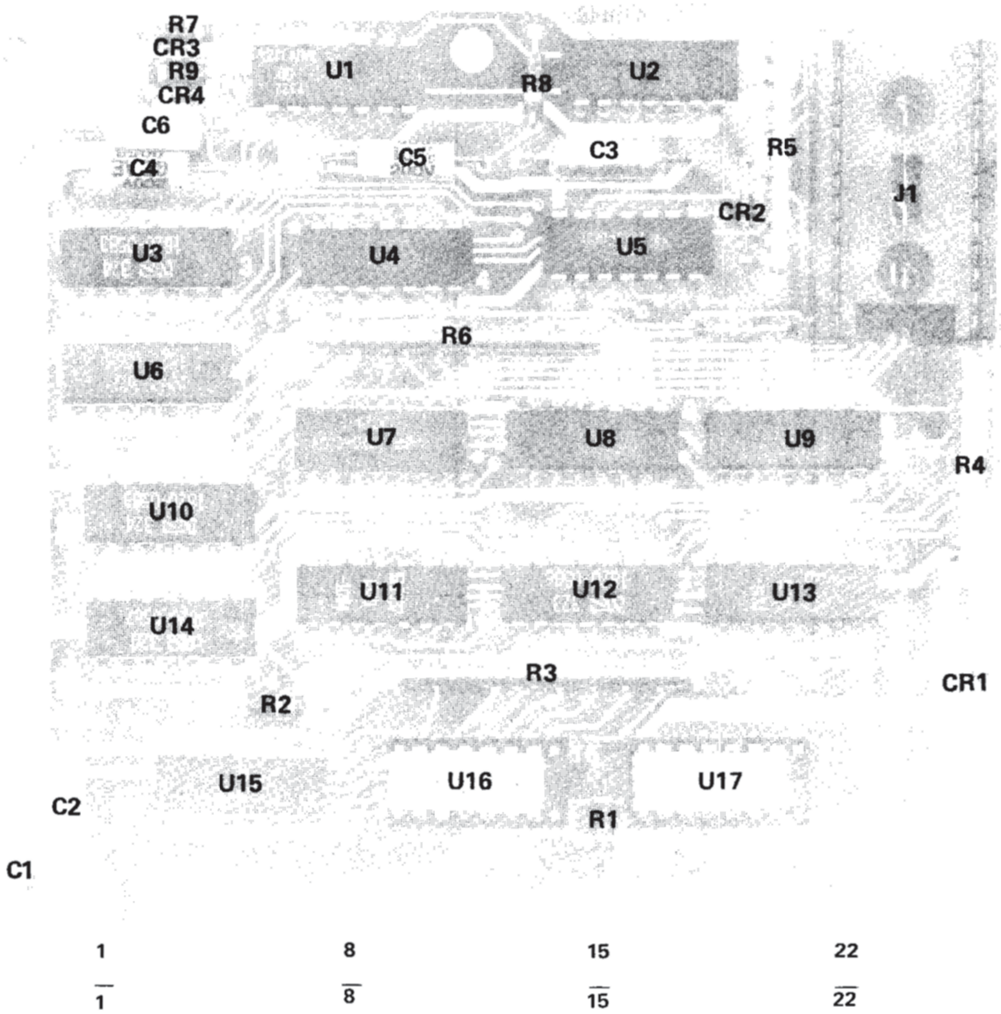
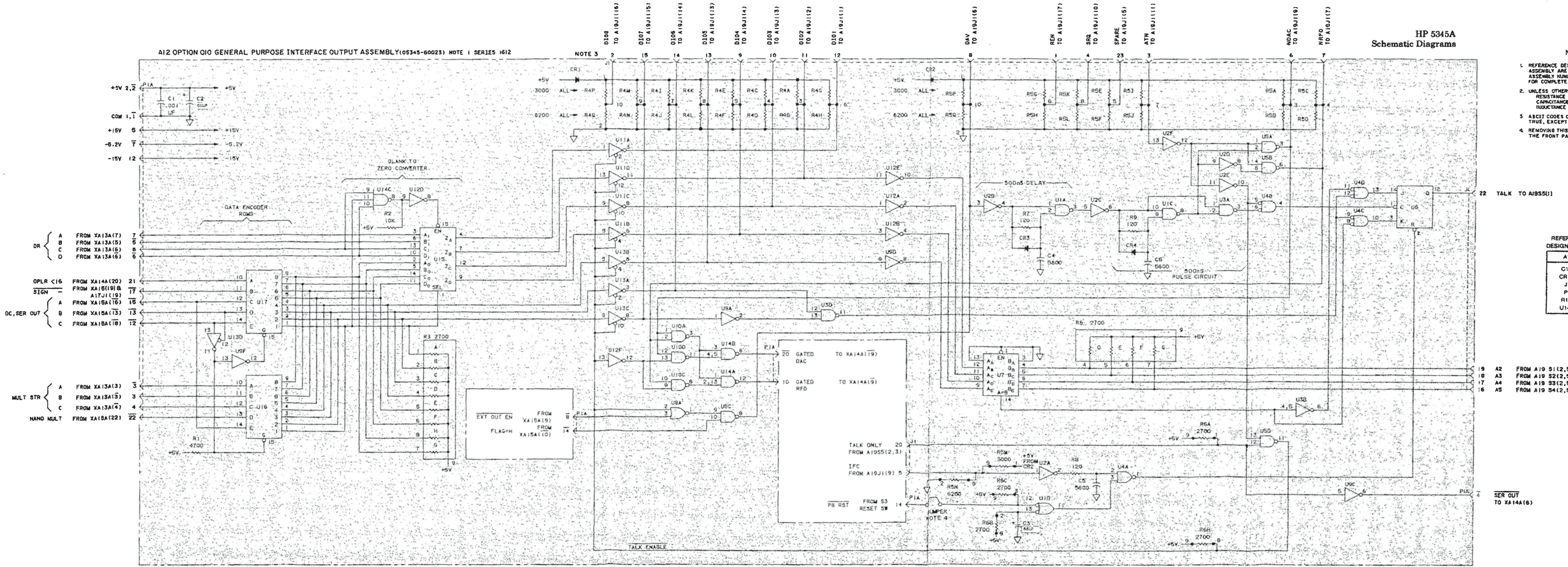

TO BUS
DAV
OUTPUT DIGITS
4
5345A DATA
5345 TO ASCII DECODER U16,U17
4
4PDT SWITCH U15
4
3
TRI-STATE OUTPUT BUFFERS U11, U13
DAV DELAY AND PULSE GENERATOR U2B, U1A, U2C, U1C
CLOCK
TALK F-F U6
TALK OUTPUT
4
ADDRESS SWITCHES
4
ADDRESS COMPARATOR U7
DAC
RFD
RESET AND CLEAR CIRCUITS U2A, U4A, U1D
$\overline{\text{EXT OUT EN}}$
OUTPUT ROUTINE CONTROL U12F, U10A,C,D U8A, U5C, U14A,B
GATED DAC
FLAG=H
GATED RFD
$\overline{\text{TALK ENABLE}}$

Figure 8-14
A11 SCALER ASSEMBLY

(See Page 8-45)


R7
CR3
R9
CR4
C6
C4
U1
R8
U2
C5
C3
R5
J1
CR2
U3
U4
U5
R6
U6
U7
U8
U9
R4
U10
U11
U12
U13
U14
R3
CR1
R2
U15
U16
U17
C2
R1
C1
1
8
15
22
$\overline{1}$
$\overline{8}$
$\overline{15}$
$\overline{22}$



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES
3. ASCII CODES ON J1 ARE NEGATIVE TRUE, EXCEPT RFD AND DAC.
4. REMOVING THIS JUMPER DISCONNECTS THE FRONT PANEL RESET SWITCH.

REFERENCE DESIGNATIONS

A12
C1-6
CR1-4
J1
P1
R1-9
U1-17

Figure 8-15. A12 Option 010 Output Interface Assembly

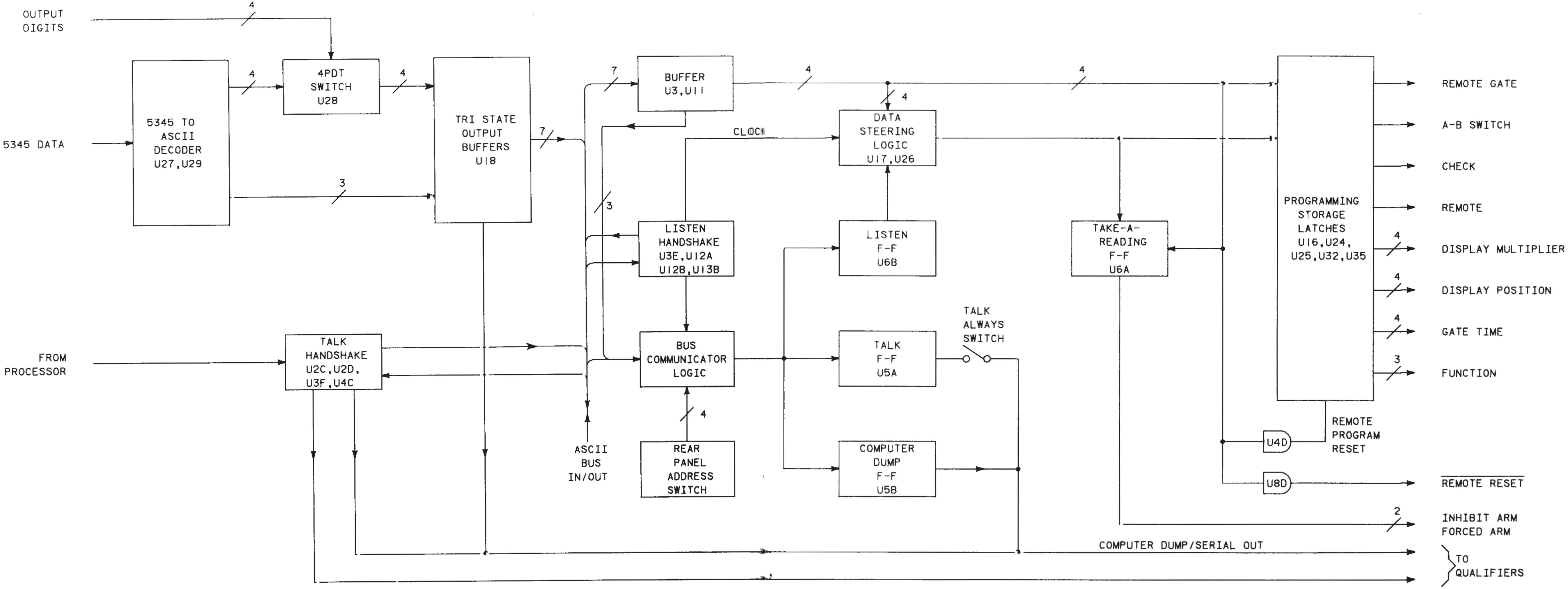
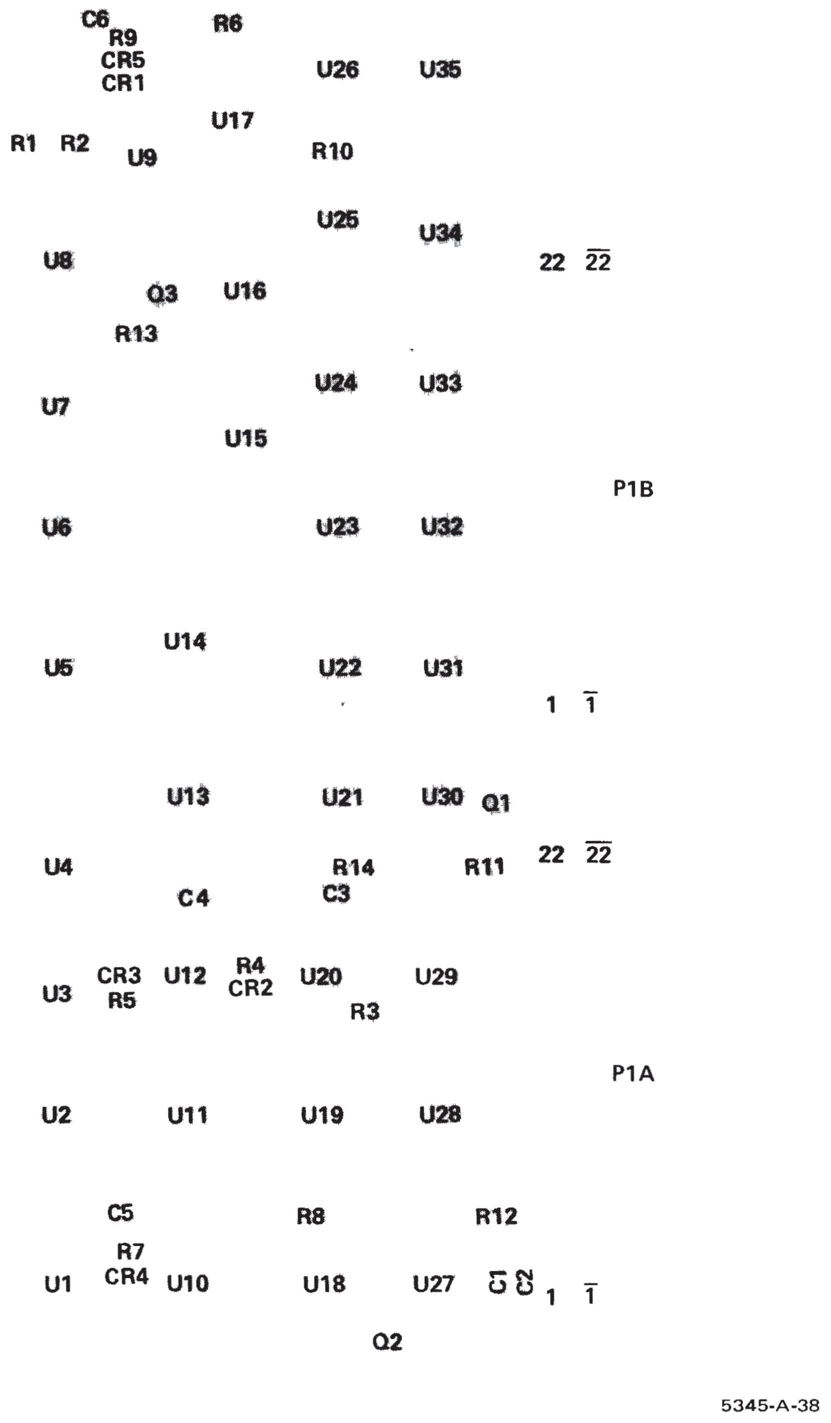
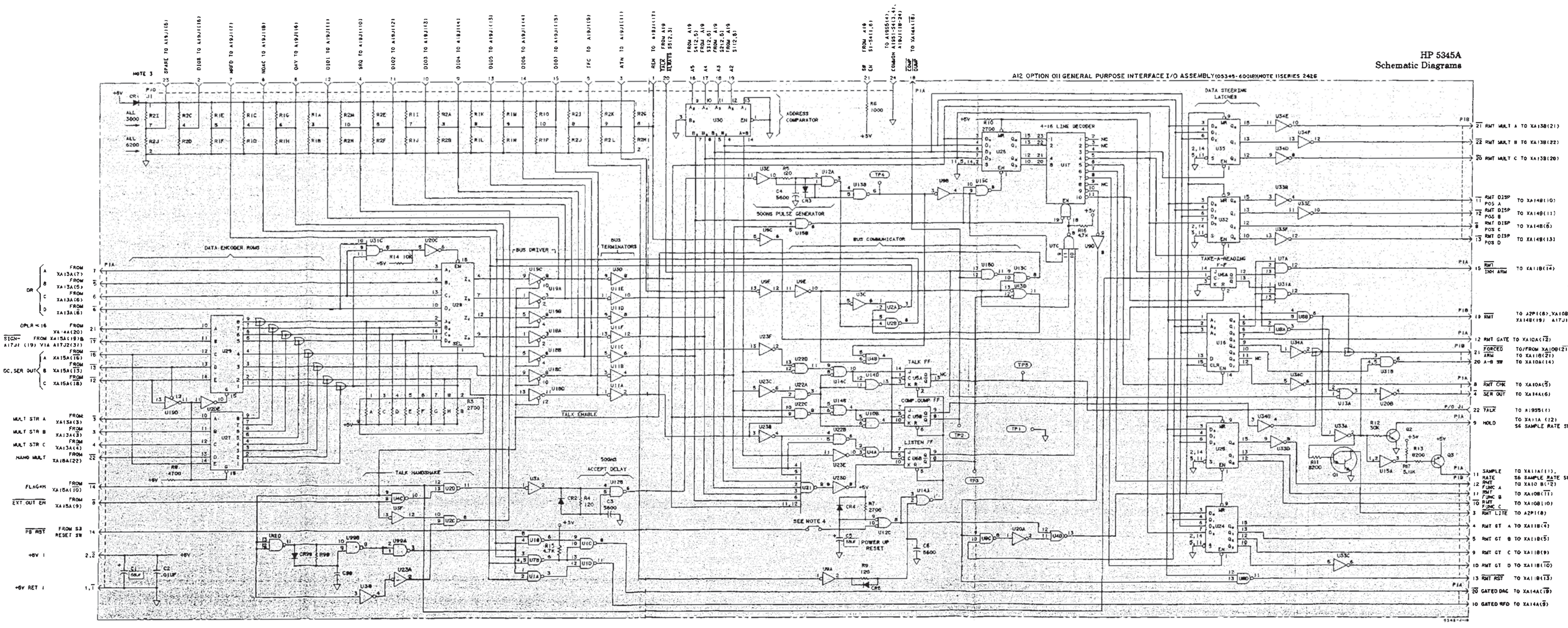


Figure 8-15

A12 OPTION 010 GENERAL PURPOSE INTERFACE OUTPUT ASSEMBLY

(See Page 8-47)


C6
R9
R6
CR5
CR1
U26
U35
U17
R1
R2
U9
R10
U25
U34
U8
22
22̄
Q3
U16
R13
U24
U33
U7
U15
P1B
U6
U23
U32
U14
U5
U22
U31
1
1̄
U13
U21
U30
Q1
U4
R14
R11
22
22̄
C4
C3
R4
CR3
U12
CR2
U20
U29
U3
R5
R3
P1A
U2
U11
U19
U28
C5
R8
R12
R7
CR4
U1
U10
U18
U27
C1
C2
1
1̄
Q2
5345-A-38



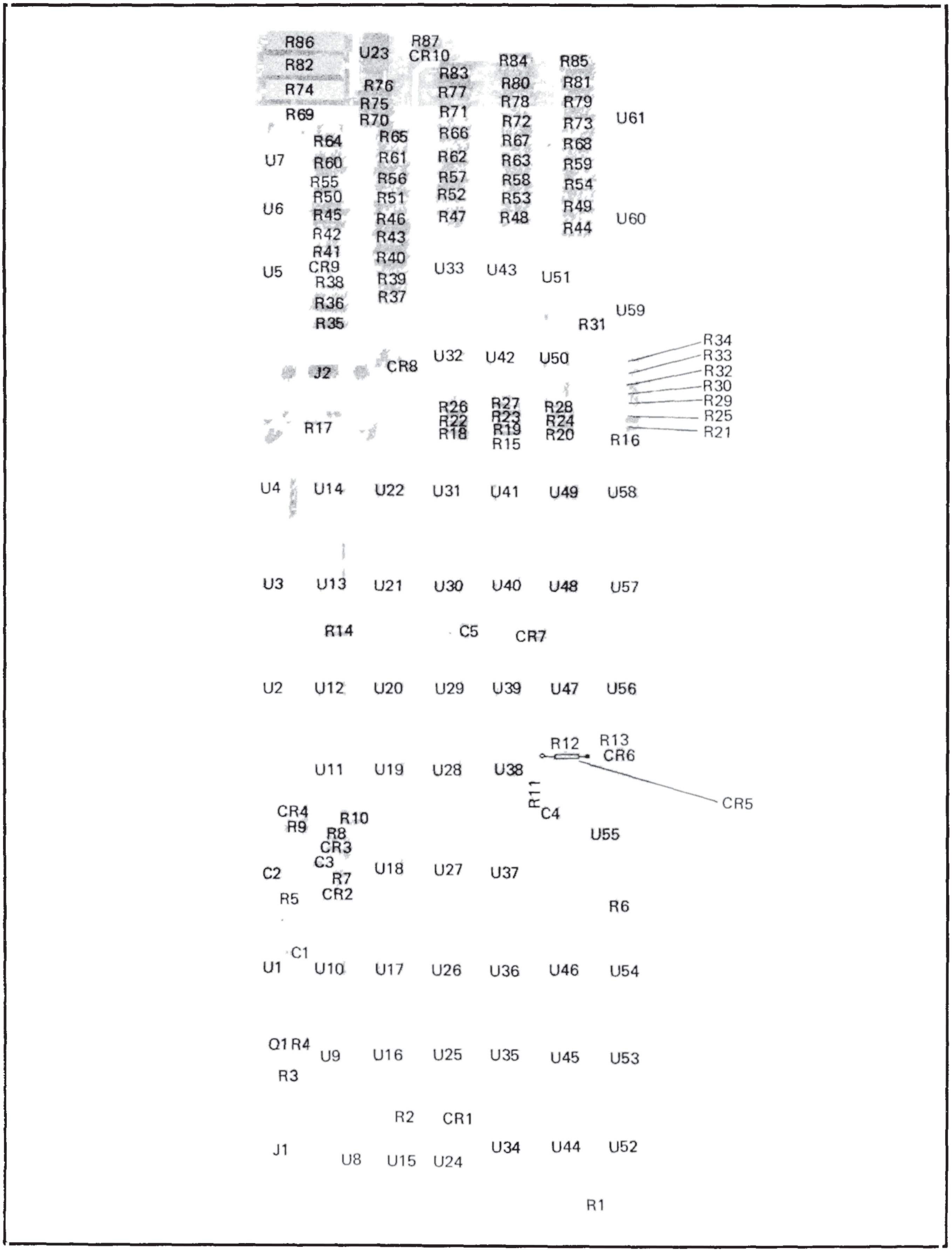
NOTES

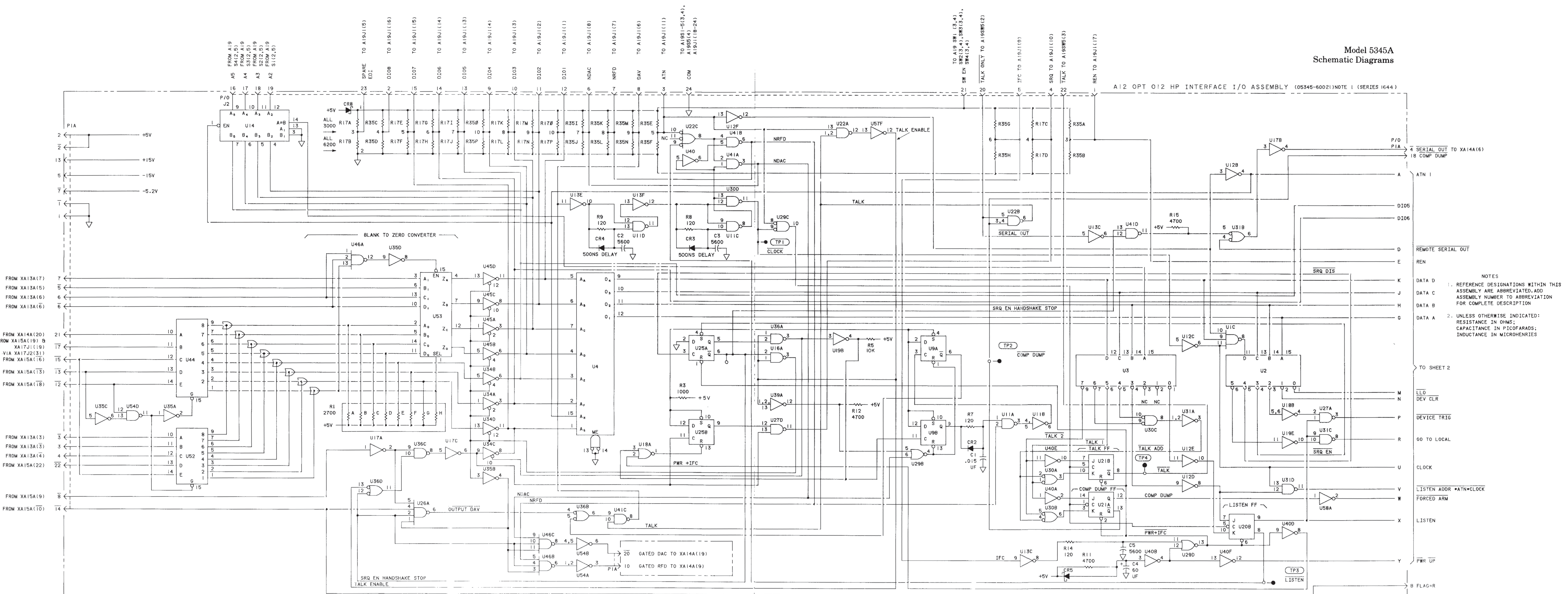
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS:
3. ASCII CODES ON J1 ARE NEGATIVE TRUE, EXCEPT RFD AND DAC
4. REMOVING THIS JUMPER DISCONNECTS THE FRONT PANEL RESET SWITCH.

REFERENCE DESIGNATIONS

A12
C1-6
CR1-5
J1
P1
Q1-3
R1-14
U1-35

Figure 8-16. A12 Option 011 I/O Interface Assembly


R86
R82
R74
R69
U23
R87
CR10
R76
R75
R70
R83
R77
R71
R84
R80
R78
R72
R85
R81
R79
R73
U61
R64
R65
R66
R67
R68
U7
R60
R61
R62
R63
R59
R55
R56
R57
R58
R54
R50
R51
R52
R53
R49
U6
R45
R46
R47
R48
R44
U60
R42
R43
R41
R40
U5
CR9
R38
R39
U33
U43
U51
R37
R36
R35
R31
U59
R34
R33
R32
R30
R29
R25
R21
U32
U42
U50
J2
CR8
R26
R22
R18
R27
R23
R19
R15
R28
R24
R20
R17
R16
U4
U14
U22
U31
U41
U49
U58
U3
U13
U21
U30
U40
U48
U57
R14
C5
CR7
U2
U12
U20
U29
U39
U47
U56
R12
R13
CR6
U11
U19
U28
U38
R11
C4
CR5
CR4
R9
R10
R8
CR3
C3
U55
C2
R7
U18
U27
U37
R5
CR2
R6
C1
U1
U10
U17
U26
U36
U46
U54
Q1
R4
U9
U16
U25
U35
U45
U53
R3
R2
CR1
J1
U8
U15
U24
U34
U44
U52
R1

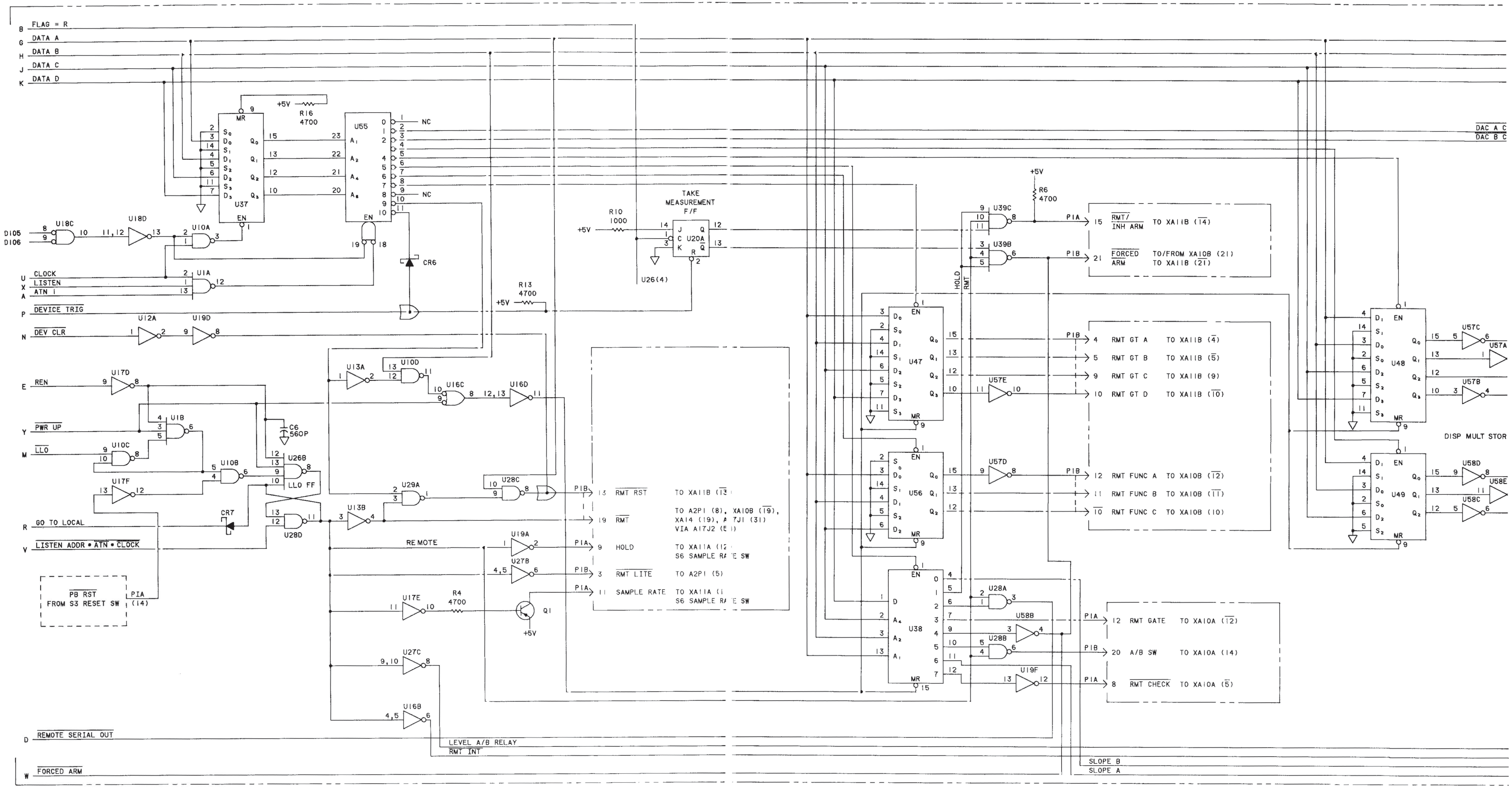


NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICOFARADS; INDUCTANCE IN MICROHENRIES

Figure 8-16A. Option 012 HP Interface I/O Assembly
(Sheet 1 of 2)

P/O OPT 12 HP INTERFACE I/O ASSEMBLY (05345-60021)NOTE 1 (SERIES



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN FARADS;
   INDUCTANCE IN HENRIES
3. * SELECT RESISTOR R75 POT A,B,C & D TO BE WITHIN RANGE.
4. RELAY ACTIVE IN THE NON-REMOTE MODE.

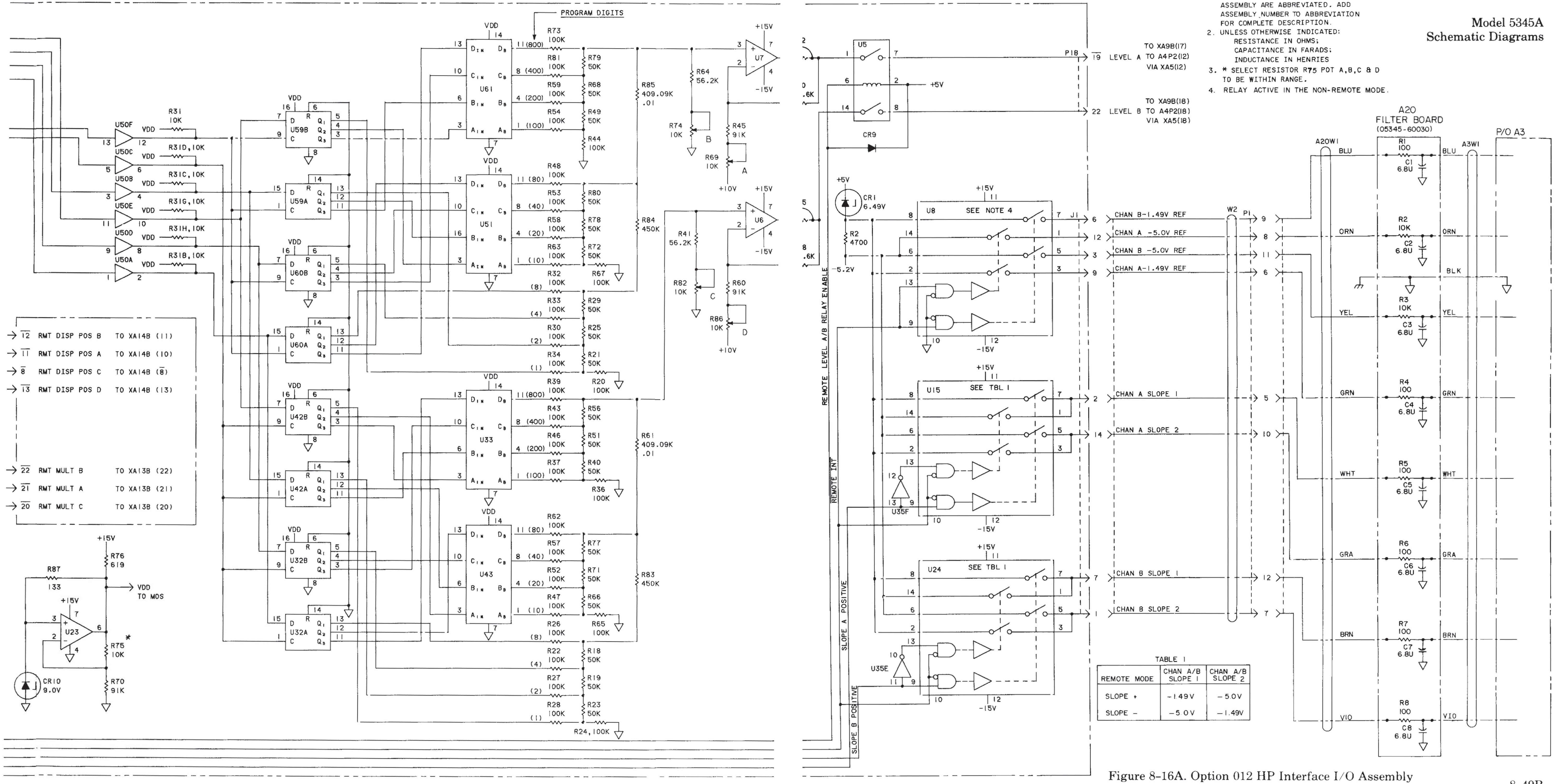


TABLE 1

REMOTE MODE	CHAN A/B SLOPE 1	CHAN A/B SLOPE 2
SLOPE +	-1.49V	-5.0V
SLOPE -	-5.0V	-1.49V

Figure 8-16A. Option 012 HP Interface I/O Assembly (Sheet 2 of 2)

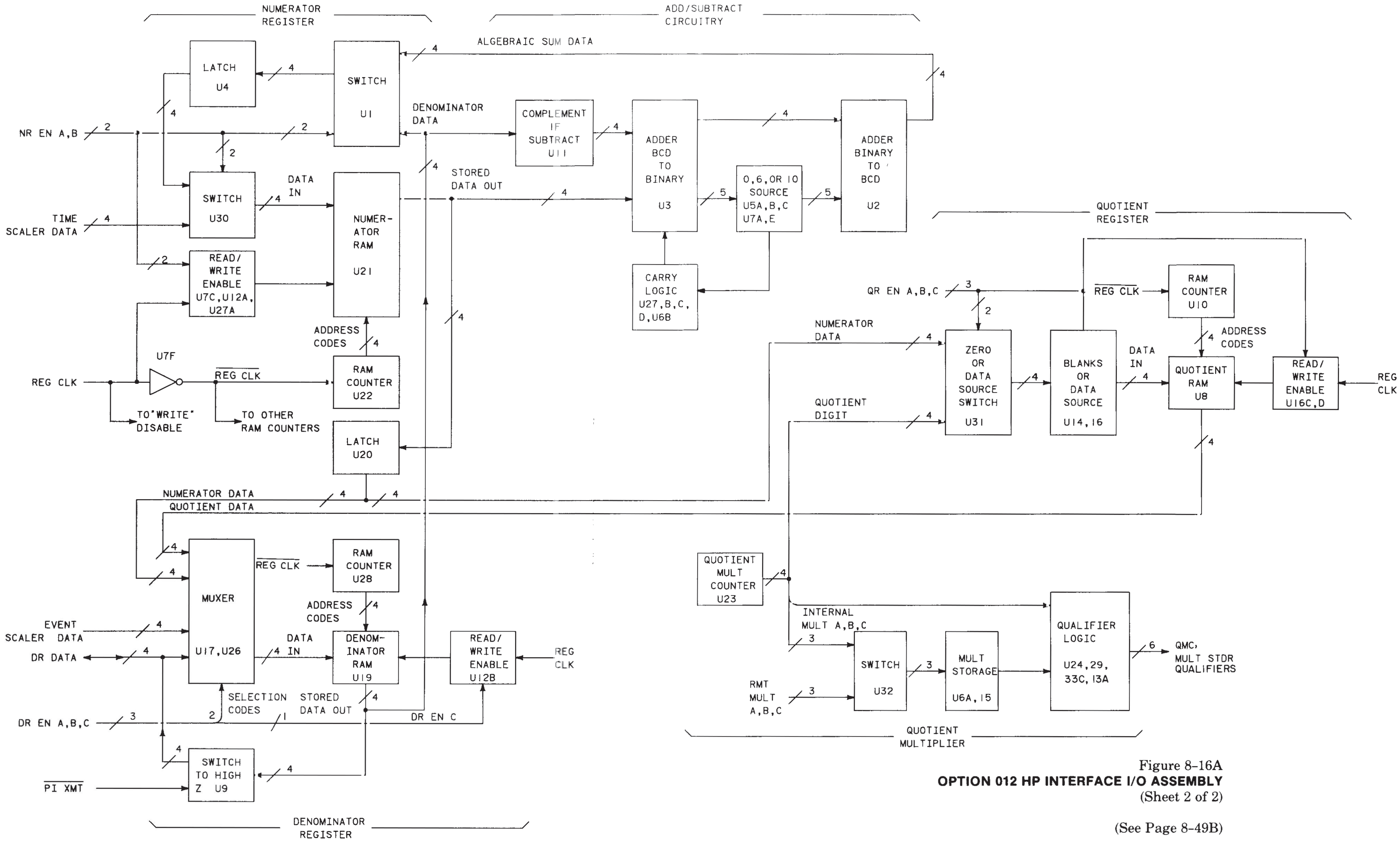
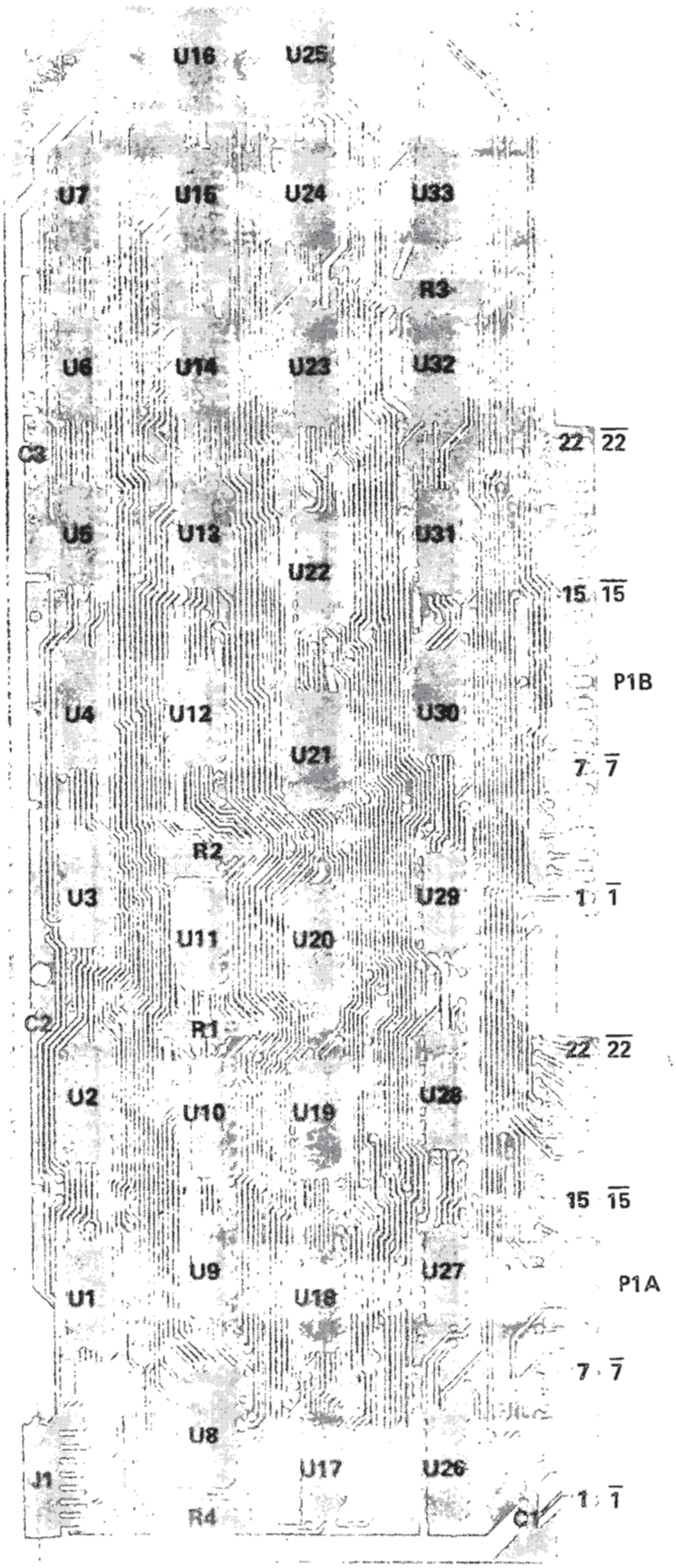
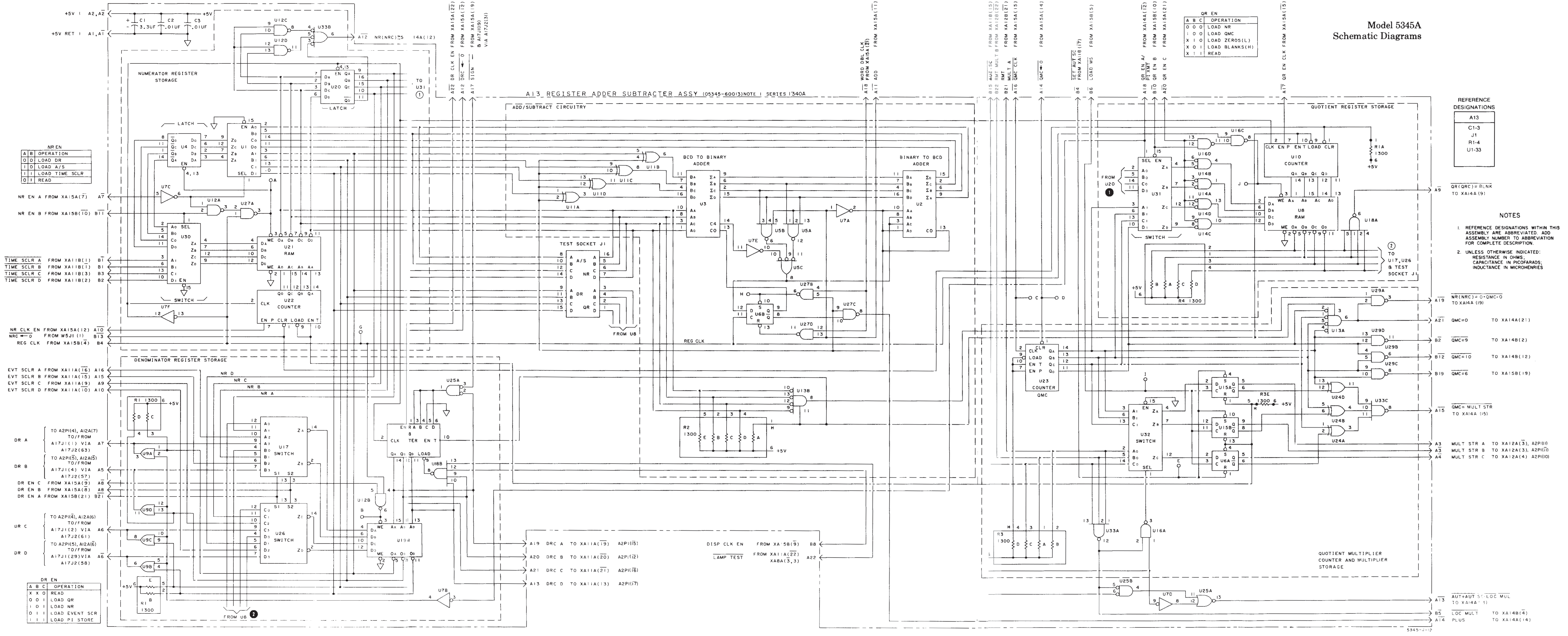


Figure 8-16A
OPTION 012 HP INTERFACE I/O ASSEMBLY
(Sheet 2 of 2)

(See Page 8-49B)


U16
U25
U7
U15
U24
U33
R3
U6
U14
U23
U32
22 $\overline{22}$
C3
U5
U13
U31
U22
15 $\overline{15}$
P1B
U4
U12
U30
U21
7 $\overline{7}$
R2
U3
U29
1 $\overline{1}$
U11
U20
C2
R1
22 $\overline{22}$
U2
U10
U19
U28
15 $\overline{15}$
U9
U27
P1A
U1
U18
7 $\overline{7}$
U8
U17
U26
J1
1 $\overline{1}$
R4
C1


A13 REGISTER ADDER SUBTRACTER ASSY (05345-60013) NOTE 1 SERIES 1340A
NUMERATOR REGISTER STORAGE
DENOMINATOR REGISTER STORAGE
ADD/SUBTRACT CIRCUITRY
QUOTIENT REGISTER STORAGE
QUOTIENT MULTIPLIER COUNTER AND MULTIPLIER STORAGE
BCD TO BINARY ADDER
BINARY TO BCD ADDER
TEST SOCKET J1
LATCH
SWITCH
U21 RAM
U22 COUNTER
U8 RAM
U10 COUNTER
U23 COUNTER
QMC
U17 SWITCH
U26 SWITCH
U31
U32 SWITCH
+5V I A2,A2
+5V RET I A1,A1
C1 3.3UF
C2 .01UF
C3 .01UF
NR EN A FROM XA15A(7) A7
NR EN B FROM XA15B(10) B11
TIME SCLR A FROM XA11B(1) B1
TIME SCLR B FROM XA11B(1) B1
TIME SCLR C FROM XA11B(3) B3
TIME SCLR D FROM XA11B(2) B2
NR CLK EN FROM XA15A(12) A10
NRC ← 0 FROM W5J1 (1) B13
REG CLK FROM XA15B(4) B4
EVT SCLR A FROM XA11A(16) A16
EVT SCLR B FROM XA11A(15) A15
EVT SCLR C FROM XA11A(9) A9
EVT SCLR D FROM XA11A(10) A10
DR A
DR B
DR C
DR D
TO A2P1(4), A12A(7) TO/FROM A17J1(1) VIA A17J2(63) A7
TO A2P1(5), A12A(5) TO/FROM A17J1(4) VIA A17J2(57) A5
DR EN C FROM XA15A(9) A8
DR EN B FROM XA15A(8) A8
DR EN A FROM XA15B(21) B21
TO A2P1(4), A12A(6) TO/FROM A17J1(2) VIA A17J2(61) A6
TO A2P1(5), A12A(6) TO/FROM A17J1(29) VIA A17J2(58) A6
FROM U8
A19 DRC A TO XA11A(19) A2P1(15)
A20 DRC B TO XA11A(20) A2P1(12)
A21 DRC C TO XA11A(21) A2P1(16)
A13 DRC D TO XA11A(13) A2P1(17)
DISP CLK EN FROM XA15B(9) B8
LAMP TEST FROM XA11A(22) XA8A(3,3) A22
A12 NR(NRC)=5 14A(12)
TO U31
A22 DR CLK EN FROM XA15A(22)
B12 DRC 0 ← FROM XA15A(12)
A17 SIGN FROM XA15A(19) & A17J1(19) VIA A17J2(31)
A18 WORD DBL CLK FROM XA15A(21)
A11 ADD FROM XA15A(11)
FROM U20
TO U17, U26 & TEST SOCKET J1
QR(QRC)=BLNK TO XA14A(9) A9
NR(NRC)=0·QMC=0 TO XA14A(19) A19
QMC=0 TO XA14A(21) A21
QMC=9 TO XA14B(2) B2
QMC=10 TO XA14B(12) B12
QMC=6 TO XA15B(19) B19
QMC= MULT STR TO XA14A(15) A15
MULT STR A TO XA12A(3), A2P1(11) A3
MULT STR B TO XA12A(3), A2P1(11) A3
MULT STR C TO XA12A(4) A2P1(10) A4
AUT+AUT SC LOC MUL TO XA14A(5) A13
LOC MULT TO XA14B(4) B5
PLUS TO XA14A(14) A14
5345-J-12

QR EN

A	B	C	OPERATION
0	0	0	LOAD NR
1	0	0	LOAD QMC
X	1	0	LOAD ZEROS(L)
X	0	1	LOAD BLANKS(H)
X	1	1	READ

NR EN

A	B	OPERATION
0	0	LOAD DR
1	0	LOAD A/S
1	1	LOAD TIME SCLR
0	1	READ

DR EN

A	B	C	OPERATION
X	X	0	READ
0	0	1	LOAD QR
1	0	1	LOAD NR
0	1	1	LOAD EVENT SCR
1	1	1	LOAD PI STORE

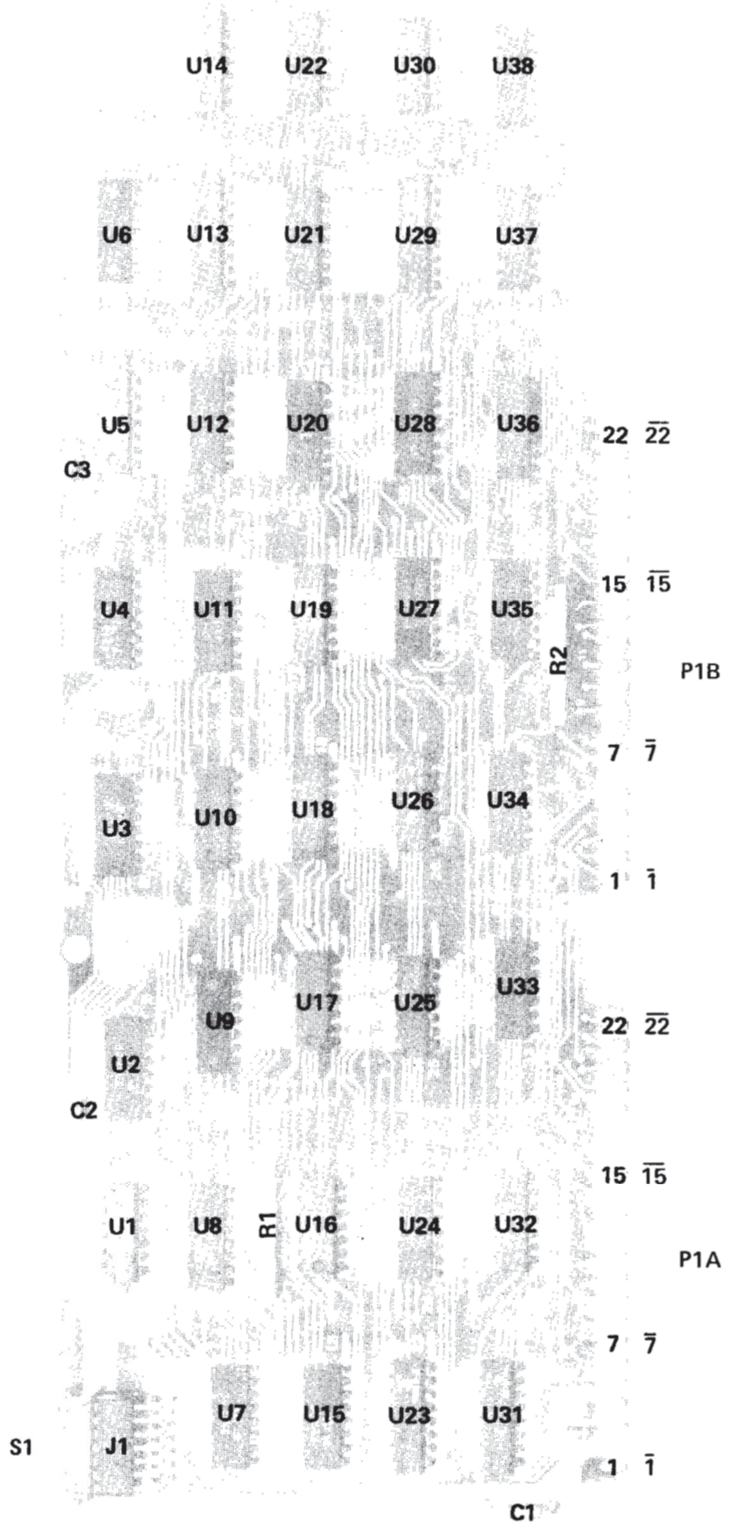
REFERENCE DESIGNATIONS

A13
C1-3 J1 R1-4 U1-33

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES

Figure 8-17. A13 Adder/Subtracter Assembly



5345-A-40

Part of Figure 8-18. A14 Qualifier Assembly

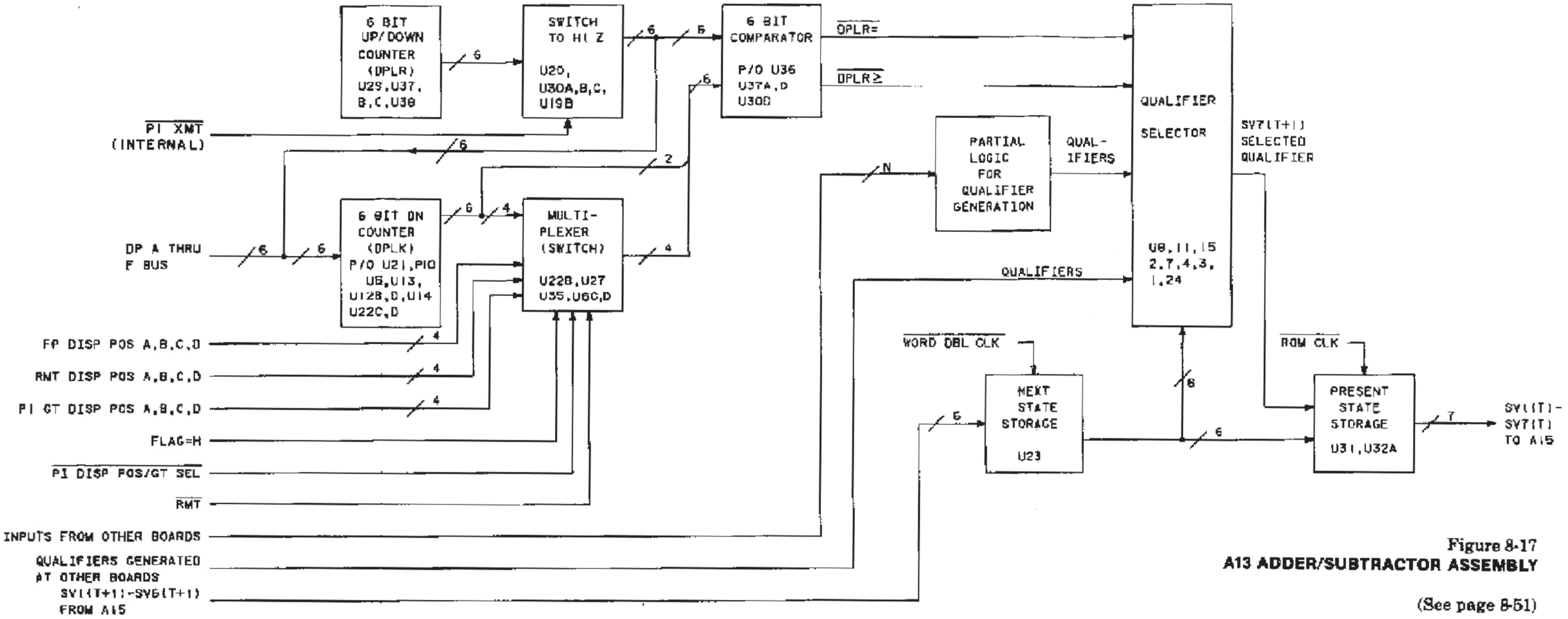

6 BIT UP/DOWN COUNTER (DPLR) U25,U37, B,C,U38
SWITCH TO HI Z U20, U30A,B,C, U19B
6 BIT COMPARATOR P/O U36 U37A,D U30D
QUALIFIER SELECTOR U8,11,15 2,7,4,3, 1,24
PARTIAL LOGIC FOR QUALIFIER GENERATION
6 BIT DN COUNTER (DPLK) P/O U21,P10 U6,U13, U12B,D,U14 U22C,D
MULTI-PLEXER (SWITCH) U22B,U27 U35,U6C,D
NEXT STATE STORAGE U23
PRESENT STATE STORAGE U31,U32A
DPLR=
DPLR≥
QUAL-IFIERS
QUALIFIERS
SV7(T+1) SELECTED QUALIFIER
WORD DBL CLK
ROM CLK
SV1(T)-SV7(T) TO A15
PI XMT (INTERNAL)
DP A THRU F BUS
FP DISP POS A,B,C,D
RMT DISP POS A,B,C,D
PI GT DISP POS A,B,C,D
FLAG=H
PI DISP POS/GT SEL
RMT
INPUTS FROM OTHER BOARDS
QUALIFIERS GENERATED AT OTHER BOARDS
SV1(T+1)-SV6(T+1) FROM A15
6
6
6
6
6
6
6
2
6
6
4
4
4
4
4
N
6
6
6
7

Figure 8-17
A13 ADDER/SUBTRACTOR ASSEMBLY

(See page 8-51)

NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES

REFERENCE DESIGNATIONS
A14
C1-3 P1 R1,2 S1 U1-38

SERVICE NOTES

The A14 assembly has seven servicing switches (S1-1-7), some of which are related to the plug-in. These switches perform the following actions when selected.

S1-1 (Closest to the display) displays time scaler measurement contents.

S1-2 Displays the complete arithmetic result in Giga or Nano units.

S1-4 Has the effect of nullifying the $\overline{\text{N DATA}}$ request from the plug-in. Useful for observing S1-3 arithmetic result without an N.

S1-5 Has the effect of nullifying the $\overline{\text{K DATA}}$ request from the plug-in. Useful for observing S1-3 arithmetic result without a K.

S1-6 Activites $\overline{\text{PI DATA}}$ without regard to plug-in status. Useful for a special servicing routine where a plug-in could display its internal data.

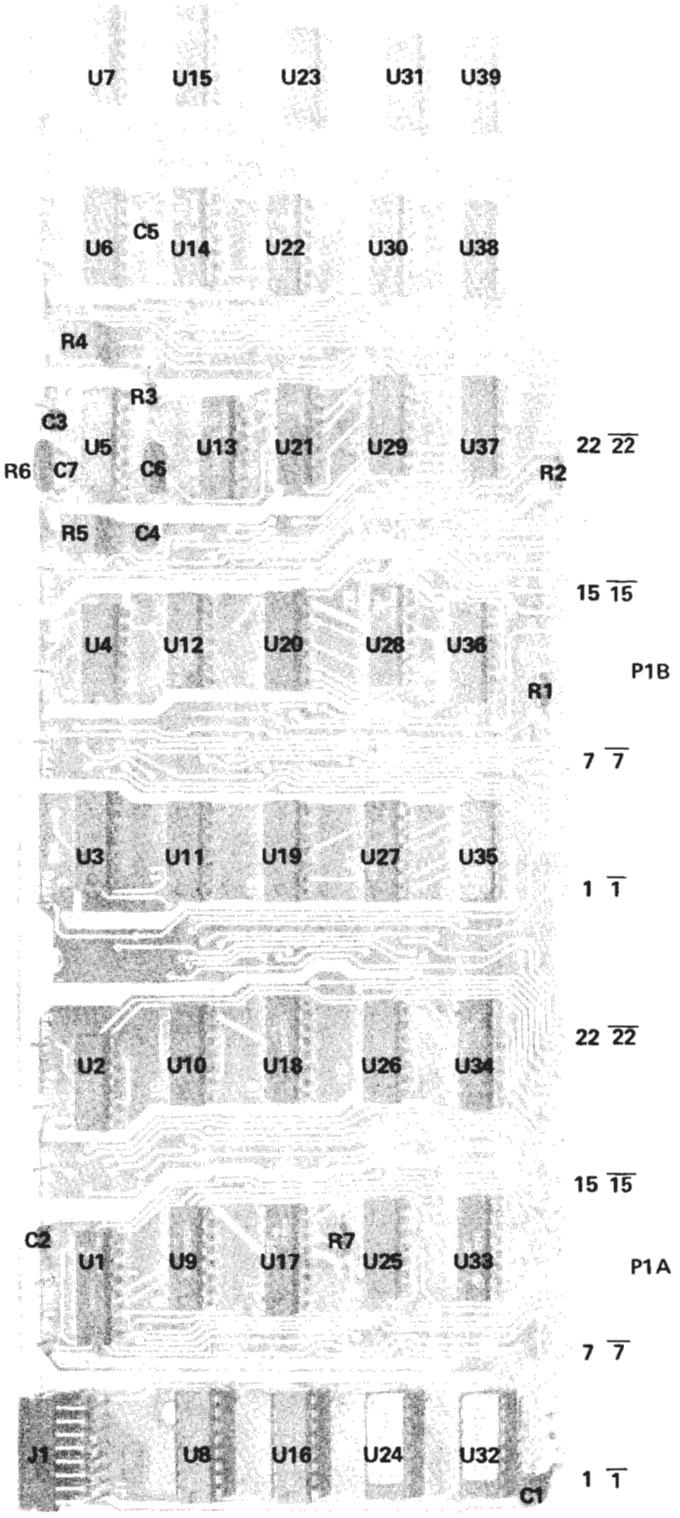
S1-7 Forces an INITIALIZE PROCESSOR qualifier. Would prevent a display cycle during a START, STOP, or PI DATA routine. Useful for viewing the processing cycle's behavior with an oscilloscope. The display cycle lasts a minimum of 50 msec making the cycle time of the processing cycle once every ~53 msec. The cycle time with S1-7 is about once every 3 msec.

A14 QUALIFIER ASSEMBLY (05345-60044) SERIES 1708
DECIMAL POINT LOCATOR FOR RESULT-6 BIT UP/DN COUNTER (DPLR)
DECIMAL POINT LOCATOR FOR PI DATA-6 BIT DOWN COUNTER (DPLK)
DECIMAL POINT BUS CONTROL
6 BIT COMPARATOR
QUALIFIER SELECTOR
ADDRESS BIT 0&1
FLAG=H FROM XA15A(10)
DPLK ← DPLK-PI FROM XA15B(17)
FP DISP POS
RMT DISP POS
PI DISP POS/GT SEL
DISP CLK TO XA15B(6) A2P1(3)
PI GT/DISP POS
WORD DBL CLK
RST
MIN GATE TIME
ROM CLK
STATE VARIA STORAGE

LINE	TO A2P1	TO XA15B	TO/FROM A17J1	VIA A17J2
DP F	—	—	6	53
DP E	—	13	17	33
DP D	17	15	20	29
DP C	16	18	8	49
DP B	12	17	7	51
DP A	15	14	43	27

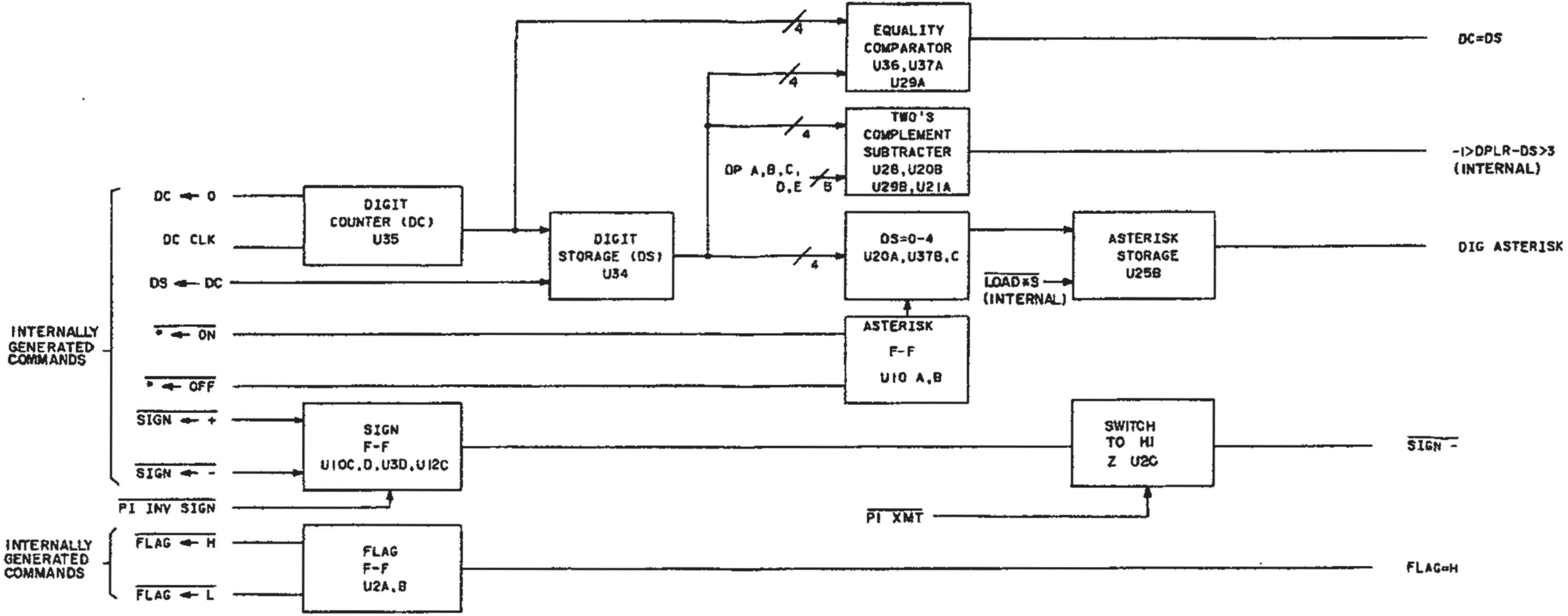
FLAG=H	$\overline{\text{PI DISP}}$ $\overline{\text{POS/GT SEL}}$	$\overline{\text{RMT}}$	DATA TO COMPARATOR(U28)
L	X	X	DPLK (6 BITS)
H	L	X	PI DISP POS (4 BITS)
H	H	L	RMT DISP POS (4 BITS)
H	H	H	FP DISP POS(4 BITS)

Figure 8-18. A14 Qualifier Assembly



5345-A-41

Part of Figure 8-19. A15 ROM Assembly


INTERNALLY GENERATED COMMANDS
DC ← 0
DC CLK
DS ← DC
* ← ON
* ← OFF
SIGN ← +
SIGN ← -
PI INV SIGN
INTERNALLY GENERATED COMMANDS
FLAG ← H
FLAG ← L
DIGIT COUNTER (DC) U35
DIGIT STORAGE (DS) U34
SIGN F-F U10C,D,U3D,U12C
FLAG F-F U2A,B
4
4
4
4
DP A,B,C, D,E
5
EQUALITY COMPARATOR U36,U37A U29A
TWO'S COMPLEMENT SUBTRACTER U28,U20B U29B,U21A
DS=0-4 U20A,U37B,C
ASTERISK F-F U10 A,B
LOAD*S (INTERNAL)
ASTERISK STORAGE U25B
SWITCH TO HI Z U2C
PI XMT
DC=DS
-1>DPLR-DS>3 (INTERNAL)
DIG ASTERISK
SIGN -
FLAG=H

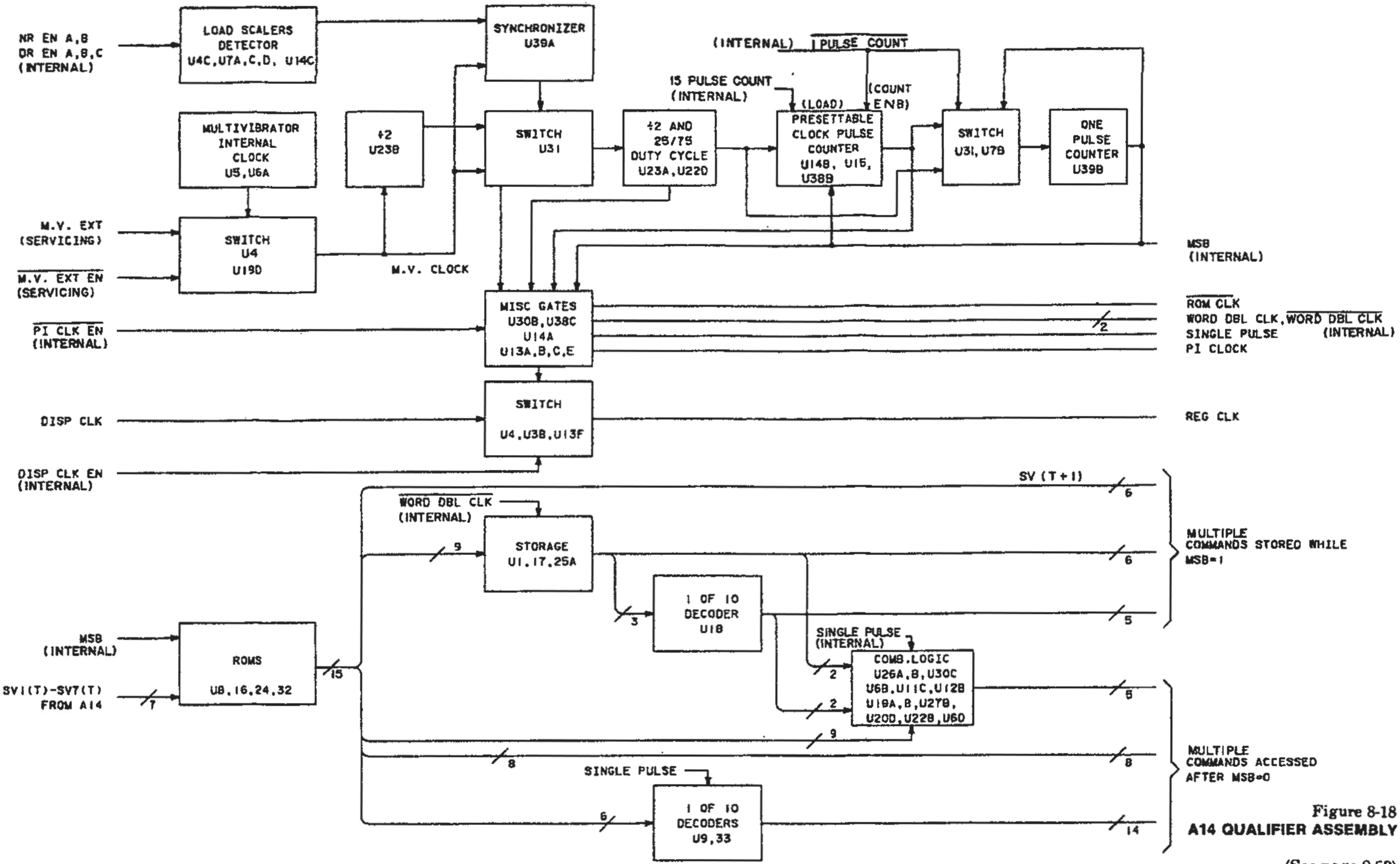


Figure 8-18
A14 QUALIFIER ASSEMBLY

(See page 8-53)

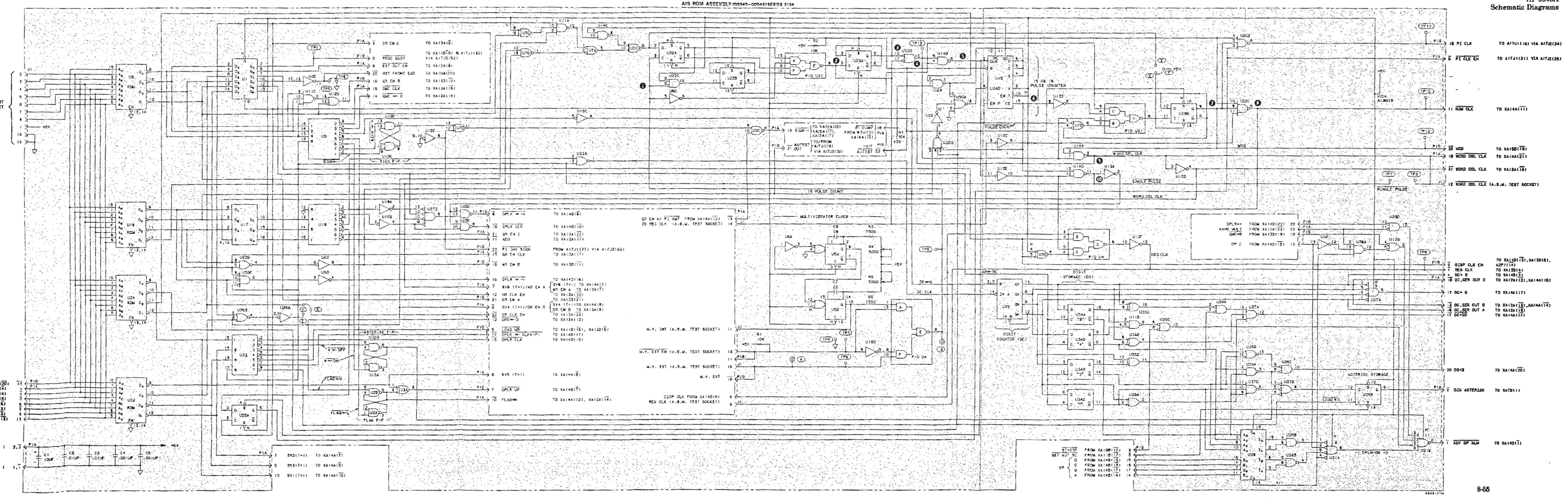


Figure 8-19. A15 ROM Assembly

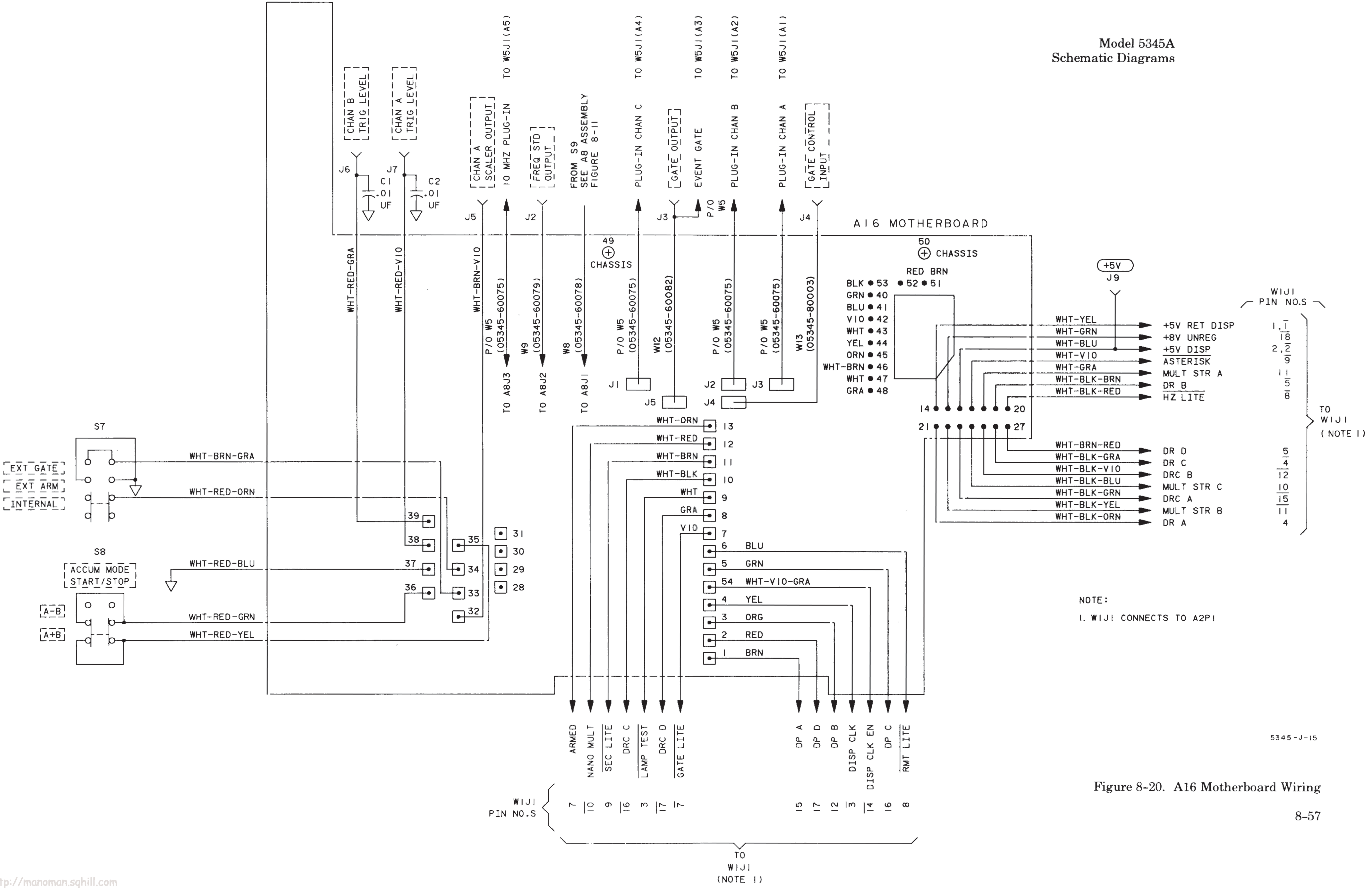
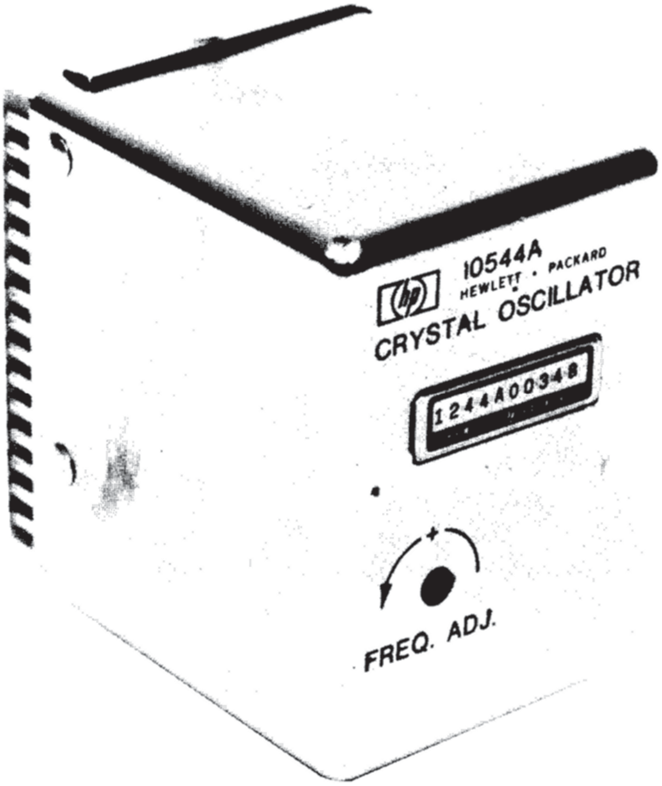


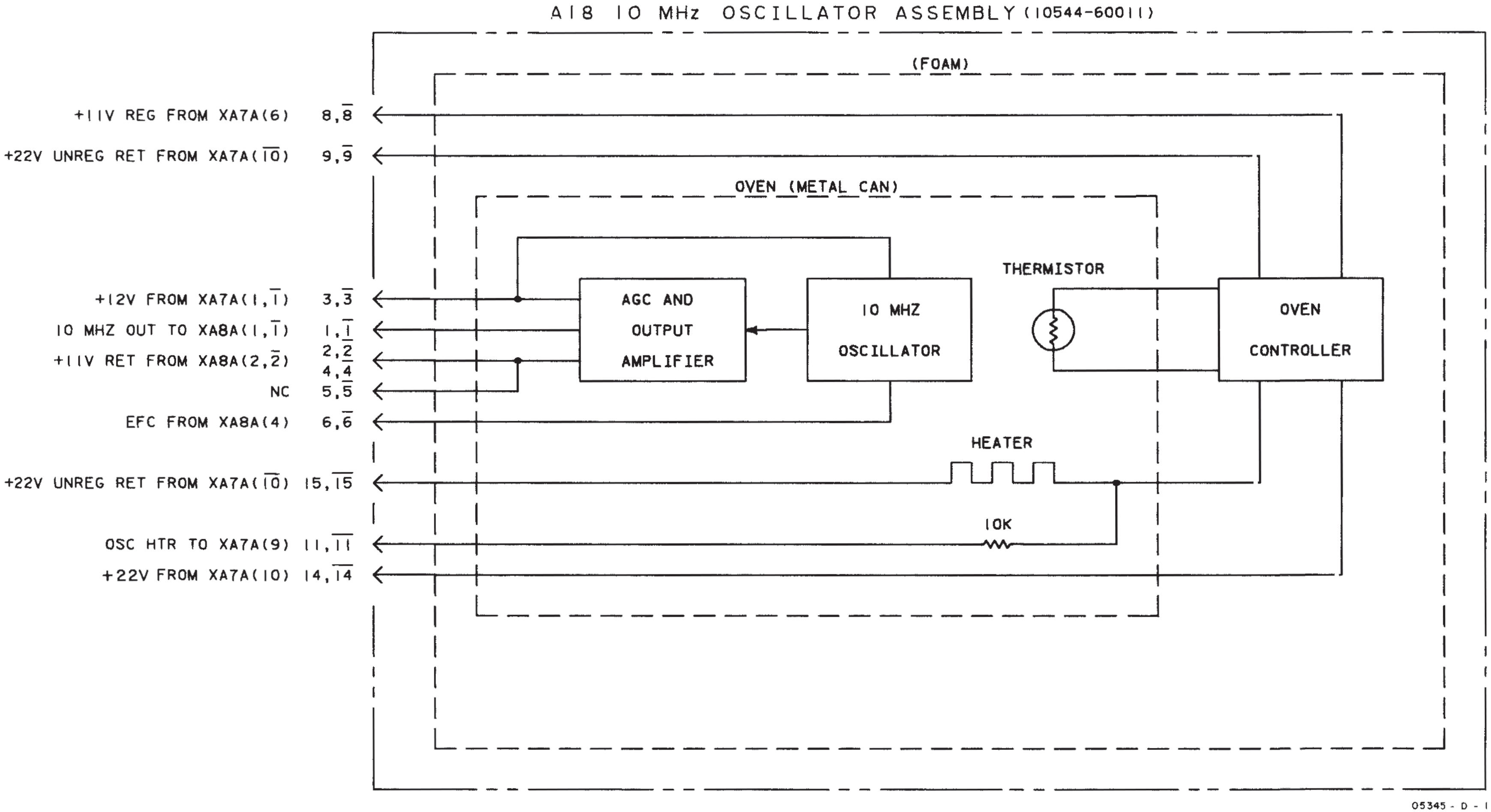
Figure 8-20. A16 Motherboard Wiring



5345-A-51

NOTE

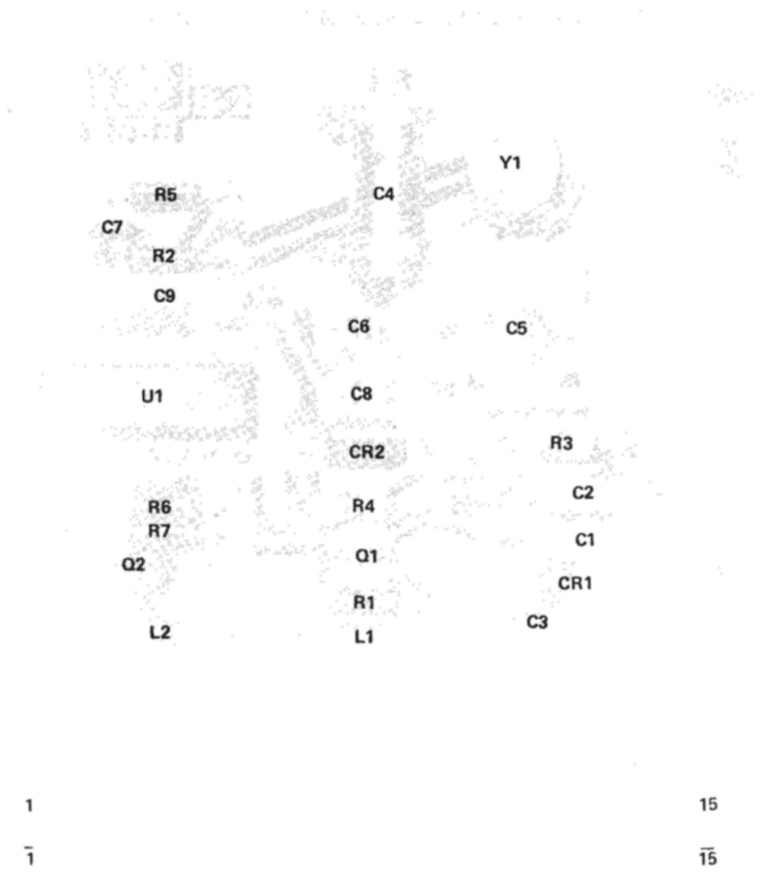
This assembly is held in place by two screws located on the bottom of A16 Motherboard.


A18 10 MHz OSCILLATOR ASSEMBLY (10544-60011)
(FOAM)
OVEN (METAL CAN)
+11V REG FROM XA7A(6) 8,$\overline{8}$
+22V UNREG RET FROM XA7A($\overline{10}$) 9,$\overline{9}$
+12V FROM XA7A(1,$\overline{1}$) 3,$\overline{3}$
10 MHZ OUT TO XA8A(1,$\overline{1}$) 1,$\overline{1}$
+11V RET FROM XA8A(2,$\overline{2}$) 2,$\overline{2}$
4,$\overline{4}$
NC 5,$\overline{5}$
EFC FROM XA8A(4) 6,$\overline{6}$
+22V UNREG RET FROM XA7A($\overline{10}$) 15,$\overline{15}$
OSC HTR TO XA7A(9) 11,$\overline{11}$
+22V FROM XA7A(10) 14,$\overline{14}$
AGC AND OUTPUT AMPLIFIER
10 MHZ OSCILLATOR
THERMISTOR
OVEN CONTROLLER
HEATER
10K
05345 - D - 1

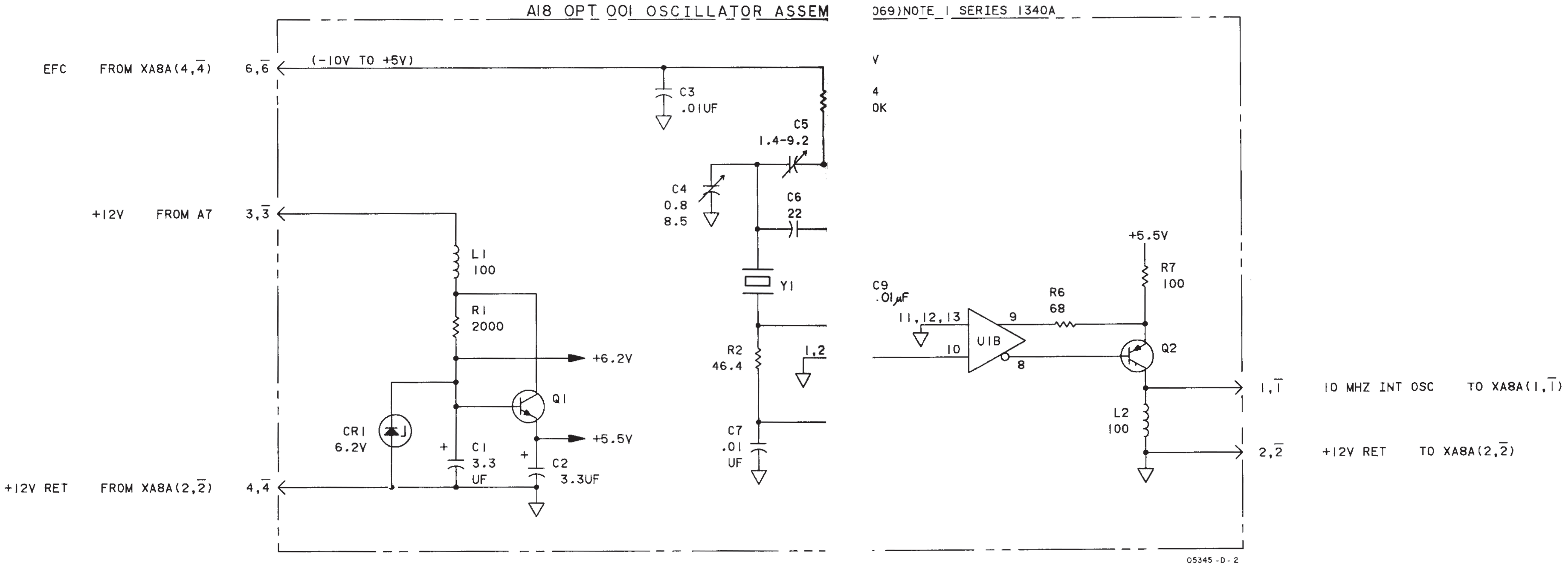
NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES

Figure 8-21. A18 10 MHz Oscillator (Oven) Assembly


Y1
R5
C4
C7
R2
C9
C6
C5
U1
C8
CR2
R3
R6
R4
C2
R7
C1
Q2
Q1
CR1
R1
C3
L2
L1
1
15
$\bar{1}$
$\overline{15}$

5345-A-42



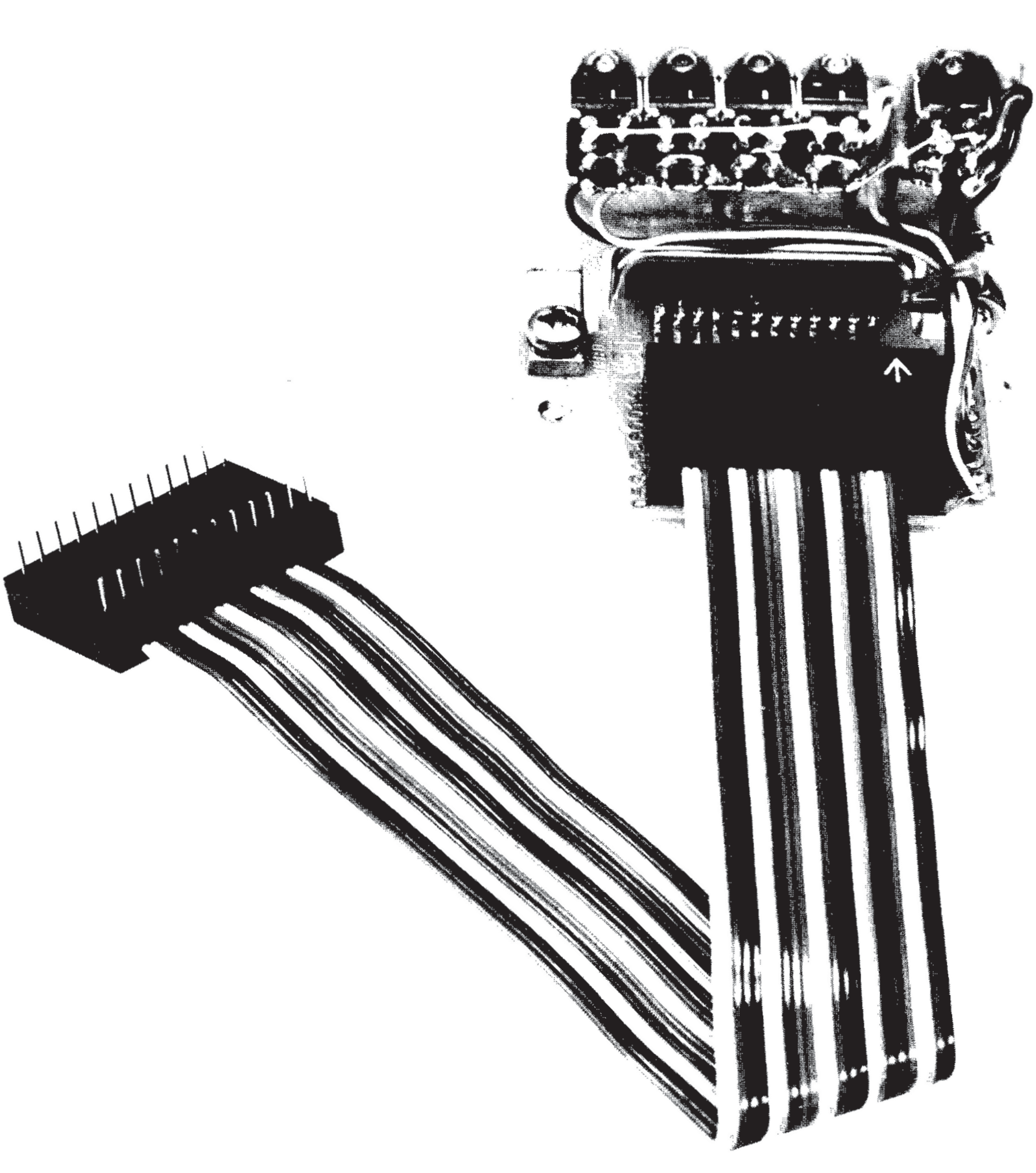
NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS;
   CAPACITANCE IN PICOFARADS;
   INDUCTANCE IN MICROHENRIES

REFERENCE DESIGNATIONS

A18
C1-9
CR1,2
L1,2
Q1,2
R1-7
U1
Y1

Figure 8-22. A18 Option 001 10 MHz Oscillator Assembly



5345-A-52

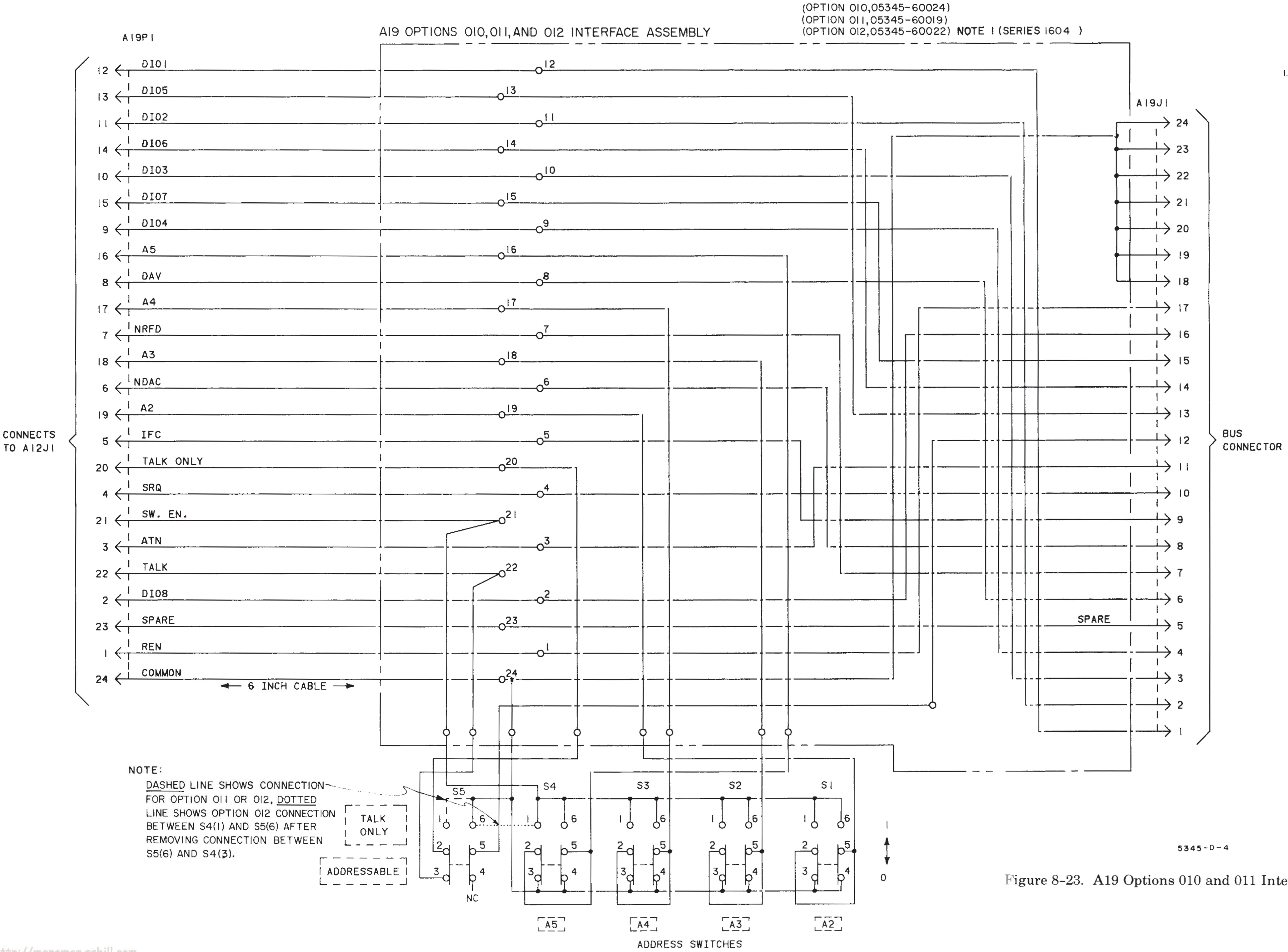
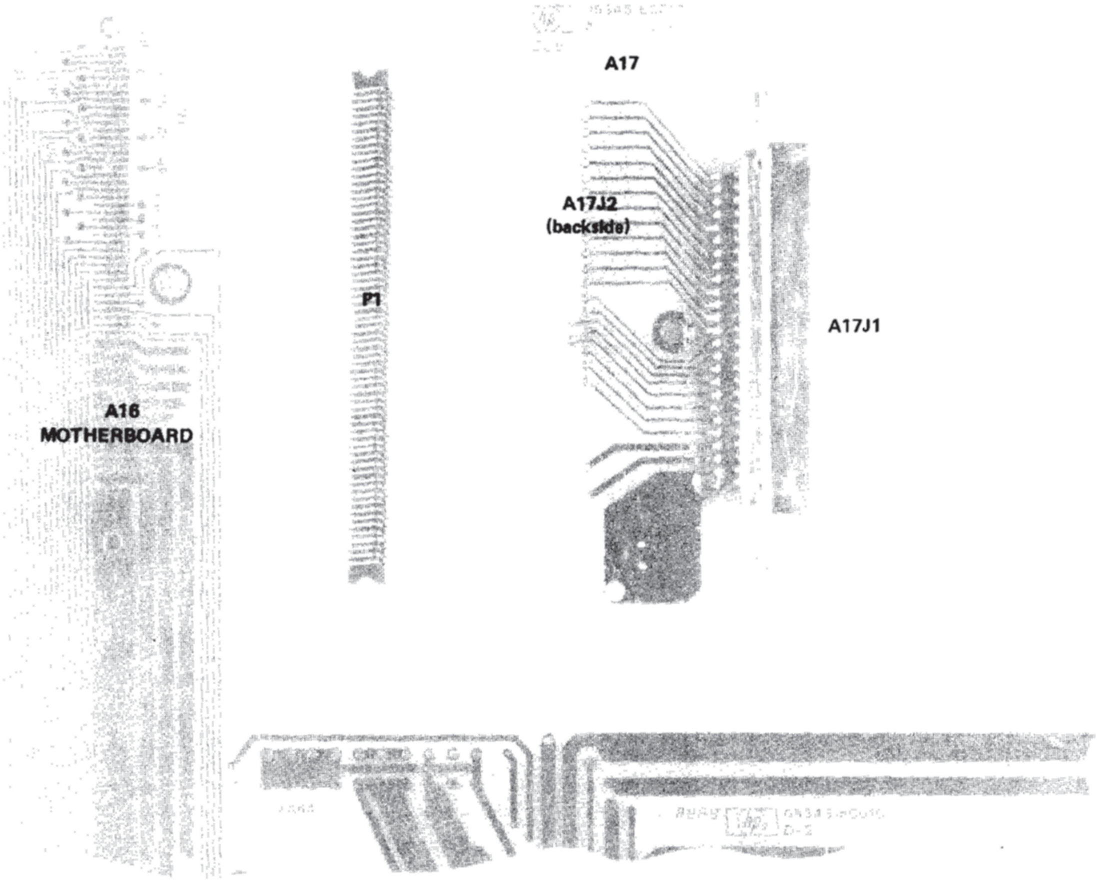

A19 OPTIONS 010, 011, AND 012 INTERFACE ASSEMBLY
(OPTION 010, 05345-60024)
(OPTION 011, 05345-60019)
(OPTION 012, 05345-60022) NOTE 1 (SERIES 1604)
A19P1
CONNECTS TO A12J1
12 DIO1
13 DIO5
11 DIO2
14 DIO6
10 DIO3
15 DIO7
9 DIO4
16 A5
8 DAV
17 A4
7 NRFD
18 A3
6 NDAC
19 A2
5 IFC
20 TALK ONLY
4 SRQ
21 SW. EN.
3 ATN
22 TALK
2 DIO8
23 SPARE
1 REN
24 COMMON
6 INCH CABLE
A19J1
BUS CONNECTOR
SPARE
NOTE:
DASHED LINE SHOWS CONNECTION FOR OPTION 011 OR 012, DOTTED LINE SHOWS OPTION 012 CONNECTION BETWEEN S4(1) AND S5(6) AFTER REMOVING CONNECTION BETWEEN S5(6) AND S4(3).
TALK ONLY
ADDRESSABLE
NC
S5
S4
S3
S2
S1
A5
A4
A3
A2
ADDRESS SWITCHES
1
0
5345-D-4

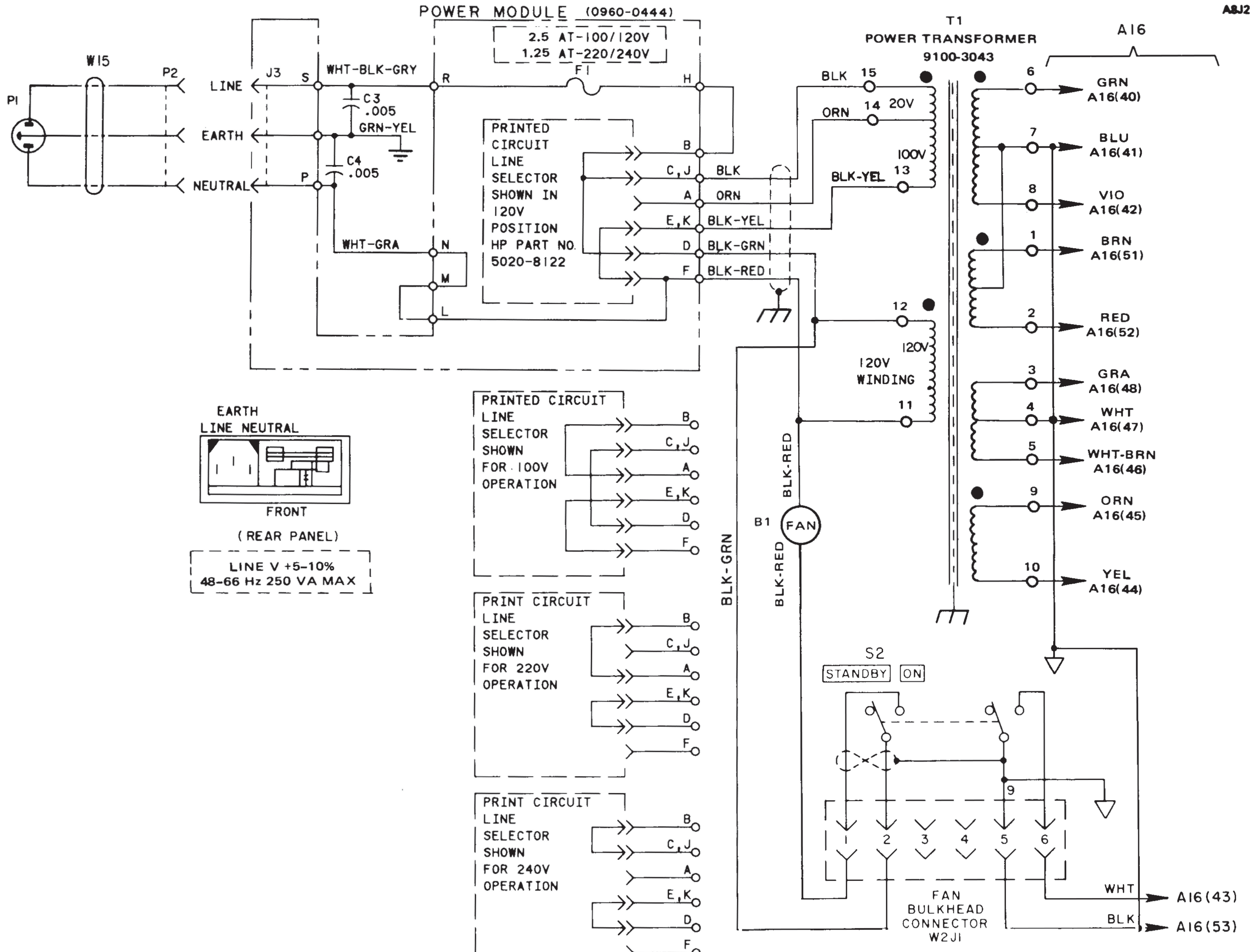
Figure 8-23. A19 Options 010 and 011 Interface Panel Assembly

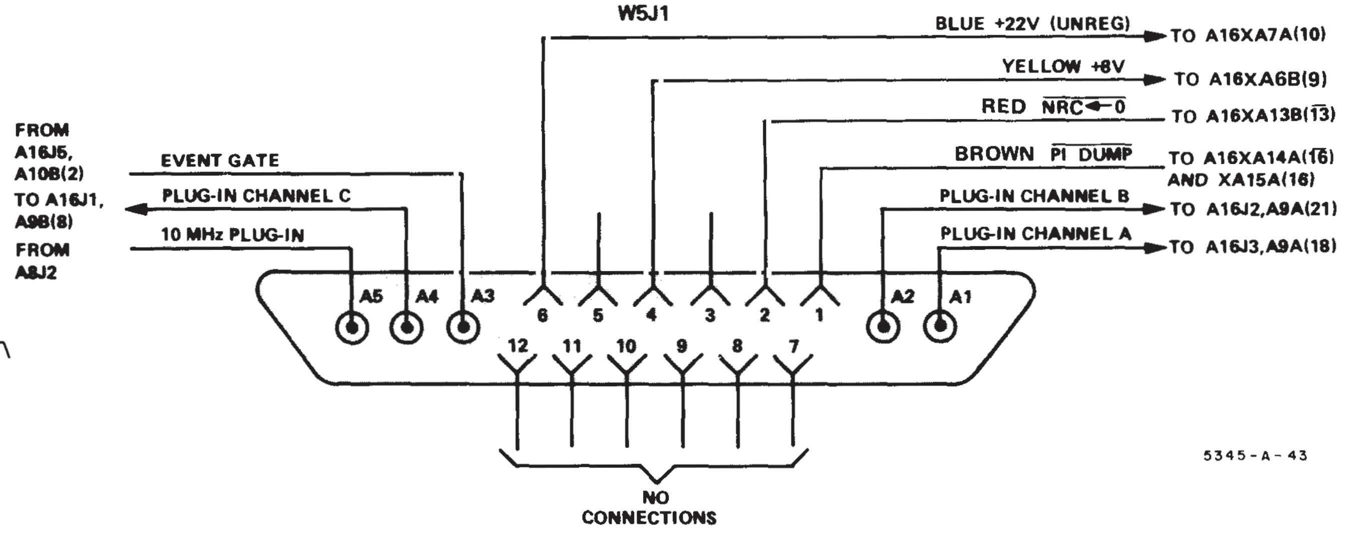
NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.



5345-A-53



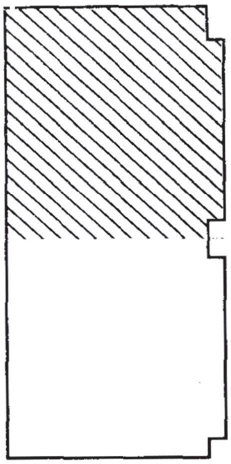


A17J1

LINE NAME	A17J1 PIN #	A16J6 PIN #	FROM	TO
ARMED	13	39	A16(13), A10B(7)	
DR A	1	63	A16(21), A13A(7)	
DR B	4	57	A16(19), A13A(5)	
DR C	2	61	A16(26), A13A(6)	
DR D	3	59	A16(27), A13A($\overline{6}$)	
DISP STR/INH PROC	15	35		A10B(22), A14A($\overline{22}$)
DP A	43	27		A14B($\overline{14}$), A15B(14), A16(1), A2P1(15)
DP B	7	51		A14B($\overline{17}$), A15B(17), A16(3), A2P1(12)
DP C	8	49		A14B($\overline{18}$), A15B(18), A16(5), A2P1(16)
DP D	20	29		A14B($\overline{15}$), A15B(15), A16(2), A2P1(17)
DP E	17	33	TO A15B(13), TO/FROM A14B($\overline{13}$)	
DP F	6	53	TO/FROM A14B($\overline{16}$)	
K DATA/PI INH ARM	40	36		A11B($\overline{20}$), A14A($\overline{15}$)
MEAS TIME	42	28	A10B($\overline{18}$)	
PI ARM	41	30		A11B($\overline{19}$)
PI CLK	16	34	A15B(12)	
PI CLK EN	21	26	A15A($\overline{6}$)	
PI DATA	14	37		A10B($\overline{8}$), A14B(7)
PI DISP POS/GT SEL	10	45		A11B($\overline{3}$), A14B(20)
PI FUNC A	36	44		A10B(11)
PI FUNC B	11	43		A10B(9)
PI FUNC C	12	41		A10B(8)
PI GT/DISP POS A	9	47		A11B(5), A14B($\overline{19}$)
PI GT/DISP POS B	28	60		A11B($\overline{6}$), A14B($\overline{20}$)
PI GT/DISP POS C	30	56		A11B($\overline{9}$), A14B($\overline{22}$)
PI GT/DISP POS D	29	58		A11B(11), A14B($\overline{21}$)
PI INH ANUN	35	46		A10A($\overline{4}$)
PI INV SIGN	27	62		A15B(20)
PI RST	34	48		A11B(20)
PI SEL	39	38	A10A($\overline{21}$)	
PROC BUSY	32	52	A15B(8)	
QR EN A/PI XMT	5	55	A14A($\overline{12}$)	
RMT	31	54	A12B(19)	
RST	38	40	A11B(4)	
SEL A•B	18	32		A10B(6)
SEL C	33	50	A10B(21)	
SIGN -	19	31	TO A10A(18), A12A($\overline{17}$), A13A(17), TO/FROM A15A(19)	
TRANS MULT	37	42		A10A($\overline{19}$)
XS GT RST INH/N DATA	26	64	TO A11B(18), A14B($\overline{2}$), TO/FROM A10B($\overline{22}$)	
+5V REG	23	10,11		
+5V RET	24,25	1-5		
+15V REG	50	6,7		
+15V RET	49	8,9		
-5.2V REG	47	16,17,18		
-5.2V RET	46	19,20,21		
-15V REG	48	12,13		
-15V RET	22	14,15		
+20V REG	45	22,23		
+20V RET	44	24,25		

5345-A-44

Figure 8-24. Wiring: Power Transformer, A17J1, and W5J1



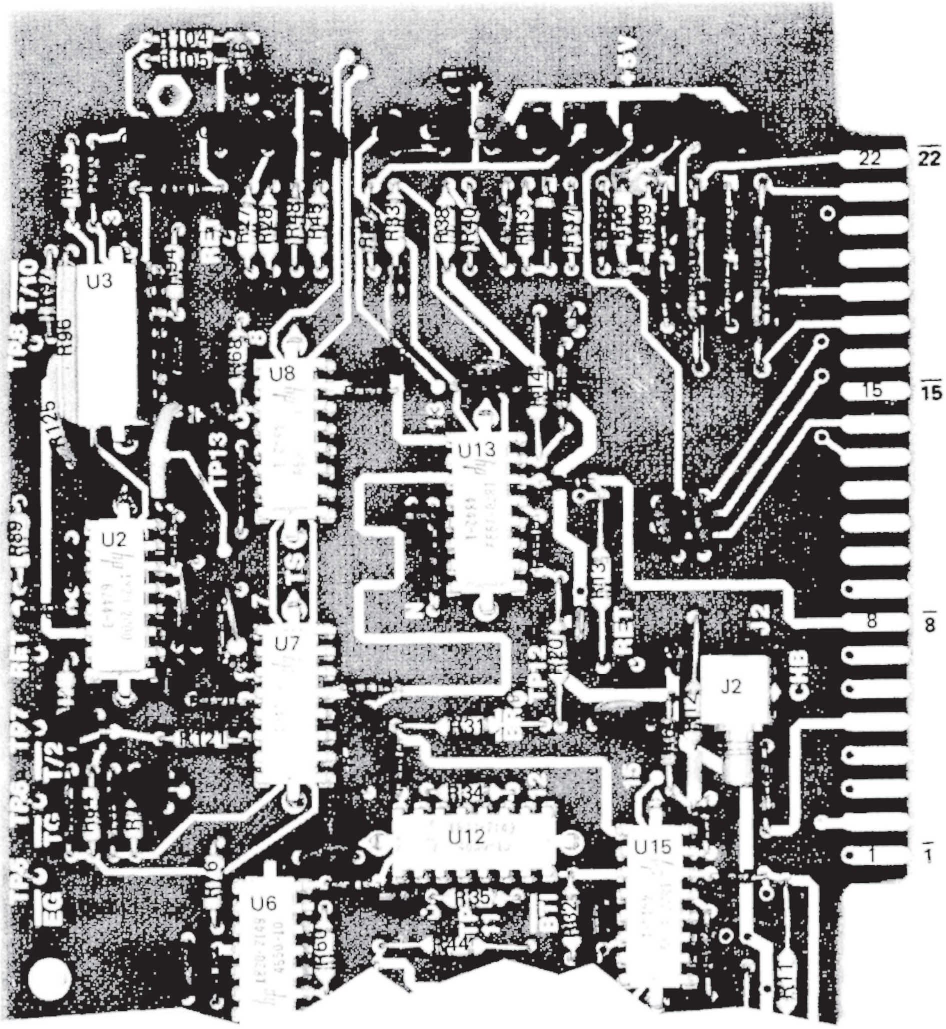
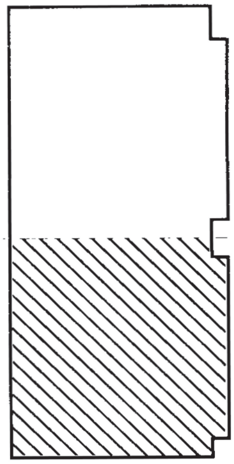


Figure 6A

A9 MAIN GATE ASSEMBLY COMPONENT LOCATOR



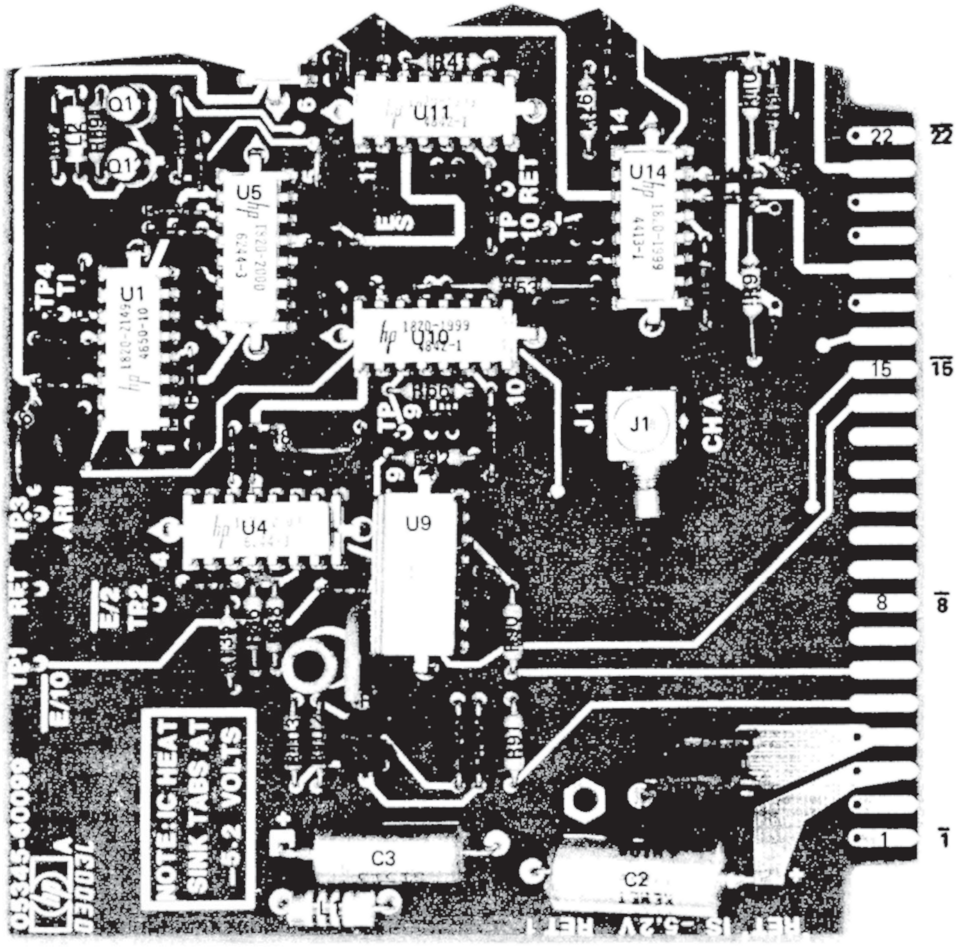


Figure 6B
A9 MAIN GATE ASSEMBLY COMPONENT LOCATOR