| | Display Ramp Start | Display Ramp Stop | Read Address Clock | Write Address Clock | L.S.Bit Write Address | L.S.Bit Read Address | Dot Joiner Sample & Hold (S & H) drive | Dot Joiner Time constant (TC) controls A B C D | 50% Hold conditions | Special Functions | Y Channel Beam Switch |
|---|--|--|--|---|---|--|--|---|--|--|---|
| Normal Mode Single Trace | From Refresh B/S Q | Analogue via TR919 | 0,909 MHz | _ | - | - | - | - | _ | Refresh Mode Selected on R's 19/23 | - |
| Normal Mode Dual Trace | | | • | | - | | | - | _ | _ | Ramp B/S Q clocks (C 708 b, on R1/11 (ALT) 2nd stage R.A.C. driver IC 708 b, clear to give chop (R12/18) |
| Refreshed Mode Ranges 7/23 Single Trace (Released) | From R.A.C. M.S.B. via Delay Circuit | From R.A.C. M.S.B. via Delay Circuit | 0,909 MHz from IC 728a, b, via gate IC 707 | From Bange Divider - See Table for frequency | From Write Address Counter (W.A.C.) | From Read Address Counter (R,A,C,) EXICEPT 50% HOL | P4 Pulse at 0,909 MHz rate via gate IC 732a D l | 0 1 0 1 | 50% Hold drives L.S.B. Write Address high and sets up Dual Trace conditions for Read Address and Dot joiner (Condition 1) | | |
| Refreshed Mode Ranges 7/23 Dual Trace (Released) | | ٠ | - | - | ÷ | From B/S IC 723a via gate IC 719 | P4 Pulse at 0,455 MHz rate via IC 725a, b, & IC 732a | 0 0 1 1 | 50% Hold drives L.S.B. write address high, (Condition 2) | _ | From L.S.B. W.A.C. |
| Refreshed Mode Range 1/6 Single Trace (Released) | | Analogue via TR 919 | 1,818 MHz from PI via IC 7206 | 1,818 MHz on all 6 ranges | | From Read Address Counter (R.A.C.) EX C E P T 50% H O L | P4 Pulse at 1,818 MHz rate via IC 725a, b, & IC 732a D] | 1 1 0 0 | Condition 1 | Write sequence stops read, Then two read sweeps before trigger is enabled | |
| Refreshed Mode Ranges 1/6 Dual Trace (Released) | - | | | | • | From B/S IC 723a via gate IC 719 | P4 Pulse at 0,909 MHz rate via gate 1C 732a | 1 0 1 0 | Condition 2 | | From L.S.B. W.A.C. |
| Roll Mode Ranges 7/23 Single Trace (Released) | From Coincidence gate via delay | From Coincidence gate via delay | 0,909 MHz from IC 728a, b, via gate IC 707 | From Range Divider - See Table for frequency | From Write Address Counter | From Read Address Counter EXCEPT 50% HOL | P4 Puise at 0,909 MHz rate via gate IC 732a D J | 0 1 0 1 | Condition 1 | - | |
| Roll Mode Range 7/23 Dual Trace (Released) | - | - | - | - | - | From B/S IC 723a via gate IC 719 | P4 Puise at 0,455 MHz rate via IC 725a, b, & IC 732a | 0 0 1 1 | Condition 2 | - | From L.S.B. W.A.C. |
| Roll Mode Range 1/6 Single Trace (Released) | From M.S.B. R.A.C. | From M.S.B. R.A.C. | 1,818 MHz from Pl via IC 720b | 1,818 MHz on all 6 ranges | | From RAC | 1,818 MHz rate via gate IC 732a D] | 1 1 0 0 | Condition 1 | Displayed information is set by W.A.C. until "STORE" Condition is reached when R.A.C. addresses store, | |
| Roll Mode Range 1/6 Dual Trace (Released) | (# | | - | - | - | From B/S IC 723a via gate IC 719 | 0,909 MHz rate via gate IC 732a | 1 0 1 0 | Condition 2 | | From L.S.B. W.A.C. |

Fig. 17 Control Condition Table

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Section 5



5.3.1 (Contd.) Ensure timebase is triggering Does Y shift control Is ENTER DATA line NO NO Check store control logic operate? at IC 733 pin 6 being switched Hi? YES YES Are write address Check range divider NO counter clock pulses circuit present at IC732 pin 10? YES Is data changing at D/A Check data path through NO convertor, IC745 store and output from pins 5 - 12? ADC. See section 5.3.4. YES Check dot joiner circuit Check that the modified L.S.B. 1. Is display dual trace? NO of the read address counter at IC719 pin 8 changes after each display sweep. 2. Check that the drive to the beam switch at IC 736 pin 8 is changing. 3. Check that L.S.B. of the write YES address counter at IC702 pin 8 is changing YES Is display distorted by step See section 5.3.4 discontinuities? NO Set TIME/CM switch to 0.5 s/cm. Ensure timebase is being triggered Press STORE button Is ARMED, TRIGGERED, STORED sequence completed NO Check store control logic correctly? YES continued overleaf

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Section 5

5.3.1 (Contd.)

