FLUKE®

Note
This manual applies to SN 6560XXX and higher.

HYDRA

2620A Data Acquisition Unit
2625A Data Logger
2635A Data Bucket

Service Manual

PN 202231
February 1997

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Caution

This is an IEC Safety Class 1 product. Before using, the ground wire in the line cord or the rear panel binding post must be connected for safety.

Interference Information

This equipment generates and uses radio frequency energy and if not installed and used in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception. It has been type tested and found to comply with the limits for a Class B computing device in accordance with the specifications of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation.

Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

There is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of more of the following measures:

- Reorient the receiving antenna
- Relocate the equipment with respect to the receiver
- Move the equipment away from the receiver
- Plug the equipment into a different outlet so that the computer and receiver are on different branch circuits

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the following booklet prepared by the Federal Communications Commission helpful: How to Identify and Resolve Radio-TV Interference Problems. This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20402. Stock No. 004-000-00345-4.

Declaration of the Manufacturer or Importer

We hereby certify that the Fluke Models 2625A Data Logger, 2620A Data Acquisition Unit and 2635A Data Bucket are in compliance with BMPT Vfg 243/1991 and is RFI suppressed. The normal operation of some equipment (e.g. signal generators) may be subject to specific restrictions. Please observe the notices in the users manual. The marketing and sales of the equipment was reported to the Central Office for Telecommunication Permits (BZT). The right to retest this equipment to verify compliance with the regulation was given to the BZT.

Bescheinigung des Herstellers/Importeurs

Hiermit wird bescheinigt, daβ Fluke Models 2625A Data Logger, 2620A Data Acquisition Unit und 2635A Data Bucket in Übereinstimung mit den Bestimmungen der BMPT-AmtsblVfg 243/1991 funk-entstört ist. Der vorschriftsmäßige Betrieb mancher Geräte (z.B. Meßsender) kann allerdings gewissen Einschränkungen unterliegen. Beachten Sie deshalb die Hinweise in der Bedienungsanleitung. Dem Bundesamt für Zulassungen in der Telekcommunikation wurde das Inverkehrbringen dieses Gerätes angezeigt und die Berechtigung zur Überprüfung der Seire auf Einhaltung der Bestimmungen eingeräumt.

Fluke Corporation

Safety Summary

Safety Terms in this Manual

This instrument has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Electronical Measuring, Control and Laboratory Equipment. This Service Manual contains information, warnings, and cautions that must be followed to ensure safe operation and to maintain the instrument in a safe condition. Use of this equipment in a manner mot specified herein may impair the protection by the equipment.

This meter is designed for IEC 64, Installation Category II use. It is not designed for use in circuits rated over 48000VA.

Warning statements identify conditions or practices that could result in personal injury or loss of life.

Caution statements identify conditions or practices that could result in damage to the equipment.

Symbols Marked on Equipment

Danger - High voltage

Ground (Earth) Terminal

Protective ground (earth) terminal. Must be connected to safety earth ground when the power cord is not used. See Section 2.

Attention — refer to the manual. This symbol indicates that information about the use of a feature is contained in the manual. This symbol appears in the following places on the rear panel:

1. Ground Binding Post (left of line power connector). Refer to “Using External DC Power” in Section 2.

2. Alarm Ouputs/Digital I/O Connectors. Refer to Appendix A, Specifications.

AC Power Source

The instrument is intended to operate from a ac power source that will not apply more than 264V ac rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is required for safe operation.

DC Power Source

The instrument may also be operated from a 9 to 16V dc power source when either the rear panel ground binding post or the power cord grounding conductor is properly connected.

Use the Proper Fuse

To avoid fire hazard, use only a fuse identical in type, voltage rating, and current rating as specified on the rear panel fuse rating label.

Grounding the Standard

The instrument utilized controlled overvoltage techniques that require the instrument to be grounded whenever normal mode or common mode ac voltage or transient voltages may occur. The enclosure must be grounded through the grounding conductor of the power cord, or if operated on battery with the power cord unplugged, through the rear panel ground binding post.

Use the Proper Power Cord

Use only the power cord and connector appropriate for the voltage and plug configuration in your country.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate the instrument in an atmosphere of explosive gas.

Do Not Remove Cover

To avoid personal injury or death, do not remove the instrument cover. Do not operate the instrument without the cover properly installed. Normal calibration is accomplished with the cover closed, and there are no user-serviceable parts inside the instrument, so there is no need for the operator to ever remove the cover. Access procedures and the warnings for such procedures are contained in the Service Manual. Service procedures are for qualified service personnel only.

Do Not Attempt to Operate if Protection May be Impaired

If the instrument appears damaged or operates abnormally, protection may be impaired. Do not attempt to operate it. When is doubt, have the instrument serviced.

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Chapter 1
Introduction and Specifications

1-1. Introduction

Hydra measures analog inputs of dc and ac volts, thermocouple and RTD temperatures, resistance, and frequency. It features 21 measurement input channels. In addition, it contains eight digital input/output lines, one totalizing input, one external scan trigger input, and four alarm output lines. Hydra is fully portable and can be ac or dc powered. An RS-232 computer interface is standard. An optional IEEE-488 computer interface is available for the Hydra Data Acquisition Unit (2620A) only.

The Hydra Data Logger (2625A) adds substantial measurement memory capabilities. The RS-232 computer interface is standard, but IEEE-488 capability is not available for the Hydra Data Logger.

The Hydra Data Bucket (2635A) adds more flexible storage for instrument setups and measurement data by adding a PCMCIA memory card and interface. The amount of storage can be easily changed by selecting a memory card of the appropriate size for the job.

The Hydra instruments share many features and functions. The term "instrument" is used to refer to all three instruments. The model number (2620A, 2625A, or 2635A) is used when discussing features unique to one instrument.

The instrument is designed for bench-top, field service, and system applications. A dual vacuum-fluorescent display uses combinations of alphanumeric characters and descriptive annunciators to provide prompting and measurement information during setup and operation modes.

Some features provided by the instrument are listed in Table 1-1.

1-2. Options and Accessories

The following items can be installed either at the factory or in the field:

- Option 2620A-05K (IEEE-488 Interface Kit) consists of a printedcircuit assembly, connecting cable, and mounting hardware. Thisfield-installable kit gives the 2620A Hydra Data Acquisition UnitIEEE-488 interface capabilities. IEEE-488 computer interfacecommands are virtually identical to RS-232 interface commands. (The2625A and 2635A cannot be equipped with an IEEE-488 Interface.)
- Accessory 2620A-100 (Connector Kit).

The instrument can be mounted in a standard 19-inch rack panel on either the right-hand or left-hand side using the Fluke M00-200-634 Rackmount Kit.

Accessories are listed in Table 1-2.

1-3. Operating Instructions

Full operating instructions are provided in the Hydra User Manual (2620A or 2625A) and in the Hydra Data Bucket User Manual (2635A). Refer to the User Manual as necessary during the maintenance and repair procedures presented in this Service Manual.

1-4. Organization of the Service Manual

This manual focuses on performance tests, calibration procedures, and component-level repair of each of the instruments. To that end, manual sections are often interdependent; effective troubleshooting may require not only reference to the troubleshooting procedures in Section 5, but also some understanding of the detailed Theory of Operation in Section 2 and some tracing of circuit operation in the Schematic Diagrams presented in Section 8.

Often, scanning the table of contents will yield an appropriate place to start using the manual. A comprehensive table of contents is presented at the front of the manual; local tables of contents are also presented at the beginning of each chapter for ease of reference. If you know the topic name, the index at the end of the manual is probably a good place to start.

The following chapter descriptions serve to introduce the manual:

Chapter 1. Introduction and Specifications

Introduces the instrument, describing its features, options, and accessories. This chapter also discusses use of the Service Manual and the various conventions used in describing the circuitry. Finally, a complete set of specifications is presented.

Chapter 2. Theory of Operation (2620A and 2625A)

This chapter first categorizes these instrument's circuitry into functional blocks, with a description of each block's role in overall operation. A detailed circuit description is then given for each block. These descriptions explore operation to the component level and fully support troubleshooting procedures defined in Chapter 5.

Chapter 2A. Theory of Operation (2635A)

This chapter first categorizes the instrument's circuitry into functional blocks, with a description of each block's role in overall operation. A detailed circuit description is then given for each block. These descriptions explore operation to the component level and fully support troubleshooting procedures defined in Chapter 5A.

Chapter 3. General Maintenance

Provides maintenance information covering handling, cleaning, and fuse replacement. Access and reassembly procedures are also explained in this chapter.

Chapter 4. Performance Testing and Calibration

This chapter provides performance verification procedures, which relate to the specifications presented in Chapter 1. To maintain these specifications, a full calibration procedure is also presented.

Chapter 5. Diagnostic Testing and Troubleshooting (2620A and 2625A)

The troubleshooting procedures presented in this chapter rely closely on both the Theory of Operation presented in Chapter 2, the Schematic Diagrams shown in Chapter 8, and the access information provided in Chapter 3.

Chapter 5A. Diagnostic Testing and Troubleshooting (2635A)

The troubleshooting procedures presented in this chapter rely closely on both the Theory of Operation presented in Chapter 2A, the Schematic Diagrams shown in Chapter 8, and the access information provided in Chapter 3.

Chapter 6. List of Replaceable Parts

Includes parts lists for all standard assemblies. Information on how and where to order parts is also provided.

Chapter 7. IEEE-488 Option (2620A only)

This chapter describes the IEEE-488 option. Included are specifications, theory of operation, maintenance, and a list of replaceable parts. Schematic diagrams for this option are included at the end of the overall Service Manual (Chapter 8).

Chapter 8. Schematic Diagrams

Includes schematic diagrams for all standard and optional assemblies. A list of mnemonic definitions is also included to aid in identifying signal name abbreviations.

Chapter 9. HYDRA Starter Calibration Software

This chapter provides an extened tutorial that demostrates how to perform a series of operations. These operations introduce you to the menu structure of the Starter with cal software, explain what the menu items do, and teach you how to use them.

1-5. Conventions

Throughout the manual set, certain notational conventions are used. A summary of these conventions follows:

- Instrument Reference

  The Hydra Data Acquisition Unit (Model 2620A), the Hydra Data Logger(Model 2625A), and the Hydra Data Bucket (Model 2635A) share manyfeatures and functions. The term Hydra refers to any of theseinstruments. The model number (e.g., 2620A, 2625A, or 2635A) isused when features unique to one instrument are being described.

- Printed Circuit Assembly

  The term "pca" is used to represent a printed circuit board and itsattached parts.

- Signal Logic Polarity

  On schematic diagrams, a signal name followed by a "*" is active (orasserted) low. Signals not so marked are active high.

- Circuit Nodes

  Individual pins or connections on a component are specified with adash (-) following the assembly and component reference designators.For example, pin 19 of U30 on assembly A1 would be A1U30-19.

- User Notation

  For front panel operation,

  XXXAn uppercase word or symbol without parentheses indicates a button to be pressed by the user. Buttons can be pressed in four ways:

  1. Press a single button to select a function or operation.
  2. Press a combination of buttons, one after the other.
  3. Press and hold down a button, then press another button.
  4. Press multiple buttons simultaneously.

For computer interface operation,

XXX	An uppercase word without parentheses identifies a command byname.
<XXX>	Angle brackets around all uppercase letters mean press the<XXX> key.
(xxx)	When associated with a keyword, a lowercase word inparentheses indicates an input required by the user.

Table 1-1. Hydra Features

- Channel Scanning

  Can be continuous scanning, scanning at an interval time, single scans, or triggered (internal or external) scans.
- Channel Monitoring

  Make measurements on a single channel and view these measurements on the display.
- Channel Scanning and Monitoring

  View measurements made for the monitor channel while scanning of all active channels continues.
- Multi-Function Display

  Left (numeric) display shows measurement readings; also used when setting numeric parameters.

  Right (alphanumeric) display used for numeric entries, channel number selection and display, status information, and operator prompts.
- Front-Panel Operation

  Almost all operations can be readily controlled with the buttons on the front panel.
- Measurement Input Function and Range

  Volts dc (VDC), volts ac (VAC), frequency (Hz), and resistance (Ω) inputs can be specified in a fixed measurement range. Autoranging, which allows the instrument to use the measurement range providing the optimum resolution, can also be selected.
- Temperature Measurement

  Thermocouple types J, K, E, T, N, R, S, B, and Hoskins Engineering Co. type C are supported.Also, DIN/IEC 751 (Pt 385) Platinum RTDs are supported.
- Totalize Events on the Totalizing Input
- Alarms Limits and Digital Output Alarm Indication
- 4-Terminal Resistance Measurements (Ch. 1 .. 10)
- RS-232 Computer Interface Operation
- Measurement Rate Selection
- Nonvolatile Memory

  Storage of minimum, maximum, and most recent measurements for all scanned channels.

  Storage of Computer Interface setup, channel configurations, and calibration values.
- Features unique to the 2625A Data Logger.

  Storage of measurement data: storage for 2047 scans of up to 21 channels, representing up to 42,987 readings.
- Features unique to the 2635A Data Bucket.

  Internal storage of measurement data for 100 scans of up to 21 channels, representing up to 2,100 readings.

  Memory card storage of instrument setup configurations so that instrument may be quickly set up to do different tasks.

  Memory card storage of measurement data for up to 4,800 scans of 10 channels on a 256K-byte card or up to 19,800 scans of 10 channels on a 1M-byte memory card.

  Enhanced RS-232 interface with higher baud rates and hardware flow control using the Clear to Send modem control signal.

Table 1-2. Accessories

Model	Description
80i-410 80i-1010	Clamp-On DC/AC Current Probes
80J-10	Current Shunt
2620A-05K	Field-installable IEEE-488 Option kit (Hydra Data Acquisition Unit only.)
2620A-100	Extra I/O Connector Set: Includes Universal Input Module, Digital I/O and Alarm Output Connectors.
262XA-801	Diconix(R) 80-column serial printer.
263XA-803	Memory Card Reader for IBM-PC or compatible personal computer. Card reader is external to the PC and connects to a PC parallel port (LPT1, LPT2, etc.). (2635A Data Bucket only).
263XA-804	256K-Byte Memory Card (2635A Data Bucket only). (This card is supplied with the instrument.)
263XA-805	1M-Byte Memory Card (2635A Data Bucket only).
26XXA-901	Hydra Logger Applications Package (Version 3.0)
C40	Soft carrying case. Provides padded protection for the instrument. Includes a pocket for the manual and pouch for the line cord.
M00-200-634	Rackmount Kit. Provides standard 19-inch rack mounting for one instrument (right or left side.)
PM 8922	Switchable X1, X10 passive probe.
RS40	Shielded RS-232 terminal interface cable. Connects the instrument to any terminal or printer with properly configured DTE connector (DB-25 socket), including an IBM PC(R), IBM PC/XT(R) or IBM PS/2 (models 25, 30, 50, P60, 70, and 80).
RS41	Shielded RS-232 modem cable. Connects the instrument to a modem with properly configured DB-25 male pin connector. Use an RS40 and an RS41 cable in series to connect with an IBM PC/AT(R).
RS42	Shielded serial printer cable. Contact Fluke for list of compatible printers.
TL20	Industrial test lead set.
TL70A	Test lead set (one set is supplied with the instrument).
Y8021	Shielded IEEE-488 one-meter (39.4 inches) cable, with plug and jack at each end.
Y8022	Shielded IEEE-488 two-meter (78.8 inches) cable, with plug and jack at each end.
Y8023	Shielded IEEE-488 four-meter (13 feet) cable, with plug and jack at each end.
Y9109	Binding post to BNC plug.
Footnote: IBM PC, IBM PC/XT, and IBM PC/AT are registered trademarks of International Business Machines	

1-6. Specifications

Table 1-3 contains the specifications for the 2620A and 2625A.

Table 1-4 contains the specifications for the 2635A.

Table 1-3. 2620A/2625A Specifications

The instrument specifications presented here are applicable within the conditions listed in the Environmental portion of this specification.

The specifications state total instrument accuracy following calibration, including:

- A/D errors
- Linearization conformity
- Initial calibration errors
- Isothermality errors
- Relay thermal emf's
- Reference junction conformity
- Temperature coefficients
- Humidity errors

Sensor inaccuracies are not included in the accuracy figures.

Accuracies at Temperatures Other Than Specified

To determine typical accuracies at temperatures intermediate to those listed in the specification tables, linearly interpolate between the applicable 0oC to 60oC and 18oC to 28oC accuracy specifications.

Response Times

Refer to Typical Scanning Rate and Maximum Autoranging Time later in this table.

DC Voltage Inputs

Resolution		
Range	**Slow**	**Fast**
300 mV	10 µV	0.1 mV
3V	0.1 mV	1 mV
30V	1 mV	10 mV
300V	10 mV	0.1V

Range	Accuracy ±(% ±V)				
	18°C to 28°C			0°C to 60°C	
	90 Days, Slow	**1 Year, Slow**	**1 Year, Fast**	**1 Year, Slow**	**1 Year, Fast**
300 mV	0.026% + 20 µV	0.031% + 20 µV	0.047% + 0.2 mV	0.070% + 20 µV	0.087% + 0.2 mV
3V	0.028% + 0.2 mV	0.033% + 0.2 mV	0.050% + 2 mV	0.072% + 0.2 mV	0.089% + 2 mV
30V	0.024% + 2 mV	0.029% + 2 mV	0.046% + 20 mV	0.090% + 2 mV	0.107% + 20 mV
300V	0.023% + 20 mV	0.028% + 20 mV	0.045% + 0.2V	0.090% + 20 mV	0.107% + 0.2V

Input Impedance

100 MΩ minimum in parallel with 150 pF maximum for all ranges 3V and below 10 MΩ in parallel with 100 pF maximum for the 30V and 300V ranges.

Normal Mode Rejection

53 dB minimum at 60 Hz ±0.1%, slow rate
47 dB minimum at 50 Hz ±0.1%, slow rate

Common Mode Rejection

120 dB minimum at dc, 1 kΩ imbalance, slow rate
120 dB minimum at 50 or 60 Hz ±0.1%, 1 kΩ imbalance, slow rate

Maximum Input

300V dc or ac rms on any range for channels 0, 1, and 11
150V dc or ac rms for channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Table 1-3. 2620A/2625A Specifications (cont)

Thermocouple Inputs

Thermocouple		Accuracy (±°C)*				
		18°C to 28°C			0°C to 60°C	
Type	Temperature (°C)	90 Days Slow	1 Year Slow	1 Year Fast	1 Year Slow	1 Year Fast
J	-100.00	0.49	0.53	1.00	0.73	1.22
	0.00	0.38	0.40	0.77	0.53	0.91
	760.00	0.49	0.54	0.97	0.91	1.35
K	-100.00	0.57	0.60	1.20	0.82	1.43
	0.00	0.42	0.44	0.88	0.57	1.02
	1000.00	0.73	0.80	1.46	1.36	2.03
	1372.00	0.95	1.05	1.89	1.85	2.70
N	-100.00	0.66	0.69	1.48	0.90	1.70
	0.00	0.51	0.53	1.14	0.66	1.29
	400.00	0.46	0.49	0.99	0.72	1.23
	1300.00	0.75	0.83	1.53	1.45	2.16
E	-100.00	0.50	0.53	0.99	0.75	1.22
	0.00	0.36	0.38	0.72	0.52	0.86
	500.00	0.40	0.43	0.77	0.71	1.05
	1000.00	0.58	0.65	1.11	1.16	1.63
T	-150.00	0.79	0.84	1.66	1.16	1.99
	0.00	0.42	0.45	0.89	0.58	1.04
	400.00	0.37	0.40	0.74	0.61	0.97
R	250.00	0.96	0.98	2.48	1.14	2.65
	1000.00	0.86	0.91	2.10	1.29	2.48
	1767.00	1.14	1.24	2.65	1.96	3.38
S	250.00	1.01	1.03	2.62	1.20	2.80
	1000.00	0.97	1.02	2.37	1.42	2.77
	1767.00	1.29	1.39	3.02	2.17	3.80
B	600.00	1.26	1.28	3.52	1.40	3.64
	1000.00	0.92	0.95	2.48	1.16	2.69
	1820.00	0.97	1.03	2.41	1.51	2.89
C	0.00	0.76	0.78	1.87	0.92	2.01
	500.00	0.66	0.69	1.53	0.96	1.81
	1000.00	0.85	0.91	1.90	1.41	2.41
	1850.00	1.47	1.61	3.18	2.70	4.29
	2316.00	2.30	2.53	4.93	4.35	6.77

* Sensor inaccuracies are not included.

Table 1-3. 2620A/2625A Specifications (cont)

Thermocouple Inputs (cont)

Input Impedance

100 MΩ minimum in parallel with 150 pF maximum

Common Mode and Normal Mode Rejection

See Specifications, DC Voltage Inputs

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Open Thermocouple Detect

Small ac signal injection and detection scheme before each measurement detects greater than 1 to 4 kΩ as open. Performed on each channel unless defeated by computer command.

RTD Inputs

Type

DIN/IEC 751, 100Ω Platinum

RTD Temperature (°C)	1 Year, 4-Wire Accuracy (±°C)					
	Resolution		18°C to 28°C		0°C to 60°C	
	Slow	Fast	Slow	Fast	Slow	Fast
-200.00	0.02	0.01	0.08	0.49	0.12	0.54
0.00	0.02	0.01	0.21	0.67	0.50	0.96
100.00	0.02	0.01	0.27	0.75	0.69	1.17
300.00	0.02	0.01	0.41	0.92	1.10	1.60
600.00	0.02	0.01	0.65	1.21	1.77	2.33

2-Wire Accuracy

Not specified

Maximum Current Through Sensor

1 mA

Typical Full Scale Voltage

0.22V

Maximum Open Circuit Voltage

3.2V

Maximum Sensor Temperature

600°C nominal
999.99°F is the maximum that can be displayed when using °F.

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Table 1-3. 2620A/2625A Specifications (cont)

AC Voltage Inputs (True RMS AC Voltage, AC-Coupled Inputs)

Range	Resolution		Minimum Input for Rated Accuracy
	Slow	Fast	
300 mV	10 µV	100 µV	20 mV
3V	100 µV	1 mV	200 mV
30V	1 mV	10 mV	2V
300V	10 mV	100 mV	20V

1 Year Accuracy ±(%±V)

Frequency	18°C to 28°C		0°C to 60°C	
	SLow	Fast	Slow	Fast
300 mV Range				
20 Hz - 50 Hz	1.43% + 0.25 mV	1.43% + 0.4 mV	1.54% + 0.25 mV	1.54% + 0.4 mV
50 Hz - 100 Hz	0.30% + 0.25 mV	0.30% + 0.4 mV	0.41% + 0.25 mV	0.41% + 0.4 mV
100 Hz - 10 kHz	0.17% + 0.25 mV	0.17% + 0.4mV	0.28% + 0.25 mV	0.28% + 0.4 mV
10 kHz - 20 kHz	0.37% + 0.25 mV	0.37% + 0.4mV	0.68% + 0.25 mV	0.68% + 0.4 mV
20 kHz - 50 kHz	1.9% + 0.30 mV	1.9% + 0.5 mV	3.0% + 0.30 mV	3.0% + 0.5 mV
50 kHz - 100 kHz	5.0% + 0.50 mV	5.0% + 1.0 mV	7.0% + 0.50 mV	7.0% + 1.0 mV
3V Range				
20 Hz - 50 Hz	1.42% + 2.5 mV	1.42% + 4 mV	1.53% + 2.5 mV	1.53% + 4 mV
50 Hz - 100 Hz	0.29% + 2.5 mV	0.29% + 4 mV	0.40% + 2.5 mV	0.40% + 4 mV
100 Hz - 10 kHz	0.14% + 2.5 mV	0.14% + 4 mV	0.25% + 2.5 mV	0.25% + 4 mV
10 kHz - 20 kHz	0.22% + 2.5 mV	0.22% + 4 mV	0.35% + 2.5 mV	0.35% + 4 mV
20 kHz - 50 kHz	0.6% + 3.0 mV	0.6% + 5 mV	0.9% + 3.0 mV	0.9% + 5 mV
50 kHz - 100 kHz	1.0% + 5.0 mV	1.0% + 10 mV	1.4% + 5.0 mV	1.4% + 10 mV
30V Range				
20 Hz - 50 Hz	1.43% + 25 mV	1.43% + 40 mV	1.58% + 25 mV	1.58% + 40 mV
50 Hz - 100 Hz	0.29% + 25 mV	0.29% + 40 mV	0.45% + 25 mV	0.45% + 40 mV
100 Hz - 10 kHz	0.15% + 25 mV	0.15% + 40 mV	0.30% + 25 mV	0.30% + 40 mV
10 kHz - 20 kHz	0.22% + 25 mV	0.22% + 40 mV	0.40% + 25 mV	0.40% + 40 mV
20 kHz - 50 kHz	0.9% + 30 mV	0.9% + 50 mV	1.1% + 30 mV	1.1% + 50 mV
50 kHz - 100 kHz	2.0% + 50 mV	2.0% + 100 mV	2.2% + 50 mV	2.2% + 100 mV
300V Range				
20 Hz - 50 Hz	1.42% + 0.25V	1.42% + 0.4V	1.57% + 0.25V	1.57% + 0.4V
50 Hz - 100 Hz	0.29% + 0.25V	0.29% + 0.4V	0.44% + 0.25V	0.44% + 0.4V
100 Hz - 10 kHz	0.14% + 0.25V	0.14% + 0.4V	0.29% + 0.25V	0.29% + 0.4V
10 kHz - 20 kHz	0.22% + 0.25V	0.22% + 0.4V	0.38% + 0.25V	0.38% + 0.4V
20 kHz - 50 kHz	0.9% + 0.30V	0.9% + 0.5V	1.0% + 0.30V	1.0% + 0.5V
50 kHz - 100 kHz	2.5% + 0.50V	2.5% + 1.0V	2.6% + 0.50V	2.6% + 1.0V

Table 1-3. 2620A/2625A Specifications (cont)

AC Voltage Inputs (True RMS AC Voltage, AC-Coupled Inputs) (cont)

Maximum Frequency	Input at Upper Frequency
20 Hz - 50 Hz	300V rms
50 Hz - 100 Hz	300V rms
100 Hz - 10 kHz	200V rms
10 kHz - 20 kHz	100V rms
20 kHz - 50 kHz	40V rms
50 kHz - 100 kHz	20V rms

Input Impedance

1 MΩ in parallel with 100 pF maximum

Maximum Crest Factor

3.0 maximum
2.0 for rated accuracy

Crest Factor Error

Non-sinusoidal input signals with crest factors between 2 and 3 and pulse widths 100 μs and longer add 0.2% to the accuracy specifications.

Common Mode Rejection

80 dB minimum at 50 or 60 Hz ±0.1%, 1 kΩ imbalance, slow rate

Maximum AC Input

300V rms or 424V peak on channels 0, 1, and 11
150V rms or 212V peak on channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded

2×10^6 Volt-Hertz product on any range, normal mode input
1×10^6 Volt-Hertz product on any range, common mode input

DC Component Error

SCAN and first MONitor measurements will be incorrect if the dc signal component exceeds 60 counts in slow rate or 10 counts in fast rate. To measure ac with a dc component present, MONitor the input and wait 5 seconds before recording the measurement.

Using Channel 0

When measuring voltages above 100V rms, the rear Input Module must be installed to obtain the rated accuracy.

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Table 1-3. 2620A/2625A Specifications (cont)

Ohms Input

Range	Resolution		Typical Full Scale Voltage	Maximum Current Through Unknown	Maximum Open Circuit Voltage
	Slow	Fast			
300Ω	10 mΩ	0.1Ω	0.22V	1 mA	3.2V
3 kΩ	0.1Ω	1Ω	0.25V	110 µA	1.5V
30 kΩ	1Ω	10Ω	0.29V	13 µA	1.5V
300 kΩ	10Ω	100Ω	0.68V	3.2 µA	3.2V
3 MΩ	100Ω	1 kΩ	2.25V	3.2 µA	3.2V
10 MΩ	1 kΩ	10 kΩ	2.72V	3.2 µA	3.2V

4-Wire Accuracy ±(% ± Ω)					
Range	18°C to 28°C			0°C to 60°C	
	90 Days, Slow	1 Year, Fast	1 Year, Fast	1 Year, Fast	1 Year, Fast
300Ω	0.056% + 20 mΩ	0.060% + 20 mΩ	0.060% + 0.2Ω	0.175% + 20 mΩ	0.175% + 0.2Ω
3 kΩ	0.053% + 0.2Ω	0.057% + 0.2Ω	0.057% + 2Ω	0.172% + 0.2Ω	0.172% + 2Ω
30 kΩ	0.055% + 2Ω	0.059% + 2Ω	0.059% + 20Ω	0.176% + 2Ω	0.176% + 20Ω
300 kΩ	0.053% + 20Ω	0.057% + 20Ω	0.057% + 200Ω	0.184% + 20Ω	0.184% + 200Ω
3 MΩ	0.059% + 200Ω	0.063% + 200Ω	0.063% + 2 kΩ	0.203% + 200Ω	0.203% + 2 kΩ
10 MΩ	0.115% + 2 kΩ	0.120% + 2 kΩ	0.200% + 30 kΩ	0.423% + 2 kΩ	0.423% + 30 kΩ

2-wire Accuracy

Not specified

Input Protection

300V dc or ac rms on all ranges

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Frequency Inputs

Frequency Range

15 Hz to greater than 1 MHz

Range	Resolution		Accuracy ±(% ± Hz)	
	Slow	Fast	Slow	Fast
15 Hz - 900 Hz	0.01 Hz	0.1 Hz	0.05% + 0.02 Hz	0.05% + 0.2 Hz
9 kHz	0.1 Hz	1 Hz	0.05% + 0.1 Hz	0.05% + 1 Hz
90 kHz	1 Hz	10 Hz	0.05% + 1 Hz	0.05% + 10 Hz
900 kHz	10 Hz	100 Hz	0.05% + 10 Hz	0.05% + 100 Hz
1 MHz	100 Hz	1 Hz	0.05% + 100 Hz	0.05% + 1 kHz

Table 1-3. 2620A/2625A Specifications (cont)

Frequency Inputs (cont)

Sensitivity

Frequency	Level (sine Wave)
15 Hz - 100 kHz	100 mV rms
100 kHz - 300 kHz	150 mV rms
300 kHz - 1 MHz	2V rms
Above 1 MHz	NotSpecified

Maximum AC Input

300V rms or 424V peak on channels 0, 1, and 11
150V rms or 212V peak on channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded

2×10^6 Volt-Hertz product on any range, normal mode input
1×10^6 Volt-Hertz product on any range, common mode input

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Typical Scanning Rate

(Channels per Second, for 1, 10, and 20 Channel Scans with Shorted Inputs)

Function	Range	Slow			Fast		
Channels:		1	10	20	1	10	20
VDC	300 mV	1.7	3.6	3.8	2.2	10.3	12.9
VDC	3V	1.7	3.6	3.8	2.2	10.3	12.9
VDC	30V	1.7	3.6	3.8	2.2	10.3	12.9
VDC	150/300V	1.7	3.5	3.8	2.2	10.2	12.8
VDC	AUTO	1.0	3.4	3.6	2.2	8.9	10.7
Temperature	J	1.5	3.1	3.5	1.9	9.5	12.1
Temperature	PT	1.0	2.5	2.6	1.7	4.2	4.5
VAC	300 mV	1.0	1.5	1.5	1.3	2.3	2.4
VAC	3V	1.0	1.5	1.5	1.3	2.3	2.4
VAC	30V	1.0	1.5	1.5	1.3	2.3	2.4
VAC	150/300V	1.0	1.5	1.5	1.3	2.3	2.4
VAC	AUTO	1.0	1.4	1.5	1.3	2.3	2.4
Ohms	300Ω	1.5	2.5	2.6	1.8	4.2	4.5
Ohms	3 kΩ	1.5	2.5	2.6	1.7	4.2	4.5
Ohms	30 kΩ	1.5	2.5	2.6	1.7	4.2	4.5
Ohms	300 kΩ	1.0	1.5	1.5	1.4	2.8	2.9
Ohms	3 MΩ	1.0	1.5	1.5	1.4	2.7	2.9
Ohms	10 MΩ	1.0	1.5	1.5	1.4	2.7	2.9
Ohms	AUTO	1.5	2.5	2.6	1.7	4.2	4.5
Frequency	any	0.5	0.6	0.7	0.6	0.7	0.7

Table 1-3. 2620A/2625A Specifications (cont)

Maximum Autoranging Time (Seconds per Channel)

Function	Range Change	Slow	Fast
VDC	300 mV to 150V	0.25	0.19
	150V to 300 mV	0.25	0.18
VAC	300 mV to 150V	1.40	1.10
	150V to 300 mV	1.40	1.10
Ohms	300Ω to 10.0 MΩ	1.70	0.75
	10.0 MΩ to 300Ω	1.70	0.60

Totalizing Inputs

Input Voltage	30V maximum -4V minimum 2V peak minimum signal
Isolation	None dc-coupled
Threshold	1.4V
Hysteresis	500 mV
Input Debouncing	None or 1.66 ms
Rate	0 to 5 kHz with debouncing off
Maximum Count	65,535

Digital Inputs

Input Voltage	30V maximum -4V minimum
Isolation	None dc-coupled
Threshold	1.4V
Hysteresis	500 mV

Trigger Inputs

Input Voltages	contact closure and TTL compatible "high" = 2.0V min, 7.0V max "low" = -0.6V min, 0.8V max
Isolation	None dc-coupled
Minimum Pulse Width	5 µs
Maximum Frequency	5 Hz
Specified Conditions	The instrument must be in the quiescent state, with no interval scans in process, no commands in the queue, no RS-232 or IEEE interface activity, and no front panel activity if the latency and repeatability performance is to be achieved. For additional information, refer to Section 5.
Maximum Latency	Latency is measured from the edge of the trigger input to the start of the first channel measurement for the Specified Conditions (above). 480 ms for fast rate, scanning DCV, ACV, ohms, and frequency only 550 ms for fast rate, scanning any thermocouple or 100 mV dc channels 440 ms for slow rate, scanning DCV, ACV, ohms, and frequency only 890 ms for slow rate, scanning any thermocouple or 100 mV dc channels
Repeatability	3 ms for the Specified Conditions (above)

Table 1-3. 2620A/2625A Specifications (cont)

Digital and Alarm Outputs	
Output Logic Levels	
Logical "zero":	0.8V max for an Iout of -1.0 mA (1 LSTTL load)
Logical "one":	3.8V min for an Iout of 0.05 mA (1 LSTTL load)
For non-TTL loads:	
Logical "zero":	1.8V max for an Iout of -20 mA 3.25V max for an Iout of -50 mA
Isolation	None
Real-Time Clock and Calendar	
Accuracy	Within 1 minute per month for 0°C to 50°C range
Battery Life	10 years minimum for Operating Temperature range
Environmental	
Warmup Time	1 hour to rated specifications 15 minutes when relative humidity is kept below 50% (non-condensing)
Operating Temperature	0°C to 60°C (32°F to 140°F)
Storage Temperature	-40°C to +75°C (-40°F to +167°F)
	Instrument storage at low temperature extremes may necessitate adding up to 0.008% to the dc voltage and ac voltage accuracy specifications. Alternatively, any resulting shift can be compensated for by recalibrating the instrument.
Relative Humidity (Non-Condensing)	90% maximum for 0°C to 28°C (32°F to 82.4°F), 75% maximum for 28°C to 35°C (82.4°F to 95°F), 50% maximum for 35°C to 60°C (95°F to 140°F), (Except 70% maximum for 0°C to 35°C (32°F to 95°F) for the 300 kΩ, 3 MΩ, and 10 MΩ ranges.)
Altitude	
Operating:	3,050m (10,000 ft) maximum
Non-operating:	12,200m (40,000 ft) maximum
Vibration	0.7g at 15 Hz 1.3g at 25 Hz 3g at 55 Hz
Shock	30g half sine per Mil-T-28800 Bench handling per Mil-T-28800
General	
Channel Capacity	21 Analog Inputs 4 Alarm Outputs 8 Digital I/O (Inputs/Outputs)
Measurement Speed	
Slow rate:	4 readings/second nominal
Fast rate:	17 readings/second nominal
1.5 readings/second nominal for ACV and high-Ω inputs For additional information, refer to Typical Scanning Rate and Maximum Autoranging Time.	

Table 1-3. 2620A/2625A Specifications (cont)

Memory Life	10 years minimum over Operating Temperature range Stores: real-time clock, set-up configuration, and measurement data
Common Mode Voltage	300V dc or ac rms maximum from any analog input(channel) to earth provided that channel to channel maximum voltage ratings are observed.
Voltage Ratings	Channels 0, 1, and 11 are rated at 300V dc or ac rms maximum from a channel terminal to earth and from a channel terminal to any other channel terminal. Channels 2 to 10 and 12 to 20 are rated at 150V dc or ac rms maximum from a channel terminal to any other channel terminal within channels 2 to 10 and 12 to 20.
Size	9.3 cm high, 21.6 cm wide, 31.2 cm deep (3.67 in high, 8.5 in wide, 12.28 in deep)
Weight	Net, 2.95 kg (6.5 lbs) Shipping, 4.0 kg (8.7 lbs)
Power	90 to 264V ac (no switching required), 50 and 60 Hz, 10 VA maximum 9V dc to 16V dc, 10W maximum If both sources are applied simultaneously, ac is used if it exceeds approximately 8.3 times dc. Automatic switchover occurs between ac and dc without interruption.(At 120V ac the equivalent dc voltage is ~14.5V.)
Standards	Complies with IEC 1010, UL 1244 and CSA Bulletin 556B. Complies with ANSI/ISA-S82.01-1988 and CSA C22.2 No. 231 when common mode voltages and channel 0, 1, and 11 inputs are restricted to 250V dc or ac rms maximum. Complies with VDE 0871B when shielded cables are used. Complies with FCC-15B, at the Class A level when shielded cables are used.
RS-232-C	
Connector:	9 pin male (DB-9P)
Signals:	TX, RX, DTR, GND
Modem Control:	full duplex
Baud rates:	300, 600, 1200, 2400, 4800, and 9600
Data format:	8 data bits, no parity bit, one stop bit, or 7 data bits, one parity bit (odd or even), one stop bit
Flow control:	XON/XOFF
Echo:	on/off
2625A Data Storage	
Storage	2047 Scans
Each scan includes:	• Time stamp • Readings for all defined analog input channels • Status of the four alarm outputs • Status of the eight digital I/O • Totalizer count
Memory	Battery-backed static RAM
Memory life:	5 years minimum at 25°C

Table 1-3. 2620A/2625A Specifications (cont)

2620A Options

IEEE-488 (Option -05K)

Capability codes:SH1, AH1, T5, L4, SR1, RL1, PP0, DC1, DT1, E1, TE0, LE0 and C0
Complies with IEEE-488.1 standard

Crosstalk Rejection

AC signals can have effects on other channels(crosstalk). These effects are discussed here by measurement function. These numbers should only be considered as references. Since crosstalk can be introduced into a measurement system in many places, each setup must be considered individually.

The effect of crosstalk could be much better than shown for "Typical"; in extreme cases, the effect could be worse than the "Worst Case" numbers.In general, the "Worst Case" information assumes that none of the guidelines for minimizing crosstalk(Section 5) have been followed; the "Typical" information assumes that the guidelines have been followed where reasonable.

These numbers assume that input L (low) is tied to earth ground; refer to "Using Shielded Wiring" in Section 5. For dc volts and thermocouple temperature measurements, a source impedance of 1 kΩ in series with the H (high) input is assumed (except where otherwise noted.)

AC Signal Crosstalk in a DC Voltage Channel

$$\text{DCV Error Tatio (CTRR)} = \left[\frac{VDC(error)}{VAC\,rms}\right]$$

Frequency	Worst case	Typical
50, 60 Hz, ±0.1%:	1.1×10^{-7}	2.0×10^{-8}
Other Frequencies:	3.8×10^{-6}	8.6×10^{-7}

For example, to find the typical effect of a 300V ac signal at 60 Hz on another channel for the 300 mV range, you would calculate: 300 X 2.0 X 10^{-8} = 0.01 mV.

AC Signal Crosstalk into an AC Voltage Channel

$$\text{ACV Error Ratio} = \left[\frac{VAC\,rms(error)}{VAC\,rms(crosstalk)\,x\,Frequency(crosstalk)}\right]$$

Range	Ratio (worst case)	Ratio (typical)
300.00 mV	$4.8 \times 10^{-8}\left[\frac{V}{V\,x\,Hz}\right]$	$1.4 \times 10^{-8}\left[\frac{V}{V\,x\,Hz}\right]$
3.0000V	$1.1 \times 10^{-7}\left[\frac{V}{V\,x\,Hz}\right]$	$3.0 \times 10^{-8}\left[\frac{V}{V\,x\,Hz}\right]$
30.000V	$1.2 \times 10^{-6}\left[\frac{V}{V\,x\,Hz}\right]$	$2.6 \times 10^{-7}\left[\frac{V}{V\,x\,Hz}\right]$
150.00/300.00V	$1.2 \times 10^{-5}\left[\frac{V}{V\,x\,Hz}\right]$	$3.4 \times 10^{-6}\left[\frac{V}{V\,x\,Hz}\right]$

For example, to find the typical effect of a 60 Hz, 220V ac signal on another channel for the the 300 mV range, you would calculate: 220 X 60 X 1.4 X 10^{-8} = 0.18 mV.

Table 1-3. 2620A/2625A Specifications (cont)

AC Signal Crosstalk into an Ohms Channel

AC Frequency = 50, 60 Hz, ±0.1%

OHMS Error Ratio = $\left[\frac{Ohmss(error)}{VACrms(crosstalk)}\right]$

Range	Ratio (worst case)	Ratio (typical)
300.00Ω	$3.3 \times 10^{-5} \left[\frac{Ohms}{VACrms}\right]$	No Effect
3.000 kΩ	$2.4 \times 10^{-6} \left[\frac{kOhms}{VACrms}\right]$	$6.7 \times 10^{-7} \left[\frac{kOhms}{VACrms}\right]$
30.000 kΩ	$3.1 \times 10^{-4} \left[\frac{kOhms}{VACrms}\right]$	$8.4 \times 10^{-5} \left[\frac{kOhms}{VACrms}\right]$
300.00 kΩ	$5.6 \times 10^{-3} \left[\frac{kOhms}{VACrms}\right]$	$3.7 \times 10^{-3} \left[\frac{kOhms}{VACrms}\right]$
3.0000 MΩ	$3.8 \times 10^{-4} \left[\frac{MOhms}{VACrms}\right]$	$3.8 \times 10^{-5} \left[\frac{MOhms}{VACrms}\right]$
10.000 MΩ	$1.4 \times 10^{-3} \left[\frac{MOhms}{VACrms}\right]$	$4.3 \times 10^{-4} \left[\frac{MOhms}{VACrms}\right]$

For example, to find the typical effect of a 60 Hz, 100V ac signal on another channel for the 30 kΩ range, you would calculate: 100 X 8.4 X 10^{-5} = 0.008 kΩ.

AC Signal Crosstalk into a Temperature Channel

Frequency = 50, 60 Hz

Temperature Error Ratio = $\left[\frac{°C(error)}{VACrms(crosstalk)}\right]$

Type	Worst case	Typical
Types J, K, E, T, N:	$2.7 \times 10^{-3} \left[\frac{°C}{VACrms}\right]$	$5.0 \times 10^{-4} \left[\frac{°C}{VACrms}\right]$
Types R, S, B, C:	$1.1 \times 10^{-2} \left[\frac{°C}{VACrms}\right]$	$2.0 \times 10^{-3} \left[\frac{°C}{VACrms}\right]$
Type PT (RTD):	$8.6 \times 10^{-5} \left[\frac{°C}{VACrms}\right]$	No Effect

AC Signal Crosstalk into a Frequency Channel

Frequency measurements are unaffected by crosstalk as long as the voltage-frequency product is kept below the following limits:

	Worst Case	Typical
V x Hz Product Limit	3.7×10^{4} (V x Hz)	1.0×10^{6} (V x Hz)

[1] These valkues assu;me no more than 1000 pF of capacitance between either end of the resistor (HI and LOW) and earth groung.

Table 1-4. 2635A Specifications

The instrument specifications presented here are applicable within the conditions listed in the Environmental portion of this specification.

The specifications state total instrument accuracy following calibration, including:

- A/D errors
- Linearization conformity
- Initial calibration errors
- Isothermality errors
- Relay thermal emf's
- Reference junction conformity
- Temperature coefficients
- Humidity errors

Sensor inaccuracies are not included in the accuracy figures.

Accuracies at Temperatures Other Than Specified

To determine typical accuracies at temperatures intermediate to those listed in the specification tables, linearly interpolate between the applicable 0°C to 60°C and 18°C to 28°C accuracy specifications.

Response Times

Refer to Typical Scanning Rate and Maximum Autoranging Time later in this table.

DC Voltage Inputs

Resolution		
Range	**Slow**	**Fast**
90 mV*	1 μV	10 μV
300 mV	10 μV	0.1 mV
3V	0.1 mV	1 mV
30V	1 mV	10 mV
150/300V	10 mV	0.1V
900V* **	10 μV	0.1 mV

Range	**Accuracy ±(% ±V)**				
	18°C to 28°C			**0°C to 60°C**	
	90 Days, Slow	**1 Year, Slow**	**1 Year, Fast**	**1 Year, Slow**	**1 Year, Fast**
90 mV*	0.29% + 7μV	0.034% + 7 μV	0.054% + 20 μV	0.074% + 7 μV	0.094% + 20 μV
300 mV	0.026% + 20 μV	0.031% + 20 μV	0.047% + 0.2 mV	0.070% + 20 μV	0.087% + 0.2 mV
3V	0.028% + 0.2 mV	0.033% + 0.2 mV	0.050% + 2 mV	0.072% + 0.2 mV	0.089% + 2 mV
30V	0.024% + 2 mV	0.029% + 2 mV	0.046% + 20 mV	0.090% + 2 mV	0.107% + 20 mV
150/300V	0.023% + 20 mV	0.028% + 20 mV	0.045% + 0.2V	0.090% + 20 mV	0.107% + 0.2V
900 mV	0.026% + 20 μV	0.031% + 21 μV	0.047% + 0.2 mV	0.070% + 20 μV	0.087% +0.2 mV

* Not used in Autoranging.
** Computer interface only (see FUNC command).

Table 1-4. 2635A Specifications (cont)

Input Impedance
100 MΩ minimum in parallel with 150 pF maximum for all ranges 3V and below 10 MΩ in parallel with 100 pF maximum for the 30V and 300V ranges.
Normal Mode Rejection
53 dB minimum at 60 Hz ±0.1%, slow rate 47 dB minimum at 50 Hz ±0.1%, slow rate
Common Mode Rejection
120 dB minimum at dc, 1 kΩ imbalance, slow rate 120 dB minimum at 50 or 60 Hz ±0.1%, 1 kΩ imbalance, slow rate
Maximum Input
300V dc or ac rms on any range for channels 0, 1, and 11 150V dc or ac rms for channels 2 to 10 and 12 to 20 Voltage ratings between channels must not be exceeded
Crosstalk Rejection
Refer to "Crosstalk Rejection" at the end of Table 1-3.

Table 1-4. 2635A Specifications (cont)

Thermocouple Inputs

Temperature Measurements - Accuracy (Thermocouples) (IPTS-68)

Thermocouple		Accuracy (±°C)*				
		18°C to 28°C			0°C to 60°C	
Type	Temperature (°C)	90 Days Slow	1 Year Slow	1 Year Fast	1 Year Slow	1 Year Fast
J	-100 to -30	0.44	0.45	0.87	0.54	1.05
	-30 to 150	0.40	0.42	0.78	0.58	1.00
	150 to 760	0.52	0.56	0.99	0.92	1.39
K	-100 to -25	0.53	0.54	1.08	0.64	1.27
	-25 to 120	0.46	0.47	0.92	0.63	1.14
	120 to 1000	0.94	1.00	1.66	1.54	2.27
	1000 to 1372	1.24	1.34	2.16	2.11	3.01
N	-100 to -25	0.65	0.66	1.39	0.75	1.57
	-25 to 120	0.57	0.58	1.20	0.70	1.37
	120 to 410	0.54	0.56	1.10	0.77	1.32
	410 to 1372	1.16	1.23	1.93	1.83	2.58
E	-100 to -25	0.44	0.46	0.86	0.55	1.05
	-25 to 350	0.43	0.45	0.76	0.66	1.02
	350 to 650	0.49	0.53	0.89	0.85	1.27
	650 to 1000	0.78	0.85	1.31	1.34	1.85
T	-150 to 0	0.72	0.73	1.46	0.83	1.68
	0 to 120	0.48	0.49	0.93	0.60	1.11
	120 to 400	0.45	0.48	0.82	0.68	1.07
R	250 to 400	1.02	1.04	2.54	1.17	2.71
	400 to 1000	1.09	1.13	2.37	1.49	2.71
	1000 to 1767	1.60	1.69	3.08	2.39	3.80
S	250 to 1000	1.19	1.24	2.70	1.26	3.00
	1000 to 1400	1.43	1.49	2.86	2.01	3.40
	1400 to 1767	1.78	1.88	3.48	2.61	4.25
B	600 to 1200	1.42	1.43	3.67	1.57	3.82
	1200 to 1550	1.36	1.40	2.70	1.78	3.09
	1550 to 1820	1.62	1.68	3.06	2.17	3.55
C	0 t 150	0.81	0.82	1.90	0.93	2.08
	150 to 650	0.81	0.85	1.71	1.16	2.07
	650 to 1000	1.05	1.11	2.10	1.59	2.63
	1000 to 1800	2.04	2.17	3.69	3.19	4.78
	1800 to 2316	3.29	3.51	5.87	5.26	7.72

* Sensor inaccuracies are not included.

Table 1-4. 2635A Specifications (cont)

Thermocouple Inputs

Temperature Measurements - Accuracy (Thermocouples) (ITS-90)

Thermocouple		Accuracy (±°C)*				
		18°C to 28°C			0°C to 60°C	
Type	Temperature (°C)	90 Days Slow	1 Year Slow	1 Year Fast	1 Year Slow	1 Year Fast
J	-100 to -30	0.44	0.45	0.88	0.54	1.06
	-30 to 150	0.41	0.43	0.79	0.59	1.01
	150 to 760	0.51	0.55	0.98	0.91	1.39
K	-100 to -25	0.54	0.55	1.10	0.65	1.28
	-25 to 120	0.47	0.49	0.94	0.65	1.16
	120 to 1000	0.75	0.82	1.47	1.35	2.08
	1000 to 1372	1.11	1.21	2.03	1.98	2.88
N	-100 to -25	0.66	0.67	1.41	0.77	1.58
	-25 to 120	0.57	0.58	1.20	0.69	1.37
	120 to 410	0.51	0.53	1.07	0.67	1.27
	410 to 1300	0.81	0.88	1.58	1.48	2.23
E	-100 to -25	0.46	0.47	0.87	0.57	1.06
	-25 to 350	0.40	0.41	0.75	0.62	0.98
	350 to 650	0.49	0.53	0.89	0.86	1.27
	650 to 1000	0.59	0.65	1.11	1.34	1.65
T	-150 to 0	0.70	0.72	1.45	0.82	1.67
	0 to 120	0.48	0.49	0.93	0.60	1.11
	120 to 400	0.40	0.43	0.78	0.63	1.02
R	250 to 400	0.96	0.98	2.48	1.13	2.66
	400 to 1000	0.92	0.94	2.32	1.27	2.54
	1000 to 1767	1.17	1.26	2.69	1.98	3.43
S	250 to 1000	1.01	1.03	2.61	1.39	2.80
	1000 to 1400	1.03	1.09	2.45	1.61	3.00
	1400 to 1767	1.32	1.41	3.06	2.17	3.85
B	600 to 1200	1.30	1.31	3.56	1.45	3.71
	1200 to 1550	0.90	0.94	2.32	1.31	2.62
	1550 to 1820	1.01	1.07	2.44	1.56	2.94
C	0 t 150	0.80	0.81	1.89	0.92	2.07
	150 to 650	0.71	0.75	1.62	1.06	1.97
	650 to 1000	0.86	0.92	1.90	1.39	2.43
	1000 to 1800	1.42	1.55	3.07	2.57	4.16
	1800 to 2316	2.34	2.56	4.92	4.32	6.78

* Sensor inaccuracies are not included.

Table 1-4. 2635A Specifications (cont)

Thermocouple Inputs (cont)

Input Impedance

100 MΩ minimum in parallel with 150 pF maximum

Common Mode and Normal Mode Rejection

See Specifications, DC Voltage Inputs

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of Table 1-3.

Open Thermocouple Detect

Small ac signal injection and detection scheme before each measurement detects greater than 1 to 4 kΩ as open. Performed on each channel unless defeated by computer command.

RTD Inputs

Type

DIN/IEC 751, 100Ω Platinum

RTD Temperature (°C)	1 Year, 4-Wire Accuracy (±°C)					
	Resolution		18°C to 28°C		0°C to 60°C	
	Slow	Fast	Slow	Fast	Slow	Fast
-200.00	0.02	0.01	0.08	0.49	0.12	0.54
0.00	0.02	0.01	0.21	0.67	0.50	0.96
100.00	0.02	0.01	0.27	0.75	0.69	1.17
300.00	0.02	0.01	0.41	0.92	1.10	1.60
600.00	0.02	0.01	0.65	1.21	1.77	2.33

2-Wire Accuracy

Not specified

Maximum Current Through Sensor

1 mA

Typical Full Scale Voltage

0.22V

Maximum Open Circuit Voltage

3.2V

Maximum Sensor Temperature

600°C nominal
999.99°F is the maximum that can be displayed when using °F.

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Table 1-4. 2635A Specifications (cont)

AC Voltage Inputs (True RMS AC Voltage, AC-Coupled Inputs)

Range	Resolution		Minimum Input for Rated Accuracy
	Slow	Fast	
300 mV	10 µV	100 µV	20 mV
3V	100 µV	1 mV	200 mV
30V	1 mV	10 mV	2V
150/300V	10 mV	100 mV	20V

1 Year Accuracy ±(%±V)

Frequency	18°C to 28°C		0°C to 60°C	
	SLow	Fast	Slow	Fast
300 mV Range				
20 Hz - 50 Hz	1.43% + 0.25 mV	1.43% + 0.4 mV	1.54% + 0.25 mV	1.54% + 0.4 mV
50 Hz - 100 Hz	0.30% + 0.25 mV	0.30% + 0.4 mV	0.41% + 0.25 mV	0.41% + 0.4 mV
100 Hz - 10 kHz	0.17% + 0.25 mV	0.17% + 0.4mV	0.28% + 0.25 mV	0.28% + 0.4 mV
10 kHz - 20 kHz	0.37% + 0.25 mV	0.37% + 0.4mV	0.68% + 0.25 mV	0.68% + 0.4 mV
20 kHz - 50 kHz	1.9% + 0.30 mV	1.9% + 0.5 mV	3.0% + 0.30 mV	3.0% + 0.5 mV
50 kHz - 100 kHz	5.0% + 0.50 mV	5.0% + 1.0 mV	7.0% + 0.50 mV	7.0% + 1.0 mV
3V Range				
20 Hz - 50 Hz	1.42% + 2.5 mV	1.42% + 4 mV	1.53% + 2.5 mV	1.53% + 4 mV
50 Hz - 100 Hz	0.29% + 2.5 mV	0.29% + 4 mV	0.40% + 2.5 mV	0.40% + 4 mV
100 Hz - 10 kHz	0.14% + 2.5 mV	0.14% + 4 mV	0.25% + 2.5 mV	0.25% + 4 mV
10 kHz - 20 kHz	0.22% + 2.5 mV	0.22% + 4 mV	0.35% + 2.5 mV	0.35% + 4 mV
20 kHz - 50 kHz	0.6% + 3.0 mV	0.6% + 5 mV	0.9% + 3.0 mV	0.9% + 5 mV
50 kHz - 100 kHz	1.0% + 5.0 mV	1.0% + 10 mV	1.4% + 5.0 mV	1.4% + 10 mV
30V Range				
20 Hz - 50 Hz	1.43% + 25 mV	1.43% + 40 mV	1.58% + 25 mV	1.58% + 40 mV
50 Hz - 100 Hz	0.29% + 25 mV	0.29% + 40 mV	0.45% + 25 mV	0.45% + 40 mV
100 Hz - 10 kHz	0.15% + 25 mV	0.15% + 40 mV	0.30% + 25 mV	0.30% + 40 mV
10 kHz - 20 kHz	0.22% + 25 mV	0.22% + 40 mV	0.40% + 25 mV	0.40% + 40 mV
20 kHz - 50 kHz	0.9% + 30 mV	0.9% + 50 mV	1.1% + 30 mV	1.1% + 50 mV
50 kHz - 100 kHz	2.0% + 50 mV	2.0% + 100 mV	2.2% + 50 mV	2.2% + 100 mV
300V Range				
20 Hz - 50 Hz	1.42% + 0.25V	1.42% + 0.4V	1.57% + 0.25V	1.57% + 0.4V
50 Hz - 100 Hz	0.29% + 0.25V	0.29% + 0.4V	0.44% + 0.25V	0.44% + 0.4V
100 Hz - 10 kHz	0.14% + 0.25V	0.14% + 0.4V	0.29% + 0.25V	0.29% + 0.4V
10 kHz - 20 kHz	0.22% + 0.25V	0.22% + 0.4V	0.38% + 0.25V	0.38% + 0.4V
20 kHz - 50 kHz	0.9% + 0.30V	0.9% + 0.5V	1.0% + 0.30V	1.0% + 0.5V
50 kHz - 100 kHz	2.5% + 0.50V	2.5% + 1.0V	2.6% + 0.50V	2.6% + 1.0V

Table 1-4. 2635A Specifications (cont)

AC Voltage Inputs (True RMS AC Voltage, AC-Coupled Inputs) (cont)

Maximum Frequency	Input at Upper Frequency
20 Hz - 50 Hz	300V rms
50 Hz - 100 Hz	300V rms
100 Hz - 10 kHz	200V rms
10 kHz - 20 kHz	100V rms
20 kHz - 50 kHz	40V rms
50 kHz - 100 kHz	20V rms

Input Impedance

1 MΩ in parallel with 100 pF maximum

Maximum Crest Factor

3.0 maximum
2.0 for rated accuracy

Crest Factor Error

Non-sinusoidal input signals with crest factors between 2 and 3 and pulse widths 100 μs and longer add 0.2% to the accuracy specifications.

Common Mode Rejection

80 dB minimum at 50 or 60 Hz ±0.1%, 1 kΩ imbalance, slow rate

Maximum AC Input

300V rms or 424V peak on channels 0, 1, and 11
150V rms or 212V peak on channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded

2×10^6 Volt-Hertz product on any range, normal mode input
1×10^6 Volt-Hertz product on any range, common mode input

DC Component Error

SCAN and first MONitor measurements will be incorrect if the dc signal component exceeds 60 counts in slow rate or 10 counts in fast rate. To measure ac with a dc component present, MONitor the input and wait 5 seconds before recording the measurement.

Using Channel 0

When measuring voltages above 100V rms, the rear Input Module must be installed to obtain the rated accuracy.

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of Table 1-3.

Table 1-4. 2635A Specifications (cont)

Ohms Input

Range	Resolution		Typical Full Scale Voltage	Maximum Current Through Unknown	Maximum Open Circuit Voltage
	Slow	Fast			
300Ω	10 mΩ	0.1Ω	0.22V	1 mA	3.2V
3 kΩ	0.1Ω	1Ω	0.25V	110 µA	1.5V
30 kΩ	1Ω	10Ω	0.29V	13 µA	1.5V
300 kΩ	10Ω	100Ω	0.68V	3.2 µA	3.2V
3 MΩ	100Ω	1 kΩ	2.25V	3.2 µA	3.2V
10 MΩ	1 kΩ	10 kΩ	2.72V	3.2 µA	3.2V

4-Wire Accuracy ±(% ± Ω)					
Range	18°C to 28°C			0°C to 60°C	
	90 Days, Slow	1 Year, Fast	1 Year, Fast	1 Year, Fast	1 Year, Fast
300Ω	0.056% + 20 mΩ	0.060% + 20 mΩ	0.060% + 0.2Ω	0.175% + 20 mΩ	0.175% + 0.2Ω
3 kΩ	0.053% + 0.2Ω	0.057% + 0.2Ω	0.057% + 2Ω	0.172% + 0.2Ω	0.172% + 2Ω
30 kΩ	0.055% + 2Ω	0.059% + 2Ω	0.059% + 20Ω	0.176% + 2Ω	0.176% + 20Ω
300 kΩ	0.053% + 20Ω	0.057% + 20Ω	0.057% + 200Ω	0.184% + 20Ω	0.184% + 200Ω
3 MΩ	0.059% + 200Ω	0.063% + 200Ω	0.063% + 2 kΩ	0.203% + 200Ω	0.203% + 2 kΩ
10 MΩ	0.115% + 2 kΩ	0.120% + 2 kΩ	0.200% + 30 kΩ	0.423% + 2 kΩ	0.423% + 30 kΩ

2-wire Accuracy

Not specified

Input Protection

300V dc or ac rms on all ranges

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of Table 1-3.

Frequency Inputs

Frequency Range

15 Hz to greater than 1 MHz

Range	Resolution		Accuracy ±(% ± Hz)	
	Slow	Fast	Slow	Fast
15 Hz - 900 Hz	0.01 Hz	0.1 Hz	0.05% + 0.02 Hz	0.05% + 0.2 Hz
9 kHz	0.1 Hz	1 Hz	0.05% + 0.1 Hz	0.05% + 1 Hz
90 kHz	1 Hz	10 Hz	0.05% + 1 Hz	0.05% + 10 Hz
900 kHz	10 Hz	100 Hz	0.05% + 10 Hz	0.05% + 100 Hz
1 MHz	100 Hz	1 Hz	0.05% + 100 Hz	0.05% + 1 kHz

Table 1-4. 2635A Specifications (cont)

Frequency Inputs (cont)

Sensitivity

Frequency	Level (sine Wave)
15 Hz - 100 kHz	100 mV rms
100 kHz - 300 kHz	150 mV rms
300 kHz - 1 MHz	2V rms
Above 1 MHz	NotSpecified

Maximum AC Input

300V rms or 424V peak on channels 0, 1, and 11
150V rms or 212V peak on channels 2 to 10 and 12 to 20
Voltage ratings between channels must not be exceeded

2×10^6 Volt-Hertz product on any range, normal mode input
1×10^6 Volt-Hertz product on any range, common mode input

Crosstalk Rejection

Refer to "Crosstalk Rejection" at the end of this table.

Typical Scanning Rate

Function	Range	Slow			Fast		
Channels:		1	10	20	1	10	20
VDC	300 mV	1.7	3.6	3.8	2.2	10.3	12.9
VDC	3V	1.7	3.6	3.8	2.2	10.3	12.9
VDC	30V	1.7	3.6	3.8	2.2	10.3	12.9
VDC	150/300V	1.7	3.5	3.8	2.2	10.2	12.8
VDC	AUTO	1.0	3.4	3.6	2.2	8.9	10.7
Temperature	J	1.5	3.1	3.5	1.9	9.5	12.1
Temperature	PT	1.0	2.5	2.6	1.7	4.2	4.5
VAC	300 mV	1.0	1.5	1.5	1.3	2.3	2.4
VAC	3V	1.0	1.5	1.5	1.3	2.3	2.4
VAC	30V	1.0	1.5	1.5	1.3	2.3	2.4
VAC	150/300V	1.0	1.5	1.5	1.3	2.3	2.4
VAC	AUTO	1.0	1.4	1.5	1.3	2.3	2.4
Ohms	300Ω	1.5	2.5	2.6	1.8	4.2	4.5
Ohms	3 kΩ	1.5	2.5	2.6	1.7	4.2	4.5
Ohms	30 kΩ	1.5	2.5	2.6	1.7	4.2	4.5
Ohms	300 kΩ	1.0	1.5	1.5	1.4	2.8	2.9
Ohms	3 MΩ	1.0	1.5	1.5	1.4	2.7	2.9
Ohms	10 MΩ	1.0	1.5	1.5	1.4	2.7	2.9
Ohms	AUTO	1.5	2.5	2.6	1.7	4.2	4.5
Frequency	any	0.5	0.6	0.7	0.6	0.7	0.7

Table 1-4. 2635A Specifications (cont)

Maximum Autoranging Time (Seconds per Channel)

Function	Range Change	Slow	Fast
VDC	300 mV to 150V	0.25	0.19
	150V to 300 mV	0.25	0.18
VAC	300 mV to 150V	1.40	1.10
	150V to 300 mV	1.40	1.10
Ohms	300Ω to 10.0 MΩ	1.70	0.75
	10.0 MΩ to 300Ω	1.50	0.60

Totalizing Inputs

Input Voltage	30V maximum -4V minimum 2V peak minimum signal
Isolation	None dc-coupled
Threshold	1.4V
Hysteresis	500 mV
Input Debouncing	None or 1.75 ms
Rate	0 to 5 kHz with debouncing off
Maximum Count	65,535

Digital Inputs

Input Voltage	30V maximum -4V minimum
Isolation	None dc-coupled
Threshold	1.4V
Hysteresis	500 mV

Trigger Inputs

Input Voltages	contact closure and TTL compatible "high" = 2.0V min, 7.0V max "low" = -0.6V min, 0.8V max
Isolation	None dc-coupled
Minimum Pulse Width	5 µs
Maximum Frequency	5 Hz
Specified Conditions	The instrument must be in the quiescent state, with no interval scans in process, no commands in the queue, no RS-232 or IEEE interface activity, and no front panel activity if the latency and repeatability performance is to be achieved. For additional information, refer to Section 5.
Maximum Latency	Latency is measured from the edge of the trigger input to the start of the first channel measurement for the Specified Conditions (above). 540 ms for fast rate, scanning DCV, ACV, ohms, and frequency only 610 ms for fast rate, scanning any thermocouple or 100 mV dc channels 500 ms for slow rate, scanning DCV, ACV, ohms, and frequency only 950 ms for slow rate, scanning any thermocouple or 100 mV dc channels
Repeatability	3 ms for the Specified Conditions (above)

Table 1-4. 2635A Specifications (cont)

Digital and Alarm Outputs	
Output Logic Levels	
Logical "zero":	0.8V max for an Iout of -1.0 mA (1 LSTTL load)
Logical "one":	3.8V min for an Iout of 0.05 mA (1 LSTTL load)
For non-TTL loads:	
Logical "zero":	1.8V max for an Iout of -20 mA 3.25V max for an Iout of -50 mA
Isolation	None
Real-Time Clock and Calendar	
Accuracy	Within 1 minute per month for 0°C to 50°C range
Battery Life	>10 unpowered instrument years for 0°C to 28°C (32°F to 82.4°F). >3 unpowered instrument years for 0°C to 50°C (32°F to 122°F). >2 unpowered instrument years for 50°C to 70°C (122°F to 158°F).
Environmental	
Warmup Time	1 hour to rated specifications 15 minutes when relative humidity is kept below 50% (non-condensing)
Operating Temperature	0°C to 60°C (32°F to 140°F)
Storage Temperature	-40°C to +70°C (-40°F to +158°F) Instrument storage at low temperature extremes may necessitate adding up to 0.008% to the dc voltage and ac voltage accuracy specifications. Alternatively, any resulting shift can be compensated for by recalibrating the instrument.
Relative Humidity (Non-Condensing)	90% maximum for 0°C to 28°C (32°F to 82.4°F), 75% maximum for 28°C to 35°C (82.4°F to 95°F), 50% maximum for 35°C to 60°C (95°F to 140°F), (Except 70% maximum for 0°C to 35°C (32°F to 95°F) for the 300 kΩ, 3 MΩ, and 10 MΩ ranges.)
Altitude	
Operating:	3,050m (10,000 ft) maximum
Non-operating:	12,200m (40,000 ft) maximum
Vibration	0.7g at 15 Hz 1.3g at 25 Hz 3g at 55 Hz
Shock	30g half sine per Mil-T-28800 Bench handling per Mil-T-28800

Table 1-4. 2635A Specifications (cont)

General	
Channel Capacity	21 Analog Inputs 4 Alarm Outputs 8 Digital I/O (Inputs/Outputs)
Measurement Speed	
Slow rate:	4 readings/second nominal
Fast rate:	17 readings/second nominal
1.5 readings/second nominal for ACV and high-Ω inputs For additional information, refer to Typical Scanning Rate and Maximum Autoranging Time.	
Nonvolatile Memory Life	>10 unpowered instrument years for 0°C to 28°C (32°F to 82.4°F). >3 unpowered instrument years for 0°C to 50°C (32°F to 122°F). >2 unpowered instrument years for 50°C to 70°C (122°F to 158°F).
Common Mode Voltage	300V dc or ac rms maximum from any analog input(channel) to earth provided that channel to channel maximum voltage ratings are observed.
Voltage Ratings	Channels 0, 1, and 11 are rated at 300V dc or ac rms maximum from a channel terminal to earth and from a channel terminal to any other channel terminal. Channels 2 to 10 and 12 to 20 are rated at 150V dc or ac rms maximum from a channel terminal to any other channel terminal within channels 2 to 10 and 12 to 20.
Size	9.3 cm high, 21.6 cm wide, 31.2 cm deep (3.67 in high, 8.5 in wide, 12.28 in deep)
Weight	Net, 2.95 kg (6.5 lbs) Shipping, 4.0 kg (8.7 lbs)
Power	90 to 264V ac (no switching required), 50 and 60 Hz, 10 VA maximum 9V dc to 16V dc, 10W maximum If both sources are applied simultaneously, ac is used if it exceeds approximately 8.3 times dc. Automatic switchover occurs between ac and dc without interruption.(At 120V ac the equivalent dc voltage is ~14.5V.)
Standards	Complies with IEC 1010, UL 1244 and CSA Bulletin 556B. Complies with ANSI/ISA-S82.01-1988 and CSA C22.2 No. 231 when common mode voltages and channel 0, 1, and 11 inputs are restricted to 250V dc or ac rms maximum. Complies with VDE 0871B when shielded cables are used. Complies with FCC-15B, at the Class A level when shielded cables are used.
RS-232-C	
Connector:	9 pin male (DB-9P)
Signals:	TX, RX, DTR, DSR, RTS, CTS, GND
Modem Control:	full duplex
Baud rates:	300, 600, 1200, 2400, 4800, 9600, 19200, AND 38400
Data format:	8 data bits, no parity bit, one stop bit, or 7 data bits, one parity bit (odd or even), one stop bit
Flow control:	XON/XOFF (Software) and CTS (Hardware)
Echo:	on/off

Chapter 2
Theory of Operation (2620A/2625A)

2-1. Introduction

The theory of operation begins with a general overview of the instrument and progresses to a detailed description of the circuits of each pca.

The instrument is first described in general terms with a Functional Block Description. Then, each block is detailed further (often to the component level) with Detailed Circuit Descriptions. Refer to Section 8 of this manual for full schematic diagrams. The Interconnect Diagram in this section (Figure 2-1) illustrates physical connections among pca's.

Signal names followed by a '*' are active (asserted) low. All other signals are active high.

2-2. Functional Block Description

Refer to Figure 2-2, Overall Functional Block Diagram, during the following functional block descriptions.

2-3. Main PCA Circuitry

The following paragraphs describe the major circuit blocks on the Main PCA.

2-4. Power Supply

The Power Supply functional block provides voltages required by the vacuum-fluorescent display (-30V dc, -5.0V dc, and filament voltage of 5.4V ac), the inguard circuitry (-5.4V dc VSS, +5.3V dc VDD, and +5.6V dc VDDR), and outguard digital circuitry of +5.1V dc (VCC).

Within the Power Supply, the Raw DC Supply converts ac line voltage to dc levels. The 5V Switching Supply converts this raw dc to 5.1V ±0.25V dc, which is used by the Inverter in generating the above-mentioned outputs. The Power Fail Detector monitors the Raw DC Supply and provides a power supply status signal to the Microprocessor in the Digital Kernel.

2-5. Digital Kernel

The Digital Kernel functional block is responsible for the coordination of all activities within the instrument. This block requires power supply voltages from the Power Supply and reset signals from the Display Assembly.

Specifically, the Digital Kernel Microprocessor performs the following functions:

- Executes the instructions in ROM.
- Stores temporary data in RAM.
- Stores instrument configuration and calibration data in nonvolatileRAM and EEPROM.
- Communicates with the microcontroller on the A/D Converter PCA viathe Serial Communication (Guard Crossing) block.
- Communicates with the Display Controller to display readings and userinterface information.
- Scans the user interface keyboard found on the Display Assembly.
- Communicates via the RS-232 interface and optional IEEE-488interfaces.
- Reads digital inputs and changes digital and alarm outputs.

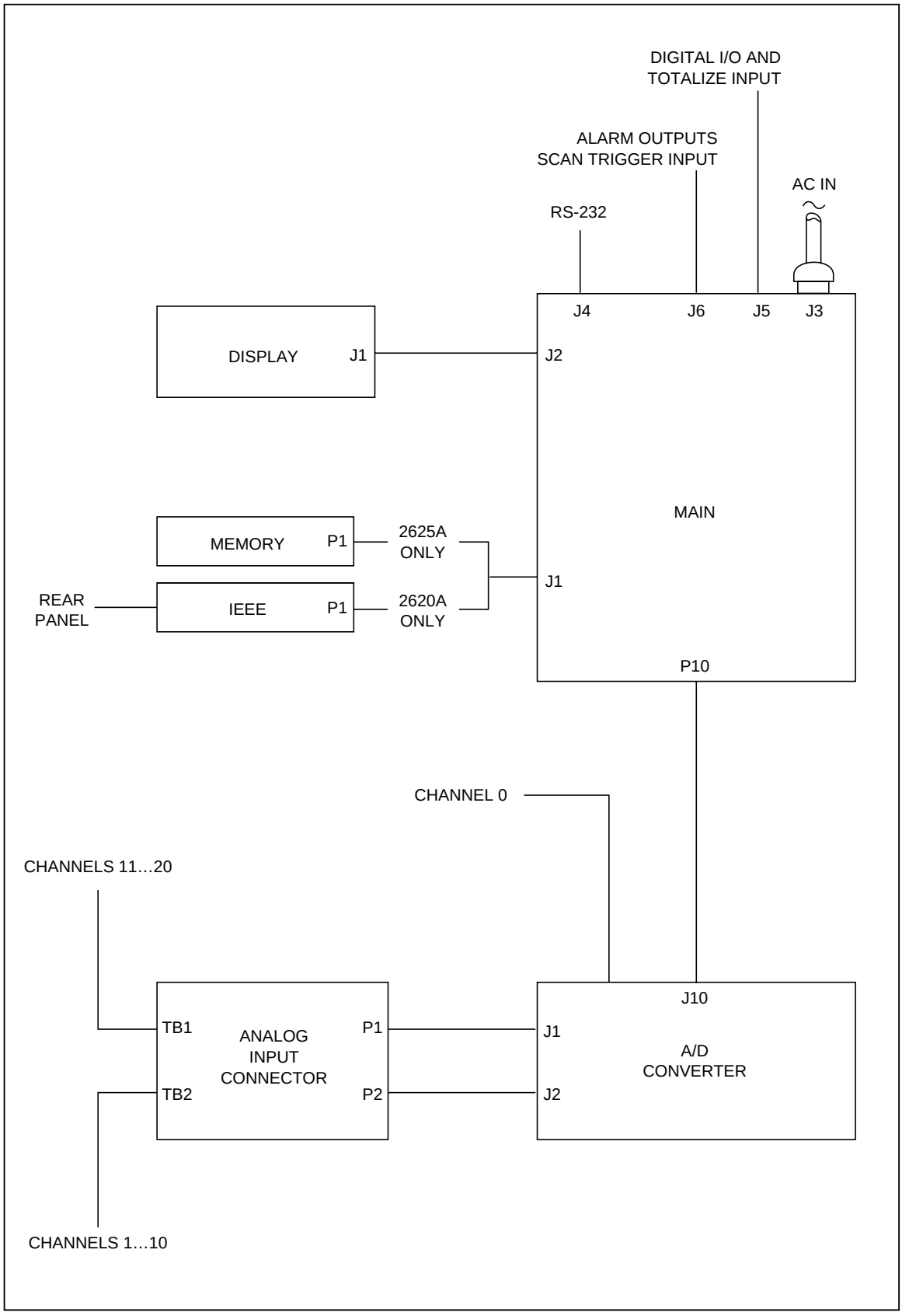
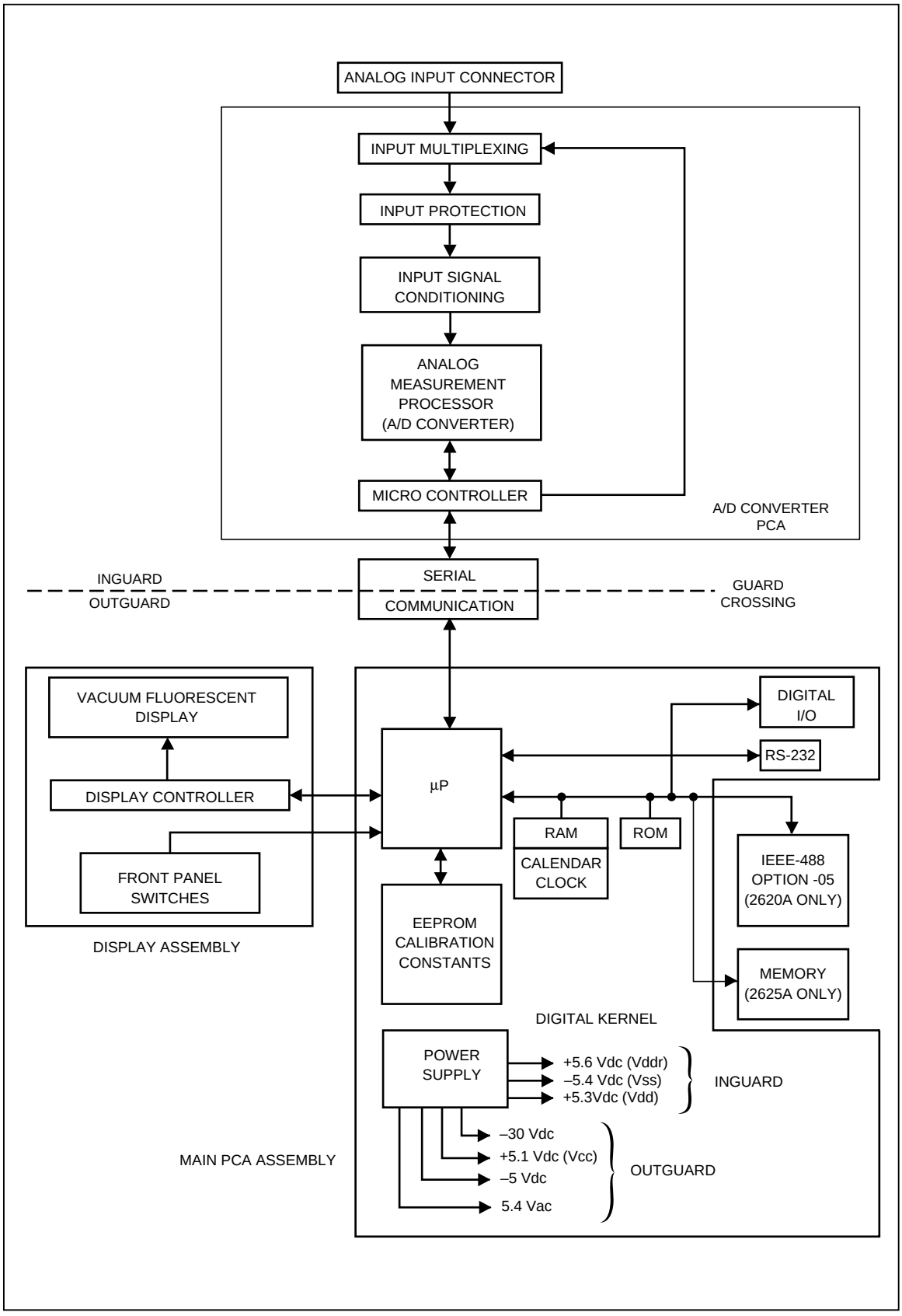


Figure 2-1. Interconnect Diagram



s2f.eps

Figure 2-2. Overall Functional Block Diagram

2-6. Serial Communication (Guard Crossing)

This functional block provides a high isolation voltage communication path between the Digital Kernel of the Main PCA and the microcontroller on the A/D Converter PCA. This bidirectional communication circuit requires power supply voltages from the Power Supply block.

2-7. Digital Inputs and Outputs

This functional block contains the Totalizer, Totalizer Debouncer, eight bidirectional Digital I/O channels, four Alarm Outputs, and the Input Threshold control circuits. These circuits require power supply voltages from the Power Supply, a reset signal from the Display PCA, and signals from the Digital Kernel.

2-8. A/D Converter PCA

The following paragraphs describe the major blocks of circuitry on the A/D Converter PCA.

2-9. Analog Measurement Processor

The Analog Measurement Processor (A3U8) provides input signal conditioning, ranging, a/d conversion, and frequency measurement. This custom chip is controlled by the A/D Microcontroller (A3U9). The A/D Microcontroller communicates with the Main PCA processor (A1U4) over a custom serial interface.

2-10. Input Protection Circuitry

This circuitry protects the instrument measurement circuits during overvoltage conditions.

2-11. Input Signal Conditioning

Here, each input is conditioned and/or scaled to a dc voltage for measurement by the a/d converter. DC voltage levels greater than 3V are attenuated. To measure resistance, a dc voltage is applied across a series connection of the input resistance and a reference resistance to develop dc voltages that can be ratioed. DC volts and ohms measurements are filtered by a passive filter. AC voltages are first scaled by an ac buffer, converted to a representative dc voltage by an rms converter, and then filtered by an active filter.

2-12. Analog-to-Digital (A/D) Converter

The dc voltage output from the signal conditioning circuits is applied to a buffer/integrator which charges a capacitor for an exact amount of time. The time required to discharge this capacitor, which is proportional to the level of the unknown input signal, is then measured by the digital counter circuits in the Analog Measurement Processor.

2-13. Inguard Microcontroller Circuitry

This microcontroller (and associated circuitry) controls all functions on the A/D Converter PCA and communicates with the digital kernel on the Main PCA. Upon request by the Main PCA, the inguard microcontroller selects the input channel to be measured through the channel selection circuitry, sets up the input signal conditioning, commands the Analog Measurement Processor to begin a conversion, stops the measurement, and then fetches the measurement result. The inguard microcontroller manipulates the result mathematically and transmits the reading to the digital kernel.

2-14. Channel Selection Circuitry

This circuitry consists of a set of relays and relay-control drivers. The relays form a tree that routes the input channels to the measurement circuitry. Two of the relays are also used to switch between 2-wire and 4-wire operation.

2-15. Open Thermocouple Check Circuitry

Under control of the Inguard Microcontroller, the open thermocouple check circuit applies a small ac signal to a thermocouple input before each measurement. If an excessive resistance is encountered, an open thermocouple input condition is reported.

2-16. Input Connector Assembly

The following paragraphs briefly describe the major sections of the Input Connector PCA, which is used for connecting most of the analog inputs to the instrument.

2-17. 20 Channel Terminals

Twenty HI and LO terminal blocks are provided in two rows, one for channels 1 through 10 and one for channels 11 through 20. The terminals can accommodate a wide range of wire sizes. The two rows of terminal blocks are maintained very close to the same temperature for accurate thermocouple measurements.

2-18. Reference Junction Temperature

A semiconductor junction is used to sense the temperature of the thermocouple input terminals. The resulting dc output voltage is proportional to the block temperature and is sent to the A/D Converter PCA for measurement.

2-19. Display PCA

The Display Assembly controller communicates with the main Microprocessor over a three-wire communication channel. Commands from the Microprocessor inform the Display Controller how to modify its internal display memory. The Display Controller then drives the grid and anode signals to illuminate the required segments on the Display. The A2 Display Assembly requires power supply voltages from the Power Supply and a clock signal from the A1U4 Microprocessor.

2-20. Memory PCA (2625A Only)

The Memory PCA is used by the Digital Kernel to store nonvolatile measurement data. This block requires power supply voltages from the Power Supply, a reset signal from the Display PCA, and signals from the Digital Kernel.

2-21. IEEE-488 Option (-05)

Theory of operation for the IEEE-488 Option (-05) is presented in Section 7 of this manual. The related schematic diagram is found in Section 8.

2-22. Detailed Circuit Description

2-23. Main PCA

The following paragraphs describe the operation of the circuits on the Main PCA. The schematic for this pca is located in Section 8.

2-24. Power Supply Circuit Description

The Hydra power supply consists of three major sections:

- Raw DC Supply

  The raw dc supply converts line voltage (90V to 264V ac) to a dcoutput of 7.5V to 35V.

- 5V Switcher Supply

  The 5V switching supply regulates the 7.5 to 35V dc input to anominal 5.1V ±0.25V dc (VCC).

- Inverter

  Using the 5V switching supply output, the inverter generates the -30Vdc, -5V dc, and 5.4V ac supply levels needed for thevacuum-fluorescent display and the RS-232 Interface. The inverteralso provides isolated +5.3V (VDD), +5.6V (VDDR), and -5.4V (VSS)outputs for the inguard circuitry.

2-25. Raw DC Supply

The raw dc supply circuitry receives input from power transformer T401, which operates on an input ranging from 90V to 264V ac. The power transformer is energized whenever the power cord is plugged into the ac line; there is no on/off switch on the primary side of the transformer. The transformer has an internal 275V ac metal-oxide varistor (MOV) to clamp line transients. The MOV normally acts as an open circuit. When the peak voltage exceeds approximately 400V, the line impedance in series with the line fuse limits transients to approximately 450V. All line voltages use a slow blow 0.125 A, 250V fuse.

On the secondary side of the transformer, rectifiers A1CR2, A1CR3, and capacitor A1C7 rectify and filter the output. When it is ON, switch A1S1 (the front panel POWER switch) connects the output of the rectifiers to the filter capacitor and the rest of the instrument. Depending on line voltage, the output of the rectifiers is between 7.5 and 35V dc. Capacitor A1C2 helps to meet electromagnetic interference (EMI) and electromagnetic compatibility (EMC) requirements.

When external dc power is used, the power switch connects the external dc source to power the instrument. The external dc input uses thermistor A1RT1 (for overcurrent protection) and diode A1CR1 (for reverse input voltage protection.) Capacitor A1C59 helps meet EMI/EMC requirements. Resistor A1R48, capacitors A1C2 and A1C39 also ensure that the instrument meets EMI/EMC performance requirements.

2-26. Auxiliary 6V Supply

Three-terminal regulator A1U19, voltage-setting resistors A1R44 and A1R46, and capacitor A1C34 make up the auxiliary 6-volt supply. This supply is used for the inverter oscillator, inverter driver, and the power fail detection circuits.

2-27. 5V Switcher

The 5V switcher supply uses a switcher supply controller/switch device A1U9 and related circuitry.The 7.5V dc to35V dc input is regulated to 5.1V dc (VCC) through pulse-width modulation at a nominal switching frequency of 100 kHz.

The output voltage of the switcher supply is controlled by varying the duty cycle (ON time) of the switching transistor in the controller/switch device A1U9. A1U9 contains the supply reference, oscillator, switch transistor, pulse-width modulator comparator, switch drive circuit, current-limit comparator, current-limit reference, and thermal limit.

Dual inductor A1T2 regulates the current that flows from the raw supply to the load as the switching transistor in A1U9 is turned on and off. Complementary switch A1CR10 conducts when the switching transistor is off.

The pulse-width modulator comparator in A1U9 compares the output to the reference and sets the ON-time/OFF-time ratio to regulate the output to 5.1V dc. A1C26 is the input filter capacitor, and A1C14 is the output filter capacitor. Proper inductor and capacitor values set the filter frequency response to ensure best overall system stability. Circuitry consisting of A1R26, A1C21, and A1C18 ensure that the switcher supply remains stable and operating in the continuous mode. Resistors A1R30 and A1R31 set the output voltage to within 5% of 5.1V.Capacitor A1C21 sets the operating frequency of the switcher at approximately 100 kHz.

Resistors A1R30 and A1R31 form a voltage divider that operates in conjunction with amplifier A1U31, which is configured as a voltage follower.A1U31-5 samples the 5.1V dc output, while A1U31-6 is the voltage divider input.The effect is to maintain the junction of R30 and R31 at 5.1V dc, resulting in an A1U31-7 output level of 6.34V dc, or 1.24V dc above the output.This feedback voltage is applied to A1U9-2, which A1U9 interprets as 1.24V dc because A1U9-3 (ground) is connected to the 5.1V dc output.

2-28. Inverter

The inverter supply uses a two transistor driven push-pull configuration. The center tap of transformer A1T1 primary is connected to the 5.1V dc VCC supply, and each side is alternately connected to common through transistors A1Q7 and A1Q8. A1R38 may be removed to disable the inverter supply for troubleshooting purposes. A1Q7 and A1Q8 are driven by the outputs of D flip-flop A1U22. Resistors A1R34 and A1R28, and diodes A1CR11 and A1CR12 shape the input drive signals to properly drive the gate of the transistors. D flip-flop A1U22 is wired as a divide-by-two counter driven by a 110-kHz square wave. The 110-kHz square wave is generated by hex inverter A1U23, which is connected as an oscillator with a frequency determined by the values of resistors A1R40 and A1R47 and capacitor A1C35. The resulting ac voltage produced across the secondary of A1T1 is rectified to provide the input to the inverter inguard and outguard supplies.

2-29. Inverter Outguard Supply

The inverter outguard supply provides three outputs: 5.4V ac, -30V dc, and -5V dc. These voltages are required by the display and RS-232 drivers and receiver. The 5.4V ac supply comes off the secondary windings (pins 6 and 7) on transformer T1, and it is biased at -24V dc with zener diode A1VR3 and resistor A1R22. Dual diodes A1CR8 and A1CR9 and capacitor A1C17 are for the -30V dc supply. Capacitors A1C30 and A1C31, and dual diodes A1CR13 form a voltage doubler circuit that generates -12 volts. Three-terminal regulator A1U18 then regulates this voltage down to -5V for the RS-232 circuit. Capacitor A1C32 is needed for transient response performance of the three-terminal regulator.

2-30. Inverter Inguard Supply

The inverter inguard supply provides three outputs: +5.3V dc (VDD) and -5.4V dc (VSS) for the inguard analog and digital circuitry, and +5.6V dc (VDDR) for the relays. Diodes A1CR5 and A1CR6, and capacitor A1C12 are for the +9.5 volt source, and diodes A1CR7 and capacitor A1C13 are for the -9.5V source.

Three-terminal regulator A1U6 regulates the 9.5V source to 5.6V for the relays. A1R5 and A1R6 set the output voltage at 5.6V. A1C6 is required for transient performance. The +5.3V regulator circuit uses A1Q2 for the series-pass element and A1Q4 as the error

amplifier. A1VR2 is the reference for the positive supply. A1R14 provides the current to bias the reference zener. A1C4 is the output filter, and A1C9 provides frequency compensation of the regulator circuit. Transistor A1Q1 and resistor A1R13 make up the current-limit circuit.

When the voltage across A1R13 increases enough to turn on A1Q1, output current is limited by removing the base drive to A1Q2.

The -5.4 volt regulator operates like the +5.3 volt regulator, except that the NPN transistors in the positive supply are PNP transistors in the negative supply, and the PNP transistors in the positive supply are NPN transistors in the negative supply. If a VDD-to-VSS short circuit occurs, diode A1CR4 ensures that current limit occurs at the limit set for the -5.4V dc or +5.3V dc supply, whichever is lower.

2-31. Power Fail Detection

The power fail detection circuit generates a signal to warn the Microprocessor that the power supply is going down. Comparator A1U24 compares the divided-down raw supply voltage and the band-gap generated reference voltage. When the raw supply voltage is greater than about 8V dc, the output of A1U24 is "high" and when the raw supply falls below 8V dc, the output goes "low". Resistors A1R39 and A1R41 make up the divider, and resistor A1R43 provides bias for the band-gap reference. Resistor A1R42 is a pull up resistor for the comparator output, and resistor A1R45 provides positive feedback to provide the comparator with some hysteresis.

2-32. Digital Kernel

The Digital Kernel is composed of the following eight functional circuit blocks: the Microprocessor, the ROM (Read-Only Memory), the NVRAM/Clock (Nonvolatile Random Access Memory and Real-Time Clock), the EEPROM (Electrically Erasable Programmable Read-Only Memory), the Counter/Timer, the RS-232 Interface, and the Option Interface.

2-33. Microprocessor

The Microprocessor uses an eight-bit data bus and a sixteen-bit address bus to access memory locations in the ROM (A1U8), the NVRAM/Clock (A1U3), the Counter/Timer (A1U2), the Digital I/O Registers (A1U13, A1U16, A1U26), the Memory PCA (A6), and the IEEE-488 PCA (A5).

The Microprocessor oscillator operates at a 4.9152-MHz frequency determined by crystal A1Y1. The A1U4-68 system clock signal (the Microprocessor oscillator frequency divided by four) is a square wave with a frequency of 1.2288 MHz. This system clock also determines the memory cycle time of 0.813 microseconds. The system clock is also used by the Display Assembly and the IEEE-488 option assembly after being damped by series resistor A1R19 to minimize the EMI generated by this signal's sharp edges.

When the address bus is stable, the Microprocessor enables either the reading of memory (by driving RD*, A1U4-67, low) or writing of memory (by driving WR*, A1U4-66, low.)

The Microprocessor uses a three-wire synchronous communication interface to store and retrieve instrument communication configuration and calibration information in the EEPROM (A1U1). See the EEPROM description for more detailed information.

The Microprocessor communicates to the Display Controller using another synchronous, three-wire communication interface described in detail in the Display Controller Theory of Operation in this section.

The Microprocessor communicates to the Microcontroller on the A/D Converter PCA (via the Serial Communication circuit) using an asynchronous communication protocol at 4800 baud. Communication to the Microcontroller (A3U9) originates at A1U4-11. Communication from the A/D's Microcontroller to the Microprocessor appears at A1U4-10. When there is no communication in progress between the Microprocessor and the Microcontroller, both of these signals are low.

2-34. Address Decoding

The upper three bits of the address bus are decoded by A1U10-3,4,5 to generate the ROM* chip select signal for the ROM (A1U10-6).

The NVRAM/Clock chip select signal (A1U21-6 going low) is generated when the ROM* and RESET* signals are high and any one of address bits 9 through 12 is high. To avoid spurious write cycles during power cycling, the INT* output of the NVRAM (A1U3-1) is used to discharge the reset circuit on the Display PCA through resistor A1R63 when the power supply level at A1U3-28 is too low (less than approximately 4.65V dc) to allow memory operations to the NVRAM.

The miscellaneous I/O chip select (hexadecimal addresses 0000 through 01FF) is decoded using the ROM* signal and address bits 9 through 12 by A1U15 and A1U21. When ROM* is high and all four of the address bits are low, the I/O* signal (A1U21-8) is low. The I/O* signal and address bits 3 through 8 are then used by A1U10 and A1U11 to generate the CNTR*, DIO*, IEEE*, and MEM* chip select signals.

Table 2-1 shows a memory map for the Microprocessor.

Table 2-1. Microprocessor Memory Map

Hexadecimal Address	Device Selected
2000 - FFFF	ROM (A1U8)
1FF8 - 1FFF	Real-Time Clock (A1U3)
0200 - 1FF7	NVRAM (A1U3)
0040 - 013F	Microprocessor Internal RAM
0038 - 003F	Counter/Timer (A1U2)
0032 (Read Only)	Digital Inputs (A1U13)
0032 (Write Only)	Digital Outputs (A1U26)
0035 (Write Only)	Alarm Outputs (A1U16)
0028 - 002F	IEEE-488 Option (2620A Only)
0005 - 0006 (Write Only)	Memory Page (2625A Only)
0004	Memory Data (2625A Only)

2-35. Serial Communication (Guard Crossing)

The transmission of information from the Microprocessor (A1U4) to the Microcontroller (A3U9) is accomplished via the circuit made up of A1U15, A1U7, A1R8, A1R16, and A3R8. The transmit output from the Microprocessor (A1U4-11) is inverted by A1U15, which drives the optocoupler LED (A1U7-2). Resistor A1R8 limits the current through the LED.

The phototransistor in A1U7 responds to the light emitted by the LED when A1U7-2 is driven low (the collector of the phototransistor (A1U7-5) goes low.) The phototransistor collector is pulled up by A3R8 on the A/D Converter PCA. When turning off, the

phototransistor base discharges through A1R16. With this arrangement, the rise and fall times of the phototransistor collector signal are nearly symmetrical.

The transmission of data from the Microcontroller (A3U9) to the Microprocessor (A1U4) is accomplished via the circuit made up of A3Q1, A3R7, A1U5, A1R7, and A1R3. The transmit output from the Microcontroller (A3U9-14) is inverted by A3Q1, which drives the optocoupler LED (A1U5-2) through resistor A3R7. The current through the LED is limited by resistor A3R7. The phototransistor in A1U5 responds to the light emitted by the LED when A1U5-2 is driven low; the emitter of the phototransistor (A1U5-4) goes high. The phototransistor collector (A1U5-5) is pulled up by VCC, and the emitter is pulled down by resistor A1R3. When turning off, the phototransistor base discharges through A1R7. With this arrangement, the rise and fall times of the phototransistor collector signal are nearly symmetrical.

2-36. Display/Keyboard Interface

The Microcontroller sends information to the Display Processor via a three-wire synchronous communication interface. The detailed description of the DISTX, DISRX, and DSCLK signals may be found in the detailed description of the Display PCA. Note that the DISRX signal is pulled down by resistor A1R1 so that Microprocessor input A1U4-15 is not floating at any time. The Display PCA also provides the system reset circuitry and watchdog timer.

The Keyboard interface is made up of six bidirectional port lines from the Microcontroller. SWR1 through SWR6 (A1U4-21 through A1U4-26, respectively) are pulled up by A2Z1 on the Display PCA. The detailed description of the Display PCA describes how the Microprocessor interfaces to the Keyboard.

2-37. ROM

The ROM provides the instruction storage for the Microprocessor. The chip select for this device (A1U8-20) goes low for any memory cycle between hexadecimal addresses 2000 and FFFF (accessing 56 kbytes). Whenever this device is chip selected for read, the instruction in the addressed location is output to the data bus and read by the Microprocessor.

2-38. NVRAM/Clock

The NVRAM/Clock (A1U3) provides the data storage and real-time clock for the instrument. A lithium battery, a crystal, and an automatic power-fail control circuit are also integrated into this single package. When the RAM* chip select signal (A1U3-20) is low, the Microprocessor is accessing one of the 8192 bytes in the NVRAM/Clock. The RD* (A1U3-22) and WR* (A1U3-27) signals go low to indicate a read or write cycle, respectively.

The internal power-fail control circuit disables access to this device and drives the INT* output (A1U3-1) low when the VCC power supply is below approximately +4.5V dc. This action keeps locations in the NVRAM/Clock from being modified while the instrument is powering up and down. When the INT* output is low, the reset circuit on the Display PCA is discharged, and a system reset occurs. Therefore, the Microprocessor is reset on power failure as soon as it can no longer access the NVRAM/Clock.

The NVRAM contains 8184 bytes of nonvolatile data storage. The nonvolatile instrument configuration information, the nonvolatile measurement data, and the Microprocessor temporary data are stored in this area.

The Clock is composed of 8-byte wide registers that allow access to the real-time clock counters. The Microprocessor accesses these registers in the same way as the NVRAM.

2-39. EEPROM

The EEPROM contains 64 registers, each of which is 16 bits long. These registers are used to provide nonvolatile storage of some of the instrument configuration information and all of the calibration information. When the Microprocessor is communicating to the EEPROM, Chip Select input (A1U1-1) is driven high to enable the EEPROM interface.

When the Microprocessor is reading data from the EEPROM, the data bits are serially shifted out on the Data Out signal (A1U1-4) with each one-to-zero transition of the Serial Clock (A1U1-2).

When the Microprocessor is writing commands and data to the EEPROM, the bits are serially shifted into the EEPROM on the Data In signal (A1U1-3) with each zero-to-one transition of the Serial Clock (A1U1-2). When the last data bit for an erase or write operation is shifted into the EEPROM, the Microprocessor pulses the Chip Select input (A1U1-1) low to start the operation. The EEPROM will then drive the Data Out signal (A1U1-4) low to indicate that it is busy writing the register. The Data Out signal goes high when the operation is complete. Since the Microprocessor waits for this signal to go high before doing anything else, an EEPROM failing to drive this signal high causes the Microprocessor to wait until the Watchdog Timer on the Display PCA resets the instrument.

The Chip Select input (A1U1-1) is always set low at the end of each EEPROM operation.

2-40. Counter/Timer

The Counter/Timer IC (A1U2) has three 16-bit counters that are used both to implement the Totalizer function and to provide a periodic 50-millisecond interrupt used for interval time operation.

The output from the Totalizer Input circuit (A1U28-3) provides the clock input for Counter 2. Counter 2 operates as a 16-bit pre-loadable down counter for the Totalizer function. This counter causes the IRQ1* interrupt (A1U2-9) to go low, interrupting the Microprocessor when the counter value changes from hexadecimal 0000 to FFFF. The Counter 2 Gate input (A1U2-2) must be low for the Totalizer to operate correctly.

Counter 3 is used as a periodic 50.0-millisecond interrupt source. This counter divides the E clock input (A1U2-17) by 61440. The IRQ1* interrupt (A1U2-9) goes low (interrupting the Microprocessor) at the end of each 50.0-millisecond period. The Counter 3 Gate input (A1U2-5) and the Counter 3 Clock input (A1U2-7) should both be low for this counter to operate correctly. The 10-Hz square wave signal observed on the Counter 3 Output pin (A1U2-6) changes state every 50.0 milliseconds.

Counter 1 is not used in the instrument, but its Clock and Output pins have been connected to available pins on the Option Interface.

2-41. RS-232 Interface

The RS-232 interface is composed of connector A1J4, RS-232 Driver/Receiver A1U25, and the hardware serial communication interface (SCI) in Microprocessor A1U4.

The SCI transmit signal (A1U4-14) goes to the RS-232 driver (A1U25-12), where it is inverted and level shifted so that the RS-232 transmit signal transitions between approximately +5.0 and -5.0V dc. When the instrument is not transmitting, the driver output A1U25-5 is approximately -5.0V dc. The RS-232 receive signal from A1J4 goes to the RS-232 receiver A1U25-4, which inverts and level shifts the signal so that the input to the SCI transitions between 0 and +5.0V dc. When nothing is being transmitted to the instrument, the receiver output (A1U25-13) is +5.0V dc.

Data Terminal Ready (DTR) is a modem control signal controlled by the Microprocessor. When the instrument is powered up, the Microprocessor port pin (A1U4-32) goes high, which results in the RS-232 driver output (A1U25-7) going to -5.0V dc. When the instrument has initialized the SCI and is ready to receive and transmit, A1U4-32 will go low, resulting in the RS-232 DTR signal (A1U25-7) going to +5.0V dc. The RS-232 DTR signal remains at +5.0V dc until the instrument is powered down.

2-42. Option Interface

The interconnection to the option slot is implemented by J1 on the Main PCA. This connector (A1J1) routes the outguard logic power supply (VCC and GND), the eight-bit data bus, RD*, WR*, E, RESET*, IEEE*, MEM*, and the lower three bits of the address bus to the option installed in the option slot. This connector also routes an interrupt signal from the IEEE-488 option to the IRQ2* input of the Microprocessor.

An option sense signal from the installed option allows the Microprocessor to identify the type of option. When the instrument is powered up, the type of PCA installed in the option slot is determined by the Microprocessor by driving the IRQ2* signal (A1U4-20) and sensing the activity on the OPS* signal (A1U4-29). The Microprocessor first sets IRQ2* low and samples the OPS* input, then sets IRQ2* high and samples the OPS* input again. Table 2-2 describes how this information is used to determine what hardware is installed in the option slot.

Table 2-2. Option Type Sensing

IRQ2* Output	State of *OPS Input for PCA:		
	None Installed	IEEE-488	Memory
0	1	0	0
1	1	0	1

2-43. Digital I/O

The following paragraphs describe the Digital Input Threshold, Digital Input Buffers, Digital and Alarm Output Drivers, Totalizer Input, and External Trigger Input circuits.

2-44. Digital Input Threshold *2-1.*

The Digital Input Threshold circuit sets the input threshold level for the Digital Input Buffers and the Totalizer Input. A software programmable voltage divider (A1U17, A1R35, A1R36, A1R37) and a unity gain buffer amplifier (A1AR1) are the main components in this circuit. The Microprocessor sets outputs A1U16-15 and A1U16-12 to select one of four input threshold levels. These outputs control the resistive divider (A1R35, A1R36, A1R37) via two drivers with open-collector outputs in A1U17. The voltage from the divider is then buffered by A1AR1 which sets the input threshold. Capacitor A1C29 filters the divider voltage at the input of A1AR1. Table 2-3 defines the programmable input threshold levels.

The instrument selects the +1.4V dc threshold level at power-up initialization.

Table 2-3. Programmable Input Threshold Levels

A1U16-15	A1U16-12	Input Threshold Voltage
0	0	+2.5V dc
0	1	+0.7V dc
1	0	+1.4V dc
1	1	+0.7V dc

2-45. Digital Input Buffers

Since the eight Digital Input Buffers are identical in design, only components used for Digital Input 0 are referenced in this description. If the Digital Output Driver (A1U27-16) is off, the input to the Digital Input Buffer is determined by the voltage level at A1J5-10. If the Digital Output Driver is on, the input of the Digital Input Buffer is the voltage at the output of the Digital Output Driver.

The Digital Input Threshold circuit and resistor network A1Z1 determine the input threshold voltage and hysteresis for inverting comparator A1AR2. The inverting input of the comparator (A1AR2-2) is protected by a series resistor (A1Z3) and diode A1CR14. A negative input clamp circuit (A1Q9, A1Z2, and A1CR17) sets a clamp voltage of approximately +0.7V dc for the protection diodes of all Digital Input Buffers. A negative input voltage at A1J5-10 causes A1CR14 to conduct current, clamping the comparator input A1AR2-2 at approximately 0V dc.

The input threshold of +1.4V dc and a hysteresis of +0.5V dc are used for all Digital Input Buffers. When the input of the Digital Input Buffer is greater than approximately +1.65V dc, the output of the inverting comparator is low. When the input then drops below about +1.15V dc, the output of the inverting comparator goes high.

2-46. Digital and Alarm Output Drivers

Since the 12 Digital Output and Alarm Output Drivers are identical in design, the following example description references only the components that are used for Alarm Output Driver 0.

The Microprocessor controls the state of Alarm Output Driver 0 by writing to latch output A1U16-2. When A1U16-2 is set high, the output of the open-collector Darlington driver (A1U17-15) sinks current through current limiting resistor A1R62. When A1U16-2 is set low, the driver output turns off and is pulled up by A1Z2 and/or the voltage of the external device that the output is driving. If the driver output is driving an external inductive load, the internal flyback diode (A1U17-9) conducts the energy into MOV A1RV1 to keep the driver output from being damaged by excessive voltage. Capacitor A1C58 ensures that the instrument meets electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance requirements.

2-47. Totalizer Input

The Totalizer Input circuit consists of Input Protection, a Digital Input Buffer circuit, and a Totalizer Debouncer circuit. The Digital Input Buffer for the totalizer is protected from electrostatic discharge (ESD) damage by A1R49 and A1C43. Refer to the detailed description of the Digital Input Buffer circuit for more information.

The Totalizer Debounce circuit allows the Microprocessor to select totalizing of either the input signal or the debounced input signal. Latch output A1U16-16 is set low by A1U4 to totalize the unmodified input signal or high to totalize the debounced input signal. This totalizer clock control is provided by A1U28; output A1U28-3 drives the totalizer counter clock input (A1U2-4).

The actual debouncing of the input signal is accomplished by A1U14, A1U20, and A1U29. An EXOR gate compares the input signal (A1U14-13) and the output of an eight-bit shift register (A1U29-9). If these signals differ, EXOR gate output A1U14-11 goes high, enabling counter A1U20 and shift register A1U29. The counter divides the system clock of 1.2288 MHz (A1U20-10) by 256 to yield a 4.8-kHz clock (A1U20-13). This signal clocks the eight-bit shift register. After approximately 1.5625 milliseconds, the input signal will have been shifted from the serial input (A1U29-10) through to the eighth output bit (A1U29-9). This forces the counter and shift register to stop. If the input signal changes state before 1.5625 milliseconds have elapsed, the counter is cleared and the shift register is preloaded again. Therefore, the input signal must remain stable for greater than 1.5625 milliseconds before that transition changes the state of the clock input of the totalizer counter (A1U2-4).

2-48. External Trigger Input Circuits

The External Trigger Input circuit can be configured by the Microprocessor to interrupt on a rising or falling edge of the XT* input (A1J6-2) or to not interrupt on any transitions of the XT* input.

The Microprocessor sets latch output A1U16-19 high for falling edge detection and low for rising edge detection of the XT* input. The Microprocessor can enable the external trigger interrupt by setting port pin A1U4-28 high or disable the interrupt by setting it low. Microprocessor port pin A1U4-28 should only be high if the instrument trigger mode of "ON" has been selected. Resistor A1R20 pulls NAND gate input A1U13 low during power-up to ensure that the external trigger interrupt input (A1U4-9) is high.

When the EXOR gate output (A1U14-3) goes high, and NAND gate input A1U12-13 is high, the output of the NAND gate (A1U12-11) goes low to interrupt the Microprocessor. The Microprocessor can also determine the state of the XT* input by reading the TRIG signal on port pin A1U4-27.

The XT* input is pulled up to +5V dc by A1Z2 and is protected from damage by ESD by A1R58, A1C54, A1Z3, and A1CR15. Capacitor A1C54 helps ensure that the instrument meets EMI/EMC performance requirements.

2-49. A/D Converter PCA

The following paragraphs describe the operation of the circuits on the A/D Converter PCA. The schematic for this pca is located in Section 8.

2-50. Analog Measurement Processor

Refer to Figure 2-3 for an overall picture of the Analog Measurement Processor chip and its peripheral circuits. Table 2-4 describes Analog Measurement Processor chip signal names.

The Analog Measurement Processor (A3U8) is a 68-pin CMOS device that, under control of the A/D Microcontroller (A3U9), performs the following functions:

- Input signal routing
- Input signal conditioning
- Range switching
- Passive filtering of dc voltage and resistance measurements
- Active filtering of ac voltage measurements
- A/D conversion
- Support for direct volts, true rms ac volts, temperature, resistance,and frequency measurements

Two separate signal paths are used, one for dc/ohms/temperature and one for ac. The volts dc (3V range and below) and temperature voltages are coupled directly to the a/d converter, while higher voltages are attenuated first. For ohms, the dc circuitry is augmented with an internal ohms source voltage regulator controlled through an extra set of switches. For volts ac, inputs are routed through the ac buffer, which uses the gain selected by the Measurement Processor (A3U8).

The a/d converter uses a modified dual-slope minor cycle method. The basic measurement unit, a minor cycle, consists of a fixed time integrate period for the unknown input, a variable time reference integrate period, a variable time hold period, and various short transition periods. A minor cycle period lasts for 25 ms or until a new minor cycle is begun, whichever comes first.

2-51. Input Protection

The instrument measurement circuits are protected when overvoltages are applied through the following comprehensive means:

- Any voltage transients on channel 0 HI or LO terminals areimmediately clamped to a peak of about 1800V or less by MOVs A3RV1and A3RV2. (This is much lower than the 2500V peaks that can beexpected on 240 VAC, IEC 664 Installation Category II, ac mains.)
- Fusible resistors A3R10 and A3R11 protect the measurement circuitryin all measurement modes by limiting currents.
- A3Q11 clamps voltages exceeding 0.7V below and approximately 6.0Vabove analog common (LO) or LO SENSE, with A3R35 limiting the inputcurrent.
- A3Q10 clamps voltages during ohms measurements with A3RT1, A3R34,A3R10, and A3Z4 limiting the input current. With large overloads,thermistor A3RT1 will heat up and increase in resistance.
- A3U8 also clamps voltages on its measurement input pins that exceedthe VDD and VSS supply rails. Resistors A3R42, A3R11, A3R10, A3RT1,A3Z4, A3R35, and A3R34 limit any input currents.
- Any excessive voltages that are clamped through A3U8 to VDD or VSS,are then also clamped by zener diodes A3VR3 and A3VR2.
- The open thermocouple detect circuitry is protected against voltagetransient damage by A3Q14 and A3Q15.
- When measuring ac volts, the ac buffer is protected by dual-diodeclamp A3CR1 and resistor network A3Z3.
- Switching induced transients are also clamped by dual-diodeA3CR4 and capacitor A3C33, and limited by resistor A3R33.

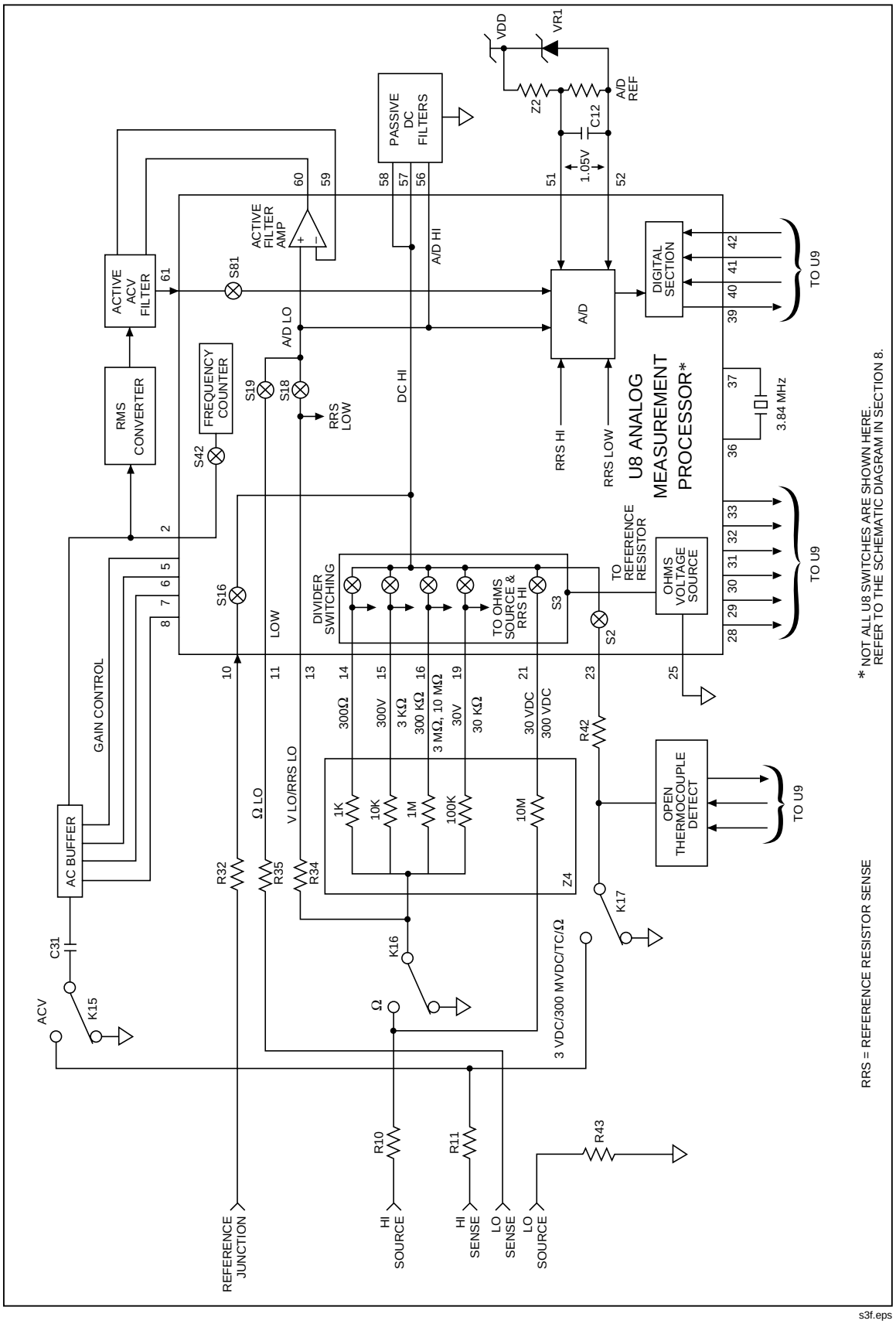


Figure 2-3. Analog Simplified Schematic Diagram

Table 2-4. Analog Measurement Processor Pin Descriptions

Pin	Name	Description
1	VDD	+5.4V supply
2	ACBO	AC buffer output
3	AIN	(not used)
4	AGND2	Analog ground
5	ACR4	AC buffer range 4 (300V)
6	ACR3	AC buffer range 3 (30V)
7	ACR2	AC buffer range 2 (3V)
8	ACR1	AC buffer range 1 (300 mV)
9	VSSA	-5.4V supply for AC ranging
10	REFJ	Reference junction input
11	DCV	A/D converter low input
12	LOW	Driven guard
13	GRD	Reference resistor sense for ohms
14	RRS	Tap #4 on the DCV input divider/ohms reference network
15	V4	Tap #3 on the DCV input divider/ohms reference network
	V3	
16	V1	Tap #1 on the DCV input divider/ohms reference network
17	GRD	Driven guard
18	V2F	Tap #2 input on the DCV input divider/ohms reference network
19	V2	Tap #2 on the DCV input divider/ohms reference network
20	GRD	Driven guard
21	V0	Tap #0 on the DCV input divider/ohms reference network
22	GRD	Driven guard
23	OVS	Ohms and volts sense input
24	GRD	Guard
25	AGND1	Analog ground
26	-	(not used)
27	DGND	Analog ground
28	FC0	Function control #0
29	FC1	Function control #1
30	FC2	Function control #2
31	FC3	Function control #3
32	FC4	(not used)
33	FC5	(not used)
34	FC6	Function control #6
35	FC7	Function control #7
36	XIN	Crystal oscillator input
37	XOUT	Crystal oscillator output
38	MRST	Master reset
39	AS	Analog send
40	AR	Analog receive
41	SK	Serial clock
42	CS	Chip select
43	BRS	(not used)
44	VSS	-5.4V dc
45	INT	Integrator output

Table 2-4. Analog Measurement Processor Pin Descriptions (cont)

Pin	Name	Description
46	SUM	Integrator summing node
47	B.1	Buffer output, 100 mV range
48	B.32	Buffer output, 300 mV range
49	B1	Buffer output, 1000 mV range
50	B3.2	Buffer output, 3V range
51	VREF+	A/D voltage reference plus
52	VREF-	A/D voltage reference minus
53	RAO	A/D reference amplifier output
54	RA+	A/D reference amplifier noninverting input
55	RA-	A/D reference amplifier inverting input
56	AFO	Passive filter 2
57	MOF	Passive filter 1 plus resistance
58	AFI	Passive filter 1
59	FAI	Filter amplifier inverting input
60	FAO	Filter amplifier output
61	RMSF	RMS output, filtered
62	AGND3	(not used, connected to filtered -5.4V dc)
63	RMSG	(not used)
64	2	RMS converter output
65	RMSO	(not used)
	CAVG	
66	VSSR	-5.4V dc, filtered
67	RMSG	(not used, pulled to filtered -5.4V dc)
68	1	(not used)
	RMSI	

2-52. Input Signal Conditioning

Each input is conditioned and/or scaled to a dc voltage appropriate for measurement by the a/d converter. DC voltage applied to the a/d converter can be handled on internal ranges of 0.1V, 0.3V, 1V, or 3V. Therefore, high-voltage dc inputs are scaled, and ohms inputs are converted to a dc voltage. Line voltage level ac inputs are first scaled and then converted to a dc voltage. Noise rejection is provided by passive and active filters.

2-53. Function Relays

Latching relays A3K15, A3K16, and A3K17 route the input signal to the proper circuit blocks to implement the desired measurement function. These relays are switched when a 6-millisecond pulse is applied to the appropriate reset or set coil by the NPN Darlington drivers in IC A3U10. The A/D Microcontroller A3U9 controls the relay drive pulses by setting the outputs of port 6. Since the other end of the relay coil is connected to the VDDR supply, a magnetic field is generated, causing the relay armature and contacts to move to (or remain in) the desired position. Function relay states are defined in Table 2-5.

Table 2-5. Function Relay States

Relay Position			
Function	**A3K17**	**A3K16**	**A3K15**
DC mV, 3V,Thermocouples	Reset	Set	Set
DC 30V, 300V	Set	Set	Set
ACV	Set	Set	Reset
Ohms, RTDs	Reset	Reset	Set
Frequency	Set	Set	Reset

2-54. DC Volts and Thermocouples

For the 3V and lower ranges (including thermocouples), the HI input signal is applied directly to the A3U8 analog processor through A3R11, A3K17, and A3R42. Capacitor A3C27 filters this input, which the analog processor then routes through S2 and other internal switches, through the passive filter, and to the internal a/d converter. The LO SENSE signal is applied to A3U8 through A3R35 and routed through internal switch A3U8-S19 to LO of the a/d converter.

Guard signals MGRD and RGRD are driven by an amplifier internal to A3U8 to a voltage appropriate for preventing leakage from the input HI signal under high humidity conditions.

For the 30V range, the HI signal is scaled by resistor network A3Z4. Here, the input is applied to pin 1 of A3Z4 so that an approximate 100:1 divider is formed by the 10-MΩ and 100.5-kΩ resistors in A3Z4 when analog processor switches S3 and S13 are closed. The attenuated HI input is then sent through internal switch S12 to the passive filter and the a/d converter. Input LO is sensed through analog processor switch S18 and resistor A3R34.

For the 300V range (Figure 2-4), the HI signal is again scaled by A3Z4. The input is applied to pin 1 of A3Z4, and a 1000:1 divider is formed by the 10-MΩ and 10.01-kΩ resistors when switches S3 and S9 are closed in A3Z4. The attenuated HI input is then sent through internal switch S10 to the passive filter and the a/d converter. LO is sensed through analog processor switch S18 and resistor A3R34.

2-55. Ohms and RTDs

Resistance measurements are made using a ratio ohms technique, as shown in Figure 2-5. A stable voltage source is connected in series with the reference resistor in A3Z4 and the unknown resistor. Since the same current flows through both resistors, the unknown resistance can be determined by multiplying the ratio of the voltage drops across the reference and the unknown resistors by the known reference resistor value.

For the RTD, 300Ω, 3-kΩ, and 30-kΩ ranges, the ratio technique is implemented by integrating the voltage across the unknown resistance for a fixed period of time and then integrating the negative of the voltage across the reference resistance for a variable time period. In this way, each minor cycle result gives the ratio directly.

For the 300-kΩ, 3-MΩ, and 10-MΩ ranges, the ratio is determined by performing two separate voltage measurements in order to improve noise rejection. One fixed-period integration is performed on the voltage across the unknown resistance, and the second integration is performed on the voltage across the reference resistance. The ratio of the two fixed-period voltge measurements is then computed by Microcontroller A3U9. The resistance measurement result is determined when A3U9 multiplies the ratio by the reference resistance value.

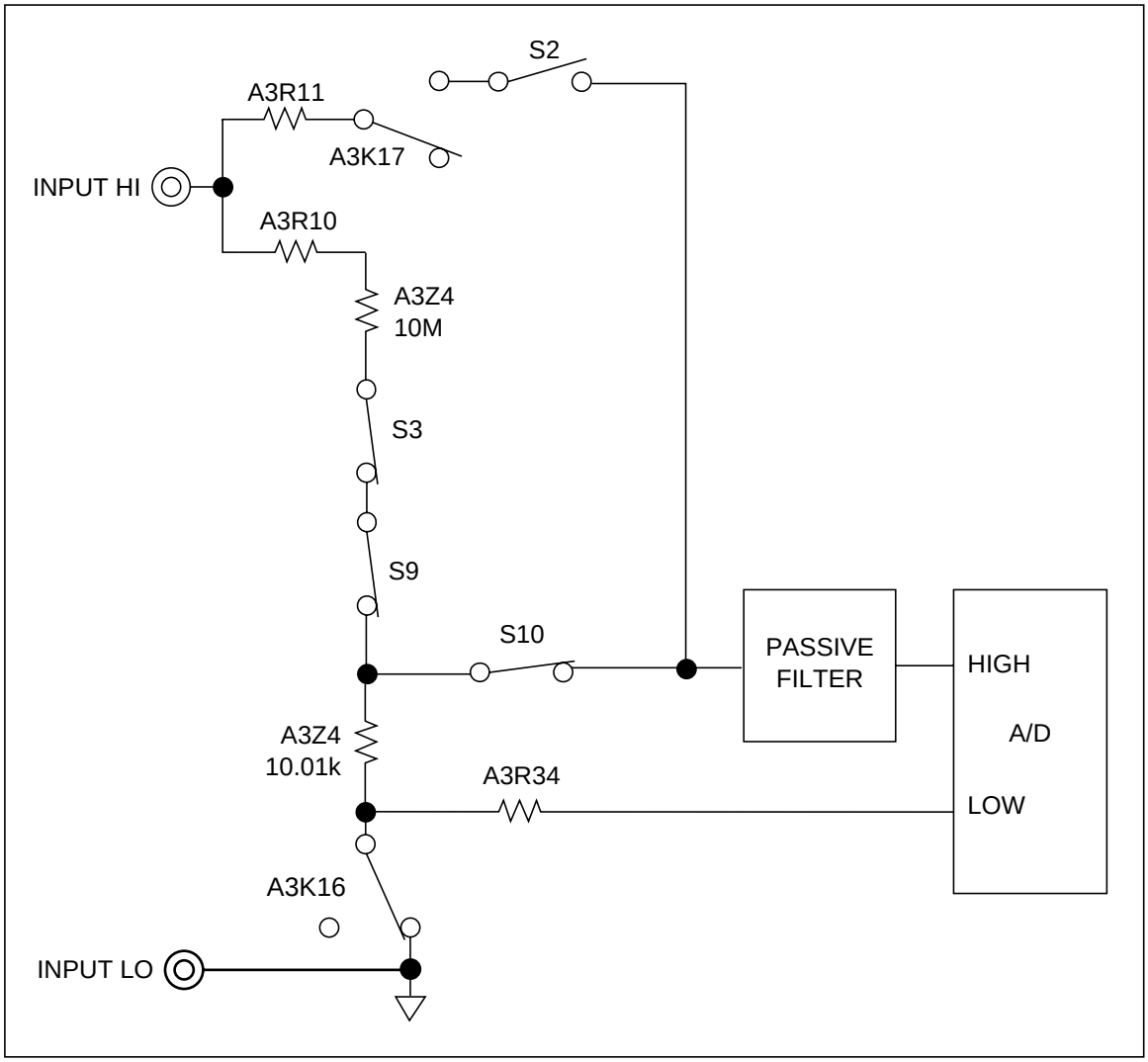


Figure 2-4. DC Volts 300V Range Simplified Schematic

When an input is switched in for a measurement, the ohms source in Analog Processor A3U8 is set to the correct voltage for the range selected and is connected to the appropriate reference resistor in network A3Z4. A measurement current then flows through A3Z4, relay A3K16, thermistor A3RT1, resistor A3R10, the unknown resistance, A3R43, ground, and the ohms source.

The resulting voltage across the unknown resistance is integrated for a fixed period of time by the A/D Converter through the HI SENSE path of A3R11, A3K17, A3R42 and A3U8 switch S2, and the LO SENSE path of A3R35 and Analog Processor switch S19. Passive filtering is provided by A3C34, A3C27, and portions or all of the DC Filter block.

The voltage across the reference resistor for the 300Ω and RTD, 3-kΩ, and 30-kΩ ranges (the 1-kΩ, 10.01-kΩ, and 100.5-kΩ resistances in A3Z4, respectively) is integrated for a variable period of time until the voltage across the integrate capacitor reaches zero. For the 300Ω and RTD range, the reference resistor voltage is switched in through Analog Processor switch S6 and applied to the A/D Converter by switch S8. For the 3-kΩ range, switches S9 and S11 perform these functions, respectively. For the 30-kΩ range, switches S13 and S14 are used. For all ranges, the voltage is routed through A3R34 to the RRS input.

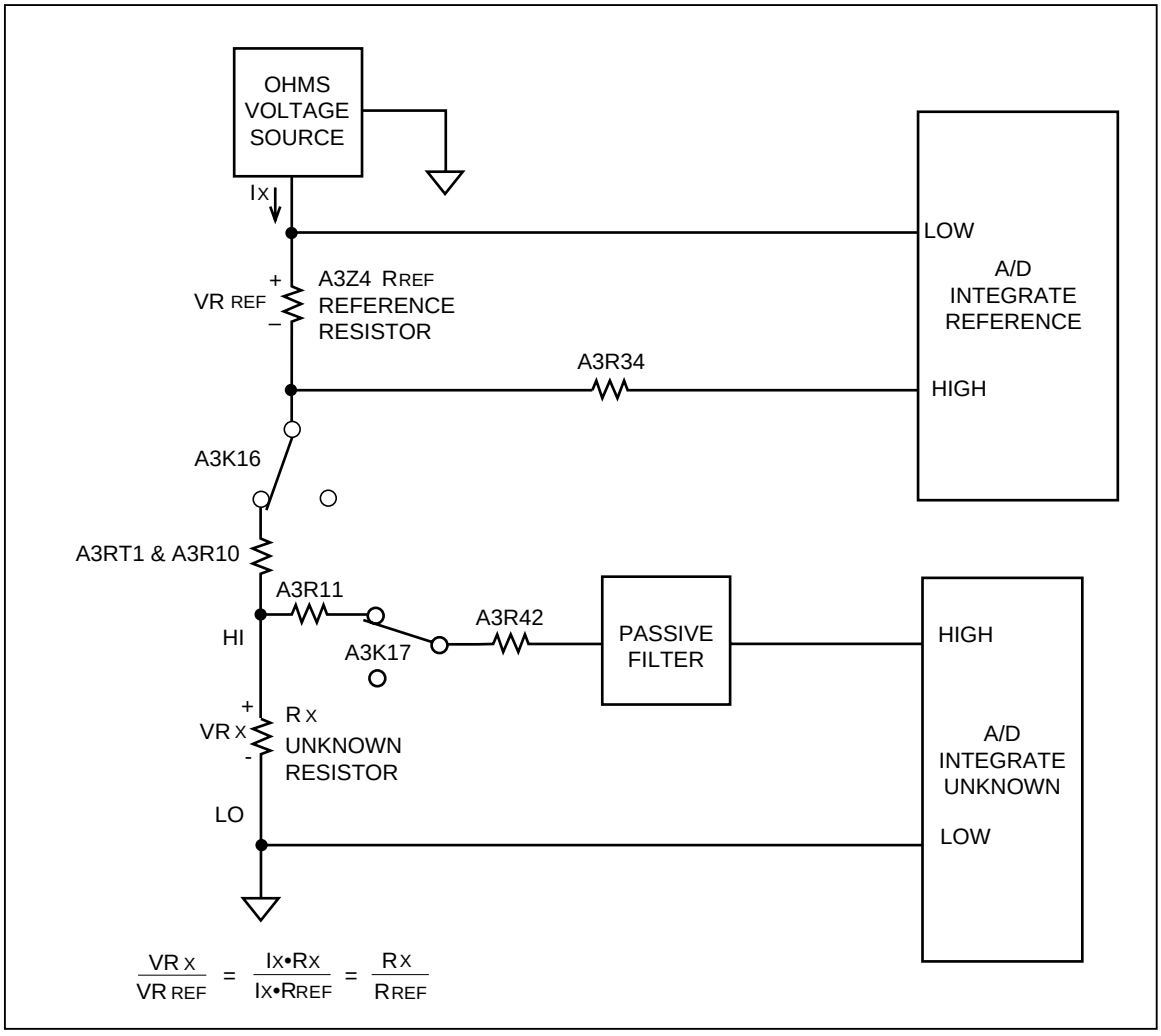


Figure 2-5. Ohms Simplified Schematic

The reference resistor for the 300-kΩ, 3-MΩ, and 10-MΩ ranges is the 1-MΩ resistor in A3Z4, which is selected by S15. The voltage across this reference is integrated during its own minor cycle(s) and is switched to a passive filter and the A/D Converter by switches S1 and S18.

When 4-wire measurements are made on any of the six ranges, separate Source and Sense signal paths are maintained to the point of the unknown resistance. The 4-wire Source path measurement current is provided by the A3U8 ohms source through one of the A3U8 internal switches (S6, S9, S13, or S15) and the appropriate reference resistor in A3Z4. The current flows through relay A3K16, thermistor A3RT1, resistor A3R10, the HI Source instrument relay contacts (A3K1 - A3K3, A3K5 - A3K14), and the HI Source lead wire, to the unknown resistance to be measured. The current flows back through the LO Source lead wire, the LO Source path of the instrument relays (A3K1 - A3K3, A3K5 - A3K14), resistor A3R43, and analog ground, to the A3U8 ohms source.

The voltage that develops across the unknown resistance is sensed through the other 2 wires of the 4-wire set. HI is sensed through the HI Sense path made up of the users HI Sense lead wire, the HI Sense contacts in the instrument relays, resistor A3R11, relay A3K17, resistor A3R42, and Analog Processor A3U8 switch S2. LO is sensed through the users LO Sense lead wire, the LO Sense contacts in the instrument relays, protection resistor A3R35, and A3U8 switch S19.

Since virtually no current flows through the sense path, no error voltages are developed that would add to the voltage across the unknown resistance; this 4-wire measurement technique eliminates user lead-wire and instrument relay contact and circuit board trace resistance errors.

2-56. AC Volts

AC-coupled ac voltage inputs are scaled by the ac buffer, converted to dc by a true rms ac-to-dc converter, filtered, and then sent to the a/d converter.

Refer to Figure 2-6. Input HI is switched to the ac buffer by dc-blocking capacitor A3C31, protection resistor A3R11, and latching relay A3K15. Resistor A3R44 and A3K15 act to discharge A3C31 between channel measurements. LO is switched to the A3U8 A/D Converter through A3R34 and S18.

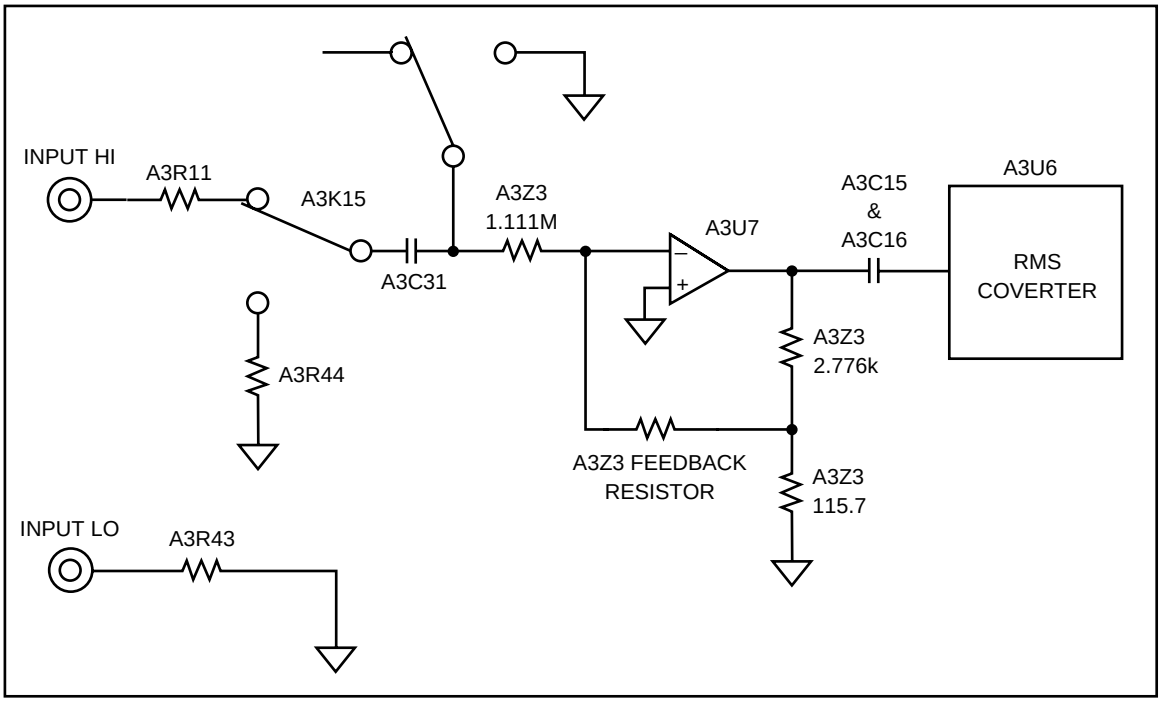


Figure 2-6. AC Buffer Simplified Schematic

JFETs A3Q3 through A3Q9 select one of the four gain (or attenuation) ranges of the buffer (wide-bandwidth op-amp A3U7.) The four JFET drive signals ACR1 through ACR4 turn the JFETs on at 0V and off at -VAC. Only one line at a time will be set at 0 volts to select a range.

The input signal to the buffer is first divided by 10, 100, or 1000 for the 300 mV, 3V, and 30V ranges, respectively. The resistance ratios used are summarized in Table 2-6. Note that the 111.1-kΩ resistor is left in parallel with the smaller (higher attenuation) resistors. The attenuated signal is then amplified by A3U7, which is set for a gain of 25 by the 2.776-kΩ and 115.7Ω resistors in A3Z3. Components A3R27 and A3C23 compensate high-frequency performance on the 300 mV range. For the 300V range, overall buffer gain is determined by the ratio of the 2.776-kΩ feedback resistor to the 1.111-MΩ input resistor.

Table 2-6. AC Volts Input Signal Dividers

Range	Drive Signal	A3Z3 Divider Resistor(s)	Overall Gain
300 mV	ACR1	111.1 kΩ	2.5
3V	ACR2	12.25 kΩ || 111.1 kΩ	0.25
30V	ACR3	1.013 kΩ || 111.1 kΩ	0.025
150/300V	ACR4	none	0.0025

The output of the buffer is ac-coupled by A3C15 and A3C16 to the true-rms ac-to-dc converter A3U6. Discharge JFET A3Q13 is switched on to remove any excess charge from the coupling capacitors A3C15 and A3C16 between channel measurements. A3C17 provides an averaging function for the converter, and resistor network A3Z1 divides the output by 2.5 before sending the signal to the active ac volts filter. Analog processor switch S81 connects the output of the active filter to HI of the A/D Converter.

Components A3R29, A3R30, A3C26, and A3C28 provide filtered power supplies (+VAC and -VAC) for the ac buffer, the ac switch JFETs, and the rms converter.

2-57. Frequency 2-1.

After any dc component is blocked by capacitors A3C15, A3C16, and A3C31, the output of the ac buffer is used to determine the input frequency. This signal is sent to the ACBO pin of analog processor A3U8 and switched to the internal frequency comparator and counter circuit by S42.

2-58. Passive and Active Filters

The passive filters are used for the dc voltage and ohms measurements. For most ranges, capacitors A3C14 and A3C11 are switched into the measurement circuit in front of the A3U8 A/D Converter by switches S86, S87, and S88. These capacitors act with the 100-kΩ series resistance provided by A3R42 or A3Z4 to filter out high-frequency noise. For the 300-kΩ range, only A3C14 is switched in by switches S86 and S85. For the 3-MΩ and 10-MΩ ranges, A3C11 or A3C14 are not switched in to keep settling times reasonably short.

Between channel measurements, the passive filters are discharged by JFET A3Q2 under control of Microcontroller A3U9 through comparator A3U14. When the ZERO signal is asserted, A3R14 pulls the gate of A3Q2 to ground, turning the JFET on and discharging A3C11. At the same time, zeroing of filter capacitors A3C14 and A3C27 is accomplished by having the Analog Processor turn on internal switches S2, S86, and S87.

The active filter is only used for ac voltage measurements. This three-pole active filter removes a significant portion of the ac ripple and noise present in the output of the rms converter without introducing any additional dc errors. The active filter op-amp within A3U8, resistors A3R20, A3R17, and A3R16, and capacitors A3C7, A3C10, and A3C6 form the filter circuit. This filter is referenced to the LO input to the a/d converter within A3U8 by the op-amp. The input to the filter is available at the RMSO pin, and the output is sent to the RMSF pin of A3U8. Switches S80 and S82, which are turned on prior to each new channel measurement, cause the filter to quickly settle (pre-charge) to near the proper dc output level.

2-59. A/D Converter

Figure 2-7 shows the dual slope a/d converter used in the instrument. The unknown input voltage is buffered and used to charge (integrate) a capacitor for an exact period of time. This integrator capacitor is then discharged by the buffered output of a stable and accurate reference voltage of opposite polarity. The capacitor discharge time, which is proportional to the level of the unknown input signal, is measured by the digital circuits in the Analog Measurement Processor. This time count becomes the conversion result.

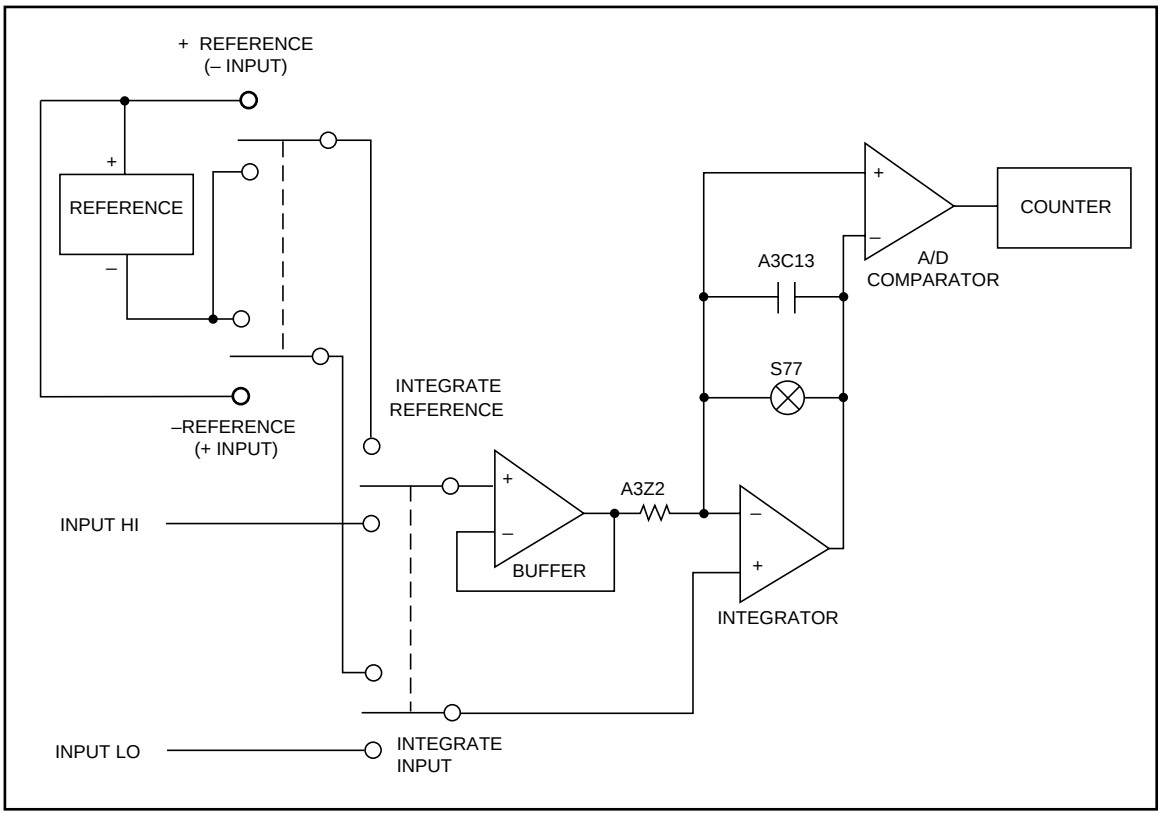


Figure 2-7. A/D Converter Simplified Schematic

In both the slow and fast measurement rates, the a/d converter uses its ±300 mV range for most measurement functions and ranges. The primary exceptions are that the 3V dc range is measured on the a/d converter 3V range, thermocouples are measured on the ±100 mV range, and the temperature reference is measured on the 1V a/d converter range. The typical overload point on a slow rate 30000 count range is 32000 display counts; the typical overload point on a fast rate 3000 count range is 3200 display counts.

During the integrate phase, the a/d buffer in the A3U8 Analog Measurement Processor applies the signal to be measured to one of the four integrator input resistors in network A3Z2. As shown on the A/D Converter schematic diagram in Section 8, the choice of resistor selects the a/d converter range. Switch S69 connects the buffer output through pin B.1 for the 100-mV range, S71 connects the output through B.32 for the 300 mV range, S73 connects to pin B1 for the 1V range, and S75 sets up the 3V range through pin B3.2.

The current through the selected integrator input resistor charges integrator capacitor A3C13, with the current dependent on the buffer output voltage. After the integrate phase, the buffer is connected to the opposite polarity reference voltage, and the integrator integrates back toward zero capacitor voltage until the comparator trips. An internal counter measures this variable integrate time. If the a/d converter input voltage is too high, the integrator overloads and does not return to its starting point by the end of the measurement phase. Switch S77 is then turned on to discharge integrate capacitor A3C13.

The reference voltage used during the variable integrate period for voltage (and high ohms) conversions is generated from zener reference diode A3VR1, which is time and temperature stable. The reference amplifier in the Analog Measurement Processor, along with resistors A3R15, A3R18, and A3R21, pulls approximately 2 mA of current through the zener. Resistors in network A3Z2 divide the zener voltage down to the reference 1.05V required by the A/D Converter.

2-60. Inguard Microcontroller Circuitry

The Microcontroller, A3U9, with its internal program memory and RAM and associated circuitry, controls measurement functions on the A/D Converter PCA and communicates with the Main (outguard) processor.

The Microcontroller communicates directly with the A3U8 Analog Measurement Processor using the CLK, CS, AR, and AS lines and can monitor the state of the analog processor using the FC[0:7] lines. Filter zeroing is controlled by the ZERO signal. The open thermocouple detect circuitry is controlled by the OTCCLK and OTCEN lines and read by the OTC line. The Microcontroller also communicates with the Main (outguard) processor serially using the IGDR line to receive and the IGDS line (driven by A3Q1) to send.

The channel and function relays are driven to the desired measurement state by signals sent out through microcontroller ports 1, 3, 4, 6, and 7.

On power up, the reset/break detect circuit made up of quad comparator A3U1, capacitors A3C1 and A3C2, and resistors A3R1 through A3R6 and A3R8 resets the Microcontroller through the RESET* line. When a break signal is received from the outguard processor, the inguard A3U9 is again reset. Therefore, if Microcontroller operation is interrupted by line transients, the outguard can regain control of the inguard by resetting A3U9.

2-61. Channel Selection Circuitry

Measurement input channel selection is accomplished by a set of latching 4-form-C relays organized in a tree structure. Relays A3K5, A3K6, and A3K8 through A3K14 select among channels 1 through 20. Relay A3K7 disconnects rear input channels 1 through 20 from the measurement circuitry between measurements. Relay A3K3 switches in the front panel channel 0 or the rear channels. Inductors A3L1 through A3L24 reduce EMI and current transients.

Selection between 2-wire and 4-wire operation for ohms measurements is performed by latching 2-form-C relays (A3K1 and A3K2.) These relays also serve to select a voltage or thermocouple rear input channel from either channels 1 through 10 or channels 11 through 20.

The coils for the relays are driven by the outputs of Darlington drivers A3U4, A3U5, A3U10, A3U11, and A3U12. The relays are switched when a 6-millisecond pulse is applied to the appropriate reset or set coil by the NPN Darlington drivers in these ICs. When the port pin of Microcontroller A3U9 connected to the input of a driver is set high, the output of the driver pulls one end of a relay set or reset coil low. Since the other end of the relay coil is connected to the VDDR supply, a magnetic field is generated, causing the relay armature and contacts to move to (or remain in) the desired position.

2-62. Open Thermocouple Check

Immediately before a thermocouple measurement, the open thermocouple check circuit applies a small, ac-coupled signal to the thermocouple input. Microcontroller A3U9 initiates the test by asserting OTCEN, causing comparator A3U14/A3R40 to turn on JFET A3Q12. Next, the Microcontroller sends a 78-kHz square wave out the OTCCLK line through A3R41, A3Q12, and A3C32 to the thermocouple input. The resulting waveform is detected by A3U13 and A3CR2, and a proportional level is stored on capacitor A3C30. Op amp A3U13 compares this detected level with the VTH threshold voltage set up by A3R37 and A3R36 and stored on A3C29. If the resistance at the input is too large, the VTH level will be exceeded and the OTC (open thermocouple check) line will be asserted. After a short delay, the Microcontroller analyzes this OTC signal, determines whether the thermocouple should be reported as open, and deasserts OTCEN and sets OTCCLK high, ending the test.

2-63. Input Connector PCA

The Input Connector assembly, which plugs into the A/D Converter PCA from the rear of the instrument, provides 20 pairs of channel terminals for connecting measurement sensors. This assembly also provides the reference junction temperature sensor circuitry used when making thermocouple measurements.

Circuit connections between the Input Connector and A/D Converter PCAs are made via connectors A4P1 and A4P2. Input channel and earth ground connections are made via A4P1, while temperature sensor connections are made through A4P2.

Input connections to channels 1 through 20 are made through terminal blocks TB1 and TB2. Channel 1 and 11 HI and LO terminals incorporate larger creepage and clearance distances and each have a metal oxide varistor (MOV) to earth ground in order to clamp voltage transients. MOVs A4RV1 through A4RV4 limit transient impulses to the more reasonable level of approximately 1800V peak instead of the 2500V peak that can be expected on 240 VAC, IEC 664 Installation Category II, ac mains. In this way, higher voltage ratings can be applied to channels 1 and 11 than can be applied to the other rear channels.

Strain relief for the user's sensor wiring is provided both by the Connector PCA housing and the two round pin headers. Each pin of the strain relief headers is electrically isolated from all other pins and circuitry.

Temperature sensor transistor A4Q1 outputs a voltage inversely proportional to the temperature of the input channel terminals. This voltage is 0.6V dc at 25ºC, increasing 2 mV with each degree decrease in temperature, or decreasing 2 mV with each degree increase in temperature. For high accuracy, A4Q1 is physically centered within and thermally linked to the 20 input terminals. Local voltage reference A4VR1 and resistors A4R1 through A4R3 set the calibrated operating current of the temperature sensor. Capacitor A4C1 shunts noise and EMI to ground.

2-64. Display PCA

Display Assembly operation is classified into six functional circuit blocks: the Main PCA Connector, the Front Panel Switches, the Display, the Beeper Drive Circuit, the Watchdog Timer/Reset Circuit, and the Display Controller. These blocks are described in the following paragraphs.

2-65. Main PCA Connector

The 20-pin Main PCA Connector (A2J1) provides the interface between the Main PCA and the other functional blocks on the Display PCA. Seven of the connector pins provide the necessary connections to the four power supply voltages (-30V dc, -5V dc, +5.1V dc, and 5.4V ac filament voltage). Six pins are used to provide the interface to the Front Panel Switches (A2SWR1 through A2SWR6). The other seven signals interface the Microprocessor (A1U4) to the Display Controller (A2U1) and pass the reset signals between the assemblies.

2-66. Front Panel Switches

The Microprocessor scans the 19 Front Panel Switches (A2S1 through A2S18, and A2S21) using only six interface signals (plus the ground connection already available from the power supply). These six signals (SWR1 through SWR6) are connected to a bidirectional I/O port on the microprocessor. Each successive column has one less switch.

This arrangement allows the unused interface signals to function as strobe signals when their respective column is driven by the Microprocessor. The Microprocessor cycles through six steps to scan the complete Front Panel Switch matrix. Table 2-7 shows the interface signal state and, if the signal state is an output, the switches that may be detected as closed.

Table 2-7. Front Panel Switch Scanning

Interface Signal States or Key Sensed						
Step	**SWR6**	**SWR5**	**SWR4**	**SWR3**	**SWR2**	**SWR1**
1	A2S8	A2S17	A2S10	A2S12	A2S18	A2S13
2	A2S1	A2S2	A2S3	A2S4	A2S11	0
3	A2S7	A2S9	A2S5	A2S6	0	Z
4	A2S14	A2S15	A2S16	0	Z	Z
5	NA	NA	0	Z	Z	Z
6	A2S21	0	Z	Z	Z	Z

A2Sn indicates switch closure sensed.
0 indicated strobe driven to logic 0
Z indicated high impedance input; state ignored.

In step 1, six port bits are set to input, and the interface signal values are read. In steps 2 through 6, the bit listed as O is set to output zero, the other bits are read, and bits indicated by a Z are ignored.

Each of the interface signals is pulled up to the +5V dc supply by a 10-kΩ resistor in network A2Z1. Normally, the resistance between any two of the interface signals is

approximately 20 kΩ. Checking resistances between any two signals (SWR1 through SWR6) verifies proper termination by resistor network A2Z1.

2-67. Display

The custom vacuum-fluorescent display (A2DS1) comprises a filament, 11 grids (numbered 0 through 10 from right to left on the display), and up to 14 anodes under each grid. The anodes make up the digits and annunciators for their respective area of the display. The grids are positioned between the filament and the anodes.

A 5.4V ac signal, biased at a -24V dc level, drives the filament. When a grid is driven to +5V dc, the electrons from the filament are accelerated toward the anodes that are under that grid. Anodes under that grid that are also driven to +5V dc are illuminated, but the anodes that are driven to -30V dc are not. Grids are driven to +5V dc one at a time, sequencing from GRID(10) to GRID(0) (left to right, as the display is viewed.)

2-68. Beeper Drive Circuit

The Beeper Drive circuit drives the speaker (A2LS1) to provide an audible response to a button press. A valid entry yields a short beep; an incorrect entry yields a longer beep.

The circuitry comprises a dual four-bit binary counter (A2U4) and a NAND gate (A2U6) used as an inverter. One four-bit free-running counter (A2U4) divides the 1.2288-MHz clock signal (E) from the microprocessor (A1U4) by 2 to generate the 614.4-kHz clock (CLK1) used by the Display Controller. This counter also divides the 1.2288-MHz clock by 16, generating the 76.8-kHz clock that drives the second four-bit binary counter (A2U4).

The second four-bit counter is controlled by an open-drain output on the Display Controller (A2U1-17) and pull-down resistor A2R1. When the beeper (A2LS1) is off, A2U1-17 is pulled to ground by A2R1. This signal is then inverted by A2U6, with A2U6-6 driving the CLR input high to hold the four-bit counter reset. Output A2U4-8 of the four-bit counter drives the parallel combination of the beeper (A2LS1) and A2R10 to ground to keep the beeper silent. When commanded by the Main Microprocessor, the Display Controller drives A2U1-17 high, enabling the beeper and driving the CLR input of the four-bit counter (A2U4-12) low. A 4.8-kHz square wave then appears at counter output A2U4-8 and across the parallel combination of A2LS1 and A2R10, causing the beeper to resonate.

2-69. Watchdog Timer and Reset Circuit

This circuit provides active high and active low reset signals to the rest of the system at a power-up or system reset if the Microprocessor does not communicate with the Display Processor for a 5-second period. The Watchdog Timer and Reset Circuit comprises dual retriggerable monostable multivibrator A2U5, NAND gates A2U6, diode A2CR3, and various resistive and capacitive timing components.

At power-up, capacitor A2C3 begins to charge up through resistor A2R3. The voltage level on A2C3 is detected by an input of Schmitt-Trigger NAND gate A2U6-12. The output of this gate (A2U6-11) then drives the active high reset signal (RESET) to the rest of the system. When the voltage on A2C3 is below the input threshold (typically +2.5V dc) of A2U6-12, A2U6-11 is high. As soon as A2C3 charges up to the threshold of A2U6-12, A2U6-11 goes low. The RESET signal drives NAND gate inputs A2U6-1 and A2U6-2 to generate the active low reset signal (RESET*) at A2U6-3.

When the RESET signal transitions from high to low (A2U5-1), the Watchdog Timer is triggered initially, causing A2U5-13 to go high. This half of the dual retriggerable monostable multivibrator uses timing components A2R2 and A2C2 to define a nominal

4.75-second watchdog timeout period. Each time a low-to-high transition of DISTX is detected on A2U5-2, capacitor A2C2 is discharged to restart the timeout period. If there are no low-to-high transitions on DISTX during the 4.75-second period, A2U5-13 transitions from high to low, triggers the other half of A2U5, and causes output A2U5-12 to go low. A2U5-12 is then inverted by A2U6 to drive the RESET signal high, causing a system reset. The low duration of A2U5-12 is determined by timing components A2Z1 and A2C4 and is nominally 460 µs. When A2U5-12 goes high again, RESET goes low to retrigger the Watchdog Timer.

2-70. Display Controller

The Display Controller is a four-bit, single-chip microcomputer with high-voltage outputs that are capable of driving a vacuum-fluorescent display directly. The controller receives commands over a three-wire communication channel from the Microprocessor on the Main Assembly. Each command is transferred serially to the Display Controller on the display transmit (DISTX) signal, with bits being clocked into the Display Controller on the rising edges of the display clock signal (DSCLK). Responses from the Display Controller are sent to the Microprocessor on the display receive signal (DISRX) and are clocked out of the Display Controller on the falling edge of DSCLK.

Series resistor A2R11 isolates DSCLK from A2U1-40, preventing this output from trying to drive A1U4-16 directly. Figure 2-8 shows the waveforms during a single command byte transfer. Note that a high DISRX signal is used to hold off further transfers until the Display Controller has processed the previously received byte of the command.

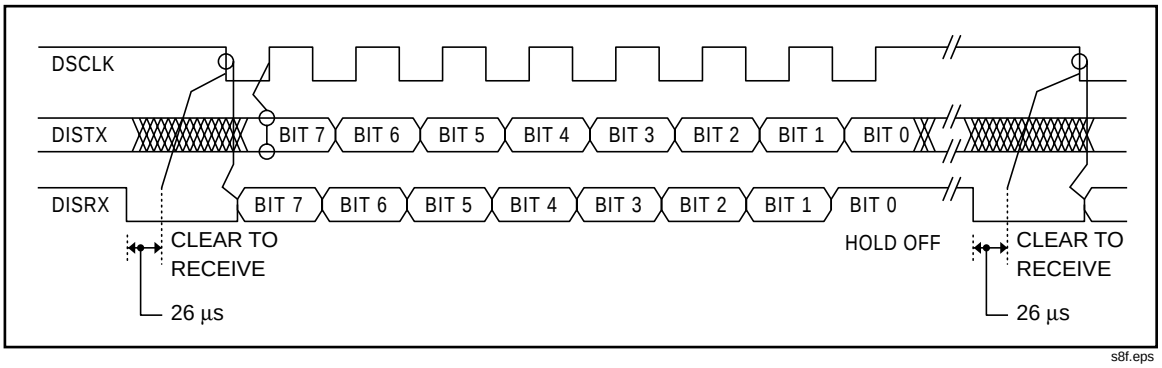


Figure 2-8. Command Byte Transfer Waveforms

Once reset, the Display Controller performs a series of self-tests, initializing display memory and holding the DISRX signal high. After DISRX goes low, the Display Controller is ready for communication; on the first command byte from the Microprocessor, the Display Controller responds with a self-test results response. If all self-tests pass, a response of 00000001 (binary) is returned. If any self-test fails, a response of 01010101 (binary) is returned. The Display Controller initializes its display memory to one of four display patterns depending on the states of the DTEST* (A2U1-41) and LTE* (A2U1-13) inputs. The DTEST* input is pulled up by A2Z1, but may be pulled down by jumpering A2TP4 to A2TP3 (GND). The LTE* input is pulled down by A2R12, but may be pulled up by jumpering A2TP5 to A2TP6 (VCC). The default conditions of DTEST* and LTE* cause the Display Controller to turn all segments on bright at power-up.

Table 2-8 defines the logic and the selection process for the four display initialization modes.

The two display test patterns are a mixture of on and off segments forming a recognizable pattern that allows for simple testing of display operation. Test patterns #1 and #2 are shown in Section 5 of this manual.

Table 2-8. Display Initialization Modes

A2TP4	A2TP5	Power-Up Display Initialization
1	1	All Segments OFF
1	0	All Segments ON (default)
0	1	Display Test Pattern #1
0	0	Display Test Pattern #2

The Display Controller provides 11 grid control outputs and 15 anode control outputs (only 14 anode control outputs are used). Each of these 26 high-voltage outputs provides an active driver to the +5V dc supply and a passive 220-kΩ (nominal) pull-down to the -30V dc supply. These pull-down resistances are internal to the Display Controller.

The Display Controller provides multiplexed drive to the vacuum-fluorescent display by strobing each grid while the segment data for that display area is present on the anode outputs. Each grid is strobed for approximately 1.14 milliseconds every 13.8 milliseconds, resulting in each grid on the display being strobed about 72 times per second. The grid strobing sequence is from GRID(10) to GRID(0), which results in left-to-right strobing of grid areas on the display. Figure 2-9 shows grid control signal timing.

The single grid strobing process involves turning off the previously enabled grid, outputting the anode data for the next grid, and then enabling the next grid. This procedure ensures that there is some time between grid strobes so that no shadowing occurs on the display. A grid is enabled only if one or more anodes are also enabled. Thus, if all anodes under a grid are to be off, the grid is not turned on. Figure 2-10 describes the timing relationship between an individual grid control signal and the anode control signals.

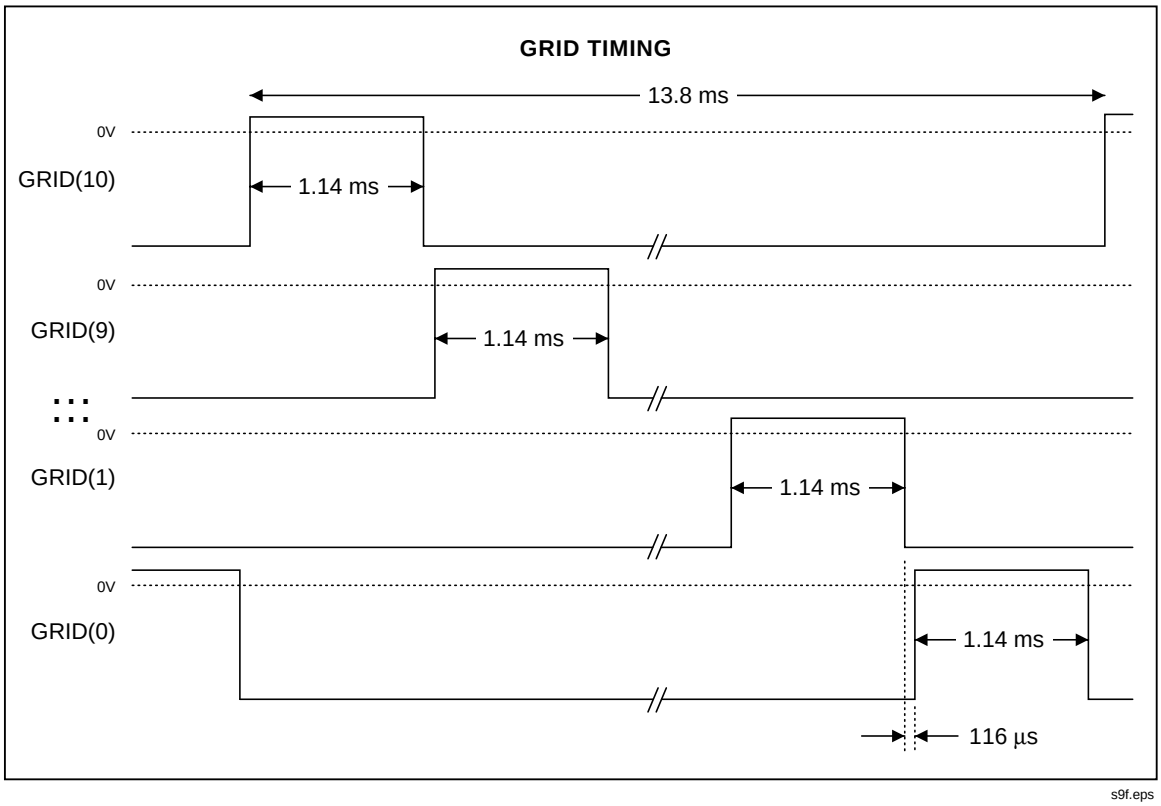


Figure 2-9. Grid Control Signal Timing

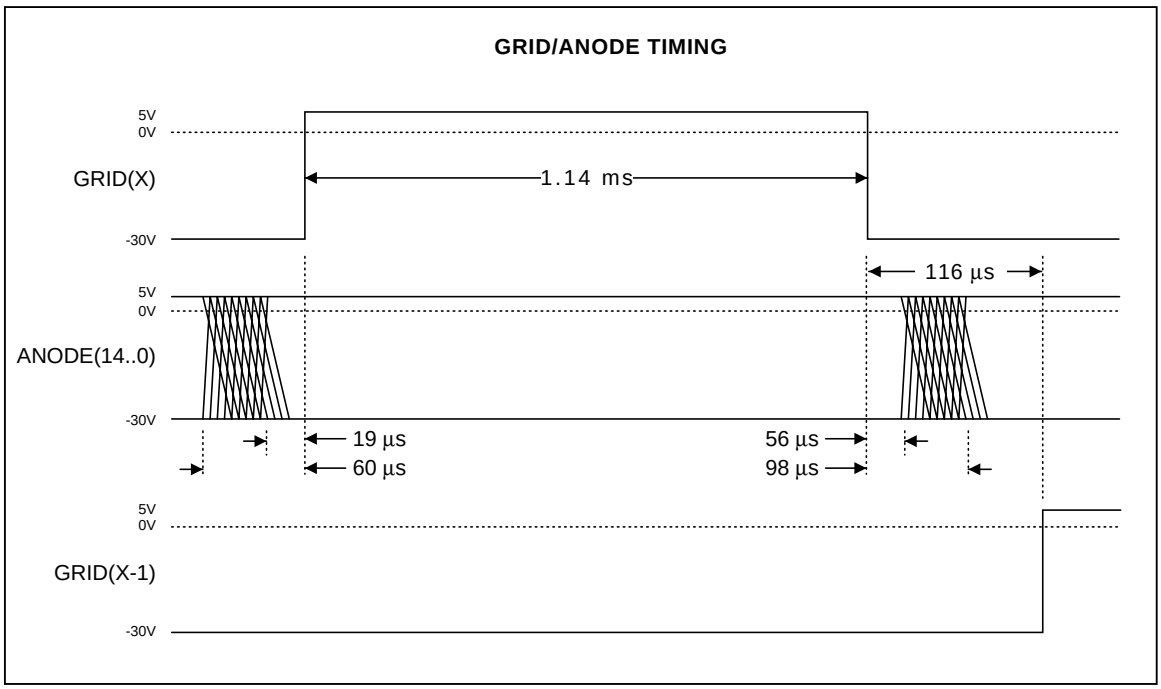


Figure 2-10. Grid-Anode Timing Relationships

2-71. Memory PCA (2625A Only)

The Memory PCA is a serially-accessed, byte-wide, nonvolatile 256K-byte memory that is capable of storing up to 2047 scans of data. The following paragraphs describe in detail the Main PCA Connector, Address Decoding, Page Register, Byte Counter, and Nonvolatile Memory blocks that make up this assembly.

2-72. Main PCA Connector

The Memory PCA interfaces to the Main PCA through a 26-pin, right angle connector (A6J1). This connector routes the eight-bit data bus, the lower three bits of the address bus, memory control and address decode signals from the Main PCA to the Memory PCA. The Memory PCA is powered by the +5.1V dc power supply (VCC). The Memory PCA is sensed by the Microprocessor on the Main PCA through the connection of A6J1-11 to the option sense signal OPS* (A6J1-22).

2-73. Address Decoding

Circuitry on the Main PCA decodes the Microprocessor address bus and provided the MEM* select signal to the Memory PCA. The 3-line to 8-line decoder (A6U8) is used to decode the three least significant address bits to get register select signals for hexadecimal addresses 4, 5, and 6. When the MEM* signal drives A6U8-4 low and the RESET* signal (A6U8-6) is high, the A0 through A2 address bits are decoded to get the MEMORY, PAGEL, and PAGEH register select signals.Address decoding is disabled when RESET* is low so that the Nonvolatile Memory cannot be accidentally modified during power-up or power-down.

2-74. Page Register

The Page Register is an 11-bit register that is writable by the Microprocessor on the Main PCA. The outputs of this register control the most significant address bits of the nonvolatile memories (A6U6 and A6U7.) When register select PAGEL goes high and

the WE* signal is low, NAND gate output A6U2-3 goes high to latch the data bus into the lower part of the page register (A6U1).When register select PAGEH goes high and the WE* signal is low, NAND gate output A6U2-8 goes high to latch the lower three bits of the data bus into the high part of the page register (A6U4).

2-75. Byte Counter

The Byte Counter is a seven-bit ripple counter that controls the lower address bits of the nonvolatile RAMs. This counter is cleared when a new value is written to the lower page register. It automatically increments at the end of each read or write access to the memory data register.

NAND gate output A6U2-3 goes high to write the lower page register and clear the Byte Counter. When data is read from or written to the Non-Volatile Memory, NAND gate output A6U2-6 goes high during the memory cycle, and then low at the end of the memory cycle. The transition from high to low increments the Byte Counter so that the next access to the memory data register will be for the next sequential byte in the Non-Volatile Memory.

2-76. Nonvolatile Memory

The Non-Volatile Memory is made up of two 128K-byte static CMOS memories with integrated lithium battery, power-fail detection, and battery switching circuitry. When the VCC (+5.1V dc) power supply is above +4.5V dc, memories A6U6 and A6U7 are fully operational. When VCC drops below approximately +4.25V dc, all access to the memory are disabled by the internal power-fail detection circuit. When VCC drops below about +3.0V dc, the battery switching circuitry disconnects VCC and connects the lithium battery to the memory so that data is retained while the instrument power is off.

The most significant bit of the Page Register (A6U4-1,16) is gated with the MEMORY register select signal by A6U5 to get the memory chip select signals (A6U5-6 and A6U5-8). Memory pages 0 through 1023 are stored in memory device A6U7, and memory pages 1024 through 2047 are stored in memory device A6U6. The WR* and RD* control signals from the Microprocessor on the Main PCA are used to enable writing of data to and reading data from the memory devices, respectively.

2-77. IEEE-488 Interface (Option -05)

Refer to Section 7 for detailed circuit description of this option.

Chapter 2A
Theory of Operation (2635A)

Title **Page**

2A-1. Introduction

The theory of operation begins with a general overview of the instrument and progresses to a detailed description of the circuits of each pca.

The instrument is first described in general terms with a Functional Block Description. Then, each block is detailed further (often to the component level) with Detailed Circuit Descriptions. Refer to Section 8 of this manual for full schematic diagrams. The Interconnect Diagram in this section (Figure 2A-1) illustrates physical connections among pca's.

Signal names followed by a '*' are active (asserted) low. All other signals are active high.

2A-2. Functional Block Description

Refer to Figure 2A-2, Overall Functional Block Diagram, during the following functional block descriptions.

2A-3. Main PCA Circuitry

The following paragraphs describe the major circuit blocks on the Main PCA.

2A-4. Power Supply

The Power Supply functional block provides voltages required by the vacuum-fluorescent display (-30V dc, -5.0V dc, and filament voltage of 5.4V ac), the inguard circuitry (-5.4V dc VSS, +5.3V dc VDD, and +5.6V dc VDDR), and outguard digital circuitry of +5.0V dc (VCC).

Within the Power Supply, the Raw DC Supply converts ac line voltage to dc levels. The 5V Switching Supply converts this raw dc to 5.0V ±0.25V dc, which is used by the Inverter in generating the above-mentioned outputs. The Power Fail Detector monitors the Raw DC Supply and provides a power supply status signal to the Microprocessor in the Digital Kernel.

2A-5. Digital Kernel

The Digital Kernel functional block is responsible for the coordination of all activities within the instrument. This block requires voltages from the Power Supply and signals from the Power-on Reset circuit.

Specifically, the Digital Kernel Microprocessor performs the following functions:

- Executes the instructions stored in FLASH EPROM.
- Stores temporary data and nonvolatile instrument configuration datain NVRAM.
- Stores instrument calibration data in FLASH EPROM.
- Communicates with the microcontroller on the A/D Converter PCA viathe Serial Communication (Guard Crossing) block.
- Communicates with the Display Controller to display readings and userinterface information.
- Communicates with the Field Programmable Gate Array, which scans theuser interface keyboard found on the Display Assembly and interfaceswith the Digital I/O hardware.
- Communicates with a host computer via the RS-232 interface.
- Stores instrument setup and measurement data on a Static RAM memorycard installed in the Memory Card Interface Assembly.
- Reads the digital inputs and changes digital and alarm outputs.

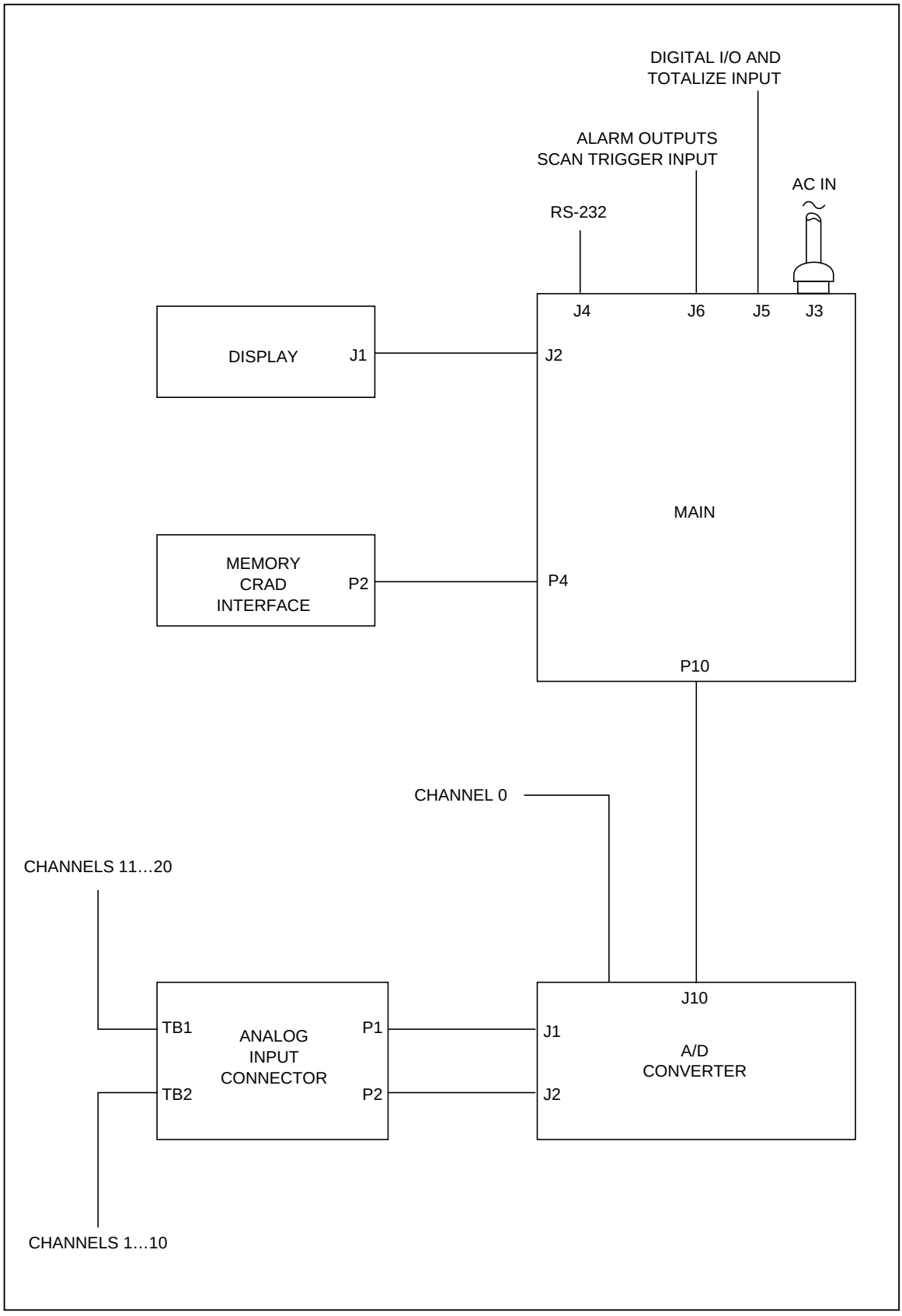
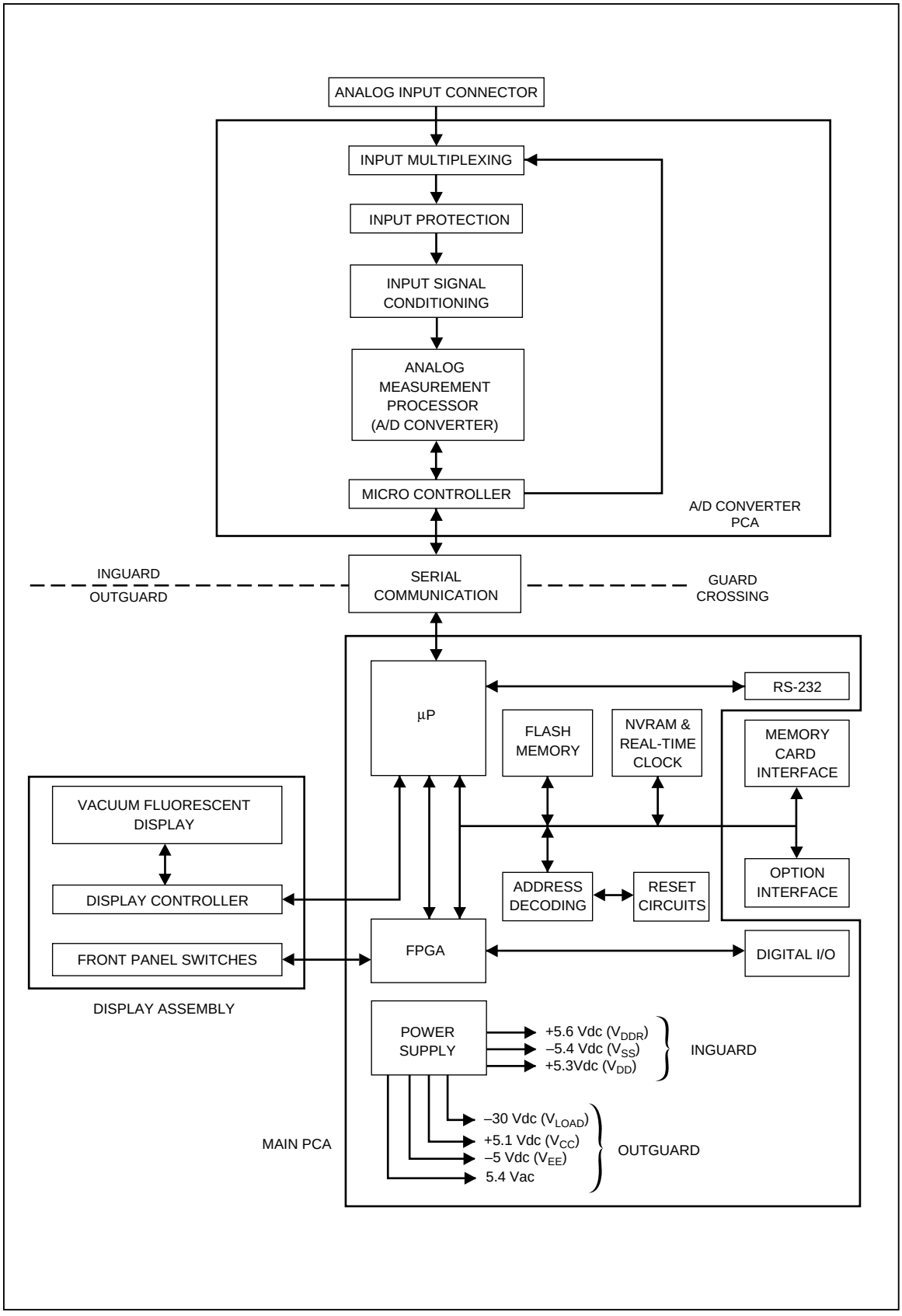


FIGURE 2A-1. InterconnectDiagram (2635A)



s12f.eps

Figure 2A-2. Overall Functional Block Diagram (2635A)

2A-6. Serial Communication (Guard Crossing)

This functional block provides a high isolation voltage communication path between the Digital Kernel of the Main PCA and the microcontroller on the A/D Converter PCA. This bidirectional communication circuit requires power supply voltages from the Power Supply block.

2A-7. Digital Inputs and Outputs

This functional block contains the Totalizer and External Trigger Input Buffers, eight bidirectional Digital I/O channels, four Alarm Outputs, and the Input Threshold control circuits. These circuits require power supply voltages from the Power Supply and signals from the Digital Kernel.

2A-8. A/D Converter PCA

The following paragraphs describe the major blocks of circuitry on the A/D Converter PCA.

2A-9. Analog Measurement Processor

The Analog Measurement Processor (A3U8) provides input signal conditioning, ranging, a/d conversion, and frequency measurement. This custom chip is controlled by the A/D Microcontroller (A3U9). The A/D Microcontroller communicates with the Main PCA Microprocessor (A1U1) over a custom serial interface.

2A-10. Input Protection Circuitry

This circuitry protects the instrument measurement circuits during overvoltage conditions.

2A-11. Input Signal Conditioning

Here, each input is conditioned and/or scaled to a dc voltage for measurement by the a/d converter. DC voltage levels greater than 3V are attenuated. To measure resistance, a dc voltage is applied across a series connection of the input resistance and a reference resistance to develop dc voltages that can be ratioed. DC volts and ohms measurements are filtered by a passive filter. AC voltages are first scaled by an ac buffer, converted to a representative dc voltage by an rms converter, and then filtered by an active filter.

2A-12. Analog-to-Digital (A/D) Converter

The dc voltage output from the signal conditioning circuits is applied to a buffer/integrator which charges a capacitor for an exact amount of time. The time required to discharge this capacitor, which is proportional to the level of the unknown input signal, is then measured by the digital counter circuits in the Analog Measurement Processor.

2A-13. Inguard Microcontroller Circuitry

This microcontroller (and associated circuitry) controls all functions on the A/D Converter PCA and communicates with the digital kernel on the Main PCA. Upon request by the Main PCA, the inguard microcontroller selects the input channel to be measured through the channel selection circuitry, sets up the input signal conditioning, commands the Analog Measurement Processor to begin a conversion, stops the measurement, and then fetches the measurement result. The inguard microcontroller manipulates the result mathematically and transmits the reading to the digital kernel.

2A-14. Channel Selection Circuitry

This circuitry consists of a set of relays and relay-control drivers. The relays form a tree that routes the input channels to the measurement circuitry. Two of the relays are also used to switch between 2-wire and 4-wire operation.

2A-15. Open Thermocouple Check Circuitry

Under control of the Inguard Microcontroller, the open thermocouple check circuit applies a small ac signal to a thermocouple input before each measurement. If an excessive resistance is encountered, an open thermocouple input condition is reported.

2A-16. Input Connector Assembly

The following paragraphs briefly describe the major sections of the Input Connector PCA, which is used for connecting most of the analog inputs to the instrument.

2A-17. 20 Channel Terminals

Twenty HI and LO terminal blocks are provided in two rows, one for channels 1 through 10 and one for channels 11 through 20. The terminals can accommodate a wide range of wire sizes. The two rows of terminal blocks are maintained very close to the same temperature for accurate thermocouple measurements.

2A-18. Reference Junction Temperature

A semiconductor junction is used to sense the temperature of the thermocouple input terminals. The resulting dc output voltage is proportional to the block temperature and is sent to the A/D Converter PCA for measurement.

2A-19. Display PCA

The Display Assembly controller communicates with the main Microprocessor over a three-wire communication channel. Commands from the Microprocessor inform the Display Controller how to modify its internal display memory. The Display Controller then drives the grid and anode signals to illuminate the required segments on the Display. The A2 Display Assembly requires power supply voltages from the Power Supply, a reset signal from the Reset Circuit, and a clock signal from the Digital Kernel.

2A-20. Memory Card Interface PCA

The Memory Card Interface PCA is used to access the memory on an industry standard memory card installed through the slot in the front panel of the instrument. This assembly allows management of the memory card power, adapts timing of accesses by the Digital Kernel to the memory card, and provides visible indicators for low battery voltage and memory card busy status.

2A-21. Detailed Circuit Description

2A-22. Main PCA

>The following paragraphs describe the operation of the circuits on the Main PCA. The schematic for this pca is located in Section 8.

2A-23. Power Supply Circuit Description

The Hydra power supply consists of three major sections:

- Raw DC Supply

  The raw dc supply converts line voltage (90V to 264V ac) to a dcoutput of 7.5V to 35V.

- 5V Switcher Supply

  The 5V switching supply regulates the 7.5 to 35V dc input to anominal 5.0V ±0.25V dc (VCC).

- Inverter

  Using the 5V switching supply output, the inverter generates the -30Vdc, -5V dc, and 5.4V ac supply levels needed for thevacuum-fluorescent display and the RS-232 Interface. The inverteralso provides isolated +5.3V (VDD), +5.6V (VDDR), and -5.4V (VSS)outputs for the inguard circuitry.

2A-24. Raw DC Supply

The raw dc supply circuitry receives input from power transformer T401, which operates on an input ranging from 90V to 264V ac. The power transformer is energized whenever the power cord is plugged into the ac line; there is no on/off switch on the primary side of the transformer. The transformer has an internal 275V ac metal-oxide varistor (MOV) to clamp line transients. The MOV normally acts as an open circuit. When the peak voltage exceeds approximately 400V, the line impedance in series with the line fuse limits transients to approximately 450V. All line voltages use a slow blow 0.125 A, 250V fuse.

On the secondary side of the transformer, rectifiers A1CR2, A1CR3, and capacitor A1C7 rectify and filter the output. When it is ON, switch A1S1 (the front panel POWER switch) connects the output of the rectifiers to the filter capacitor and the rest of the instrument. Depending on line voltage, the output of the rectifiers is between 7.5 and 35V dc. Capacitor A1C2 helps to meet electromagnetic interference (EMI) and electromagnetic compatibility (EMC) requirements.

When external dc power is used, the power switch connects the external dc source to power the instrument. The external dc input uses thermistor A1RT1 (for overcurrent protection) and diode A1CR1 (for reverse input voltage protection.) Capacitor A1C59 helps meet EMI/EMC requirements. Resistor A1R48, capacitors A1C2 and A1C39 also ensure that the instrument meets EMI/EMC performance requirements.

2A-25. Auxiliary 6V Supply

Three-terminal regulator A1U19, voltage-setting resistors A1R44 and A1R46, and capacitor A1C34 make up the auxiliary 6-volt supply. This supply is used for the inverter oscillator, inverter driver, and the power fail detection circuits.

2A-26. 5V Switcher

The 5V switcher supply uses a switcher supply controller/switch device A1U9 and related circuitry.The 7.5V dc to 35V dc input is regulated to 5.1V dc (VCC) through pulse-width modulation at a nominal switching frequency of 100 kHz.

The output voltage of the switcher supply is controlled by varying the duty cycle (ON time) of the switching transistor in the controller/switch device A1U9. A1U9 contains the supply reference, oscillator, switch transistor, pulse-width modulator comparator, switch drive circuit, current-limit comparator, current-limit reference, and thermal limit. Dual inductor A1T2 regulates the current that flows from the raw supply to the load as the switching transistor in A1U9 is turned on and off. Complementary switchA1CR10 conducts when the switching transistor is off.

The pulse-width modulator comparator in A1U9 compares the output to the reference and sets the ON-time/OFF-time ratio to regulate the output to 5.1V dc. A1C26 is the input filter capacitor, and A1C14 is the output filter capacitor. Proper inductor and capacitor values set the filter frequency response to ensure best overall system stability. Circuitry consisting of A1R26, A1C21, and A1C18 ensure that the switcher supply remains stable and operating in the continuous mode. Resistors A1R30 and A1R31 set the output voltage to within 5% of 5.1V.Capacitor A1C21 sets the operating frequency of the switcher at approximately 100 kHz.

Resistors A1R30 and A1R31 form a voltage divider that operates in conjunction with amplifier A1U28, which is configured as a voltage follower.A1U28-5 samples the 5.1V dc output, while A1U28-6 is the voltage divider input.The effect is to maintain the junction of R30 and R31 at 5.1V dc, resulting in an A1U28-7 output level of 6.34V dc, or 1.24V dc above the output.This feedback voltage is applied to A1U9-2, which A1U9 interprets as 1.24V dc because A1U9-3 (ground) is connected to the 5.1V dc output.

A1U9 maintains the feedback and reference voltages at 1.24V dc and thus regulates the 5.1V dc source.

2A-27. Inverter

The inverter supply uses a two transistor driven push-pull configuration. The center tap of transformer A1T1 primary is connected to the 5.0V dc VCC supply, and each side is alternately connected to common through transistors A1Q7 and A1Q8. A1R38 may be removed to disable the inverter supply for troubleshooting purposes. A1Q7 and A1Q8 are driven by the outputs of D flip-flop A1U22. Resistors A1R34 and A1R28, and diodes A1CR11 and A1CR12 shape the input drive signals to properly drive the gate of the transistors. D flip-flop A1U22 is wired as a divide-by-two counter driven by a 110-kHz square wave. The 110-kHz square wave is generated by hex inverter A1U23, which is connected as an oscillator with a frequency determined by the values of resistors A1R40 and A1R47 and capacitor A1C35. The resulting ac voltage produced across the secondary of A1T1 is rectified to provide the input to the inverter inguard and outguard supplies.

2A-28. Inverter Outguard Supply

The inverter outguard supply provides three outputs: 5.4V ac, -30V dc, and -5V dc. These voltages are required by the display and RS-232 drivers and receiver. The 5.4V ac supply comes off the secondary windings (pins 6 and 7) on transformer T1, and it is biased at -24V dc with zener diode A1VR3 and resistor A1R22. Dual diodes A1CR8 and A1CR9 and capacitor A1C17 are for the -30V dc supply. Capacitors A1C30 and A1C31, and dual diodes A1CR13 form a voltage doubler circuit that generates -12 volts. Three-terminal regulator A1U18 then regulates this voltage down to -5V for the RS-232 circuit. Capacitor A1C32 is needed for transient response performance of the three-terminal regulator.

2A-29. Inverter Inguard Supply

The inverter inguard supply provides three outputs: +5.3V dc (VDD) and -5.4V dc (VSS) for the inguard analog and digital circuitry, and +5.6V dc (VDDR) for the relays. Diodes A1CR5 and A1CR6, and capacitor A1C12 are for the +9.5 volt source, and diodes A1CR7 and capacitor A1C13 are for the -9.5V source.

Three-terminal regulator A1U6 regulates the 9.5V source to 5.6V for the relays. A1R5 and A1R6 set the output voltage at 5.6V. A1C6 is required for transient performance. The +5.3V regulator circuit uses A1Q2 for the series-pass element and A1Q4 as the error amplifier. A1VR2 is the reference for the positive supply. A1R14 provides the current to bias the reference zener. A1C4 is the output filter, and A1C9 provides frequency compensation of the regulator circuit. Transistor A1Q1 and resistor A1R13 make up the current-limit circuit.

When the voltage across A1R13 increases enough to turn on A1Q1, output current is limited by removing the base drive to A1Q2.

The -5.4 volt regulator operates like the +5.3 volt regulator, except that the NPN transistors in the positive supply are PNP transistors in the negative supply, and the PNP transistors in the positive supply are NPN transistors in the negative supply. If a VDD-to-VSS short circuit occurs, diode A1CR4 ensures that current limit occurs at the limit set for the -5.4V dc or +5.3V dc supply, whichever is lower.

2A-30. Power Fail Detection

The power fail detection circuit generates a signal to warn the Microprocessor that the power supply is going down. A comparator in A1U10 compares the divided-down raw supply voltage to a voltage reference internal to A1U10. When the raw supply voltage is greater than about 8V dc, the output of A1U10 is "high" and when the raw supply falls below 8V dc, the output goes "low". Resistors A1R19 and A1R20 make up the divider, and capacitor A1C74 provides filtering of high frequency noise at the comparator input. The reference voltage internal to A1U10 is nominally 1.3 volts dc.

2A-31. Digital Kernel

The Digital Kernel is composed of the following nine functional circuit blocks: the Reset Circuits, the Microprocessor, the Address Decoding, the Flash Memory, the Nonvolatile Static RAM and Real-Time Clock, the FPGA (Field Programmable Gate Array), the Serial Communication (Guard Crossing), the RS-232 Interface, and the Option Interface.

2A-32. Reset Circuits

The Power-On Reset signal (POR*, A1U10-7) is generated by the Microprocessor Supervisor, which monitors the voltage of VCC at A1U10-2. If VCC is less than +4.65 volts, then A1U10-7 will be driven low. POR* drives the enable inputs of the four tri-state buffers in A1U2, causing the HALT*, RESET*, ORST*, and DRST* signals to be driven low when POR* is low. When POR* goes high, the tri-state buffer outputs (A1U2) go to their high-impedance state and the pull-up resistors pull the outputs to a high level.

When HALT* and RESET* are both driven low, the Microprocessor (A1U1) is reset and will begin execution when they both go high. The Microprocessor may execute a "reset" instruction during normal operation to drive A1U1-92 low for approximately 10 microseconds to reset all system hardware connected to the RESET* signal.

The Display Reset signal (DRST*) is driven low by A1U2-6 when POR* is low, or it may be driven low by the Microprocessor (A1U1-56) if the instrument firmware needs to reset only the display hardware. For example, the firmware resets the display hardware after the FPGA is loaded at power-up and the Display Clock (DCLK) signal from the FPGA begins normal operation. This ensures that the Display Processor is properly reset while DCLK is active.

The Option Reset signal (ORST*) is driven low by A1U2-3 when POR* is low, or it may be driven low by the Microprocessor (A1U1-58) if the instrument firmware needs to reset only the Option Interface hardware. For example, the firmware resets any option interface hardware after the FPGA is loaded at power-up and the Option Clock (OCLK) signal from the FPGA begins normal operation. This ensures that any Option Interface hardware is properly reset while OCLK is active.

2A-33. Microprocessor

The Microprocessor uses a 16-bit data bus and a 19-bit address bus to access locations in the Flash Memory (A1U14 and A1U16), the Nonvolatile Static RAM (A1U20 and A1U24), the Real-Time Clock (A1U12), the FPGA (A1U25), the Memory Card Interface PCA (A6), and the Option Interface (A1J1). All of the data bus lines and the lowest 12 address lines have series termination resistors located near the Microprocessor (A1U1) to ensure that the instrument meets EMI/EMC performance requirements. When a memory access is done to the upper half of the data bus (D15 through D8), the upper data strobe (UDS*) goes low. When a memory access is done to the lower half of the data bus (D7 through D0), the lower data strobe (LDS*) goes low. When a memory access is a read cycle, R/W* must be high. Conversely for any write cycle, R/W* must be low.

The Microprocessor is a variant of the popular Motorola 68000 processor and is enhanced by including hardware support for clock generation, address decoding, timers, parallel ports, synchronous and asynchronous serial communications, interrupt controller, DMA (Direct Memory Access) controllers, and a watchdog timer.

The 12.288-MHz system clock signal (A1TP11) is generated by the oscillator circuit composed of A1U1, A1Y1, A1R2, A1C3, and A1C8. This clock goes through a series termination resistor (A1R107) to the FPGA (A1U25) and also through another series termination resistor (A1R86) to the Memory Card Interface (A1P4). These resistors are necessary to ensure that the instrument meets EMI/EMC performance requirements.

The Microprocessor has four software programmed address decoders that include wait state control logic. These four outputs are used to enable external memory and I/O components during read and write bus cycles. See "Address Decoding" for a complete description.

One sixteen-bit timer in the Microprocessor is used to generate a regular interrupt every 53.333 milliseconds. This timer uses the 12.288-MHz system clock (A1TP11) as a clock source. The timer changes the state of parallel port pin A1U1-113 each time that it interrupts the Microprocessor. The signal at A1U1-113 should be a 9.375-Hz square wave (period of 106.67 milliseconds).

Another 16-bit timer is used as the totalizer counter. The totalizer signal originating at J5-2 goes through the totalizer input buffer, the FPGA, and then to the external clock input for this timer in the Microprocessor (U1-114 and TP20). See the Totalizer part of "Digital I/O" for a complete description.

The Microprocessor has two parallel ports. Many of the parallel port pins are either used as software controlled signals or as inputs or outputs of timers and serial communication channels. Port A has 16 bits and Port B has 12 bits.

The Microprocessor communicates to the Display Controller using a synchronous, three-wire communication interface controlled by hardware in the Microprocessor. Information is communicated to the Display Controller to display user interface menus and measurement data. Details of this communication are described in the Display Controller Theory of Operation in this section.

The Microprocess communicated to the Microcontroller on the A/D Converter PCA (via the Serial Communication circuit) using an asynchronous communication channel at 4800 baud. Communication to the Microcontroller (A3U9) originates at A1U1-54. Communication from the A/D's Microcontroller to the Microprocessor appears at A1U1-53. When there is no communication in progress between the Microprocessor and the Microcontroller, both of these signals are high.

The Microprocessor uses another asynchronous communication channel to communicate to external computing or modem equipment through the RS-232 interface. This interface is described in detail in the RS-232 Interface Theory of Operation in this section.

The third asynchronous communication channel in the Microprocessor is connected to the Option Interface (J1) but is not used in the instrument at this time.

The interrupt controller in the Microprocessor prioritizes interrupts received from hardware devices both internal and external to the Microprocessor. Table 2A-1 lists interrupt sources from highest to lowest priority.

Table 2A-1. Microprocessor Interrupt Sources (2635A)

Pin	Signal Name	Description
A1U1-95	XTINT*	External Trigger Interrupt (Highest Priority)
A1U1-96	CINT*	Real-Time Clock Interrupt; once per second
A1U1-121	KINT*	Keyboard Interrupt; interrupts on each debounced change of keyboard conditions.
		RS-232 Interface Interrupt; internal to the Microprocessor.
		A/D Communication Interrupt; internal to the Microprocessor.
		Timer Interrupt every 53.333 milliseconds; internal to the Microprocessor.
A1U1-119	MCINT*	Memory Card Interface Interrupt; interrupts when a memory card is inserted, removed, powered up or powered down.
		Totalizer Interrupt; internal to the Microprocessor. Interrupts on totalizer overflow from a count of 65535 to 0.
A1U1-97	OINT*	Option Interface Interrupt; not currently used in this product.

The Microprocessor also has several internal DMA (Direct Memory Access) controllers that are used by the serial communication channels. Each serial communication channel has a DMA channel that handles character reception and another that handles character transmission. The use of these DMA controllers is transparent to the external operation of the Microprocessor, but it is important to understand that communication is handled at hardware speeds without the need for an interrupt for each character being transferred.

A watchdog timer internal to the Microprocessor is programmed to have a 10-second timeout interval. If the code executed by the Microprocessor fails to reinitialize the watchdog timer every 10 seconds or less, then A1U1-117 (POR*) is driven low for 16 cycles of SCLK (approximately 1.3 microseconds). This results in a complete hardware reset of the instrument, which restarts operation.

2A-34. Address Decoding

The four chip-select outputs on the Microprocessor are individual software programmed elements that allow the Microprocessor to select the base address, the size, and the number of wait states for the memory accessed by each output.

The FLASH* signal (A1U1-128) enables accesses to 128 kilobytes of Flash Memory (A1U14 and A1U16). The FLASH* signal goes through jumper W3, which must always be installed during normal instrument operation. W3 is removed only during the initial programming of the Flash Memory during production at the factory. The SRAM* signal enables the Nonvolatile Static RAM (A1U20 and A1U24), and the MCARD* signal goes to the Memory Card Interface PCA (A6). The I/O* signal goes to the I/O Decoder (A1U11), which decodes small areas of address space for I/O devices like the FPGA, the Real-Time Clock, and the Option Interface. There are no wait states for accesses to FLASH* and SRAM*, but two wait states are used for any access to I/O*. Each wait state adds approximately 83 nanoseconds to the length of a memory read or write cycle. The Memory Card Interface handles wait state timing for any accesses to MCARD*.

When the Microprocessor is starting up (also referred to as "booting"), the address decoding maps the address space as shown in Table 2A-2.

Table 2A-2. Booting Microprocessor Memory Map (2635A)

Hexadecimal Address	Device Selected
000000 - 03FFFF	Flash (A1U14 and A1U16)
100000 - 13FFFF	NVRAM (A1U20 and A1U24)
300000 - 30007F	FPGA Configuration (A1U25)
300080 - 3000FF	Real-Time Clock (A1U12)
300100 - 30017F	Option Interface (A1J1)
310000 - 311FFF	Memory Card Interface (A1P4)
400000 - 401000	Microprocessor Internal

Just before beginning execution of the instrument code, the address decoding is changed to map the address space as shown in Table 2A-3. This change switches the positions of Flash Memory and Nonvolatile Static RAM within the address space of the Microprocessor.

Table 2A-3. Instrument Microprocessor Memory Map (2635A)

Hexadecimal Address	Device Selected
000000 - 03FFFF	NVRAM (A1U20 and A1U24)
100000 - 13FFFF	Flash (A1U14 and A1U16)
300000 - 300007	FPGA Control / Status (A1U25)
300008 - 30000F	Alarm Outputs (A1U25)
300010 - 300017	Digital Outputs (A1U25)
300018 - 30001F (Read Only)	Digital Inputs (A1U25)
300020 - 300027 (Read Only)	Keyboard Input (A1U25)
300080 - 3000FF	Real-Time Clock (A1U12)
300100 - 30017F	Option Interface (A1J1)
310000 - 311FFF	Memory Card Interface (A1P4)
400000 - 401000	Microprocessor Internal

2A-35. Flash EPROM

The Flash EPROM is an electrically erasable and programmable memory that provides storage of instructions for the Microprocessor and measurement calibration data.

A switching power supply composed of A1U15, A1T3, A1CR21, and A1C66 through A1C69 generates a nominal +12 volt programming power supply (VPP) when the Microprocessor drives VPPEN high (A1U15-2). Resistor A1R35 pulls A1U15-2 to near ground during power-up to ensure that A1U15 is not enabled while the Microprocessor is being reset. When the power supply is not enabled, the output voltage (VPP) should be about 0.1 volt less than the input voltage of the power supply (VCC).

The only time that the programming power supply is active is when new firmware is being loaded or new calibration constants are being stored into the Flash EPROM. The code executed immediately after power-up is stored in an area of the Flash EPROM (known as the Boot Block) that is only eraseable and reprogrammable if BBVPP (A1U14-30 and A1U16-30) is at a nominal +12 volts. This may be accomplished by installing jumper A1W1, but this should only be done by a trained technican, and A1W1 should never be installed unless it is necessary to update the Boot firmware. In normal operation, resistor A1R73 and diode A1CR20 pull BBVPP up to about 0.25 volts less than VCC.

The FLASH* chip select (A1U1-128) for these devices goes low for any memory access to A1U14 or A1U16. The FLASH* signal goes through jumper W3, which must always be installed during normal instrument operation. W3 is removed only during the initial programming of the Flash Memory during production at the factory. A1U14 is connected to the high 8 bits of the data bus, so read accesses are enabled by the Read Upper (RDU*) signal going low, and write accesses are enabled by the Write Upper (WRU*) signal going low. A1U16 is connected to the low 8 bits of the data bus, so read accesses are enabled by the Read Lower (RDL*) signal going low, and write accesses are enabled by the Write Lower (WRL*) signal going low.

2A-36. NVRAM/Real-Time Clock

The Nonvolatile Static RAM (NVRAM) provides the storage of data and configuration information for the instrument. The Real-Time Clock maintains time and calendar date information for use by the instrument.

A nonvolatile power supply (VBB) biases A1U12, A1U20, A1U24, and A1U26. The Microprocessor Supervisor (A1U10) monitors the voltage on VCC (A1U10-2). If VCC is greater than the voltage of the lithium battery (A1U10-8), A1U10 switches VCC from A1U10-2 to A1U10-1 (VBB). If VCC drops below the voltage of the lithium battery (A1U10-8), A1U10 will switch voltage from lithium battery A1BT1 through current-limiting resistor A1R98 to A1U10-1 (VBB). The nominal current required from the lithium battery (A1BT1) at room temperature with the instrument powered down is approximately 2 microamperes. This can be easily measured by checking the voltage across A1R98.

The SRAM* address decode output (A1U1-127) for the 128 kilobytes of NVRAM goes low for any memory access to A1U20 or A1U24. This signal must go through two NAND gates in A1U26 to the NVRAM chip select inputs (A1U20-22 and A1U24-22). This ensures that when the instrument is powered down and A1U10-7 is driven low, A1U20-22 and A1U24-22 will be driven high so that the contents of the NVRAM cannot be changed and the power dissipated by the NVRAM is minimized. Jumper A1W4 in A<18> is not used in the current instrument; it should be installed only if more NVRAM is needed in a future instrument that needs 512 kilobytes of NVRAM using the same circuit board. A1U24 is connected to the high 8 bits of the data bus, so read accesses are enabled by the Read Upper (RDU*;A1U24-24) signal going low, and write accesses are enabled by the Write Upper (WRU*;A1U24-29) signal going low. A1U20 is connected to the low 8 bits of the data bus, so read accesses are enabled by the Read Lower (RDL*;A1U20-24) signal going low, and write accesses are enabled by the Write Lower (WRL*;A1U20-29) signal going low.

Memory accesses to the Real-Time Clock (A1U12) are enabled by the RTC* address decode output (A1U11-16). This signal must go through two NAND gates in A1U26 to the Real-Time Clock chip select input (A1U12-18). This ensures that when the instrument is powered down and A1U10-7 is driven low, A1U12-18 will be driven high so that the contents of the Real-Time Clock cannot be changed, and the power dissipated by the Real-Time Clock is minimized. A1U12 is connected to the low 8 bits of the data bus, so read accesses are enabled by the Read Lower (RDL*;A1U12-19) signal going low, and write accesses are enabled by the Write Lower (WRL*;A1U12-20) signal going low. When the instrument is powered up, the accuracy of the timebase generated by the internal crystal may be tested by measuring the frequency of the 1-Hz square wave output (A1U12-4). The Real-Time Clock also has an interrupt output (A1U12-3) that is used by the Microprocessor to time the interval between scans when a scan interval is set in the instrument. There should be one interrupt per second from the Real-Time Clock.

2A-37. Serial Communication (Guard Crossing)

The transmission of information from the Microprocessor (A1U1) to the Microcontroller (A3U9) is accomplished via the circuit made up of A1Q10, A1U7, A1R8, A1R16, and A3R8. The transmit output from the Microprocessor (A1U1-54) is buffered by A1Q10, which then switches current through optocoupler LED (A1U7-2). Resistor A1R8 limits the current through the LED.

The phototransistor in A1U7 responds to the light emitted by the LED when A1U1-54 is driven low. (The collector of the phototransistor, A1U7-5, goes low.) The phototransistor collector is pulled up by A3R8 on the A/D Converter PCA. When turning off, the phototransistor base discharges through A1R16. With this arrangement, the rise and fall times of the phototransistor collector signal are nearly symmetrical.

The transmission of data from the Microcontroller (A3U9) to the Microprocessor (A1U1) is accomplished via the circuit made up of A3Q1, A3R7, A1U5, A1R7, and A1R3. The transmit output from the Microcontroller (A3U9-14) is inverted by A3Q1, which drives the optocoupler LED (A1U5-2) through resistor A3R7. The current through the LED is limited by resistor A3R7. The phototransistor in A1U5 responds to the light emitted by the LED when A1U5-2 is driven low. (The collector of the phototransistor, A1U5-4, goes low.) The phototransistor collector (A1U5-5) is pulled up by resistor A1R3. When turning off, the phototransistor base discharges through A1R7. With this arrangement, the rise and fall times of the phototransistor collector signal are nearly symmetrical.

2A-38. Display/Keyboard Interface

The Microprocessor sends information to the Display Processor via a three-wire synchronous communication interface. The detailed description of the DISTX, DISRX, and DSCLK signals may be found in the detailed description of the Display PCA. Note that the DISRX signal is pulled down by resistor A1R1 so that Microprocessor inputs A1U1-49 and A1U1-118 are not floating at any time.

The Display Clock (DCLK) is a 1.024-MHz clock that is generated by the FPGA. Series resistor A1R85 is necessary to ensure that the instrument meets EMI/EMC performance requirements. The Display Assembly is reset when the Display Reset (DRST*) signal is driven low. The reset circuit on the Display Assembly is discharged through resistor A1R21, which limits the peak current from A2C3. DRST* is driven low at power-up, or it may be driven low by the Microprocessor (A1U1-56).

The Keyboard interface is made up of six bidirectional I/O lines from the Field Programmable Gate Array (FPGA). SWR1 through SWR6 (A1U25-67, A1U25-68, A1U25-71, A1U25-73, A1U25-70, A1U25-69, respectively) are pulled up by A2Z1 on the Display PCA. Hardware in the FPGA scans the keyboard switch array, detects and debounces switch changes, and interrupts the Microprocessor to indicate that a debounced keypress is available. A detailed description of this may be found under the following heading "Field Programmable Gate Array (FPGA)".

2A-39. Field Programmable Gate Array (FPGA)

The FPGA is a complex programmable logic device that contains the following six functional elements after the Microprocessor has loaded the configuration into the FPGA: Clock Dividers, Internal Register Address Decoding, Keyboard Scanner, Digital I/O Buffers and Latches, Totalizer Debouncing and Mode Selection, and the External Trigger Logic.

When the instrument is powered up, the FPGA clears its configuration memory and waits until RESET* (A1U25-78) goes high. The FPGA then tests its mode pins and should determine that it is in "peripheral" configuration mode (A1U25-54 high; A1U25-52 low; A1U25-56 high). In this mode the Microprocessor must load the configuration information into the FPGA before the FGPA logic can begin operation.

The Microprocessor first makes sure that the FPGA is ready to be configured by driving XD/P* (A1U25-80) low and then pulsing the RESET* (A1U25-78) input low for about 10 microseconds. The Microprocessor then waits until the XINIT* (A1U25-65) output goes high, indicating that the FPGA has been initialized and is ready for configuration. The Microprocessor then writes a byte of configuration data to the FPGA by driving PGA* (A1U25-88) low and latching the data on the data inputs (D<8> through D<15>) by pulsing WRU* (A1U25-5) low and then back high. The XRDY (A1U25-99) output then goes low to indicate that the FPGA is busy loading that configuration byte. The Microprocessor will then wait until XRDY goes high again before loading the next configuration byte, and the sequence is repeated until the last byte is loaded. While the configuration data is being loaded, the FPGA drives the XD/P* signal (A1U25-80) low. When the FPGA has been completely configured, the XD/P* signal is released and pulled high by resistor A1R70. The Microprocessor will repeat the configuration sequence if XD/P* (A1U25-80) does not go high when it is expected to.

Clock Dividers

The 12.288-MHz system clock (A1U25-30) is divided down by the Clock Dividers to create the 3.072-MHz Option Clock (OCLK; A1U25-22) and 1.024-MHz Display Clock (DCLK; A1U25-19). The Display Clock is not a square wave; it is low for 2/3 of a cycle and high for the other 1/3. The Display Clock is also used internal to the FPGA to create the 128-kHz Totalizer Debouncer Clock and the 4-kHz Keyboard Scanner Clock.

Internal Register Address Decoding

The FPGA logic decodes four bits of the address bus (A<3> through A<6>), the PGA* chip select signal (A1U25-88), RDU* (A1U25-95), and WRU* (A1U25-5) to allow the Microprocessor to read five registers and write to three registers implemented in the FPGA logic. The absolute addresses are listed in Table 2A-1.

Keyboard Scanner

The Keyboard Scanner sequences through the array of switches on the Display Assembly to detect and debounce switch closures. After a switch closure is detected, it must remain closed for at least 16 milliseconds before the Microprocessor will be interrupted and the Keyboard Input register will be read from the FPGA. When the keyboard interrupt (KINT*, A1U25-62) goes low, the Keyboard Scanner stops scanning until the Microprocessor reads the Keyboard Input register which automatically clears the interrupt by driving KINT* high again. The FPGA will interrupt the Microprocessor again when the switch on the Display Assembly is detected as open again. Actually the Microprocessor will be interrupted once for each debounced change in the contents of the Keyboard Input register. See also the information on "Front Panel Switches" in the "Display PCA" section for this instrument.

The Microprocessor can enable or disable the Keyboard Scanner by changing the state of a bit in the Control/Status register that is in the FPGA. The Keyboard Scanner is disabled if the instrument is in either the RWLS or LWLS state (see User Manual; RWLS and LWLS Computer Interface Commands).

Digital I/O Buffers and Latches

The FPGA logic implements internal registers for the eight Digital Outputs (DO<0> through DO<7>) and the four Alarm Outputs (AO<0> through AO<3>). These registers are both written and read by the Microprocessor. The FPGA logic also implements an eight-bit input buffer so that the Microprocessor can read the eight Digital Input lines (DI<0> through DI<7>). See also "Digital Input Buffers" and "Digital and Alarm Output Drivers".

Totalizer Debouncing and Mode Selection

Logic internal to the FPGA lets the Microprocessor enable a debouncer in the Totalizer input signal path. The detailed description of the Totalizer Debouncer and Mode Selection may be found under the heading "Totalizer Input".

External Trigger Logic

Logic internal to the FPGA allows the Microprocessor to set up the External Trigger Logic to interrupt on rising or falling edges of the XTI input to the FPGA. The detailed

description of the External Trigger operation may be found in the "External Trigger Input Circuits" section.

2A-40. RS-232 Interface

The RS-232 interface is composed of connector A1J4, RS-232 Driver/Receiver A1U13, and the serial communication hardware in Microprocessor A1U1.

The serial communication transmit signal (A1U1-80) goes to the RS-232 driver (A1U13-14), where it is inverted and level shifted so that the RS-232 transmit signal transitions between approximately +5.0 and -5.0V dc. When the instrument is not transmitting, the driver output (TP13;A1U13-3) is approximately -5.0V dc. The RS-232 receive signal from A1J4 goes to the RS-232 receiver A1U13-4, which inverts and level shifts the signal so that the input to the serial communication hardware transitions between 0 and +5.0V dc. When nothing is being transmitted to the instrument, the receiver output (TP12;A1U13-13) is +5.0V dc.

Data Terminal Ready (DTR) and Request To Send (RTS) are modem control signals controlled by the Microprocessor. When the instrument is powered up, the Microprocessor initially sets DTR and RTS false by setting A1U1-61 and A1U1-79 high, which results in the RS-232 driver outputs (A1U13-7 and A1U13-5 respectively) going to -5.0V dc. When the instrument has initialized the RS-232 interface and is ready to receive and transmit, A1U1-61 and A1U1-79 will go low, resulting in the RS-232 DTR and RTS signals going to +5.0V dc. The RS-232 DTR and RTS signals will remain at +5.0V dc until the instrument is powered down except for a short period of time when the user changes RS-232 communication parameters from the front panel of the instrument.

Clear To Send (CTS) and Data Set Ready (DSR) are modem control inputs from the attached RS-232 equipment. Of these signals, only CTS is used when CTS flow control is enabled when CTS is turned on via the RS-232 communication setup menu. The CTS modem control signal from A1J4 goes to the RS-232 receiver A1U13-6, which inverts and level shifts the signal so that the input to the Microprocessor (A1U1-51) transitions between 0 and +5.0V dc. When the instrument is cleared to send characters to the RS-232 interface, the receiver output (A1U13-11) is +5.0V dc. If the RS-232 CTS signal is not driven by the attached RS-232 equipment, the receiver output (A1U13-11) is near 0V dc.

2A-41. Option Interface

The interconnection to the option slot is implemented by J1 on the Main PCA. This connector (A1J1) routes the outguard logic power supply (VCC and GND), eight bits of the data bus (D<8> through D<15>), RDU*, WRU*, OCLK, RESET*, OPTE*, and the lower three bits of the address bus to the hardware installed in the option slot. This connector also routes an interrupt signal (OINT*) from the option hardware to the IRQ1* input of the Microprocessor (A1U1-97). The OPTE*, RDU*, and WRU* signals pass through series resistors that are necessary to ensure that the instrument meets EMI/EMC performance requirements.

An option sense signal from the installed option allows the Microprocessor to detect whether or not option hardware is installed. Currently there is no optional hardware available for this instrument.

2A-42. Digital I/O

The following paragraphs describe the Digital Input Threshold, Digital Input Buffers, Digital and Alarm Output Drivers, Totalizer Input, and External Trigger Input circuits.

2A-43. Digital Input Threshold

The Digital Input Threshold circuit sets the input threshold level for the Digital Input Buffers and the Totalizer Input. A fixed value voltage divider (A1R36, A1R37) and a unity gain buffer amplifier (A1U8) are the main components in this circuit. The voltage from the divider (approximately +1.4V dc) is then buffered by A1U8, which sets the input threshold. Capacitor A1C29 filters the divider voltage at the input of A1U8.

2A-44. Digital Input Buffers

Since the eight Digital Input Buffers are identical in design, only components used for Digital Input 0 are referenced in this description. If the Digital Output Driver (A1U17-12) is off, the input to the Digital Input Buffer is determined by the voltage level at A1J5-10. If the Digital Output Driver is on, the input of the Digital Input Buffer is the voltage at the output of the Digital Output Driver.

The Digital Input Threshold circuit and resistor network A1Z1 determine the input threshold voltage and hysteresis for inverting comparator A1U3. The inverting input of the comparator (A1U3-13) is protected by a series resistor (A1Z3) and diode A1CR14. A negative input clamp circuit (A1Q9, A1Z2, and A1CR17) sets a clamp voltage of approximately +0.7V dc for the protection diodes of all Digital Input Buffers. A negative input voltage at A1J5-10 causes A1CR14 to conduct current, clamping the comparator input A1U3-13 at approximately 0V dc.

The input threshold of +1.4V dc and a hysteresis of +0.5V dc are used for all Digital Input Buffers. When the input of the Digital Input Buffer is greater than approximately +1.25V dc, the output of the inverting comparator is low. When the input then drops below about +0.75V dc, the output of the inverting comparator goes high.

2A-45. Digital and Alarm Output Drivers

Since the 12 Digital Output and Alarm Output Drivers are identical in design, the following example description references only the components that are used for Alarm Output Driver 0.

The Microprocessor controls the state of Alarm Output Driver 0 by writing to the Alarm Output register in the FPGA (A1U25) to set the level of output A1U25-63. When A1U25-63 is set high, the output of the open-collector Darlington driver (A1U17-16) sinks current through current-limiting resistor A1R62. When A1U25-63 is set low, the driver output turns off and is pulled up by A1Z2 and/or the voltage of the external device that the output is driving. If the driver output is driving an external inductive load, the internal flyback diode (A1U17-9) conducts the energy into MOV A1RV1 to keep the driver output from being damaged by excessive voltage. Capacitor A1C58 ensures that the instrument meets electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance requirements.

2A-46. Totalizer Input

The Totalizer Input circuit consists of Input Protection, a Digital Input Buffer circuit, and a Totalizer Debouncing circuit. The Digital Input Buffer for the totalizer is protected from electrostatic discharge (ESD) damage by A1R49 and A1C43. Refer to the detailed description of the Digital Input Buffer circuit for more information.

The Totalizer Debounce circuit in the FPGA (A1U25) allows the Microprocessor to select totalizing of either the input signal or the debounced input signal. The buffered Totalizer Input signal (TOTI*) goes into the FPGA at A1U25-12. Inside the FPGA, the totalizer signal is routed to the Totalizer Output (TOTO, A1U25-8) which then goes to a 16-bit counter in the Microprocessor (A1U1-114; TP20).

The actual debouncing of the input signal is accomplished by A1U25. Counters divide the 12.288-MHz system clock down to 128 kHz for the debouncing circuit. An EXOR gate compares the input signal (TOTI*) and the latched output of the debouncer. If these signals differ, the EXOR gate output goes high, enabling the debouncer. If the input remains stable for 1.75 milliseconds, the totalizer output (TOTO, A1U25-8) changes state. If the input does not remain stable for 1.75 milliseconds, the totalizer output does not change state. For a stable totalizer input of +5V dc, the totalizer output (TOTO, A1U25-8) will be 0.0V dc. For a stable totalizer input of +0.0V dc, the totalizer output (TOTO, A1U25-8) will be +5V dc.

2A-47. External Trigger Input Circuits

The External Trigger Input circuit can be configured by the Microprocessor to interrupt on a rising or falling edge of the XT* input (A1J6-2) or to not interrupt on any transitions of the XT* input. The falling edge of the XT* input is used by the instrument firmware as an indication to start scanning, and the rising edge is used as an indication to stop scanning.

The External Trigger Input is pulled up to +5V dc by A1Z2 and is protected from electrostatic discharge (ESD) damage by A1R58, A1C54, A1Z3, and A1CR15. Capacitor A1C54 helps ensure that the instrument meets EMI/EMC performance requirements.

The input (XTI) is then routed to the FPGA (A1U25), which contains the External Trigger control circuitry. The Microprocessor sets control register bits in the FPGA (A1U25) to control the external trigger circuit. The External Trigger control circuit output (A1U25-9) drives the non-maskable interrupt on the Microprocessor (A1U1-95).

If External Triggering is enabled (see User Manual), the Microprocessor sets FPGA control register bits to allow a low level on the XT* input to cause the External Trigger Interrupt (XTINT*; A1U25-9) to go low. The Microprocessor then changes the FPGA control register bits to allow a high level on the XT* input to cause XTINT* (A1U25-9) to go low. Thus the Microprocessor can detect both rising and falling edges on the XT* input. Normally, the XTINT* output of the FPGA (A1U25-9) should be low only for a few microseconds at any time. If it is held low constantly, the instrument will not be able to operate. Resistor A1R64 pulls the XTINT* output high to ensure that it is high during power-up.

2A-48. A/D Converter PCA

The following paragraphs describe the operation of the circuits on the A/D Converter PCA. The schematic for this pca is located in Section 8.

2A-49. Analog Measurement Processor

Refer to Figure 2A-3 for an overall picture of the Analog Measurement Processor chip and its peripheral circuits. Table 2A-4 describes Analog Measurement Processor chip signal names.

The Analog Measurement Processor (A3U8) is a 68-pin CMOS device that, under control of the A/D Microcontroller (A3U9), performs the following functions:

- Input signal routing
- Input signal conditioning
- Range switching

- Passive filtering of dc voltage and resistance measurements
- Active filtering of ac voltage measurements
- A/D conversion
- Support for direct volts, true rms ac volts, temperature, resistance,and frequency measurements

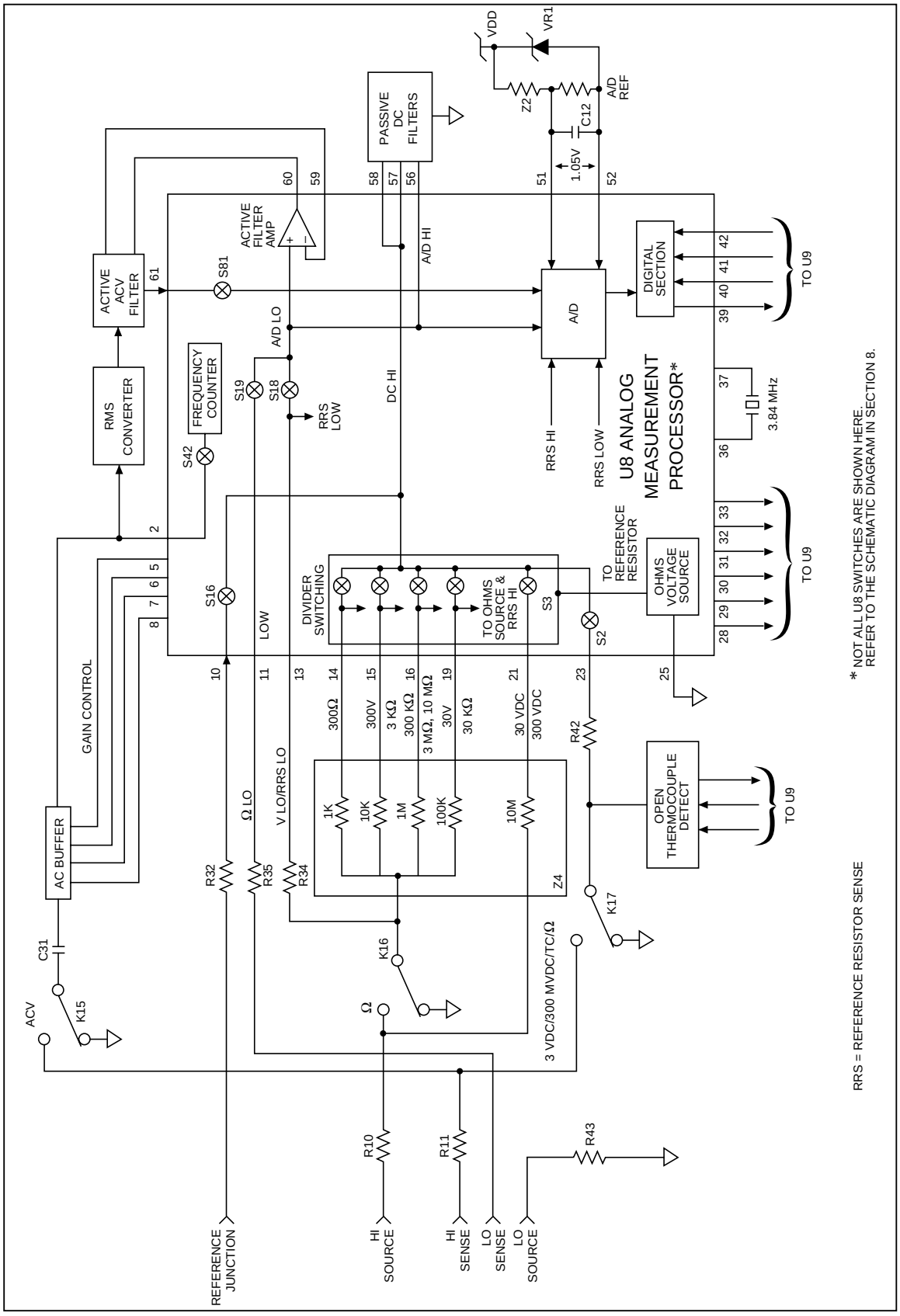


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Figure 2A-3. Analog Simplified SchematicDiagram (2635A)

Table 2A-4. Analog Measurement Processor Pin Descriptions (2635A)

Pin	Name	Description
1	VDD	+5.4V supply
2	ACBO	AC buffer output
3	AIN	(not used)
4	AGND2	Analog ground
5	ACR4	AC buffer range 4 (300V)
6	ACR3	AC buffer range 3 (30V)
7	ACR2	AC buffer range 2 (3V)
8	ACR1	AC buffer range 1 (300 mV)
9	VSSA	-5.4V supply for AC ranging
10	REFJ	Reference junction input
11	DCV	A/D converter low input
12	LOW	Driven guard
13	GRD	Reference resistor sense for ohms
14	RRS	Tap #4 on the DCV input divider/ohms reference network
15	V4	Tap #3 on the DCV input divider/ohms reference network
	V3	
16	V1	Tap #1 on the DCV input divider/ohms reference network
17	GRD	Driven guard
18	V2F	Tap #2 input on the DCV input divider/ohms reference network
19	V2	Tap #2 on the DCV input divider/ohms reference network
20	GRD	Driven guard
21	V0	Tap #0 on the DCV input divider/ohms reference network
22	GRD	Driven guard
23	OVS	Ohms and volts sense input
24	GRD	Guard
25	AGND1	Analog ground
26	-	(not used)
27	DGND	Analog ground
28	FC0	Function control #0
29	FC1	Function control #1
30	FC2	Function control #2
31	FC3	Function control #3
32	FC4	(not used)
33	FC5	(not used)
34	FC6	Function control #6
35	FC7	Function control #7
36	XIN	Crystal oscillator input
37	XOUT	Crystal oscillator output
38	MRST	Master reset
39	AS	Analog send
40	AR	Analog receive
41	SK	Serial clock
42	CS	Chip select
43	BRS	(not used)
44	VSS	-5.4V dc
45	INT	Integrator output
46	SUM	Integrator summing node
47	B.1	Buffer output, 100 mV range
48	B.32	Buffer output, 300 mV range
49	B1	Buffer output, 1000 mV range
50	B3.2	Buffer output, 3V range

Table 2A-4. Analog Measurement Processor Pin Descriptions (2635A) (cont)

Pin	Name	Description
51	VREF+	A/D voltage reference plus
52	VREF-	A/D voltage reference minus
53	RAO	A/D reference amplifier output
54	RA+	A/D reference amplifier noninverting input
55	RA-	A/D reference amplifier inverting input
56	AFO	Passive filter 2
57	MOF	Passive filter 1 plus resistance
58	AFI	Passive filter 1
59	FAI	Filter amplifier inverting input
60	FAO	Filter amplifier output
61	RMSF	RMS output, filtered
62	AGND3	(not used, connected to filtered -5.4V dc)
63	RMSG2	(not used)
64	RMSO	RMS converter output
65	CAVG	(not used)
66	VSSR	-5.4V dc, filtered
67	RMSG1	(not used, pulled to filtered -5.4V dc)
68	RMSI	(not used)

Two separate signal paths are used, one for dc/ohms/temperature and one for ac. The volts dc (3V range and below) and temperature voltages are coupled directly to the a/d converter, while higher voltages are attenuated first. For ohms, the dc circuitry is augmented with an internal ohms source voltage regulator controlled through an extra set of switches. For volts ac, inputs are routed through the ac buffer, which uses the gain selected by the Measurement Processor (A3U8).

The a/d converter uses a modified dual-slope minor cycle method. The basic measurement unit, a minor cycle, consists of a fixed time integrate period for the unknown input, a variable time reference integrate period, a variable time hold period, and various short transition periods. A minor cycle period lasts for 25 ms or until a new minor cycle is begun, whichever comes first.

2A-50. Input Protection

The instrument measurement circuits are protected when overvoltages are applied through the following comprehensive means:

- Any voltage transients on channel 0 HI or LO terminals areimmediately clamped to a peak of about 1800V or less by MOVs A3RV1and A3RV2. (This is much lower than the 2500V peaks that can beexpected on 240 VAC, IEC 664 Installation Category II, ac mains.)
- Fusible resistors A3R10 and A3R11 protect the measurement circuitryin all measurement modes by limiting currents.
- A3Q11 clamps voltages exceeding 0.7V below and approximately 6.0Vabove analog common (LO) or LO SENSE, with A3R35 limiting the inputcurrent.
- A3Q10 clamps voltages during ohms measurements with A3RT1, A3R34,A3R10, and A3Z4 limiting the input current. With large overloads,thermistor A3RT1 will heat up and increase in resistance.
- A3U8 also clamps voltages on its measurement input pins that exceedthe VDD and VSS supply rails. Resistors A3R42, A3R11, A3R10, A3RT1,A3Z4, A3R35, and A3R34 limit any input currents.
- Any excessive voltages that are clamped through A3U8 to VDD or VSS,are then also clamped by zener diodes A3VR3 and A3VR2.

- The open thermocouple detect circuitry is protected against voltagetransient damage by A3Q14 and A3Q15.
- When measuring ac volts, the ac buffer is protected by dual-diodeclamp A3CR1 and resistor network A3Z3.
- Switching induced transients are also clamped by dual-diodeA3CR4 and capacitor A3C33, and limited by resistor A3R33.

2A-51. Input Signal Conditioning

Each input is conditioned and/or scaled to a dc voltage appropriate for measurement by the a/d converter. DC voltage applied to the a/d converter can be handled on internal ranges of 0.1V, 0.3V, 1V, or 3V. Therefore, high-voltage dc inputs are scaled, and ohms inputs are converted to a dc voltage. Line voltage level ac inputs are first scaled and then converted to a dc voltage. Noise rejection is provided by passive and active filters.

2A-52. Function Relays

Latching relays A3K15, A3K16, and A3K17 route the input signal to the proper circuit blocks to implement the desired measurement function. These relays are switched when a 6-millisecond pulse is applied to the appropriate reset or set coil by the NPN Darlington drivers in IC A3U10. The A/D Microcontroller A3U9 controls the relay drive pulses by setting the outputs of port 6. Since the other end of the relay coil is connected to the VDDR supply, a magnetic field is generated, causing the relay armature and contacts to move to (or remain in) the desired position. Function relay states are defined in Table 2A-5.

Table 2A-5. Function Relay States (2635A)

Relay Position			
Function	**A3K17**	**A3K16**	**A3K15**
DC mV, 3V,Thermocouples	Reset	Set	Set
DC 30V, 300V	Set	Set	Set
ACV	Set	Set	Reset
Ohms, RTDs	Reset	Reset	Set
Frequency	Set	Set	Reset

2A-53. DC Volts and Thermocouples

For the 3V and lower ranges (including thermocouples), the HI input signal is applied directly to the A3U8 analog processor through A3R11, A3K17, and A3R42. Capacitor A3C27 filters this input, which the analog processor then routes through S2 and other internal switches, through the passive filter, and to the internal a/d converter. The LO SENSE signal is applied to A3U8 through A3R35 and routed through internal switch A3U8-S19 to LO of the a/d converter.

Guard signals MGRD and RGRD are driven by an amplifier internal to A3U8 to a voltage appropriate for preventing leakage from the input HI signal under high humidity conditions.

For the 30V range, the HI signal is scaled by resistor network A3Z4. Here, the input is applied to pin 1 of A3Z4 so that an approximate 100:1 divider is formed by the 10-MΩ and 100.5-kΩ resistors in A3Z4 when analog processor switches S3 and S13 are closed. The attenuated HI input is then sent through internal switch S12 to the passive filter and the a/d converter. Input LO is sensed through analog processor switch S18 and resistor A3R34.

For the 300V range (Figure 2A-4), the HI signal is again scaled by A3Z4. The input is applied to pin 1 of A3Z4, and a 1000:1 divider is formed by the 10-MΩ and 10.01-kΩ resistors when switches S3 and S9 are closed in A3Z4. The attenuated HI input is then sent through internal switch S10 to the passive filter and the a/d converter. LO is sensed through analog processor switch S18 and resistor A3R34.

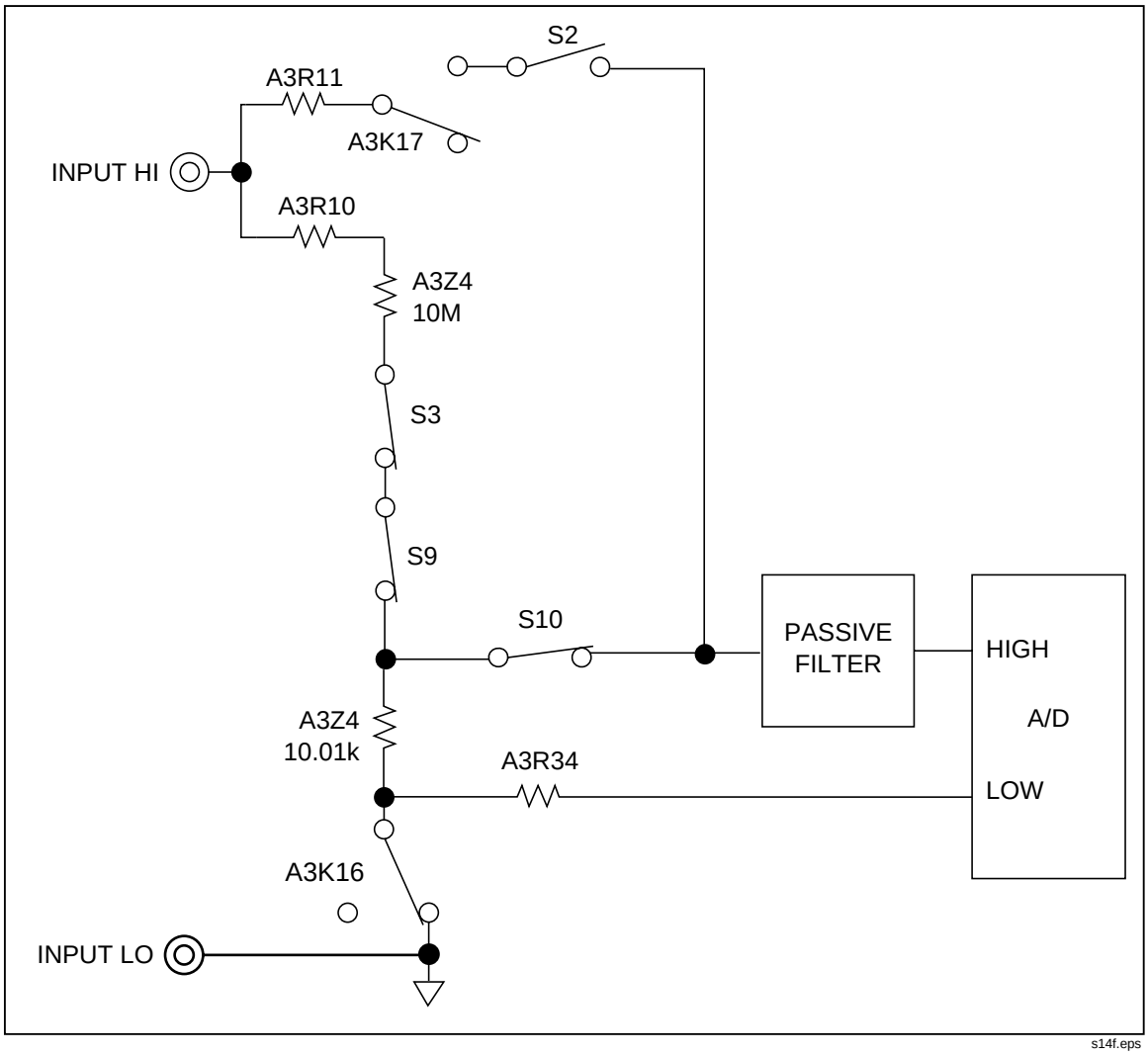


Figure 2A-4. DC Volts 300V Range Simplified Schematic (2635A)

2A-54. Ohms and RTDs

Resistance measurements are made using a ratio ohms technique, as shown in Figure 2A-5. A stable voltage source is connected in series with the reference resistor in A3Z4 and the unknown resistor. Since the same current flows through both resistors, the unknown resistance can be determined by multiplying the ratio of the voltage drops across the reference and the unknown resistors by the known reference resistor value.

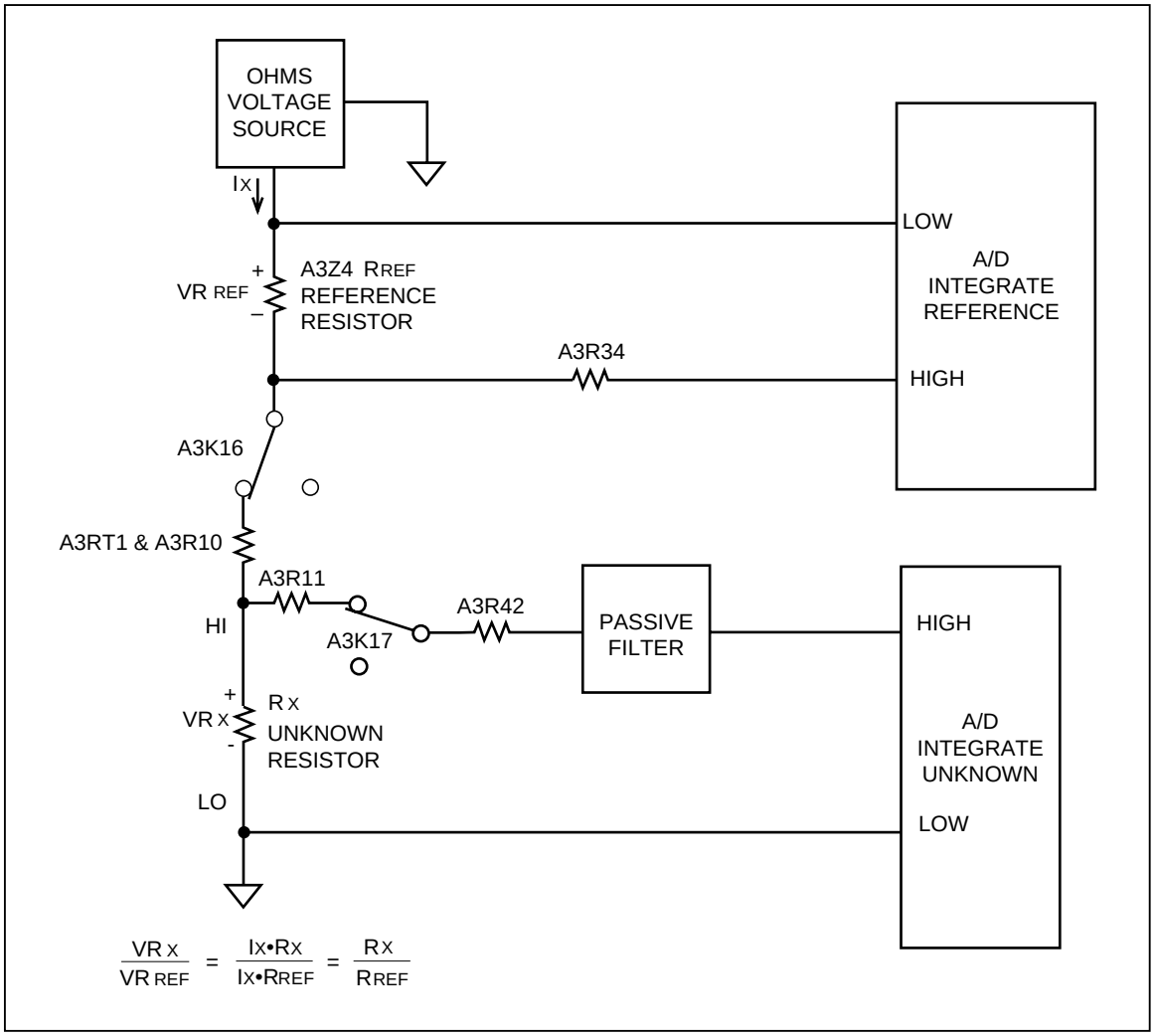


Figure 2A-5. Ohms Simplified Schematic (2635A)

For the RTD, 300Ω, 3-kΩ, and 30-kΩ ranges, the ratio technique is implemented by integrating the voltage across the unknown resistance for a fixed period of time and then integrating the negative of the voltage across the reference resistance for a variable time period. In this way, each minor cycle result gives the ratio directly.

For the 300-kΩ, 3-MΩ, and 10-MΩ ranges, the ratio is determined by performing two separate voltage measurements in order to improve noise rejection. One fixed-period integration is performed on the voltage across the unknown resistance, and the second integration is performed on the voltage across the reference resistance. The ratio of the two fixed-period voltge measurements is then computed by Microcontroller A3U9. The resistance measurement result is determined when A3U9 multiplies the ratio by the reference resistance value.

When an input is switched in for a measurement, the ohms source in Analog Processor A3U8 is set to the correct voltage for the range selected and is connected to the appropriate reference resistor in network A3Z4. A measurement current then flows through A3Z4, relay A3K16, thermistor A3RT1, resistor A3R10, the unknown resistance, A3R43, ground, and the ohms source.

The resulting voltage across the unknown resistance is integrated for a fixed period of time by the A/D Converter through the HI SENSE path of A3R11, A3K17, A3R42 and

A3U8 switch S2, and the LO SENSE path of A3R35 and Analog Processor switch S19. Passive filtering is provided by A3C34, A3C27, and portions or all of the DC Filter block.

The voltage across the reference resistor for the 300Ω and RTD, 3-kΩ, and 30-kΩ ranges (the 1-kΩ, 10.01-kΩ, and 100.5-kΩ resistances in A3Z4, respectively) is integrated for a variable period of time until the voltage across the integrate capacitor reaches zero. For the 300Ω and RTD range, the reference resistor voltage is switched in through Analog Processor switch S6 and applied to the A/D Converter by switch S8. For the 3-kΩ range, switches S9 and S11 perform these functions, respectively. For the 30-kΩ range, switches S13 and S14 are used. For all ranges, the voltage is routed through A3R34 to the RRS input.

The reference resistor for the 300-kΩ, 3-MΩ, and 10-MΩ ranges is the 1-MΩ resistor in A3Z4, which is selected by S15. The voltage across this reference is integrated during its own minor cycle(s) and is switched to a passive filter and the A/D Converter by switches S1 and S18.

When 4-wire measurements are made on any of the six ranges, separate Source and Sense signal paths are maintained to the point of the unknown resistance. The 4-wire Source path measurement current is provided by the A3U8 ohms source through one of the A3U8 internal switches (S6, S9, S13, or S15) and the appropriate reference resistor in A3Z4. The current flows through relay A3K16, thermistor A3RT1, resistor A3R10, the HI Source instrument relay contacts (A3K1 - A3K3, A3K5 - A3K14), and the HI Source lead wire, to the unknown resistance to be measured. The current flows back through the LO Source lead wire, the LO Source path of the instrument relays (A3K1 - A3K3, A3K5 - A3K14), resistor A3R43, and analog ground, to the A3U8 ohms source.

The voltage that develops across the unknown resistance is sensed through the other 2 wires of the 4-wire set. HI is sensed through the HI Sense path made up of the users HI Sense lead wire, the HI Sense contacts in the instrument relays, resistor A3R11, relay A3K17, resistor A3R42, and Analog Processor A3U8 switch S2. LO is sensed through the users LO Sense lead wire, the LO Sense contacts in the instrument relays, protection resistor A3R35, and A3U8 switch S19.

Since virtually no current flows through the sense path, no error voltages are developed that would add to the voltage across the unknown resistance; this 4-wire measurement technique eliminates user lead-wire and instrument relay contact and circuit board trace resistance errors.

2A-55. AC Volts

AC-coupled ac voltage inputs are scaled by the ac buffer, converted to dc by a true rms ac-to-dc converter, filtered, and then sent to the a/d converter.

Refer to Figure 2A-6. Input HI is switched to the ac buffer by dc-blocking capacitor A3C31, protection resistor A3R11, and latching relay A3K15. Resistor A3R44 and A3K15 act to discharge A3C31 between channel measurements. LO is switched to the A3U8 A/D Converter through A3R34 and S18.

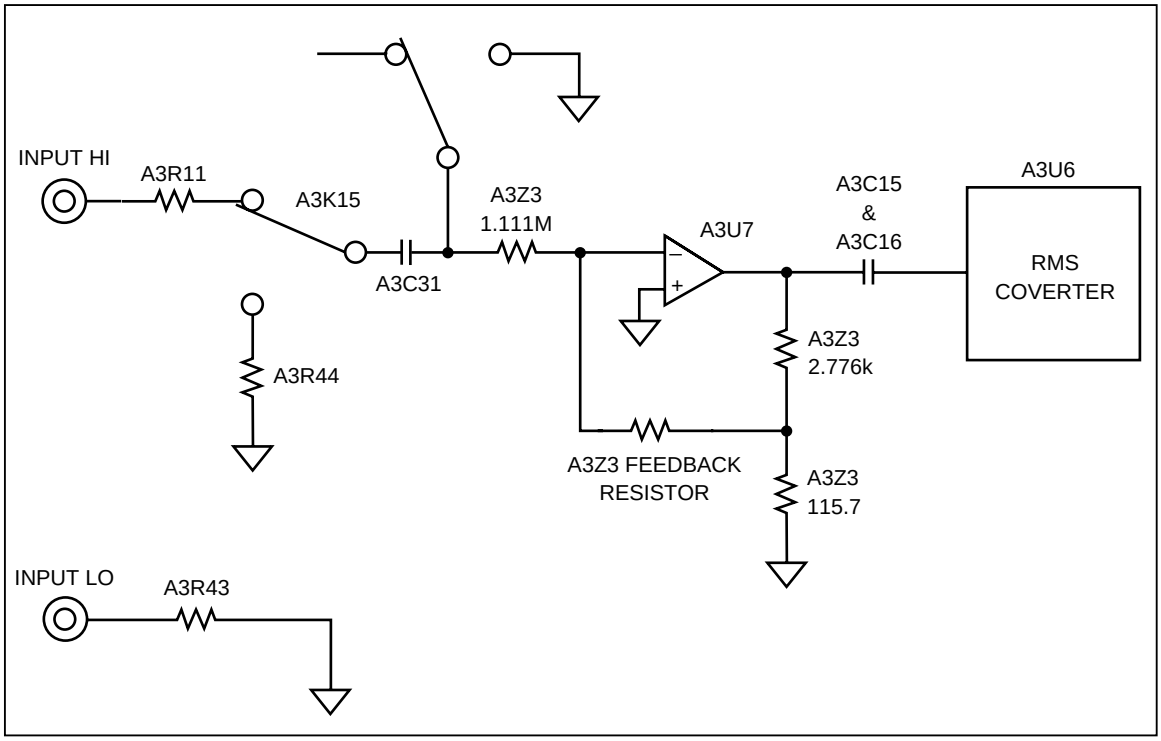


Figure 2A-6. AC Buffer Simplified Schematic (2635A)

JFETs A3Q3 through A3Q9 select one of the four gain (or attenuation) ranges of the buffer (wide-bandwidth op-amp A3U7.) The four JFET drive signals ACR1 through ACR4 turn the JFETs on at 0V and off at -VAC. Only one line at a time will be set at 0 volts to select a range.

The input signal to the buffer is first divided by 10, 100, or 1000 for the 300 mV, 3V, and 30V ranges, respectively. The resistance ratios used are summarized in Table 2A-6. Note that the 111.1-kΩ resistor is left in parallel with the smaller (higher attenuation) resistors. The attenuated signal is then amplified by A3U7, which is set for a gain of 25 by the 2.776-kΩ and 115.7Ω resistors in A3Z3. Components A3R27 and A3C23 compensate high-frequency performance on the 300 mV range. For the 300V range, overall buffer gain is determined by the ratio of the 2.776-kΩ feedback resistor to the 1.111-MΩ input resistor.

Table 2A-6. AC Volts Input Signal Dividers (2635A)

Range	Drive Signal	A3Z3 Divider Resistor(s)	Overall Gain
300 mV	ACR1	111.1 kΩ	2.5
3V	ACR2	12.25 kΩ || 111.1 kΩ	0.25
30V	ACR3	1.013 kΩ || 111.1 kΩ	0.025
150/300V	ACR4	none	0.0025

The output of the buffer is ac-coupled by A3C15 and A3C16 to the true-rms ac-to-dc converter A3U6. Discharge JFET A3Q13 is switched on to remove any excess charge from the coupling capacitors A3C15 and A3C16 between channel measurements. A3C17 provides an averaging function for the converter, and resistor network A3Z1 divides the output by 2.5 before sending the signal to the active ac volts filter. Analog processor switch S81 connects the output of the active filter to HI of the A/D Converter. Components A3R29, A3R30, A3C26, and A3C28 provide filtered power supplies (+VAC and -VAC) for the ac buffer, the ac switch JFETs, and the rms converter.

2A-56. Frequency

After any dc component is blocked by capacitors A3C15, A3C16, and A3C31, the output of the ac buffer is used to determine the input frequency. This signal is sent to the ACBO pin of analog processor A3U8 and switched to the internal frequency comparator and counter circuit by S42.

2A-57. Passive and Active Filters

The passive filters are used for the dc voltage and ohms measurements. For most ranges, capacitors A3C14 and A3C11 are switched into the measurement circuit in front of the A3U8 A/D Converter by switches S86, S87, and S88. These capacitors act with the 100-kΩ series resistance provided by A3R42 or A3Z4 to filter out high-frequency noise. For the 300-kΩ range, only A3C14 is switched in by switches S86 and S85. For the 3-MΩ and 10-MΩ ranges, A3C11 or A3C14 are not switched in to keep settling times reasonably short.

Between channel measurements, the passive filters are discharged by JFET A3Q2 under control of Microcontroller A3U9 through comparator A3U14. When the ZERO signal is asserted, A3R14 pulls the gate of A3Q2 to ground, turning the JFET on and discharging A3C11. At the same time, zeroing of filter capacitors A3C14 and A3C27 is accomplished by having the Analog Processor turn on internal switches S2, S86, and S87.

The active filter is only used for ac voltage measurements. This three-pole active filter removes a significant portion of the ac ripple and noise present in the output of the rms converter without introducing any additional dc errors. The active filter op-amp within A3U8, resistors A3R20, A3R17, and A3R16, and capacitors A3C7, A3C10, and A3C6 form the filter circuit. This filter is referenced to the LO input to the a/d converter within A3U8 by the op-amp. The input to the filter is available at the RMSO pin, and the output is sent to the RMSF pin of A3U8. Switches S80 and S82, which are turned on prior to each new channel measurement, cause the filter to quickly settle (pre-charge) to near the proper dc output level.

2A-58. A/D Converter

Figure 2A-7 shows the dual slope a/d converter used in the instrument. The unknown input voltage is buffered and used to charge (integrate) a capacitor for an exact period of time. This integrator capacitor is then discharged by the buffered output of a stable and accurate reference voltage of opposite polarity. The capacitor discharge time, which is proportional to the level of the unknown input signal, is measured by the digital circuits in the Analog Measurement Processor. This time count becomes the conversion result.

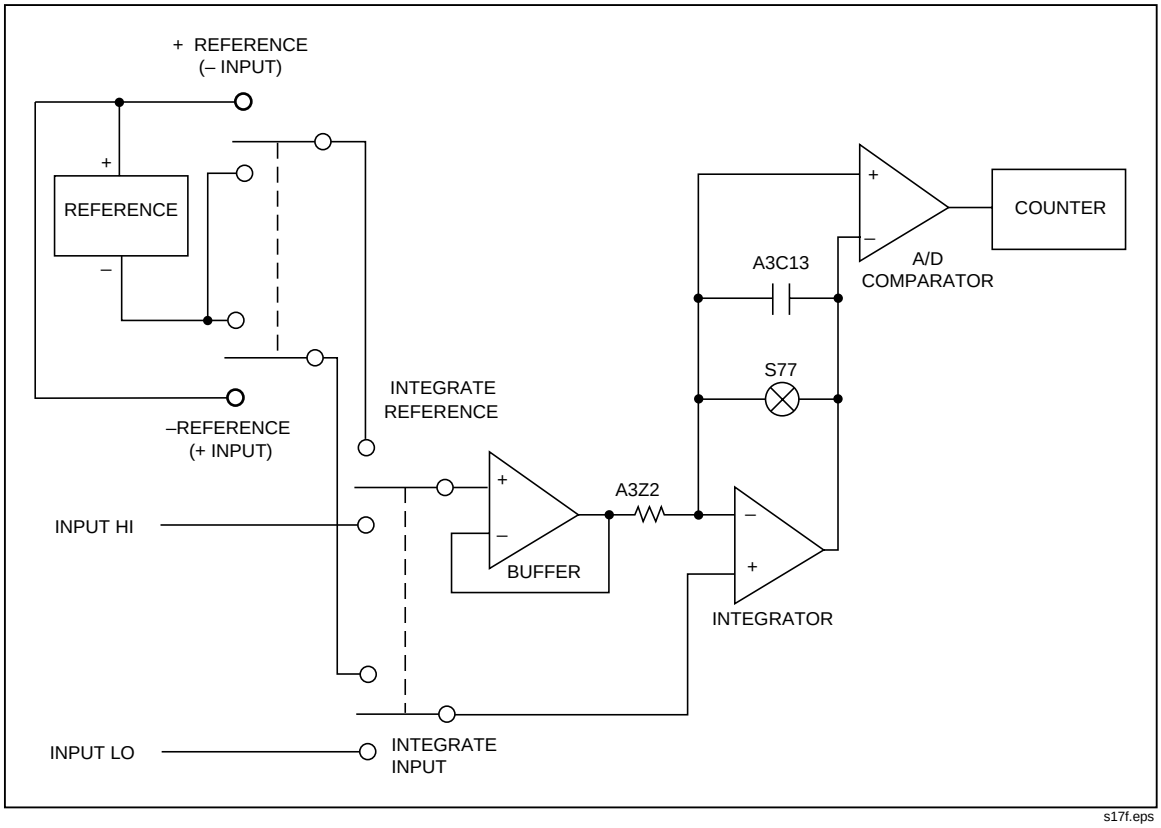


Figure 2A-7. A/D Converter Simplified Schematic (2635A)

In both the slow and fast measurement rates, the a/d converter uses its ±300 mV range for most measurement functions and ranges. The primary exceptions are that the 3V dc range is measured on the a/d converter 3V range, thermocouples are measured on the ±100 mV range, and the temperature reference is measured on the 1V a/d converter range. The typical overload point on a slow rate 30000 count range is 32000 display counts; the typical overload point on a fast rate 3000 count range is 3200 display counts.

During the integrate phase, the a/d buffer in the A3U8 Analog Measurement Processor applies the signal to be measured to one of the four integrator input resistors in network A3Z2. As shown on the A/D Converter schematic diagram in Section 8, the choice of resistor selects the a/d converter range. Switch S69 connects the buffer output through pin B.1 for the 100-mV range, S71 connects the output through B.32 for the 300 mV range, S73 connects to pin B1 for the 1V range, and S75 sets up the 3V range through pin B3.2.

The current through the selected integrator input resistor charges integrator capacitor A3C13, with the current dependent on the buffer output voltage. After the integrate phase, the buffer is connected to the opposite polarity reference voltage, and the integrator integrates back toward zero capacitor voltage until the comparator trips. An internal counter measures this variable integrate time. If the a/d converter input voltage is too high, the integrator overloads and does not return to its starting point by the end of the measurement phase. Switch S77 is then turned on to discharge integrate capacitor A3C13.

The reference voltage used during the variable integrate period for voltage (and high ohms) conversions is generated from zener reference diode A3VR1, which is time and temperature stable. The reference amplifier in the Analog Measurement Processor, along with resistors A3R15, A3R18, and A3R21, pulls approximately 2 mA of current through the zener. Resistors in network A3Z2 divide the zener voltage down to the reference 1.05V required by the A/D Converter.

2A-59. Inguard Microcontroller Circuitry

The Microcontroller, A3U9, with its internal program memory and RAM and associated circuitry, controls measurement functions on the A/D Converter PCA and communicates with the Main (outguard) processor.

The Microcontroller communicates directly with the A3U8 Analog Measurement Processor using the CLK, CS, AR, and AS lines and can monitor the state of the analog processor using the FC[0:7] lines. Filter zeroing is controlled by the ZERO signal. The open thermocouple detect circuitry is controlled by the OTCCLK and OTCEN lines and read by the OTC line. The Microcontroller also communicates with the Main (outguard) processor serially using the IGDR line to receive and the IGDS line (driven by A3Q1) to send.

The channel and function relays are driven to the desired measurement state by signals sent out through microcontroller ports 1, 3, 4, 6, and 7.

On power up, the reset/break detect circuit made up of quad comparator A3U1, capacitors A3C1 and A3C2, and resistors A3R1 through A3R6 and A3R8 resets the Microcontroller through the RESET* line. When a break signal is received from the outguard processor, the inguard A3U9 is again reset. Therefore, if Microcontroller operation is interrupted by line transients, the outguard can regain control of the inguard by resetting A3U9.

2A-60. Channel Selection Circuitry

Measurement input channel selection is accomplished by a set of latching 4-form-C relays organized in a tree structure. Relays A3K5, A3K6, and A3K8 through A3K14 select among channels 1 through 20. Relay A3K7 disconnects rear input channels 1 through 20 from the measurement circuitry between measurements. Relay A3K3 switches in the front panel channel 0 or the rear channels. Inductors A3L1 through A3L24 reduce EMI and current transients.

Selection between 2-wire and 4-wire operation for ohms measurements is performed by latching 2-form-C relays (A3K1 and A3K2.) These relays also serve to select a voltage or thermocouple rear input channel from either channels 1 through 10 or channels 11 through 20.

The coils for the relays are driven by the outputs of Darlington drivers A3U4, A3U5, A3U10, A3U11, and A3U12. The relays are switched when a 6-millisecond pulse is applied to the appropriate reset or set coil by the NPN Darlington drivers in these ICs. When the port pin of Microcontroller A3U9 connected to the input of a driver is set high, the output of the driver pulls one end of a relay set or reset coil low. Since the other end of the relay coil is connected to the VDDR supply, a magnetic field is generated, causing the relay armature and contacts to move to (or remain in) the desired position.

2A-61. Open Thermocouple Check

Immediately before a thermocouple measurement, the open thermocouple check circuit applies a small, ac-coupled signal to the thermocouple input. Microcontroller A3U9 initiates the test by asserting OTCEN, causing comparator A3U14/A3R40 to turn on JFET A3Q12. Next, the Microcontroller sends a 78-kHz square wave out the OTCCLK line through A3R41, A3Q12, and A3C32 to the thermocouple input. The resulting waveform is detected by A3U13 and A3CR2, and a proportional level is stored on capacitor A3C30. Op amp A3U13 compares this detected level with the VTH threshold voltage set up by A3R37 and A3R36 and stored on A3C29. If the resistance at the input is too large, the VTH level will be exceeded and the OTC (open thermocouple check) line will be asserted. After a short delay, the Microcontroller analyzes this OTC signal, determines whether the thermocouple should be reported as open, and deasserts OTCEN and sets OTCCLK high, ending the test.

2A-62. Input Connector PCA

The Input Connector assembly, which plugs into the A/D Converter PCA from the rear of the instrument, provides 20 pairs of channel terminals for connecting measurement sensors. This assembly also provides the reference junction temperature sensor circuitry used when making thermocouple measurements.

Circuit connections between the Input Connector and A/D Converter PCAs are made via connectors A4P1 and A4P2. Input channel and earth ground connections are made via A4P1, while temperature sensor connections are made through A4P2.

Input connections to channels 1 through 20 are made through terminal blocks TB1 and TB2. Channel 1 and 11 HI and LO terminals incorporate larger creepage and clearance distances and each have a metal oxide varistor (MOV) to earth ground in order to clamp voltage transients. MOVs A4RV1 through A4RV4 limit transient impulses to the more reasonable level of approximately 1800V peak instead of the 2500V peak that can be expected on 240 VAC, IEC 664 Installation Category II, ac mains. In this way, higher voltage ratings can be applied to channels 1 and 11 than can be applied to the other rear channels.

Strain relief for the user's sensor wiring is provided both by the Connector PCA housing and the two round pin headers. Each pin of the strain relief headers is electrically isolated from all other pins and circuitry.

Temperature sensor transistor A4Q1 outputs a voltage inversely proportional to the temperature of the input channel terminals. This voltage is 0.6V dc at 25 ºC, increasing 2 mV with each degree decrease in temperature, or decreasing 2 mV with each degree increase in temperature. For high accuracy, A4Q1 is physically centered within and thermally linked to the 20 input terminals. Local voltage reference A4VR1 and resistors A4R1 through A4R3 set the calibrated operating current of the temperature sensor. Capacitor A4C1 shunts noise and EMI to ground.

2A-63. Display PCA

Display Assembly operation is classified into six functional circuit blocks: the Main PCA Connector, the Front Panel Switches, the Display, the Beeper Drive Circuit, the Watchdog Timer/Reset Circuit, and the Display Controller. These blocks are described in the following paragraphs.

2A-64. Main PCA Connector

The 20-pin Main PCA Connector (A2J1) provides the interface between the Main PCA and the other functional blocks on the Display PCA. Seven of the connector pins provide the necessary connections to the four power supply voltages. (See the following table.)

Power Supply	A2J1 Pins	Nominal Voltage
VCC	8	+5.0V dc
VEE	6	-5.0V dc
VLOAD	7	-30V dc
FIL1 to FIL2	2 to 3	5.4V ac

Six pins are used to provide the interface to the Front Panel Switches (A2SWR1 through A2SWR6). The other seven signals interface the Microprocessor (A1U1) to the Display Controller (A2U1) and pass the reset signals between the assemblies.

2A-65. Front Panel Switches

The FPGA scans the 19 Front Panel Switches (A2S1 through A2S18, and A2S21) using only six interface signals (plus the ground connection already available from the power supply). These six signals (SWR1 through SWR6) are connected to bidirectional I/O pins on the FPGA. Each successive column has one less switch.

This arrangement allows the unused interface signals to function as strobe signals when their respective column is driven by the FPGA. The FPGA cycles through six steps to scan the complete Front Panel Switch matrix. Table 2A-7 shows the interface signal state and, if the signal state is an output, the switches that may be detected as closed.

Table 2A-7. Front Panel Switch Scanning (2635A)

Interface Signal States or Key Sensed						
Step	**SWR6**	**SWR5**	**SWR4**	**SWR3**	**SWR2**	**SWR1**
1	A2S8	A2S17	A2S10	A2S12	A2S18	A2S13
2	A2S1	A2S2	A2S3	A2S4	A2S11	0
3	A2S7	A2S9	A2S5	A2S6	0	Z
4	A2S14	A2S15	A2S16	0	Z	Z
5	NA	NA	0	Z	Z	Z
6	A2S21	0	Z	Z	Z	Z

A2Sn indicates switch closure sensed.
0 indicated strobe driven to logic 0
Z indicated high impedance input; state ignored.

In step 1, six I/O pins are set to input, and the interface signal values are read. In steps 2 through 6, the pin listed as O is set to output zero, the other pins are read, and pins indicated by a Z are ignored.

Each of the interface signals is pulled up to the +5V dc supply by a 10-kΩ resistor in network A2Z1. Normally, the resistance between any two of the interface signals is approximately 20 kΩ. Checking resistances between any two signals (SWR1 through SWR6) verifies proper termination by resistor network A2Z1.

2A-66. Display

The custom vacuum-fluorescent display (A2DS1) comprises a filament, 11 grids (numbered 0 through 10 from right to left on the display), and up to 14 anodes under each grid. The anodes make up the digits and annunciators for their respective area of the display. The grids are positioned between the filament and the anodes.

A 5.4V ac signal, biased at a -24V dc level, drives the filament. When a grid is driven to +5V dc, the electrons from the filament are accelerated toward the anodes that are under that grid. Anodes under that grid that are also driven to +5V dc are illuminated, but the anodes that are driven to -30V dc are not. Grids are driven to +5V dc one at a time, sequencing from GRID(10) to GRID(0) (left to right, as the display is viewed.)

2A-67. Beeper Drive Circuit

The Beeper Drive circuit drives the speaker (A2LS1) to provide an audible response to a button press. A valid entry yields a short beep; an incorrect entry yields a longer beep.

The circuitry comprises a dual four-bit binary counter (A2U4) and a NAND gate (A2U6) used as an inverter. One four-bit free-running counter (A2U4) divides the 1.024-MHz clock signal (E) from the FPGA (DSCLK) by 2 to generate the 512-kHz clock (CLK1) used by the Display Controller. This counter also divides the 1.024-MHz clock by 16, generating the 64-kHz clock that drives the second four-bit binary counter (A2U4).

The second four-bit counter is controlled by an open-drain output on the Display Controller (A2U1-17) and pull-down resistor A2R1. When the beeper (A2LS1) is off, A2U1-17 is pulled to ground by A2R1. This signal is then inverted by A2U6, with A2U6-6 driving the CLR input high to hold the four-bit counter reset. Output A2U4-8 of the four-bit counter drives the parallel combination of the beeper (A2LS1) and A2R10 to ground to keep the beeper silent. When commanded by the Microprocessor, the Display Controller drives A2U1-17 high, enabling the beeper and driving the CLR input of the four-bit counter (A2U4-12) low. A 4-kHz square wave then appears at counter output A2U4-8 and across the parallel combination of A2LS1 and A2R10, causing the beeper to resonate.

2A-68. Watchdog Timer and Reset Circuit

The Watchdog Timer and Reset circuit has been defeated by the insertion of the jumper between TP1 and TP3 on the Display Assembly. In this instrument, the reset circuitry is on the Main Assembly and the Watchdog Timer is part of the Microprocessor (A1U1).

The Display Reset signal (DRST*) drives the RESET2* signal on the Display Assembly low when the instrument is being reset. This discharges capacitor A2C3, and NAND gate output A2U6-11 provides an active high reset signal to the Display Processor. The Watchdog Timer on the Display Assembly (A2U5, A2U6 and various resistive and capacitive timing components) is held "cleared" by TP1 being held at 0V dc by a jumper, and output A2U5-12 will always be high.

2A-69. Display Controller

The Display Controller is a four-bit, single-chip microcomputer with high-voltage outputs that are capable of driving a vacuum-fluorescent display directly. The controller receives commands over a three-wire communication channel from the Microprocessor on the Main Assembly. Each command is transferred serially to the Display Controller on the display transmit (DISTX) signal, with bits being clocked into the Display Controller on the rising edges of the display clock signal (DSCLK). Responses from the Display Controller are sent to the Microprocessor on the display receive signal (DISRX) and are clocked out of the Display Controller on the falling edge of DSCLK.

Series resistor A2R11 isolates DSCLK from A2U1-40, preventing this output from trying to drive A1U1-77 directly. Figure 2A-8 shows the waveforms during a single command byte transfer. Note that a high DISRX signal is used to hold off further transfers until the Display Controller has processed the previously received byte of the command.

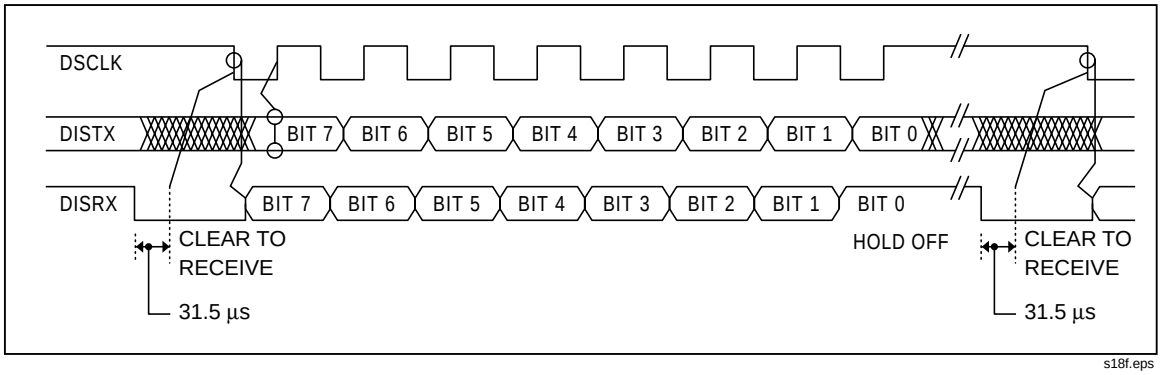


Figure 2A-8. Command Byte Transfer Waveforms (2635A)

Once reset, the Display Controller performs a series of self-tests, initializing display memory and holding the DISRX signal high. After DISRX goes low, the Display Controller is ready for communication. On the first command byte from the Microprocessor, the Display Controller responds with a self-test results response. If all self-tests pass, a response of 00000001 (binary) is returned. If any self-test fails, a response of 01010101 (binary) is returned. The Display Controller initializes its display memory to one of four display patterns depending on the states of the DTEST* (A2U1-41) and LTE* (A2U1-13) inputs. The DTEST* input is pulled up by A2Z1, but may be pulled down by jumpering A2TP4 to A2TP3 (GND). The LTE* input is pulled down by A2R12, but may be pulled up by jumpering A2TP5 to A2TP6 (VCC). The default conditions of DTEST* and LTE* cause the Display Controller to turn all segments on bright at power-up.

Table 2A-8 defines the logic and the selection process for the four display initialization modes.

Table 2A-8. Display Initialization Modes (2635A)

A2TP4	A2TP5	Power-Up Display Initialization
1	1	All Segments OFF
1	0	All Segments ON (default)
0	1	Display Test Pattern #1
0	0	Display Test Pattern #2

The two display test patterns are a mixture of on and off segments forming a recognizable pattern that allows for simple testing of display operation. Test patterns #1 and #2 are shown in Section 5 of this manual.

The Display Controller provides 11 grid control outputs and 15 anode control outputs. (Only 14 anode control outputs are used.) Each of these 26 high-voltage outputs provides an active driver to the +5V dc supply and a passive 220-kΩ (nominal) pull-down to the -30V dc supply. These pull-down resistances are internal to the Display Controller.

The Display Controller provides multiplexed drive to the vacuum-fluorescent display by strobing each grid while the segment data for that display area is present on the anode outputs. Each grid is strobed for approximately 1.37 milliseconds every 16.56 milliseconds, resulting in each grid on the display being strobed about 60.4 times per second. The grid strobing sequence is from GRID(10) to GRID(0), which results in left-to-right strobing of grid areas on the display. Figure 2A-9 shows grid control signal timing.

The single grid strobing process involves turning off the previously enabled grid, outputting the anode data for the next grid, and then enabling the next grid. This procedure ensures that there is some time between grid strobes so that no shadowing occurs on the display. A grid is enabled only if one or more anodes are also enabled. Thus, if all anodes under a grid are to be off, the grid is not turned on. Figure 2A-10 describes the timing relationship between an individual grid control signal and the anode control signals.

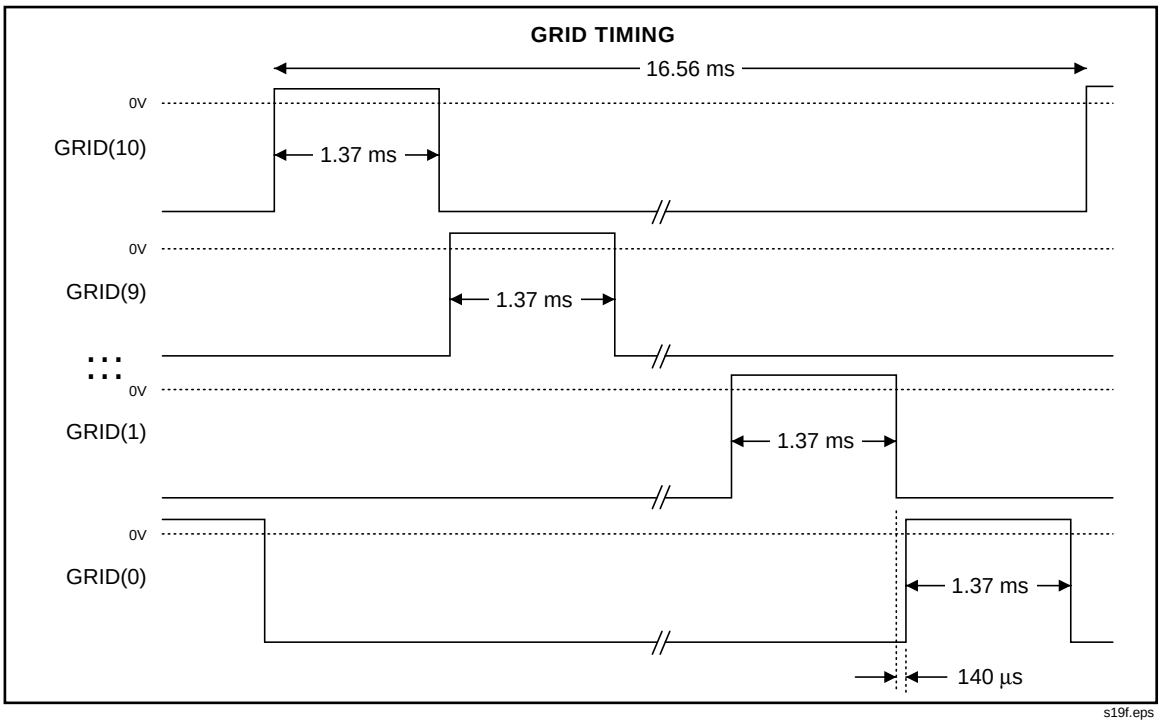


Figure 2A-9. Grid Control Signal Timing (2635A)

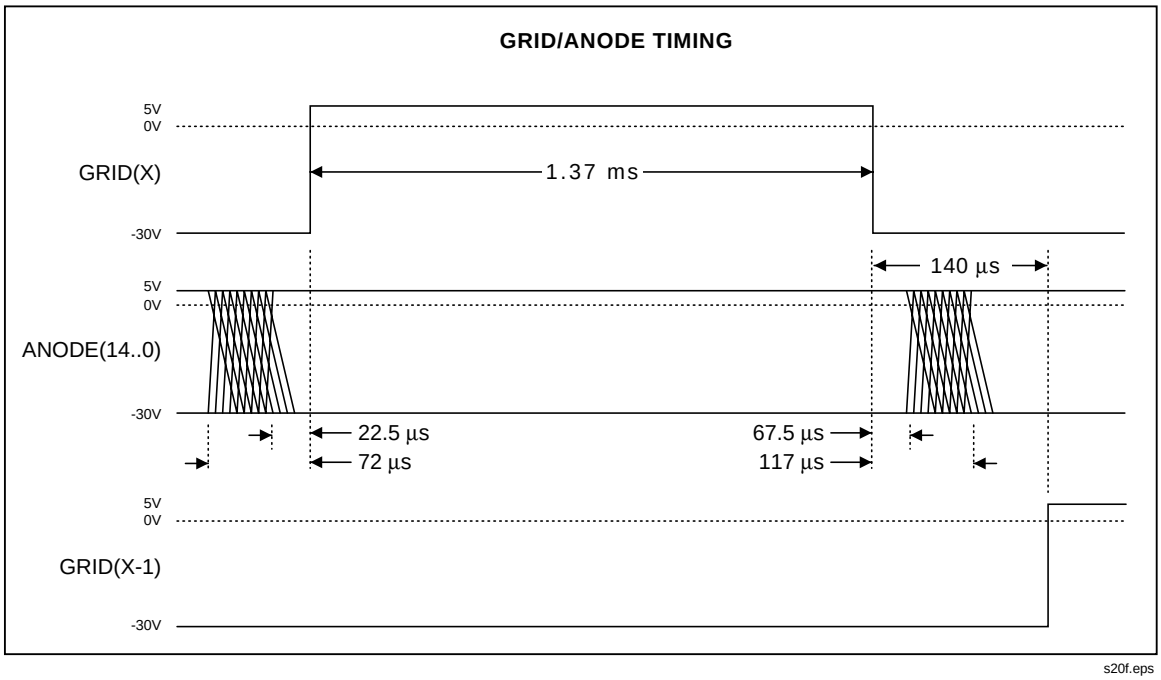


Figure 2A-10. Grid-Anode Timing Relationships (2635A)

2A-70. Memory Card Interface PCA

The Memory Card Interface Assembly operation is composed of four functional circuit blocks: the Main PCA Connector, the Microprocessor Interface, the Memory Card Controller, and the PCMCIA Memory Card Connector. These blocks are described in the following paragraphs.

2A-71. Main PCA Connector

The Memory Card Interface PCA interfaces to the Main PCA through a 40-pin, right angle connector (A6P2). This connector routes eight bits of the Microprocessor data bus, the lower four bits of the address bus, memory control, interrupt and address decode signals from the Main PCA to the Memory Card Interface PCA. The Memory Card Interface PCA is powered by the +5.0V dc power supply (VCC). The pinout of the high density ribbon cable that connects the Main PCA to the Memory Card Interface PCAis carefully selected to prevent cross-talk between signals and to provide low impedance connections to the VCC power supply.

2A-72. Microprocessor Interface

The timing of Microprocessor read and write accesses to the Memory Card Controller (A6U1) are controlled internally by the Memory Card Controller which determines whether wait states are required when the Microprocessor accesses one of its internal registers.

When a register in the Memory Card Controller (A6U1) is read, the four address bits select one of the internal registers to read and then the XMCARD* signal (A6U1-49) is driven to a low level by the Microprocessor. The XRDU* signal (A6U1-50) is then driven low by A1U11-14 to enable the data outputs from the Memory Card Controller (D8 through D15). At the end of the read access, both XMCARD* and XRDU* are driven high again.

When a register in the Memory Card Controller (A6U1) is written, the four address bits select one of the internal registers to write and then the XMCARD* signal (A6U1-49) is driven to a low level by the Microprocessor. The XWRU* signal (A6U1-51) is then driven low by A1U11-13 to initiatethe transfer of the data bus inputs on the Memory Card Controller (D8 through D15) to the internal register. At the end of the write access, both XMCARD* and XRDU* are driven high again and the data is latched into the internal register.

If no wait states are required, the DTACK* signal (A6U1-58) will be driven low after the next low to high transition of the system clock (A6U1-30) to indicate to the Microprocessor that the data transfer has been acknowledged and the read or write access may be completed. The DTACK* signal is a tri-state bus that is pulled up to VCC by resistor A1R83 and pulled low by devices being accessed by the Microprocessor.

If wait states are required, the DTACK* signal (A6U1-58)will not go low until the proper number of wait states have been inserted.The Memory Card Controller counts cycles of the system clock (A6U1-30) and when the correct number of wait states have been done, the DTACK* signal will go low.

Accesses to internal registers should be done with no wait states, and accesses through the Memory Card Controller to the Memory Card automatically add two wait states.

2A-73. Memory Card Controller

The Memory Card Controller (A6U1) is a Field Programmable Gate Array (FPGA) that automatically loads its configuration upon power-up from a serial memory device (A6U3).While it is configuring, the FPGA holds the memory CE input (A6U3-4) low and toggles the CLK input (A6U3-2) to serially shift the configuration data out of the memory on the D output (A6U3-1) and into the FPGA.When configuration is complete, the FPGA should release the CE input(A6U3-4) allowing it to be pulled high by resistor A6R8.

The Memory Card Controller provides a register based interface for the Microprocessor to use to access data stored on industry standard PCMCIA memory cards. A 26 bit counter controls the address bus (CA<0> through CA<25>) to the PCMCIA Memory Card Connector (A6P1). An eight bit data bus(CD<0> through CD<7>) and memory card control signals (REG*, CE1*, CRD*, and CWR*) control accesses to memory on the card.

The REG* signal (A6U1-8) is like an additional address bit. When REG* is slow (A6U1-8), read and write accesses go to "attribute" memory on the card. Attribute memory is typically a small EEPROM on the memory card that contains special information that specifies the manufacturer of the card, type and size of memory on the card, memory speed, etc. When REG* is high, read and write accesses go to the "common" memory on the card. Common memory is the Static RAM on the memory cards used in this instrument.

Typically, information is read and written to the memory card in a sequential manner where the address counter automatically increments after the end of each read or write cycle. When the Memory Card Controller reads data from the memory card data bus (CD<0> through CD<7>), CE1* (A6U1-62) goes low followed by CRD* (A6U1-63) going low. The data from the memory card then goes through the Memory Card controller and is read by the Microprocessor on the D8 through D15 data bus lines.Data is written to the memory card in a similar manner, except that the data goes from the Microprocessor through the memory Card Controller and to the Memory Card with CWR* (A6U2-64) going low to enable the writing of the data to the memory. The purpose of A6U2 and resistors A6R2, A6R5, and A6R7 is to ensure that data on the Memory Card is not accidentally modified during the time that the instrument is being powered up or down. Each of the Memory Card data bus lines (CD<0> through CD<7>) has a series resistor (A6Z2) that helps ensure that the instrument meets EMI/EMC performance requirements.

The Memory Card Controller detects the insertion and removal of a Memory Card and interrupts the microprocessor by driving the MCINT* signal(A6U1-60) low. When a Memory Card is inserted in the PCMCIA Memory Card Connector, the CD1 (A6U1-19) and CD2 (A6U1-21) inputs on the Memory Card Controller are driven to 0V dc and Microprocessor (A1U1) is interrupted. The Microprocessor then powers up the Memory Card by setting A6U1-26 low, which turns on FET A6Q1 by driving the gate low through resistor A6R13. When FET A6Q1 is turned on the Memory Card power (CVCC and CVPP) is approximately +5.0V dc. When the Microprocessor has completed a data transfer with the Memory Card, FET A6Q1 is turned off again by driving A6U1-26 high.

When a Memory Card is inserted and powered up, the Memory Card outputs some status signals to the Memory Card Controller. If the Memory Card write protect switch is protecting data on the card, the WP signal (A6U1-22) is high. The status of the Memory Card battery is output on the BVD1 (A6P1-18) and BVD2 (A6P1-20) pins of the Memory Card Connector. If either of these battery status signals is low when the Memory Card is powered up, then the Microprocessor will turn on LED A6DS2 by driving A6U1-24 low. The Busy status LED (A6DS1) is turned on by driving A6U1-25 low when the Microprocessor has powered up the Memory Card and is transferring data to or from the card.

2A-74.PCMCIA Memory Card Connector

The PCMCIA Memory Card Connector (A6P1) is a 68 pin connector that meets the requirements of the Personal Computer Memory Card International Association. This connector has pins that are three different lengths: the card detection pins (CD1 and CD2) are the shortest, the power and ground pins are the longest, and the rest of the pins are a length in between. This ensures that on memory card insertion, the power and

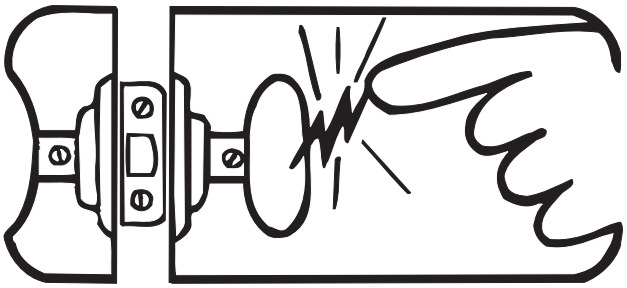
ground pins are mated first followed by the reset of the input / output signals with the card detection signals mating last. This sequence is reversed on memory card removal.

The PCMCIA Memory Card Connector has a metal shell that is connected to chassis ground to help ensure that the instrument meets EMI/EMC and ESD performance requirements. A push-button mechanism is included to allow easy ejection of the Memory Card.

static awareness

A Message From

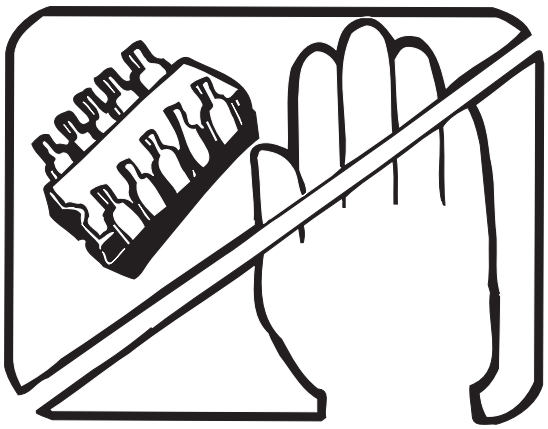
Fluke Corporation



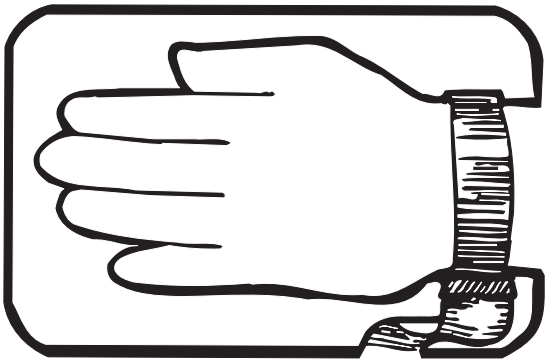
Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

1. Knowing that there is a problem.
2. Leaning the guidelines for handling them.
3. Using the procedures, packaging, and bench techniques that are recommended.

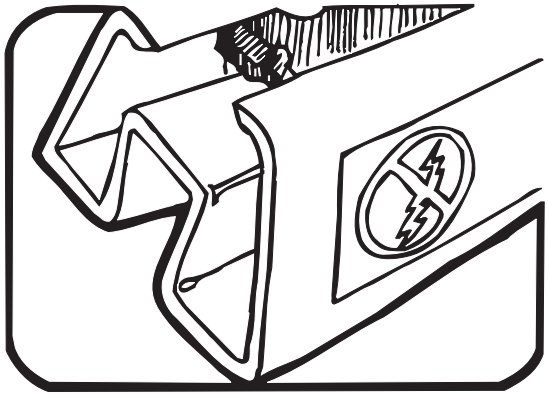
The following practices should be followed to minimize damage to S.S. (static sensitive) devices.



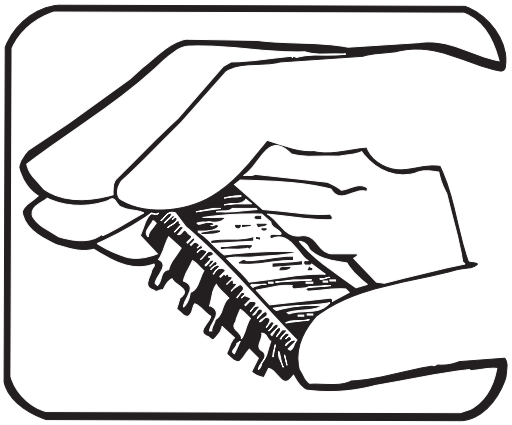
1. MINIMIZE HANDLING



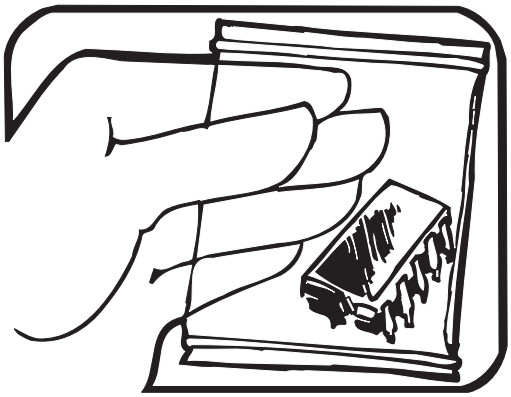
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESISTANCE GROUNDING WRIST STRAP.



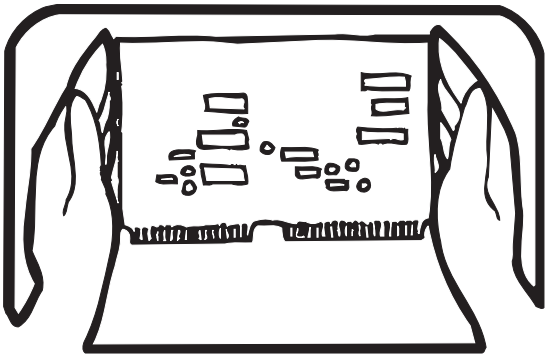
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



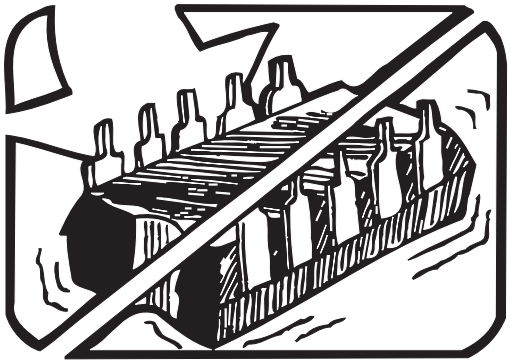
4. HANDLE S.S. DEVICES BY THE BODY.



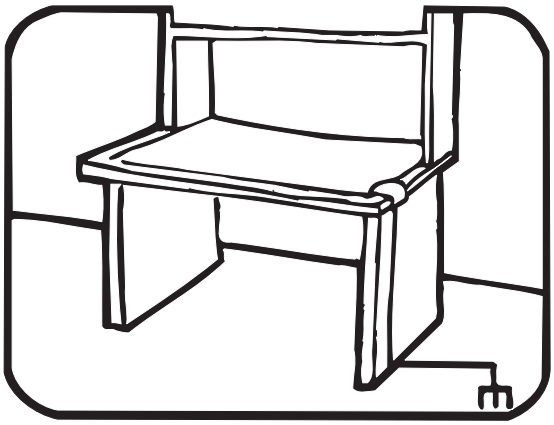
5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT.



8. WHEN REMOVING PLUG-IN ASSEMBLIES HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS PROTECT INSTALLED S.S. DEVICES.



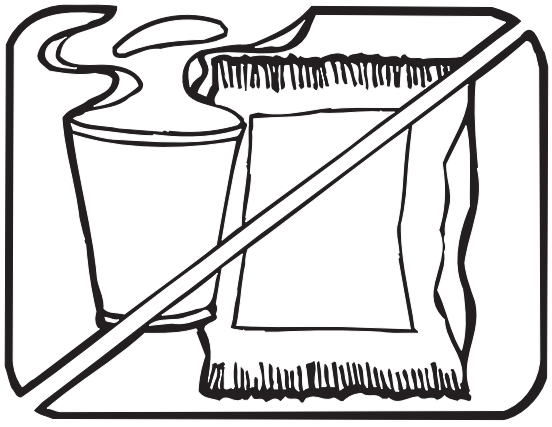
6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION.

10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.

11. ONLY GROUNDED-TIP SOLDERING IRONS SHOULD BE USED.



7. AVOID PLASTIC,VINYL AND STYROFOAM® IN WORK AREA.

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Chapter 3
General Maintenance

3-1. Introduction

This section provides handling, cleaning, fuse replacement, disassembly, and assembly instructions.

3-2. Warranty Repairs and Shipping

If your instrument is under warranty, see the warranty information at the front of this manual for instructions on returning the unit. The list of authorized service facilities is included in Section 6.

3-3. General Maintenance

3-4. Required Equipment

Equipment required for calibration, troubleshooting, and repair of the instrument is listed in Section 4 (Table 4-1.)

Refer to the Fluke "Surface Mount Device Soldering Kit" for a list of special tools required to perform circuit assembly repair. (In the USA, call 1-800-526-4731 to order).

3-5. Power Requirements

⚠ Warning

To avoid shock hazard, connect the instrument powercord to a power receptacle with earth ground.

If you have not already done so, plug the line cord into the connector on the rear of the instrument. The instrument operates on any line voltage between 90V ac and 264V ac and at any frequency between 45 and 440 Hz. However, the instrument is warranted only to meet published specifications at 50/60 Hz. The instrument also operates from dc power (9 to 16V dc). DC input power is connected to the rear input connector J6, pin 8 (DCH), and pin 7 (DCL). If both ac and dc power sources are connected to the instrument, the ac power source is used if the ac line voltage exceeds approximately 8.3 times the dc voltage. Automatic switchover between ac and dc occurs without interrupting instrument operation. The instrument draws a maximum of 10 VA on ac line power or 4W on dc power.

3-6. Static Safe Handling

All integrated circuits, including surface mounted ICs, are susceptible to damage from electrostatic discharge (ESD). Modern integrated circuit assemblies are more susceptible to damage from ESD than ever before. Integrated circuits today can be built with circuit lines less than one micron thick, allowing more than a million transistors on a 1/4-inch square chip. These submicron structures are sensitive to static voltages under 100 volts. This much voltage can be generated on a dry day by simply moving your arm. A person can develop a charge of 2,000 volts by walking across a vinyl tile floor, and polyester clothing can easily generate 5,000 to 15,000 volts during movement against the wearer. These low voltage static problems are often undetected because a static charge must be in the 30,000 to 40,000 volt range before a person feels a shock.

Most electronic components manufactured today can be degraded or destroyed by ESD. While protection networks are used in CMOS devices, they merely reduce, not eliminate component susceptibility to ESD.

ESD may not cause an immediate failure in a component; a delayed failure or wounding effect is caused when the semiconductor's insulation layers or junctions are punctured. The static problem is thus complicated in that failure may occur anywhere from two hours to six months after the initial damage.

Two failure modes are associated with ESD. First, a person who has acquired a static charge can touch a component or assembly and cause a transient discharge to pass through the device. The resulting current ruptures the junctions of a semiconductor. The second failure mode does not require contact with another object. Simply exposing a device to the electric field surrounding a charged object can destroy or degrade a component. MOS devices can fail when exposed to static fields as low as 30 volts.

Observe the following rules for handling static-sensitive devices:

1. Handle all static-sensitive components at a static-safe work area.

   Use grounded static control table mats on all repair benches, and always wear a grounded wrist strap. Handle boards by their nonconductive edges only. Store plastic, vinyl, and Styrofoam objects outside the work area.

2. Store and transport all static-sensitive components and assemblies in static shielding bags or containers.

   Static shielding bags and containers protect components and assemblies from direct static discharge and external static fields. Store components in their original packages until they are ready for use.

3-7. Servicing Surface-Mount Assemblies

Hydra incorporates Surface-Mount Technology (SMT) for printed circuit assemblies (pca's). Surface-mount components are much smaller than their predecessors, with leads soldered directly to the surface of a circuit board; no plated through-holes are used. Unique servicing, troubleshooting, and repair techniques are required to support this technology.

Refer to Section 5 for additional information. Also, refer to the Fluke "Surface Mount Device Soldering Kit" for a complete discussion of these techniques (in the USA, call 1-800-526-4731 to order).

3-8. Cleaning

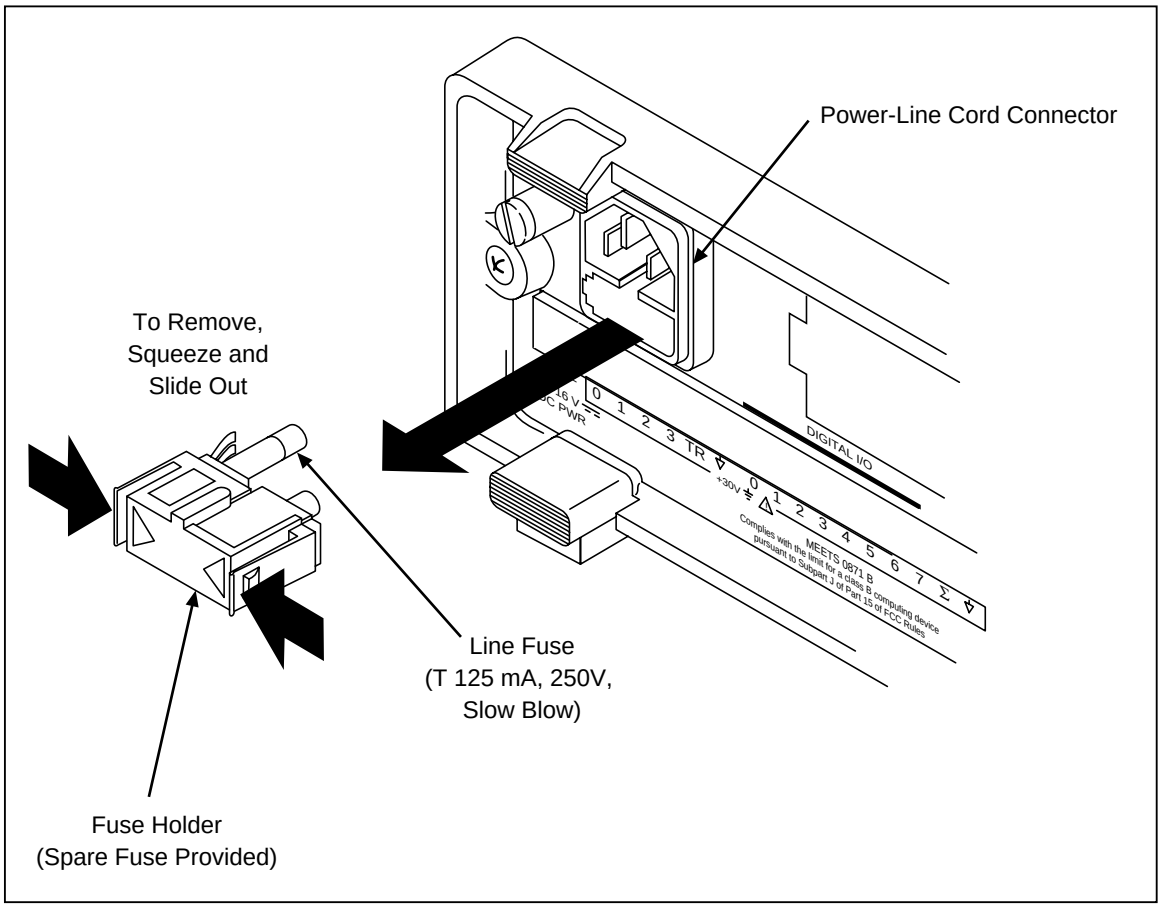
⚠ Warning

To avoid electrical shock or damage to the instrument, never allow water inside the case. To avoid damaging the instrument's housing, never apply solvents to the instrument.

If the instrument requires cleaning, wipe it down with a cloth that is lightly dampened with water or a mild detergent. Do not use aromatic hydrocarbons, chlorinated solvents, or methanol-based fluids when wiping the instrument. Dry the instrument thoroughly after cleaning.

3-9. Line Fuse Replacement

The line fuse (125 mA, 250V, slow blow, Fluke Part Number 822254) is located on the rear panel. The fuse is in series with the power supply. For replacement, unplug the line cord and remove the fuse holder (with fuse) as shown in Figure 3-1. The instrument is shipped with a replacement fuse loosely secured in the fuse holder.



s21f.eps

Figure 3-1. Replacing the Line Fuse

3-10. Disassembly Procedures

The following paragraphs describe disassembly of the instrument in sequence from the fully assembled instrument to the chassis level. Start and end your disassembly at the appropriate heading levels.

⚠ Warning

Opening the case may expose hazardous voltages.Always disconnect the power cord and measuringinputs before opening the case. And remember thatrepairs or servicing should be performed only byqualified personnel.

3-11. Remove the Instrument Case

Use the following procedure to remove the instrument case.

1. Make sure the instrument is powered off and disconnected from the power source (ac or dc).
2. Remove the screw from the bottom of the case, and remove the two screws from the rear bezel as shown in Figure 3-2. While holding the front panel, slide the case and rear bezel off the chassis. (At this point, the rear bezel is not secured to the case.)

3-12. Remove Handle and Mounting Brackets

Refer to Figure 3-3 during this procedure. Pull each handle pivot out slightly at the handle mounting brackets, then rotate the handle up over the display. With the handle pointing straight up, pull out and disengage one pivot at a time.

Use a Phillips screwdriver to remove the two handle mounting brackets. Note that these brackets must be reinstalled in their original positions. Therefore, the inside of each bracket is labeled (R for right, L for left) as viewed from the front of the instrument.

3-13. Remove the Front Panel Assembly

Note

*Parts referenced by letter (e.g., **A**) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).*

Use the following procedure to remove the Front Panel Assembly (E):

1. Remove the leads connected to the two input terminals. Using needle nose pliers, pull and disconnect the wires at the rear of the VΩ and COM input terminals.
2. Using needle nose pliers, disconnect the display ribbon cable (G) on the Main PCA (H) by alternately pulling up on each end of its connector. Avoid breaking the alignment tabs on the Main PCA side of this connection.
3. Remove the Front Panel Assembly by releasing the four snap retainers (I) securing it to the chassis. Using needle nose pliers, disconnect the display ribbon cable (G) on the Display PCA (K) by alternately pulling up on each end of its connector. Avoid breaking the alignment tabs on the Display PCA side of this connection. The ribbon cable (G) may be left attached to the chassis.
4. The green power switch activator rod (J) extending from the power switch on the Main PCA through the Front Panel Assembly can now be removed. Squeeze the end of the rod at the power switch and lift up; the bar disengages smoothly from the switch.

3-14. Remove the Display PCA

Two movable tabs hold the Display PCA (K) in place on the back of the Front Panel Assembly. Release one tab at a time. Then, while prying slightly at the top of the Display PCA, lift the pca out of its securing slots. Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).

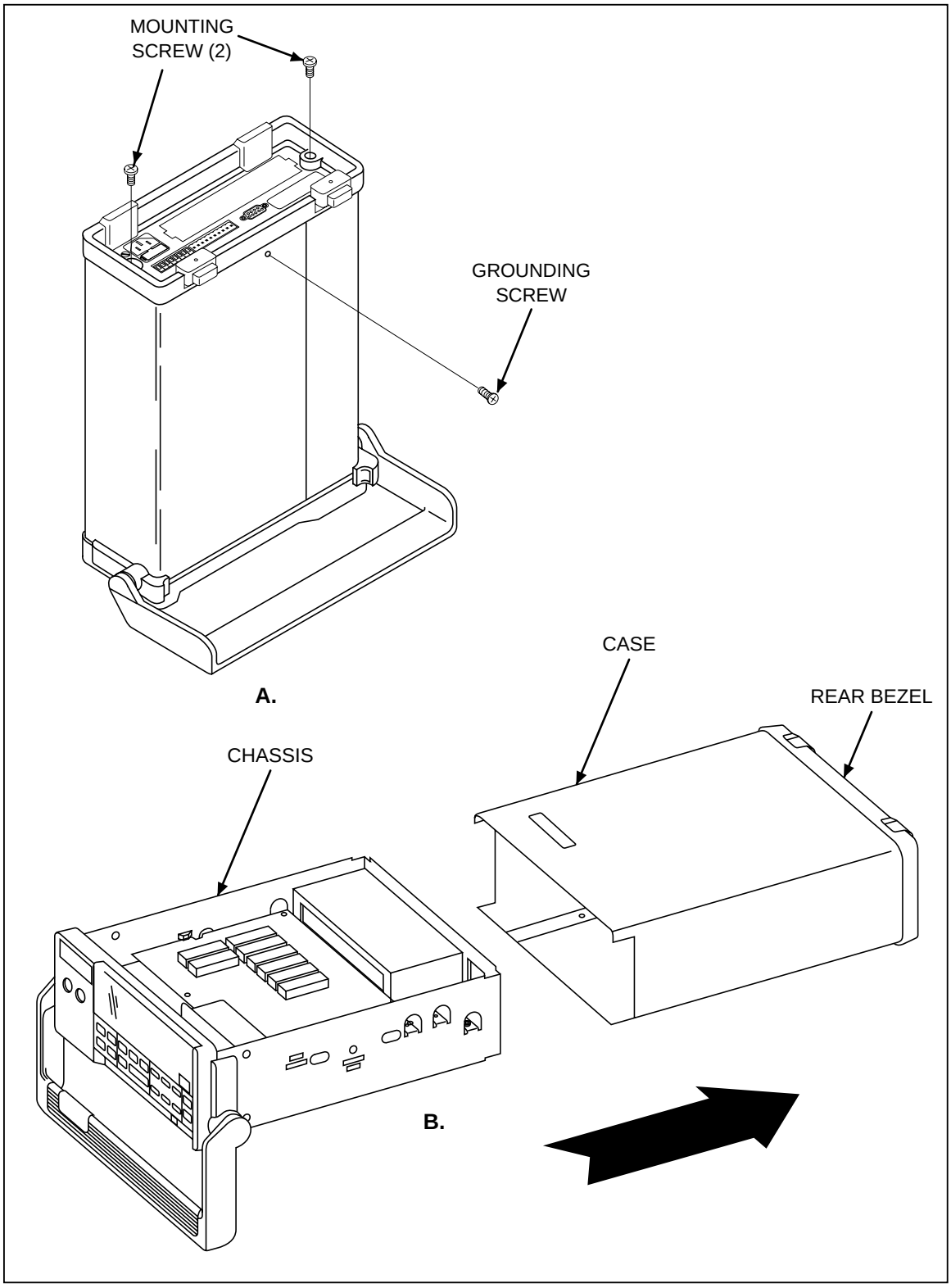


Figure 3-2. Removing the Case

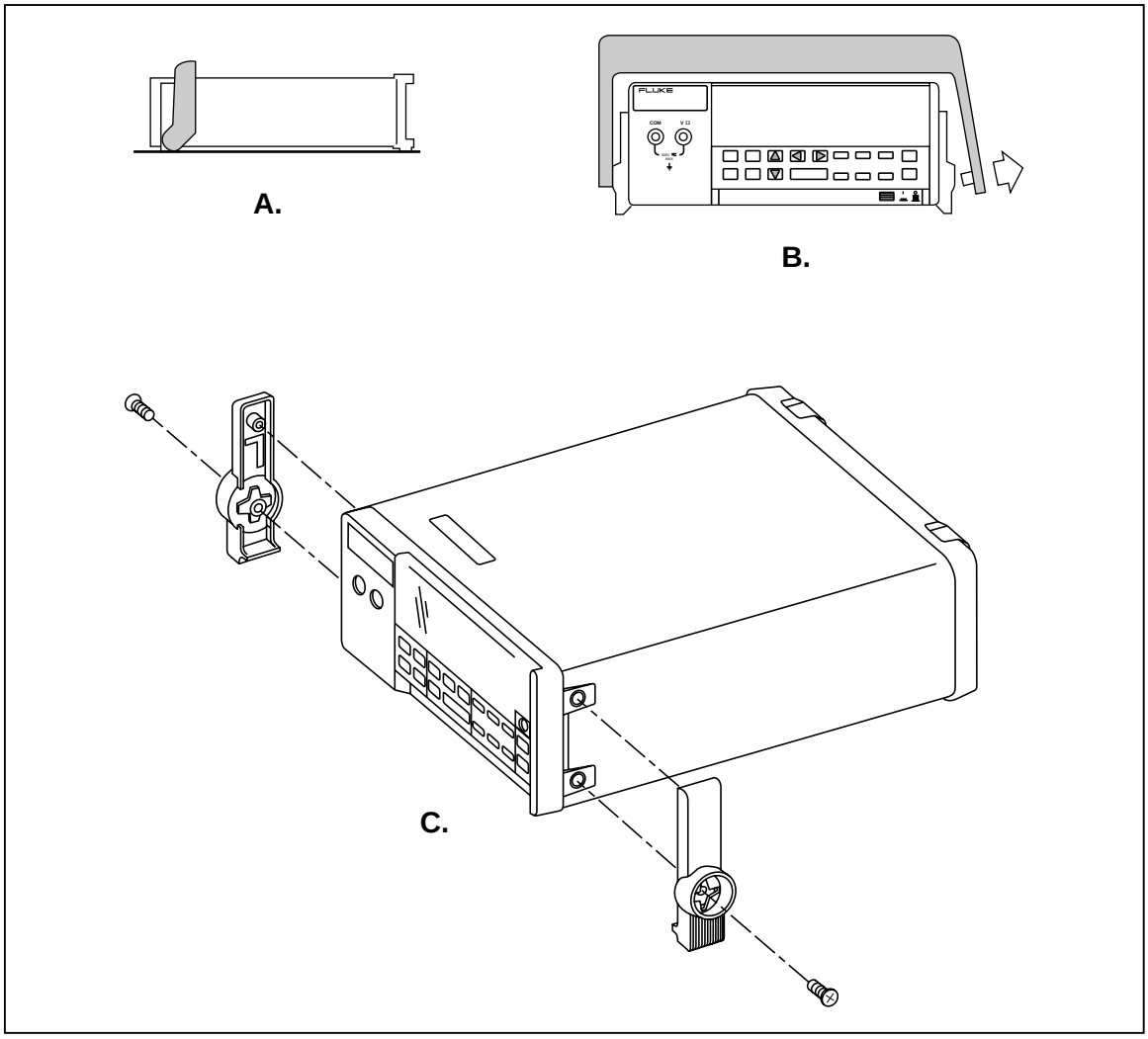


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Figure 3-3. Removing the Handle and Handle Mounting Brackets

Note

The Display PCA provides a space for a center securing screw. If the two tabs are intact, this screw is not necessary. If a tab is broken, a screw can be used as an additional securing device.

The elastomeric Keypad Assembly (L) can now be lifted away from the Front Panel Assembly.

Only if necessary, gently remove the display window (M) by releasing the two snaps along its inside, bottom edge. While pushing slightly on the rear of the window, gently lever each snap by pressing against an adjacent edge on the keypad housing.

Caution

Avoid using ammonia or methyl-alcohol cleaningagents on either the Front Panel or the displaywindow. These types of cleaners can damage surfacefeatures and markings. Use an isopropyl-basedcleaning agent or water to clean the Front Paneland the display window.

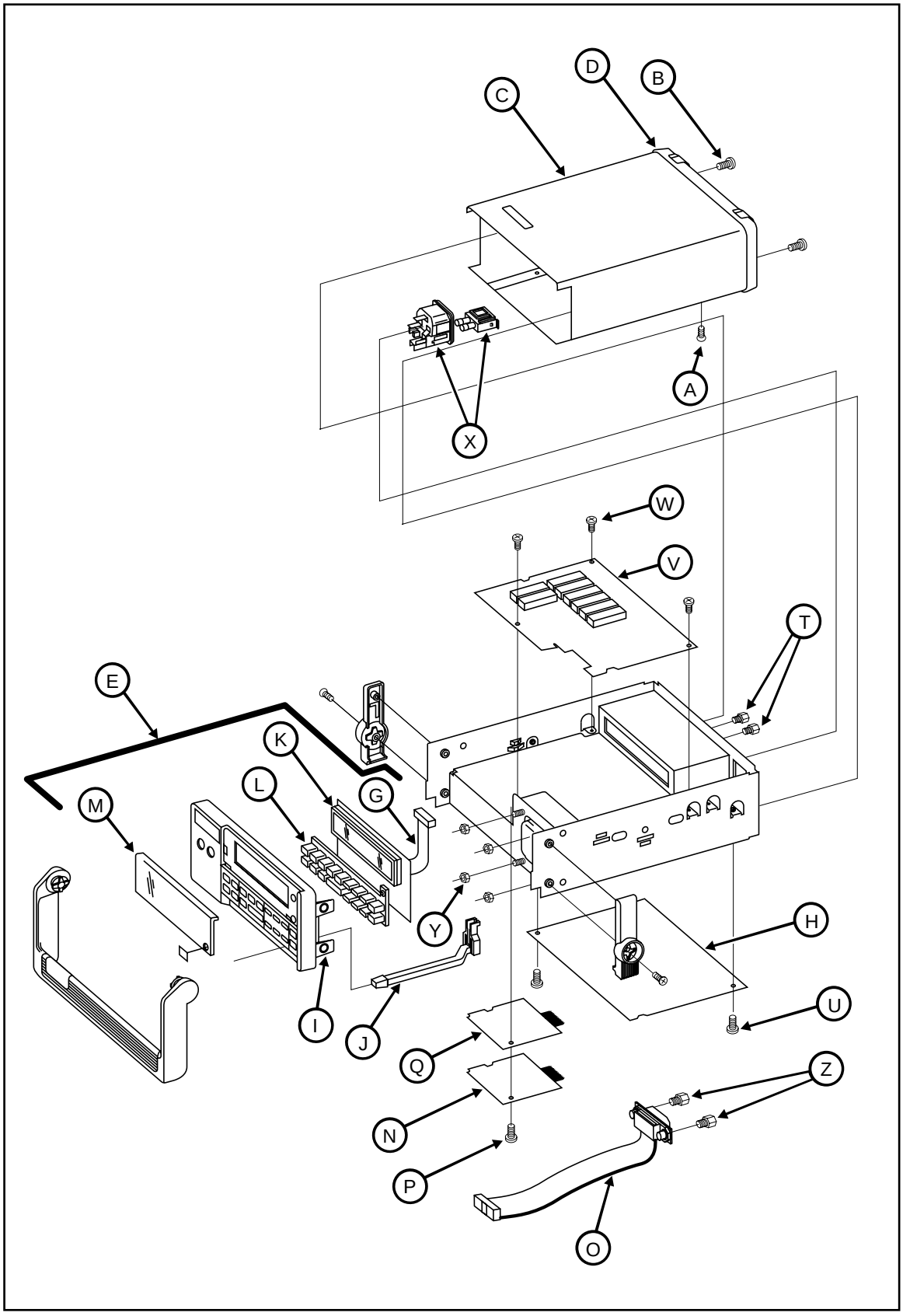
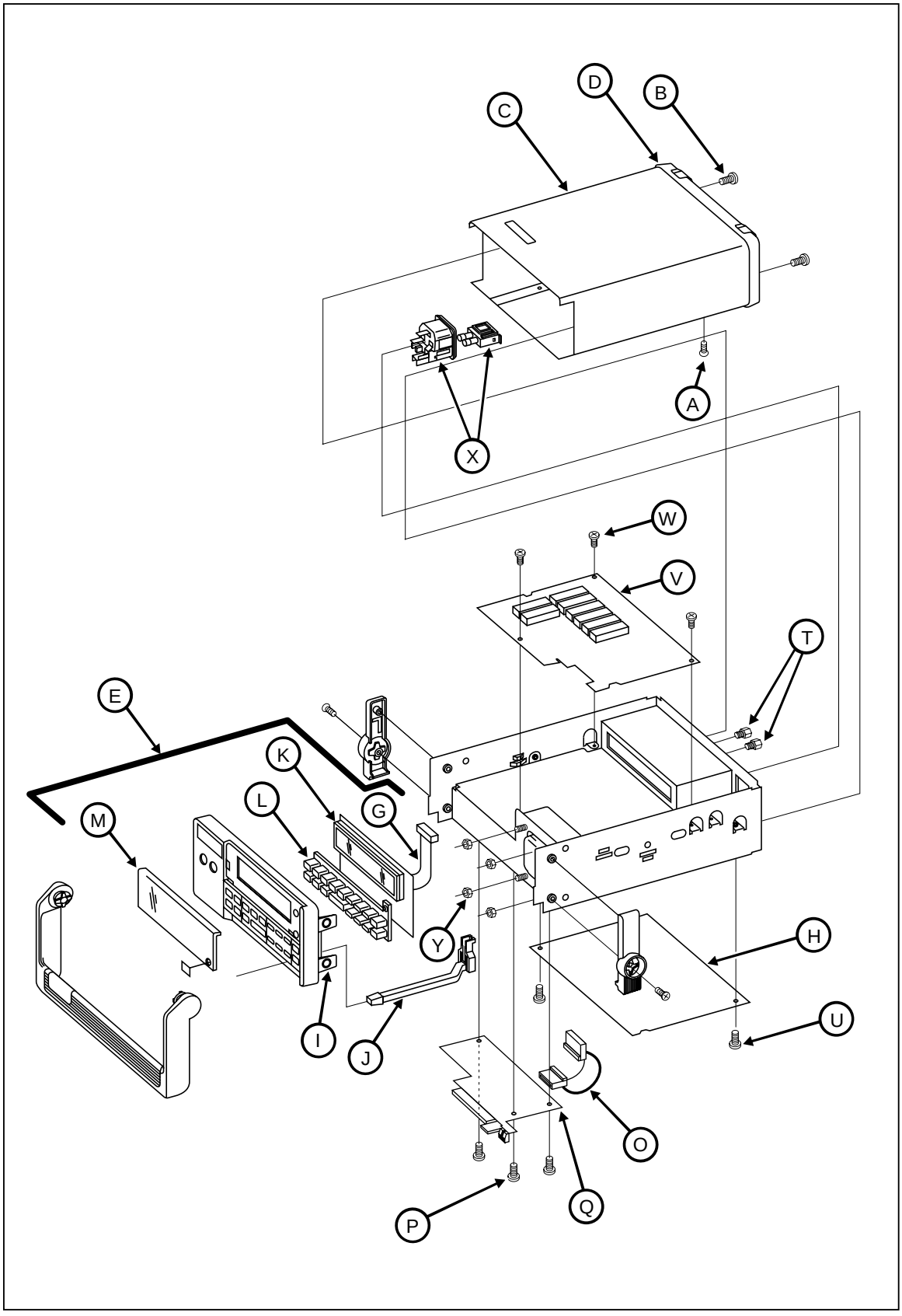


Figure 3-4. 2620A and 2625A Assembly Details



s25f.eps

Figure 3-5. 2635A Assembly Details

3-15. Remove the IEEE-488 Option (2620A Only)

Section 7 of this manual provides a detailed removal procedure for the IEEE-488 option. The following removal instructions provide the essentials of this procedure. Parts referenced by letter (e.g., A) are shown in Figure 3-4. If necessary, refer to the complete procedure in Section 7.

1. From the bottom of the instrument, locate the IEEE-488 PCA (N). This pca is connected to the front of Main PCA, with a ribbon cable (O) leading across both pca's to the Rear Panel.
2. Use needle nose pliers to disconnect the 24-line cable assembly at the IEEE-488 PCA, alternately pulling on each end of the cable connector. Leave the other end of this cable attached to its Rear Panel connector.
3. Remove the 6-32, 1/4-inch panhead Phillips screw (P) securing the IEEE-488 PCA.
4. Disengage the IEEE-488 PCA by sliding it away from the Main PCA.

3-16. Remove the Memory PCA (2625A Only)

Use the following procedure to remove the Memory PCA from the 2625A Data Logger. Parts referenced by letter (e.g., A) are shown in Figure 3-4.

1. From the bottom of the instrument, locate the Memory PCA (Q). This pca is connected to front of the Main PCA.

   Note

   You might want to verify that this is the Memory PCA. The Memory PCA and the IEEE-488 PCA occupy the same position and use the same connection to the Main PCA. The Memory PCA is a standard part of the Hydra Data Logger (Model 2625A). The IEEE-488 PCA is not available with the 2625A but is optional with the Hydra Data Acquisition Unit (Model 2620A).

2. Remove the panhead Phillips screw (P) securing the Memory PCA.
3. Disengage the Memory PCA by sliding it away from the Main PCA.

3-17. Remove the Memory Card I/F PCA (2635A Only)

Use the following procedure to remove the Memory Card I/F PCA from the 2635A Data Bucket. Parts referenced by letter (e.g., A) are shown in Figure 3-5.

1. From the bottom of the instrument, locate the Memory Card I/F PCA (Q). This pca is in the front of the instrument near the center, and is connected to the Main PCA by a high-density ribbon cable (O).
2. Remove the three 6-32, 1/4-inch panhead Phillips screws (P) securing the Memory Card I/F PCA.
3. Disconnect the high-density ribbon cable (O) from the connector on the Memory Card I/F PCA (Q) and remove the assembly from the chassis.

3-18. Remove the Main PCA

With the IEEE-488 option (2620A) and the Memory PCA (2625A) or Memory Card I/F PCA (2635A) removed, the Main PCA (H) can be removed. Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A). Use the following procedure:

1. If it is still attached, remove the green power switch activator rod (J) extending from the power switch on the Main PCA through the Front Panel Assembly. Squeeze the end of the rod at the power switch and lift up; the bar disengages smoothly from the switch.
2. Using needle nose pliers, disconnect the display ribbon cable (G) on the Main PCA (H) by alternately pulling up on each end of its connector. Avoid breaking the alignment tabs on the Main PCA side of this connection. (This connector has already been detached if the Front Panel Assembly was removed.)
3. Detach the transformer connector at the Main PCA.
4. Detach the Main-to-A/D Converter cable at the A/D Converter PCA.
5. If installed, pull off the ALARM OUTPUTS and DIGITAL I/O terminal strips from the Rear Panel.
6. Remove the RS-232 connector screws (T) at the Rear Panel. Use a 3/16-inch nut driver to loosen the connector securing hardware.
7. If installed, remove the IEEE-488 connector. Use a 7-mm nutdriver to loosen the two securing screws on the rear panel.
8. Now remove the two screws (U) securing the Main PCA to the chassis. Slide the Main PCA forward. Then, while matching the pca edge indentations to the guide tabs on each chassis side, lift the Main PCA up and away from the chassis.

3-19. Remove the A/D Converter PCA

Use the following procedure to remove the A/D Converter PCA (V). Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).

1. If necessary, remove the leads connecting the two front panel input terminals to the A/D Converter PCA. Using needle nose pliers, pull and disconnect the wires at the rear of the VΩ (red) and COM (black) input terminals. (These leads are already disconnected if the Front Panel Assembly has been removed.)
2. At the A/D Converter PCA, detach the cable leading to the Main PCA.
3. From the Rear Panel, pull out the Input Module.
4. Remove the three Phillips head screws (W) securing the A/D Converter PCA to the chassis.
5. Now slide the A/D Converter PCA forward to match the indentations in the pca edges to the guides in the chassis. Then lift the pca out.

3-20. Disconnect Miscellaneous Chassis Components

Use the following procedure to disconnect the remaining hardware from the chassis. Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).

1. Use needle nose pliers to remove the internal connections at the line power plug (X). Remove the ground screw prior to disconnecting the ground wire from the plug.
2. Remove the power plug by releasing its two snaps one at a time.
3. Disconnect the power transformer by removing the four 5/16-inch nuts (Y) that secure it to the right side of the chassis.
4. If installed, remove the 7-mm IEEE-488 connector screws (Z) (2620A only).

3-21. Assembly Procedures

Generally, assembly procedures follow a reverse sequence of disassembly procedures. As some differences do apply, assembly is described separately in the following paragraphs. Begin assembly at the appropriate level, as defined by the heading. References are made to items in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A) for assembly details of standard instrument parts.

Note

Parts referenced by letter (e.g., A) are shown in Figure 3-4 (2620A or 2625A) or Figure 3-5 (2635A).

3-22. Install Miscellaneous Chassis Components

Use the following procedure to replace any items that have been removed from the basic chassis.

1. Replace the power transformer along the right side of the chassis. Use four 5/16-inch hex nuts (Y).
2. Snap the power plug into position.
3. Use needle nose pliers to replace the interior connections at the power plug. Also, attach the ground wire at its chassis connection.

3-23. Install the A/D Converter PCA

1. Fit the A/D Converter PCA (L) so that the chassis guides pass through notches on both sides of the pca. Then slide the pca back until it is snug against the Input Module enclosure.
2. Fasten the A/D Converter PCA to the chassis with three 6-32, 1/4-inch panhead screws (W).
3. If the Front Panel Assembly is installed, attach the leads connecting the two input terminals to the A/D Converter PCA. Using needle nose pliers, push the wire connectors firmly onto the recessed input terminal pins (red to VΩ and black to COM.)
4. At the A/D Converter PCA, attach the cable leading to the Main PCA.
5. From the Rear Panel, push the Input Module back into place.

3-24. Install the Main PCA

1. Fit the Main PCA (H) so that the chassis guides pass through notches on both sides of the pca. Then slide the pca back until it is snug against the Rear Panel.
2. Replace the RS-232 connector screws (T) on the rear of the chassis. Use a 3/16-inch nut driver to tighten the connector hardware.
3. Fasten the Main PCA to the chassis with two 6-32, 1/4-inch panhead screws (U).
4. Connect the transformer cable at connector J3 on the Main PCA. Verify that the connector is aligned correctly (all three pins connected.)
5. Plug the Front Panel cable onto its connector (J2) on the Main PCA.
6. From the Rear Panel, push the ALARM OUTPUTS and DIGITAL I/O terminal strips onto their appropriate connectors.

3-25. Install the IEEE-488 Option (2620A Only)

Both the instruction sheet provided with the IEEE-488 Option and Section 7 of this manual fully describe installation. The following instructions provide installation procedure essentials. If necessary, refer to Section 7, paying particular attention to Figures 7-2 and 7-3.

1. Place the IEEE-488 PCA (N) into position so that the edge of the pca fits into the chassis guide. Then line up connecting pins with the matching connector on the Main PCA, and slide the pca into position.
2. Install the single 6-32, 1/4-inch panhead Phillips screw in the corner of the IEEE-488 PCA.
3. If necessary, attach the rear panel connector using a 7-mm nut driver.
4. At the pca, attach the ribbon cable leading from the rear panel connector.

3-26. Install the Memory PCA (2625A Only)

Note

The Memory PCA and the IEEE-488 PCA occupy the same position and use the same connection to the Main PCA. The Memory PCA is a standard part of the Hydra Data Logger (Model 2625A). The IEEE-488 PCA is not available with the 2625A but is optional with the Hydra Data Acquisition Unit (Model 2620A).

1. Place the Memory PCA into position so that the edge of the pca fits in the chassis guide. Then line up connecting pins with the matching connector on the Main PCA, and slide the pca into position.
2. Install the single 6-32, 1/4-inch panhead Phillips screw in the corner of the Memory PCA.

3-27. Install the Memory Card I/F PCA (2635A Only)

1. Place the Memory Card I/F PCA (Q) into position so that the three mounting holes line up with the chassis supports located at the front-center of the chassis.
2. Install the three 6-32, 1/4-inch panhead Phillips screws in the mounting holes of the Memory Card I/F PCA.
3. Reconnect the high-density ribbon cable (O) to the connector on the Memory Card Interface PCA (Q).

3-28. Assemble the Front Panel Assembly

As appropriate, use the following steps to assemble the Front Panel Assembly.

1. Clean the lens (M) with deionized air and, if necessary, isopropyl alcohol. Then gently snap the lens into the front panel tabs.
2. Fit the elastomeric keypad assembly (L) through the Front Panel Assembly.
3. Slide the Display PCA into the bottom securing tabs on the back of the Front Panel Assembly. Then gently snap the pca into place.

Note

The Display PCA provides a space for a center screw. If the peripheral tabs are intact, this screw is not necessary. If some of the tabs are broken, the screw can be used as an additional securing device.

4. Connect the 20-pin cable (G) to the Display PCA.

3-29. Install the Front Panel Assembly

Use the following procedure when installing the Front Panel Assembly:

1. Position the Front Panel Assembly into place and snap the four tab retainers (I) onto the chassis.
2. Observing the alignment orientation provided by tabs on the connector, attach the display ribbon cable connector (G) on the Main PCA.
3. Using needle nose pliers, connect the wires at the rear of the recessed input terminals (Red to VΩ, Black to COM).

3-30. Install the Handle and Mounting Brackets

Refer to Figure 3-3 during the following procedure. Use a Phillips head screwdriver to attach the two handle mounting brackets. Note that these brackets must be reinstalled in their original positions. Therefore, the inside of each bracket is labeled with an R or an L, in reference to the front view of the instrument.

Now, engage the handle. Point the handle straight up. Then pull out on each end of the handle to engage the respective pivot in its bracket. Pull out slightly on both pivots to rotate the handle to the desired position.

3-31. Install the Instrument Case

Reinstall the instrument case, checking that it seats properly in the front panel. Attach the rear bezel with the two panhead Phillips screws and secure the case with the flathead Phillips screw in the bottom. Refer to Figure 3-2.

Chapter 4
Performance Testing and Calibration

4-1. Introduction

This section of the Service Manual provides performance tests that can be used at any time to verify that Hydra (2620A, 2625A, or 2635A) operation is within published specifications. A complete calibration procedure is also included. The performance test and, if necessary, the calibration procedure can be performed periodically as well as after service or repair.

4-2. Required Equipment

Equipment required for Performance Testing and Calibration is listed in Table 4-1.

Table 4-1. Recommended Test Equipment

Instrument Type	Minimum Specifications			Recommended Model
Multifunction Calibrator	DC Voltage: Range: 90 mV to 300V dc. Accuracy: 0.005%			Fluke 5700A
	AC Voltage:			
	Frequency 1 kHz 100 kHz	Voltage 29 mV to 300V 15 mV to 300V	Accuracy 0.05% 1.25%	
	Frequency:			
	10 kHz	1V rms	.0125%	
Decade Resistance Source	290Ω or 190Ω 2.9 kΩ1.9 kΩ 29 kΩ19 kΩ 290 kΩ190 kΩ 2.9 MΩ1.9 MΩ		Accuracy 0.003% 0.003% 0.003% 0.003% 0.0005%	Fluke 5700A
Mercury Thermometer	0.02 degrees Celsius resolution			Princo ASTM-56C
Thermocouple Probe	Type K			Fluke P-20K
Room Temperature Oil/Water Bath	Thermos bottle and cap			
Multimeter	Measures +5V dc.			Fluke 77
Signal Generator	Sinewave, 0.5 to 1V rms 10 Hz to 5 kHz			Fluke PM5136
Alternate Equipment List (Minimum specifications are the same as in the Standard Equipment List)				
Instrument Type DMM Calibrator Function/Signal Generator Decade Resistance Source	Recommended Model Fluke 5500A Fluke PM5193 or Fluke PM5136 Gen Rad 1433H			

4-3. Performance Tests

When received, the instrument is calibrated and in operating condition. The following performance verification procedures are provided for acceptance testing upon initial receipt or to verify correct operation at any time. All tests may be performed in sequence to verify overall operation, or the tests may be run independently.

If the instrument fails any of these performance tests, calibration adjustment and/or repair is needed. To perform these tests, use a Fluke 5700A Multifunction Calibrator or equipment that meets the minimum specifications given in Table 4-1.

Each of the measurements listed in the following steps assumes the instrument is being tested after a 1/2 hour warmup, in an environment with an ambient temperature of 18 to 28 degrees Celsius and with a relative humidity of less than 70%.

Note

All measurements listed in the performance test tables are made in the slow reading rate unless otherwise noted.

⚠ Warning

Hydra contains high voltages that can be dangerous or fatal. Only qualified personnel should attempt to service the instrument.

4-4. Accuracy Verification Test

1. Power up the instrument and wait 1/2 hour for its temperature to stabilize.
2. Connect a cable from the Output VA HI and LO connectors of the 5700A to the VΩ and COM connectors on the Hydra front panel. Select the channel 0 function and range on Hydra and the input level from the 5700A using the values listed in Table 4-2. Press MON to measure and display the measurement value for channel 0. The display should read between the minimum and maximum values (inclusive) listed in the table.

4-5. Channel Integrity Test

Verify that the Accuracy Verification Test for channel 0 meets minimum acceptable levels before performing this test.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect a pair of test leads to the H (high) and L (low) terminals of channel 1. Reinstall the Input Module into the instrument.
3. Connect the ends of the test leads together to apply a short (0 ohms).
4. Reconnect power, and turn the instrument ON.
5. For channel 1, select the 2-terminal ohms function and 300-ohms range on Hydra. Press MON and ensure that the display reads a resistance of less than or equal to 4.0Ω. (This test assumes that lead wire resistances are less than 0.1Ω.)
6. Open the ends of the test leads and ensure that the display reads "OL" (overload).
7. Press MON to stop the measurement.

Table 4-2. Performance Tests (Voltage, Resistance, and Frequency)

FUNCTION	RANGE	INPUT LEVEL	FREQUENCY	DISPLAY ACCURACY (1 Year, 18-28°C)	
				MIN	MAX
DC Volts	90 mV *	short (0)	—	-0.007	0.007
	90 mV *	90 mV	—	89.962	90.038
	300 mV	short (0V)	—	-0.02	0.02
	300 mV	150 mV	—	149.93	150.07
	300 mV	290 mV	—	289.89	290.11
	900 mV* **	900 mV	—	899.70	900.30
	3V	2.9V	—	2.8988	2.9012
	3V	-2.9V	—	-2.9012	-2.8988
	30V	29V	—	28.990	29.010
	150V	150V	—	149.94	150.06
	300V	290V	—	289.90	290.10
* Range only used on 2635A (not used in autoranging). ** Computer I/F only (see FUNC command).					
Note *Voltages greater than 150V can only be applied to channels 0, 1, and 11.*					
AC Volts	300 mV	20 mV	1 kHz	19.71	20.28
	300 mV	20 mV	100 kHz	18.50	21.50
	300 mV	290 mV	1 kHz	289.26	290.74
	300 mV	900 mV	100 kHz	275.00	305.00
	3V	2.9V	1 kHz	2.8934	2.9066
	30V	29V	1 kHz	28.931	29.069
	150V	150V	1 kHz	149.54	150.46
	300V	290V	1 kHz	289.34	290.66
Note *Voltages greater than 150V can only be applied to channels 0, 1, and 11. The rear Input Module must be installed when measuring ac volts on channel 0.*					
Resistance (4-Terminal)					
Note *For 2-terminal measurements, the resistance accuracy given in this table applies to channel 0 only and makes allowance for up to 0.05Ω of lead wire resistance. You must add any additional lead wire resistance present in your set up to the resistance values given in this table.*					
Using inputs in decades of 3:					
	300Ω	short		0.00	0.09
	—	300Ω		299.80	300.27
	3 kΩ	short		0.0000	0.0003
	—	3 kΩ		2.9981	3.0020
	30 kΩ	30 kΩ		29.980	30.020
	300 kΩ	300 kΩ		299.81	300.19
	3 MΩ	3 MΩ		2.9979	3.0021
Using inputs in decades of 1.9:					
	300Ω	short		0.00	0.09
	—	190Ω		189.87	190.20
	3 kΩ	short		0.0000	0.0003
	—	1.9 kΩ		1.8987	1.9014
	30 kΩ	19 kΩ		18.987	19.013
	300 kΩ	190 kΩ		189.87	190.13
	3 MΩ	1.9 MΩ		1.8986	1.9014

Table 4-2. Performance Tests (Voltage, Resistance, and Frequency) (cont)

FUNCTION	RANGE	INPUT LEVEL	FREQUENCY	DISPLAY ACCURACY (1 Year, 18-28°C)	
				MIN	MAX
	300Ω	short		0.00	0.09
	—	100Ω		99.92	100.15
	3 kΩ	short		0.0000	0.0003
	3 kΩ	1 kΩ		0.9992	1.0009
	30 kΩ	10 kΩ		9.992	10.008
	300 kΩ	100 kΩ		99.92	100.08
	3 MΩ	1 MΩ		0.9992	1.0008
	10 MΩ	10		9.986	10.014
* Optional test point if standards available.					
Note *All channels (0 through 20) can accommodate 2-terminal resistance measurements. Channel 0, with only two connections, cannot be used for 4-terminal measurements. Four-terminal resistance measurements can be defined for channels 1 through 10 only. Channels 11 through 20 are used, as required, for 4-terminal to provide the additional two connections. For example, a 4-terminal set up on channel 1 uses channels 1 and 11, each channel providing two connections.*					
Frequency	90 kHz	10 kHz/2V p-p		9.994	10.006

8. Connect a cable from the Output VA HI and LO of the 5700A to the Input Module test leads (observe proper polarity).
9. Select the VDC function and 300-volt range on Hydra and apply 0V dc from the 5700A. Then apply 290V dc input from the 5700A. Ensure the display reads between the minimum and maximum values as shown in Table 4-2 for the 0 and 290V dc input levels.

   Note

   Channels 0, 1, and 11 can accommodate a maximum input of 300V dc or ac. However, the maximum input for all other channels can only be 150V dc or ac.
10. With the exception of the selected voltage range and input voltagefrom the 5700A, repeat steps 1 through 9 for each remaining InputModule channel (2 through 20). Channels 2 through 10 and 12 through20 should be configured for the 150V dc range and an input voltageof 150 volts.

4-6. Thermocouple Measurement Range Accuracy Test

Verify that the Accuracy Verification Test for channel 0 meets minimum acceptable levels before performing this test.

Thermocouple temperature measurements are accomplished using the Hydra internal 100 mV and 1V dc ranges. (The ranges are not configurable by the operator.) This procedure provides the means to test these ranges.

Testing the 100 mV and 1V dc ranges requires computer interfacing with a host (terminal or computer). The host must send commands to select these ranges. These ranges cannot be selected from the Hydra front panel.

1. Ensure that communication parameters (i.e., transmission mode, baud rate, parity, and echo mode) on Hydra and the host are properly configured to send and receive serial data. Refer to Section 4 of the Hydra Users Manual.
2. Power up Hydra, and wait 1/2 hour for its temperature to stabilize.
3. Connect a cable from the Output VA HI and LO connectors of the 5700A to the VΩ and COM connectors on the Hydra front panel.
4. Set the 5700A to output 0V dc.
5. Using either a terminal or a computer running a terminal emulation program as the selected host, send the following commands to Hydra:

   FUNC 0,VDC,I100MV <CR>

   MON 1,0 <CR>

   MON_VAL? <CR>

   The returned value for channel 0 should be 0 mV ±0.007 mV.

   Set the 5700A to output 90 mV DC. Send the following command:

   MON_VAL? <CR>

   The value returned should now be 90 mV ±0.038 mV (between 89.962 and 90.038 mV).
6. Change the Hydra channel 0 function to the internal 1V dc range by redefining channel 0. Send the following commands:

   MON 0 <CR>

   FUNC 0,VDC,I1V <CR>

   Set the 5700A to output 0.9V dc. Send the following commands:

   MON 1,0 <CR>

   MON_VAL? <CR>

   The value returned should be 900 mV ±0.22 mV (899.78 to 900.22 mV.)

4-7. 4-Terminal Resistance Test

Verify that the channel 0 accuracy verification tests for dc volts and ohms meet minimum acceptable levels.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect a pair of test leads (keep as short as possible) to the H (high) and L (low) terminals of channel 1 and a second pair of test leads to the H and L terminals of channel 11. Reinstall the Input Module into the instrument.
3. Observing polarity, connect the channel 1 test leads to the Sense HI and LO terminals of the 5700A and the channel 11 test leads to the Output HI and LO terminals of the 5700A. Route wires with the method shown in Figure 4-1. Connect the wires to the terminals shown in Figure 4-2.

   Note

   4-terminal connections are made using pairs of channels. 4-terminal measurements can be made only on channels 1 through 10. The accompanying pairs are channels 11 through 20.

4. Switch the instrument ON.
5. Select the 4-terminal OHMS function, AUTO range, for channel 1 on Hydra.
6. Set the 5700A to output the resistance values listed in Table 4-2 (Use decades of 1.9).
7. On Hydra press MON and ensure the display reads between the minimum and maximum values (inclusive) shown in Table 4-2.
8. The 4-terminal Resistance Test is complete. However, if you desire to perform this test on other Input Module channels (2 through 10), repeat steps 1 through 7, substituting in the appropriate channel number.

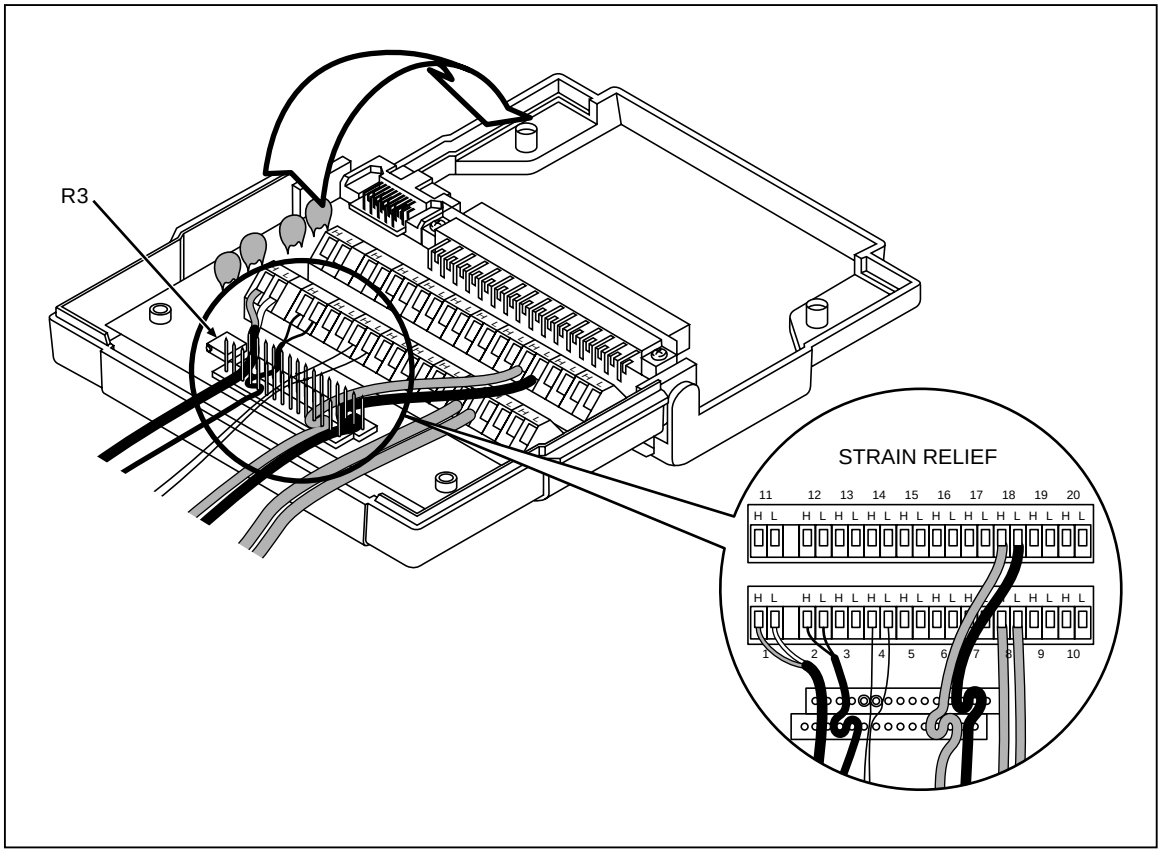


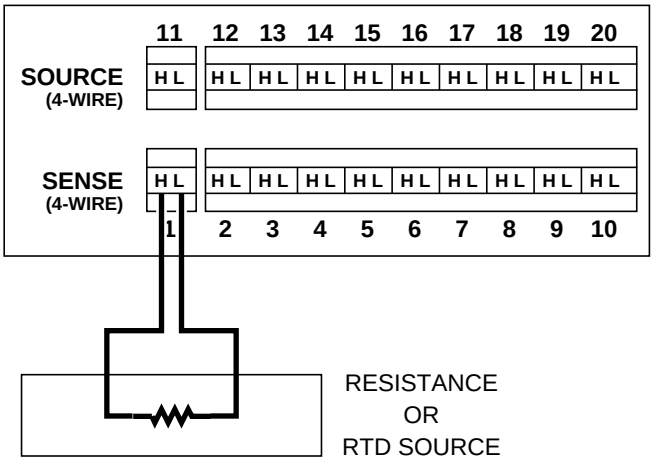
Figure 4-1. Input Module

4-8. Thermocouple Temperature Accuracy Test

Verify that the Thermocouple Measurement Range Accuracy Test meets minimum acceptable levels before performing this test.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module, and connect a K-type thermocouple to the H (high) and L (low) terminals of channel 1. (See Table 4-3 for lead colors). Then reinstall the Input Module into the instrument.

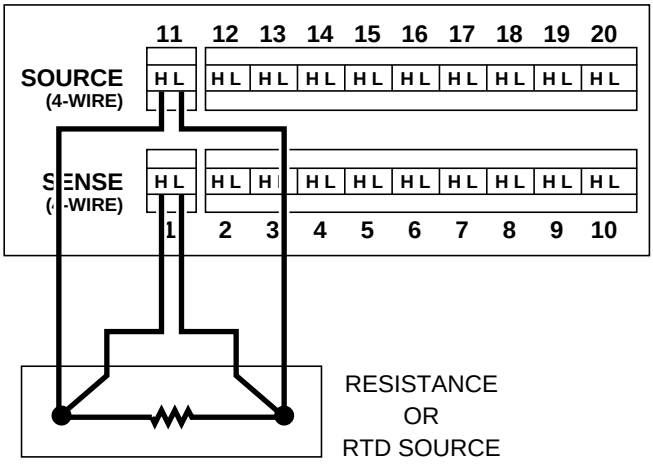
2-WIRE (2T) CONNECTION



USE H AND L TERMINALS FOR ANY CHANNEL.

- CHANNEL 0 ON FRONT PANEL
- CHANNELS 1 THROUGH 20 ON REAR PANEL INPUT MODULE (CHANNEL 1 SHOWN HERE).

4-WIRE (4T) CONNECTION



USE H AND L TERMINALS FOR TWO CHANNELS ON REAR PANEL INPUT MODULE. CONNECTIONS FOR CHANNEL 1 SHOWN HERE WITH CHANNEL 11 PROVIDING ADDITIONAL TWO CONNECTIONS.

FOR EACH 4-WIRE CONNECTION, ONE SENSE CHANNEL (1 THROUGH 10) AND ONE SOURCE CHANNEL (SENSE CHANNEL NUMBER +10 = 11 THROUGH 20) ARE USED.

s27f.eps

Figure 4-2. 2T and 4T Connections

Note

If other than a K type thermocouple is used, be sure that the instrument is set up for the type of thermocouple used.

3. Reconnect power and switch the instrument ON.
4. Insert the thermocouple and a mercury thermometer (.02 degrees Celsius resolution) in a room temperature bath. Allow 20 minutes for thermal stabilization.
5. Select the temperature function and K thermocouple type for channel 1. Then press MON.
6. The value displayed should be the temperature of the room temperature bath (within tolerances given in Table 4-4) as measured by the mercury thermometer.
7. The Thermocouple Temperature Accuracy Test is complete. However if you desire to perform this test on any other Input Module channel (2 through 20) repeat steps 1 through 6 substituting in the appropriate channel number.

Table 4-3. Thermocouple Information

Type	Positive Lead Material	Positive Lead Color		Negative Lead Material	Usable Range (°C)
		ANSI*	IEC**		
J	Iron	White	Black	Constantan	-200 to 760
C†	Tungsten (5% Rhenium)	White	—	Tungsten (26% Rhenium)	0 to 2316
b	Platinum (30% Rhodium)	Gray	—	Platinum (6% Rhodium)	0 to 1820
S	Platinum	Black	Orange	Platinum (10% Rhodium)	-50 to 1768
R	Platinum	Black	Orange	Platinum (13% Rhodium)	-50 to 1768
N	NICROSIL	Orange	—	NISIL	-270 to 1300
T‡	Copper	Blue	Brown	Constantan	-270 to 400
E	Chromel	Purple	Violet	Constantan	-270 to 1000
K	Chromel	Yellow	Green	Alumel	-270 to 1372

* American National Standards Institute (ANSI) device negative lead is always red.
** International Electrotechnical Commission (IEC) device negative lead is always white.
† Not an ANSI designation but a Hoskins Engineering Company designation.
‡ An ANSI type T is supplied with the meter.

Table 4-4. Performance Tests for Thermocouple Temperature Function

Thermocouple Type	Themocouple Temperature Function 1 Year @ 18-28°C
J	± 0.4°C
K	± 0.5°C
N	± 0.6°C
E	± 0.4°C
T	± 0.5°C

4-9. Open Thermocouple Response Test

Use the following procedure to test the open thermocouple response:

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect test leads to the H (high) and L (low) terminals of channel 1. Reinstall the Input Module into the instrument.
3. Reconnect power and switch the instrument ON.
4. Connect the test leads from the Input Module to an 820 ohm resistor.
5. Select the temperature function and K thermocouple type for channel 1. Then press MON.
6. The value displayed should approximate the ambient temperature.
7. Replace the 820-ohm resistor with a 4-kilohm resistor to simulate a high resistance or open thermocouple.
8. Verify a reading of "otc".
9. The Open Thermocouple Response Test is complete. However if you desire to perform this test on any other Input Module channel (2 through 20) repeat steps 1 through 8, substituting the appropriate channel number.

4-10. RTD Temperature Accuracy Test

The following two RTD Temperature Accuracy Tests are different in that one uses a Decade Resistance Source and the other uses an RTD. Only one of the tests needs to be performed to verify operation.

4-11. RTD Temperature Accuracy Test (Using Decade Resistance Source).

Verify that the channel 0 accuracy verification tests for dc volts and 300-ohm range meet minimum acceptable levels.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect a pair of test leads (keep as short as possible) to the H (high) and L (low) terminals of channel 1. For 4-terminal performance testing, connect a second pair of test leads to the H (high) and L (low) terminals of channel 11. Reinstall the Input Module into the instrument.
3. Connect the channel 1 test leads to the Output HI and LO terminals on the Decade Resistance Source. For 4-terminal performance testing, also connect channel 11's test leads to the Output HI and LO terminals of the Decade Resistance Source. Connect as shown in Figures 4-1 and 4-2.

   Note

   4-terminal connections are made using pairs of channels. 4-terminal measurements can only be made on channels 1 through 10. The accompanying pairs are channels 11 through 20.
4. Switch the instrument ON.
5. Select the 4-terminal RTD temperature function, RTD type PT, for channel 1 on Hydra.
6. Press MON. For each resistance, ensure that the display reads within the range shown in Table 4-5.

7. The RTD Temperature Accuracy test is complete. However, if you desire to perform this test on Input Module channels (2 through 10), repeat steps 1 through 5 substituting in the appropriate channel number.

Note

The only type of temperature measurement that can be made on channel 0 is 2-terminal RTD. Channels 11 through 20 support only 2-terminal RTDs.

Table 4-5. Performance Tests for RTD Temperature Function (Resistance Source)

Decade Reisitance Source	Simulated °C Temperature		Temperature Accuracy Specifications 1 Year @ 18-28°C
	2620A/2635A*	2635A*	
100Ω	0	0	±0.24°C
200Ω	266.58	266.34	±0.48°C
300Ω	558.00	557.70	±0.75°C

* RTD temperature linearizations changed between the 2620A/2625A and 2635A Hydra instrument firmware. The 2620A & 2625A Hydra instruments are based on the International Practical Temperature Scale of 1968 (IPTS-68). The 2635A Hydra Instrument is based on the International Temperature Scale of 1990 (ITS-90).

These figures assume that RTD R0 is set to 100.00Ω for each channel.

Accuracy given is for 4-wire measurements only.

4-12. RTD Temperature Accuracy Test (Using DIN/IEC 751).

1. Switch OFF power to the instrument and disconnect all other high voltage inputs.
2. Remove the Input Module from the rear of the instrument. Open the Input Module and connect a Platinum RTD, conforming to the European Standards IEC 751 (DIN 43760).

   2-terminal RTD: Connect the RTD excitation leads to the H (high) and L (low) terminals of channel 1.

   4-terminal RTD: Connect the RTD excitation leads (one red and one black wire) to the H (high) and L (low) terminals of channel 11. Connect the second pair of RTD red and black leads to the H and L leads of channel 1. (Refer to Figures 4-1 and 4-2 for proper connection.) Reinstall the Input Module into the instrument.

   Note

   4-terminal connections are made using pairs of channels. 4-terminal measurements can only be made on channels 1 through 10. Their accompanying pairs are channels 11 through 20.
3. Switch the instrument ON.
4. Insert the RTD probe and a mercury thermometer in a room temperature bath. Allow 20 minutes for thermal stabilization.
5. Depending on the type of connection made in step 2, select either the 2-Terminal or 4-Terminal RTD temperature function, RTD type PT (DIN IEC 751), for channel 1 on Hydra. Press MON and ensure the display reads the temperature of the room temperature bath (within tolerances shown in Table 4-6) as measured by the mercury thermometer.

6. The RTD Temperature Accuracy test is complete. However, if you desire to perform this test on any other channel (0 or 2 through 20), repeat steps 1 through 5, substituting the appropriate channel number.

Note

The only type of temperature measurement that can be made on channel 0 is 2-terminal RTD. Channels 11 through 20 support only 2-terminal RTDs.

Table 4-6. Performance Tests for RTD Temperature Function (DIN/IEC 751)

RTD Type (DIN 43760 RTD)	Temperature Accuracy Specifications 1 Year @ 18-28°C
2-wire (channel 0)	-0.65°C to +0.70°C
4-wire	-0.65°C
(Assumes RTD R0 is set to 100.00Ω for each channel.)	

4-13. Digital Input/Output Verification Tests

Digital Input/Output verification testing requires computer interfacing with a host (terminal or computer). The host must send commands to the instrument to control the digital lines for this test. Refer to Section 4 of the Hydra Users Manual for a description of configuring and operating the instrument.

4-14. Digital Output Test.

1. Ensure that communication parameters (i.e., transmission mode, baud rate, parity, and echo mode) on Hydra and the host are properly configured to send and receive serial data.
2. Switch OFF power to the instrument and disconnect all high voltage inputs.
3. Remove the ten-terminal Digital I/O connector from the rear of the instrument and all external connections to it. Connect short wires (to be used as test leads) to the ground (⏚) and 0 through 7 terminals. Leave the other wire ends unconnected at this time. Reinstall the connector.
4. Switch power ON to both Hydra and the host. Verify that Hydra is not scanning. If Hydra is scanning, press SCAN to turn scanning off, then cycle power off and on again.
5. Using a digital multimeter (DMM), verify that all digital outputs (0-7) are in the OFF or HIGH state. This is done by connecting the low or common of the multimeter to the ground test lead and the high of the multimeter to the digital output and verifying a voltage greater than +3.8V dc.
6. Using either a terminal or a computer running a terminal emulation program, set up Hydra to turn Digital Outputs ON (LOW state).

   In sequence send the following commands to Hydra and measure that the correct Digital Output line measures less than +0.8V dc (LOW state.)

   DO_LEVEL 0,0 <CR>

   Verify that output 0 measures a LOW state.

   DO_LEVEL 1,0 <CR>

   Verify that output 1 measures a LOW state.

   DO_LEVEL 2,0 <CR>

   Verify output 2 measures a LOW state.

   Repeat the command for all eight outputs.
7. Set up Hydra to turn Digital Outputs OFF (HIGH state).

Send the following commands to Hydra in sequence, and measure that the correct Digital Output line measures greater than +3.8V dc (HIGH state.)

DO_LEVEL 0,1 <CR>

Verify that output 0 measures a HIGH state.

DO_LEVEL 1,1 <CR>

Verify that output 1 measures a HIGH state.

Repeat the command for all eight outputs.

4-15. Digital Input Test

1. Perform the DIGITAL OUTPUT TEST steps 1 through 5.
2. Using either a terminal or a computer running a terminal emulation program, read the Hydra Digital Input lines.

   Send the following command to Hydra:

   DIO_LEVELS? <CR>

   Verify that the returned value is 255.

   Note

   The number returned is the decimal equivalent of the Digital Input binary word (status of inputs 0 through 7). See Table 4-7 to determine if the number returned corresponds to the inputs jumpered to ground in this test.

3. Jumper input 0 to ground by connecting the ground test lead to the input 0 test lead.

   Then send the following command to Hydra:

   DIO_LEVELS? <CR>

   Verify that the returned value is 254.
4. Disconnect input 0 from ground, then jumper input 1 to ground.

   Send the command: DIO_LEVELS? <CR>

   Verify that the returned value is 253.
5. Repeat step 4 for each input and verify the correct returned value (See Table 4-7).

Table 4-7. Digital Input Values

Terminal Grounded	State of Digital Inputs	Decimal Value
none	Inputs 0-7, all HIGH	255
0	Inputs 1-7 HIGH, input 0 LOW	254
1	Inputs 0,2-7 HIGH, input 1 LOW	253
2	Inputs 0-1 and 3-7 HIGH, input 2 LOW	251
3	Inputs 0-2 and 4-7 HIGH, input 3 LOW	247
4	Inputs 0-3 and 5-7 HIGH, input 4 LOW	239
5	Inputs 0-4 and 6-7 HIGH, input 5 LOW	223
6	Inputs 0-5 and 7 HIGH, input 6 LOW	191
7	Inputs 0-6 HIGH, input 7 LOW	127

4-16. Totalizer Test

This totalizer verification test requires toggling Digital Output line 0 and using it as the Totalizer input. The test requires computer interfacing with a host (terminal or

computer). The host must send commands to Hydra to control the digital line for this test.

1. Ensure that communication parameters (i.e., transmission mode, baud rate, parity, and echo mode) on Hydra and the host are properly configured to send and receive serial data. Refer to Section 4 of the Hydra Users Manual.
2. Switch OFF power to the instrument and disconnect all high voltage inputs.
3. Remove the ten-terminal Digital I/O connector from the rear of the instrument and all external connections to it. Connect short wires (to be used as test leads) to the 0 terminal and the Totalizer ($\sum$) terminal. Leave other ends of wires unconnected at this time. Reinstall the connector.
4. Switch ON power to both Hydra and the host.
5. Press the TOTAL button on the front panel of Hydra.

   Verify that Hydra displays a 0 value.
6. Jumper output 0 to the Totalizer ($\sum$) input by connecting the ($\sum$) terminal test lead to the output 0 test lead.
7. Using either a terminal or a computer running a terminal emulation program, set up Hydra to toggle (turn ON and OFF) Digital Output 0.

   Send the following commands to Hydra in sequence, and verify that Hydra measures and displays the correct total value:

   DO_LEVEL 0,0 <CR>
   DO_LEVEL 0,1 <CR>

   Verify that Hydra displays a totalizer count of 1.
8. Send the following commands in sequence:

   DO_LEVEL 0,0 <CR>
   DO_LEVEL 0,1 <CR>

   A totalizer count of 2 should now be displayed.
9. Repeat step 8 for each incremental totalizing count.
10. Set the Hydra totalized count to a value near full range (65535) and test for overload.

    Send the following commands to Hydra:

    TOTAL 65534 <CR>
    DO_LEVEL 0,0 <CR>
    DO_LEVEL 0,1 <CR>

    A totalizer count of 65535 should be displayed.
11. Send:

    DO_LEVEL 0,0 <CR>
    DO_LEVEL 0,1 <CR>

    The Hydra display should now read "OL", indicating that the counter has been overrun.

4-17. Totalizer Sensitivity Test

1. Perform a successful Totalizer Test.
2. Remove the jumper connecting the $\sum$ terminal test lead to the output 0 test lead.

3. Verify that Hydra is still in the total measuring mode. If not, press the TOTAL button. Reset the totalizer count shown on the display by pressing the SHIFT and TOTAL(ZERO) buttons.

   The Hydra display should now show a value of 0.

4. Connect the output of the signal generator to the $\sum$ and ⏚ terminals.
5. Program the signal generator to output a 1.5V rms sine signal at 10 Hz.

   The Hydra display should now show the totalizing value incrementing at a 10 count per second rate.

4-18. Dedicated Alarm Output Test

The Dedicated Alarm Output Test verifies that Alarm Outputs 0 through 3 are functioning properly. Because this test is dependent on voltage readings the Accuracy Verification Test for channel 0 and the Channel Integrity Test for channels 1 through 3 should be performed if voltage readings are suspect.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the eight-terminal Alarm Output connector from the rear of Hydra and all external connections to it. Connect short wires (to be used as test leads) to the [⏚] and 0 through 3 terminals. Leave the other ends of the wires unconnected at this time. Reinstall the connector.
3. Remove the Input Module from the rear of Hydra. Open the Input Module and jumper the H (high) terminal of channels 1, 2, and 3 together. Connect a test lead to the H of channel 1. Also jumper the L (low) terminals of channel 1, 2, and 3 together. Connect a second test lead to the L of channel 1. Reinstall the Input Module into Hydra. Refer to Figure 4-3.
4. Switch power ON.
5. Using a digital multimeter (DMM), verify that alarm outputs 0 through 3 are in the OFF or HIGH state. Perform this test by connecting the low or common of the multimeter to the ground test lead and the high of the multimeter to the alarm output. Verify a voltage greater than +3.8V dc.
6. Connect a cable from the Output VA HI and LO connectors of the 5700A to the VΩ and COM connectors on the front panel of Hydra. Then jumper the Hydra VΩ terminal to the H (high) test lead of the Input Module and the COM terminal to the L (low) test lead.
7. On Hydra, select the VDC function, 3V range, and assign a HI alarm limit of +1.0000 for channels 0 through 3. Set up all other channels (4-20) to the OFF function. Select a scan interval of 5 seconds.
8. Set the 5700A to output +0.9900 volts.
9. Press SCAN. Hydra should scan channels 0 through 3 every 5 seconds.
10. Using a digital multimeter, again verify that alarm outputs 0 through 3 are in the OFF or HIGH state.
11. Set the 5700A to output +1.1000 volts. Verify that the alarm outputs 0 through 3 are in the ON or LOW state (measure less than +0.8V dc).

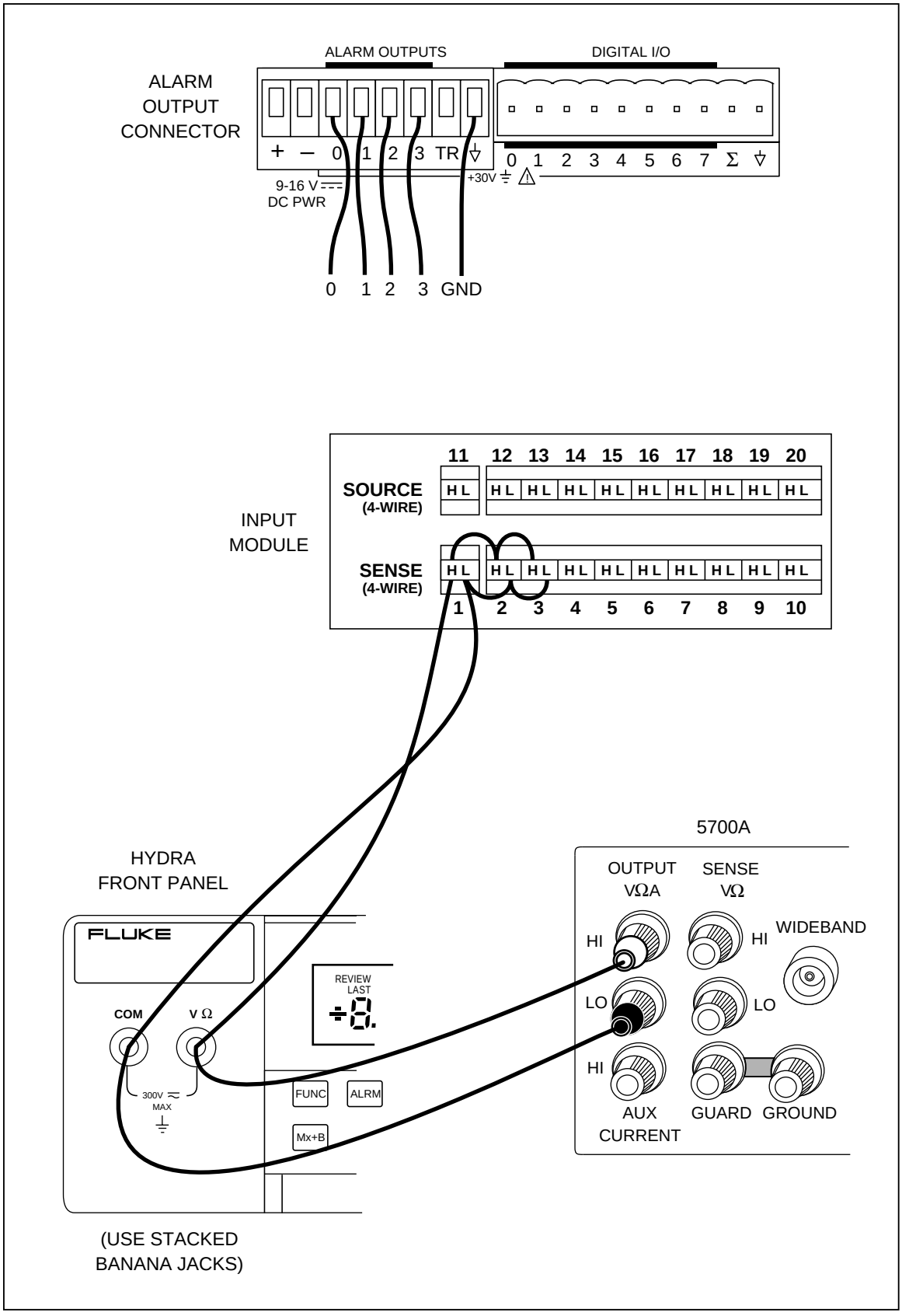


Figure 4-3. Dedicated Alarms Test

4-19. External Trigger Input Test

The External Trigger Input Test verifies that the rear panel trigger input of Hydra is functioning properly.

1. Switch OFF power to the instrument and disconnect all high voltage inputs.
2. Remove the eight-terminal Alarm Output connector from the rear of Hydra and all external connections to it. Connect short wires (to be used as test leads) to the ⏚ and TR terminals. Leave other ends of wires unconnected at this time. Reinstall the connector. Refer to Figure 4-4.
3. Switch power ON.
4. On Hydra, select the VDC function, 30V range for channels 0 through 5. Select a scan interval of 30 seconds.
5. Select trigger ON to enable the external trigger input. Press SHIFT, then MON(TRIGS). (The display shows TRIG.) Then press either the up or down arrow buttons until the display shows ON. Finally, press ENTER.
6. Press the Hydra SCAN button. Hydra should scan channels 0 through 5 once every 30 seconds.
7. During the interval when scanning is not occurring, connect (short) the test leads of the TR and ground Alarm Output terminals.

   Ensure the connection causes a single scan to occur.
8. Disconnect (open) the TR and ground connection.

   Ensure the scan continues to execute at its specified interval.

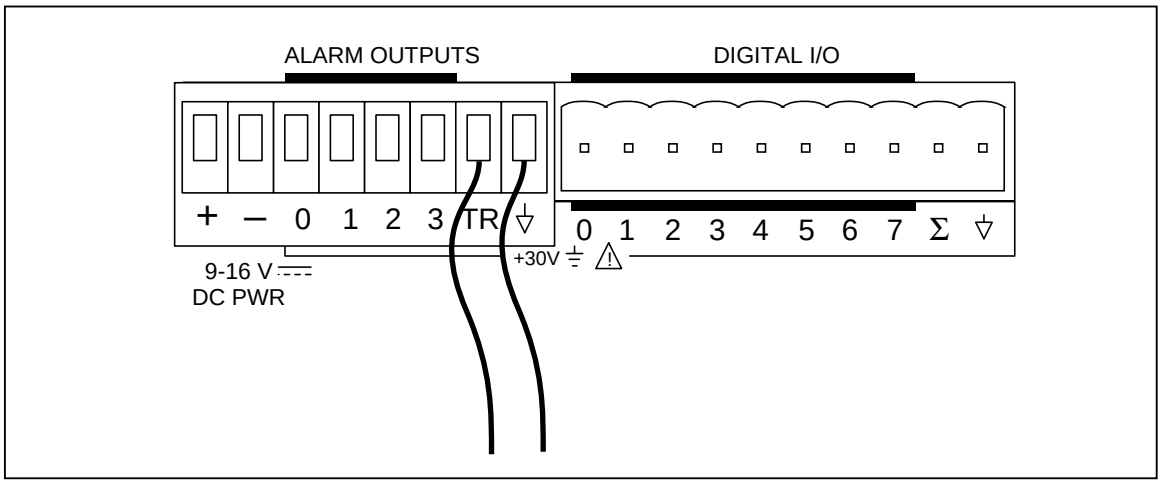


Figure 4-4. External Trigger Test

4-20. Calibration

Hydra calibration is controlled with computer interface commands. The 2620A may be calibrated by using the IEEE-488 or RS-232 interface, but the 2625A and 2635A may only be calibrated via their RS-232 interface. Local (front panel) calibration is not possible.

Activate calibration mode by pressing and holding the CAL Enable button (front panel) for approximately 4 seconds. Release the button after Hydra beeps and the CAL annunciator lights.

Note

The CAL Enable button is located on the right side of the display and is recessed beneath a calibration seal. Press this button with a blunt-tipped object. Avoid using a sharper-tipped object (such as a pencil). Do not press CAL ENABLE unless you intend to calibrate the instrument. If you have activated Calibration and wish to exit calibration immediately, press CAL ENABLE momentarily a second time.

The instrument must be stabilized in an environment with ambient temperature of 22 to 24ºC and relative humidity of less than 70% and have been turned on for at least 1/2 hour prior to calibration.

The instrument should normally be calibrated on a regular cycle, typically every 90 days or 1 year. The chosen calibration cycle depends on the accuracy specification you wish to maintain. The instrument should also be calibrated if it fails the performance test or has undergone repair.

The instrument features closed-case calibration controlled over the Computer Interface. Using known reference sources, closed-case calibration has many advantages. There are no parts to disassemble, no mechanical adjustments to make, and the instrument can be calibrated by an automated instrumentation system.

Once the instrument is in calibration mode, closed-case calibration can be made for the four calibration groups: Volts DC, Volts AC, Resistance, and Frequency. Once begun, each group must be completed successfully for the results of the calibration to be made permanent. It is not necessary to perform all calibration groups. Each group is independent of the other three groups; completion of a group sets the constants for that group.

Analog inputs are made at the rear-panel Input Module, and computer interface commands are used to control each step of the process. Either of the following two closed-case calibration procedures can be used:

- Using Hydra Starter Calibration Software

  This procedure uses software supplied with this Service Manual.Instructions for each step are presented on the PC screen.

- Using a Terminal

  This procedure relies on individual commands for each step. A summaryof these commands is presented in Table 4-8.

With either closed-case procedure, an additional procedure (reference junction calibration) may be used to calibrate the thermocouple temperature function. This procedure requires physical access to the rear panel Input Module.

Note

The instrument returns a Device Dependent Error prompt (!>) if a calibration step fails. Usually, this happens if the reference is not within an anticipated range (5 to 15%, depending on the step). At this point, the response to the CAL_STEP? command equals the raw, uncalibrated reading taken on the reference input. Refer to Calibration Failures in Section 5 for more information.

To provide accuracy at full range, calibration is not recommended below one-third of full range (10000 counts).

Table 4-8. Calibration Mode Computer Interface Commands

<table>
<tr><th>Command</th><th>Description</th></tr>
<tr><td>Cal x</td><td>Start calibration of a new function.
<table>
<tr><td>x</td><td>Function to calibrate</td></tr>
<tr><td>1</td><td>VDC</td></tr>
<tr><td>2</td><td>VAC</td></tr>
<tr><td>3</td><td>ohms</td></tr>
<tr><td>4</td><td>Frequency</td></tr>
</table></td></tr>
<tr><td>CAL_CLR</td><td>Reset all calibration constants to nominal values, clearing present calibration.</td></tr>
<tr><td>CAL_CONST? xx</td><td>Return the value of the calibration constant indicated by xx.</td></tr>
<tr><td>CAL_REF?</td><td>Return the present calibration reference.</td></tr>
<tr><td>CAL_REF < value></td><td>Calibrate to <value>, rather than the default calibration reference value.</td></tr>
<tr><td>CAL_STEP?</td><td>Calibrate and return the calibrated value of the input.</td></tr>
<tr><td>EEREG? xx</td><td>Return the contents of the specified EEPROM register (xx).</td></tr>
<tr><td colspan="2">The following additional computer interface commands can be used in calibration mode. Use of any other command results in an execution error. Refer to Section 4 of the Hydra Users Manual for complete information about these computer interface commands.

*CLS *ESE *ESE?*ESR?*IDN?*OPC *OPC?*RST *SRE *SRE?*STB?*TRG *WAI IEE IEE?IER?LOCS LWLS REMS RWLS</td></tr>
</table>

4-21. Using Hydra Starter Calibration Software

This procedure uses the Hydra Starter Package (with Calibration Software) for closed-case calibration. This software runs on an IBM PC or equivalent using the RS-232 interface. It consists of the following three files:

- An executable file (CAL.EXE)
- A help text file (CAL.HLP)
- A configuration initialization file (CAL.INI)

4-22. Setup Procedure Using Starter

Use the following procedure to set up Hydra and the PC prior to using the calibration feature of the Hydra Starter Package:

1. Connect a pair of test leads to the channel 1 H (high) and L (low) terminals on the Input Module. Connect a second pair of test leads to channel 11. (This second pair is used only for 4-wire resistance calibration.) Install the Input Module into Hydra.
2. Using the RS40 Terminal Interface Cable, connect the PC COM port to the Hydra RS-232 port. Use an RS40 and an RS41 cable in series to connect to the COM port on an IBM PC/AT.

3. From the CAL directory on the PC, type CAL. Then press any key to start the program and access the SETUP menu.
4. On Hydra, press POWER ON. After the initialization process has concluded, use the following procedure to set up communications:
   a. Press SHIFT and then LIST(COMM).
   b. With 'BAUd' displayed, use the UP or DOWN arrow key to selectthe desired baud rate. Then press ENTER.
   c. With 'PAR' (parity) displayed, use the UP or DOWN arrow key toselect the parity. Then press ENTER.
   d. With 'CtS' (2635A only; Clear to Send) displayed, use the UP orDOWN arrow key to select the Clear to Send flow control 'OFF'.Then press ENTER.
   e. With 'ECHO' displayed, use the UP or DOWN arrow key to select'OFF'. Then press ENTER. Communications setup for Hydra is nowcomplete.
5. On the PC, use the SETUP menu to match the communication parameters defined above for Hydra.
6. On Hydra, break the calibration seal on the front panel display. Then press and hold the CAL Enable button (approximately 4 seconds) until 'CAL' is displayed. Press this button with a blunt-tipped object. Avoid using a sharper-tipped object (such as a pencil).
7. On the PC, use the right and left arrow keys to select CAL. Then press the ENTER key. A message asking if you want to calibrate is displayed. Press Y and ENTER. The next displayed message specifies the voltage to be applied to channel 1.

4-23. Calibration Procedure Using Starter

Use the following procedure to calibrate Hydra with the Hydra Starter Package:

1. Connect the channel 1 test leads to the 5700A output.
2. On the 5700A, select the output voltage specified on the PC (step 7 above.)
3. On the PC, press ENTER. If the input voltage is within a predetermined acceptable boundary, Hydra performs a calibration for this step. The program then prompts you for the next input value.

   Note

   "Bad Calibration Input Value" is returned if the input is not acceptable (the calibration step could not be executed.) Verify that the input to Hydra channel 1 is the correct value and polarity. Also verify that the 5700A is in OPERATE mode. If the input is correct and "Bad Calibration Input Value" is still returned, repair of Hydra may be required.
4. Following the prompts, complete all steps for this calibration group.
5. You will then be asked if you want to perform the next calibration group. Press Y - ENTER.
6. Following the prompts, complete all steps in the remaining calibration groups.

4-24. Using a Terminal

This procedure can be used with either a terminal or a computer running a terminal emulation program.

4-25. Setup Procedure Using a Terminal.

Use the following procedure to set up Hydra and the PC:

1. Connect a pair of test leads to the high and low terminals of channel 1 on the Hydra Input Module. Connect a second pair of test leads to channel 11.
2. Install the Input Module into Hydra.
3. Connect the COM port of the PC or terminal to the Hydra RS-232 port using an RS40 Terminal Interface Cable. Use an RS40 and an RS41 cable in series to connect to the COM port on an IBM PC/AT.
4. On Hydra, press POWER ON. After the initialization process has concluded, use the following procedure to set up communications:
   a. Press SHIFT and then LIST(COMM).
   b. With 'BAUd' displayed, use the UP or DOWN arrow key to selectthe desired baud rate. Then press ENTER.
   c. With 'PAR' (parity) displayed, use the UP or DOWN arrow key toselect the parity. Then press ENTER.
   d. With 'CtS' (2635A only; Clear to Send) displayed, use the UP orDOWN arrow key to select the Clear to Send flow control 'OFF'.Then press ENTER.
   e. With 'ECHO' displayed, use the UP or DOWN arrow key to select'ON'. Then press ENTER. Communications setup for Hydra is nowcomplete.
5. On the terminal, match the communication parameters used for Hydra (above).
6. On Hydra, break the calibration seal on the front panel display. Then press and hold the CAL Enable button (approximately 4 seconds) until CAL is shown on the Hydra display. Press this button with a blunt-tipped object. Avoid using a sharper-tipped object (such as a pencil).
7. Connect the channel 1 test leads to the output of a 5700A.

4-26. Calibration Procedure Using a Terminal

Calibration procedures using a terminal (or a computer program that emulates a terminal) are presented in the following tables:

- DC Volts (CAL 1) Calibration:Table 4-9
- AC Volts (CAL 2) Calibration:Table 4-10
- Ohms (CAL 3) Calibration:Tables 4-11, 4-12
- Frequency (CAL 4) Calibration: Table 4-13

In the tables, the CAL_REF? query asks Hydra for the next calibration reference value. If some other value is to be used, the CAL_REF xxx.xxxx command tells Hydra the calibration reference value to expect.

To provide accuracy at full range, calibration is not recommended below one-third of full range (10000 counts).

Once the calibrator output has been set to Hydra, the CAL_STEP? query performs the calibration step and returns the calibrated value of the input. The response to CAL_STEP? must be received before each new step can begin. With some steps, a noticeable delay may be encountered.

Table 4-9. DC Volts Calibration

Command	Response	Action
CAL 1	=>	Puts Hydra in VDC Calibration.
CAL_REF?	+90.000E-3	You output 90 mV dc from the 5700A. Wait about 10 seconds.
CAL_STEP?		Hydra computes calibration constant 1 and returns the calibrated reading (for example, +90.000E-3.)
Note *If the input is incorrect, the "!>" response signifies that a Device Dependent Error was generated. The calibration step could not be executed. Verify that the input to Hydra channel 1 is the correct value and polarity. Also verify that the 5700A is in OPERATE mode. If the input is correct, Hydra may require repair.*		
CAL_REF?	+900.00E-3	You output 900 mV dc from the 5700A. Wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 2 and returns the calibrated reading.
CAL_REF?	+290.00E-3	You output 290 mV dc and wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 3 and returns the calibrated reading.
CAL_REF?	+2.9000E+0	You output 2.9V dc and wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 4 and returns the calibrated reading.
CAL_REF?	+29.000E+0	You output 29V dc and wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 5 and returns the calibrated reading.
CAL_REF?	+290.00E+0	You output 290V dc and wait 4 seconds.
CAL_STEP?		Hydra computes calibration constant 6 returns the calibrated reading. Now change the 5700A output to 0.0V dc

4-27. Ohms Calibration

Resistor values of 290Ω, 2.9 kΩ, 29 kΩ, 290 kΩ, and 2.9 MΩ are preferred. Use either fixed resistors or a decade resistance source having the required accuracy (see Table 4-1.) Connect the channel 11 test leads and the channel 1 test leads to the source resistance. Refer to Figure 4-5 and Table 4-11 for related setup and calibration procedures.

The 5700A can also be used as a resistance source. Connect the 5700A to Hydra for 4-Wire Ohms Calibration. Connect the channel 11 test leads to the 5700A OUTPUT terminals and the channel 1 test leads to the 5700A SENSE terminals. Verify that 5700A EXT SNS is ON. Select the 5700A output as specified in each step. Refer to Figure 4-6 and Table 4-12 for related setup and calibration procedures.

Note

The 300 kΩ, 3 MΩ, and 10 MΩ ranges are sensitive to noise. Any movement of the input leads can cause noisy readings. Use shielded leads and verify these two calibration points at the conclusion of calibration.

Table 4-10. AC Volts Calibration

Command	Response	Action
CAL 2	=>	Puts Hydra in VAC Calibration.
CAL_REF?	+029.00E-3	You output 29 mV ac at 1 kHz from the 5700A. Wait about 8 seconds.
CAL_STEP?		Hydra computes calibration constant 7 and returns the calibrated reading (for example, +029.00E-3.)
Note *If the input is incorrect, the "!>" response signifies that a Device Dependent Error was generated. The calibration step could not be executed. Verify that the input to Hydra channel 1 is the correct value and polarity. Also verify that the 5700A is in OPERATE mode. If the input is correct, Hydra may require repair.*		
CAL_REF?	+290.00E-3	You output 290 mV at 1 kHz from the 5700A. Wait 8 seconds.
CAL_STEP?		Hydra computes calibration constant 8 and returns the calibrated reading.
CAL_REF?	+0.2900E+0	You output 290 mV at 1 kHz from the 5700A and wait 8 seconds.
CAL_STEP?		Hydra computes calibration constant 9 and returns the calibrated reading.
CAL_REF?	+2.9000E+0	You output 2.9V at 1 kHz from the 5700A and wait 8 seconds.
CAL_STEP?		Hydra computes calibration constants 10 and 11 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 10 only.)
CAL_REF?	+29.000E+0	You output 29V at 1 kHz and wait 8 seconds.
CAL_STEP?		Hydra computes calibration constants 12 and 13 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 11 only.)
CAL_REF?	+290.00E+0	You output 290V at 1 kHz and wait 8 seconds.
CAL_STEP?		Hydra computes calibration constant 14 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 12.)

4-28. Reference Junction Calibration

Note

This procedure is necessary only if the Input Module has been repaired or damaged, or if R3 on the Input Module has been inadvertently adjusted.

If thermocouple readings taken in the Thermocouple Temperature Accuracy Test section of the performance tests are found to be out of tolerance, the Input Module Reference Junction may require calibration. First, check the volts dc calibration. If volts dc calibration is correct, perform the following steps:

1. Perform the Volts DC group calibration.
2. Switch OFF power to Hydra, and remove the Input Module from the rear of the instrument.

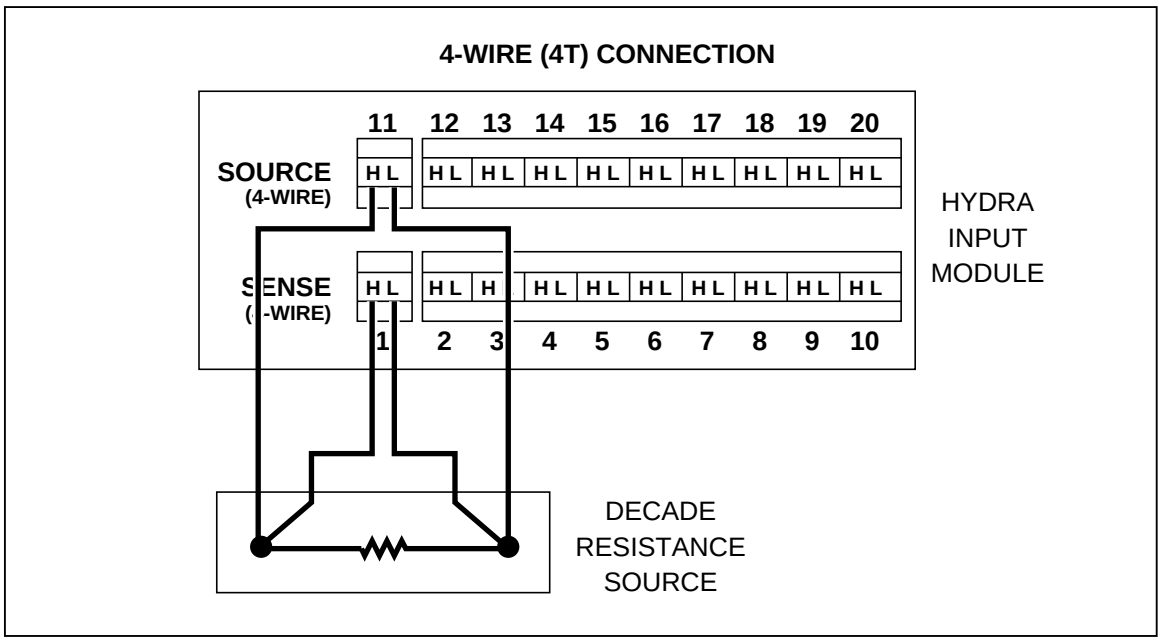


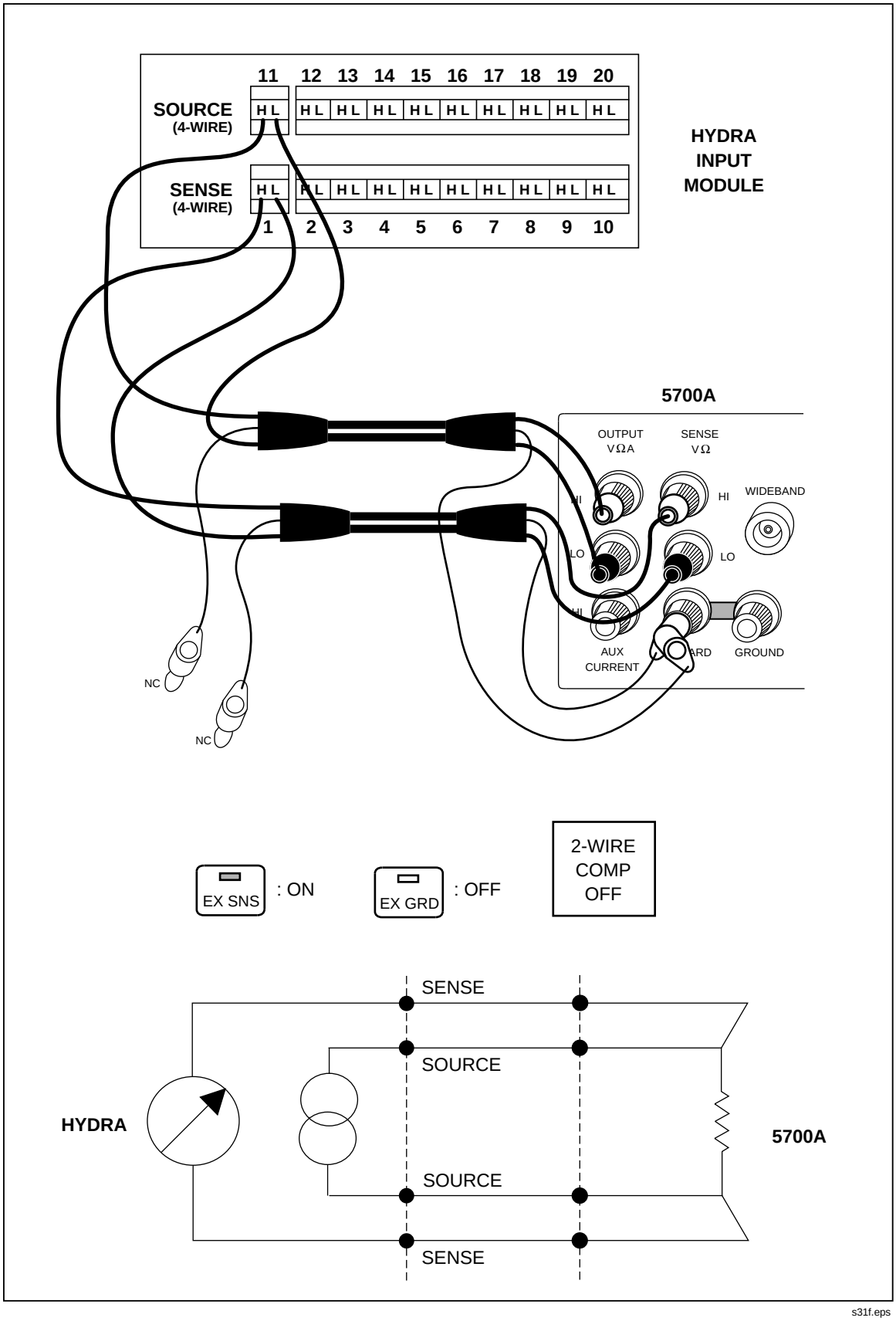
Figure 4-5. 4-Terminal Connections to Decade Resistance Source

3. Remove the module top cover by loosening the two securing screws, fully opening the module top and gently prying either of the hinge ears away from the main body of the module. Refer to Figure 4-1.
4. Connect a KNBS thermocouple to the H (high) and L (low) terminals of channel 15. Refer to Table 4-3 for thermocouple lead colors. Reinstall the module (without the top cover) into the instrument.
5. Press the Hydra POWER button ON.
6. Insert the thermocouple and a mercury thermometer in a stable, thermally-isolated, room-temperature bath. Allow 20 minutes for thermal stabilization.
7. Select the temperature function and K thermocouple type for channel 15. Select the slow measurement rate. Then press MON.
8. Adjust resistor R3 (see Figure 4-1) on the Input Module until Hydra displays the same temperature reading as the mercury thermometer.
9. Calibration of the Input Module is now complete. Remove the Input Module and disconnect the thermocouple. Then attach and secure the module cover.

4-29. Concluding Calibration

At the conclusion of this type of calibration, first make sure the source is cleared. Then press the CAL Enable button on the instrument to exit calibration mode.

Calibration mode can also be exited at any time by sending the *RST Computer Interface command. If this command is sent prior to completion of all calibration points for the selected function, no changes are made to nonvolatile calibration memory for that function.



s31f.eps

Figure 4-6. 4-Terminal Connections to the 5700A

Table 4-11. 4-Wire Ohms Calibration (Fixed Resistor)

Command	Response	Action
CAL 3	=>	Puts Hydra in OHMS Calibration.
CAL_REF?	+290.00E+0	You source 290Ω from the decade resistance source or fixed resistor.
CAL_STEP?		Hydra computes calibration constant 15 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 13.)
Note *If the input is incorrect, the "!>" response signifies that a Device Dependent Error has been generated. The calibration step could not be executed.Verify that the input to Hydra channel 1 is the correct value. If the input is correct, Hydra may require repair.*		
CAL_REF?	+2.9000E+3	You source 2900Ω.
CAL_STEP?		Hydra computes calibration constant 16 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 14.)
CAL_REF?	+29.000E+3	You source 29000Ω.
CAL_STEP?		Hydra computes calibration constant 17 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 15.)
CAL_REF?	+290.00E+3	You source 290000Ω.
CAL_STEP?		Hydra computes calibration constant 18 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 16.)
CAL_REF?	+2.9000E+6	You source 2900000Ω.
CAL_STEP?		Hydra computes calibration constants 19 and 20 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constants 17 and 18.)

4-30. Updating 2635A Data Bucket Embedded Instrument Firmware

The instrument firmware in the 2635A Hydra Data Bucket can be easily updated without even opening the instrument case or replacing any parts. The instrument firmware is stored in electrically eraseable and programmable Flash memory.

A diskette which contains the necessary software and the latest release of 2635A Data Bucket firmware may be obtained from either your local Fluke authorized service center or the Fluke factory. The local service centers are listed in Section 6 of this manual. Contact the one nearest you. To request the "2635A Embedded Firmware Memory Loader" diskette from the factory, telephone or send a fax to:

Fluke Corporation, Data Acquisition Sales Support Telephone: (206) 356-5870 FAX: (206) 356-5790

Table 4-12. 4-Wire Ohms Calibration (5700A)

Command	Action
CAL 3	Puts Hydra in OHMS Calibration
Note *With the following CAL_REF commands, send the actual resistance value (e.g., xxx.xxxxx) displayed by the 5700A.*	
	Source 190Ω from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxx.xxxxx	
CAL_STEP?	Hydra computes calibration constant 15 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 13.)
Note *If the input is incorrect, the "!>" response signifies that a Device Dependent Error has been generated. The calibration step could not be executed.Verify that the input to Hydra channel 1 is the correct value. Also verify that the 5700A is in OPERATE mode. If the input is correct, Hydra may require repair.*	
	Source 1.9 kΩ from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxxx.xxxx	
CAL_STEP?	Hydra computes calibration constant 16 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 14.) Source 19 kΩ from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxxxx.xxx	
CAL_STEP?	Hydra computes calibration constant 17 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 15.) Source 190 kilohms from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxxxxx.xx	
CAL_STEP?	Hydra computes calibration constant 18 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constant 16.) Source 1.9 megohms from the 5700A. Then wait 4 seconds for the 5700A to settle.
CAL_REF xxxxxxx.x	
CAL_STEP?	Hydra computes calibration constants 19 and 20 and returns the calibrated reading. (For software versions lower than 5.4, this step computes calibration constants 17 and 18.) Now set the 5700A output to 0.

4-31. Using the PC Compatible Firmware Loader Software

This procedure uses the 2635A Embedded Firmware Memory Loader Package for closed-case updating of the internal firmware in the 2635A. This software runs on an IBM PC or equivalent using the RS-232 interface. It consists of the following files:

- An executable file (LD2635.EXE)
- A text file containing usage information (README.TXT)
- A 2635A instrument firmware file (DB_6_9.HEX for example)
- A batch file to load the firmware via COM port #1 (LOADC1.BAT)
- A batch file to load the firmware via COM port #2 (LOADC2.BAT)

Firmware downloading may be accomplished by using either of the two methods that are described in the following paragraphs.

- Default Instrument Firmware Download Procedure
- Using LD2635 Firmware Loader Directly

Table 4-13. Frequency Calibration

Command	Response	Action
CAL 4	=>	Put Hydra in Frequency Cal.
CAL_REF?	+10.000E+3	Output 2.9 volts ac at 10 kHz from the 5700A. Wait about 8 seconds.
CAL_STEP?		Hydra computes calibration constant 21 and returns the calibrated reading (for example, +10.000E+3.) (For software versions lower than 5.4, this step computes calibration constant 19.)
Note *If the input is incorrect, the "!>" response signifies that a Device Dependent Error has been generated. The calibration step could not be executed.Verify that the input to Hydra channel 1 is the correct value. Also verify that the 5700A is in OPERATE mode. If the input is correct, Hydra may require repair.*		
		Now set the 5700A output to 0V dc.

4-32. Setup Procedure for Firmware Download

Use the following procedure to set up the 2635A and the PC, before attempting to download firmware to the instrument:

1. Copy the files from the diskette to your PC hard drive. All following PC operations should be done in the directory on the PC where these files are located.
2. Using the RS40 Terminal Interface Cable, connect the PC COM port to be used to the 2635A RS-232 port. Use an RS40 and an RS41 cable in series to connect to the COM port on an IBM PC/AT.
3. On the 2635A, press POWER ON. After the initialization process has concluded, use the following procedure to set up communications:
   a. Press SHIFT and then LIST(COMM).
   b. With 'BAUd' displayed, use the UP or DOWN arrow key to select'19200' baud. Then press ENTER.
   c. With 'PAR' (parity) displayed, use the UP or DOWN arrow key toselect 'no' parity. Then press ENTER.
   d. With 'CtS' displayed, use the UP or DOWN arrow key to selectthe Clear to Send flow control 'On'. Then press ENTER.
   e. With 'ECHO' displayed, use the UP or DOWN arrow key to select'OFF'. Then press ENTER. Communications setup for the 2635A isnow complete.

4-33. Default Instrument Firmware Download Procedure

Use the following procedure to download the version of 2635A instrument firmware that is distributed on the diskette:

1. If it is important to retain the channel programming information in the instrument, store a copy of the instrument configuration setup on a memory card. Refer to section on "Using SETUP STORE" in section 3 of the 2635A Data Bucket Users Manual.
2. To load the instrument firmware, run 'LOADC1.BAT' if COM port #1 is to being used. Otherwise, run 'LOADC2.BAT' if COM port #2 is to being used. These batch files execute 'LD2635' in batch mode with the proper command line switches to download the default instrument firmware via the proper COM port.
3. After successful loading of the instrument firmware, the instrument will be reset to begin normal operation. It is not abnormal to see an "ERROR 6" indication displayed by the instrument as it begins operation again. This just indicates that the internal instrument configuration has been reset to factory defaults. If you saved the instrument configuration during step 1, you can reload it into the instrument now. Refer to section "Using SETUP LOAD" in section 3 of the 2635A Data Bucket Users Manual.

4-34. Using LD2635 Firmware Loader Directly

The 'LD2635' program may be used interactively or in batch mode by using command line switches. The command line syntax is

LD2635 [/B /Cn /Fname]

where the command line switches are defined as follows:

/B Execute in batch mode; program exits when firmware programming is complete. If batch mode is not specified, user is asked whether or not another instrument is to be updated each time an instrument is completed. (/Cn and /Fname switches must be included if batch mode is specified.)

/Cn Use COMM port #n (n = 1 or 2)

/Fname Download named firmware file to the 2635A

For example, to program multiple instruments with version 6.8 of the instrument firmware via COM port #2, execute:

ld2635 /fdb_6_9.hex /c2

or to do the same with only one instrument:

ld2635 /b /fdb_6_9.hex /c2

The 'ld2635' program can be used interactively by running it without any command line switches. It will then request the name of the firmware file and the COM port to be used before going on to update the firmware in the instrument. Since this is not batch mode, the user is asked whether or not another instrument is to be updated each time an instrument is completed.

If any errors are detected in establishing communication with the 2635A or updating the firmware in the instrument, descriptive error messages will be printed to the PC console before the program exits. Make sure that the PC is connected to the 2635A as previously described, and that the 2635A communication parameters have been set correctly.

Chapter 5
Diagnostic Testing and Troubleshooting (2620A/2625A)

Title **Page**

5-1. Introduction

Hydra provides error code information and semi-modular design to aid in troubleshooting. This section explains the error codes and describes procedures needed to isolate a problem to a specific functional area. Finally, troubleshooting hints for each functional area are presented.

But first, if the instrument fails, check the line voltage fuse and replace as needed. If the problem persists, verify that you are operating the instrument correctly by reviewing the operating instructions found in the Hydra Users Manual.

⚠ Warning

Opening the case may expose hazardous voltages.Always disconnect the power cord and measuringinputs before opening the case. And remember thatrepairs or servicing should be performed only byqualified personnel.

Required equipment is listed in Section 4 of this manual.

Signal names followed by a '*' are active (asserted) low. Signal names not so marked are active high.

5-2. Servicing Surface-Mount Assemblies

Hydra incorporates Surface-Mount Technology (SMT) for printed circuit assemblies (pca's). Surface-mount components are much smaller than their predecessors, with leads soldered directly to the surface of a circuit board; no plated through-holes are used. Unique servicing, troubleshooting, and repair techniques are required to support this technology. The information offered in the following paragraphs serves only as an introduction to SMT. It is not recommended that repair be attempted based only on the information presented here. Refer to the Fluke "Surface Mount Device Soldering Kit" for a complete demonstration and discussion of these techniques. (In the USA, call 1-800-526-4731 to order.)

Since sockets are seldom used with SMT, "shotgun" troubleshooting cannot be used; a fault should be isolated to the component level before a part is replaced. Surface-mount assemblies are probed from the component side. The probes should make contact only with the pads in front of the component leads. With the close spacing involved, ordinary test probes can easily short two adjacent pins on an SMT IC.

This Service Manual is a vital source for component locations and values. With limited space on the circuit board, chip component locations are seldom labeled. Figures provided in Section 6 of this manual provide this information. Also, remember that chip components are not individually labeled; keep any new or removed component in a labeled package.

Surface-mount components are removed and replaced by reflowing all the solder connections at the same time. Special considerations are required.

- The solder tool uses regulated hot air to melt the solder; there isno direct contact between the tool and the component.
- Surface-mount assemblies require rework with wire solder rather thanwith solder paste. A 0.025-inch diameter wire solder composed of 63%tin and 37% lead is recommended. A 60/40 solder is also acceptable.

- A good connection with SMT requires only enough solder to make apositive metallic contact. Too much solder causes bridging, while toolittle solder can cause weak or open solder joints. With SMT, theanchoring effect of the through-holes is missing; solder provides theonly means of mechanical fastening. Therefore, the pca must beespecially clean to ensure a strong connection. An oxidized pca padcauses the solder to wick up the component lead, leaving littlesolder on the pad itself.

Refer to the Fluke "Surface Mount Device Soldering Kit" for a complete discussion of these techniques.

5-3. Error Codes

At reset, the Hydra software performs power-up self-tests and initialization of ROM, NVRAM, Display, EEPROM, and measurement hardware. Self-test failures are reported on the display with "Error" in the left display and an error code (1-9,A,b,C) in the right display.

Several of these error codes might never be displayed. Certainly, errors 4 and 5, which signify a faulty or dead display, could not be reported in the normal (displayed) manner. Other errors might not appear on the display. Therefore, the following additional methods exist for accessing error information:

- The computer interfaces can be used to determine self-check statususing the *TST? query. Refer to Section 4 of the Hydra Users Manualfor a description of the *TST? response. Note that the extent of theerror-producing damage could also cause the instrument to halt beforethe computer interfaces are operational.
- The POWERUP? computer interface command can be used to determinewhich errors were detected at power-up. POWERUP? uses the sameresponse format as *TST?; refer to *TST? in Section 4 of the HydraUsers Manual.
- The keyboard scan lines (A1U4, SWR1-5), which are also used as statusindicators, can be checked as a last resort for accessing errorinformation. The software sets SWR1 (A1U4-21) low to indicate thatthe basic operation of the processor, ROM, and ROM decode circuitryis intact. SWR2 (A1U4-22) is set low if the ROM (A1U8) check passes.SWR3 (A1U4-23) is set low if the external NVRAM (A1U3) check passes,and SWR4 (A1U4-24) is set low if the internal RAM (A1U4) checkpasses. Then, if the display self-check passes, SWR5 (A1U4-25) isset low to indicate that the display is operational.

Table 5-1 describes the error codes.

Note

Each error code is displayed for 2 seconds.

Table 5-1. Error Codes

Error	Description
1	ROM (A1U8) checksum error
2	External RAM (A1U3) test failed
3	Internal RAM (A1U4) test failed
4	Display power-up test failure
5	Display not responding
6	Instrument configuration corrupted
7	EEPROM instrument configuration corrupted
8	EEPROM calibration data corrupted
9	A/D not responding
A	A/D ROM test failure (A3U9)
b	A/D RAM test failure (A3U9)
C	A/D self test failure
Refer to Troubleshooting information later in this section.	
Error 1	ROM (A1U8) checksum match failed. All the bytes in the ROM (including a checksum byte) are summed.
Error 2	External RAM (A1U3) check failed.
Error 3	Internal RAM (A1U4) check failed. Complementary patterns are alternately written and read from each RAM location for both external RAM and the 256 bytes internal to the 6303Y Microprocessor (A1U4). If the pattern read from any RAM location is not the same as the pattern written, the test fails.
Error 4	Display self-check failed
Error 5	Display dead. The display processor automatically performs a self-check on power-up, and the Microprocessor attempts to read the result of this test.
Error 6	Instrument configuration The instrument configuration information stored in nonvolatile RAM (A1U3) has been corrupted. (The Cyclic Redundancy Checksum on this memory is not correct for the information stored there.) The instrument configuration is reset to the default configuration.
Error 7	EEPROM instrument configuration corrupted or EEPROM not initialized.
Error 8	EEPROM calibration data corrupted. The EEPROM (A1U1) is divided into two storage areas: the instrument configuration storage and calibration data storage. Each area uses a Cyclic Redundancy Checksum (CRC), against which the data is checked on power-up. • Error 7 is reported if the instrument configuration check finds an error; the instrument configuration is set to factory defaults. • If the calibration data CRC verification indicates that there is calibration data that is in error, the front panel CAL annunciator is turned on, and Error 8 is reported.
Note *Errors 7 and 8 should always appear the first time an instrument is powered up with a new, uninitialized EEPROM.Error 8 continues to appear at subsequent power-ups until the instrument is fully calibrated.*	
Error 9	A/D Microcomputer (A3U9) failed to respond This error is displayed if communication cannot be established with the 6301Y Microcomputer (A3U9).
Error A	A/D ROM test failure All bytes of internal ROM for the 6301Y Microcomputer (A3U9) (including the checksum byte) are summed.

Table 5-1. Error Codes (cont)

Error	Description
Error b	A/D RAM test failure Complementary patterns are alternately written to and read from each location of the 256 bytes of RAM internal to the 6301Y Microcomputer (A3U9).
Error C	A/D self test failed The Analog Measurement Processor (A3U8) is programmed to do self test measurements.

5-4. General Troubleshooting Procedures

Hydra allows for some fault isolation using self-diagnostic routines and descriptive error codes. However, these features are somewhat limited and do not provide in-depth troubleshooting tools.

Hydra incorporates a semi-modular design; determining modules not related to a problem constitutes the first step in the troubleshooting process.

As a first step, remove the IEEE-488 Option (if installed) from the Data Acquisition Unit (2620A) or the Memory PCA from the Data Logger (2625A). Refer to Section 3 of this manual for removal procedures. If removal of either of these assemblies results in improved instrument operation, refer to Section 7 for IEEE-488 Option troubleshooting or later in this section for Memory PCA troubleshooting.

Measuring the power supplies helps to isolate a problem further. Refer to Table 5-2 and Figure 5-1 for test point identification and readings. If power supply loading is suspected, disconnect the Display PCA at A1J2. If this action solves the loading problem, proceed to Display Assembly Troubleshooting elsewhere in this section. Otherwise, refer to Power Supply Troubleshooting.

Table 5-2. Preregulated Power Supplies

PREREGULATED VOLTAGE	MEASUREMENT POINTS	RESULTING SUPPLY
-9.0V	A1CR13-2 to A1TP1	VEE
-30V	A1TP4 to A1TP1	VLOAD
+9.25V	A1CR5 cathode to A1TP30	VDD, VDDR
-8.75V	A1CR7 anode and A1TP30	VSS

If the power supplies appear good, check the E clock signal to determine whether the Main PCA or the Display PCA is causing the problem. A correct display depends on the E clock signal. Missing segments, intensified digits, a strobing display, or a blank display can be caused by a faulty E clock.

Use an oscilloscope to check for the E clock at Microprocessor A1U4, pin 68. Look for a 1.2288-MHz square wave that transitions from 0 to 5V dc (VCC).

- If this signal is present, the Display PCA is probably faulty. Referto Display Assembly Troubleshooting elsewhere in this section.
- If the E clock is something other than a 1.2288-MHz square wave,isolate the digital section of the Main PCA by disconnecting theDisplay PCA at J2. Then check the E clock again, and refer to DigitalTroubleshooting elsewhere in this section for further problemisolation.

Refer to the Schematic Diagrams in Section 8 during the following troubleshooting instructions. Also, these diagrams are useful in troubleshooting circuits not specifically covered here.

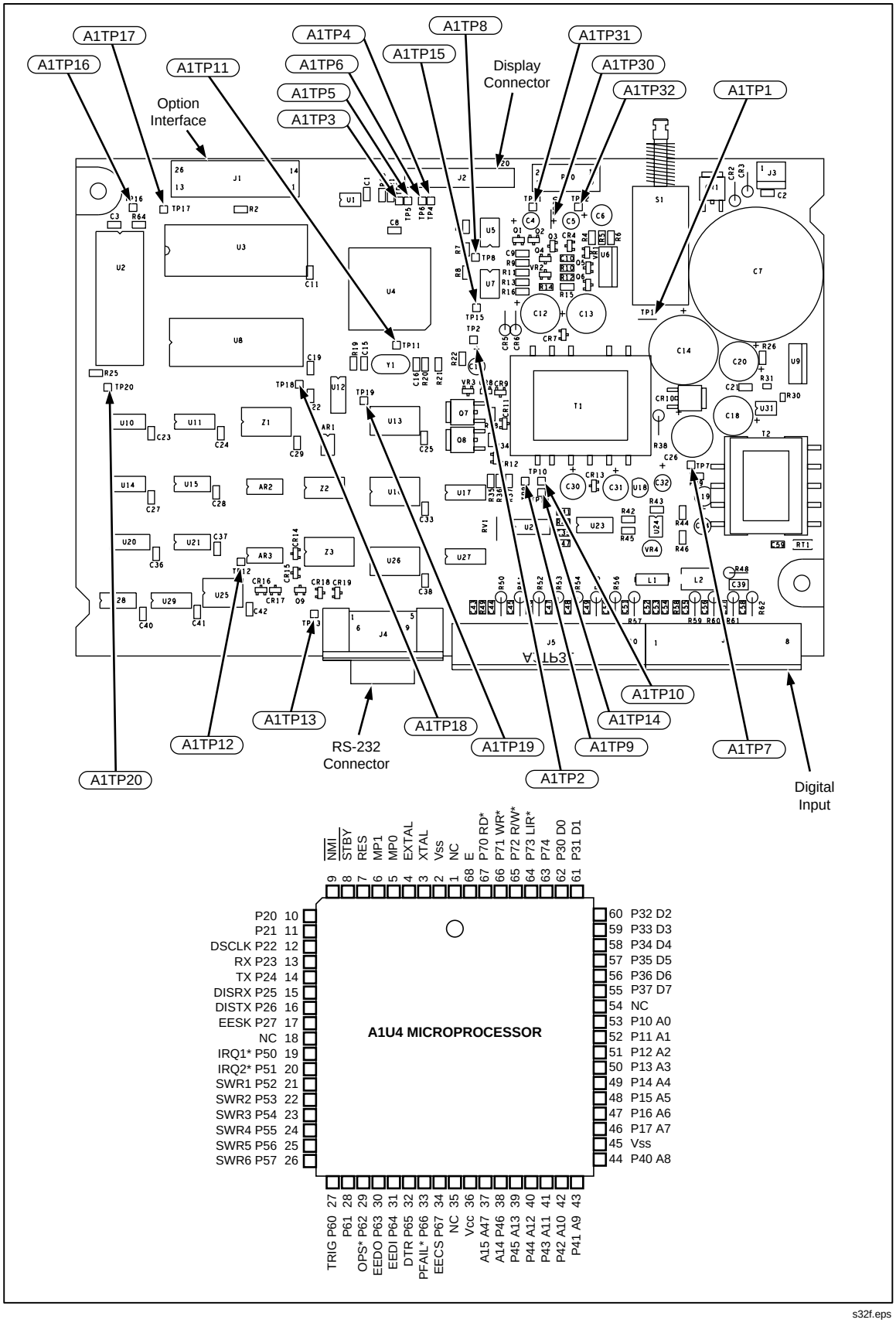


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Figure 5-1. Test Point Locator, Main PCA (A1)

5-5. Power Supply Troubleshooting

⚠ Warning

To avoid electric shock, disconnect all channelinputs from the instrument before performing anytroubleshooting operations.

5-6. Raw DC Supply

With the instrument connected to line power (120V ac, 60 Hz) and turned ON, check for approximately 14V dc between A1TP1 (GND) and the "+" terminal of capacitor A1C7 (or the cathode of either A1CR2 or A1CR3). (This voltage is approximately 30V dc at 240V ac line.) If no voltage or a very low voltage is present, check for approximately 24V ac across the secondary of the power transformer (or approximately 50V ac at 240V ac line.)

The voltage at the output of A1U19 (also A1TP7), should be about +5.2V dc. At 120V ac, 60-Hz line power input, the line current is approximately 29 mA with the IEEE-488 Option installed or 20 mA without the IEEE-488 Option installed. At 50-Hz, 120V ac line power input, there is a 5-10% increase in these two current figures.

5-7. Power Fail Detection

The Power Fail Detection circuit monitors the Raw Supply so that the Microprocessor can be signaled when power is failing. Check for approximately 1.23V dc between the inverting comparator input (A1U24-2) and GND (A1TP1). If the Raw Supply voltage is higher than approximately +8.3V dc, comparator output (A1U24-1) should be near VCC. If the comparator output is near 0V dc during normal operation, the Microprocessor will sense that power is failing and will not be able to complete a scan operation.

5-8. 5-Volt Switching Supply

Use an oscilloscope to troubleshoot the 5-volt switching supply. With the oscilloscope common connected to A1TP1, check the waveform at either A1U9, pin 4 or A1T1, pin 2 to determine the loading on the 5-volt switching supply. The output voltage of the 5-volt switching supply at A1TP2 (VCC) is normally about 5.1V dc with respect to A1TP1 (GND). Note that a fault in the load (high or low resistance) can appear as a faulty output voltage of the 5-volt switching supply.

- Normal Load:

The signal at A1U9-4 (with respect to A1TP1) is a square wave with a period of 9 µs to 11 µs and an ON (voltage is low) duty ratio of about 0.38 with the line voltage at 120V ac. The amplitude is usually about 15V p-p. The positive-going edge will be "fuzzy" as the duty ratio is varying to compensate for the ripple of the raw supply and the pulsing load of the inverter supply. See Figure 5-2A (NORMAL LOAD).

- Very Heavy Load:

Under heavy load (example: A3 A/D Converter PCA has a short circuit) it could load down the power supply voltage such that the current limiting feature is folding the supply back. For example, if the supply is folded back due to excessive current draw, unplug the ribbon cable at A3J10 on the A/D Converter PCA. When tracking down power supply loads, use a sensitive voltmeter and look for resistive drops across filter chokes, low value decoupling resistors, and circuit traces. Also check for devices that are too warm. On the A3 A/D Converter PCA, all devices run cool except A3U5 microprocessor and A3U8 FPGA, which run warm, but not hot.

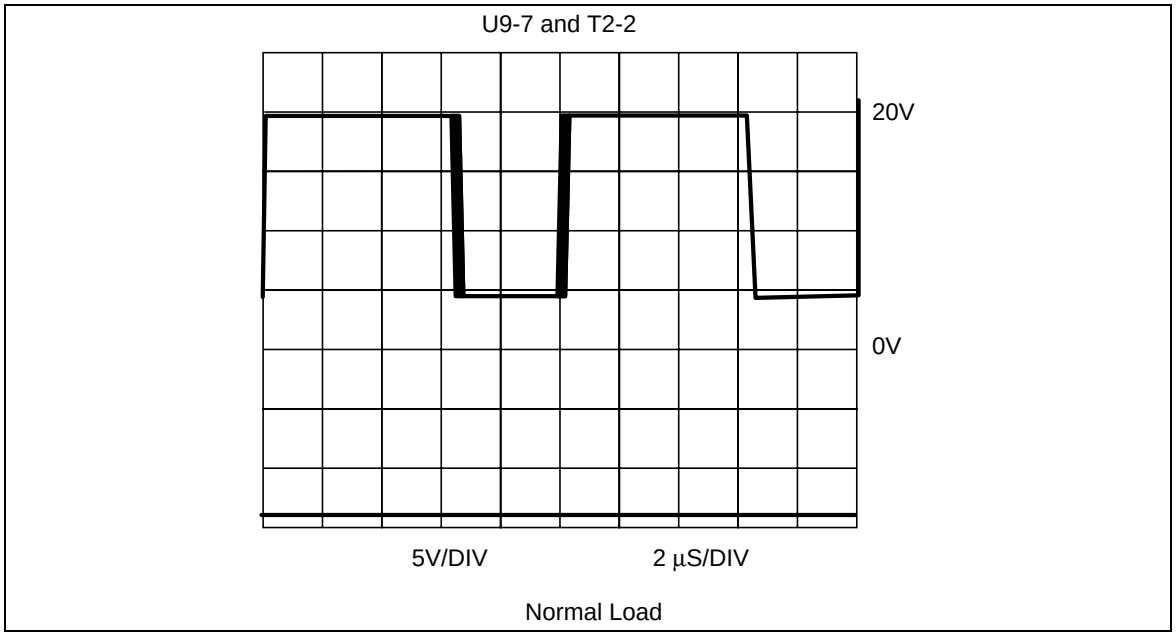


Figure 5-2. 5-Volt Switching Supply

If no square wave is present at A1U9-7, the oscillator can be checked by looking at the signal at A1U9-3. The oscilloscope should be ac-coupled for this measurement. This waveform should be a sawtooth signal with an amplitude of 0.6V p-p and a period of approximately 14 us. Failure of the oscillator is usually caused by a defective capacitor A1C21 or defective A1U9.

The output current of the 5-volt switching supply can be determined by measuring the voltage across the current limit current sense resistors (A1R29, A1R30 and A1R31). The current shunt is approximately 0.167 ohms. With line voltage at 120V ac and the instrument not actively measuring, typical voltages across the current sense resistors are as follows:

- 2620A Instrument without options: 28 mV
- 2620A Instrument with IEEE-488 Option: 50 mV
- 2625A Instrument: 28 mV

5-9. Inverter

Use an oscilloscope to troubleshoot the inverter supply. The outputs of the inverter supply are -5V dc, -30V dc, and 5.4V ac outguard, and +5.3V dc, -5.4V dc, and +5.6V dc inguard. Refer to Figure 5-3. The signal at the drains of the two inverter switch FETs (A1Q7 and A1Q8) should be a 10V peak square wave with a period of approximately 18 us. The gate signal is a 5.1V peak square wave with rounded leading and trailing edges. The leading edge has a small positive rounded pulse with an amplitude of 1.8V peak and a pulse width of about 0.3 µs. The signal at A1U22-5 and A1U22-6 is a symmetrical square wave with an amplitude of 5.1V peak and a period of about 18 µs. The negative-going trailing edge of both square waves is slower than the rising edge and has a small bump at about 1.5 volts. The signal at A1U22-3 (TP14) is a symmetrical square wave with a period of about 9 µs.

For the inverter to operate, the 110-kHz oscillator must be operating properly. If the signal at A1U22-3 is missing, begin by checking the voltage at A1TP7. The voltage should be about 5.1V dc. Then, using an oscilloscope, check for a square wave signal at A1U23-9 and a square wave signal at A1U23-8. If the FETs are getting proper drive signals, failures that heavily load the inverter supply will usually cause the inverter to draw enough current to make the switcher supply go into current limit. Shorted rectifier diodes and shorted electrolytic capacitors will cause heavy load conditions for the inverter.

Note

When making voltage measurements in the invertercircuit, remember that there are two separategrounds. The outguard ground is the 'GND' testpoint (A1TP1), and the inguard ground is the'COM' test point (A1TP30).

The inguard regulator circuits for VDD and VSS have current limits. Shorts and heavy loads between VDD and COM, VSS and COM, and VDD and VSS will cause one or both supplies to go into current limit. The current supplied by either supply can be checked by measuring the voltage across the current sense resistors, A1R13 and A1R15. The typical voltage across A1R13 is 0.30 and the typical voltage across A1R15 is 0.40V.

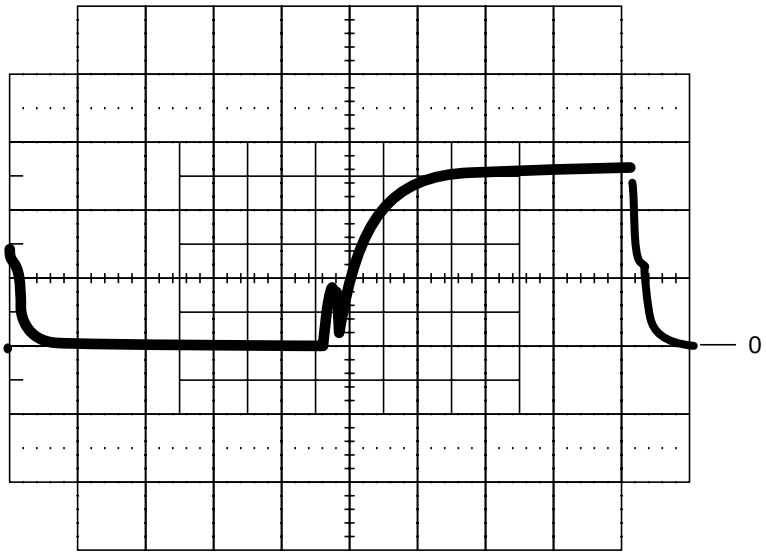
Generally, open electrolytic capacitors in the inverter supply will cause excessive ripple for the affected supply. Also, the rectified dc voltage for the supply with the open capacitor will be lower than normal. Normal voltage levels at the rectifier outputs for each inverter supply are shown in Table 5-2.

The loads for the inguard supplies can be disconnected by removing the cable to the A/D Converter PCA at A3J10. The inguard regulator circuits and VDDR regulator will operate with no loads, and troubleshooting can be performed by making voltage measurements.

The normal input current to the inverter supply is about 11.25 mA, or 0.225 mV across A1R38 (when the instrument is not measuring).

Table 5-3 provides a Power Supply troubleshooting guide.

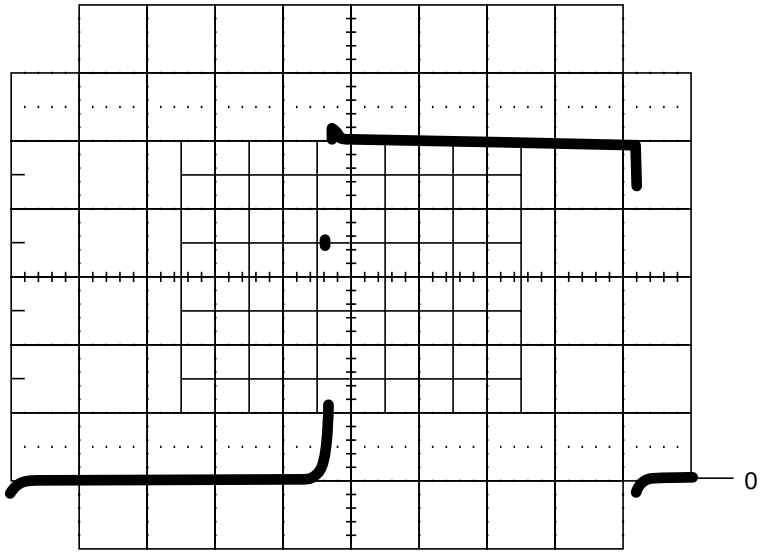
TP9 AND TP10



2V/DIV 2µS/DIV

FET GATE SIGNAL

Q7, Q8, OR T1-1 OR -3



2V/DIV 2µS/DIV

FET DRAIN SIGNAL

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Figure 5-3. Inverter FET Drive Signals

5-10. Analog Troubleshooting

⚠ Warning

To avoid electric shock, disconnect all channelinputs from the instrument before performing anytroubleshooting operations.

Refer to Figure 5-4 and Figure 5-5 for test point locations on the A/D Converter PCA.

First, check for analog-related errors displayed at power up. An 'Error 9' means that the Main Microprocessor A1U4 is not able to communicate with the A/D Microcontroller A3U9. 'Error A' and 'Error b' mean that a failure has occurred in the internal memory of the A/D Microcontroller A3U9. 'Error C' means that the Analog Measurement Processor A3U8 is not functioning properly.

Check the inguard power supplies on the Main PCA with and without the A/D Converter PCA connected. The inguard supplies must be measured with respect to COM testpoint A1TP30.

Power Supply	Test Location	Acceptable Range
VDD	A1TP31	+5.00 to 5.70V dc
VSS	A1TP32	-5.10 to -5.75V dc
VDDR	A1C6	5.30 to 5.95V dc

Check the inguard supply voltages on the A/D Converter PCA with respect to A3TP9. The following table lists the components nearest the power supply test points.

Power Supply	Test Location	Acceptable Range
VDD	A3C8	5.00 to 5.70V dc
VSS	A3C9	-5.10 to -5.75V dc
VDDR	A3C19	5.30 to 5.95V dc
+VAC	A3CR1	4.7 to 5.7V dc
-VAC	A3C26	-4.8 to -5.7V dc

Table 5-3. Power Supply Troubleshooting Guide

Symptom	Fault
Line fuse blows.	- Shorted A1CR2 or A1CR3. - Shorted A1CR10. - Shorted A1C7. - Shorted A1C26.
Supply voltage for A1U23 and A1U22 is greater than 7V (7 to 30V).	Input-to-output short of A1U19. This fault may have caused damage to A1Q7 and A1Q8.
VCC (5.1V) supply is at the raw supply level (7.5 to 35V dc).	Shorted switch transistor in A1U9 (A1U9-5 to 7). Open A1C26 can cause switch transistor to short.
VCC (5.1V) supply shows excessive ripple (about 1V p-p).	A1C14 open.
VCC is below approximately 4.5V. Duty cycle of 5V switcher supply is very low (ON time near 0.1).	Drain-to-source short of A1Q7 or A1Q8.
VCC is about 1.5V. 5V switcher supply is in current limit.	Shorted A1CR5 or A1CR6.
VCC is below approximately 1V. 5V switcher supply is in current limit, with very low duty cycle (ON time near 0.1).	Shorted A1C14.
VCC is below approximately 4.5V. 5V switcher supply is in current limit, with very low duty cycle (ON time near 0.1).	- Q or Q* output of A1U22 stuck high. - A1U23 pin 8 output stuck high or low. - Shorted A1CR7 - Shorted A1CR9 (either diode), pins 1-3 or 2-3. - Shorted A1C30. A1CR13 may also be damaged. - Shorted A1C31. A1CR13 may also be damaged. - Shorted A1C12. - Shorted A1C13. - Shorted A1CR8 (either diode), pins 1-3 or 2-3.
VLOAD (-30V dc) Inverter Supply is at -36V.	Q output of A1U22 stuck low.
VLOAD (-30V dc) Inverter Supply is OFF.	Q* output of A1U22 stuck low.
VLOAD (-30V dc) Inverter Supply ripple.	- Open A1CR8 (either diode). - Open A1CR9 (either diode).
VDD (5.3V dc) supply at approximately 9.2V.	Emitter-to-collector short of A1Q2.
VSS (-5.4V dc) supply at approximately -9.2V.	Emitter-to-collector short of A1Q5.
VDDR (5.6V dc) supply at approximately 10V.	Input-to-output short of A1U6.
VDDR supply has 4-to-5 volt spikes when the A/D relays are switched (set or reset).	Open A1C12.
VEE (-5V dc) supply is low (near zero).	- Open A1C30. - A1CR13 open.
A1CR13, Diode 1-3 shorted or open.	A1C30 may be shorted.
VEE supply is high (near -9V).	Input-to-Output short of A1U18.
A1U18 input has large square wave component.	Open A1C31.

Table 5-3. Power Supply Troubleshooting Guide (cont)

Symptom	Fault
A1U18 hot.	Shorted A1C32
A1U18 oscillates.	Open A1C32.
A1U19 oscillates.	Open A1C34.
A1U19 very hot.	- Shorted A1U22 (VCC to VSS). - Shorted A1U23 (VCC to VSS).
A1U19 hot.	Shorted A1C34.

Check that the inguard Microcontroller A3U9 RESET* line is de-asserted. Check VDD at A3TP1, referenced to A3TP9.

Check that the microcontroller crystal oscillator is running. When measured with a high input impedance oscilloscope or timer/counter, the oscillator output at A3TP10 should be a 3.6864-MHz sine wave (271.3 ns period), and the divided-down E clock output at A3U9 pin 68 should be a 921.6 kHz-square wave (1.085 µs period).

Check outguard to inguard communication. Setup an input channel and enable monitor measurements on that channel, causing the outguard to transmit to the inguard approximately every 10 seconds.

On the Main PCA, look for outguard-to-inguard communication (5.1V (VCC) to near 0V pulses) at A1TP15, referenced to A1TP1. On the A/D Converter PCA, check for 5.35V (VDD) to near 0V pulses at A3TP8, referenced to A3TP9.

At the start of outguard-to-inguard communication, the A/D Microcontroller (A3U9) should be RESET. Check for this reset pulse (5.35V (VDD) to near 0V, lasting approximately 1-ms) on A3TP1 with respect to A3TP9.

Check for the following inguard-to-outguard communication activity:

PCA	Test Point	To	Pulses
A/D Converter	A3TP7	A3TP9	5.55V (VDDR) to 0.7V
Main	A1TP8	A1TP1	0V dc to 5.1V (VCC)

Lack of outguard-to-inguard communication activity may be due to improper operation of circuit elements other than A3U9. Using a high input impedance oscilloscope or timer/counter, check for proper Analog Processor (A3U8) crystal oscillator operation. A 3.84-MHz sine wave (260 ns period) should be present at A3U8 pin 37 with respect to A3TP9.

Check the A/D Converter voltage reference:

A3TP12 to A3TP11 (across A3C12) = +1.05V (+0.10V, -0.02V)

Setup the instrument to measure ohms on the 300Ω range. Monitor ohms on a channel with an input of approximately 270Ω. Check that the Analog Processor IC (A3U8) is making A/D conversions. The integrator output waveform at A3TP13 (referenced to A3TP9) should resemble the waveform shown in Figure 5-6.

Check for channel relay operation by setting up a channel and selecting and de-selecting monitor measurement mode. One or more relays should click each time the monitor button is pressed or channels are changed.

In general, check that the relays are getting the proper drive pulse signals for specific functions and channels and that they are in the correct position.

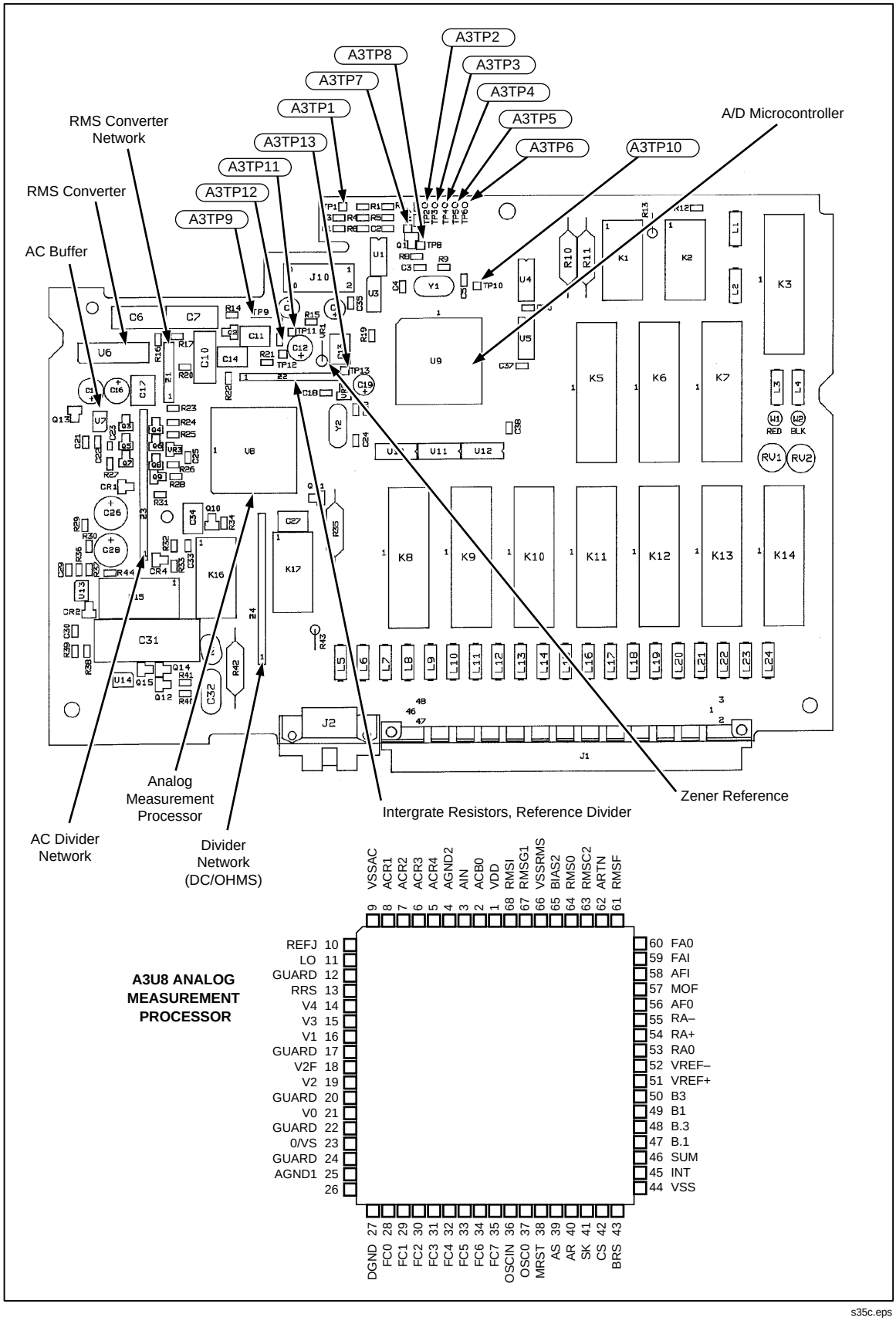

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Figure 5-4. Test Points, A/D Converter PCA (A3, A3U9)

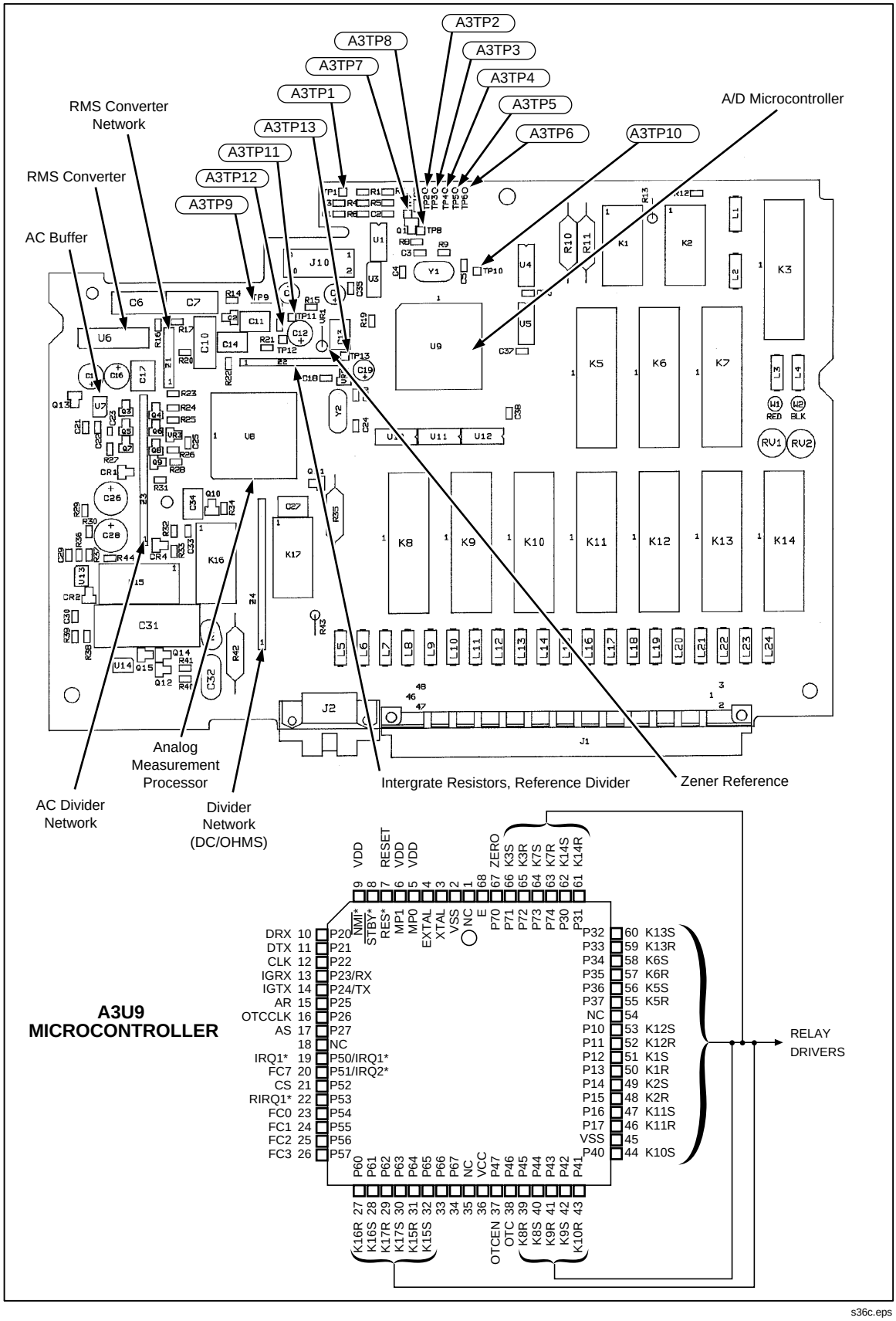

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Figure 5-5. Test Points, A/D Converter PCA (A3, A3U9)

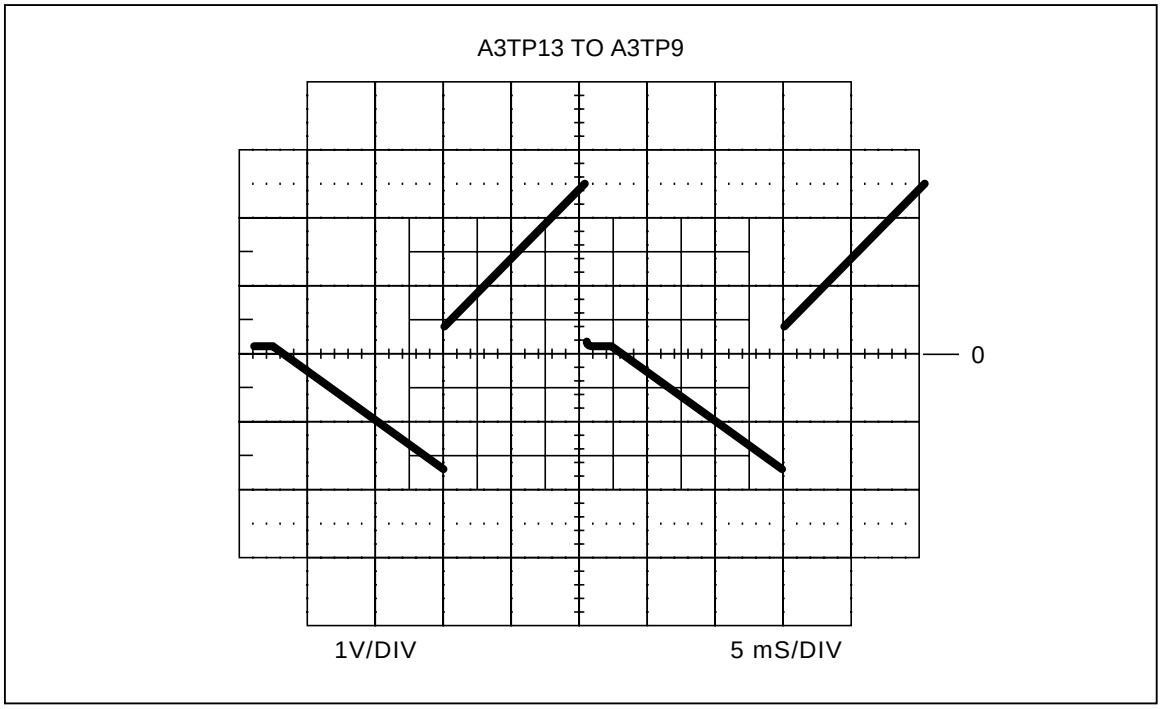


Figure 5-6. Integrator Output

5-11. DC Volts Troubleshooting

Setup the instrument to measure a specific channel on the 300 mV or 3V range, and apply an input to that channel. Then trace the HI signal (referenced to the input channel LO terminal) as described in Table 5-4.

If the input HI path traces out properly, remove the input from the channel and trace continuity through the LO path. Check among A3L4-A3L24, A3K1-A3K14, A3R35, A3R43, and A3U8 pin 11.

Table 5-4. DC Volts HI Troubleshooting

Checkpoint	Signal Description	Possible Fault
A3R11 HI	Input	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12, A3L1, A3L2, A3L3
A3U8 pin 23	Input	A3R11, A3K17, A3R42, A3C32
A3U8 pin 58	Input, DC filter output	A3U8, A3Q2

5-12. AC Volts Troubleshooting

Setup the instrument to measure a channel on the 300 mV ac range, and apply a signal to that channel. Then trace this HI signal (referenced to the input channel LO terminal) as described in Table 5-5.

If the input HI path traces out properly, remove the input from the channel, and trace continuity through the LO path. Check among A3L4 through A3L24, A3K1 through A3K14, A3R43, A3R34, A3K16, and A3U8 pin 13.

Table 5-5. AC Volts HI Troubleshooting

Checkpoint	Signal Description	Possible Fault
A3R11 HI	Input	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12 A3L1, A3L2, A3L3
A3Z3 pin 1	Input	A3R11, A3C31, A3K15
A3U6 pin 13	Amplified (X 2.5) input	A3U7, A3Z3, A3Q3 through A3Q9, A3C15, A3C16, A3R24, A3A25, A3R26, A3R27, A3R28, A3C23, A3U6, A3Q13, A3U8
A3Z1 pin 2	DC equivalent of original input	A3Z1, A3U8, A3R20, A3C6, A3C7, A3C10, A3R16, A3R17
A3U8 pin 61	DC equivalent of original input	A3Z1, A3U8, A3R20, A3C6, A3C7, A3C10, A3R16, A3R17

5-13. Ohms Troubleshooting

Setup a channel with an open input for the desired ohms range and place the instrument in monitor mode on that channel. Use a meter with high input impedance to measure the open-circuit voltage at the channel input for the ohms range as listed in Table 5-6. If a high input impedance meter is not available, only the 30-kΩ and lower ranges can be checked.

Table 5-6. Ohms Open-Circuit Voltage

Range	Voltage
300Ω	3V
3 kΩ	1.3V
30 kΩ	1.3V
300 kΩ	3V
3 MΩ	3V
10 MΩ	3V

If the proper voltage is not measured, setup a channel on the 300Ω range (open input), and have the instrument monitor that channel. Check for 3V dc with respect to A3TP9, and work through the HI SOURCE and HI SENSE paths as described in Table 5-7.

If the HI path works correctly, trace continuity through the LO path. Check among A3L4 through A3L24, A3K1 through A3K14, A3R35, A3U8 pin 11, A3R43, A3K16, A3R34, and A3U8 pin 13.

Table 5-7. Ohms HI Troubleshooting

Checkpoint	Signal Description	Possible Fault
A3U8 pin 14	Ohms Source	A3U8
A3R10 HI SRC	Ohms Source	A3R10, A3K16, A3RT1, A3Z4, A3Q10
Channel HI	Ohms Source	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12, A3L1, A3L2, A3L3
A3U8 pin 23	Ohms Source	A3R11, A3K17, A3R42, A3C32
A3U8 pin 58	Ohms Source filter output	A3U8, A3Q2

5-14. Digital Kernel Troubleshooting

At power-up, if the display does not light or lights up and fails to report errors or begin operation, use the following troubleshooting procedures.

First check the state of SWR1 (A1U4-21). If this status line is less than 0.8V, basic processor operation is intact. Examining SWR2 through SWR5 (A1U4-22 through -25, respectively) should indicate how far the software progressed before finding an error. If the state of SWR1 is not less than 0.8V, the problem may be in the 6303Y Microprocessor (A1U4), the ROM or NVRAM decode circuitry (A1U10 and A1U21), the ROM (A1U8) or NVRAM (A1U3), or the address/data lines among these parts.

Note

The functions of SWR1 through SWR5 as power-upstatus lines persist for only 3 to 4 seconds. Thesefunctions end when the keyboard scanner beginsoperation (if it can). Extremely difficult casesmay require the use of an oscilloscope triggered onthe falling edge of SWR1 to examine the states ofSWR2 through SWR5.

To determine the relative health of the 6303Y Microprocessor (A1U4), first check for a valid E clock at pin 68. The default for the E clock after reset is a rectangular wave with a period of 1.221 µs and a duty cycle of about 67%.

If the processor is able to fetch instructions from the ROM, the software initializes the processor, and the E clock becomes a square wave with a period of 0.814 us. Since this initialization occurs almost immediately with a working instrument, the resulting square wave on the E clock line is a good indication that the software has begun to execute.

If the E clock remains a 1.221 µs rectangular wave, the SWR2 (A1U4-22) keyboard scan line might be shorted to ground. This condition would cause the Microprocessor to HALT after reset. Check whether the 6303Y Microprocessor is attempting to access ROM; LIR* (A1U4-64) should transition for a short period of time after reset. If it does, the 6303Y Microprocessor is probably operational, and the problem is external to the processor.

The processor can execute an instruction that stops both itself and the E clock. Therefore, the absence of any activity on pin 68 does not necessarily mean that A1U4 or A1Y1 is bad. If some other failure prevents proper ROM access, the processor may have just "gone to sleep". This can be verified by checking for a rectangular wave occurring at pin 68 for a short time after RESET* transitions high on pin 7. A1U4 and A1Y1 are probably operational if this rectangular wave is at least momentarily present.

To check the ROM decode circuitry, verify that A1U10-6 is transitioning low and that these transitions correspond roughly to the low-going transitions of LIR*. Pin 6 must be low when LIR* is low. Verify that this signal also appears at the ROM Chip Enable, A1U8-20. If the ROM Chip Enable is present, the problem is with the ROM itself or there is a fault in the address/data lines among the 6303Y Microprocessor, ROM, NVRAM, and Option Connector.

If SWR1 (A1U4-21) and SWR2 (A1U4-22) transition low, but SWR3 (A1U4-23) remains high, the problem is with the NVRAM decode circuitry (A1U15, A1U21), the external NVRAM (A1U3), or the address/data/control lines between the NVRAM and the 6303Y Microprocessor.

To check the NVRAM decode circuitry, verify that A1U21-6 is transitioning low and that these transitions correspond approximately to the low-going transitions of WR* (A1U4-66). It may be necessary to continually reset (power on) the instrument to check these lines, since the activity probably halts quickly when the instrument software goes awry. Verify that the signal on A1U21-6 also appears at the NVRAM Chip Enable, A1U3-20. If the NVRAM Chip Enable is present, the problem is with either the NVRAM itself or the address, data, RD*, or WR* lines between the 6303Y Microprocessor and the external NVRAM.

Figure 5-7 shows the timing relationships of the 6303Y Microprocessor lines LIR* and WR* to the system clock (E) and the address lines A0..A15. The ROM and NVRAM Chip Enables correspond to the active (low) region shown for the address lines.

If the instrument powers up without any errors, but does not recognize front-panel button presses or computer interface commands, the problem may be in the Counter/Timer (A1U2). Normally, this component generates a regular 50-millisecond interrupt at the IRQ* output (A1U2-9). If this output is low (and never goes high), the Microprocessor (A1U4) is failing to recognize the interrupt or the microprocessor interface to A1U2 is not working correctly. Also check output A1U2-6 for a 10-Hz square wave. If this output is not correct, check for the E clock at A1U2-17, and verify the microprocessor interface signals (CNTR*, D0 .. D7, A0 .. A2, R/W*, and RESET*.)

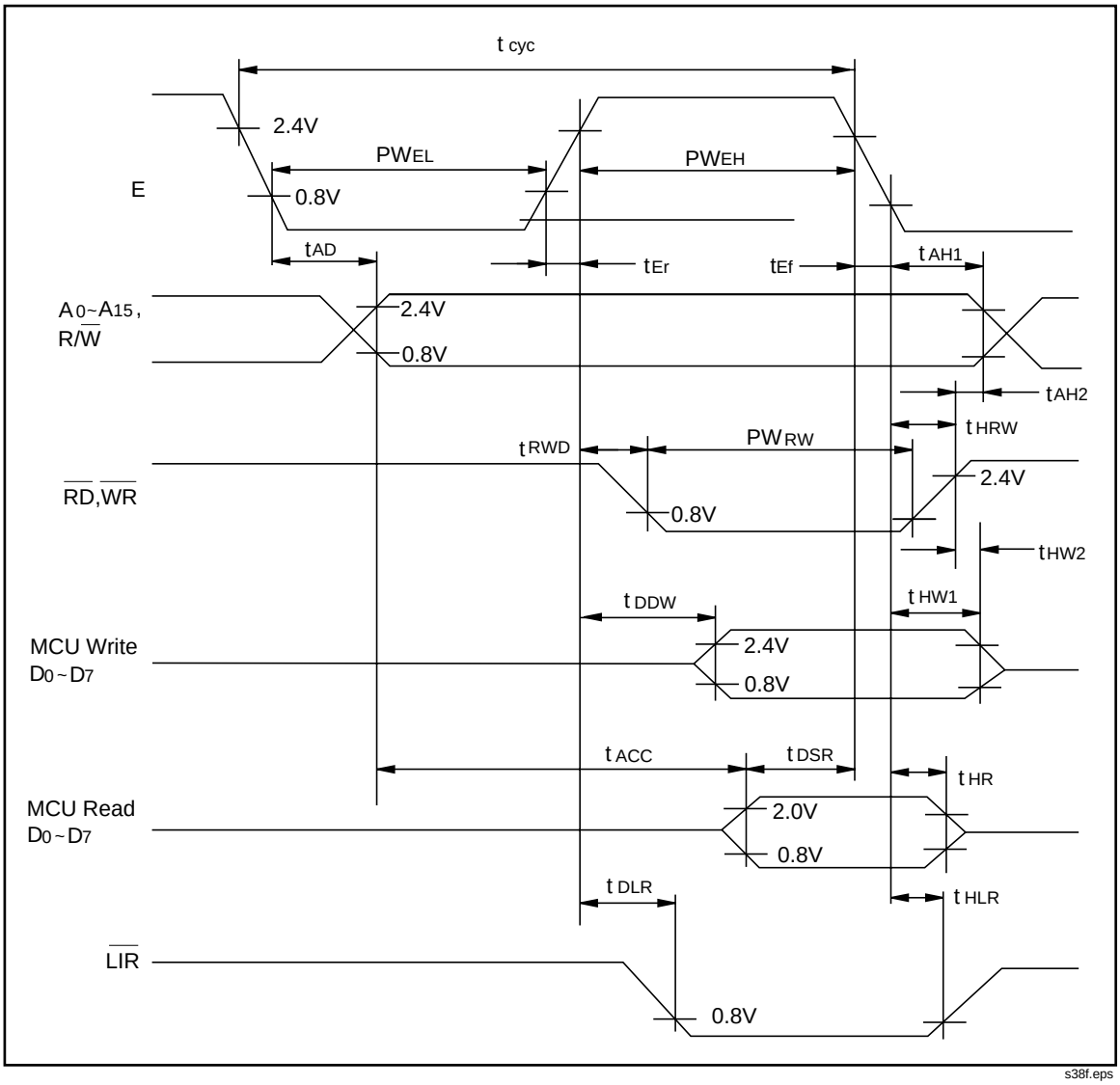


Figure 5-7. Microprocessor Timing

5-15. Digital and Alarm Output Troubleshooting

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Since the structure of the eight Digital Outputs and four Alarm Outputs is very similar, the troubleshooting procedure presented here does not refer to specific device and pin numbers. First verify that the input of the Output Driver (A1U17 or A1U27) is low and that the output is near +5V dc. If the input is high, the problem may be in the address decoding (A1U12 and A1U15) or the associated octal D-type flip-flop (A1U16 or A1U26). If the output is not near +5V dc, use an ohmmeter to check the pull-up resistor in A1Z2.

Use the proper computer interface command to change the state of the Digital Output (DO_LEVEL x,1) or Alarm Output (ALARM_DO_LEVEL x,1), where x is the number of the output being checked. Now verify that the input of the Output Driver is high and that the output is near +0.8V dc. If there is no change in the input, check the address decoding and operation of the associated octal D-type flip-flop (A1U16 or A1U26.) If the output failed to change, the problem is most likely the inverting output driver (A1U17 or A1U27).

5-16. Digital Input Troubleshooting

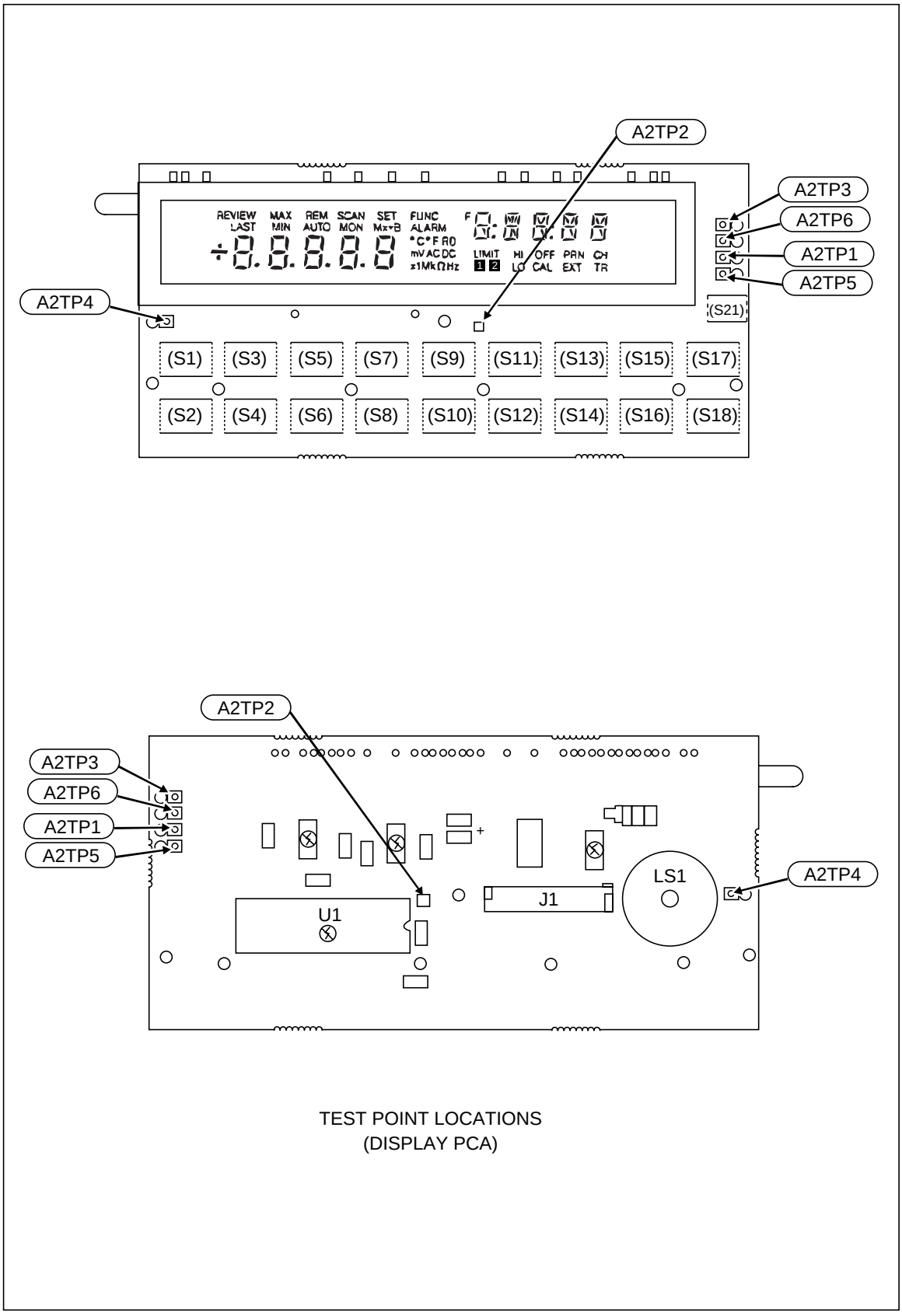
Power up Hydra while holding down the CANCL button to reset the instrument configuration. Verify that the Input Buffer Threshold circuit generates approximately 1.4V dc at A1TP18. Drive the Digital Input (A1J5) to be checked with a signal generator outputting a 100-Hz square wave that transitions from 0 to +5V dc. The signal generator output common should be connected to Common (A1J5-1). Verify that the output of the Input Buffer is a 100 Hz square wave that is the inverse of the input signal.

If the Input Buffer does not function correctly, the problem is probably A1Z1, A1Z3, or the associated comparator (A1AR2 or A1AR3). If the Input Buffer functions correctly, but Hydra is not able to read the state of the Digital Input correctly, the problem is most likely the tri-state buffer A1U13. If Hydra is not able to read the states of any of the eight Digital Inputs correctly, the problem is most likely the address decoding (A1U10 and A1U12) for the tri-state buffer.

5-17. Totalizer Troubleshooting

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Verify that the Input Buffer Threshold circuit generates approximately 1.4V dc at A1TP18. Drive the Totalizer Input (A1J5-2) with a signal generator outputting a 100-Hz square wave that transitions from 0 to +5V dc. The signal generator output common should be connected to Common (A1J5-1). Verify that the output of the Input Buffer (A1AR1-7) is a 100-Hz square wave that is the inverse of the input signal. Verify also that the input to the totalizer counter (A1TP20) is a buffered form of the signal just verified at the output of the Input Buffer.

Use the following procedure to troubleshoot the totalizer input debouncer, Enable the totalizer debouncer by sending the TOTAL_DBNC 1 Computer Interface command to the instrument; verify that A1U16-16 is now high. With the signal generator still connected and outputting a 100-Hz square wave, verify that A1U14 drives the clear input of the counter (A1U20-11) low for 1.67 milliseconds after each edge of the input signal. Verify that counter output A1U20-13 generates a 4.8-kHz clock while A1U20-11 is low. Verify that the shift register output (A1U29-9) changes to the same state as the totalizer input signal about 1.67 milliseconds after a transition occurs on the totalizer input signal (A1U29-10).



TEST POINT LOCATIONS
(DISPLAY PCA)

s39f.eps

Figure 5-8. Test Points, Display PCA (A2)

5-18. Display Assembly Troubleshooting

The following discussion is helpful if it has been determined that the Display Assembly is faulty. Refer to Figure 5-8 for Display PCA test points. This initial determination may not be arrived at easily, since an improperly operating display may be the result of a hardware or software problem that is not a direct functional part of the Display Assembly. Consult the General Troubleshooting Procedures found earlier in this section for procedures to isolate the fault to the Display Assembly. Use the following discussion of display software operation when troubleshooting problems within a known faulty Display Assembly. A Display Extender Cable (PN 867952) is available for use during troubleshooting. Note that this cable must be twisted to mate correctly to the connectors on Display and Main PCAs.

The Display Controller reads the DTEST* and LTE* inputs to determine how to initialize the display memory. DTEST* and LTE* default to logic 1 and logic 0, respectively, to cause all display segments to be initialized to "on". DTEST* is connected to test points A2TP4, and LTE* is connected to A2TP5. Either test point can be jumpered to VCC (A2TP6) or GND (A2TP3) to select other display initialization patterns. Display Test Patterns #1 and #2 are a mixture of "on" and "off" segments with a recognizable pattern to aid in troubleshooting problems involving individual display segments. When either of the special display patterns is selected, the beeper is also sounded for testing without interaction with the Microprocessor. Table 5-8 indicates the display initialization possibilities.

Table 5-8. Display Initialization

A2TP4 DTEST*	A2TP5 LTE*	POWER-UP DISPLAY INITIALIZATION
1	1	All Segments OFF
1	0	All Segments ON (default)
0	1	Display Test Pattern #1
0	0	Display Test Pattern #2

Figure 5-9 shows the timing of communications between the Microprocessor and the Display Controller. Figures 5-10 and 5-11 show Display Test Patterns #1 and #2, respectively. Refer to the Display Assembly schematic diagram in Section 8 for information on grid and anode assignments.

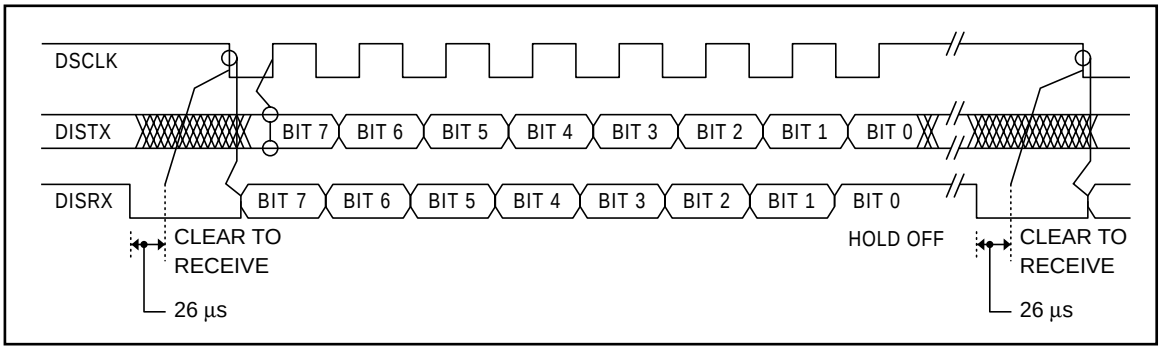
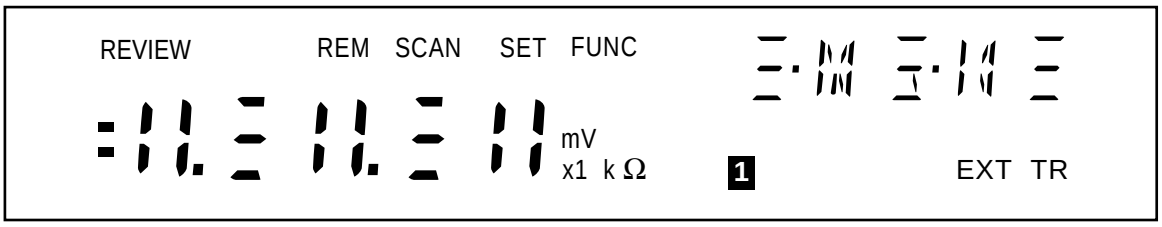
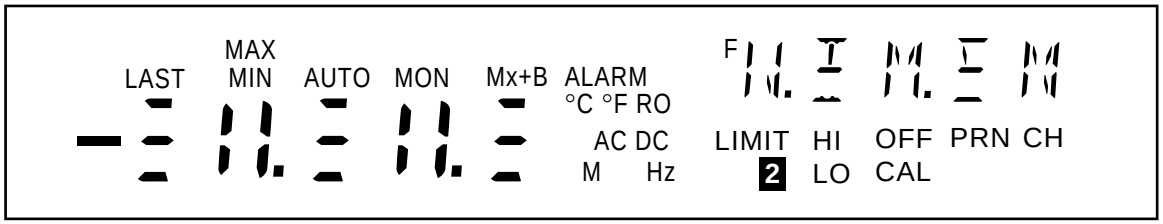


Figure 5-9. Display Controller to Microprocessor Signals



s41f.eps

Figure 5-10. Display Test Pattern #1



s42f.eps

Figure 5-11. Display Test Pattern #2

When a Hydra display is initially powered up, all display segments should come on automatically. If this display does not appear, proceed with the following steps:

Note

If the display is operational but has problems whenfront-panel buttons are pressed, proceed directlyto step 9.

1. Check the three power supplies with respect to GND (A2TP3 or A2U1-42) on the Display Assembly.
   - VCC (A2U1-21) 4.85 to 5.35V dc
   - VEE (A2U1-4)-4.75 to -5.25V dc
   - VLOAD (A2U1-5)-28.5 to -32.0V dc
2. Check the filament drive signals FIL1 and FIL2; these connect to the last two pins on each end of A2DS1. These signals should be 5.4V ac with FIL2 biased to be about 6.8V dc higher than the VLOAD supply (nominally a -23.2V dc level). FIL1 and FIL2 should be 180 degrees out of phase. If the dc bias of FIL2 is not at about -23.2V dc, the display segments that should be "off" will show a shadowing (or speckling) effect.

Note

It may be necessary to disable the watchdog resetby jumpering A2TP1 (A2U5-3, A2U5-11) to GND (A2TP3) toverify the following items.

3. Check the clock signal CLK1 at A2TP2, A2U1-2, and A2U4-3. This signal should be a 614.4-kHz square wave (1.628 ms per cycle). This signal depends on an E clock signal of 1.2288 MHz from the Hydra Main Assembly. If the E clock is 819.2 kHz (1.221 ms per cycle), it is possible that SWR2 (A2J1-16) is shorted to ground, causing the Microprocessor to HALT at power-up.
4. Check the state of the RESET signal (A2U1-1). This signal should be low once the reset time is completed (after power-up). Also verify that the RESET* signal (A2U6-3) is high after the reset time is completed.

5. Verify that the DISRX signal (A2U1-39) goes low after RESET (A2U1-1) goes low. If this sequence does not occur, communication to the Microprocessor is held off with the DISRX signal high. If DISRX stays high but is not shorted to VCC, A2U1 must be faulty.
6. Verify activity for both the DISTX and DSCLK signals. These signals are driven by the Microprocessor and must be transitioning for the Display Controller to receive commands from the Microprocessor.
7. If all segments of a particular digit do not turn on at power-up, the grid drive from A2U1 may not be connected properly to A2DS1. Grids are numbered from 10 to 0 (left to right as the display is viewed). For a digit to be enabled, the respective grid drive signals (GRID(10:0)) must be at approximately VCC (4.85 to 5.35V dc.) For a digit to be disabled, the drive must be at VLOAD (-28.5 to -32.0V dc.)
8. If a segment under each of several (or all) grids fails to be turned on (or off) properly, one of the anode drive signals may not be connected properly from A2U1 to A2DS1. When an anode signal is at VCC, and a grid signal is at VCC, the corresponding segment on the display is illuminated.
9. If the Microprocessor has difficulty recognizing front-panel button presses, the switch scanning signals (SWR1 through SWR6, A1U4-21 through -26, respectively) should be checked. When no switch contacts are being closed, the switch scanning lines should have about 20 kΩ of resistance between each other (through two 10-kΩ pullup resistors to VCC). Unless one of the switches is closed, none of the switch scanning lines should be shorted directly to GND at any time.

5-19. Variations in the Display

Note

The following procedure will not work with Hydra's Mainframe Firmware version 5.5.

Under normal operation, the display presents various combinations of brightly and dimly lit annunciators and digits. However, you may encounter other, random irregularities across different areas of the display under the following circumstances:

- After prolonged periods of displaying the same information.
- If the display has not been used for a prolonged period.

This phenomenon can be cleared by activating the entire display and leaving it on overnight (or at least for several hours). Use the following procedure to keep the display fully lit:

1. With power OFF, press and hold SHIFT, then press power ON.
2. Wait a moment for the instrument to beep, then release SHIFT. The entire display will now stay on until you are ready to deactivate it.
3. At the end of the activation period, press any button on the front panel; the instrument resumes the mode in effect prior to the power interruption (Active or Inactive.)

5-20. Calibration Failures

5-21. Introduction

Calibration of Hydra through the computer interface is described in Section 4 of this manual. Generally, a calibration failure is indicated by a Device Dependent Error and a "!>" prompt after a CAL_STEP? command if the RS-232 interface is being used. If the IEEE-488 interface is being used, the Device Dependent Error may be detected by reading the Event Status Register (see the Hydra User Manual). These indications occur if the analog input varies from what the instrument expects to see by more than ±5% or ±15%, depending on the calibration step.

Before suspecting a fault with Hydra, verify that the calibration is being conducted properly.

- Check the connections between the source and the instrument. Are allthe connections in place?
- Check the output of the calibration source. Does it equal the valuecalled for by this calibration step?
- Check the calibration source. Is it in operate mode? Has it revertedto standby?

If a calibration step has failed, Hydra remains on that step so that the output from the calibration source may be corrected or the calibration reference value (CAL_REF) being used by Hydra may be changed if it was improperly entered. The calibration step may be repeated by sending the CAL_STEP? command to Hydra again.

Calibration of Hydra utilizes a simple "calibration by function" approach. If you suspect calibration errors, but the instrument does not exhibit the symptoms mentioned above, verify that you are observing the following calibration rules:

- Independent calibration of any function results in the storage ofcalibration constants for that function only.
- Once calibration is begun, all steps for that function must becompleted before the calibration constants are stored. If all stepsare not completed and the procedure is terminated, no constants forthat function are stored; only calibration constants for previouslycompleted functions are stored.

5-22. Calibration-Related Components

If the calibration setup is correct, a faulty component within Hydra may be causing the failure. Each measurement function depends on a combination of components in and around the Analog Measurement Processor (A3U8).

RMS Converter	A3U6
AC Buffer	A3U7
Zener Reference	A3VR1
Divider Network (DC/Ohms)	A3Z4
Integrate Resistors, Reference Divider	A3Z2
AC Divider Network	A3Z3
RMS Converter Network	A3Z1

Basic dc measurements depend on the zener reference (A3VR1), reference divider network (A3Z2), and integrate resistors (A3Z2). Resistance measurements and dc measurements above three volts additionally depend on the resistors in the dc divider network (A3Z4). AC measurements depend on the ac divider network (A3Z3), ac buffer (A3U7), and RMS converter (A3U6), as well as the basic dc measurement components.

Note

During calibration, the measurement rateis selected automatically as required by thecalibration step.

Table 5-9 or Table 5-10 may be useful in isolating a calibration problem to specific components. Table 5-9 can be used with a Hydra having a main software version number of 5.4 or higher. Table 5-10 can be used with main software versions lower than 5.4. Note that the software version number is not marked on the Hydra case. Use either of the following two methods to determine your software version number:

- From the Hydra front panel, simultaneously press [ltb] and [rtb]. Themain software version number (e.g., "5.4") appears in the leftdisplay. (The A/D software version number (e.g., A4.7 appears in theright display.) Press [cnc] to return to normal front paneloperation.
- Over the computer interface, send the *IDN? query. The main softwareversion (e.g., "M5.4") is returned as part of the response. Refer toSection 4 of the Hydra Users Manual for a more detailed descriptionof *IDN?.

Table 5-9. Calibration Faults (for software versions 5.4 and above)

Input	Range	Calibration Constant		Related Components
		Number	Acceptable Values	
DC Volts				
0.09000V	100 mV	1	1.0315 to 1.1565	A3VR1, A3Z2
0.9000V	1V	2	1.0340 to 1.1540	A3VR1, A3Z2
0.29000V	300 mV	3	1.0315 to 1.1565	A3VR1, A3Z2
2.9000V	3V	4	1.0315 to 1.1565	A3VR1, A3Z2
29.000V	30V	5	1.0340 to 1.1640	A3VR1, A3Z2, A3Z4
290.00V	300V	6	1.0290 to 1.1590	A3VR1, A3Z2, A3Z4
AC Volts (1 kHz)				
0.02900V	300 mV	7	-0.001 to 0.001	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.29000V	300 mV	8	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.2900V	3V	9	-0.01 to 0.01	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.9000V	3V	10	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.900V	30V	11	-0.1 to 0.1	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.000V	30V	12	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.00V	300V	13	-1.0 to 1.0	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
290.00V	300V	14	1.0040 to 1.1840	
Ohms				
290.00Ω	300Ω	15	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 kΩ	3 kΩ	16	0.9975 to 1.0125	A3Z2, A3Z4
29.000 kΩ	30 kΩ	17	1.0015 to 1.0165	A3Z2, A3Z4
290.00 kΩ	300 kΩ	18	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 MΩ	3 MΩ	19	0.9990 to 1.0090	A3Z2, A3Z4
2.9000 MΩ	10 MΩ	20	0.9990 to 1.0090	A3Z2, A3Z4
Frequency				
10.000 kHz 2.9V rms		21	0.9995 to 1.00050005	A3Y2

5-23. Retrieving Calibration Constants

If a calibration error is suspected, the stored constant can be retrieved and verified over the computer interface. Acceptable calibration constants for each function and range are listed in Table 5-9 (software version 5.4 and higher) or 5-10 (software versions lower than 5.4.) Retrieve the constant with the following command:

CAL_CONST? xx (where xx denotes the calibration constant number)

Table 5-10. Calibration Faults (for sotware versions lower than 5.4)

Input	Range	Calibration Constant		Related Components
		Number	Acceptable Values	
DC Volts				
0.09000V	100 mV	1	1.0315 to 1.1565	A3VR1, A3Z2
0.9000V	1V	2	1.0340 to 1.1540	A3VR1, A3Z2
0.29000V	30 mV0	3	1.0315 to 1.1565	A3VR1, A3Z2
2.9000V	3V	4	1.0315 to 1.1565	A3VR1, A3Z2
29.000V	30V	5	1.0340 to 1.1640	A3VR1, A3Z2, A3Z4
290.00V	300V	6	1.0290 to 1.1590	A3VR1, A3Z2, A3Z4
AC Volts (1 kHz)				
0.02900V	300 mV	7	-0.001 to 0.001	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.29000V	300 mV	8	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.2900V	3V	9	-0.01 to 0.01	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.9000V	3V	10	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.000V	30V	11	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
290.00V	300V	12	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
Ohms				
290.00Ω	300Ω	13	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 kΩ	3 kΩ	14	0.9975 to 1.0125	A3Z2, A3Z4
29.000 kΩv	30 kΩ	15	1.0015 to 1.0165	A3Z2, A3Z4
290.00 kΩ	300 kΩ	16	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 MΩ	3 MΩ	17	0.9990 to 1.0090	A3Z2, A3Z4
2.9000 MΩ	10 MΩ	18	0.9990 to 1.0090	A3Z2, A3Z4
Frequency				
10.000 kHz 2.9V rms		19	0.9995 to 1.0005	A3Y2

5-24. Replacing the EEPROM (A1U1)

The EEPROM provides nonvolatile storage for the instrument serial number, some of the instrument configuration, and all calibration information. If the EEPROM is replaced during repair, the new EEPROM can be programmed with the 7-digit serial number found on the rear panel of the instrument or any 7-digit identifier of your choosing. Note that the serial number is not programmed prior to shipment from the factory.

The following command may be used to program the serial number into the EEPROM:

SERIAL XXXXXXX (xxxxxxx denotes the 7-digit number. Leading zeros

The serial number of the instrument can be accessed by using the "SERIAL?" command. The response will be "0" (if the serial number has not yet been set) or the 7-digit serial number.

5-25. IEEE-488 Interface PCA (A5) Troubleshooting

Refer to Section 7 for a discussion of troubleshooting the IEEE-488 Assembly.

5-26. Memory PCA (A6) Troubleshooting

5-27. Power-Up Problems

The following discussion identifies probable fault areas if the installation of a Memory PCA causes power-up failure for the instrument. The problem is probably a short on A6J1; the Microprocessor on the Main PCA is prevented from accessing ROM and RAM correctly. Make the following checks:

- First check for a GND-to-VCC short on the Memory PCA.
- There may also be a short between an interface signal and VCC, GND,or another interface signal. Check signals D0 .. D7, A0 .. A2, RD*,WR*, MEM*, and RESET*.
- The short may be due to a CMOS input that has been damaged due tostatic discharge; the short is then detectable only when the circuitis powered up. Use an oscilloscope to check activity on each of theinterface signals. Verify that signals are able to transitionnormally between 0 and 5.1V dc (VCC).

5-28. Failure to Detect Memory PCA

If the PRINT destination cannot be set to "StorE", Hydra was unable to determine that the Memory PCA was installed at power-up. The PRINT destination selection procedure is described in Section 3 of the User Manual.

If the Memory PCA is not detected by instrument software, there may be a problem with the IRQ2* or OPS* signal. The Memory PCA connects these two signals when it is installed. A fault with A1R2 or the Microprocessor (A1U4) could also result in failure to detect the Memory PCA.

5-29. Failure to Store Data

Configure the instrument to fast reading rate, 3V dc range on channel 1, and scan interval of 0:00:00. Setup storage of all scan data to the Memory PCA: press SHIFT PRINT, select "StorE", press ENTER, select "ALL", and press ENTER. Then, if the "PRN" annunciator is not on, enable data storage by pressing PRINT ("PRN" annunciator comes on.)Finally, enable scanning press SCAN.

While the instrument is scanning, check that data is being stored correctly. Use an oscilloscope to monitor activity on the 7 outputs of the Byte Counter (A6U3) and the 11 outputs of the Page Register (A6U1 and A6U4). Since the repetition rate is fairly low, it may be necessary to use a storage oscilloscope to capture the activity. If either of these circuit elements is not functioning, check the Address Decode circuit (A6U2, A6U5, A6U8) for activity at the end of every scan.

If the outputs of the Page Register and the Byte Counter are showing reasonable activity, verify that these signals are also being received by the Nonvolatile Memories (A6U6 and A6U7). Check CS*, WR*, and OE* inputs on A6U6 and A6U7 for proper activity.

There may also be a problem in reading data back from the Memory PCA. After allowing the Memory PCA to fill with scan data ("F" annunciator on the display lit), turn off scanning (press SCAN). Now press the LIST button and select the "StorE" entry in the menu. While the Hydra is formatting and sending the Memory PCA contents to the RS-232 interface, again monitor the circuit areas described above for reasonable voltage levels and activity.

Chapter 5A
Diagnostic Testing and Troubleshooting (2635A)

5A-1. Introduction

Hydra provides error code information and semi-modular design to aid in troubleshooting. This section explains the error codes and describes procedures needed to isolate a problem to a specific functional area. Finally, troubleshooting hints for each functional area are presented.

But first, if the instrument fails, check the line voltage fuse and replace as needed. If the problem persists, verify that you are operating the instrument correctly by reviewing the operating instructions found in the Hydra Users Manual.

⚠ Warning

Opening the case may expose hazardous voltages. Always disconnect the power cord and measuringinputs before opening the case. And remember that repairs or servicing should be performed only by qualified personnel.

Required equipment is listed in Section 4 of this manual.

Signal names followed by a '*' are active (asserted) low. Signal names not so marked are active high.

5A-2. Servicing Surface-Mount Assemblies

Hydra incorporates Surface-Mount Technology (SMT) for printed circuit assemblies (pca's). Surface-mount components are much smaller than their predecessors, with leads soldered directly to the surface of a circuit board; no plated through-holes are used. Unique servicing, troubleshooting, and repair techniques are required to support this technology. The information offered in the following paragraphs serves only as an introduction to SMT. It is not recommended that repair be attempted based only on the information presented here. Refer to the Fluke "Surface Mount Device Soldering Kit" for a complete demonstration and discussion of these techniques. (In the USA, call 1-800-526-4731 to order.)

Since sockets are seldom used with SMT, "shotgun" troubleshooting cannot be used; a fault should be isolated to the component level before a part is replaced. Surface-mount assemblies are probed from the component side. The probes should make contact only with the pads in front of the component leads. With the close spacing involved, ordinary test probes can easily short two adjacent pins on an SMT IC.

This Service Manual is a vital source for component locations and values. With limited space on the circuit board, chip component locations are seldom labeled. Figures provided in Section 6 of this manual provide this information. Also, remember that chip components are not individually labeled; keep any new or removed component in a labeled package.

Surface-mount components are removed and replaced by reflowing all the solder connections at the same time. Special considerations are required.

- The solder tool uses regulated hot air to melt the solder; there isno direct contact between the tool and the component.

- Surface-mount assemblies require rework with wire solder rather thanwith solder paste. A 0.025-inch diameter wire solder composed of 63%tin and 37% lead is recommended. A 60/40 solder is also acceptable.
- A good connection with SMT requires only enough solder to make apositive metallic contact. Too much solder causes bridging, while toolittle solder can cause weak or open solder joints. With SMT, theanchoring effect of the through-holes is missing; solder provides theonly means of mechanical fastening. Therefore, the pca must beespecially clean to ensure a strong connection. An oxidized pca padcauses the solder to wick up the component lead, leaving littlesolder on the pad itself.

Refer to the Fluke "Surface Mount Device Soldering Kit" for a complete discussion of these techniques.

5A-3. Error Codes

At reset, the Hydra Data Bucket software performs power-up self-tests and initialization of Flash Memory, NVRAM, Display, Calibration Data, and measurement hardware. Self-test failures are reported on the display with "Error" in the left display and an error code (1-9,A,b,C,d) in the right display.

Several of these error codes might never be displayed. Certainly, errors 4 and 5, which signify a faulty or dead display, could not be reported in the normal (displayed) manner. Other errors might not appear on the display. Therefore, the following additional methods exist for accessing error information:

- If 'boot' is displayed at power-up, it is likely that one ofthe memory tests failed (Errors 1 through 3). To determinewhat the error status was, connect a terminal or computer to theRS-232 interface (19200 baud, 8 data bits, no parity). Send a carriagereturn or line feed character to the instrument and it should sendback a prompt that shows a number followed by a '>' character. Thenumber is interpreted in the same way as the responses for the *TST?and POWERUP? commands; refer to *TST? in Section 4 of the HydraUsers Manual. For example, a '4>' prompt indicates that the test ofthe NVRAM (A1U20 and A1U24) failed and the instrument was not ableto safely power-up and operate.
- The computer interfaces can be used to determine self-check statususing the *TST? query. Refer to Section 4 of the Hydra Data BucketUsers Manual for a description of the *TST? response. Note that theextent of the error-producing damage could also cause the instrumentto halt before the computer interfaces are operational.
- The POWERUP? computer interface command can be used to determinewhich errors were detected at power-up. POWERUP? uses the sameresponse format as *TST?; refer to *TST? in Section 4 of the HydraData Bucket Users Manual.

Table 5A-1 describes the error codes.

Note

Each error code is displayed for 2 seconds.

Table 5A-1. Error Codes (2635A)

Error	Description
1	Boot Firmware (A1U14 and A1U16) Checksum Error
2	Instrument Firmware (A1U14 and A1U16) Checksum Error
3	NVRAM (A1U20 and A1U24) Test Failed
4	Display Power-up Test Failure
5	Display Not Responding
6	Instrument Configuration Corrupted
7	Instrument Calibration Data Corrupted
8	Instrument Not Calibrated
9	A/D Converter Not Responding
A	A/D Converter ROM Test Failure (A3U9)
b	A/D Converter RAM Test Failure (A3U9)
C	A/D Converter Self Test Failure
d	Memory Card Interface Not Installed
Refer to Troubleshooting information later in this section	
Error 1	Boot Firmware (A1U14 and A1U16) Checksum Error All the bytes in the Boot section of Firmware (including a checksum) are summed.
Error 2	Instrument Firmware (A1U14 and A1U16) Checksum Error All the bytes in the Instrument section of Firmware (including a checksum) are summed.
Error 3	NVRAM (A1U20 and A1U24) Test Failed A test pattern of data is written to and then read from the NVRAM locations that are not used for Non-volatile instrument configuration and measurement data. If the pattern read from any RAM location is not the same as the pattern written, the test fails.
Error 4	Display Power-up Test Failure
Error 5	Display Not Responding The display processor automatically performs a self-check on power-up, and the Microprocessor attempts to read the result of this test.
Error 6	Instrument Configuration Corrupted The instrument configuration information stored in nonvolatile RAM (A1U20 and A1U24) has been corrupted. (The Cyclic Redundancy Checksum on this memory is not correct for the information stored there.) The instrument configuration is reset to the default configuration.
Error 7	Instrument Calibration Data Corrupted The Flash Memory (A1U14 and A1U16) is divided into three storage areas: the Boot Firmware, the Calibration Data, and the Instrument Firmware. The Calibration Data uses a Cyclic Redundancy Checksum (CRC) for data security, against which the data is checked on power-up.
Error 8	Instrument Not Calibrated The calibration data includes status information to indicate which of the measurement functions (Volts DC, Volts AC, Ohms, and Frequency) have been calibrated. If any functions have not been calibrated, this error is reported.
Note *Errors 7 and 8 should always appear the first time an instrument is powered up with a new, uninitialized Flash Memory. Error 8 continues to appear at subsequent power-ups until the instrument is fully calibrated.*	

Table 5A-1. Error Codes (2635A) (cont)

Error	Description
Error 9	A/D Converter Not Responding This error is displayed if communication cannot be established with the 6301Y Microcomputer (A3U9).
Error A	A/D Converter ROM Test Failure (A3U9) All bytes of internal ROM for the 6301Y Microcomputer (A3U9) (including the checksum byte) are summed.
Error b	A/D Converter RAM Test Failure (A3U9) Complementary patterns are alternately written to and read from each location of the 256 bytes of RAM internal to the 6301Y Microcomputer (A3U9).
Error C	A/D Converter Self Test Failure The Analog Measurement Processor (A3U8) is programmed to do self test measurements.
Error d	Memory Card Interface Not Installed The Microprocessor checks the system at power-up to determine whether the Memory Card Interface is installed.

5A-4. General Troubleshooting Procedures

Hydra allows for some fault isolation using self-diagnostic routines and descriptive error codes. However, these features are somewhat limited and do not provide in-depth troubleshooting tools.

Hydra incorporates a semi-modular design; determining modules not related to a problem constitutes the first step in the troubleshooting process.

As a first step, remove the Memory Card Interface (A6) from the Hydra Databucket (2635A). Refer to Section 3 of this manual for removal procedures. If removal of this assembly results in improved instrument operation, refer to the Memory Card Interface troubleshooting found later in this section.

Measuring the power supplies helps to isolate a problem further. Refer to Table 5A-2 and Figure 5A-1 for test point identification and readings. If power supply loading is suspected, disconnect the Display PCA at A1J2. If this action solves the loading problem, proceed to Display Assembly Troubleshooting elsewhere in this section. Otherwise, refer to Power Supply Troubleshooting.

Table 5A-2. Preregulated Power Supplies (2635A)

Preregulated Voltage	Measurement Points	Resulting Supply
-8.9V	A1CR13-2 to A1TP1	VEE
-30.9V	A1TP4 to A1TP1	VLOAD
+9.2V	A1CR5 cathode to A1TP30	VDD, VDDR
-8.6V	A1CR7 anode and A1TP30	VSS

If the power supplies appear to be good, check the Display clock signal (DCLK (A1R85) and E clock signal (A2U4-1)). This clock signal is not symmetrical; it should be about +5.0 volts for about 325 nanoseconds and then near 0 volts for about 651 nanoseconds. If it is not correct at either measurement point, remove the Display Assembly and check the Display clock again at A1R85. If it is now correct, the problem is most likely on the Display Assembly. If it is still incorrect, the problem is probably in the Digital Kernel on the Main Assembly.

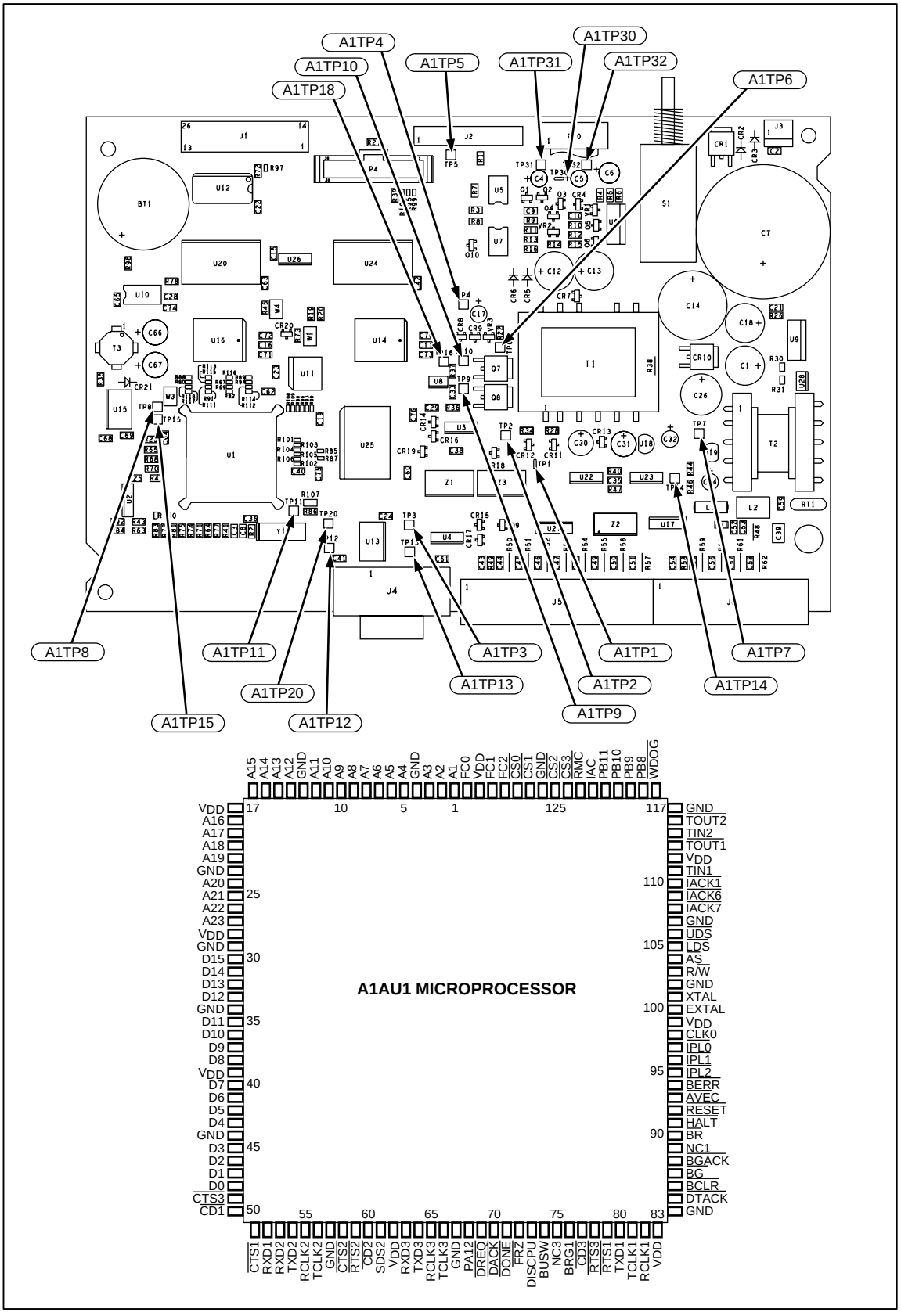


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Figure 5A-1. Test Point Locator, Main PCA (A1) (2635A)

Refer to the Schematic Diagrams in Section 8 during the following troubleshooting instructions. Also, these diagrams are useful in troubleshooting circuits not specifically covered here.

5A-5. Power Supply Troubleshooting

⚠ Warning

To avoid electric shock, disconnect all channel inputs from the instrument before performing any troubleshooting operations.

5A-6. Raw DC Supply

With the instrument connected to line power (120V ac, 60 Hz) and turned ON, check for approximately 14V dc between A1TP1 (GND) and the "+" terminal of capacitor A1C7 (or the cathode of either A1CR2 or A1CR3). (This voltage is approximately 30V dc at 240V ac line.) If no voltage or a very low voltage is present, check for approximately 24V ac across the secondary of the power transformer (or approximately 50V ac at 240V ac line).

The voltage at the output of A1U19 (also A1TP7), should be about +5.3V dc. At 120V ac, 60-Hz line power input, the Hydra Databucket line current is approximately 24 mA. At 50-Hz, 120V ac line power input, there is a 5 to 10% increase in this current figure.

5A-7. Power Fail Detection

The Power Fail Detection circuit monitors the Raw Supply so that the Microprocessor can be signaled when power is failing. A reference voltage of nominally 1.3 volts dc (internal to A1U10) is compared to the voltage at A1U10-4. If A1U10-4 is less than about 1.3 volts dc, the power fail output (A1U10-5) should be low. This corresponds to a raw supply voltage of about 8 volts dc (A1C7). If the raw supply voltage is greater than 8 volts dc, the power fail output (A1U10-5) should be high. If the power fail output is near 0V dc during normal operation, the Microprocessor will sense that power is failing and will not be able to complete a scan operation.

5A-8. 5-Volt Switching Supply

Use an oscilloscope to troubleshoot the 5-volt switching supply. With the oscilloscope common connected to A1TP1, check the waveform at either A1U9, pin 4 or A1T1, pin 2 to determine the loading on the 5-volt switching supply. The output voltage of the 5-volt switching supply at A1TP2 (VCC) is normally about 5.0V dc with respect to A1TP1 (GND).

- Normal Load:

The signal at A1U9-4 (with respect to A1TP1) is a square wave with a period of 9 µs to 11 µs and an ON (voltage is low) duty ratio of about 0.38 with the line voltage at 120V ac. The amplitude is usually about 15V p-p. The positive-going edge will be "fuzzy" as the duty ratio is varying to compensate for the ripple of the raw supply and the pulsing load of the inverter supply. See Figure 5A-2 (NORMAL LOAD).

- Very Heavy Load or 5V Supply Shorted:

Under heavy load (example: A3 A/D Converter PCA has a short circuit) it could load down the power supply voltage such that the current limiting feature is folding the supply back. For example, if the supply is folded back due to excessive current draw, unplug the ribbon cable at A3J10 on the A/D Converter PCA. When tracking down power supply loads, use a sensitive voltmeter and look for resistive drops across filter chokes, low value decoupling resistors, and circuit traces. Also check for devices that are too warm. On the A3 A/D Converter PCA, all devices run cool except A3U5 microprocessor and A3U8 FPGA, which run warm, but not hot.

5A-9. Inverter

Use an oscilloscope to troubleshoot the inverter supply. The outputs of the inverter supply are -5V dc (VEE), -30V dc (VLOAD), and 5.4V ac (FIL1 and FIL2) outguard, and +5.3V dc (VDD), -5.4V dc (VSS), and +5.6V dc (VDDR) inguard. Refer to Figure 5A-3. The signal at the drains of the two inverter switch FETs (A1Q7 and A1Q8) should be a 10V peak square wave with a period of approximately 18 us. The gate signal is a 5.1V peak square wave with rounded leading and trailing edges. The leading edge has a small positive rounded pulse with an amplitude of 1.8V peak and a pulse width of about 0.3 us. The signal at A1U22-5 and A1U22-6 is a symmetrical square wave with an amplitude of 5.1V peak and a period of about 18 us. The negative-going trailing edge of both square waves is slower than the rising edge and has a small bump at about 1.5 volts. The signal at A1U22-3 (TP14) is a symmetrical square wave with a period of about 9 us.

For the inverter to operate, the 110-kHz oscillator must be operating properly. If the signal at A1U22-3 is missing, begin by checking the voltage at A1TP7. The voltage should be about +5.3V dc. Then, using an oscilloscope, check for a square wave signal at A1U23-9 and a square wave signal at A1U23-8. If the FETs are getting proper drive signals, failures that heavily load the inverter supply will usually cause the inverter to draw enough current to make the switcher supply go into current limit. Shorted rectifier diodes and shorted electrolytic capacitors will cause heavy load conditions for the inverter.

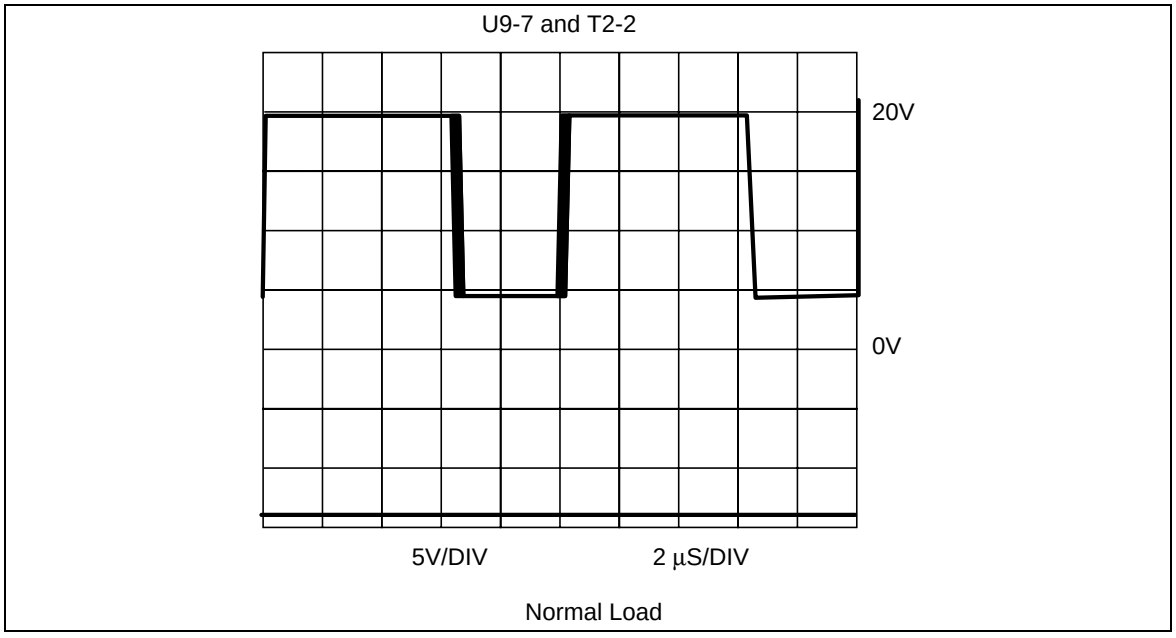
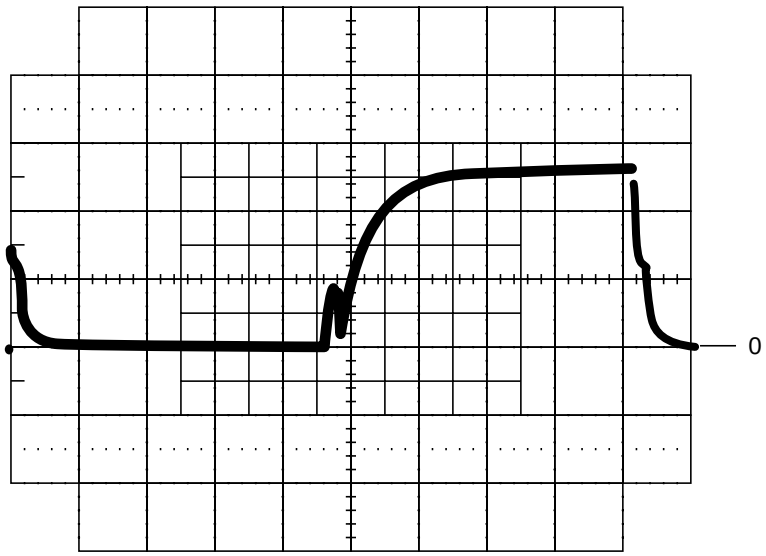


Figure 5A-2. 5-Volt Switching Supply (2635A)

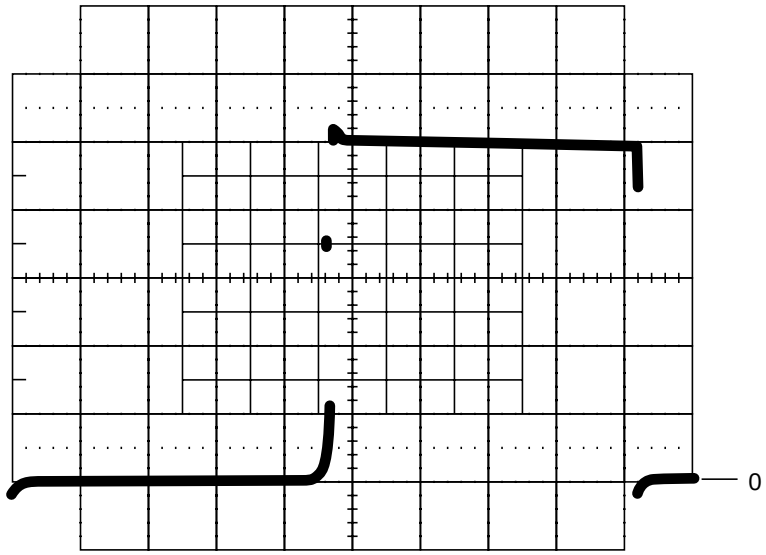
TP9 AND TP10



2V/DIV 2µS/DIV

FET GATE SIGNAL

Q7, Q8, OR T1-1 OR -3



2V/DIV 2µS/DIV

FET DRAIN SIGNAL

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Figure 5A-3. Inverter FET Drive Signals (2635A)

Note

When making voltage measurements in the invertercircuit, remember that there are two separategrounds. The outguard ground is the 'GND' testpoint (A1TP1), and the inguard ground is the'COM' test point (A1TP30).

The inguard regulator circuits for VDD and VSS have current limits. Shorts and heavy loads between VDD and COM, VSS and COM, and VDD and VSS will cause one or both supplies to go into current limit. The current supplied by either supply can be checked by measuring the voltage across the current sense resistors, A1R13 and A1R15. The typical voltage across A1R13 is 0.30, and the typical voltage across A1R15 is 0.40V.

Generally, open electrolytic capacitors in the inverter supply will cause excessive ripple for the affected supply. Also, the rectified dc voltage for the supply with the open capacitor will be lower than normal. Normal voltage levels at the rectifier outputs for each inverter supply are shown in Table 5A-2.

The loads for the inguard supplies can be disconnected by removing the cable to the A/D Converter PCA at A3J10. The inguard regulator circuits and VDDR regulator will operate with no loads, and troubleshooting can be performed by making voltage measurements.

The normal input current to the inverter supply is about 11.25 mA, or 0.225 mV across A1R38 (when the instrument is not measuring).

Table 5A-3 provides a Power Supply troubleshooting guide.

5A-10. Analog Troubleshooting

⚠ Warning

To avoid electric shock, disconnect all channelinputs from the instrument before performing anytroubleshooting operations.

Refer to Figure 5A-4 and Figure 5A-5 for test point locations on the A/D Converter PCA.

First, check for analog-related errors displayed at power up. An 'Error 9' means that the Main Microprocessor A1U1 is not able to communicate with the A/D Microcontroller A3U9. 'Error A' and 'Error b' mean that a failure has occurred in the internal memory of the A/D Microcontroller A3U9. 'Error C' means that the Analog Measurement Processor A3U8 is not functioning properly.

Check the inguard power supplies on the Main PCA with and without the A/D Converter PCA connected. The inguard supplies must be measured with respect to COM testpoint A1TP30.

Power Supply	Test Location	Acceptable Range
VDD	A1TP31	5.00 to 5.70V dc
VSS	A1TP32	-5.10 to -5.75V dc
VDDR	A1C6+	5.30 to 5.95V dc

Table 5A-3. Power Supply Troubleshooting Guide (2635A)

Symptom	Fault
Line fuse blows.	- Shorted A1CR2 or A1CR3. - Shorted A1CR10. - Shorted A1C7. - Shorted A1C26.
Supply voltage for A1U23 and A1U22 is greater than 7V (7 to 30V).	Input-to-output short of A1U19. This fault may have caused damage to A1Q7 and A1Q8.
VCC (5.1V) supply is at the raw supply level (7.5 to 35V dc).	Shorted switch transistor in A1U9 (A1U9-5 to 7). Open A1C26 can cause switch transistor to short.
VCC (5.1V) supply shows excessive ripple (about 1V p-p).	A1C14 open.
VCC is below approximately 4.5V. Duty cycle of 5V switcher supply is very low (ON time near 0.1).	Drain-to-source short of A1Q7 or A1Q8.
VCC is about 1.5V. 5V switcher supply is in current limit.	Shorted A1CR5 or A1CR6.
VCC is below approximately 1V. 5V switcher supply is in current limit, with very low duty cycle (ON time near 0.1).	Shorted A1C14.
VCC is below approximately 4.5V. 5V switcher supply is in current limit, with very low duty cycle (ON time near 0.1).	- Q or Q* output of A1U22 stuck high. - A1U23 pin 8 output stuck high or low. - Shorted A1CR7 - Shorted A1CR9 (either diode), pins 1-3 or 2-3. - Shorted A1C30. A1CR13 may also be damaged. - Shorted A1C31. A1CR13 may also be damaged. - Shorted A1C12. - Shorted A1C13. - Shorted A1CR8 (either diode), pins 1-3 or 2-3.
VLOAD (-30V dc) Inverter Supply is at -36V.	Q output of A1U22 stuck low.
VLOAD (-30V dc) Inverter Supply is OFF.	Q* output of A1U22 stuck low.
VLOAD (-30V dc) Inverter Supply ripple.	- Open A1CR8 (either diode). - Open A1CR9 (either diode).
VDD (5.3V dc) supply at approximately 9.2V.	Emitter-to-collector short of A1Q2.
VSS (-5.4V dc) supply at approximately -9.2V.	Emitter-to-collector short of A1Q5.
VDDR (5.6V dc) supply at approximately 10V.	Input-to-output short of A1U6.
VDDR supply has 4-to-5 volt spikes when the A/D relays are switched (set or reset).	Open A1C12.
VEE (-5V dc) supply is low (near zero).	- Open A1C30. - A1CR13 open.
A1CR13, Diode 1-3 shorted or open.	A1C30 may be shorted.
VEE supply is high (near -9V).	Input-to-Output short of A1U18.
A1U18 input has large square wave component.	Open A1C31.

Table 5A-3. Power Supply Troubleshooting Guide (2635A) (cont)

Symptom	Fault
A1U18 hot.	Shorted A1C32
A1U18 oscillates.	Open A1C32.
A1U19 oscillates.	Open A1C34.
A1U19 very hot.	- Shorted A1U22 (VCC to VSS). - Shorted A1U23 (VCC to VSS).
A1U19 hot.	Shorted A1C34.

Check the inguard supply voltages on the A/D Converter PCA with respect to A3TP9. The following table lists the components nearest the power supply test points.

Power Supply	Nearest Component	Acceptable Range
VDD	A3C8	5.00 to 5.70V dc
VSS	A3C9	-5.10 to -5.75V dc
VDDR	A3C19	5.30 to 5.95V dc
+VAC	A3CR1	4.7 to 5.7V dc
-VAC	A3C26	-4.8 to -5.7V dc

Check that the inguard Microcontroller A3U9 RESET* line is de-asserted. Check VDD at A3TP1, referenced to A3TP9.

Check that the microcontroller crystal oscillator is running. When measured with a high input impedance oscilloscope or timer/counter, the oscillator output at A3TP10 should be a 3.6864-MHz sine wave (271.3 ns period), and the divided-down E clock output at A3U9 pin 68 should be a 921.6 kHz-square wave (1.085 µs period).

Check outguard to inguard communication. Setup an input channel and enable monitor measurements on that channel, causing the outguard to transmit to the inguard approximately every 10 seconds.

On the Main PCA, look for outguard-to-inguard communication (5.0V (VCC) to near 0V pulses) at A1TP15, referenced to A1TP1. On the A/D Converter PCA, check for 5.35V (VDD) to near 0V pulses at A3TP8, referenced to A3TP9.

At the start of outguard-to-inguard communication, the A/D Microcontroller (A3U9) should be RESET. Check for this reset pulse (5.35V (VDD) to near 0V, lasting approximately 1 millisecond) on A3TP1 with respect to A3TP9.

Check for the following inguard-to-outguard communication activity:

PCA	Test Point	To	Pulses
A/D Converter	A3TP7	A3TP9	5.55V (VDDR) to 0.7V
Main	A1TP8	A1TP1	5.0V dc (VCC) to 0.0V

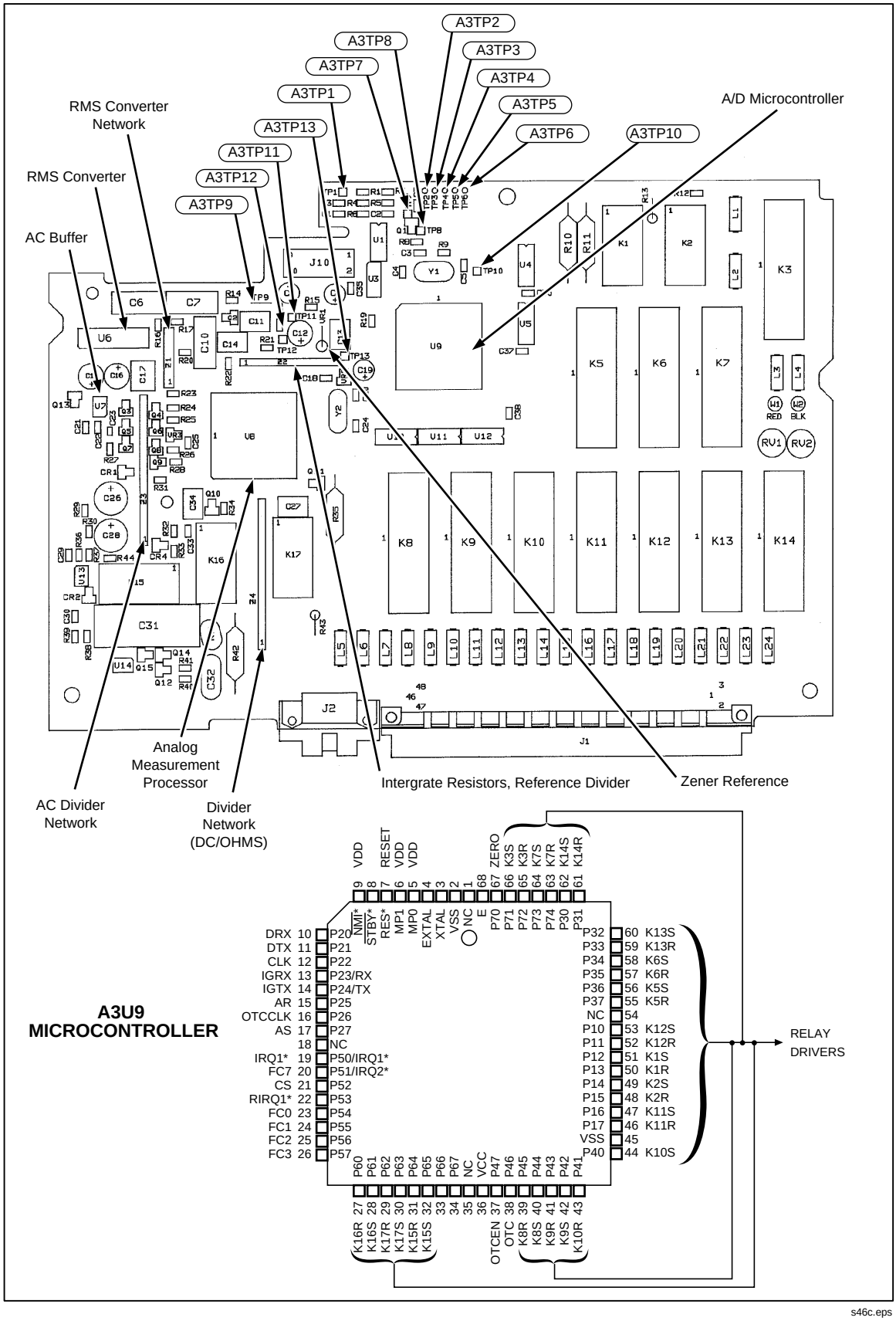

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Figure 5A-4. Test Points, A/D Converter PCA (A3, A3U8) (2635A)

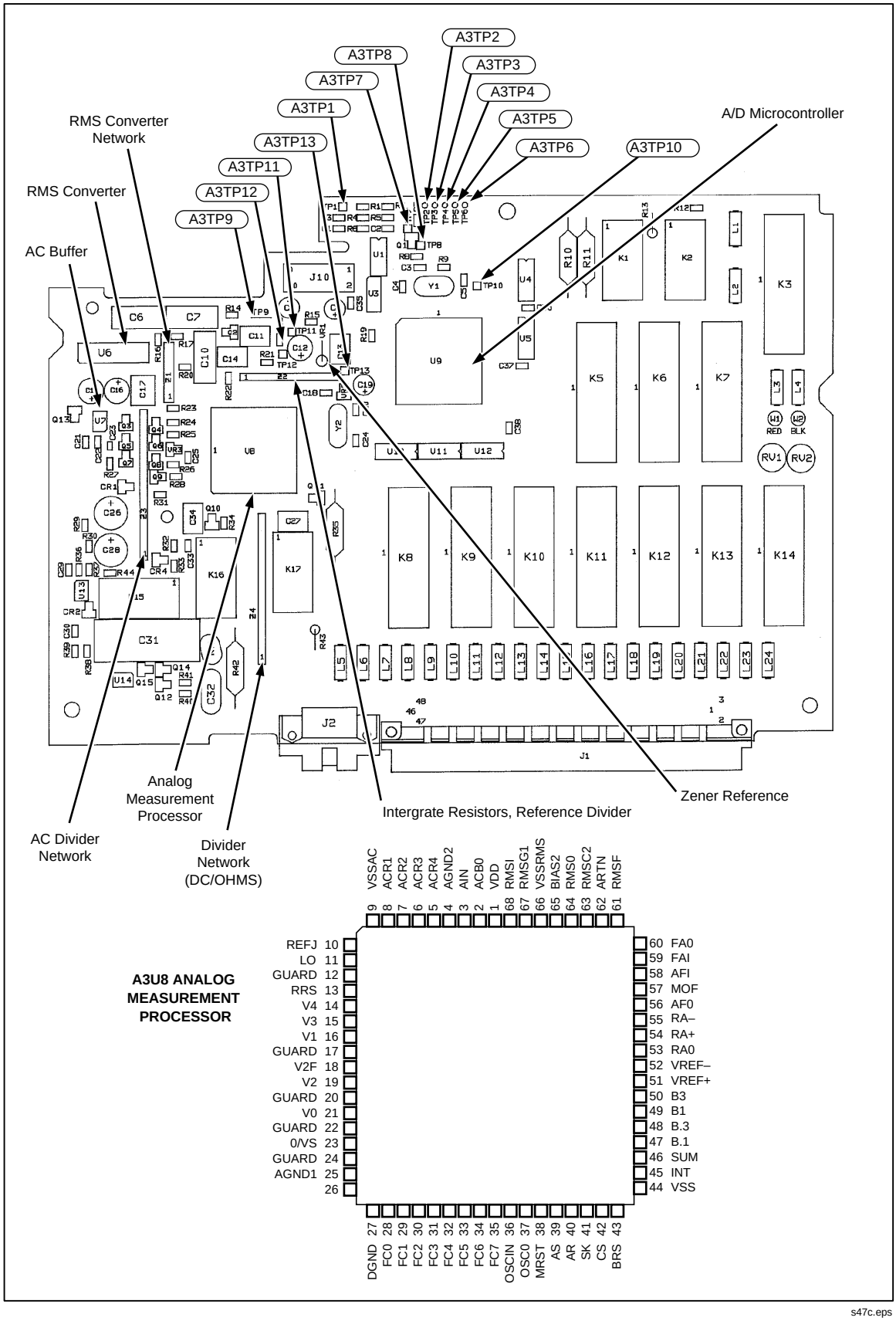

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Figure 5A-5. Test Points, A/D Converter PCA (A3U9) (2635A)

Lack of outguard-to-inguard communication activity may be due to improper operation of circuit elements other than A3U9. Using a high input impedance oscilloscope or timer/counter, check for proper Analog Processor (A3U8) crystal oscillator operation. A 3.84-MHz sine wave (260 ns period) should be present at A3U8 pin 37 with respect to A3TP9.

Check the A/D Converter voltage reference:

A3TP12 to A3TP11 (across A3C12) = +1.05V (+0.10V, -0.02V)

Setup the instrument to measure ohms on the 300Ω range. Monitor ohms on a channel with an input of approximately 270Ω. Check that the Analog Processor IC (A3U8) is making A/D conversions. The integrator output waveform at A3TP13 (referenced to A3TP9) should resemble the waveform shown in Figure 5A-6.

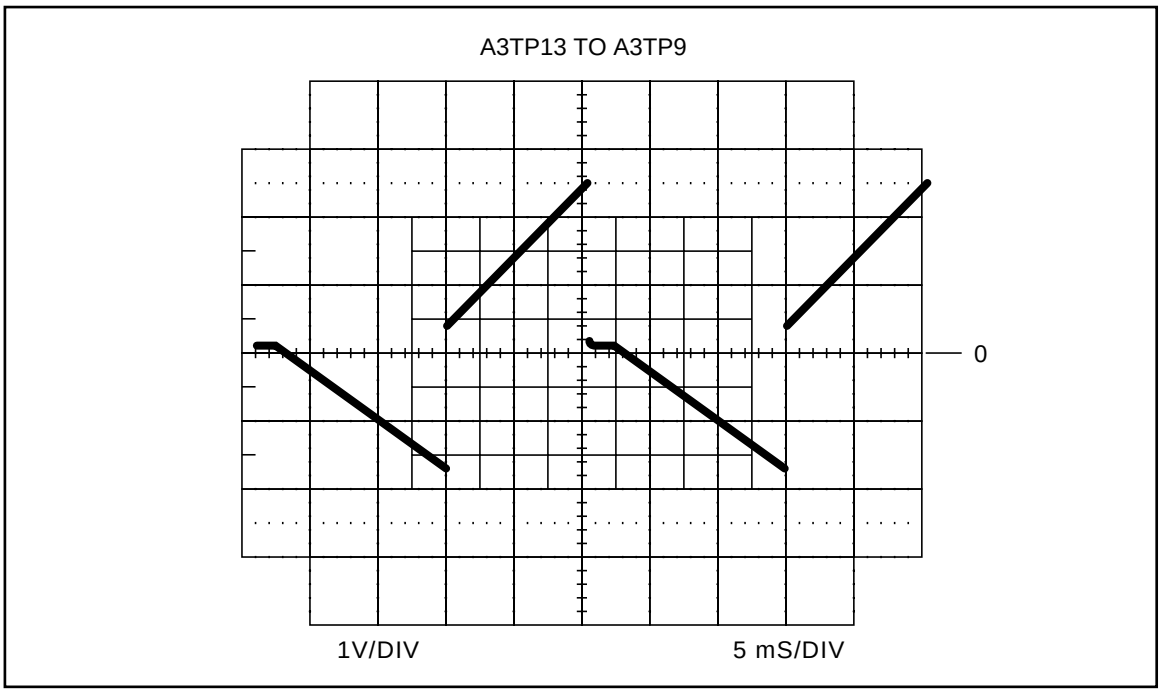


Figure 5A-6. Integrator Output (2635A)

Check for channel relay operation by setting up a channel and selecting and de-selecting monitor measurement mode. One or more relays should click each time the monitor button is pressed or channels are changed.

In general, check that the relays are getting the proper drive pulse signals for specific functions and channels and that they are in the correct position.

5A-11. DC Volts Troubleshooting

Setup the instrument to measure a specific channel on the 300 mV or 3V range, and apply an input to that channel. Then trace the HI signal (referenced to the input channel LO terminal) as described in Table 5A-4.

If the input HI path traces out properly, remove the input from the channel and trace continuity through the LO path. Check among A3L4-A3L24, A3K1-A3K14, A3R35, A3R43, and A3U8 pin 11.

Table 5A-4. DC Volts HI Troubleshooting (2635A)

Checkpoint	Signal Description	Possible Fault
A3R11 HI	Input	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12, A3L1, A3L2, A3L3
A3U8 pin 23	Input	A3R11, A3K17, A3R42, A3C32
A3U8 pin 58	Input, DC filter output	A3U8, A3Q2

5A-12. AC Volts Troubleshooting

Setup the instrument to measure a channel on the 300 mV ac range, and apply a signal to that channel. Then trace this HI signal (referenced to the input channel LO terminal) as described in Table 5A-5.

If the input HI path traces out properly, remove the input from the channel, and trace continuity through the LO path. Check among A3L4 through A3L24, A3K1 through A3K14, A3R43, A3R34, A3K16, and A3U8 pin 13.

Table 5A-5. AC Volts HI Troubleshooting (2635A)

Checkpoint	Signal Description	Possible Fault
A3R11 HI	Input	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12 A3L1, A3L2, A3L3
A3Z3 pin 1	Input	A3R11, A3C31, A3K15
A3U6 pin 13	Amplified (X 2.5) input	A3U7, A3Z3, A3Q3 through A3Q9, A3C15, A3C16, A3R24, A3A25, A3R26, A3R27, A3R28, A3C23, A3U6, A3Q13, A3U8
A3Z1 pin 2	DC equivalent of original input	A3Z1, A3U8, A3R20, A3C6, A3C7, A3C10, A3R16, A3R17
A3U8 pin 61	DC equivalent of original input	A3Z1, A3U8, A3R20, A3C6, A3C7, A3C10, A3R16, A3R17

5A-13. Ohms Troubleshooting

Setup a channel with an open input for the desired ohms range and place the instrument in monitor mode on that channel. Use a meter with high input impedance to measure the open-circuit voltage at the channel input for the ohms range as listed in Table 5A-6. If a high input impedance meter is not available, only the 30-kΩ and lower ranges can be checked.

If the proper voltage is not measured, setup a channel on the 300Ω range (open input), and have the instrument monitor that channel. Check for 3V dc with respect to A3TP9, and work through the HI SOURCE and HI SENSE paths as described in Table 5A-7.

If the HI path works correctly, trace continuity through the LO path. Check among A3L4 through A3L24, A3K1 through A3K14, A3R35, A3U8 pin 11, A3R43, A3K16, A3R34, and A3U8 pin 13.

Table 5A-6. Ohms Open-Circuit Voltage (2635A)

Range	Voltage
300Ω	3V
3 kΩ	1.3V
30 kΩ	1.3V
300 kΩ	3V
3 MΩ	3V
10 MΩ	3V

Table 5A-7. Ohms HI Troubleshooting (2635A)

Checkpoint	Signal Description	Possible Fault
A3U8 pin 14	Ohms Source	A3U8
A3R10 HI SRC	Ohms Source	A3R10, A3K16, A3RT1, A3Z4, A3Q10
Channel HI	Ohms Source	A3K1 through A3K14, A3U4, A3U5, A3U11, A3U12, A3L1, A3L2, A3L3
A3U8 pin 23	Ohms Source	A3R11, A3K17, A3R42, A3C32
A3U8 pin 58	Ohms Source filter output	A3U8, A3Q2

5A-14. Digital Kernel Troubleshooting

At power-up, if the display does not light or lights up and fails to report errors or begin operation, use the following troubleshooting procedures.

To determine the relative health of the MC68302 Microprocessor (A1U1), first check for a valid system clock (SCLK) at TP11. Use an oscilloscope to check for the SCLK clock at A1TP11. Look for a 12.288-MHz square wave that transitions from 0 to 5V dc (VCC).

- If this signal is present, check for a similar waveform at pinA1U25-30 of the FPGA. If a 12.288-MHz square wave is not presentthere, resistor A1R107 is probably bad.
- If the SCLK signal (A1TP11) is something other than a 12.288-MHzsquare wave, it is most likely that the problem is related to thecrystal oscillator circuit (A1U1, A1Y1, A1C3, A1C8, or A1R2).

If the SCLK signal is good, check the Display Clock (DCLK) output from A1U25-19. DCLK should have a frequency of 1.024-MHz (period of 976 nanoseconds). The DCLK signal is not symmetrical; use an oscilloscope to verify that it is high for about 325 nanoseconds and then low for about 651 nanoseconds. The operation of the Display assembly depends on the DCLK signal. Missing segments, intensified digits, a strobing display, or a blank display can be caused by a faulty DCLK clock.

- If the DCLK signal (A1U25-19) is not present but the SCLK signal iscorrect at A1U25-30, the problem may be that A1U25 was notconfigured correctly at power-up or A1U25 is defective.
- If the OCLK signal (A1U25-22) is a 3.072-MHz square wave but the DCLKsignal is wrong, A1U25 must be defective.

During instrument power-up, the RESET* and HALT* signals are held low for 140 to 280 milliseconds after the VCC power supply is greater than 4.65 volts dc. Before the Microprocessor can begin execution of the firmware stored in the Flash Memory, the reset circuit must release the RESET* and HALT* signals (A1U2-11 and A1U2-8 respectively) and allow them to go high. Verification of the operation of the RESET* and HALT* signals is best done by using a storage oscilloscope.

After the Microprocessor has begun execution of the instructions stored in Flash Memory (A1U14 and A1U16), the Microprocessor may drive the HALT* signal (A1U1-91) low if the instructions executed are not correct. Another sign of incorrect instruction execution is the Bus Error signal (BERR*;A1U1-94) going low to indicate that an access to an unused area of memory space was done. To troubleshoot these problems, use an oscilloscope to check the activity of the address, data, and control signals to the Flash Memory devices (A1U14 and A1U16). It may also be useful to check signal continuity by using a DMM with the instrument power off.

To check the Flash Memory control signals, verify that A1U1-128 is going low and is also appearing on pins A1U14-22 and A1U16-22 of the Flash Memory devices. It may be necessary to continually reset (power on) the instrument to check these lines, since the activity probably halts quickly when the instrument software goes awry. Verify that RDU* (A1U11-14 and A1U14-24) goes low when A1U1-128 is low. Verify that RDL* (A1U11-19 and A1U16-24) goes low when A1U1-128 is low. If all this is true, the problem is with the Flash Memory or there is a fault in the address/data lines from the MC68302 Microprocessor.

Verify that the XINIT* output (A1U25-65) goes high after RESET* goes high. Verify that the mode pins and extra chip select input on the FPGA (A1U25) are properly connected to VCC and GND. Pins 6, 29, 54, and 56 must be about 5 volts dc. Pins 52 and 93 must be near 0 volts dc. If the Microprocessor is able to correctly fetch instructions from the Flash Memory, the Microprocessor tries to program the FPGA.

Address decoding for I/O devices like the FPGA is done by A1U11. Verify that the PGA* output (A1U11-12) goes low when the Microprocessor attempts to access the FPGA. Verify the address and I/O* inputs to A1-U11 (pins 2 through 8) according to the decoding shown in the following table.

Output	A<12>	A<11>	A<10>	A<9>	A<8>	A<7>	I/O*
PGA* (A1U11-12)	0	0	0	0	0	0	0
RTC* (A1U11-16)	0	0	0	0	0	1	0
OPTE* (A1U11-12)	0	0	0	0	1	0	0

Programming of the FPGA is initiated by the Microprocessor by driving the XD/P* (A1U25-80) and RESET* (A1U25-78) signals low simultaneously. RESET* is pulsed low by the Microprocessor for approximately 10 microseconds. The Microprocessor then waits for XINIT* (A1U25-65) to go high; if this doesn't happen, the Watchdog Timer in the Microprocessor will reset the instrument after several seconds by driving POR* (A1U1-117) low. Verify that the Microprocessor waits until XRDY (A1U25-99) is high before writing each byte to the FPGA. (A1U25-88 and A1U25-5 both go low during the write cycle.) Check the XD/P* signal (A1U25-80) at the end of the FPGA programming; if it doesn't go high, the Microprocessor will repeat the FPGA programming sequence until it works correctly or the Watchdog Timer in the Microprocessor resets the instrument by driving POR* (A1U1-117) low. If FPGA programming is failing, check the D<8> through D<15>, PGA*, WRU*, XINIT*, XRDY, XD/P*, and RESET* signals for activity with an oscilloscope. It may also be necessary to check the continuity of these signals with a DMM when the instrument power is off.

If the instrument powers up and displays 'boot,' it is likely that one of the memory test errors (Errors 1 through 3) was detected. To determine what the error status was, connect a terminal or computer to the RS-232 interface (19200 baud, 8 data bits, no parity). Assuming that the RS-232 interface is functional, send a carriage return or line feed character to the instrument, and it should send back a prompt that shows a number followed by a '>' character. The number is interpreted in the same way as the responses for the *TST?and POWERUP? commands; refer to *TST? in Section 4 of the Hydra Data Bucket Users Manual. For example, a '4>' prompt indicates that the test of the NVRAM (A1U20 and A1U24) failed and the instrument was not able to safely power-up and operate.

Now send a 't' character followed by a carriage return to the instrument to request a retest of the firmware stored in Flash Memory. If both the boot firmware and the instrument firmware checksums are correct, the response will be as follows:

Boot image OK

Hydra image OK

0>

If the boot firmware checksum is not correct, the message "Bad boot image -- use at own risk!" might be seen. The code that must be executed to generate this message is part of the boot firmware that is bad, so there is no guarantee that this message will be seen.

If the instrument firmware checksum is not correct, one of the following error messages may be seen:

Bad rom pointer	"Invalid pointer to checksum structure"
Bad checksum pointer	"Invalid pointer to instrument checksum"
Bad checksum	"Incorrect instrument checksum"

Invalid instrument firmware may be corrected by using a personal computer to load new instrument firmware into the Hydra Databucket. To do this see the section entitled "Updating the 2635A Instrument Firmware" in Section 4 of this manual.

If the NVRAM (A1U20 and A1U24) do not operate correctly, the problem must be corrected before new instrument firmware may be loaded or the instrument can power up completely. Use an oscilloscope to check the activity of the address, data, and control signals to the NVRAM devices (A1U14 and A1U16). It may be necessary to continually reset (power on) the instrument to check these lines, since the activity probably halts quickly when the instrument software goes awry. To check the NVRAM control signals, verify that A1U1-127 is going low, propogating through A1U26, and also appearing on pins A1U20-22 and A1U24-22 of the NVRAM devices. Verify that RDU* (A1U11-14 and A1U24-24) goes low when A1U1-127 is low. Verify that RDL* (A1U11-19 and A1U20-24) goes low when A1U1-127 is low. If all this is true, the problem is with the NVRAM itself or there is a fault in the address/data lines from the MC68302 Microprocessor. It may also be useful to check signal continuity by using a DMM with the instrument power off. Verify also that pin 30 on A1U24 and A1U20 is pulled up to approximately 5.0 volts dc by resistor A1R45.

Figure 5A-7 shows the timing relationships of the MC68302 Microprocessor address, data, and memory control signals used for memory read and write cycles. The chip selects from the Microprocessor (FLASH*, SRAM*, XMCARD*, and I/O*) are decoded internally from the address bus and the address strobe (AS*) signal. Therefore the AS* waveform is the same as the chip select signal for the device that the Microprocessor is accessing.

If the instrument powers up without any errors, but does not recognize front-panel button presses, the problem may be in the Keyboard Interrupt (KINT*) signal from the FPGA. If the KINT* output (A1U25-62) is low (and never goes high), the Microprocessor (A1U1) is failing to recognize the interrupt, or the microprocessor interface to A1U25 is not working correctly. Verify that the KINT* signal gets to the input pin (A1U1-121) on the Microprocessor.

If the interval time does not count down properly when scanning is enabled, the problem may be in the Real-Time Clock Interrupt (CINT*) signal from the Real-Time Clock (A1U12). If the CINT* output (A1U12-3) is low (and never goes high), the Microprocessor (A1U1) is failing to recognize the interrupt or the microprocessor interface to A1U12 is not working correctly. Verify that the CINT* signal gets to the input pin (A1U1-96) on the Microprocessor. Also verify that the Real-Time Clock is actively keeping time by checking for a 1-Hz square wave output on A1U12-4. Pin A1U12-2 must also be properly connected to GND for the Real-Time Clock to operate. The interface to the Microprocessor operates very much like the interface to NVRAM device A1U20.

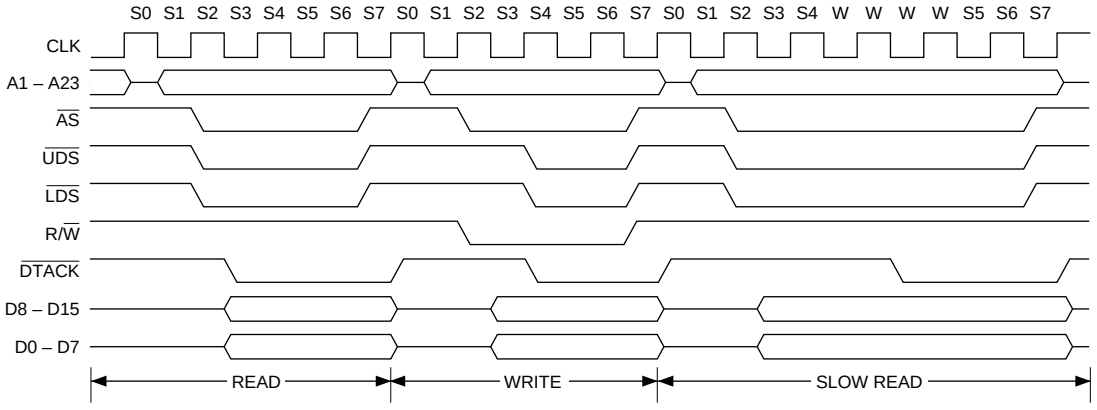
5A-15. Digital and Alarm Output Troubleshooting

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Since the structure of the eight Digital Outputs and four Alarm Outputs is very similar, the troubleshooting procedure presented here does not refer to specific device and pin numbers. First verify that the input of the Output Driver (A1U17 or A1U27) is low and that the output is near +5V dc. If the input is high, the problem may be in the FPGA (A1U25). If the output is not near +5V dc, use an ohmmeter to check the pull-up resistor in A1Z2.

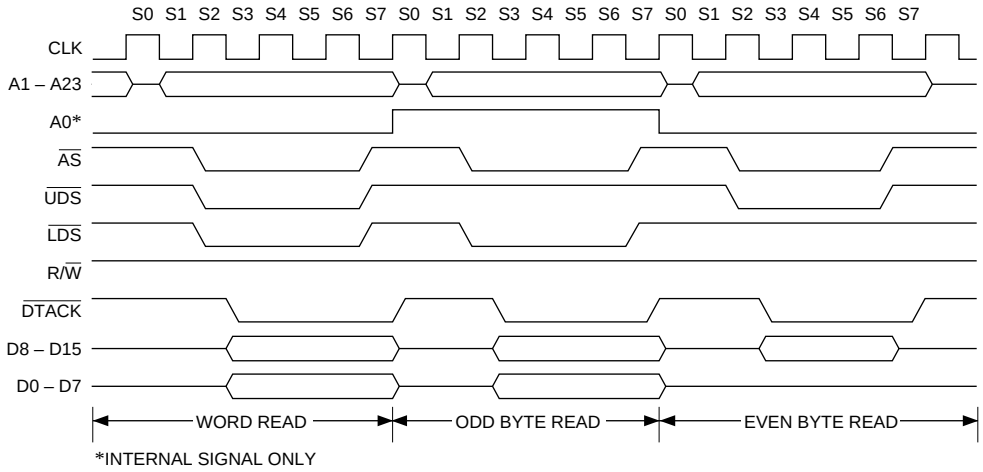
Use the proper computer interface command to change the state of the Digital Output (DO_LEVEL x,1) or Alarm Output (ALARM_DO_LEVEL x,1), where x is the number of the output being checked. Now verify that the input of the Output Driver is high and that the output is near +0.8V dc. If there is no change in the input, check the address signals to the FPGA (A1U25-85, A1U25-90, A1U25-96, A1U25-97) and the behavior of the output pin on the FPGA that goes to the input of the Output Driver (A1U17 or A1U27). If the output of the Output Driver fails to change when the input does, the problem is most likely the inverting output driver (A1U17 or A1U27).

5A-16. Digital Input Troubleshooting

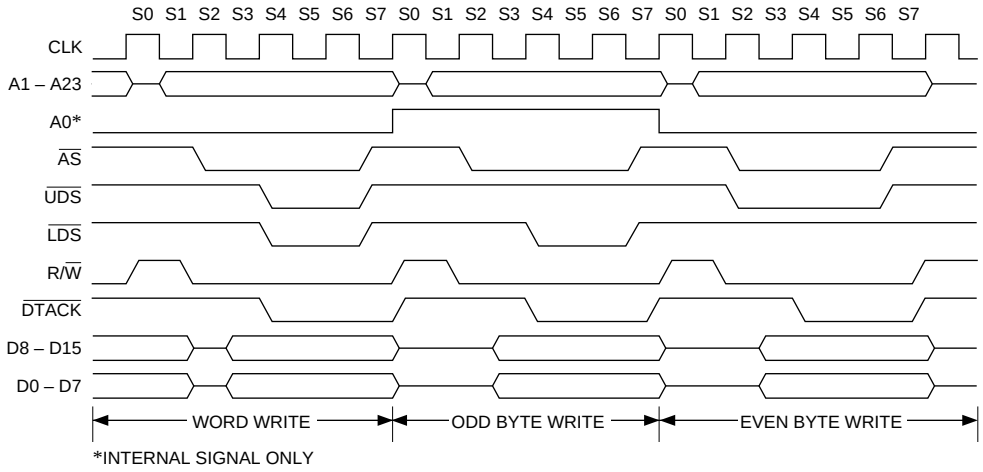
Power up Hydra while holding down the CANCL button to reset the instrument configuration. Verify that the Input Buffer Threshold circuit generates approximately 1.4V dc at A1TP18. Drive the Digital Input (A1J5) to be checked with a signal generator outputting a 100-Hz square wave that transitions from 0 to +5V dc. The signal generator output common should be connected to Common (A1J5-1). Verify that the output of the Input Buffer is a 100-Hz square wave that is the inverse of the input signal.



READ AND WRITE CYCLE TIMING DIAGRAM



WORD AND BYTE READ CYCLE TIMING DIAGRAM



WORD AND BYTE WRITE CYCLE TIMING DIAGRAM

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Figure 5A-7. Microprocessor Timing (2635A)

If the Input Buffer does not function correctly, the problem is probably A1Z1, A1Z3, or the associated comparator (A1U3 or A1U4). If the Input Buffer functions correctly, but Hydra is not able to read the state of the Digital Input correctly, the problem is most likely the FPGA (A1U25). If Hydra is not able to read the states of any of the eight Digital Inputs correctly, the problem is most likely in the address signals going to the FPGA (A1U25-85, A1U25-90, A1U25-96, A1U25-97).

5A-17. Totalizer Troubleshooting

Power up Hydra while holding down the CANCL button to reset the instrument configuration. Verify that the Input Buffer Threshold circuit generates approximately 1.4V dc at A1TP18. Drive the Totalizer Input (A1J5-2) with a signal generator outputting a 100-Hz square wave that transitions from 0 to +5V dc. The signal generator output common should be connected to Common (A1J5-1). Verify that the output of the Input Buffer (A1U8-1) is a 100-Hz square wave that is the inverse of the input signal. Verify also that the input to the totalizer counter (A1TP20) is a buffered form of the signal just verified at the output of the Input Buffer.

Use the following procedure to troubleshoot the totalizer input debouncer, Enable the totalizer debouncer by sending the TOTAL_DBNC 1 Computer Interface command to the instrument. With the signal generator still connected and outputting a 100-Hz square wave, verify that the waveform at the input to the totalizer counter (A1TP20) is delayed by 1.75 milliseconds from the waveform at A1U8-1.

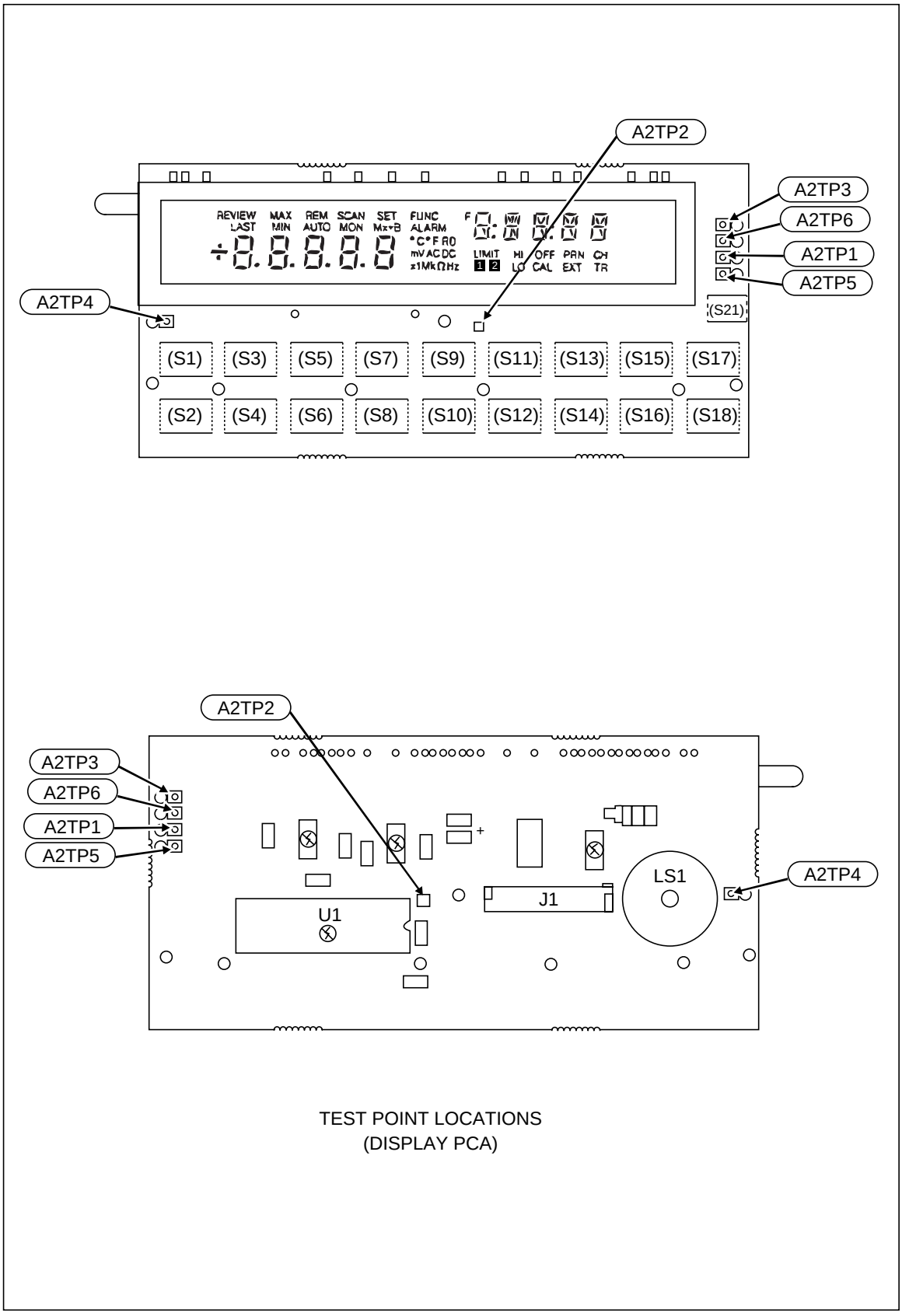
5A-18. Display Assembly Troubleshooting.

The following discussion is helpful if it has been determined that the Display Assembly is faulty. Refer to Figure 5A-8 for Display PCA test points. This initial determination may not be arrived at easily, since an improperly operating display may be the result of a hardware or software problem that is not a direct functional part of the Display Assembly. Consult the General Troubleshooting Procedures found earlier in this section for procedures to isolate the fault to the Display Assembly. Use the following discussion of display software operation when troubleshooting problems within a known faulty Display Assembly. A Display Extender Cable (PN 867952) is available for use during troubleshooting. Note that this cable must be twisted to mate correctly to the connectors on Display and Main PCAs.

The Display Controller reads the DTEST* and LTE* inputs to determine how to initialize the display memory. DTEST* (A2TP4) and LTE* (A2TP5) default to logic 1 and logic 0, respectively, to cause all display segments to be initialized to "on."Either test point can be jumpered to VCC (A2TP6) or GND (A2TP3) to select other display initialization patterns. Display Test Patterns #1 and #2 are a mixture of "on" and "off" segments with a recognizable pattern to aid in troubleshooting problems involving individual display segments. When either of the special display patterns is selected, the beeper is also sounded for testing without interaction with the Microprocessor. Table 5A-8 indicates the display initialization possibilities.

Figure 5A-9 shows the timing of communications between the Microprocessor and the Display Controller. Figures 5A-10 and 5A-11 show Display Test Patterns #1 and #2, respectively. Refer to the Display Assembly schematic diagram in Section 8 for information on grid and anode assignments.

When a Hydra display is initially powered up, all display segments should come on automatically. If this display does not appear, proceed with the following steps:



TEST POINT LOCATIONS
(DISPLAY PCA)

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Figure 5A-8. Test Points, Display PCA (A2) (2635A)

Table 5A-8. Display Initialization (2635A)

A2TP4 DTEST*	A2TP5 LTE*	POWER-UP DISPLAY INITIALIZATION
1	1	All Segments OFF
1	0	All Segments ON (default)
0	1	Display Test Pattern #1
0	0	Display Test Pattern #2

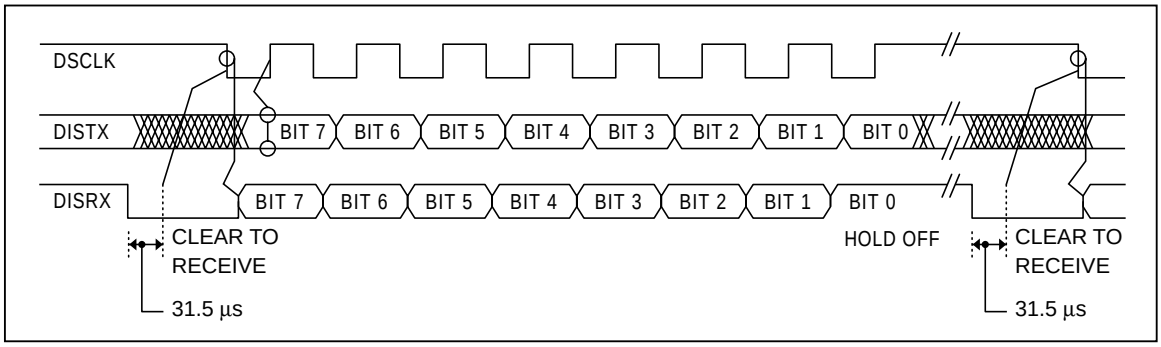


Figure 5A-9. Display Controller to Microprocessor Signals (2635A)

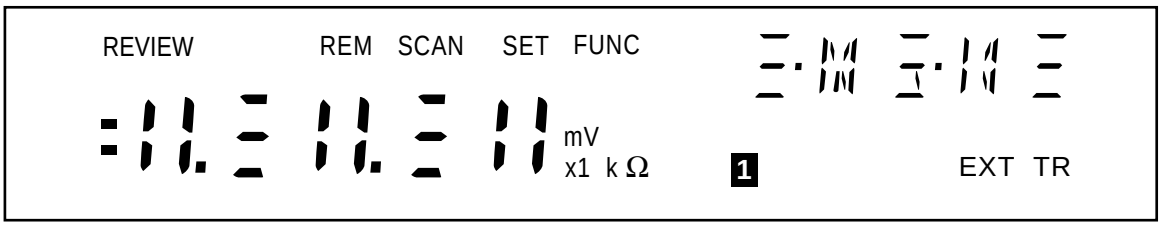


Figure 5A-10. Display Test Pattern #1 (2635A)

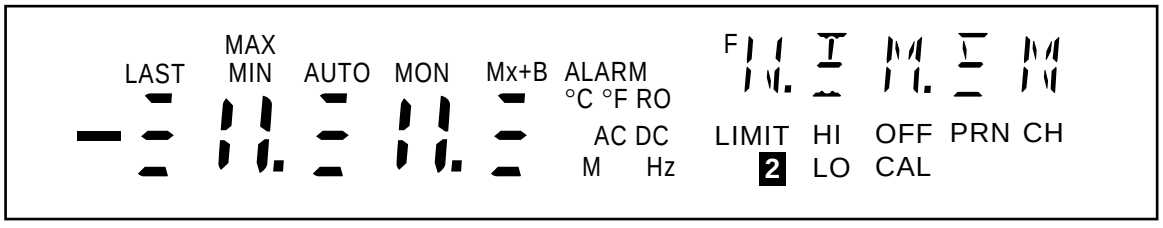


Figure 5A-11. Display Test Pattern #2 (2635A)

Note

If the display is operational but has problems whenfront-panel buttons are pressed, proceed directlyto step 9.

1. Check the three power supplies with respect to GND (A2TP3 or A2U1-42) on the Display Assembly.

VCC (A2U1-21)	4.75 to 5.25V dc
VEE (A2U1-4)	-4.75 to -5.25V dc
VLOAD A2U1-5)	-28.5 to -32.0V dc

2. Check the filament drive signals FIL1 and FIL2; these connect to the last two pins on each end of A2DS1. These signals should be 5.4V ac with FIL2 biased to be about 6.8V dc higher than the VLOAD supply (nominally a -23.2V dc level). FIL1 and FIL2 should be 180 degrees out of phase. If the dc bias of FIL2 is not at about -23.2V dc, the display segments that should be "off" will show a shadowing (or speckling) effect.
3. Check the clock signal CLK1 at A2TP2, A2U1-2, and A2U4-3. This signal should be a 512-kHz square wave (1.953 microseconds per cycle). This signal depends on an E clock signal (also known as DCLK) of 1.024 MHz from the Main Assembly. If the E clock is not correct, the problem may be in A1U25 or in the ribbon cable system connecting the two assemblies.
4. Check the state of the RESET signal (A2U1-1). This signal should be low once the reset time is completed (after power-up). Also verify that the RESET* signal (A2U6-3) is high after the reset time is completed.
5. Verify that the DISRX signal (A2U1-39) goes low after RESET (A2U1-1) goes low. If this sequence does not occur, communication to the Microprocessor is held off with the DISRX signal high. If DISRX stays high but is not shorted to VCC, A2U1 must be faulty.
6. Verify activity for both the DISTX and DSCLK signals. These signals are driven by the Microprocessor and must be transitioning for the Display Controller to receive commands from the Microprocessor.
7. If all segments of a particular digit do not turn on at power-up, the grid drive from A2U1 may not be connected properly to A2DS1. Grids are numbered from 10 to 0 (left to right as the display is viewed). For a digit to be enabled, the respective grid drive signals (GRID(10:0)) must be at approximately VCC (4.75 to 5.25V dc.) For a digit to be disabled, the drive must be at VLOAD (-28.5 to -32.0V dc.)
8. If a segment under each of several (or all) grids fails to be turned on (or off) properly, one of the anode drive signals may not be connected properly from A2U1 to A2DS1. When an anode signal is at VCC, and a grid signal is at VCC, the corresponding segment on the display is illuminated.
9. If the Microprocessor has difficulty recognizing front-panel button presses, the switch scanning signals SWR1 through SWR6 should be checked (A1U25-67, A1U25-68, A1U25-71, A1U25-73, A1U25-70, and A1U25-69 respectively). When no switch contacts are being closed, the switch scanning lines should have about 20-kΩ of resistance between each other (through two 10-kΩ pullup resistors to VCC). Unless one of the switches is closed, none of the switch scanning lines should be shorted directly to GND at any time.

5A-19. Variations in the Display

Under normal operation, the display presents various combinations of brightly and dimly lit annunciators and digits. However, you may encounter other, random irregularities across different areas of the display under the following circumstances:

- After prolonged periods of displaying the same information.
- If the display has not been used for a prolonged period.

This phenomenon can be cleared by activating the entire display and leaving it on overnight (or at least for several hours). Use the following procedure to keep the display fully lit:

1. With power OFF, press and hold SHIFT, then press power ON.

2. Wait a moment for the instrument to beep, then release SHIFT. The entire display will now stay on until you are ready to deactivate it.
3. At the end of the activation period, press any button on the front panel; the instrument resumes the mode in effect prior to the power interruption (Active or Inactive.)

5A-20. Calibration Failures

5A-21. Introduction

Calibration of Hydra through the computer interface is described in Section 4 of this manual. Generally, a calibration failure is indicated by a Device Dependent Error and a "!>" prompt after a CAL_STEP? command if the RS-232 interface is being used. This occurs if the analog input varies from what the instrument expects to see by more than ±5% or ±15%, depending on the calibration step.

Before suspecting a fault with Hydra, verify that the calibration is being conducted properly.

- Check the connections between the source and the instrument. Are allthe connections in place?
- Check the output of the calibration source. Does it equal the valuecalled for by this calibration step?
- Check the calibration source. Is it in operate mode? Has it revertedto standby?

If a calibration step has failed, Hydra remains on that step so that the output from the calibration source may be corrected or the calibration reference value (CAL_REF) being used by Hydra may be changed if it was improperly entered. The calibration step may be repeated by sending the CAL_STEP? command to Hydra again.

Calibration of Hydra utilizes a simple "calibration by function" approach. If you suspect calibration errors, but the instrument does not exhibit the symptoms mentioned above, verify that you are observing the following calibration rules:

- Independent calibration of any function results in the storage ofcalibration constants for that function only.
- Once calibration is begun, all steps for that function must becompleted before the calibration constants are stored. If all stepsare not completed and the procedure is terminated, no constants forthat function are stored; only calibration constants for previouslycompleted functions are stored.

5A-22. Calibration-Related Components

If the calibration setup is correct, a faulty component within Hydra may be causing the failure. Each measurement function depends on a combination of components in and around the Analog Measurement Processor (A3U8).

RMS Converter	A3U6
AC Buffer	A3U7
Zener Reference	A3VR1
Divider Network (DC/Ohms)	A3Z4
Integrate Resistors, Reference Divider	A3Z2
AC Divider Network	A3Z3
RMS Converter Network	A3Z1

Basic dc measurements depend on the zener reference (A3VR1), reference divider network (A3Z2), and integrate resistors (A3Z2). Resistance measurements and dc measurements above three volts additionally depend on the resistors in the dc divider network (A3Z4). AC measurements depend on the ac divider network (A3Z3), ac buffer (A3U7), and RMS converter (A3U6), as well as the basic dc measurement components.

Note

During calibration, the measurement rateis selected automatically as required by thecalibration step.

Table 5A-9 may be useful in isolating a calibration problem to specific components.

Table 5A-9. Calibration Faults (for software versions 5.4 and above) (2635A)

Input	Range	Calibration Constant		Related Components
		Number	Acceptable Values	
DC Volts				
0.09000V	100 mV	1	1.0315 to 1.1565	A3VR1, A3Z2
0.9000V	1V	2	1.0340 to 1.1540	A3VR1, A3Z2
0.29000V	300 mV	3	1.0315 to 1.1565	A3VR1, A3Z2
2.9000V	3V	4	1.0315 to 1.1565	A3VR1, A3Z2
29.000V	30V	5	1.0340 to 1.1640	A3VR1, A3Z2, A3Z4
290.00V	300V	6	1.0290 to 1.1590	A3VR1, A3Z2, A3Z4
AC Volts (1 kHz)				
0.02900V	300 mV	7	-0.001 to 0.001	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.29000V	300 mV	8	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
0.2900V	3V	9	-0.01 to 0.01	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.9000V	3V	10	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
2.900V	30V	11	-0.1 to 0.1	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.000V	30V	12	1.0040 to 1.1840	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
29.00V	300V	13	-1.0 to 1.0	A3U6, A3VR1, A3Z1, A3Z2, A3Z3
290.00V	300V	14	1.0040 to 1.1840	
Ohms				
290.00Ω	300Ω	15	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 kΩ	3 kΩ	16	0.9975 to 1.0125	A3Z2, A3Z4
29.000 kΩ	30 kΩ	17	1.0015 to 1.0165	A3Z2, A3Z4
290.00 kΩ	300 kΩ	18	0.9965 to 1.0115	A3Z2, A3Z4
2.9000 MΩ	3 MΩ	19	0.9990 to 1.0090	A3Z2, A3Z4
2.9000 MΩ	10 MΩ	20	0.9990 to 1.0090	A3Z2, A3Z4
Frequency				
10.000 kHz 2.9V rms		21	0.9995 to 1.00050005	A3Y2

5A-23. Retrieving Calibration Constants

If a calibration error is suspected, the stored constant can be retrieved and verified over the computer interface. Acceptable calibration constants for each function and range are listed in Table 5A-9. Retrieve the constant with the following command:

CAL_CONST? xx (where xx denotes the calibration constant number)

The entire calibration of the Hydra Databucket can be retrieved from the instrument in tabular form by using the following command:

EEM_LIST?

The instrument response from this command shows the currently used FLASH memory block and page numbers, and each calibration constant in hexadecimal and floating point with a description of what function and range each calibration constant is used on. The following is a sample of a typical EEM_LIST? response:

```
Page 10 of Parameter Block 1 is currently in use.
Register  Hex Value  F.P. Value         Description
-----------------------------------------------------------------
0-1   0x3F8A847A1.   0821679100         Millivolt DC Gain
2-3   0x3F8A5D751.   08097711           Volt DC Gain
4-5   0x3F8A63571.   0811566300         Millivolt DC Gain
6-7   0x3F8A5BC01.   08092503           Volt DC Gain
8-9   0x3F8B4F571.   088358830          Volt DC Gain
10-11 0x3F8A7C8A1.   0819256150/300     Volt DC Gain
12-13 0xB8F20A00     -0.0001154300      Millivolt AC Offset
14-15 0x3F8A51191.   0805999300         Millivolt AC Gain
16-17 0xBA974800     -0.00115423        Volt AC Offset
18-19 0x3F8A7F291.   08200563           Volt AC Gain
20-21 0xBC3A6C00     -0.011378330       Volt AC Offset
22-23 0x3F8A863A1.   082221330          Volt AC Gain
24-25 0xBDE81400     -0.1133194150/300  Volt AC Offset
26-27 0x3F8AC8861.   0842445150/300     Volt AC Gain
28-29 0x3F808EAB1.   0043539            300 Ohm Gain
30-31 0x3F8097591.   0046188            3 Kilo Ohm Gain
32-33 0x3F80FD781.   0077353            30 Kilo Ohm Gain
34-35 0x3F7FF46C0.   9998233            300 Kilo Ohm Gain
36-37 0x3F7FFDD00.   9999666            3 Mega Ohm Gain
38-39 0x3F7FFDD00.   9999666            10/30 Mega Ohm Gain
40-41 0x3F80073D1.   0002209            Frequency Gain
42    0x000F                           Calibration Status
43-44 0xAAAAAAAA                       Product Serial Number
45    0xFFFF                           Unused EEM Register #1
46    0xFFFF                           Unused EEM Register #2
47    0xFFFF                           Unused EEM Register #3
48    0x62F4                           CRC of EEM Data (0x62F4)
```

5A-24. Replacing the Flash Memory (A1U14 and A1U16)

The FLASH Memory provides nonvolatile storage for the instrument serial number, the instrument firmware, and all calibration information. If the "boot" firmware in FLASH memory has been determined to be faulty, A1U14 and A1U16 must both be replaced. Many other problems may be corrected by loading new instrument firmware in the instrument (see the section entitled "Updating the 2635A Instrument Firmware" in Section 4 of this manual), or recalibrating the instrument.

If the FLASH Memories must be replaced during repair, the instrument must be recalibrated. The new FLASH Memory can be programmed with the 7-digit serial number found on the rear panel of the instrument or any 7-digit identifier of your choosing. Note that the serial number is not programmed prior to shipment from the factory.

The following command may be used to program the serial number into the FLASH Memory:

SERIAL XXXXXXX (xxxxxxx denotes the 7-digit number. Leading zeros must be entered. Note: once entered, the number cannot be changed.)

The serial number of the instrument can be accessed by using the “SERIAL?” command. The response will be “0”)if the serial number has not yet been set) or the 7-digit serial number.

5A-25. Memory Card I/F PCA (A6) Troubleshooting.

5A-26. Power-Up Problems

The following discussion identifies probable fault areas if the installation of a Memory Card I/F PCA causes power-up failure for the instrument. The problem is probably a short on A6P2; the Microprocessor on the Main Assembly is prevented from accessing Flash Memory and NVRAM correctly. Make the following checks:

- First check for a GND-to-VCC short on the Memory Card I/F PCA.
- There may also be a short between an interface signal and VCC, GND, or another interface signal. Check signals D8 .. D15, A1 .. A4, XRDU*, XWRU*, MCARD*, XSCLK, DTACK*, MCINT*, and RESET*.
- The short may be due to a CMOS input that has been damaged due to static discharge; the short is then detectable only when the circuit is powered up. Use an oscilloscope to check activity on each of the interface signals. Verify that signals are able to transition normally between 0 and 5.0V dc (VCC).

5A-27. Failure to Detect Memory Card I/F PCA

Proper detection of the Memory Card Interface depends on the FPGA (A6U1) being properly configured at power-up. Proper FPGA configuration is indicated by a low to high transition on A6U1-80 shortly after power-up. Normally A6U1-80 should be high before RESET* (A6U1-78) goes high. If the Memory Card Interface is not installed properly, an "ERROR d" is displayed by the Microprocessor during power-up. The Microprocessor checks for the presence of the Memory Card Interface by attempting to read one of the registers in the Memory Card Controller (A6U1). If A6U1-58 fails to drive the DTACK* signal low during the read access, the Microprocessor will abort the memory cycle and report the Memory Card Interface as being not installed.

Verify the RESET*, XMCARD*, XRDU*, XSCLK, and DTACK* signals on the Memory Card Interface. RESET* (A6U1-78) must be high. Using a storage oscilloscope, verify that DTACK* (A6U1-58) goes low while XMCARD* (A6U1-49) is low for the first read memory cycle to the Memory Card Controller (A6U1) during instrument power-up. It may be necessary to cycle the power on the instrument several times to verify this operation.

5A-28. Failure to Detect Insertion of Memory Card

When a Memory Card is inserted into the Memory Card Interface, the card detect signals (CD1 and CD2; A6U1-19 and A6U1-21) are driven low. Verify that the Memory Card Controller detects this and interrupts the Microprocessor (A1U1) by driving the MCINT* signal (A6U1-60) low. Failure to generate the interrupt may be due to problems with the data bus (D8..D15), the address bus (A1..A4), or one of the control signals (XSCLK, XMCARD*, XWRU*, XRDU*, and RESET*). Consult the schematics found in Section 8 of this manual and verify these interconnections. Consider the ribbon cable that connects the Main Assembly (A1) to the Memory Card Interface Assembly (A6) as a possible source of the problem as well. It may be necessary to repeatedly insert and remove the card to observe the behavior of these signals.

5A-29. Failure to Power Card / Illuminate the Busy Led

When a Memory Card is properly inserted and then detected by the Microprocessor (A1U1), the Memory Card should be powered up and the BUSY LED should be illuminated for a short period of time. If the BUSY LED is not visibly illuminated when the card is inserted, verify the following things using a storage oscilloscope. Verify that the gate of transistor A6Q1 is driven low by A6U1-26 (check both ends of resistor A6R13). When the gate of A6Q1 is near 0 volts dc, the drain of transistor (A6Q1-5 through A6Q1-8) should be near 5 volts dc.

Approximately 50 milliseconds after the transistor drain pins (A6Q1-5 through A6Q1-8) go to about 5 volts dc, the BUSY LED should be turned on by A6U1-25 going low to sink current through the LED (A6DS1) and current limiting resistor (A6R10). When the Microprocessor (A1U1) is done accessing data on the memory card, A6U1-25 and A6U1-26 will both go high again to turn off the BUSY LED and the card power supply. If the 50 millisecond delay between the memory card power being turned on and the BUSY LED being turned on may be extended up to a total of 250 milliseconds if the RDY/BSY signal (A6U1-23) is being held low by the memory card.

5A-30. Failure to Illuminate the Battery Led

The yellow BATTERY LED is controlled by a Memory Card Controller output (A6U1-24). The Microprocessor checks the BVD1 and BVD2 outputs (A6U1-18 and A6U1-20 respectively) from the memory card about 50 milliseconds after it is powered up. The BATTERY LED is turned on by A6U1-24 going low to sink current through the LED (A6DS2) and current limiting resistor (A6R11).

Verify that the BATTERY LED state matches the state of the BVD1 and BVD2 signals as shown in the following table (H = 5 volts dc, L = 0 volts dc).

Battery LED	BVD1	BVD2
Off	H	H
On	H	L
On	L	H
On	L	L

5A-31. Failure to Write to Memory Card

The installed memory card controls the state of the write protect (WP) signal that is an input to the Memory Card Controller (A6U1-22). This signal must be near 0 volts dc when the memory card is powered up and any operation requiring write access to the memory card is done. Verify that the state of the WP signal (A6U1-22) correctly follows the state of the write protect switch on the memory card as indicated in the following table (H = 5 volts dc, L = 0 volts dc).

Write Protect	WP (A6U1-22)
Enabled	L
Disabled	H

If the problem with the interface has not been isolated yet, the problem is probably in the card address (CA<0> .. CA<25>, REG*), card data (CD<0> .. CD<7>), and control signals (CE1*, CRD*, CWR*). The card data (CD<0> .. CD<7>) signals each go through a series termination resistor (Z2) so verify these series resistances. The control signals (CE1*, CRD*, CWR*) each go from the Memory Card Controller (A6U1) through an analog switch (A6U2) as they go to the Memory Card Connector (A6P1), so verify that each control signal functions properly. The card read (CRD*) and card write (CWR*) signals must go low for read and write cycles respectively. The following table describes the memory card access modes to "attribute" memory (only read accesses are done by the instrument).

Memory Card Access Modes

Transfer Mode	REG*	CE1*	CRD*	CWR*	Data Direction
No Operation	x	H	H	H	
Attribute Byte Read	L	L	L	H	CD->D
Common Byte Read	H	L	L	H	CD->D
Common Byte Write	H	L	H	L	D->CD

5A-32. Write/Read Memory Card Test (Destructive)

The instrument has a special computer interface command that may be used gain diagnostic information about what is failing to function correctly in the Memory Card Interface.

⚠ Warning

Use of the following command will destroy any data stored on the memory card that is installed in the instrument. After completion of the troubleshooting and repair of the memory card interface, the memory card used must be formatted again before it may be used again for data storage.

To make use of this command, connect a terminal or computer to the RS-232 interface and set the instrument communication parameters as follows:

- Press SHIFT and then LIST(COMM).
- With 'BAUd' displayed, use the UP or DOWN arrow key to select the desired baud rate. Then press ENTER.
- With 'PAR' (parity) displayed, use the UP or DOWN arrow key to select the parity. Then press ENTER.

- With 'CtS' (Clear to Send) displayed, use the UP or DOWN arrow key to select 'OFF'. Then press ENTER.
- With 'ECHO' displayed, use the UP or DOWN arrow key to select 'ON'. Then press ENTER. Communications setup for Hydra is now complete.

Assuming that the RS-232 interface is functional, send a carriage return or line feed character to the instrument and it should send back a prompt. With a Static RAM memory card installed in the instrument, send the following command followed by a carriage return or line feed:

MCARD_DESTRUCTIVE_TEST? <size> where the <size> parameter is the number of kbytes (1024 bytes) of the card to test. Use <size> = 256 for a 256 kbyte card and <size> = 1024 for a 1 Mbyte card.<end>

This command writes data to the memory card and then reads and compares the data to the pattern that was written. A maximum of twenty lines of output will be generated, but all locations on the card are sequentially written and then read. The messages output by this command are summarized below:

```
MEMORY CARD IS NOT INSERTED!
```

The Memory Card Controller doesn't recognize that the memory card is inserted in connector A6P1. Verify that A6U1-19 and A6U1-21 are both near 0 volts dc.

```
MEMORY CARD IS WRITE PROTECTED!
```

The Memory Card Controller is indicating that the memory card is write protected. Verify that the switch on the rear edge of the memory card is in the proper position and that A6U1-22 is near 0 volts dc when the memory card is powered up.

```
MEMORY CARD TEST PASSED.
```

The memory card test passed without detecting any errors.

```
ADDRESS 0x000000: DATA WAS 0x14, EXPECTED 0xC9
ADDRESS 0x000001: DATA WAS 0x3D, EXPECTED 0x2D
ADDRESS 0x000002: DATA WAS 0xAB, EXPECTED 0xBD
```

These are typical errors indicating in hexadecimal the address, the data that was read from the card and the data that was expected. It may be possible to get some indication of which address or data signals to probe with an oscilloscope to determine where the fault is.

When probing signals to detect activity, it may be useful to change the <size> parameter to be 16384 so that it will attempt to test the card as if it is a 16 Mbyte memory card. This guarantees that error messages will be output, but it will take longer to complete the test thus allowing more time to probe signals before having to send the memory card test command again.

Chapter 6
List of Replaceable Parts

Title **Page**

6-1. Introduction

This section contains an illustrated list of replaceable parts for the 2620A, 2625A, and 2635A. Parts are listed by assembly; alphabetized by reference designator. Each assembly is accompanied by an illustration showing the location of each part and its reference designator. The parts lists give the following information:

- Reference designator
- An indication if the part is subject to damage by static discharge
- Description
- Fluke stock number
- Total quantity
- Any special notes (i.e., factory-selected part)

Caution

A * symbol indicates a device that may be damaged by static discharge.

6-2. How to Obtain Parts

Electrical components may be ordered directly from the manufacturer by using the manufacturers part number, or from the Fluke Corporation and its authorized representatives by using the part number under the heading FLUKE STOCK NO. In the U.S., order directly from the Fluke Parts Dept. by calling 1-800-526-4731. Parts price information is available from the Fluke Corporation or its representatives. Prices are also available in a Fluke Replacement Parts Catalog which is available on request.

In the event that the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions, if necessary.

To ensure prompt delivery of the correct part, include the following information when you place an order:

- Part number and revision level of the pca containing the part.
- Reference designator
- Fluke stock number
- Description (as given under the DESCRIPTION heading)
- Quantity
- Instrument Model, Serial Number, and Firmware Numbers

Note

*Instrument Firmware Numbers can be retrieved over the computer interface using the *IDN? query. Refer to Section 4 of the Hydra Users Manual for more information.*

6-3. Manual Status Information

The Manual Status Information table that precedes the parts list defines the assembly revision levels that are documented in the manual. Revision levels are printed on the component side of each pca.

6-4. Newer Instruments

Changes and improvements made to the instrument are identified by incrementing the revision letter marked on the affected pca. These changes are documented on a manual supplement which, when applicable, is included with the manual.

6-5. Service Centers

To locate an authorized service center, call Fluke using any of the phone numbers listed below, or visit us on the World Wide Web: www.fluke.com

1-800-443-5853 in U.S.A and Canada

31 40 267 8200 in Europe

206-356-5500 from other countries

6-6.

Note

This instrument may contain a Nickel-Cadmium battery. Do not mix with the solid waste stream. Spent batteries should be disposed of by a qualified recycler or hazardous materials handler. Contact your authorized Fluke service center for recycling information.

⚠ Warning

This instrument contains two fusible resistors (pn 650085). To ensure safety, use exact replacement only.

Manual Status Information

Ref. or Option No.	Assembly Name	Fluke Part No.	Revision
A1	2620A/2625A Main PCA	814186	F
A1	2635A Main PCA	925669	C
A2	Display PCA	814194	-
A3	A/D Converter PCA	814202	K
A4	Analog Input PCA	814210	C
A5	IEEE-488 Interface PCA	872593	A
A6	2625A Memory PCA	886135	A
A6	2635A Memory Card I/F PCA	931977	B

Table 6-1. 2620A/2625A Final Assembly

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
A1		MAIN PCA	814186	1	
A2		DISPLAY PCA	814914	1	
A3		A/D CONVERTER PCA	814202	1	
A4		ANALOG INPUT PCA	814210	1	
A5		IEEE-488 INTERFACE PCA	872593	1	1
A6		MEMORY PCA	886135	1	
F1,2	⚠	FUSE,5X20MM,0.125A,250V,SLOW	822254	2	6
H50		SCREW,FH,P,LOCK,STL,8-32,.375	114116	2	
H51		SCREW,PH,P,LOCK,SS,6-32,.375	334458	2	
H52		SCREW,PH,P,LOCK,STL,6-32,.250	152140	7	
H53		SCREW,FHU,P,LOCK,SS,6-32,.250	320093	4	
H54		SCREW,TH,P,SS,4-40,.187	721118	2	
H65		SCREW,KNURL,SL,CAPT,STL,6-32,.500	876479	2	
H70		NUT,HEX,STL,6-32	110551	4	
MP1		BEZEL,REAR, GRAY #8.	874081	1	
MP2		ISOTHERMAL CASE,BOTTOM	874107	1	
MP3		ISOTHERMAL CASE,TOP	874110	1	
MP4		SEAL,CALIBRATION	735274	1	
MP5		DECAL,REAR PANEL	874128	1	
MP6		ROD,POWER SWITCH	784827	1	
MP7		LABEL, CE MARK, SILVER	600715	1	
MP10		CHASSIS ASSY	871561	1	
MP11		FRONT PANEL	795062	1	
MP12		ELASTOMERIC KEYPAD	795070	1	
MP13		CASE FOOT,BLACK	824433	2	
MP14		HANDLE, PAINTED GRAY #8	949511	1	
MP15		LENS, FRONT PANEL	784777	1	
MP16		MOUNTING PLATE,HANDLE (LEFT)	884267	1	
MP17		MOUNTING PLATE,HANDLE (RIGHT)	884270	1	
MP18		CASE,OUTER	884262	1	
MP20		COVER,IEEE	885983	1	
MP22		PWR PLUG,PANEL,6.3A,250V,3 WIRE	780817	1	
MP25		DECAL,ISOTHERMAL CASE	874131	1	
MP26		NAMEPLATE	877845	1	2
MP35		DECAL, CSA	864470	1	
MP43		TEST LEAD ASSY, TL70A	855820	1	
MP47		PWR PLUG PART,FUSE HOLDER	780825	1	
MP48		CONN ACC,D-SUB,FEMALE SCREWLOCK,.250	844704	2	
MP59		DECAL, NAMEPLATE	784736	1	3
MP66		TERM STRIP,SOCKET,.197CTR,8 POS	875877	1	
MP67		TERM STRIP,SOCKET,.197CTR,10 POS	875880	1	

Table 6-1. 2620A/2625A Final Assembly (cont)

Reference Designator	Description	Fluke Stock No	Tot Qty	Notes
MP80	HYDRA STARTER SOFTWARE	890645	1	
MP99	T/C CABLE,ASSY	871512	1	
MP101	LABEL,VINYL,1.500,.312	844712	4	
T1	TRANSFORMER,POWER,100-240V	931105	1	
TM1	HYDRA MANUAL SET (ENGLISH)	886015	1	4
TM2	HYDRA (STARTERS PKG) APPLICATION SOFTWA	890632	1	
TM3	HYDRA & DATA BUCKETSERVICE MANUAL	202231	0	5
TM4	HYDRA DATA LOGGER MANUAL	891457	0	5
TM5	HYDRA USERS MANUAL (GERMAN)	919220	0	5
TM6	HYDRA USERS MANUAL (FRENCH)	885991	0	5
W1	WIRE ASSY,GROUND	874099	1	
W2	CABLE ASSY,FLAT,20 COND,MMOD,FERRITE	876185	1	
W4	CORD,LINE,5-15/IEC,3-18AWG,SVT,7.5 FT	284174	1	

1. THIS IS AN OPTION ONLY. NOT AVAILABLE FOR THE 2625A
2. USED ON THE 2620A ONLY.
3. USED ON THE 2625A ONLY.
4. INCLUDES: HYDRA USERS MANUAL (885988), AND HYDRA QUICK SETUP CARD (895883).
5. AVAILABLE THROUGH PARTS DEPARTMENT.

⚠ TO ENSURE SAFETY, USE EXACT REPLACEMENT ONLY.

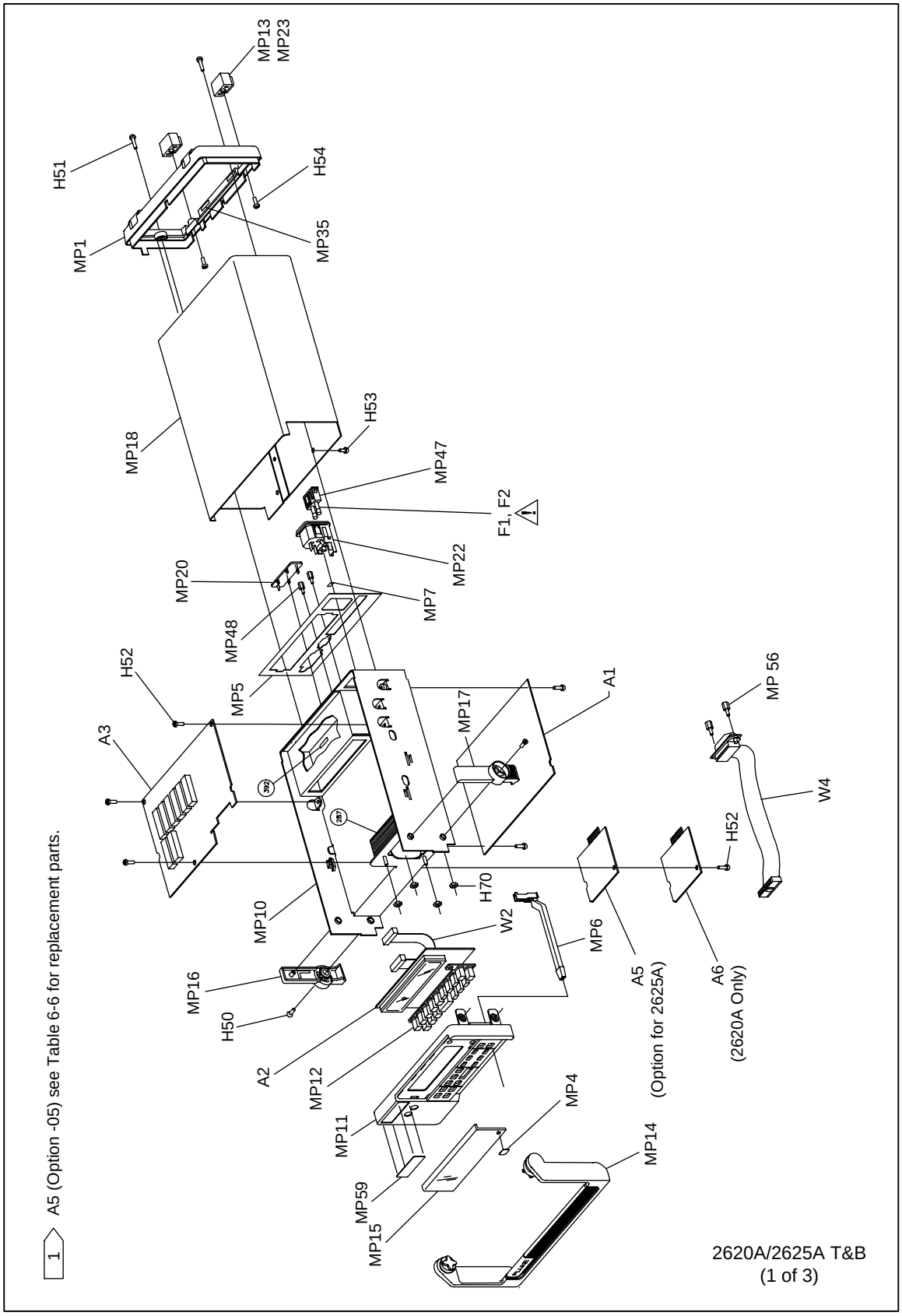
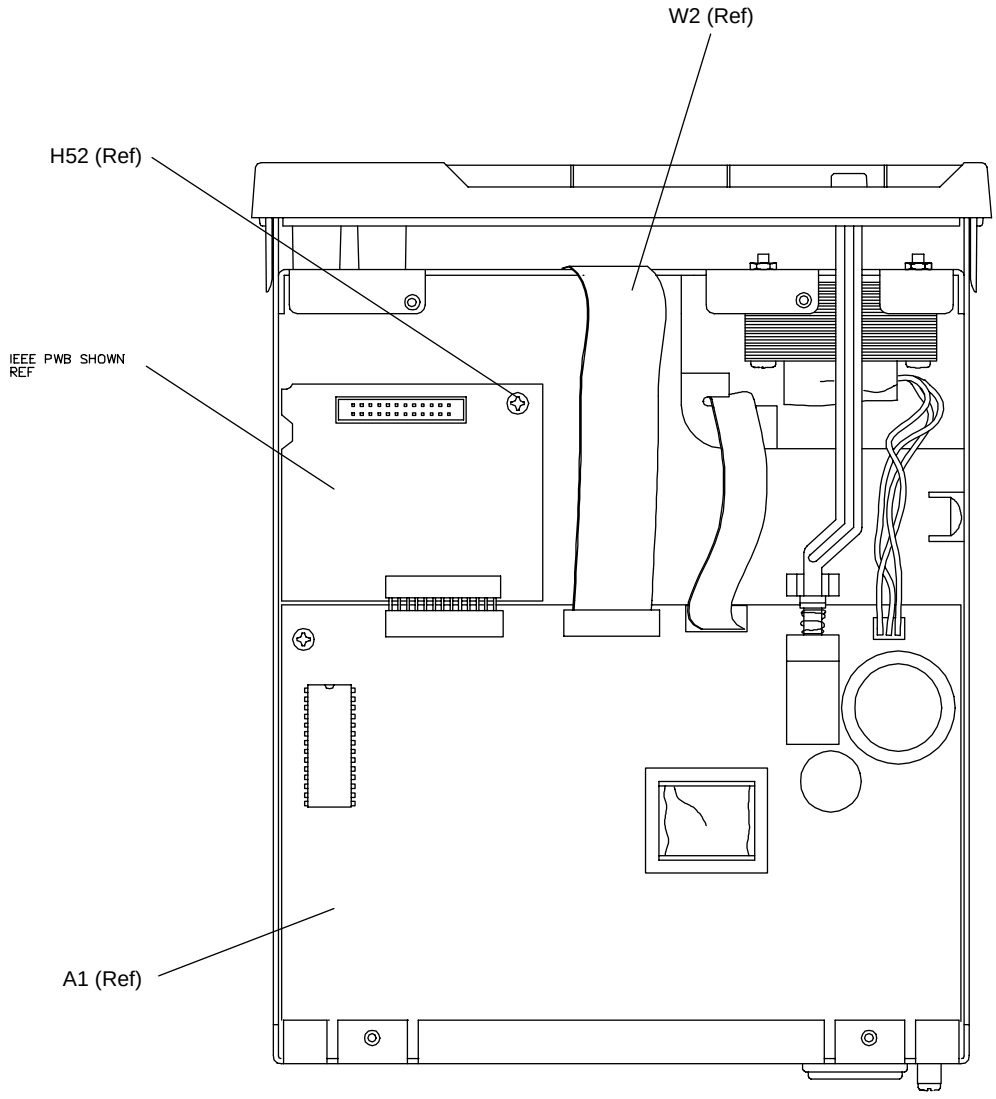


Figure 6-1. 2620A/2625A Final Assembly



Bottom View

2620A/2625A T&B
(2 of 3)

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Figure 6-1. 2620A/2625A Final Assembly (cont)

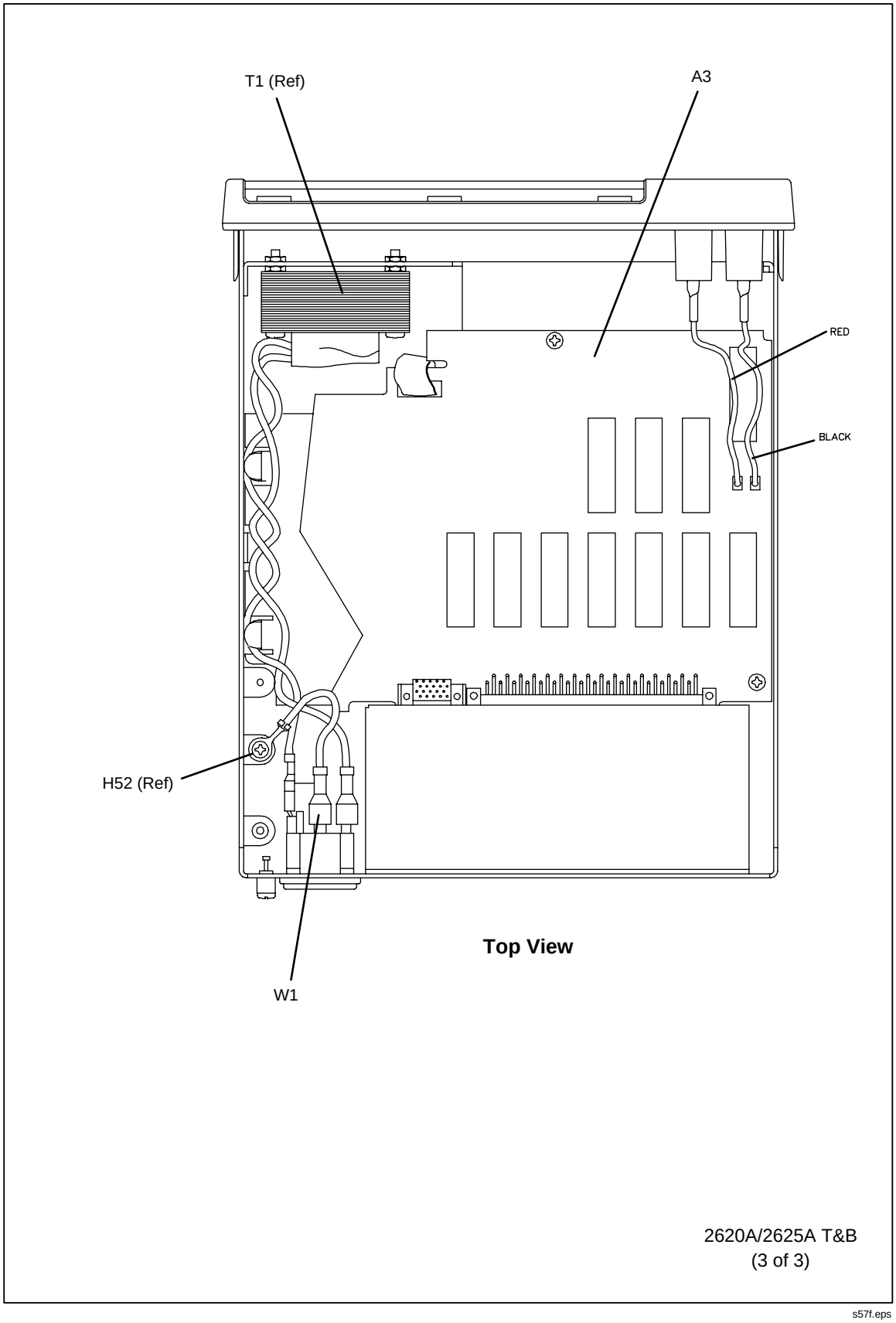

Figure 6-1. 2620A/2625A Final Assembly (cont)

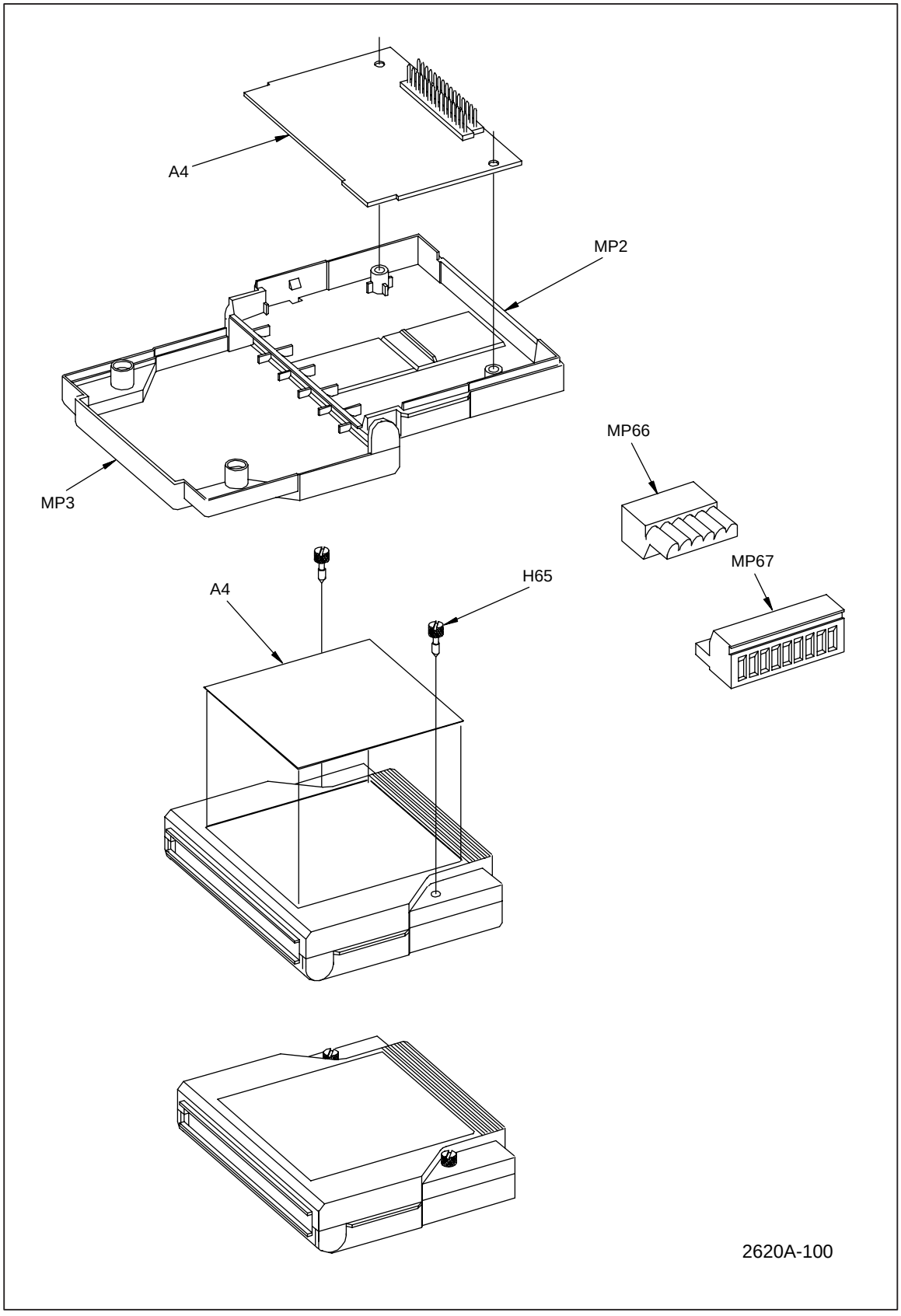

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Figure 6-1. 2620A/2625A Final Assembly (cont)

Table 6-2. 2635A Final Assembly

Reference Designator	Description	Fluke Stock No	Tot Qty	Notes
A1	MAIN PCA	925669	1	
A2	DISPLAY PCA	814194	1	
A3	A/C CONVERTER PCA	814202	1	
A4	ANALOG INPUT PCA	814210	1	
A6	MEMORY CARD I/F PCA	931977	1	
F1,2	⚠ FUSE,5X20MM,0.125A,250V,SLOW	822254	2	4
H50	SCREW,FH,P,LOCK,STL,8-32,.375	114116	2	
H51	SCREW,PH,P,LOCK,SS,6-32,.375	334458	2	
H52	SCREW,PH,P,LOCK,STL,6-32,.250	152140	8	
H53	SCREW,FHU,P,LOCK,SS,6-32,.250	320093	4	
H54	SCREW,TH,P,SS,4-40,.187	721118	2	
H65	SCREW,KNURL,SL,CAPT,STL,6-32,.500	876479	2	
H70	NUT,HEX,STL,6-32	110551	4	
MP1	BEZEL,REAR, GRAY #8.	874081	1	
MP2	ISOTHERMAL CASE,BOTTOM	874107	1	
MP3	ISOTHERMAL CASE,TOP	874110	1	
MP4	SEAL,CALIBRATION	735274	1	
MP5	DECAL,REAR PANEL	874128	1	
MP6	ROD,POWER SWITCH	784827	1	
MP10	CHASSIS ASSY	871561	1	
MP7	LABEL, CE MARK, SILVER	600715	1	
MP11	PANEL,FRONT	932058	1	
MP12	KEYPAD,ELASTOMERIC	932066	1	
MP13	CASE FOOT,BLACK	824433	2	
MP14	HANDLE, PAINTED GRAY #8	949511	1	
MP15	LENS, FRONT PANEL	784777	1	
MP16	MOUNTING PLATE,HANDLE (LEFT)	884267	1	
MP17	MOUNTING PLATE,HANDLE (RIGHT)	884270	1	
MP18	CASE,OUTER	884262	1	
MP22	PWR PLUG,PANEL,6.3A,250V,3 WIRE	780817	1	
MP25	DECAL,ISOTHERMAL CASE	874131	1	
MP35	DECAL, CSA	864470	1	
MP43	TEST LEAD ASSY, TL70A	855820	1	
MP47	PWR PLUG PART,FUSE HOLDER	780825	1	
MP48	CONN ACC,D-SUB,FEMALE SCREWLOCK,.250	844704	2	
MP59	NAMEPLATE	931873	1	
MP66	TERM STRIP,SOCKET,.197CTR,8 POS	875877	1	
MP67	TERM STRIP,SOCKET,.197CTR,10 POS	875880	1	
MP80	HYDRA STARTER SOFTWARE	890645	1	
MP99	T/C CABLE,ASSY	871512	1	
MP101	LABEL,VINYL,1.500,.312	844712	4	

Table 6-2. 2635A Final Assembly (cont)

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
MP111		LABEL,PAPER,ITS-90	928101	1	
MP112	*	CARD,MEMORY,SRAM,256KB,BATTERY	927512	1	1
MP998		COVER,IEEE	885983	1	
T1		TRANSFORMER,POWER,100-240V	931105	1	
TM1		HYDRA DATA BUCKET MANUAL SET (ENGLISH)	932160	1	2
TM2		HYDRA (STARTERS PKG) APPLICATION SOFTWA	890632	1	
TM3		HYDRA & DATA BUCKET SERVICE MANUAL	889589	1	3
TM4		HYDRA DATA BUCKET USERS MANUAL (FRENCH)	931902	1	3
TM5		HYDRA DATA BUCKET USERS MANUAL (GERMAN)	931907	1	3
W1		WIRE ASSY,GROUND	874099	1	
W2		CABLE ASSY,FLAT,20 COND,MMOD,FERRITE	876185	1	
W3		CABLE, MEMORY	931113	1	
W4		CORD,LINE,5-15/IEC,3-18AWG,SVT,7.5 FT	284174	1	

1. FOR 256KB MEMORY CARD ORDER FLUKE PN 927512.
   FOR 1 MB MEMORY CARD ORDER FLUKE PN 927517
   FOR 2 MB MEMORY CARD ORDER FLUKE PN 944313.
2. INCLUDES: HYDRA USERS MANUAL (885988), AND HYDRA QUICK SETUP CARD (895883).
3. AVAILABLE THROUGH PARTS DEPARTMENT.

⚠ TO ENSURE SAFETY, USE EXACT REPLACEMENT ONLY.

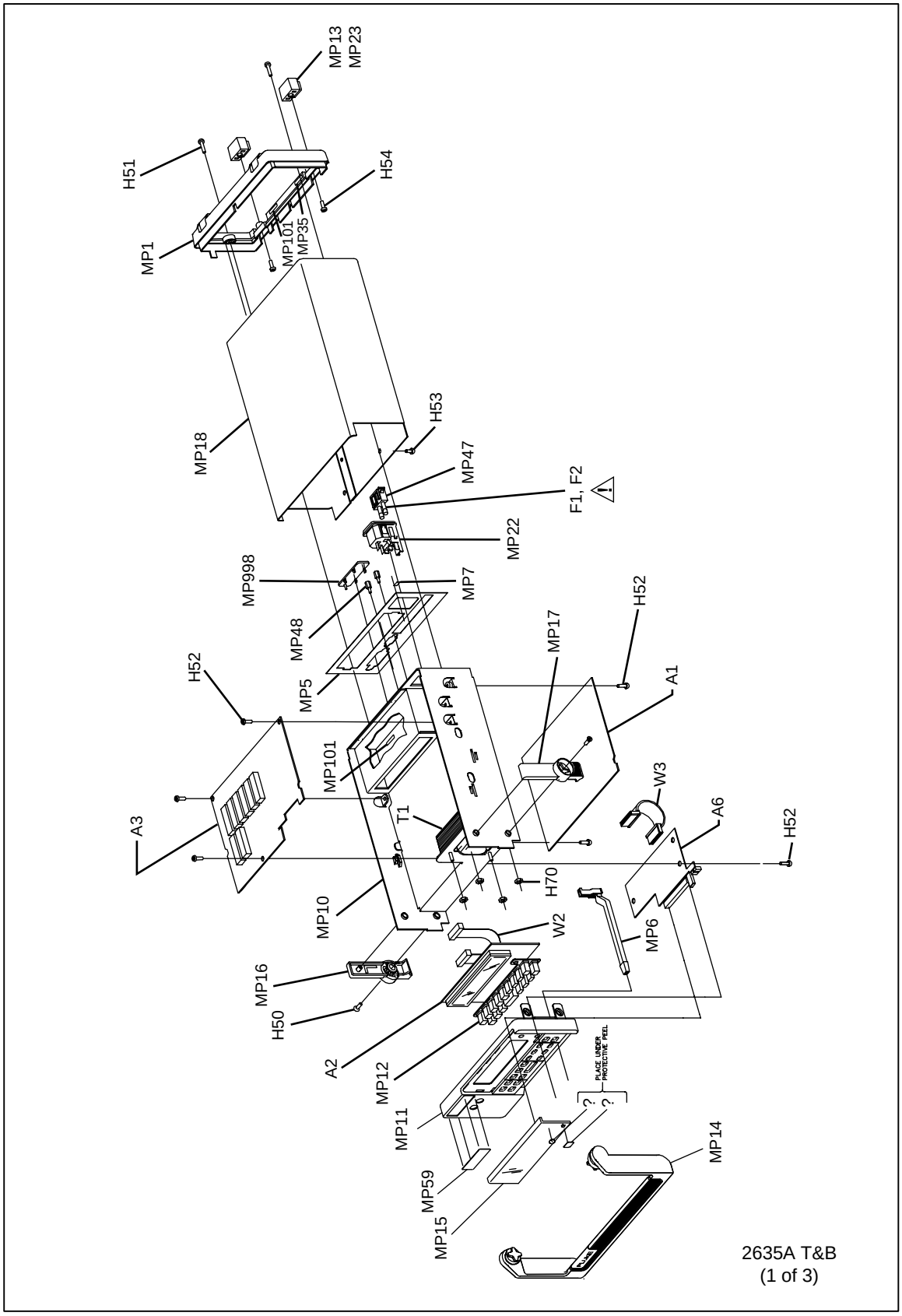

Figure 6-2. 2635A Final Assembly

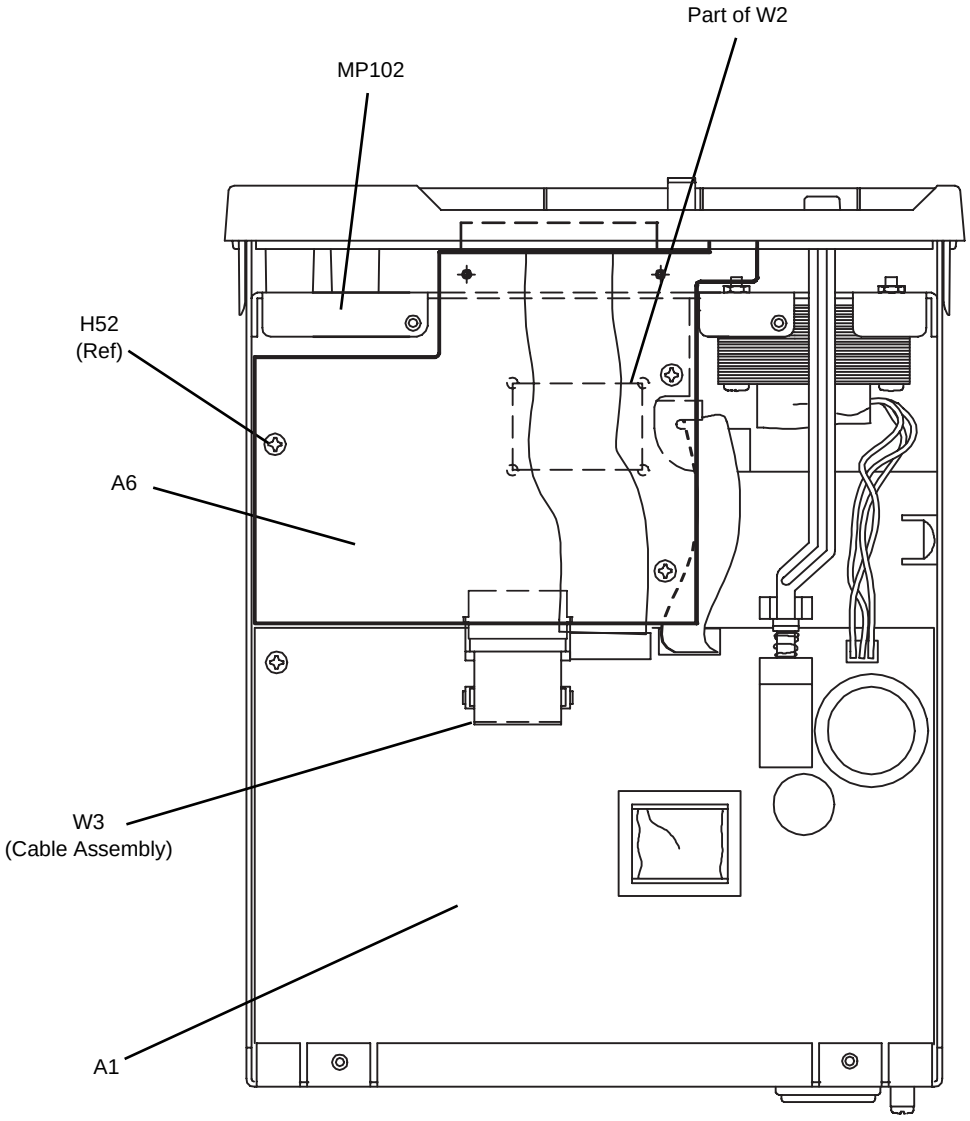

Figure 6-2. 2635A Final Assembly (cont)

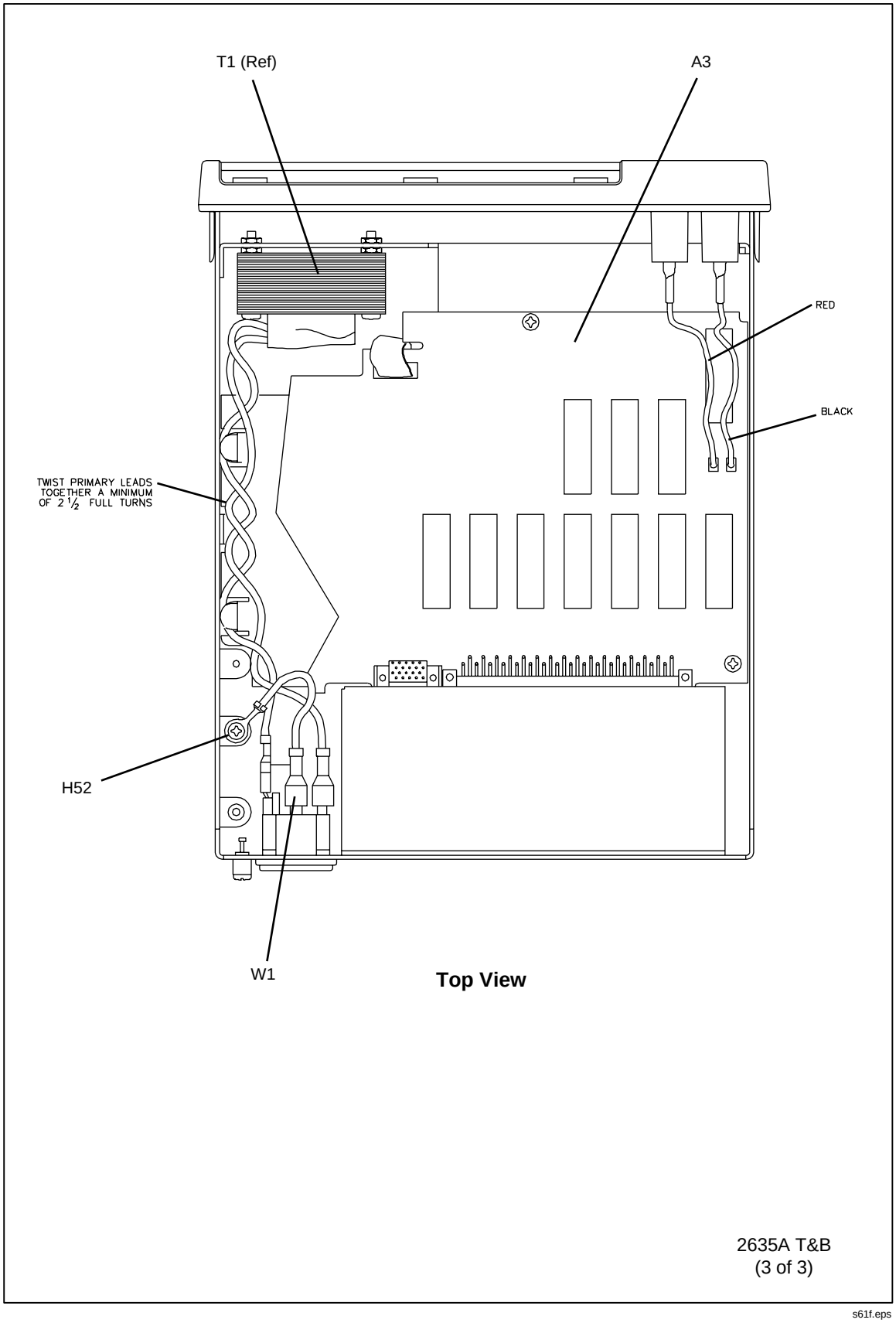

Figure 6-2. 2635A Final Assembly (cont)

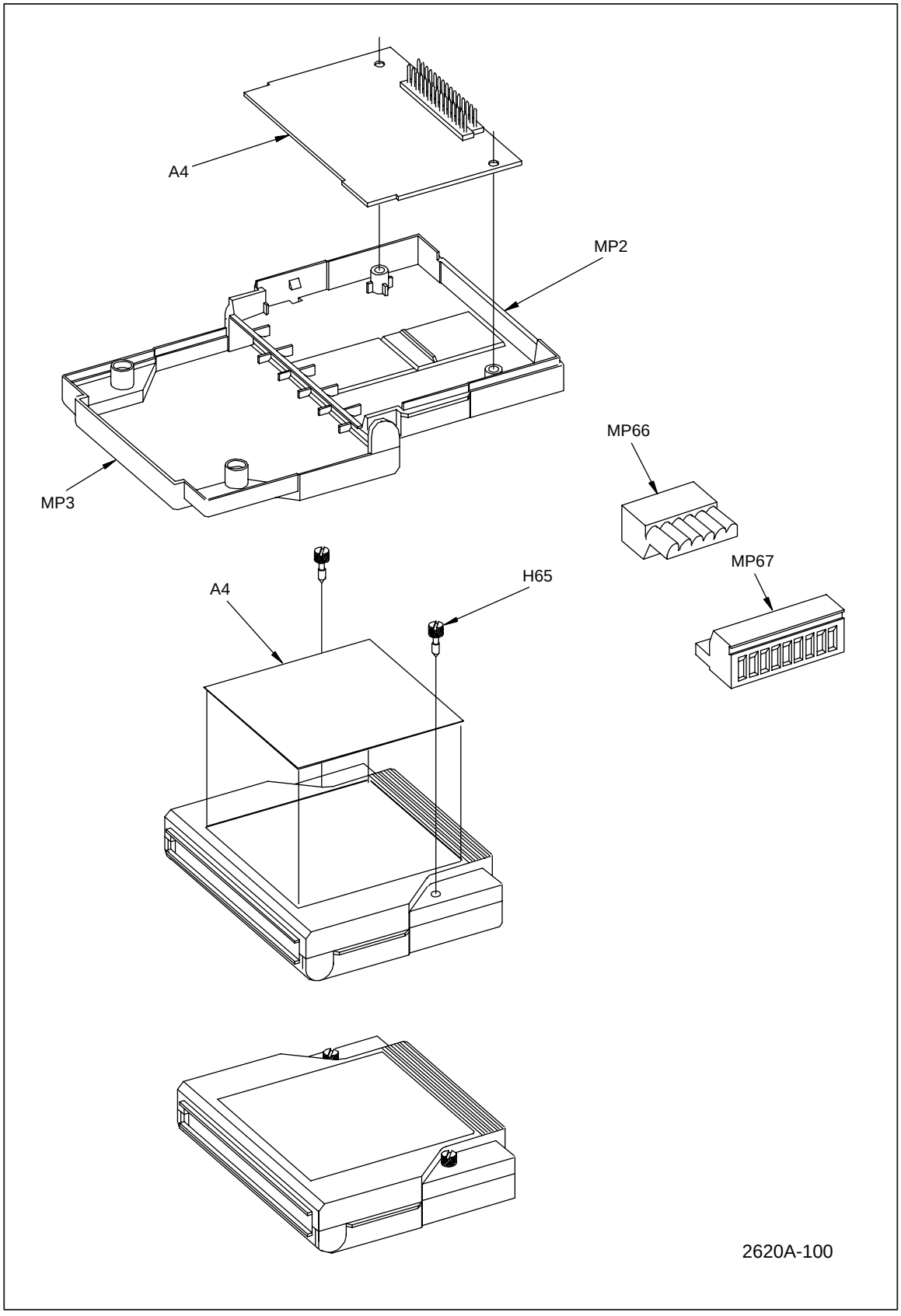

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Figure 6-2. 2635A Final Assembly (cont)

Table 6-3. 2620A/2625A A1 Main PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
AR1	*	IC,OP AMP,DUAL,LOW POWER,SOIC	867932	1	
AR2,AR3	*	IC,OP AMP,QUAD,LOW POWER,SOIC	742569	2	
C1,C3,C8, C11,C19,C21- C25,C27-29, C33,C36-38, C40-42		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287 747287 747287 747287 747287	20	
C2		CAP,CER,0.033UF,+-10%,200V,X7R,1206	602547	1	
C4,C5,C32, C34		CAP,AL,1UF,+-20%,50V	782805 782805	4	
C6		CAP,AL,10UF,+-20%,63V,SOLV PROOF	816843	1	
C7		CAP,AL,10000UF,+-20%,35V,SOLV PROOF	875203	1	
C9,C10,C43- C52,C54-59		CAP,CER,180PF,+-10%,50V,C0G,1206	769778 769778	18	
C12,C13		CAP,AL,470UF,+-20%,16V,SOLV PROOF	772855	2	
C14		CAP,AL,2200UF,+-20%,10V,SOLV PROOF	875208	1	
C15,C16		CAP,CER,33PF,+-10%,50V,C0G,1206	769240	2	
C17		CAP,AL,2.2UF,+-20%,50V	769687	1	
C18,C20		CAP,AL,220UF,+-20%,35V,SOLV PROOF	929708	2	
C26		CAP,AL,47UF,+-20%,100V,SOLV PROOF	837492	1	
C30,C31		CAP,AL,47UF,+-20%,50V,SOLV PROOF	822403	2	
C35,C53		CAP,CER,1000PF,+-5%,50V,C0G,1206	867408	2	
C39		CAP,CER,0.047UF,+-10%,100V,X7R	844733	1	
CR1,CR10		DIODE,SI,60 PIV,3 AMP,SCHOTTKY	943097	2	
CR2,CR3		DIODE,SI,600 PIV,1.5 AMP	112383	2	
CR4,CR11, CR12	* 	DIODE,SI,BV=75V,IO=250MA,SOT-23	830489 830489	3	
CR5,CR6	*	DIODE,SI,40 PIV,1 AMP,SCHOTTKY	837732	2	
CR7,CR14- CR16,CR18, CR19	* * *	DIODE,SI,BV=70V,IO=50MA,DUAL,S0T-23	742544 742544 742544	6	
CR8,CR9, CR13,CR17	*	DIODE,SI,BV=100,IO=100MA,DUAL,SOT-23	821116 821116	4	
J1		SOCKET,2 ROW,PWB,0.100C,RT ANG,26 POS	543512	1	
J2		HEADER,1 ROW,.050CTR,20 PIN	831529	1	
J3		HEADER,1 ROW,.100CTR,3 PIN	845334	1	
J4		CONN,D-SUB,PWB,RT ANG,9 PIN	855221	1	
J5		HEADER,1 ROW,.197CTR,RT ANG,10 PIN	875695	1	
J6		HEADER,1 ROW,.197CTR,RT ANG,8 PIN	875690	1	
L1		FERRITE CHIP,95 OHMS @100 MHZ,3612	867734	1	
L2		CHOKE,6TURN	320911	1	
P10		CABLE ASSY,FLAT,10 CONDUCT,6.0”	714022	1	
Q1-3	*	TRANSISTOR,SI,PNP,40V,300MW,SOT-23	742684	3	
Q4-6	*	TRANSISTOR,SI,NPN,60V,350MW,SOT-23	742676	3	
Q7,Q8	*	TRANSISTOR,SI,N-MOS,50W,D-PAK	927806	2	

Table 6-3. 2620A/2625A A1 Main PCA (Cont)

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
Q9	*	TRANSISTOR,SI,NPN,30V,200MW,SOT-23	820902	1	
R1,R2,R11,	*	RES,CERM,47K,+-5%,.125W,200PPM	746685	5	
R12,R22	*		746685		
R3,R4,R14,	*	RES,CERM,10K,+-5%,.125W,200PPM	746610	9	
R20,R21,R25,	*		746610		
R42,R47,R64	*		746610		
R5	*	RES,CERM,1K,+-1%,.125W,100PPM,1206	783241	1	
R6	*	RES,CERM,3.32K,+-1%,.125W,100PPM	810788	1	
R7,R16	*	RES,CERM,100K,+-5%,.125W,200PPM	740548	2	
R8,R63	*	RES,CERM,270,+-5%,.125W,200PPM	746354	2	
R9,R10,R35	*	RES,CERM,4.7K,+-5%,.125W,200PPM	740522	3	
R13	*	RES,CERM,20,+-5%,.125W,200PPM,1206	746222	1	
R15	*	RES,CERM,33,+-5%,.125W,200PPM,1206	746248	1	
R19,R28,	*	RES,CERM,470,+-5%,.125W,200PPM	740506	5	
R34,R49,R58	*		740506		
R26	*	RES,CERM,100,+-5%,.125W,200PPM	746297	1	
R30	*	RES,CERM,45.3K,+-1%,0.1W,100PPM	930201	1	
R31	*	RES,CERM,11K,+-1%,0.1W,100PPM,0805	928796	1	
R36,R37	*	RES,CERM,15K,+-5%,.125W,200PPM	746628	2	
R38	*	RES JUMPER,0.02,0.25W	682575	1	
R39	*	RES,CERM,63.4K,+-1%,.125W,100PPM	836627	1	
R40	*	RES,CERM,5.1K,+-5%,.125W,200PPM	746560	1	
R41	*	RES,CERM,11K,+-1%,.125W,100PPM	867291	1	
R43	*	RES,CERM,39K,+-5%,.125W,200PPM	746677	1	
R44	*	RES,CERM,1.30K,+-1%,.125W,100PPM	780999	1	
R45	*	RES,CERM,1M,+-1%,.125W,100PPM,1206	836387	1	
R46	*	RES,CERM,4.02K,+-1%,.125W,100PPM	783266	1	
R48		RES,CF,10K,+-5%,0.25W	697102	1	
R50-57,R59-		RES,CF,47,+-5%,0.25W	822189	12	
R62			822189		
RT1		THERMISTOR,DISC,0.46,25 C	875240	1	
RV1		VARISTOR,39V,+-20%,1.0MA	831735	1	
S1		SWITCH,PUSHBUTTON,DPDT,PUSH-PUSH	836361	1	
T1		TRANSFORMER,INVERTER	873968	1	
T2		INDUCTOR,FXD,DUAL,EE24-25,0.4M	817379	1	
TP1,TP30		JUMPER,WIRE,NONINSUL,0.200CTR	816090	2	
U1		IC,CMOS,64 X 16 BIT EEPROM,SERIAL,SO8	876789	1	
U2	*	IC,NMOS,TRPL PROGRAMMABLE TIME	866991	1	
U3	*	MODULE,8KX8 SRAM,ZERO PWR,TIME	867945	1	
U4	*	IC,CMOS,8-BIT MPU,1.5MHZ,256BY	876896	1	
U5,U7	*	ISOLATOR,OPTO,LED TO TRANSISTOR	851790	2	
U6	*	IC,VOLT REG,ADJ,1.2 TO 37 V,1.5 AMPS	460410	1	
U8	*	2620A-PROGRAMMED EPROM	894555	1	
U9	*	IC,V REG,SWITCHING,100KHZ,5A,T0-220	929591	1	

Table 6-3. 2620A/2625A A1 Main PCA (Cont)

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
U10	*	IC,CMOS,TRIPLE 3 INPUT NOR GATE,SOIC	867981	1	
U11	*	IC,CMOS,3-8 LINE DCDR W ENABLE,SOIC	783019	1	
U12,U28	*	IC,CMOS,QUAD INPUT NAND GATE,SOIC	830703	2	
U13	*	IC,CMOS,OCTL LINE DRVR,SOIC	801043	1	
U14	*	IC,CMOS,QUAD 2 INPUT XOR GATE,SOIC	867973	1	
U15	*	IC,CMOS,QUAD INPUT NOR GATE,SOIC	830711	1	
U16,U26	*	IC,CMOS,OCTAL D F/F,+EDG TRG,SOIC	838029	2	
U17,U27	*	IC,ARRAY,7 NPN DARLINGTON PAIR	821009	2	
U18	*	IC,VOLT REG,FIXED,-5.0 VOLTS,0.1 AMPS	454793	1	
U19	*	IC,VOLT REG,ADJ,1.2 TO 32 V,0.1 A	810242	1	
U20	*	IC,CMOS,12 STAGE BIN RIPPLE CNTR,SOIC	831636	1	
U21	*	IC,CMOS,TRIPLE 3 INPUT NAND GATE,SOIC	867978	1	
U22	*	IC,CMOS,DUAL D F/F,+EDG TRG,SOIC	782995	1	
U23	*	IC,CMOS,HEX INVERTER,UNBUFFERED,SOIC	806893	1	
U24	*	IC,COMPARATOR,DUAL,LOW PWR,SOIC	837211	1	
U25	*	IC,CMOS,RS232 DRIVER/RECEIVER,SOIC	821538	1	
U29	*	IC,CMOS,8 BIT P/S-IN,S-OUT SHFT,SOIC	782904	1	
U31	*	IC,OP AMP,DUAL,LOW POWER,SOIC	867932	1	
VR1	*	ZENER,UNCOMP,5.6V,5%,20MA,0.2W	875604	1	
VR2	*	ZENER,UNCOMP,6.0V,5%,20MA,0.2W	837161	1	
VR3	*	ZENER,UNCOMP,6.8V,5%,20MA,0.2W	837195	1	
VR4	*	IC, 1.23V,150 PPM T.C.,BANDGAP V, REF	634451	1	
Y1		CRYSTAL,4.9152 MHZ,+/- 0.005%,HC-18/U	800367	1	
Z1		RES,CERM,NET,CUSTOM	821157	1	
Z2		RES,CERM,SOIC,16 PIN,15 RES,22K,+-2%	867841	1	
Z3		RES,CERM,SOIC,20 PIN,10 RES,47K,+-2%	867846	1	

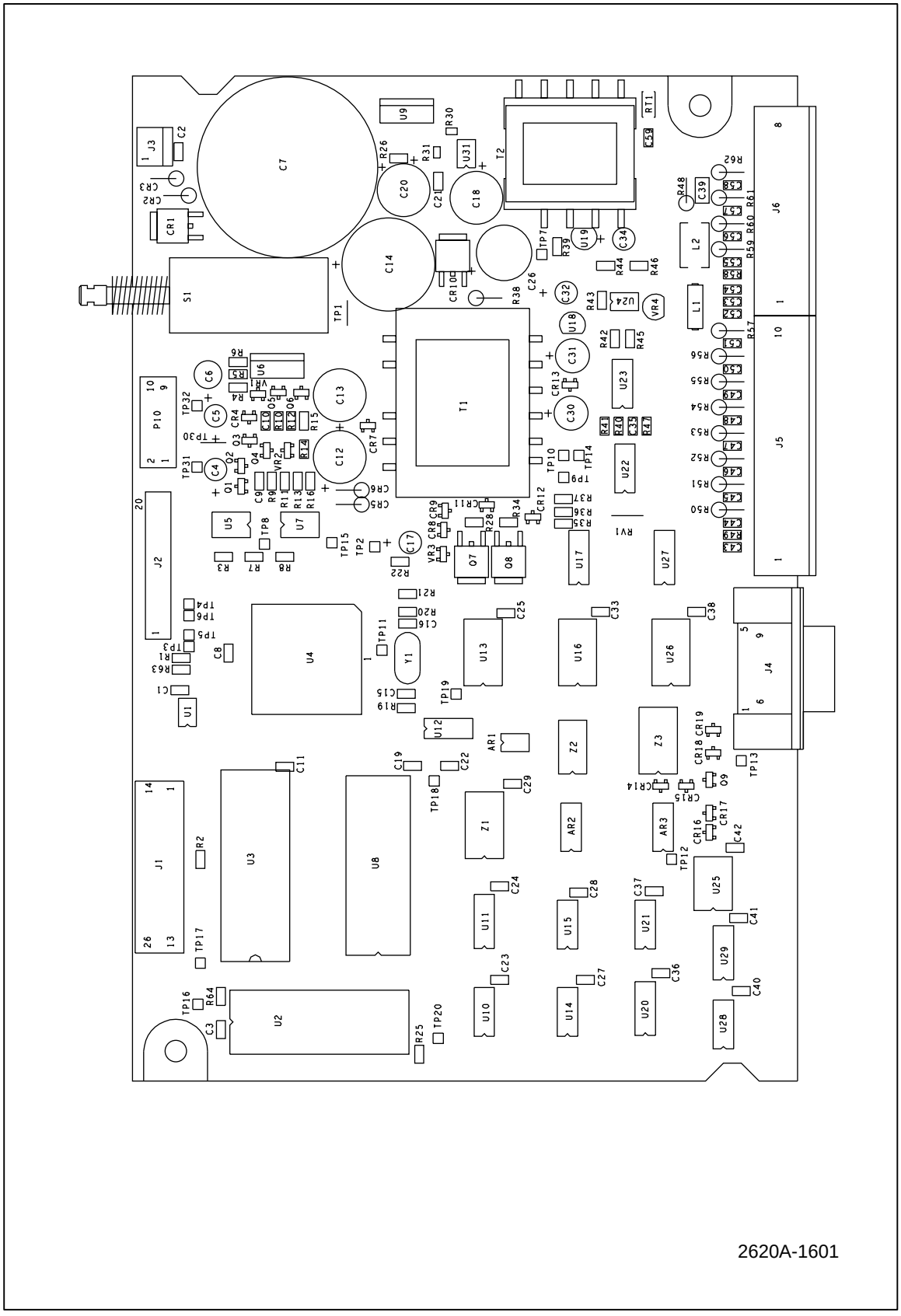

Figure 6-3. 2620A/2625A A1 Main PCA

Table 6-4. 2635A A1 Main PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
BT1		BATTERY,LITHIUM,3.0V,0.560AH	821439	1	
C1,C18		CAP,AL,220UF,+-20%,35V,SOLV PROOF	929708	2	
C2		CAP,CER,0.033UF,+-10%,200V,X7R,1206	602547	1	
C3,C8		CAP,CER,27PF,+-10%,50V,C0G,1206	800508	2	
C4,C5,C32,		CAP,AL,1UF,+-20%,50V	782805	4	
C34			782805		
C6		CAP,AL,10UF,+-20%,63V,SOLV PROOOF	816843	1	
C7		CAP,AL,10000UF,+-20%,35V,SOLV PROOF	875203	1	
C9,C10,C43-		CAP,CER,180PF,+-10%,50V,C0G,1206	769778	18	
C52,C54-59			769778		
C11,C15,C16,		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	30	
C19,C21-25,			747287		
C28,C29,C33,			747287		
C36,C38 C40-			747287		
C42,C60-65,			747287		
C68,C70-73,			747287		
C75,C76			747287		
C12,C13		CAP,AL,470UF,+-20%,16V,SOLV PROOF	772855	2	
C14		CAP,AL,2200UF,+-20%,10V,SOLV PROOF	875208	1	
C17		CAP,AL,2.2UF,+-20%,50V	769687	1	
C26		CAP,AL,47UF,+-20%,100V,SOLV PROOF	837492	1	
C30,C31,C66,		CAP,AL,47UF,+-20%,50V,SOLV PROOF	822403	4	
C67			822403		
C35,C53,C74		CAP,CER,1000PF,+-5%,50V,C0G,1206	867408	3	
C39		CAP,CER,0.047UF,+-10%,100V,X7R	844733	1	
C69		CAP,CER,4700PF,+-10%,50V,X7R,1206	832279	1	
CR1,CR10		DIODE,SI,60 PIV,3 AMP,SCHOTTKY	943097	2	
CR2,CR3		DIODE,SI,600 PIV,1.5 AMP	112383	2	
CR4,CR11,	*	DIODE,SI,BV=75V,IO=250MA,SOT-23	830489	4	
CR12,CR20	*		830489		
CR5,CR6,	*	DIODE,SI,40 PIV,1 AMP,SCHOTTKY	837732	3	
CR21	*		837732		
CR7,CR14-	*	DIODE,SI,BV=70V,IO=50MA,DUAL,SOT-23	742544	6	
CR16,CR18,	*		742544		
CR19	*		742544		
CR8,CR9,	*	DIODE,SI,BV=100,IO=100MA,DUAL,SOT-23	821116	4	
CR13,CR017	*		821116		
J1		SOCKET,2 ROW,PWB,0.100C,RT ANG,26 POS	543512	1	
J2		HEADER,1 ROW,.050CTR,20 PIN	831529	1	
J3		HEADER,1 ROW,.100CTR,3 PIN	845334	1	
J4		CONN,D-SUB,PWB,RT ANG,9 PIN	855221	1	
J5		HEADER,1 ROW,.197CTR,RT ANG,10 PIN	875695	1	
J6		HEADER,1 ROW,.197CTR,RT ANG,8 PIN	875690	1	
L1		FERRITE CHIP,95 OHMS @100 MHZ,3612	867734	1	
L2		CHOKE,6TURN	320911	1	

Table 6-4. 2635A A1 Main PCA (cont)

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
MP101		PCB ASSY, MAIN SM	932017	1	
P4		HEADER,2 ROW,.050CTR,40 PIN	838573	1	
P10		CABLE ASSY,FLAT,10 CONDUCT,6.0”	714022	1	
Q1-3,Q10	*	TRANSISTOR,SI,PNP,40V,300MW,SOT-23	742684	4	
Q4-6	*	TRANSISTOR,SI,NPN,60V,350MW,SOT-23	742676	3	
Q7,Q8	*	TRANSISTOR,SI,N-MOS,50W,D-PAK	927806	2	
Q9	*	TRANSISTOR,SI,NPN,30V,200MW,SOT-23	820902	1	
R1,R11,R12,	*	RES,CERM,47K,+-5%,.125W,200PPM	746685	6	
R22,R25,R45	*		746685		
R2	*	RES,CERM,698K,+-1%,.125W,100PPM	867296	1	
R3,R4,R14,	*	RES,CERM,10K,+-5%,.125W,200PPM	746610	16	
R42,R47,R64,	*		746610		
R65,R68,R70,	*		746610		
R72-75,R78,	*		746610		
R79,R81	*		746610		
R5,R98	*	RES,CERM,1K,+-1%,.125W,100PPM,1206	783241	2	
R6	*	RES,CERM,3.32K,+-1%,.125W,100PPM	810788	1	
R7,R16,R35	*	RES,CERM,100K,+-5%,.125W,200PPM	740548	3	
R8,R21	*	RES,CERM,270,+-5%,.125W,200PPM	746354	2	
R9,R10,R39,	*	RES,CERM,4.7K,+-5%,.125W,200PPM	740522	7	
R41,R71,R77,	*		740522		
R83	*		740522		
R13	*	RES,CERM,20,+-5%,.125W,200PPM,1206	746222	1	
R15,R86,R107	*	RES,CERM,33,+-5%,.125W,200PPM,1206	746248	3	
R19,R31	*	RES,CERM,11K,+-1%,0.1W,100PPM,1206	928796	2	
R20	*	RES,CERM,59K,+-1%,.125W,100PPM	851803	1	
R26	*	RES,CERM,100,+-5%,.125W,200PPM	746297	1	
R28,R34,R49,	*	RES,CERM,470,+-5%,.125W,200PPM	740506	4	
R58	*		740506		
R30	*	RES,CERM,45.3K,+-1%,0.1W,100PPM	930201	1	
R36	*	RES,CERM,3.6K,+-5%,.125W,200PPM	746537	1	
R37	*	RES,CERM,9.1K,+-5%,.125W,200PPM	746602	1	
R38	*	RES JUMPER,0.02,0.25W	682575	1	
R40	*	RES,CERM,5.1K,+-5%,.125W,200PPM	746560	1	
R43,R63,R84,	*	RES,CERM,1.5K,+-5%,.125W,200PPM	746438	4	
R92	*		746438		
R44	*	RES,CERM,1.30K,+-1%,.125W,100PPM	780999	1	
R46	*	RES,CERM,4.02K,+-1%,.125W,100PPM	783266	1	
R48	*	RES,CF,10K,+-5%,0.25W	697102	1	
R50-57,R59-	*	RES,CF,47,+-5%,0.25W	822189	12	
R62	*		822189		

Table 6-4. 2635A A1 Main PCA (cont)

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
R66,R67,R69,	*	RES,CERM,47,+-5%,.0625W,200PPM	927707	35	
R80,R82,R85,	*		927707		
R87-91,R93-	*		927707		
R97 R99-106,	*		927707		
R108-118	*		927707		
RT1		THERMISTOR,DISC,0.46,25 C	875240	1	
RV1		VARISTOR,41.5V,+-9%,1.0MA,1206	914114	1	
S1		SWITCH,PUSHBUTTON,DPDT,PUSH-PUSH	836361	1	
T1		TRANSFORMER,INVERTER	873968	1	
T2		INDUCTOR,FXD,DUAL,EE24-25,0.4MH,1.2A	817379	1	
T3		INDUCTOR,20UH,+-20%,1.15ADC	914007	1	
TP1,TP30		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	2	
U1	*	IC,INTEGR MLTIPROTOCOL MPU,16 MHZ,QFP	910831	1	
U2	*	IC,CMOS,QUAD BUS BUFFER W/3-ST,SOIC	866801	1	
U3,U4	*	IC,OP AMP,QUAD,LOW POWER,SOIC	742569	2	
U5,U7	*	ISOLATOR,OPTO,LED TO TRANSISTOR	851790	2	
U6	*	IC,VOLT REG,ADJ,1.2 TO 37 V,1.	460410	1	
U8,U28	*	IC,OP AMP,DUAL,LOW POWER,SOIC	867932	2	
U9	*	IC,V REG,SWITCHING,100KHZ,5A,TO-220	929591	1	
U10	**	IC,CMOS,MICROPROCESSOR SUPERVISOR,DIP	913975	1	
U11	*	GAL,PROGRAMMED,I/O DECODER	931910	1	
U12	*	IC,CMOS,PARALLEL I/O CAL/CLCK	914036	1	
U13	*	IC,CMOS,RS232 DRIVER/RECEIVER,SOIC	821538	1	
U14,U16	*	IC,FLASH,128K X 8,12 V,BOT BOOT,PLCC	914106	2	
U15	*	IC,CMOS,REGULATOR,STEP-UP,PWM,SO16	914080	1	
U17,U27	*	IC,ARRAY,7 NPN DARLINGTON PAIR	821009	2	
U18	*	IC,VOLT REG,FIXED,-5.0 VOLTS,0.1 AMPS	454793	1	
U19	*	IC,VOLT REG,ADJ,1.2 TO 32 V,0.1 A	810242	1	
U20,U24	*	IC,CMOS,SRAM,128K X 8,100 NS,SO32	914101	2	
U22	*	IC,CMOS,DUAL D F/F,+EDG TRG,SOIC	782995	1	
U23	*	IC,CMOS,HEX INVERTER,UNBUFFERED,SOIC	806893	1	
U25	*	IC,PROG GATE ARRAY,3000 G,70 MHZ,PQFP	887138	1	
U26	*	IC,CMOS,QUAD INPUT NAND GATE,SOIC	830703	1	
VR1	*	ZENER,UNCOMP,5.6V,5%,20MA,0.2W	875604	1	
VR2	*	ZENER,UNCOMP,6.0V,5%,20MA,0.2W	837161	1	
VR3	*	ZENER,UNCOMP,6.8V,5%,20MA,0.2W	837195	1	
W3		HEADER,1 ROW,.100CTR,2 PIN	643916	1	
Y1		CRYSTAL,12.288MHZ,50PPM,SURFACE MT	913942	1	
Z1		RES,CERM,NET,CUSTOM	821157	1	
Z2		RES,CERM,SOIC,16 PIN,15 RES,22	867841	1	
Z3		RES,CERM,SOIC,20 PIN,10 RES,47	867846	1	

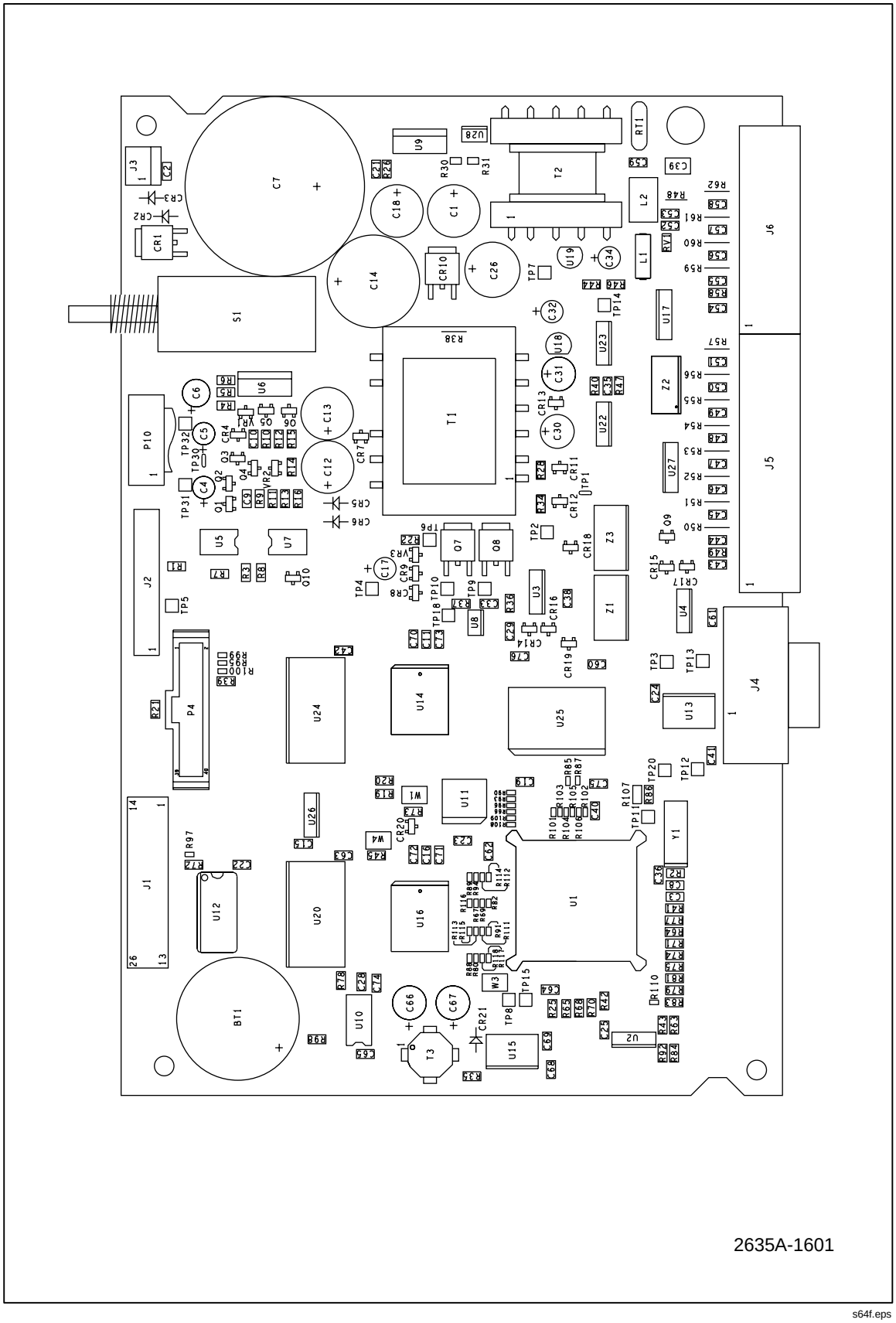

Figure 6-4. 2635A A1 Main PCA

Table 6-5. A2 Display PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
C1,C3-6		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	5	
C2		CAP,TA,4.7UF,+-20%,16V,3528	745976	1	
CR3	*	DIODE,SI,BV=75V,IO=250MA,SOT-23	830489	1	
DS1		TUBE,DISPLAY,VAC FLUOR,7 SEG,10 CHAR	783522	1	
J1		HEADER,1 ROW,.050CTR,20 PIN	831529	1	
LS1		AF TRANSD,PIEZO,22 MM	602490	1	
MP102		DISPLAY, PWB ASSY, SM	873901	1	
MP321		WIRE,JUMPER,TEF,22AWG,WHT,.300	528257	1	
R1,R10,R12	*	RES,CERM,10K,+-5%,.125W,200PPM	746610	3	
R2	*	RES,CERM,2.2M,+-5%,.125W,200PPM	811778	1	
R3	*	RES,CERM,1.2M,+-5%,.125W,200PPM	806240	1	
R11	*	RES,CERM,1K,+-5%,.125W,200PPM,1206	745992	1	
U1	*	IC,CMOS,4-BIT MPU,FLUKE 45-90002	820993	1	
U4	*	IC,CMOS,DUAL DIV BY 16 BIN CNTR,SOIC	837054	1	
U5	*	IC,CMOS,DUAL MONOSTB MULTIVBRTR,SOIC	806620	1	
U6	*	IC,CMOS,QUAD 2 IN NAND W/SCHMT,SOIC	837245	1	
W1		WIRE,JUMPER,TEF,22AWG,WHT,.300	528257	1	1
Z1		RES,CERM,SOIC,16 PIN,15 RES,10K,+-2%	836296	1	

1. W1 IS NOT INSTALLED ON 2620A AND 2625A INSTRUMENTS.

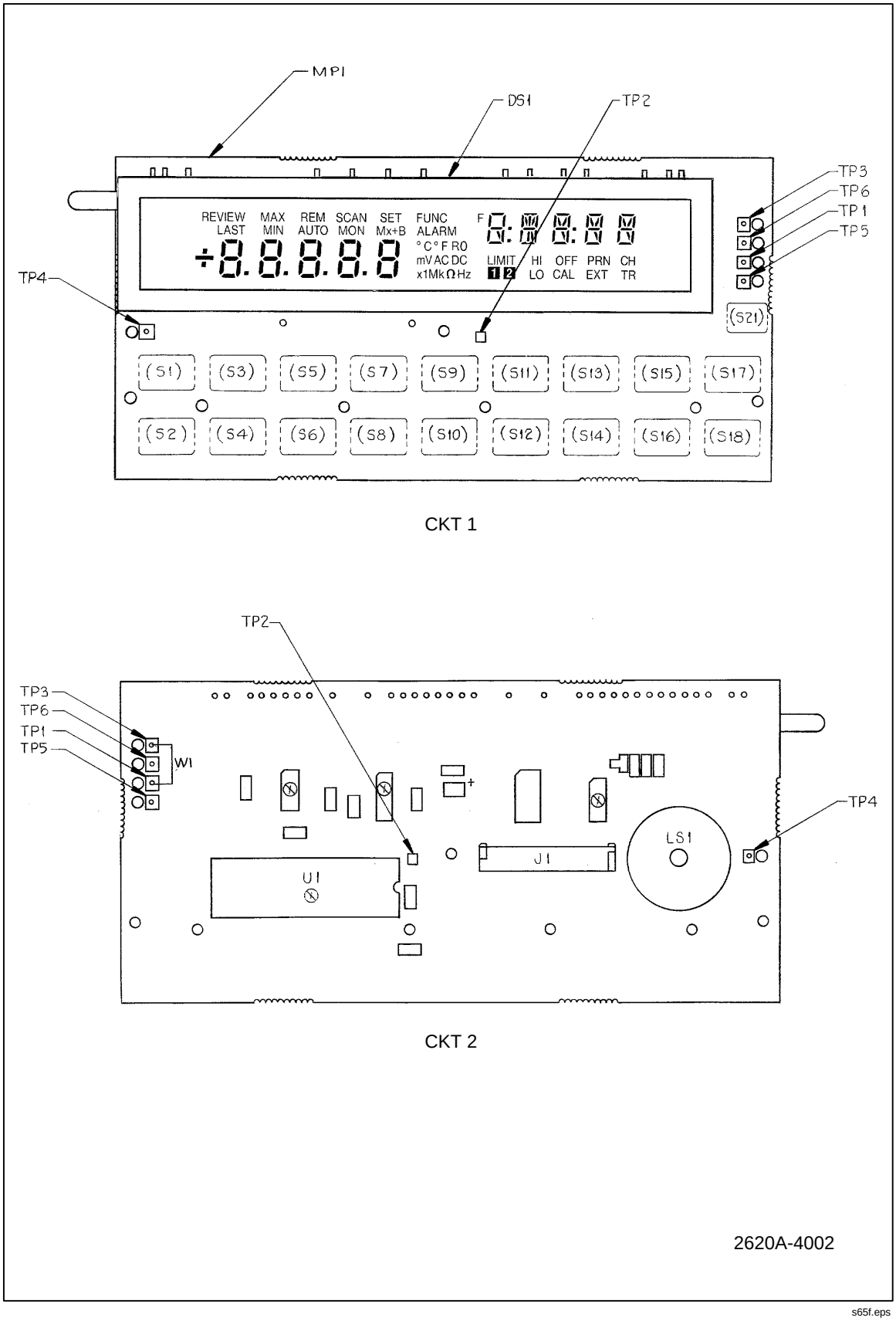

Figure 6-5. A2 Display PCA

Table 6-6. A3 A/D Converter PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
C1-3,C18,C21, C22,C25,C29, C33		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287 747287 747287	9	
C4,C5		CAP,CER,15PF,+-10%,50V,C0G,1206	837393	2	
C6,C7,C10		CAP,POLYPR,0.1UF,+-10%,160V	446781	3	
C8,C9,C19		CAP,TA,10UF,+-20%,10V	714766	3	
C11		CAP,POLYPR,2200PF,+-5%,100V	854505	1	
C12		CAP,TA,2.2UF,+-10%,35V	697433	1	
C13		CAP,POLYPR,0.033UF,+-10%,63V	721050	1	
C14,C34		CAP,POLYPR,1000PF,+-1%,100V	844816	2	
C15,C16		CAP,TA,33UF,+-10%,6V	866897	2	
C17		CAP,POLYES,1UF,+-10%,50V	733089	1	
C20,C24		CAP,CER,4.3PF,+-10%,50V,C0G,1206	844738	2	
C23		CAP,CER,4.3PF,+-0.5PF,50V,C0G,0805	514216	1	
C26,C28		CAP,AL,470UF,+-20%,10V,SOLV PROOF	822387	2	
C27		CAP,POLYPR,100PF,+-1%,100V	844803	1	
C30		CAP,CER,0.01UF,+-10%,50V,X7R,1206	747261	1	
C31		CAP,POLYES,0.1UF,+-10%,1000V	837518	1	
C32		CAP,CER,2500PF,+-20%,250V,X7R	485680	1	
C35-38		CAP,CER,180PF,+-10%,50V,C0G,1206	769778	4	
CR1,CR2,CR4	*	DIODE,SI,BV=70V,IO=50MA,DUAL,SOT-23	742320	3	
J1		CONN,DIN41612,TYPE C,RT ANG,48 PIN	867333	1	
J2		CONN,MICRO-RIBBON,PLUG,RT ANG,20 POS	876107	1	
J10		HEADER,2 ROW,.100CTR,10 PIN	756858	1	
K1,K2,K15-17		RELAY,ARMATURE,2 FORM C,5VDC,LATCH	603001	5	
K3,K5-14		RELAY,ARMATURE,4 FORM C,5 V,LATCH	642444	11	2
L1-24		FERRITE CHIP,95 OHMS @100 MHZ,3612	867734	24	
MP125,MP126		RIVET,S-TUB,OVAL,AL,.087,.343	838458	2	
Q1	*	TRANSISTOR,SI,PNP,40V,300MW,SOT-23	742684	1	
Q2,Q12,Q13	*	TRANSISTOR,SI,N-JFET,SEL,SOT-23	876263	3	
Q3-9	*	TRANSISTOR,SI,N-JFET,SEL,SOT-23	820860	7	
Q10,Q11,Q14, Q15	* *	TRANSISTOR,SI,NPN,25V,0.3W,SEL,SOT-23	821637 821637	4	
R1	*	RES,CERM,10K,+-1%,.125W,100PPM	769794	1	
R2,R36,R40, R41	* *	RES,CERM,30.1K,+-1%,.125W,100PPM	801258 801258	4	
R3,R4	*	RES,CERM,470K,+-5%,.125W,200PPM	746792	2	
R5	*	RES,CERM,100K,+-1%,.125W,100PPM	769802	1	
R6,R08,R9, R19,R23,R34	* *	RES,CERM,10K,+-5%,.125W,200PPM	746610 746610	6	
R7	*	RES,CERM,360,+-5%,.125W,200PPM	783290	1	
R10,R11	⚠	RES,MF,1K,+-1%,100PPM,FLMPRF,FUSIBLE	650085	2	1
R12,R33,R39, R44	* *	RES,CERM,1K,+-5%,.125W,200PPM,1206	745992 745992	4	

Table 6-6. A3 A/D Converter PCA (cont)

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
R13,R43		RES,CF,270,+-5%,0.25W	810424	2	
R14,R24-28	*	RES,CERM,47K,+-5%,.125W,200PPM	746685	6	
R15	*	RES,CERM,61.9K,+-1%,.125W,100PPM	821330	1	
R16,R17,R20	*	RES,CERM,200K,+-5%,.125W,200PPM	746743	3	
R18	*	RES,CERM,16.9K,+-1%,.125W,100PPM	836635	1	
R21	*	RES,CERM,845,+-1%,.125W,100PPM	821322	1	
R22	*	RES,CERM,91K,+-5%,.125W,200PPM	811828	1	
R29,R30	*	RES,CERM,22,+-5%,.125W,200PPM,1206	746230	2	
R31,R32,R38	*	RES,CERM,100K,+-5%,.125W,200PPM	740548	3	
R35,R42	*	RES,CERM,100K,+-5%,3W	820811	2	
R37	*	RES,CERM,24.9K,+-1%,.125W,100PPM	867689	1	
R45,R46		RES,MF,10K,+-1%,0.100W,100PPM	601432	2	
RT1		THERMISTOR,DISC,POS,1K,+-40%,25 C	820878	1	
RV1,RV2		VARISTOR,910,+-10%,1.0MA	876193	2	
TP9		JUMPER,WIRE,NONINSUL,0.200CTR	816090	1	
U1	*	IC,COMPARATOR,QUAD,14 PIN,SOIC	741561	1	
U3	*	IC,CMOS,DUAL D F/F,+EDG TRG,SOIC	782995	1	
U4,U5,U10-12	*	IC,ARRAY,7 NPN DARLINGTON PAIRS,SOIC	821009	5	
U6	*	IC,BPLR,TRUE RMS TO DC CONVERTER	707653	1	
U7	*	IC,OP AMP,JFET INPUT,DECOMP,SOIC	837237	1	
U8	*	MEAS PROCESSOR & A/D CONV, CMOS IC.	776195	1	
U9	*	IC,CMOS,MCU,8 BIT,1 MHZ,ROMMEDPLCC68	601317	1	
U13	*	IC,OP AMP,DUAL,HIGH BW,SNGL SUP,SO8	929075	1	
U14	*	IC,COMPARATOR,DUAL,LOW PWR,SOIC	837211	1	
VR1	*	STABILITY TESTED ZENER	387217	1	
VR2,VR3	*	ZENER,UNCOMP,6.0V,5%,20MA,0.2W,SOT-23	837161	2	
W1		WIRE ASSY,(H)	834929	1	
W2		WIRE ASSY,INPUT (L)	874086	1	
Y1		CRYSTAL,3.6864MHZ,+-0.005%,HC-18V	570606	1	
Y2		CRYSTAL,3.84MHZ,+-0.05%,HC-18/U	650390	1	
Z1		RNET,CERM,SIP,2620 LO V DIVIDER	849984	1	
Z2		RNET,MF,POLY,SIP,2620 A TO D CONV	884544	1	
Z3		RNET,CERM,SIP,2620 HI V AMP GAIN	847363	1	
Z4		RNET,MF,POLY,SIP,2620 HI V DIVIDER	851100	1	

1. ⚠ FUSIBLE RESISTOR. TO ENSURE SAFETY, USE EXACT REPLACEMENT ONLY.
2. SEE DETAIL IN FIGURE 6-6 FOR RELAY INSTALLATION POLARITY.

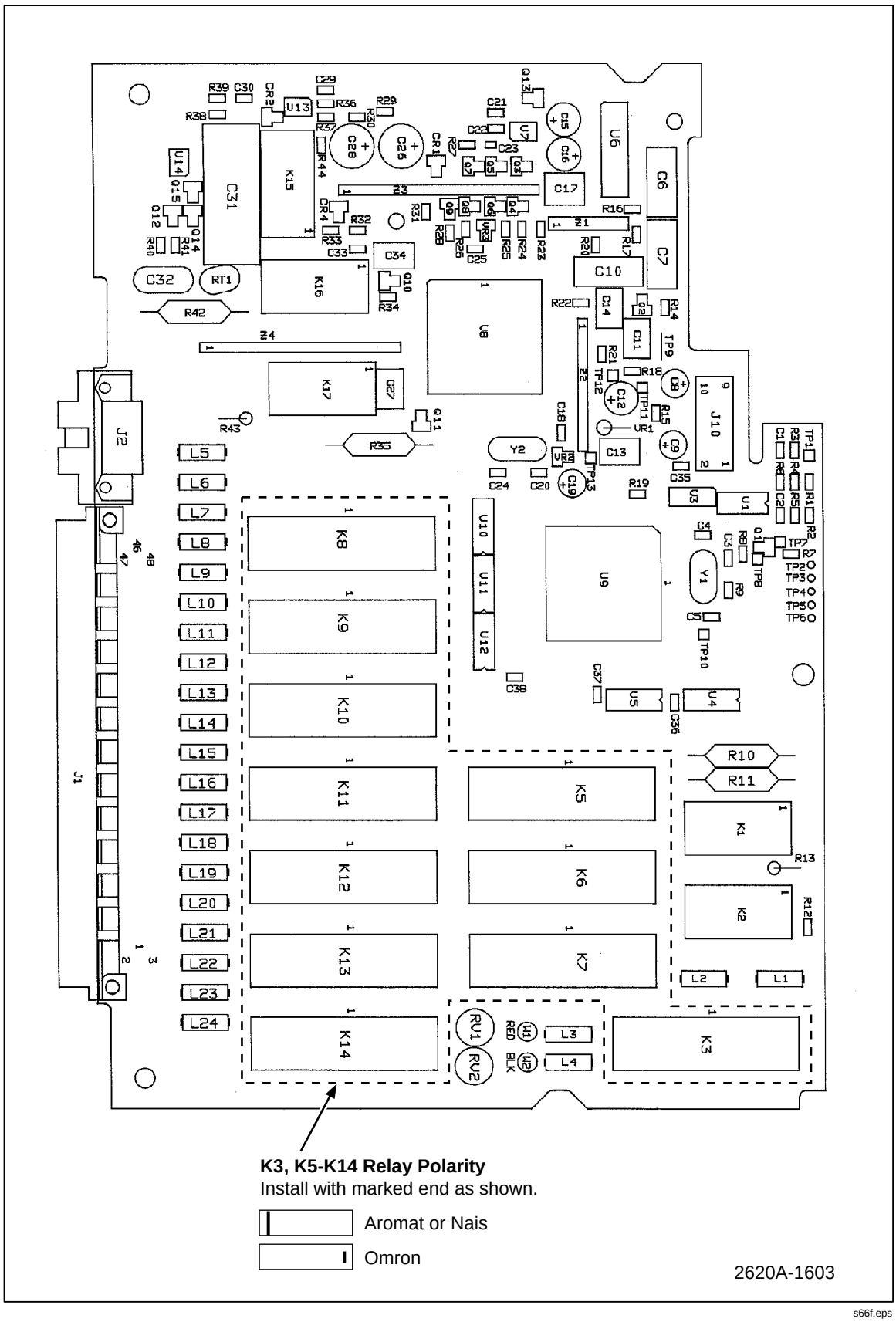

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Figure 6-6. A3 A/D Converter PCA

Table 6-7. A4 Analog Input PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
C1		CAP,CER,1000PF,+-5%,50V,C0G,1206	867408	1	
H55		RIVET,S-TUB,OVAL,AL,.087,.375	106473	2	
L1		CORE,BALUN,FERRITE,.136,.079,.093	106184	1	
M1,M2		HEADER,1 ROW,.156CTR,15 PIN	414458	2	
MP4		ANALOG INPUT CONNECTOR,PWB	873815	1	
P1		CONN,DIN41612,TYPE R,RT ANG,48 SCKT	867338	1	
P2		CONN,MICRO-RIBBON,REC,RT ANG,20 POS	876102	1	
Q1	*	TRANSISTOR,SI,NPN,TMP SENSR,SEL,TO-92	741538	1	
R1		RES,MF,5.49K,+-1%,0.125W,100PPM	334565	1	
R2		RES,MF,10K,+-1%,0.125W,25PPM	328120	1	
R3		RES,VAR,CERM,50K,+-10%,0.5W	876573	1	
RV1-4		VARISTOR,910,+-10%,1.0MA	876193	4	
TB1,TB2		TERM STRIP,PWB,45 ANG,.197CTR,20 POS	875195	2	
VR1		IC, 2.5V,100 PPM T.C.,BANDGAP REF	723478	1	
REFER TO TABLE 6-1 FOR ORDERING INFORMATION ON CASE TOP, BOTTOM AND DECAL.					

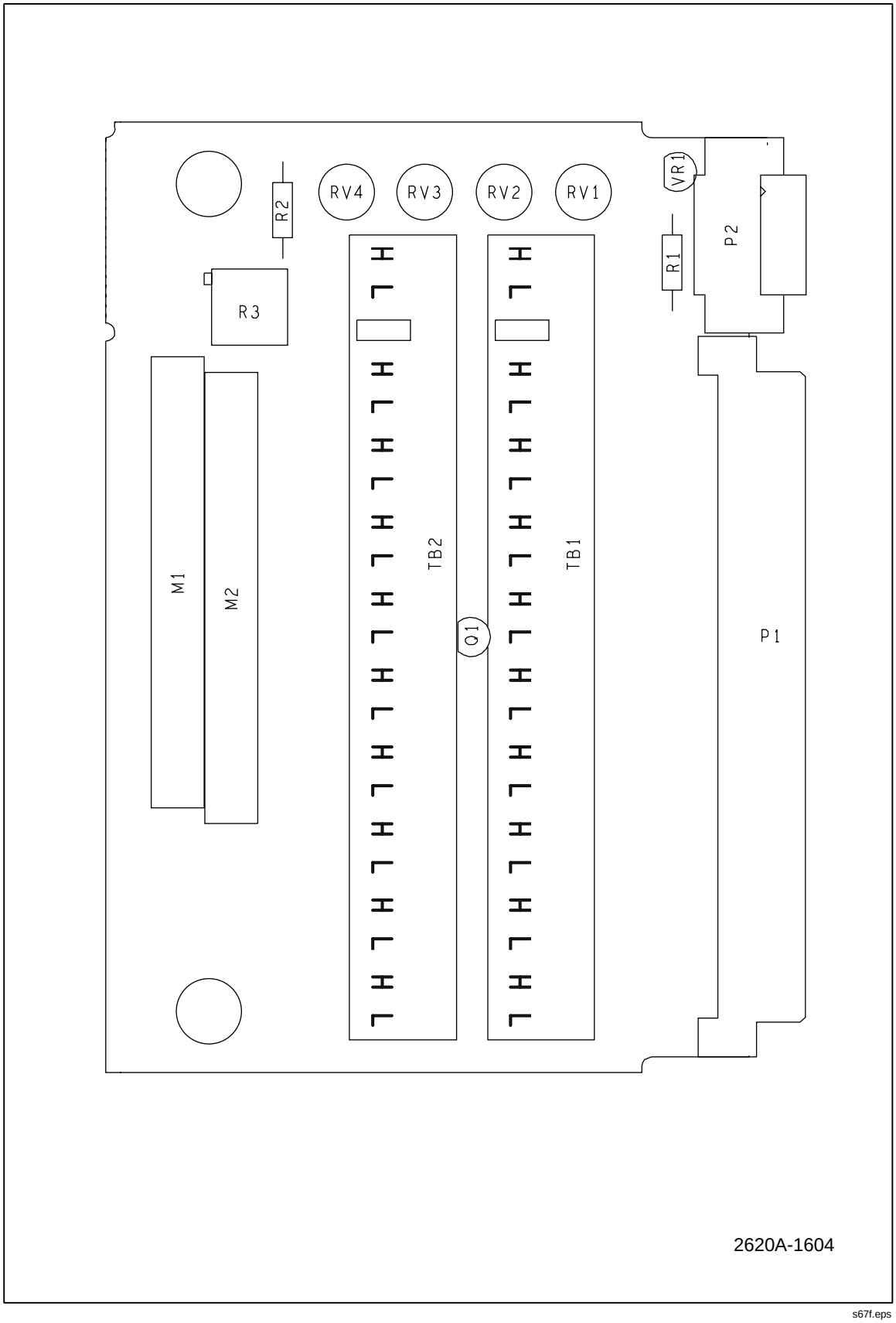

Figure 6-7. A4 Analog Input PCA

Table 6-8. A5 (Option -05) IEEE-488 Interface PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
C1-3		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	3	
J1		HEADER,2 ROW,.100CTR,RT ANG,26 PIN	512590	1	
J2		HEADER,2 ROW,.100CTR,24 PIN	831834	1	
R1	*	RES,CERM,5.1K,+-5%,.125W,200PPM	746560	1	
TP1		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	1	
U1	*	IC,NMOS,GPIB CONTROLLER,PLCC	887190	1	
U2	*	IC,LSTTL,OCTAL GPIB XCVR,SOIC	831651	1	
U3	*	IC,LSTTL,OCTAL GPIB XCVR,SOIC	831669	1	
U4	*	IC,CMOS,QUAD INPUT NAND GATE,SOIC	830703	1	
ATTACHING HARDWARE AND CABLE ARE LISTED BELOW:					
H52		SCREW,PH,PSTL,LOCK,6-32,250	152140		
MP56		CONN ACC,MICRO-RIBBON,SCREW LOCK KIT	836585		
W4		IEEE,CABLE ASSY	874094		

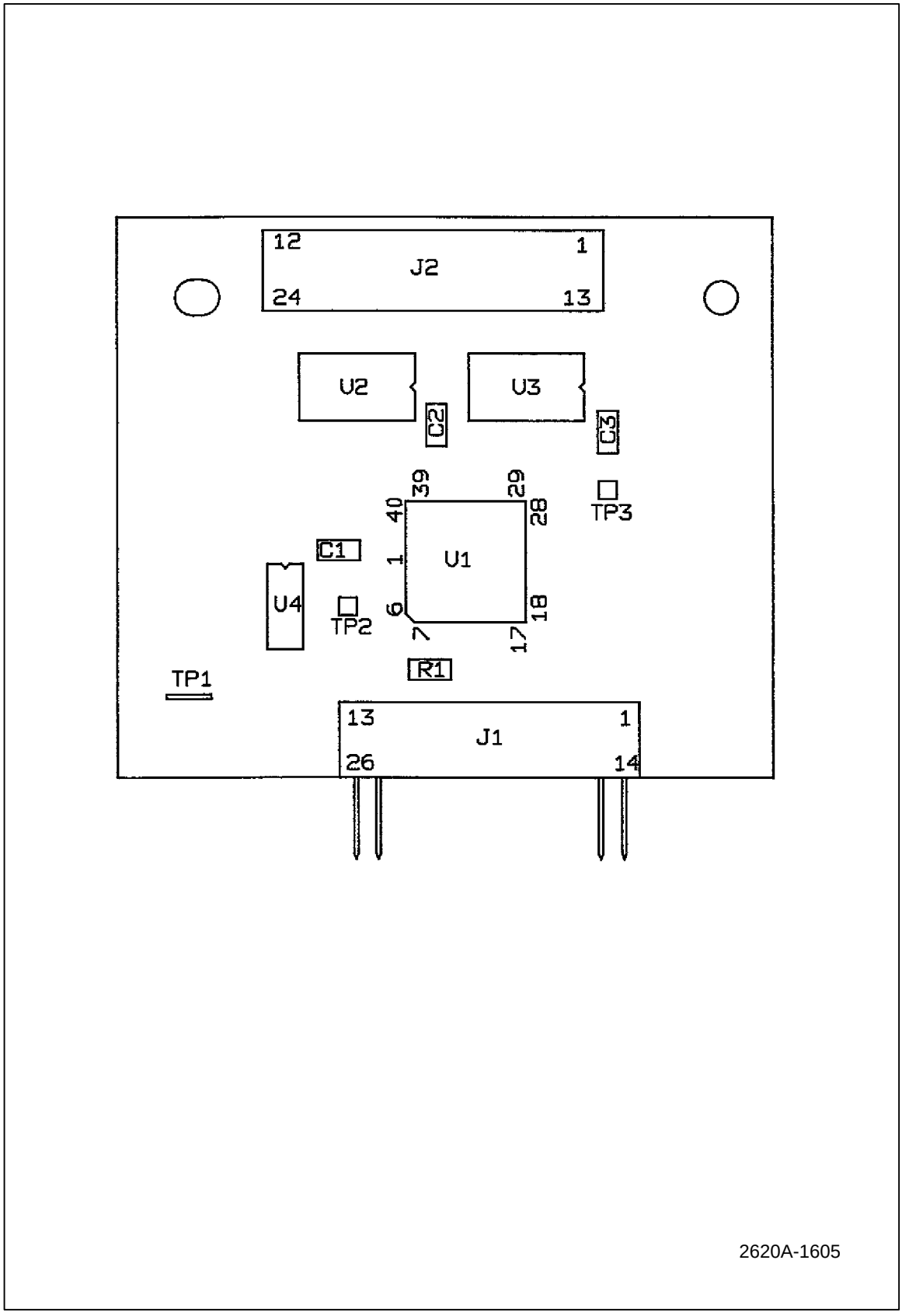

Figure 6-8. A5 IEEE-488 Interface PCA (Option -05)

Table 6-9. 2625A A6 Memory PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
C1-8		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	8	
J1		HEADER,2 ROW,.100CTR,RT ANG,26 PIN	512590	1	
TP1,TP2		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	2	
U1	*	IC,CMOS,OCTAL D TRANSPARNT LATCH,SOIC	876235	1	
U2	*	IC,CMOS,QUAD 2 INPUT AND GATE,SOIC	853317	1	
U3	*	IC,CMOS,DUAL DIV BY 16 BIN CNTR,SOIC	837054	1	
U4	*	IC,CMOS,4BIT BISTBL LTCH W/ENABL,SOIC	876243	1	
U5	*	IC,CMOS,QUAD INPUT NAND GATE,SOIC	830703	1	
U6,U7	*	IC,CMOS,128K X 8 SRAM,120 NSEC,NVM	876250	2	
U8	*	IC,CMOS,3-8 LINE DCDR W/ENABLE,SOIC	867726	1	

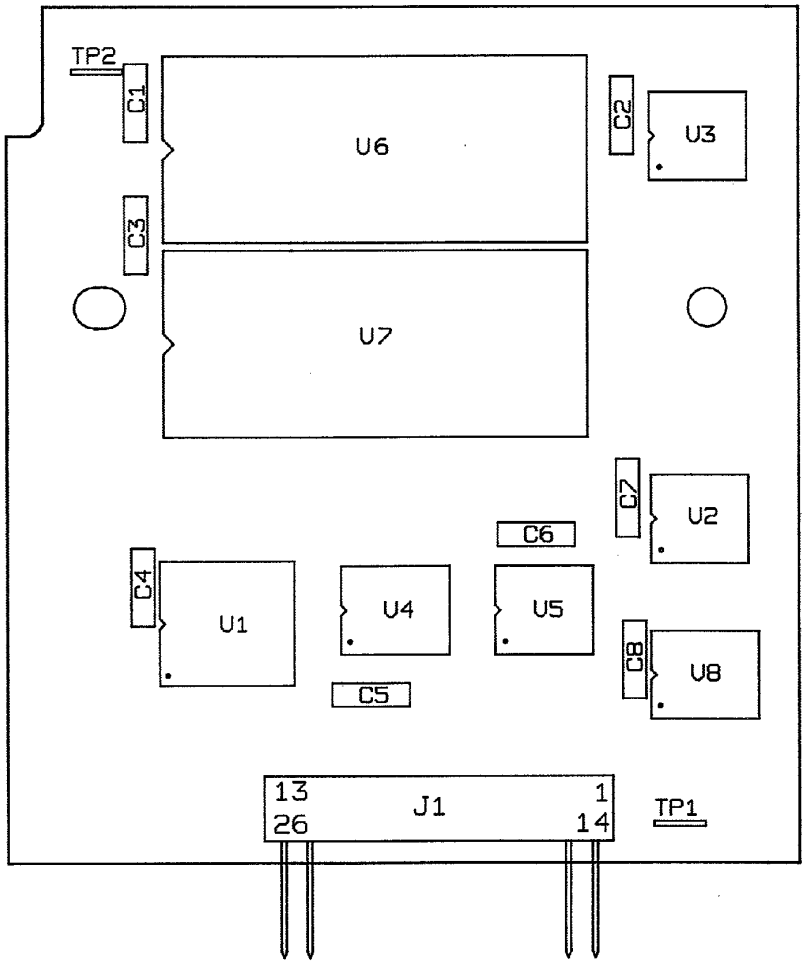

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Figure 6-9. 2625A A6 Memory PCA

Table 6-10. 2635A A6 Memory Card I/F PCA

Reference Designator		Description	Fluke Stock No	Tot Qty	Notes
C1-4,C6-8		CAP,CER,0.1UF,+-10%,25V,X7R,1206	747287	7	
C5		CAP,TA,47UF,+-20%,10V,7343	867580	1	
C9		CAP,TA,1UF,+-20%,35V,3528	866970	1	
DS1		LED,RED,RIGHT ANGLE,3.0 MCD	927389	1	
DS2		LED,YELLOW,RIGHT ANGLE,3 MCD	914242	1	
P1		CONN,MEMORY CARD,HEADER,RT ANG,68 PIN	914184	1	
P2		HEADER,2 ROW,.050CTR,RT ANG,40 PIN	838540	1	
Q1	*	TRANSISTOR,SI,P-MOS,2W,SOIC	914031	1	
R1,R3,R4,R8	*	RES,CERM,10K,+-5%,.125W,200PPM	746610	4	
R2,R5,R7,	*	RES,CERM,47K,+-5%,.125W,200PPM	746685	8	
R9,R12,R14,	*		746685		
R16,R17	*		746685		
R6,R10,R11	*	RES,CERM,360,+-5%,.125W,200PPM	783290	3	
R13	*	RES,CERM,1.5K,+-5%,.125W,200PPM	746438	1	
R15	*	RES,CERM,33,+-5%,.125W,200PPM,1206	746248	1	
TP1		TERM,UNINSUL,WIRE FORM,TEST POINT	781237	1	
U1	*	IC,PROG GATE ARRAY,3000 G,70 MHZ, PQFP	601275	1	
U2	*	IC,CMOS,QUAD BILATERAL SWITCH,SOIC	914098	1	
U3	*	IC,EPROM,36KBIT,SERIAL,PROGRAMMED, SO8	601267	1	
Z2		RES,CERM,SOIC,16 PIN,8 RES,100	838086	1	

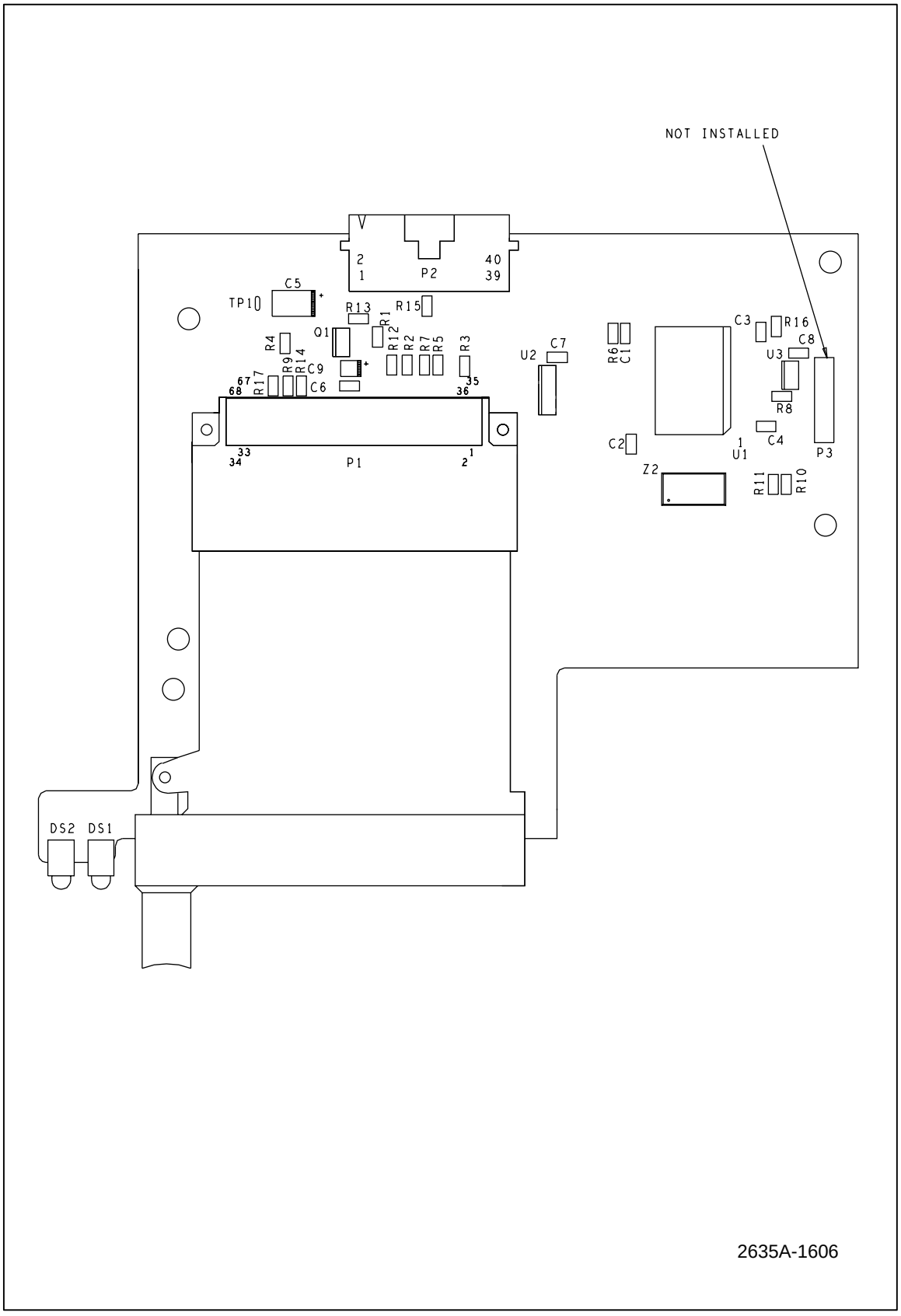

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Figure 6-10. 2635A A6 Memory Card I/F PCA

Chapter 7
IEEE-488 Option -05

Title **Page**

7-1. Introduction

The IEEE-488 Interface turns the Data Acquisition Unit 2620A into a fully programmable instrument for use with the IEEE Standard 488.1 (1987) interface bus (IEEE-488 bus). With the IEEE-488 Interface, the instrument can become part of an automated instrumentation system.

The IEEE-488 Interface cannot be used with the Hydra Data Logger (2625A).

7-2. Theory of Operation

7-3. Functional Block Description

The IEEE-488 Assembly (A5) requires power supply voltages, address, data and control signals from the instrument Main Assembly (A1) to operate. The A5 assembly implements the circuitry necessary to satisfy the IEEE-488.1 standard for programmable instrumentation.

7-4. IEEE-488 PCA Detailed Circuit Description (2620A Only)

The IEEE-488 PCA comprises the following functional blocks: the Main PCA Connector, the IEEE-488 Controller, and the IEEE-488 Transceivers and Connector. These three blocks are described in the following paragraphs. Refer to Section 8 for a schematic diagram of the IEEE-488 PCA.

Pin numbering for the IEEE Controller (A5U1) differs somewhat on early production units. All A5U1 pin references in this section relate to newer production units. Differences for early production units can be identified by referencing the manufacturer's number on the A5U1 chip with the information provided in Table 7-1.

Table 7-1. A5U1 Pin Differences

WD9914 (Early Production A5U1)		TMS9914A (Newer Production A5U1)	
REFERENCE	**NAME**	**NAME**	**REFERENCE**
A5U1-1	ACCRQ*	(nc)	A5U1-1
A5U1-2	ACCGR*	ACCRQ*	A5U1-2
A5U1-3	CE*	ACCGR*	A5U1-3
A5U1-4	WE*	CD*	A5U1-4
A5U1-5	DBIN	WE*	A5U1-5
A5U1-6	(nc)	DBIN	A5U1-6
A5U1-17	(nc)	D1	A5U1-17
A5U1-19	D1	D0	A5U1-19
A5U1-20	D0	CLK	A5U1-20
A5U1-21	CLK	RESET*	A5U1-21
A5U1-22	RESET*	VSS	A5U1-22
A5U1-23	VSS	TE	A5U1-23
A5U1-24	TE	REM	A5U1-24
A5U1-25	REN	IFC	A5U1-25
A5U1-26	IFC	NDAC	A5U1-26
A5U1-27	NDAC	NRFD	A5U1-27
A5U1-28	NRFD	(nc)	A5U1-28

7-5. Main PCA Connector

The IEEE-488 PCA interfaces to the Main PCA through a 26-pin, right-angle connector (A5J1). This connector routes the 8-bit data bus, the lower three bits of the address bus, memory control, system clock, and address decode signals from the Main PCA to the IEEE-488 PCA. The IRQ2* interrupt request signal is routed from the IEEE-488 PCA to the Main PCA. The IEEE-488 PCA is powered by the +5.1V dc power supply (VCC). The IEEE-488 PCA is sensed by the Microprocessor on the Main PCA through the connection of logic common to the option sense signal OPS* (A5J1-22).

7-6. IEEE-488 Controller

The IEEE-488 Controller (A5U1) is an integrated circuit that performs the transfer of information between the IEEE-488 standard bus and the Main PCA Microprocessor (A1U4). Once it has been programmed by the Microprocessor via the eight-register microprocessor interface, A5U1 performs IEEE-488 bus transactions independently until it must interrupt the Microprocessor for additional information or data.

The IEEE-488 Controller is clocked by a 1.2288-MHz square-wave clock. This clock (A5U1-20) is generated by the Microprocessor. The IEEE-488 Controller uses this clock to run the internal state machines that handle IEEE-488 bus transactions. The IEEE-488 Controller is reset when the system RESET* signal (A5U1-21) is low.

For each character that it receives or transmits, the IEEE-488 Controller generates an interrupt to the Microprocessor. These interrupts are generated by driving the open-drain interrupt output A5U1-10 low. This signal drives the IRQ2* input to the Microprocessor low. When the Microprocessor responds to the interrupt and takes the necessary actions by reading and writing registers in the IEEE-488 Controller, A5U1-10 goes high again. Resistor A5R1 provides a pull-up termination on open-drain interrupt output A5U1-10.

When the Microprocessor performs a memory cycle to the IEEE-488 Controller, the lower three bits of the address bus select the register being accessed in A5U1. When a memory read cycle is performed, chip-enable A5U1-4 goes low, and A5U1-6 (DBIN) goes high. These actions enable A5U1, driving the contents of the selected register onto the data bus to the Microprocessor. When a memory write cycle is performed, chip-enable A5U1-4 goes low, and A5U1-5 (WE*) goes first low and then high to latch the data being driven from the Microprocessor into the IEEE-488 Controller.

The IEEE-488 Controller interfaces to the IEEE-488 Transceivers using an eight-bit data bus, eight interface signals, and two transceiver control signals (A5U1-33 and A5U1-23).

The controller-in-charge signal (A5U1-33), which should always be high, controls the direction of the SRQ, ATN, IFC, and REN IEEE-488 transceivers in A5U3.

The talk enable output (A5U1-2) is either low when the IEEE-488 Controller is not addressed to talk or high when the controller is addressed to talk. This signal determines the direction of all IEEE-488 Transceivers except SRQ, ATN, IFC, and REN.

7-7. IEEE-488 Transceivers/Connector

The IEEE-488 Transceivers (A5U2 and A5U3) are octal transceivers that are specifically designed to exhibit the proper electrical drive characteristics to meet the IEEE-488 standard. These transceivers are configured to match the control signals available on the IEEE-488 Controller. Assuming that A5U1-33 is always high, Table 7-2 describes the transceiver direction control. The IEEE-488 Transceivers connect to a 24-position connector (A5J2), which mates with the ribbon cable leading to the IEEE-488 connector mounted at the rear of the instrument chassis.

Table 7-2. IEEE-488 Transceiver Control

TRANSCEIVER	TE = 0 (LISTENER)	TE = 1 (TALKER)
DI01..DI08	Receiver	Transmitter
SRQ	Transmitter	Transmitter
ATN	Receiver	Receiver
EOI	Receiver	Receiver (ATN = 0)
-	Receiver	Transmitter (ATN = 1)
DAV	Receiver	Transmitter
NRFD	Transmitter	Receiver
NDAC	Transmitter	Receiver
IFC	Receiver	Receiver
REN	Receiver	Receiver

7-8. General Maintenance

7-9. Removing the IEEE-488 Option

Remove the instrument cover as shown in Figure 7-1. Then remove the IEEE-488 Option with the following procedure:

Note

Parts referenced by letter (e.g., A) are shown in Section 3 (Figure 3-4.)

1. From the bottom of the instrument, locate the IEEE-488 PCA (N). This pca is connected to the front of Main PCA, with a ribbon cable (O) leading across both pca's to the Rear Panel. Refer to Figure 7-1.
2. Use needle nose pliers to disconnect the 24-line cable assembly at the IEEE-488 PCA, alternately pulling on each end of the cable connector. Leave the other end of this cable attached to its Rear Panel connector.
3. Remove the 6-32, 1/4-inch panhead Phillips screw (P) securing the IEEE-488 PCA. See Figure 7-1.
4. Disengage the IEEE-488 PCA by sliding it away from the Main PCA.

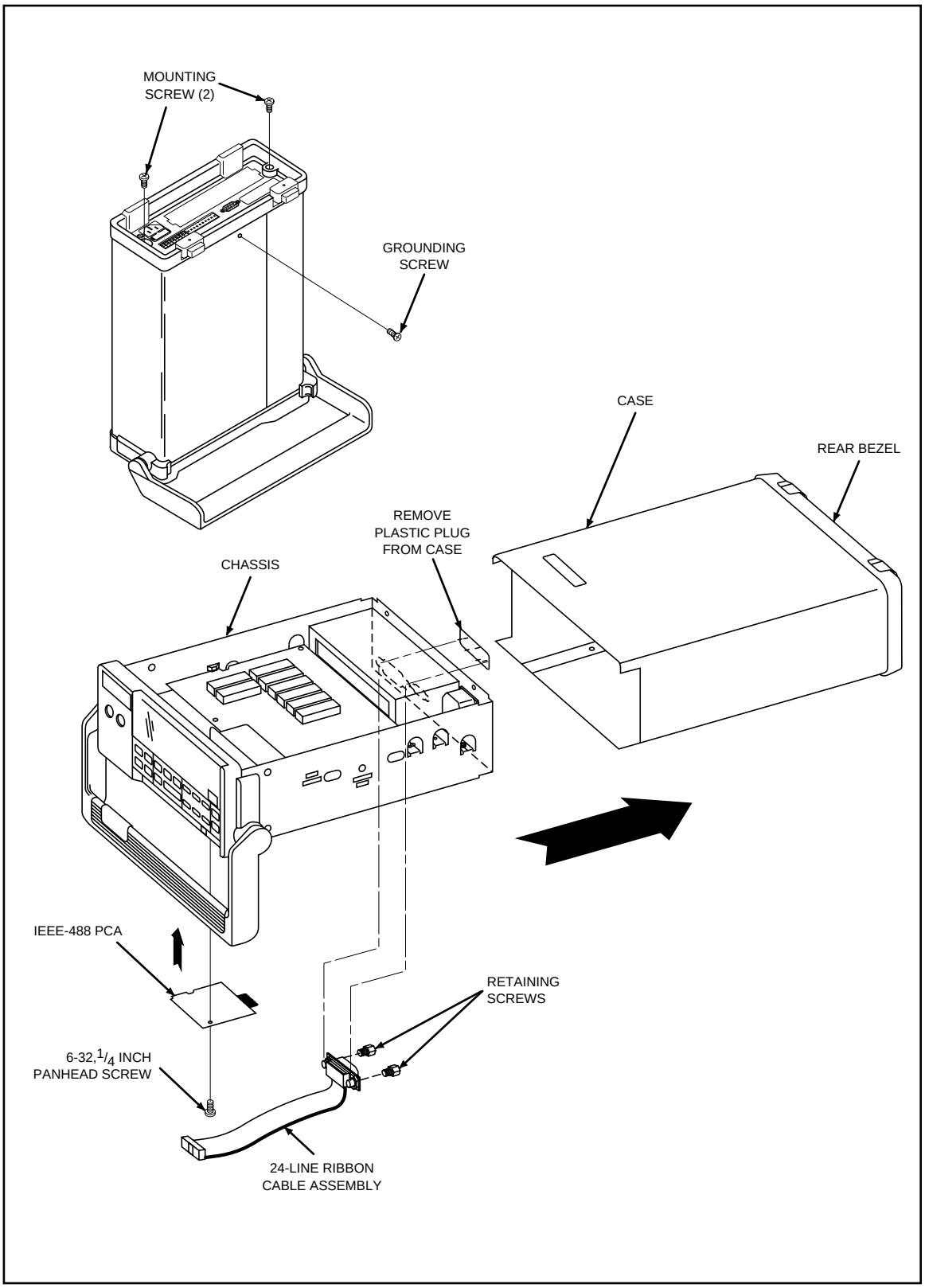


Figure 7-1. Installation

7-10. Installing the IEEE-488 Option

1. Place the IEEE-488 PCA into position so that the edge of the pca fits in the chassis guide. Then line up connecting pins with the matching connector on the Main PCA, and slide the pca into position.
2. Install the single 6-32, 1/4-inch panhead Phillips head screw in the corner of the IEEE-488 PCA.
3. If necessary, attach the rear panel connector using 7 mm nut driver.
4. At the pca, attach the ribbon cable leading from the rear panel connector.

7-11. Performance Testing

Use the following performance test program to verify operation of the IEEE-488 Interface. This program is written for use with the Fluke 1722A Instrument Controller and its interpreted BASIC language. The program may be adapted to the language of any IEEE-488 controller.

```
140 IA% = 0%!                              instrument IEEE address
150 S% = -1%!                              initialize spl response
160 TERM!                                  terminate input only on EOI
170 INIT PORT 0                            ! initialize IEEE-488 bus
180 CLEAR @@IA%                            ! selective device clear
190 PRINT @@IA%,"*cls"                     ! clear instrument status
200 ON SRQ GOTO 530                        ! enable SRQ interrupt
210 PRINT @@IA%,"*cls;*sre 16;*idn?"       ! SRQ on Message Available
220 WAIT 500% FOR SRQ                      ! allow time to execute commands
230 IF S% >>= 0% THEN 260
240 PRINT "Instrument failed to generate a Service Request"
250 STOP
260 PRINT "Serial Poll =";S%;"(should be 80)."
270 PRINT "Identification Query Response = ";R$
280 STOP
500 !
510 ! Service Request interrupt
520 !
530 S% = SPL(IA%)                          ! get instrument serial poll status
540 IF S% AND 16% THEN 550 ELSE 560
550 INPUT LINE @IA%,R$                     ! if MAV set get the response
560 RESUME 230                             ! end of SRQ interrupt
999 END
```

This performance test communicates to an instrument that has been configured for IEEE-488 operation at address 0. Lines 170 and 180 initialize the IEEE-488 bus and send a selective device clear to the instrument. A multiple byte command is sent to the instrument (by line 190) to clear the instrument status. Another command sequence (including a query) is sent to the instrument by line 210; the instrument asserts Service Request (SRQ) to signal that a response is available. Lines 530 through 560 first poll the instrument for status, then input the response from the instrument. Lines 230 through 270 test for proper operation and print the results.

7-12. Troubleshooting

7-13. Power-Up Problems

The following discussion identifies probable fault areas if the installation of an IEEE-488 Option causes power-up failure for the instrument. The problem is probably a short on A5J1; the Microprocessor on the Main Assembly is prevented from accessing ROM and RAM correctly.

- First check if VCC is shorted to GND on the IEEE Assembly.
- The short may also be caused by an interface signal to either VCC, GND, or another interface signal. The logical signals to check are D7 .. D0, A2 .. A0, RD*, IEEE*, WR*, E, RESET*, and IRQ2*.
- The short may be due to a CMOS input that has been damaged due to static discharge; the short is then detectable only when the circuit is powered up. Use an oscilloscope to check activity on each of the interface signals. Verify that signals are able to transition normally between 0 and 5V dc.

7-14. Communication Problems

7-15. Failure to Select IEEE-488 Option

IEEE-488 Interface selection procedures are described in Section 3 of the Hydra User Manual.

If the IEEE-488 option is not detected by instrument software, there may be a problem with the OPS* signal. The IEEE option grounds the OPS* signal (A5J1-22), which is normally pulled up to VCC on the instrument Main PCA. The Microprocessor determines that the IEEE-488 option is not installed if OPS* (A1U4-29) is high during the power-up option detection.

7-16. Failure to Handshake on IEEE-488 Bus

After power-up or when the active computer interface is changed from RS-232 to IEEE-488, the Microprocessor sends six write cycles to initialize A5U1. The IRQ2* interrupt is then enabled, and the serial poll status byte is initialized. At this point, the IEEE-488 option is ready to respond to transactions on the IEEE-488 bus.

7-17. Failure to Enter Remote

If the IEEE-488 option does not enter remote, check that the remote/local control circuit is operating properly. When the IEEE-488 option is the active instrument interface, the remote/local control state is polled by the Microprocessor approximately every 400 ms. Normally, A5U1-4 goes low for approximately 800 ns during the read cycle that checks the state of A5U1. If D(0) (A5U1-11) is low during the read cycle, A5U1 is in the local state. If A5U1-11 is high during the read cycle, A5U1 is in the remote state. When A5U1 indicates that it is in remote, the REM indicator on the display is turned on.

7-18. Failure to Receive Multiple Character Commands

Monitor the IRQ2* interrupt signal from A5U1-10 during attempts to communicate with the instrument. Each byte received with the ATN signal (A5U1-31) high should cause the interrupt signal to go low. Verify that the signal arrives at A5J1 properly. An interrupt not detected by A1U4 will remain low indefinitely. A5U1-10 will go high only when both the interrupt is detected and the received byte is removed from A5U1 by A1U4.

7-19. Failure to Transmit Query Responses

Check that TE (A5U1-23) goes high when the interface is addressed to talk. This signal must go high to allow the bus interface transceivers to change the direction of DIO1 through DIO8, EOI, DAV, NRFD, and NDAC. Verify that each of these signals passes through A5U2 and A5U3 properly.

7-20. Failure to Generate an End or Identify (EOI)

When the IEEE-488 option sends the Line Feed termination character at the end of a response, the EOI signal should also be set true. When EOI is true, A5U1-30 should go low. Follow this signal from A5J2 through A5U3 to A5U1.

7-21. Failure to Generate a Service Request (SRQ)

When a Service Request is being generated, A5U1-32 should be low. Follow this signal through A5U3 to connector A5J2. When a Serial Poll (SPL) is performed by the IEEE-488 bus controller, A5U1-32 will go high again.

Note

If the instrument is in the remote state without front panel lockout (i.e., REMS), a service request can be sent from the front panel by pressing the up arrow button.

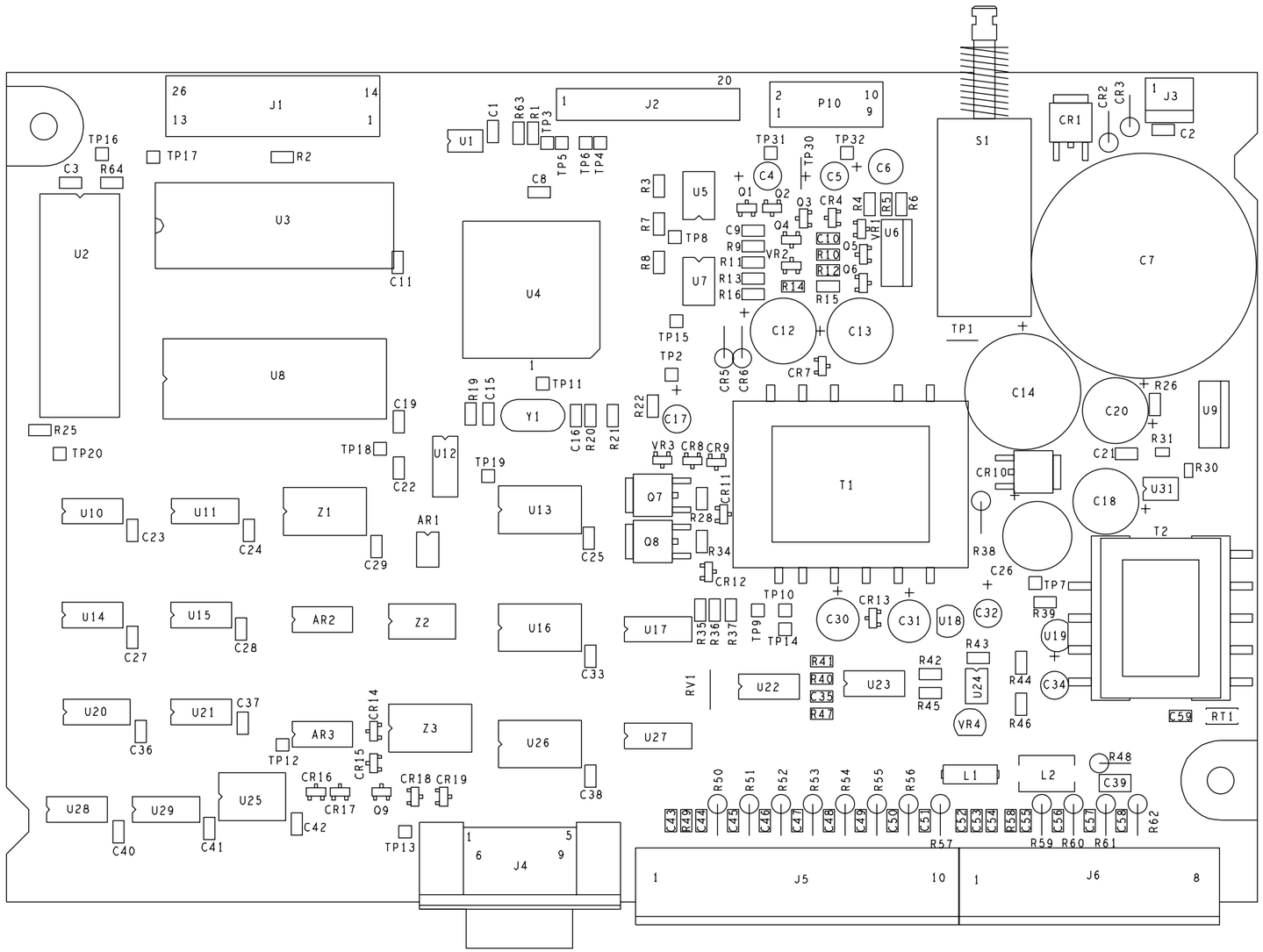
7-22. List of Replaceable Parts

Refer to Section 6 for an illustrated parts list of the IEEE-488 Option.

7-23. Schematic Diagram

The schematic diagram for the IEEE-488 Option is included in Section 8 of this manual.

Chapter 8
Schematic Diagrams



NOTE: TP2-TP20, TP31 AND TP32 ARE NOT COMPONENTS.

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Figure 8-1. A1 Main PCA (2620A/2625A)

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W 5%.
   ALL CAPACITOR VALUES ARE IN MICROFARADS.

REF DES	POWER SUPPLY PIN NUMBERS					
	VCC	GND	VEE	VDDR	COM	DO_GND
A01AR1	8	4	-	-	-	-
A01AR2	4	11	-	-	-	-
A01AR3	4	11	-	-	-	-
A01U1	8	5	-	-	-	-
A01U2	14,16	1,2,5,7,26	-	-	-	-
A01U3	26,28	14	-	-	-	-
A01U4	5,36	2,6,45	-	-	-	-
A01U5	5	-	-	1	-	-
A01U7	-	-	-	-	4	-
A01U8	28	14,22	-	-	-	-
A01U9	3	-	-	-	-	-
A01U10	14	7	-	-	-	-
A01U11	16	5,8	-	-	-	-
A01U12	14	7	-	-	-	-
A01U13	20	10	-	-	-	-
A01U14	4,9,10,14	7	-	-	-	-
A01U15	14	7	-	-	-	-
A01U16	20	10	-	-	-	-
A01U17	-	-	-	-	-	8
A01U20	16	8	-	-	-	-
A01U21	13,14	7	-	-	-	-
A01U22	-	7,11,12	-	-	-	-
A01U23	-	7,11,13	-	-	-	-
A01U24	-	4,5,6	-	-	-	-
A01U25	1,16	2,6,9,14	8	-	-	-
A01U26	20	10	-	-	-	-
A01U27	-	-	-	-	-	8
A01U28	14	7	-	-	-	-
A01U29	16	8,15	-	-	-	-
A01U31	5	2,3,4	-	-	-	-
A01Z2	16	-	-	-	-	-

REFERENCE DESIGNATIONS		
LAST USED		NOT USED
AR	AR3	
C	C59	
CR	CR19	
J	J6	
L	L2	
P	P10	P1-P9
Q	Q9	
R	R64	R17-18,23-24,27,29,32-33
RT	RT1	
RV	RV1	
S	S1	
T	T2	
TP	TP32	TP21-29
U	U31	U30
VR	VR4	
W	W1	
Y	Y1	
Z	Z3	

INTERCONNECT DIAGRAM

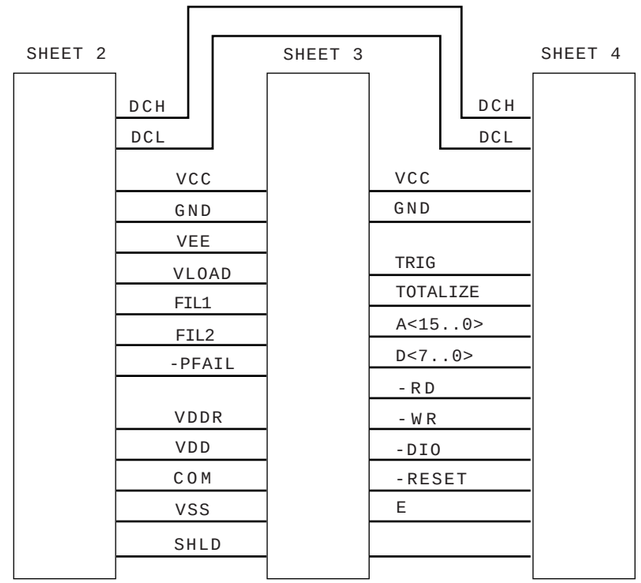

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Figure 8-1. A1 Main PCA (2620A/2625A) (cont)

RAW SUPPLY
1/8A SB
250V
L
N
EG
T401
J3
CR1
MBRD360
CR3
1N5397
CR2
1N5397
C2
.033
S1
P1
P2
C1
C2
RT1
RXE065
C59
180PF
DCL
R48
10K
C39
.047
C7
10000
35V
DCH
DCL
PFAIL*
POWER FAIL DETECTION
R39
63.4K
1%
R41
11.0K
1%
R43
39K
R45
1.0M
1%
VCC
R42
10K
U24
LM393DT
VR4
LM385
1.23V
U19
TL317
IN OUT
ADJ
TP7
IBIAS
R44
1.30K
1%
C34
1.0
R46
4.02K
1%
INGUARD SUPPLIES
U6
LM317
IN OUT
ADJ
+5.6V
VDDR
SH3
R6
3.32K
1%
R5
1.00K
1%
C6
10
63V
+5.2V
VDD
SH3
R13
20
Q1
MMBT3906
Q2
MMBT3906
C9
180PF
VR2
1N5233
6.0V
TP31
C4
1.0
50V
R11
47K
R9
4.7K
Q4
MMBT3904
TP30
COM
COM
SH3
INVERTER
T1
CR5
MBR140
CR6
MBR140
CR7
BAW56
C12
470
16V
C13
470
16V
R14
10K
R4
10K
R12
47K
R10
4.7K
Q3
MMBT3906
VR1
1N5232
5.6V
C10
180PF
C5
1.0
50V
Q6
MMBT3904
CR4
BAS16
TP32
R15
33
Q5
MMBT3904
VSS
SH3
-5.6V
SHLD
SH3
TP5
TP6
FIL1
SH3
5VAC
FIL2
SH3
OUTGUARD SUPPLIES
CR9
MMBD7000
CR8
MMBD7000
TP4
-30V
VLOAD
SH3
VR3
1N5235B
6.8V
C17
2.2
50V
UNUSED
U31
LM358DT
T2
SWITCHER
U9
LT1170
VIN VSW
FB
GND VC
C26
47
100V
CR10
MBRD360
LM358DT
U31
R26
100
C21
.1
25V
R31
11.0K
1%
C20
220
35V
C18
220
35V
R30
45.3K
1%
C14
2200
10V
VCC
+5.1V
TP2
TP1
UNUSED
U23
HCU04
U24
LM393DT
U22
HC74
R34
470
CR12
BAS16
TP9
Q8
CR11
BAS16
TP10
Q7
R28
470
R38
0.02
U18
79L05
IN OUT
GND
CR13
MMBD7000
C30
47
50V
C31
47
50V
C32
1.0
50V
R22
47K
TP3
-5.0V
VEE

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Figure 8-1. A1 Main PCA (2620A/2625A) (cont)

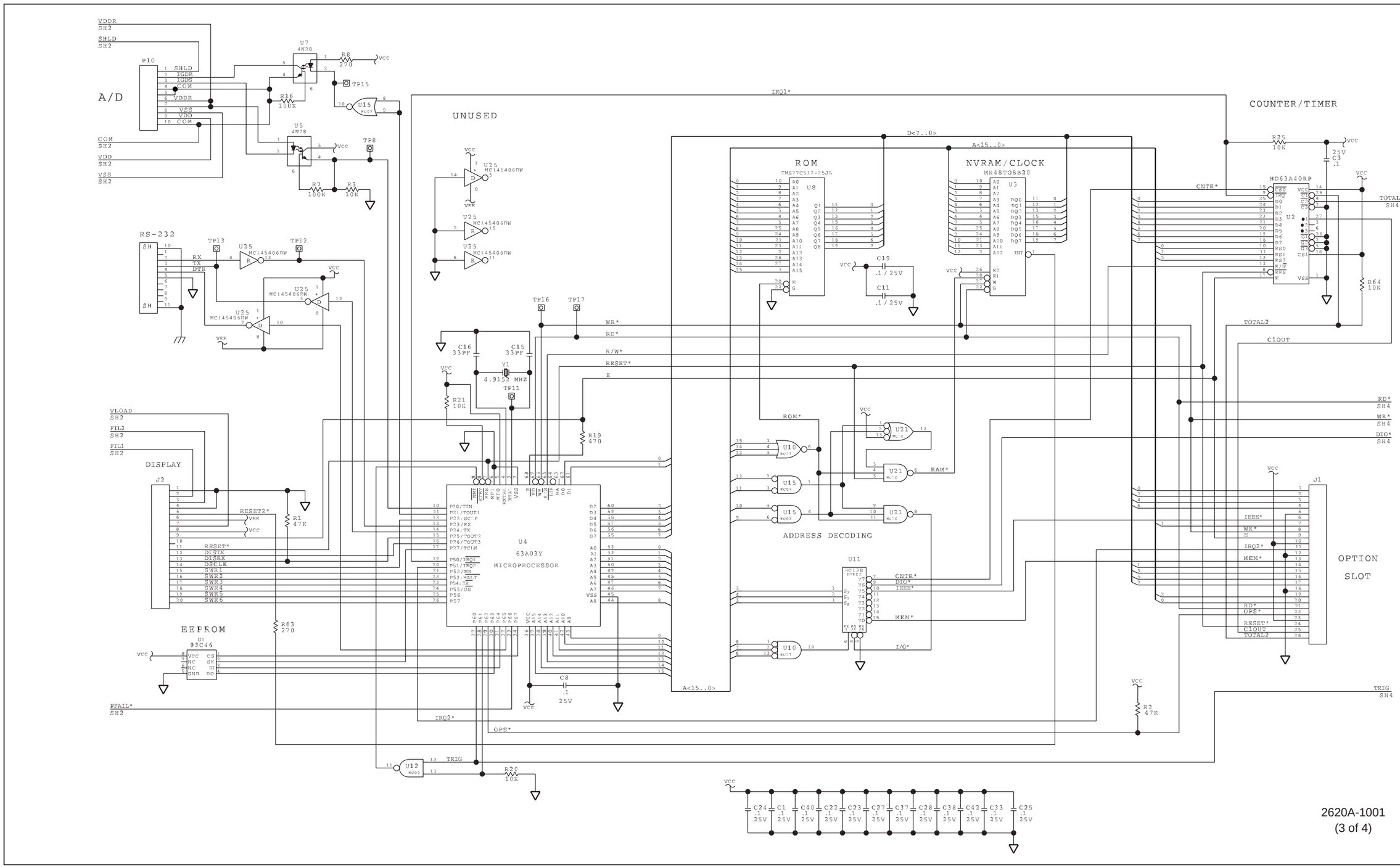

Figure 8-1. A1 Main PCA (2620A/2625A) (cont)

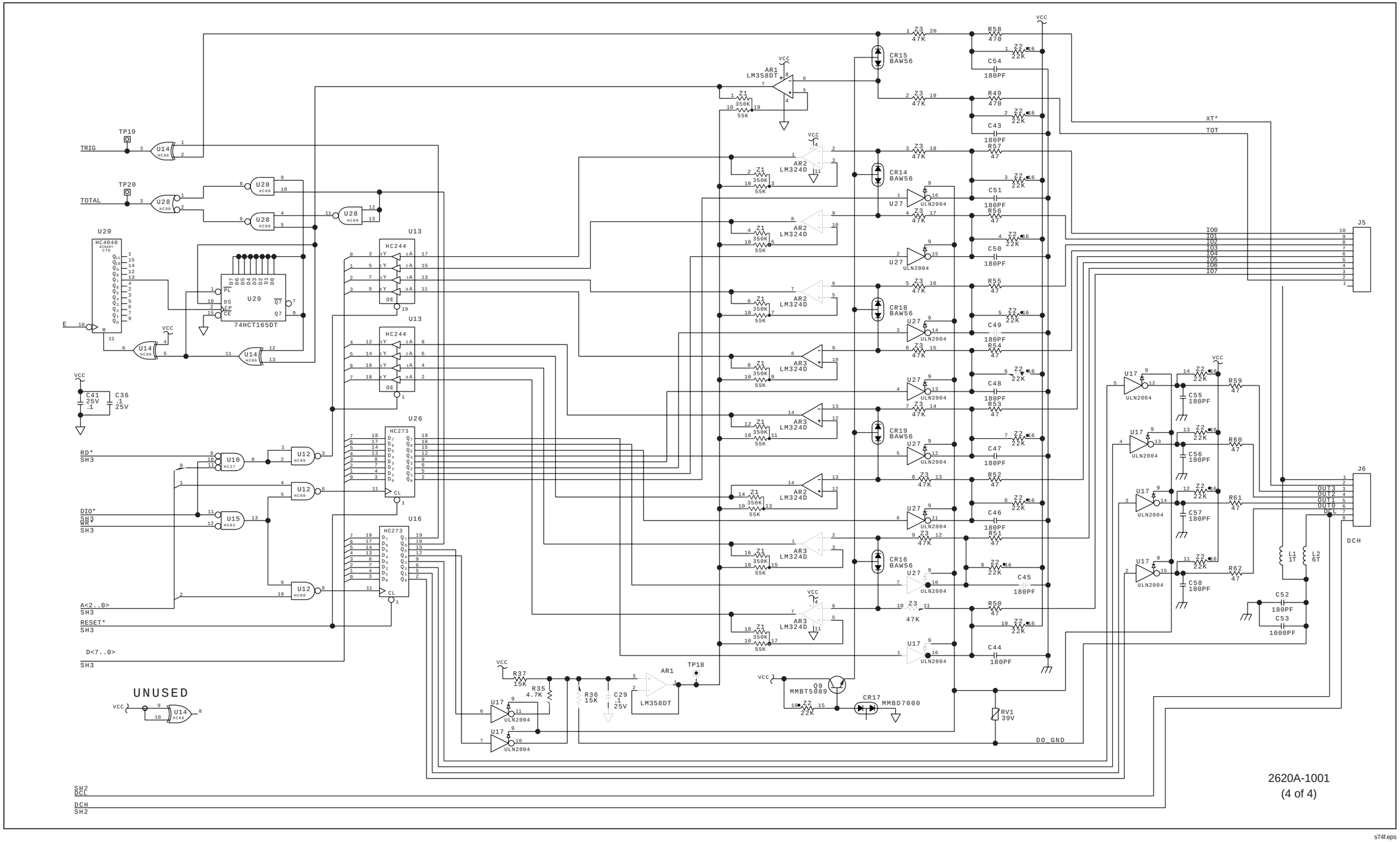

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Figure 8-1. A1 Main PCA (2620A/2625A) (cont)

REF DES	POWER SUPPLY PIN NUMBERS				
	GND	VCC (5.0V dc)	VBB (+5V dc)	COM	VDDR (5.6V dc)
A1U1	3, 13, 23,	18, 28,	--	--	--
--	29, 34,	39, 62,	--	--	--
--	44, 50,	72, 74,	--	--	--
--	57, 67,	83, 99,	--	--	--
--	73, 84,	112, 131	--	--	--
--	102, 107,	--	--	--	--
--	116, 126	--	--	--	--
A1U2	2, 5, 7,	14	--	--	--
--	9, 12	--	--	--	--
A1U3	11	4	--	--	--
A1U4	11	4	--	--	--
A1U5	4	--	--	--	1
A1U7	--	--	--	4	--
A1U8	4	8	--	--	--
A1U9	--	4	--	--	--
A1U10	3	2	1	--	--
A1U11	10	20	--	--	--
A1U12	1, 2, 12,	--	24	--	--
--	21	--	--	--	--
A1U13	9	1, 16	--	--	--
A1U14	16	32	--	--	--
A1U15	7, 8, 9	16	--	--	--
A1U16	16	32	--	--	--
A1U20	16	--	32	--	--
A1U22	7, 11, 12	--	--	--	--
A1U23	7, 11, 13	--	--	--	--
A1U24	16	--	32	--	--
A1U25	4, 16, 28,	3, 6, 27,	--	--	--
--	52, 53,	29, 41,	--	--	--
--	66, 77,	54, 55,	--	--	--
--	93	56, 79,	--	--	--
--	--	91	--	--	--
A1U26	7	--	9, 12, 14	--	--
A1Z2	--	16	--	--	--

Reference Designations		
Lasted Used		**Not Used**
BT	BT1	--
C	C76	C27, 37
CR	CR21	--
J	J6	--
L	L2	--
P	P10	P1-3, 5-9
Q	Q10	--
R	R118	R76
RT	RT1	--
RV	RV1	--
S	S1	--
T	T3	--
TP	TP32	TP16-17, 19, 21-29
U	U27	U21
VR	VR3	--
W	W4	W2
Y	Y1	--
Z	Z3	--

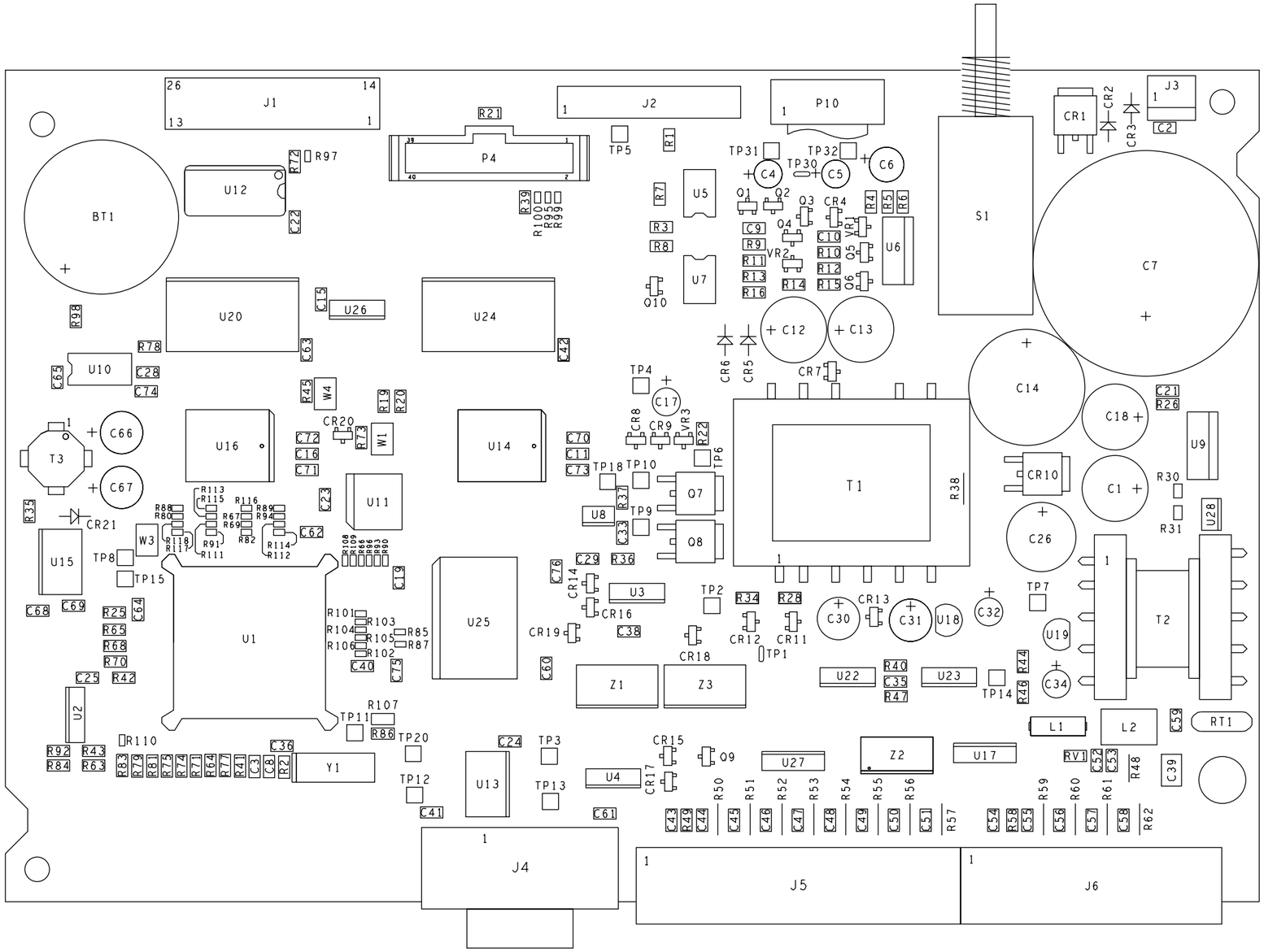

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Figure 8-2. A1 Main PCA (2635A)

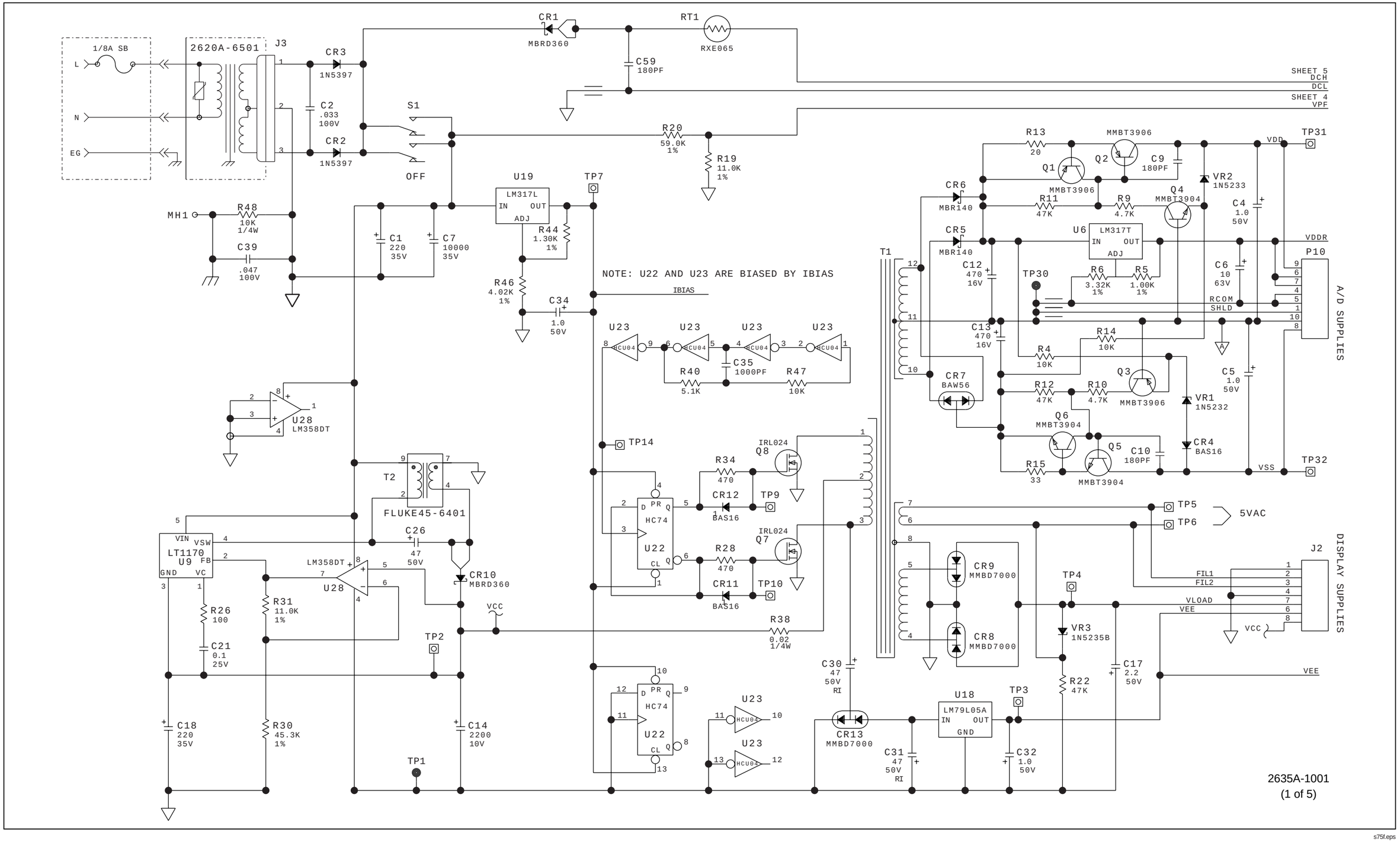

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Figure 8-2. A1 Main PCA (2635A) (cont)

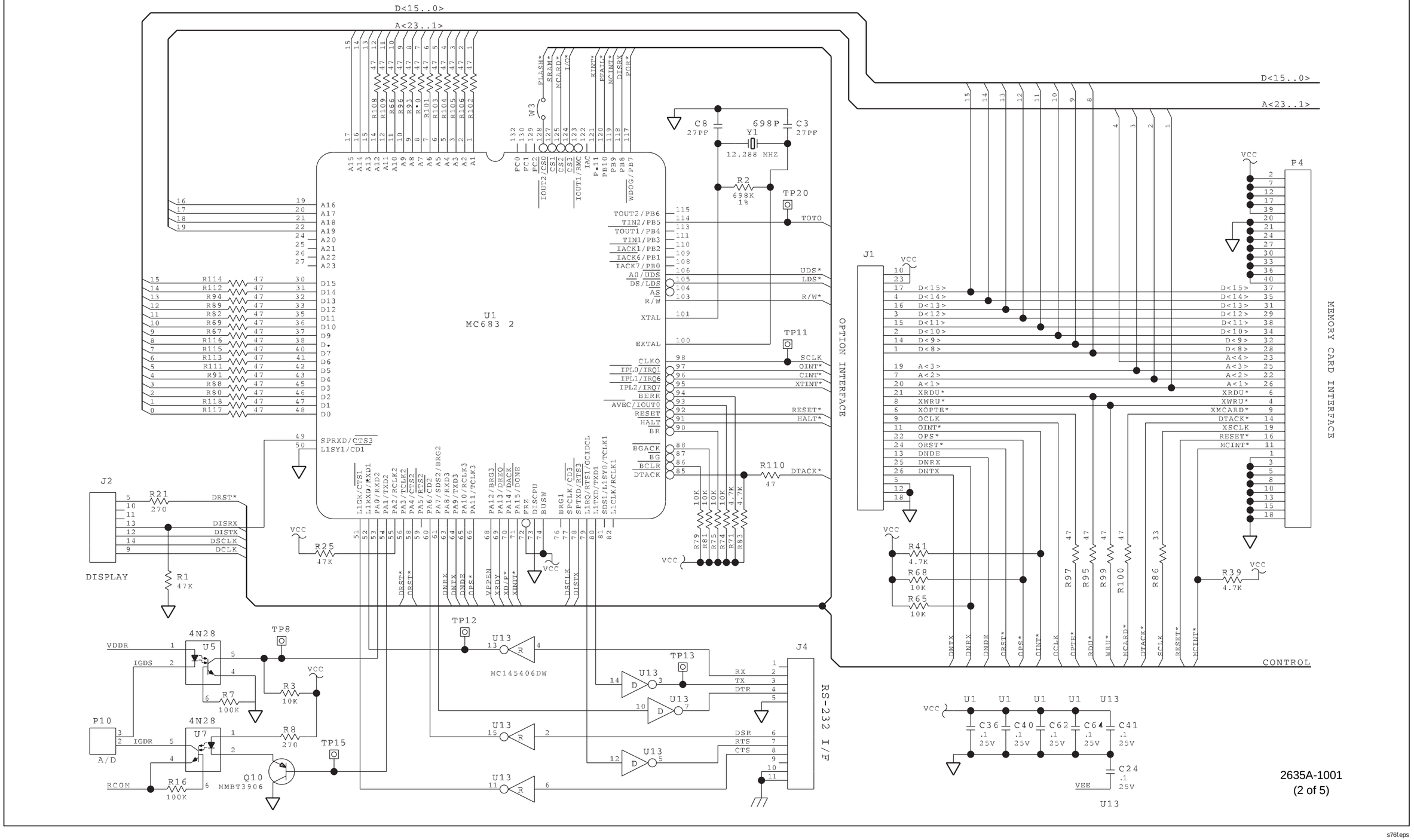

Figure 8-2. A1 Main PCA (2635A) (cont)

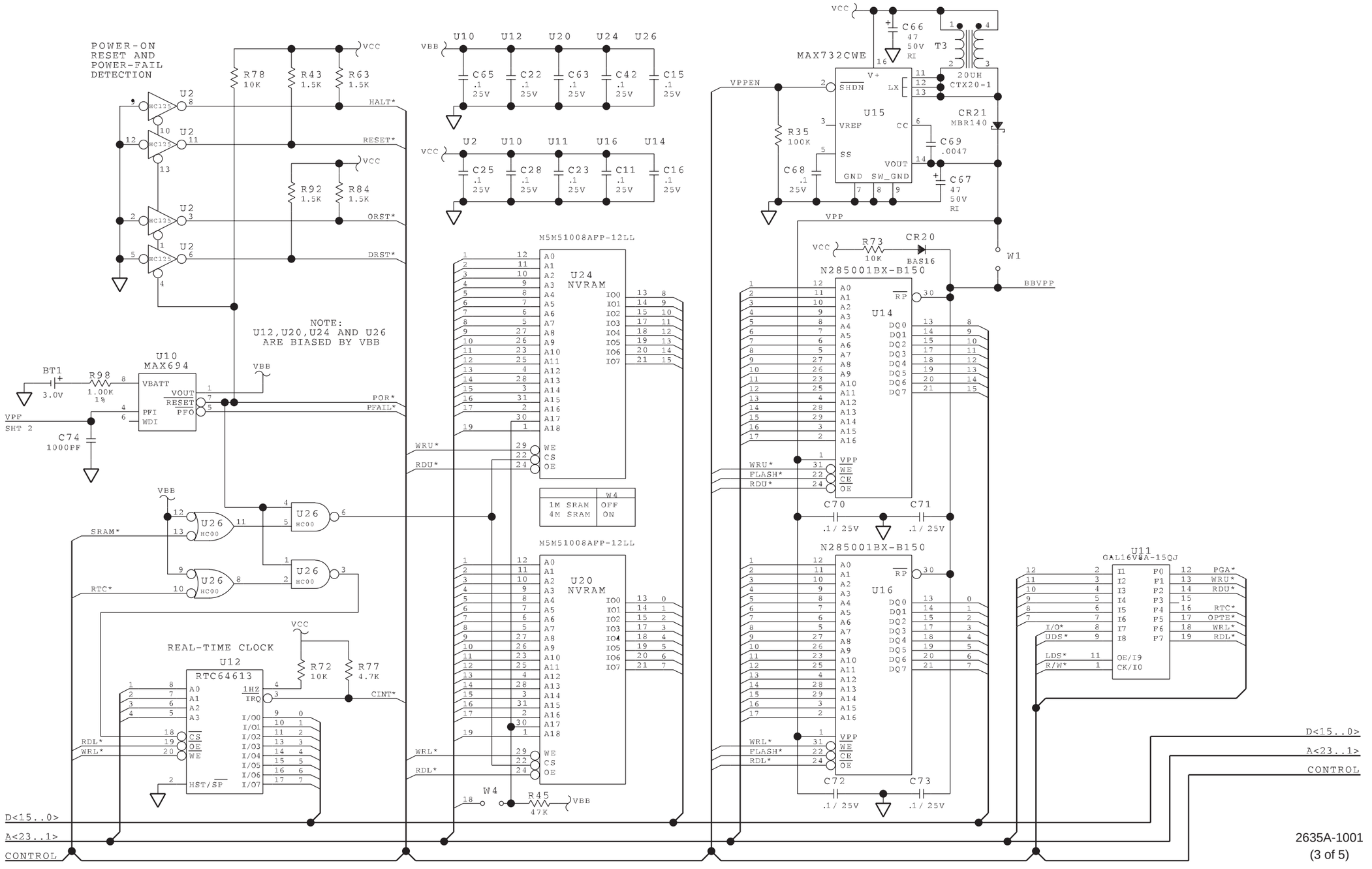

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Figure 8-2. A1 Main PCA (2635A) (cont)

TABLE	
P/N	NOUN
931985	2635A
949503	2635A-1MB
949508	2635A-2MB

J2
KEYBOARD I/F
15 SWR1
16 SWR2
20 SWR6
19 SWR5
17 SWR3
18 SWR4

A<23..1>
XTI
RDU*
OCLK
R87 47
PGA*
SCLK
R107 33
XRDY
RESET*
VCC
D<15..0>
KINT*
CONTROL

U25
XC3030-70PQ100C
CS0-IO 88
CS1-IO 93
D0-DIN-IO 100
D1-IO 98
D2-IO 94
D3-IO 92
D4-IO 89
D5-IO 87
D6-IO 83
D7-IO 81
TCLKIN-IO 30
XTL1-BCLKIN-IO 82
XTL2-IO 76
CCLK 2
M0-RTRIG 54
M1-RDATA 52
M2-IO 56
RDY/BUSY-RCLK-IO 99
RESET 78
PWRDWN 29
PAD5 22 PAD6 21 PAD15 11 PAD16 10 PAD25 97 PAD26 96 PAD27 95 PAD31 90 PAD35 86 PAD36 85 PAD37 84 PAD42 75 PAD43 74 PAD44 73 PAD45 72 PAD46 71 PAD47 70 PAD48 69 PAD49 68 PAD50 67 PAD52 64 PAD53 63
PAD54 62 PAD55 61 PAD56 60 PAD58 58 PAD61 51 PAD62 50 PAD63 49 PAD64 48 PAD65 47 PAD66 46 PAD67 45 PAD68 44 PAD69 43 PAD70 42 PAD71 40 PAD72 39 PAD73 38 PAD74 37 PAD75 36 PAD76 35 PAD77 34 PAD78 33 PAD79 32
A0-WS-IO 5
A1-CS2-IO 6
A2-IO 8
A3-IO 9
A4-IO 13
A5-IO 15
A6-IO 18
A7-IO 20
A8-IO 24
A9-IO 26
A10-IO 25
A11-IO 23
A12-IO 19
A13-IO 17
A14-IO 14
A15-IO 12
INIT-IO 65
HDC-IO 57
LDC-IO 59
DOUT-IO 1
DONE-PG 80

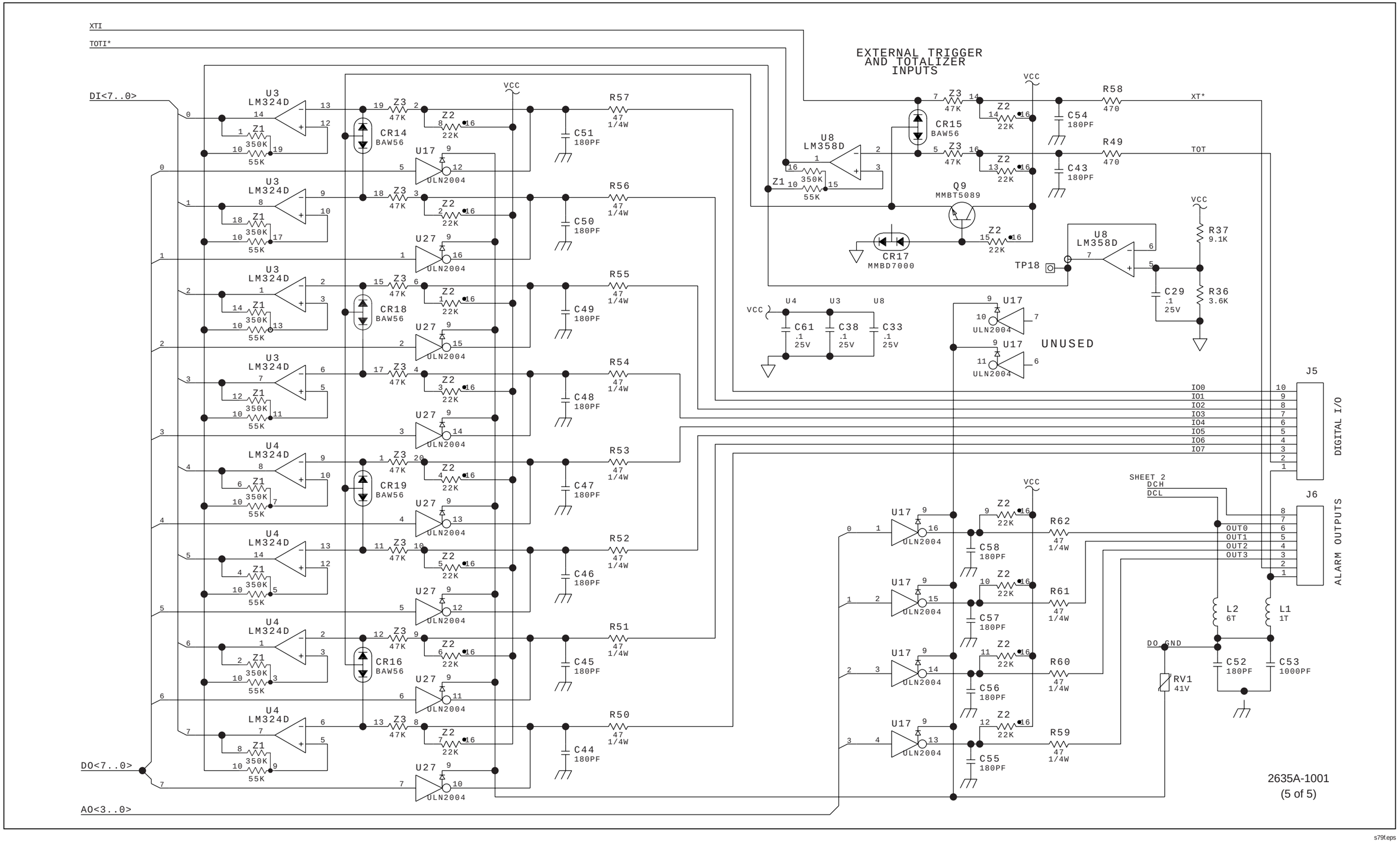
VCC
R42 10K
R70 10K
R64 10K
WRU*
TOTO
XTINT*
R85 47
DCLK
TOTI*
XINIT*
XD/P*
DI<7..0>
DO<7..0>
AO<3..0>

U25 U25 U25 U25
VCC
C60 .1 25V
C19 .1 25V
C76 .1 25V
C75 .1 25V

2635A-1001
(4 of 5)

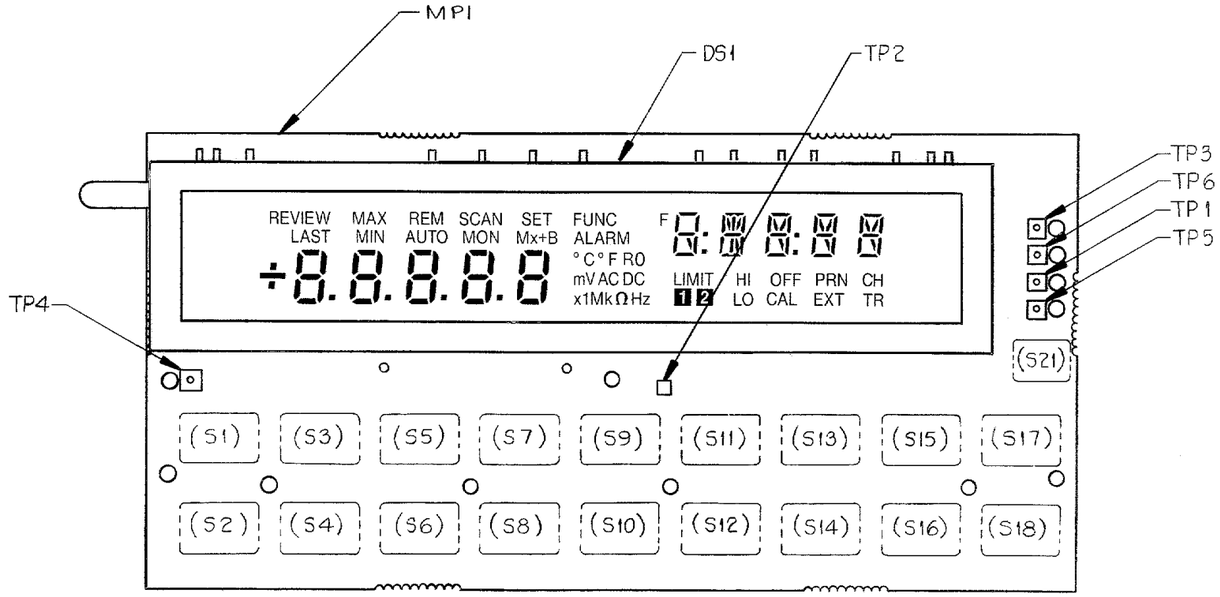
s78f.eps

Figure 8-2. A1 Main PCA (2635A) (cont)

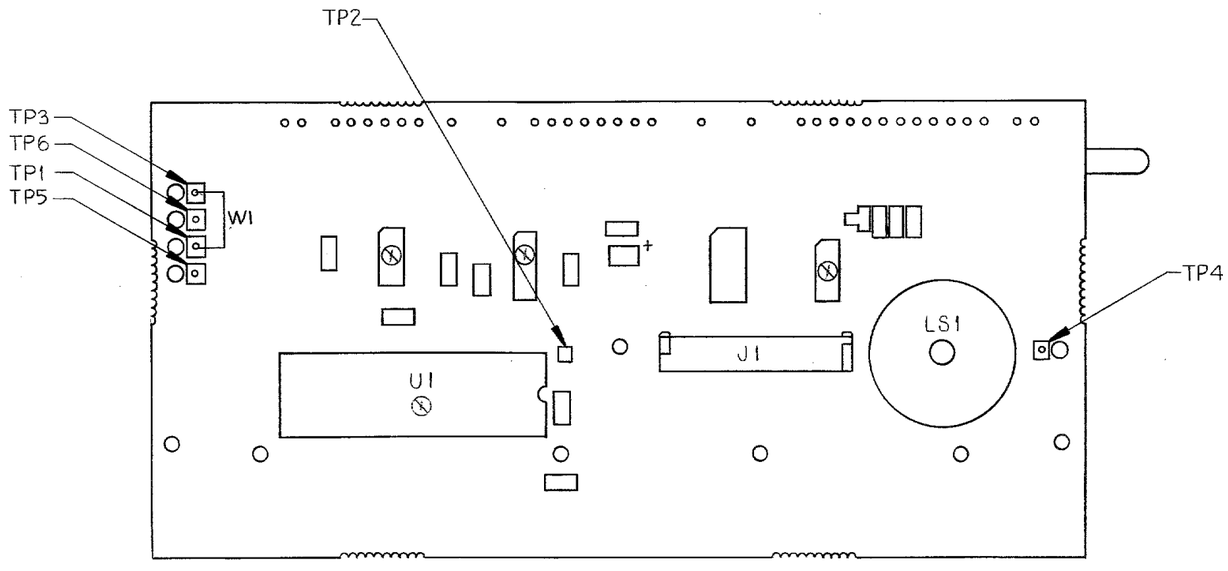


s79f.eps

Figure 8-2. A1 Main PCA (2635A) (cont)



CKT 1



CKT 2

2620A-4002

s90f.eps

Figure 8-3. A2 Display PCA

REF DES	POWER SUPPLY PIN NUMBERS			
	VCC (5.1V dc)	GND	VEE (5.0V dc)	VLOAD (-28.5 to -30.0V dc)
A2U1	21	42	4	5
A2U4	16	2, 8	--	--
A2U5	10, 16	8	--	--
A2U6	14	7, 9, 10	--	--
A2Z1	16	--	--	--

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCES ARE IN OHMS, 1/8W, +/- 5%.
2. ALL CAPACITANCES ARE IN MICROFARADS.

4 SEE DETAIL A.

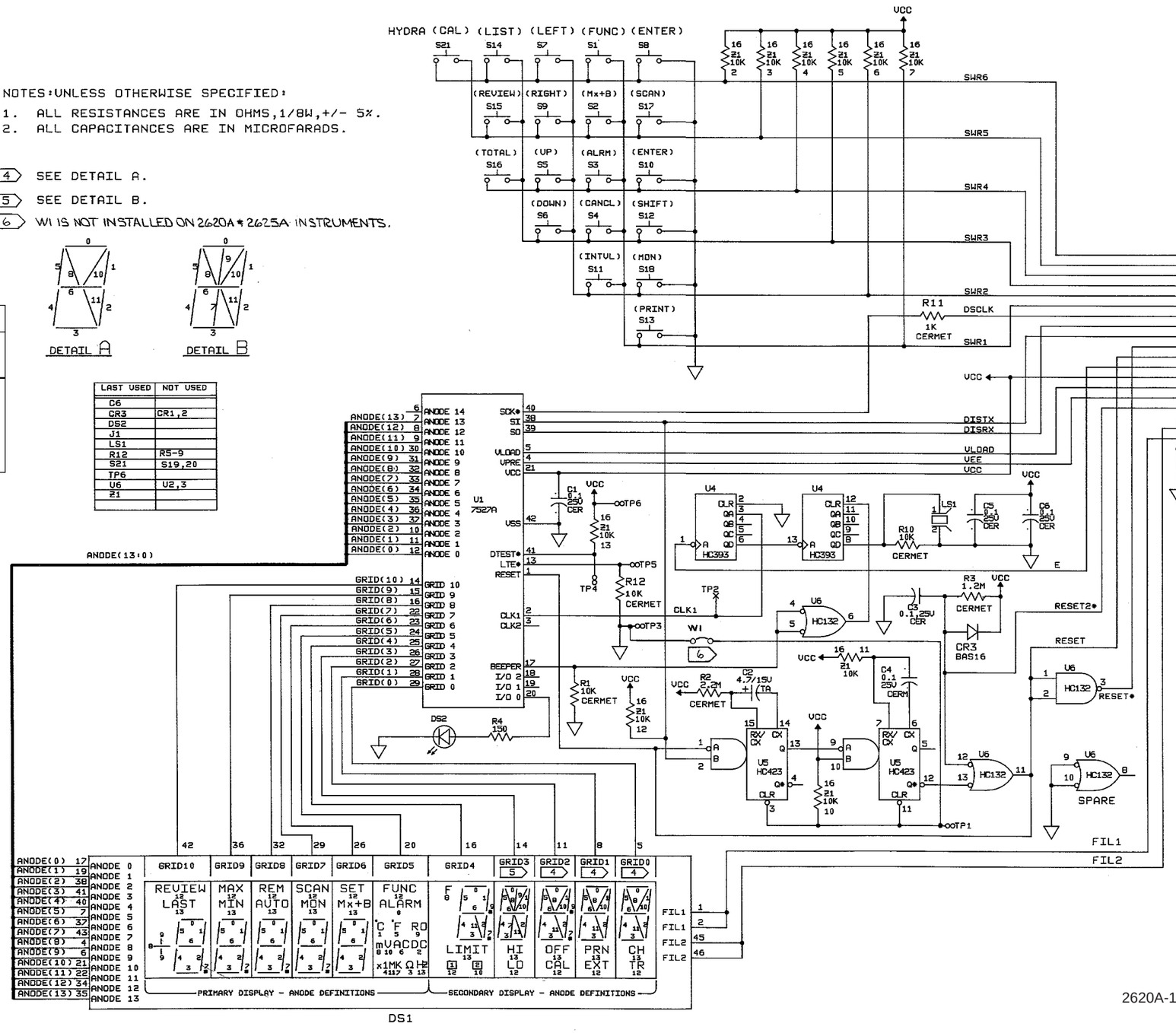
5 SEE DETAIL B.

6 W1 IS NOT INSTALLED ON 2620A & 2625A INSTRUMENTS.

DETAIL A

DETAIL B

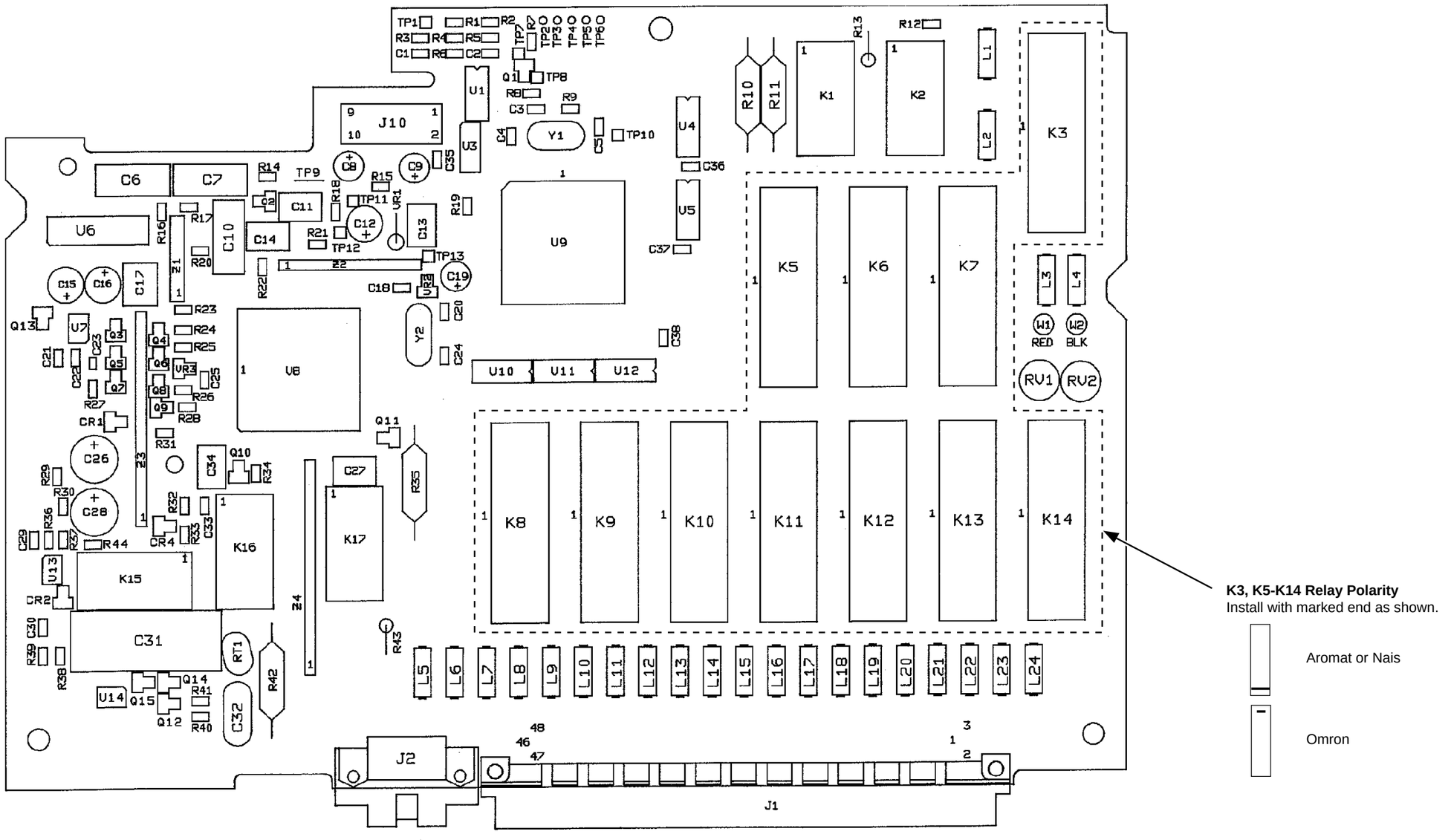
LAST USED	NOT USED
C6	
CR3	CR1,2
DS2	
J1	
LS1	
R12	R5-9
S21	S19,20
TP6	
U6	U2,3
Z1	



2620A-1002

s80c.eps

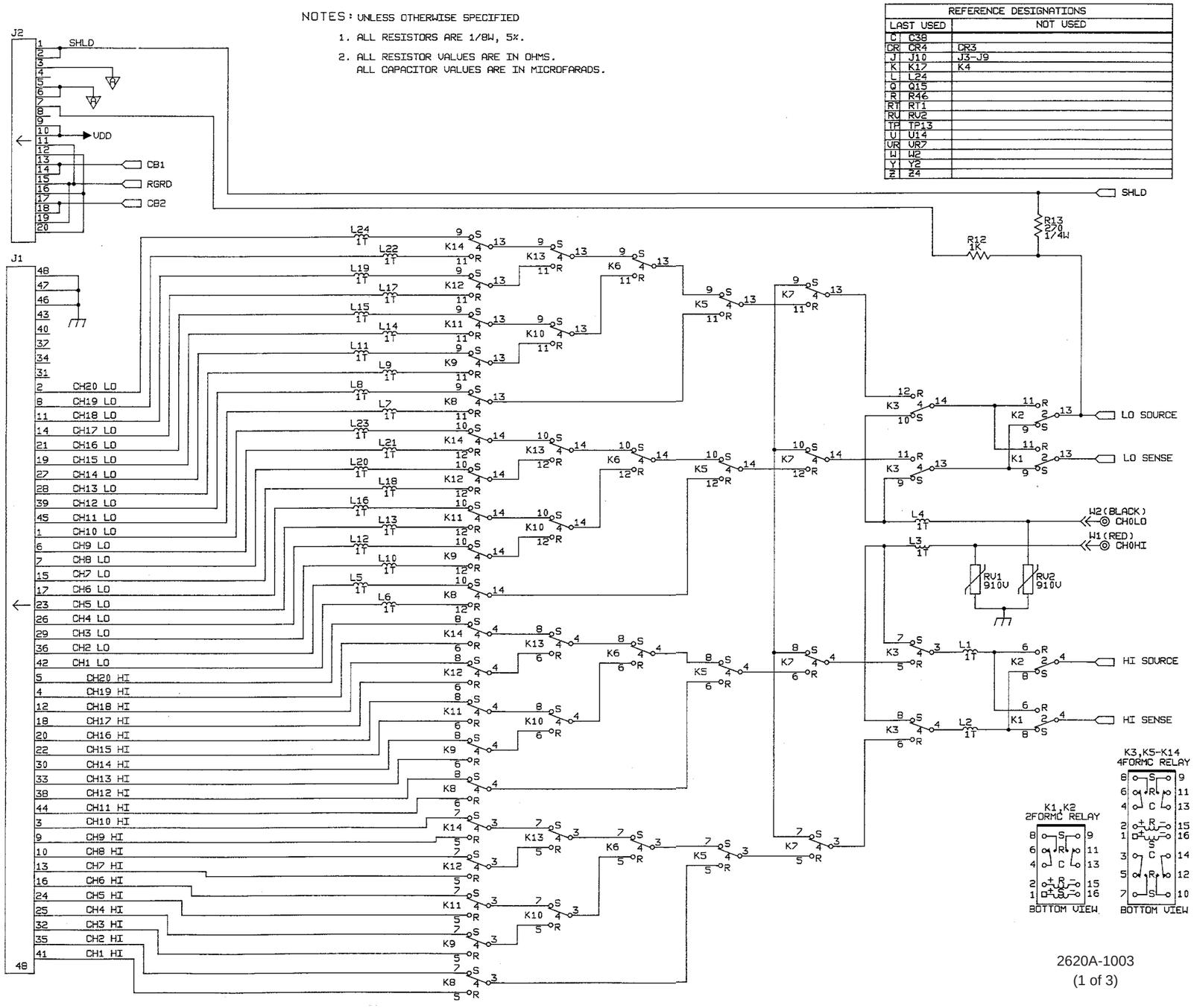
Figure 8-3. A2 Display PCA (cont)



s91c.eps

Figure 8-4. A3 A/D Converter PCA

REF DES	POWER SUPPLY PIN NUMBERS				
	VCC (5.3V dc)	VSS (5.4V dc)	ANALOG_GND	VDDR (5.6V dc)	RCOM
A3U1	3	--	10, 11, 12	--	--
A3U2	1, 16	8	6, 9	--	--
A3U3	1, 10, 11,	--	2, 7	--	--
--	12, 13, 14	--	--	--	--
A3U4	--	--	--	9	8
A3U5	--	--	--	9	8
A3U6	--	--	1, 3, 4	--	--
A3U7	--	--	3	--	--
A3U8	1	44	4, 25, 27, 38	--	--
A3U9	5, 6, 9, 36	--	2, 45	--	--
A3U10	--	--	--	9	8
A3U11	--	--	--	9	8
A3U12	--	--	--	9	8
A3U13	8	--	4	--	--
A3U14	8	4	--	--	--
A3Z1	--	--	4	--	--
A3Z2	1	--	--	--	--
A3Z3	--	--	8	--	--



s81c.eps

Figure 8-4. A3 A/D Converter PCA (cont)

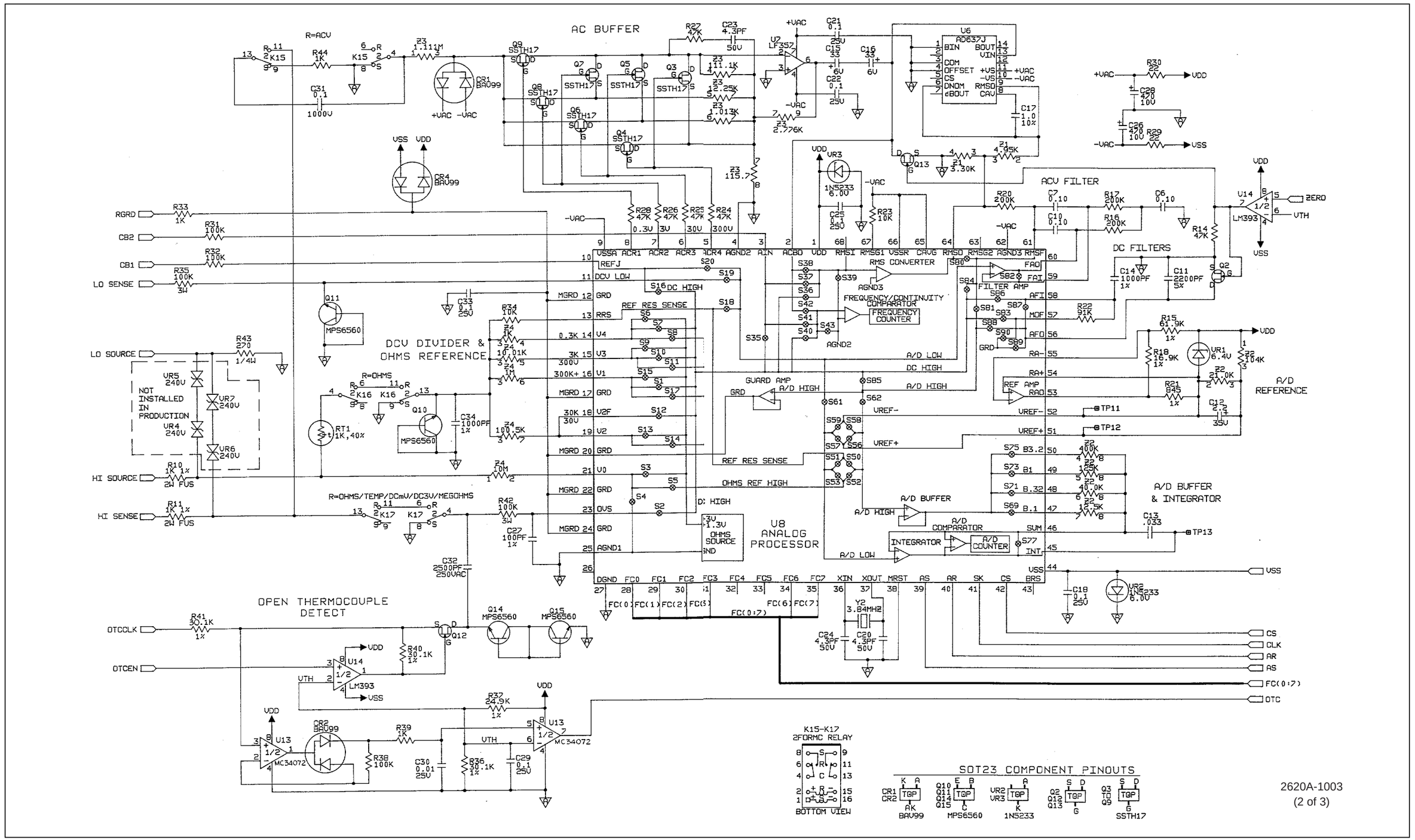


Figure 8-4. A3 A/D Converter PCA (cont)

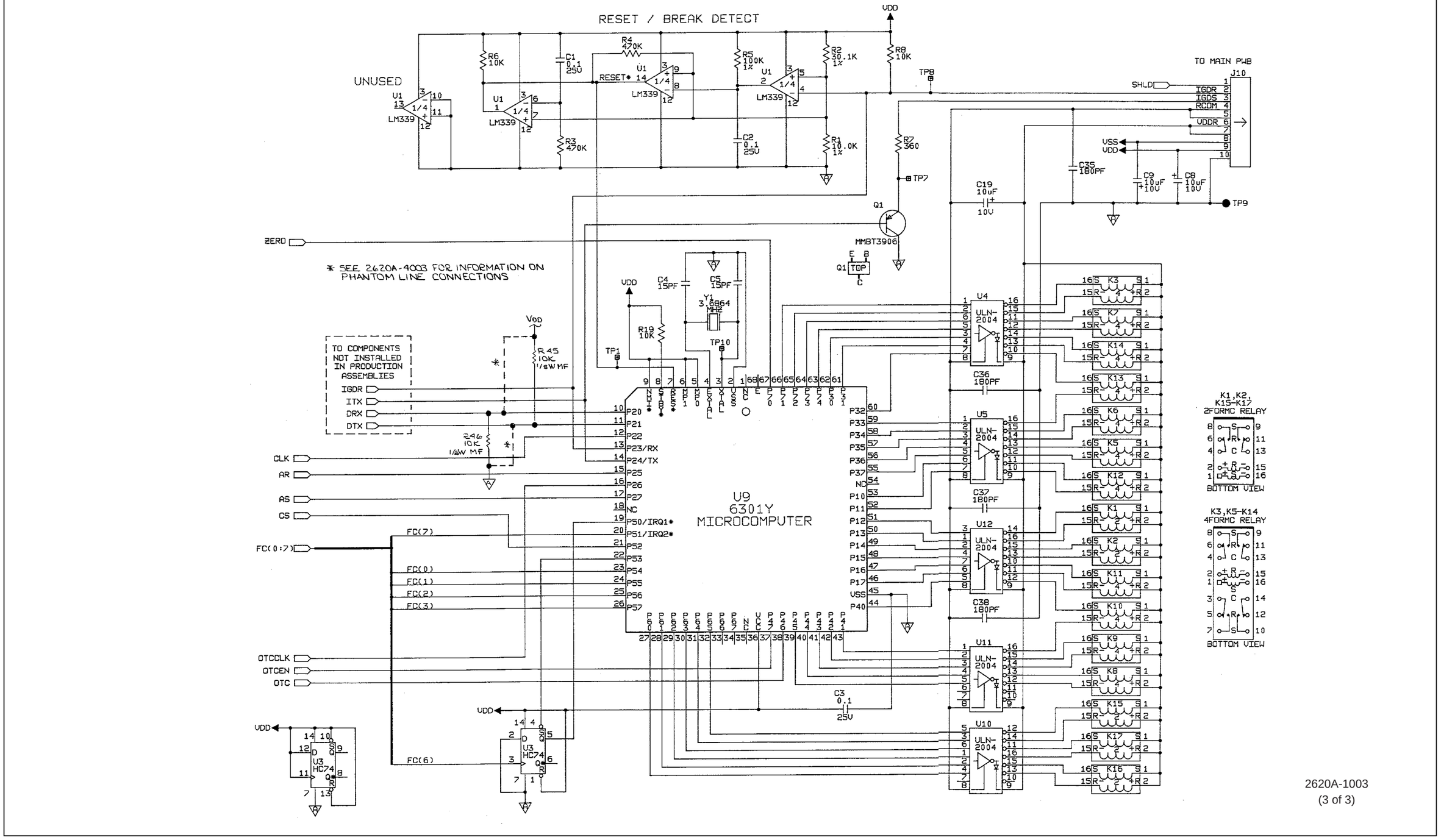
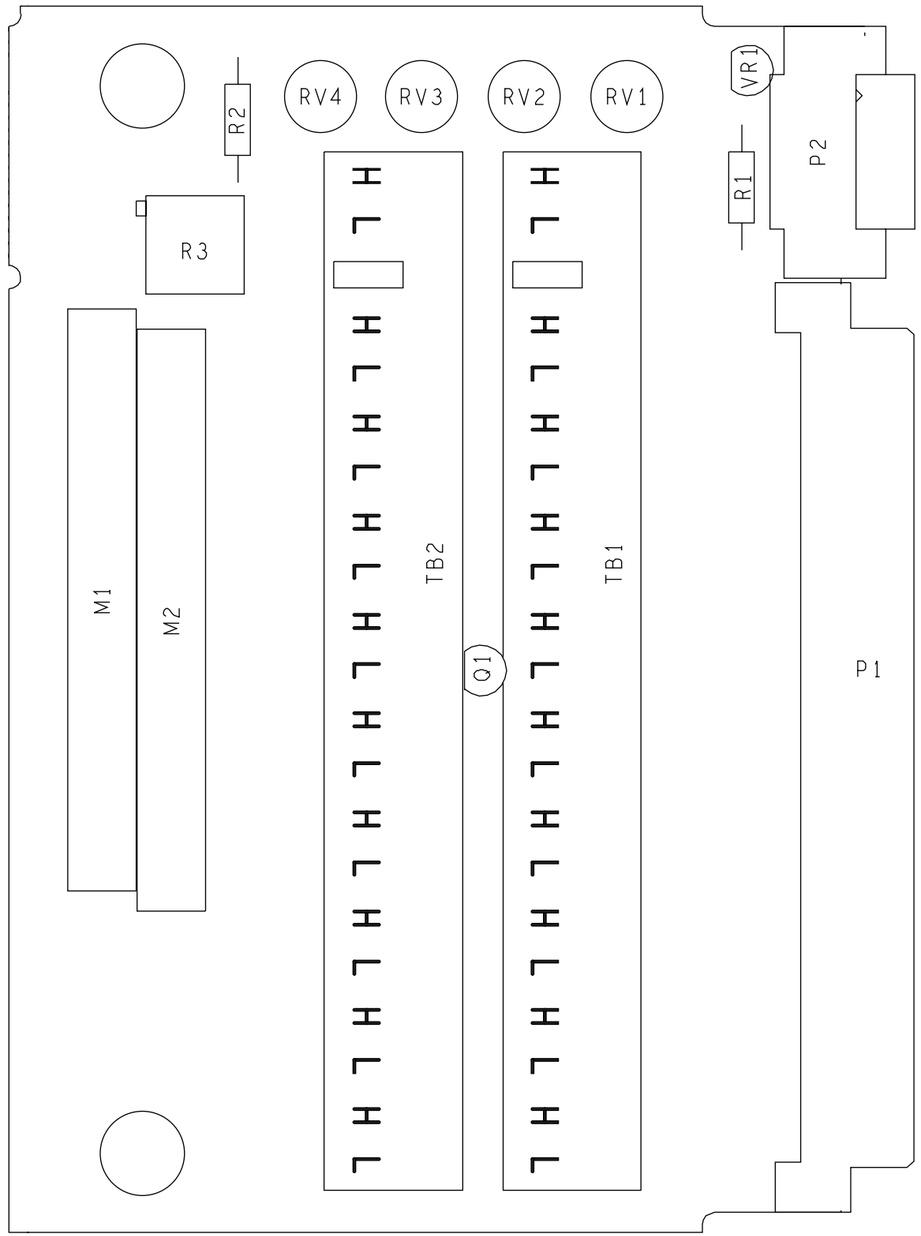


Figure 8-4. A3 A/D Converter PCA (cont)



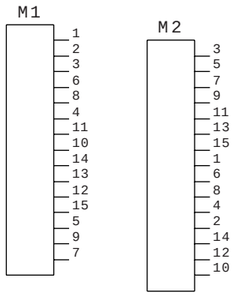
s92f.eps

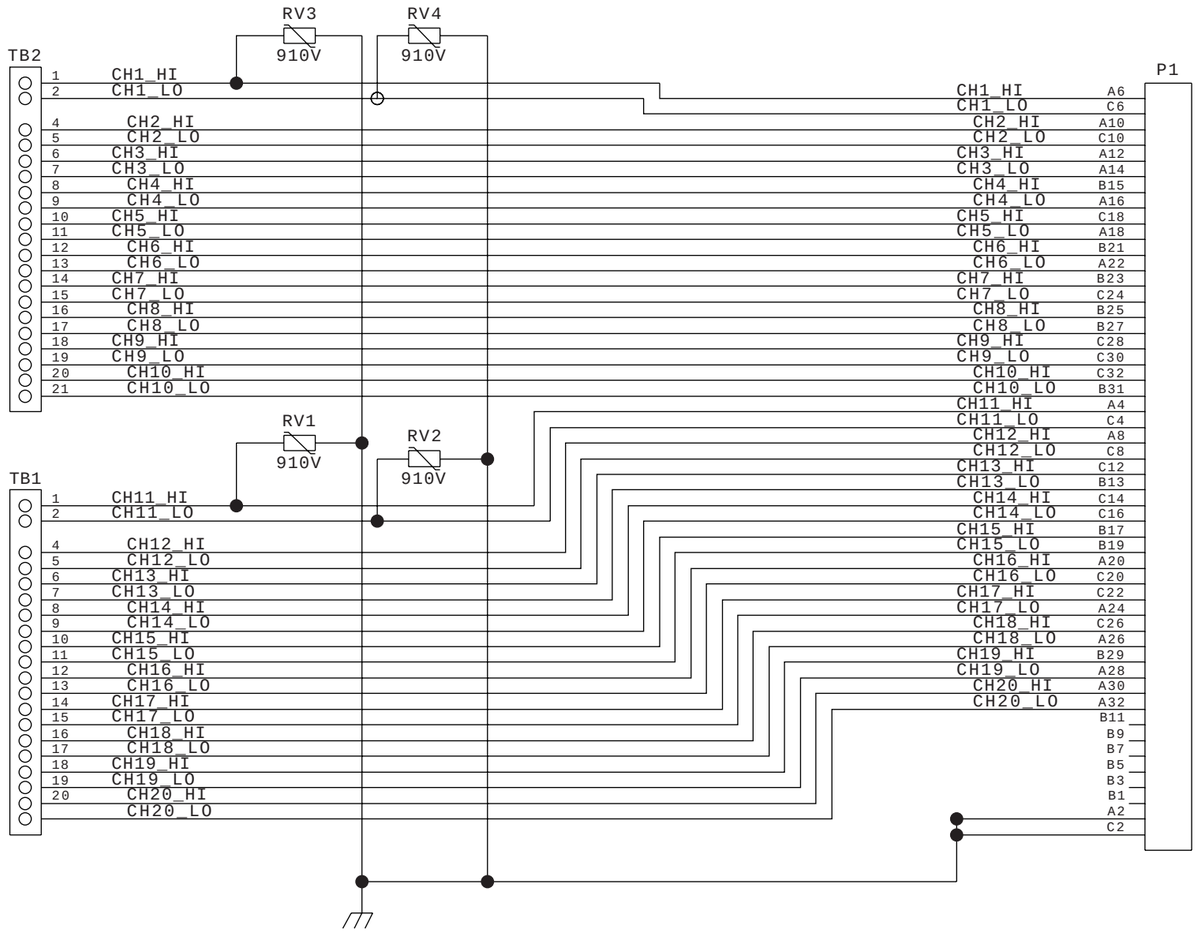
Figure 8-5. A4 Analog Input PCA

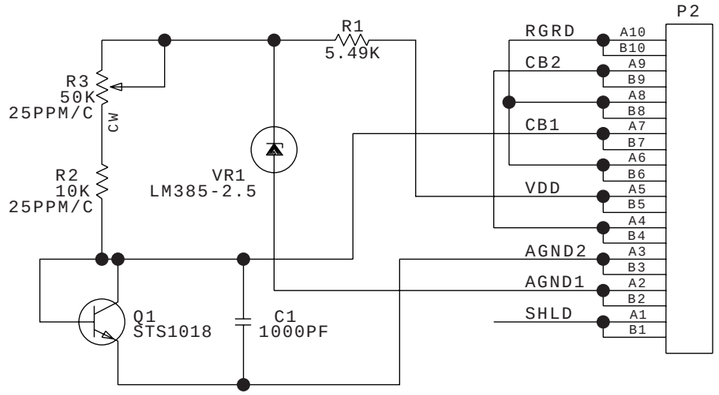
NOTES:

UNLESS OTHERWISE SPECIFIED.

1. ALL CAPACITOR VALUES ARE IN MICROFARADS.



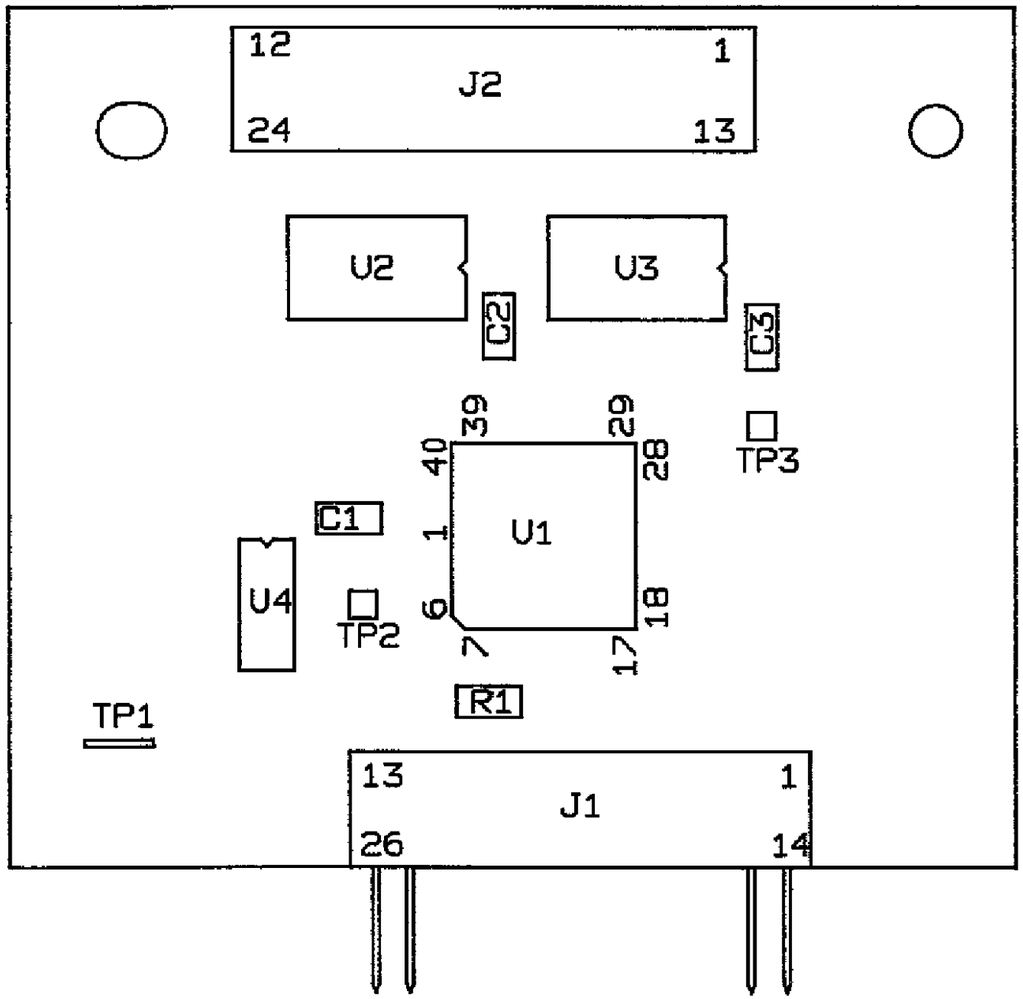




2620A-1004

s84f.eps

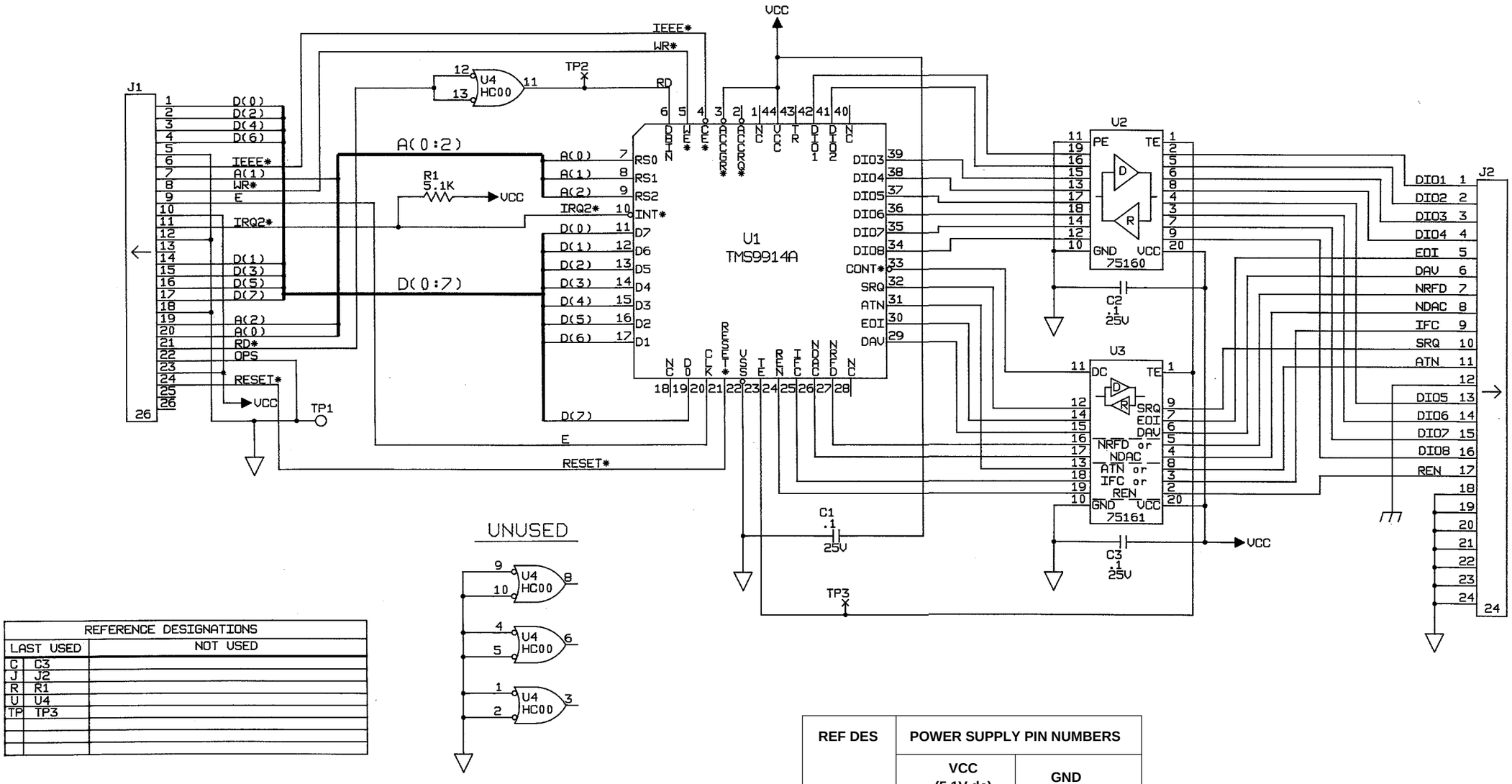
Figure 8-5. A4 Analog Input PCA (cont)



2620A-1605

s93f.eps

Figure 8-6. A5 IEEE-488 Interface PCA (2620A Only)



REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C C3	
J J2	
R R1	
U U4	
TP TP3	

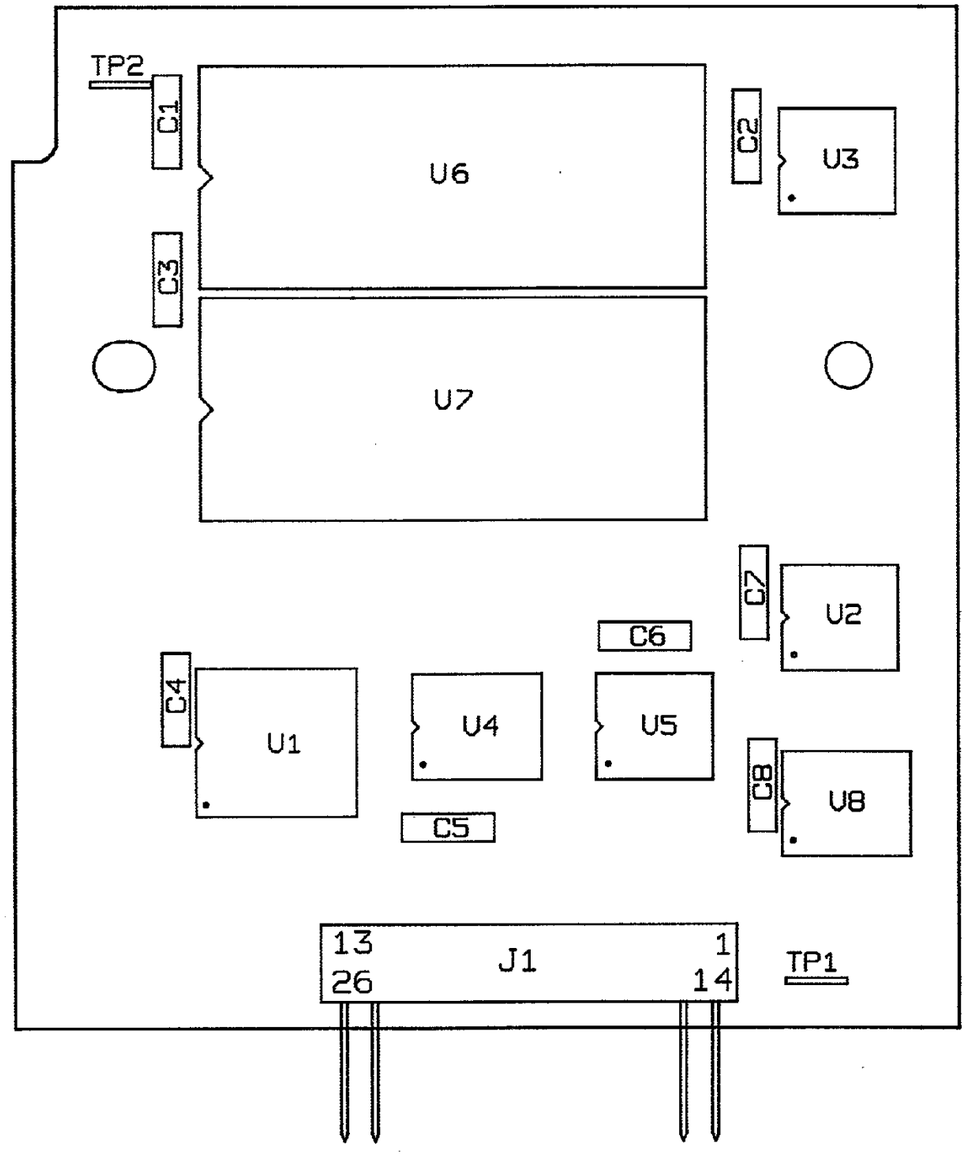
REF DES	POWER SUPPLY PIN NUMBERS	
	VCC (5.1V dc)	GND
A5U1	3, 44	22
A5U2	20	10,11
A5U3	20	10
A5U4	14	1,2,4,5,7,9,10

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE 1/4W, 5%.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.

2620A-1005

s85c.eps

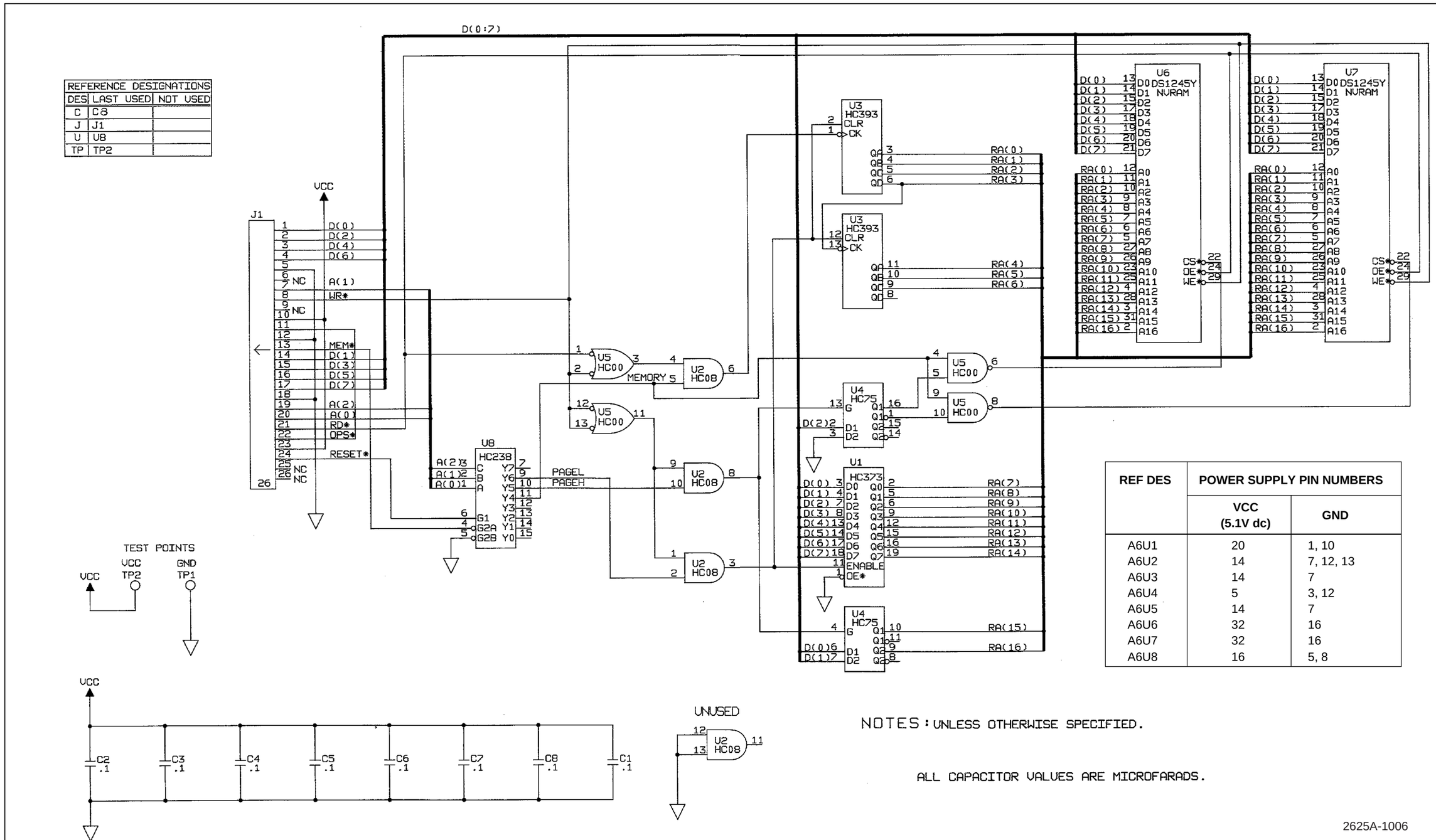
Figure 8-6. A5 IEEE-488 Interface PCA (2620A Only) (cont)



2625A-1606

s94f.eps

Figure 8-7. A6 Memory PCA (2625A)



REF DES	POWER SUPPLY PIN NUMBERS	
	VCC (5.1V dc)	GND
A6U1	20	1, 10
A6U2	14	7, 12, 13
A6U3	14	7
A6U4	5	3, 12
A6U5	14	7
A6U6	32	16
A6U7	32	16
A6U8	16	5, 8

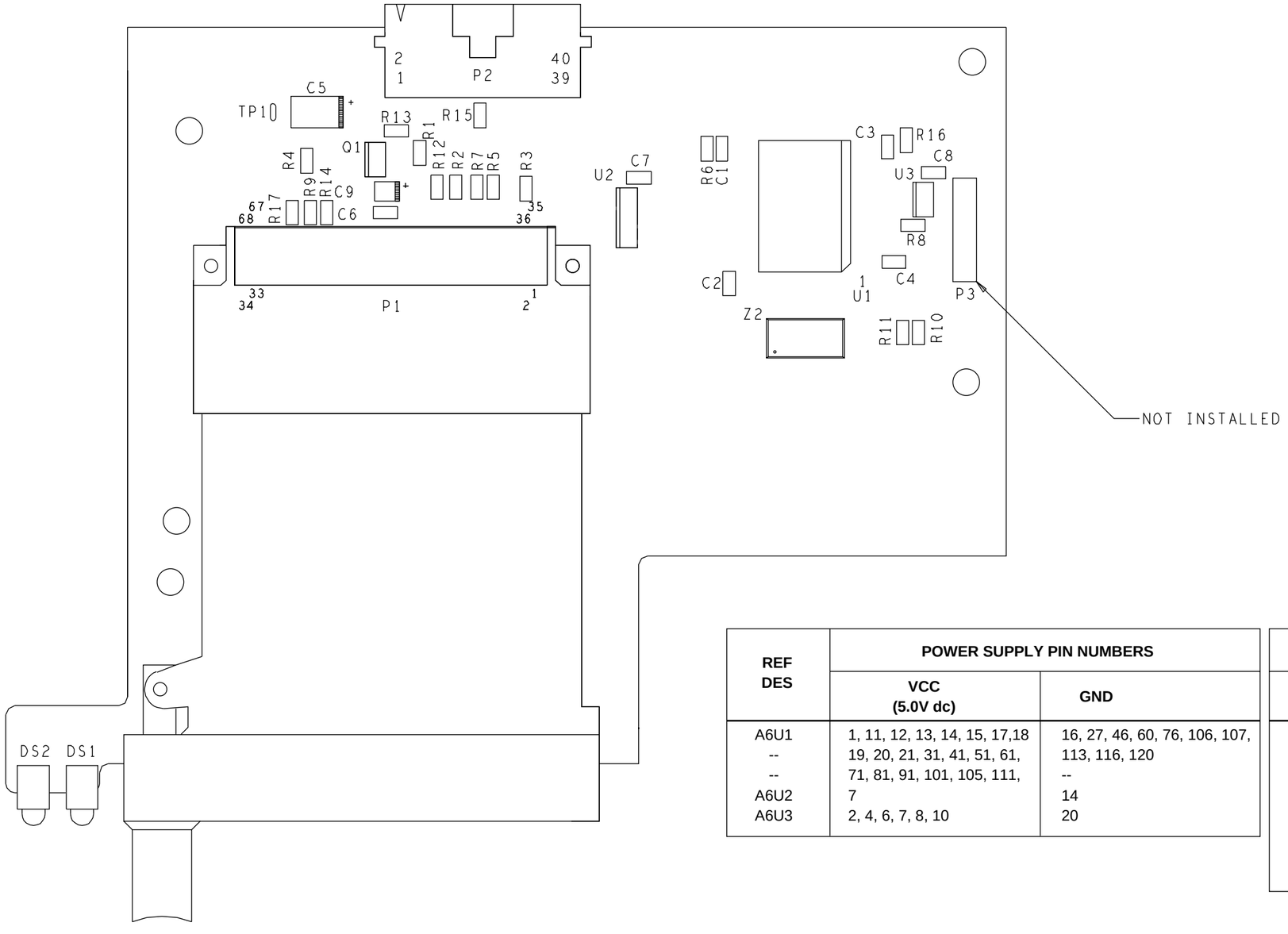
NOTES: UNLESS OTHERWISE SPECIFIED.

ALL CAPACITOR VALUES ARE MICROFARADS.

2625A-1006

s86c.eps

Figure 8-7. A6 Memory PCA (2625A) (cont)



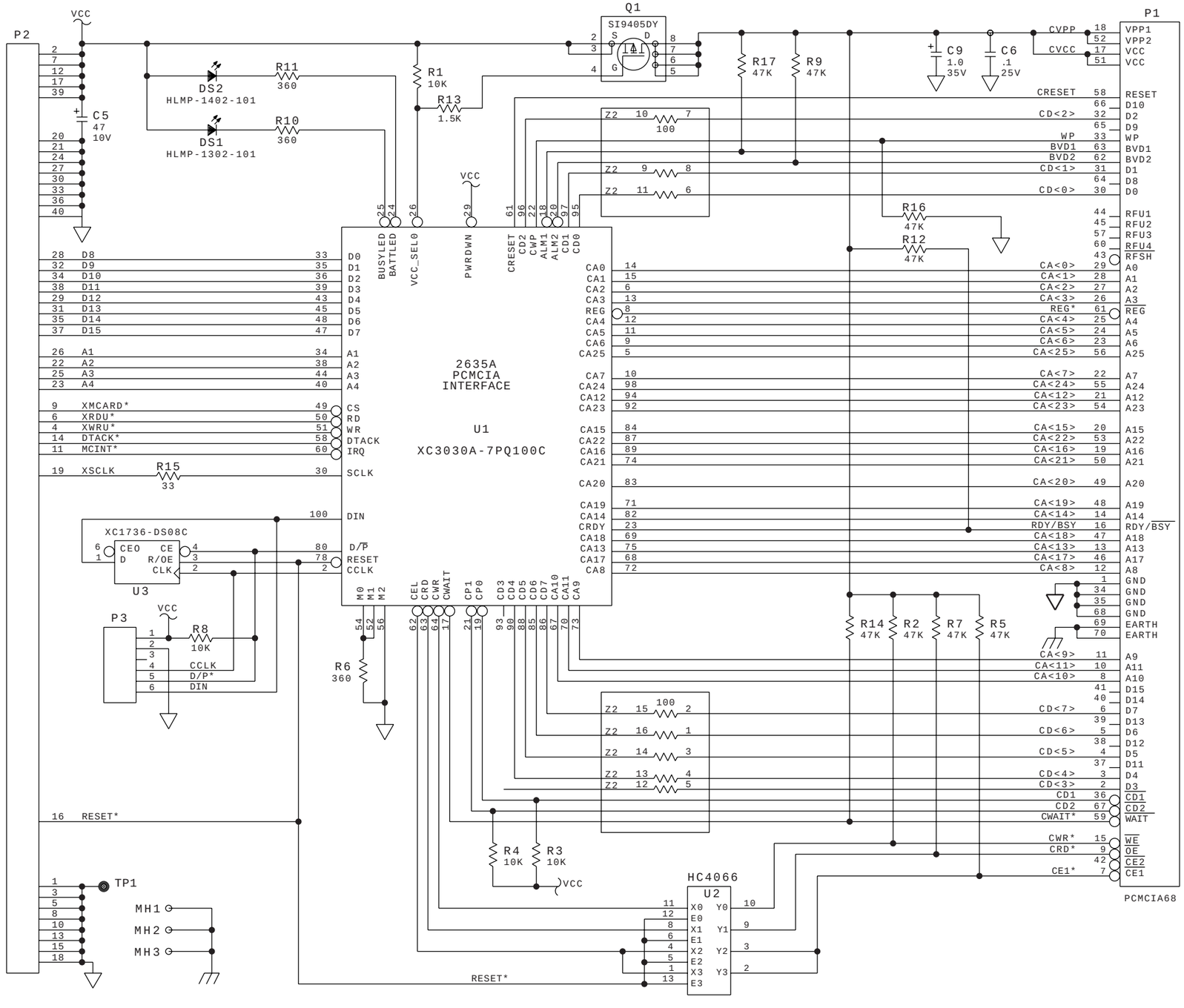
REF DES	POWER SUPPLY PIN NUMBERS	
	VCC (5.0V dc)	GND
A6U1	1, 11, 12, 13, 14, 15, 17,18	16, 27, 46, 60, 76, 106, 107,
--	19, 20, 21, 31, 41, 51, 61,	113, 116, 120
--	71, 81, 91, 101, 105, 111,	--
A6U2	7	14
A6U3	2, 4, 6, 7, 8, 10	20

Reference Designations		
Lasted Used		Not Used
C	C9	--
DS	DS2	--
P	P2	--
Q	Q1	--
R	R15	R14
TP	TP1	--
U	U3	--
Z	Z3	Z1

2635A-1606

s95f.eps

Figure 8-8. A6 Memory Card I/F PCA (2635A)



NOTES; UNLESS OTHERWISE SPECIFIED

1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS.
3. ALL RESISTOR ARE 1/8W,5%.
4. THIS DRAWING IS ARCHIVED ON TAPE: 2635A-C97006:MT. SEE SCD: 2635A-C90006.

2635A-1006

s87f.eps

Figure 8-8. A6 Memory Card I/F PCA (2635A) (cont)