# 5440B/AF Direct Voltage Calibrator

Service Manual

FLUKE

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## WARNING



is used in the operation of this equipment

# **DEATH ON CONTACT**

may result if personnel fail to observe safety precautions

TO AVOID ELECTRICAL SHOCK HAZARD, THE OPERATOR SHOULD NOT ELECTRICALLY CONTACT THE OUTPUT HI OR SENSE HI TERMINALS OF THE INSTRUMENT. DURING NORMAL OPERATION OR SYSTEM SELF TEST, LETHAL VOLTAGES OF UP TO 1100V DC MAY BE PRESENT ON THESE TERMINALS. IN THE EVENT OF MULTIPLE INSTRUMENT FAILURES, LETHAL VOLTAGES OF UP TO 1400V DC MAY BE PRESENT ON THESE TERMINALS.

Never work on the instrument unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections for the line power ac input connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through vital organs of the body.



## FIRST AID FOR ELECTRIC SHOCK

#### RESCUE

#### FREE VICTIM FROM CONTACT WITH LIVE CONDUCTOR QUICKLY. AVOID CONTACT WITH EITHER LIVE CONDUCTOR OR VICTIM'S BODY.

Shut off high voltage at once and ground circuit. If high voltage cannot be turned off quickly, ground circuit.

An ax with a dry wooden handle may be used to cut high voltage line. Use extreme caution to avoid resulting electric flash.

If circuit cannot be broken or grounded, use a dry board, dry clothing, or other nonconductor to free victim.

#### SYMPTOMS

#### NEVER ACCEPT ORDINARY AND GENERAL TESTS FOR DEATH.

Symptoms of electric shock may include unconsciousness, failure to breathe, absence of pulse, pallor, and stiffness, as well as severe burns. WHENEVER VICTIM IS NOT BREATHING PROPERLY, GIVE ARTIFICIAL RESPIRATION.

#### TREATMENT

#### START ARTIFICIAL RESPIRATION IMMEDIATELY.

Perform artificial respiration at scene of accident, unless victim's or operator's life is endangered. IN THIS CASE ONLY, remove victim to safe location nearby. If new location is more than a few feet away, give artificial respiration while victim is being moved.

After starting artificial respiration, continue without loss of rhythm for at least FOUR HOURS, or until victim is breathing without help. If you have to change operators while giving artificial respiration, do so without losing rhythm of respiration.

## AFTER VICTIM REVIVES

Be prepared to resume artificial respiration, as he may stop breathing again.

When victim is COMPLETELY CONSCIOUS, give him a stimulant (NOT AN ALCOHOLIC DRINK) such as a teaspoonful of aromatic spirits of ammonia in a small glass of water, hot coffee, or hot tea.





#### **POSITION VICTIM**

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Place victim in face-upward position and kneel close to his ear.

### CLEAR THROAT

Turn head to one side and quickly wipe out any fluid, mucus, or foreign body from mouth and throat with fingers.

#### **OPEN AIR PASSAGE**

Tilt head back and extend neck to open air passage.

#### LIFT JAW FORWARD

Place thumb in victim's mouth and grasp jaw firmly. Lift jaw forward to pull tongue out of air passage. Do not attempt to hold or depress tongue.



### PINCH NOSTRILS CLOSED

With other hand pinch nostrils closed to prevent air leak.

#### FORM TIGHT SEAL WITH LIPS

Rescuer's wide-open mouth completely surrounds and seals open mouth of victim. This is not a kissing or puckered position — mouth of rescuer must be wide-open.

#### BLOW

Exhale firmly into victim's mouth until chest is seen to lift. This can be seen by rescuer without difficulty.



### REMOVE MOUTH AND INHALE

During this time, rescuer can hear and feel escape for air from lungs. Readjust position if air does not flow freely in and out of victim's lungs.

Continue at a rate of 12 to 20 times per minute.

Breathing should be normal in rate with only moderate increase in volume, so that rescue breathing can be continued for long periods without fatigue. Do not breathe too forcibly or too large a volume if victim is an infant or small child.

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Frontispiece, 5440 Series Direct Voltage Calibrator

## Section 1 **Introduction and Specifications**

#### THE MANUAL SET

The Fluke 5440B/5442A Direct Voltage Calibrators are documented by an Operator Manual and a Service Manual. The Operator Manual contains all the information necessary to install and operate the Calibrators including periodic internal and external calibration. The Service Manual contains information to maintain, diagnose, calibrate, and repair the instruments.

#### THE SERVICE MANUAL

The 5440 Series Service Manual documents the 5440B/5442A Direct Voltage Calibrators. The Service Manual includes a theory of operation, general maintenance procedures, performance tests, calibration procedures, troubleshooting information, a list of replaceable parts, and schematic diagrams. The Service Manual, however, does not document the 5440A Calibrator. For information regarding the 5440A Calibrator, refer to the 5440A Service Manual (P/N 611683).

#### SHIPPING INFORMATION

The 5440B/5442A is packaged and shipped in a foam-packed container. Upon receipt of the instrument, make a thorough inspection to reveal any possible shipping damage. Special instructions for inspection and claims are included on the shipping container.

If reshipment of the instrument is necessary, the original container or an equivalent should be used. Do not use loose fill packaging material. Loose fill can allow the instrument to settle to one corner of the carton where the instrument can be damaged during shipment. As a minimum, surround the instrument with two to three inches of resilient material or foam-in-place packing.

#### **SERVICE INFORMATION**

Each Fluke 5440B/5442A Direct Voltage Calibrator is warranted for a period of one year upon delivery to the original purchaser. The Warranty is located at the front of this manual.

Factory authorized service (including calibration) for the 5440B/5442A is available at selected Fluke Technical Service Centers. For service and or calibration, contact the nearest Fluke Technical Service Center. The local technical service center will help get the required service for the instrument. A list of Fluke Technical Service Centers is given in Section 7. If requested, an estimate will be provided before work is begun on instruments that are beyond the warranty period.

1-2

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#### ACCESSORIES

The accessories available for use with the 5440B/5442A are listed in Table 1-1. All necessary service information for accessories is provided in Section 6.

#### **SPECIFICATIONS**

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Specifications for the 5440B/5442A are contained in Tables 1-2 and 1-3 at the end of this section. The outside dimensions of the 5440B/5442A are shown in Figure 1-1.

MODEL NUMBER	DESCRIPTION
5440A-7001	Procedure Storage Module. (FOR 5440BONLY) Stores up to 60 front panel settings of the 5440B. Non-volatile EAROM. Self contained.
5440A-7002	Low Thermal EMF Plug-in Cables.
	Three special length cables with shielded leads.
Y8021	IEEE-488 Compatible Cable (Armored), one meter length.
Y8022	IEEE-488 Compatible Cable (Armored), two meter length.
Y8023	IEEE-488 Compatible Cable (Armored), four meter length.
Y5001	Interface Cable for the 5205A. (FOR 5440B ONLY)
Y5002	Interface Cable for the 5220A. (FOR 5440B ONLY)
Y5003	RS-232-C Cable for the 1776B Printer, 5 foot length
Y5004	RS-232-C Cable for the 1776B Printer, 10 foot length
Y1709	RS-232-C Cable for the 1780A Display.

#### Table 1-1. Accessories



Figure 1-1. Outline Dimension Drawing

utput Voltage: 0 to utput Current: (see	1100V resolution specificati	ion)		
140B: utput Uncertainty		ration Standards, ±6		
RANGE	UNCERTAINTY 30 DAYS	SPECIFICATION: ±	(PPM OF OUTPUT	+ MICROVOLTS
0V to 11V 11V to 22V 22V to 275V 275V to 1100V	1.5 + 5 μV 1.5 + 8 μV 2.5 + 100 μV 2.5 + 400 μV	2.0 + 5 μV 2.0 + 8 μV 3.5 + 100 μV 3.5 + 400 μV	$2.5 + 5 \mu V 2.5 + 8 \mu V 4.5 + 100 \mu V 4.5 + 400 \mu V$	$\begin{array}{c} 3.5 + 5 \ \mu V \\ 3.5 + 8 \ \mu V \\ 6.0 + 100 \ \mu V \\ 6.0 + 400 \ \mu V \end{array}$
DIVIDED OUTPUT	Г			
0-220 mV 0.22-2.2V	4 + 0.5 μV 3 + 1 μV	5 + 0.5 μV 4.5 + 1.0 μV	6.5 + 0.5 μV 6 + 1.0 μV	10 + 0.5 μV 8 + 1.0 μV

	Compared to Calibr	-		
RANGE	30 DAYS	90 DAYS	180 DAYS	1 YEAR
0V to 11V 11V to 22V 22V to 275V 275V to 1100V	$2.5 + 5 \mu V$ $2.5 + 8 \mu V$ $3.0 + 100 \mu V$ $3.0 + 400 \mu V$	3.0 + 5 μV 3.0 + 8 μV 3.5 + 100 μV 4.0 + 400 μV	$\begin{array}{c} 4.5 + 5 \ \mu V \\ 4.5 + 8 \ \mu V \\ 5.0 + 100 \ \mu V \\ 5.5 + 400 \ \mu V \end{array}$	$6.5 + 5 \mu V$ $6.5 + 8 \mu V$ $7.0 + 100 \mu V$ $8.0 + 400 \mu V$
	<u>к при при при при при при при при при при</u>			
0-220 mV 0.22-2.2V	6 + 0.5 μV 4 + 1 μV	7 + 0.5 μV 6 + 1.0 μV	9 + 0.5 μV 8 + 1.0 μV	12 + 0.5 μV 11 + 1.0 μV
ncertainty of Calib	oration Standards (Fi	uke 732A and 752A	) Compared to Nati	onal Standards
	RANGE	U	NCERTAINTY OF S	TANDARDS
	0V to 11V 11V to 22V 22V to 275V 75V to 1100V		1.5 PPM 1.5 PPM 1.7 PPM 2.0 PPM	
_			4.0 PPM 2.0 PPM	, ,
Dutput Uncertainty ( The output uncert algebraic sum fo specifications for	Compared to Natonal ainty compared to nat r each range of the uncertainty of calibrat er standards are used.	ional standards for th output uncertainty ion standards listed	compared to nationa above are those for th	al standards. The ne Fluke 732A and

#### **Output Stability**

Specifications apply for initial stabilizations of two hours, constant ambient temperature of  $\pm 1^{\circ}$ C, constant line voltage, constant load, and measurement bandwidth of 0.1 Hz to 1 Hz.

DANCE	±(P	PM OF SETTING + FLOO	R)
RANGE	10 MINUTES	24 HOURS	30 DAYS*
0V to 11V 11V to 22V 22V to 275V 275V to 1100V	$\begin{array}{c} 0.2 + 2 \ \mu V \\ 0.2 + 3 \ \mu V \\ 0.3 + 40 \ \mu V \\ 0.3 + 200 \ \mu V \end{array}$	$\begin{array}{c} 0.3 + 3 \ \mu V \\ 0.4 + 4 \ \mu V \\ 0.3 + 50 \ \mu V \\ 0.3 + 200 \ \mu V \end{array}$	$\begin{array}{c} 0.5 + 3 \ \mu V \\ 0.5 + 4.5 \ \mu V \\ 1.0 + 60 \ \mu V \\ 1.0 + 300 \ \mu V \end{array}$
			I
0 mV to 220 mV 0.22V to 2.2V	0.5 + 0.2 μV 0.5 + 0.2 μV	$0.5 + 0.2 \ \mu V$ $0.5 + 0.5 \ \mu V$	$2 + 0.3 \mu V$ $2 + 0.7 \mu V$

\*For best results, use internal calibration for periods exceeding one day.

#### Table 1-2. General Specifications (cont)

#### Temperature Coefficient of Output

These specifications apply for ambient temperatures outside the  $\pm 5^{\circ}$ C range of the uncertainty specifications listed earlier.

RANGE	±(PPM OF SETTING) PER °C			
RANGE	0-10°C	10-30°C	30-40°C	40-50°C
0V to 11V	0.15 ppm	0.1 ppm	0.4 ppm	1.0 ppm
11V to 22V	0.15 ppm	0.1 ppm	0.4 ppm	1.0 ppm
22V to 275V	0.2 ppm	0.2 ppm	0.6 ppm	1.5 ppm
275V to 1100V	0.2 ppm	0.2 ppm	1.0 ppm	1.5 ppm
DIVIDED OUTPUT				
0-220 mV	0.5 ppm	0.5 ppm	0.5 ppm	1.2 ppm
0.22-2.2∨	0.5 ppm	0.5 ppm	0.5 ppm	1.2 ppm

#### Linearity

These specifications apply for the ambient temperature range of 15° C to 30° C within  $\pm$ 5° C of the external calibration temperature.

RANGE	<b>±PPM OF OUTPUT + MICROVOLTS)</b>
0 mV to 220 mV	0.5 ppm + 0.2 μV
0.22V to 2.2V	0.7 ppm + 0.3 μV
0V to 11V	0.5 ppm + 1.5 μV
11V to 22V	0.5 ppm
22V to 275V	0.5 ppm + 40 μV
275V to 1110V	1.0 ppm

#### RESOLUTION

RANGE	RESOLUTION	MAXIMUM SETTING	MAXIMUM LOAD OR OUTPUT RESISTANCE
0V to 11V	1 µV	11.00000V	60 mA
11V to 22V	1 <i>μ</i> V	22.00000V	60 mA
22V to 275V	10 <i>μ</i> V	275.000000V	25 mA
275V to 1100V	100 <i>µ</i> V	· 1100.0000V	25 mA
DIVIDED OUTPUT			
0 to 220 mV	0.01 <i>μ</i> V	220.00000 mV	495Ω
0.22V to 2.2V	0.1 <i>μ</i> V	2.2000000	450Ω

#### OUTPUT NOISE

RANGË	BANDWIDTH		
RANGE	0.1 HZ TO 10 HZ	10 HZ TO 10 KHZ	
0 mV to 220 mV	0.1 <i>µ</i> V	5 μV	
0.22V to 2.2V	0.2 <i>μ</i> V	15 μV	
0V to 11V	1.5 μV	30 µV	
11V to 22V	3.0 µV	50 µV	
22V to 275V	35 µV	150 μV	
275V to 1100V	100 μV	300 µV	

#### Table 1-2. General Specifications (cont)

#### **Common Mode Rejection**

Greater than 140 dB for frequencies from dc to 400 Hz.

#### **Output Settling Time**

Time to settle within a given uncertainty band of final value, for a change in programmed output within a given range.

BANGE	±PARTS PER MILLION OF CHANGE*		
	3 SECONDS	5 SECONDS	10 SECONDS
0 mV to 220 mV, 0.22V to 2.2V, 0V to 11V, and 11V to 22V	7 ppm	2 ppm	0.5 ppm
22V to 275V 275V to 1110V		-	3 ppm

\*Add 0.5 seconds for any change in range up to 22V, 1.0 second for a change from 22V up, and 0.5 seconds for a change from STBY to OPER.

#### Line Power Requirements

NOMINAL SETTING	VOLTAGE LIMITS	FUSE	TYPICAL POWER
100V	90-110V	2A/250V	84 watts when in
110V	99-121V	2A/250V	standby at nominal
115V	103.5-126.5V	2A/250V	line, 145 watts
120V	108-132V	2A/250V	when in 1100V
200V	180-220V	1A/250V	range 25 mA
220V	198-242V	1A/250V	output and high line
230V	207-253V	1A/250V	
240V	216-264V	1A/250V	

#### Line Regulation

Less than  $\pm 0.1$  ppm of range for a line voltage change  $\pm 10\%$  of nominal.

#### Load Regulation

Less than  $\pm 0.1$  ppm change of output for change from no-load to full-load or from full-load to no-load for output load impedances greater than 80 ohms.

Table 1-3.	. Physical and	Environmental	Specifications
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CONDITION	TEMPERATURE	% RELATIVE HUMIDITY (NON-CONDENSING)
Non-Operating	-40°C to +75°C 0°C to +50°C	Not controlled ≪95% ±5%
Operating	0 to 30° C +30 to +40° C +40 to +50° C <sup>2</sup>	≪95% ±5% ¹ ≪75% ±5% ≪45% ±5%

Notes: <sup>1</sup> Accuracy degradation above 80% R.H.

<sup>2</sup> Instrument accuracy is degraded above 40°C due to loss of oven regulation.

#### Aititude

Non-Operating 0-12,200m (40,000 feet) Operating 0-3,050m (10,000 feet)

#### Vibration

FREQUENCY	FORCE FREQUENCY	
5-15 Hz	0.7G at 15 Hz	0.06 in
15-25 Hz	1.3G at 25 Hz	0.04 in
25-55 Hz	3G at 55 Hz	0.02 in

Shock: 18 shocks, 20G, 1/2 sinewayes.

Size: 61cm L x 43cm W x 24cm H (24.0in L x 17.0in W x 8.75in H). Weight: 30.2 kg (66.4 lb) Warranty: 1 year, parts and labor (see specific warranty policy). Compliance with External Standards ANSI C39.5 Dec 1980 IEC 348 Second Edition 1978 EMI/RFI Review Standards **EMI/RFI** Conducted Emissions FCC Rules Part 15, Subpart J VDE 0871 VDE 0871 FCC Part 15 J Class MIL STD 461B CISPR 11 Radiated EMI/RFI Emissions Meets or exceeds all VDE and FCC requirements.

## Section 2 Theory of Operation

#### INTRODUCTION

This section contains the theory of operation for the 5440B/5442A. The theory of operation is divided as follows:

- Functional Overview of Hardware: subdivided into digital, analog, and power supply circuits, supported by block diagrams.
- Detailed Circuit Analysis: subdivided into digital and analog circuits and supported by the schematics in Section 8 of this manual.
- Functional Overview of Software: supported by block diagrams.
- Discussion of internal/external calibration methods used in the 5440B/5442A. (Additional information on internal/external calibration methods used in the 5440B/5442A is contained in the Appendix.)

#### FUNCTIONAL OVERVIEW OF HARDWARE

The 5440B/5442A is composed of three basic types of circuits as illustrated in Figure 2-1. These circuits are digital, analog, and power supply. The digital circuits control the analog circuits and the operator interface. Digital circuits also control the IEEE-488, RS-232 port, and Boost interfaces. The analog circuits generate and control the output of the 5440B/5442A. The power supply circuits generate and control all internal operating voltages for the 5440B/5442A. A guard circuit isolates the analog circuits and some of the power supply circuits from the digital circuits.

#### Digital Circuits

The digital circuits are controlled by three microprocessors as illustrated in Figure 2-2. Use divides the digital circuits into three areas: main control logic, front panel control logic, and guarded control logic. Each area has an associated microprocessor. Central control for the 5440B/5442A is provided by the main control logic circuits. The main control logic indirectly controls the analog circuits through the guarded control logic. The main control logic also communicates with the operator through the front panel control logic and controls the IEEE-488, RS-232, and Boost interface ports (5440B).

#### MAIN CONTROL LOGIC

The main control logic circuits (as shown in Figure 2-2) are not guarded and consist of the central controller (the main microprocessor), main memory (Memory PCA), and input/output circuits (I/O Assembly).

#### 2-1

#### 2-2

#### 2-3

2-4



Figure 2-1. Block Diagram

The main microprocessor generates all control sequences to the guarded control logic. These sequences include instructions for setting the 5440B/5442A output to the programmed value and comprehensive self-test and diagnostic procedures.

The I/O Assembly circuits allow the main microprocessor to communicate over the IEEE-488, RS-232, and Boost interfaces to remote devices (5440B). 5440B/5442A self-test and diagnostic data is transmitted over the RS-232 interface to a printer or monitor. The Boost interface (5440B) drives and controls a 5220A or a 5205A during boost operation. The IEEE-488 interface can be used to operate the 5440B/5442A from a remote station and communicate with other IEEE-488 devices.

The 5440B/5442A is designed also to be controlled by the IEEE-488 interface. The main microprocessor interprets messages from the external IEEE-488 interface controller and sends the appropriate responses back over the IEEE-488 interface.

The main microprocessor communicates with the front panel microprocessor through a serial data link to perform three main functions: front panel displays, operator interface (local operation), and communication with the 5440A-7001 Procedure Storage Module (5440B).

During local operation, the front panel microprocessor interprets key entries (front panel setups) and sends the information to the main microprocessor. The main microprocessor responds with the appropriate control sequences to the guarded control logic. The guarded control logic, in turn, drives the analog circuits to the correct output level. Front panel setups can be stored using the Procedure Storage Module. The front panel microprocessor interprets stored test setups the same way it interprets individual key entries (5440B).





During local or remote operation, self-test and diagnostic information is sent to the front panel microprocessor from the main microprocessor. This information appears on the front panel alphanumeric display. The self-test and diagnostic results may also be sent out on the RS-232 port.

Digital self-tests are controlled by the main microprocessor. Depending upon the setting of the self-test switches (located on the Controller PCA, the Guard Crossing PCA and the Front Panel Controller PCA) several special self-test routines are executed to exercise portions of the digital logic circuits.

When the Calibrator is turned on or when it is reset by the front panel RESET key or an IEEE-488 interface RESET message, the main microprocessor reads the Boot ROM and sets up the Calibrator according to the ROM program.

#### FRONT PANEL CONTROL LOGIC

The front panel control logic is contained on the Front Panel Controller PCA. The front panel logic is a local input/output area. Inputs are entered by the operator using the keyboard or obtained from the Procedure Storage Module. The front panel microprocessor interprets these inputs and sends the information to the main control logic. The main control logic interprets and sends this information to the guarded control logic to drive the analog circuits. The main control logic also returns information to the front panel logic for display.

#### GUARDED CONTROL LOGIC

The guarded control logic (refer to Figure 2-2) optically isolates the analog circuits from the main control logic circuits. Main control logic sequences are sent to the guarded control logic microprocessor, which relays them through optoisolators. The main function of the guarded microprocessor is to pass control sequences to the analog circuits. The guarded microprocessor also performs three secondary functions:

- Provides status information to the main control logic on command.
- Refreshes the analog circuits to improve system operation.
- Continually monitors the guarded circuits to detect fault conditions.

The guarded logic uses two time-out monitor (or watch-dog) circuits to ensure safety. If either the main microprocessor or the guarded microprocessor fail to execute their programs correctly, a time-out monitor circuit places the 5440B/5442A in Standby. The instrument can only be restarted by pressing the RESET button on the front panel.

The guarded logic has one self-test switch. The operator can use this switch to provide limited self-test capability of the guarded logic.

#### **Analog Circuits**

Figure 2-3 shows a functional block diagram of the analog circuits in the 5440B/5442A. The analog circuits establish a stable dc reference voltage and provide precise amplification and attenuation of this reference voltage to produce output voltages from -1100 to +1100V dc in six ranges. Refer to Figure 2-4. A 13V dc reference and a pulse-width modulated DAC on the REF/DAC Analog PCA produce -11 to +11V dc under control of the REF/DAC Digital PCA. The Preamp PCA, the Output PCA, and the Sample String PCA form an inverting amplifier with four digitally controlled gains. The Output/HV Control PCA controls generation of voltages greater than 22V dc by feeding the voltages, +KV and -KV,



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to the Output PCA where they are added in series with the low-voltage amplifier output. Other important analog circuits include a high-resolution, high-sensitivity analog-to-digital converter and switching circuits. The high resolution analog-to-digital converter is used to monitor internal and output voltage levels. The switching circuits implement the internal calibration features.

#### OVENED REFERENCE

The ovened reference circuit is located on the REF/DAC Analog PCA. The ovened reference provides a temperature stable reference voltage for the d/a converter on that pca. The ovened reference circuit is composed of two 6.5V hybrid reference amplifiers cascaded in series to produce a summed voltage of 13V dc. The amplifier components are selected for low noise, good stability, and a low temperature coefficient. The oven maintains the reference amplifier environment at a constant 50°C. Sources of secondary errors have been substantially reduced by eliminating reference voltage adjustments.

#### DIGITAL-TO-ANALOG CONVERTER

The digital-to-analog converter (DAC) is located on the REF/DAC Analog PCA and is controlled by the REF/DAC Digital PCA. The 13V dc reference voltage from the ovened reference is applied through relays to the DAC (Figure 2-4). The relay position determines the polarity of the reference voltage and subsequently, the polarity of the output.



Figure 2-3, 5440 Analog Circuit Block Diagram

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Figure 2-4. DAC Simplified Schematic

The reference voltage is pulse-width modulated by two pairs of FET switches. The voltage is then filtered to a de level by a filter/amplifier circuit. Each FET pair switches between its input voltage and ground at a frequency of 83 Hz. The FET switches vary the duty cycle of the square wave, and therefore, the DAC output voltage. The first switching circuit provides a coarse control of the DAC output voltage, while the second switching circuit provides fine control of the DAC output voltage. The outputs of both switching circuits are summed at the input of the filter/amplifier. The filter/amplifier is located in the same ovened environment as the 13V de reference for stable temperature coefficient performance.

In normal operation, the output of the DAC is between -11V and +11V. The first switching circuit provides about 0.55 mV of resolution in the DAC output, while the second switching circuit provides about 75 nV of resolution in the DAC output.

The absolute value of the DAC output is determined by the duty cycle of the pulse width drive signals generated on the REF/DAC Digital PCA. The commands for the pulse width drive signals of the two switching circuits are sent to the REF/DAC Digital PCA, via the guarded control logic, from the main control logic as two 15-bit words. These words are generated through an algorithm that uses constants generated and stored by the Internal Calibration and External Calibration procedures. Each of the six output ranges has a set of calibration constants. 5440B/5442A output ranges are listed in Table 2-1.

#### Table 2-1. Output Ranges

RANGE NAME	OUTPUT VOLTAGE RANGE (VDC)	FUNCTION
0.2 Volt	-0.22 to +0.22	Divider Output
2 Volt	-2.2 to -0.22 and +0.22 to +2.2	
11 Volt	-11 to +11	DC Calibrator Output
22 Volt	-22 to -11 and +11 to +22	
250 Volt	-275 to -22 and +22 to +275	
1100 Volt	-1100 to -275 and +275 to +1100	

#### OUTPUT AMPLIFIER AND OUTPUT DIVIDER

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As Figure 2-5 shows, parts of the output amplifier circuit are contained on the Preamp PCA, the Output PCA, and the Sample String PCA. The output divider circuit is contained on the Output PCA. The output amplifier has four gain settings, one for each of the ranges (11V, 22V, 275V, and 1100V). To produce the two ranges below 11V (0.2V and 2V), the 22V range of the output amplifier is divided by the output divider circuit.

The preamplifier is a low noise, low drift, high gain amplifier, whose output drives the high power output stage on the Output PCA. The preamplifier circuit is located in a temperature-controlled oven to reduce the effects of thermal coefficients due to external temperature changes.

The power output stage consists of transistors Q1 and Q2. For the 11V and 22V output ranges, the transistors receive their source voltages from the low voltage power supply labeled -30 OP and +30 OP. For the 275V and 1100V ranges, the transistors receive their source voltages from the high voltage power supply labeled -KV and +KV. The high voltage power supply originates on the Filter B PCA and is supplied to the Output PCA via the Output/HV Control PCA, which controls the power supply voltage.

During normal operation, the signal from the output amplifier is connected to the front panel or the rear panel output terminals. During Boost Mode operation, the output amplifier is connected to the rear panel Boost Interfaces (J5 and J7). During Divider Mode operation, the signal from the output amplifier is connected to the output divider circuit on the Output PCA. The divider circuit divides the 22V output of the output amplifier by 10 or 100 to produce the 2V and 0.2V Divider outputs. The output of the divider circuit is connected to the Divider Output terminals on the front panel or the rear panel.

The Sample String PCA contains the precision resistors that set the gain of the output amplifier circuit. The gain is set for each output range using relays to change the value of R2. See Table 2-2. The value of R1 is 20 k $\Omega$ . All of the precision resistors are enclosed in a temperature-stable oven to reduce the effect of thermal drift because of external temperature changes and self heating at 1100V output operation.



Figure 2-5. Output Amplifier Simplified Schematic

#### Table 2-2. Output Gain

OUTPUT RANGE	OUTPUT GAIN	VALUE OF SAMPLE STRING R2 IN KILOHMS
0.22	2	40
2.2	2	40
11	1	20
22	2	40
275	25	500
1100	100	2000

#### OUTPUT SENSING CIRCUIT

The output sensing circuit is directly connected to the output terminals for Internal Sense operation, or the output sensing circuit is directly connected to the SENSE HI and SENSE LO binding posts for External Sense operation. The output sensing circuit is unique in that it appears as a very high impedance to the output. It produces a compensating current (equal in magnitude but opposite in polarity to the current flowing through the feedback resistors, R2 on the Sample String PCA) that reduces sense currents to less than 1% of the current flowing through the sample string resistors. The output sensing circuit also generates a compensating current for the SENSE LO terminals.

#### HV CONTROL LOOP

The HV (High-Voltage) Control Loop is distributed on the Output PCA, the Output/HV Control PCA, and the Filter B PCA. As shown in Figure 2-5, the OP COM signal is fed back to the Output/HV Control PCA to control the - KV and + KV signals that will be applied to the Output PCA.

#### Monitoring System

The monitoring system of the 5440B/5442A is illustrated by the block diagram in Figure 2-6. This monitoring system provides three distinct functions:

- During normal operation, the monitoring system measures the output voltage and current of the 5440B/5442A. If the voltage is 5% over or under the programmed voltage, or if the current exceeds the specified limits, the monitoring system places the instrument into Standby mode.
- During analog and high voltage loop self-tests, the monitoring system functionally checks the circuits in the 5440B/5442A for proper operation.
- During the Internal Calibration procedure, the monitoring system takes measurements of various circuits in the 5440B/5442A for the Internal Calibration function.

The four multiplexers in the monitoring system receive their digital commands from the main microprocessor via the Guard Crossing PCA. If a multiplexer is being addressed (except for the multiplexer on the REF/DAC Digital PCA), the specified test point is connected to the ANALOG DATA OUT line. This line is routed to the REF/DAC Digital PCA where it is multiplexed; along with test points located on this pca, and sent to the a/d converter. The a/d converter has an input range of -1.1V to +1.1V. Signals greater than  $\pm 1.1V$  are attenuated before they reach the a/d converter. Signals that are way below the a/d converter input limit are amplified before being applied. The 12-bit (plus sign bit and overrange bit) output of the a/d converter is sent to the main microprocessor via the Guard Crossing PCA.

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Figure 2-6. Monitoring System Block Diagram

#### **Power Supply Circuits**

The power supply circuits transform the line power into the supply voltages required by the analog and digital circuits. As Figure 2-7 shows, the power supply circuits consist of six assemblies. The Outside Guard Regulator PCA and the Outside Guard Term PCA supply the analog and digital circuits that are outside the guard. The Inside Regulator PCA, the Guarded Xfmr Term PCA, the Filter A PCA, and the Filter B PCA, supply the analog and digital circuits that are inside the guard.

#### **GUARDED XFMR TERM PCA, A11**

The ac line source input to the 5440B/5442A is applied to the power supply via the Guarded Xfmr Term PCA. Refer to Figure 2-7. AC line power passes through the line fuse F1 and power switch S4. The line voltage select switches (S1, S2, and S3) set the primary taps of T1 to the correct input voltage. Power is delivered through T1 to the rest of the guarded power supply circuits. The fan and the primary of the transformer on the Outside Guard Term PCA are permanently connected to taps on one primary of the guarded transformer. This provides nominal 115V ac by autotransformer action when the line switches are correctly set.

Fuse F1 provides overall fuse protection for the 5440B/5442A. Individual secondary windings contain fuses that protect the transformer from damage in the event that a short in a secondary circuit does not reflect enough current to the primary winding to blow the line fuse.

#### FILTER A PCA, A12

The Filter A PCA receives ac voltages from the Guarded Xfmr Term PCA and provides rectified and filtered dc voltages to the Inside Regulator PCA. Test points at the top of the Filter A PCA provide the means for checking the dc output voltages.

#### INSIDE REGULATOR PCA, A10

The Inside Regulator PCA contains the regulator circuits for auxiliary supply voltages used by circuits inside the guard. Comparator circuits on the pca continuously monitor the regulated supply voltages to detect any large deviation from nominal output voltage. A deviation of approximately 12 percent from nominal produces an output low signal from the monitor circuit. The output low signal turns on the LED indicator at the top of the circuit board and produces a logic low on the GPSF line as a signal to the microprocessor.

#### FILTER B PCA, A13

The Filter B PCA contains the circuits that produce the high voltage supply used for output voltages above 22V. This pca also contains the rectifier/filter circuit for the 20V oven supply (20V OVN) for the heater windings of the ovens. The high voltage power supply is controlled by triac switching and square wave driver lines from the Output/HV Control PCA.

#### OUTSIDE GUARD TERM PCA, A19

The Outside Guard Term PCA contains the transformers, rectifiers, and filters that supply the raw voltages to the Outside Guard Regulator PCA. Each secondary winding has its own fuse to prevent transformer damage in the event that a short in the secondary fails to blow the line fuse. Test points at the top of the printed circuit boards allow voltage checks of the unregulated supplies.

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#### OUTSIDE GUARD REGULATOR PCA, A17

The Outside Guard Regulator PCA provides auxiliary power and error detection for circuits outside the guard (including the front panel). Test points located at the top of the printed circuit board provide a means of checking the individual supply voltages.

All supplies are continuously monitored by the error detection circuit. The outputs of the power supply monitors are ORed in the error detection circuit to provide an output signal (PSF) that is monitored by the microprocessor. If one of the regulated outputs is defective, the PSF signal to the microprocessor will cause the appropriate power supply fault LED (located near the top of A17) to turn on.

The POP signal is the power-on-preset signal. POP is used to clear latches and start logic circuits from a known state following power supply turn-on or interruption.

#### DETAILED CIRCUIT ANALYSIS

Detailed Circuit Analysis is presented as a means of understanding the 5440B/5442A at a component level. Service technicians may find the analyses helpful when using the troubleshooting information presented later in this manual. The analyses are broken down by digital and analog circuits.

#### Digital Circuits

The following discussions are detailed circuit analyses of the digital circuits in the 5440B/5442A. These discussions are referenced to the schematics in the back of this manual. It is recommended that you read the Hardware Functional Overview before the detailed circuit analysis.

The discussions are arranged by assembly or function, whichever is most relevant.

#### CONTROLLER PCA, A16

The Controller PCA works in conjunction with the Memory PCA, the I/O Assembly, and the Guard Crossing PCA to provide for the main control of the digital circuits, and via the Guard Crossing PCA, the analog circuits. The Controller PCA can be broken down into the following functional circuits. Each of these circuits will be discussed in the following paragraphs.

- Boot ROM
- Fault Indicators (LEDs)
- Watchdog
- Front panel UART Interface
- Interrupts
- Timers
- Troubleshooting Switches

Boot ROM, Fault Indicators, and Watchdog

The boot ROM (U36) contains the programs necessary to detect memory (checksum) errors, power supply errors, and some I/O errors. The Z80 microprocessor, (U11) is buffered from

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the main digital bus by U13, U14, U15, and U16 to prevent outside bus faults from inhibiting the power-up tests. On power-up, the microprocessor is instructed to test-boot the ROM memory. When a checksum error is detected, one of the four fault indicators (LEDs) on the Controller PCA (CR2 through CR5) is displayed. If an error is detected in the boot ROM, the microprocessor continues with the test-boot. If there are numerous errors, the microprocessor may hang up. Two seconds after a hangup occurs, a watchdog circuit (U30 and Q1) forces the system RESET line to an active state. As a result, the guarded and unguarded logic is reset, and a fault LED (CR7) on the Keyboard Assembly is turned on via a separately wired line (labeled \*FAULT).

The other fault indicators on the Controller PCA are: MEMORY fault, FPC fault (Front Panel Communication), and INTERRUPTS fault. The MEMORY fault (CR2) occurs if a checksum error is found in the ROMs, RAMs, or EAROM located on the Memory PCA. The FPC fault (CR4) occurs when communication with the Front Panel Controller PCA is impossible. (The fault may be caused by either the Controller PCA or the Front Panel Controller PCA.) This fault causes the microprocessor to wait until the watchdog circuit sets the system into watchdog reset. The RESET signal is sent to the only non-maskable interrupt pin on the microprocessor (NMI). This allows the microprocessor to differentiate between a watchdog reset and a power-up reset. The INTERRUPTS fault indicator is CR3. It stays lit when the interrupt lines are not working properly. This usually indicates that a line is being held active low by a portion of the circuit.

On power-up all the fault indicators are turned on. As the microprocessor determines that the circuits are operating correctly, they turn off one at a time in the following order:

- 1. BOOT ROM/MAIN MPU
- 2. MEMORY
- 3. INTERRUPTS
- 4. FPC (front panel communications)

It is possible that all functions, following the function under test, are operating properly but were not tested because of the watchdog reset. For example, a memory failure will prevent the testing of interrupts and front panel communication.

#### Front Panel UART Interface

The front panel UART interface consists of UART, U25, and its associated support logic. Serial data transmission occurs only when FPINT (front panel controller status line) indicates that it is ready for another byte. When the front panel microprocessor sends data to the main microprocessor, the status line DR (data received, on U25-19) becomes true (high). This causes two other actions. First, the RINT status line (U28-11) is set false, signaling the front panel microprocessor to wait before the next data transmission. Second, the main microprocessor is interrupted with the received data byte. The UART status bits provide the main microprocessor with information on the validity of the incoming data. The status bits are PE (parity), FE (framing), and OE (overrun) error information.

#### Interrupts

There are seven interrupts on the Controller PCA. The priority of these interrupts is determined by the priority encoder, U20. The interrupts may be selectively masked by the interrupt mask circuit (U31, U35, and U37).



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The highest priority interrupt is PSF (power supply fault), and the lowest is IKHZINT (one kilohertz interrupt). The following interrupts are generated on the Controller PCA 1/50 SEC, FPINT, TIMER 1, and 1KHZINT. The PSF interrupt is generated on the Outside Guard Regulator PCA. The GUARDINT (guarded interrupt) is generated on the Guard Crossing PCA, and the IEEEINT (IEEE-488 interrupt) and RS232INT (RS-232 interrupt) are generated on the I/O Assembly.

#### Timers

There are three timers on the Controller PCA. These timers are contained in a single device, an Intel P8253 (U19). The outputs of the timers are used to produce interrupts, at specific intervals, to the main microprocessor. The IKHZINT identifies periods when information can be sent to the other microprocessors and the I/O devices. The 1/50 second (1/50 SEC) interrupt is used as the system clock. TIMER 1 is used to indicate the end of programming or erasing time for the EEROM located on the Memory PCA. Timer 1 also supplies the control line to the Memory PCA to turn off the EEROM power supply. The EEROM power supply will be discussed later in the Memory PCA paragraphs.

#### **Troubleshooting Switches**

Switch S1 and U24 comprise the Troubleshooting Switches circuit. This circuit can be used to help debug certain problems occurring in 5440B/5442A. Switch S1-1 (bit D4) must be closed (active low) on power-up of the instrument, or all switch settings will be ignored. A table that lists the tests associated with the different switch settings and describes the function of the tests is located in Section 4 of this manual.

The memory address allocations for the Controller PCA are listed in Table 2-3.

#### MEMORY PCA, A15

The Memory PCA consists of RAM (U30-32), EPROM (U10-U15), EEPROM (U29, and EEPROM programming circuitry. On power-up, the 6K bytes of RAM are checked for read/write errors, and the 48K bytes of EPROM are checked for checksum errors. The 2K bytes of EEROM are checked for checksum errors before and after programming sequences.

The EEPROM is used to store calibration constants, IEEE-488 address information, and RS-232 baud rate information. The EEPROM circuitry provides a separate programming voltage for the EEPROM. Programming data for the EEPROM is provided by logic circuits on the Memory PCA, with the exception of the TIMER 1 signal from the Controller PCA. The TIMER 1 signal is used to end the programming cycle. It takes 40 seconds to completely erase and write an EEPROM.

Table 2-4 lists the address allocations for the Memory PCA.

#### I/O ASSEMBLY

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The I/O Assembly provides three interfaces in the 5440B/5442A for remote communication. These interfaces are:

- IEEE-488 (talk and listen)
- RS-232 (transmit only)
- 5205/5220 (high power voltage amplifier or high current transconductance amplifier interface)

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DEVICE	ADDRESS/FUNCTION
Memory	
ROM (boot)	0000-1FFF
1/0	
Timer Intel 8253	
Clock 0 (1/50 SEC)	00 hex
Clock 1 (TIMER 1)	01 hex
Clock 2 (1KHZINT)	02 hex
control	03 hex
Clear Timer Interrupts	10 hex
bit d3	Clears the 1/50 SEC interrupt.
bit d2	Clears the TIMER 1 interrupt.
bit d1	Clears the 1KHZ interrupt.
Front panel interface	
and troubleshooting	
switches	04 hex
transmit/receive	18 hex
read status	LSB of troubleshooting switches.
bit d7	2nd bit of troubleshooting switches.
bit d6	MSB of troubleshooting switches.
bit d5	Selects troubleshooting switches.
bit d4	Front panel data received error indicator.
bit d3	Front panel ready to receive data.
bit d2 bit d1	Data received from front panel.
bit d0	A16 UART ready to send data to front panel
	All GART ready to serve data to more parts
Interrupts read interrupts	08 hex
mask interrupts	08 hex
I7	Power supply failure.
16	Guard interface interrupt.
15	IEEE-488 interrupt.
13	1/50 SEC interrupt.
13	Front panel interrupt.
12	RS-232 interrupt.
11 1	TIMER 1 interrupt.
10	1 KHZ interrupt.
Watchdog	
clear watchdog	0C hex
Fault Indicators	
write	14 hex
bit d3	Front panel communications fault.
bit d2	Interrupt fault, interrupt will not clear.
bit d1	Memory PCA (A15) fault.
	ROM boot checksum error.
bit d0	

#### Table 2-3. Controller PCA Address Allocations

DEVICE	ADDRESS
ROM	2000-DFFF HEX
RAM	E000-F7FF HEX
EEROM	F800-FFFF HEX
I/O ADDRESSES Clear chip select Set chip select Clear program Set program Clear output enable Set output enable Turn on programming voltage	20 HEX 24 HEX 21 HEX 25 HEX 22 HEX 26 HEX 23 HEX

Table 2-4, Memory PCA Address Allocations

The IEEE-488 interface allows the 5440B/5442A to be operated by any IEEE-488 compatible controller or to talk with any IEEE-488 device. The RS-232 interface allows the 5440B/5442A to output its test and self-test diagnostic data to any RS-232 compatible printer or monitor. The other interface port allows the 5440B/5442A to work with the Fluke 5205 High Power amplifier or the Fluke 5220 High Current amplifier in the Boost mode.

#### IEEE-488 Interface

The IEEE-488 interface consists of IEEE-488 chip U16, IEEE-488 bus buffers U17 and U19, and associated logic U5 and U18. Bus transceivers U1, U2, and U3 transmit data to and from the IEEE-488 interface circuits and the main controller. The bus transceivers are shared by all three interface circuits.

#### **RS-232 Interface**

The RS-232 interface consists of the UART U11 and the baud rate select chip U12. The RS-232 interface is capable of operating from 50 to 9,600 baud, and is set using the front panel controls or IEEE-488 Interface. The 5440 is configured as a modem. This means that it transmits on J4-3 (RECV) and expects DTR (Data Terminal Ready) on J4-20 to indicate that the receiving device is ready for another byte. The instrument is shipped with DTR jumpered to DSR (Data Set Ready); this holds the DTR line true (high) so that the instrument expects the receiving device to always be ready for transmission. As a result, this jumper may have to be cut to allow a printer to use the DTR line to hold off the 5440 until it is actually ready to receive more data. Some printers, especially those that operate above 1200 baud, need to control the DTR line to function properly with the 5440B/5442A. In this case a jumper on the RS-232 port must be cut.

#### **Boost Interface**

The 5205A/5220A interface circuits are shown on the same schematic page as the IEEE-488 circuits. The 5205A signals are those with the 5205 prefix. The signals for the bus operated 5220A are those with a BC or BD prefix. Signals with the BC prefix are 5220A addresses, and signals with the BD prefix are 5220A data.

A detailed list of the I/O addresses is given in Table 2-5.

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#### GUARD CROSSING (UNGUARDED PORTION)

The unguarded portion of the Guard Crossing PCA (right side of the A14 schematic) provides the communication link (guard crossing) between the main controller (an unguarded circuit) and the guarded circuits. The linking is through optoisolators. The guard crossing consists of a bidirectional serial link UART (U22) with handshake lines and an unguarded reset control line (\*RESET) on P71-9. On power-up, the \*RESET line resets both the unguarded circuits and the guarded microprocessor (U3 pin 6). This action synchronizes the guard and main (unguarded) microprocessors. The rest of the guarded circuits are reset with a guarded reset line (GPOP on P70-28). When the main microprocessor wants to talk to the guarded microprocessor, the guard ready line (GRDY on U9 pin 6) is checked to see if the guard is ready to receive a byte of data. When a correct data command string is sent to the guarded microprocessor is ready to send data to the main microprocessor, the unguarded ready line (UGRDY on U3 pin 19) is checked. This line is controlled by the data received status line (DR) of the guard crossing UART. The maximum transfer speed is 65K baud.

Table 2-6, lists the unguarded I/O addresses.

#### GUARD CROSSING (GUARDED PORTION)

The guarded digital circuits are controlled by the guarded microprocessor, U3 (MC68701) on the Guard Crossing PCA. U3 is responsible for communicating with the main microprocessor on the Controller PCA and executing its commands. The microprocessor is supported by 2K bytes of EPROM, 256 bytes of RAM, a UART, a timer, and 24 lines of I/O.

On power-up, the microprocessor checks its own memory and performs a check on the guarded digital bus. In addition, the five analog pea's are assigned a unique status. Each pea is interrogated for its status, which is then returned on the guarded data bus. Errors or incorrect responses are flagged as faults and reported to main microprocessor.

The Guard Crossing PCA contains three sliding switches S1, S2, and S3. Switch S2, labeled BIT TEST, is only monitored on power-up. Switch S2 causes the guarded microprocessor to enter a state where communication with the main microprocessor is ignored. A walking 0 is sent on the guarded data lines, address lines, and control lines. This self-test may be used to check the proper operation of all I/O lines connected to U3. It also checks the protective resistor networks Z1, Z2, and Z5. This self-test requires that U1 be removed from the pca before beginning the test.

Switch S1, labeled MONITOR, allows the microprocessor to force the guarded control lines to tristate. This essentially removes the guard crossing from the guarded bus, permitting a checkout of the unguarded circuits with a microprocessor troubleshooter (e.g., the Fluke 9000 series). In this state, there is no danger of calling up destructive combinations of relays in the analog pca's. Because of the communication loss, the main microprocessor will report a guard communication fault to the front panel but will continue to operate.

Switch \$3, labeled ACK, controls the status line ACK. This line is driven by the particular analog pca with which the guarded microprocessor is communicating. By closing the switch, the guarded microprocessor assumes that all pca's are receiving the correct data. This allows the 5440B/5442A to be operated during troubleshooting without all the analog pca's being plugged in.

I/O DEVICE	
1EEE-488 IC	40 - 47 hex
RS-232 transmit/receive	48 hex
RS-232 status	68 hex
bit d7	1
bit d6	1
bit d5	Data received by UART indicator.
bit d4	Parity error indicator.
bit d3	Framing error indicator.
bit d2	Overrun error indicator.
· bit d1	Printer terminal ready to receive (0).
bit d0	UART Transmitter buffer empty.
RS-232 baud rate select	70 hex
5220 status	53 hex
bit d7	<b>1</b>
bit d6	1
bit d5	1
bit d4	<b>1</b>
bit d3	1
bit d2	5220 overload
bit d1	5220 operating.
bit d0	5220 in remote control.
5220A control	55 hex
bit d7	
bit d6	1
bit d5	1
bit d4	1
bit d3	Output current through rear.
bit d2	5220 lockout 5220A frontpanel controls.
bit d1	5220 operate.
bit d0	5220 in remote control.
5205 status	
bit d7	5205 attached.
bit d6	5205 trip (fault).
bit d5	5205 operating.
bit d4	Unused.
bit d3	1
bit d2	1
bit d1	"ACK" bit from connector J2.
bit d0	"ACK" from 5220A, connector J3.
5205 control	
bit d7	1
bit d6	1
bit d5	1
bit d4	· • • • •
bit d3	Connect 5440A analog output to J7 (5220A).
bit d3	Connect 5440A analog output to J5 (5205A).
bit d1	5205 remote control.
bit d0	5205 operate.
Dit UV	

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#### Table 2-5. I/O Assembly Address Allocations

I/O DEVICE	ADDRESS/FUNCTION
UART read/write	30 hex
guard status	32 hex
bit d7	1
bit d6	1
bit d5	0
bit d4	Framing error (FE) indicator.
bit d3	Overrun error (OE) indicator.
bit d2	Guard ready to receive data (GRDY).
bit d1	Data received from guard (DR).
bit d0	UART ready to transmit character (TBRE)

#### Table 2-6. Unguarded I/O Addresses

The guarded bus consists of the following signals:

- Eight data lines (GDO GD7)
- Six address lines (GA0 GA6)
- Read (GRD), write (GWR), and acknowledge (ACK)
- Guard reset (GPOP) and guarded power supply monitor (GPSF)
- Analog output to rear binding posts (RO)
- Two DAC control lines (DAC relay logic select, DRLS and DAC analog multiplexer select, DAMS)

The data, address, read, and write lines are controlled by the guard microprocessor. The ACK line is controlled by the analog pea being addressed. The RO line is controlled by the slot in which the Output PCA is placed. This line is active low when the Output PCA is installed in the slot providing rear output. The Inside Regulator PCA produces the GPOP and GPSF (guarded power supply fault) signals.

IC U5 on the Guard Crossing PCA is a watchdog circuit that trips if the guarded microprocessor stops operating. When the watchdog trips, the analog buffers are set to their power-up state by the GPOP signal, and the guard fault indicator (LED CR1) lights. This generally occurs if the guard microprocessor is trying to communicate with the main microprocessor (and the main microprocessor cannot read the data). The watchdog times out after two seconds. The guard microprocessor will attempt to restart after clearing the analog buffers. If the main microprocessor continues to be unable to communicate, the guard crossing circuits will stay in an infinite loop sustained by the action of the watchdog circuit.

#### FRONT PANEL CONTROL LOGIC

# The front panel control logic is located on the Front Panel Controller PCA. The front panel control logic receives inputs from the Keyboard Assembly and the Procedure Storage Module. The front panel interfaces the instrument to the user and supplies user input to the main logic. The front panel also provides the user with messages on the status of the instrument and general operating menu selections.


#### FRONT PANEL CONTROLLER PCA, A2

The Front Panel Controller PCA provides the main control of the front panel logic. This pca provides the following:

- 32K bytes of EPROM (U22)
- 4K bytes of RAM (U20 and U21)
- A 4 millisecond clock (U9 and U13)
- A LED fault indicator (CR4)
- Troubleshooting switches (U19 and S1 S4)
- A 40-character dot matrix Vacuum Fluorescent Display (VFD) interface
- Main control logic serial interface (UART U5)
- Keyboard interface
- 16-Segment VFD interface
- Procedure Storage Module interface
- EEPROM control

To reduce spurious RFI emissions from the front panel, the front panel microprocessor clock frequency is reduced to one megahertz, and in general, the front panel control logic operates at a slower speed than the main control logic.

On power-up, the front panel fault LED, CR4 (FPC), is turned on. After the front panel microprocessor (U15) checks the RAM, ROM, and interrupt circuits, the LED is turned off by reset line RST. Interrupts are generated by the four millisecond clock U9 and U13. After power-up, the front panel attempts to communicate with main control logic through the UART U5. If communication between the front panel and main control logic is not established or breaks down, the main control watchdog circuit will be triggered after two seconds. When the watchdog circuit triggers, the reset line at J1-14 (RST) to the front panel becomes active and turns on CR4. The main watchdog also sends the FAULT signal to the keyboard to light CR7, the front-panel fault annunciator. If the 5V logic supply is inoperative, only CR7 on the keyboard will light, because it and the main watchdog circuit are both powered by the HR (High Reliability) 5V supply.

For communication to begin, the FINT (front panel ready) and RINT (rear or main ready) handshake lines must indicate that the microprocessors are ready for data. The front panel FINT line is controlled by the data received (DR) status line (U5 pin 19). Until communication is established, the message, FRONT PANEL RUNNING appears on the dot matrix display. Serial communication with main control logic circuits occurs at 65K baud.

The dot matrix display consists of a vacuum fluorescent display of 2 lines of 20 characters in a 5- by 7-dot character pattern. The display is controlled by state machine U47 and decoder U48. The state machine advances address counter U39 and U46, which provides six bits of synchronous address control to RAMs U42 and U43 through buffer U41. Addresses 0 through 39, corresponding to the locations for each dot-matrix ASCII character, are

addressed sequentially. As each character is accessed in RAM, PROM U44 presents one column of information on its output to Parallel-In, Serial-Out U45. Since five columns are needed to fully represent the ASCII character, the column addressing is accomplished with one half of binary counter U49. The column advance is controlled by the state machine. The loading of U45 and the subsequent scrial shifting is also controlled by the state machine. Once one column of character information is parallel loaded into U45, it is shifted into the display drivers U4-U6. Seven shifts are accomplished per column. The shift count, ENDSHIFT, is stored in one half of U49 and fed back to the state machine. Other feedback terms are the end column count, ENDSCAN; the state of the display refresh clock, LSCLK; and whether the address is odd or even, 2NDWORD. The display drivers are serial-in, parallel-out, high-voltage VFD drivers. The shifting and latching is again controlled by the state machine. Multivibrator U50 provides the required refresh timing for the display. Grid control is accomplished by providing a data input of 1 to the grid driver U7 on address 0 of the address counter. This 1 is serially shifted to each address to provide a unique grid drive per character column. Since the display has two rows, the top and bottom corresponding characters are driven by one grid. This necessitates loading two characters of information into the character drivers. As each grid is activated during the refresh cycle, the top and bottom character will be lit.

The 16-segment display consists of a Vacuum Fluorescent Display of one line of 12 characters in a 16-segment alphanumeric pattern. The display is similar in control to the dot matrix display (described above). The display is controlled by state machine U64 and decoder U65. The column count and shift count is advanced in binary counter U83. Address counter U56 provides a four-bit address to RAMs U59 and U60 through buffer U57. The segment information is decoded through PROM U61 and loaded into Parallel-In, Serial-Out U62. Only two columns of information are needed to describe one alphanumeric pattern. Eight shifts are made to load the information into the digit driver U2. Grid control is accomplished in the same manner as the dot-matrix display with grid driver U3. Multivibrator U67 provides the refresh for the display. U68 synchronizes the feedback of LSCLK for both the dot matrix and the 16-segment display.

Like the Controller PCA, the Front Panel Controller PCA has four troubleshooting switches. These switches are scanned during power-up. Switch S1 must be closed during the scan to enable the troubleshooting routines. During these routines, communication between the front panel and the main control logic is suspended. Because of this break, the main control logic watchdog circuit must be disabled, either by removing the pca or jumpering E5 to E6 on the Controller PCA. A table that lists the tests associated with the different switch settings and describes the function of the tests is located in Section 4 (Maintenance) of this manual.

Table 2-7 lists the addresses and bit assignments for front panel operation.

The front panel also contains the necessary circuits to interface with the Keyboard Assembly, the Display Control PCA, and the Procedure Storage Module. Information on these interfaces is given in the following paragraphs.

# KEYBOARD ASSEMBLY, A1

The Keyboard Assembly does not provide any interrupts to the front panel microprocessor. As a result, the keys must be continuously scanned for keystrokes. To initialize the keys, an FF (hex) is sent to front panel I/O address at 40 (hex). The keys are read from I/O address 40 (hex), bits d0 through d7. Reading any value but FF (hex) indicates that a keystroke is occurring. On detection of a keystroke, the front panel microprocessor sends a "walking 0" to each row sequentially. This detects a low on the key pressed, by way of buffers U4 and U5. Only the cursor control keys repeat their function continuously while the key is depressed.



The keyboard also contains the annunciator LEDs, CR1 through CR6, used to indicate the instrument configuration. The drive and controlling electronics for these annunciators (U33) are on the Front Panel Controller PCA. Fault annunciator CR7 is lit by the FAULT signal coming from the main watchdog circuit.

DEVICE	ADDRESS/FUNCTION
Memory Addresses	
EPROM EAROM RAM Dot Matrix Display	0000-7FFF (hex) C000-C7FF (hex) E800-F7FF data is ASCII - 20 Hex (ex A = 21 hex)
I/O addresses	
I/O addresses UART main logic interface front panel status bit d7 bit d6 bit d5 bit d4 bit d3 bit d2 bit d1 bit d0 interrupt clear keyboard indicator LEDs bit d7 bit d6 bit d5 bit d4 bit d3 bit d2 bit d4 bit d3 bit d4 bit d4 bit d3 bit d4 bit d3 bit d4 bit d3 bit d4 bit d3 bit d4 bit d5 bit d4 bit d4 bit d4 bit d5 bit d4 bit d4 bit d5 bit d4 bit d4 b	0 (hex) 10 (hex) 1 1 UART transmitter buffer empty. Parity or framing error. Main microprocessor ready for more data indicator. Overun error. Clock interrupt status. Data received in UART from main microprocessor indicator. 10 (hex) 20 (hex) 0PR LED STBY LED EXT (guard) LED EXT (guard) LED EXT (sense) LED ON (divider) LED REAR LED not used not used 30 (hex) 1 1 Bits d5 - d3 represent the revision number of the
bit d3 bit d2 bit d1 bit d0 keyboard scan front panel fault LED troubleshooting routines 16-segment VFD select	front panel. M1 M2 0 40 (hex) 50 (hex) write 50 (hex) read 60-6B (hex) 2

**Table 2-7. Front Panel Address and Bit Assignments** 

DEVICE	ADDRESS/FUNCTION	
storage module control	70-77 (hex)	
clear CS	70 (hex)	
clear PGM	71 (hex)	
Enable latch	72 (hex)	
U56 on front panel		
controller PCA.		
set CS	73 (hex)	
set PGM	74 (hex)	
Disable latch	75 (hex)	
U56 on front panel		
controller PCA.		
Clear programming	76 (hex)	
voltage to 6 volts.		
Turn on programming	77 (hex)	
voltage (21V - 25V dc).		

#### Table 2-7. Front Panel Address and Bit Assignments (cont)

M1 and M2 represent the status of the storage module. If M1 and M2 are 0, then the module is write protected. If M1 is 0 and M2 is 1, then the EAROM is made by Hitachi. If M1 is 1 and M2 is 0, then the EAROM is made by Intel. If M1 and M2 are 1, then no storage module is connected. These status bits are set by the factory.

2 For digits:

Write to 6X (where X = A hex, for the leftmost char (sign) and X = 0 (hex), for the rightmost char (units)

The data bits used are 10 hex for 0 to 19 hex for 9, 1A for M, 1B for V, 1C for A, 1D for +, 1E for —, 1F for blank.

#### **DISPLAY CONTROL PCA, A2A2**

The display control PCA consists of the display drivers for both the dot matrix and the 16-segment displays, the vacuum fluorescent displays, and a switching power supply. The switching power supply provides the cathode, anode, and grid voltages for the two displays. Power and control signals for the display are brought through connector J4.

# PROCEDURE STORAGE MODULE

The Procedure Storage Module contains a 16K (2K x 8) EEPROM (U1) and protection circuits (current-limiting resistors). Write-protect switch S1 on the module enables or disables the write capability to the module. The programming voltage and control is provided by the Front Panel Controller PCA. This circuit is exactly the smae as the EEPROM circuit described in the discussion of the Memory PCA.

# **Analog Circuits**

The following discussions are detailed circuit analyses of the analog circuits in the 5440B/5442A. These discussions are referenced to the schematics in the back of this manual. The discussions are arranged by assembly or function, whichever is most relevant.

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# **GUARDED XFMR TERM PCA, A11**

The Guarded Xfmr Term PCA is responsible for converting incoming line voltages in the range of 100V to 240V ac, to the required ac voltages used by the Filter A PCA, the Filter B PCA, and the Outside Guard Term PCA. Switches S1, S2, and S3 provide the means of configuring the primary of T1 to allow the 5440B/5442A to accept input line voltages from 100V to 240V ac. The switches are set according to the line voltage source. A spark gap device (E1) is placed across the primary windings to protect the instrument from incorrect line voltage switch settings. The primary winding, either directly or by autotransformer action, provides 115V ac to the fan assembly, the front panel power-on indicator, and the Outside Guard Term PCA. The secondaries of T1 provide fuse-protected ac voltages to the Filter A PCA and Filter B PCA.

### FILTER A PCA, A12

The Filter A PCA receives eight different ac voltages from the Guarded Xfmr Term PCA and produces 13 different output voltages. These outputs consist of 12 filtered and unregulated dc voltages and one ac voltage. The ac output voltage on P4-32 goes to P60-33 on the Inside Regulator PCA. The ac output voltage is used to trigger the guarded power-on-preset circuit (GPOP) on the Inside Regulator PCA. Most outputs have separate commons that allow them to float independently of one another. Each dc power supply uses a full-wave rectifier. Rectified signals are passed through capacitive input type filters before being used as outputs.

#### **INSIDE REGULATOR PCA, A10**

The Inside Regulator PCA provides regulated voltages for the guarded analog pca assemblies. In addition to the regulator circuits, this assembly contains circuitry that continuously monitors the output voltage of the regulators and provides a fault signal if any supply deviates from nominal by more than about 12%. The monitor circuits consist of a voltage comparator and resistive dividers arranged to balance a positive voltage against a negative voltage. If either the positive or the negative voltage deviates from nominal by more than the predetermined limits, the comparator trips and produces a logic signal indicating a fault condition. When a problem is detected, an LED indicator (CR21), located at the top center of the pca, is turned on and the guarded power supply fault line (GPSF) is pulled low. The GPSF signal is sent to the guarded microprocessor, which in turn informs the main microprocessor to send the appropriate information to cause an error message to appear on the Alphanumeric Display. Certain power supply faults that will cause the 5440B/5442A to malfunction can go undetected by the monitoring circuit. Excessive power supply ripple or oscillations are two types of faults that cannot be detected by the monitoring circuit.

The comparator circuits that monitor regulator outputs common to S-COM receive their operating voltages from the  $\pm 17S$  supplies. Other comparators, which are isolated from S-COM, receive operating voltages from the regulators they monitor and couple their logic output signals back to the S-COM reference by means of opto-isolators. The fault circuits receive operating voltage from a separate 5V dc power supply designated GHR  $\pm 5$  (guarded high reliability,  $\pm 5$  volt supply). This separate power supply allows the monitoring circuits to operate when the guarded logic power supply is malfunctioning.

Two of the regulated supplies provide power for logic circuits, which could be damaged by an overvoltage condition. To prevent this from happening, crowbar circuits have been provided that monitor the output of the +5V DAC and +5 LH supplies and fire a triac, which will open an input fuse if an overvoltage condition occurs. The regulator circuit in the +5 LH

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supply receives operating power from the +175 supply and, if F2 blows, the regulator attempts to provide full output current through Q19 from the +175 supply. To prevent this, Q24 and Q25 sense an open fuse and turn off the regulator circuit U10.

# OUTPUT PCA, A4

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The main function of the Output PCA is to take the low power signal from the Preamp PCA and amplify it to the required output level.

The output power amplifier consists of two transistors, Q3 and Q4, connected in a bridge configuration with the two auxiliary supplies, +30 OP and -30 OP. OP COM, the common connection for the two supplies, is the high output of the amplifier. The emitters of the two transistors connect to the low output through current-limit sensing resistors R7 and R8. The input signal to the output amplifier is applied to the common connection of two diodes, CR1 and CR2. Current through the diodes produces a voltage drop that biases transistors Q3 and Q4 on, keeping them in a linear operating region of the transconductance curve. Excessive current through the current-sensing resistors, R7 or R8, produces a voltage drop that turns on one of the current-limit transistors, Q1 or Q2. This diverts current from the base drive of Q3 or Q4, thereby limiting output current.

For the 11V and 22V ranges, OP COM is connected to OUT HI (P10-1) by the closure of relay K3. For the 275V and 1100V ranges, the OP COM signal is fed to the Output/HV Control PCA where it is used to control the high voltage power supply ( $\pm$ KV). This supply is switched to the output by K2 while K1 controls the polarity.

Current-limiting transistors, Q1 and Q2, limit the maximum output current to approximately 80 mA. The output of Q1 and Q2 removes some of the drive current from the output transistors (Q3 and Q4), holding the current near the maximum until the controller sets the instrument to standby. The current is also monitored by the main microprocessor via the monitoring system. A voltage (I COM), proportional to the output current is sampled every two seconds by the monitoring system. The main microprocessor compares this voltage against software limits. These limits have a default setting of  $\pm 65$  mA at power-up and may be changed to other levels by the user. If the current limit is exceeded, the main microprocessor places the instrument into standby.

For the divided output ranges of 2.2V and 0.2V, the unit remains configured in the 22V range but routes voltages through the precision divider network to the front panel or rear panel output terminals labeled DIVIDER. Relay K6 connects OP COM (and the local sense signal, 20V LOCAL) to the input of the divider. Relay K5 selects the ratio used to develop the 2.2V DIVIDER output (divider ratio of 10) and the 0.22V DIVIDER output (divider ratio of 100).

The Zero Amplifier (U9) is used only during the output zeroing process of the internal calibration. During internal calibration, K7 shorts the input to U9, and the analog-to-digital (A/D converter) makes a measurement of the output of U9 to establish an absolute value for zero. Relay K7 is then energized, connecting the OUT HI signal to the input of U9. Another measurement is taken. The difference of the two measurements is proportional to the offset of the 5440B/5442A output. The Zero Amplifier has two gain ranges of 100 and 1000. The gain range is selected by Q23 (FET). When FET Q23 is on, a gain of 100 is selected. When FET Q23 is turned off, a gain of 1000 is selected. The output of U9 (SDPZC) is sent to a multiplexer on the Output/HV Control PCA to be read by the a/d converter.

#### CAUTION

The Sense-Current Cancellation circuitry is at the same electrical potential as the output voltage of the calibrator. To avoid electrical shock, use extreme care in servicing this circuit.

U1 and its associated circuitry provide a sense-current cancellation function that effectively removes the error due to the voltage drop in long sense leads. This is accomplished by diverting the sense current, which would ordinarily flow through the sense lead, through a current source or sink, (depending upon polarity of the output) and back to the low output.

R13, R14, and R15 are connected in series as the range resistor for the high voltage (1100V) range of the cancellation circuit. The + input terminal of the op-amp U1 is connected to the high-sense terminal. By feedback amplifier action, the - input terminal of the amplifier is also at the potential of the high-sense terminal. The 5 M $\Omega$  resistor between low sense and the - input terminal then produces a current proportional to the output voltage. At 1000V output, the current is 200  $\mu$ A—the same value as the low-sense current at 1000V output. The current flowing in the range resistor is provided by the output of the op-amp U1 and also flows through the resistor R4. To produce the current through R4, the output voltage of the op-amp must then be 10V, assuming 200  $\mu$ A output current through R4. The 10V drop produces another current of 500  $\mu$ A in R11, connected between the amplifier + input terminal and the amplifier output. This current flows to the high-sense terminal to exactly cancel the 500  $\mu$ A in the high-sense lead. The ultimate source of both currents is the power supply for the op-amp, which is connected to the high-output terminal of the calibrator. Both the 200  $\mu$ A current in the low-sense lead and the 500  $\mu$ A current in the high-sense lead have thus been diverted from the external-sense leads to the high-output terminal, where the current is returned through the output stage of the amplifier and to the low output.

The range resistor for each range of the sense-current cancellation circuit is selected by closing the proper combination of relays K2, K9 and K10. R30, a 2K resistor in series with the range resistors, provides a divided output voltage signal to the output voltage monitor function.

The main microprocessor, via the monitoring system, monitors the output voltage of the instrument by measuring the voltage across R30. The voltage across R30 is sent to a multiplexer (via SDPOV) on the Output/HV Control PCA and then to the REF/DAC Digital PCA where it is read by the a/d converter. The main microprocessor takes the a/d converter reading and converts it to output voltage and compares this to the programmed output level. If the monitored value does not agree with the programmed level (within 5%), then the main microprocessor sets the instrument into standby and sends an error message to the Alphanumeric Display. Following a change in the programmed output of the calibrator, the output voltage monitor function is suppressed for four seconds to allow the output voltage to settle. Following this delay, the output voltage will be sampled every two seconds, and the output will be switched to standby if the voltage is outside the tolerance limits.

#### OUTPUT/HV CONTROL PCA, A5

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The Output/HV Control PCA provides the following in the 5440B/5442A:

- Generates the digital control signals for the relays on the Output PCA.
- Produces the triac control signals (TS1 through TS4)
- Produces the square wave drive signal (IB + and IB ) for the Filter B PCA
- Contains part of the monitoring system circuitry.

The digital logic address lines (GA0 through GA6) are buffered by U22 and U23, then sent to decoder U27. The four outputs of the decoder proceed to an eight-input OR gate (U35). The signal from U35-13 drives U37-6, which inverts the signal at U37-4 to drive U38-13 (a

tri-state buffer). When the Output/HV Control PCA is addressed, the output of U-38 pulls the Acknowledge (ACK) line low. The data lines (GD0 through GD7) are buffered by U20, U21 and part of U22, then proceed to four latches (U24, U26, U28, and U29). The latches are clocked by the signal  $\overline{GWR}$  (Guarded Write) from the main microprocessor and by the appropriate address. The decoded address lines and the  $\overline{GWR}$  signal are sent through gates U36 and U37 to the clock (CLK) inputs of the latches. The latches are cleared by  $\overline{GPOP}$ (Guarded POP). The outputs of U29 go to relay drivers U31 through U34. These relay drivers are used to energize the relays on the Output PCA.

Four of the outputs from U28 are buffered by U30 and become the triac control lines TS1 through TS4. These control lines are then sent to the Filter B PCA.

The other outputs of U28 are used as follows. The ZCA line (U28-9) controls the gain range of the Zero Amplifier on the Output PCA. Output U28-6 (CS2) is used to control transmission of the square-wave drive signal and to prevent K7 (on the Output PCA) from closing during high voltage operation. The RESET output (U28-5) prevents U1 from oscillating when it is not in high voltage operation.

The two outputs (CT1 and CT2) from latch U24 are used to control relay driver U7. The four outputs of U26 are the address lines for the multiplexer U25. This multiplexer takes inputs from eight different sources and sends them out on a single line (ANALOG DATA OUT) to the a/d converter on the REF/DAC Digital PCA. The ANALOG DATA OUT line contains the multiplexed, monitoring system signals.

The revision level of the Output/HV Control PCA can be determined by reading the tri-state buffer, U20. The inputs to this buffer are configured (by tying inputs to LCOM or + 5LH) to represent the pca's revision level. The buffer U20 is enabled (read) when the guarded read line \*GRD and the appropriate address (from address decoder U27-7) are sent to AND gate U36 (and subsequently NOR gate U36).

The analog circuits of the Output/HV Control PCA generate a square wave whose amplitude is varied by the OP COM signal from the Output PCA. This square wave eventually goes to the Filter B PCA where it is used to generate the high voltage output for the 275V and 1100V ranges.

U1 is a 555-type timer IC, connected to produce a symmetrical square wave of fixed amplitude. The output, pin 3, is connected to a variable attenuator consisting of a series resistor, R5, and a shunt-connected FET, Q1. The amplitude of the square wave passed through the attenuator is a function of the conductance of the FET, Q1, which is controlled by the FET gate signal. A more negative signal on the gate decreases conductance of the FET and increases the amplitude of the square wave passed to the following amplifier stages.

The signal on the gate of Q1 is derived from OPCOM, originating on the OUTPUT PCA, A4, and modified by the reversible polarity amplifier, U2. The reversible polarity amplifier is necessary because the polarity of the OPCOM signal for an increase in output voltage reverses with a change in output polarity of the calibrator. An understanding of the operation of the circuit is best obtained by following the signal path through the amplifier in response to a change in output voltage.

Assume that the calibrator is programmed to deliver a positive polarity voltage to the high-output terminal at a potential greater than 22V. Also assume that an increase in output voltage is programmed. The increased voltage requires a higher output from the high-voltage auxiliary supply and, consequently, it requires a higher amplitude drive signal from the

square-wave generator that provides the primary power source for the high voltage transformer. For a positive polarity output, relay K1 on the A4 OUTPUT PCA is de-energized. The drive for K1 comes from U31, pin 3, on the A5 OUTPUT/HV CONTROL PCA. When K1 is de-energized, U31, pin 3, is high (+5V). This point is also connected to R103 (sheet 2 of the schematic diagram for A5), which turns off Q16 and Q15. With Q15 turned off, the FETs Q13 and Q14 are turned on fully. Q14 ties the + input of the amplifier U2 to ground, and Q13 connects the incoming OPCOM signal to the inverting input of U2 where it is amplified and inverted and applied to the gate of the attenuator FET, Q1. For an increase in output voltage in the positive polarity, the OPCOM signal is more positive. The positive-going signal is inverted by U2 to become more negative when applied to the attenuator, thereby increasing the amplitude of the square wave. If the calibrator is programmed for a negative output voltage, the OPCOM signal will be more negative for an increase in output voltage, so the amplifier U2 is programmed to be a follower instead of an inverter. For negative polarity, the relay K1 is closed, and the signal to the base of Q16 is low, turning on Q16 and Q15. The FETs Q13 and Q14 are turned off, and the amplifier U2 is then configured as a follower with the negative-going OPCOM signal applied to the + input and passed to the attenuator FET. The negative-going signal decreases the conductance of the FET U1, increasing the amplitude of the square-wave signal. When the high-voltage circuits are not enabled (the calibrator is in one of the low-voltage ranges), the drive signal CS2 applied to the base of Q11 is low, turning on Q11 and Q10, and thereby shorting out the output of the amplifier U2. With no negative drive signal, FET Q1 is turned on fully, shorting any square-wave input signal to ground. As further assurance, the square-wave oscillator, U1, is turned off by a low signal applied to the RESET terminal, pin 4.

#### FILTER B PCA, A13

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The Filter B PCA contains the circuitry that generates the voltages used to produce output voltages above 22V. It also contains the rectifiers and filter for the 20V oven supply.

The squarewave circuit on the Output/HV Control PCA provides the base drive for Q12 and Q13. This push-pull stage drives the primary of a high voltage transformer, T1. The resulting high-voltage square wave is rectified by a bridge rectifier (CR23 through CR26), then filtered by C16. This filtered high voltage supply  $(\pm KV)$  is sent to the Output PCA.

In order to minimize the power dissipation in Q12 and Q13, their supply voltage is varied in four steps depending on the 5440B/5442A output voltage. Taps on the power transformer are selected by turning on the appropriate pair of triacs, Q1 through Q8. The triac pairs are controlled by photocoupler triac drives U1 through U8, which are turned on by the Output/HV Control PCA via lines TS + and TS - . The selected transformer taps are rectified by one of four full-wave rectifiers (CR19 through CR22) and then filtered by C21 and C22 to provide + TSV(P) and - TSV(P). Transistors Q9 and Q10 are used as current sources to provide keep-alive current to the selected triac gates while the ac voltage waveform is below the conduction level for the triac. Transistors Q11 and Q14 sense the current being drawn by Q12 and Q13. If this current becomes excessive, a signal (I LIM + and I LIM -) is sent back to the Output/HV Control PCA, which reduces the drive to Q12 and Q13 so they are not damaged.

The supply voltage for the three ovens in the 5440B/5442A is located on the Filter B PCA. Bridge rectifier CR17 rectifies the 20V ac signal (+20V OVN AC), from the power transformer, then C18 filters it to produce the unregulated 20V oven voltage (+20V OVN, OVN COM).

# SAMPLE STRING PCA, A6

The Sample String PCA contains the precision resistors that are used to determine the gain of the output amplifiers. These resistors are in a temperature stable oven to minimize the drift due to changes in the external temperature and self heating at high voltage. The Sample String PCA also contains the control circuits for this oven.

The simplified circuit diagram in Figure 2-8A shows how the Sample String PCA relates to the other analog circuits. In the 5440B/5442A, the gain of the output loop is a function of RF divided by RIN. Relays on the Sample String PCA can be energized by the main microprocessor to select one of four gains, 1, 2, 25, or 100. The resistor configurations for these four gains are shown in Figure 2-8B. The 11V from the DAC on the REF/DAC Analog PCA is amplified by 1 to get the 11V output range, by 2 to get the 22V output range, etc.

The relays on the Sample String PCA allow the resistors to be placed in a special bridge configuration for internal calibration. Figure 2-9 is a simplified diagram of the Gain Shift Measurement Configuration. The 13.2V reference voltage is one leg of the bridge, the DAC amplifier/filter inverts the reference voltage to provide a second leg of the bridge. The parallel combination of R32 and R35 forms a 20 k $\Omega$  resistor for the third leg, and the range resistor to be compared to the R32/R35 combination is the fourth leg. The range resistors are switched by the relays to provide parallel combinations of resistors that equal nearly 20 k $\Omega$ kilohm so that they may be compared to the R32/R35 20 k $\Omega$  resistor in a 1:1 ratio as equal legs of the bridge. The bridge unbalance is measured by the Analog-to-Digital (A/D) Converter, which is preceded by the Prc-Amp configured as a follower amplifier with a gain of 600 to amplify the microvolt-level signals to the proper level for the A/D Converter. For the 11V range gain determination, the parallel combination of R31 and R34 is switched into the bridge for comparison. For the 22V range, the combination of R30 and R33 is compared, and the overall range correction is calculated as the sum of corrections for R31/R34 and R30/R33. For the 1100V range, ten 200 k $\Omega$  resistors are used in series to obtain a resistance of 2 M  $\Omega.$ The relays K6, K7, K8, and K9 are closed in the calibrate mode to place the ten resistors in parallel to obtain a 20 k $\Omega$  resistor that can be compared against the R32/R35 20 k $\Omega$ . Since the percent error in the parallel arrangement is the same as the percent error in the series arrangement, the correction factor may be calculated from this measurement. The same resistors are used in the 275V range by connecting them in a series/parallel arrangement, so the correction factor is the same for both the 1100V range and the 275V range.

The oven control circuits of the Sample String PCA start with two thermistors, (RT1 and RT2) that have a negative temperature coefficient. Thermistor RT1 is used in the oven-temperature control circuit, and RT2 is used in the oven-temperature protection circuit.

When the 5440B/5442A is turned off and the oven is cold, both thermistors (RT1 and RT2) have high resistance. When the 5440B/5442A is turned on, Q3 conducts and the 20V oven heater supply (VOVN) is applied to the collectors of a Darlington pair (Q1 and Q2). The inverting input of U15 is connected through R12 to SCOM. Until the oven reaches the desired temperature, the voltage at the non-inverting input of U15 is above 0V, thus the output of U15 is a positive voltage. The positive voltage at the output of U15 turns on the Darlington pair and applies VOVN to the heater winding.

The oven temperature is maintained as follows: A zener diode, (VR8) provides 6V at the top of R8. The same 6V is applied to U15-2 through R6. The op amp U15 inverts this voltage and applies it to the bottom of thermistor RT1. As the oven temperature approaches  $55^{\circ}$ C, the resistance of RT1 approaches that of R8. This causes the non-inverting input of U15 to approach 0V, reducing the output at U15-7, thus reducing the current source to the heater winding. When  $55^{\circ}$ C is reached, the output of U15 is reduced to where the current, supplied to the heater winding, is just enough to maintain the temperature of the oven.



Figure 2-8. Sample String PCA, Simplified Circuit Diagram



Figure 2-9. Gain Shift Measurements, Configuration of Analog Circuits

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The heater winding is a coil of resistive wire around an aluminum block that is in the oven. The precision resistors are placed into holes drilled in the aluminum block. The two thermistors are also set into holes of the block so that the control circuit holds the temperature of the entire block constant, and the oven temperature protection circuit accurately monitors the oven temperature.

The oven temperature protection circuit consists of RT2, U16, Q3, and Q4. As long as U16-2 remains more positive than U16-3, the output of U16-7 is a positive voltage. This positive voltage turns on Q4 and subsequently Q3, supplying 20V (TP5) to the heater coils. If abnormal conditions cause the oven to overheat, RT2 decreases in resistance, making U16-3 more positive than U16-2. This causes the output at U16-7 to become negative, removing the oven supply from the heater windings. This circuit limits the oven temperature to a maximum of  $65^{\circ}$ C.

When the operator initiates the analog self-tests, the signals at TP1 and TP2 (OT1 and OT2) are measured to determine if the oven is at the proper temperature. TP1 and TP2 are measured by the main microprocessor via the monitoring system (and the multiplexer on the Preamp PCA). The signals OT1 and OT2 (Oven Temperature 1 and Oven Temperature 2) are equal when the oven temperature is correct. If the analog self tests are performed before the instrument has time to stabilize, the offset of the two signals (test points) results in a low oven-temperature error message on the Alphanumeric Display.

#### PREAMP PCA, A7

The digital logic circuits of the Preamp PCA are discussed first. Address lines GA1 through GA6 are buffered by U13, then sent to decoder U16, which decodes the addresses used by this pca. The three outputs of U16 are sent to U17, which is a multiple-input OR gate. The output of U17 drives Q14, which pulls the \*ACK (acknowledge) line low whenever the Preamp PCA is addressed.

Data lines GD0 through GD5 are buffered by U11. Data lines GD6 and GD7 are buffered by U12. The buffered data lines are sent to the inputs of latches U19 through U22. The clock signal for these latches comes from U15, which ANDs the appropriate address from U16 and the \*GWR (guarded write) signal from U12-12. The latches are cleared by the \*GPOP signal from U12-4. The outputs of latches U21 and U22 are connected to relay drivers U23 through U25, which close relays K1 through K5. The outputs of latch U20 drive amplifiers Q9 through Q11. The amplifiers (Q9 through Q11) drive the FET switches (Q3 through Q5) on and off. The output of latch U19 is sent to the multiplexer (U18). This multiplexer connects any one of seven test signals to the ANALOG DATA OUT (analog data output) line.

The revision level of the Preamp PCA can be determined by reading the tri-state buffer, U10. The inputs to this buffer are configured (by tying inputs to LCOM or +5LH) to represent the pca's revision level. The buffer U10 is enabled (read) when the guarded read line \*GRD and the appropriate address (from address decoder U12) are sent to AND gate U15 (and subsequently NOR gate U15).

The analog circuits of the Preamp PCA form a low-noise, low-drift, high-gain amplifier whose output drives the power output stage on the Output PCA. The amplifier's input is the output of the DAC on the REF/DAC Analog PCA.

The PREAMP SJ (Preamp Summing Junction) signal comes in at P41-13. Slow (dc and low-frequency) changes in this signal are applied to U3, a differential amplifier, through L2 and R17. The collectors of U3 drive U4, a common-base stage, which then drives U5, U6,

and U7. From here the signal is routed through K5 to PREAMP OUT at P41-38. Rapidly changing signals are directed to U6 through R81/C82, bypassing the relatively slowly responding circuits of U3, U4, and U5.

During internal calibration, relay K5 is closed, configuring the Preamp as a non-inverting amplifier with a gain of approximately 600. (Refer to Figure 2-9 for a simplified diagram of the Preamp, as configured during internal calibration.) The output of the Preamp (B-CAL) goes through a protection circuit to multiplexer U18. This connects the Preamp to the ANALOG DATA OUT line, which goes to the a/d converter on the REF/DAC Digital PCA.

The oven control circuitry on the Preamp PCA is identical to the one used on the Sample String PCA, except for the temperature (which is maintained at 50°C instead of 55°C) and the oven temperature protection circuit. The oven temperature protection is provided by thermistor RT2. If the oven control circuit malfunctions and the oven temperature rises to more than 65°C, Q15 conducts and clamps the base of Q12, thus preventing further temperature rise. The voltage at the junction between RT2 and R87 follows the oven temperature during self test. This point is at or close to zero volts when the oven is at the proper operating temperature.

#### **REF/DAC DIGITAL PCA, A8**

The REF/DAC Digital PCA generates two square wave signals used by the pulse-width modulated DAC on the REF/DAC Analog PCA. It also contains the a/d converter used by the monitoring system to relay information to the main microprocessor.

The square wave drive signals originate from an 8-MHz oscillator (U12) feeding a frequency divider (U13). The divide-by-four output (U13-4) of the frequency divider is inverted by U25 and applied to U11, a programmable interval timer (PIT). The PIT is configured to produce two 83-Hz square waves that have a programmable duty cycle. The duty cycle is determined by the number of counts loaded into U11 by the main microprocessor. The number of counts range from zero (0% duty cycle) to 24095 (100% duty cycle). Each count requires 15 bits, and the count is loaded into U11 in 8-bit bytes from the guarded data bus (GD0 through GD7). The address lines (GA0 through GA6) are buffered by U3 and U4. GA0 and GA1 select the register in U11 that will be loaded with data. Address lines GA2 through GA6 are decoded by U5 and fed to U6. The output of U6 is the acknowledge (ACK) signal to the main microprocessor, indicating that the address has been decoded. The output from U5, pin 15, goes to the chip select (\*CS) for the register U11. This signal, in conjunction with \*WR, loads the data into U11. The output U5, pin 15, is also used to clear the D-type flip-flop U22. When U22 is cleared, its Q output goes high and enables the divider U13. The POP (Power On Preset) is applied to the preset input of U22, which sets its Q output low, disabling the divider U13 and hence its 2-MHz clock output.

The two outputs of U11 are buffered by U25 and drive photocouplers U17 and U18. The outputs of the photocouplers are sent to the D input of U19 and U20 (Dual D-type flip-flops). The flip-flops are clocked by the 2-MHz output of U13, which is fed through buffer U25 and pulse transformers T1 and T2. The outputs of the pulse transformers are amplified by Q1 and Q2 before being applied as the clock input to U19 and U20. The outputs of U19 and U20 follow their D inputs in unison with the 2 MHz clock to ensure that the square waves to the REF/DAC Analog PCA have jitter-free transitions. This is done to prevent rattle and noise on the output of the REF/DAC Analog PCA DAC.

Square waves to the REF/DAC Analog PCA are isolated for the following reasons: to prevent noise in the digital circuits from entering the analog circuits of the DAC and to provide a voltage level transition for the FET switch drive signal on the REF/DAC Analog PCA.



A retriggerable one-shot (U32) is triggered by the 2 MHz clock from Q1. When the 2 MHz clock stops, the one-shot times out and resets the outputs of U19 to zero. This causes the output of the REF/DAC Analog PCA DAC to be zero.

The REF/DAC Digital PCA provides one other isolated signal to the REF/DAC Analog PCA. This signal (Z) enables or disables the offset circuit on the REF/DAC Analog PCA. Data line GD7 is fed to the D input of U22, clocked by the output of U9. This gate ANDs the \*WR signal and an output of the address decoder (U5-14). The output of U22 is buffered by U25, then drives the photocoupler U39. The output of U39 drives Q3, whose output is then sent to the REF/DAC Analog PCA.

The revision level of the REF/DAC Digital PCA can be determined by reading the tri-state buffer, U1. The inputs to this buffer are configured (by tying inputs to LCOM or + 5LH) to represent the pca's revision level. The buffer U1 is enabled (read) when the guarded read line \*RD and the appropriate address (from address decoder U5) is sent to AND gate U9.

The a/d converter is a 12-bit (plus sign bit and overrange bit) binary a/d converter with an input voltage range of  $\pm 1.1$ V. The IN LOW input is connected to the low-noise common, RCOM. The IN HI input is connected to the output of multiplexer U40. The components R63, R46, VR1, VR2, Q4, and Q5 form an input protection circuit for the a/d converter. The multiplexer U40 is used to connect the input of the a/d converter to the ANALOG DATA OUT signal or to one of several voltage monitoring points on the REF/DAC Digital PCA. Two of the monitoring points are at the output of reference IC, U24. This IC supplies a precise voltage of 2.5V which is divided to .973V by R52, R53, R58, R59, and R62. This voltage is used to calibrate the a/d converter at the beginning of internal calibration and the analog self-test.

The digital inputs to U40 come from latch U42. The latch is clocked by the \*WR signal and the \*SELF signal (decoded from the address bus) after those two signals are ANDed by U41. The latch U42 is cleared by the \*POP signal.

The operating voltages for the a/d converter are referenced to the  $\pm 5$ VL source, which is filtered by U38, R37, R38, C40, and C41. The extra filtering is required to provide a noise-free voltage supply for the a/d converter.

The a/d converter takes a reading when requested to do so by the main microprocessor. The main microprocessor monitors the status of the a/d converter for the completion of the reading. The main microprocessor then reads the binary output of the a/d converter via the guard crossing.

To start a reading, pin 26 (RUN/HOLD) of the a/d converter must be set high. This is done by flip-flop U31. The \*WR and \*TRIGGER (one of the address lines) signals are ANDed by U41, which is used to drive the preset input of U31. When the output of U41 goes high, the Q output of U31 is set high. When the a/d converter completes a reading, it sets the Status Line (pin 2) low. This low on pin 2 is inverted by U23 at pin 6 and then proceeds to the clock input of U31 (pin 3). This causes U31 to reset (Q output goes low), and the RUN/HOLD input of the a/d converter goes low. The low input to the RUN/HOLD line causes the present a/d converter reading to be held until it can be read by the main microprocessor.

The STATUS line also goes to a tri-state buffer (U8), whose output (at pin 11) goes to GD6. The tri-state buffer is enabled by \*RD and \*TRIGGER, ANDed by U9 (\*TRIGGER is from the address decoder U5). This is how the main microprocessor reads the status of the a/d converter to determine when a reading has been completed. A completed reading is read out in two bytes, a low byte and a high byte. The status of address line A0 determines which byte is read out. Address line A0 is connected, via tri-state buffer U21, to the a/d converter inputs \*LBEN (Low Byte Enable) and \*HBEN (High Byte Enable). The tri-state buffer (U21) is enabled by the \*A/D signal from the address decoder U5. \*A/D is low when data is being read from the a/d converter. Data from the a/d converter is placed on the data bus by tri-state buffers U14 and U21. The tri-state buffers are enabled by \*RD and \*A/D, which is ANDed by U9. The output of U9 also sets the \*CE (Chip Enable) on the a/d low. When the A0 line is low, the low byte output is enabled (outputs B1 through B8 are active). When the A0 line is high, the high byte is enabled (outputs B9 through B12, POL and OR are active. POL is the sign bit, and OR is the overrange bit.

Refer to Table 2-8 for a description of the A/D Digital Inputs.

#### REF/DAC ANALOG PCA, A9

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The REF/DAC Analog PCA contains a pulse-width modulated DAC circuit and a stable, 13V low-noise reference circuit. The control logic for the DAC circuit is contained on the REF/DAC Digital PCA. The reference circuit and critical components of the DAC circuit are enclosed in a temperature-controlled oven.

Data lines GD0 through GD5 are buffered by U23, and data lines GD6 and GD7 are buffered by U24. Only data lines GD0 through GD3 are used on this pca. The buffered data lines GD0 through GD3 are sent to latches U21 and U25 where they are clocked through by \*GWR (guarded write) ANDed with the decoded address lines (\*DAMS and \*DRLS) from the REF/DAC Digital PCA. The latches are cleared by the \*GPOP (guarded power on preset) line. The outputs of U21 are sent to multiplexer U20 as the binary control inputs (and one inhibit input). The control inputs select one of the eight multiplexer inputs to be connected to the output of the multiplexer (ANALOG DATA OUT). By using the multiplexer, via the ANALOG DATA OUT line, the main microprocessor can monitor eight voltage test points on the REF/DAC Analog PCA. The single output from U25 controls relays K1 and K2. These relays switch the polarity of the 13V reference voltage.

The oven control circuitry is identical to the one described for the Preamp PCA.

DIGITAL INPUT	DESCRIPTION	NOTES
LBEN	lower bit enable	(b1- b8)
HBEN	higher bit enable	(b9 - b12, POL, OR)
RUN/HOLD	measurement being taken/measurement not being taken	
STATUS	ready for controller to look at data or take another reading.	

Table 2-8. A/D Digital Input	Table	2-8.	A/D	Digital	Inputs
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The 13V reference circuit consists of two cascaded 6.5V reference amplifiers (U3 and U6) and their associated components. The 6.5V output of the first reference amplifier (U3) is buffered by U4 and drives the load of R24. The 6.5V output of the second reference amplifier (U6) is in series with R24 to provide a total of 13V at the input to U5. The output of buffer U5 drives an emitter follower (Q4) that provides the reference output (REF OUT HI). U5, Q2, and Q4 form a wide dynamic range buffer with very low output impedance. This prevents noise spikes, caused by the rapid load changes of the DAC circuit, from appearing on the reference supply. The 13V reference supply is used as a reference voltage for a voltage regulator consisting of U2 and Q1, which provides the 19.8V collector supply of U6.

The reference supply is connected to the DAC circuit by relays K1 and K2. These relays allow the polarity of the reference voltage to be reversed. When de-energized, the relays connect the REF OUT LO line to RCOM (TP19) and the REF OUT HI line to VREF (TP18). When energized, the relays connect the REF OUT HI line to RCOM (TP19) and REF OUT LO to VREF (TP18).

The pulse-width modulated DAC circuit has two switching circuits. The first switching circuit provides output resolution in 0.55 mV steps. The second switching circuit provides output resolution in 75 nV steps. Therefore, the output of the DAC circuit can be set from 0.0V to  $\pm 11$ V, in 75 nV steps.

The first switching circuit consists of FETs 09, 010, and 012. The FET pair, 09 and 010. are in series with the reference voltage while Q12 shunts it. When Q9 and Q10 are conducting and Q12 is off, the reference voltage is connected to R69. When Q12 is conducting and Q9 and Q10 are off, the output of the switching circuit is 0V. FETs Q9 and Q10 are turned on and off by Q13, whose drive signal is FQ1 (from the REF/DAC Digital PCA). When Q13 is turned off, Q9 and Q10 are turned on by the 13V applied to their gates. The supply voltage for Q13 is provided by the buffer amplifier setup of U8 and Q7. When Q13 turns on, the gates of Q9 and Q10 go to V1(FH), which turns the FETs off. The signal V1(FH) and V1(FC) are the high and common of a floating 5V power supply from + 5DAC and DAC COM (P51-29 and P51-30). With the reference set for positive polarity, V1(FH) is connected to the -17V supply via K2, CR5, and VR13 (a 5.1V zener). This makes the voltage at V1(FH) about = 11.3V, relative to A COM (and RCOM). With the reference set for negative polarity, V1(FH) is connected to -24V via K2 and CR14. This makes the voltage at V1(FH) about -23.3V, relative to ACOM. This negative voltage on the FET gates turns them off. Also, when Q13 is on, it draws current from Q7 through four current-regulating diodes (CR8, CR9, CR21, and CR22). When O13 turns off, these diodes charge stray capacitance to bring the FET gate voltage up to 13.2V. The shunt FET Q12 is turned off and on the same way as Q9 and Q10. The switching signal comes from FQ1 via U28, Q32, and Q14. The gate of Q12 is switched between RCOM and V1(FH).

The operation of the second switching circuit is similar to the first switching circuit. The reference voltage is first divided down by R49 and R50 to 1.72V. This voltage is buffered by U9, whose output goes to FET Q16, which is in series with the voltage. The gate of Q16 is driven between 1.72V (FET on) and V2(FC) (FET off) by Q20. V2(FC) is at -5V, referenced to ACOM. The drive for Q20 is SQ from the REF/DAC Digital PCA. The shunt FET is Q17, and its gate is switched between ACOM and V2(FC) (FET off) by Q21 driven by \*SQ. The output of this circuit is divided down by R47 and R44 to 4.5 mV.

The DAC circuit must be linear down to a 0V output. The first switching circuit output is linear down to a duty-cycle of 0.04% (10 counts). This produces an output of approximately 5.5 mV. To obtain a linear DAC circuit output of 0V, an offset circuit, with a constant output of -5.5 mV, is summed with the output of the two switching circuits. The result of the sum

is 0V at the output of the DAC circuit. Therefore, the offset circuit allows the DAC circuit output to be zero even though the count remains above 10. (Refer to the Detailed Theory of Operation for the REF/DAC Digital PCA for an explanation of the counts.) The input of the offset circuit (inverting amplifier U7 and associated components) is the 13V reference voltage via FET switch Q18. The gain of U7 is negative 0.2 producing an output of -2.64V. This voltage is reduced to -26.4 mV by divider network R37/R38. The level is reduced by R39 to -5.5 mV.

The outputs of the two switching circuits and the offset circuit are summed together at the junction of R69, R48, and R39. The junction of these resistors is the summing junction for the amplifier/filter combination, which extracts the dc component from the square wave. The amplifier/filter combination starts with differential pair U16. The current source for U16 is Q24. The differential pair in U16 is the first stage for the differential pair in U15. The bias level for U15 is set by Q23 and CR15. Overvoltage protection is provided by Q25 and Q26. The differential output of U15 is used to drive U12. The bias level for U12 is established by R84 and R85. Q25, Q26, Q27, and Q28 protect against amplifier latch-up from transients. The output of U12 drives the plus (+) input of U11. The minus (-) input to U11 is connected to the summing junction via C37. This couples high frequency signals directly to U11. The output of U11 (pin 6) is connected back to the summing junction via C36. This makes the amplifier an integrator for the pulse-width modulated square-wave input signal. The output at U11-6 drives a 5-pole active filter (U10 and associated components). The output of this filter is a pure dc voltage that is then buffered by U14. The output of U14 provides the DAC circuit output that is sent to the Sample String PCA.

The overall gain (negative one) of the amplifier/filter is determined by R69 and R73. Since the on resistance of FETs Q9 and Q10 is in series with R69, their resistance can affect the gain of the amplifier/filter. To null the effect that Q9 and Q10 have on the overall gain, two identical FETs (Q29 and Q30) are placed in series with R73 to balance out the resistances.

Figure 2-9 is a simplified diagram showing how the analog circuits are configured during internal calibration. The following is done to REF/DAC Analog PCA to configure the analog circuits during internal calibration:

- 1. The offset circuit is disabled by turning off Q18 with the Z signal from the REF/DAC Digital PCA.
- 2. The first switching circuit remains on by setting its duty cycle to 100% with the FQ1 signal from the REF/DAC Digital PCA.
- 3. The second switching circuit remains turned off by setting its duty cycle to 0%. This is done with the SQ and \*SQ signals from the REF/DAC Digital PCA.

These changes place the 13V reference voltage at the input of the amplifier/filter. Since the gain of the amplifier/filter is -1, its output is the reference voltage with its polarity reversed.

# SOFTWARE FUNCTIONAL OVERVIEW

As Figure 2-10 shows, the 5440B/5442A software is conceptually organized into two major parts with the machine state between. The first part controls the internal instrument interfaces (interfaces between the software and the control circuits). The second part controls the local and remote external interfaces. The machine state is an internal representation of how the analog hardware is to be configured (output voltage, range, mode, etc.).





Figure 2-10. 5440A Software Process Diagram

Figure 2-10 also shows the five 5440B/5442A software processes:

- Local interface
- Remote interface
- Command processor
- Analog control
- Printer and nonvolatile memory control

Each of the functions runs independently, as if they were running on separate microprocessors. The functional separation of software is different from the physical separation. Physically, most of the local interface software resides in the front panel microprocessor, and the remaining interface software resides in the main microprocessor.

The two user interfaces, remote and local, translate the specific interface commands into the very simple commands expected by the command processor. The command processor executes all user commands.

For example, the user interface and command processor functions in the following manner when a new output voltage is entered from the front panel. First, the local interface software interacts with the operator by displaying the keys pressed and prompting for additional input. When the operator enters the selected output by pressing the ENTER/YES (DATA ENTRY) key, the local interface software sends a message to the command processor requesting that the output change. The command processor then checks the new output against the programmed limits. If the new output is within limits, it is written in the machine state data area. The command processor tells the analog control and the local interface to change the output value. The local interface software updates the output displays. The analog control software makes the appropriate changes to the analog hardware.

Since the 5440B/5442A software processes are independently executing pieces of software, they have three unique properties.

- Each of the processes runs at its own speed. As a result, the analog control process can take as much time as is necessary to set up the analog hardware without holding up the operator interface.
- The command processor has the ability to abort long operations. For example, the internal calibration is executed by the analog control process and can take up to six minutes to complete. When the operator aborts an internal calibration by pressing the RESET key, the command processor signals the analog control to stop executing the internal calibration.
- Multiple activities can be carried on simultaneously by the software. For example, the
  printer and nonvolatile memory control process is used to print listings and to store or
  recall EEPROM data. The analog control of the instrument can still proceed (including
  monitoring analog circuits for faults) while simultaneously printing or writing to
  nonvolatile memory.

# External and Internal Calibration

External calibration should be performed every 30 days to maintain the specifications given in Section 1 of this manual. The External Calibration procedure uses external calibration equipment to calibrate the instrument. The Internal Calibration procedure should be performed every day and does not use external calibration equipment. The Internal Calibration procedure compensates for circuit drift in the 5440B/5442A. A theoretical description of the External and Internal Calibration procedures is contained in Appendix A of this manual. The following discussion contains additional information on the External and Internal Calibration procedures.

The Internal Calibration procedure is a user-initiated automated procedure. The software required to perform this procedure is contained in the main microprocessor memory of the instrument. The Internal Calibration procedure first calibrates the internal a/d converter, located on the REF/DAC Digital PCA. A 2.5V reference on the REF/DAC Digital PCA is divided down to 0.973V. This voltage is sent to the a/d converter and a reading is taken. The output of the a/d converter is a binary number that is divided into 0.973. This provides a calibration constant that is the resolution of the a/d converter, expressed as mV per binary number. When the calibration constants are listed on a printer after the Internal Calibration procedure is completed, the constant is called A/D Gain (see Figure 2-11).

CONSTANT	10V RANGE	20V RANGE	250V RANGE	1000V RANGE
Gain	+.54313609 mV	+1.0862640 mV	+13.577998 mV	+54.311978 mV
2V Gain		+1.0862762 mV		
.2V Gain		+1.0862863 mV		
+Offset	+4.8645389 mV	+9.7681830 mV	+122.47198 mV	+490.39426 mV
~Offset	+5.5948529 mV	+11 149847 mV	+139.00318 mV	+555.53586 mV
Gain Shift	,Û PPM	- <b>()</b> PPN	~.() PPM	Ü PP@

Figure 2-11. Calibration Constants, Sample Listing

The next step is to zero the output of the instrument on the +10V range. The main microprocessor sets the output of the instrument to 0V using the calibration constants contained in memory. If the instrument has never been calibrated, then default constants are used. The a/d converter is then connected to the output of the Zero Amplifier on the Output PCA, and two readings are taken. The first reading is taken with the input of the Zero Amplifier shorted. The second reading is taken with the input of the Zero Amplifier connected to the output of the 5440B/5442A. The difference between the two readings is proportional to the difference between the programmed output (0V) and the actual output voltage of the 5440B/5442A. This offset is converted to microvolts by the Internal Calibration program.

The Internal Calibration procedure will provide a printout, like the one shown in Figure 2-12, as the procedure is executed. The printout indicates the step being executed (e.g.,  $\pm 10V$  ZERO), then gives the values for N1 and N2 (N1 and N2 are the counts for the first and second switching circuits in the REF/DAC Analog PCA DAC). The first set of N1 and N2 values are determined from the calibration constants in memory The next value listed on the printout is the offset. If the offset is too large, the program calculates a new set of values for N1 and N2 which should bring the output within limits.

The DAC (on the REF/DAC Analog PCA) is set with the new values for N1 and N2, then two more readings are taken with the a/d converter. As the two new readings are made, the printout shows the two new values for N1, N2, and the new offset. If the offset is still out of limits, the Internal Calibration program will try again with the new values of N1 and N2. If the original offset was small, only one additional correction may be required to zero the output of the 5440B/5442A. A large offset may require several corrections.

After zeroing the +10V range, the constant called resolution ratio (RR) is determined. The final value of N1 from the +10V ZERO step is decreased by one count. The final value of N2 from the +10V ZERO step is increased by the value of RR in memory. Two readings are taken, and the offset is determined. If the offset is out of limits, the N2 count is changed until it is within limits. The change in the N2 count from this step is the new value for RR. If the calibration constants are listed after internal calibration, this value is shown under the heading Resolution Ratio.

```
5440A INTERNAL CALIBRATION
JOHN FLUKE MEG. CO., INC.
+10V ZERO
           2, N2=14250, Offset
                                -1.2uV
    i: Ni=
    2: N1= 7, N2=14266, Offset
                                --.3uV
RESOLUTION RATIO
    1: N1= 6, N2=21558, Offset
                               -.iuV
-10V ZERO
    1: N1=
           9, N2= 9500, Offset
                                -1.0uV
            9, N2= 9487, Offset
    2: N1=
                                 ∼.2uV
+20V ZERO
           7, N2=14529, Offset
                                +1.5uV
    1: NJ=
-20V ZERO
    1: N1=
            9, N2= 9220, Offset
                                -1.ÚuV
+250V ZERO
            7, N2=14729, Offset
                                -9.1uV
    1: N1=
~250V ZER0
            9, N2= 9023, Offset
                               -12.1uV
    1; N1=
+1000V ZERO
            2, N2=14797, Offset --71,8uV
    1: N1=
~1000V ZERO
            9, N2= 8959, Offset -76.74V
     1; N1=
GAIN SHIFT
     +10: +376.24uV
     +20:
         +442.87uV
     a Mit: +451.03aU
     -Hit
         -838.11uV
     -20:
          -830.32vV
         -764.04uV
    -10:
END OF INTERNAL CALIBRATION
```

Figure 2-12. Internal Calibration Monitor, Sample Listing

The Internal Calibration procedure continues, zeroing the other ranges with a similar procedure. The only variation is on the high voltage ranges if the offset is large. A large offset will cause the a/d converter to overrange and therefore, no offset can be calculated or printed out. When this occurs, the gain of the Zero Amplifier is changed from 1000 to 100, and a new reading is taken. The offset can now be calculated and printed out. When the zeroing procedure brings the offset low enough, the gain of the Zero Amplifier is changed back to 1000, and the procedure continues.

After performing the output zeroing procedure, the Internal Calibration program performs gain shift measurements. The program sets up the internal circuitry of the 5440B/5442A into a special configuration. (See Figure 2-9 for a simplified diagram.) The discussion in Appendix A, describes the difference in this configuration for the three sets of measurements that are taken. If a printer is connected while the Internal Calibration procedure is being performed, the heading, Gain Shift is printed, then six readings are printed out labeled +10, +20, +HV, -HV, -20, and -10. Referring to the equations in Appendix A, the value of +10 is

(V1)new in equation 13, and the value -10 is (V2)new. In equation 14, the +20 value is (V1)new and the -20 value is (V2)new. In equations 15 and 16, the + HV value is (V1)new, and the - HV value is (V2)new.

After the Internal Calibration procedure has finished, the calibration constants can be read on the Alphanumeric Display of the 5440B/5442A front panel and on a printer or video display terminal via the IEEE-488 or RS-232 interface ports. Figure 2-11 illustrates an example of a calibration constant printout obtained by using a printer connected to the RS-232 interface port. The gain constants are listed first, followed by the offset values. The line labeled Gain Shift gives the gain shift in ppm from the last Internal or External Calibration procedure.

The shift in offset values is not listed, but if the values from the previous calibration have been recorded, the shifts can be calculated by taking the difference of the current and previous values for each range and polarity.

All the values shown in Figure 2-11 can also be read out through the Alphanumeric Display. When this is done, the constants are read out one at a time in the same order as they appear in Figure 2-11 (reading left to right, top to bottom). So the first constant read is the 10V range gain constant and the last read is the A/D Gain.

Internal calibration cannot correct for all the drifts in the 5440B/5442A (like the 13V reference drift), so the External Calibration procedure must be performed periodically. Doing this accurately sets the gain constants. After performing the External Calibration procedure, the new constants can be read out as already described.





Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

- 1. Knowing that there is a problem.
- 2. Learning the guidelines for handling them.
- 3. Using the procedures, and packaging and bench techniques that are recommended.

The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol " 🚫 "

The following practices should be followed to minimize damage to S.S. devices.



1. MINIMIZE HANDLING



2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES. USE A HIGH RESIS-TANCE GROUNDING WRIST STRAP.



4. HANDLE S.S. DEVICES BY THE BODY



5. USE STATIC SHIELDING CONTAINERS FOR HANDLING AND TRANSPORT



6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA

> PORTIONS REPRINTED WITH PERMISSION FROM TEKTRONIX, INC. AND GENERAL DYNAMICS, POMONA DIV.



8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR HELPS TO PROTECT INSTALLED SS DEVICES.



- 9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
- 10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.
- 11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

A complete line of static shielding bags and accessories is available from Fluke Parts Department, Telephone 800-526-4731 or write to:

JOHN FLUKE MFG. CO., INC. PARTS DEPT. M/S 86 9028 EVERGREEN WAY EVERETT, WA 98204



J0089D-07U8604/SE EN Litho in U.S.A. Rev. 1 MAR 86

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# Section 3 Maintenance and Calibration Information

#### WARNING

# THESE SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRICAL SHOCK, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN THE OPERATION INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

#### INTRODUCTION

The information in this section contains maintenance and calibration information for the 5440B/5442A. The information is divided into general maintenance, calibration checks and adjustments, acceptance test procedures, an internal calibration procedure, and an external calibration procedure. To verify proper operation of the instrument, the Acceptance Test should be performed upon receipt of the 5440B/5442A or at any other time.

### **REQUIRED TEST EQUIPMENT**

Table 3-1 lists the test equipment necessary to complete the tests and procedures in this section. If the recommended test equipment is not available, test equipment with equivalent specifications or better can be substituted.

#### LOCATION OF MAJOR MODULES

Figure 3-1 shows the location of all major modules in the 5440B/5442A. The view shown is from the top of the instrument.

# ACCESS PROCEDURES

The following paragraphs contain procedures that provide access to the interior of the 5440B/5442A and removal instructions for two pca's.

#### Interior Access Procedure

#### CAUTION

## To prevent shipping damage to the pca's, always place the plastic pca retainers in the original configuration when reassembling the 5440B, 5442A.

This procedure describes how to gain access to the interior of the instrument. There are two outer and two inner covers on the 5440B/5442A. The two outer covers are top and bottom pairs. One inner cover shields the guarded pca's and the other shields the digital pca's. Complete the following procedure to gain access to the interior of the 5440B/5442A:

# 3-2

3-1

# 3-3

3-4

# Table 3-1. List of Required Test Equipment

Voltage Reference Standard	10V dc, 1.5 ppm absolute uncertainty	Fluke 732A
oltage Divider 0.2 ppm ratio uncertainty at 10:1 @ up to 100V input andard 0.5 ppm ratio uncertainty at 100:1 @ 1kV input		Fluke 752A
DMM	Fluke 8505A* or 8502A* Fluke 8520A w/-010 or Fluke 8522A	
Null Detector	1 $\mu$ V range $\pm$ 3% end-scale absolute uncertainty > 10 <sup>12</sup> $\Omega$ leakage to cas	Fluke 845AR or 845AB
Metered Output 0 to 130V ac at 3A Auto-Transformer		General Radio Variac
Low-Thermal EMF Shielded Cables		Fluke 5440A-7002 or 5440A-7003
Load Resistors 100 ohms ±1%, ½W, 1kΩ, ±1% 1W		
Oscilloscope 0.1V Vertical Sensitivity 100 kHz Bandwidth		TEK 7603
Differential Amplifier		
True RMS Voltmeter	100 mV range	Fluke 931B
*Calibrated to the 90 d	ay specifications.	

- 1. Remove the line cord from the instrument.
- 2. Remove the screws holding the top and bottom covers in place. (Three screws are located along the front edge and five screws are located along the back edge.)
- 3. Lift the covers off the instrument.
- 4. Remove the screws (four each) from the sides of the inner covers, and remove the inner covers. The interior of the 5440B/5442A is now accessible.

To reassemble the 5440B/5442A, logically reverse the four steps above.

# Guarded Xfmr Term PCA Access Procedure, A11

Complete the following procedure to gain access to or remove the Guarded Xfmr Term PCA:

- 1. Use the procedure in paragraph 3-5 to gain access to the interior of the 5440B/5442A.
- 2. Remove the four screws located along the sides of the Guarded Xfmr Term PCA.
- 3. Using the handle provided, carefully lift the Guarded Xfmr Term PCA from the 5440B/5442A.

To reassemble, logically reverse the three steps of this procedure.





Figure 3-1. 5440B Module Locations

# **Outside Guard Term PCA Access Procedure, A19**

Complete the following procedure to gain access to or remove the Outside Guard Term PCA:

- 1. Use the procedure in paragraph 3-5 to gain access to the interior of the 5440B/5442A.
- 2. Remove the six screws located along the rear of the Outside Guard Term PCA.
- 3. Carefully remove the Outside Guard Term PCA from the 5440B/5442A. If the transformer on the pca will not clear the fan on the rear panel, remove the fan. To remove the fan, disconnect the power plug from the fan and remove the two 1/4-inch nuts that hold the fan in place. Lift the fan from the 5440B/5442A.

To reassemble, logically reverse the three steps of this procedure.

# Front Panel Access Procedure

3-8

Complete the following procedure to gain access to the Front Panel PCA for troubleshooting or repair:

- 1. Remove the top cover and place the instrument on its rear handles, with the bottom facing you.
- 2. Remove the bottom cover, and place the instrument in its normal position.
- 3. Remove the Procedure Storage Module.
- 4. Remove the four screws from each side at the rear of the front handles (do not remove the handle decals).
- 5. Pull the front panel forward. If you wish, you can leave the front panel connected to the instrument via the Interconnect (ribbon) Cable.

# **Changing Output Terminals from Front to Rear**

3-9

# NOTE

A 5442A Calibrator must be equipped with a 5442A-01 option to obtain rear output.

The 5440B/5442A is shipped from the factory with its output (from the Output PCA) connected to terminals on the front panel. The terminals located on the rear panel of the instrument are not connected. Use the following procedure to connect the 5440B/5442A output to the rear panel terminals:

- 1. Use the procedure in paragraph 3-5 to gain access to the interior of the 5440B/5442A.
- 2. Using the card extractors, remove the Output PCA from the motherboard connector and the card cage.
- 3. Insert the Output PCA into the adjacent card slot (labeled REAR OUTPUT) towards the rear. Press the pca firmly into the motherboard connector.
- 4. Reattach the covers of the instrument.

# GENERAL MAINTENANCE INFORMATION

The following paragraphs describe general maintenance procedures. The Air Filter Maintenance procedure should be performed periodically under a routine maintenance program. The Cleaning Modules procedure should only be performed when the modules look dirty.

the second second second

#### **Cleaning Modules**

#### CAUTION

Instantaneous or delayed electrostatic discharge damage can be caused by improper handling of the modules and by the use of a vacuum cleaner with static-inducing brushes. To prevent damage by electrostatic discharge, observe the precautions described on the Static Awareness sheet located in front of this section. Remove all modules from the 5440B/5442A before using a vacuum cleaner on the chassis. Do not use the vacuum cleaner on the modules.

If a visual inspection of the instrument shows excessive dirt buildup, clean the appropriate portions of the instrument. After all the modules have been removed, use a vacuum cleaner or low pressure air to clean the 5440B/5442A chassis.

Use low pressure air to clean dust from the modules. If conditions warrant, clean the modules with water-based commercial cleaning systems such as dishwashers. When cleaning the modules with water, observe the following precautionary procedure:

- 1. Remove all plug-in relays and oven covers from the pca's and separate all piggy-back assemblies.
- 2. In geographic areas with exceptionally hard water, use Reagent Grade 2 water (deionized or distilled water), or better, for cleaning the Sample String PCA and for the final rinse of the pca's. To remove all ions, spray or run the water during the final rinse so that the pca surface is thoroughly covered.
- 3. Thoroughly dry all modules using one of the following methods. Method a is preferred.
  - a. Dry the modules in a low-temperature drying chamber or an infrared drying rack with a temperature range of 49 to 72°C (120 to 160°F).
  - b. If neither a drying chamber nor a drying rack is available, air-dry the modules at ambient room temperatures for at least two days.

#### NOTE

A satisfactory cleaning method consists of holding the pca's under running hot water until they are clean. Rinse and dry the pca's according to the above procedures.

#### **Cleaning Edge Connectors**

#### CAUTION

Never use an eraser to clean edge connectors. Use of an eraser to clean module edge connectors can cause static discharge damage on the modules and abrade the surface plating. 3-12

#### 3-10

If visual inspection shows that the module edge connectors need cleaning, use a mixture of 70% isopropyl alcohol and 30% water on a clean, lint-free cloth.

# Air Filter Maintenance

3-13

3-14

## CAUTION

# If the filter is cleaned with water, make sure that it is thoroughly dry before reinstalling it.

Visually inspect the air filter at the rear of the fan compartment periodically for dirt and contaminants. Clean the filter, when necessary, using the following procedure:

- 1. Disconnect the line power cord from the instrument.
- 2. Remove the four screws that hold the filter frame in place, then remove the filter frame and the filter.
- 3. Clean the filter using either clean dry air or a mild solution of detergent and water.
- 4. Thoroughly dry the filter if it was cleaned with water.
- 5. Reinstall the filter and filter frame.

#### Line Voltage Selection

The 5440B/5442A can operate from any of the eight line voltages listed in Table 3-2 at line frequencies from 50 to 60 Hz. The instrument should arrive configured for the line power specified at the time of purchase. The factory configuration is marked on the rear panel decal.

Use the following procedure to select a line voltage configuration:

- 1. Determine the line voltage range from the eight ranges listed in Table 3-2. Be sure to select a range that includes the expected fluctuations.
- 2. Set the line voltage select switches, shown in Figure 3-2, to the positions listed for that range in Table 3-2.
- 3. Verify that the proper line fuse is installed. Refer to Table 3-2 for the correct line fuse values.

LINE VOLTAGE RANGE (VAC)			LINE VOLTAGE RANGE (VAC) LINE VOLTAGE SELECTION SWITCH POSITIONS*			
NOMINAL	MINAL TOLERANCE					FUSE VALUE
	-10%	+10%	S1	S2	S3	TALUL
100	90	110	Up	Up	Down	
110	99	121	Up	Up	Up	MDX 2A
115	103.5	126.5	Up	Down	Down	
120	108	132	Up	Down	Up	
200	180	220	Down	Up	Down	
220	198	242	Down	Ųр	Up	MDX 1A
230	207	253	Down	Down	Down	
240	216	264	Down	Down	Up	

Table 3-2.	5440A	Line	Power	Voltage	Selection





Figure 3-2. Line Voltage Select Switches

#### **Fuse Replacement Procedures**

In addition to the line power fuse, the 5440B/5442A has 36 other fuses, located on four internal pca's. These fuses protect the transformer secondary and some regulator circuits. See Table 2-2 in the 5440B Operator's Manual for information about replacing the line power fuse.

Use the following procedure to replace circuit protection fuses:

- 1. Use the Access Procedure to remove the appropriate pca from the 5440B/5442A.
- 2. Locate and replace the defective fuse(s). Table 3-3 gives the correct value and location of the circuit protection fuses.
- 3. If the fuse fails a second time, troubleshooting and/or repair is indicated.

# CALIBRATION ADJUSTMENTS

Because of its internal and external calibration functions, the 5440B/5442A does not require periodic adjustments. The following calibration checks and adjustment procedures are required only in the event of malfunction on the listed assembly.

3-16

PCB LOCATION	FUSE REFERENCE DESIGNATION	REPLACE WITH FUSE TYPE:	CIRCUIT PROTECTED
A10 Inside Regulator PCB	F1 F2	4A, 125V	+5V DAC +5V LH
	F2	10A, 125V	20V AC Oven
A11 Guarded Xfmr Term PCB	F3 F4 F5 F6 F7 F8 F9 F10 F11 F12	10A, 125V Pico Fuse	TS5 TS4 TS3 TS2 TS1 TS1 TS2 TS3 TS4 TS5
	F13 F14	2A, 125V Pico Fuse	±17S AC
	F15 F16	1A, 125V Pico Fuse	30 FR AC 15 FR AC
	F17 F18	3A, 125V Pico Fuse	HRG AC HRG AC
	F19 F20	1A, 125V Pico Fuse	OP AC OP AC
	F23 F24	5A, 125V SLO-BLO	LH AC LH AC
	F25 F26	1.5A, 125V Pico Fuse	DAC AC DAC AC
	F27 F28	1A, 125V Pico Fuse	HVS HVS
A17 Outside Guard Regulator PCB	F1	4A, 125V	+5V Regulator
A18 I/O Assembly	F1	1/4A, 250V	+5V Supply
	F1	2A, 125V Pico Fuse	Unregulated +29V DC Supply
A19 Outside Guard Term PCB	F2 F3	5A, 125V SLO BLO	Unregulated +5V DC Supply OG POP GEN and Unregulated +5V DC Supply
	F4	2A, 125V Pico Fuse	Unregulated +29V DC Supply
	F5 F6	3A, 125V Pico Fuse	Unregulated HR +5V Unregulated HR +5V

# Table 3-3. Circuit Protection Fuses

3-17

# **Outside Guard Power Supply**

Use the following procedure to check and adjust the power supply on the Outside Guard Regulator PCA:

- 1. Connect the DMM common to TP1 on the Outside Guard Regulator PCA.
- 2. Set the DMM to measure dc volts.
- 3. For each step in Table 3-4, set the DMM to an appropriate range, connect the positive lead to the indicated test point, and verify or adjust the indicated potentiometer for the specified voltage.

Table 3-4.	Outside	Guard	Power	Supply	Checks	and Adjusta	nents

STEP	TEST POINT	ADJ. POINT	SPECIFIED VOLTAGE
1	TP2	R22	+5.15, ± 0.00V dc
2	TP3	n/a	+5.00, ± 0.25∨ dc
3	TP4	R18	$\pm 28.0, \pm 0.00 V dc$
4	TP5	n/a	+12.0, ± 0.60V dc
5	TP6	n/a	-12.0, $\pm$ 0.60V dc
6	TP8	n/a	-5.00, $\pm$ 0.25V dc
7	TP7	n/a	-29V dc
7	197	n/a	-297 86

# Inside Guard Power Supply

3-18

Use the following procedure to check and adjust the power supply on the Inside Guard Regulator PCA:

- 1. Set the DMM to measure dc volts.
- 2. For each step in Table 3-5:

Table 3-5. Inside	<b>Guard Power</b>	Supply Checks	and Adjustments

STEP	TEST POINT COMMON LEAD	TEST POINT POSITIVE LEAD	ADJ. POINT	SPECIFIED VOLTAGE
1	TP1	TP2	n/a	+17.0, ±1.00V dc
2	TP1	TP3	n/a	-17.0, $\pm$ 1.00V dc
3	TP1	TP4	R95	+5.00, ±0.25V dc
4	TP1	TP5	n/a	-5.00, ±0.25∨ dc
5	TP1	TP6	n/a	-24.0, ±1.30V dc
6	TP1	TP10	n/a	+5.00, ±0.25V dc
7	TP7	TP8	n/a	+30.0, ±1.50V dc
8	TP7	TP9	n/a	-30.0, ±1.50V dc
9	TP11	TP12	n/a	+30.0, ±1.50V dc
10	TP11	TP13	n/a	-15.0, ±0.80V dc
11	TP14	TP15	n/a	+5.00, ±0.25V dc
12	TP16	TP17	n/a	+15.0, ±0.80V dc
13	TP16	TP18	n/a	-15.0, ±0.80V dc

- a. Set the DMM to an appropriate range.
- b. Connect the leads of the DMM to the indicated test points.
- c. Verify or adjust the indicated potentiometer for the specified voltage.

# **Square Wave Generator**

The square-wave generator duty cycle adjustment is located on the Output/HV Control PCA. The test point for this adjustment is located on the Output PCA.

Use the following procedure to adjust the duty cycle of the square wave generator:

1. Set the oscilloscope to:

ac coupling 200 mV/div vertical deflection 200  $\mu$ s/div horizontal deflection

- 2. Connect the oscilloscope common to the front panel terminal, OUTPUT LOW.
- 3. Connect the oscilloscope probe to TP2 on the Output PCA.
- 4. Program the 5440B/5442A for a 1100V output.
- 5. Adjust R3 on the Output/HV Control PCA to the minimum ac signal on the oscilloscope.

# ACCEPTANCE TEST PROCEDURE

The Acceptance Test Procedure should be used for incoming inspection and routine performance checks. The Acceptance Test may be conducted before performing an External Calibration.

The Acceptance Test Procedure is divided into sequentially arranged subtests that verify different aspects of the 5440B/5442A performance. Perform the tests in the sequence shown The necessary test equipment is listed in Table 3-1. Allow the instrument to warm up for a minimum of two hours before starting the procedure.

# Self-Tests

Complete the following procedure to have the 5440B/5442A test its digital and analog circuits:

1. Press the RESET key, then verify that the 5440B/5442A is in the power-up reset state.

In the power-up reset state, the message VOLTAGE MODE appears on the alphanumeric display, the 16-Segment Display reads +00000.00 mV, and the OUTPUT STATE indicator STBY is illuminated.

NOTE

# 3-21

3-20







2. Press the SERV key, then press the SELF TEST (soft) key, then press the DIGITAL TEST (soft) key. The following message appears on the Alphanumeric Display while the 5440B/5442A performs a test of the digital circuits.

### PERFORMING DIGITAL SELF-TEST . WAIT

3. Wait for the following message to appear on the alphanumeric display. The message indicates that the instrument has passed its digital self-test.

#### VOLTAGE MODE

4. Press the SERV key, then press the SELF TEST (soft) key, then press the ANALOG TEST (soft) key. The following message appears on the alphanumeric display:

### REMOVE OUTPUT LEADS & DO ANALOG TEST ?

- 5. Remove all connections from the front panel and the rear panel output of the 5440B/5442A.
- 6. Press the ENTER(YES) (DATA ENTRY) key. While the analog self-test is running, the following messages appear on the 16-Segment and alphanumeric displays.

22.000000V

### PERFORMING ANALOG SELF-TEST . WAIT

7. Wait for the following message to appear on the alphanumeric display. The message indicates that the 5440B/5442A has passed the analog self-test.

#### VOLTAGE MODE

#### WARNING

# TO AVOID ELECTRICAL SHOCK HAZARD, DO NOT MAKE ELECTRICAL CONTACT WITH THE OUTPUT HI OR SENSE HI TERMINAL. LETHAL VOLTAGES ARE PRESENT ON THESE TERMINALS DURING THE HIGH VOLTAGE TEST.

8. Press the SERV key, then press the SELF TEST (soft) key, then press the HIGH V TEST (soft) key. The following message appears on the alphanumeric display:

#### REMOVE OUTPUT LEADS & DO HIGH VOLT TEST?

9. Remove all connections from the front panel and the rear panel of the 5440B/5442A.
10. Press the ENTER/YES (DATA ENTRY) key. While the high voltage loop self-test is running, the following messages appear on the 16-Segment and alphanumeric displays.

 $1100.0000\mathbf{V}$ 

### DOING HIGH VOLTAGE ANALOG OUTPUT TEST

11. Wait for the following message to appear on the alphanumeric display. It indicates that the 5440B/5442A has passed the high-voltage loop self-test.

VOLTAGE MODE

# **Line Regulation Test**

3-22

The Line Regulation Test determines whether or not the 5440B/5442A output voltage remains within specified limits with line voltage changes of  $\pm 10\%$ .

Complete the following procedure, using the data in Table 3-6, to verify line regulation performance:

- 1. Set 5440B/5442A POWER off.
- 2. Connect the 5440B/5442A line power cord to ac power through the Metered Autotransformer. Adjust the Metered Autotransformer to the line voltage setting of the 5440B/5442A.
- 3. Set 5440B/5442A POWER on. Verify that the POWER and STBY indicators are turned on and that the message VOLTAGE MODE appears in the alphanumeric display.
- 4. Connect the test equipment as shown in Figure 3-3.
- 5. Program a 5440B/5442A output of 10V (using the DATA ENTRY keys).
- 6. Using the EDIT OUTPUT keys, obtain a null reading on the null meter  $\pm 0.5 \,\mu$ V.
- 7. Adjust the Metered Autotransformer to the low line voltage tolerance level of Table 3-6.
- 8. Verify that the null detector indicates less than a  $\pm 1 \mu V$  deviation.
- 9. Adjust the Metered Autotransformer to the high line voltage tolerance level of Table 3-6.
- 10. Verify that the null detector indicates less than a  $\pm 1 \mu V$  deviation.
- 11. Set 5440B/5442A POWER off. Verify that the POWER indicator turns off.
- 12. Disconnect the Metered Autotransformer from the 5440B/5442A and connect the 5440B/5442A directly to line power.
- 13. Set 5440B/5442A POWER on. Verify that the POWER indicator is on. Allow the instrument to warm up for a minimum period that is twice as long as the period it was turned off.



······································	LINE VOLTAGES	·				
	TOLERANCE (VAC)					
	LOW	HIGH				
100	90	110				
110	99	121				
115	103.5	126.5				
120	108	132				
200	180	220				
220	198	242				
230	207	253				
240	216	264				



Figure 3-3. Line Regulation Test

# **Output Voltage Test**

3-23

The following procedure tests the output performance of the 5440B/5442A. There are two stages to this test, Divider Output and DC Calibrator Output. Complete the following procedure to gain confidence in the 5440B/5442A output performance:

### NOTE

. .

Use of a 6-1/2 digit DMM in the following procedure provides a convenient check of output voltage. But a 6-1/2 digit DMM is not sufficiently accurate to verify instrument absolute uncertainty or linearity. An adequate method of verifying instrument absolute uncertainty is to step through the External Calibration Procedure using the specified test equipment, and measuring the resulting errors.

TEST FUNCTION	PROGRAMMED UUT		ANCE (V DC)
TEST FUNCTION	OUTPUT (V DC)	FROM	то
	0	-0.000001	+0.000001
Divider Output	+0.1	+.0999985	+1000015
·	+1	+0.999991	+1.000009
	0	-0.000005	+0.000005
DC Calibrator	+1	+0.999996	+1.000004
Output	+5	+4.999983	+5.000017
	+20	+19.99992	+20.00008
	-20	-19.99992	-20.00008
	+100	+99.9993	+100.0007
	+1000	+999.994	+1000.006





Figure 3-4. Output Voltage Test: DIVIDER OUTPUT

- d. For each row in the divider output test function, set the output of the 5440B/5442A to the programmed 5440B/5442A output value using the DATA ENTRY keys.
- e. Verify that the corrected DMM reading is within the output tolerance levels of Table 3-7.
- 3. Complete the following steps for each of the dc calibrator output test functions in Table 3-7:
  - a. Connect the equipment as shown in Figure 3-5.
  - b. Set the DMM for maximum resolution of the programmed output voltage value. Short the input of the DMM and zero the DMM reading. If the DMM cannot be zeroed, record the reading and subtract this value from subsequent DMM readings.
  - c. Press the RESET key.
  - d. For each row in the dc calibrator output test function, set the output of the 5440B/5442A to the programmed output value using the DATA ENTRY keys.

# e. Press the OPR/STBY (OUTPUT STATE) key, and verify that the OPR indicator is on.

f. Verify that the DMM reading is within the tolerance values of Table 3-7.



Figure 3-5. Output Voltage Test: DC CALIBRATOR OUTPUT

#### **Output Noise Test**

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The following procedures are used to test the output noise of the 5440B/5442A. There are two stages to this test; 0.1 Hz to 10 Hz, and 10 Hz to 10 kHz.

Complete the following procedure to verify the output noise from 0.1 Hz to 10 Hz:

- 1. Place the DMM into Math Program 8 with the Display Option Register set to registor 8.3 (Standard Deviation Computed Variable) as follows:
  - a. Press SHIFT, 8, and PROGRAM SELECTION. Then press SHIFT, 0, ., 1, PROGRAM SELECTION, 8, ., 3, PROGRAM DATA.
  - b. Set the DMM to 200 mV DC Range, 1000 mS Filter, and 20 Samples/Second.
  - c. Set PROGRAMS IN USE to the ON position.
- 2. Perform the External Calibration Procedure on the 5440B/5442A, skipping the divider out and 10V sections of the cal sequence.
- 3. Set the standard voltage on the 20V range for 100 mV and place the 5440B/5442A in operate.
- 4. Connect the DMM to the 5440B/5442A output and press the DMM reset button once. After 10 seconds the DMM should read less than .0010E-3.
- 5. Press the NO button on the 5440B/5442A to advance to the 250V range and set the standard voltage back to 100 mV.
- 6. Press the reset button on the DMM once and verify that it reads less than .0100E-3 after 10 seconds.
- 7. Press the RESET key on the 5440B/5442A to terminate the procedure.

Complete the following procedure to verify the output noise from 10 Hz to 10 kHz:

- Connect the dual banana jack end of the special shielded twisted pair cable (see Figure 3-6) to the output of the 5440B/5442A.
- 2. Connect each of the BNC connectors on the other end of the cable to the HIGH and LOW inputs of the 7A22 Differential Amplifier, plugged into a 7603 Oscilloscope mainframe.
- 3. Set the 7A22 controls as follows:

Low Frequency -3 dB	10 Hz
High Frequency -3 dB	10 kHz
AC Coupling	both inputs
Volts/Div Vertical Deflection	$50 \ \mu V$

- 4. Set the scope horizontal deflection to 2 mS/Div.
- 5. Connect a True RMS Voltmeter set to the 100 mV range to the VERTICAL SIGNAL OUT BNC connector on the rear of the scope.
- 6. Set the 5440B/5442A to 6.5V and OPERATE.
- 7. After 10 seconds settling time, observe a reading on the voltmeter of less than 30 mV.
- 8. Adjust the 7A22 Volts/Div control to 500  $\mu$ V.
- 9. Connect a 12 k $\Omega$  load to the 5440B/5442A output for a load current of approximately 20 mA.
- 10. Set the 5440B/5442A to 250V and OPERATE. Wait for settling and observe a reading of less than 150 mV on the voltmeter. Typical output noise waveforms of 5440B/5442A are shown in Figure 3-7.

# Current Limit Test

Complete the following procedure to verify that the 5440B/5442A will output rated current without tripping and to verify that the current limit circuit trips at the correct value during an overcurrent condition:

#### NOTE

The operator can program a valid current limit up to 65 mA on the 11V and 22V ranges and 27.5 mA on higher ranges. However, the maximum guaranteed output current without overcurrent trip is 60 mA on the 11V and 22V ranges and 25 mA on higher ranges. In addition, if the selected output voltage is greater than 22V, the programmed current limit will be 27.5 mA unless the user selects a lower limit.

- 1. Press the RESET key. Verify that the 5440B/5442A is in the power-up reset state and the message VOLTAGE MODE appears on the alphanumeric display.
- 2. Connect the equipment as shown in Figure 3-8, but with the load disconnected.







n = 1 - 1



Figure 3-7. Typical Output Noise Waveforms

- 3. Program the 5440B/5442A for an output of 6V using the DATA ENTRY keys, then press the OPR/STBY (OUTPUT STATE) key so that the OPR indicator is on.
- 4. Allow 5 seconds for the output to settle, then apply the load as shown in Figure 3-8. Verify that the output does not trip.
- 5. Remove the load. Program the 5440B/5442A for an output of 10V using the DATA ENTRY keys.
- 6. Allow 5 seconds for the output to settle, then apply the load as shown in Figure 3-8. Verify that the output does trip.



Figure 3-8. Current Limit Test

7. Verify that the following message appears on the alphanumeric display within approximately 2 seconds, which indicates the output circuit has tripped:

OUTPUT LIMIT FAULT OUTPUT OVERCURRENT

#### NOTE

The error message may read:

#### OUTPUT LIMIT FAULT OUTPUT UNDERVOLTAGE

The message depends upon which function the monitor circuit was checking when the overload occurred, output voltage or output current.

- 8. Program the 5440B/5442A for an output current limit of 20 mA. Program the 5440B/5442A for an output of 1.86V using the DATA ENTRY keys. (Do not use the divider output.)
- 9. With the 100 $\Omega$  load still connected, set the OPR/STBY switch to Operate (OPR indicator is lit). Verify that the 5440B/5442A does not trip.

- 10. Using the EDIT OUTPUT keys, increase the output of the 5440B/5442A by .01V at a time.
- 11. Verify that the 5440B/5442A goes to standby and the following message appears on the alphanumeric display, when the output is between 1.86 and 2.14V:

OUTPUT LIMIT FAULT OUTPUT OVERCURRENT

- 12. Disconnect the load and reconnect a 1 k $\Omega$  load.
- 13. Program the 5440B/5442A for an output of 25V and a current limit of 27.5 mA. Allow five seconds for settling.
- 14. Connect the load and verify the output does not trip.
- 15. Select an output of 35V. Note that in approximately two seconds an output limited condition of step 11 above appears in the display.

# **External Sense Test**

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- Complete the following procedure to verify that the external sense circuit compensates for test lead losses:
  - 1. Press the RESET key. Verify that the 5440B/5442A is in the power-up reset state.
  - 2. Connect the equipment as shown in Figure 3-9 with the DMM set to the 2V range.
  - 3. Program the 5440B/5442A for an output of 2V using the DATA ENTRY keys, then press the OPR/STBY and SENSE (OUTPUT STATE) keys so that the OPR and EXT indicators are on.
  - 4. Record the DMM reading.
  - 5. Remove the 100 $\Omega$  load. Verify that the DMM reading does not change more than 1.0  $\mu$ V.



#### Figure 3-9. External Sense Test

# INTERNAL CALIBRATION PROCEDURE

The Internal Calibration Procedure is an automated procedure during which the 5440B/5442A measures most of the changes in the analog circuit parameters that may affect the accuracy of the 5440B/5442A output. These measurements are used to calculate new calibration constants. The new calibration constants are automatically entered to correct the 5440B/5442A output accuracy. The Internal Calibration Procedure can be initiated from the front panel or by IEEE-488 interface. Once the procedure has been initiated, no further operator assistance is needed.

Though the Internal Calibration Procedure is automatic, the 5440B/5442A provides three monitor features:

- While the procedure is in progress, milestone messages appear in the alphanumeric display so that the operator knows that function is being calibrated. These messages can also be reported using the IEEE-488 Interface.
- While the procedure is in progress, calibration data can be printed using the RS-232 interface. To use this feature, refer to the Analog Diagnostics Printout procedure, located in Section 4 of this manual.
- Once the Internal Calibration Procedure is finished, the new calibration constants can be displayed on the front panel or reported using the IEEE-488 Interface or the RS-232 Interface. Refer to the IEEE-488 Interface Setup or the RS-232 Interface Setup information in the 5440B/5442A Operator Manual.

Complete the following procedure to initiate an internal calibration:

- 1. Set 5440B/5442A POWER on. Allow the 5440B/5442A to warm up for at least 2 hours.
- 2. Press the SVCE (DATA ENTRY) key, then press the CAL SERV (soft) key, then press the INT CAL (soft) key. The following message appears on the alphanumeric display:

REMOVE OUTPUT LEADS & PROCEED WITH INTCAL?

- 3. Remove all connections from the front panel and the rear panel of the 5440B/5442A.
- 4. Press the ENTER/YES (DATA ENTRY) key. The 5440B/5442A proceeds with the internal calibration sequence. Each function being calibrated is shown on the alphanumeric display. When the internal calibration is finished, the following message appears on the alphanumeric display:

VOLTAGE MODE

#### EXTERNAL CALIBRATION PROCEDURE

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External Calibration is a semi-automatic procedure that compares the Calibrator's output to traceable voltage standards and corrects the Calibrator's output for long-term drift of the internal voltage reference. The recommended procedure uses the Fluke 732A Direct Voltage Reference Standard and the Fluke 752A Reference Divider to establish the necessary voltage standards which are then compared to the Calibrator with the Fluke 845A Null Detector.



External Calibration should be performed at an interval from 30 days to 1 year, depending upon the level of accuracy you wish to maintain.

The principal function of External Calibration is to correct for any shift in the Calibrator's internal voltage reference. A second function is to correct for long-term drift in the internal voltage divider resistors used for the 2.0V and 0.2V divided output ranges. All other time- and temperature-dependent changes in the Calibrator are corrected by the Internal Calibration procedure.

An abbreviated External Calibration procedure ("10V Cal") may be used following Internal Calibration to complete the calibration of all ranges except the 0.2V and 2.0V ranges. The abbreviated procedure is performed by comparing the Calibrator's output at 10V to the 732A Reference Standard, generating a calibration factor, and then applying the same correction factor to all ranges to correct for reference voltage shift.

The External Calibration procedure is arranged so that the 10V range is calibrated first, followed by the 20V, 0.2V, 2.0V, 250V, and 1100V ranges. If the full calibration procedure is used, each range is compared against the calibration standards, and a correction factor is determined for that range. If the abbreviated procedure is to be used, calibration of all ranges except 10V is skipped in the procedure, and the 10V range correction factor is applied.

To perform External Calibration, proceed as follows:

1. Perform the Internal Calibration procedure described earlier in this section.

#### NOTE

Ensure the Calibrator has warmed up before performing Internal Calibration.

- 2. Connect the test equipment as shown in Figure 3-10.
- 3. Turn on the Calibrator and all test equipment, and ensure that the 2-hour warm-up period has been satisfied before performing the calibration procedure.
- 4. Adjust the zero setting on the 845A Null Detector. Calibrate the 752A Reference Divider. Set the 752A for the 10V range.
- 5. Remove the decal covering the CAL/NORMAL switch, and set the CAL/NORMAL switch on the rear panel of the Calibrator to the CAL position.
- 6. Initiate External Calibration by pressing the following sequence of keys and soft keys: SVCE, CAL SVCE, EXT CAL. The following message appears on the alphanumeric display:

PERFORM EXTERNAL CALIBRATION?

7. Press the ENTER(YES) key. The following message appears on the alphanumeric display:

CONNECT OUTPUT FOR 10 VOLT EXT CAL?



Figure 3-10. External Calibration

8. Press the ENTER(YES) key. The following message appears on the alphanumeric display:

EXT CAL OF 10V RANGE STD V=10.00000V?

9. If the voltage reference standard is not exactly 10V, the exact value may be entered at this time with the numeric DATA ENTRY keys. When the alphanumeric display indicates the correct voltage, press the ENTER(YES) key. The following message appears on the alphanumeric display:

EDIT OUTPUT VOLTAGE, PUSH ENTER WHEN NULL

- 10. Set the OPR/STBY key to Operate (OPR indicator on). Switch the 845A Null Detector to OPR, and adjust the output voltage of the Calibrator using the EDIT OUTPUT keys to obtain a null indication on the Null Detector.
- 11. Switch the null detector to ZERO, and press the ENTER(YES) key. The following message will appear on the alphanumeric display:

EXT CAL OF 20V RANGE STD V=10.00000V?

12. At this point the decision may be made whether to perform the complete calibration procedure or the abbreviated procedure. To perform the complete calibration procedure, follow the prompting of the alphanumeric display to calibrate each range as follows:

a. Set the 752A range for the STD V indicated, and press the ENTER(YES) key.

b. Set the Calibrator to OPR, and edit for null.

c. Press the ENTER(YES) key, and go to the next range.

13. To perform the abbreviated procedure, when the display prompts for the 20V range as above, press the CLEAR(NO) key. The Calibrator then displays the following prompt:

CONNECT DIVIDER OUT FOR 2V & .2V EXTCAL?

14. Press the CLEAR(NO) key again. The Calibrator then displays the following prompt:

CONNECT OUTPUT FOR HI VOLT EXT. CAL?

15. Press the CLEAR(NO) key. The Calibrator then displays the following prompt:

WRITING TO NV MEMORY WAIT

# NOTE

Writing the calibration constants into memory takes about 35 to 40 seconds, after which the Calibrator returns to 0.0V output, standby, and Voltage Mode. If the complete calibration procedure is run, it concludes in the same way. The Calibrator writes the calibration constants into memory and returns to Standby as soon as the calibration of the 1100V range is completed.

16. Set the CAL/NORMAL switch to the NORMAL position, and cover the switch with a certification decal.

OUTPUT RANGE (V)	MESSAGE	VOLTAGE BEING NULLED (VDC)
none	CONNECT 5440 DIVIDER OUTPUT TO DO EXTCAL?	none
0.2	EXT CAL OF .2V RANGE STD V = .10000000 V?	0.1 (1)
2	EXT CAL OF 2V RANGE STD V = 1.0000000 V?	1 (1)
none	CONNECT TO 5440A OUTPUT TERMINALS ?	noné
10	EXT CAL OF 10V RANGE STD V = 10.000000 V?	10
20	EXT CAL OF 20V RANGE STD V = 10.000000 V?	10
100	EXT CAL OF 100V RANGE STD V = 100.00000 V	10
1000	EXT CAL OF 1000V RANGE STD V = 1000.0000 V?	10

#### Table 3-8. External Calibration Procedure



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Figure 3-11. Equipment Connections Equivalent to Use of the Fluke 752A

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# Section 4 Troubleshooting Information

#### INTRODUCTION

This section contains troubleshooting information for the 5440B/5442A. The following procedures and text explain how to use the extensive self-diagnostic capabilities of the 5440B/5442A. This section also includes additional troubleshooting information that supplements the self-diagnostic routines when they are not adequate in isolating the fault. In addition, a summary of all error messages and the corresponding actions taken by the instrument are provided at the end of this section under the heading 5440B/5442A Error Codes Summary.

# USING THE 5440B/5442A SELF DIAGNOSTICS

The 5440B/5442A Self Diagnostics have two major categories:

- Automatic (or monitoring) diagnostics.
- User-initiated diagnostics.

Once the instrument is energized, the automatic diagnostics do not require any user interface. The user-initiated diagnostics require minimal user interface. Both of these self-diagnostic routines provide fault indicators or operator prompts and error messages. In addition, the user-initiated diagnostic self-test results (for the analog and high voltage loop) may be printed out on an external printer for closer observation and historical reference.

Use of the self-diagnostic capabilities in the 5440B/5442A is an appropriate start in diagnosing a fault with the instrument. But first the technician should ensure that the problem is the 5440B/5442A and not some other piece of equipment. If a problem arises in a calibration system, check for the following items:

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- Proper and secure equipment interconnections.
- Adequate line voltage source(s).
- Proper use of the 5440B/5442A (e.g., output limits not exceeded).

Once these items have been verified, perform the Acceptance Test Procedure (located in Section 3 of this manual) to ascertain if there is a fault in the instrument.

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# AUTOMATIC SELF DIAGNOSTICS

The automatic self-diagnostics feature has two separate tasks. These are:

- Power-up Digital Tests
- Monitoring Functions

By testing the serial communication links between the microprocessors and between the digital and analog circuits, the power-up digital tests help ensure that the rest of the self diagnostics will function correctly. The monitoring functions of the automatic diagnostics detect functional failures during normal operation (e.g., output exceeding or below programmed voltage, serial link communication faults, etc.)

# **Power-up Digital Tests**

When the instrument is energized, the three microprocessors test the serial communication link between them. They also test some of their digital support circuits. The test routines are under software control, located in the RAM of each microprocessor. The tests performed by the microprocessors are explained in the following paragraphs.

# NOTE

The troubleshooting switches must be disabled for the Power-up diagnostics to run. (See the paragraphs on Troubleshooting Switches, later in this section.)

The main microprocessor performs the following diagnostic routines (in sequence):

- Boot ROM
- Main memory
- Interrupt bus
- Front-panel communications

At the beginning of the test sequence, an LED fault indicator is turned on, representing the status for each of the aforementioned circuits. As each test is successfully passed, the corresponding LED is turned off. If the LEDs do not turn off and stay off, a fault has been detected. Descriptions of the four main microprocessor tests are as follows:

- The boot ROM test is a simple checksum.
- The main memory test includes a ROM checksum, writing and verifying each RAM location, and reading a pattern from the last ROM.
- The interrupt bus test attempts to change the state of each of the interrupt lines, and enables those interrupts found to be operational.
- The front-panel communications test verifies proper communication between the main and front-panel microprocessors.



The front-panel microprocessor performs the following diagnostic routine:

- All LEDs are turned on (if not already on), and a memory test on ROM and RAM is performed. If there are no errors, the Front Panel PCA self-test LED is turned off.
- The front-panel microprocessor turns off all LEDs, and the message FRONT PANEL • RUNNING appears on the alphanumeric display.
- After communication is established with the main microprocessor the message VOLTAGE MODE appears on the alphanumeric display.

The guarded microprocessor performs the following diagnostic routine:

- A memory test is performed on ROM and RAM.
- The guarded digital bus is diagnosed for bus errors (e.g., lines held high or low).
- The digitally controlled analog pca's are checked for digital operation (e.g., responding to their addresses).
- If any errors occur, a message is sent to the main microprocessor.

#### **Monitoring Functions**

The automatic diagnostics monitoring functions, enabled at power-up, run continuously during normal operation. The monitor alternately samples output voltage and output current at approximately 1 second intervals to determine if these parameters are within the allowable tolerance of programmed values.

# OVER/UNDER VOLTAGE MONITOR

The output voltage of the 5440B/5442A is divided down by a resistor network that is a part of the sense current cancellation circuit located on the Output PCA. The output resistor of the divider is A4R30. The input resistor changes with the selected output range (10V, 22V, 275V and 1100V). The divided output (SDPOV) is sent to the multiplexer U25 on the Output/HV Control PCA where it is selected as an input to the a/d converter on the REF/DAC Digital PCA. The a/d converter reading is multiplied by a scaling factor, and the result is compared to the programmed value. If there is a deviation of more than 5%, a fault is detected, and the 5440B/5442A is placed in Standby mode and an appropriate message is sent to the alphanumeric display. The Over/Under Voltage Monitor function is disabled while the output of the instrument is being programmed.

#### OUTPUT CURRENT MONITOR

The output current of the 5440B/5442A flows through either R7 or R8 (depending upon polarity) located on the Output PCA. The voltage drop across R7 or R8 (I MON) is used as the current monitor signal to the a/d converter on the REF/DAC Digital PCA. The magnitude of the I MON signal is compared to the programmed output current limits. If the current limits are exceeded, the instrument is placed in Standby mode, and an error message appears on the alphanumeric display. The Output Current Monitor circuit has a 2-second delay to prevent transients from sending the instrument into Standby mode. The Output Current Monitor function is disabled while the output of the instrument is being programmed.

If the 5440B/5442A is connected to an impedance that is low enough to produce a current-limiting effect, the output voltage will probably drop below the programmed output

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voltage. If this occurs, the Over/Under Voltage Monitor may place the instrument in standby mode, and the message OUTPUT UNDERVOLTAGE appears on the alphanumeric display, even though the fault was caused by an overcurrent condition. This occurs because the monitor circuit alternately samples output voltage and output current, and the fault condition may be detected by either function depending upon which monitor function occurs first after the fault.

# POWER SUPPLY MONITORS

Both the Inside Regulator and the Outside Guard Regulator PCAs contain circuits to monitor the output of their regulated power supplies. The positive and negative voltages from a power supply are compared to each other by comparator ICs and resistor networks. If either polarity deviates more than 12 percent from the other, or if both go to 0 volts, the comparator activates a logic circuit that pulls the Power Supply Fault (PSF or GPSF) line low. The low on the PSF or GPSF line is sent to the controller, which places the instrument in Standby and turns on an LED (fault indicator) on the Regulator PCA. The monitor circuits cannot detect power supply faults where both supply polarities increase or decrease by the same amount. This type of fault is very unlikely because the regulators use independent circuits to produce the positive and negative polarities of regulated voltage.

# **USER-INITIATED DIAGNOSTICS**

The user-initiated diagnostics require a minimum of operator interface and are executed under control of the instrument. The operator is required to either set switches or press a few keys and verify the results. User-initiated diagnostics are divided into the following categories:

- Troubleshooting Switches
- Self-Tests (Analog, HV Loop, and Digital)

The troubleshooting switches are located on three different modules: the Controller PCA, the Front Panel Controller PCA, and the Guard Crossing PCA. These troubleshooting switches provide the user with predefined routines that send conditioning signals to aid in fault isolation. These routines do not provide fault messages to the front panel display.

The self tests are user-initiated from the keyboard (or IEEE-488 interface) and call up specific test programs for the analog, analog/high voltage loop (hv loop), and digital circuits. These test programs measure significant circuit parameters and display the result on the alphanumeric display. The results of the analog and hv loop self tests may also be sent to an external printer.

If a fault is detected during the analog or hv loop self tests, the routine (and the printout if connected) is stopped until the error is cleared. When a fault occurs, an error message indicating the nature of the fault appears on the alphanumeric display.

# Self-Tests

The following text and procedures describe how to use the self-test features of the 5440B/5442A. Information on how to call up the tests, what circuits are tested, and additional troubleshooting guidelines are given for each self test. Although they are separate tests, the analog and hv loop self tests are usually performed at the same time. The analog and hv loop self test may be performed once a week as a part of a routine preventive maintenance program.

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# **DIGITAL SELF-TEST**

The following procedure initiates the digital self test:

1. Call up the digital self test using one of the following steps:

IEEE-488	Send a TSTD device-dependent message on the IEEE-488 interface.
Front panel keyboard	Press the SERV key, then press the SELF TEST

(soft) key, then press the DIGITAL TEST (soft) key.

2. The following message appears on the alphanumeric display:

PERFORMING DIGITAL SELF-TEST. WAIT

3. If a fault is found, the self test stops and an error message appears on the alphanumeric display. Record the fault and press CLEAR to stop the test. Then refer to the paragraphs on Self-Test Error Messages and Printout Summary contained later in this section.

#### NOTE

Allow the instrument to warm up at least 1 hour before performing the Analog Self-Test or HV Loop Self-test procedure. This will ensure correct operating temperature of the ovened circuits.

#### NOTE

If the REF/DAC Analog PCA or the Preamp PCA has been repaired or replaced, perform an Internal Calibration before performing the Analog Self-Test.

#### ANALOG SELF-TEST

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Connect a printer to the RS-232 port, and enable the analog diagnostics printout as follows:

- 1. Connect the printer to the 5440B/5442A. Use an RS-232 Cable (and necessary adapters).
- 2. Press the SVCE (DATA ENTRY) key, then press the PORT SVCE (soft) key, then press the RS232 BAUD (soft) key. The instrument should default to a baud rate of 1200. Use the FASTER RS232 or SLOWER RS232 (soft) keys to set the baud rate. Press the center soft key to enter the selected baud rate into non-volatile memory.
- 3. When the baud rate is correct for the intended printer, press the SVCE (DATA ENTRY) key, then press the MONIT ON/OFF (soft) key, then press the MONIT ON (soft) key.
- 4. The instrument is now configured to print out the analog and hv loop self-test results.

The following procedure initiates the analog self test:

1. Call up the analog self test using one of the following steps:

IEEE-488	Send a TSTA device-dependent message on the IEEE-488 interface.
Front panel keyboard	Press the SVCE key, then press the SELF TEST (soft) key, then press the ANALOG TEST (soft) key.

2. Verify that the following message appears on the alphanumeric display:

REMOVE OUTPUT LEADS & DO ANALOG TEST ?

- 3. Remove all connections from the front panel and the rear panel Output or Boost Interface terminals of the 5440B/5442A.
- 4. Press the ENTER/YES (DATA ENTRY) key. The 5440B/5442A now performs a test of the analog circuits. The voltages measured at each test point are printed out, and the following message appears on the 16-Segment display:

22.000000V

5. While the analog self test is running, verify that the following message appears on the alphanumeric display:

PERFORMING ANALOG SELF-TEST. WAIT

- 6. If a fault is found, the self test stops and an error message appears on the alphanumeric display. Record the error message and press the CLEAR key to stop the test. Then refer to the paragraphs on Self-Test Error Messages and Printout Summary contained later in this section.
- 7. If no faults are found, the 5440B/5442A is returned to the default set up for the present operating mode.

#### **HV SELF-TEST**

4-13

#### WARNING

### TO AVOID ELECTRICAL SHOCK HAZARD, DO NOT MAKE ELECTRICAL CONTACT WITH THE OUTPUT HI OR SENSE HI TERMINALS. LETHAL VOLTAGES ARE PRESENT ON THESE TERMINALS DURING THE HIGH VOLTAGE TEST.

#### NOTE

The analog diagnostic printout (monitor) function may be enabled for the HV Loop Self-Test procedure (see Analog Self-Test procedure).

The following procedure initiates the high voltage self test:

1. Call up the high voltage self test using one of the following steps.

**IEEE-488** 

Send a TSTH device-dependent message on the (EEE-488 interface.

# Front panel keyboard Press the SERV key, then press the SELF TEST (soft) key, then press the HIGH V TEST (soft) key.

2. Verify that the following message appears on the alphanumeric display:

# REMOVE OUTPUT LEADS & DO HIGH VOLT TEST?

- 3. Remove all connections from the front panel and the rear panel Output or Boost Interface terminals of the 5440B/5442A.
- 4. Press the ENTER/YES (DATA ENTRY) key. The 5440B/5442A now performs a test of the high voltage circuits. The voltages measured at each test point are printed out and the following message appears on the 16-Segment display:

1100.0000V

5. While the high voltage self test is running, verify that the following message appears on the alphanumeric display:

### DOING HIGH VOLTAGE ANALOG OUTPUT TEST

- 6. If a fault is found, the self test stops and an error message appears on the alphanumeric display. Record the error message and press the CLEAR key to stop the test. Then refer to the paragraphs on Self-Test Error Messages and Printout Summary contained later in this section.
- 7. If no faults are found, the 5440B/5442A is returned to the default set up for the present operating mode.

#### Self-Test Error Messages and Printout Summary

# When any of the self test routines detect a fault, the test stops, and an error message appears on the alphanumeric display. Table 4-1 lists all the error messages by numeric order of the IEEE-488 Error Code Number. For each error message, Table 4-1 also gives an Action Code and the module(s) most likely to be defective. Refer to Table 4-2 for an explanation of the Action Codes.

If a printer is connected to the 5440B/5442A during the analog and HV Loop self tests and the Monitor function is enabled, a printout is produced. The printout contains additional information to help isolate a fault. Figures 4-2 and 4-3 contain typical samples of the analog and HV Self-Test printouts. Table 4-3 provides additional information, indexed to the analog and HV Loop Self-Test printouts, that is necessary to interpret the printout. Table 4-3 contains the measured signals, their location, location of the multiplexer used, signal limits, error messages, suspected malfunctioning assembly and other pertinent data. Refer to Figure 3-1 for the name and location of the pca's called out in Table 4-3.

The self tests cannot always isolate a fault to a module with absolute certainty. Instead, the self test identifies module(s) most likely to be defective. There are also faults that cannot be detected by the self tests at all. Because of these reasons, the self tests are only recommended as a starting point in diagnosing failures in the 5440B/5442A. The paragraphs on Module Fault Isolation provide more specific diagnostic information for the analog modules of the 5440B/5442A. Additional diagnostics information for the digital modules is covered in the paragraphs on Troubleshooting Switches.

5440A ERROR MESSAGE IEEE-488 ACTION ALPHANUMERIC DISPLAY REPORT TYPE	IEEE-488 REPORT	ACTION	SUSPECT MODULE(S) OR ACTION REQUIRED	PROBABILITY OF FAULT	COMMENTS	
POWER SUPPLY FAULT TEST UNGUARDED POWER	æ	v	A17 Outside Guard Regulator PCA A19 Outside Guard Term PCA*	MOT FOW	Unguarded power supply failure.	
POWER SUPPLY FAULT CHECK GUARDED POWER	თ	υ	A10 Inside Regulator PCA A12 Filter A PCA A11 Guarded Xfmr Term PCA*	HGH MED LOW D	Guarded power supply failure.	
MAIN CONTROL FAULT CHECK MAIN CONTROLLER	₽ ₽	υ	A16 Controller PCA Other PCA	HIGH	Boot ROM failure. The ROM located on the A16 Controller PCA failed the checksum test.	
MAIN CONTROL FAULT CHECK MAIN MEMORY	<b>F</b> -	υ	A15 Memory PCA Other PCA	HIGH	Main memory failure. The RAM or the ROM on the A15 Memory PCA failed to test true.	
MAIN CONTROL FAULT CHECK MAIN NV MEMORY	₩ ₩	۲	A15 Memory PCA Other PCA	ном	Non-volatile memory failure. The EAROM containing calibration data, IEEE-488 address, and baud rate setting was not programmed.	
MAIN INTERRUPT FAULT CHECK S OUTPUT TIMER	24	U	A16 Controller PCA	НОН	The serial output clock to the main microprocessor failed.	
MAIN INTERRUPT FAULT CHECK NVMEMORY TIMER	55	o	A16 Controller PCA	HIGH	The clock used to program the non-volatile memory failed.	
MAIN INTERRUPT FAULT CHECK SERIAL INPUT	26	U	A16 Controller PCA A18 I/O Assembly	нідн МЕD	The RS-232-C interface interrupt could not be cleared.	
MAIN INTERRUPT FAULT CHECK INPUT FR FRONT	27	<u>о</u>	A16 Controller PCA A2 Front Panel Controller PCA	HIGH	The front panel interrupt could not be cleared.	
MAIN INTERRUPT FAULT CHECK MAIN CLOCK	28	<u>ں</u>	A16 Main Controller PCA	HGH	The system timer interrupt failed.	
MAIN INTERRUPT FAULT CHECK REMOTE INPUT	53	<u>о</u>	A16 Controller Assembly A18 I/O Assembly	HIGH	The IEEE-488 interface IC failed.	
MAIN INTERRUPT FAULT CHECK INPUT FR GUARD	30	0	A16 Main Controller PCA A14 Guard Crossing PCA	HIGH MED	The guard interrupt failed. If the front panel operates all right, then the A14 Guard Crossing PCA is probably defective.	
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						10		·••		DA Err		000	149 -	5011		an y (	cont	/								-
COMMENTS		Front panel memory failed.	Front panel microprocessor interrupt failed.	Guard crossing memory failed.		Guarded data bus fault.		Guarded address bus fault.		Guarded control bus fault (HU/WH of AUK line).						• •	Guarded status bus fault (GPOP, GPSF, DRLS,	DAMS line).								
PROBABILITY	OF FAULT	нон	HIGH	HIGH								MEU	MED	MED	MED	MED								HIGH	MO I	MED
ſ	OR ACTION REQUIRED	A2 Front Panel Controller PCA	A2 Front Panel Controller PCA	A14 Guard Crossing PCA		Guarded bus fault. Remove the	following modules one at a	time using ure removing procedure: turn the power off,	remove the module, then turn	power on. The error will not appear when the defective	module is removed.	A14 Guard Crossing PCA	A5 Output/HV Control PCA	A6 Sample String PCA	A7 Preamp PCA	A8 REF/DAC Digital PCA	Guarded data bus fault. Remove	the following modules one at a	time using the following	procedure: turn the power off,	remove the module, men turn power on The error will not	appear when the defective	module is removed.	A14 Guard Crossing PCA	A3 Mother Board PCA	A10 Inside Regulator PCA
ACTION	ТУРЕ	J	o	ပ		o											0								., .	
IEEE-488 ACTION	REPORT	32	ĸ	40		41		42		43							41									1841
5440A ERROR MESSAGE	ALPHANUMERIC DISPLAY REPORT	FRONT DIGITAL FAULT	FRONT DIGITAL FAULT	INSIDE GUARD FAULT	CHECK GUARD MEMORY	INSIDE GUARD FAULT	CHECK GUARD DATA BUS	INSIDE GUARD FAULT	CHECK GUARD ADDR BUS	INSIDE GUARD FAULT CHECK GUARD CTRL BUS							INSIDE GUARD FAULT	CHECK GUARD STATUS								

			T	able 4-	1. 5440A	Error Codes	Summary	(cont)
COMMENTS	A8 REF/DAC Digital PCA acknowledge failure.	A7 Preamp PCA acknowledge failure.	A6 Sample String PCA acknowledge failure.	A5 Output/HV Control PCA acknowledge failure.	Guard communication error. The A14 Guard Crossing PCA did not respond to the main microprocessor with the expected data.	Guard timeout. The A14 Guard Crossing PCA did not respond to the main microprocessor within the required time period.	Local communication error. A communication error occurred between the front microprocessor and the main microprocessor.	Analog measurement bus fault. * Note: Errors 56 and 57 may be caused by a low or noisy +5V togic supply on A17. Before changing A14, verify both +5V supplies.
PROBABILITY OF FAULT	HIGH	нон	нвн	HIGH	HIGH	HIGH HIGH	HIGH MED	
SUSPECT MODULE(S) OR ACTION REQUIRED	A8 REF/DAC Digital PCA	A7 Preamp PCA	A6 Sample String PCA	A5 Output/HV Control PCA	A14 Guard Crossing PCA	A8 REF/DAC Digital PCA (A/D) (during normal operation) A14 Guard Crossing PCA (after Power-up only)	A16 Controller PCA A2 Front Panel Controller PCA	Place the ACK switch on the A14 Guard Crossing PCA on (1) and remove the following modules one at a time: A5 Output/HV Control PCA, A7 Preamp PCA, and A9 REF/DAC Anatog PCA. The error message will change when the defective module is pulled. If all three module is pulled. If all three module is pulled. If with no change in the error message, replace the A8 REF/DAC Digital PCA.
ACTION	U	O	O	o	o	U	o	0
IEEE-488 ACTION REPORT TYPE	48	<del>6</del> 4	50	51	*56	*57	64	22
5440A ERROR MESSAGE IEEE-468 ALPHANUMERIC DISPLAY REPORT	BOARD ACK FAULT CHECK DAC BOARD	BOARD ACK FAULT CHECK PREAMP BOARD	BOARD ACK FAULT CHECK SAMPLE STRING	BOARD ACK FAULT CHECK OUTPUT BOARD	GUARD COMMUNIC FAULT CHECK GARBLED DATA	GUARD COMMUNIC FAULT GUARD NOT ANSWERING	FRONT COMMUNIC FAULT	ANALOG MEASURE FAULT CHECK ANALOG BUSS



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5440A ERROR MESSAGE ALPHANUMERIC DISPLAY	IEEE-488 ACTI REPORT TYP	ACTION	SUSPECT MODULE(S) OR ACTION REQUIRED	PROBABILITY OF FAULT	COMMENTS
			A8 REF/DAC Digital PCA A9 REF/DAC Analog PCA A7 Preamp PCA A5 Output/HV Control PCA	MED MED MED	
ANALOG MEASURE FAULT CHECK ZERO AMP	73	o	Run the Analog Self-Test		Zero amplifier fault.
ANALOG MEASURE FAULT UNABLE TO ZERO RANGE	74	o	Run the Analog-Self-Test		Unable to zero a range during an Internal Calibration.
ANALOG MEASURE FAULT GAIN SHIFT TOO LARGE	75	υ	Run the Analog Self-Test		An invalid gain shift measurement was made.
DAC DIGITAL FAULT CHECK A TO D	80	Ö	A8 REF/DAC Digital PCA	нсн	A-to-D converter on the A8 REF/DAC Digital PCB failed.
DAC DIGITAL FAULT CHECK FIRST SWITCH	81	<u>.</u> 0	A8 REF/DAC Digital PCA	нан	First switch control signal on the A8 REF/DAC Digital PCA failed.
DAC DIGITAL FAULT SECOND SWITCH	82	o	A8 REF/DAC Digital PCA	HIGH	Second switch control signal on A8 REF/DAC Digital PCA failed.
DAC DIGITAL FAULT BIAS SIGNAL	8	0	A8 REF/DAC Digital PCA	HIGH	The bias control signal on the A8 REF/DAC Digital PCA failed.
DAC ANALOG FAULT CHECK 0V OUTPUT	87	o	A9 REF/DAC Analog PCA	HIGH	The 0V output of the A9 REF/DAC Analog PCA failed.
DAC ANALOG FAULT CHECK REFERENCE	88	0	A9 REF/DAC Analog PCA	нон	The reference on the A9 REF/DAC Analog PCA failed.
DAC ANALOG FAULT CHECK -5V REGULATOR	68	o	A9 REF/DAC Analog PCA	нСн	The -5V regulator on the A9 REF/DAC Analog PCA failed.
DAC ANALOG FAULT CHECK +10V OUTPUT	6	o	A9 REF/DAC Analog PCA	нісн	The +10V output of the A9REF/DAC Analog PCA failed.
DAC ANALOG FAULT CHECK -10V OUTPUT	91	ບ່	A9 REF/DAC Analog PCA	HIGH	The -10V output of the A9 REF/DAC Analog PCA failed.

5440A ERROR MESSAGE IEEE-488	IEEE-488 ACT REPORT TY	ACTION	SUSPECT MODULE(S) 0 OR ACTION REQUIRED	PROBABILITY OF FAULT	COMMENTS
DAC ANALOG FAULT CHECK DAC FILTER	92	U	A9 REF/DAC Analog PCA	нан	The filter on the A9 REF/DAC Analog PCA failed.
DAC ANALOG FAULT CHECK +5V DAC CKT	88 8	o	A9 REF/DAC Analog PCA	нен	The 0V output of the A9 REF/DAC Analog PCA failed.
DAC ANALOG FAULT CHECK SECOND SPEED	94	ç	A9 REF/DAC Analog PCA	нон	The bias circuit on the A9 REF/DAC Analog PCA failed.
DAC ANALOG FAULT CHECK DAC OVEN	35	o	A9 REF/DAC Analog PCA	нан	The oven on the A9 REF/DAC Analog PCA failed or insufficient warm-up time was allowed.
GRD PWR SUPPLY FAULT CHECK +5V DAC REC	96	U	A10 Inside Regulator PCA A12 Filter A PCA A11 Guarded Xfmr Term PCA*	HIGH MED LOW	The +5V regulator on the A10 Inside Regulator PCA failed.
GRD PWR SUPPLY FAULT CHECK +20V OVEN	67	υ	A13 Filter B PCA A11 Guarded Xfmr Term PCA <sup>+</sup>	MED HIGH	The +20V Oven Supply failed.
PREAMP ANALOG FAULT CHECK INTCAL CONFIG	104	U	A7 Preamp PCA	MED	The internal Calibration configuration on the A7 Preamp PCA failed.
P-AMP/OUT BRDS FAULT CHECK 10V/20V RANGE	107	o	A7 Preamp PCA A5 Output/HV Control PCA A4 Output PCA	MED LOW MED	The 10V/20V range failed.
P-AMP/OUT BRDS FAULT CHECK -10V OUTPUT	108	v	A7 Preamp PCA A5 Output/HV Control PCA A4 Output PCA	MED LOW HIGH	The -10V output did not work properly.
P-AMP/OUT BRDS FAULT CHECK STANDBY CONFIG	109	o	A7 Preamp PCA A5 Output/HV Control PCA A4 Output PCA	MED LOW HIGH	The Standby didn't work properly.
PRE-AMP ANALOG FAULT CHECK PRE-AMP OVEN	110	U	A7 Preamp PCA	нідн	The A7 Preamp PCA oven failed, or insufficient warm-up time was allowed.
OUTPUT BOARDS FAULT CHECK ZERO AMP	112	0	A5 Output/HV Control PCA A4 Output PCA	ном Нідн	The zero amp on the A5 Output/HV Control PCA or the A4 Output PCA failed.

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COMMENTS	The 2V range failed.	The current limit circuit failed.	The 0.2V range failed.	The 250V range failed.	The 10V Internal Calibration configuration didn't work properly.	The 20V Internal Calibration configuration didn't work properly.	The 1 kV range didn't work properly.	The High Voltage Internal Calibration configuration did not work.	The oven on the A6 Sample String PCA is defective or insufficient warm-up time was allowed.	The -275V range did not work.	The +275V range did not work.	The +550V range did not work.
PROBABILITY OF FAULT	H9IH rom	HOH	HOH	MED MED	MED	MED	MED	MED	HOH	MED MED	MED MED	MED MED
SUSPECT MODULE(S) OR ACTION REQUIRED	A5 Output/HV Control PCA A4 Output PCA	A5 Output/HV Control PCA A4 Output PCA	A5 Output/HV Control PCA A4 Output PCA	A7 Preamp PCA A5 Output/HV Control PCA A4 Output PCA	A6 Sample String PCA	A6 Sample String PCA	A6 Sample String PCA	A7 Preamp PCA A6 Sample String PCA	A6 Sample String PCA	A13 Fitter B PCA A4 Output PCA	A13 Filter B PCA A5 Output/HV Control PCA A4 Output PCA	A13 Filter B PCA A5 Output/HV Control PCA A4 Output PCA
ACTION TYPE	с	o	с	ပ	o	o	o	ပ	ပ	o	ပ	o
IEEE-488 ACTION REPORT TYPE	113	114 .	115	116	120	121	122	123	124	128	129	. 130
5440A ERROR MESSAGE ALPHANUMERIC DISPLAY	OUTPUT BOARDS FAULT CHECK 2V RANGE	OUTPUT BOARDS FAULT CHECK CURR LIM CKT	OUTPUT BOARDS FAULT CHECK .2V RANGE	P-AMP/OUT BRDS FAULT CHECK 250V RANGE	SAMPLE STRING FAULT CHECK 10V INTCAL	SAMPLE STRING FAULT CHECK 20V INTCAL	SAMPLE STRING FAULT CHECK 1 KV RANGE	P-AMP/S-STRING FAULT CHECK HIGH V INTCAL	SAMPLE STRING FAULT CHECK S-STRING OVEN	FIL B/OUT BRDS FAULT CHECK -275V RANGE	FIL B/OUT BRDS FAULT CHECK +275V RANGE	FIL B/OUT BRDS FAULT CHECK +550 RANGE

88 ACTION SUSPECT MODULE(S) PRO RT TYPE OR ACTION REQUIRED OF	AODULE(S) REQUIRED	DBABILIT DF FAULT	<u>≻</u>	COMMENTS The 4.875M rande did not work
131 C A13 Filter B PCA MED A5 Output/HV Control PCA MED A4 Output PCA MED		ΞΞΣ	٥٥۵	The ∻875V range did not work.
132 C A13 Filter B PCA M A5 Output/HV Control PCA M A4 Output PCA M		222	MED MED	The +1100V range did not work.
136 C Check the front panel terminals	Check the front panel terminals.			The output was over the output current limit.
137 C A8 REF/DAC Digital PCA H A9 REF/DAC Analog PCA N A4 Output PCA N		I 2 2	HIGH MED MED	The output was over voltage.
138 C A8 REF/DAC Digital PCA A9 REF/DAC Analog PCA A4 Output PCA			HIGH MED MED	The output was under voltage.
144 C A18 I/O Assembly		-	MED	The wrong type instrument is connected to the Boost Interface.
145 D A18 I/O Assembly		_	MED	No instrument is connected to the Boost Interface.
146 B Check the instrument connected to the Boost Interface.	Check the instrument connected to the Boost Interface.			Voltage boost trip.
147 B Check the instrument connected to the Boost Interface.	Check the instrument connected to the Boost Interface.			Current boost trip.
152 A Check the IEEE-488 interface connector.	Check the IEEE-488 interface connector.			IEEE-488 interface source handshake error.
153 A Check the IEEE-488 interface controller program.	Check the IEEE-488 interface controller program.			IEEE-488 interface terminator error. The A18 I/O Assembly received a carriage return (CR) without a line feed (LF).



5440A EHROH MESSAGE ALPHANUMERIC DISPLAY	IEEE-408 AC	ACTION	SUSPECT MODULE(S) OR ACTION REQUIRED	PROBABILITY OF FAULT	COMMENTS
IEEE488 REMOTE ERROR EXPECTING SEPARATOR	154	A	Check the IEEE-488 interface controller program.		IEEE-488 interface separator error. The A18 I/O Assembly received a 5440A Statement from which a separator was missing.
IEEE488 REMOTE ERROR EXPECTING HEADER	155	۲	Check the IEEE-488 interface controller program.		IEEE-488 interface header error. The A18 I/O Assembly received a 5440A Statement with an invalid header.
IEEE488 REMOTE ERROR EXPECTING NUMBER	156	Κ.	Check the IEEE-488 interface controller program.	· -	IEEE-488 interface numeric error. The A18 I/O Assembly received a 5440A Statement with an invalid numeric string.
IEEE488 REMOTE ERROR BUFFER OVERFLOW	157	۲	Check the IEEE-488 interface controller program.		IEEE-488 interface buffer overflow. The A18 I/O Assembly received a 5440A Statement with more than 127 characters.
IEEE488 REMOTE ERROR BAD CHARACTER	158	¥	Check the IEEE-488 interface controller program.		IEEE-488 interface character error. The A18 I/O Assembly received an invalid character.
RS232C SERIAL ERROR	160	۲	A18 I/O Assembly Interface Incompatibility	MED HIGH	The printer port handshake timed out. This means that the handshake on the RS-232-C interface was not completed.
USER ENTRY ERROR NUMBER OUT OF RANGE	168	K	Operator error.		A numeric parameter entered at the front panel was not within the allowable range for that parameter.
USER ENTRY ERROR OUTPUT OUT OF RANGE	169	۲.	Operator error.		An output was entered at the front panel that was not within the output entry limits for that mode.
USER ENTRY ERROR LIMITS OUT OF RANGE	0/1	۲.	Operator error.		A limit was entered at the front panel that was not within the allowable maximums and minimums for that limit.
USER ENTRY ERROR DIVIDER OUT OF RANGE	E.	<b>A</b>	Operator error.	, , ,	The DIV OUTPUT STATE key was used incorrectly.
			•		

5440A ERROR MESSAGE	IEEE-488 ACT	ACTION		PROBABILITY	COMMENTS	
ALPHANUMERIC DISPLAY	REPORT	ТҮРЕ	OR ACTION REQUIRED	OF FAULT		
USER ENTRY ERROR IN OUTPUT TERMINAL	172	¥	Operator error.		The SENSE OUTPUT STATE key was used incorrectly.	
USER ENTRY ERROR IN OUTPUT TERMINAL	173	۲	Operator error.		The GUARD OUTPUT STATE key was used incorrectly.	
USER ENTRY ERROR CAL SWITCH LOCKED	174	۲	Set the CAL/NORMAL Switch to the NORMAL position. A18 I/O Assembly	HIGH MED	An External Calibration was attempted with the rear panel CAL/NORMAL Switch is in the NORMAL position.	
USER ENTRY ERROR INSTRUMENT IS BUSY	175	۲	Operator error.		A command was entered, from the front panel, that is not allowed in the present instrument state.	
STORAGE MODULE ERROR CANNOT READ MODULE	none	4	5440A-7001 Storage Module A2 Front Panel Controller PCA	HIGH MED	Data could not be read from the 5440A-7001 Storage Module.	
STORAGE MODULE ERROR CANNOT READ MODULE	none	<	5440A-7001 Storage Module A2 Front Panel Controller PCA A17 Outside Guard Regulator PCA	HIGH MED A	Data could not be written to the 5440A-7001 Storage Module.	
SEQUENCING ERROR MUST XFR MOD TO MEM	none	4	Store the test sequence in sequence memory.		There is no test sequence in sequence memory.	
SEQUENCING ERROR NO SUCH STEP NUMBER	none	۲	Operator error.		The step number selected is not in sequence memory.	•••
SEQUENCING ERROR SEQ MEMORY IS FULL	none	<	None		Sequence memory is full.	
SEQUENCING ERROR	none	Å	5440A-7001 Storage Module	HIGH	There is a bad step in sequence memory.	

# Table 4-1, 5440A Error Codes Summary (cont)

BAD STEP IN SEQ MEM SEQUENCING ERROR

	Table 4-2. 5440A Action Code Definitions
CODE	ACTION
А	The error is reported and no action is taken.
в	The error is reported and the 5440A is set to Standby.
С	The error is reported, the 5440A is set to Standby, and any operation in progress is aborted.
D	The error is reported, and the 5440A is reset to the default setup for Voltage Mode operation.

#### **Troubleshooting Switches**

4-15

The following procedure and tables describe how to use the troubleshooting switches in the 5440B/5442A to isolate faults within the digital modules.

To use the troubleshooting switches on the Controller and Front Panel Controller PCAs, perform the following steps:

- 1. Set the 5440B/5442A POWER switch to OFF.
- 2. Remove the covers and guard shield from the 5440B/5442A.
- 3. Place the Controller PCA on an extender card. The Front Panel Controller PCA cannot be placed on an extender card and must be removed. (Refer to the Front Panel Access procedures in Section 3 of this manual.)
- 4. Set S1 to 0 on either the Controller or the Front Panel Controller PCA (this enables the troubleshooting switch mode).
- 5. Set the 5440B/5442A POWER switch to ON.
- 6. Refer to Table 4-4 for switch settings on the Controller PCA or Table 4-5 for switch settings on the Front Panel Controller PCA.
- 7. Note the TEST and TEST FUNCTION DESCRIPTION for each of the switch settings and probe the appropriate signals on the extender card.

#### NOTE

Be sure to reset S1 to 1 before reinstalling the Controller PCA or the Front Panel Assembly.

The Guard Crossing PCA has one troubleshooting switch, S2. This switch is used to send a "walking zero" pattern to the address, data, and control buses.

- 1. Set the 5440B/5442A POWER switch to OFF.
- 2. Remove the cover and guard shield from the instrument.
- 3. Place the Guard Crossing PCA on an extender card.
- 4. Remove A14U1 (prevents bus conflicts).
- 5. Remove all analog PCAs.

SUSPECT	PCA(S)	AB	A9 A6 A7 A8	AB		A9	A8 	A8 A7 A5	A8 A7 A5 A9	A8 A7 A5 A9 A9	A8 A7 A9 A9 A10	A8 A7 A5 A9 A9 A10	A8 A7 A5 A9 A9 A9 A9 A9	A8 A7 A9 A9 A9 A9 A8 A3	A8 A7 A9 A9 A9 A9 A9 A9 A9	
FRONT PANEL	ERROH MESSAGE(S)	DAC DIGITAL FAULT CHECK A/D	DAC ANALOG FAULT CHECK REFERENCE	DAC DIGITAL FAULT CHECK A/D		ANALOG MEASURE FAULT	CHECK ANALOG BUS?	CHECK ANALOG BUS?	CHECK ANALOG BUS? DAC ANALOG FAULT CHECK REFERENCE	CHECK ANALOG BUS? DAC ANALOG FAULT CHECK REFERENCE DAC ANALOG FAULT CHECK +5V DAC CKT	CHECK ANALOG BUS? DAC ANALOG FAULT CHECK REFERENCE DAC ANALOG FAULT CHECK +5V DAC CKT GRD PWR SUPPLY FAULT CHECK +5V DAC REG	CHECK ANALOG BUS? DAC ANALOG FAULT CHECK REFERENCE DAC ANALOG FAULT CHECK +5V DAC CKT GRD PWR SUPPLY FAUL CHECK +5V DAC REG	CHECK ANALOG BUS? DAC ANALOG FAULT CHECK REFERENCE DAC ANALOG FAULT CHECK +5V DAC CKT GRD PWR SUPPLY FAUL CHECK +5V DAC REG CHECK -5V DAC REG DAC ANALOG FAULT DAC ANALOG FAULT	CHECK ANALOG BUS? DAC ANALOG FAULT CHECK REFERENCE DAC ANALOG FAULT CHECK +5V DAC CKT GRD PWR SUPPLY FAUL CHECK -5V DAC REG CHECK -5V DAC REG DAC ANALOG FAULT CHECK -5V REGULATOR DAC DIGITAL FAULT CHECK FIRST SWITCH	CHECK ANALOG BUS? DAC ANALOG FAULT CHECK REFERENCE DAC ANALOG FAULT CHECK +5V DAC CKT GRD PWR SUPPLY FAUL CHECK +5V DAC REG CHECK +5V DAC REG DAC ANALOG FAULT DAC ANALOG FAULT CHECK FIRST SWITCH	CHECK ANALOG BUS? DAC ANALOG FAULT CHECK REFERENCE DAC ANALOG FAULT CHECK +5V DAC FAULT CHECK +5V DAC REG CHECK -5V DAC REG DAC ANALOG FAULT CHECK -5V REGULATOF DAC DIGITAL FAULT CHECK FIRST SWITCH
CIRCUIT	TESTED	Check and Cat. A/D	RCOM offset voltage			Analog	Measurement	Measurement bus	Measurement bus DAC Analog Reference	Measurement bus DAC Analog Reference +5V DAC Supply	Measurement bus DAC Analog Reference +5V DAC Supply	Measurement bus DAC Analog Reference +5V DAC Supply	Measurement bus DAC Analog Reference +5V DAC Supply -5V DAC	Measurement bus DAC Analog Heference +5V DAC Supply -5V DAC Supply First	Measurement bus DAC Analog Heference +5V DAC Supply Supply First Switching Control Logic Logic	Measurement bus DAC Analog Heference +5V DAC Supply -5V DAC Supply Firsl Switching Control Logic
OFFSET'		0.0V	-2.3 mV	-2.3 mv		V0.0		+3.7 mV dc	+3.7 mV dc 0.0V	+3.7 mV dc 0.0V -2.3 mV	+3.7 mV dc 0.0V -2.3 mV -3.5 mV	+3.7 mV dc 0.0V -2.3 mV -3.5 mV	+3.7 mV dc 0.0V -2.3 mV -3.5 mV -3.4 mV	+3.7 mV dc 0.0V -2.3 mV -3.5 mV -3.4 mV -2.3 mV	+3.7 mV dc 0.0V -2.3 mV -3.5 mV -2.3 mV -2.3 mV	+3.7 mV dc 0.0V -2.3 mV -3.5 mV -3.5 mV -2.3 mV -2.3 mV
GAIN		1.0	0.1	389		.07132		05882	05882	05882 07132 02924	.05882 .07132 .02924 .02315	02882 07132 02924 .02925	.05882 .07132 .02924 .02315 .02315	.05882 .07132 .02924 .02315 .02315 .02315	.05882 .07132 .02924 .02315 .02315 .02315	.05882 .07132 .02924 .02315 .02315 .02315
Q/¥		0.0V	-2.3 mV	+0.970V dc	ounts)	+0.941V dc		+1.004V dc	1							
MUX LOCATION	IC PIN#	140-14 0.0V	U40-12	U40-4	- ADM2 o	U20-13		U25-12	U25-12 U20-13	U25-12 U20-13 U40-15			<u>↓                                    </u>			
	PCA	t AB	2 A8	A8	ounts -	64 4		A5				A9 A	A9 A9 A9 A9 A9 A9 A9 A9	A9 A	A9 A	A9 A9 A9 A9 A9 A9 A9 A9 A9 A9 A9 A9 A9 A
LOCATION	PCA IC/TP	U40-14 TP11	U40-12 TP11	U24-2 U24-3	DM3 c /Count	TP18		8dT 1P8	TP8 TP9 TP18 TP18 TP19	TP8 TP9 TP18 TP18 TP19 TP15	TP8 TP9 TP18 TP19 TP15 TP15 TP10	TP8 TP19 TP19 TP15 TP10 4 Nom	TP18 TP18 TP18 TP15 TP15 TP15 TP16 TP16 TP11 TP11 TP11	TP8 TP9 TP19 TP19 TP15 TP10 TP11 TP10 TP11 TP11	TP8 TP9 TP19 TP19 TP19 TP10 TP10 TP11 TP11 TP11 TP11 TP11 TP11	TP8 TP9 TP19 TP19 TP15 TP10 TP11 TP11 TP11 TP11 TP11 TP11 TP11
2 CO LO LO LO	PCA	A8	AB	A8	285/(A 83 mV	6Y 3		A5				A5 A9 A3 - M	A 49 A 49 A 49 A 49 A 49 A 49 A 49 A 49	A5 A9 A3 A9 A3 A9 A3 A9 A9 A9	A 49 A 49 A 49 A 49 A 49 A 49 A 49 A 49	A9 A9 A9 A9 A9 A9 A9 A9 A9 A9 A9 A9 A9 A
URED NAL	NOM. VALUE	0 <sup>.0</sup> V	-2.3 mV	+2.5V dc	actor = .97 alue = + .2	+13.2V dc		+17.0V dc	+17.0V dc +13.2V dc	+17.0V dc +13.2V dc -11.3V	+17.0V dc +13.2V dc -11.3V -16.3V	VIEL         +17.0V         dc         A5         TP8         A5           +17S         +17.0V         dc         A5         TP8         A5           VREF         +13.2V         dc         A9         TP19         A9           V1(FH)         -11.3V         A9         TP15         A8           V1(FC)         -16.3V         A9         TP10         A9           V1(FC)         -16.3V         A9         TP10         A9           +5V DAC Supply = M3 - M4 Nominal =         +5V DAC Supply = M3 - M4 Nominal =         A9	+17.0V dc +13.2V dc -11.3V -16.3V Supply = M	+17.0V dc +13.2V dc -11.3V -16.3V Supply = M -16.2V	+17.0V dc +13.2V dc -11.3V -16.3V Supply = M -5.0V -16.2V	Viety         +17.0V dc         45           +175         +13.2V dc         A9           V1(FH)         -11.3V         A9           V1(FC)         -16.3V         A9           V1(FC)         -16.3V         A9           V1(FC)         -16.2V         A9           FO1         -5.0V         A9           FO1         -16.2V         A9           FO1         -16.2V         A9           FO1         -16.2V         A9           A9         A9         A9
MEASURED	MNEM-	RCOM	SCOM	+2.5V Ref	A/D Cal. F <sub>2</sub> Nominal Va	Reference (Vref)				+17S +17S VREF V1(FH)						
STIMIT		+1.0 mV -1.0 mV	-1.0 mV -3.5 mV	A/N	+.340 mV dd A/D Cal. Factor = .97285/(ADM3 counts - ADM2 counts) +.225 mV dd Nominal Value = + .283 mV/Count	+14.0V dc +12.5V dc		+19.00V dc +15.00V dc	+19.00V dc +15.00V dc +14.0V dc +12.5V dc	+19.00V dc +15.00V dc +14.0V dc +12.5V dc -8.6V -14.1V	+19.00V dc +15.00V dc +14.0V dc +12.5V dc -8.6V -14.1V -13.25V -13.25V	+19.00V dc +15.00V dc +14.0V dc +12.5V dc -8.6V -14.1V -13.25V -13.5V -13.5V -13.5V dc +4.50V dc	+19.00V dc +15.00V dc +14.0V dc +12.5V dc -8.6V -14.1V -14.1V -13.25V -13.25V -13.25V -13.25V -14.50V dc +4.50V dc +4.50V dc	+19.00V dc +15.00V dc +14.0V dc +12.5V dc -8.6V -14.1V -13.25V -13.25V -13.25V -13.25V -13.25V dc +4.50V dc +4.50V dc -3.25V dc -13.25V	+19.00V dc +15.00V dc +12.5V dc -8.6V -14.1V -14.1V -13.25V -13.25V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.5V -13.	+19.00V dc +15.00V dc +14.0V dc +12.5V dc -14.1V -13.25V -13.25V -13.25V -13.25V -13.25V dc +4.50V dc +4.50V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V -13.25V
D) X		ADM1	ADM2	ADM3	ADC1	١W		M2								

Table 4-3. Analog Self-Diagnostics

1		MEAS	MEASURED	SIG	NAL	2	MUX						
LIMITS	ŝ	MNEM-	SIGNAL A- NOM. C VALUE	PC LOC	PCA IC/TP	PCA LOC	CA IC PIN #	A/D INPUT	GAIN	OFFSET <sup>4</sup>	CIRCUIT	FRONT PANEL ERROR MESSAGE(S)	SUSPECT PCA(S)
+.25V dc 25V	웡	Average	Average - 50% Vatue = C2 -	5		minal	M8 Nominal = 0.0V dc				First Switching Circuit Control Logic	DAC DIGITAL FAULT CHECK FIRST SWITCH	AB
-4.15V -5.50V	* *	SQT	-4.9V	A8 A9	U20-5 TP11	A8	U40-1	-0.488V	.09911	-2.3 mV	Second Switching	DAC DIGHTAL FAULT CHECK SECOND SWITCH	A8
0.0V -2.5V		SQT	-1.25V	A8 A9	U20-5 TP11	AB	U40-1	-0.126V	.09911	-2.3 mV	Circuit Control Lonie		
-2.0V -4.0V		Average V	Average Voltage = (0.5) M9 +	- 6W (s	+ (0.5) M10	M10 ‡	Nominal = 3.0V dc	= 3.0V dc			5 70 1		
-2.0V -4.0V	~ ~	SOT	× .	A9 A9	U20-5 TP11	ÅB	U40-1	-0.30V	09911	-2.3 mV			
+ 25V - 25V	+.25V dc 25V	Average	- 50% Value = C4	5	- M11 P	Nomin	Nominal = 0.0V dc	융					
-10.5V -20.0V	25	Z [V1 (FH)]#	-15.0V	A8 A9	U39-5 TP11	A8	U40-2	-0.486V	.03226	-2.3 mV	Bias Control	DAC DIGITAL FAULT CHECK BIAS SIGNAL	A8
-11.0V -21.5V	SV SV	Z [V1 (FH)]	-16.2V	A8 A9	U39-5 TP11	A8	U40-2	-0.525V	.03226	-2.3 mV	Logic		
+ + -	+1.5V dc +0.6V dc	Signal Shi	Signal Shift = $M12 - M13$ Nominal = $\pm 1.1V$ dc	13 N	ominal -	= +1.1	IV dc						
-9.5V -10.5V	V 5V	DAC OUT	-10.0V	A9	TP16 TP19	A9	U20-12	-0.995V	11660	-3.7 mV	DAC Output, -10V	DAC ANALOG FAULT CHECK -10V OUTPUT	A9
0 + + +	+10.5V dc +9.5V dc	DAC OUT	+10.0V dc	A9	TP16 TP19	A9	U20-12	+0.987V dc	.09911	-4.1 mV	DAC Output, +10V	DAC ANALOG FAULT CHECK +10V OUTPUT	A9
+0.15V -0.15V	+0.15V dc -0.15V	FILTER TEST 2	0.0V dc	A9	U10-6 TP19	A9_	U20-14	-4.1 mV	.09911	-4.1 mV	DAC Filter	DAC ANALOG FAULT CHECK DAC FILTER	49 A
1-1-0	+1.6 mV dc -1.6 mV	+1.6 mV dc DAC OUT -1.6 mV	ob Vo.0	A9	TP16 TP19	A9	U20-2	0.0V dc	1.0	0.0V dc	DAC Output, 0V	DAC ANALOG FAULT CHECK OV OUTPUT	A9
+0.5 mV -3.5 mV	+0.5 mV dc -3.5 mV	DAC OUT	-1.5 mV dc -	A9	TP16 TP19	θ¥	.U20-2	+1.5 mV dc	1.0	0.0V dc -	DAC Output, 0V+1.5 mV dc	DAC ANALOG FAULT CHECK SECOND SWITCH	A9
<del>-</del> + +	+1.9 mV dc +1.1 mV dc		DAC Output Shift = M17	117 - Mi	εΩ	minal	Nominal = +1.5 mV dc	V dc			Checking 2nd Switch Circuit		· · ·

## Table 4-3. Analog Self-Diagnostics (cont)

SUSPECT	PCA(S)	Ţ	A7			98 A	A6	A5 A4	A7 A55					А7 А5 А4	A7 A5 A4	A7 A5 A4 A5 A4 A4
FRONT PANEL	ERROR MESSAGE(S)		PRE-AMP ANALOG FAULT CHECK INTCAL CONFIG			SAMPLE STRING FAULT CHECK 10V INTCAL	SAMPLE STRING FAULT CHECK 20V INTCAL	OUTPUT BOARDS FAULT CHECK ZERO AMP	P-AMP/OUT BRDS FAULT CHECK 10V/20V RANGE					P/AMP/OUT BRDS FAULT CHECK -10V OUTPUT	P/AMP/OUT BHDS FAULT CHECK -10V OUTPUT P-AMP/OUT BRDS FAULT CHECK STANDBY CONFIG	P/AMP/OUT BHDS FAULT CHECK -10V OUTPUT P-AMP/OUT BRDS FAULT CHECK STANDBY CONFIG OUTPUT BOARDS FAULT CHECK 2V RANGE
CIRCUIT	TESTED		INTCAL Conf DAC Out = 0V	DAC OUT = +1.5 mV dc		10V INTCAL	20V INTCAL	Zero Amp. input shorted	+10V Range, oV Out.	+10V Range, 0V +5 mV Out.	+10V Range, +10V Out.	+20V Range. +20V Out.		-10V Range, -10V Out.	-10V Range, -10V Out. Standby	-10V Range, -10V Out. Standby +2V Range, +.2V Out.
	OFFSET'		0.0V dc	0.0V dc		0.0V dc	0.0V dc	0.0V dc	0.0V dc	0.0V dc	0.0V dc	0.0V dc	004.40		0.0V dc	0.0V dc
-	GAIN		59.03	59.03		595.6	595.6	100.1	100.1	100.1	.040	.020	.040		.040	.040 .02434
Ç	INPUT <sup>2</sup>		0.0V dc	88.5 mV dc	= +1.5 mV dc	0.0V dc	0.0V dc	0.0V dc	0.0V dc	+0.50V dc	+0.40V dc	+0.40V dc	- 0.40V		0.0V dc	
MUX			U18-12	U18-12		U18-15	U18-15	U25-15	U25-15	U25-15	U25-13	U25-13	U25-13		U25-13	
	1		Å7	A7	Nominal	A7	A7	A5	A.5	AS	42 42	1 A5	t A5		A5	A5 A5
SIGNAL			TP6 TP4	TP6 TP4	19 - M20	TP6 TP4	TP6 TP4	TP10 TP11	TP10 TP11	TP10 TP11	5440AOutpu Terminals	5440AOutput Terminals	5440AOutput Terminals		TP2 TP11	
ы З		5	A7	A7	N N	A7	¥7	A4	A4	A4	5440 Tern	5440 Tern	5440 Tern		¥4	
MEASURED	NOM.	VALUE	0.0V dc °	+1.5 mV dc °	Output Shift	0.0V dc <sup>9</sup>	0.0V dc %	0.0V dc	0.0V dc	+5.0V dc	+10.0V dc 5440AOutput Terminals	+20.0V dc	-10.0V		0.0V dc	0.0V dc +20.0V dc
MEAS	MNEM- N	ONIC	PREAMP	PREAMP OUT	PRE-AMP Output Shift = M19	PREAMP	PREAMP	SDPZC (Zero Amp Outi	SDPZC (Zero Amp Out)	SDPZC (ZeroAmp out)	(5440A (Output)	(5440A Outhuth	(5440A Output)	+		
	LIMITS		+2.4 mV do PREAMP -2.4 mV OUT	+1.25 mV	+1.7 mV dc +1.3 mV dc	+1.6 mV dc PREAMP -1.6 mV dc PREAMP	T 8	8	+2.1 mV dc -2.1 mV	+7.5 mV dc SDPZC +2.5mV dc (Zero Amp out)	+10.3V dc +9.7V dc	+20.6V dc +10.4V dc	-9.7V -10.3V		+15 mV dc -15 mV	+15 mV dc -15 mV +21.0V dc +19.0V dc
	N/C		M19	M20	5	M21	M22	M23	M24	M25	MI26	M27	M28		RZW	W30

Table 4-3. Analog Self-Diagnostics (cont)

.



A5 A4 A6
OUTPUT BOARDS FAULT CHECK .2V RANGE P.AMP/S.STRING FAILT
HV INTCAL P. AMP/S
.020 0.0V dc
+0.40V .020 dc +0.40V .020 dc
U25-13 +0.4 U25-13 +0.4 U25-13 +0.4 dc
A5 U25-13
5440A Sutput Terminals
+20.0V dc 5- +20.0V dc 0 +20.0V dc 1
. ୦୮ ଅ ୦୮ ଅ ଏ
-1.6 mV OUT +20.6V dc (5440A +19.4V dc Output) +20.6V dc (5440A

# Table 4-3. Analog Self-Diagnostics (cont)

		Table 4-3. Analog Self-Diagnostics (cont)
SUSPECT	feitra	
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CIRCUIT	TESTEU	TES: The second IC or TP location is the reference used for the measurement. The second IC or TP location is the reference used for the measurement. The second IC or TP location is the reference used for the measurement. Represents the amount of signal gain from the signals source (MEASURED SIGNAL) are at a DIFFET figure is the voltage difference between RCOM while many of the signals measured (MEASURED SIGNAL) are at a DFFSET figure is the voltage difference between RCOM and the common used by the MESURED SIGNAL) are at a DFFSET figure is the voltage difference between RCOM and the common used by the MESURED SIGNAL) are at DFFSET figure is the voltage difference between RCOM and the common used by the MESURED SIGNAL. The problemace common). Nominal velue varies from one instrument to the next. For MT it is between -9.3V to -12.8V. For C2 it is between -12. This signal is an 83 Hz square wave with a <i>p</i> -plevel that is between the values measured for M8 and M1. The avera the signal is an 83 Hz square wave with a <i>p</i> -plevel that is between the values measured for M8 and M1. The avera This signal is an 83 Hz square wave with a <i>p</i> -plevel that is between the values measured for M8 and M1. The avera the LMITS and the V01MAL VLLE (MESURAL) of this signal are referenced to the input of the preamp. The masured directly. Instead the output of the preamp and divide the reading by 595. This is the voltage referenced to the input of the Zero Amp and cannot be measured directly. Instead the output of the masured directly. This addited by 100. This signal has a 0.5V p-p ripple on it. Nominal value for a stabilized oven terme.
OFFSET'		N) + OFFSET. SMAL, NOMIN Basured (MEA, ad by the MEA mount of curr asured for M6 asured for M6 reamp and d preamp and d treatly. h
GAIN		ement. ALUE)(GAI (SURED SI e signals m ommon use a the value of the value signal are re thour of the not be measi
A/D		the measu OMINAL V OMINAL V ource (ME) and the c between th between th thu jot this sure the ou p and can
MUX LOCATION	PCA IC/TPI PCA IC PIN #	<ul> <li>The second IC or TP location is the reference used for the measurement.</li> <li>The second IC or TP location is the reference used for the measurement.</li> <li>AJD INPUT (nominal value) = (MEASURED SIGNAL, NOMINAL VALUE)(GAIM) + OFFSET.</li> <li>Represents the amount of signal gain from the signals source (MEASURED SIGNAL, NOMINAL VALUE) (GAIM) + OFFSET figure is the values of the values of the values of the values the values of the values the values of the values of the values and the values of the values of the values of the presented to the values the values of the presented to the values the values of the presented to the values the values of the presented to the output of the presented to the neasured the neasured to the neasured the output of the preamp and do the relation of the output of the preamp and the rational has a 0.5V p-p ripple on it.</li> <li>'This signal has a 0.5V p-p ripple on it.</li> </ul>
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1 MITS		NOTES: AID AID AID AID AID AID AID AID
(	) È	

# Table 4-3, Analog Self-Diagnostics (cont)
4-16

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- 6. Set A14S2 to 1 (closed).
- 7. Set the 5440B/5442A POWER switch to ON.

#### NOTE

Be sure to replace U1 and reset S1 to 0 (open) before reinstalling the pca.

#### CAUTION

Do not use an oscilloscope or meter with a grounded input for measurements inside the 5440B/5442A. If either the (FC) or (FH) power supplies are inadvertently shorted to S COM, damage to the A9 REF/DAC Analog PCA will occur and F25 and F26 pico fuses on the A11 Guarded Transformer Termination PCA will open.

#### **MODULE FAULT ISOLATION**

The following procedures are intended to aid in diagnosing faults to a modular level when Self Diagnostics are insufficient for this task.

#### **Analog Modules**

Modular fault isolation procedures for analog circuits are provided by a troubleshooting tree and associated procedures. The Analog Troubleshooting Tree should be used after the Self Diagnostics have been performed for the following reasons.

ŞWI	гсн з	SETTI	NGS	
S1-1 d4	S1-2 d5	\$1-3 d6	\$1-4 d7	TEST AND TEST FUNCTION DESCRIPTION
0	0	0	0	The ASCII character ENQ (05 HEX) is continuously sent to the UART on the Guard Crossing PCA, provided that the status signal GRDY is true (active high).
0	0	0	.0	RS-232 output data test. Data is sent continuously to the RS-232 interface port on the I/O PCA provided that the status line DTR is true (active high). DTR can be set high by connecting the status line to DSR.
0	0	ţ	0	No test. Main microprocessor continuously updates the watchdog circuit.
0	0	1	1	Memory and fault indicators (LEDs) test. Memory ROM is read from and memory RAM is written to. Fault indicators are sequentially activated.
0	1	0	0	Front panel communications test. ASCII character ENQ (05 HEX) is sent continuously to the UART on the Front Panel Controller PCA, provided that status line FINT is true (active high).
0	1	0	1	IEEE-488 interface test. 5440A is configured as an IEEE-488 talker only. Assuming that a listener device is present, a message is continuously sent.
• 0	1	1	0	No test. Main microprocessor continuously updates the watchdog circuit.
¢	1	1	1	No test. Main microprocessor continuously updates the watchdog circuit

Table 4-4. Controller Troubleshooting Switch Settings

1. The resulting test functions assumes that S1-1 was closed during power-up."

2. 0 = switch closed, 1 = switch open.

- The Self Diagnostics may have difficulties isolating a fault to a specific PCA. ÷
- Self Diagnostics circuitry itself may be at fault. ٠

The Analog Troubleshooting Tree is contained in Figure 4-1. To use this tree, perform the following steps:

- 1. Remove the top cover and guard shield from the instrument.
- Set the 5440B/5442A POWER switch to ON. 2.
- 3. Verify that no power supply fault indicators are turned on.
- 4. Connect a 6-1/2 digit DMM to the output terminals of the unit (DIVIDER OUTPUT terminals for outputs under 2.2V).
- 5. Start with the top-most block in Figure 4-1. Perform the instruction contained within the block, and follow the appropriate prompt to the next block until the specific malfunctioning PCA is found. (Refer to the Overall Analog Diagram in Section 7 to aid in diagnosis.)

SWITCH SETTINGS				
S1-1 d4	\$1-2 d5	S1-3 d6	S1-4 d7	TEST AND TEST FUNCTION DESCRIPTION
0	0	0	0	Front panel display test. Checks all data and address lines to the seven segment and dot matrix displays by sending test patterns. Keyboard annunciators are blinked.
0	0	0	1	No specific test performed.
0	0	1	0	Storage module interface test. Data is continuously sent to the storage module interface and the EEROM control circuits are switched on and off. (3.)
0	0	1	1	Keyboard test. The keyboard switches are read. A digit, representing the pressed key, is displayed on the 16-segment display and the column is displayed by the missing cursor under a digit.
0	1	0	0	Main control logic communications test. The ASCII character, ACK, is continuously sent to the front panel interface circuit, when status line RINT is true (active high).
0	1	0	1	Data/Address bus test. Front panel ROM is read and the RAM is written to
0	1	1	0	No specific test performed.
0	1	1	1	No specific test performed.
NOT	L ES:	1	1	

Table 4-5. Front Panel Controller Troubleshooting Switch Settings

1. The resulting test functions assumes that S1-1 was closed during power-up.

2. 0 = switch closed, 1 = switch open.

3. To prevent the loss of previously stored front panel test set-ups, remove the Storage Module before performing this test.



Figure 4-1. Analog Troubleshooting Tree

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#### HV Loop Troubleshooting Procedure

4-18

The following procedure aids in troubleshooting faults in the high voltage output circuit of the 5440B/5442A. Diagnosing faults within this circuit is difficult because of the interaction and number of pca's involved. Special test equipment for this procedure is listed in Table 4-6.

The two general types of problems caused by the high voltage output loop are:

- Output over/undervoltage or output overcurrent.
- Unstable output voltages above 22V (but not below).

This generalization provides a logical division in the HV Loop Troubleshooting Procedure.

REQUIRED EQUIPMENT	REQUIRED SPECIFICATIONS	RECOMMENDED TEST EQUIPMENT
DMM	6½-digit	Fluke 8500 Series
DMM	3½-digit	Fluke 70 Series
Oscilloscope	30 MHz, X10 probe	
PCA Extender	5440 analog/digital extender	P/N 608281
DC Power Supply	0 - 0.44V dc, ±1%	
		· · · · · · · · · · · · · · · · · · ·

#### Table 4-6. HV Loop Troubleshooting Test Equipment

#### OVERRIDING THE OUTPUT MONITOR

### 4-19

The output monitoring feature of the 5440B/5442A places the unit in Standby within a few seconds of detecting an output deviation of  $\pm 5\%$  from the programmed voltage. However, a few seconds delay, before Standby is engaged, allows time to take critical readings without having to defeat the output monitor trip function. The output monitor feature can be disabled when it is necessary to examine the fault that caused the malfunction. The following procedure describes how to override the output monitor feature for troubleshooting.

Use the following procedure to override the output monitor feature of the 5440B/5442A:

- 1. Connect the DC Power Supply (see Table 4-6 for recommended type) to the Output/HV Control PCA as follows: Lo to TP5 (SCOM) and High to TP13 (SDPOV).
- 2. Adjust the DC Power Supply to 0.44V for a full-scale output or to a value less than this that is proportional to the programmed output level.

#### NOTE

Unless otherwise specified, all measurements in this procedure are referenced to SCOM, A4TP5 or the OUTPUT LO front panel terminal post (which are at the same potential).

#### OVER/UNDERVOLTAGE OR OVERCURRENT PROBLEMS

If the output voltage varies significantly from the programmed value, the voltages within the loop should be "against the rail" (amplifiers operating near the level of their supply voltage). Perform the following steps to verify this condition:

- 1. Program a voltage between 23V and 1100V, using the lowest voltage that displays an overvoltage problem.
- 2. Measure the voltage at A5TP6 (OPCOM). If the loop is functioning correctly at this point, the voltage should be approximately 4V dc to 5V dc. This reading should increase 1.4 mV for an increase in output voltage of 1V between 23V and 1100V. The polarity of the voltage at A5TP6 is the same as the output voltage polarity.

#### WARNING

#### TO AVOID ELECTRICAL SHOCK HAZARD, BE AWARE THAT LETHAL VOLTAGES MAY EXIST ON THE EXPOSED PCAS AND CHASSIS PARTS REGARDLESS OF THE PROGRAMMED OUTPUT VOLTAGE. PROBLEMS IN THE VOLTAGE SENSING OR VOLTAGE DRIVING CIRCUITRY MAY CAUSE THE OUTPUT VOLTAGE TO BE CONSIDERABLY HIGHER THAN THAT PROGRAMMED.

Note whether the voltage measured at A5TP6 is appropriate for the loop response. For example, if the output is going open loop, then, for any voltage called above 22V dc (that is any voltage on the 275V range), the output will probably rise to its limit of 700V dc before tripping the unit into standby. If the loop is open for voltages on the 1100V range (voltages above 275V dc), the output will reach about 1160V before tripping. If these conditions exist, the voltage at A5TP6 (OPCOM) will be approximately + 27V dc (for positive outputs) or -27V (for negative outputs).

#### OPEN LOOP PROBLEMS

#### 4-21

If the conditions of the previous procedure are met, the following steps should be performed to find where the loss of feedback occurs. Suspect the sense path relays on the Preamp PCA or on the Sample String PCA. To determine where the problem is, perform the following:

- 1. Set the 5440B/5442A POWER switch to OFF.
- 2. Place the Sample String PCA on the extender card.
- 3. Set the 5440B/5442A POWER switch to ON. Program a voltage that displays the output fault.
- 4. Measure the voltage at A6P31-1 (HVSS). If this voltage is not at the output voltage level, then the fault is most likely on the Preamp PCA (specifically K1 or the K1 driver circuit). If the HVSS voltage does parallel the output, then the fault is most likely on the Sample String PCA (specifically K4 or K5 and their associated driver circuits).

#### UNDERVOLTAGE OUTPUT PROBLEMS

#### 4-22

Malfunctions where the output is low or non-existent (for voltages on either the 275V or 1100V ranges) can occur for two reasons. Either a drive or output signal path is open, for one or both ranges, or the relay contacts are closed when they should not be (or the triacs on the

Filter B PCA are conducting when they should not be). The second type of problem may often involve an overcurrent condition that causes the unit to display the error message OUTPUT OVERCURRENT after the unit resets to Standby mode.

The following procedure is for conditions where the output is low and there is no overcurrent message:

#### NOTE

If the output is low, the voltage at A5TP6 (OPCOM) should be either 27V or -27V (polarity is the same as the polarity of the programmed output voltage). The voltage at A7TP5 (Preamp PCA) should be  $\pm 7V$  to 8V (polarity should be opposite from the programmed output voltage polarity).

- 1. Set the 5440B/5442A POWER switch to OFF.
- 2. Place the Output PCA on the extender card.
- 3. Set the 5440B/5442A POWER switch to ON. Program a voltage that displays the output fault.
- 4. Measure the voltage across A4C13 (the large tubular capacitor near the bottom-center of the pca).

#### WARNING

## TO AVOID ELECTRICAL SHOCK, BE AWARE THAT LETHAL VOLTAGES (1100V DC) MAY BE PRESENT ACROSS CAPACITOR A4C13.

- 5. The voltage measured in Step 4 should be approximately 23V higher than the programmed output. If the voltage is not approximately 23V higher, there is a fault on the Output PCA, specifically relays K1 or K2 and their associated drive signals. The relay drive signals come from the Output/HV Control PCA.
- 6. Check for proper low relay drive signals on the appropriate pins of A4P11. If the drive signals agree with the table on the first sheet of the Overall Analog Diagram (located in the schematic section of this manual), then the Output PCA is defective. If not, the Output/HV Control PCA is suspect.
- 7. If the voltage across C13 is less than the programmed output (plus 23V), then the problem is likely in the Output/HV Control PCA or the Filter B PCA. Refer to the paragraphs on Isolating Faults Between the Output/HV Control and Filter B PCAs.

The following procedure is for conditions where the output is low and there is an overcurrent message:

- 1. Set the 5440B/5442A POWER switch to OFF.
- 2. Remove all pca's from extenders and reinstall them inside the unit.
- 3. Set the oscilloscope for dc coupling and use the x10 probe.
- 4. Connect the oscilloscope to A5TP3 (VC) and the common on A5TP9.

- 5. Connect the DMM to A5TP3 and the low terminal on A5TP9.
- 6. Set the 5440B/5442A POWER switch to ON. Program a voltage that displays the output fault.
- 7. Examine the signal on the oscilloscope. The normal signal is a clean, zero-centered square wave, with rise time under 1 microsecond and symmetry within 10% of 50% duty cycle. The normal p-p amplitude varies between 4V p-p for an output of 23V to 80V p-p for an output of 1000V.
- 8. Examine the reading on the DMM. The dc voltage should be less than 0.1V for all output levels above 23V dc.
- 9. If the waveform in Step 5 is less than 80V p-p and A5TP6 is an extreme, then the problem is most likely on the HV/Output Control PCA. If the waveform is the expected level then the problem is either on the HV/Output Control PCA or the Filter B PCA. If the problem is not traceable at this point, refer to the next procedure to isolate the fault between the two pca's.

#### ISOLATING FAULTS BETWEEN THE OUTPUT/HV CONTROL AND FILTER B PCS 4-23

As shown on the second sheet of the Overall Analog Diagram (the HV Control Circuit diagram), the HV/Output Control PCA provides the control signals (TS1 through TS4) for the triacs. These signals turn on the triacs that in turn provide dc voltages at A13TP1 (+TSV) and A13TP3 (-TSV) according to the output voltage programmed. The voltages at A13TP1 and A13TP3 for the corresponding programmed output are listed in Table 4-7.

The following steps will help isolate faults between the Output/HV Control and Filter B PCAs:

- 1. Set the 5440B/5442A POWER switch to ON.
- 2. Program a voltage that displays the output fault.
- 3. Measure the voltage at A13TP1 and A13TP3 with respect to A13TP2 and compare the results to the voltages listed in Table 4-7 for the indicated range.
- 4. If the voltages in Step 2 are within limits, then the fault is with the Filter B PCA. If the voltages do not meet the requirements, proceed to Step 5.
- 5. Perform the following:
  - a. Set the 5440B/5442A POWER switch to OFF.
  - b. Place the HV/Output Control PCA on the extender.
- c. Set the 5440B/5442A POWER switch to ON.
  - d. Measure the TS signals on the P21 connecter (refer to the schematic). If the signals are correct, then the Filter B PCA is at fault. If not then HV/Output Control PCA is at fault.

		VOLTAGES AT				
		A13TP1	A13TP3			
TS1 TS2 TS3 TS4	23V - 275V 276V - 550V 551V - 875V 876V - 1100V	$40V \pm 15V$ $40V \pm 10V$ $55V \pm 10V$ $70V \pm 10V$	40V ± 15V 40V ± 10V 55V ± 10V 70V ± 10V			

#### Table 4-7. Triac Drive Voltages

#### OTHER HIGH OUTPUT PROBLEMS

Another possible problem occurs when a programmed output is too high, and the feedback loop closes but the output is still too high (and at source voltage). This problem occurs because the drive signal is stuck high at some point in the loop. To troubleshoot this problem, follow the procedure used in troubleshooting for a low output with the following exceptions: the control signals should be trying to reduce the output, and expected control signal conditions should be reversed where applicable.

#### OUTPUT OVERCURRENT FAULTS

As mentioned before, loop faults that point to an overcurrent condition when there is no load connected to the instrument, are probably caused by an incorrect relay closure.

#### NOTE

If an overcurrent condition is present on the 22V range and below, the problem is most likely on the Output PCA and caused by shorted output transistors.

Perform the following steps to determine if the incorrect relay closure is on the Preamp PCA or the Sample String PCA:

- 1. Place the Preamp PCA on the extender.
- 2. Using the DMM, measure the feedback signal on sense lines HVSS through 20VSC.
- 3. The relation of these signals to each range is shown on the Overall Analog Diagram. Use the values shown on the Overall Analog Diagram in conjunction with the Preamp PCA schematic to determine if an incorrect relay is closed.

#### UNSTABLE OUTPUTS

Unstable outputs on either the 275V or the 1100V ranges (but not the lower ranges) will usually result from one of two sources: either the relays on the Output PCA, Sample String PCA, and Preamp PCA, or (especially when both ranges are involved) the high voltage loop control circuits (as shown on the third sheet of the Overall Analog Diagram). Because of the nature of feedback, propagating around the loop, it may be necessary to break the loop before the fault is found. If the fault is caused by severe problems on the Output/HV Control PCA or Filter B PCA, then the Undervoltage Output procedures should be adequate in isolating the problem without breaking the loop. The loop will usually compensate for output variations up to  $\pm$  5V. If the output is within this range, the problem is probably not with the Output/HV Control PCA or the Filter B PCA.

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4-25

4-26

#### 4-30

Use the following procedure to break the high voltage control loop, when doing so is necessary for troubleshooting:

- 1. Set the 5440B/5442A POWER switch to OFF.
- 2. Remove the Preamp PCA.
- 3. Set A14S3 (the ACK switch on the Guard Crossing PCA) to 1 (open). This prevents the unit from tripping due to no response from the missing Preamp PCA.
- 4. Connect the power supply between A4TP13 (HI) and A4TP5 (SCOM).
- 5. Set the supply to 0.4V dc  $\pm 1\%$ .
- 6. Connect another power supply between A4TP2 (OPCOM HI) and A4TP5 (SCOM).
- 7. Set the second power supply to 4V dc.
- 8. Set the 5440B/5442A POWER switch to ON, set OUTPUT STATE to OPR.
- 9. Program an output for 250V dc. After a minute or so the output voltage should begin to approach its final value. After three or four minutes the output should be stable within  $\pm 1V$ .
- 10. Small adjustments to the 4V dc supply should bring the output closer to 250V dc. The loop will probably compensate for  $\pm$  5V variations. If not, the problem is probably not in the Output/HV Control PCA or the Filter B PCA.

#### **Digital Modules**

4-27

The following procedures are intended to aid in diagnosing a communication fault between the front panel microprocessor and the main microprocessor.

FRONT PANEL/MAIN MICROPROCESSOR COMMUNICATION FAULT ISOLATION 4-28

This procedure should be used when there is a conflict between what appears on the alphanumeric display and the fault indicators on the Front Panel PCA (top center LED) and Controller PCA (FPC LED). The message FRONT PANEL RUNNING appears on the alphanumeric display while the two fault indicators are turned on. This problem occurs because the self diagnostics cannot isolate the fault.

To isolate the problem, perform the following steps:

#### NOTE

It is assumed that the top cover and guard shield have been removed from the instrument. Otherwise, the fault indicators would not be visible.

- 1. Set the 5440B/5442A POWER switch to OFF.
- 2. Place the Controller PCA on the extender card.
- 3. Set troubleshooting switch \$1 to 0.
- 4. Set the 5440B/5442A POWER switch to ON.

- 5. Set the troubleshooting switches on the Controller PCA to 0010.
- 6. Using a dc-coupled oscilloscope, verify that logic pulses are present at P80-24 (\$0) and P80-25 (\$0).
- 7. Using a dc-coupled oscilloscope, verify that there is logic activity on P80-2 (FINT) and P80-22 (FINT)

If there is activity on the pins in Step 6, but not on the pins of Step 7, then the problem is probably on the Front Panel Controller. If there is activity on the pins of Step 7 and not on the pins of Step 6, then the problem is probably on the Controller PCA. If the conditions for Steps 6 and 7 are met, proceed to the Front Panel Link Test.

#### FRONT PANEL LINK TEST

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- 1. Set the 5440B/5442A POWER switch to OFF.
- 2. Replace the Controller PCA on the motherboard.
- 3. Remove the bottom cover from the 5440B/5442A. (This allows access to the front panel.)
- 4. Remove the front panel as follows:
  - a. Remove the Program Storage Module (if present).
  - b. Remove the four screws located directly behind the front handles.
  - c. Lift away the front panel and place it on top of the instrument. Be careful not to stress the interconnect cable.
- 5. On the Front Panel Controller PCA, set the troubleshooting switches to 0100.
- 6. Set the 5440B/5442A POWER switch to ON.
- 7. Set the troubleshooting switches on the Controller PCA to 0010.
- 8. Using a dc-coupled oscilloscope, verify that logic pulses are present at P80-24 (S0) and P80-25 (S0).
- 9. Using a dc-coupled oscilloscope, verify that there is logic activity on P80-2 (FINT) and P80-22 (FINT).

If there is activity on the pins in Step 6, but not on the pins of Step 7, then the problem is probably on the Controller PCA. If there is activity on the pins of Step 7 and not on the pins of Step 6, then the problem is probably on the Front Panel Controller.

#### NOTE

The assembly-at-fault conclusions from this test are opposite from those in the previous procedure (Front Panel/Main Microprocessor Communication Fault Isolation).

#### NOTE

Before returning the unit to normal operation, set the 5440B/5442A POWER switch to OFF and return all troubleshooting switches to 1.

# Section 5 List of Replaceable Parts

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A15 Memory PCA		5-46	5-16	5-47
A16 Controller PCA		5-48	5-17	5-49
A17 Outside Guard Regulator PCA		5-50	5-18	5-51
A18 I/O PCA		5-52	5-19	5-53
A19 Outside Guard Terminator PCA		5-54	5-20	5-55
A20 Power Switch PCA		5-56	5-21	5-57
A22 Display PCA		5-58	5-22	5-59
A23 I/O Connector PCA	5-23	5-60	5-23	5-60

### INTRODUCTION

This section contains an illustrated listing of replaceable parts for the 5440B/AF Direct Voltage Calibrator. Ordering procedures for parts and a cross-reference to federal supply codes are also provided in this section. Both mechanical and electrical components are listed by reference designators. Each assembly is accompanied by an illustration showing the location of each part and its reference designation.

### PARTS ORDERING INFORMATION

Electrical components may be ordered directly from the manufacturer by using the manufacturer's part number, or from the John Fluke Mfg. Co., Inc. and its authorized representatives by using the part number under the heading FLUKE STOCK NO.

To ensure prompt delivery of the correct part, include the following information:

- 1. Fluke Stock Number.
- 2. Description (as given under the DESCRIPTION heading).
- 3. Reference Designator.
- 4. Quantity.
- 5. Part Number and Revision Level of Component's PCA.

Parts price information is available from the John Fluke Mfg. Co., Inc. or its representatives.

#### CAUTION

#### DEVICES INDICATED BY THE ABOVE SYMBOL ARE SUBJECT TO DAMAGE BY STATIC DISCHARGE

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#### TABLE 5-1. 54408/AF FINAL ASSEMBLY (See Figure 5-1.)

REFERENC: DESIGNAT	E OR 105>	SDESCRIPTION	FLUKE STOCK	MFRS SFLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	QTY	Q6
A 1		* KEYBOARD ASSEMBLY	803932	87536	803932	1 1	
A 2 A 3		A MULARDADA DECA	(7(30) Laraty	87536 87536	797357 608059	í	
н э А 4		<ul> <li>KEYBOARD ASSEMBLY</li> <li>FRONT FANEL CONTROLLER PCA</li> <li>MOTHEREDARD FCA</li> <li>OUTPUT FCA</li> <li>OUTPUT FCA</li> <li>SAMPLE STRING FCA</li> <li>PREAME FCA</li> <li>REF/DAC DIGITAL PCA</li> <li>REF/DAC ANALOG FCA</li> <li>INSIDE REGULATOR PCA</li> <li>GUARDED TRANSFORMER TERMINATION FCA</li> </ul>	797316	87536	797373	t	
A 5		* OUTPUT/HV CONTROL PCA	653618	89536	608182	1	
A 6		* SAMPLE STRING PCA	653626	87556	608190	i,	
A 7		* PREAMP PCA	653634	89536	608208	1	
A 8 A 9		* REF/DAC DIGITAL PCA	704177 457440	89536 89536	609784 608232	1	
A 9 A 10		<pre>x REF_2DH2, HNMEDG FCH i INSIDE REGULATOR PCA % GUARDED TRANSFORMER TERMINATION PCA % FILTER &amp; PCA % GUARD CROSSING PCA % GUARD CROSSING PCA % OUTSIDE GUARD REGULATOR PCA % OUTSIDE GUARD TERMINATOR PCA % OUTSIDE GUARD TERMINATOR PCA % DUSFLAY PCA % DISPLAY PCA % I/O CONNECTOR PCA WHISPER VENTURI ROTRON #271016 CAP,OIL,1UF,+=10Z.1.5KV CAP.CER.0.005UF,+=20Z.3000V,Z5U CAP,CER.0.005UF,+=20Z.3000V,Z5U CAP.CER.0.005UF,+=10Z.100V CAP.CER.0.005UF,+=10Z.100V CAP.CER.0.0047UF,+=10Z.100V CAP.AL,34000UF.+100=10Z.15V JUMPER,LINK,BINDING POST FUSE.1/4 X 1-1/4,FAST.2A,250V % CREW, MACH,PHP,STL,0=32X3/8 % CREW,MACH,PHP,STL,0=32X3/8 % CREW,MACH,PHP,STL,0=32X3/16 % CREW,MACH,PHP,STL,0=32X3/16 % CREW,MACH,PHP,STL,0=32X3/16 % CREW,MACH,PHP,STL,0=32X3/16 % CREW,MACH,PHP,STL,0=32X5/16 % CREW</pre>	653659	89536	608257	1	
A 11		* GUARDED TRANSFORMER TERMINATION PCA	608075	87556	408075	í	
A 12		* FILTER A PCA	653568	87556	608083	1	
A 13		* FILTER & PCA	653576	87536	608071	1	
A 14		* GUARD CROSSING PCA	603667 75074A	87208	611707 748533		
A 15 A 16		* MEMORY PCA	748464	89536	748335	, i	
A 17		* OUTSIDE GUARD REGULATOR PCA	767152	89536	767103	1	
A 18		# 1/0 PCA	758730	89536	748376	í	
A 19		* OUTSIDE GUARD TERMINATOR PCA	758797	89536	758797	f	
A 20		* POWER SWITCH PCA	608067	87556	608067	1	
A 22		* DISPLAY PCA	767160	87536	767111	}	
A 23		* I/O CONNECTOR PCA	803757	87030 69977	803957 WR2A1-027117	1	
B 1 B 2		WHISPER VERIORI Dotdom #374044	422535	87877	271016	į	
	2	CAP.011.119.4~107.1.5KV	247023	56289	264970	2	
	4	CAP, CER, 0, 005UF, +202, 3000V, 25U	188003	71590	2DDH6R502M	Ż	
C 5		CAP, CER. 0. 0047UF, +-10%, 500V. Z5R	106724	71590	CF-472	1	
C 6		CAF. POLYCA, 0.47UF, +-10%, 100V	288860	84411		1	
<u> </u>		CAF, AL, 34000UF. +100-10%. 15V	423533	56289	36DX343G015AF2B	1	
E 1 F 1		SUMPER, LINK, BINDING FUSI Surg 1/4 y 1.4/4 East 36 350V	170720	00000V 89534	21171 109173	i	
F 1 H 1		YONEW MACH PHP YTL A-3081/2004	152140	89536	152140	8	
H 2		SCREW, MACH, FHP, STL, 8-32 X 7/16	396159	89536	306159	6	
н з		SCREW, CAP, SCKT, STL, 8-32X3/8	295105	89536	295105	4	
H 4		SCREW, MACH, PHP, STL. 6-32X5/8	152181	87536	152181	2	
н ş		SCREW, MACH, PHP, STL, 6-32X5/16	152157	89536	152157	4 i	
<u>H</u> 6		SCREW, THD FORM, FHP, S.STL, 6-20X1/2	176172	87538	176172 682112		
И 7 Н 8		YAN AUU,FILIEK,AL W/FUAM,4.079W Yangu maru kup shi 9-39 y 7/1a	306159	89536	306139	10	
н 8 Н 9		SCREW, MGG, MM, STC, STL, SCR 7, 10	295105	89536	275105	4	
H 10		SCREW, MACH, PHP, STL, 6-32X5/16	152157	89536	152157	4	
H 11		NUT.STL.CAP EXT LW.6-32X7/64	152819	89536	152819	2	
H 12		NUT, MACH, HEX, STL, 10-32	110536	89536	110536	2 2	
H 13		SCREW, MACH, PHP, SIL, 6-32X5716 SCREW, MACH, PHP, SIL, 6-32X5716	102107	87336 90436	152157 228890	4	
H 14 H 15		SCREW,MHCH,FRF,GTG,GTGAAA773 SCREW MARM PHP.STL.A-32X5/16	152157	89536	152157	18	
Н 16		SCREW, THD FORM, PHP, S.STL.8-18X1/2	306233	89536	306233	18	
H 17		SCREW, MACH, PHP, STL, 4-40X1/4	129890	73734	19022	9	
H 18		WASHER, LOCK, INTRNL, STEEL. 48	110320	89536	1 1 9320	.8	
H 19		SCREW, MACH, PHP, STL, 6-32X3/8	152165 320093	87536	152165	13	
H 20		SCREW, MACH, PHP, STL, 6-32X3/8 SCREW, MACH, PHUP, S. STL, 6-32X1/9	222404	89536 83058	320093 PC97476	ទេ	
H 21 H 22		NUT. NYLON, PUSH-IN SCREW,MACH,PHP.STL.8-32X3/8	114124	89536	114124	16	
H 23		SCREW, MACH, FHUP, S. STL, 8-32X1/4	320101	89536	320101	4	
H 24		SCREW, MACH, PHP, STL, 6-32X3/8	152165	89536	152165	4	
H 25		SCREW, MACH, FHUP, S. STL, 6-32X1/4	320093	89536	320093	8	
H 26		SCREW, MACH, PHP SEMS, STL. 6-32X1/2	177030	89536	177030	4	
H 27		SCREW, MACH, PHP. STL. 6-32X5/16	152157	89536	152157	2 4	
H 28 H 29		SCREW, MACH, PHP, STL, 6-32X1/2 SEREW, MACH, FHUP, S.STL, 6-32X1/4	152173 320093	89536 89536	152173 320093	8	
H 29 H 30		SCREW, MACH, FHF, S.STL, 4-40X1/4	320077	89536	320077	2	
		SCREW, MACH, PHP, STL, 6-32X3/8	152165	89536	152165	12	
н эл		SCREW, MACH, PHP, STL. 6-32X5/16	152157	89536	152157	4	
H 31 H 32		SCREW, MACH, PHP, STL, 8-32X1/2	159749	89536	159749	6	
H 32 H 33			659243	89536	659243	2	
H 32 H 33 MP 1		DECAL, FRONT CORNER			151100	7	
H 32 H 33 MP 1 MP 2		CORNER HANDLE, FRONT 8,75 INCH	656199	89536	656199 751982	2 1	
H 32 H 33 MP 1 MP 2 MP 3		CORNER HANDLE, FRONT 8.75 INCH Keybrd Bracket, Left	656199 751982	89536 89536	751982	2 1 1	
H 32 H 33 MP 1 MP 2 MP 3 MP 4		CORNER HANDLE, FRONT 8.75 INCH Keybrd Bracket, Left Keybrd Bracket, Right	656199 751982 751990	89536 89536 89536		t	
H 32 H 33 MP 1 MP 2 MP 3 MP 4 MP 5		CORNER HANDLE, FRONT 8.75 INCH Keybrd Bracket, Left Keybrd Bracket, Right Front Panel Painted	656199 751982 751980 738781 738757	89536 89536	751982 751990	1 1 1	
H 32 H 33 MP 1 MP 2 MP 3 MP 4 MP 5 MP 7		CORNER HANDLE, FRONT 8.75 INCH Keybrd Bracket, Left Keybrd Bracket, Right	656199 751982 751990 738781 738757 629154	89536 89536 89536 89536 89536 89536	751982 751990 738781 738757 629154	1 1 1 1	
H 32 H 33 MP 1 MP 2 MP 3 MP 4 MP 5 MP 5 MP 7 MP 8		CORNER HANDLE, FRONT 8.75 INCH Keybrd Bracket, left Keybrd Bracket, right Front Panel Painted Keyboard Decal Nameplate, fluke Decal-Pwr-Switch	656199 751982 751990 738781 738757 629154 634766	89536 89536 89536 89536 89536 89536 89536	751982 751990 738781 738757 629154 634766	1 1 1 1 1	
H 32 H 33 MP 1 MP 2 MP 3 MP 4 MP 5 MP 7		CORNER HANDLE, FRONT 8.75 INCH Keybrd Bracket, Left Keybrd Bracket, Right Front Panel Painted Keyboard Decal Nameplate, fluke	656199 751982 751990 738781 738757 629154	89536 89536 89536 89536 89536 89536	751982 751990 738781 738757 629154	1 1 1 1	

TABLE 5-1.	5440B/AF	FINAL	ASSEMBLY
(SEC FIGURE	5-1.)		

		(SEE FIGURE S-1.)						21
REF DES A−>	ERENCE IGNATOR NUMERICS>	<pre>SDESCRIFTION</pre>	FLUKE STOCK ND	MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	101 QTY	R 2 Q-	א 0 ד -E
MP	1;	REAR-PANEL	582544	89536	582544	í		
MP	12	REAR CORNER BRACKET	606186	89536	606186	2		
MP	13	CORNER HANDLE, FRONT 8.75 INCH	656199	89536	656199	2		
MP	14	DECAL, REAR CORNER	685180	89536	685180	2		
MP	15	FILTER-ERAME	582734	89536	582734	1		
MP	16	MTG DUTPUT CAP	613679	89536	613679	. i		
MP	17	NAMEPLATE, SERIAL -REAR PANEL~	472795	89536	472795	1		
MP	18	LEET-CHASSIS-SIDE	582551	89536	582551	1		
MP	19	BINDING POST FLATE	582809	89536	582809	1		
MP	20	GUIDE.CARD.PCB.6-1/2 X .312 X .125	526009	89556	326009	31		
MP	21	RIGHT-CHASSIS-SIDE	582569	89536	582569	1		
MP	22	BOTTOM-GUARD-COVER	582700	89536	582700	í		
MF	27	BODE FLUG, FOLYETHELENE, E/S/16 HOLE	187799	89534	197799	10		
MP	74	OUTRUT-PANEL-DECAL	604967	82536	404967	1		
MP	75	BINDING-POST-ASSY-SR-GRN	637868	89536	437868	1		
MP	24	RINDING TO STUDY TO STUDY	637876	89534	637976	1		
MP	27	RINDING FORT ACTION DEC	A37892	89536	437892	3		
MP	20	STADIAG COT MANY OF NEW STADIAG SCOTTASSY ACCESSIN	437900	89534	637900	3		
MP	20	TNNED-FMASSIS FORT AT AND	453507	80536	453527	4		
MP	30	REAR-BULKIES CONT	A53535	89534	452535	÷		
MP	21	CRRMMET RUBBER	501593	83330	91119	÷		
MP	30	MTC ONTPUT CAP	413479	RESTA	A13479			
MP	77	RATTOM-COVER	582585	89534	382585	ŝ		
MP	34	STOT, STALLE BALL TYPE (DARK DARER)	453923	89534	453923	4		
MP	प्रमद	KEY-TOP-PUR-SU	640334	89536	640334	í		
Μŕ	36	CABLE TIE.4" .0.100"W.0.75 DIA	172080	89534	172080	Å		
MP	37	TOP-CUARD-COVER	582692	89536	587492	÷		
MP	307 3243	TOP REAR COVER	749596	89574	749594			
MP	20	TAR-COVER	587577	99534	582577	, 1		
ń۴.	40	101 000000	421776	89536	421776	10		
MF	44	ΕΕΑΕ ΗΟΠΑΙΝΟ ΜΙΟ ΟΝΤΈΠΤ	803945	89536	803945	1		
MP	47)	STDE TETAWDAT	524012	42700	524012	2	5	
MP	74	CHV6616 61 DE 24	200070	00554	320012	í		
ME	40	CAO DACK O 7744 CON	491576	07530	207072 A04576	2		
MP	44	EAR RACK O 374 FRW SAAAD/SAADA VED SUICIN	750040	07.330	7500()	4		
TM		CETTING CIADTER CLIDE	750044	07030	750044	1		
тм	2	SAAA VEGIEV ADEBATADU MAMUAL	751074	07330	754044			
TM	4	SAAG DEMOTE DOCCOMMINE CUIDE	757004	07000	757004	1		
111	3	SARADZAS VEDUTCE MANUAL	102000	07330	004005	1		
una Nu	-7	JAAVDIAL SERVICE HENDEL (AV) ELACTYLEEADLENTELEAD	604000	07000	480500	1		
ω W	-	СНОДСТВОЗУТКЕНАТОРГОТТОРГОНС Солит антонт сао саріс Ассу	217004	07000	217004	1		
พ ม		TROAT VUITUT CHE CHDEE HAAT Pood itme d/a s…is/tee 7…ioaue sve	74740+	07230	7674	1		
w	0	CONDICINE, MAR DELOY TECHONOGISYI	000401	07030	202401	,		
		RINDING-FOST-ASSY-RK-BLU RINDING-FOST-ASSY-CF-RED RINDING-FOST-ASSY-CF-RED RINDING-FOST-ASSY REAR-RULKHEAD-ASSY GROMMET. RUBBER MTG OUTPUT CAP ROTTOM-COVER FOOT. SINGLE BALL TYPE (DARK UMBER) KEY-TOP-FWR-SW CABLE TIE,4*L,0.100*W,0.75 DIA TOP-GUARD-COVER TOP REAR COVER TOP-COVER DORCAS REAR HOUSING W/O OUTPUT SIDE TRIM-24* CHASSIS SLIDE. 24 EAR RACK 8 3/4* FRW S440B/5442A VFD SHIELD GETTING STARTED GUIDE S440 SERIES OPERATORS MANUAL 5440 REMOTE PROGRAMMING GUIDE S440B/AF SERVICE MANUAL CABLE-ASSY CORD,LINE,R/A 5-15/IEC,3-18AWG.SVT S440B/AF RECOMMENDED SPARE PARTS KIT	812289					

NOTE 1 = FOR 230V LINE. ORDER P/N 109272 1A SLOW BLOW.



Figure 5-1. Final Assembly







Figure 5-1. Final Assembly (cont)



Figure 5-1. Final Assembly (cont)



Figure 5-1. Final Assembly (cont)

YABLE 5-2. AY KEYBUARD ASSEMBLY (see Figure 5-2.)

	\$	FLOKE STOCK NOmin	MERS SPU 7 CODE -	MARUFACTURERS PARI NUMBER 	(01 Q14	R 5 -Q	0 { 
. 1- 5	CAP, CER, 0.220F, 4-20%, 50V, ZSU	519157		RFE111250224M30V	5	1	
	* LED,RED,LIGHT BAR,PCB MOUNT	534834	28480	HLMP 2300	2	1	
	* LED, YELLOW, RECTANGULAR, PCB MOUNT	650648	873.56	650648	5		
CR 2- 6	SCREW, MACH, FHUP, S.SIL. 6-33X1/4	320093	89536	320093	3		
1 1	SOCKET, 1 ROW, PWB, 0.100CTR, 4 POS	681957	87536	481957	7		
) 17 16° 1	SWITCH-COVER-LEFT	651026	89536	651026	1		
ም 1 የድ 2	2MILCH-COACK-WIDDFE	651934	89536	551034	1		
11° 4 11° 3- 6	SPACER, SWAGED, RND, BRASS, 4-32X0.375	494542	89536	494542	3		
11° 3	SWITCH-COVER-RIGHT	651042	89536	551042	1		
1P 4	LABEL, ADHENIVE, PCB, 0.375X1.0	807032	89536	807032	1		
1F \$	KEY-TOP-RESET	639963	89536	639963	1		
11: 5			89536	059971	1		
1P 7	KEY-TOP-11	639989	89536	639989	1		
1, F 8	KEY-T0P-"2"	639997	89536	639997	1		
,. ነም ፡	KEY-TOP-131	640003	89536	640003	1		
112 10	KEY-TUP-"4"	640011	89536	640011	1		
1P 11	KEY-TOP-151	640029	89536	640029	1		
1P 12	ΚĖΥ-ΤΟ₽- <b>*</b> 6"	640037	89536	640037	1		
1P 13	KEY-TOP-*7*	440045 4	89536	440045	1		
119 14	KEY-T0P-18"	640052	89536	640052	1		
1P 15	KEY-TOP- 9	440060	89536	\$40050 	!		
1P 16	KEY-TOP-, ~	640078	89536	640078	1		
18 17	KEYTOP+/-	640086	89536	640086	1		
MP 19	KEY-TOP-M	640094	89536	640094	1		
1P 19	KEY-TOP-ARROW	640102	89536	640102	4		
HP 20	KEY-TOP-CLEAR~(NQ)	640128	89536	640128	!		
1P 21	KEY-TOP-ENTER-(YES)	640136	87536	640136	1		
YP 22	KEY-TOP-CHNG-SIGN	640144	89556	640144	1		
1P 23	KEY-TOP-R-CALL-REF	640151	87536	640151			
MP 24	大市人	640169	89536	640169			
1P 25	KEY-TOP-OPR/STBY	640177		540177			
1P 26	KEA-LOB-SEMSE	640185	89536	640185	1		- N
4P 27	KEY-TOP-DIV	640193	89536	640193	4		
4P 28	KEY-TOP-GUARD	640201	89336	640201			
1F 27	KEY-TOP-LIMITS	640250	89536	640250	4		
1P 30	KEY-TOP-LIST KEY-TOP-LIST KEY-TOP-SVCE KEY-TOP-SVCE	640268	89536	640268	ļ,		
1P 31	KEY-TOP-SVCE	340284	89536	649284			
1P 32	KEY-TOP-LIST	640292	89536	640292			
1P 33	KEY-TOP-BOOST	\$49276	89536	640276	3		
MP 34	KEY-TOP-BLANK	640326	89536	640326	14	7	
1P 35	SPACER L.E.D	541284		541284	1	•	
° 3	CABLE ASSY, FLAT. 24 COND, 10.0, DIP CONN	460815	89536	460816 2N3904	ź		
2 1-7	* TRANSISTOR, SI, NEN, SMALL SIGNAL	218396	04713	CR251-4-5P8K2	7	1	
R 1 7	RES, CF, 8.2K, +-5%, 0.25W	441675	80031	513473	34	,	
S 1-5,8-	SWITCH, PUSHBUTTON, SPST KEYBOARD	513473 513473	89534	513473			
5 17, 20- 24.							
5 27-29,31-		513473					
5 39, 41, 42	our to a cuchadur to at coor somethic $AeV$	743161	87536	743161	1		
5 40	SWITCH, FUSHBUTTON, SPST, MOMENTARY	408393	02735	CD4071FE	, i		
U 1	* IC.CMOS,QUAD 2 INPUT OR GATE		12040	MM74C173N	2	1	
ປ ຊ. ຊັ	* IC.CMOS.QUAD D LATCH.+EDG TRG,W/RESET	412(42	12040	MM80C97N	2	1	
U 4.5	# IC.CMOS.HEX BUFFER W/3-STATE OUTPUT CONTENT TO ON DIV	376236	91506	324-AG390	1		
XP 3 Z 1	SOCKET,IC.24 PIN Res.net.dip.16 pin.8 res.1k.+-5%	358119	01121	314	1		
			17 1 T 10		\$		





Figure 5-2. A1 Keyboard Assembly

TABLE 5-3. A2 FRONT PANEL CONTROLLER PCA (SEE FIGURE 5-3.)

	(SEE FIGURE 5-3.)							-
REFERENCE Designator A->Numerics>	S	FLUKE Stock NO	HFRS SPLY Code-	MANUFACTURERS Part Number Or Generic Type	TOT QTY		N 0 -E	
C 1-3	CAP, CER, 220PF, +-22, 100V, COG	512111 519157	51406	RPE121	3			
C 4, 5, 13 C 42, 51 53 C 6 8	CAP.AL.47UF.+~20%.10V	519157 613984	89536	613984	3			
Č 9	CAP, AL, 15UF, +-20%, 35V	614024	89536 72982	614024 5835-000Y5-U103Z	1			
C 9 C 44 C 45	CAP, CER, 0.010P, #80#207, 237, 130 CAP, POLYES, 0.001UF, #~107, 50V	720938	89536	720938	į			
C 46	CAP, POLYES, 0.0010F, +102, 50V CAP, POLYES, 4700FF, +52, 50V CAP, POLYES, 0.010F, +102, 50V	739987	89536 89536	739987 715037	1 2			
CR 1, 2	* ZENER, UNCOMP, 6V TRANSIENT SUPPRESSOR	208922	24444	115908	2	1		
CR 3 DS 1	* DIGDE,SI, 100 PIV, 1.0 AMP * LED,RED,PCB MOUNT,LUM INT=2.0MCD	343491 534859		1N4002 HLMP3301/5082-4655	1	ł		
E 1-6	PIN, SINGLE, PWB, 0.025 SQ				6			
J 1, 4 R 1-3, 5	PIN, SINGLE, PWB, 0.025 SQ HEADER, 1 ROW, 0.100CTR, 10 PIN RES, CF, 100, +5X, 0.25W RES, CF, 160, +5X, 0.25W RES, CF, 200, +5X, 0.25W RES, CF, 51, +5X, 0.25W RES, MF, 154K, +-1X, 0.125W, 100PPM RES, MF, 192K, +1X, 0.125W, 100PPM RES, MF, 121K, +1X, 0.125W, 100PPM RES, MF, 121K, +1X, 0.125W, 100PPM SWITCH, MODULE, SPST, DIP, 4 F0S	478693	87536 80031	478693 CR251-4-5P100E	4			
R 4	RES, CF, 1K, 4-5%, 0.25W	343426	80031	CR251-4-5P1K	1			
R 6 R 7	RES,CF,200,+~5%,0.25W RES,CF,51,+~5%,0.25W	41451	80031 80031	CR251-4-5P200E CR251-4-5P51E	1			
R 17	RES, MF, 154K, +-12, 0.125W, 100PPM	289447	91637	CMF551543F	1			
R 18 R 21	RES,MF,182K,+~1%,0.125W,100PPM RES MF 42 7K,+~1%,0.125W,100PPM	241091	87538 91637	241091 CMF554222F	1			
R 22	RES, MF, 121K, 4-17, 0.125W, 100FPM	229369	89536	229369	1			
ያ 1 ፑድ 1 14	SWITCH, MODULE, SPST, DIP, 4 PDS TERM, FASTON, TAB, SOLDR, 0, 110 WIDE	408559	00779	435166~2 62395	14			
UÍ	* IC,LSTTL,QUAD RS422 LINE RCVR,3-STATE	525303	12040	DS3486N MC3487F	1	í		
U 2 U 3,54	* IC,LSTTL,QUAD DIFFERENTIAL LINE DRVR * IC,TTL,QUAD 2 INPUT AND GATE		04713 01295		2	í		
U 4 <sup>°</sup>	* IC.CMOS,QUAD 2 INFUT OR GATE	408393	027 <b>35</b>	CD4071BE	1	í		
U 5 U 6	* IC.CMOS,UNIV ASYNC RECEIVR/TRANSMITER * IC.CMOS,QUAD 2 INPUT NOR GATE	355172	02735	1M6402CPL CD4001AE	i	1		
U 7	OSCILLATOR SMHZ. TTL CLOCK		09969		1	1		
() 8 () 9	* IC,CMOS,DUAL DIV BY 16 BINARY CNTR * IC,CMOS,14STAGE RIPPLE CARRY BIN CNTR	741488 394486		741488 CD4020AE	i	1		
U 10,12	# IC,TTL,HEX BUFFER W/OPEN COLLECTOR	418236	01295	SN7407N CD4049AE	2 1	t t		
U 11 U 13	<pre>w IC,CMOS,HEX INVERTER * IC,CMOS,DUAL D F/F,+EDG TRG W/SETARST</pre>	381848 536433			1	÷		
U 14, 19	# IC, CMOS, NEX BUFFER W/3-STATE OUTPUT	407759		MM80C97N MK3880-4CPU	2 1	1		
U 15 U 16-18	* IC,NMOS,8 BIT MICROCOMPUTER * IC,LSTTL,3-8 LINE DCDR W/ENABLE	478073 407585		SN74LS138N	3	i		
U 20, 21	* IC, 2K X 8 STAT RAM	584144 751867		uPD4016C-2 751867	2	1		
U 22 U 23	* FRONT EPROM 0 BUILD DWG * IC,LSTTL.OCTL BUS TRNSCVR W/3~ST OUT			SN74LS245N	í	į		
U 24~ 26	<pre>w IC,CMOS,HEX BUFFER # IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR</pre>	381830	02735	CD4050AE SN74LS273N	3 1	1		
	* IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	2	Ì		
U 39, 49, 63	* IC,DUAL DIV BY 16 BINARY COUNTER * IC,LSTTL,HEX BUFFER W/3-STATE OUTPUT	483578 536458	01295 01295		32	1		
U 40,41 U 42,43,59,	* IC,256 X 4 STAT RAM ,3-STATE OUT	429860		· · · · · · · · · · · · · · · · · · ·	4	Ē.		
U 60	# * FRONT DOT MATRIX CHAR BUILD DWG	429860 751883	87536	751883	í	1		
U 44 U 45,62	* IC,LSTTL, BBIT SER/PAR-IN, SER-OUT SHFT	495671	01295	SN74LS166N	2	1		
U 46	* IC,16R6 LOG ARRAY,5440B-99204 * IC,16R8 LOG ARRAY,5440B-99206	751950 751875	89536 89536	751958	1	r I		
U 47 U 48,65	<pre># IC,16R8 LOG ARRAY,5440B-99206 # IC,LSTTL,8BIT ADDRSABLE LATCH,W/CLR</pre>	419242	01295	SN74LS259N	2	1		
U 50, 67	* IC,LSTTL,RETRG MONOSTAB MULTIVB W/CLR	404186 393058	01295	SN74LS123N SN74LS04N	2	1		
U 53,66 U 55	# IC,LSTTL,HEX INVERTER # IC,LSTTL,TRIPLE 3 INPUT AND GATE	393082	04713	SN74LS11N	1	1		
U 56	# IC, CMOS, DUAL SYNC BINRY UP CNTR	355164 478347	04713	MC14520BCP SN74LS241N	1	1		
U 57 U 58	* IC,LSTTL.OCTL LINE DRVR W/3-ST OUT * IC,CMOS,DUAL 4 INPUT NOR GATE	363820	01295 02735	CD4002AE	į.	i		
Ū 61	* FRONT 14-SEG CHAR BUILD DWG	751891	89536	751891 751941	f 1	1		
U 64 U 68	* IC,16R8 LOG ARRAY,5440B~99202 * IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	751941 393124	87536 01275	SN74LS74N	i	- i		
XE 1, 4	JUMPER, REC, 2 POS, . 100CTR, .025 SQ POST	530253	00079	530153-2 NTL RADB-109	2			
XU 5,15 XU 8	SOCKET,IC,40 PIN Socket,IC,14 PIN	429282 276527	09922 09922	DIL840F-108 DIL88P-108	ŝ			
XU 20, 21, 44, XU 61	SOCKET, IC, 24 PIN	376236 376236	91506	324-AC39D	5		1 1	
XU 22	SOCKET, IC, 28 PIN	448217	91506	328-AG39D DILB20F-108	1			
XU 46,47,64 Z 1,2	SOCKET,IC,20 PIN Res,Net,Sif,10 Pin,9 Res,4.7K,+-2%	454421 484063	09922 80031	95081002CL	2	1		
Z 3~ 5, 12~	RES, NET, SIP, 8 PIN, 7 RES, 10K, +-2%	412924		95081002CL	7			
Z 15 Z 6	RES,NET,DIP.14 PIN.8 RES.33,+-5%	412924 413575	01121	314	1			

#### TABLE 5-6. A5 OUTPUT/HV CONTROL PCA (SEE FIGURE 5-6.)

	(SEE FIGURE S-6.)						
REFERENCE DESIGNATOR A->NUMERICS>	S DESCRIPTION	FLUKE STOCK	MFRS SPLY CODE-	OR GENERIC TYPE	TOT QTY	R 5 -Q	0 T E
	RES, CF, 470, +-57, 0.25W	343434	80031	CR251-4-5P470E 62395	3 10		
TP 1" 3, 6" TP 12	TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889 512889	45000	62373	10		
Uİ	* IC, BPLR, TIMER, 8 PIN DIP	402610	18324	LM555CN	1		
U 2	* IC, OP AMP, DUAL, COMPENSATED, 8 PIN DIP	414284	12040	LM1458N	1	1	
ป 3	* IC, OP AMP, DUAL, JEET INPUT, 8 PIN DIP		02735	CA082E	í	1	
U 7,31-34	* IC, TTL, DUAL NAND DRVR W/OPEN COLLECT	329706	01295	SN75452P	5	1	
U 20	* IC, CMOS, HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	1	1	
U 21-23	* IC, CMOS, HEX BUFFER	381830	02735	CD4050AE	3	1	
U 24, 26	* IC.CMOS,QUAD D F/F,+EDG TRG,W/CLR	452912	12040	MM74C175N	2	1	
U 25	* IC, CMOS, 8-1 LINE MUX/DEMUX ANALOG SW	452805	02735	CD4051BE	1	1	
Ü 27	# IC.LSTTL.3-8 LINE DCDR W/ENABLE		01295	SN74LS13BN	1	1	
U 28, 29	* IC,LSTTL, OCTAL D F/F, +EDG TRG, W/CLEAR	454892	01295	SN74LS273N	2	1	
บ 30	* IC.TTL.HEX INVERTER W/OPEN COLLECTOR		01295	SN7406N	1	t	
U 35	* IC,CMOS,8 INPUT NAND GATE	504860	04713	MC140688CP	1	1	
Ŭ 36,37	* IC, CHOS, QUAD 2 INPUT NOR GATE	355172	02735	ED4001AE	2	1	
u 3a	* IC,LSTTL,QUAD BUS DFR W/3-STATE OUT	472746	01295	SN74LS125N	1	1	
VR 1, 5, 6	# ZENER, UNCOMP, 20.0V, 5%, 23.0MA, 1.0W	2769B0	12969	UZ8712	3	3	
VR 2	* ZENER, UNCOMP, 3.3V, 10%, 20.0MA, 0.4W		04713	1N746	1	1	
VR 7	# ZENER, UNCOMP, 6.8V, 5Z, 37.0MA, 1.0W		12969	UZ8706	ŧ	1	
XU 25	SOCKET, IC, 16 PIN	276535	91506	316-AG39D	1		
Z 1- 3	RES.NET.DIP.14 PIN.7 RES.1K.+-5%		01121	314	ż		
ž 5	RES, NET, SIP, 10 PIN, 9 RES, 4.7K, +-2%	484063	80031	95081002CL	1		
	RES, NET, DIP, 16 PIN.8 RES, 240, +-54	424457	01121	314	1		
Z 6 Z 7	RES, NET, DIP, 16 PIN, 8 RES, 470, +-5%	501239		314	1		
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Figure 5-3. A2 Front Panel Controller

#### TABLE 5-4. A3 MOTHERBOARD PCA (See Figure 5-4.)

				(SEE FIGURE 5-4.)						М
DES A->I		108 2108-	>	S	FLUKE STOCK NO	MFRS SPLY CODE-		тот QTY		0 T
Ċ	2			CAP. CER. 1000PF. +-20%, 3000V, 250	105635	56289		1		
č	3			CAP, POLYES, 0, 1UF, +-20%, 250V AC	542233	55112		1	1	
FL	ī.	2		FILTER, LINE, 115V/3A, 230V/3A, PNL MNT	321273	05245	3EF2	1		
Η.	1			SCREW, MACH, PHP, STL, 6-32X5/16	152157	89536	152157	2		
Ĥ	2			NUT, MACH, HEX, STL, 6-32	119551	89536		1		
й	3			NUT, MACH, HEX, BR, 1/4-28	110619	89536	119619	i		
н	4			SCREW, MACH, FHP, STL, 4-40X3/0	276709	87536	276709	2		
Ň	5				110635	89536	110635	2		
3	2			CONN.PWD EDGE, REC, 0.150 CTR, 22 POS	459883	00777		1		
Ē		7.	f Ø		422550	00779	2-583407-0	27		
Ĵ		20,			422550					
Ĵ		53,			422550					
Ē		70			422550					
Ĵ		83			422550					
J	86.	90.	71		422550					
J	8	1 - 1		CONN, PWB, EDGE, REC, 0.150 CTR, 24 POS	295352	00779	583650-9	1		
J	30,	31,	40,	CONN, PWB EDGE, REC. 0.150 CTR, 6 POS	291708	91662	6398-006-313-001	28		
Ĵ	41				291708					
Ĺ.	1			OUT-PUT-CHOKE-ASSY	637835	89536	637835	1		
MP	1			LINE-CORD-BRACKET	582650	89536	582650	1		
MF'	2			HLDR, FUSE, 1/4 X 1-1/4, LOPROFILE, PNLMT		89536		1		
MP	3			CABLE TIE, 4"L, 0.100"W, 0.75 DIA	172080	89336	172080	7	í	
Ŕ	í.	2		RES.CF.1H.+-5%.0.25W	348987	80031	CR251-4-5P1M	2		
R	З,	4		RES, MF, 1M, +1%, 1W, 100PPM	177188	89536	177188	2		
Ř	5			RES, CF, 10, +-52, 0, 25W	340075	80031	CR251-4-5P10E	1		
RJ	۹.	2		VARISTOR, 22V, +-20%, 1.0MA	500777	03508		2		
RΥ	3			VARISTOR, 430V, 20%, 1.0MA	519355	07214	V275LA15AS14K275	1		
ω	1			HOST-CABLE ASSY	617886	89536	617886	1		
W	2			FAN-CABLE	629188	87536	629188	1		
W	3			POWER-CABLE	608570		608570	1		
W	4			REAR-OUTPUT	608576	39536	608596	1		
ų.	5			MAINS-CABLE-ASSY	653543	89536	653543	1		

.





Figure 5-4. A3 Motherboard PCA

#### TABLE 5-5. A4 OUTPUT PCA (See figure 5-5.)

FERENCE	(SEE FIGURE 5-5.)	FLUKE	MFRS	MANUFACTURERS		Ŕ	N Ö
SIGNATOR.	SDESCRIPTION	STOCK NO	SPLY CODÉ	PART NUMBER 			т Е
1, 2 3, 5, 16,	CAP,CER,0.22UF,+-20%,50V,25U CAP,CER,0.22UF,+-20%,50V,25U	309849 519157	71590		2 6		
26, 36, 37 4	CAP,FOLYCA,0.47UF,+-10%,100V	519157 288860	84411	X463UW	1		
6,7	CAP, AL, 47UF, +50-20%, 16V	436006		SM/VB	2		
a	CAP, CER, 33PF, +-2%, 100V, COG	513226		RFE121	1		
9	CAP, POLYES, 0.33UF, +-20%, 2000V	423301		X675HV	1		
10- 12	CAF, CER, 330PF, +-5%, 100V, COG	528620 528539		RPE121	3		
13 14, 15	CAP,CER,1000PF,+-5%,50V,CUG Cap,Ta,15UF,+-20%,20V	519686		RPE113 1960156X0020KE4	ż		
38	CAF, POLYES, 10F, +-10%, 100V	447847			í		
39, 40	ELECTRO, MIN,LO LÉAK, 4.7MF, 35V	603993		603993	2		
41, 42 43, 44	CAP,AL,100UF,+50-20%,35V CAP,AL,2.2UF,+-20%,50V	416982 614875		SM/VB 614875	2 2		
45, 46	CAP, AL, 100UF, +50-20%, 100V	641225		641225	2		
1-10,12-	* DIODE, SI, BV= 75.0V, ID=150MA, 500 MW	203323	07910	1N4448	22		
20, 22- 24	*	203323		150/57			
1 2	SCREW, MACH, PHP, STL, 6-32X5/16 SCREW, MACH, PHP, STL, 4-40X5/16	152157		152157 152116	4		
1, 8	RELAY, ARMATURE, 4 FORM C, 4.5VDC	519405		AZ431-E-5551-2	ź		
2, 5, 6	RELAY, ARMATURE, 6 FORM C, 4.5VDC	602953			3		
3, 7, 9,	RELAY,ARMATURE,2 FORM C,4.5VDC	514240	26806	AZ-420-12-203	4		
10 11	RELAY,REED,1 FORM A,4.5VDC	514240 424408	21317	PA111085-5	1		
11 1− 4	CHOKE, ATURN	320911	89536	320911	4		
1	ISOLATOR-RESISTOR-SET	650697 641852 641860 606095 613687	89536	650697	1		
2 3	RESISTOR-SET-COVER	641852	89536	641852	1		
3 4	RESISTOR-SET-BACK OUTPUT-SHIELÐ	641860 484895	87336 80576	641860 606095			
5	HEATSINK-OUTPUT	613687	89536	613687	2		
6	HEATSINK-OUTPUT SLEEV, TEFLON, 0.027ID, NATURAL E HECTOR POR 1/14IN NOM	196717	89536	196717			
7	ESECTOR/FOB/17 TOTRI NON	494724			2		
9 9	MOUSETAIL,\$2829-75-3,HOLE SIZE .046 Spacer,Swaged,RND,Brass,6-32X0.100	352021	89536 89536	422873 352021	4		
íó	SPACER, SWAGED, RND, BRASS, 4-40X0.625	347526		347526	Ą		
í	* TRANSISTOR, SI, NPN, SMALL SIGNAL	218396	04713	2N3904	1	1	
2 3	* TRANSISTOR, SI, PNP, SMALL SIGNAL	195974		2N3906	1	1	
	* TRANSISTOR,SI,BV=325V, 200,TO-66 * Transistor,SI,BV=300V, 200,TO-66	190710	04713	2N3739 2N6425	ł	4	
4 1	* TRANSISTOR, SI, PNP, SMALL SIGNAL		04713		i	Í	
2	* TRANSISTOR, SI, NPN, SMALL SIGNAL	218081		MP\$6520	1	1	
23	* TRANSISTOR, SI, N-JFET, TO-92, SWITCH		15818 91637	U2366J CMF551741F	2	1	
1, 2 3, 4	RES,MF,1.74K,+-1%,0.125W,100PPH RES,MF,1.37K,+-1%,0.125W,100PPM	448241		CMF55	2		
5, 6	RES, MF, 6.49K, +-12, 0.125W, 100PPM		91637	CMF556491F	2		
7, 8	RES.MF, 52.3, +-1%, 0.5W, 100PPM	155069		155069	2 2		
9,10 11	RES, MF, 10K, +-1%, 0.125W, 100PPM RES, MF, 20K, +-0.1%, 0.125W, 25PPM	168260 340420	91637	CMF551002F CMF55			
2	RES, MF, 50K, +-0.12, 0.125W, 25PPM	340257		CMF5550028	i		
13, 14	RES, MF, 2M, +-12, 0.5W, 100PPM	217760	91637	CMF651-2-1P2L	2		
15, 16	RES, MF, 1M, +-1%, 0, 125W, 100PPM	268797	91637	CMF551004F	2 1		
17- 24 25	RESISTOR SET RES,MF,665K,+-1%,0.125W,100PPM	638015 375980	89536 91637	638015 CMF55	i		
26, 27	RES, MF, 100K, +-0.12, 0.125W, 25PPM	340166	91637	CMF551003B	2		
28	RES, MF, 9.31K, +-12, 0.125W, 100PPM	379040	91637	CMF55	۲.	- t	
29	RES, MF, 5.11K, +-1%, 0.125W, 100PPM	294868	91637	CMF555111F	1		
30 32	RES, MF, 2K, +-0.1%, 0.125W, 25PPM RES, CF, 51, +-5%, 0.25W	340174 414540	91637 80031	CMF552001B CR251-4-5P51E	i		
33, 45	RES, HF, 200K, +-1%, 0.125W, 100PPM	261701	91637	CMF552003F	2		
34	RES, MF, 4.99K, +-12, 0.125W, 100PPM	148252	91637	MFF1-84991	1		
35, 38 74	RES,CF,2K,+~5%,0.25W RES,CF,1K,+~5%,0.25W	441469 343426	80031 80031	CR251-4-5P2K CR251-4-5P1K	2		
36 37	RES, MF, 2K, +-12, 0.5W, 100PPM	151266	91637	CMF552001F	Ť		
40- 43	RES, CF, 1, 6M, +-5%, 0.25W	442566	80031	CR-25	4		
44	RES, MF, 18.2K, +-14, 0.125W, 100PPM	236810	91637	CMF55	5		
46 81	RES,MF,2K,+-1%,0.125W,100PPM RES,MF,1K,+-1%,0.125W,100PPM	235226 168229	91637 91637	CMF552001F CMF551001F	ł		
82	RES,CF,100,+-57,0.125W	348771	80031	CR251-4-5P100E	1		
83, 84	RES, CF, 10, +-5%, 0.25W	340075	80031	CR251-4-5P10E	2		
0.ff	RES, MF, 100K, +-1%, 0.125W, 100PPM	248807	91637 91637	CMF551003F	1		
85			710.57	CMF55			
86	RES.MF.11K.+-12.0.125W,100PPM RES.CE.10K.+-57.0.25W	293621 348839			2		
	RES,MF,11K,+-1X,0.125W,100PPM RES,CF,10K,+-5X,0.25W RES,CF,100K,+-5X,0.25W	348839 348920	80031 80031	CR251-4-5P10K CR251-4-5P100K	2 2 12		

DÉSI	EREN( IGNA1	TÓR	>	s	DESCRIPTION	FLUKE Stock NO	MFRS SPLY Code-	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	8 2 Q-	ر 1 1
	,										
FP 1	13				ter and a large transformer and and terms and an	512889	<b></b>	(AE 350			
ΓP –					SOCKET, SINGLE, PWB, FOR 0.080 FIN	170480	74970	105-752	!		
J	1				IC, OP AMP, GEN PURPOSE, TO-78 METAL CAN	288928	12040	LH308AH	1	1	
	9				IC, OP AMP, LO-OFFSET VOLTAGE, LO-NOISE	605980	06665	0P-07DP	1	_	
٧R	1			* Z	ENER, UNCOMP, 75.5V, 10%, 33.0MA, 10.0W	604058	04713	1 N3002AR	1	5	
VR	2			¥ 2,	ZENER, UNCOMP, 75.0V, 10%, 33.0MA, 10.0W	604041	04713	1N3002A	1	1	
/R	4,	5		×Ζ	ENER, UNCOMP, 3.3V, 10X, 20.0MA, 0.4W	309799	04713	1N746	2	1	
/R	6.	7			ENER, UNCOMP, 6.8V, 5%, 37.0MA, 1.0W		12969	UZ9706	2	í	
VR	8,	9			ENER, COMP, 6.4V, 2%, 2 PPM TC, 1.0MA		01537	SZG20287	2	í	
VR	10,	-			ENER, UNCOMP, 20.0V, 5%, 6.2MA, 0.4W	180463	04713	19688	2	Í.	
ĸĸ	ĩ	8			RELAY SOCKET, & POLE	281253	77342	27E348	ŝ	•	
ĸκ	- 11	ĕ			RELAY SOCKET, ACCESSORY, SPRING, & POLE	417188	89536	417188	5		
X K	3,	-	9,		ELAY SOCKET, ACCESSORY, SPRING, 2 POLE	376459	77342	200249	ă		
ĸĸ	10	6.1	7,	0	NERT BOUNDIJHUUSDOUNIJOENINGJE FULS	376459	11076	****71	-		
		7	~	-	CLAX SOCKET O DOLE		33340	075501	~		
KK	3,	6	9,	h	KELAY SOCKET,2 POLE	376665	(1542	275501	4		
KK.	10			_		376665					
κU	1				NOCKET,IC,TÓ-99,8 PIN,CIRCULAR	408450	89536	408450	1		
ΧU	9			S	SOCKET,IC,8 PIN	478016	91506	308-AG39D	1		

#### TABLE 5-5. A4 OUTPUT PCA (See Figure 5-5.)



Figure 5-5, A4 Output PCA

## TABLE 5-6. AS OUTPUT/HV CONTROL PCA (SEE FIGURE 5-6.)

	(SEE FIGURE 5-6.)					
EFERENCE		FLUKE Stock	MFRS SPly	MANUFACTURERS PART NUMBER	TOT	R S
ESIGNATOR ->NUMERICS>	S DESCRIPTION	NO	CODE-	OR GENERIC TYPE	QTY	Q -
					1	
1	CAP.PDLYES.0.01UF,+-10%,400V CAP.CER.0.01UF,+80-20%,25V,Y5U CAP.CER.0.1UF,+80-20%,25V,Y5K CAP.AL,100UF,+75-10%,16V CAP.AL,6.8UF,+-20%,16V CAP.AL,60UF,+75-10%,15V,NON-POLAR CAP.CEP.27EF,+-27%,100V,COE	402818	70000	E235-000Y5-114077	÷	
2	CAP, CER, 0.010F, +80-202, 25V, 150	332(86	74500	14-E0-407		
3	CAP, CER, 0.10F, +80-20Z, 25V, 15K	307177	11390	01-20-103	-	
4	CAP, AL, 100UF, +75-107, 16V	436914	02043	3L ((7007	1 1 1	
6	CAP, AL, 6.80F, +-297, 16V	013772	87336	013772 700		
7	CAP, AL, 100UF, +75-102, 15V, NUN-PULAK	124714	56287	RPE121	÷	
8, 13	CHELGENIZIFFITTAAIIVVIJOUG	362749 528620	21,120		2 1	
9	CAM, GER, 330FF, +-34, 1987, LOG		51406	71941	į	
10	CAP, PULTES, 0.10F, 4~102, 100V	393439		8121-A100-W5R-102M	_	
11, 12, 21		402966 422576		1960157X0020TA1	ĩ	
		603993		603793	Á	
17, 18, 22,	ELECTRO, MIN, LO SEMRY HIMME, JOY	603993	07500	000,70	•	
23	PAR AL 4000F +50-707 351	416982	62643	2H/AB	2	
24, 25		148924	72982		2	
26, 27	CAP, CER, 0.22UF, +-20%, 50V, Z5U	519157	51406		40	
51- 68, 83-	CMF, CER, 01220F, 7-208, 300, 230	519157	2.700			
100,112-115	CAP, AL, 47UF, +-20%, 10V	613984	89536	613984	3	
71-76,81,	CAP, CER, 470FF, +-20%, 100V, X7R	358275	72982		8	
82	Chi (CER, HIVIT) · EVALIVATIATA	358275		•••••		
101-111	CAP, CER, 0.01UF, +-20%, 100V, %7R	407361	72982	8121-A100-W5R-103M	11	
( 1- 7, 9,	* DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323		1N4448	11	í
10, 13, 14	*	203323				
15, 16	* DIBDE,SI, 100 PIV, 1.0 AMP	343491	01295	1N4002	2	
1	SCREW, MACH, PHP, STL., 6-32X5/16	152157	89536	152157	4	
i	SOCKET, SINGLE, PWB, FOR 0.018-0.040 PIN		00779	390598-2	4	
1-13	CHOKE, STURN	320911	89536	320911	13	
• •	SPACER, SWAGED, RND, BRASS, 6-32X0.100	352021	89536	352021	4	
2	EJECTOR, PCB, 1/16IN. NOM	494724	32559	CP-66		
> 3	HEATSINK, PCB MOUNT	309930	13103	CP-66 6001811 U3422J	2	
1, 13, 14		370072	15918	U3422J	3	1
2-4,6		370684	04713	MPS A 42	4	1
5. 10. 11.	* TRANSISTOR, SI, PNP, SMALL SIGNAL	195974	64713	2N3906	4	í
16	#	195974				
	* TRANSISTOR, SI, BV=325V, 20W, TO-66	190710	04713	2N3739	1	1
7 8 15	* TRANSISTOR, SI, BV=300V, 20W, TO-66	586784	04713	2N6425	1	1
15	# TRANSISTOR, SI, NPN, SMALL SIGNAL	218396	04713		í	1
1	RES,MF,30.9K,+-12,0.125W,100PPM	235275			1	
2	RES,MF,68.1K,+-12,0.125W,100PPM	236828	91637		1	
3		267880		190PC103B	1	1
4, 8,10,	RES,CF,10K,+-5Z,0.25W	348839	80031	CR251-4-5P10K	11	
14, 15, 71,		348839				
72, 90, 92-		348839				
94		348839	01477	0865514796	1	
5	RES, MF, 14, 7K, +-12, 0.125W, 100PPM	220229		CMF551472F CP251-4-5015K	2	
7,36	RES.EF.15K.+=3Z.Q.230	348824	00031 00031	CR251-4-5P15K CP251-4-5P329	Ĩ	
9	RES,CF,3.9K,+~5%,0.25W	3420VV	80021	CR251-4-5P3K9 CR251-4-5P1K8	2	
11, 12		441527	80031	CR251-4-5P3K	ĩ	
13	RES,CF,3K,+-5%,0.25W			HB3005	ż	
16, 17 40, 40, 25	RES,CC,30,+-5%,2W RES,CC,2K,+-5%,2W	276998		HB	4	
18, 19, 25, 24	REDJUGJERJT-JAJEW	276998	V. (	*- <del></del>		
26	RES.CC.150.+-5%.2W	235192	0f121	HB	2	
20, 21 22, 23	RES,CF,100,+-5%,0.25W	348771	80031	CR251-4-5P100E	2	
24, 23	RES,CF,2.7K,+-5%,0.25W	386490	80031	CR251-4-5P2K7	Ť	
27, 28	RES, CF, 100K, +-5%, 0.25W	348920	80031	CR251-4-5P100K	2	
27, 20	RES.CF.51K.+~5%.0.25W	376434	80031	CR251-4-5P51K	1	
30	RES.CF, 430, +-5%, 0.25W	441568	80031		1	
31	RES, CF, 1M, +-5%, 0.25W	348987	80031	CR251-4-5P1M	1	
32, 73, 76	RES, CF, 14K, +-52, 0.25W	442376	80031	CR251-4-5P16K	3	
33- 35	RES, MF, (OK, +-12, 0.125W, 100PPM	168260	91637		3	
37	RES,HF,30.1K,+-1Z,0.125W,100PPM	168286	91637		!	
38	RES, MF, 110K, +-12, 0.125W, 100PPM	234708	91637	CMF551103F	1	
38 39	RES,CC,470,+~5%,0.5W	108787	01121	EB4715	1	
40	RES,CF,6.8K,+~5%,0.25W	368761	80031	CR251-4-5P6K8	1	
61, 62, 64,	RES, CF, 1K, +-52, 0.25W	343426	80031	CR251-4-5F1K	9	
74, 75, 83,		343426				
103,105,111		343426			~	
63,104	RES,CF,2.2K,+-5%,0.25W	343400	89031		2	
	RES, CF, 10, +-5%, 0.25W	340075	80031		2	
65,66	RES,CF,2K,+-5%,0.25W	441469	80031	CR251-4-5P2K	2 5	
	ACAJO, ENJ. BRIVING					
81, 82	RES,CF,4.7K,+-5%,0.25W	348821	01121	CB4725		
81, 82		348821 442293 334110	80031	CR251-4-5P120E	í í	

#### TABLE 5-6. A5 OUTPUT/HV CONTROL PCA (SEE FIGURE 5-6.)

	(SEE FIGURE S-6.)						
REFERENCE Designator A>Numerics>	S	FLUKE STOCK	MFRS SPLY CODE-	OR GENERIC TYPE	TOT QTY	R 5 -Q	0 T E
	RES, CF, 470, +-57, 0.25W	343434	80031	CR251-4-5P470E 62395	3 10		
TP 1" 3, 6" TP 12	TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889 512889	47000	62373	10		
Uİ	* IC, BPLR, TIMER, 8 PIN DIP	402610	18324	LM555CN	1		
U 2	* IC, OP AMP, DUAL, COMPENSATED, 8 PIN DIP	414284	12040	LM1458N	1	1	
ป 3	* IC, OP AMP, DUAL, JEET INPUT, 8 PIN DIP		02735	CA082E	í	1	
U 7,31-34	* IC, TTL, DUAL NAND DRVR W/OPEN COLLECT	329706	01295	SN75452P	5	1	
U 20	* IC, CMOS, HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	1	1	
U 21-23	* IC, CMOS, HEX BUFFER	381830	02735	CD4050AE	3	1	
U 24, 26	* IC.CMOS,QUAD D F/F,+EDG TRG,W/CLR	452912	12040	MM74C175N	2	1	
U 25	* IC, CMOS, 8-1 LINE MUX/DEMUX ANALOG SW	452805	02735	CD4051BE	1	1	
Ü 27	* IC.LSTTL.3-8 LINE DCDR W/ENABLE		01295	SN74LS13BN	1	1	
U 28, 29	* IC,LSTTL, OCTAL D F/F, +EDG TRG, W/CLEAR	454892	01295	SN74LS273N	2	1	
บ 30	* IC.TTL.HEX INVERTER W/OPEN COLLECTOR		01295	SN7406N	1	t	
U 35	* IC,CMOS,8 INPUT NAND GATE	504860	04713	MC140688CP	1	1	
Ŭ 36,37	* IC, CMOS, QUAD 2 INPUT NOR GATE	355172	02735	ED4001AE	2	1	
u 3a	* IC,LSTTL,QUAD BUS DER W/3-STATE OUT	472746	01295	SN74LS125N	1	1	
VR 1, 5, 6	# ZENER, UNCOMP, 20.0V, 5%, 23.0MA, 1.0W	2769B0	12969	UZ8712	3	3	
VR 2	* ZENER, UNCOMP, 3.3V, 10%, 20.0MA, 0.4W		04713	1N746	1	1	
VR 7	# ZENER, UNCOMP, 6.8V, 5Z, 37.0MA, 1.0W		12969	UZ8706	ŧ	1	
XU 25	SOCKET, IC, 16 PIN	276535	91506	316-AG39D	1		
Z 1- 3	RES.NET.DIP.14 PIN.7 RES.1K.+-5%		01121	314	ż		
ž 5	RES, NET, SIP, 10 PIN, 9 RES, 4.7K, +-2%	484063	80031	95081002CL	1		
	RES, NET, DIP, 16 PIN.8 RES, 240, +-54	424457	01121	314	1		
Z 6 Z 7	RES, NET, DIP, (6 PIN, 8 RES, 470, +-5%	501239		314	1		
	ermenterment for matter and an ermenter for a set for a set for						





#### TABLE 5-7. A6 SAMPLE STRING PCA (SEE FIGURE 5-7.)

	(SEE FIGURE 5-7.)						-
REFERENCE DESIGNATOR A->NUMERICS>	SDESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE	MANUFACTURERS Part Number or generic type	TOT QTY	R S -Q	N 0 T E
C 1, 2, 20 C 3- 19, 24- C 35	CAP,AL,10UF,+-20%,35V CAP,CER,0.22UF,+-20%,50V,Z5U	603985 519157 519157	74840 51406	RLR RPE111Z5U224M50V	3 29	í	
Č 21, 22	CAP, CER, 100PF, +-10Z, 1000V, S3N	105593	71590	DD101	2		
C 36, 37	CAP, CER, 1000PF, +-5%, 50V, COG	528539	51406	RPE113	2		
CR 1- 9	* DICDE, SI, BV# 75.0V, IC#150MA, 500 MW	203323	07910 89536	1N4448 152173	9 4	1	
н 1 н 2	SCREW, MACH, PHP, STL, 6-32X1/2 SCREW, MACH, PHP, SISTL, 6-32X1/4	152173 385401	87536	385401	- 7		
มี 3	SCREW, MACH, PHP, STL, 6-32X3/8	152165	89536	152165	9		
K 1~ 5, 9	RELAY, ARMATURE, 6 FORM C, 4.5VDC	602953	77342	R10-E-5874-1	6		
K 6 8	RELAY, ARMATURE, 4 FORM C, 4.5VDC	519405	26806	AZ431-E-5551-2	3		
MP 1	OVEN-COVER-S-STRING	606103		606103	1		
MP 2 MP 3	OVEN-BACK-S-STRING HEAT SINK, XISTOR THERMALLOY 6072B	604111 473686	89536 89536	406111 473686			
MP 3 MP 4	SPACER, SWAGED, RND, BRASS, 0.1501DX0.150		89536	631861	À		
MP 5	SPACER, SWAGED, RND, BRASS, 6-32X0.437	423806	89536	423896	4		
MP 6	SPACER, SWAGED, RND, BRASS, 6-32X0.100	352021	89536	352021	2		
MP 7	SPACER, HEX, NYLON, 6-32X0.500	658153		658153	4		
MP 8 MP 9	SAMPLE-STRING-OVEN-INSUL-SIDE-A Sample-String-Oven-Insul-Side-B	654608 654616	89536 89536	654608 654616	2		
MP 10	SAMPLE-STRING-OVEN-INSUL-BACK		89536		ī		
MP 11	SAMPLE-STRING-OVEN-INSUL-TOP	654632	89536		1		
MP 12	TAPE, TRANSP, POLYEST, DBL CDAT, 1*W	696542	89536	696542	_		
MP 13	SLEEV, TEFLON, 0.042ID, NATURAL	175976	89536	175976	2		
MP 14	EJECTOR, PCB, 1/16IN. NOM	494724	32559 89536	CP-66 196717	2		
MP 15 Q 1, 4	SLEEV, TEFLON, 0.027ID, NATURAL * TRANSISTOR, SI, NPN, SMALL SIGNAL	218081	04714	MPS6520	2	1	
Q 2	* TRANSISTOR, SI, BV= 70V, 90W, TO-127	325720	04713		Ť	- ÷	
Q 3	* TRANSISTOR, SI, BV= 70V, 90W, TO-127	325738	04713		1	1	
R 1- 4, 13, R 19	RES.CF.10K.+-5%.0.25W	348839 348839	80031	CR251-4-5P10K	6		
R 5 R 6,7	RES,CF,1K,+-5%,0.25W RES,MF,49.9K,+-1%,0.125W,100PPM	343426 268821	80031 91637	CR251-4-5F1K CNF554992F	2		
R 8	RES, MF, 3.09K, +-12, 0.125W, 100PPM	235150	91637	CMF55	Ť		
R 9	RES, CF, 2K, +-5%, 0.25W	441469	80031	CR251-4-5P2K	1		
R 11	RES,CC,10M,+-5%,0.25W	194944	01121	CB1065	1		
R 12,38	RES, MF, 100K, +-1%, 0.125W, 100PPM	248807	91637	CMF551003F	2		
R 15,16 R 17	RES,MF,1.1108K,+~0.1%,0.125W,25PPM RES,MF,2194,+~0.25%,0.125W,50PPM	485359 375345	91637 91637	485359 CKF55	ĩ		
R 18	RES, CF, 3K, +-5%, 0.25W	441527	80031	CR251-4-5F3K	1		
R 20-25	RESISTOR SET	637991	89536	637991	1	1	
R 36	RES,CF,220,+-5%,0.25W	342626	80031	CR251-4-5P220E	1		
R 37	RES, CC, 620, +5%, 2W	222174	01121		1		
R 39 R 40	RES,MF,2573,+-0.12,0.125W,25PPM RES,MF,3.48K,+-0.12,0.125W,100PPM	321463 375881	91637 91637	CMF55 CHF55			
RT 1, 2	THERMISTOR, BEAD, NEG., 3.6K, +-5%, 50C	643403	50157	1110313	ż		
TP 1- 6, 8- TP 10	TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889 512889	02660	62395	9		
U 1	* IC.CHOS.HEX BUFFER W/3-STATE OUTPUT	407759	12040		1		
U 2	* IC, CMOS, QUAD 2 INPUT OR GATE	408393	02735		1 उ	1	
U 3-5 U 6	* IC,CHOS,HEX BUFFER * IC,LSTTL,OCTAL D F/F,+EDG TRG.W/CLEAR	381830 454892	02735 01295	CD4050AE SN74LS273N	ĩ	÷	
ยัวั	W IC,LSTTL, 3-8 LINE DCDR W/ENABLE	407585	01295	SN74L5138N	Í.	- İ	
ย่อ	* IC, CMOS, HEX INVERTER	381848	02735	CD4049AE	1	1	
ย 9 เม	* IC.LSTTL,QUAD BUS BFR W/3-STATE OUT	472746	01295	SN74LS125N	1	1	
U 10-14	* IC, TTL, DUAL NAND DRVR W/OPEN COLLECT	329706	01295	SN75452P		4	
ป 15 เวิ 16	* IC,OP AMP,DUAL,JFET INPUT,8 PIN DIP * IC,COMPARATOR,8 PIN DIP	495192 352195	12040 01295	LF353BN SN72311P	i	i	
U 17	* IC, VOLT REG, FIXED, +5 VOLTS, 0.1 AMPS	429910	07263	uA78L05AWC	i	i	
VR 8, 9	* ZENER, UNCOMP, 6.0V, 5%, 20.0MA, 0.4W	325795	11532	TD333407	2	2	
XK 1- 9	RELAY SOCKET, 6 POLE	281253	77342	27E34B	9		
XK 1~ 9	RELAY SOCKET, ACCESSORY, SPRING, 6 POLE	417188	89536	417188	93		
Z (- 3	RES,NET,DIP,14 PIN,7 RES,1K,+-32	407445	01121	314	3	f	



Figure 5-7. A6 Sample String PCA

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#### TABLE 5-8. A7 PREAMP PCA (See Figure 5-8.)

DES A1	FERENCE SIGNATOR NUMERICS	>	DESCRIPTION		CK D	MFRS SPLY Cod <b>e</b> -	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY		0 T -E
C	9, ii		CAF, POLYPR, 0.047UF, +-102, 50V CAF, POLYST, 0.047UF, +-202, 1200V CAF, POLYST, 0.22UF, +-102, 100V CAF, CER, 0.22UF, +-202, 50V, 25U	4133	328	84411	JF86	2		
С	10		CAF, POLYST, 0.047UF, +-20%, 1200V	1905	561		126300	1		
С	12		CAP, POLYES, 0.22UF, +-10%, 100V	4361	113	73445	C280MAH1A220K	1	,	
С	13, 20, 2		CAP,CER,0.22UF,+-20%,50V,25U	5191	157	51406	RPE11125U224M50V	22	t	
c	25, 26, 3			2171	1.27					
ç	38, 52- 6			5191 5191						
ç	63-66,7 72	υ,		5191						
с с с	14, 41- 4	6	CAP, CER, 100PF, +-2%, 100V, COG	5126		51406	RPE121	7		
ō	15, 16	-	CAP, CER, 0.0012UF, +-10%, 500V, Z5R	1067	732	71590	CF122	2		
C	17		CAP,CER,33PF,+~2%,100V,COG	5132		51406	RPE121	1		
C	18, 19		CAP, CER, 0.01UF, +-20%, 100V, X7R	4073		72982	8121-A100-W5R-103M	2		
C	22		CAF, CER, 680PF, +-20%, 100V, X7R			51406 60705	RPE 561CR3LBA102EE680K	i		
C C	2 <b>4</b> 27		CAP, CER, 48PF, +-102, 1000V, S3N CAP, CER, 22PF, +-102, 1000V, COG	3691		56289	C030B102F220H	i		
č	28, 29		CAP, CER, 330FF, +-5%, 100V, COG	5284	121	51406		2		
č	32		CAF, POLYES, 0.82UF, +-10%, 100V	4784		80031	719A1	1		
С	33		CAF, CER, 0.001UF, +-20%, 100V, X7R	4029		72982	8121-A100-W5R-102M	1		
C	35, 37, 4	0	CAP,AL,10UF,+-20%,35V	6039		74840	RLR	3 11	£	
CR	5-8,i		DIODE,SI,BV= 75.0V,IO=150MA,500 /	1W 2033 2033		07910	1 N4448		+	
CR H	15, 18, f	Y	* SCREW, MACH, PHP, STL, 6-32X3/8			89536	152165	13		
Ĥ	1		SCREW, MACH, PHP, STL, 6-32X1/4			89536	152140	1		
Ĥ	3		SCREW, MACH, PHP, STL, 6-32X3/4	1142		73734	19048	2		
Ĥ	4		NUT, NYLON, PUSH-IN				PC97476	4		
н	5		SCREW, THD FORM, RHP, STL, 8-15X3/4	2334		89536	233635	4 4		
н	6		SCREW, MACH, PHP, STL, 6-32X7/8			89536 89536	114868			
L V	42		HEADER, 1 ROW, 0.100CTR, 8 PIN			87538 77342	474213 R10-E-5874-1	Ś		
ĸ	1~5 5		RELAY,ARMATURE,6 FORM C,4.5VDC	602		11076				
Ľ	1 7		CHOKE, 6TURN	320	911	89536	320911	7		
	1			606 606	129		606129	1		
MP			OVEN-BACK-PRE-AHP	606	137	89536		1		
ME			OVEN-HEATER-'A'	606			606269	2 1		
MP			OVEN-COVER-PRE-AMP OVEN-BACK-PRE-AMP OVEN-HEATER-AMP PRE-AMP-OVEN-SPREADER PRE-AMP-OVEN-HEATER	606) 606)			606228 606236	ż		
MP MP			PRE-AMP-OVEN-HEATER HEAT SINK, XISTOR THERMALLOY 607:	26 473/		89536	473686	ī		
HP			EJECTOR, PCB, 1/16IN. NOM	494		32559		2		
HP			SPACER, RND, NYLON, 0.187IDX0.500.	2891	835	89536	289835	4		
MP			CHOPPER-CAN		+		605246	1		
MP			DAC-OVEN-INSUL-SIDE-A	659		89536	659318	1		
MP			PRE-AMP-OVEN-INSUL-BACK	659		89536 89536		i		
мр Мр			PRE-AMP-OVEN-INSUL-TOP PRE-AMP-OVEN-INSUL-SIDE	659			659359	ż		
MP			SLEEV, POLYOL, SHRINK, .0930461D,	BLACK 149	443	87536	149443			
MP			SLEEV, TEFLON, 0.027ID, NATURAL	196	717	89536	196717			
MP			SLEEV, TEFLON, 0.0661D, NATURAL SPACER, SWAGED, RND, BRASS, 6-32X0.1	113			113845			
MP			SPACER, SWAGED, RND, BRASS, 6-32X0.1	00 352		89536		2 1		
HP			COMPONENT HOLDER			98159 89536		ł		
MP MP			PRE-AMP OVEN INSULATION GUARD Spacer, Swaged, RND, BRASS, 6-32X0.14			89536	352021	2		
Q	1, 2,	6	* TRANSISTOR, SI, NPN, SMALL SIGNAL	218			MP \$6520	7	1	
ē	8, 12, 1		*	218						
Q	3		<pre># TRANSISTOR,SI,N-JFET,TO-92,SWITC</pre>			15818	U2366J	1	- !	
Q	4, 5		<pre># TRANSISTOR,SI,N-JFET,T0-92</pre>	376		15818	U2810J	2 3	12	
Q	9-11		TRANSISTOR, SI, PNP, SMALL SIGNAL TRANSISTOR, SI, PNP, SMALL SIGNAL		898 720	04713 04713	MPS6522 MJE3055	1	1	
Q Q	13 14		₩ TRANSISTOR,SI,BV= 70V, 90W,TO~12 ₩ TRANSISTOR,SI,NPN,SMALL SIGNAL	218		04713	2N3904	i	1	
Q	16- 19		* TRANSISTOR, SI, N-JFET, TO-92		099	27014	SF53017	4	1	
คิ		<b>6</b> ÷	RES, CC, 15, +-5%, 2W	234	955	01121	нв	6		
R	8			234				4		
R	9,10,4		RES,CF,10,+-5%,0.25W		075	80031	CR251-4-5P10E	6		
Ř	50, 56, 5	7	RES.HF.4.99K.+-1%,0.125W,100PPH	340	252	91637	MFF1-84991	f		
R R	12 17		RES.MF.4.99K.+-1%,0.125W.100PPM		252	91637	MFF1-84991	1		
R	18, 53		RES, MF, 10K, +-12, 0.125W, 100PPM		260	91637	CMF551002F	2		
R	19		RES, MF, 6.19K, +-1%, 0.125W, 100PPM	283	911	91637	CHF556191F	1		
R	21, 22		RES, MF, 399K, +-0.12, 0.1250, 25PPM		212	91637	CMF553993B	2		
R	25, 54	. ,	RES.MF, 20K, +-1%, 0.125W, 100PPM		872	91637	CMF552002F CP251	25		
R	26, 35, 4	¥1,	RES, CF, 10K, +-5%, 0.25W		837 839	80031	CR251-4-5P10K	2		
R	68, 77 27		RES, MF, 100K, +-1%, 0.1254, 100PPM		807	91637	CHF551003F	1		
Ŕ	29		RES, MF, 14K, +-1%, 0.125W, 100PPM		057	91637	CMFSS	1	1	
Ŕ	30, 48		RES, MF, 499K, +-17, 0.125W, 100PPM		813	91637	CMF554993F	2		

## TABLE 5-8, A7 PREAMP PCA (See Figure 5-8.)

2 3 (		TOR RICS		···-· 2	DESCRIPTION	FLUKE STOCK NO	MFR <i>S</i> SPLY CODE-	MANUFACTURERS Part Number or generic type	TOT QTY	я 2 9	א 10 ד 2~
	31,			 6E	S, MF, 10.7K, +-1%, 0.125W, 100PPM	293613	91637	CMF 55	2	-	
è.	32	00			S, MF, 4, 32K, +-1%, 0.125W, 100PFM	294819		CMF554321F	Ī		
è		40,	76		S,CF,S1K,+-5%,0.25W	376434	80031	CR251-4-5P51K	ż		
è .		42-			S, CF, 20K, +-5%, 0.254	441477	80031	CR251-4-5P20K	6		
5	74,	75	44,			441477			0		
č –	37			ŔĽ	S, MF, 162K, +-1%, 0.125W, 100PPM	375998	91637	CHF55	1		
2	38			RE	S,MF,7.15K,+~1%,0.125W,100PPM	260356	91637	CMF557151F	1		
	39			RÉ	S,MF,1.1K,+-1%,0.125W,100PPM	241497	91637	CMF551101F	1		
	45			RE	S,MF,2K,+-1%,0.125W,100PPM	235226	91637	CMF552001F	1		
	51,	60		RE	S, MF, 9.09K, +-1%, 0.125W, 100PPM	221663	91637	CMF559091F	2		
	52,	61,	65,	RE	S, MF, 1K, +-1Z, 0.125W, 100PPM	168229	91637	CMF551001F	5		
:	Ðí,	97				168229					
ŧ	50			RE	S, MF, 60.4K, +-1%, 0.125W, 100PPH	291419	91637	CMF556042F	1		
:	59,	78,	79,	RE	S, MF, 49.9K, +-1%, 0.125W, 100FPH	268821	91437	CMF554992F	5		
	90,					268821					
	62		-	RE	S, CF, 51, +52, 0.254	414540	80031	CR251-4-5P51E	1		
	63				S, MF, 1K, +-0.12, 0.125W, 25PPM	340380	91637	CMF55	1		
	64				S, CF, 2K, +5%, 0.25W	441469	80031	CR251-4-5P2K	1		
	67				S, CF, 8.2, +-5%, 0.25W	442269	80031	CR251-4-5P8E2	1		
	71				S, MF, 556.39K, +-0.1%, 0.125W, 25PPM	485367	91637	CMF55	- i		
		98,	99		S, CF, 1K, +-5%, 0.25W	343426		CR251-4-5P1K	ż		
		84,			S,CF,4.3K,+-5%,0.25W	441576	80031	CR251-4-5P4K3	3		
	87,		00		S, MF, 3.01K, +~1Z, 0.123W, 100PPM	312645	91637	CNF553011F	2		
	88	7 16			S,CF,3K,+-5%,0.25W	441527	80031	CR251-4-5P3K	-		
									i		
	94 95				S,CC,10M,+-5%,0.25W	194944 148189	01121 01121	CB1065 CB1045	2		
					S,CC,100K,+~5%,0.25W						
Ŧ	96	2			S, MF, 39.2K, +-12, 0.125W, 100FPM	236414	91637	CMF553922F			
T	1.	,2			ERMISTOR, BEAD, NEG., 3.6K, +-52, 50C	643403	50157	1110313			
۴	<u></u> **	13			RM, FASTON, TAB, SOLDR, 0.110 WIDE	512889		62395	13		
	3				ANSISTOR, SI, NPN, DUAL, TO-5	478099					
	4				ANSISTOR, SI, NPN, DUAL, TO-5	478099		LH3940H	1	1 1	
	5	-			, OP AMP, LO-OFFSET VOLTAGE, LO-NOISE	605980	04445	0P-07DP	í	1	
	6,	7			, OP AMP, JFET INPUT, TO-5 CASE	429837	12040	LESSAF	2	1	
	. 7				, OF AMP, DUAL, JEET INPUT, 8 PIN DIP	495192	12040	LF353BN	1		
	10				, CMOS, HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	1		
	11-	13			,CMOS,HEX BUFFER	381830	02735	CD4050AE	3	í	
	15				,CMOS,QUAD 2 INPUT NOR GATE	355172	02735	CD4001AE	1	1	
	16				LSTTL, 3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	1	1	
	17				,CMOS,8 INPUT NAND GATE	504860	04713	MC140688CP	1	1	
	ទេ				,CMOS,8-1 LINE MUX/DEMUX ANALOG SW	452805	02735	CD4051BE	1	1	
	19,	20		* IC	,CMOS,QUAD D F/F,+EDG TRG,W/CLR	452912	12040	MM74C175N	2	1	
	21,	22		* IC	LSTTL,QUAD D F/F,+EDG TRG,W/CLR	393215	01295	SN74LS175N	2	1	
	23-	25		* IC	,TTL,DUAL NAND DRVR W/OPEN COLLECT	329706	01295	SN75452P	3	+	
R	•			H ZE	NER, UNCOMP, 4.2V, 5%, 20.0MA. 0.4W	325811	07910	1N753A	1	3	
R	2,	3		⇒ ZE	NER, UNCOMP, 3.3V, 10%, 20.0MA, 0.4W	309799	04713	1N746	2	1	
ĸ	1-	5		RE	LAY SOCKET, & POLE	281253	77342	27E348	5		
ĸ	1	5			LAY SOCKET, ACCESSORY, SPRING, & POLE	417188	89536	417198	52		
U I	6,	7			CKET, IC, T0-99,8 PIN, CIRCULAR	408450	89536	408450	2		
J	10				CKET, IC, 16 PIN	276535	91506	316-AG39D	1		
	í				S,NET,SIP,6 PIN,5 RES,3.6K,+-2%,	478818	80031	95081002CL	1	1	
	5-	7			S, NET, DIP, 14 PIN, 7 RES, 10K, 4-5%	364000	01121	314	3	1	
	8				S.NET, SIP, 10 PIN, 9 RES, 10K, +-22	414003	80031	95081002CL	1		

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Figure 5-8. A7 Preamp PCA

## TABLE 5-9. A8 REF/DAC DIGITAL PCA (SEE FIGURE 5-9.)

SIG	ENCE NATOR MERIC		S D	ESCRIFTION	FLUKE Stock NO	NFRS SPLY Code-	MANUFACTURERS Part Number or generic type		8 2 ~Q	-
2) 2) 3)	1 2~ 17 2, 28 5~ 38 1, 44	, 19- , 29 , 40,		,+50-202,14V 2uf,+-202,50v,25u			SM/VB RPE111Z5U224M50V	1 29		
3				PF,+-102,500V,X7W	105734	71590	BB60301KW7W	1		
3) 3)			CAP, POLYES,	0.1UF,++10%,100V 0.15UF,+-5%,50V	393439 343616	80031 84411	719A1 X46UW0.15-5P50V			
33			CAP, FOLYCA,	0.33UF,+-10%,100V	284703	84411	X463UW	1		
3				PF,+-52,500V			CD15FD750J0 X463UW1029,50W	1		
3) 4)				1UF,+-10%,50V 5UF,+80-20%,25V,Y <b>5U</b>	271619 148924	72982	5855-000-Y5U0-503Z	Í.		
(	1. 6		* DIODE, SI, BV	= 75.0V,ID=150MA,500 MW	203323		1N4448	6 7	+	
	1 2			PHP,STL,6-32X1/4 PHP,STL,6-32X5/16	152140 152157	89536 89536	152140 152157	2		
:	3			PHP, STL , 4-32X1/2	152173	89536	152173	4		
	1, 3	, 5	CHOKE, STURN		320911 320911	89536	320911	5		
	7 1		EJECTOR, PCB	,1/16IN. NOM	494724	32559	CP-66	2 7		
	2		SPACER, SWAG	ED, RND, BRASS, 6-32X0.500	284380	89536	284380	7		
	3 4		DAC-DIGITAL DAC-DIGITAL	-SHIELD-RÉAR	606160 606178	89536 89536	606160 606178	- i		
•	5		SHIELD-DAC-	DIGITAL-A/D	608018	89536	608018	1		
	1, 2		* TRANSISTOR,	SI,NPN,SMALL SIGNAL	159 <b>855</b> 218081	07910 04714	C\$23030 MP\$6520	2	1	
	3 4, 5		* TRANSISTOR,	SI,NPN,SMALL SIGNAL SI,NPN,SMALL SIGNAL SI,N-JFET,TO-92	483099	27014	SF53017	2	Í	
	1 3		RES, CF, 1K, +		343426	80031	CR251-4-5P1K	9		
	0, 22 7, 64				343426 343426					
	4, 8		RES, CF, 270,	+~5%,0,25W	348789	80031	CR251-4-5P270E	.3		
	5, 26		RES,CF,10K,	+-5%,0.25W	348839 348839	80031	CR251-4-5P10K	13		
	4, 35 8, 41				348839					
4	4, 46				348839					
	3 6, 9		RES,CF,510,	+5%.0.25W	348839 441600	80031	CR251-4-5F510E	2		
1	2		RES,CF,4.7K	,+-52,0.25W	348821	01121	CB4725	1		
	4, 18 5, 19		RES, CF, 560, RES, CF, 470,		385948 343434	80031 80031	CR251-4-5P560E CR251-4-5P470E	2		
	6, 20		RES, CF, 33, +	-5x,0.254	414524	80031	CR251-4-5P330E	2		
	7, 21		RES, CF, 620,	+~5%,0.25₩ ,+~5%,0.25₩	414524 442319 348920	80031 80031	CR251-4-5P620E CR251-4-5P100K	2 3		
	3, 50 4	1 - 21	RES, CF, 160K	,+-5%,0.25W	442442	80031	CR251-4-5P160K	1		
	7				441535	80031	CR251-4-5P300K	1 1 3		
	0 3, 55	. 61	RES, CF, 10, + RES, MF, 10K,		340075 168260	80031 91637	CR251-4-5P10E CMF551002F			
- 4	5	,	RES, HF, 38.3	K,+-1%,0.125W,100PPM	241372	91637	CMF553832F	i		
	7 18			,+-1%,0.125W,100PPM K,+-1%,0.125W,100PPM	248807 241380	91637 91637	CMF551003F CMF55	i t		
5	2, 53	, 58,		-0.05%,0.14,25PPM	514265	91637	PTF	4		
	9 4		650 ME 400M	,+-12,0.125W,100PPM	514265 276626	91637	CMF55	4		
	6			K,+-12,0.125W,100PPM	221663	91637	CMF 559091F	Í		
6	0			、+-12、0、125W、100PPM メートの、12 の、125W、258時間	289504 344440	91637 91637	CMF553323F CMF552152F	1		
	2 2, 63		RES, NF, 21.5 RES, CF, 200,	K,+-0.1%,0.125W,25PPM +-5%,0.25W	344440	80031	CR251-4-5P200E	2		
	1, 2		PULSE TRANS	FORMER	420901	89536	420901	2		
	1 12 1, 14	, 21		,TAB,SOLDR,0.110 WIDE BUFFER W/3-STATE OUTPUT	512889 407759	02660	62395 Mm80C97N	12		
	2- 4		* IC, CMOS, HEX	BUFFER	381830	02735	CD4050AE	3	1	
	5			8 LINE DCDR W/ENABLE	407585 504860	01295 04713	SN74LS138N MC14069BCP	1	ł	
	6 8			NPUT NAND GATE AD BUS BFR W/3-STATE OUT	472746	01295	SN74LS125N	i	i	
	9		* IC.CMOS.QUA	D 2 INPUT OR GATE	408393	02735	CD4071BE	1	1	
	1 2			GRAMMABLE INTERVAL TIMER 8mHz,TTL CLOCK	584177 584169	33297 09969	uPD8253C X0-33D-15-8-MHZ	i	i	
1	3		* IC, DUAL DIV	BY 16 BINARY COUNTER	483578	01295	SN74LS393N	į	Į.	
1	7,18 9,20			TO,HI-SPEED,LED TO GATE L D F/F,+EDG TRG,W/SET&CLR	504522 418269	28480 01295	HCPL-2601(5082-436 SN74874N	2	1	
	7, 20 2			AL D F/F, +EDG TRG, W/SETBOLK	393124	01295	SN74LS74N	Ĩ	1	
	3		* IC,LSTTL,HE	X INVERTER 0 PPM T.C.,BANDGAP REF	393058 472845	01295 04713	SN74LS04N MC1403V	1	1	
				99 FFA I.I. SANULAP KEP	472845	04(13				
2	4 5			INVERTER W/OPEN COLLECTOR	407593	01295	SN7406N	1	1	

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#### TABLE 5-9. A8 REF/DAC DIGITAL PCA (SEE FIGURE 5-9.)

DES	ÉRÉNC I GNAT NUMER	-	2	DESCRIPTION	FLUKE STOCK	MFRS SPLY CODE-	MANUFACTURERS Part Number Or generic type	TOT QTY	א 2 קרי	м О Т ‴Е	
U	31		#	IC, CMOS, DUAL D F/F, +EDG TRIG	340117	02735	CD4013AE	1			
U	32			IC.LSTTL.RETRG MONOSTAB MULTIVE W/CLR	412734	01295	SN74LS122N	- i	1		
U	38			IC, OP AMP, DUAL, JEET INPUT, 8 PIN DIP	495192	12040	LF353BN	i.	i		
U	39			ISOLATOR. OPTO.LED TO TRNSISTOR	536045	14936	NCT-26	Í.	i.		
U	40		×	IC.CMOS.8-1 LINE MUX/DEMUX ANALOG SW	452805	02735	CD4051BE	1	1		
ប	4 t		*	IC, CHOS, QUAD 2 INPUT NOR GATE	355172	02735	CD4001AE	1	1		
U	42		¥	IC, CHOS, QUAD D F/F, +EDG TRG	536292	04713	MC14175B	1	1		
٧R	1,	2	×	ZENER, UNCOMP, 3.3V, 102, 20.0MA, 0.4W	309799	04713	1N746	2	2		
XU	t i			SOCKET, IC, 24 PIN	376236	91506	324-AG39D	1			
XU	13			SOCKET, IC, 14 PIN	276527	09922	DILB8P-108	t			
XU	30			SOCKET, IC, 40 PIN	429282	09922	DILB40P-108	1			
χų	40			SOCKET,IC,16 PIN	276535	91506	316-AG39D	í			
Z	4			RES,NET,SIP,10 PIN,9 RES,10K,+-2%	414003	80031	95081002CL	1	1		
Z	6	8		RES,NET,DIP,14 PIN,7 RES,1K,+-5%	407445	01121	314	3			
							•				



Figure 5-9. A8 REF/DAC Digital PCA

#### TABLE 5-10. A9 REF/DAC ANALOG PCA (SEE FIGURE 5-10.)

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				(SEE FIGURE 5-10.)						
REFERENC DESIGNAT A->NUMER	CE FOR RES-	>	2	DESCRIPTION	FLUKË STOCK NO	MFRS SPLY Code	MANUFACTURERS Part Number or generic type	TOT QTY		N 0 T
							1.00 1.00 Feb 1.00 Feb 1.00 Feb 1.00 Feb 1.00 Feb 1.00 Feb 1.00 Feb 1.00 Feb 1.00 Feb 1.00 Feb 1.00 Feb 1.00 Feb			au
AR 1			×	REF-AMP-SET Cap, AL, 22UF, +-20%, 50V Cap, AL, 6.8UF, +-20%, 35V Cap, Cer, 0.22UF, +-20%, 50V, <b>Z5U</b>	638007	89536	638007	1 2		í
<u> </u>	2			CAP, AL, 220F, +-20%, 50V	614362	87730	614362 643189 56511175/1004856/	8		
C 3-		11		CAP, AL, 6.80F, +~20%, 35V	643187	87038	RPE111Z5U224M50V	14	1	
C 10,	18,	27,		CAP, CER, 0.220F, +=20%, 50V, 250	519157	21490	RFE111230224030V	17	•	
C 28, C 43,	34,	40,			519157					
	46, 53,				519157					
C 64,		02,			519157					
	15,	21		CAR CER 33RE +27 (88) COG	513226	51406	RPE121	3		
C 13	10			CAP.CEP.100PF.+*107.1000V.S3N	105593	71590	DD-101	2		
C 14				CAP, CER, 100PF, +-102, 1000V, S3N CAP, CER, 0.0012UF, +-102, 500V, Z5R	106732	71590	CF122	1		
C 16,	22			CAP, TA, 1UF, +-10%, 35V	161919	56289	196D010X0035G	2 5		
C 17,	23,	45,		CAP,CER,33PF,+-2%,100V,COG	513226	51406	RPE121	2		
C 76,	78			AND DOLVED A DOUR & 40% FOU	513226	00574	696492	2		
C 19, C 24	20			CAP, PULIES, 0.2207, 4-107, 50V	696492	07930 00534	670472 494 <b>4</b> 97	1		
C 25,	24			CAP. AL 22001E. +50-202.35V	460279	89536	460279	2		
C 25,	26			CAP. CER. 330PF. +-5%. 100V. COG	460279 528620	51406	RPE121	2		
Č 29,	30.	32.		CAP, CER. 330PF, +-5%, 100V, COG	528620	51406	RPE121	4		
C 33		-			528620					
C 33 C 36				CAP, CER, 0.0012UF, +-102, 500V, Z5R CAP, CER, 0.0012UF, +-102, 500V, Z5R CAP, CER, 33PF, +-22, 100V, COG CAP, CER, 33PF, +-22, 100V, COG CAP, POLYES, 0.22UF, +-102, 50V CAP, POLYES, 0.22UF, +-102, 50V CAP, AL, 220UF, +50-20%, 35V CAP, CER, 330PF, +-52, 100V, COG CAP, CER, 330PF, +-52, 100V, COG CAP, CER, 330PF, +-52, 100V, COG CAP, CER, 330PF, +-52, 100V, MERMETIC CAP, FOLYES, 0.82UF, +-102, 100V	659102	84411		1		
C 37				CAP, FOLYES, 0.82UF, +-102, 50V	530477	84411	X663F	!		
				CAP, FOLYES, 0.82UF, +-102, 100V	478644	80031	(17A)	2		
C 40,	41			CAP, CER, 0.0012UF, +-107, 500V, 25R	105732	71279	C280MAH1A220K	ร์		
C 42				CAP, FULTES, 0, 220F, +-10%, 100V	430113	73442	1960475X9015HA1			
C 44 C 51				CAP DOLYES A ACCUE +(AY CSAV	23448A	73445	C2BOMAE/A22K	i		
C 60,	A1			CAP,FOLYES,0.820F,++102,50V CAP,FOLYES,0.820F,++102,100V CAP,CER,0.00(20F,++102,100V CAP,FOLYES,0.220F,++102,100V CAP,TA,4.70F,++202,50V CAP,POLYES,0.0220F,++102,250V CAP,AL,150F,++202,35V CAP,FOLYES,10F,++102,100V CAP,CER,1000PF,++52,50V,COG DIODE,SI,BV= 75.0V,10±150MA,500 MW	614024	89536	614024	ż		
	73,	75		CAP. POLYES. 10F. +-102. 100V	447847	73445	C280MAH/A1H	5		
C 79		<b>,</b> –		CAP, CER, 1000PF, +-5%, 50V, COG	528539	51406	RPE113	1		
CR 1,	2,	5,	×	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	9	1	
CR 14-	10,	25						2	í	
CR 19,	20		*	DIDDE,SI, 100 PIV, 1.0 AMP	343491	01295 00574	1N4002 152165	21		
H 1 H 2				ろしれたが、FRUF, FREF, STE, 67928970 NUT MARY NEV CTI といなつ	110551	89536	110551	ĩ		
ี่ ผื่ รื่				SCREW, MACH, PHP, STL, 6~32X7/8	152165 110551 114868	89536				
H 4				SCREW, MACH, PHP, STL, 6-32X3/4	114223	73734	19048	2		
J 52,	53			SCREW, MACH, PHP, STL, 6-32X3/8 NUT, MACH, HEX, STL, 6-32 SCREW, MACH, PHP, STL, 6-32X7/8 SCREW, MACH, PHP, STL, 6-32X3/4 HEADER, 1 ROW, 0.100CTR, 8 PIN RELAY, ARMATURE, 6 FORM C.4.5VDC	474213	89536	474213	4 2 2 2		
К 1,	2				602953	77342	R10-E-5874-1			
L 1	5,	7		CHOKE, GTURN OVEN-DIVIDER-DAC OVEN-BACK-DAC DAC OVEN SPACER TOP OVEN PLATE, DAC OVEN-HEATER-"A" INSULATOR, DAC OVEN OVEN-HEATER-"B" DAC-OVEN-COVER HEATSINK SLEEV, FOLYOL, SHRINK, 093-, 046ID, BLACK	320911	89536	320911	6		
MP 1				OVEN-DIVIDER-DAC	686140	87230	000140 404450	i		
MP 2 MP 3				DAC OVEN SPACER	582676	89536	582676	i		
MP 4				TOP OVEN PLATE, DAC	606251	89536	606251	1		
MP 5				OVEN-HEATER-"A"	606269	89536	606269	{ 2 1		
MP 6				INSULATOR, DAC OVEN	735209	89536	735209	1		
MP 7				OVEN-REATER-"B"	651083	87536	651983	2 1		
MP 8				DAC-OVEN-COVER	606244	17107	000444 4030B-TT	2		
MP 9 MP 10				STEEN TEELON & A27TD NATURA!	194717	89536	194717	-		
MP 11				SLEEV, FOLYOL, SHRINK, .093046ID, BLACK	149443	89536	149443			
MP 12				SLEEV, TEFLON, 0.0661D, NATURAL	113845	89536	113845			
MP 13				SPACER, RND, NYLON, 0.1871DX0.500.	289835	89536	289835	4		
MP 14				CHOPPER-CAN	605246	89536	605246	1.		
MP 15				EJECTOR, PCB, 1/16IN, NOM	494724	32559	CP-66 (50200	2		
MP 16				DAC-OVEN-INSUL-BACK	659292	-89536	659292 659300			
MP 17				DAC-OVEN-INSUL-TOP DAC-OVEN-INSUL-SIDE-A	459300 459318	89536 89536	659300 659318	2		
MP 18 MP 19				DAC-OVENINSULSIDEA DAC-OVENINSULSIDEB	659326	89536	659326	2222		
MF 20				SPACER, MOUNT, NYLON	152207	07047	10123-DAP	2		
MP 21				SPACER, SWAGED, RND, BRASS, 6-32X0.100	352021	89536	352021	2		
Q 1,	2,	4	×	TRANSISTOR, SI, NPN, SMALL SIGNAL	218081	04714	MP\$6520	3	1	
<u> </u>		15,	×	TRANSISTOR, SI, NPN, SMALL SIGNAL	218081	04714	HP\$6520	5	i	
Q 23,	24		横い	TRANSFERRO ST BY- DAY RAN TR.197	218081 325738	04713	MJE2955	í	í	
Q 6 Q 8-	11,	21-	H H		284927	07910	TCR5305	ន់	2	
Q 24	,	£1	- 14 - 14	stostistik artijoonneni nauji-210 na	284927		· ····································			
	10,	27,	*	N-CHANNEL, 4 PC. SET	404244	89536	404244	1	1	
Q 30			¥		404244			~		
Q 30 Q 12,			Ħ	TRANSISTOR, SI, N-JFET, TO-92, SWITCH	261578	15818	U2366J	2	1	
Q (3,	14,			TRANSISTOR, SI, NPN, SMALL SIGNAL	159855	07910	CS23030	•	1	
Q 21, Q 15	31,	ک د	¥	TRANSISTOR, SI, NPN, DUAL, TO-5	159855 478099	12040	LM3940M	1	1	
Q 15,	17			TRANSISTOR, SI, N-JFET, SWITCHING, TO-92	370072	15818	U3422J	2	1	



TABLE 5-10.	A9 REF/DAC	ANALOG F	°CA
(SEE FIGURE	5-10.)		

REFERENCE DESIGNATOR A>NUMERICS>	\$DESCRIFTION-	FLUKE STOCK NO	SPLY CODE-	MANUFACTURERS PART NUMBER OR GENERIC TYPE	QTY	Я 2 Ф-	
	* TRANSISTOR, SI, NPN, DUAL, TO-5	478079		LM3940M	1		
Q 16 Q 25-28	<pre># TRANSISTOR,SI,N-JFET,TO-92</pre>	483099		SF53017	4	2	
	★ TRANSISTOR,SI,N-JFET,TO-92 RES,CF,1K,+~5%,0、25W	343426	80031	CR251-4-5P1K	4		
R 14		343426	00574	256990	1	í	
R 4 K 7	9.0K +03% .25W BOBBINAXIAL LEAD RES.MF.200.+-1%.0.125W.100PPM	256990 245340		CHF552000F	i	•	
R 9	18K	648220		648220	1	1	
R 10	RES.CE.100K.+~5%.0.25W	348920	80031	CR251-4-5P100K	1	1	
R 12	RES, CF, 2K, +~5X, 0.25W	441469 296665	80031	CR251-4-5P2K			
R 13 R 16	RES, HF, 30.1,+-12,0.125W,100PPM RES, MF,1K,+-12,0.125W,100PPM	168229	91637	CHF55 CMF551001F	- i		
R 18,28	1.68K .25W WW RESISTOR	168229 683847 281832 683839	89536	683847	ż	1	
R 20	RES, CC, 5.1, +-5%, 0.25W	281832	01121	CB5R15	1	1	
R 22,26	RES,CC,5.1,+-5%,0.25W 5.18K .25W WW RESISTOR RES,CF,1.3K,+-5%,0.25W RES,MF,100K,+-0.1%,0.125W,25PFM	683839	89536	683837 CR251-4-5P1K3	2 1		
R 24 R 25	RES,CF,T.SK,TTSK,0.23W RFS MF.100K.+~0.12.0.125W.25PPM	340166	91637	CMF5510030	i		
R 26	RES, MF, 7, 68K, +-0.12, 0.125W, 25PPM RES, MF, 49, 9K, +-12, 0.125W, 100PPM	658575	91637	CMF55	1		
R 30, 92, 98,	RES.HF,49.9K,+-12,0.125W,100PPM	268821	91637	CMF554992F	4		
R 99		268821 368753	90031	CR251-4-5P30K	f		
R 32 R 33	RES,CF,30K,+~5%,0,25W RES,MF,499K,+~1%,0,125W,25PPM	260513		260513	12		
R 34, 37	RES, MF, 100K, +-1%, 0.125W, 25PPM	293472	91637	CHF551003F	2		
R 38	RES, MF, 1K, +-0.12, 0.125W, 25PPM	340380	91637	CMFS5	1 1		
R 39	RES, MF, 249K, +-1%, 0.125W, 25PPM RES, CE, 10, +-5%, 0.25M	379131 340075	91637 88831	CMF35 CR251-4-5F10E	4		
Ř 40,41,60, R 61	RES,CF,10,+-5%,0.25W	340075	00001	GREDT 4 DI TVE	·		
R 42, 43	RES, CF, 150, +-5%, 0.25W	340075 343442 340174 193342	80031	CR251-4-5P150	2		
R 44	RES, NF, 2K, +-0.12, 0.125W, 25PPH	340174	91637	CMF552001B	1		
Ř 45	RES,CC,5.1K,+-5%,0.25W	193342	01121 91637	CB5125 CMF55	1		
R 46 R 47	RES.MF. 750K.+-0.12.0.125W.25PPM	435164	91637		i		
R 48	RES, MF, 124K, +-12, 0.125W, 25PPM	479352	91637	CMF55	1		j.
R 49	RES, MF, (00K, +-0.1%, 0, 125W, 25PPM	340166	91637	CMF551003B	1		
R 50 R 51	RES,MF,15K,4~1%,0.120W,20FFM RES ME 400V 4.12 0 (050 100RPM	328161 276626	91637		ł		
R 51 R 52, 84,101	RES, NF, 2K, +-0.1%, 0.125W, 25PPH RES, CC, 5.1K, +-5%, 0.25W RES, MF, 255K, +-1%, 0.125W, 100PPM RES, MF, 750K, +-0.1%, 0.125W, 25PPM RES, MF, 124K, +-1%, 0.125W, 25PPM RES, MF, 100K, +-0.1%, 0.125W, 25PPM RES, MF, 15K, +-1%, 0.125W, 100PPM RES, MF, 10K, +-1%, 0.125W, 100PPM RES, MF, 10K, +-1%, 0.25W, 100PPM RES, MF, 10K, +-1%, 0.25W, 100PPM	\$68260	91637	CMF551002F	1 1 3 3		
R 54, 59,114	855 PE 201 4-57 8 254	441477	80031	CR251-4-5F20K	3		
R 55	RES, MF, 4.99K, +-12, 0.125W, 100PPH	168252	91637	MFF1-84991	1		
R 57,58	RES,CF,240,+-5%,0.25W	376624	80031	CR251-4-5P240E CR251-4-5P200K CMF551004F 686139 CMF553011F	2 1		
r 63 r 68, 94	RES,CF,200K,+-5%,0.25W RES,MF,1M,+-1%,0.125W,100FFM	268797	91637	CMF551004F	2		
R 69, 73	MATCHED RESISTOR SET	686139	89536	686139	1		
R 70	RES, MF, 3.01K, +-1%, 0.125W, 100PPM RES, MF, 100K, +-1%, 0.125W, 100PPM RES, NF, 100K, +-1%, 0.125W, 100PPM RES, NF, 47, +-5%, 0.25W	312645	91637	CMF353011F	1 2		
R 72,86 R 74,77	RES, CF, 47, +-52, 0, 25W	248807 441592		CMF 551003F CR251-4-5P47E	ź		
R 75,126,128,		221663		CMF559091F	4		
R 130		221663			_		
R 76, 97,127,	RES,MF,1K,+-1%,0.125W,100PPM	168229	91637	CMF551001F	5		
R 129,131 R 78	RES. MF, 20K, +-1%, 0.125W, 100PPM	168229	91637	CMF552002F	í		
Ř 79,81	RES.MF. 399K. +-0.1%,0.125W,25PPM	417212			2	í	
R 85	RES, HF, 6. 19K, +-1%, 0. 125W, 100PPM	283911	91637	CMF556191F	1		
R 87	RES,MF,402K,+~1%,0.125W,100PPM	217984	91637	CMF554023F CMF557501F	2		
r 89 r 89	RES,MF,7.50K,+-1%,0.125W,100FPM RES,MF,15.4K,+-1%,0.125W,100FPM	223529 261651	91637 91637	CMF551542F	i		
R 90	RES, MF, 22.1K, +-1%, 0.125W, 100PPM	235234	91637	CMF552212F	1	1	
R 93	RES, MF, 681, +-12, 0.125W, 100PPM	543785	91637	CHF556810F	1		
R 95	RES,CC,6.8M,++5%,0.25W	394064	01121	CB CR251-4-5P1K			
R 94 K 100,108	RES,CF,1K,+-5%,0.25W RES,MF,2.94K,+-1%,0.125W,100PPM	343426 261628	80031 91637	CMF552941F	2		
R 102-104,106	RES, MF, 18.2K, +-1X, 0.125W, 100PPM	236810	91637	CMF55	4		
R 113	RES,CC,1K,+-5%,0.5W	108597	01121	CB1025	<u> </u>		
8 115 P 114	RES,CF,2M,+-5%,0.25W	442582 194944	80031 01121	CR231-4-5P2M CB1065			
R 116 R 118-125	RES,CC,10M,+~5%,0.25W Res,CC,10,+~10%,2W	174744	01121	HB HB	8		
R 132-137	RES, CF, 10K, +~5%, 0, 25W	348839	80031	CR251-4-5P10K	6		
R 138	RES, MF, 130K, +-12, 0.1250, 100PPM	241083	91637	CMF5515035	1		
RT 1, 2	THERMISTOR, BEAD, NEG., 3.6K, +~5%, 50C TERM EASTON TAR SOLDE & 440 MIDE	643403 512889	50157 02660	1H10313 62395	2 17		
TP 2- 16, 18, TP 19	TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889	ATGOA		• •		
U 1	* IC, VOLT REG, FIXED, -5 VOLTS, 1.3 AMPS	394551	04713	MC7905CT	1		
U 2, 4, 5	* IC, OP AMP, GENERAL PURPOSE, 8 PIN DIP	478107	12040	308AN	3 1	1	
U 7 U 8, 9, 11	* IC,OP AMP,GEN PURPOSE,TO-78 METAL CAN * IC,OP AMP,JFET INPUT,TO-5 CASE	288928 429837	12040 12040	LM308AH LF356F	3	÷	
u u, /, //	. Logar thirgarks kithlythe in writte				-		

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#### TABLE 5-10. A9 REF/DAC ANALOG PCA (See Figure 5-10.)

REFERENCE FLUKE MFRS MANUFACTURERS DESIGNATOR STOCK SPLY PART NUMBER A->NUMERICS> SDESCRIPTION	TOT QTY	א 2 -Q	0 Ť ~É
U 10, 12 * IC, OP AMP, GENERAL PURPOSE, TO-78 CASE 413732 12040 LM308N	2	1	
U 13 * IC.OP AMP.DUAL.JET INPUT.8 PIN DIP 495192 12040 LF353BN	í	- i	
U 14 * IC,OP AMP,LO-OFFSET VOLTAGE,LO-NOISE 605980 06665 0P-07DP	i	÷	
U 20 * IC, CMOS, 8-1 LINE MUX/DEMUX ANALGG SW 452805 02735 CD4051BE	1	4	
U 21, 25 * IC,LSTTL, QUAD D F/F, +EDG TRG, W/CLR 393215 01295 SN74LS175N		í	
U 22 * IC, CHOS, QUAD 2 INPUT NOR GATE 355172 02735 CD4001AE		÷	
U 23, 24 * IC, CMOS, HEX BUFFER 38(830 02735 CD4050AE	ż	÷	
U 26 * IC, TTL, UAL NAND DRVR W/OPEN COLLECT 329706 01295 SN75452P	ĩ	÷	
U 28 * IC, TTL, SUAD 2 INFUT NOR GATE 288845 01295 SN7402N	÷	÷	
VR 1, 7 * ZENER, UNCOMP, 15.0V. 52, 8.5MA, 0.4W 266601 04713 1N9658	2	- 1	
VR 3 * ZENER, UNCOMP, 10.0V, 102, 20.0MA, 0.4W 180406 04713 1N758		÷	
VR 5 W ZENER, UNCOMP, 4.77, 102, 20.0MA, 0.4W 387084 07910 1N750	÷	i	
VR 6 * ZENEK, UNCOMP, 6.2V, 57, 20.0MA, 0,4W 325811 07910 (N753A			
VR 10, 11, 14 * ZENER, UNCOMP, 3.3V, 102, 20.0MA, 0.4W 369799 04713 (N746		ĩ	
VR 12 * ZENER, UNCOMP, 15.0V, 52, 8.5MA, 0.4W 266601 04713 1N965B			
VR 12 * ZENER, UNCOMP, 5.1V, 52, 20.0MA, 0.4W 159798 04713 1N751A		1	
W 1 REFERENCE-CABLE 608604 89536 608604			
	1		
	ž		
XU 7- 9, 11 SOCKET,IC,TO-99,8 PIN,CIRCULAR 408450 89536 408450 XU 20 SOCKET.IC.16 PIN 276535 91506 316-AG39D	4		
	2		
Z 3, 4 RES,NET,DIP,14 PIN,7 RES,1K,+-5% 407445 01121 314	2	1	

FOTE 1 = INCLUDES R19,821,827,829,03,06





# TABLE 5-11. ATO INSIDE REGULATOR PCA (SEE FIGURE 5-11.)

FERENCE SIGNATOR >NUMERICS>		FLUKE Stock ND	MFRS SPLY Code-				7 E
7	CAP, CER, 0.22UF, +-20%, 50V, Z5U CAP, AL, 47UF, +-20%, 10V CAP, CER, 0.1UF, +-20%, 100V, Z5V CAP, AL, 22UF, +-20%, 50V		51406	RPE11175U224M50V	· {		
8, 28	CAP, AL, 47UF, +-20%, 10V	613984	89536	613984	2		
9, 42, 43	CAF, CER, 0.1UF, +-20%, 100V, 25V	149146	56289	33C4196	3		
10, 12, 14,	CAP, AL, 22UF, +-20%, 50V	614362	89536	61 4 3 6 2	10		
18, 20, 24,							
26, 35, 37, 39		614362 614362					
1, 13, 21,	CAP, CER, 0.22UF, +-202, 50V, 25U	309849	71590	CW3COC224K	8		
25, 27, 34,		309849	(12/0	OWGGGGZZ TK			
36, 44		309849					
17, 19, 41	CAP, TA, 10UF, +-202, 35V CAP, CER, 470PF, +-202, 100V, X7R CAP, AL, 2UF, +75-102, 150V	417683	56289	196D106X0035KA1	З		
23	CAP, CER, 470PF, +-20%, 100V, X7R	358275	72982	8111-A100-W5R-471M	1		
30 31	CAP,AL,2UF,+75-10%,150V CAP,AL,100UF,+75-10%,150V				!		
32, 45	CAP,AL,100UF,+75-102,16V CAP,TA,1UF,+~102,35V	436014 161919 603793	54288	SL 196D010X0035G	2		
3, 38	ELECTRO, MIN,LO LEAK, 4.7MF, 35V	603993	89536	603993	ž		
0	CAP, CER, 1200PF, +-20%, 100V, X7R		72982				
1- 10, 13,		343491	01295	1N4002	17	1	
15, 16, (8,	*	343491					
1, 23, 24 5, 14	# # THYRISTOR,SI,TRIAC,VBO=400V,8.0A	343491	ホウウマド	T2800D	2		
9, 20, 22	* DIODE,SI,BV= 75.0V,IO=150MA,500 MW			1N4448	3	1 1	
21	* LED, RED, CLIP MOUNT, LUM INT=0.8MCD		12040		Ť	i	
i, 2	FUSE, 1/4 X 1-1/4, FAST, 4A, 250V		71400		2	•	
1	SCREW, MACH, PHP, STL, 6-32X5/16	152157		152157	18		
1	HEATSINK		91502	PA1-1CB	5		
2	HEAT SINK, XISTOR THERMALLOY 60728	473686		473686	!		
3 5	HEATSINK, OUTER, UI		13103		1		
5	EJECTOR, PCB, 1/16IN. NOM Spacer, Swaged, RND, Brass, 6-32x0, 100	494724 352021	32559 89536	CP-66 352021	2 18		
6, 8	SPACER, SWAGED, RND, BRASS, 6-32X0, 100 * TRANSISTOR, SI, BV= 60V, 65W, T0-220 * TRANSISTOR SI BV= 60V, 50W T0-220	386128	01295	T1P120	2	f	
0, 16	· · · · · · · · · · · · · · · · · · ·	483693			2	2	
2, 18, 21-	# TRANSISTOR, SI, NPN, SHALL SIGNAL	218396	04713	2N3904	6	1	
3, 25	*	218396					
3, 24 9	* TRANSISTOR, SI, PNP, SHALL SIGNAL	195974		2N3906	2	1	
20	* TRANSISTOR,SI,BV= 45V, 30W,TO-220 * TRANSISTOR,SI,BV= 50V,117W,TO-3	325761 183012		D44C5 40251	1	1	
9, 25, 27	RES, CF, 1K, +-52, 0.25W	343426	80031		3	•	
0, 13, 16,	RES, CC, 1.8K, +-10Z, 2W	185983	01121	HD1821	4		
:8		185983					
1, 14, 18	RES, MF, 464, +-12, 0.125W, 100PPM		91637		3		
2, 15, 17 9	RES,MF,10.2K,+-1%,0.125W,100PPM RES,CF,100,+-5%,0.25W	293605 348771			3 1		
20, 46, 55,	RES, CF, 6.8K, +-5%, 0.25W	348771 368761 368761 151324 325712 342618 343418 348920	80031	CR251-4-5P6K8	4		
3		369761	,		•		
21, 22	RES,MF,1K,+-1%,0.5W,100PFM	151324	91637	CMF651-2-1P1K	2	1	
23	RES, WW, 0.15, +-5%, 2W	325712	75042	BMH	1		
24 26	RES,CF,56,+~52,0.25W	342618	80031	CR251-4-5P56E	1		
51-33	RES,CF,1.5K,+~5%,0.25W RES,CF,100K,+~5%,0.25W	343410	80031	CR251-4-5P1K5 CR251-4-5P100K	ż		
34, 35,111,	RES, CF, 3K, +-5%, 0.25W	441527	80031	CR251-4-5P3K	4		
12		441527			,		
36	RES, CF, 1H, +-3%, 0.25W	348987	80031	CR251-4-5P1M	1		
37	RES, MF, 130, +-1%, 0.125W, 100PPM	485698	91637	CMF551300F	1		
38 39	RES,MF,(K,+-1%,0.125W,(00FPM RES,CF,510,+-5%,0.25W	168229	91637	CMF551001F CP251-4-50510F	1		
10, 41, 57	RES, MF, 16.9K, +-12, 0.125W, 100PPM	441400 267146	80031 91637	CR251-4-5F510E CMF551692F	3		
12, 45, 59,	RES, MF, 15K, +-12, 0.125W, 100PPM	285296	91637	CMF551502F	5		
65, 66, 75		285294			_		
13, 44, 60	RES, MF, 2, 05K, +-1%, 0, 125W, 100PFM	293704	91637	CMF552051F	3		
47, 56, 64 48	RES, CF, 2, 2K, +-5%, 0, 25W	343400	80031	CR251-4-5P2K2	3		
19, 50	RES,CF,330,+-5%,0.25W RES,MF,4.99K,+-1%,0.125W,100PPM	368720 168252	80031 91637	CR251-4-5P330E MFF1-84991	f 2		
51, 54	RES, MF, 4.42K, +-1%, 0.125W, 100PPM	288514	91637	CHF554421F	ź		
52, 53	RES, NF, 604, +-12, 0. 125W, 100PPM	320309	91637	CMF556040F	ž		
58	RES,MF,24.3K,+-1%,0.125W,100PPM	236745	91637	CMF55	1		
61	RES, MF, 2.87K, +-12, 0.125W, 100PPM	185629	91637	CHF552871F	1		
62 47 78 88	RES, MF, 21K, +-0.52, 0.125W, 100PPM	229484	91637	CHF55	1		
67, 70, 80 68, 69, 79	RES,MF,13.3K,+-12,0.125W,100PPM RES,MF,1.82K,+-12,0.125W,100PPM	296566 293670	91637 91637	CMF551332F CMF551821F	3		
	RES, CF, 15K, +-52, 0.25W	348854	80031	CR251-4-5P15K	3		
71, 81, 92							
71, 81, 92 72, 82, 93,	RES, CF, 10K, +-5X, 0.25W	348839	80031	CR251-4-5P10K	16		
71. 81, 92		348839 348839 348870	80031 80031	CR251-4-5P10K CR251-4-5P22K	16 3		





TABLE 5-11. A10 INSIDE REGULATOR PCA (SEE FIGURE 5-11.)

DES	GRENCE IGNATOR NUMERIC		2	DESCRIPTION-	FLUKE STOCK	MFR <i>S</i> SPLY Code-	MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	R S -Q 	0 T E
R	74, 84	95		RES,MF,30.1K,+-1%,0.125W,100PPM	168286	91637	MFF1-83012F	3		
Ŕ	76, 86			RES, CF. 1.2K, +-52, 0.25W	441378	80031	CR251-4-5P1K2	3		
R	77,87			RES, MF, 26.7K, +-1%, 0.125W, 100PPM	245779	91637	CHF552672F	3		
R	78, 88			RES, MF, 3.65K, +-12, 0.125W, 100PPM	293779	91637	CMF553651f	3		
R	95	, 9,		RES, VAR, CERM, 1K, +-10%, 0.5W	285155	71450	360S102A	1		
R	96			RES, MF, 1.43K, +-12,0.125W, 100PPM	325662	91637	CMF551431F	1		
Ŕ	97			RES, MF, 4.75K, +-1%, 0.125W, 100PPM	260579	91637	CMF554751F	1		
	113			RES, CF, 39, +-5%, 0.25W	340836	80031	CR251-4-5P39E	1		
TP	1. 15	5		TERM, FASTON, TAB, SOLDR, 0, 110 WIDE	512889	02660	62395	15	10	
Ť₽	16- 18			SOCKET, SINGLE, PWB, FOR 0,080 PIN	170480	74970	105-752	3		
Ů.	1, 4		×	IC, VOLT REG, FIXED, +5 VOLTS, 1.5 AMPS	355107	12040	LM340T-5	2 2		
ŭ	2, 6	5		IC, VOLT REG, ADJ, 1.2 TO 37 V, 1.5 AMPS	473793	12040	LM317MP	2	1	
ŭ		2, 15		IC, VOLT REG, FIXED, -15 VOLTS, 1.5 AMPS	413179	04713	MC7915CP	3	1	
ษั	7			IC, VOLT REG, ADJ, NEG, -1.2VT0-37V.	707661	12040	LH337HP			
Ū	â		×	IC,VOLT REG,ADJ,1.2 TO 37 V,1.5 AMPS	460410	12040	LM317T		)	
Ū	10		*	IC, VOLT REG, ADJ, 2 TO 37 VOLT, 0.15 AMP	379420	04713	MC1723CL	2	1	
ü	11		¥	IC,VOLT REG,FIXED,-24 VOLTS,1.5 AMPS	418251	04713	MC7924CP	1	1	
Ų	12, 18	3		IC, CMOS, MEX INVERTER	381848	02735	CD4049AE	4	- 1	
Ú	13			IC,CHOS,RETRIG/RESET MULTIVIBRATOR	393512	02735	CD4098AE	1	1	
U	14		×	IC, VOLT REG, FIXED, +15 VOLTS, 1.5 AMPS	413187	04713	HC7815CT	- 1		
U	16		×	IC, VOLT REG, FIXED, -5 VOLTS, 1.5 AMPS	394551	04713	MC7905CT	;	1	
Ü	17, 20	9- 22,		IC,COMPARATOR,DUAL,LO-PWR,8 FIN DIP	478354	12040	LM393N	6	1	
Ū	24, 20	د	*		478354			,	-	
Ū	19			IC,LSTTL,QUAD 2 IN NOR GATE W/OPN COL	414037	01295	SN74LS33N	1	2	
U	23. 25	5, 27		ISOLATOR, OPTO, LED TO TRANSISTOR	380014	01295	T1L116	33	- !	
VR		2, 8	H	ZENER, UNCOMP, 16.0V, 5Z, 7.8MA, 0.4W	325837	04713	1 N946B	3		
VR		7		ZENER, UNCOMP, 5.6V, 5%, 20.0MA, 0.4W	277236	07910	1N752A	2 3	1	
VR		6	*	ZENER, UNCOMP, 22.0V, 5%, 11.5MA, 1.0W	483824	12969	U28722	3 3	1	
VR	10-12	2		ZENER,UNCOMP, 15.0V, 5%, 8.5MA, 0.4W	266601	04713	1N965B	د ،	1	
VR	13		H	ZENER, UNCOMP, 38.0V, 5%, 7.0MA, 1.0W	284364	12969	UZ8734		1	
XF	2			FUSÉ,CLIP,PCB,1/4X1-1/4	756460	89536	756460	4		

N

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Figure 5-11. A10 Inside Regulator PCA

			(SEE FIGURE 5-12.)						N
REF DES A->	ERENCE IGNATOR NUMERIC	s>	SDESCRIPTION	FLUKE STOCK ND	MFRS SPLY CODE~	MANUFACTURERS Part Number or generic Type	TOT RTY		0 T
c	i- 4		CAP,CER.0.05UF,+-20%,100V,Z5V SURGE PROT.230V,+-15% FUSE,1/4 X 1-1/4,SLOW,5A,250V FUSE,PICO,FAST,10A,125V	149161	56289	55C23A1	4		
C E	t		SURGE PROT.230V.+-15%	500363	25088	B1-A230	1	50	
F	2		FUSE 1/4 X 1-1/4.SLOW, 5A.250V	107215	71400	ndas	1		
F	3-12		FUSE PICO, FAST, 10A, 125V	615443	71400	GFA	10	10	
F	13. 14		FUSE, 0.19X0.60, SLOW, 2A, 250V, FIGTAIL	806349	89536	806349	2		
F	15		FUSE, PICO, FAST, 2A, 125V	696450	71400	GFI-SAMAX	í	10	
F	16, 19	. 20.	FUSE PICO FAST 1A 125V	696435	71400	GFI-SAMAX	5	5	
F	27, 28			696435					
F	17, 18		FUSE.PICO.FAST.3A.125V	460915	71400	GFA3	2	5	
F	23, 24		FUSE.0.275 X 1.275, FAST, 5A, 125V	713859	71400	NDV	2 2 2	25	
f	25, 26		FUSE, PICO, FAST, 3A, 125V FUSE, 0.275 X 1.275, FAST, 5A, 125V FUSE, PICO, FAST, 1.5A, 125V SCREW, HACH, PHP, STL, 6-32X5/16	655316	71400	GFI-SAMAX	2	10	
н	1		SCREW, HACH, PHP, STL, 6-32X5/16	152157	89536	152157	4		
н	2		SCREW, MACH, PHP, STL, 8-32X3/8	114124	89336	114124	8		
М	3		WASHER FLAT, STEEL, \$10,0,031 THK	110262	89536	110262	4		
н	4		WASHER, FLAT, FIBER, ¢10,0.063 THK	410346	89536	110346	4		
H	5		SCREW, MACH, RHS, STL, 10-32X2-1/4 Insulator XFMR Can	658500	89536	658500	4		
MF	1		INSULATOR XFMR CAN	632216	89536	632216	1		
MP	3 4 5 1 2		INSULATOR XFMR CAN Sleevpvc,0.186ID,Cléar		69536	113829			
MP	2 3		SLEEV.PVC.0.263ID.CLEAR	113977	89536	113977		10	
MP	4		MAIN XEMR BRKT BOTTOM	606194	89336	606194	1		
MP	5		GROMMET, RUBBER	100073	83330	2149	6		
MP	6		MAIN XEMR BRKT TOP	606210	89536	606210	1		
MP	7		CAN-MAIN-XFMR	634758	89536	634758	1		
MP	8		SLEEV.PVC,0.133ID.CLEAR	190306	89536	190306	5		
MP	Ŷ		MAIN XFMR ANGLE BRKT	606301	89536	606301	4	10	
R	2. 3		RES.WW.4.99.+-1%.2.5W	655019	89536	655019	2	1	
RY	2		SLEEVPVC,0.1861D,CLEAR SLEEV,PVC,0.2631D,CLEAR MAIN XFMR BRKT BOTTOM GROMMET, RUBBER MAIN XFMR BRKT TOP CAN-MAIN-XFMR SLEEV,PVC,0.1331D,CLEAR MAIN XFMR ANGLE BRKT RES,WW,4.99,+-12,2.5W VARISTOR,209V,+-202,1.0MA SWITCH,SLIDE,DPDT,POWER TRANSFORMER FOWER	500355	09214	V130LA10A	1		
\$	1- 3		SWITCH.SLIDE, DPDT.FOWER	234278	89536	234278	3		
T	+		TRANSFORMER FOWER	617332	89536	617332	1		
XF	2		FUSE, CLIP, PCB, 1/4X1-1/4	756460	87536	756460	2		

# TABLE 5-12. A11 GUARDED TRANSFORMER TERMINATION PCA (SEE FIGURE 5-12.)



Figure 5-12. A11 Guarded Transformer Termination PCA

	(SEE FIGURE 5-13.)						
REFERENCE DESIGNATOR A->NUMERICS>	SDESCRIPTION	FLUKE STOCK	MFRS SPLY Code	MANUFACTURERS Part Number 	TOT QTY	R S - Q	N 0 7 
	CAP, AL, 50000UF, +100-102, 15V	423525	56289	36DX503G015BC2B	1		
čż	CAP, AL, 2200UF, +75-20%, 16V	364182	25088	B41010/2000/15	1		
Č 5, 14, 15	CAP, AL, 220UF, +75-202, 100V	381947	74840	TTA	3		
C 6	CAP, AL, 100UF, +75-20%, 80V	381939	74840	TTA	1		
Č 7, 8	CAP, AL, 2100UF, +75-102, 40V	248666	56289	39D218G040JP4	2		
Č 10	CAP, AL, 150UF, +50-102, 63V	170274	80031	3070	1		
C 1 C 2 C 5, 14, 15 C 4 C 7, 8 C 10 C 11, 12, 19,	CAP, AL, 100UF, +50-102, 40V	236919	73445	ET101X040A6	4		
C 20	,,	236919					
CR 1, 2	* DIODE,51, 200 PIV, 3.0 AMP	331090	14099	3SH2	2		
CR 3- 8	* DIODE, SI, 100 PIV, 1.0 AMP	343491	01295	1N4002	6	1	
CR 9-11, 15,	* DIODE, SI, RECT, BRIDGE, BV×200V, IQ=1,0A	296509	09423	FB200	5	2	
CR 18	*	296509					
MP 1	COMPONENT HOLDER	104794	98159	2829-115-3	7		
MP 2	EJECTOR, PCB. 1/16IN. NOM	494724	32559	CP66	2		
HP 3	CABLE TIE,8*1,0.091*W,2.0 DIA	331157	89536	331157	2		
MP 4	TAB-CAP-MOUNT	607952	89536	607952	2		
R 1, 2	RES, CC, 470, +-10%, 1W	109710	01121	GB	2		
R 5	RES, CC, 10K, +-10%, 1W	109389	44655	GB	1		
R 6	RES, CC, 5, 1K, +-5%, 0, 5W	107108	01121	EÐ	1	1	
R 7- 9,15	RES, CC. 5.1K, +5%, 1W	109918	01121	GB	4		
R 10, 11	RES, CC, tok, +-5%, 0.5W	109165	01121	EB1035	2		
R 22-33	RES, CF, 1K, +-5%, 0.25W	343426	80031	CR251-4-5P1K	12		
TP 1-19	TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889	02660	62395	19		



Figure 5-13. A12 Filter A PCA

### TABLE 5-14. A13 FILTER B PCA (SEE FIGURE 5-14.)

				(SEE FIGURE 5-14.)						
DES A->	ERENCE IGNATOR NUMERICS		S	DESCRIPTION	FLUKE STOCK	MFRS SPLY Code-	MANUFACTURERS Part Number Or generic type	TOT QTY	R 5 -Q	т
С	12, 13			CAP, AL, 470UF, +30-20%, 80V	E74440			2		
С	16			CAP, POLYES, 0.33UF, +-20%, 2000V	423301	84411	X675HV	ŧ		
С	ខេ			CAP,AL,1700F,+30-202,30V CAP,AL,10000UF,+30-202,2000V CAP,AL,10000UF,+30-202,35V CAP.AL,1700UF,+75-102,100V	614990	89536	614990	1		
С	21, 22			CAP, AL, 1700UF, +75-10%, 100V	423541	56289	36D172G100AB2B	2 2		
CR	1, 2		×	DIODE.SI, 100 PIV, 1.0 AMP	343491	01295	1N4002	2	- 2	
CR	17		¥	DIODE, SI, RECT, BRIDGE, BV# 50V, 10#6.28A	428839	09713	MDA970-1	1	- 1	
CR	19- 22,	27		DIODE, SI, RECT, BRIDGE, BV=200V, IO#1.0A	296509	09423	FB200	5	1	
ČŔ	23- 26			DIODE, SI, HIGH VOLTAGE, 2K PIV, 40 MA	418616	83003	VA20X	4	1	
н	1			SCREW, MACH, PHP, STL, 6-32X1/4	152140	89536	152140	6		
H	2			SCREW, MACH, PHP, STL, 4-40X1-1/2	154380	73734	19032	2		
н	3			NUT, HACH, HEX, STL, 4-40	110635	89536	110635	2		
Ĥ				SCREW, MACH, PHP, STL, 6-32X3/8	152145	89536	152165	2422		
MF	4 1			HEATSINK	342675	13103	6003-B-2	2		
MF	2			HEATSINK	352765	91502	PA1-1CB			
MP	3			HOUSETAIL, 02829-115-4, HOLE SIZE .067	422907	89536	422907	- 11		
MF	4			SPACER . SWAGED , RND , BRASS , 6-32X0 . 100	352021	89536	352021	10		
MP	5			SPACER, SWAGED, RND, BRASS, 6-32X0.437	423806	89536	423806	4		
MF	6			TAB-CAP-MOUNT	607952	89536	607952	4		
Q			×	THYRISTOR, SI, TRIAC, VBO=200V, 8.0A	413013	02735	T2800B	8		
ହି	9, 11			TRANSISTOR, SI, BV=100V, 20, T0-220	454041	04713	MJE15029	2	2	
ê.	10, 14			TRANSISTOR, SI, BV=100V, 40W, TD-220	454033	04713	MJE15028	2	2	
ନି	12			TRANSISTOR, SI, BV=250V, 200W, TO-3	586792		MJ15012	1	ſ	
Q.	13			TRANSISTOR, SI, BV=250V, 200W, TO-3	586800		HJ15011	f	1	
Ř	1, 2			RES, CF, 100, +5%, 0.25W	348771	80031	CR251-4-5F100E	2		
R	3, 4			RES, CC, 5.1K, +-5%, 1W	109918	01121	GB	2 2 3		
R	5-7			RES, CC, 330K, +-5%, 1W	109777	01121	GB3345	3		
Ř	8				107742	01121	KB	1		
R	14			RES, CC, 1K, +-10%, 1W	109371	01121	GB1021	i i		
R	16, 18			DEC. ME. 200.4.(7.0.5W.100PPM	151480	91637	CMF651-2-12200E	1 2 2		
R	17, 19			RES, MF, 200, +-12, 0.5W, 100PPM RES, CC, 18K, +-102, 1W	109447	01121	GB1831	2		
R	20, 21			RES, WW, 0.33, +-5%, 2W	219402	75042	BMH	23		
R	22- 24			RES, CF, 1K, +-5%, 0.25W	343426	80031	CR251-4-5P1K	3	t	
T	1			TRANSFORMER HIGH VOLTAGE	617316		617316	ĩ		
TF	1- 4			TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889	02660	62395	4		
ย่	1~ 4			ISOLATOR, OPTO, TRIAC DRIVER	586826	04713	NOC3011	ė	1	
VR	1, 2			ZENER, UNCOMP, 5.6V, 5%, 20.0MA, 0.4W		07910	1N752A	2	- 1	
VR	3, 4			ZENER, UNCOMP, 140.0V, 5%, 1.8MA, 1.0W	340703	12969	UZ0114	22	i	
¥17	a, 4		1	Frueviouscus, Lagrad, Swy (10000) (100	0-14140	12/4/		-	,	

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Figure 5-14. A13 Filter B PCA

# TABLE 5-15. A14 GUARD CROSSING PCA (SEE FIGURE 5-15.)

					(SEE FIGURE 5-15.)						
DES Am		TOR RICS			DESCRIFTION-			MANUFACTURERS PART NUMBER OR GENERIC TYPE	TOT QTY	R S Q	N О Т —Е
С С	í- 27,	24,	26, 35,		CAF, CER, 0.22UF, +-20%, 50V, 25U	519157 519157		RPE11125U224M50V	31		
Ç	37					519157					
Ċ		36				613984		6f 3984	2		
ų,		29			CAP, AL, 6.8UF, +-20%, 16V	613992	89536	613992	2		
С Ф <i>5</i>	-	31				362749			2		
	1	2		*		534859					
L MP	1, 1	~			CHOKE, 6TURN	320911	89536	320911	2		
MP	2					541284		541284	1	1	
MF	3					494724		CP66	2		
Ŕ	š				HOUSETAIL,+2829-75-3.HOLE SIZE .046 RES.CF,20K,+-5%,0.25W			422873	1	1	
R		3.	5,		RES, CF, 1K, +-5%, 0.25W	441477 343426		CR251-4-5220K	1		
R	20	Ξ,			Neb)er/18/1 5%,01250	343420	80031	CR251-4-5P1K	4		
R		18			RES,CF,1M,+~5%,0.25W	348987	80031	CD254-4-5049			
R	6	•••			RES, CC, 120, +-10%, 0.5W	108696	01121	CR251-4-5P1H EB1211	2		
R		8,	17		RES, CF, 10K, +-5%, 0, 25W	348839	80031	CR251-4-5P10K	ż		
R			12,			441436	80031	CR251-4-5P180E	6		
R		16,				441436	00001	01201-4-011002			
S	1	3			SWITCH, SLIDE, DPDT	707700	10389	23-021-114	3	1	
TP	1-	7			TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889	02660	62395	7	•	
u	1,	20,	21		IC, CHOS, HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	ż	1	
U	2,	11		×	IC, TTL, MEX INVERTER W/OPEN COLLECTOR	407593	01295	SN7406N	3 2	í	
U	3			- #	GUARD MICROCOMPUTER BUILD DRAWING	704189	89536	704189	Ŧ	i	
U	4			- #	IC,LSTTL,HEX INVERTER W/SCHMT TRIG	483180	01295	SN74LS14N	÷.	Ť	
U	5				IC, CMOS, MONOSTABL/ASTABL MULTIVIBRATR		12040	CD4047B	í	1	
U	4-	9,	23	- #	ISOLATOR, OPTO, HI-SPEED, LED TO XSISTOR	407742	28480	HP5082-4351	5		
U	10				IC,LSTTL,QUAD 2 INPUT NOR GATE	393041	01295	SN74LSO2N	5 1	1	
U U	12				IC,LSTTL,QUAD 2 INFUT OR GATE	393108	01295	SN74LS32N	1	1	
U.	13				IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	1	1	
U.	14				IC,LSTTL,QUAD 2 INPUT NAND GATE	393033		SN741-SOON	t	1	
U	15				IC, LSTTL, OCTL LINE DRVR W/3-STATE OUT			SN74LS244N	1	1	
ŭ	16				IC,LSTTL,DUAL 4 INPUT AND GATE	408708	01295	SN74LS21N	1	1	
U U	17				IC, LSTTL, OCTL BUS TRNSCVR W/3-ST OUT		01295	SN74LS245N	1		
U U	18				IC,LSTTL,HEX BUFFER W/NOR ENABLE	483800	01295	SN74LS367N	1	f	
U	19				IC, CMOS, DUAL D F/F, +EDG TRG W/SET&RST		04713		1	1	
U	22				IC, CMOS, UNIV ASYNC RECEIVR/TRANSMITER		32293	1M6402CPL	1	1	
VR	1			*	ZENER, UNCOMP, &V TRANSIENT SUPPRESSOR		24444	1N5908	1	í	
XU	1 7				SOCKET, IC, 16 PIN	276535	91506	316-AG39D	1		
XU XU	3, 6-	22	23		SOCKET, IC, 40 PIN	429282	09922	DILB40P-108	2 5		
Ŷ	- 1	7,	<i>4</i> 0		SOCKET, IC, 8 PIN CRYSTAL, 4MHZ, +-0.022, HC-10/U	478016	91506	308-AG39D	<u>,</u>		
ż	1,	3,	5	Ħ	CRYSTAL, 4HHZ, +-0.02%, HC-10/U RES, NET, DIP, 16 PIN, 8 RES, 16, +5% RES, NET, SIP, 6 PIN, 5 RES, 10K, +-2% RES, NET, SIP, 10 PIN, 9 RES, 100K, +-2% RES, NET, SIP, 10 PIN, 9 RES, 10K, +-2%	474872	89536	474072	1		
z	2	Ψ,	-		REC NET CIP & DIN C DEC (AV )	358119	01121	314	3		
7	4				REC NET CID (A DIM O DEC (ADAV 1207	200070	80031	95081002CL	1		
Z Z	2,	7			RES, NET, SIP, 10 PIN, 9 RES, 100K, +-22 RES, NET, SIP, 10 PIN, 9 RES, 10K, +-22	401038	80031	95081002CL	1	,	
ż		10			NEW/NET/J2/// V/ IN/// NE3/ VK/+-2/	41 4003 484063	80031 80031	95081002CL	2	í	
ź	9'				RES, NET, SIP, 6 PIN, 5 RES, 4.7K, +-22	484065	80031	95081002CL			
	•					779070	0003	95081002CL	1		





### TABLE 5-16. A15 MEMORY PCA (See Figure 5-16.)

			(SEE FIGURE 5-16.)						
D	REFERENCE DESIGNATOR A->NUMERICS>		NATOR		MFRS SPLY Code-	HANUFACTURERS Part Number or generic type	TOT	R 5 Q	N T T
C C	1- 15, 19- 21, 24- 34		5, 92, 97.2207, 1° 20%, 307, 230	810101	71400	RPE111Z5U224M50V	29		
C C	35		CAP,AL,47UF,+-20%,10V	613984	89536	613984	f		
C	38		CAP, POLYES, 0. 120F, +-52, 100V	461582	73445		- i		
Ċ	२ १		DIODE, SI, BV= 75.0V, IO= 50MA, 500 MW	203323	07910		i	1	
Ē	2		JUMPER, REC, 2 POS, . 100CTR, .025 SQ POST		00079		ŕ	-	
J			PIN,SINGLE,PWB,0.025 SQ	267500	00779		ż		
M	° 1		EJECTOR, PCB, 1/16IN. NOM	494724	32559		3 2		
R	15		RES, MF, 37.4K, +-12, 0.125W, 100PPM		91637	CMF553742F	ĩ		
R	16		RES, MF, 15K, +-12, 0.125W, 100PPM	285296	91637		i	í	
R	18		RES.CF.1K.+~52.0.25W	343426	80031	CR251-4-5P1K	i i	•	
ΤI	<b>1-5</b>		TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889	02660		5		
U	1	H	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	1		
U	2- 4, 24		IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035	01295	SN74LS244N	4	1	
U	5		IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74L500N	1	- i	
Ü	6	×	IC,LSTTL,RUAD 2 INPUT NOR GATE	393041	01295	SN74LS02N	Í	1	
Ų	8, 9, 20	×	IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	3	1	
U	10	×	MAIN EPROM 1 BUILD DWG V2.1	813006	89536	813006	1	1	
u	11	*	MAIN EPROM 2 BUILD DWG V2.1	812014	89536	812014	í		
U	12	×	MAIN EPROM 3 BUILD DWG V2.1	813022	89536	813022	Í.	1	
U	13	ŧ.	MAIN EPROM 4 BUILD DWG V2.1	813030	89536	813030	1	í	
U	14	×	MAIN EPROM 5 BUILD DWG V2.1	813048	89536	813048	1	- <b>f</b> -	
U	15	*	MAIN EPROM & BUILD DWG V2.1	813055	89536	813035	í	1	
U	19	×	IC,LSTTL,QUAD 2 INPUT NAND GATE IC,LSTTL,QUAD 2 INPUT NAND GATE IC,LSTTL,QUAD 2 INPUT NOR GATE IC,LSTTL,QUAD 2 INPUT NOR GATE MAIN EPROM 1 BUILD DWG V2.1 MAIN EPROM 2 BUILD DWG V2.1 MAIN EPROM 3 BUILD DWG V2.1 MAIN EPROM 4 BUILD DWG V2.1 MAIN EPROM 5 BUILD DWG V2.1 IC,LSTTL,QUAD 2 INPUT OR GATE IC,TTL,QUAD 2 INPUT OR GATE IC,TTL,QUAD 2 INPUT AND GATE IC,TTL,OCTAL D F/F.+EDG TRG	393108	01295	SN74LS32N	f	1	
ų	21	×	IC,TTL,QUAD 2 INPUT AND GATE	393066	01295	SN74LS08N	1	1	
U	25, 26	¥	IC,TTL,OCTAL D F/F,+EDG TRG IC,LSTTL,QUAD D F/F,+EDG TRG,W/CLR IC,LSTTL,QUAD SET/RESET LATCH IC, 2K X 8 EAROM	473223	01295	SN74LS374N	2	ſ	
บ	27		IC,LSTTL,QUAD D F/F,+EDG TRG,W/CLR	393215	01295	SN74LS175N	í	1	
U U	28		IC,LSTTL,QUAD SET/RESET LATCH	404210	01295	SN74LS279N	ŧ	1	
ម	29	*	IC, 2K X 8 EAROM	585794	51157		1	+	
U	30- 32	×	IC, 2K X 8 STAT RAM	584144	33297	uPD4016C-2	3	1	
ប	33	×	IC,LSTTL,HEX BUFFER W/NOR ENABLE	483900	01295	SN74LS367N	\$	t	
×	1 4		SOCKET, IC, 24 PIN	376236	91506	324-AG39D	4		
ž	5~ f0		SOCKET, IC, 28 PIN	376236 448217	91506	328-AG39D	6		
Z	1		RES, NET, SIP, 10 PIN, 9 RES, 100K, 4-2X	461038	80031	95081002CL	1		
Z	2		RES,NEG,SIP,8 PIN,7 RES,1K,+-2%	414557	80031	95081002CL	1		
Z	3- 5		RES,NET,SIF,10 PIN,16 RES,330/680,5%	520429	01121	1-SIF-400E	3	1	



5440B/AF

# TABLE 5-17. A16 CONTROLLER PCA (SEE FIGURE 5-17.)

REFERENCE Designato A>Numeri	r C\$>	SDESCRIPTION	FLUKE STOCK	MFRS SFLY Code	MANUFACTURERS PART NUMBER DR GENERIC TYPE	TOT QTY	R 5 -Q
C 1 C 10- 1 C 19, 2 C 24, 2 C 29, 3 C 36, 4	4, 8, 6, 18, 1, 22, 5, 27- 2, 34, 0- 42	CAP,CER,0.22UF,+-20%,50V,Z5U	519157 519157 519157 519157 519157 519157 519157	51406		29	
C 7	_		160317	02799	DM15E330J	1	
C 38, 3	ዋ	CAP, AL, 10UF, +-20%, 35V	603985	74840	RLR	2	
C 43 C 44, 4	w.	CAP,CER,1.0UF,+-202,50V,25U	436782	72982	8131-050-601-105M	1	
C 44,4 CK 1		CAP,CER,220PF,+-2%,100V,COG * DIODE,S1, 100 P1V, 1.0 AMP	512111 343491	51406	RPE121 1N4002	2	4
	5	* LED,RED,FCH MOUNT,LUM INT#2.0MCD	534859	20480	HLMP3301/5082-4655	4	1
É4,		JUMPER, REC, 2 POS, . 100CTR, . 025 SQ POST		00079	530153-2	2	•
J 1- 4	6	PIN, SINGLE, PWB, 0.025 SQ	267500	00779	87022-1	6	
MP ( MP 2		CONTROLLER	582510	89536	582510	1	
MP 2 Q 1		EJECTOR,PCB.1/16IN. NOM * TRANSISTOR,SI,NPN,SMALL SIGNAL	494724	32559	CP-66	2	
	0, 21	RES, CF, 100, +-52, 0.25W	218396 348771	04713 80031	2N3904 CR251-4-5P100E	1 3	í
R 2		RES, CF, 51, +5%, 0.25W	414540	80031	CR251-4-5P51E	1	
	9, 17,	RES,CF,4.7K,+-5%,0.25W	348821	01121	CB4725	5	
<u>Ř</u> 22, 2-	4		348821				
R 4 R 5., 4	,	RES,CF,1.5K,+~5%,0.25W	343418	80031	CR251-4-5P1K5	1	
R 5, 4 R 8	9	RES,CF,10K,+-5%,0.25W RES,CF,8.2K,+-5%,0.25W	348839	80031	CR251-4-5P10K	2	
R 15, 14	6	RES,CF, (M, +-52, 0.25W	441675 348987	80031 80031	CR251-4-5P8K2 CR251-4-5P1M	1 2	
R 19		RES, CF, 180, +-52, 0.25W	441436	80031	CR251-4-5F180E	ī	
R 23		RES.CF,1K,+52,0.25W	343426	80031	CR251-4-5P1K	i	
<u> </u>	-	SWITCH, MODULE, SPST, DIP, 4 POS	408559	00779	435166-2	t	
	7	TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889	02640	62395	?	
U 1 U 2		OSCILLATOR, 8MHZ, TTL CLOCK * IC, TTL, HEX INVERTER W/OPEN COLLECTOR	584169 407593	07767	X0-33D-15-8-MHZ	1	
<u>-</u>	4	* IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295 01295	SN7406N SN74LS74N	2	1
U 5		* IC, LSTTL, QUAD 2 INPUT NAND GATE	393033	01295	SN74LSOON	ĩ	i
U 6		* IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	i i	-i -
ย ย 10		* IC, DUAL DIV BY 16 BINARY COUNTER	483578	01295	SN74LS393N	1	1
U 11		* IC,LSTTL,QUAD 2 IN NAND W/SCHMT TRIG * IC,NMOS,8 BIT MICROCOMPUTER	504449 478073	01295 50088	SN74LS132N	1	ţ
ū 12, 18	3	* IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	MK3880-4CPU SN74LS138N	ż	1 1
U 13		* IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	1	i
U 14-16 U 34	5, 24,	* IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035 429035	01295	SN74LS244N	5	1
U 17, 27 U 32, 37		* IC,LSTTL,QUAD 2 INPUT OR GATE *	393108 393108	01295	SN74LS32N	5	1
Ŭ 19	•	* IC,NMOS PROGRAMMABLE INTERVAL TIMER	584177	33297	uPD8253C		1
U 20		* IC,LSTTL,8-3 LINE PRIORITY ENCOR,3-ST	483669	01295	SN74LS348N	i	i
U 21		* IC, LSTTL, HEX BUFFER W/NOR ENABLE	483800	01295	SN74LS367N	1 i s	í
U 22 U 23		* IC,LSTTL,QUAD SET/RESET LATCH	404210	01295	SN74LS279N	1 .4	í
U 23 U 25		* IC,LSTTL,QUAD D F/F,+EDG TRG,W/CLR * IC,CMOS,UNIV ASYNC RECEIVR/TRANSMITER	393215	01295	SN74LS175N	1.	
Ŭ 26		* IC,LSTTL,TRIPLE 3 INPUT NOR GATE	393090	32293 01295	186402CPL SN74LS27N	1	1
Ū 28		* IC,LSTTL,QUAD DIFFERENTIAL LINE DRVR	525295				1
U 29			525303	12040	DS3486N	i	i
U 30		* IC, CHOS, MONOSTABL/ASTABL MULTIVIBRATR	535575	12040	CD4047B	t	1
U 35 U 36		* IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	1	1
U 36 XU (1, 25		* MAIN EFROM 0 BUILD DWG V2.1 Socket.ic,40 Fin	812990	89536 09922	812990 DILB40P-108	í	í
XU 19	r	SOCKET, IC, 24 PIN	429282 376236	91506	324-AG39D	2 1	
XU 36		SOCKET, IC, 28 PIN	448217	91506	328-AG39D	i	
Z <u>1</u> , 3	5	RES,NET,SIP, to PIN,9 RES,4.7K,+-2%	484063	80031	95081002CL	2	1
Z 2		RES, NET, SIP, 10 PIN, 9 RES, 10K, +-2%	414003	80031	95081002CL	1	
Z 4 Z 5		RES,NET,SIP,8 PIN,7 RES,4.7K,+-2% RES,NET,SIP,8 PIN,4 RES,220,+-2%	412916	80031	95081002CL	1	
z ő		RES,NET,SIP.6 PIN.5 RES.4.7K.+-22	529511 494690	80031 80031	95081002CL 95081002CL	1 1	
·						•	

N T O T E



Figure 5-17, A16 Controller PCA

					(SEE FIGURE 5-18.)						
	EREN					FLUKE	MFRS	MANUFACTURERS		Ŕ	0 T
	NUME	RICS			DESCRIPTION		CODE~			Q	-E
С	í.	15,		-	CAP. CER. 0.22UF. +-20%.50V.75U	309849	71590	CW3COC224K	3		
ĉ		16			CAP, CER, 0.22UF, +-202, 50V, Z5U CAP, AL, 47UF, +-202, 35V CAP, TA, 1UF, +-102, 35V CAP, TA, 1UF, +-102, 35V CAP, AL, 100UF, +75-102, 16V CAP, AL, 100UF, +50-202, 50V CAP, AL, 100UF, +50-202, 50V	603977	74840	RLR	2		
C	3				CAP, TA, 1UF, +-102, 35V	161919	56289	196D010X0035G	1		
0000	4				CAF, AL, 100UF, +75-102, 16V	436014	62643	SL	1		
c	5		~~		CAP, AL, 6.8UF, +-20%, 16V	613992	89536	613992	<u></u>		
C		19,	20		CAP, AL, 1000F, 100-20%, 50V	647731 487007	89536 89536	649731 603993	3 2		
č		11 12,	13		ELECTRD, MIN,LO LEAK, 4.7MF, 35V CAP,AL,22UF,+-20%,50V	603993 614362			3		
č	14				CAP, CER, 1200PF, +-202, 100V, X7R	358283		8121-A100-W5R-122M	š		
ç	18				CAP,AL,1UF,+-20%,50V	602342	62643		- i		
CŔ		8,	13	×	DIODE,SI, 400 PIV, 1.0 AMP DIODE,SI,BV= 75.0V,IO=150MA,500 MW	368738		1 N 4 0 0 4	9	1	
CR	-	11						1N4448	3	1	
CR F	12			*	LED,RED,CLIP,MOUNT,LUM INT=0.8MCD			NLS5053	1	1	
ĥ	1				FUSE,1/4 X 1-1/4,FAST,4A,250V SCREW,MACH,PHP,STL,6~32X5/16			AGC4A250V 152157	10		
н	ż				SCREW, MACH, PHP, STL, 6-32X3/8			152165	4		
Ĵ	1,	2			SOCKET, SINGLE, PWB, FOR 0.018-0.040 PIN				4	5	
MP	2				HEAT SINK, FOR USE WITH TO-3 6051B	508200	89536	508200	1		
MP	3				HEATSINK	352765		PA1-1CB	4		
MP	4				HEATSINK-OUTSIDE-REG			618801	1		
MP MP	7				EJECTOR, PCB, 1/16IN, NOM SPACER, SWAGED, RND, BRASS, 6-32X0, 100	494724 352021	32559 89536	352021	14		
Q	í			×	TRANSISTOR, SI, BV# 50V, 117W, T0-3	103012			1	í	
	2				THYRISTOR, SI, TRIAC, VBO=400V, 8.0A			T2800D	1	i	
Q Q Q Q R R	3,	6			TRANSISTOR, SI, NPN, SMALL SIGNAL			2N3904	2	1	
Q	5			×	TRANSISTOR, SI, BV# 45V, 30W, TO-220	325761	09214	D44C5	1	1	
Q	?			Ħ	TRANSISTOR, SI, PNP, SMALL SIGNAL	195974			1		
8	1				RES,WW,0.15,+~52,2W	325712	75042	BWH	!		
Ř	23				RES,0W,0.15,7+57,2W RES,CF,1.5K,+-57,0.25W RES,CF,54,+-57,0.25W RES,CF,1K,+-57,68.25W		80031 80031	CR251-4-5P1K5 CR251-4-5P56E			
Ř		5.	23-		RES.CF.1K.+=52.0.25W	343426	80031	CR251-4-5F\$8	ื่อ		
R	27,		-,			343426		0.201 1 51 76	-		
R			10		RES, CF, 100K, +-5%, 0.25W	348920	80031	CR251-4-5P100K	3		
R		11,	55,		RES, CF, 100K, +-5%, 0.25W RES, CF, 3K, +-5%, 0.25W	441527	80031	CR251-4-5P3K	4		
R	56					441527	00074	00064-4-6044			
R	9 16				RES,CF,1M,+-5%,0.25W RES,MF,237,+-1%,0.125W,100PPM RES,MF,3.92K, +/-1%,0.5W,100PPM	348787	80031 91637	CR251-4-5F1M CMF552370F			
Ŕ	17				RES.MF.3.92K. +/-12.0.5W.100PPM	160713	89536	160713			
R	19,	22			RES, VAR, CERM, 1K, +-10%, 0.5W	285155	71450	360S102A	2	1	
R			41,		RES, MF, 1.43K, +-1%, 0.125W, 100PPM	325662	91637	CMF551431F	4		
R	42					325662					
R	21				RES, MF, 4.75K, +-12, 0.125W, 100PPM	260679	91637	CMF554751F	1		
R R	30	38,	30		RES,MF,24.2K,+/-1%,0.125W,100PPM RES,MF,12.1K,+-1%,0.125W,100PPM	236745 234997	89536 91637	236745 CKF551212F	3		
R	32	,	9,		RES, MF, 20.5K, +/-12, 0.125W, 100PPM		89536	261669	ĭ		
R	33				RES, MF, 3.48K, +-12, 0.125W, 100PFM	269687	91637		1		
R		40,			RES, MF, 10, 5K, +-1%, 0.125W, 100PPM			CMF551052F	3		
R		44,						CR251-4-5P5K1	3		
R		45,	53		RES, CF, 2, 2K, +-5%, 0, 25W	343400	80031	CR251-4-5P2K2	3 2		
R R	46, 48,				RES, MF, 4.99K, +–12, 0.125U, 100PPM RES, MF, 4.42K, +–12, 0.125U, 100PPM	168252 288514	91637	MFF1-84991 CMF554421F	2		
Ř	49,				RES,MF,604,+-1%,0.125W,100PPM	320309	91637	CMF556040F	2		
R	54				RES, CF, 330, +-5%, 0.25W	368720	80031	CR251-4-5P330E	1		
R	57				RES, CF, 39, +5%, 0.25W	340836	80031	CR251-4-5839E	1		
TP	<b>1</b> -	6,	8		TERM, UNINSUL, FEEDTHRU, HOLE, TURRET	179283	88245	20108-5	?		
U U	1				IC, VOLT REG, ADJ, 2 TO 37 VOLT, 0.15 AMP	379420	04713	MC1723CL	1	1	
U U	23				IC,CMOS,RETRIG/RESET MULTIVIBRATOR IC,CMOS,HEX INVERTER	393512 381848	02735 02735	CD4098AE CD4049AE	1	1	
Ŭ	5				IC, VOLT REG, FIXED, +12 VOLTS, 1.5 AMPS	413195	04713	MC7812TP	i	i	
Ũ	- 6				IC, VOLT REG, HIGH VOLTAGE	723353	89536	723353	i	1	
U	7			¥	IC, VOLT REC, FIXED, -12 VOLTS, 1.5 AMPS	381665	04713	MC7912CP	1	1	
U.	8				IC, VOLT REG, FIXED, -5 VOLTS, 1.5 AMPS	394551	94713	MC7905CT	1	1	
Ü	. 9	40			IC, VOLT REG, FIXED, +5 VOLTS, 1.5 AMPS	355107	12040	LM340T-5	1 3	1	
U U	10 13	12			IC,COMPARATOR,DUAL,LO-PWR,8 PIN DIP IC,LSTTL,HEX INVERTER	478354 393058	12040 01295	LM393N SN74LS04N	1	÷	
ŭ	14				IC,TTL,TRIPLE 3 INPUT NOR GATE	392951	01295	SN7427N	i	i	
- VR	1				ZENER, UNCOMP, 5.6V, 5%, 20.0MA, 0.4W	277236	07910	1N752A	1	2	
VR	2.	3		¥	ZENER, UNCOMP, 6.8V, 5%, 37.0MA, 1.0W	454595	12969	UZ8706	2	1	
XF	1				HLDR, FUSE, 1/4, PWB MT	485219	91833	3529	2		

## TABLE 5-18. A17 OUTSIDE GUARD REGULATOR PCA (SEE FIGURE 5-18.)





REFERENCE DESIGNATOR A->NUMERICS>		>	5	DESCRIPTION	FLUKE STOCK NO	MFRS SPLY CODE-	MANUFACTURERS Part Number Or generic Type	TOT QTY	R 5 -Q	N O T -É	
с с с		3, 16,	5- 18-		CAP, CER, 0.22UF, +-202, 50V, 25U	519157 519157 519157		RPE111Z5U224N50V	32		
С	34				CAP, AL, 47UF, +-20%, 10V CAP, CER, 56PF, +-2%, 100V, COG	613984	89536	613984	1		
С	37, 3	38			CAP, CER, 56PF, +-2%, 100V, COG	512970	51406	RPE121	2		
F	1				FUSE, 1/4 X 1-1/4, FAS, 0, 25A, 250V	109314	71400	AGC1-4	1		
н	1				SCREW, MACH, PHP, STL, 6-32X1/4	152140	89536	152140	10		
J	9				SOCKET.2 ROW.PWB.0.100CTR.50 POS	519538	00779	86418-8	1	5	
۴.,	Α,	5			CHOKE, GTURN	320911	89536	320911	2		
MP	1				HLDR,FUSE,1/4,PWB MT	485219	91833	3529	2	1	
MP	2				BULKHEAD-1/0	637967	89536	637767	1		
R	េ				SUCKEW, MHUM, FMF, 311, 342, 342, 344 SOCKET, 2 ROW, PWB, 0, 100CTR, 50 POS CHOKE, 4TURN HLDR, FUSE, 1/4, PWB MT BULKHEAD-1/0 RES, CC, 10, +-5%, 0, 25W RES, CC, 10, +-5%, 0, 25W RES, CC, 10, +-10%, 25W TERM, FASTON, TAB, SOLDR, 0, 110 WIDE	108597	01121	CB1025	1		
R	2				RES, CC, 10M, +-5%, 0, 25W	194944	01121	CB1065	1 2 1		
R		9			RES,CF,1K,+-5%,0.25W	343426	80031	CR251-4-5P1K	2		
R	4				RES, CC, 10, +-10%, 2W	110163	01121	HB			
ΤP	i	5			TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512889	02660	62395	5 1		
U	1			×	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	1		
ប	2,	3		×	IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035	01295	SN74LS244N	2	1	
υ	5			¥	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	ŚN74LSOON	1	1	
U	6				IC.LSTTL.QUAD 2 INPUT NOR GATE	393041	01295	SN74LS02N	1	1	
U	7			*	IC,LSTTL,8 INPUT NAND GATE	404889	01295	SN74LS30N	1	1	
Ð	8			¥	IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	i	1	
Ð	9,1	13,	22-		IC, CMOS, HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	6	1	
U	25	-		×		407759					
U	10, 1	i 8		×	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	2	1	
υ	11				IC, CMOS, UNIV ASYNC RECEIVR/TRANSMITER	453464	32293	1M6402CFL	i	1	
Ð	12			×	IC, CMOS, PROGRAMBLE BIT RATE GENERATOR	418731	07263	F4702/34702	í		
U	14			×	IC.TTL.QUAD RS232C LINE RECEIVER	414045	12040	LM1 489	í	1	
υ	15			*	IC, TTL, QUAD RS232C LINE DRIVER	414052	12040	LM1488	í	í	
U	16				IC,NMOS,GPIB ADAPTER	585240	01295	THS9914ANL	1	1	
U	17			×	IC, LSTTL, OCTAL GPIB XCVR W/OPEN COL	585224	01295	5N75160AN	1	1	
υ	19				IC, LSTTL, OCTAL GPIR ACTV FULL-UP XCVR		01295	SN75161AN	4	4	
U	20				IC, CMOS, RUAD 2 INPUT NAND GATE	418509	12940	MM74C00N	1	1	200
U	21				IC. CMOS, HEX INVERTER	404677	12040	MM74CQ4N	-1	1	
ú	26				IC.TTL.HEX INVERTER W/OPEN COLLECTOR	407593	01295	SN7406N	1	1	
Ú	27				IC,LSTTL,DUAL D F/F, +EDG TRG,W/CLR	393124	01295	SN74LS74N	1	2	
Ū	28				TC, LSTTL, QUAD D F/F, +EDG TRG, W/CLR	393215	01295	SN74LS175N	- i	1	
Ũ	29				IC.CHOS,QUAD D F/F,+EDG TRG,W/CLR	452912	12040	MM74C175N	i	í	
ΧU	<b>i</b> i, 1	i 6			SOCKET, IC. 40 PIN	429282	09922	DILB40P-108		•	
XŬ	17, 2				SOCKET, IC. 20 PIN	454421	09922	DILB20P-108	221232		
Ŷ	1			×	CRYSTAL, 2.4576MHZ, +-0.01%, HC-33/U	435370	89536	435370	៍		
ż		7		••	RES.NET.SIF.10 FIN.9 RES.10K.+2%	414003	80031	95091002CL	2		
7			10		RES, NET, SIF, 2 FIN. 7 RES, 4.7K. +-2%	412916	80031	95081002CL	ã		
Z Z	6,	9	• 4		RES.NET.DJP.16 FIN.8 RES.1K.+-5%	358119	01121	314	ž		
ź	8				RES, NET, SIF, 8 FIN, 7 RES, 10K, +-2%	412924	80031	9508100201.	ĩ		
-					in a second second second second second second second second second second second second second second second s	- F.M. 7 B. 7	· ·	·	•		

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5-52



Figure 5-19. A18 I/O PCA

					(SEE FIGURE 5-20.)						N
DES	REFERENCE Designator A->numerics>			2		FLUKE STOCK NO	HFRS SPLY Code-	MANUFACTURERS Part Number Or Generic Type	TOT QTY	R S ~Q	C T
С	í,	3			CAP, AL, 220UF, +50-10%, 63V	185850	80031	ET221X063A02	2		
С	4				CAF, AL, 2200UF, +75-20%, 16V	364182	25088	B41010/2000/15	- 1		
C C C	5,	6			CAP, CER, 0, 05UF, +-20%, 100V, 25V	149161	56289	55C23A1	2		
ĒR	ĩ	-		×	DIODE, SI, RECT, BRIDGE, BV=200V, IO=1.0A	296509	09423	FB200	1		
CR	2,	3			DIODE,SI, 200 PIV, 3.0 AMP	331090	14099	3SH2	2	1	
CR	5,	6			DIODE,SI, 100 PIV, 1.0 AMP	343491	01295	1N4002	2	1	
E	- i -	8			TERM, UNINSUL, FEEDTHRU, HOLE, TURRET	101741	89536	101741	8		
F	Í,	4			FUSE, PICO, FAST, 2A, 125V	696450	71400	GFI-5AMAX	2	íð	
F	2,	3			FUSE, 0.275 X 1.275, FAST, 5A, 125V	713859	71400	MDV	2	ίÐ	
F	5	6			FUSE PICO FAST 3A, 125V	460915	71400	GFA3	2		
. H	1				SCREW, MACH, PHP, ST, 8-32X1-3/4	602581	89536	602581	4		
н	2				SCREW, MACH, PHP, STL, 6-32X5/16	152157	89536	152157	- 4		
H	3				WASHER,FLAT,STEEL,\$8,0.031 THK	110288	89536	110288	4		
н	4				WASHER,FLAT,FIBER,#8,0.063 THK	110353	73734	1472	4		
MF	2				OUTSIDE-XFMR-BKT-A	582775	89536	582775	2		
MP	3				OUTSIDE-XFMR-BKT-B	582783	89536	582783	2		
MP	4				COMPONENT HOLDER	422865	98159	2829-75-2	3		
MP	5				CABLE TIE,4"L,0.100"W,0.75 DIA	172080	87536	172080	1		
R	1,	З,	4		RES,CC,4.7K,+-10Z,0.5W	108381	01121	EB	3	1	
R	2				RES,CC,820,+-5%,1W	266379	01121	GB8215	1		
R	6	9			RES,CF,1K,+~5%,0.25W	343426	80031	CR251-4-5P1K	4		
Ť	1				POWER TRANSFORMER, AUX	758649	89536	758649	1	- 4	
TP	1-	5			TERM, FASTON, TAB, SOLDR, 0.110 WIDE		02660	62395	5	10	
W	1				OUTSIDE TERMINATOR CABLE	617902	89536	617902	1		
ų.	2				OUTSIDE TERMINATOR CABLE	617910	89536	617910	1		

TABLE 5-20. A19 OUTSIDE GUARD TERMINATOR PCA (SEE FIGURE 5-20.)



5-54

5440B/AF



Figure 5-20. A19 Outside Guard Terminator PCA

.

REFERENCE Designator A- ) numerics)		SDESCRIPTION	FLUKE Stock NO	MFRS SPLY Code-	MANUFACTURERS Part Number Or Generic Type	ТОТ QTY	R 5 -Q	N 0 T -E
ĊR	1	* DIODE,SI, 400 PIV, 1.0 AMP	368738	04713	1N4004	1		
DS	2	* LED, GREEN, RECTANGULAR, PCB MOUNT	650879	12040	NSL54124	÷	ŧ	
MP	+	INSULATOR, POWER SWITCH	383158	89536	383158	i	•	
MP	2	SPACER, SWAGED, RND, BRASS, 6-32X0, 375	494542	89536	494542	ż		
R	1	RES, WW, 3.3K, +-5%, 3W	520536	12697	VC3D	Ē	1	
S	4	POWER SWITCH	291526	89536	291526	Í		

.

#### TABLE 5-21. A20 POWER SWITCH PCA (SEE FIGURE 5-21,)



Figure 5-21. A20 Power Switch PCA

.



					(SEE FIGURE 5-22.)						N
REFERENCE DESIGNATOR A->NUMERICS>				FLUKE MFRS Stock SFLY NO CODE-		MANUFACTURERS Part Number Or generic type	ТОТ QTY	R S -Q	0 T E		
с	i			-	CAP, TA, 6.8UF, +-20%, 35V	363713	56289	1960685X0035KA1	í		
с с с с с с с с с с с с с	5				CAP, POLYES, 0.0220F, +10%, 50V CAP, AL, 15UF, +20%, 35V	715268	89536	715268	1		
ř	2 3,	Δ			CAP AL 15UF. +-202.35V	614024	89536	614024	2		
ĉ	4	-			CAP, TA, 47UF, +-20%, 20V	348516	56289	196D476X0020TE4	1		
ř	5,	A			CAP, TA, 10UF, +-20%, 10V	176214	56289	196D106X0010KA1	2		
ř	7-				CAP, CER, 0.22UF, +-20%, 50V, Z5U	519157	51406	RPE111Z5U224M50V	7		
č	15,				CAP, TA, 4, 70F, +-20%, 50V	363721	56289	196D475X9015HA1	2		
ČR	1	10			DIODE, SI, RECT, BRIDGE, BV= 50V, IO=1.0A	418582	83003	VMOB	1	í	
CR		3			DIODE, SI, N-JFET, CURRENT REG, IF=5.3 MA	334714	07910	TCR5315	2	í	
DS	÷,				TUBE, DISPLAY, VAC FLOR, 14-SEG 12-DIGIT	741215	89536	741215	1		
DS	ż				TUBE, DISPLAY, VAC FLORESCENT, 2X20 CHAR	741223	89536	741223	1		
MP	ž				SPACER, SWAGED, RND, DRASS, 0.150IDX0.437		89536	520205	2		
MP	3				TAPE, FOAM, VINYL, ADHESIVE, TWO SIDE	756684	89536	756684			
MP	4				TAPE, FOAM, ADHESIVE-ONE OR TWO SIDES	756692	89536	756692			
Q	1,	2			TRANSISTOR, SI, NFN, SHALL SIGNAL	272237	89536	272237	2 2 1	2	
ö	ż'	4			TRANSISTOR, SI, PNP, SMALL SIGNAL	352369	12040	2N4403	2	- 1	
Q R		-			RES, MF, 2.61K, +-1%, 0.125W, 100PPM	289983	91637	CMF552611F	1	í	
R	ż,		6,		RES, CF, 1K, +-5%, 0.25W	343426	80031	CR251-4-5P1K	4		
R	7	ч,	Ψ,			343426					
R	8,	0			RES.CF,2,+-5%,0.25W	442053	80031	CR251-4-5P2E	2		
T	· · ·				TRANSFORMER, INVERTER	767129	89536	767129	1		
te -	÷	6			TERM, FASTON, TAB, SOLDR, 0.110 WIDE	512887	02660	62395	6		
U I		0			IC, REGULATING PULSE WIDTH MODULATOR	454678	01295	SG3524N	1		
บ	2	÷			IC, BIMOS, VAC FLUORESCENT DISPLAY DRVR		89536	741355	6	í	
	2	(			CABLE ASSY, FLAT, 20 CONDUCT, 4.5	714014	89536	714014	Í.		
N XU	2-	7			SOCKET.IC.40 PIN	429282	09922	DILB40P-108	6		



Figure 5-22. A22 Display PCA

TABLE 5-23.	A23 1/0	CONNECTOR	PCA
(SEE FIGURE	5-23.)		

				(SEE FIGURE 5-23.)						N
REFERENCE DESIGNATOR A->NUMERICS>		>	F S DESCRIPTION		MFRS SPLY CODE	MANUFACTURERS PART NUMBER OR GENERIC TYPE	ТОТ QTY 	R 5 -Q	0 T ~E	
CR		2		* DIODE,SI, HV= 75.0V, IO=150MA,500 MW	203323	07910	1N4448	2		
н	4	**		SCREW. CONNECTOR MOUNTING	429472	89536	429472	2		
Й	2			CONN ACC, D-SUB, JACK SCREW, 4~40	448092	89536	448092	2		
н	ŝ			WASHER,LOCK,SPLIT,STEEL,#8	111070	89536	111070	2		
14	4			SCREW, MACH, PHP SEMS, STL, 4-40X1/4	185918	89536	185918	8		
1	1			CONN, MICRO-RIBBON, REC, PWB, 24 FOS	441337	02660	57-20240-8	1		
J	2,	3		CONN, MICRO-RIBBON, REC, PWB, 36 POS	478750	89536	478750	2		
.1	4,	9		CONN, D-SUB, PWB, 25 SCKT	614743	28198	MD25F-3000-14	1		
	5,	7		CONN, MICRO-RIBBON, REC, PWB, 14 POS	478743	89536	478743	2		
	ิล์	•		HEADER, 1 ROW. 100 CTR, RT ANGLE, 12 PIN	742965	89536	742965	1		
.i	10			HEADER, 1 ROW, 0.100CTR, RT ANG, 10 PIN	542076	89536	542076	1		
Ř	1.	2		RELAY.REED.2 FORM A.5VDC	340638	71482	MRB2A05	2		
MF	4			LABEL, ADHESIVE, PCB, 0, 375X1.0	807032	89536	807032	1	1	
MF	2			SPACER, SWAGED, RND, BRASS, 6-32X0, 150	296145	89536	296145	2		
MF	3			SPACER, SWAGED, RMD, BRASS, 4-40X0, 250	340547	89536	340547	2		
MP	4			SPACER, SWAGED, RND, BRASS, 4-40X0, 187	335604	89536	335604	8		
9	8			HEADER, PROGRAMMED	504373	51167	14-675-191	í		
P	9			PIN, SINGLE, PWB, 0, 025 SQ	267633	00779	86144-1	50	1	
s	1			SWITCH, SLIDE, DPDT	572016	19389	23-021-158	í		
хJ	2.	3,	5,	CONN ACC.MICRO-RIBBON,LATCH	412700	13511	57-1001	8		
хĴ	7	ω,			412700					
X.1 X.1	2,	З,	5,	CONN ACC, MICRO-RIBBON, SPRING	412718	71785	436-99-22-205	8		
XP	8			SOCKET, IC, 14 PIN	370304	09922	DILB14P-108	1		



Figure 5-23. A23 I/O Connector PCA

# Section 5A General Information

### INTRODUCTION

This section contains general information for the 5440B/AF. This information includes: the pca revision levels documented in this manual, a list of Federal Supply Codes For Manufacturers, a list of the Fluke Technical Service Centers, and a list of the U.S. and International Sales Centers for Fluke equipment.

## **MANUAL STATUS**

Table 5A-1 defines the assembly revision levels that are documented in this manual. To identify the revision level of the pca's in your instrument, refer to the revision level (marked in ink) on the component side of the pca.

### CHANGES AND IMPROVEMENTS

As changes and improvements are made to the instrument, they are identified by incrementing the revision level of the affected assembly. These changes are documented on a supplemental change/errata sheet that, when appropriate, is inserted in the front of the manual.

### 5A-1

5A-2

### 5A-3

### 5A-1



### Table 5A-1. Manual Status Information


## Section 6 Accessories

#### INTRODUCTION

This section contains service information for the accessories used with the 5440B/5442A. Because most of the accessories available for the 5440B/5442A are cables, this information is limited. Replacing cables when they are defective is often less expensive than repairing them.

#### ADDITIONAL PROCEDURE STORAGE MODULE (5440A-7001)

The 5440A-7001 Additional Procedure Storage Module provides non-volatile storage for up to 60 front panel setups. Front panel setups are placed into EEPROM memory in the storage module by the front panel microprocessor. Using the MEMORY CONTROL keys (on the 5440B/5442A front panel) any instrument operating configuration can be saved permanently, without having to rekey the setup.

There is no applicable service information for the 5440A-7001 Additional Procedure Storage Module.

#### LOW THERMAL EMF PLUG-IN CABLES (5440A-7002)

The 5440A-7002 Low Thermal EMF Plug-in Cables are three special length, shielded cables. These cables are constructed to minimize thermal emf in the connections between the 5440A output and the input of the device the 5440A is driving.

The cables should be stored in an area that is free from potential contaminants (e.g., dust, grease, excessive humidity, etc.). To prolong the life of the cables, store them in loose coils; do not store them in bundles.

#### ACCESSORY CABLES

There are several accessory cables for the 5440B/5442A. There is no applicable service information for the 5440B/5442A accessory cables.

#### 1780 RS-232-C Cable (Y1709)

The Y1709 cable is two meters long and is intended to connect a 1780A Infotouch Display to the 5440B/5442A. This cable extends the RS-232-C interface on the 5440B/5442A.

### 5205A Interface Cable (Y5001)

The Y5001 interface cable connects the Fluke 5205A Precision Power Amplifier to the 5440B Boost Interface. This cable is 0.7 meters long and has two connectors on each end. One connector on each end is for control signals, and the other connector on each end is for the boost voltage output of the 5440B.

#### 6-4

6-3

## 6-5

6-6

6-1

6-1

## 5220A Interface Cable (Y5002)

The Y5002 interface cable connects the Fluke 5220A Transconductance Amplifier to the 5440B Boost Interface. This cable is 0.7 meters long and has two connectors on each end. One connector on each end is for control signals, and the other connector on each end is for the boost voltage output of the 5440B.

## Armored IEEE-488 Interface Cables (Y8021, Y8022, Y8023)

These three cables provide an IEEE-488 interface from the 5440B/5442A to any IEEE-488 compatible device. The three lengths are: one meter for the Y8021, two meters for the Y8022, and four meters for the Y8023.

## RS-232-C Printer Cables (Y5003, Y5004)

These cables connect an RS-232-C compatible printer such as the Fluke model 1776B to the 5440B/5442A printer interface port. Y5003 is 5 feet long and Y5004 is 10 feet long. These cables have male connections at both ends.

## Extender Kit (Y5021)

This kit contains the extender cables and PCAs required for servicing the 5440B/5442A. Component parts of the kit are as follows:

Analog/Digital Extender PCA (P/N 608281) Filter A & B Extender PCA (P/N 608117)



6-7

6-8

6-9

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# Section 7 Schematic Diagrams

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i

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Figure 7-1. Overall Analog





FIG, 7-1 a Sht lof 3



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Figure 7-1. Overall Analog Diagram (cont)



Figure 7-1. Overall Analog Diagram (cont)









Figure 7-1. Overall Analog Diagram (cont)

FIG. 7-2 Shti of3





Figure 7-2. A1 Keyboard Assembly





FIG. 7-20 Sht 10F3



F16.7-20 Sht 20F3





Figure 7-2. A1 Keyboard Assembly (cont)

FIG. 7-3 Sht 1 of 3



FIG. 7-3 ShT 2 of 3 5





3 NOT USED

Figure 7-3. A2 Front Panel Controller

5440B/AF

F16. 7-3 Sht 30F3



5442A-1706

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#### Figure 7-3. A2 Front Panel Controller

F/6 7-30 Sht 10 F3



FIG. 7-30 Sht 20+3



Figure 7-3



Figure 7-10. A9 REF/DAC Analog PCA (cont)

FIG. 7-36 Sht 10F3



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NOTES:

. P.A.L. - PROGRAMABLE ARRAY LOGIC



Figure 7-3. A2 Front Panel Controller (cont)



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Figure 7-3. A2 Front Panel Controller (cont)

FIG. 7-3C Sht 1 of 3 ......



FIG. 7-3C sht 20+3



FIG. 7-3 C Sht 3 . F 3

. . . .



Figure 7-3. A2 Front Panel Controller (cont)

FIG. 7.4 Sht 10F2

5440B/AF



Figure 7-4. A3 Motherboard PCA





F16.7-40 Sht 1 of 3

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FIG. 7-4 a sht 20f3



Figure 7-4. A3 Mo

FIG. 7-4 a Sht 30f3

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Figure 7-4. A3 Motherboard PCA (cont)

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FIG.7-46 Sht 10F3
FIG.7-4 b sht 2 of 3 5440B/AF



Figure 7-4. A3 Motherboard PCA (cont)

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FIG. 7-4 b sht 3 0F3 5440B/AF

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Figure 7-4. A3 Motherboard PCA (cont)

FIG. 7-4C sht 1 of 3





Figure 7-4. A3 Motherbo



<sup>7-15</sup> 

F16.7.4d Sht10F2

5440B/AF



Figure 7-4. A3 Motherboard PCA (cont)



7-16

FIG. 7-4 E sht 1 of 3



F16, 7-4 C ShT 20F3



Figure 7-4. A3 Motherboard PCA (co

FIG. 7-4 C Sht 3 of 3

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5440B/AF



Figure 7-4. A3 Motherboard PCA (cont)

F16.7-5 Sht 1.fz

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5440B/AF



Figure 7- $\varepsilon$ 

5440B/AF

FIG. 7-5 Sht 20FZ



Figure 7-5. A4 Output PCA

F16: 7-5 a Sht 1 of3





Figure 7-5. A4 Output PCA (

FIG 7-50 Sht 3 of 3



FIG. 7-6 SAT 10F2



7-20



Figure 7-6. A5 Output/HV Control PCA

F16.7-6a Sht 10+3



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FIG. 7-6 Qu Sht 2 of 3



Figure 7-6. A5



Figure 7-6. A5 Output/HV Control PCA (cont)

7-21

F16.7-6b Sht 10f2

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5440B/AF



Figure 7-6. A5 Output/HV



7-22

F16.7-6 C Sht 1 of 3



F16. 7-6 C sht 20f3





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F16. 7-7 sht 1 of 2

5440B/AF



F167-7 5440B/AF Sht 20F2



		RELAYS					
		Γ		-	Γ	K9	
			ļ			×ө	
						k7	
OPERATING STATES	EI.	K2	кз	KĄ	۲5	260	
POP CON DITION	0	٥	٥	0	0	0	
STANDBY	0	0	0	0	0	0	
0.2V RANGE	0	٥	٥	۵	٥	٥	
zv	٥	0	٥	٥	٩	0	
104	۵.	0	0	Q	٥	0	
207	0	٥	٥	0	٥	٥	
250V	0	0	0	1	I.	٥	
1	0	0	0	1	٥	0	
INT CAL -IOV RANGE	1	Q	٥	٥	0	0	
INT. CAL -ZOV BANGE	0	1	ì	0	0	0	
INT. CAL -IKV BANGE	0	ð	٥	1	1	۱,	

5440A-1630

Figure 7-7. A6 Sample String PCA

FIG 7-7 Q Sht lof 3



FIG. 7-70 SHT 2073



Figure 7-7. A6 Sample String PC



Figure 7-7. A6 Sample String PCA (cont)



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F16.7-8 Sht 20F 3



5440B/A



Figure 7-8. A7 Preamp PCA

F16.7-8 a. Sht 10f3

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FIG. 7-80 Sht 20f3





5440B/AF



Figure 7-8. A7 Preamp PCA (cont)
FIG. 7-8 b Sht 10F3



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FIG. 7-8 C Sht 10f 3



F16. 7-8C sht 20f3





5440B/AF



Figure 7



5440A-1750

Figure 7-9. A8 REF/DAC Digital PCA

F16.7-9 a Sht 1 of 3





Figure 7-9. A8 REF/DAC Di



FIG. 7-9 b sht 1 of 2

5440B/AF



Figure 7-9. A8



F16. 7-96 Sht 20f2



Figure 7-9. A8 REF/DAC Digital PCA (cont)

5440A-1750

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FIG. 7-9 C sht 1 of 3





F16.79C Sht 30f3



Figure 7-9. A8 REF/DAC Digital PCA (cont)

F16.7-10 ShtioF 3



FIG. 7-10 SHT 20F3





F16.7-10 Q SAT 1673





Figure 7-10. A9 REF/DAC Analog



Figure 7-10. A9 REF/DAC Analog PCA (cont)





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Figure 7



Figure 7-10. A9 REF/DAC Analog PCA (cont)

FIG. 7-10 C sht10F3







Figure 7-10. A9 REF/DAC

affect to the



Figure 7-10. A9 REF/DAC Analog PCA (cont)

FIG.7-11 Sht1.F3



FIG. 7-11 sht 20f3



5440A-1660

5440B/AF

5440B/AF

FIG. 7-11 Sht 3of 3



5440A-1660



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Figure 7-11. A10 Inside Regulator PCA

FIG. 7-11 a Sht 10f 3



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Figure 7-11. A10 Inside Regulator PC

FIG. 7-11 a

5440B/AF



Figure 7-11. A10 Inside Regulator PCA (cont)



Figure 7-12. A11 Guarded Transformer Termination PCA


FIG. 7-12a sht 1043





F16,7-12 a sht 30-f3

5440A-4003 GUARDED XFMR TERMINATOR







FIG. 7-13 a Sht 1 of 3



〔)



Figure 7-13. A12 Filter A PC

Sht 3 of 3	F	16.7-	13 a		
241 241 2		Sht	3 of	3	

NOTES: UNLESS OTHERWISE SPECIFIED I. ALL RESISTORS IW CC.

- 2. ALL RESISTOR VALUES IN OHMS.
- 3. ALL CAP VALUES IN MICROFARADS.

4 HOOV ISOLATION REQUIRED ON THIS CIRCUIT.



5440A-1004

Figure 7-13. A12 Filter A PCA (cont)



. . . . . . . . . .

Figure 7-14. A13 Filter  $\boldsymbol{E}$ 







FIG. 7-14 a

Sht 20F3







Figure 7-15. A14 Guard Crossi



FIG. 7-15 a Sht ( of 3





Figure 7-15. A14 Guard Cross



<sup>7-47</sup> 

F16.7-16 Sht 10f 20



Figure 7



## Figure 7-16. A15 Memory PCA

F16.7-16a sht lof-3





Figure 7-16. A15 Memory



Figure 7-16. A15 Memory PCA (cont)







5440B-1680

F16. 7-172 Sht 10f3



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FIG.7-17a Sht 30F3





Figure 7-17. A16 Controller PCA (cont)







Figure 7-16. A15 Memory PCA (cont)

7-52

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FIG. 7-17 C Sht 20F3









FIG. 7-18 Sht lof 2

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Figu



Figure 7-18. A17 Outside Guard Regulator PCA





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NOTES: UNLESS OTHERWISE SPECIFIED.

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1. IF RESISTOR IS MARKED NE IT IS AN 19 W, 190 METAL FILM TYPE. IF THE RESISTOR IS NOT MARKED IT IS 14 W, 590 DEPOSITED CARBON TYPE UNLESS OTHERWISE INDICATED.

2 ALL RESISTOR VALUES IN OHMS 3 ALL CAP VALUES IN MICROFARADS. A HEATSINK REQUIRED

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ĸ QI
FIG. 7-18 a Sht 24f 3





Figure 7-18. A17 Outside Guar



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uaru negulalvi FOA (Coli

FIG. 7-19 Sht 1 of 2-

5440B/AF



7-56



7-56

FIG. 7-19 a Sht 1.F 3



FIG. 7-19 a Sht 2 of 3



Figure 7-19. A18



7-57

P16.7-19 b Sht 1 of 2



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7-58



FIG.7-19 C Sht 2 of 3





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F16. 7-20a sht 20F 3





7-61







7-62



FIG. 7-21 a Sht 2 of 3





<u>,</u>										
		111111-111			<u>ئے</u>					
	•			D						
	G20 DS2				<b>5.1</b>					
				0						
63			**	manî	1					
FUNCTION PA1	PIN 26	FUNCTION PA24		PBII	AN 37	Fu				
1	25 24	25 26	3 2 53	13	36 39	[				
4	23 22	27	54	14	40	6				
6	21	28 29	55 56	5	41 42					
7	20 19	30 31	57 58	17	43 +4					
9 10	18 17	32 33	59	19 20	45 46					
11	16 15	34 35	61	21 22	47 48					
13 14	14 13	PA36	43 27	<b>R</b> R	47 50					
15	12	2	28	25	51					
<i>к</i> 17	11	3 4	29 30	20	94 93	·				
18	9 8	5	31 32	29 29	92 91					
20	7 6	7	33 34	30 31	90 89					
22	5	9	35	32 1633	88 87					
PA 23 F F		PB 10	36	p	01	Gy J				
L F	\$2					L				
		612 22 23		D51						
				() () () () () () () () () () () () () (	21					
		6	28	2	20					
		с d	8	3 4	19 18					
			24	5	17 No					
		2	26 25	8	15 N					
		9 1 1 1	3	9 10	13 12					
			2	11	11	U				
		+H P-1	6	F	1					
	11	קסי	23	F	30					
	L_4	PCOM	22	!	J	ĺ				

CHARACTER PATTERN PIN CONNECTION



	ការពេត្	D52		دے ت ۱۱۱۱۱۱۱۱۱	,	C 2 3 7 7 8 9 C 9 C 9 9 C 9 C 9 9 C 9 C 9 9 C 9 C 9		
FUNCTION	PIN	FUNCTION	PN	FUNCTION	AN	FUNCTION	PIN	
PA1	26	PAZH	3	PBII	37	PB 34	80	
2	25	25	2	12	30	35	85	
3	24	26	53	13	39	30	84	
4	23	27	54	14	40	G1	83	
5	22	28	55	15	41	2	82	
6	21	-29	56	Ko	42	3	6/	
7	20 19	30	57 58	17	43 44	4	60 79	
8	19 18	31 32	58 59	18	45	5	78	
4	18	33	40	20	46	4	77	
ĩ	16	34	61	21	-47	l á l	70	
12	15	35	62	22	48	9	75	
13	14	PA36	63	23	49	10	74	
14	<b>.</b> 3	PBI	27	24	50	//	73	
15	12	2	<b>20</b>	25	51	12	72	
10	jł –	3	29	20	94	13	7/	
17	ю	4	30	27	93	#	70	
18	9	5	31	28	92	15	69	
19	8	6	32	29	97	Ko	68	
20	7	7	33	30	90	/7	67	
21	6	8	34	3/	89	18 19	46	
22	5	9	35	32	88		45	
PA 23	4	PB 10	36	P833	87	620	1 10	
F	1					i		
F	\$2			<u> </u>				



Figure 7-21. A22 Display PCA (cont)



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Figure 7



FIG-7-22 Sht 1073



FIG. 7-22 Sht 20F3





Figure 7-22. A23 I/O Connector PCA (cont)

# Appendix A Recent Innovations in Direct Volts Calibrator Design

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## ABSTRACT

High accuracy direct voltage calibration systems have traditionally been based upon precision resistive voltage dividers that are manually calibrated at frequent intervals to maintain the required resistance ratio. Because of resistance temperature coefficients, high accuracy is only attainable when systems are used in temperature controlled environments, typically  $23^{\circ}C \pm 1^{\circ}C$ .

This paper describes the design approach used in a direct voltage calibrator that does not require manual adjustment of resistor ratios to maintain accuracy. Internal calibration is an automated, microprocessor-controlled operation requiring no operator intervention. Resistance ratio determination and derivation of calibration constants are described. Design of the environmental controls that allow the instrument to deliver a rated accuracy of 4 ppm while operating in ambient temperatures  $\pm$  5°C from the calibration temperature will be discussed.

# INTRODUCTION

For many years, high accuracy direct voltage calibration systems have been based upon precision resistive voltage dividers which had to be manually calibrated at frequent intervals to maintain required resistance ratio accuracy. These systems were restricted to environmentally controlled areas because of resistance temperature coefficients of the voltage dividers. An additional restriction was manual operation only, because the high quality switching required for the resistance decades ruled out the use of relays.

To overcome these limitations an engineering project was initiated to develop a direct voltage calibrator suitable for calibration of high accuracy 6-1/2 and 7-1/2 digit voltmeters, that was remotely programmable and could be operated over a reasonable temperature range. The instrument developed as a result of this project was the Fluke Model 5440A Direct Voltage Calibrator. It has a basic accuracy specification of 0.0004% (4 ppm), is IEEE-488 programmable, can be calibrated completely without manual adjustments and can be used without degradation of specifications in ambient temperatures of 15 to 30°C. The 5440B and 5442A Direct Voltage Calibrators are descendants of the 5440A and use the same design approach.

These objectives were met by building into the instrument a unique system for measuring system and component errors and, with the calculation and control capabilities of the microprocessor, compensating these errors to near zero. This paper will examine in detail the automated measurements and procedures that accomplish this calibration process.

# **BLOCK DIAGRAM DESCRIPTION**

A block diagram of the 5440A analog section is shown in Figure 1. It consists of a very stable Reference Voltage Source (Vref), a Digital to Analog Converter (DAC), and a Power Amplifier. The reference is a very stable constant voltage source of approximately 13.2V dc. The reference polarity can be changed by relays in series with the output. The DAC is a pulse width modulated (PWM) type. Refer to Figure 2. An electronic switch at the input to the filter alternates between Vref and ground at a constant frequency of 83 Hz. This signal is then filtered by a low pass filter to yield the dc component. This dc voltage can be varied, from zero volts to Vref, by changing the duty cycle which is a ratio of time the switch is connected to the reference voltage source to the total period. The duty cycle is controlled by the microprocessor.

Refer to Figure 3. The inverting power amplifier consists of two parts, a very high gain preamp and a current amplifier that supplies up to 25 mA to the load. The gain of the power amplifier is changed by switching in different feedback ratios for the ranges of the instrument's output. For the ten volt range the gain is one, for the 20V range it is two, for the 250V range the gain is 25 and for the 1000V range it is 100. The 20V range is divided by a resistive divider with division ratios of 10 and 100 to give the 2V and 0.2V ranges respectively.



Figure 1. 5440A Simplified Block Diagram, Analog Section



Figure 2. Simplified Diagram of PWM DAC



Figure 3. Simplified Diagram of Power Amplifier

## SYSTEM DESIGN

Calibrating the 5440A differs considerably from the technique used in previous calibrators. The most notable difference is that there are no potentiometers to be adjusted to trim resistors. Instead each part of the instrument is designed for extreme stability and linearity so that the output voltage can be related to the DAC duty cycle by a simple equation. Calibrating the instrument involves determining by measurements the constants used in this equation. Once determined the microprocessor can calculate the proper DAC duty cycle required to give the desired output. The performance of the DAC is the key element in producing a high accuracy calibrator. The most important characteristic is linearity; its output voltage versus its duty cycle can be characterized by a straight line formula. This formula is shown in equation 1.

Equation 1:

y = ax + b

A straight line equation has only two constants to find, a and b. Once found, the operation of the DAC is fully characterized. The microprocessor controls the duty cycle through a count loaded into a counter in the DAC. This count will be called N1. With a count of zero the duty cycle is zero and the output of the DAC is zero. With a count of 24096, the duty cycle is 100% and the output of the DAC is equal to Vref. The resolution of this circuit is equal to the change in output with a change of one count. This is equal to equation 2.

Equation 2:

Resolution =  $Vref/24096 = 550 \,\mu V/Count$ 

This is not sufficient resolution for a voltage calibrator so further division is necessary. Since switching speed places practical limits on minimum pulse width, other means must be found to obtain the required resolution. To this end a second switching circuit is employed. Refer to Figure 4. This circuit uses the same switching frequency (83 Hz) and has the same range of counts, zero to 24096 (this count will be called N2), but has an input reference voltage that is attenuated from the 13.2V dc of the first switching circuit. The output of this second switching circuit is further attenuated before it is applied to the summing junction of the active filter. The overall attenuation, which will be termed RR (ratio of resolutions) is typically 7200. This makes the voltage resolution of the second switching circuit, and thus the DAC, equal to equation 3.

Equation 3:

Resolution =  $550 \mu V/7200 = 76 nV/count$ 

The exact value for RR is determined as a part of the instrument calibration.

The filter takes the pulses from the two switching circuits and filters out the dc component with a multiple pole filter that has an overall dc gain of negative one at dc. The DAC output also includes an offset voltage (Vos). This offset comes from two sources within the DAC. First, there is the offset voltage in the amplifier of the DAC active filter. Second, there is a fixed offset introduced to improve linearity. The DAC is very linear down to N1 = 10, so to get good linearity down to zero volts it is required that the DAC be able to put out zero volts with N1 = 10. To accomplish this a fixed offset or bias of -5.5 mV, equivalent to N1 = 10, is introduced at the input of the filter. This offset is obtained by inverting Vref, attenuating it to the proper level, and injecting it at the input of the filter (refer to Figure 4). The instrument outputs a negative voltage by reversing the polarity of the reference. In the DAC this changes the fixed bias polarity but not the filter offset voltage. As a result the sum of these two offsets changes when the polarity is reversed. This results in two values for the offset, one for positive polarity and one for negative polarity. The output of the DAC is given by equation 4.



Figure 4. Dual Switching DAC

Equation 4:

$$DAC Out = (GF)\{(Vref)(DC1) + (Vref/RR)(DC2) - (Vosdp)\}$$

Where:

Vref = Reference Voltage (13.2V).

DC1 = Duty Cycle of the 1st switching circuit.

DC2 = Duty Cycle of the 2nd switching circuit.

GF = Gain of the DAC Filter (-1).

RR = Attenuation factor of the 2nd switching circuit.

Vosdp = DAC offset voltage where polarity is positive or negative.

Equations 5 and 6 relate the duty cycle to N1 and N2.

Equation 5:

DC1 = N1/24096

Equation 6:

DC2 = N2/24096

Factoring equations 5 and 6 and substituting it into equation 4 gives the formula shown in equation 7.

Equation 7:

DAC Vout =  $(GF){(Vref/24096)(N1 + N2/RR) - (Vosdp)}$ 

Relating equation 7 to equation 1, the constant, (Vref/24096)(GF) is the value for "a". The variable, (N1 + N2/.RR) is the value of "x" and the offset voltage (-Vosdp) is the value for "b".

Following the DAC is the power amplifier whose gain is controlled by the microprocessor for different ranges. This amplifier also has an offset voltage of its own which is slightly different for each range. Following the power amplifier is a divider that is used only on the 0.2V and two volt ranges. The offset alters the overall gain of the power amplifier when used but does not add any offset voltage of its own. The formula for the output of the power amplifier is shown in equation 8.

Equation 8:

 $PA Vout = (GPAx){(PA Vin) + (Vosax)}$ 

Where:

PA Vout = Power amplifier output voltage.

x = Range (0.2V, 2V, 10V, 20V, 250V, or 1100V).

GPAx = Gain of the power amplifier and divider (when used) on range x.

PA Vin = Power amplifier input voltage.

Vosax = Power amplifier offset voltage on range x.

The input to the Power amplifier is the output of the DAC, so equation 7 can be substituted for PA Vin in equation 8. The result is equation 9.

Equation 9:

PAVout = (GPAx)(GF)(Vref/24096)(N1 + N2/RR) - (GPAx)(GF)(Vosdp) + (GPAx)(Vosax)

The output of the power amplifier is connected to the instrument's output terminals so the above equation is equal to the output voltage of the 5440A. Equation 10 shows the same formula with some substitutions.

Equation 10:

5440A Vout = Kx(N1 + N2/RR) - Vosxp

Where:

5440A Vout = 5440A output voltage.

x = Range (0.2V, 2V, 10V, 20V, 250V, or 1000V).

 $K_x = (GPAx)(GF)(Vref/24096).$ 

Vosxp = (GPAx)(GF)(Vosdp) - (GPAx)(Vosax).

Equation 10 also has the same form as equation 1 where:

y = 5440A Vout.

a = Kx.

 $\mathbf{x} = (\mathbf{N}\mathbf{1} + \mathbf{N}\mathbf{2}/\mathbf{R}\mathbf{R}).$ 

b = -Vosxp.

### CALIBRATION PROCESSES

To calibrate the 5440A it is necessary only to determine the values for Kx, Vosxp, and RR. Since the output is characterized by a straight line, finding the values for Kx and Vosxp only requires finding two points on that line. Since the DAC is linear down to zero volts it is one of the two points used. To find this point the instrument performs an auto zero process whereby it is zeroed, under program control, on each range and for both polarities. It is during this process that the value for RR is determined. Since RR is the ratio of resolutions, its value is equal to the number of N2 counts that changes the output by the same amount as one N1 count. After the instrument has been set to zero volts on the ten volt range, N1 is decremented by one count and N2 incremented until the output is again zero volts. The number of counts, added to N2 to reach zero, is equal to RR.

The hardware used to perform the auto-zeroing, shown in Figure 5, consists of a low noise amplifier and a low thermal EMF relay connected to the 5440A output. The 5440A contains a 12-bit, plus sign bit, a/d that is controlled by a microprocessor. The a/d input can be switched from various points within the 5440A circuitry by multiplexers. One of these points is the output of the low noise amplifier. The auto-zero process first measures the amplifier output with the input connected to SENSE LO which places a short circuit or zero volts on the input. The output reading is not normally zero as the amplifier has an offset voltage less than or equal to  $250\mu$ V. The voltage read is stored by the microprocessor. The output of the 5440A is set to zero by the microprocessor according to the values of Kx, Vosxp, and RR that it has previously stored in memory. The relay is then closed and a new reading taken. The difference between these two readings, divided by the gain of the amplifier, equals the zero offset of the 5440A. If the 5440A output is offset too far, the DAC output is incremented or decremented by a programmed amount in the direction that achieves zero. Another set of readings is taken and the process repeated until the difference from zero is within prescribed limits. The program then stores the N1 and N2 count required for zero and goes on to the next range.

The next step is to find the second point on the straight line. The best point would be one closest to Vref as possible. Because of the excellent linearity of the DAC, a point half-way up the line can be used with satisfactory results. This process requires external equipment and operator intervention so is called External Calibration (EXT CAL).

Figure 6 shows the connection of external equipment used to calibrate the ten volt and 20V ranges. A null detector with a microvolt resolution, like the Fluke 845A, is connected between the 5440A HI output and the HI output of a precision ten volt reference standard like the Fluke 732A.



Figure 5. Auto-Zero Circuit



Figure 6. External Calibration of the 10V and 20V Ranges

The operator first connects the external equipment then enters the exact voltage of the reference voltage standard through the 5440A keyboard. If the Fluke 732A is used the standard voltage is ten volts. The 5440A then outputs the same voltage as the standard using the values for constants currently in memory. The null detector then indicates how much the 5440A output differs from that of the voltage standard. The operator then increments or decrements the 5440A output until the null detector reads zero volts. At that point the 5440A is putting out the same voltage as the voltage standard. The "ENTER" button is pressed and the values for N1 and N2 used to determine this voltage are stored in memory.

Refer to Figure 7. To calibrate the other ranges a precision voltage divider, like the Fluke 752A, is required. This divider is used to divide 100V on the 250V range by ten, and 1000V on the 1000V range by 100, to get ten volts. This voltage is again compared to the ten volts from the 732A standard.

Refer to Figure 8. To calibrate the 2V range, the 752A divides the ten volts from the 732A by ten to get 1V that is compared to the 5440A output. For the 0.2V range, the 752A divides the ten volts by 100 to get 0.1V.

When all six ranges have been calibrated with the external equipment, the program then calculates the new values of K and Vos. It does this by using the values of N1, N2, and RR it has stored in memory from the auto-zero process and EXT CAL. The value of K for each of the six ranges is calculated using equation 11.



Figure 7. External Calibration of the 250V and 1000V Ranges



Figure 8. External Calibration of the 0.2V and 2.0V Ranges

Equation 11:

$$Kx = Std Vx / \{ (N1sx - N1zxp) + (N2sx - N2zxp) / RR \}$$

Where:

x = Range (0.2V, 2V, 10V, 20V, 250V, and 1000V).

Std Vx = Voltage standard voltage used on range x.

N1sx and N2sx = N1 and N2 used by the 5440A to output a voltage equal to the standard on range x.

N1zxp and N2zxp = N1 and N2 used by the 5440A to output zero volts on positive polarity and range x.

There are eight values for Vos, one for each polarity, for the ten through 1000V ranges. The Vos values for the 0.2V and 2V ranges when scaled by ten and 100 respectively, are close enough to the 20V range values that the 20V range values are used without further correction. Equations 12 is used to calculate Vos.

Equation 12:

Vosxp = Kx (Nlzxp + N2zxp/RR)

Where:

Vosxp = Offset voltage for positive or negative polarity on Range x.

x = Range (10V, 20V, 250V, and 1000V).

Kx = Value of K for range x.

N1zxp and N2zxp = N1 and N2 used by the 5440A to output zero volts on positive or negative polarity and range x.

Once all the values of K and Vos are calculated, they, and RR are stored in non-volatile memory so they will not be lost when power is turned off. This completes the calibration of the 5440A, a process normally done every 30 days.

## IMPROVING PERFORMANCE WITH INTERNAL CALIBRATION

To improve the 5440A accuracy between the 30 day calibrations, Internal Calibration (INT CAL) is normally run daily. Internal Calibration first goes through the auto-zero process on the ten through 1000V ranges, then finds the value for RR as already described. From this information any change in the values of Vos can be corrected using the new values of N1z and N2z.

The value of K can also change if the value of Vref, DAC gain, and/or power amplifier gain changes. A second part of INT CAL switches the instrument into a special configuration that allows measurement of any shift in the value of K due to a shift in DAC or power amplifier gain, and thus determines the correction for the shift. Any shift in the value of Vref can only be corrected for by EXT CAL.



The special configuration used during INT CAL to determine the gain shift in the ten volt range is shown in Figure 9. To achieve this configuration:

- 1. In the DAC, the reference is connected directly to the filter input. This is accomplished by setting the first switching circuit to 100% duty cycle and the second switching circuit to 0% duty cycle.
- 2. The DAC bias supply is disconnected.
- 3. The power amplifier feedback resistance that connects between the power amplifier output and the preamp input is disconnected from the power amplifier output and connected to the reference.
- 4. The preamp is disconnected from the current amplifier and configured into a non-inverting amplifier with a gain of approximately 600. Its output is connected to the a/d through a multiplexer.



Figure 9. Internal Calibration, Gain Shift Measurement Configuration

The gain of the DAC and the power amplifier are set by resistors. This special configuration places these resistors in a type of bridge configuration so that small shifts in resistor ratios (and thus the gain) can be accurately measured. Since the resistors are not exactly equal, and there is offset voltage in the DAC filter amplifier, the voltage at the input to the preamp is not normally zero but is less than 1.2 mV. Through the preamp, with its gain and offset voltage, the maximum voltage at the input to the a/d is less than 1V. The voltage at the input of the a/d is a function the DAC filter offset voltage, the preamp, and the resistor ratio. To overcome this problem, the program takes two measurements and then subtracts one from the other. The first measurement is taken with the connections as shown in Figure 10, and the second taken after the polarity of the reference is reversed. When the second reading is subtracted from the first the offset voltages drop out of the calculation leaving only the effect of the resistor ratios. The difference of the two measurements varies in direct proportion to the total shift in gain of the DAC and power amplifier. When EXT CAL is performed, the value of K is accurately set and stored in memory. Since INT CAL is always run prior to EXT CAL a set of readings for the instrument's gain shift is taken and stored. The next time INT CAL is run, a new set of readings is taken and their difference compared to those stored when EXT CAL was run. Any change in the differences is proportional to any gain shift so the program uses the amount of change to determine how much to change the value of K. using equation 13.

Equation 13:

$$K10 = {(V1 - V2)old - (V1 - V2)new}/24096$$

Where:

V1 and V2 are the voltages at the input of the preamp with a positive and negative Vref respectively, for the ten volt range.

The "old" values are those in memory from the last time INT CAL was run.

The "new" values are the current readings. As implemented in the 5440A a change in gain of 0.1 ppm can be determined.

#### NOTE

This technique cannot measure the actual gain accurately but only small shifts in gain. As mentioned earlier it does not correct for drifts in Vref but any drift in Vref does not affect the accuracy of determining the gain shift.

This same technique can be used to determine the gain shift of the 20V, 250V, and 1000V ranges. The feedback resistance used on these ranges is 40 k $\Omega$ , 500 k $\Omega$ , and 2M $\Omega$  respectively, so none of them can be compared directly with the 20 k $\Omega$  reference resistor. This problem is solved on the 20V range by splitting the 40 k $\Omega$  into two 20 k $\Omega$  resistors. One of the 20 k $\Omega$  resistors is used for the ten volt range. The other 20 k $\Omega$  resistor is then switched into the bridge and compared separately. The shift in K due to this 20 k $\Omega$  is calculated and then added to the shift already calculated for the ten volt range and this becomes the shift for the 20V range. Equation 14 is for the shift in K for the 20V range.

Equation 14:

$$K20 = K10 + {(V1 - V2)old - (V1 - V2)new}/24096$$

Where:

V1 and V2 are for the 20V range.

Refer to Figure 10. The 250V range and the 1000V range use the same ten 200 k $\Omega$  resistors configured differently for each range. For INT CAL, all ten are connected in parallel to give 20 k $\Omega$  which is switched into the comparison bridge. Again a set of readings is taken and their difference calculated. The shift in gain using the resistors in parallel can be related to the shift in K for the 250V range and 1 kV range where the resistors are used in a different configuration. The shift is simply multiplied by the gain for that range as shown in the equations 15 and 16.



Figure 10. Configuration of Ten 200K Resistors for the 250V and 1000V Ranges

Equation 15:

 $K250 = 25{(V1 - V2)old - (V1 - V2)new}/24096$ 

Equation 16:

 $K1KV = 100{(V1 - V2)old - (V1 - V2)new}/24096$ 

Where:

V1 and V2 are the bridge readings taken for the ten 200 k $\Omega$  resistors in parallel.

The shift in the values of K for the 0.2V and 2V ranges cannot be determined by INT CAL. Since these ranges are obtained by dividing down the 20V range, which is corrected by INT CAL, only the drift in the divider ratios degrades the accuracy of the values of K. These ratios are stable enough as to only require calibration every 30 days by EXT CAL.

# ENVIRONMENTAL CONTROLS

The internal and external calibration procedures are designed to correct for long term (greater than 24 hours) changes that take place in the instrument components and circuitry. To ensure short term stability, it is important that sensitive circuit components be maintained in a very stable environment. The 5440A package design includes three temperature controlled component ovens. The first oven encloses the solid-state reference components and sensitive DAC components, the second contains the preamplifier and the third encloses the power amplifier range resistors. The ovens are made by surrounding a section of the printed circuit board with thick aluminum blocks that contain heater resistors. This assembly is then covered with a foam insulation layer and a protective cover. The oven temperature is proportionally controlled using a stable glass bead thermistor sensing element to maintain a temperature of about 50°C. A second thermistor in each oven is used to monitor temperature for instrument self-test data.

In addition to temperature stabilization, sensitive components are selected and matched for very low temperature coefficient. The direct result of this selection and temperature control is the ability of the instrument to operate at full rated accuracy specifications over a wide range of ambient temperature.

#### PERFORMANCE

The internal calibration procedure described is initiated by pressing front panel keys. Once started it is a completely automatic process taking about five minutes. It is normally done once every 24 hours but may be initiated at any time, for example, to correct for large changes in ambient temperature. Internal calibration corrects for all component shifts except the reference element and the resistive dividers for the 0.2V and 2V ranges. External calibration, normally performed at 30 day intervals, corrects for shift in the reference and the low voltage divider. It requires use of a null detector, an external reference voltage and a voltage divider. It requires about 15 minutes to perform and involves the operator through prompting by the alphanumeric display. No mechanical adjustments are required; only incrementing or decrementing output voltage from the front panel.