

SR6670A

## PowerAmplifier

**Professional Series** 

# **Owner's Manual**



PV ONLY

Graphic for illustration only-will use photo-plotted image

### **IMPORTANT!**

### FOR YOUR PROTECTION, PLEASE READ THE FOLLOWING:



The symbols shown above are internationally accepted symbols that warn of potential hazards with electrical products. The lightning flash with arrowhead symbol within an equilateral triangle warns that there are hazardous voltages and the risk of electric shock within the unit. The exclamation point within an equilateral triangle alerts the user to refer to important information in the user manual.

These symbols are a Warning that there are no User Serviceable Parts inside this equipment and that there are Hazardous Voltages present. Do not open this equipment yourself. Refer all servicing to qualified personnel. Do not make any internal adjustments or additions to this equipment at any time. Do not tamper with the internal electronics. Failure to follow these instructions may cause a Shock Hazard and may void Warranty Service to this equipment.

This equipment should be operated only at the voltage indicated on the rear panel. Replace the fuse only with the same type and rating as indicated on the rear panel.

This equipment must be grounded for correct operation. Do not defeat the safety ground by using a ground lift adapter or by physically removing the ground prong from the plug.

The power cord should be routed so that it cannot be walked upon or pinched by items placed upon or against it. The power cord should be unplugged from the outlet when the equipment is to be unused for a long period of time. This equipment should be located away from heat sources and should be properly ventilated.

Do not expose this equipment to rain or moisture.

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# Introduction

#### JBL 6670A

Thankyou for purchasing this JBL Power amplifier. We encourage you to read and to make use of the material contained in this manual. We welcome your suggestions and comments on our products and on this manual.

#### Features:

The two rack-space, JBL 6670A is an all solid-state power amplifier capable of delivering up to 600 watts per channel into 4 Ohms with both channels driven, with independent protection circuitry on each channel.

It has a switching power supply, and is available in one 110/120 Volt version.

A choice of optional signal processing boards may be installed to provide either a Peak Compressor with High Pass Filter or an Electronic Crossover for Bi-amp operation.

Parallel XLR and <sup>1</sup>/<sub>4</sub>" phone connectors feed fully active bridging differentially balanced circuitry.

A rear- panel switch selects between three modes of operation: Stereo, Dual Mono (single input to both channels) and Bridge Mono output.

Neutrik Speakon<sup>®</sup> connectors supply Left, Right and Auxiliary (Stereo, Bridge or Bi-amp) speaker outputs.

The chassis has both front and rear rack mounting brackets.

Dual variable-speed fans draw filtered cooling air through rear vents, exhausting through front grilles.

### Contents of Shipping Container

Your new JBL power amplifier was carefully packed at the factory, and the container was designed to protect the unit during shipment. Nevertheless, we recommend careful examination of the shipping carton and its contents for any sign of physical damage which may have occurred in transit. If damage is evident, do not destroy any of the packing material or the carton, and immediately notify the carrier of a possible claim for damage. Damage claims must be made by vou.

The shipping carton should contain:

- The JBL amplifier with model number as shown on the shipping container
- This instruction manual
- · An envelope containing rack mounting hardware
- 2 each: 4 conductor male Speakon<sup>•</sup> connectors (Neutrik NL4FC)
- AC power cord

# Front Panel



Graphic for illustration only-will use photo-plotted image

#### Controls

- [1] Power Switch: Push ON, Push OFF
- [2] Channel A Gain control: Log potentiometer
- [3] Channel B Gain control: Log potentiometer

### Status Indicators etc.

[4	Power:	Green LED
[5	i] Clip:	Red LED
[6	[] Signal Present:	Green LED indicates a signal of -26 dB or above.
[7	'] Standby:	Red LED illuminates during the turn-on sequence or whenever the indicated channel is shut down by its protection circuitry.
[ 8	] Exhaust Vents:	Must be unobstructed to allow cooling air flow.

# Rear Panel



Graphic for illustration only-will use photo-plotted image

#### Connectors

[1]	Input Connectors:	Parallel XLR and 1/4" TRS phone plugs.
[2]	Output Connectors:	Neutrik Speakon <sup>®</sup> Connectors for: Channel A Channel B Aux (Channel A + Channel B)
Switch	es etc.	
[3]	Amplifier Mode Switch:	Selects amplifier mode: Stereo, Dual Mono or Bridge Mono.
[4]	Ground Lift Switch:	Isolates Signal Ground from Chassis Ground (see Grounding recommendations).
[5]	Cooling Fans:	Two variable-speed DC fans draw in cool air which is exhausted by front-panel vents.

#### Amplifier Mode Switch

Stereo:

Input to Channel A:

Output of Channel A is controlled by Channel A level control. Input to Channel B:

Output of Channel B is controlled by Channel B level control.

#### Dual Mono:

Signal is input to Channel A: (Input B is not used). Output on Channel A is controlled by the Channel A level control. Output on Channel B is controlled by the Channel B level control. Dual Mono mode feeds the input of Channel A to both channels. Thus avoiding the use of a patch or Y-cord, when both channels of the amplifier are being driven by the same signal.

# Signal Processing Options

#### Bridge Mono

This mode configures the two channels as a single mono amplifier with the combined power of both channels.

Signal is input to Channel A. Use Channel A level control .

Channel B input is not used. Channel B level control is inoperative.

	Channel A			Channel B	
lodes	MODE	INPUT	LEVEL Control	INPUT	LEVEL Control
	STEREO	A	A	В	В
	DUAL MONO	A	A	A	В
	BRIDGE	A	A	A	A
	BI-AMP	LF	A	HF	В

### Signal Processing Options

Two optional, accessory signal processing boards are available and may be installed in the 6670A by your JBL dealer.

NOTE: These options can <u>not</u> be installed simultaneously.

Peak Compressor and High Pass Filter Option:

LDR Compressor activated by peak clipping. Action is automatic. 18 dB per octave high pass filter frequency is selectable by DIP switch to 20 Hz or 40 Hz.

#### **Electronic Crossover Option:**

This option provides bi-amplified operation by assigning a low-pass filter to Channel A and a high-pass filter to Channel B. The slope of the tracking filters is 24 dB per octave. The filter frequency is selectable by plug-in SIP resistor networks. The unit is shipped with 800 Hz SIP installed. Other standard freqencies are: 80 Hz, 120 Hz, 500 Hz, 800 Hz, 1200 Hz and 7k Hz: A 6 dB per octave constant directivity boost at 3050 Hz is jumper selectable by a two position shunt.

Table 1 -Amplifier Modes

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# Installation

#### WARNING

CHECK THAT THE AC LINE VOLTAGE AT YOUR INSTALLATION IS CORRECT FOR THE AMPLIFIER. IF YOUR AC SUPPLY VOLTAGE IS DIFFERENT, DO NOT PROCEED ANY FURTHER WITH INSTALLATION.

A significant fire and shock hazard may exist if the amplifier is connected to an AC power source other than that for which it is rated and labelled.

. Power consumption at the rated power of 600 watts per channel is in excess of 2000 watts (23.8 amps) and each SR6670A should be connected to a 110/120

VOLT CIRCUIT CAPABLE OF SUPPLYING AT LEAST 30 AMPS.

THERE ARE NO USER-ACCESSIBLE FUSES.

REFER ALL SERVICING TO QUALIFIED SERVICE PERSONNEL.

#### **Rack Mounting**

Rack mount the amplifier with the enclosed rack mounting hardware. Additional rack ears are supplied to support the rear of the amplifier and should be used whenever possible

The amplifier will operate satisfactorily over a range of ambient temperatures from  $0^{\circ}$ C to +50°C (+32°F to +122°F), and up to 80% non-condensing relative humidity.

The amplifier is fan-cooled, with air flow from rear to front. For correct operation of the amplifier and long life of its internal components, an unimpeded source of cool air must be made available at the rear of the unit. In most cases, this will only mean that vent grilles be provided in the rack, but some installations may require additional supplies of cooling air. Do not obstruct the front panel exhaust grilles.

Although internal circuitry is sufficiently shielded from moderate electromagnetic fields, avoid mounting the unit near large power transformers or motors etc.

WILL ADD HOKE INFO OF CURICER DRIMU.

# Grounding and Safety

### Grounding

Grounding is a complex subject and is critical to obtaining optimum performance from a sound system. Good grounding practices have three goals:

- 1 Safety.
- 2 Maintenance of system signal ground integrity.
- 3 The prevention of oscillation and hum which may be caused by differing potentials within the system or RFI (Radio Frequency Interference) or Electromagnetic induction.

### Safety

For safe operation, the amplifier must be connected to a good mechanical ground. This provides an adequate rereturn current path for any voltage which might appear on the chassis. Without this path, the unit can be a shock hazard. In addition, a good quality ground on the chassis provides shielding from external fields.

To comply with safety regulations and to protect our customers, we provide this product with a ground connection through a three-wire power cord. Connection of this equipment to non-grounded AC supplies does not comply with National Electrical Codes and may result in costly legal ramifications.

#### Grounding Guidelines

The number of variables involved in system design makes it impossible to establish fixed grounding "rules" - however, several techniques have evolved which have proved effective in most situations.

These practices are offered as guidelines towards establishing an effective safety grounding scheme and should result in a stable sound system.

The practices are summarised below and then discussed in further detail.

- 1 Develop a grounding scheme and follow it as closely as possible.
- 2 Ensure that all equipment has a solid MECHANICAL (safety) ground.
- 3 Connect all Green Safety Line -Cord grounds directly to a common point (whenever possible) i.e. use a "star system".
- 4 Eliminate duplicate ground paths Ground Loops.
- 5 Use twin conductor cable even with unbalanced sources. Do <u>not</u> use shields as signal current carrying conductors •

## Grounding and Safety

#### **Recommended Practices**

#### 1 Grounding Scheme:

Use these guidelines to design a grounding scheme. Determine how each piece of equipment will be grounded, how shields will be connected etc. Follow the scheme carefully!

#### 2 Mechanical Grounds:

Grounds are provided for safety ! Do not remove them ! Ensure that AC sockets are securely grounded and that the ground wire is capable of carrying the full current capacity of the circuit breaker or fuse feeding the socket.

#### 3 Star System:

In an ideal system all chassis safety mechanical ground wires are connected directly to a common point at the building's main electrical service entry ground busbar. To best facilitate such a convention, the use of Isolated - Ground Receptacles is recommended. With Isolated - Ground Receptacles (orange in color), each individual ground is returned separately to the distribution panel. With this type of Safety Grounding, all of the chassis are at the same potential and therefore very little, if any shield currents will flow. There should be no intermediate connections to any other grounds. This is known as a "star sytem" of grounding.

#### 4 Ground Loops:

The major cause of ground loops is duplicate grounding, which occurs when a component is grounded via its own AC connection and has a second path to ground through a cable shield to another component's chassis ground. These different path lengths may cause a significant potential between the **audio** ground of the signal source and the **mechanical** ground to which the amplifier has been connected. A voltage is developed, which induces a spurious signal - usually hum, into the signal wiring. Attention to grounding should eliminate ground loops. See "Troubleshooting" on Page 18.

The Signal Ground Lift switch either connects the Signal Ground directly to the chassis or "lifts" the Signal Ground by 150 ohms at low frequencies (60 Hz). At frequencies above 60 Hz, the signal-to-chassis ground impedance decreases to a few milliohms at RF frequencies. The use of this switch reduces the shield currents flowing between two or more chassis.

#### 5 Twin Conductor Cable:

The 6670A's input circuits consist of balanced, differential amplifiers, and will not unbalance floating or balanced output sources. Balanced wiring is recommended, especially when running long lines, due to the ability of a "balanced" input to reject signals (such as hum fields) which are induced equally into each of the signal carrying conductors - Common Mode Rejection.

## Grounding and Safety

### Unbalanced Sources

The use of twin-conductor shielded cable is recommended, especially when interfacing the SR6670A with equipment having *unbalanced* outputs.

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In order to take advantage of, SR6670A's superior Common Mode Rejection to reduce hum and noise, the wiring convention of Table 2 on page 12 should be used:

In unbalanced equipment, the signal ground is usually the sleeve of a • ¼" TS phone jack or RCA connector. It may also appear on a Barrier Strip. The shield of the twin-conductor cable is connected to ground at one end only - usually at the source. It is not connected to the *Input* sleeve or to Pin #1 of the SR6670A's input connectors. By connecting the equipment in this way, induced noise (hum and buzz) caused by differences in potential between various pieces of equipment will be reduced by the SR6670A's inputs common-mode rejection.

#### Long Cable Runs

Longer input cables should be balanced or floating to reduce susceptibility to RFI (radio frequency interference) and hum. If the output of the device feeding the amplifier is balanced or floating, simply use a dual-conductor shielded cable. If the source is unbalanced, an isolation transformer may be necessary at its output, to supply a balanced signal.

Also, balanced wiring is more reliable, since it does not depend on the shield wire itself to complete the signal connection. Stranded shield wires are more vulnerable than the protected internal wires, especially in portable installations. A broken ground connection would result in a loss of audio or a very loud hum. Using twinconductor cable, a broken shield may only result in a slight increase in noise or hum due to the lack of shielding.

# Input Connections

#### Input Connectors

The input connectors are XLR and 1/4" phone jacks wired in parallel.

#### NOTE:

IEC standards designate XLR Pin 2 as Positive or "Hot" with pin 3 as Negative or "Low".

Newer JBL products conform to these standards.

JBL equipment manufactured before 1991 was wired with Pin 3 "Hot" Wire the connectors according to the tables below.

SOURCE	CABLE	SR6670A	
SIGNAL		XLR	TRS
High / +	High / +	2	Tip
Low / -	Low / -	3	Ring
Ground	Shield	1	Sleeve

SOURCE	CABLE	SR66	570A
SIGNAL		XLR	TRS
High / +	High / +	2	Tip
Ground	Low/-	3	Ring
Ground	Shield		

□ Wire the signal carrying conductor to the XLR connector pin 2 and wire the low conductor to pin 3. The unused XLR pin 1 may also be connected to shield ground if that is compatible with your grounding scheme.

Table 2: Balanced Source

Table 3: Unbalanced Source

# Output Connections

### Output connectors

Loudspeaker connections use the supplied Neutrik Speakon<sup>®</sup> NL4FC 4 conductor connectors. See Page 14 for wiring configurations.



#### Cable size:

Outside Diameter:6-15 mm (1/4" -5/8")Maximum wire size per contact:6 mm²(solid), 10 AWG<br/>4 mm² (stranded), 12 AWGNote: cable screws require 1.5 mm?? metric hex wrench.

Rear Panel: Output Connectors



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## Output Connections

## Speakon<sup>®</sup> Connector Wiring

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### Stereo

	Channel A			
1+ 1- 2+ 2-				
Signal	Ground			

Channel B			
1+	1-	2+	2-
Signal	Ground		

Aux				
Chan	inel A	Char	nel B	
1+	1-	2+	2-	
Signal	Ground	Signal	Ground	

### **Bi-Amplified**

Bridge-Mono

Channel A - Low Frequency			
1+	1-	2+	2
Signal	Ground		

Channel B - High Frequency				
1+	1-	2+	2	
Signal	Ground			

Alx			
Low Frequency		High Fr	equency
1+	1-	2+	2-
Signal	Ground	Signal	Ground

		Aux	n Na San San San San San San San San San Sa
14	1-	2+	2
Signal+	•	Signal-	

# Turn On Procedure

### Turn on procedure

0	Set the rear panel Mode switch to the required position:
	Stereo, Dual Mono or Bridge Mono.
0	Set the level controls at minimum.
8	Connect audio input and output wiring.
4	Apply program to the input.
6	Turn the power on. The POWER and STANDBY indicators will be illuminated. There is a short delay before signal passes through the amplifier. During this time, the fans will operate at high speed to indicate correct operation and the internal operating points will stabilize. After a few seconds, the STANDBY indicators go off and the bypass relays engage, allowing signal to pass through the unit.
6	Adjust the level controls for desired performance.

# Troubleshooting

Symptom : No Sound

Possible Causes:

#### Power Off:

Check that the power indicator light on the front panel of the amplifier is lit. If it is not, confirm that the amplifier power switch pushbutton is on (depressed) and that the unit is connected to an active AC mains source.

Power On, No Signal Audible:

Input:

The Signal Present light will illuminate when audio is present at the amplifier input at a level of -26 dBv.

Confirm that active audio lines are connected to the amplifier input(s) according to the connection and wiring schemes shown in this manual.

If the amplifier is set in dual mono or bridge mode, the Channel B input terminals are inactive, and input must be to Channel A only.

#### Output:

Check the loudspeaker wiring. In Bridge mode, check that the loudspeaker is connected to the AUX socket and is wired correctly (See Section ??? - Output wiring).

If audio is being fed to the amplifier and the loudspeaker wiring is correct, check that the gain controls are advanced sufficiently to feed output to the loudspeakers.

Standby indicator:

If a STANDBY indicator remains illuminated, it indicates several possible fault conditions:

1 There may be an input overload or infrasonic (below approximately 10 Hz) or DC signals present in the input signal.

2 There may be a short circuit or very low impedance load across the amplifier output terminals.

3 The amplifier may be overheating because the air behind the amplifier may be too hot or the vents may be blocked.

# Maintenance

Physical		
	Dimensions:	19 inch Rack Mounting.
		3 ½ in high (89 mm) by 14 ½ in (368 mm) deep.
		16 in (406 mm) depth to rear of rear rack mounting ears.
	Net Weight	34.2 lbs (75.25 Kilograms)
	Shipping Weight	41 lbs (90.2 Kilograms)
	Materials	Chassis is plated and painted steel. Rack ears and handles are painted aluminum.

### Maintenance

This JBL product is all solid state, ruggedly constructed and uses the finest components. As such it will provide years of trouble free use with normal care. All parts are conservatively rated for their application.

No special preventive maintenance is required.

The metal and plastic surfaces of the unit may be cleaned with a damp cloth. In case of heavy dirt, a non-abrasive household cleaner such as Formula 409<sup>®</sup> or Fantastik<sup>®</sup> may be used. Do not spray the cleaner directly onto the front of the unit, as it may destroy the lubricants in the switches and controls! Spray cleaner onto a cloth and then use the cloth to clean the unit.

#### WARNING:

THERE ARE NO USER SERVICEABLE PARTS INSIDE.

The full AC line voltage as well as high voltage/high current DC are

PRESENT AT SEVERAL POINTS INSIDE THE CHASSIS.

REFER ALL SERVICING TO QUALIFIED SERVICE PERSONNEL.

# Warranty

### Warranty

This product is warranted by the manufacturer to the original USA purchaser against defects in material and workmanship for a period of three years from the date of purchase. Complete terms of the USA Limited Warranty are stated on the warranty card packed with this manual. If this product was purchased in another country, contact your JBL dealer or distributor for information on the terms of the warranty applicable in your country.

If your JBL product ever needs service, please write or telephone:

JBL Professional (Attn: Customer Service Department), 8370 Balboa Boulevard, Northridge, CA 91329 (818) 893-8411

JBL may direct you to an authorized JBL Service Agency, or ask you to return your unit to the factory for repair. In either case, you will need to present the original bill of sale to establish the date of purchase. DO NOT ship your JBL product to the factory without prior authorization.

All products shipped to the factory must be accompanied by a Return Authorization (R.A.) Number and must be shipped prepaid. COD shipments will not be accepted. The RA number should be marked on the shipping label. Be sure the unit is well packed in a sturdy carton, with shock absorbing material such as styrofoam pellets or "bubble-pack" surrounding the unit. Pay particular attention to protecting the controls and switches and make sure that the unit cannot drift around in the shipping box. Shipping damage caused by inadequate packing is not covered by the JBL warranty. Tape a note to the top of the unit, describing the problem, include your name and a phone number where we may contact you if necessary, and give us instructions for returning the product. JBL will pay return shipping costs on any repair covered under the terms of this warranty.

Field repairs are not normally authorized during the warranty period, and repair attempts by unqualified personnel may invalidate the warranty.

# Specifications

### Electrical

Output Power

Impedance	4 ohms	8 ohms	8 ohms bridge	16 ohms bridge
Rated power	600 W	360 W	1200 W	720 W
Midband power	650 W		1300 W	780 W

**Rated Power** is minimum continuous sine wave output per channel, with both channels driving their rated load over a power bandwidth of 20 Hz to 20 kHz. Maximum total harmonic or intermodulation distortion measured at any power level from 250 milliwatts to rated power is less than 0.1%. Maximum Transient Intermodulation Distortion is less than 0.05%.

Midband Power is maximum output power per channel, with both channels driven, at onset of clipping with 1 k Hz sine wave, THD 1%.

Frequency Response:	+0, -1 dB, 20 Hz to 20 kHz, at any level up to rated power.
Output Noise Floor:	< -69 dBu
Signal to Noise ratio:	At least 104 dB below rated output (15.7 kHz noise bandwidth, A-weighted).
Total Harmonic Distortion:	250mW to rated power:
	8 Ohm load < 0.05% 20 Hz to 20 kHz
	4 Ohm load <0.1% 20 Hz to 20 kHz
Input	Balanced bridging differential amplifier.
Input Impedance:	40 k ohms differential input;
	20 k ohms unbalanced (single-ended) input.
Input Sensitivity:	+4 dBu (1.228V) for rated output into 4 Ohm load.
Maximum Input Level:	+24 dBu (12.28V rms).
Input Common Mode Rejection	> 66 dB 20 Hz to 20 kHz
Rise Time:	Less than 6 microseconds (limited by input filter).
Slew Rate:	" Greater than 35 volts per microsecond
Gain:	31.2 dB +/- 0.4 dB (36.4V/V nominal) for rated power into 4 ohms

# Specifications

Output Impedance:	0.025 ohms in series with 2 µHy
Damping Factor:	Greater than 200 at any frequency from 20 Hz to 1 kHz into 8 Ohm load.
	Greater than 30 at any frequency from 20 Hz to 20 kHz into 8 Ohm load.
DC Output Offset:	± 10 millivolts maximum.
Input Connectors:	Female XLR style 3 pin and '4" two-conductor Phone jacks wired in parallel.
Output Connectors:	Neutrik Speakon® NL4FC.
Polarit <del>y.</del>	Positive-going signal on pin 2 of XLR or Tip of TRS jack gives positive-going signal at "+"output terminal.
Controls	Channel Gain (2), Power, Stereo/Bridge Mono/Dual Mono Switch, Ground Lift Switch
Indicators:	Power (1), Standby (2), Signal Present (2), Clip (2)
Amplifier Protection:	Current source shutdown for temperature, SOA (Safe Operating Area), timing and DC fault conditions
Speaker Protection:	Independent series/shunt speaker relays
AC Power: AC mains protection:	Internal Fuses: 110/120 Volt 30 amp 3AB
Power Line Voltage Range:	
	120VAC nominal 90V to 132V, 50/60 Hz
Typical Power Consumption:	
4 Ohm load on ea	ich channel - both channels driven
At idle:	150 watts - 1.3 amps
At 1/8 rated output:	765 watts - 11.5 amps
At 1/3 rated output:	1236 watts - 15.9 amps
At rated output:	2040 watts - 23.8 amps
Operating Temperature:	0* to 50* C
Cooling:	Forced air: two variable-speed 80 mm DC fans

# Troubleshooting

	The Standby mode automatically resets itself and may cycle in and out as long as the fault condition remains. The amplifier will automatically return to normal operation three to five seconds after the fault condition has been corrected.
	Note that the two channels operate independently and one channel may be in the Standby mode while the other operates normally. In Bridge mono mode, if one channel shuts down, the output power is reduced by 6 dB.
Symptom:	Weak and/or Distorted Audio
	Check that a clean signal is being fed to the amplifier. It is possible that the amplifier is reproducing problems originating elsewhere in the audio chain.
	Confirm that the input wiring is correct. If only one side of a floating audio line is connected to the amplifier input, the resultant audio will be weak and distorted, and will have poor frequency response.
	Check that the input line is not being loaded down by too low an impedance. This can occur if more than one terminating resistor is connected across the line, or if the same line is feeding the inputs of multiple devices without isolation, particularly if the unit feeding the line does not have a low output impedance. Confirm that the output impedance specification of the feeding device and the input impedance specifications of the device(s) connected to it are compatible.
	Remove other devices
Symptom:	Hum and/or Buzz
	Make certain that the grounding schemes of the audio signal path and the chassis and power line mains of all units in the system are connected according to the recommen- dations in the Grounding Section of this manual, and follow those guidelines to isolate and correct the problem.
	Hum - Ground loop
	First, lift the ground by means of the rear panel switch marked "GROUND LIFT" - Audio ground will then be isolated from the chassis and and will be referenced to the signal source, The chassis ground will still be connected to mechanical ground for shock protection.

In some instances, the voltage difference between the grounds will be so great that a direct connection to mechanical ground is not possible without hum in the output. The use of an isolation transformer in the input signal line may allow the signal to be connected while maintaining ground isolation.

## Troubleshooting

Check for this using a 3 prong to 2 prong AC adaptor between the power cord and the power outlet, temporarily ungrounding the unit. Try the amplifier with both settings of the ground lift switch. Determine which connection works best.

REMEMBER, FOR SAFETY YOU MUST STILL HAVE A CONNECTION TO CHASSIS GROUND.

This is normally made through a properly grounded third pin connection. However, in some installations, a different method of grounding may be acceptable for both safety and noise. Any alternate method of grounding should assume that full line current will flow in the ground wire under fault conditions, and the wire must be sized accordingly.

#### Hum - Other Possible Causes:

Check the audio at an earlier stage in the chain to confirm that the noise is not already in the input signal.

Power amplifiers have large mains transformers which handle high currents, and, consequently, have significant magnetic fields surrounding them. Some low level equipment is susceptible to hum being induced from external magnetic fields. As a general rule, low level equipment should not be mounted in close proximity to power amplifiers to avoid induction of this type of hum.

Be certain that all audio wiring except for loudspeaker lines is well shielded, and that low level wiring is not run parallel to and/or in close proximity to AC mains wiring, particularly high current and/or lighting lines. If the buzzing changes character or intensity when electrical lighting conditions change, the noise is being induced into the audio from the lighting equipment. It is always advisable to run lighting equipment from its own mains power source and the audio equipment from a separate source. The services of a qualified electrician may be required to solve such problems.

#### Symptom: Intermittent Audio

Check the other equipment and the wiring to make certain that the signal is not intermittent earlier in the chain and that the loudspeakers are solidly connected to the amplifier outputs.

If the audio goes off at the same time that the Standby light on the amplifier is illuminated, see above.

#### JBL SR6670A Power Amplifier High Frequency Switching Power Supply Theory of Operation November 2, 1992 Rev 2 CP

Please refer to Power Supply Schematic drawing # 273769 for reference during the following theory of operation.

A quick overview of the Power Supply shows it provides the high current ±90 volt supplies to the power amplifier's output stages, ±100 volts for the power amplifier front end, bipolar 15 volt supplies to the Input assembly, +5 volts for logic functions, an unregulated bipolar 24 volt power supply for the amplifiers fans, and a Fast Off control function to the power amplifiers should a load condition arise that could cause the power supply to exceed its ratings.

Power line isolation from the AC line Hot is done by the high frequency switching transformer T1. On the primary side of the T1, the circuit functions can be divided up into seven distinct functions. These functions are as follows:

- 1. The power line noise filter.
- 2. Bridge rectifier and filters.
- 3. MOSFET switching transistors.
- 4. Current monitoring transformer & circuitry.
- 5. Low voltage dropout and initial power up circuitry.
- 6. Switchmode controller power supply and gate drive monitoring.
- 7. Switchmode controller.

On the secondary side of T1 one finds the unregulated  $\pm 90$  volt and  $\pm 100$  volt power supplies, regulated  $\pm 15$  volt and  $\pm 5$  volt supplies, a daughter PCB which contains a linear temperature controlled fan speed drive, a temperature sensing protection circuit for the power supply, and an optically isolated power amplifier shutdown circuit.

#### I. Primary Side Circuitry.

### A. Voltage Selection, Rectification and Filtering.

The first element seen by the AC power mains when it enters the product is a potted Line Filter assembly. Current flows from the filter through the power switch S1 which switches both sides of the power line to the fuse F1. Next in the path is a current inrush limiting resistor which limits the initial inrush surge to a value less than 17 amps peak for a 120 V ac power line. Shunting the surge limiting resistor R2 is a triac Q1 whose gate drive is optically isolated from the power line by opto isolator U3. If upon power up, the internal power supply housekeeping circuitry determines that all

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Please refer to Power Supply Schematic drawing # 273769 for reference during the following theory of operation.

A quick overview of the Power Supply shows it provides the high current ±90 volt supplies to the power amplifier's output stages, ±100 volts for the power amplifier front end, bipolar 15 volt supplies to the Input assembly, +5 volts for logic functions, an unregulated bipolar 24 volt power supply for the amplifiers fans, and a Fast Off control function to the power amplifiers should a load condition arise that could cause the power supply to exceed its ratings.

Power line isolation from the AC line Hot is done by the high frequency switching transformer T1. On the primary side of the T1, the circuit functions can be divided up into seven distinct functions. These functions are as follows:

- 1. The power line noise filter.
- 2. Bridge rectifier and filters.
- 3. MOSFET switching transistors.
- 4. Current monitoring transformer & circuitry.
- 5. Low voltage dropout and initial power up circuitry.
- 6. Switchmode controller power supply and gate drive monitoring.
- 7. Switchmode controller.

On the secondary side of T1 one finds the unregulated  $\pm 90$  volt and  $\pm 100$  volt power supplies, regulated  $\pm 15$  volt and  $\pm 5$  volt supplies, a daughter PCB which contains a linear temperature controlled fan speed drive, a temperature sensing protection circuit for the power supply, and an optically isolated power amplifier shutdown circuit.

#### I. Primary Side Circuitry.

### A. Voltage Selection, Rectification and Filtering.

The first element seen by the AC power mains when it enters the product is a potted Line Filter assembly. Current flows from the filter through the power switch S1 which switches both sides of the power line to the fuse F1. Next in the path is a current inrush limiting resistor which limits the initial inrush surge to a value less than 17 amps peak for a 120 V ac power line. Shunting the surge limiting resistor R2 is a triac Q1 whose gate drive is optically isolated from the power line by opto isolator U3. If upon power up, the internal power supply housekeeping circuitry determines that all

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circuit functions are operating properly, gate drive to the opto isolator U3 and turns on the triac which shorts out the series limiting resistor R2. Following the Triac is a bridge rectifier BR1.

For 100 and 120 V ac operation the bridge rectifier and input capacitors C5, & C6 are configured as a half wave voltage doubler circuit with circuit board jumpers W1 and W2 installed on the PCB. Chokes L1 and L2 provide additional high frequency filtering from the MOSFET switches that are connected across the additional filter capacitors C7, C8, C9 & At the line frequency of 50/60 Hz capacitors C5, C7, & C10. C9 are connected in parallel as are capacitors C6, C8, & C10 with the negative terminals of C5, C7, & C9 connected the positive terminals of C6, C8, & C10. The common node of the juncture of the input filter capacitors has the option of being configured either for full wave bridge operation 230 V ac operation by the omission of jumpers W1 and W2, or for half wave doubler operation with the inclusion of the jumpers as stated previously.

The negative terminals of C6, C8, & C10 is the negative most potential in the circuit and is the primary side 'ground' reference, and should not be confused with the secondary grounds. Rectified 340 V DC appears at the positive terminals of C5, C7, & C9. Is important for the operation of the power supply that the source impedance of the AC line is low because the input filter capacitors charge up to the peak of the input line voltage. If there is considerable resistance in the AC line, the large peak charging currents drawn by the 13,200 uF of input capacitance will cause a large IR drop in the AC power line. Consequently, the input capacitors will not charge up to the full 340 V dc. For example, a 0.5 ohm total source impedance can drop 10 volts of voltage with 20 Amp peak charging current.

#### B. Power MOSFET Switching and Converter Type.

MOSFET switching transistor pairs Q2 & Q3 and Q4 & Q5 are connected in series across the 340 Volt DC supply. The output of each pair is the source-drain node of the Q2, Q3, and Q4, Q5. Across the output nodes is the series circuit of the primary of power transformer T1, the primary (a short piece of #16 AWG wire) of current transformer T2, and coupling capacitor C11.

If we ignore the type of drive (which determines the type of Converter the configuration takes) for the moment, the switching action of the MOSFET switches is as follows:

Switching pairs Q2, Q3, and Q4, Q5 alternately turn on and off at a rate of 62.5 kHz alternately reversing the 340 V DC across T1's primary. For example, when Q3 is turned on, Q2 is

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driven off. At the same time, Q4 turns on, and Q5 is turned off. For reliability is imperative that neither of the switching transistor pairs be allowed to conduct simultaneously between each other would happen if either pair of Q2, & Q3 or Q4, & Q5 conducted simultaneously against each Switching 340 volts and high peak currents at high other. frequencies takes a finite amount of time and even the smallest overlap in conduction between any of the switches will cause the MOSFETS to conduct against themselves and be Turning on a MOSFET is easier than turning it off destroyed. To turn the MOSFET because of the physics of the device. either on or off quickly, the peak gate current is in the ampere region, and consequently the gate drive circuitry must be capable of sourcing and sinking several amps of peak current if the switching frequency is high. Consequently, most switching power supply controller IC's have the appropriate dead zones built into their timing functions that is supposed to minimize, if not eliminate, the aforementioned cross-conduction problems.

Capacitor Cll serves a dual function of preventing Tl's core from saturating should there be the slightest asymmetry in the switching drive across the primary, and its value is chosen to resonate with the leakage inductance of the transformer Tl. If the peak current in the primary exceeds a preset value of 40 A, sufficient peak voltage will be present at the secondary side of T2 to initiate self protection of the supply.

It is in the control action of the gate drive where this power supply differs from most square wave converters. First off, the supply is not a closed-loop Pulse-Width-Modulated power supply, nor is it a simple square wave converter. For reasons of long term reliability and power supply noise, the control circuitry configuration chosen is a Zero Voltage Switching Quasi-Resonant power supply. Switching action of the MOSFET switches and the resonate circuit of C11 and T1 is actually quite simple if viewed from the proper perspective.

When, for example, switches Q2 and Q4 switch +340 V volts at the start of T1' primary (the dot), the current in the primary linearly increases from 'ground' through C11 in the primary until it reaches its maximum value as determined by the inductance and on time. At that point, the gate drive voltage is removed for a short period of time. During this interval, the resonant circuit formed by C11 and the leakage inductance of T1 allow the transformer core to reset itself in the opposite direction as the fields collapse before the opposite switching pair, Q3 and Q5, turn on. Thus, the switches turn on with essentially zero voltage across them and dissipate minimum power because the only losses are conductive losses (current x's Rds(on) ) not switching losses (340 V x's current x's average transition time). With this type of drive

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the primary current is sinusoidal for lower radiated and conducted noise.

#### C. Drive Control Circuitry and Housekeeping.

Gate drive control for the MOSFET switches and all other housekeeping functions are performed by the Switchmode controller IC U1, hex Schmidt trigger U2 and all associated circuitry. The theory of operation of the drive and housekeeping section is less straight forward than the switching operation of the MOSFET switches and merits a more detailed discussion as operation of the housekeeping section is not intuitively obvious.

Gate drive control and the housekeeping functions are best understood if one first understands the basic philosophical concepts behind the circuit implementation. Two auxiliary housekeeping functions have been added to the PWM controller IC U1 and its associated functions to insure that the power supply is well behaved under all power line and amplifier In power converter design, it is the undefined conditions. states of operation that ultimately result in undesirable performance aberrations and poor reliability. During abnormal AC power line perturbations, for example, the power supply should not catch its self midway in the power up sequence which could result in premature shut-off of the power amplifier, or worse yet, a continuous recycling of the unit. Performance of the supply during low line conditions is paramount, and the lower line limits need to be well defined. For reliability, the critical MOSFET gate drive is constantly monitored to insure that some type of load condition or drive condition does not pull the supply out of resonance.

Addressing the issues of power supply start up , low line conditions and gate drive monitoring, is hex Schmidt trigger U2 is divided into two sections consisting of three U2. sections each. Each of these sections controls the power supply voltage available to the PWM controller IC U1. The first group of three inverters on the right hand side of the schematic (output pins #'s 2, 4, & 12) make up the low voltage dropout detector and provides a "kick start" voltage to the PWM controller during the power up sequence. If upon power up, the second group of three comparators in U2 determines that all is functioning correctly, then the output of the group continues to keep the source of power to the controller. If things are not functioning properly, then power is removed from the controller and operation ceases. The circuit will not recycle until AC power is removed.

Operation of the first section is as follows:

Seventeen volts DC is provided to the housekeeping section by zener regulator CR8 and current source resistor R4. R4 is

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sourced to the mid-point of the six filter capacitors where the power supply voltage is 170 V DC which reduces its dissipation. Of note, is the fact that the action of the lowvoltage dropout detector shuts the unit off before the 17 volt Zener drops out of regulation.

When power is first applied, capacitors C13 and C14 have no charge on them and hold the inputs (pins #1 & 3 respectively) of the first two inverter sections to ground. Thus the both inverters outputs are high within 1 volt of the 17 volt supply. With the output of inverter #2 high (pin #4), the negative end of capacitor C15 is also high causing the output of the third section (pin #12) to be low. With pin #12 low, the gate of MOSFET Q6 is not enhanced and the MOSFET is off. This is important because Q6 is connected as a series pass transistor that supplies start-up voltage to the PWM controller IC. Input voltage for Q6 is derived from the power supply mid-point for the same dissipation reasons as in the case for R4. In series with the drain of Q6 is CR27 which prevents the substrate parasitic diode inside of Q6 from becoming forward biased when a separate low voltage Lab Supply is used for the initial power up and adjustment phases.

Resistor R15 and capacitor C13 have a short 47 ms time constant and will cause the first inverters output (pin #2) to change states if the power line voltage is approximately 1/2 of its nominal value (60 V rms). Transistor Q8, diodes CR5, & CR4, and resistors R12, R13, & R14 make up a cycle-by-cycle low AC line voltage detector that will allow R16 to continue charging up C13 if the line voltage is too low. Resistors R12, R13, & R14 form a voltage divider from the high side of the line to the primary common. Output is taken at the R13, R14 node (0.1479 :1) and AC coupled through C12 to CR5 into the emitter of the common base stage Q8. For positive AC line peaks, CR5 is back biased and the maximum peak swing is clamped to +17 volt supply by CR4. When the primary AC swing goes negative, the anode end of CR5 is pulled below the power supply 'ground' which forward biases CR5 and turns on Q5 which discharges any charge on C13 and holds pin #1 low. The inverter output, pin #2 is therefore high.

If the AC line voltage is above 60 V rms, pin #2 remains high and allows C14 to continue to charge up through R16 because CR6 is back biased. When the voltage on C14 reaches 2/3 of the 17 volt supply, the second stage trips causing the output (pin # 4) to go low.

At this point we must digress a bit to point out that the output of the second inverter also keeps the saturated shunt switch transistor Q10 'on' during this initial power up sequence. Transistor Q10 is across the LED drive of optocouplers U3, & U4 that are current sourced by R25. With Q10 on, both LEDs in the optocouplers are off and the Triac Q1

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is still off leaving the current limiting resistor R2 still in the primary path.

When pin #4 is low, C15 pulls the input of the third stage (pin #13) low and the output (pin #12) changes to a high state therefore turning on Q6 which supplies power to the PWM IC U1 for a short period of time as C15 continues to charge up through R17. Once the voltage on C15 reaches the trigger trip point of 2/3 supply voltage, the inverter changes state removing gate drive voltage to Q6. Q6 then drops off line, and power in maintained to the PWM controller by transistor Q7 only if the gate drive is determined to be correct.

If the line voltage is too low, the input (pin # 1 of the first stage is allowed to charge up to the supply causing the output (pin #2) to be held low. With the output of the first inverter is low, diode CR6 prevents capacitor C14 from charging up. Thus the output (pin #4) remains high, the triac is held off, Q6 cannot be turned on, and consequently no power is supplied to the PWM controller and the power supply will not start.

The function of the gate drive monitoring circuitry is to control the low voltage supply to the PWM IC U1. If the gate drive output of Ul is incorrectly adjusted for too high a dead time, or not functioning properly, series-pass transistor Q7 is turned off and the system shuts down. The gate drive output of U1 pin #11 is coupled to the base of Q9 via voltage divider R21, & R22. If the duty cycle of the gate drive is greater than about 80% (the unit is set for a 87.5 % duty cycle for resonant operation), Miller Integrator capacitor C18 will charge up and keep Q9 turned on pulling the collector and the input (pin #5) of the sixth inverter low. The output of the sixth Converter is inverted again by the fifth inverter whose output (pin #8) remains low. When pin #8 is low and pin #4 of the low voltage sensing circuit is also low, transistor 010 is turned off and both U3 and U4 are on. The triac Q1 now turns on and shorts out R2. Opto isolator U4 clamps the base emitter of Q16 to ground causing the collector of Q16 to rise to +5 volts which allows the power amplifier modules to now turn on and load down the power supply. If U4 is not allowed to turn on, the base of Q16 is held high through R42, the output of Q16 falls to a Vsat of ground, the cathode of diodes CR39 in the power amplifiers are grounded and the power amplifier will not start its power-up sequence.

With pin #8 of U2 held low, diode CR7 holds the input of the (pin #11) the fourth inverter low thus its output is high (pin #10) and turns on MOSFET Q7 that is the series pass transistor which supplies power to U1. The power supply voltage to U1 sits below the +17 volt supply by the gate threshold voltage of Q7 somewhere between 2 and 4.5 volts.

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If the gate drive duty cycle is too low, the input pin of the sixth inverter (pin #5) rises high causing the output pin # 8 of fifth inverter to go high turning on Q10 thus shutting down opto isolators U3 & U4. Diode CR7 becomes back biased and releases C17 to be charged up through R19. When the voltage at pin #11 exceeds the positive threshold voltage, the output (pin #10) goes low and Q7 is turned off.

#### D. <u>PWM Controller IC, MOSFET Gate Drive and Current</u> Limiting.

Linear IC U1 is a second-generation IC switch mode controller optimized for high frequency power MOSFET drive. It contains a internal regulated reference regulator, oscillator, softstart circuitry, error amplifier, comparators and latches, drive shutdown, and provides two symmetrical inverted gate drive signals for the switching MOSFETS. In the actual implementation of U1, the internal soft-start feature is defeated. However, initial soft starting is provided by the over-current shut-down circuitry.

Resistor R28 in series trim pot R29 connected to pin # 6 of U1 and C23 determine the free running oscillator frequency. As the overall resistance between pin #6 and 'ground' decreases, the frequency of oscillation increases. A small resistance between pins # 5 & 6 can be used to increase the dead time between the alternate MOSFET pair gate drive (the dead time is a small time interval when neither pair of MOSFETS are turned on). Trim pot R27 is used to set the dead time to a period of 1 microsecond.

The inverting input of the internal error amplifier pin #1 is referenced to a +4.5 volts by dividing down the 340 V dc supply by resistors R10, R11, & R26. This voltage reference serves to provide over voltage protection for the supply should the input voltage rise to a value 10% higher than nominal line voltage (120 V AC). The positive input (pin #2) of the error amplifier is held to the +5.1 volt internal reference regulator by direct connection to pin #16. Should the line voltage exceed 132 V ac, the voltage on pin #1 exceeds the 5.1 V reference, and the error amplifier shuts down the PWM controller.

Over current protection is accomplished by using two different shutdown mechanisms in the IC. The first phase of over current protection makes use of shutdown port pin #10. Peak primary current is sensed by current transformer T2. The AC signal is fill-wave rectified by CR1 and CR2, and loaded by R5, R6, &R7. When the peak primary current causes the voltage at the output to exceed the 6.8 volt Zener voltage of CR9, the current drawn through R31 will cause the voltage present at pin #10 to increase to some positive value. The voltage at present at pin #10 is also supplied to the base of Q11 through

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a base current limiting resistor R30. As Q11 turns on, it pulls pin #9, the loop compensation pin negative which reduces the duty cycle of the gate drive.

Normally a reduction in duty cycle would reduce the peak primary current, but in the case of the quasi-resonant topology an reduction in pulse width initially increases the peak current because the primary circuit is being pulled out of resonance. Eventually, the loop will stabilize in a nonresonant condition, albeit less power and peak current. Absolute shutdown of the supply occurs when the voltage present at pin #10 exceeds 1.2 volts. When this happens the shutdown directly accesses the PWM latch and terminates the gate drive within 200 ns. The outputs remain off for the duration of the clock period before the circuit can restart itself.

Gate drive to the switching MOSFETS is transformer coupled by gate drive transformer T3. Because of the high input and feedback capacitance of the large geometry switching MOSFETS, the direct outputs of U1 have insufficient peak current drive capability. Consequently, two complementary MOSFET buffer stages are added to the outputs of U1. Transistors Q12, Q13, Q14, & Q15 serve as the complementary drive for T3. Note that the output buffer is not operated as a source follower but in the inverted mode whereas the gates are easily turned on and off.

#### E. Thermal Shutdown

The thermal protection and fan speed circuitry is located on the daughter PCB and carries its own reference designators not to be confused with the reference designators on the main PCB.

Thermal protection for the power supply is sensed on both of the power supply heat sinks and is of the load disconnect variety. If the power amplifiers' and their subsequent loads present a load sufficient to cause excessive heating of either the input or the output diode bridges, or the switching MOSFETS, the thermal protection circuitry shuts off the power amplifiers thus removing the load from the power supply, and at the same time increases the fans to full speed to cool down the unit. During the power supply thermal shutdown period, the power supply still runs.

Circuitry for the thermal protection is located on the soldered-in daughter PCB. Positive temperature coefficient resistors R4 and R8 do the thermal sensing. Resistor R4 is mounted on the heat sink that carries the switching MOSFETS and output diode bridges BR2 and BR3. Similarly, R8 is located on the heat sink which carries triac Q1, input bridge rectifier BR1, and fan series pass regulator transistor Q17. At nominal operating temperatures the cold resistance is

JBL SR6670A Power Supply Theory of Operation Page 9 of 12 11/02/92 RS C. At 80 degrees C

typically 330 ohms or less at 25 degrees C. At 80 degrees C, the resistance increases to a minimum of 2200 ohms.

Both R4 and R8 and resistors R1 and R3 bias the negative inputs (pins 2 & 6 respectively) of dual comparator U1 to a nominal bias voltage of 0.5 volts above the -15 volt regulated supply. The positive inputs (pins 3 & 5 respectively) of the dual comparator are biased to a point 2.7 volts above the -15 volt supply by resistive divider R2 and R5. In the normal state of operation, the outputs of both comparators are high because the negative inputs are below the reference voltage on the positive inputs. If either R4 or R8 heat up and increase in value above 2.2 kohms the voltage on the negative inputs goes above the positive inputs, and the collector OR'd comparators change state with the output going low to -15 V. The output of the comparators is coupled to the collector of Q16 through R43 and CR25. Diode CR26 is normally reverse biased under these conditions. Since the collector of Q16 and the outputs of U1 are normally at +5 V, there is no potential difference across CR25, and it is effectively out of the When a thermal problem is sensed and the output of circuit. U1 changes state to -15 V, and the node of CR25, CR26, and R43 is clamped to -0.6 V below ground on the secondary side. Since the anode of CR25 is held to -0.6 V, the anode is at ground and pulls the Audio Enable/Fast-Off low therefore shutting off both power amplifier channels. Diode CR1 now becomes forward biased and together with R6 and pull down the threshold voltage on the positive inputs by shunting R5 with This action provides some cool-down hysterysis into the R6. system.

#### F. <u>Fan Speed Control</u>.

Most of the fan speed control circuitry is located on a daughter PC board located on the power supply PCB. The series-pass transistor that supplies current to the two fans, Q17, is located on the power supply heat sink that contains the triac U3 and the input bridge rectifier BR1.

Since the daughter PCB is a different assembly, it carries its own specific reference designators, not to be confused with the reference designators on the main PCB.

The fan control circuitry has several functions. First, full voltage is applied to the fan during initial startup for a short period of time to insure that the fan always starts at low ambient temperatures. Second, a 20 degree C dead zone is purposely designed into the control circuitry to insure that the fan remains at the slowest running speed during average signal conditions. Third, the fan speed linearly increases when the heat sink temperature exceeds 45 degrees C. Above 45 degrees C the fan voltage begins to ramp up from 12 volts to 27.6 volts reaching its maximum at 75 degrees C.

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DC input to the fan speed control circuitry is generated by each of the power amplifier modules. At 25 degrees C the output voltage is adjusted for 0 V dc. As the heat sinks warm up, the control voltage increases at a rate of 39 mV per degree C. At 85 degrees C the fan speed control voltage is therefore 2.34 V dc. Each channels fan control signal is diode OR'd by CR3 and CR4. Resistor R10 and CR5 supply a small reverse voltage on the order of 550 mV which is fed to the cathodes of the diodes via bias resistor R10. High frequency filtering is done by C1. U2B is connected as a voltage follower and buffers the junction of CR3 and CR4. Since the amplifier gain is unity, the voltage at the output pin #7 is the same as the voltage which appears at the anode of CR5. The voltage at pin #7 remains around 550 mV until the control signal voltage increases to a point where either of the diodes become forward biased. Once the control signal overcomes the forward drop of the diode and the reverse bias developed at CR5, the output voltage of U2B will increase. For the values given, the output voltage of U2B will vary from +0.55 to +1.5 V dc for the full range of operation. The circuit values are chosen so that an increase in temperature of 20 degrees C will result in almost constant fan speed.

U2A is configured as an inverting summing amplifier with a control voltage gain determined by the ratio of R15 to R13 (15 V/V), and offset voltage gain determined by the ratio of R15 to R14. The input signals for this stage are the buffered output signal from the first stage U2B and the -15 volt supply. With the values shown, the output voltage of U2A pin #1 ranges from a quiescent level of  $\pm 1.89$  V dc to  $\pm 13$  V dc for full speed. The output of U2A is connected to the  $\pm 15$  volt supply through the series string of CR7, R12, CR6, and R11. For the values shown, about 1.1 mA flows from the  $\pm 15$  volt supply to the output of U2A.

Transistor Ql has its base connected to the junction of CR6 and R12, and, with emitter resistor R10, is more commonly known as a current mirror. Diode CR6 offsets the  $V_{be}$  of Ql. Since the emitter resistor of Ql is the same value of R11, any voltage changes across R11 are mirrored across R10. A 2:1 change in current in R11 causes a corresponding 2:1 change in current in Q1.

Level translation from the regulated bipolar 15 volt regulators to the unregulated bipolar 24 volt input to the regulators is done by Q1's collector. The collector load resistor (R16) for Q1 is also the input bias resistor for the fan speed control amplifier. Transistors Q2, Q3, and Q17 and their associated components comprise the fan speed control amplifier which operates on the unregulated side of the low voltage supplys. Because the 24 volt fans draw 0.5 amps of current, excessive dissipation on the + and - 15 volt

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regulators is eliminated if the source voltage for the fans is located before the regulators. With the fans located on the primary side of the regulators, 48 volts is available under normal conditions for the fan supplies. At full speed, the fan series pass transistor Q17 will dissipate 10 Watts of heat. Dissipating 10 Watts of heat in Q17 is not a problem because Q17 is located on one of the main power supply heat sinks. From a packaging stand point, this is a better choice than attempting 5 Watts of dissipation in the 15 volt regulators.

Transistors Q2 and Q3 form the input differential amplifier and are current sourced by resistor R17 which supplies 1.86 mA of current to both transistors. The collector load for Q2 (R44) is located on the main PCB. For heat sink temperatures less than 45 degrees C, the voltage developed across R16 by the current mirror Q1 is 6 volts. Transistor Q17 is the second stage of the circuit, and is the fan driver (or seriespass) transistor with its the load being the fans and resistors R20 and R19. R19 and R20 are also the feedback resistors and set the gain of the fan speed control amplifier Capacitor C3 is also connected across the fans to 2.0 V/V. and acts as a filter to remove most of the fans' PWM noise. Since the range of the control voltage into the current mirror is 2.2:1 the fan control amplifier input voltage will vary from 6 V to 13.75 causing a corresponding 12 V to 27.5 V change in output voltage.

Components CR7, CR8, C2, and CR9 are used for high speed start-up and for the thermal-off conditions. When power is first applied and the 15 volt supplies come up, and pin # 1 of U2A finds its normal operating point which would result in a nominal fan voltage of 12 V. At the instant of start-up, however, C2 has no charge and consequently holds the cathode of CR8 to -15 V. This back biases CR7 and pulls the R12 to within on diode drop of the -15 V supply. This action has the same effect as the output of U2A going to the -15 V supply and which by action of the current mirror causes the fan speed control amplifier to supply full voltage to the fans. As capacitor C2 charges through R11 and R12, the fan speed decreases until the voltage at the positive terminal of C2 is the same as is on pin #1 of U2A. To insure that the fan goes through the start-up cycle if power to the unit is removed and then cycled back on in a short interval, diode CR9 provides a rapid discharge path for C2 once the 15 volt supplies drop to 50% of their initial value.

Full fan speed during thermal shut-down is accomplished by the addition of CR2 which is connected to the output of the thermal comparators UIA&B and diode OR'd into the current mirror circuitry. During the thermal-off conditions, one of the outputs of UIA&B changes state from +15 to -15 V. This action pulls R12 to within one diode drop of the -15 V supply

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and the fan speeds up to maximum. When the power supply heat sinks cool down, the U1A&B changes state to +15 V which inturn back biases CR8 and normal fan operation resumes under control of the power amplifier heat sink temperature and associated circuitry.

#### II. Secondary Side Components.

The high current  $\pm 90$  volt supplies are full-wave rectified by 30 Amp half-wave bridges BR2 and BR3. Between BR2 and BR3's outputs are two Amobeads (placed on the leads of the bridges) that reduce the diode bridges reverse recovery energy and hence RFI noise. Capacitors C34 and C35 are the input filters connected directly to the fullwave rectifiers. Floating on top of the  $\pm 90$  volt supplies are two 10 volt supplies that supply  $\pm 100$  volts to the power amplifier front end and driver stages. These 10 volt supplies are full-wave rectified by CR10, CR11, CR22 and CR23. Bleeder resistors R37, R38, R39, & R40 discharge the filter capacitors after the power has been removed.

Three low voltage regulated power supplies are provided by U5, the +15 volt regulator, U6, the -15 volt regulator , and U7, the +5 volt regulator. Diodes CR18, CR21, & CR24 protect the regulators in a event where the input of the regulator falls below the output of the regulator. Diodes CR19 and CR20 prevent the regulators from becoming reverse biased in an event of a load failure such as a shorted IC. Amobeads are also used to ameliorate the reverse recovery effects of the rectifiers in generating RFI for the bipolar 15 volt supplies. Fuses F2 and F3 provide protection for the low voltage secondary in the unlikely event of a shorted power rectifier diode or defective regulator.

#### General Overall System Description

#### Theory of System Design

December 9, 1991

Rev 1 CP

For purposes of discussion, please refer to the SR6660A Block and Wiring Diagram drawing # 263175.

The SR6660A is basically a modular in design and consists of two identical Power Amplifier Modules, an Input Module, a LED Display Module, a high current Output Connector Module, and a High Frequency Switching Power Supply.

In order to minimize the total number of discrete wires and cable harnesses that would normally be required to interconnect the various assemblies, all control lines from the Power Supply and Power Amplifier Modules terminate at the Input Module. For example, all of the control lines for the LED status indicators for each Power Amplifier pass through the Input Module to the LED Display Module on one common 16 conductor ribbon cable, thus eliminating the need of using two separate cables from each Power Amplifier Module in addition to the input cables that already exist. Each Power Amplifier Module has two high-current output lines, a 10 conductor power cable, and one 16 conductor Input/Control Line cable.

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All the audio signal control functions of Gain, Stereo operation, Dual Mono operation, and Mono-Bridge operation are implemented in the Input Module. The Input Module in addition to performing the signal switching and level functions supplies 12.2 dB of system gain, and is also the interface point for the optional accessory modules. Two three pin programming shunts break the signal normal in the Input Module to facilitate the accessory functions.

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From the Input Module, the signal is fed to the Power Amplifier Module where an additional 20 dB of voltage is provided.

Supplying power to all assemblies is a 2.5 KVA high frequency switching Power Supply Module that provides the  $\pm 90$  volt high current power supply and the  $\pm 100$  volt supplies to the Power Amplifier Modules, the  $\pm 15$  volt supplies to the Input Module, and  $\pm 5$  volts for logic functions.

# Input Stage Theory of Operation December 10,1991 Rev 1 CP

Please refer to schematic drawing # 261724 for reference during the theory of operation for the Input Stage Assembly.

The Input Stage assembly used in the SR6660A serves several functions. First, it is the equipment interface with the outside world that accommodates either differential or unbalanced inputs. Second, it provides all of the control functions for power amplifier configuration such modes of operation, gain, and system grounding. Third, it is the point where the accessories are interfaced to the system.

For independent two channel operation the signal paths are identical, so the theory of operation will be essentially be confined to Channel A.

Input to the power amplifier appears on either the 3-pin Female XLR connectors J1 & J3, or on the tip-ring-sleeve 1/4" phone jacks J2 & J4. Both the XLR and the phone jacks are wired in parallel with pin #2 of the XLR connected to the tip of the phone jack, and pin #3 of the XLR to the ring of the phone jack.

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Following the IEC convention, pin #2 of the XLR connector is the + Input to the system, and pin #3 is the - input to thesysrem.

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Resistors R1 & R2 set the maximum input impedance in the audio band to 20 kilohms  $\pm 1$ %. Hence the differential input impedance is 40 kilohms, and for unbalanced operation the input impedance is 20 kilohms. Resistors R3 & R4 and capacitors C1 & C2 provide high frequency attenuation of unwanted RF signals shunting the signals to ground. Capacitor C3 is not ground referenced and shorts the two inputs together at high frequencies further desensitizing the circuit to RFI. To achieve the maximum amount of common mode rejection at low frequencies such as AC power line components, the inputs to the differential amplifier stage are direct coupled because the finite difference in input capacitor reactance can degenerate the ultimate input common mode rejection by as much as 40 dB caused by typical production tolerances in the input capacitors if they were used.

Differential to unbalanced conversion of the input signal is done using the classic three op amp version of an instrumental amplifier made of U2A&B, and U3B for Channel A. Op amp U2A&B is set for a voltage gain of unity and serves as a very high impedance buffer on the input resistors R1, R2, and the RFI network at the input, while providing a very low source impedance for the differential summing amplifier U3B. Resistors R5 & R6 are in series with the high impedance input of the IC's and serve two functions. First, R5 & R6 limit the maximum input current

into the input devices of the IC if for any reason a fault at the input exceeds the  $\pm 15$  volt power supply. Second, they define the minimum input impedance of the system when the amplifier is switched off, yet is still connected across a distribution line that is still active with other products that are operational. Although the input buffer stage has its input impedance in the megohm range when it is active, the input characteristics look like a couple of low impedance diodes when the power is switched off and would therefore severely load down any audio distribution line. A disadvantage, however, is that their inclusion adds another 17.8 nV/(Hz)<sup>1/2</sup> to the system.

Operational amplifier U3B sums the outputs of U2A&B with a nominal voltage gain of 0.487 (-6.2 dB). Resistors R10, R12, R11, & R8 set the gain of this stage. Trim pot R7 is used to trim the common mode rejection of the input stage. The topology used is not the classical trim at the positive input for reasons of long term temperature drift, adjustment sensitivity, and component tolerance. In the configuration shown, the trim pot is voltage driven and its tolerance is removed from the circuit. The circuit and be adjusted for common mode rejections of over 100 dB with this configuration, the only limiting factor being the mechanical stability of the trim pot selected.

Because the summing gain is -6.2 dB, the input stage will handle signals up to +27.5 dBu (18.37 V rms) differentially. Above that point both the input buffers and the summing amplifier begin

clipping simultaneously. For unbalanced input signals, the maximum input signal level is still limited to the maximum input signal that can be handled by a unity gain buffer which is +21.5 dBu (9.21 V rms) for the IC'c used and  $\pm 15$  volt power supplies.

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Operation of Channel B is identical except for the signal routing for the various modes of operation.

Channel A's input stage output appears at P9 which is programmed for continuous signal transmission of the signal to the Channel A Gain Control, and at pin #13 of connector P2 to supply a signal for the signal present indicator on the power amplifier module.

Since the Input PCB is located on the rear panel of the SR6660A, the Gain Controls are located of the front panel, and the 2.5 KVA high frequency switching power supply is between the two, proper shielding of the cable connecting the gain controls to the input PCB is imperative. The shielded cable used is a 100% electrostatically shielded cable that has its shield terminated at the power supply return on the Input PCB. Should the shield contact any other conductor, or the chassis, HF switching noise will be present in the output of the power amplifier.

The function of P9 and its mating shunt J9 is to break the signal loop to insert an optional Compressor/Limiter module or a Two-Way Electronic Crossover into the system. Channel A's input stage

output is also is routed to the Mode Switch SW1 which selects either Stereo, Dual Mono, or Mono Bridge mode of operation.

From the Channel A Gain control, the signal next goes to op amp U5A set for a gain of 8.32 V/V (18.4 dB) that makes up for the 6.2 dB loss in the input stage and provides for a more favorable system gain structure in rejecting power supply induced noise in the system. Resistors R16 and R17 set the gain of this stage. Capacitor C18 aids in the RFI immunity of the stage by providing a common mode path to both inputs at high frequencies. Resistor R15 provides a finite impedance to the input which minimizes the minute high frequency ground currents that can floe in the signal grounds if the Gain control is turned all the way down. Overall voltage gain for the Input Module is 12.2 dB (4.07 V/V).

The signal path of Channel B's input stage is not as straight forward as in Channel A. The output of the Channel B input stage is first routed to the Mode Switch SW1A. Also routed to other sections of SW1 is the output of Channel A's input stage, the output of Channel A's signal amplifier U5A, and the input to Channel B's signal amplifier through R33. In the Stereo Mode of operation the signal path is as in Channel A. For the Dual Mono Mode of operation, the <u>Output</u> of Channel A's input stage feeds both gain controls, and also a signal for Channel B's signal present line on P3.

In the Mono Bridge Mode of operation, the Channel B input stage is not used as all gain control functions are done with the Channel A Gain Control. The output of the Channel A signal amplifier U5A is connected to the negative input (pin #6) of U5B through R32 and SW1C. The positive input of U5B is grounded through SW1B. In this configuration U5B functions as a unity gain inverting amplifier as determined by the ratio of R35 divided by R32. Although the noise gain of U5B increases to 22 dB, the output noise floor does not sufficiently to degrade the S/N ratio of the amplifier. Both halves of U5 now feed identical but out of phase signals to the A, & B channel power modules.

Power supply filtering for the module is done with L1, L2, L3, C13, C14, C15, & C16. At the power supply ripple frequency of 125 kHz the inductors present a reactance of 259 ohms which limits the power supply return ground currents. Inductor L3 provides a low impedance ground path at low frequencies, but breaks up the high frequency ground currents that would flow between the three main system grounds. These grounds are the power supply AC ground located near the front of the chassis (grounds for high frequency inverters must be kept short **S**f they are not grounds), the third wire safety ground located on the rear panel, and the main circuit signal ground located at the mid point of the chassis in the rear center. Ideally all these grounds should be at the same point, but that is a physical impossibility.

Signal Ground and Chassis Ground lift is done with switch SW2A that shorts out the parallel RC network R36, C17, & C22. When the two grounds are separated the AC impedance between chassis and the audio ground is 91 ohms which is sufficient to break up any ground-loop phenomena with external equipment. For good RFI immunity in applications where there is substantial RF on the input cabling, the shield (pin #1 of the XLR) must have a low impedance path to the chassis to be effective. This requirement, however in mutually exclusive with the concept of a Ground Lift switch. The network as previously described solves both of these system problems.

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As was discussed in the in the General Overall System Description section, the Input Module serves as a central communications hub for the entire amplifier. Many control functions from the power amplifier modules are routed through the Input Module as can be easily seen by inspection of the schematic diagram.

## Power Amplifier and Slave Assembly

Theory of Operation

December 12, 1991 Rev 1 CP

Please refer to schematic drawing # 261693 during the Power Amplifier theory of operation section. To simplify the analysis of the schematic, the power amplifier circuitry can be thought of consisting of a basic amplifier section and a housekeeping section that monitors and controls the operation of the amplifier. The primary housekeeping section performs the following functions:

- 1. Provides a delayed power up for silent turn-on.
- 2. Mutes the output in event of power supply failure or large AC power line drop outs thus preventing the subsequent power up phenomena caused by down-stream equipment.
- 3. Provides an intelligent power transistor safeoperating-area (SOA) protection for the output stage.
- 4. Provides a linear DC signal for the fan speed control and independent thermal shut-down for each channel.
- 5. Provides for DC speaker protection.

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The secondary housekeeping functions consist of all of the LED display functions, reporting functions to the microprocessor in the ES1200, control signals to the peak compressor, and a fast-

off control line that is activated by either loss of AC power or over current conditions in the power supply.

Because almost all of the power amplifier functions are controlled by the primary housekeeping circuitry, we will begin the theory of operation with the housekeeping section.

## Housekeeping Section

## A. Low Voltage Power Supplies

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To enable the power amplifier to operate over a large range of power supply voltages where the  $\pm$ Vcc1 supplies could vary from  $\pm$ 32 Vdc to  $\pm$ 100 Vdc, the bipolar 15 volt power supply for the control circuits is derived from the main high current power supplies by constant current sourcing Zener diode regulators. Since the operation of both the positive and negative 15 volt supplies is identical, we will analyze the positive supply only. Diodes CR1 & CR2 are biased through R2 at a nominal bias current Large fluctuations in power supply voltage will cause of 1 mA. a relatively shift in bias voltage as a 2:1 change in power supply voltage will result in less than a 10% change in the reference voltage established by the two diodes. Consequently the base of Q1 is held at about 1.2 volts below +Vcc1. At normal operating temperatures, 0.6 volts appears across Q1's emitter resistor R1 thereby establishing a relatively constant current of 40 mA. The collector of Q1, however, has two 15 volt zener

diodes CR13, & CR14 is series. CR14 is the +15 volt supply and is bypassed by C16. The action of CR13, however, is not so obvious. The purpose of CR13 is provide enough power supply hysterysis to insure that the power amplifier will go through the entire re-timing cycle should the power be turned off and then re-cycled on before all supplies were totally discharged. As the +Vccl power supply discharges to a point where the absolute voltage drops below 32 volts the Zener diode CR13 becomes back biased and therefore unable to supply any current to the Zener regulator CR14. At this point there is a rapid decrease in the 15 volt power supplies and the amplifier is muted. Since the dropout voltage of the output relay K1 is not predictable and is around 32 volts, it is important that the housekeeping circuitry have a rapid off feature past a pre determined value. With the exception of the output relay, the preponderance of the housekeeping current draw is between the  $\pm 15$  volt supplies.

B. Turn-On Delay and Protection Timing

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All delay/timing functions are controlled by one section of comparator U2 (pins # 8,9 & 12). When power is first applied, pin #8, the negative input of U2 is biased to a point between 2.5 and 3.9 volts by the series network R92 & CR40. U2's positive input (pin #9), however is held at ground potential as capacitor C21 begins to charge through resistors R88 & R87. During this time, the output of U2 (pin#14) is held to within one Vsat of the -15 volt supply, and the power amplifier circuitry is totally off as there is no bias current flowing in any of the power

amplifier stages. After a period of approximately one second, the voltage on U2's positive input exceeds the bias voltage on the negative input and the comparator changes state with the output voltage rapidly rising from -14 volts to +5 volts. Because IC's U2 and U3 are comparators with open NPN transistor collectors for outputs, some form of collector pull-up resistor is necessary. Consequently the maximum output voltage developed at pin #14 is limited to +5.1 volts by the fact all load current is sourced through pull-up resistor R89 which also sources current to resistor R103 that is diode clamped to ground by CR42, and resistors R50 & R51 that are also clamped to ground by the base-emitter junction of Q19 (the relay driver), and the Standby LED shunt switching transistor Q27 via R110 & R109. U2's output voltage is purposely clamped to +5 volts because it also sends a 5 volt reporting signal via series resistor R116 to microprocessor for future use.

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When the output of U2 (#14) changes state from low to high, the power amplifier circuitry is turned on by the mute switch transistor Q30. Since resistors R50 & R51 supply base current to Q19, the output relay is energized. A short delay for the relay is provided by the time constant of C9 & R51 that allow all turnon transients to settle out before the load is engaged. Diode CR18 prevents Q19 base-emitter junction from breaking down when the output of U2 is low at -14 volts. Fast relay turn-off is provided by the inclusion of diode CR10 that becomes forward biased when U2' output goes low (negative).

Transistor Q30 is a switch in series with the bias voltage string that turns on and off the first stage current source transistors Q21 & Q41. Starting at the +15 volt supply, the most positive portion of the circuit, current flows through R72, CR32, R73, Q30, R121, CR40, & R120 to the -15 volt supply when Q30 is on. Q30 is biased on through resistor R103 when U2's output is high, and has the base clamped to one diode drop above ground by CR42. Operating as a saturated switch, the collector to emitter voltage of Q30 approaches 0.2 volts, hence resistors R73 & R21 are essentially tied together. Bias current through the network has a nominal value of 1.07 mA and will vary in proportion to the tolerance (5% typ) of the + & - 15 volt Zeners CR14 & CR16 respectively.

#### C. DC Speaker Protection

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Symmetrical equal threshold DC protection is provided by Q24, CR37, R87, R88, R85, R49, & C20. For a positive going fault, capacitor C20 begins to charge up through R49 until Q23 turns on. When Q23 turns on, the timing capacitor C21 is discharged through R89 and Q23. R89 limits the peak current in Q23. With C21 discharged, comparator U2 (#14) changes to the low state thereby turning off Q30.

Circuit action for negative faults, however, is somewhat different. A negative fault will charge up C20 in the opposite direction and turn on Q22 and therefore grounding the negative gate bias that holds the JFET Q24 off as Q24 needs at least 7

volts of negative gate voltage to remain in the off state. With no gate bias, Q24 turns on and discharges the timing capacitor as Q23 did for positive going faults.

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# D. Microprocessor Mute and Low Voltage Power Supply Shutdown.

The uP Mute function is provided by the second section of U2 (pins 10, 11, & 13) that has its negative input (#10) referenced to the bias voltage developed at pin #8. The positive input (#11) is biased to a point 2/3 of the total supply voltage by R90 & R91 and typically sits at +5 volts. Control from the uP into the timing circuit is diode coupled via CR39 to pin #11. A logic low (0 volts) at the cathode end of the diode clamps the positive input below the reference voltage on the negative input causing the output of U2 to change from its normally high state to the -15 volt supply discharging C21 through the current limiting collector load resistor R129. When C21 is discharged and the second section of U2 is held on, output current for U2 (#13) is supplied through diode CR37.

If the +15 volt supply is lost or at a low value, three things happen. First, neither the bias reference voltage can be developed on pins #9 & 10 of the first two comparators of U2, nor is there any voltage available to charge up the timing capacitor C21. Second, the reference voltage developed at the positive input by the series bias string of R90 & R91 sits at a potential below the reference voltage on the negative input. Consequently,

the output of the comparator is held in the negative most state preventing any timing cycle. If the -15 volt supply fails, then Q24 turns on, discharges C21, and clamps the positive input of the timing comparator to ground preventing output of the comparator from ever going high and turning on the power amplifier.

## E. Thermal/Fan Speed Control

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Thermal sensing is done by Q7 which is mounted on the heat sink and is connected as a base emitter multiplier. In the active region with 2.2 mA of collector current, the Vbe(on) voltage is centered around 650 mV at 25 degrees C. Q7's Vbe is multiplied by the ratio of R14/R13 +1 and is 17.4 x's Vbe or approximately 11.3 volts nominal. Since the base emitter junction decreases about 2 to 2.2 mV per degree C (the exact value is a function of the semiconductor fabrication process) the actual multiplied value for the device chosen is close to -39 mV per degree C. R58 served as the current source load for Q7. Transistor Q20 with diode CR20, trim pot R52 and R53 form an adjustable voltage source to the emitter of Q7 so that the voltage developed at the collector of Q7 can be trimmed to a nominal value of 0 volts with respect ground, thus allowing for a typical production spread in base emitter on voltages.. During the trimming process the emitter of the adjustable voltage source Q20 raises or lowers the entire Vbe multiplier section as a whole entity. As Q7 heats up, the multiplied temperature coefficient of the base emitter multiplier causes the collector to emitter voltage to collapse

therefore raising the voltage at the collector of Q7 from zero volts to a positive value at the rate of 39 mV per degree C. Q7's collector voltage is routed to the power supply assembly via connector P3 and provides a linear temperature control voltage for the fan speed control circuitry and to the negative input (#6) of the third section of the quad comparator U2. Bias for U2's positive input (#7) is derived by the ground referenced voltage divider R55 & R54 setting the positive input at +2.31 volts  $\pm 5$ % Under normal operating conditions, the comparator output is held high by the collector pull-up resistor R57 therefore back biasing CR21. At heat sink temperatures approaching 85 degrees C, the temperature dependent action of Q7 causes the voltage at the negative input to rise to a point where the reference voltage on the positive input is exceeded. At that point, the comparator output (#1) changes state with the output going to within a volt of the -15 volt supply and discharging the timing capacitor C21 through CR22. Heat sink cool-down hysterysis is designed into the circuit by the action of resistor R56 and CR21. When the output is in the low state, the additional current pulled through load resistor R55 causes the reference voltage on the positive input to decrease from 2.31 volts to 1.95 volts thus adding about 10 degrees of cool-down hysterysis into the system.

#### F. SOA Shutdown

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Absolute amplifier shutdown during fault conditions (why continue to source many amps of current into a short circuit?) is

guaranteed by the action of the one-shot multivibrator formed by the fourth section of U2. Components C12, R60, R61, CR48, CR23, & C11 along with the last section of U2 comprise the one-shot. During quiescent conditions R60 holds the positive input (#5) high with respect to the negative input (#4) that is ground Resistor R59 serves as the collector pull-up referenced. resistor for this stage and holds the output positive which reverse biases CR48 under quiescent conditions. Trigger input to the one-shot is made with R61 that is connected to the collector of Q39 that functions as a level shifting transistor from the negative high current supply -Vcc1. When Q39 is turned on, the node connected to the positive input (#5) is pulled slightly below ground buy the negative pulses generated every time Q39 turns on. Input protection of the comparator is provided by CR24 if for any reason a pulse tries to pull the input below the -15 volt supply. Capacitor C12 integrates the negative going pulses and begins to charge up with the voltage at the positive going increasingly negative. When the voltage falls below the ground referenced negative input, the comparator changes state and its output goes to negative 15 volts. When the output goes low, capacitor C11 pulls the positive input to the -15 volt supply before it begins to charge up through diode CR24 (which is now forward biased) and resistor R60. This action insures that the output of the one-shot will stay low for a period of time determined by the time constant of R61 and C11 (the charging time is approx 70 usec.) for the output of the SOA one-shot to discharge the timing capacitor C21 through CR38 and R129. Once the voltage on Cll reaches a point where the anode end of CR48 is

above ground reference of the negative input, the comparator changes state, with the output again rising high. Capacitor C11 then discharges its remaining 14 to 15 volt charge pn C21 through R59 and CR23.

II. Secondary Housekeeping Functions - Peak Detection, Signal Present, and LED Status Indicators

#### A. LED Indicators

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It is helpful to refer to the LED Display schematic drawing # 261614 in conjunction with the power amplifier schematic to understand the LED signal indication portion of the circuitry.

To reduce excessive dissipation in the  $\pm 15$  volt regulators, and insure quiet operation, all LED indicators are series connected for minimal power supply current draw. Current for the LED's is provided by current source transistor Q25. R98 & R95 bias the current source transistor base to a point 1.2 volts below the  $\pm 15$ volt supply. Since the Vbe(on) voltage for Q25 is 0.6 volts, 0.6 volts also appears across emitter resistor R97 setting the LED current to 8 mA. All of the LED's are controlled by saturated shunt switching transistors which divert the constant LED current through the saturated switch rather than through the LEDs. Because three of the LEDs are shunted by the open collector outputs of U3, the sequence of the LEDs in the series string is

of consequence. Starting from the collector of Q25 and progressing down to the -15 volt supply the LEDs are as follows:

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- 1. Signal Present
- 2. Standby
- 3. Power
- 4. -24 dB
- 5. -6 dB
- 6. Peak

In the normal state of operation, all LEDs except the Power LED are off and the current passes through the saturated switches. Transistor Q26 is the shunt switch for the Signal Present LED, and Q27 is the switch for the Standby LED. U3 output pin #1 shunts the Peak LED, pin #14 the -6 dB LED, and pin #13 the -24 dB LED (note that the -6 & -24 dB LEDs are used on other models).

All sections of the quad comparator U3 are biased from a common resistive ladder consisting of resistors R111 through R115. This ladder is referenced to the positive +Vccl unregulated rail so that the signal level LED's retain their calibration below maximum output as the power supply voltage changes. Reading the schematic from left to right , the first section of U3 (output pin #2) has a positive bias on the positive input and is normally high +15 volt state. R96 is the output pull-up resistor. Consequently, the base of Q26, the Signal Present switch, is held positive with respect to its emitter and the device is turned on.

B. Signal Present Detection

The signal present amplifier U1B (pins 5,6,& 7) is set for a gain of 25.5 V/V sufficient enough to amplify the 19 mV signal input signal to a point where CR27 turns on and half wave rectifies the signal that is subsequently averaged by R62, R63, & C13. When the rectified signal level exceeds the 67 mV bias on the positive input, the output of U3 (#2) changes state turning off Q26 and the Signal Present LED on.

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The Standby LED switch is Q27 which is driven from the output of the timing comparator U2 (#14) through resistors R109 & R110. When the output of U2 is low (-14V), Q27 is off and the Standby LED is on. When U2 changes states and turns on the power amplifier, the +5 volts applied to R110 turns Q27 on shunting the current around the Standby LED.

Output signal as metered by the -6 dB and -24 dB LEDs is controlled by half wave rectifying an attenuated output signal via CR25, R93, R107, & C28. The maximum peak output signal must be limited (normally it could be ±90 volts peak) to a value below the ±15 volt supplies to prevent damage to U3, hence R93 and R107 are a 9.9:1 attenuator. Signal averaging is done by the time constant of R107 and C28. As the signal averaged DC exceeds the preset reference voltage on the negative inputs of the comparators which holds them in a low state, the comparators release each of the respective LEDs as the internal output transistors are no longer shunting current around the respective LED's.

#### C. Peak Detection

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Although the Peak LED shunt switch works as in the signal level LEDs, the detection scheme merits somewhat a more detailed discussion of operation as the operation of the circuitry is not obvious. Control for the peak section is implemented with a bipolar peak detector ULA (pin #1).

R67, CR30, & R66 form a series bias string that insures that U1B is always in the low state because the negative input (pin #2) of the comparator is 0.6 volts above the positive input (pin #3). Thus with the output low, diode CR26 is back biased and no positive voltage is developed at the positive input (#9) of U3.

Pin #2 the negative input is also connected to the collector of Q35 through resistor R80 that limits the maximum current during detection to maximum value of 0.9 mA during the worst case no load, high line conditions (maximum signal swing). Q35 has its base connected to the -Vccl supply which level shifts the detected peak signal up to comparator U1A. In similar fashion pin #3 the positive input is connected to Q40 through R128 which level shifts the detected signal downward to the comparator. Diodes CR31, CR28, & CR29 are used in conjunction with CR30 to clamp the maximum peak signal into the comparator to a level less than 1.3 volts.

For positive peaks, operation is as follows:

When the peak signal level at the collector of Q18 rises above the +Vccl power supply by approximately 1.2 volts (two diode drops), level shifting transistor Q40 turns on as it is now being current sourced by transistor Q18 and now operates in the common base mode of operation. Clamping the signal swing to +Vccl supply also prevents Q18 from being driven into saturation at high frequencies during over-drive conditions eliminating the phenomena commonly known as "sticking". During the peak clamping process, Q40 pulls the collector end of R128 very close to +Vcc1. Current then flows through R128 & R66 to the -15 volt supply, back biases CR30, and to ground through CR28 and CR31 which is now forward biased. Thus the voltage on the positive input rises above the negative input by one diode drop and the comparator changes state generating positive output pulses. The positive pulses turn on CR26, and are averaged by R94, C29, & R108. This DC voltage appears as a variable bias on pin #7 of the peak LED comparator and will cause U3 to change state once the 2.25 volt threshold is exceeded. The output of UIA is also routed to the Input PCBA through the 16 pin I/O connector P3 for signal control in the Peak Limiter/Compressor option module.

Peak detection operates in similar fashion for negative detected pulses except the action is reversed. During detection, Q35 is now turned on and pulls R80 to the -Vcc1 supply. This pulls the positive input below the negative input by back biasing CR30. Now current flows from the +15 volt supply through R67 and CR31, and to ground through the now forward biased diode CR31 and CR29.

Since the negative input is now one diode drop below the positive input the input polarity is reversed and the comparator changes state.

#### III.

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# Power Amplifier Section

The SR6660A power amplifier circuit topology is complementarysymmetry symmetrical six stage design (it is possible to argue semantics at this point and refer to the design as a three stage design) that is optimized for wide open-loop bandwidth and high linearity for any type of load.

Short circuit protection, and abnormal load protection for the amplifier is a two phase process and consists of summed VI (voltage and current) sensing that triggers total amplifier shut down via the Housekeeping section for sustained faults, and also instantaneous protection should load conditions take the output stage outside the transient safe operating area. By using a two phase protection scheme the SR6660A can deliver considerably more useful power into a reactive loudspeaker load than if more conventional methods such as brute force current limiting are used.

Because the gain and output stages of the amplifier are totally symmetrical the preponderance of the discussion will be limited to the positive half of the circuit.

The SR6660A's input stage consists of two complementary NPN and PNP cascode connected differential amplifiers. Each of the NPN and PNP differential amplifiers Q28A&B and Q29A&D are matched dual monolithic pairs that exhibit low noise and high gain, thus eliminating the requirement of an integrator to maintain a reasonably low DC offset at the output of the amplifier. The positive differential amplifier consists of matched NPN pair Q28, NPN current source Q41, and NPN cascode transistor Q31. A cascode input configuration is used for several reasons. First, a cascode topology yields the greatest high frequency bandwidth and lowest distortion. Second, it allows for the use of a low noise high gain input pair to be used because the cascade device stands off the high voltage +Vcc2 that can be as high as +115 V Typically low noise, high gain devices have breakdown dc. voltages form 40 to 80 volts. The cascode transistor Q31 increases the bandwidth of the stage by effectively shorting out the voltage dependent non-linear internal feedback capacitance (Cob) present in every semiconductor. This capacitance is commonly referred to as Miller Capacitance and it is one of the dominate sources of high frequency distortion in large signal amplifiers. Similarly, transistors Q21, Q36, & Q29A&B form the negative half differential amplifier.

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When transistor Q30 turns on, the voltage developed across R120 is mirrored to the emitter resistor (R119) of the positive differential amplifier current source Q41. Diode CR43 tracks changes in ambient temperature and keeps the operating point of Q28 constant. Since 1.1 volts is developed across R120, the

voltage across R119 is also 1.1 volts setting the current source for 2.15 mA of current total. This current is evenly split between the two halves of Q28 with each half operating at 1.07 mA. Diodes CR33 & CR34 in series with the collector load R75 perform a similar temperature compensation function for the subsequent two following stages Q32 and Q18.

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The overall voltage gain of the first stage is determined by the transconductance of the first stage (0.039mhos), emitter resistors R69 & R70 (R117 & R118) and the collector load(s) R75 (R123). Since the transconductance is a constant, the voltage gain of the first stage is function of the passive components, not the specific semiconductor parameters.

Because the input stage's output is taken single ended, the voltage gain is one half that of the balanced condition because only half of the available output signal is present. For the values given, the first stage gain as measured from the bases of Q28A&B is 8.47 V/V or 18.55 dB. With 1.07 mA of operating current, the voltage drop across the collector load R75 is nominally 2.66 volts. Generous emitter degeneration linearizes the first stage, reduces distortion and increases the high frequency bandwidth of the stage. Under normal 600 W operation (48.99 V rms) the nominal AC signal voltage 272 mV across the collector resistor. Under severe overdrive or under slewing conditions the signal level developed can be as high as 5.2 V pp. The action of the negative half is identical except that the semiconductor and voltage polarities are reversed if measured

with respect to ground. Buffering the first stage collector load(s) from the large non-linear signal dependent collector to base capacitance(s) of the large geometry device Q18 and Q17 that provide the full output signal swing, are emitter followers Q32 and Q37. Emitter resistors R77 & R125 set the operating current to 4 mA per device.

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Passive components R75, R76 and C18 totally control the frequency response of the input stage making its frequency response independent of transistor parameters. A second pole in the openloop frequency response starts at 52 kHz and a zero is introduced at 2.6 MHz. Resistors R38 and R36 provide a positive real part in the bases of Q18 and Q17 and prevents any internal parasitic oscillations in the 10's of Mhz region.

The 2.66 volts dropped across the respective collector loads R75 and R123 also appears across emitter resistors R39 and R37 therefore setting the third stage quiescent operating current to 32.2 mA. The voltage gain of the third stage is limited to a much lower finite value than is typical by the inclusion of collector load resistors R33 and R34. The net overall voltage gain for the third stage is 180 V/V (45.1 dB). The 25 kHz dominate pole in the amplifier's open-loop frequency response is set at this stage by capacitors C6 & C7 breaking against the parallel combination of R33 & R34. There is also two other benefits obtained by locating the dominate pole at the third stage. First is the fact that the frequency compensation network has a symmetrical charge up and discharge path for the

compensation components, and second, the reduction in driving point impedance presented to the output stage offsets the reduction in loop gain at high frequencies keeping the output impedance relatively constant.

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The last stage is a triple Darlington emitter follower comprised of pre-drivers Q15 & Q14, drivers Q16 & Q13, and sixteen 17 amp 230 volt output devices Q9, Q10, Q11, Q12, Q6, Q5, Q4, & Q3 located on the main power amplifier circuit board, and Q1, Q2, Q3, Q4, Q5, Q6, Q7, & Q8 located on the slave circuit board. Overall voltage gain for output stage is -0.5 dB setting the overall open-loop gain of the amplifier to 62 dB.

Closed-loop gain and frequency response is determined by resistors R100, R101, R102, R68. Capacitors C30 and C17 determine the low and high frequency 3 dB points respectively. The closed-loop high frequency -3 dB point is set by R68 and feedback zero capacitor C17, and is 169 kHz. The low frequency -3 dB point is determined by R102 & C30 and is 0.8 Hz. It is germane to note that the power amplifier is configured as a differential input with a voltage gain of 10 (20 dB). By using a differential approach in the input, it is possible to take advantage of the common-mode rejection of the circuit, thereby rejecting the differences in potential between the Input PCB and the power amplifier modules. Operating the amplifier in a differential mode is necessary when dealing with a high frequency switching power supply that generates over 4 mV of HF noise in the internal grounding cables between modules.

Resistor R99 limits the minimum gain of the module when it is energized outside of the chassis. When installed in the chassis, R99 is shorted out by the system grounds.

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The three stage output section has a combined current gain of over 640,000 which reflects the typical 4 ohm load back to the driving point of the third stage as a 2.5 M ohm load in parallel with the already well defined impedance of 7500 ohms. Consequently, any type of load operating within the safe operating area of the amplifier will not modify the transfer characteristics of the circuit. Setting the overall output impedance for the amplifier is the impedance of inductor L1, the contact resistance of relay K1, and the contact resistance of output Faston connectors connected to P1 & P2. If it were not for the mechanical connections, wire resistance, and L1 the damping factor could be 15,000. Inductor L1 is necessary, however inasmuch it serves as a very high impedance at RF frequencies looking back into the amplifier, thus preventing the amplifier from demodulating the signals that travel back to the power amplifier through the speaker lines. This is necessary if long (500+ feet) unshielded speaker lines are run in a high RFI environment.

Bias for the output stage is set by a conjugate feedback pair Vbe multiplier Q8 & Q42. Transistor Q8 is the thermal sensing unit and is attached to the heat sink to track the junction temperatures of output stage. By scaling the resistor values so

that Q8's base current causes insignificant voltage drops in the biasing resistors R15, R16 ,& R17, Q8's Vbe is multiplied by the ratio of the R17 divided by the total resistance is the base-toemitter junctions plus 1. Transistor Q8 operates at about 1 mA of collector causing sufficient drop across its load resistor R130 to turn on Q42 which carries the remaining 30 mA of current flowing from Q18 to Q17. At 25 degrees C the nominal bias voltage developed across the emitter to collector of Q42 is 3.4 volts decreasing at the rate of 0.0145 volts/degree C.

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Diodes CR49, CR50, CR51, CR11, & Q40 control the positive high frequency overload characteristics of the circuit and provide the peak detection function as previously mentioned in the Housekeeping section. In similar fashion CR52, CR53, CR54, CR9 & Q35 perform the same functions for negative going swings. Circuit action will cause an indication at even the slightest amount of peak clipping. Distortion levels of less than 0.01% are easily detected.

By using this method of clamping the maximum peak drive to a value of 1.2 volts above (or below) the  $\pm$ Vcc1 supplies and using higher supply voltages ( $\pm$ Vcc2) for the large signal voltage amplification stage and the pre-drivers and drivers, maximum output stage efficiency is achieved enabling one to obtain more than 20% more output power from the same power supply as opposed to the single supply approach.

The series string of the three diodes CR49, 50, & 51 set the base of pre-driver transistor at a maximum peak voltage of 0.6 volts below the +Vccl power supply. By summing the individual baseemitter drops, it can be determined that the output device emitters can pull up to within 1.8 volts of the power supply voltage. With typical loads, the maximum peak signal swing is 2 volts below the bottom of the ripple, not the average power supply DC voltage.

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Output stage protection is an average sensing type that reacts to instantaneous peaks yet also responds to the longer term average before initiating the limiting/protection function. Circuit action is most easily understood if one begins to investigate the circuit action with a shorted load. When the load is shorted all of the output stage emitter resistors are effectively grounded. Positive and negative current sensing is achieved by monitoring the current in emitter resistors R19 & R12 respectively. As the amplifier tries to develop an output signal the output stage current tries to increase dramatically because the overall load is 0.33 ohms divided by 8. Consequently, there is a rapid increase in voltage across the emitter resistors. R27 & R79 form a 0.828:1.woltage divider across R19. For Q33 the positive protection device to turn on and clamp the driving signal to ground, at least 0.7 volts need to be developed across R79 which translates to 0.844 volts across the 0.33 ohm resistor R19 indicating that a peak current of 2.6 amps per device is flowing.

The 2.6 amps peak is well with in the short term transient SOA of the output devices but outside the continuous ratings as 1600 Watts would be dissipated on the heat sink.. For 8 paralleled devices this translates into over 20 amps of peak load current under short circuit conditions. Protection for the negative side is identical and involves Q38, R127, R28, & R12 except the polarities are reversed. Diodes CR36 & CR46 serve to prevent the collector-to-base junctions of Q33 & Q38 from becoming reverse biased during limiting action with reactive loads.

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To prevent catastrophic failure, yet allow for a large dynamic range of loads, a second time dependent loop is added. Connected across the bases through resistors R105 & R104 of both Q33 & Q38 is an additional transistor Q34. Under short circuit conditions, Q34's base is effectively tied to ground through R12 while R105 begins to supply enough current to turn on Q34. Q34's collector level shifts down to the -Vcc2 supply through collector resistor R106. Capacitor C26 integrates the detected pulses building up sufficient voltage to turn on Q39 and therefore trigger the SOA shutdown one-shot.

For high voltage operation such as with loads of 2 ohms or less, the peak load current is over 40 Amps. Here the opposite occurs as with a short circuit where the voltage across the output devices is at the full +Vccl. Under maximum peak signal swings, the load current is at maximum while the voltage across the output devices is minimum. Reactive load operation falls in between and can, in some cases, be worse. To allow for this mode

of operation, an output load voltage dependent reverse bias is developed across R79 by the addition of R78 & CR35. Using a 4 ohm load for example, the maximum peak signal swing with nominal line voltage is 81 volts corresponding to a peak load current of 20.25 Amps total or 2.53 Amps per device. 2.53 Amps through a 0.33 ohm resistor (R19) develops a 0.835 peak signal that is added to the peak load voltage of 81 volts bringing the voltage at TP#1 to 81.835 volts. Conventional network analysis will show about 1 volt of reverse bias is developed across R79 because current now flows through R78 and diode CR35 that is now forward To overcome the reverse bias produced as a function of biased. output signal swing considerably more than 21 amps must flow through the output stage. In the SR6660A the circuit parameters are adjusted so that the unit will develop 1400 Watts into 2 ohm loads before limiting.

All power supply filtering functions are located on the Slave PCB. Inductor L3 and capacitors C3, C4, and C5 serve to filter out the high frequency ripple generated at the positive power supply +Vcc1 and limit the maximum ripple current to less than 4 mA of high frequency current flowing in the power supply ground returns. Inductor L1 and capacitor C1 serve the same purpose for the stacked supply +Vcc2. Components L3, C6, C7, C8, and L2 and C2 perform the same functions for the negative power supplies.





FILE: 259641.SCH / FLOPPY: YES NO

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1724	SH REV.	1			
	REVISIONS		DATE	APPROVED	
IAL RELEASE	DESCHIPTION		DAIE	AFFRONCO	
UNNECT WIRE BETWEEN S	W1B & (R31/021), ADDED 553	2 AND DIGDE DWGS	11/12/91 12/09/91	NFB	
1→P1 2→P1	CH A INPUT + CH A WIPER -	$\rightarrow$	CHANNE GAIN C	LA	
$ \xrightarrow{3} P1  \xrightarrow{4} P1  \xrightarrow{7} P1 $	CH A GND		CHANNE		
2 > P11 3 > P11 4 > P11	CH B WIPER - Shield Ch B GND	$\rightarrow$	GAIN C	,	
15 ₽2 16→ P2	CH A+ OUTPUT CH A- OUTPUT				
$7 \xrightarrow{12} P2$	FAN SPEED CO	NTROL			
11>P2	CH A PEAK SI				
13)P2	CH A SIGNAL	PRESENT	OUTPUT		
8>P2	FAST OFF / (	UP RELAY	MUTE)		
<del>× 9</del> >₽2	(THERMAL STA	TUST		TO	
X-14>F2	GND	X		CHANNEL	ļ
	SIGNAL LED	3		A	
<u>2</u> >₽2	POWER LED			POWER	
3→P2	STANDBY LED			AMP	
4)P2	(-24dB LED)			l	
5>₽2	(-6dB LED)				
6→P2	PEAK LED				
7>P2	-15VDC				
<del>×_10</del> →P2	(STANDBY ST	ATUS uP)			
		_			
15 P3	<u>CH B+ OUTPU</u>				
	CH B- OUTPU				
<u>12</u> →P3	FAN SPEED C				
11>P3	CH B PEAK S	IGNAL			
<u>13</u> >P3	CH B SIGNAL	PHESENI	UUIPUI		
8→P3	FAST OFF /		Y MUIE/		
× 9>P3	(THERMAL ST	ATUSI		TO	
<del>X 143</del> 73	GND			CHANNEL	
	SIGNAL LED			B	Ì
2→P3	POWER LED	)		POWER	
3→P3 4→P3	(-24dB LED)			AMP	1
¥>₽3 \$>₽3	(-2406 LED)				
ŶP3 ŝ>₽3	PEAK LED				Į
Z → P3	-15VDC				
→P3 ×-10→P3	(STANDBY S	TATUS)			
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# DEC 2 0 1991

# H.E. DOC. CONTROL

APPROVAL	DATE	harman electronics					
C. O'BRIEN	12/9/91	A Harman International Company Northridge, California 91329, U.S.A.					
CHECKED		TITLE	INPUT	SR6660	) A (		
WANUFACTURING							
PRODUCT ASSURANCE		SI7E	DRAWING NO.	61724	AEV 2		
PRODUCT ACCOUNTER			201/24				
ENGINEERING		SCALE	NONE	SHEET 1	0F 1		
$\bigcirc$		FILE: 2617	14.SCH	FLOPPY: YES	N0 □		






		261647				
THESE DRIWINGS AND SPECIFICATIONS ARE THE PROPERTY OF HARMAN FLECTRONICS. THEY ARE			REVISIO	NS .		
THESE DR/WINGS AND SPECIFICATIONS ARE THE PROPERTY OF HARMAN FLECTRONICS. THEY ARE ISSUED IN STRICT CONFIDENCE AND SHALL NOT BE REPRODUCED, COPIED, ON USED AS THE BASIS FOR MANUFACTURE OF APPARATUS WITHOUT WRITTEN PERMISSION.	ECO		DESCRIPTI	ON	DATE	APPHOVED
WITHOUT WRITTEN PERMISSION.		1 3/1-	TIAL RELEASE		(0+24-31	MB
+VCC2		L1 620H				
		VEUI				
$ \xrightarrow{J_{1}} \overset{J_{1}}{\xrightarrow{J_{2}}} \xrightarrow{J_{1}} \overset{J_{1}}{\xrightarrow{J_{1}}} \xrightarrow{J_{1}} \overset{J_{1}}{\xrightarrow{J_{1}}} \xrightarrow{J_{1}} \overset{J_{1}}{\xrightarrow{J_{1}}} \xrightarrow{J_{1}} \overset{J_{1}}{\xrightarrow{J_{1}}} \xrightarrow{J_{1}} \overset{J_{1}}{\xrightarrow{J_{1}}} \xrightarrow{J_{1}} \overset{J_{1}}{\xrightarrow{J_{1}}} \overset{J_{1}}} \overset{J_{1}}{J_$	•	L3 	P1 P1 3			
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$\xrightarrow{)}^{j'}$			$\begin{array}{c} P_1 \\ P_1 \\ P_1 \\ \hline \\ $			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	+1 C8 7 2700uF 1094					
$\rightarrow$ $\stackrel{J_1}{\rightarrow}$ $\stackrel{J_2}{\rightarrow}$ $\stackrel{J_1}{\rightarrow}$ $\stackrel{J_2}{\rightarrow}$ $\stackrel{J_1}{\rightarrow}$ $\stackrel{J_2}{\rightarrow}$ $\stackrel{J_3}{\rightarrow}$		L4 SSUH	$\xrightarrow{\begin{array}{c} P_1 \\ P_1 \\ P_1 \\ g \end{array}}$			
+ C2 - VCC2 J1		L2	P1 10→		RECEIVED	
		62uH				
<ul> <li>6. FOR DC &amp; AC VOLTAGES, REFER TO POWER AMPLIFIER SCHEMATIC DRAWING #261693.</li> <li>5. FOR TEST SPECIFICATIONS REFER TO DRAWING #262376. LAST Q : Q8</li> </ul>					DCT 2 5 1991 DOC. CONTR	₹OL
LAST J : U LAST P : P2 LAST L : L4 LAST C : C8	UNLESS OTHERW DIMENSIONS ARI TOLERANCES ARI FRACTIONS D	ECTHALS ANGLES	APPROVAL DATE	A Harman International /51 Northridge, California	Company	
LAST R : R16 4. FOR PCB ASSEMBLY DRAWING, REFER TO DRAWING #261625. 3. F DENOTES FUSE RESISTOR.	WATERTAL	<u>xx ± x = "</u>	CHECKED MANUFACTURING	SLAVE	SCHEMAT	IC
2. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE 1/4W, 5% FUSE RESISTORS (F).	۱ 	۸A	PRODUCT ASSURANCE	SIZE DRAWING NO.	261647	REV 1
1. FOR RELATED DOCUMENT, SEE POWER AMPLIFIER SCHEMATIC 261693. GENERAL NOTES: NEXT ASSY USED ON	FINISH		ENGINEERING	SCALE NONE		1 OF 1
	1			ETLE: 261647.SCH		

FILE: 261647.SCH







21	JUN	1995
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## Single level Bill of Material Procedure: PDC-R-07

BOM Num	ber : 277494-001 - ;	AMP, SR6670A	,115v		Phantoms Exp Revision: 5	loded
Item# X	Part Number Description	Quantity.	Al	t-Part# .Oper#.		Designat
001	262554 DWG,ASY,FINAL,SR6	DWG	L	10		
002	263175 BLOCK-DIAG, INR-COM	DWG NN,SR667 A	L	10		
020	24-16443 BTN, PWR, SR	1.0000 A	L	95	м. -	
025	24-16500 KNOB, INP, CTRL, SR, H	2.0000 MP B	L	95		
030	25-16959 BRKT, REAR-RACK, MN1	2.0000 SG, SR-A 3	L	95		
040	257488 CHAS	1.0000 3	L	95		
045	257675 Baffle	2.0000	L	95		
050	257959 SCR,EYE,W210-1/2	2.0000 1	L	95		
055	258349 Shld, PS, SR6670A	1.0000	L	ِ 95		
060	28-0102 WSHR,#10,FLT,THK	4.0000	L	95		
062	28-0062 WSHR,#8,FLT	2.0000	: L	95		
D65	30-0057 SCR,6-32X3/8,PPH	3.0000	ŕ	95	н 1. 1.	
070	30-0215 SCR,8X3/8",SHWH,B,	4.0000	•	95		
)75	30-0307 SCR,8-32X1/2,SEMS	2.0000	L	95		
)76	29-0051 NUT,6,HEX	1.0000	L	95		
)77	28-0097 WSHR, <b>#6,STAR,L</b> K	1.0000	L	95		-
)78	256207 TIE-WRAP,4",BLK	· 17.0000 1	т.	95		•

21 JUN 1995

BOM Number : 277494-001 - AMP, SR6670A, 115V

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Single level Bill of Material Procedure: PDC-R-07 Phantoms Exploded Revision: 5

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•	Item <b>#</b> X	Part NumberQu Description	antity.	Al Inv	t-Part#. .Oper#.	Reference Designator.
	079	36-0181 FSTNR, MNTG, 4WAY, ADH	5.0000	AL	95	
	080	97-17015 LBL, FUSE, WARN	1.0000	<b>A L</b> (	95	
	081	30-0331 SCR,RLK,6-32X3/8",PF	2.0000 PH,BZ 1	) 3 L	95	
	083	278903-001 CLMP, CABL, FLT, NYL, SF	10.0000 CC-4 1	A L	95	
	085	97-17016 LBL, SER#	1.0000	السيلية	95	
	090	VP59010 LBL, CAUT, INFINITY	1.0000	CL	95	
	095	36-0529 POST,SPRT,1/8",HT	4.0000 E	3 L	95	
	100	30-0333 SCR,10-32X1/2,PPH,ZN	14.0000 E	3 L	95	
	105 P	261416 ASY, PCBA, DSPL, SR6670	1.0000 A 5	i L	95	
	005	261427 DWG,PCBA,DSPL,SR6670	DWG A *	L	10	
	010	262292 PROC, TEST, LED, SR6670	DWG A *	L	10	
	015	261614 SCHEM, DSPL, SR6670A	DWG A	L	10	· ·
	020	262281 SPEC, TEST, LED, SR6670	DWG A *	L.	10	
	025	13-0587 Led, grn, sub-Mini	3.0000 B	Ĺ	95	CR1,3,5
	030	13-0586 Led, red, sub-mini	4.0000 B	L	95	CR2,4,6,7
	035	262653 CONN, HDR, 16PIN, 90DEG	1.0000 ,.1"S 1	L	95	P1 💕
	040	261405 PNL,PCB,DSPL,SR6670A	0.1250 2	L	95	
	21 JUN 1 BOM Numb	995 er : 277494-001 - Амр	, SR6670A	,115V	. **	Single level Bill of Material Procedure: PDC-R-07 Phantoms Exploded Revision: 5
	Item# X	Part NumberQua Description	antity. Rev	Alt Inv	-Part#. .Oper#.	••••••Reference Designator.
	045	50788 SLDR,BAR	0.0100	L	95	•

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	010	276171-001 COVR, CHAS, SR6670A	1.0000 1	L	95
	015	257026 Lens, Led, es/sr	2.0000 1	L	95
l < >	025	30-0333 SCR,10-32X1/2,PPH,ZN	4.0000 B	L	95
	030	265678 TAPE,XFMR,1",3M,ADH	0.0100 A	L	95

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· ,	035	30-0126 6.0000 SCR,6-32X1/2,PFH,RLK,BO A L 95
	040	27-0609 1.0000 J1,2 ASY,CABL,A-SPK,HI/LO 2 L 95
	045	27-0611 1.0000 J3,4 ASY,CABL,B-SPK,HI/LO 3 L 95
	065	257193 1.0000 ASY,CABL,CHAS-GND/LINE-FL 2 L 95
	070	260828 1.0000 ASY,CABL,INP,PWR-SPLY,SR/ 4 L 95
	075 I	262717-001 1.0000 ASY,PWR-CORD,SR6670A 1 L 95
	001	262717 DWG ASY,PWR-CORD,SR6670A 4 L 10
	005	262235 1.0000 TERM,RING,#10,INTL-T A L 95
	010	36-0406 2.0000 FASTON,16-14GA,FEM,.250 * L 95
	015	36-0546 1.0000 CORD,PWR,14/3,SJT,5.5' C L 10
	080	27-0604 1.0000 ASY,CABL,INP-DSPL,ES/SR 2 L 95
	085	27-0605 2.0000 ASY,CABL,INP-AMP/CH-A 1 L 95
)	21 JUN	Procedure: PDC-R-07 Phantoms Fraleded
	BOM Num	ber : 277494-001 - AMP, SR6670A, 115V Revision: 5
	Item <b>#</b> X	Part NumberQuantityAlt-Part#Reference Designator. DescriptionRev Inv .Oper#.
	090 P	261735 1.0000 ASY,PCBA,INP,SR6670A 3 L 95
	001	261746 DWG DWG,PCBA,INP,SR6670A 2 L 10
	005	261724 DWG SCHEM, INP, SR6670A AL 10
	010	262279 DWG PROC,TEST,INP,SR6670A * L 10
	015	262257 DWG SPEC,TEST,INP,SR6670A * L 10
	025	27-0342 2.0000 J1,3 CONN,FEM,PC,XLR BL 95
	030	27-0343 2.0000 J2,4 CONN,PHONE,PC,MNT L 95

1							
Ì		015	256352 SCR,10-32X3/4,TRX,C/Z	1.0000	L	95	
		020	256405 5 WSHR, <b>#</b> 10,LK,EXTL	5.0000	L	95	
	).	025	257532 3 SCR,6-32X1/2PPH,ROLOK,	3.0000 ,c/z a	L	95	
		030	29-0066 3 NUT,10-32,HEX	3.0000	L	95	
ļ		035	30-0057 8 SCR,6-32X3/8,PPH	3.0000	L	95	
		040	36-0333 1 STRN-RLF,CORD,AC HEYCO	L.0000 D SR	L	95	
		045 P	276114-001 2 ASY,FAN,SR6670A	2.0000 3	L	95	
and the second second		001	276114 DWG,ASY,FAN,SR6670A	DWG 2	L	10	
		011	27-0571 2 CONN, ID, SKT, 2POS, .098"	.0000 A	L	95	
		012	307268-001 2 FAN, 24VDC, 4200RPM, 40CF	.0000 M,8 %	L	् 95 ँ <b>(</b>	
		050	31-0066 4 RVT,POP,.125X.441 AD43	-0000 -45 A	L	95	XLR MNTG
		055 P	261526 1 ASY, PCBA, SPKN, ES1200A/	.0000 SR6 4	L	95	
	)	001	261515 DWG, PCBA, SPKN, ES1200A/	DWG SR6 3	L	10	
		002	261495 SCHEM, SPKN, ES1200A/SR6	DWG 670 1	L	10	
		21 JUN :	1995			Si	ngle level Bill of Material
Ì		BOM Num	per : 277494-001 - AMP,SI	R6670A,	115V		Procedure: PDC-R-07 Phantoms Exploded Revision: 5
		Item <b>#</b> X	Part Number Quant Description	tity. Rev	Alt Inv	-Part# .Oper#.	Reference Designator.
		003	262367 SPEC, TEST, SPKN, ES1200A,	DWG /SR *	L	10	
		004	262378 PROC, TEST, SPKN, ES1200A/	DWG /sr *:	L	10	
		011	25-17045 1. PL,MNTG,SPEAKON	.0000 12	L	95	
		012	261504 0. PNL,SPKN,ES1200A/SR6670	.2500 DA 21	L	95	
		030	27-0646 3. CONN, SPEAKON, F, PCB	.0000 c 1	L	95	J5,6,7
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	002	261647				
	002	261647 SCHEM, SLV-AMP, ES/SR	DWG	A L	10	
	052	50404 RTV,SIL,RBR	1.0000 1	BL	95	
)	500	14-0858 CAP-EL,2700UF,20%,10	12.0000 0V F	ЗL	95	C3,4,5,6,7,8
	503	27-0531 HDR,10POS,.156",.045	2.0000 ",SQ #	A L	95	P1
	506	13-0595 XSTR,2SC4029,NPN	8.0000 E	3 L	95	Q1,2,3,4
	509	13-0596 XSTR,2SA1553,PNP	8.0000 E	BL	95	Q5,6,7,8
	512	X 280636-001 ASY,AXL,SLV-AMP,ES/S	2.0000 R 1	L	95	
	515	P 280647-001 ASY,CS400,SLV-AMP,ES	2.0000 /SR 1	L	95	
	500	14-0726 CAP-EL,470UF,20%,25V	4.0000 ,RD D	L	95	C1,2
	503	17-0027 INDUC,62UH,2.5A	4.0000 B	L	95	L1,2
	506	17-0037 CHOKE, PWR, LINE, 56UH	4.0000 B	L	95	L3,4
	509	27-0218 TERM, SPADE, .250, PCMN	2.0000 Г А	L	95	P2
	512	187-00051-00 ; RES,.33-0HM,5W	16.0000	L	95	R2,5,7,8,11,12,15,16
	070	50788 SLDR,BAR	0.0200	L	95	
	080	284546-001 SLDR,WR,.040,285,RMA,	0.0200 FLUX в	L	95	
	125	P 258087 ASY, PNL, REAR, SR6670A	1.0000	L	95	
	21 JUN	1995				Single level Bill of Material
	BOM Nur	nber : 277494-001 - AMP,	SR6670A,	115	•	Procedure: PDC-R-07 Phantoms Exploded Revision: 5
	Item <b>#</b> ]	Part NumberQua Description	ntity. Rev	A Inv	lt-Part#. .Oper#.	••••••Reference Designator.
	001	262629 DWG,ASY,PNL,REAR,SR66	DWG 70a 3	L	10	
	011	25-16970 PNL, REAR, SR6670A	1.0000 14	L	95	
	012	256341 LFANGUARDABOMM	2.0000	L	95	

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	035	27-0672 CONN, RCPT, 10P, .1"BOT	1.0000 ,E 2	A L	95	J5
•	040	17-0049 COIL,330UH	3.0000 1	A L	95	L1,2,3
	045	27-0565 HDR,4POS,.098"SP	2.0000	A L	95	P1,11
'	050	27-0650 HDR,90D,16POS,.1"CTR	3.0000 ,SHRD #	A L	95	P2,3,4
	055	27-0649 HDR,90D,14POS,.1"CTR	1.0000 ,SHRD #	A L	95	P5
	060	27-0676 SHNT/JMPR,.1"CTR	2.0000 F	L	95	P9,10
	065	27-0677 HDR,STR,3PIN,.1"SP	2.0000 P	L	95	P9,10
	070	52926-001 Pot, TRIM, 10K, 30%, VTM	2.0000 T A	L	95	R7,24
	075	15-16416 SW,SLIDE,3P3T,PCMT	2.0000 A	L	95	SW1,2
	080	13-0276 IC,NE5532AF	4.0000 A	L	95	V1,2,3,5
	21 JUN BOM Numi	1995 ber : 277494-001 - Амр,	, SR6670A	,115v	Si	ngle level Bill of Material Procedure: PDC-R-07 Phantoms Exploded Revision: 5
( )	Item <b>#</b> X	Part NumberQua Description	antity. Rev	Al	t-Part# .Oper#.	Reference Designator.
	085 X	258131 ASY,RAD,INP,SR6670A	1.0000 6	L	95	
	090	27-0656 ASY,CABL,LG-GND,ESA/S	2.0000 SRA 3	L	95	
	095	27-0657 Asy,CABL,SHT-GND,ESA/	1.0000 /sra 4	L	95	
	095 X	260817-001 ASY,CABL,4COND,INP,PC	1.0000 DT 4	L	95	
	100	50788 SLDR, BAR	0.0100	L	95	
	105	284546-001 SLDR,WR,.040,285,RMA,	0.0100 FLUX B	L	95	
	130 P	262642 Asy, covr, sr6670A	1.0000	L	95	
	001	262607 DWG, ASY, COVR, SR6670A	DWG 2	L	10	
	005	25-16578-002 CAST,2U,HDL,SILVER,ME	2.0000 TALL B	L	95	

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 Item#	X	Part NumberQ Description	uantity.	≥v	Alt Inv	t-Part# .Oper#.	Reference Designator.
512		13-0595 XSTR, 2SC4029, NPN	10-0000	) B	L .	95	<b>Q9,10,11,12,16</b> M/06
518		13-0735 XSTR,2SA1006B,PNP,2	4.0000 50V	) A	L	95	Q14,18 - NO.C.
521		13-0677 XSTR,2SC2336B,NPN,2	4.0000 50V	) A	L	95	Q15,17 - NOC
527		N32-48679 WR,22G,BLK,1007,SOL	4.0000	)	L	95	W1,2,3,4,5,6,8
535	X	258107 ASY,RAD,PWR-AMP,ES/	2.0000 SR 1	) .0	L	95	
538	P	280669-001 ASY,CS400,PWR-AMP,S	2.0000 R6670A		L	95	
500		257642 CAP-MP,.1UF,10%,250	4.0000 V	1	L	95	C22,23
503		14-0857 CAP-FPP,.033UF,10%,	2.0000 200V,R		L	95	C27
506		13-0719 RECT, 3A, 200V, 1N5402	4.0000	A	L	95	CR5,8
509		187-00051-00 RES,.33-OHM,5W	16.0000		L	95	R6,8,10,12,19,21,23 25
512		187-01801-02 RES,1.8K,5%,3W	2.0000	8	L	95	R40
515		187-00062-00 RES,MP,.47,10%,5W,R	16.0000 D	A	L	95	R41,42,43,44,45,46 47,48
518		255718 RES-MO,10-онм,5%,3W	8.0000	1	L	95	R81,82,83,84
521		13-0304 IC,TL072CP,OP-AMP,D0	2.0000 JAL	A	L	95	Ul
524		HM13-0238 IC,LM339N,LIN	4.0000		L	95	U2,3
541		285332-001 ADH,CLR,CYANOACRYLA	0.0200 TE,501		L	95	
065	P	261636 ASY,PCBA,SLV-AMP,ES,	2.0000 /SR	3	L	95	
21 JUN						Sin	gle level Bill of Material Procedure: PDC-R-07 Phantoms Exploded
		er : 277494-001 - AME					Revision: 5
item <b>#</b> :	X (	Part Number Qu Description	antity.	7	Alt Inv	-Part# .Oper#.	Reference Designator.
001	:	261625	DWG				

261625 DWG DWG,PCBA,SLV-AMP,ES/SR 2 L

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21 JUN 1995	Single level Bill of Material Procedure: PDC-R-07
BOM Number : 277494-001 - AMP, SR6670A, 115V	Phantoms Exploded Revision: 5
Item# X Part Number QuantityAlt-Part# DescriptionRev Inv .Oper#	<pre>#Reference Designator. #.</pre>
500 15-0410 2.0000 COVR,RLY,T90N BL 95	PART OF K1
503 15-0501 2.0000 RLY,SPDT,48V,30A AL 95	K1
506 36-0403 2.0000 MGNT,CER,BASE L 95	PART OF K1
509 X 16-14573 2.0000 COIL,AIR,CORE,2.2UH 2 L 95	Ll
512 27-0218 2.0000 TERM, SPADE, . 250, PCMNT A L 95	P2
515 27-0641 2.0000 TER,TAB,MALE,.187" A L 95	P1
518 27-0636 2.0000 HDR,STR,16POS,.1"CTR AL 95	P3
520 13-0679 2.0000 XSTR,2SC3381,NPN,80V,DUAL A L 95	Q28 H30 )
523 13-0678 2.0000 XSTR,2SA1349,PNP,80V,DUAL A L 95	Q29 H36 1
526 15-0496 2.0000 POT,TRIM,500,M,HZMT,CRMT A L 95	R15
529 15-0493 2.0000 POT,TRIM,10K,M,HZMT,CRMT A L 95	R52
531 280352-001 12.0000 TERM, TEST-PT, PCMT % L 95	TP1,2,3,4,5,6
532 P 258098 2.0000 KIT,PREP,PWR-AMP,ES/SR 6 L 95	
500 13-0289 2.0000 XSTR,MJE350 A L 95	Ql
503 13-0288 4.0000 XSTR,MJE340 A L 95	Q2,8
506 <b>13-0596</b> XSTR,2SA1553,PNP B L	<b>23:4,5,6,13</b> € 509
509 13-0676 2.0000 XSTR,2SA1360,PNP,150V B L 95	Q7 .
21 JUN 1995	Single level Bill of Material
BOM Number : $277494-001 - MP SP66702 1157$	Procedure: PDC-R-07 Phantoms Exploded

BOM Number : 277494-001 - AMP, SR6670A, 115V

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Revision: 5

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	120 1	258076 2.0000 ASY,AMP,MODUL,ES/SR 9 L	95
	001	262774 DWG DWG,ASY,AMP,MODUL,ES/SR 2	10
)	21 JUN	1995	Single level Bill of Material Procedure: PDC-R-07
	BOM Nun	aber : 277494-001 - AMP,SR6670A,115V	Phantoms Exploded Revision: 5
	Item# X	Part Number QuantityAlt DescriptionRev Inv	t-Part#Reference Designator. .Oper#.
	005	25-17047 2.0000 HTSK,MAIN,MOD,ES/SR,1200 14 L	95
	010	256253 4.0000 STNDF,6/32X3/8,RND,PHEN 1 L	95
	015	256264 8.0000 STNDF,6/32X1-3/8,HEX,ALUM 1 L	95
	025	257508 2.0000 ASY,CABL,14-CONDUCTOR,AMP 3 L	95
	030	263734 52.0000 SCR,4-40X1/2,HXSKTHD A L	95
	035	260084 2.0000 INSLR,PWR-AMP,SR6670A 2 L	95
	040	260095 2.0000 INSLR,SLAVE-AMP,SR6670A 2 L	95
)	045	51100 52.0000 WSHR,4,FLT,.250,OD 1 L	95
	050	51145 8.0000 SPCR,SHLDR,JBL2R B L	95
	055	27-0614 2.0000 ASY,CABL,AMP-PWR,CH-A&CH- 3 L	95
	060 P	261702 2.0000 ASY,PCBA,PWR-AMP,SR6670A 9 L	95
	001	261713 DWG DWG,PCBA,PWR-AMP,SR6670A 2 L	10
	002	261693 DWG SCHEM,AMP-PWR,SR6670A B L	10
	003	262411 DWG PROC,TEST,PWR-AMP,ES1200A * L	10
	004	262409 DWG SPEC,TEST,PWR-AMP,ES1200A * L	10
	115	258351 0.0200 ADH,GEL,LOCTITE,454 A L	95
	120	258362 0.0200 ACLTR,TAK,PAK,LOCTITE,710 * L	95

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	135	267237-001 LBL,FUSE,SR6670A	1.0000	2 L	95		
	140	50403 Compound, Thermal	0.4320	A L	95		
	145	50361 Kapton, Tape	1.0000	L	95		
	150	50788 SLDR, BAR	0.0100	L	95		
	21 JUN	1995				Single level Bill of Material Procedure: PDC-R-07	
	BOM Num	ber : 277494-001 - AMP	, SR6670A	,115v		Phantoms Exploded Revision: 5	
	Item <b>#</b> X	Part NumberQu Description	antity.	Al Inv	lt-Part# .Oper#	••• ••••Reference Designator.	
	155	284546-001 SLDR,WR,.040,285,RMA	0.0100 .,FLUX B	L	95		
	115 P	10-16922 KIT,SHIP,SR	1.0000 6	L	95		
	005	06-0001 MNL, SR6670A	1.0000	L	95		
	010	25–14284 LBL,WARN,ELEC-SHOCK	1.0000 D	L	95		
	015	256374 CTN, SR6670A	1.0000	L	95		
)	025	27–0589 Conn, Speakon, M, Cabl	2.0000 B	L	95		
	030	97-59660 Card, warr	1.0000	L	95		
	035 P	10–16524 KIT,RACK,SCR-SR	1.0000	L	95		
	010	30-0320 SCR,10-32X3/4,PBH,SS	4.0000 B	L	95		
	020	28-0107 WSHR,#10,FLT,FBR	4.0000 B	L	95		
	030	36-0306 COIN, ENVELOPE	1.0000	L	95		
	040	33-0147 BAG,POLY,12"X16"	1.0000 A	L	95		
	045	99-0164 CAP,PROTECT,CORD,PWR,	1.0000 BLU	L	95		
	050	281763-001 PKG, INSR, TRAY, FOAM, SR	1.0000 6670 1	L	95		
	055	281774-001 PKG,CAP,END,SR6670A	2.0000	L	95		

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•	515	274051-001 Fuse,sb,2.5A,250V,2A	2.0000 G,PGT		95	F2,3
	518	274258-001 CORE,BEAD,AB4X2X6,SU	2.0000 PPR	AL	95	FB3,4
)	521	255478 XSTR,N-FET,MTP5N20	1.0000	A L	95	Q6
	524	13-0671 XSTR,MTP3055E,FET	3.0000	A L	95	Q7,13,15
	527	13-0672 XSTR,MTP2955,FET	2.0000	AL	95	Q12,14
	533	255533 RES-MO,27K,5%,2W	1.0000	* L	95	R3
	21 JUN	-				Single level Bill of Material Procedure: PDC-R-07 Phantoms Exploded
	BOM Num	ber : 277494-001 - AMP	,SR6670	A,115V		Revision: 5
	Item <b>#</b> X	Part NumberQu Description	antity. Re	Al v Inv	t-Part#. .Oper#.	Reference Designator.
	536	255509 RES-MO,24K,5%,2W	1.0000	1 L	95	R4
	539	182-25100-00 RES-CF,5.1-OHM,5%,1/2	1.0000 2W 2	A L	95	R32
	542	182-11500-00 RES-CF,15-OHM,5%,1/21	4.0000 ₩ 5	έL	95	R33,34,35,36
)	545	182-03302-00 RES-CF,33K,5%,1/2W	2.0000	L	95	R38,39
	548	50621 IC,SG3525A	1.0000	LL .	95	Ul
	551	262061 IC,LM74C14N,HEX,INV	1.0000	2 L	95	U2
	554	255368 OPTOISOLATOR, MOC3063	1.0000 /	A L	95	<b>U</b> 3
	557	262706 OPTOISOLATOR, H11A1T, S	1.0000 SR667 1	LL	95	<b>U4</b>
	560	13-0194 IC,7815,RGLTR,TO-220	1.0000 E	3 L	95	υ5
	563	13-0195 IC,7915,RGLTR,TO-220	1.0000	L	95	<b>U6</b>
	566	13-0284 IC,7805CT,TO-220,V-RE	1.0000 EG E	L	95	<b>U7</b>
	125	274731-001 INSLR,TO220,ALUM-OX,.	1.0000 .062" A	L	95	
	130	257838 SLVG,GLAS,3/8,CLASS-C	0.5000 2 A	L	95	

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602       P 274828-001       1.0000         KIT, PREP, PWR-SPLY, MTRBRD,       7 L       95         028       258338       2.0000         HTSK, TO-220, SR6670A       2 L       95         030       31-0067       1.0000		
HTSK, TO-220, SR6670A 2 L 95		
) 030 31-0067 1.0000 RVT,POP,.125X.345 RADS 41 L 95		
032 50403 0.0480 COMPOUND, THERMAL A L 95		
034 32-0418 0.6500 TBG,PVC,22GA,105C ALPHA P B L 95		
036 268221-001 1.0000 SHRK-TBG,1.5"DIAX2"LG,BLK B L 95		
038 N32-58870 0.1250 WR,16GA,SOLID L 95		
040 32-0228 0.2000 SHRK, TUBG, BLK, FP301X, 3/16 L 95		
Pro	evel Bill of Material cedure: PDC-R-07 ntoms Exploded	
BOM Number : 277494-001 - AMP, SR6670A, 115V Re	Revision: 5	
Item# X Part Number QuantityAlt-Part# DescriptionRev Inv .Oper#.	Reference Designator.	
042 99-0183 0.2500 WR,BUSS,22G,SOLID 1 L 95		
500         17-0031         2.0000         L1,2           )         COIL,TOR,80UH,10A         B L         95		
503 187-00052-00 1.0000 R2 RES,10-OHM,10%,12W L 95		
509 17-0032 1.0000 T2 INDUC, CRRNT, SNSG, 200CT BL 95		
605 X 274839-001 1.0000 ASY,RAD,PWR-SPLY,MTRBRD,S 6 L 95		
608 P 280658-001 1.0000 ASY,CS400,PWR-SPLY,MTHRBR 2 L 95		
500         14-0763         4.0000         C1,2,           CAP-CD,.01UF,AC,LINE         L         95	3,4	
503 271112-001 1.0000 C11 CAP-MPP,1UF,10%,400V,AX B L 95		
506         14-0868         1.0000         C30           CAP-CD,.1UF,500V         A L         95		

	503	271585-001 RECT, BRDG, 30A, 400V, 3			95	BR2
	506	271574-001 RECT, BRDG, 30A, 400V, 1	1.0000 NCT,50		95	BR3
)	512	14–0796 CAP–EL,2200UF,20%,20	6.0000 00V		95	C5,6,7,8,9,10
	515	14-0858 CAP-EL,2700UF,20%,10	2.0000 00V	BL	95	C27,28
	524	15–0484 Fuse,FB,30A,125V,3A	1.0000 B	A L	95	Fl
	530	274258-001 Core, BEAD, AB4X2X6, St			95	FB1,2
	533	36-0540 CLIP,FUSE,1/4",PCMT,	2.0000 /EAR	8 L	95	J2,3
	536	27-0218 TERM, SPADE, . 250, PCM	2.0000 VT 2	A L	95	P1,2
	539	27-0531 HDR,10POS,.156",.045	2.0000 5",SQ 1		95	P3,4
	542	27-0635 HDR,STR,14POS,.1"CTF	1.0000	A L	95	P5
	21 JUN	1995				
		ber : 277494-001 - AMF	<b>, s</b> R66702	A,115V		ngle level Bill of Material Procedure: PDC-R-07 Phantoms Exploded Revision: 5
)	BOM Num	ber : 277494-001 - Amf	antity.	Al	t-Part <b>#.</b>	Procedure: PDC-R-07 Phantoms Exploded
)	BOM Num	ber : 277494-001 - AMF Part NumberQu	antity. Rev 2.0000	Al v Inv	t-Part <b>#.</b>	Procedure: PDC-R-07 Phantoms Exploded Revision: 5
)	BOM Num Item <b>#</b> X	ber : 277494-001 - AMF Part NumberQu Description 27-0570	antity. Rev 2.0000 7 1.0000	Al v Inv	t-Part# .Oper#.	Procedure: PDC-R-07 Phantoms Exploded Revision: 5 Reference Designator.
)	BOM Num Item <b>#</b> X 545	ber : 277494-001 - AMF Part Number Qu Description 27-0570 HDR,2POS,.098"SP 13-0725	antity. 2.0000 7 1.0000 7 4.0000	Al 7 Inv A L A L	t-Part# .Oper#. 95	Procedure: PDC-R-07 Phantoms Exploded Revision: 5 Reference Designator. P6,7
)	BOM Num Item <b>#</b> X 545 548	<pre>ber : 277494-001 - AMF Part NumberQu Description 27-0570 HDR,2POS,.098"SP 13-0725 TRIAC,40A,400V 13-0597</pre>	antity. 2.0000 1.0000 4.0000 FP360 E 1.0000	Al 7 Inv A L A L	t-Part# .Oper#. 95 95	Procedure: PDC-R-07 Phantoms Exploded Revision: 5 Reference Designator. P6,7 Q1
)	BOM Num Item <b>#</b> X 545 548 551	<pre>ber : 277494-001 - AMF Part Number Qu Description 27-0570 HDR,2POS,.098"SP 13-0725 TRIAC,40A,400V 13-0597 FET,N-CH,23A,400V,IR 255401</pre>	antity. 2.0000 1.0000 FP360 E 1.0000 A 1.0000	Al 7 Inv 1 L 1 L 3 L	t-Part# .Oper#. 95 95 95	Procedure: PDC-R-07 Phantoms Exploded Revision: 5 Reference Designator. P6,7 Q1 Q2,3,4,5
)	BOM Num Item <b>#</b> X 545 548 551 563	<pre>ber : 277494-001 - AMF Part NumberQu Description 27-0570 HDR,2POS,.098"SP 13-0725 TRIAC,40A,400V 13-0597 FET,N-CH,23A,400V,IR 255401 XSTR,PNP,TIP115 15-0496</pre>	antity. 2.0000 1.0000 FP360 E 1.0000 CRMT A 1.0000	Inv L L L L	t-Part# .Oper#. 95 95 95 95	Procedure: PDC-R-07 Phantoms Exploded Revision: 5 Reference Designator. P6,7 Q1 Q2,3,4,5 Q17 y/o/C.
)	BOM Num Item# X 545 548 551 563 566	<pre>ber : 277494-001 - AMF Part Number Qu Description 27-0570 HDR,2POS,.098"SP 13-0725 TRIAC,40A,400V 13-0597 FET,N-CH,23A,400V,IR 255401 XSTR,PNP,TIP115 15-0496 POT,TRIM,500,M,HZMT, 255434</pre>	antity. 2.0000 1.0000 FP360 E 1.0000 CRMT A 1.0000 A 1.0000 A	Inv L L L L	<pre>t-Part# Oper#. 95 95 95 95 95</pre>	Procedure: PDC-R-07 Phantoms Exploded Revision: 5 Reference Designator. P6,7 Q1 Q2,3,4,5 Q17 y/o/c. R27
)	BOM Num Item# X 545 548 551 563 566 569	<pre>ber : 277494-001 - AMF Part Number Qu Description 27-0570 HDR,2POS,.098"SP 13-0725 TRIAC,40A,400V 13-0597 FET,N-CH,23A,400V,IR 255401 XSTR,PNP,TIP115 15-0496 POT,TRIM,500,M,HZMT, 255434 POT,TRIM,5K,20%</pre>	antity. 2.0000 1.0000 FP360 1.0000 CRMT 1.0000 CRMT 1.0000 R 1.0000 B 1.0000	Inv L L L L L	t-Part <b>#</b> 95 95 95 95 95 95 95	Procedure: PDC-R-07 Phantoms Exploded Revision: 5 Reference Designator. P6,7 Q1 Q2,3,4,5 Q17 y/o/c. R27 R29

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	<b>011</b>	P 270185-001 ASY, PCBA, FAN-CTRL	1.0000 8 L	95	
	001	270185 DWG,PCBA,DTRBD	DWG 3 L	10	
)	002	274806 SCHEM, PWR-SPLY, DGHTR	DWG	10	
	500	260643 HDR,90-DEG,12POS,.10	1.0000	95	P1
	503	27-0570 HDR,2POS,.098"SP	2.0000 A L	95	P2,3
	506	X 280603-001 ASY, RAD, FAN-CTRL, SR6	1.0000	95	
	509	X 280614-001 ASY,AXL,FAN-CTRL,SR6	1.0000	95	
	512	P 280625-001 Asy, IC, FAN-CTRL, SR66	1.0000 70a 1 L	95	
	012	270205-001 PNL, PCB, FAN-CTRL	0.1660 2 L	95	
	500	13-0534 IC,LM393	1.0000 A L	95	Ul
	503	274368-001 IC,TL072C,OPAMP,TI/S	1.0000 r A L	95	<b>U</b> 2
	014	256275 WSHR,6,3/8X.031,FLT,F	3.0000 FBR 1 L	95	
, )	21 JU	N 1995			Single level Bill of Material Procedure: PDC-R-07
	Bom N	umber : 277494-001 - AMP,	Phantoms Exploded Revision: 5		
	Item <b>#</b>	X Part Number Qua Description	ntity Rev Inv	Alt-Part#. .Oper#.	Reference Designator.
•	016	256207 TIE-WRAP,4",BLK	1.0000 1 L	95	
	018	269005-001 SCR,6-32X2-1/4,SLRH,C	1.0000 Z * L	95	
	020	28-0061 WSHR, <b>#</b> 6,FLT,SML-PATT	1.0000 L	95	
	022	28-0090 WSHR,#6,STAR	1.0000 L	95	
	024	29-0051 NUT,6,HEX	1.0000 L	95	
	026	50404 RTV,SIL,RBR	0.5000 B L	95	
	500	-303941-001			

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081	28-0097 WSHR, <b>#</b> 6,STAR,LK	11.0000 L	95	
082	28-0067 WSHR, <b>#6</b> ,FLT,LRG-PA	11.0000 TT L	95	
083	30-0036 SCR,4-40X3/8,SKTBI	1.0000 NHD L	95	
084	278529-001 SCR,6-32X3/4,HH,CZ	1.0000 % L	95	
085	30–0327 SCR, 3х5мм, Ррн	2.0000 L	95	
086	278124-001 ADH,LOCTITE,222,TH	0.0450 RDLK BL	95	
090	P 272732-001 ASY, THERMISTOR, SR6	2.0000 670a 1 L	95	
001	272732 DWG,AST,THERMISTOR	DWG ,SR6670 1 L	10	
005	27-0571 CONN, ID, SKT, 2POS,	2.0000 098" A L	95	
010	32-0227 Shrk, Tubg, Blk, FP30	0.2000 1,X3/32 L	95	
015	32-0444 WR,24G,YEL,1569,7X	1.6000 32 L	95	
020	189-00008-00 THMS, PTC, 2.2K/80-DI	2.0000 Eg,c a l	95	
095	257182 ASY,CABL,SW/FLTR,NI	1.0000 UT 1 L	95	
100	257202 ASY,CABL,SW/PCBA,HC	1.0000 DT 3 L	95	
21 J	UN 1995			Single level Bill of Material
BOM	Number : 277494-001 - AM	P, SR6670A, 115	7	Procedure: PDC-R-07 Phantoms Exploded Revision: 5
Itemi	X Part NumberQ Description	uantity Rev Inv	Alt-Part#. .Oper#.	••••••Reference Designator.
105	257224 Asy,Cabl,SW/PCBA/NE	1.0000 UT 2 L	95	. · · · · · · · · · · · · · · · · · · ·
110	257235 Asy,Cabl,SW/Fltr,Ho	1.0000 T 2 L	95	
115	P 274817-001 PCBA, PWR-SPLY, MTHRB	1.0000 RD,SR6 8 L	95	
001	274817 DWG,PCBA,PWR-SPLY,M	DWG THRBRD 5 L	10	
002	273769 SCHEM, PWR-SPLY, SR66	DWG 70a Bl	10	

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, '	0 <u>5</u> 0	284546-001 SLDR,WR,.040,285,RM	0.0100 A,FLUX B L	95		
•	110	P 09-0108 ASY, PWR-SPLY, ES/SR,	1.0000 115V 22 L	95	Sec	
	001	262576 DWG,ASY,PWR-SPLY,SR	DWG 6670a 5 l	10		
	005	262389 SPEC, TEST, PWR-SPLY,	DWG Es/Sr * L	10		
	010	262391 PROC, TEST, PWR-SPLY,	DWG Es/Sr * L	10		
	015	275198-001 HTSK, PWR-SPLY, SR667	2.0000 OA 1 L	95	n an an an Anna an Anna an Anna an Anna Anna Anna an Anna an Anna Anna	
	020	257455 Covr, Chas, Ps	1.0000 3 L	95	a da serie da serie Esta da serie	
	025	257466 PNL, CHAS, PS	1.0000 2 L	95		
	030	275207-001 Chas, Pwr-Sply, SR667	1.0000 0a 1 L	95		
	032	51145 SPCR, SHLDR, JBL2R	1.0000 B L	95		
	035	VP59010 LBL,CAUT,INFINITY	1.0000 C L	95		
	040	30-0331 SCR,RLK,6-32X3/8",P	5.0000 PH,BZ B L	95		
	045	<b>30-0266</b> SCR, 6-32X5/8, РРН	4.0000 L	95		
	046	30–0057 SCR, 6–32X3/8, PPH	13.0000 L	95	- 	
	050	258164 SCR,6-32X3/8,HXH,W/(	9.0000 D,FLAN 1 L	95		
•	060	17-0038 FLTR, SW-PWR-SPLY, 202	1.0000 A B L	95		
	21 JUN	1995		· · ·	Single level Bill of Materia	1
	BOM Nun	mber : 277494-001 - AME	9, SR6670A, 115V	,	Procedure: PDC-R-07 Phantoms Exploded Revision: 5	<b>-</b>
			antityA	lt-Part	#Reference Designator	•
• •	065	36-0526 INS,AL,OX,TO-218	6.0000 B L	95		· •••.
	070	36-0547 CLIP, SPRNG	6.0000 A L	95		
	080	15-0507 SW, PWR, DPST, 15A	1.0000 C L	95	SW1	-
	·•		- <b>-</b>	. = =		