LinnDrum™

TECHNICAL INFORMATION

TABLE OF CONTENTS

CPU-COMPUTER SECTION

I. FUNCTIONS

A. Generate system clock.

B. Buffer Z80 data and address lines.

C. Decode address space.

D. Control retention of ram data when power is off.

II. OPERATION

A. The system clock is a 4MhZ crystal controlled digital feedback oscillator. This 4MhZ signal is divided down to 2 MhZ by one half of U8 (74LS74) to assure 50% duty cycle. This 2MhZ signal drives pin 6 of U1 (Z-80).

B. The Z-80's data lines are each connected to an input and an output of a tri-state buffer (U4 or U5, 74LS244). The buffers are controlled by the RD and WR signals from U1 for bidirectional operation.

1. Address lines A0 through A11 are buffered by U2 and U3 (74LS365).

2. The BUSREQ (pin 25), WAIT (PIN 24), NMI (pin 17), and INT (pin 16) inputs to U1 are pulled up to +5 volts by 2.4 K resistors to disable their function.

C. 16K of the Z-80's address space is used in the Linndrum. Rom and I/O occupy the bottom 8K of this (A13 low). Ram occupies the upper 8K (A13 high). A13 selects between the two decoders of U7 and is gated by U35 (74LS32) with MREQ. The low numbered decoder of U7 is used to select between Rom, keyboard and I/O. The high numbered decoder selects the 4 ram chips.

1. When A12 through A7 are high, U6 sends a low to U7 to switch from Rom to keyboard and I/O. A6 distinguishes between keyboard and I/O, but is ignored in decoding the Rom.

2. The other half of U7 uses A11 and A12 to select the Ram chips. The select lines to each Ram and the WR signal are gated with the power down signal to prevent memory access when the TTL supply is not at sufficient voltage.

D. The power down signal is essentially the power stable signal gated by MREQ. This prevents interruption of a memory access in progress when the power goes down.

CPU-I/O SECTION

I. FUNCTION

A. Scan keyboard and debounce.

B. Decode output devices/Trigger drum voices.

C. Read trigger inputs.

D. Read tape inputs.

E. Drive displays.

F. Generate tempo clock.

II. OPERATION

A. To scan the keyboard, the CPU reads the address location of a column of the keyboard matrix.

1. If any keys are depressed in that column, they connect the low on one of the U29 gates (74LS05) to a corresponding input of U28 (74LS244). When U28 is enabled, the computer reads the results of that column scan. The play/stop switch has its own input to U28 which is read with each keyboard read.

B. Output device decoding/Drum voice triggering.

1. U20 and U21 (74LS138) are enabled by the out strobe enable line from U7 & U35. They decode address lines A0 through A2. A3 selects between U20 and U21. It is connected to an active low enable on U20 and an active high enable on U21. These two decoders send strobes to 16 output devices-one for each of 10 drum sounds, 5 output latches (U16, U17, U18, U22, & U23 (74LS374) and the click/beep generator.

2. Data to the drum card is gated by tri-state buffer U19 (74365) to reduce noise on the drum card. When data is to be used, the computer sets the pin 9 output of U16 low to enable D0, D1, D2, and D3 on the drum card

3. Whenever a key closure or opening is detected, the Z-80 sends an IOREQ to trigger one half of U30 (LM556). U30 generates a 3 ms. pulse which the CPU reads through U28. The CPU waits until the high-going pulse returns low, and reads the key again to see if it is still in the same state. Only when it confirms this does it respond to the key command.

This prevents multiple triggering from contact bounce.

C. The READ INPORT signal from U7 and U35 puts data from the trigger, cassette and sync inputs onto the data bus through U15.

1. The trigger input circuits put out a digital pulse in response to rapid changes in the input signal. A trigger will only be generated if the envelope of the signal is increasing. Sharp transients trigger. Sustained tones will only cause a trigger when they begin. The input signal is applied to a trimpot to adjust gain from 1 to 10. The 2 sides of the A1 OPAMP and D12 and D13 act as a full wave rectifier. The next stage filters this rectified signal. The third stage runs open loop and acts as a combination differentiator-comparator. The output resistors make the ±15 volt output of the third stage compatible with TTL logic levels.

D. The sync and cassette input circuits are zero crossing detectors. D7, D8, D9 and D10 provide about 1.4 volts of noise immunity. U38 operates as a logarithmic amplifier and controls the output transistors which translate the signal to TTL levels for U15.

E. The displays are driven by decoders U24, U25, U26 and U27 (74LS47) through resistors in resistor packs RP4, RP5, RP6 and RP7 (150Ω). The 2 pairs of decoders are fed data from latches U22 and U23, which are each selected by device decoder U20 (74LS138). Data from the computer is written into the latches as though they were memory locations.

1. The LED indicators are driven directly from latches U17, U18 and part of U16 via resistors in resistor packs RP1, RP2 and RP3 (150). The latches are selected by U20 (74LS138). The output of U16 that drives the "pattern" LED also feeds an inverter which drives the "song" LED whenever the "pattern" LED is off.

2. U16 also drives the cassette output, the trigger output, a line to enable the tape sync output and a line that enables data to the drum card.

F. The tempo clock is generated by an RC controlled oscillator U30 (LM556). The tempo pot on the front panel varies the frequency from about 60 hZ to 300 hZ. This is divided in half by U8 and is put on the data bus by U15. When playing and recording, the CPU uses this signal to determine the length of a 1/192 note.

G. While the Linndrum is playing or recording, it sets a latch output of U16 high, allowing the inverted tempo signal to go out to the tape sync output transistor Q3.

1. At the same time it sends the trigger signal from another latch output of U16 to the trigger output transistor. When the Linndrum is running on external sync, the trigger output will follow the tempo of the sync input. The sync output will follow the tempo of the internal oscillator.

2. The cassette output is driven by a latch output from U16. Two 220 resistors divide the voltage to approximately 2.5V for cassette recorder line inputs.

DRUM SOUND GENERATOR CIRCUIT OVERVIEW

The three drum sound generator circuits (SNR/SSTK, TOM/CGA, MUX DRUMS) share a common method of doing the following:

1. Decoding strobe and data lines from the CPU.

2. Clocking data out of the proms.

3. Converting data from the proms to an analog waveform.

1. A drum strobe consists of two low-going pulses on a voice strobe line, each with its four bit data "word".The first pulse clocks a low on D0 into the D0 latch, resetting the drum circuit. The second pulse clocks a high on D0 and data on the other three lines into their latches, to select the appropriate drum sound.

2. On the second pulse of the drum strobe, the output of the D0 latch enables the counters. The outputs of the counters sequentially address all 4,096 words in the prom. For each address output by the counters, the data word at that address is output to the D to A converter. When count is complete it will reset the latches for a one chip sound; otherwise, it will continue the count for each prom in the drum sound.

3. The prom output is fed to a multiplying digital to analog converter (Am 6070). The 6070 output is the product of the current input (pin 11) and the transfer function of the digital input. The differential current outputs are converted to a voltage by an op amp.

DRM BOARD-MUX DRUMS

I FUNCTIONS

A. Decode strobe & data lines

1. Bass, Tamb, Cbsa
2. HiHat
3. Ride & Crash
4. Claps & Cowbell

B. Provide sequential addressing of proms

1. Bass, Tamb, Cbsa
2. HiHat
3. Ride & Crash
4. Claps & Cowbell

C. Provide multiplex timing circuity

D. Convert prom data to an analog signal

E. Select correct output channel for drum played

F. Filter bass output

G. Control hihat decay

II OPERATING DESCRIPTION

A. Decodes strobe & data lines

1. Bass, Tambourine, and Cabasa: Use drum strobes and D0 & D1 data decoded by a latch (U57, U56, U59 respectively) to select drum and volume level to play.

2. HiHat: Uses two latches (U60 & U39) to decode the drum strobe and D0, D1, D2. D0 enables or disables the drum circuit. D1 selects volume level to play, and D2 selects between open & closed HiHat.

3. Ride and Crash: Each uses a latch (U21 and U40 respectively) to decode drum strobes.

4. Claps and Cowbell: Share a latch (U58) to decode the drum strobe and D0.

B. Provides sequential addressing of proms

1. Bass, Tambourine and Cabasa: Use a 13 bit ripple counter to address the proms. On the second pulse of the drum strobe the counters are enabled and begin sequentially counting through the prom's

addresses. When the count reaches 4096 the 13th bit goes high, clearing the latches and disabling the counters.

2. HiHat: Uses a 15 bit ripple counter to address its proms. On the second pulse of the drum strobe the counters are enabled and begin sequentially counting through the proms' addresses. The 13th and 14th bits are used to enable the four hihat proms in order. This is done with U34 (74 LS 139) which decodes these two inputs and outputs a low to the correct prom select. When the count reaches 16384, the 15th bit goes high, clearing the latches and disabling the counters.

3. Ride and Crash: Each use a 16 bit ripple counter to address the proms. On the second pulse of the drum strobe the counters are enabled and begin sequentially counting through the proms' addresses. The 13th, 14th and 15th bits are decoded by U1 and U20 resectively (74 LS 138's) to provide a low to the correct prom select. When the count reaches 32768 the 16th bit goes high, clearing the latches and disabling the counters.

4. Claps and Cowbell: Each uses a 13 bit ripple counter to address its prom. On the second pulse of the drum strobe the counters are enabled and begin sequentially counting through the prom's addresses. When the count reaches 4096 the 13th bit goes high, clearing the latches and disabling the counters.

C. Provide Multiplex timing cirurity

1. U77 (74LS627) is a voltage controlled oscillator used to generate a clock for the MUX drum circuit. TP1 varies a voltage input on U77 pin 2. This voltage determines the frequency of the square wave output on pin 6.

2. This output is applied to the clock 2 input of the counter U75 (74LS393). Outputs A2 (LSB) & B2 are decoded by U34 (74LS139) and U36 (74LS74) to provide timed enables for the 6070, 74LS138 and 4051 every time a drum circuit is enabled.

3. B2 is used as the clock 1 input. Outputs A1, B1 and C1 (MSB) are decoded by U74 (74LS138) to enable each drum circuit one at a time.

4. When U74 enables a drum circuit, it outputs a low pulse that enables that voice's prom. If the voice's counter is enabled it increments the counters. The prom outputs the data stored at that

address onto the data bus. If the counters are not enabled the prom outputs the data stored at address 000H, which is 00H.

D. Convert prom data to an analog signal

1. The output of the proms is fed to a multiplying DAC. The DAC output is the product of the current input (pin 11) and the transfer function of the data input. The differential curent outputs are converted to a voltage by U89 (TL082).

E. Select correct output channel for drum played

1. The multiplexed analog signal is fed to pin 3, U83 (CD4051). After the signal for each voice has settled, U83 is enabled to connect the signal to one of the sample and hold capacitors and op-amps. The digital inputs on pins 9, 10, and 11 select which output channel.

F. Filter bass output

1. The bass signal is run through a voltage controlled filter. This circuit is the same as the TOM/CGA filter.

G. The Hat signal is run through a voltage controlled amplifier U91 (CEM3360).

1. When a HAT strobe occurs, U37 (LM556) outputs a 5 ms high going pulse. This charges the 1μf capacitor, which discharges through two paths. If the HAT is open (pin 5, U39 high), it discharges only through the 1Meg resistor. If the HAT is closed (pin 5, U39 low), it also discarges through the HiHat decay control on the front panel.

2. The VCA makes the shaped pulse the amplitude envelope for the Hat output.

DRM BOARD-SNR/SSTK,CLICK,BEEP

A. Decode strobe and data lines.

B. Generate clock of proper frequency based on tuning pot setting on the mixer and the CV input.

C. Provide sequential addressing for proms.

D. Convert prom data to an analog signal.

E. Select correct output for drum played.

F. Provide click output

G. Provide beep output.

A) On the first pulse, D0 is low; which will clear the counters and reset the circuit in case it had been playing a drum. The rest of the data bits are not used.
On the second pulse, all four data bits are used to select which drum and what volume to play at.

	D0 U41,Q1	D1 U41,Q2;$\overline{Q2}$		D2 U42,Q1	D3 U42,Q2
NODRUMS	H	X	X	X	X
SSTK	L	H	L	H	H
SNAR1	L	L	H	L	L
SNAR2	L	L	H	H	L
SNAR3	L	L	H	L	H

D0 - Used to turn drum circuit on and off.
D1 - Selects between SNR prom and SSTK prom and correct output channel.
D2&D3 - Selects volume for drum played.

B) The snare tuning pot on the MXR board supplies a voltage level to U95 which sums it with the control voltage input, if any. This is passed on to the diode protected CV input of U80, a voltage controlled oscillator. U80 outputs a square

wave signal whose frequency is determined by the voltage on the CV input. This output provides clock pulses to the counters.

C) The counters U61 & U62 (74 LS 393's) are set up as a 13 bit ripple counter. The first 12 bits count through the addresses of the prom selected. When the count reaches 4096 the 13th bit goes high, is inverted by U76 (74LS00) and clears the latches.

D) The output of the proms is fed to a multiplying digital to analog converter (DAC). The DAC output is a product of the current input (pin 11) and the transfer function of the data input. The volume level selected by D2 & D3 determines the current input on pin 11. The differential current outputs are converted to a voltage by U103 (4558).

E) U90 (CD4053) selects the correct output for the drum played based on the signal at pin 11. A low from Q2 of U42 selects pin 13 as the output and a high on Q2 selects pin 12.

F) When a click strobe is received from the CPU the falling edge of the pulse triggers U65 (LM556). This output is a high going 1 ms. pulse. It is routed through a blocking cap to the click direct output jack and to the MXR board via the 40 pin dip connector.

G) When a beep signal is received from the CPU, U76 buffers it and routes it thru a .01μf blocking cap to the 40 pin dip connector.

DRM BOARD-TOM/CGA

I. FUNCTIONS

A. Decode strobe and data lines.

B. Generate clock of proper frequency based on tuning pot settings on the mixer and the CV input.

C. Provide sequential addressing for proms.

D. Provide prom select signals.

E. Convert prom data to an analog signal.

F. Filter analog signals.

G. Select correct output for drum played.

II. OPERATING DESCRIPTION

A. On the first pulse, DO is low; which will clear the counters, and reset the circuit in case it had been playing a drum. The rest of the data bits are not used.
On the second pulse, all four data bits are used to select which drum is to play.

	DO U73,Q1	D1 U73,Q2	D3 U72,Q2	D2 U72,Q1
		"C"	"B"	"A"
NO DRUMS	L	X	X	X
LO CGA	H	L	L	L
HI CGA	H	L	L	H
LO TOM	H	H	L	L
MID TOM	H	H	L	H
HI TOM	H	H	H	L

B. The five tuning pots on the MXR board supply voltage levels to U81 (4051). One of these levels is selected by the data on A, B, and C inputs and passed on to the output (pin 3). U80 (74 LS 627) is a voltage

controlled oscillator used to generate the clock signal, based on the voltage level applied to its control voltage input. The output of U80 provides the clock for the counters.

C. The counters U70 & U71 (74 LS 393's) are set up as 14 bit ripple counter. The first 12 bits count through the addresses of the "A" prom. When the count reaches 4096 the 13th bit goes high disabling the "A" prom, and enabling the "B" prom. When the count reaches 8192 the 14th bit goes high to clear the latches and disable the counters.

D. The Q2 output of U73 enables the TOM or CGA proms. The CGA enable is gated so that neither pair of proms is enabled when no TOMs or CGAs are playing.

E. The output of the proms is fed to a multiplying DAC. The DAC output is the product of the current input (pin 11) and the transfer function of the data input. The differential current outputs are converted to a voltage by U85 (4558).

F. The TOM/CGA circuit uses a CEM 3320 voltage controlled filter to reduce noise at low signal levels.

1. When a TOM/CGA strobe occurs, U22 (LM556) outputs a 5 ms pulse. U84 (TL082) and releated circuitry shapes the pulse as shown in figure 1.

2. This shaped pulse is applied to U86 pin 12, the control voltage input of the voltage controlled filter. The CV input controls the frequency of the four poles. It allows the attack transients through with little filtering. As the drum sound decays U86 filters the digitizing noise.

G. The analog output is fed to U87 (CD4051). U87 connects that signal to one of the output op-amps "U". The digital inputs, pins 9, 10 and 11 select which op-amp. Pin 6 is used to reduce output noise when no TOMs or CGAs are playing.

DRM BOARD/5VSR BOARD-POWER SUPPLY

I. FUNCTIONS

A. Supply TTL voltage to all devices except CMOS and OP AMPS.

B. Supply CMOS voltage to CMOS rams (U9, U10, U11, U12,) and three CMOS I.C.'s (U33, U36, U37) on CPU board and U63 on the DRM board.

C. Supply battery voltage to the CMOS devices for memory retention when AC power is interrupted.

D. Supply analog voltage to all OP Amps on DRM & CPU boards.

E. Generate power stable line for CPU.

II. OPERATING DESCRIPTION

A. TTL VOLTAGE

1. Voltage from the transformer is rectified by diodes D10, D11, D12, D13 and filtered by C36 (27,000μF). All these components are located on the drum board.

2. This front end voltage approximately 12V is fed through pin 2 of the 7 pin molex. This is filtered further on the 5VSR board by C3.

3. The switching regulator UR2 alternately connects and disconnects the front end to the inductor L1. VR2 varies the duty cycle of alternation to control the voltage after the LC choke. Ground is supplied on pins 3 and 5 of the 7 pin molex.

4. C2 is the timing cap for the switching frequency. C1 is a filter cap for the current limit circuit. L1 is an RF choke to smooth the output of VR2.

5. The current limit circuit is used with National regulators only. When the current through R5 is too high, its voltage drop causes transistor Q1 and Q2 to pull down the voltage on the voltage reference line of VR2.

6. The output of the regulator VR2 is seen at pin 7 of of the 7-pin molex. This output may be varied by adjusting the value of the trimpot on the 5VSR board which in conjunction with R3 & R4 sets a voltage for the Error Amplifier Input of VR2.

B. CMOS VOLTAGE

1. Front end is applied on pin 1 of VR1. R2 sets a ground reference above ground causing an output of approximately 5.9V. This is dropped through D1 to approximately 5.3V. This output can be seen on pin 1 of the 7 pin molex. The diode keeps the batteries from draining through VR1 in power down mode. R1 is for trickle charging the batteries.

C. BATTERIES

1. BATT 1, BATT 2, BATT 3 are in series to provide approximately 4.0 volts when completely charged. They should never be below 3.2 volts.

D. ANALOG VOLTAGE (DRM BOARD)

1. D14, D15, D16, D17, form a bridge providing front ends for +15 and -15 volts; around a center tapped ground on the transformer.

2. -15 VOLTS

   a. The -15v front end is filtered by C17 and fed to pin 2 of VR 4.
   b. Pin 1 of VR4 is ground.
   c. VR4 regulates this front end to approximately -15v. C19 filters the output voltage on pin 3 of VR4.

3. +15 VOLTS

   a. The +15v front end is filtered by C16 and fed to pin 1 of VR3.
   b. Pin 2 of VR3 is ground.
   c. VR3 regulates this front end to approximately +15v. C18 filters the output voltage on pin 3 of VR3.

E. POWER STABLE

1. The circuit consisting of R20, C11 and VR2 on DRM board sets up a stable voltage reference of 1.23 volts, for pin
15 of U63.

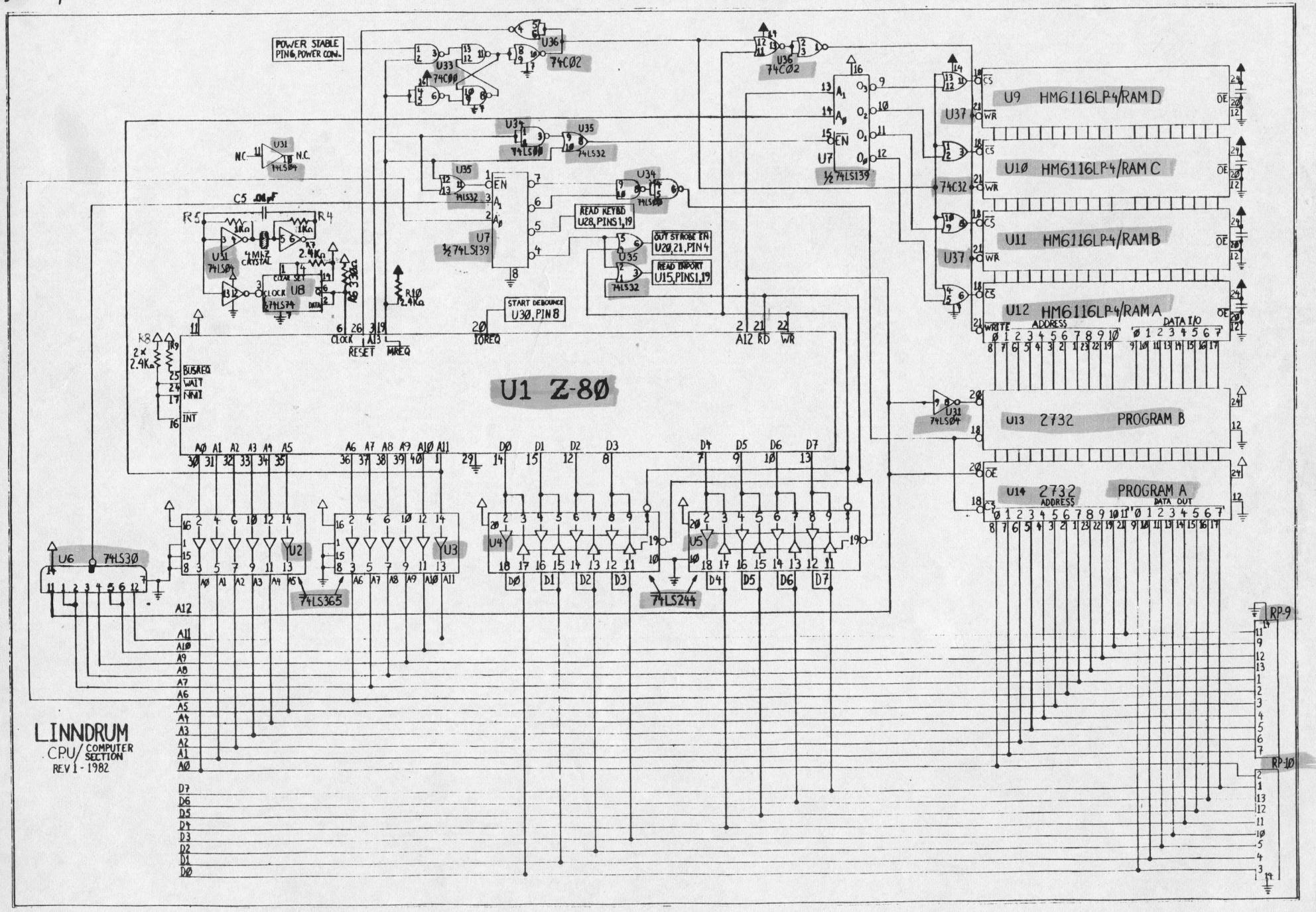
2. +15 volt front end is fed thru a voltage divider consisting of R25 and R26.

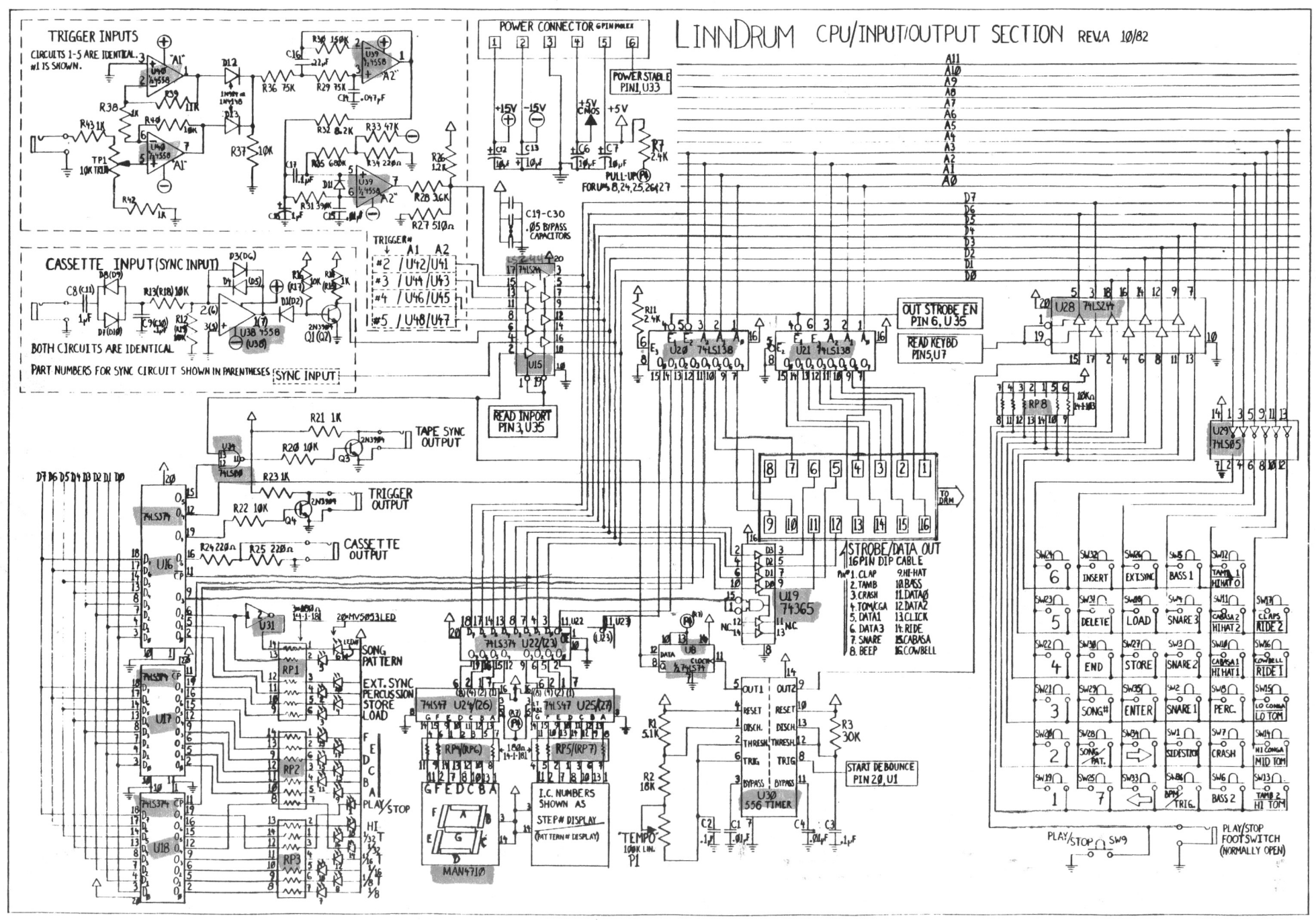
3. The divided front end is fed to the circuit consisting of R24, D18, and C15. This circuit delays the signal, fed to pin 14 of U63, by the

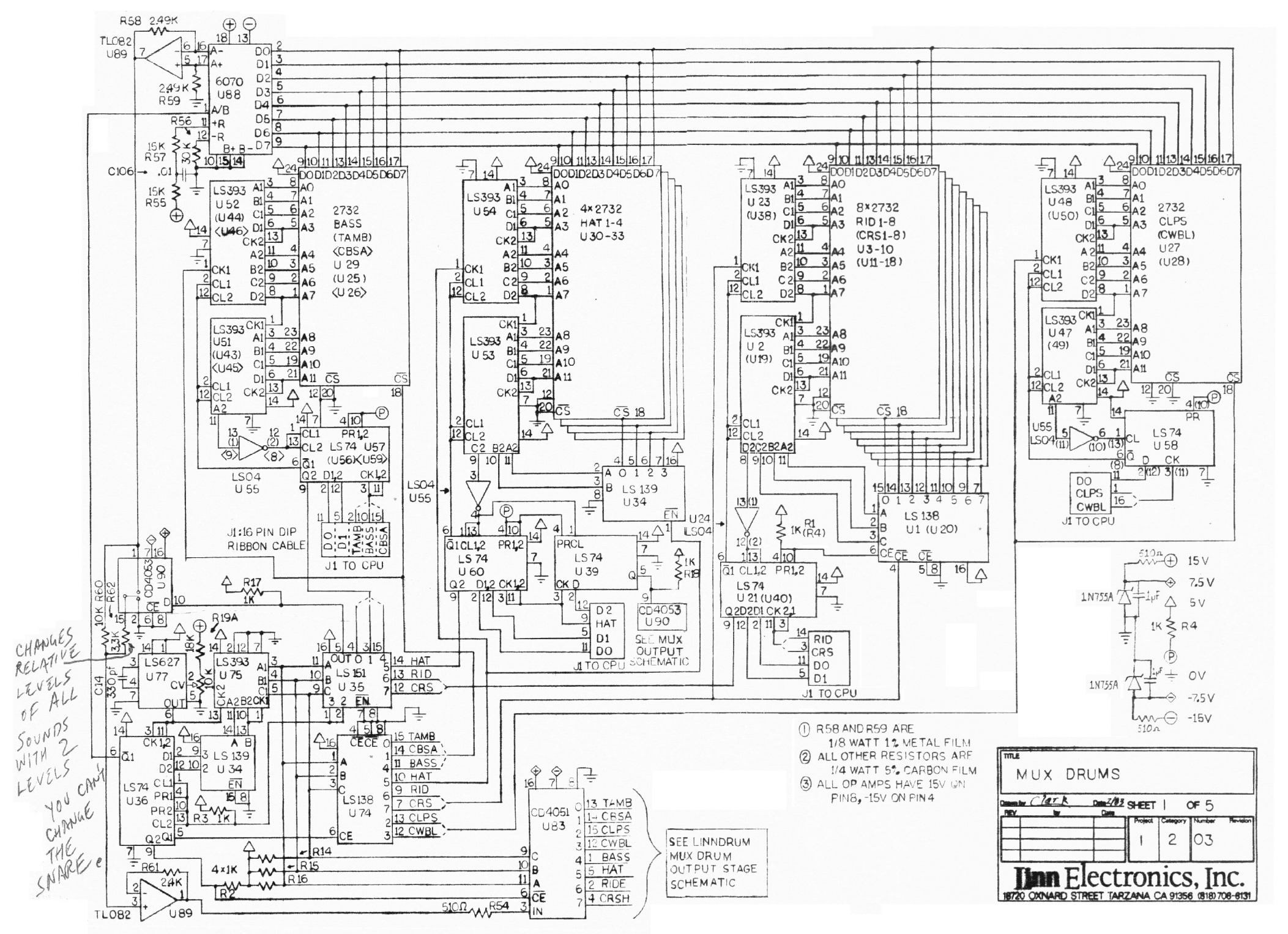
amount of time it takes to charge C15 (approx. .5 sec).

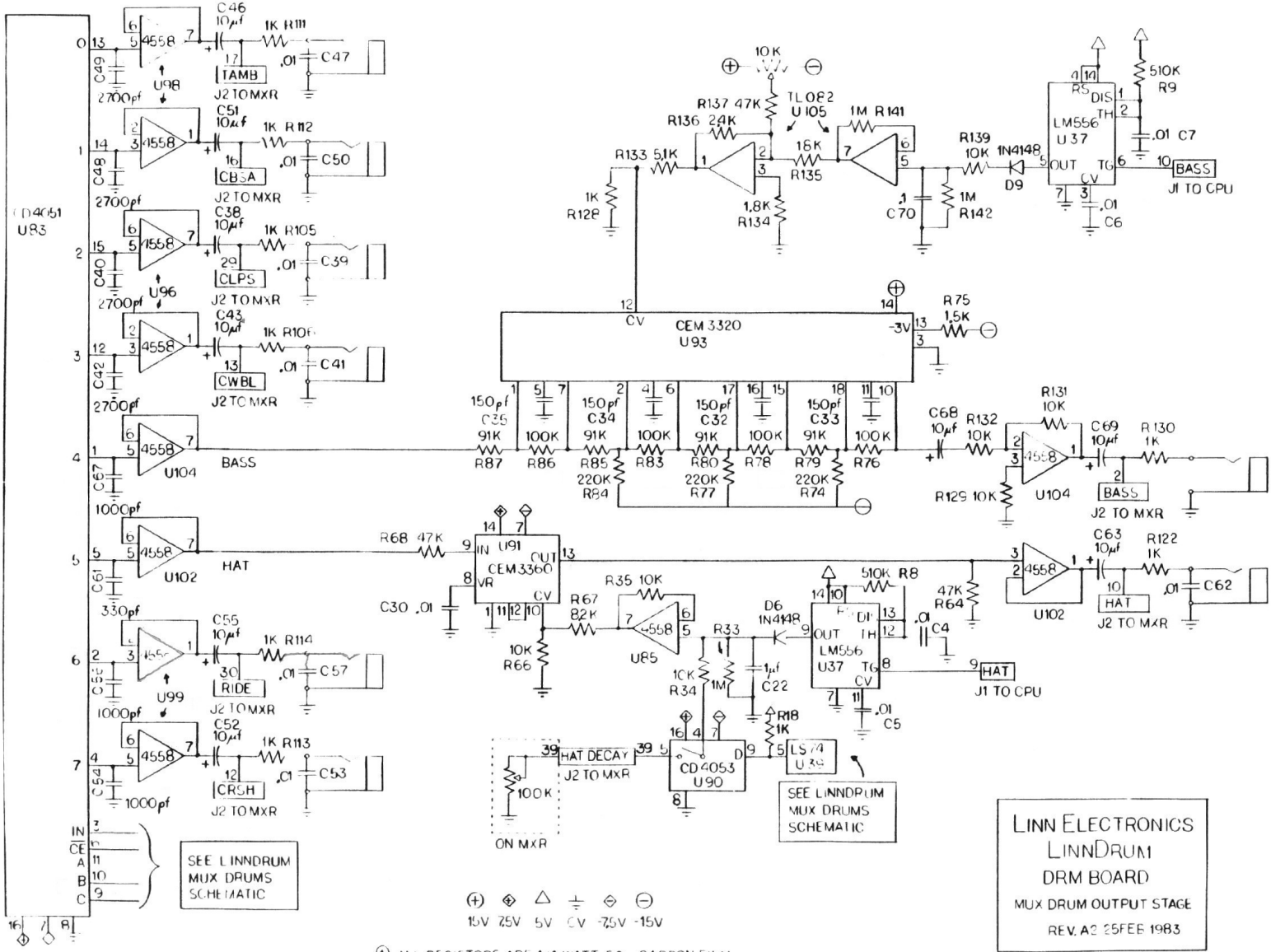
4. U63 compares that with the reference voltage on pin 15, if it exceeds that voltage, it will cause the output on pin 16 to go high, indicating stable AC power to the CPU board.

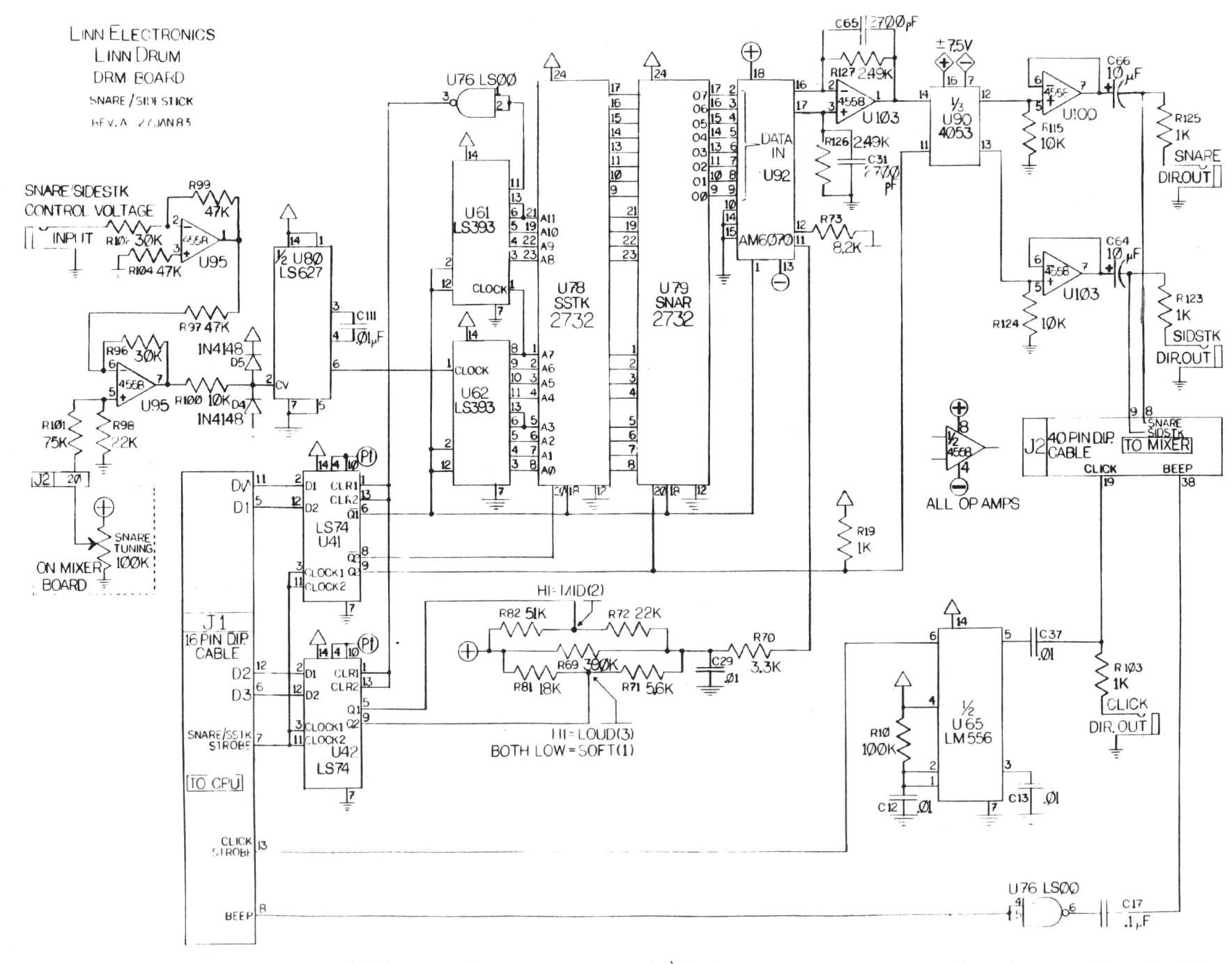
5. R23 sets the amount of hysteresis.

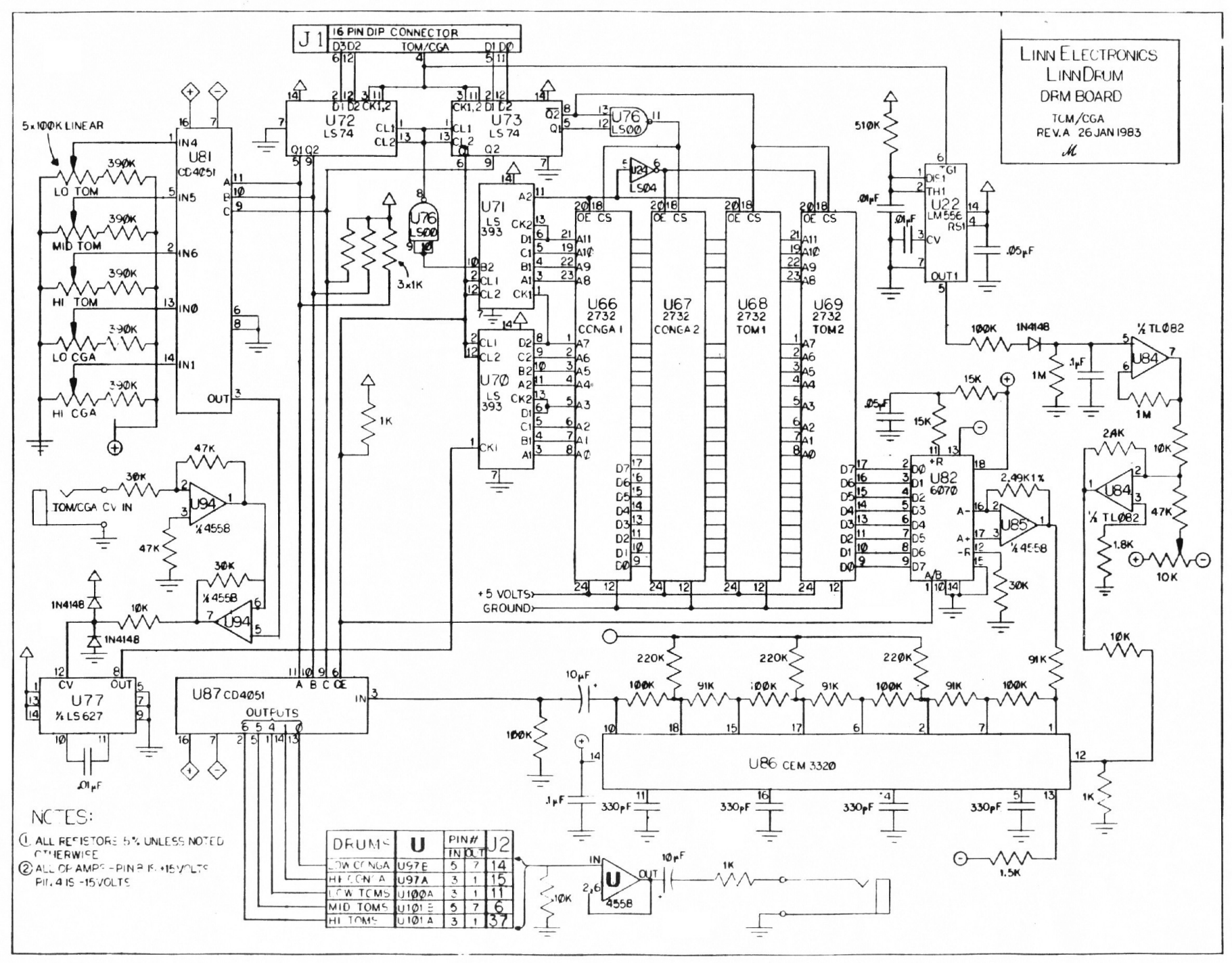

POWER STABLE
PIN6, POWER CONN.
U36
74C02
U33
74C00
U37
74LS00
U35
74LS32
U31
74LS04
NC
N.C.
C5 .04µF
R5
10KΩ
R4
1KΩ
R7
2.4KΩ
4MHZ CRYSTAL
U8
74LS74
R6
330Ω
R10
2.4KΩ
U7
½ 74LS139
U34
74LS86
READ KEYBD
U28, PINS 1,19
OUT STROBE EN
U20,21, PIN 4
READ INPORT
U15, PINS 1,19
START DEBOUNCE
U30, PIN 8
CLOCK
RESET
MREQ
IOREQ
A12
RD
WR
R8
2x 2.4KΩ
R9
BUSREQ
WAIT
NMI
INT
U1 Z-80
U6 74LS30
U2
U3
74LS365
U4
U5
74LS244
U9 HM6116LP-4/RAM D
U10 HM6116LP-4/RAM C
U11 HM6116LP-4/RAM B
U12 HM6116LP-4/RAM A
74C32
WRITE ADDRESS
DATA I/O
U13 2732 PROGRAM B
U14 2732 PROGRAM A
ADDRESS
DATA OUT
RP-9
RP-10
LINNDRUM
CPU/ COMPUTER SECTION
REV 1 - 1982

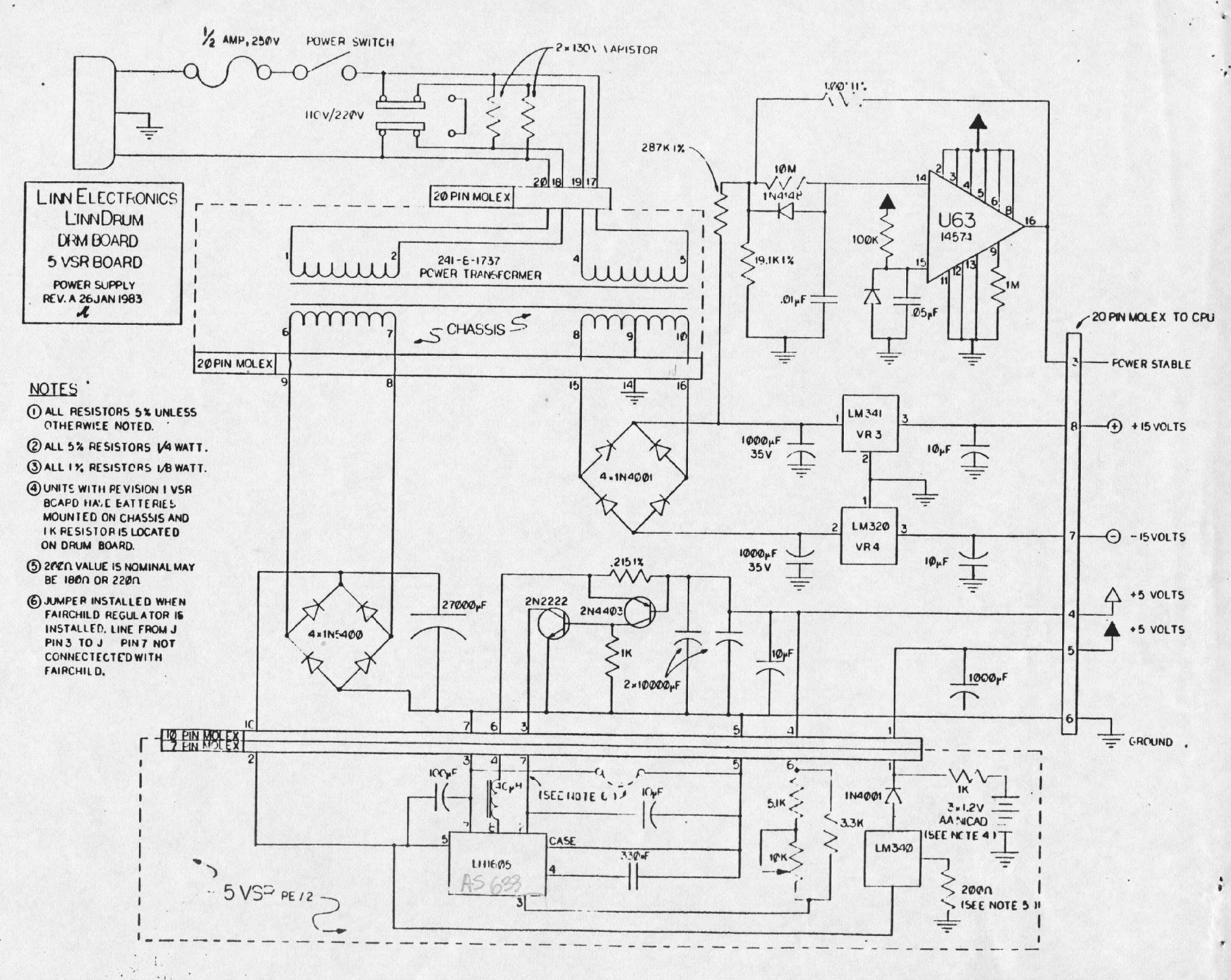

LINNDRUM CPU/INPUT/OUTPUT SECTION REV.A 10/82
TRIGGER INPUTS
CIRCUITS 1-5 ARE IDENTICAL. #1 IS SHOWN.
POWER CONNECTOR 6 PIN MOLEX
POWER STABLE PIN1, U33
PULL-UP(P8) FOR U#S 8,24,25,26&27
C19-C30 .05 BYPASS CAPACITORS
CASSETTE INPUT (SYNC INPUT)
BOTH CIRCUITS ARE IDENTICAL
PART NUMBERS FOR SYNC CIRCUIT SHOWN IN PARENTHESES
SYNC INPUT
TRIGGER# A1 A2
#2 / U42 / U41
#3 / U44 / U43
#4 / U46 / U45
#5 / U48 / U47
READ INPORT PIN 3, U35
OUT STROBE EN PIN 6, U35
READ KEYBD PIN 5, U7
TAPE SYNC OUTPUT
TRIGGER OUTPUT
CASSETTE OUTPUT
STROBE/DATA OUT 16 PIN DIP CABLE
1. CLAP
2. TAMB
3. CRASH
4. TOM/CGA
5. DATA1
6. DATA3
7. SNARE
8. BEEP
9. HI-HAT
10. BASS
11. DATA0
12. DATA2
13. CLICK
14. RIDE
15. CABASA
16. COWBELL
TO DRM
SONG PATTERN
EXT. SYNC
PERCUSSION STORE
LOAD
PLAY/STOP
HI 1/32T 1/16T 1/16 1/8T 1/8
I.C. NUMBERS SHOWN AS STEP# DISPLAY (PATTERN# DISPLAY)
MAN4710
TEMPO 100K LIN. P1
START DEBOUNCE PIN 20, U1
PLAY/STOP SW9
PLAY/STOP FOOTSWITCH (NORMALLY OPEN)


R58 2.49K
TL082 U89
2.49K R59
6070 U88
A/B
+R
-R
B+ B-
R56 30K
R57 15K
C106 .01
R55 15K
LS393 U52 (U44) <U46>
LS393 U51 (U43) <U45>
LS393 U54
LS393 U53
LS393 U23 (U38)
LS393 U2 (U19)
LS393 U48 (U50)
LS393 U47 (49)
2732 BASS (TAMB) <CBSA> U 29 (U 25) <U 26>
4×2732 HAT 1-4 U30-33
8×2732 RID 1-8 (CRS1-8) U3-10 (U11-18)
2732 CLPS (CWBL) U27 (U28)
LS04 U 55
LS74 U57 (U56)(U59)
LS74 U 60
LS74 U 39
LS74 U 21 (U40)
LS74 U 58
LS 139 U 34
LS 138 U1 (U 20)
J1:16 PIN DIP RIBBON CABLE
J1 TO CPU
LS04 U55
U24 LS04
CD4053 U90
SEE MUX OUTPUT SCHEMATIC
R1 1K (R4)
R17 1K
R19A
10K R60
R62
CD4053 U 90
LS627 U77
LS393 U75
LS 151 U 35
LS 139 U 34
LS74 U36
LS138 U 74
CD4051 U83
SEE LINNDRUM MUX DRUM OUTPUT STAGE SCHEMATIC
R61 24K
TL082 U89
R2 4×1K
R14
R15
R16
R3 1K
510Ω R54
510Ω
15 V
7.5 V
5 V
1K R4
0V
-7.5 V
-15V
1N755A
1μF
CHANGES RELATIVE LEVELS OF ALL SOUNDS WITH 2 LEVELS YOU CAN'T CHANGE THE SNARE e
① R58 AND R59 ARE 1/8 WATT 1% METAL FILM
② ALL OTHER RESISTORS ARE 1/4 WATT 5% CARBON FILM
③ ALL OP AMPS HAVE 15V ON PIN8, -15V ON PIN4
TITLE
MUX DRUMS
Drawn by Clark Date 2/83 SHEET 1 OF 5
REV. by Date
Project 1 Category 2 Number 03 Revision
Linn Electronics, Inc.
18720 OXNARD STREET TARZANA CA 91356 (818)708-8131


CD4051 U83
C46 10µf
1K R111
TAMB
J2 TO MXR
C49 2700pf
U98
C51 10µf
1K R112
CBSA
J2 TO MXR
C48 2700pf
C38 10µf
1K R105
CLPS
J2 TO MXR
C40 2700pf
U96
C43 10µf
CWBL
J2 TO MXR
C42 2700pf
C67 1000pf
U104
BASS
C61 330pf
U102
HAT
C55 10µf
1K R114
RIDE
J2 TO MXR
C58 1000pf
U99
C52 10µf
1K R113
CRSH
J2 TO MXR
C54 1000pf
IN
CE
A
B
C
SEE LINNDRUM MUX DRUMS SCHEMATIC
10K
R137 47K
TL082 U105
R136 24K
R133 5.1K
1K R128
1M R141
18K R135
1.8K R134
R139 10K
1N4148 D9
.1 C70
1M R142
510K R9
LM556 U37
.01 C7
.01 C6
BASS
J1 TO CPU
CEM 3320 U93
CV
-3V
R75 1.5K
150pf C35
150pf C34
150pf C32
150pf C33
91K R87
100K R86
91K R85
220K R84
100K R83
91K R80
220K R77
100K R78
91K R79
220K R74
100K R76
C68 10µf
R132 10K
R131 10K
R129 10K
U104
C69 10µf
R130 1K
BASS
J2 TO MXR
R68 47K
U91 CEM3360
C30 .01
R67 82K
10K R66
R35 10K
U85
D6 1N4148
R33
1K R34
1M
1µf C22
R18 1K
510K R8
LM556 U37
.01 C4
.01 C5
HAT
J1 TO CPU
47K R64
U102
C63 10µf
R122 1K
.01 C62
HAT
J2 TO MXR
HAT DECAY
J2 TO MXR
100K
ON MXR
CD4053 U90
LS74 U39
SEE LINNDRUM MUX DRUMS SCHEMATIC
15V 25V 5V 0V -75V -15V
① ALL RESISTORS ARE 1/4 WATT, 5%, CARBON FILM
② ALL OP AMPS HAVE 15V ON PIN8, -15V ON PIN4
LINN ELECTRONICS
LINNDRUM
DRM BOARD
MUX DRUM OUTPUT STAGE
REV. A2 25FEB 1983

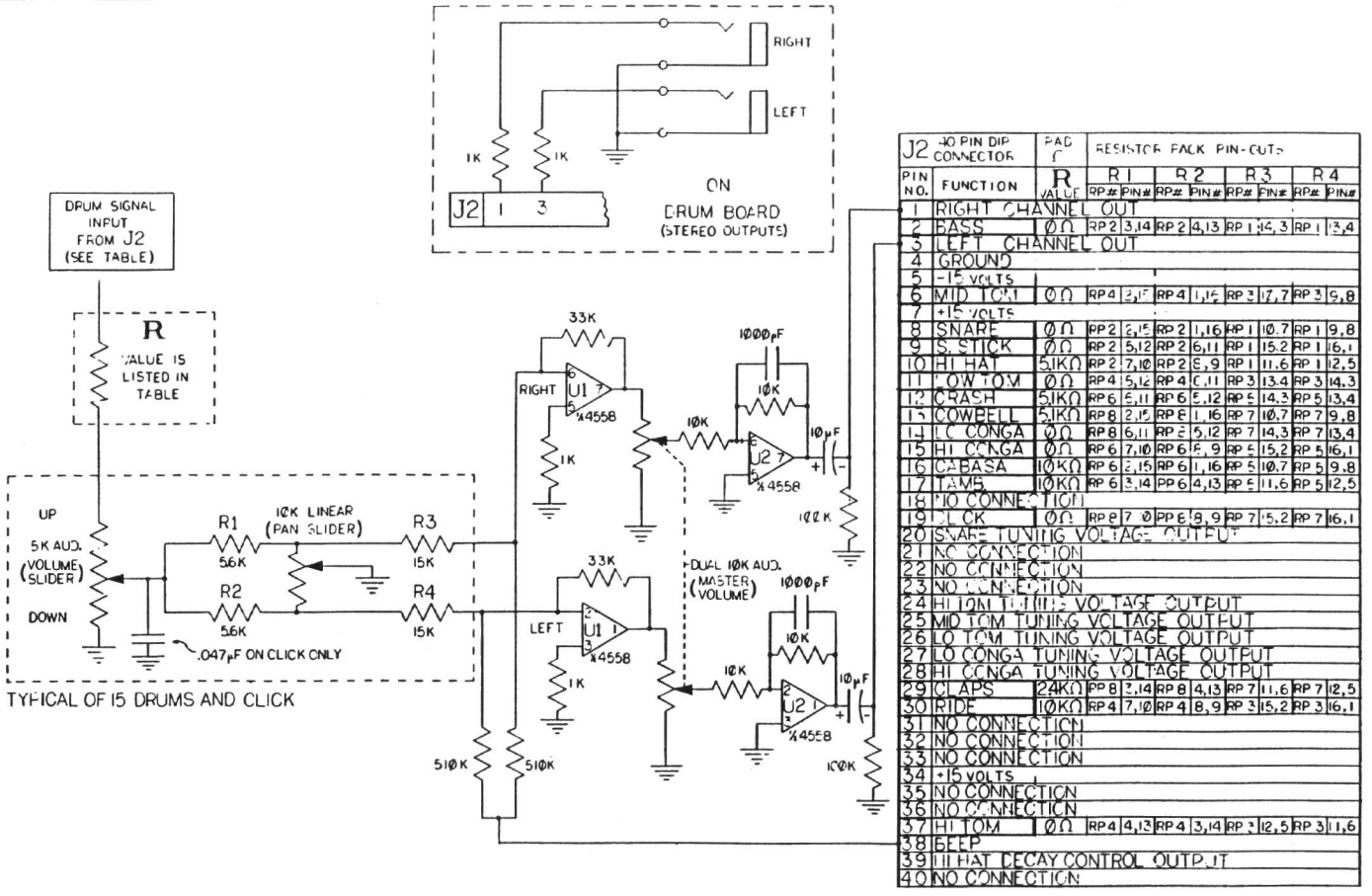

LINN ELECTRONICS
LINN DRUM
DRM BOARD
SNARE / SIDESTICK
REV. A 27JAN83
SNARE/SIDESTK CONTROL VOLTAGE
INPUT
R99 47K
R100 30K
R104 47K
U95
R97 47K
R96 30K
U95
R101 75K
R98 22K
R100 10K
1N4148 D5
1N4148 D4
J2 20
SNARE TUNING 100K
ON MIXER BOARD
½ U80 LS627
C111 .01µF
U76 LS00
U61 LS393
U62 LS393
CLOCK
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
U78 SSTK 2732
U79 SNAR 2732
DATA IN U92
AM6070
R73 8.2K
C65 2700pF
R127 249K
R126 249K
C31 2700 PF
U103
±7.5V
⅓ U90 4053
U100
C66 10µF
R115 10K
R125 1K
SNARE DIR.OUT
U103
C64 10µF
R124 10K
R123 1K
SIDSTK DIR.OUT
½ 4558
ALL OP AMPS
J2 40 PIN DIP CABLE
TO MIXER
SNARE
SIDSTK
CLICK
BEEP
R19 1K
J1 16 PIN DIP CABLE
D0
D1
D2
D3
SNARE/SSTK STROBE
TO CPU
CLICK STROBE
BEEP
U41 LS74
U42 LS74
HI=MID(2)
R82 51K
R72 22K
R69 390K
R70 3.3K
C29 .01
R81 18K
R71 5.6K
HI=LOUD(3)
BOTH LOW=SOFT(1)
R10 100K
½ U65 LM556
C12 .01
C13 .01
C37 .01
R103 1K
CLICK DIR.OUT
U76 LS00
C17 .1µF


LINN ELECTRONICS
LINNDRUM
DRM BOARD
TOM/CGA
REV.A 26 JAN 1983
J1 16 PIN DIP CONNECTOR
D3 D2 TOM/CGA D1 D0
5x100K LINEAR
LO TOM
MID TOM
HI TOM
LO CGA
HI CGA
390K
U81 CD4051
U72 LS74
U73 LS74
U71 LS 393
U70 LS 393
U76 LS00
U24 LS04
3x1K
1K
U66 2732 CONGA 1
U67 2732 CONGA 2
U68 2732 TOM1
U69 2732 TOM2
OE CS
510K
.01µF
U22 LM556
.05µF
100K
1N4148
½ TL082
U84
1M
.1µF
15K
U82 6070
2.49K 1%
U85 ¼ 4558
30K
2.4K
10K
47K
1.8K
TOM/CGA CV IN
U94 ¼ 4558
+5 VOLTS
GROUND
U77 ½ LS 627
U87 CD4051
OUTPUTS
220K
91K
10µF
U86 CEM 3320
330pF
1.5K
NOTES:
1. ALL RESISTORS 5% UNLESS NOTED OTHERWISE
2. ALL OP AMPS - PIN 8 IS +15 VOLTS PIN 4 IS -15 VOLTS
DRUMS | U | PIN# IN | PIN# OUT | J2
LOW CONGA | U97E | 5 | 7 | 14
HI CONGA | U97A | 3 | 1 | 15
LOW TOMS | U100A | 3 | 1 | 11
MID TOMS | U101B | 5 | 7 | 6
HI TOMS | U101A | 3 | 1 | 37



NOTES

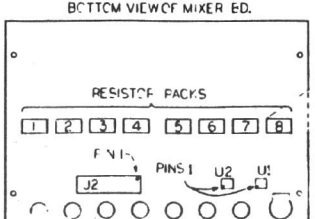
1. ALL RESISTORS 5% UNLESS OTHERWISE NOTED.
2. ALL 5% RESISTORS 1/4 WATT.
3. ALL 1% RESISTORS 1/8 WATT.
4. UNITS WITH REVISION 1 VSR BOARD HAVE BATTERIES MOUNTED ON CHASSIS AND 1K RESISTOR IS LOCATED ON DRUM BOARD.
5. 200Ω VALUE IS NOMINAL MAY BE 180Ω OR 220Ω
6. JUMPER INSTALLED WHEN FAIRCHILD REGULATOR IS INSTALLED. LINE FROM J PIN 3 TO J PIN 7 NOT CONNECTECTED WITH FAIRCHILD.

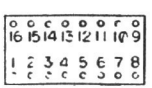


J2 40 PIN DIP CONNECTOR		PAD R	RESISTOR PACK PIN-OUTS							
			R1		R2		R3		R4	
PIN NO.	FUNCTION	VALUE	RP#	PIN#	RP#	PIN#	RP#	PIN#	RP#	PIN#
1	RIGHT CHANNEL OUT									
2	BASS	0Ω	RP2	3,14	RP2	4,13	RP1	14,3	RP1	13,4
3	LEFT CHANNEL OUT									
4	GROUND									
5	-15 VOLTS									
6	MID TOM	0Ω	RP4	2,15	RP4	1,16	RP3	17,7	RP3	9,8
7	+15 VOLTS									
8	SNARE	0Ω	RP2	2,15	RP2	1,16	RP1	10,7	RP1	9,8
9	S. STICK	0Ω	RP2	5,12	RP2	6,11	RP1	15,2	RP1	16,1
10	HI HAT	5.1KΩ	RP2	7,10	RP2	8,9	RP1	11,6	RP1	12,5
11	LOW TOM	0Ω	RP4	5,12	RP4	6,11	RP3	13,4	RP3	14,3
12	CRASH	5.1KΩ	RP6	6,11	RP6	5,12	RP5	14,3	RP5	13,4
13	COWBELL	5.1KΩ	RP8	2,15	RP8	1,16	RP7	10,7	RP7	9,8
14	LC CONGA	0Ω	RP8	6,11	RP8	5,12	RP7	14,3	RP7	13,4
15	HI CONGA	0Ω	RP6	7,10	RP6	8,9	RP5	15,2	RP5	16,1
16	CABASA	10KΩ	RP6	2,15	RP6	1,16	RP5	10,7	RP5	9,8
17	TAMB	10KΩ	RP6	3,14	RP6	4,13	RP5	11,6	RP5	12,5
18	NO CONNECTION									
19	CLICK	0Ω	RP8	7,10	RP8	8,9	RP7	15,2	RP7	16,1
20	SNARE TUNING VOLTAGE OUTPUT									
21	NO CONNECTION									
22	NO CONNECTION									
23	NO CONNECTION									
24	HI TOM TUNING VOLTAGE OUTPUT									
25	MID TOM TUNING VOLTAGE OUTPUT									
26	LO TOM TUNING VOLTAGE OUTPUT									
27	LO CONGA TUNING VOLTAGE OUTPUT									
28	HI CONGA TUNING VOLTAGE OUTPUT									
29	CLAPS	24KΩ	RP8	3,14	RP8	4,13	RP7	11,6	RP7	12,5
30	RIDE	10KΩ	RP4	7,10	RP4	8,9	RP3	15,2	RP3	16,1
31	NO CONNECTION									
32	NO CONNECTION									
33	NO CONNECTION									
34	+15 VOLTS									
35	NO CONNECTION									
36	NO CONNECTION									
37	HI TOM	0Ω	RP4	4,13	RP4	3,14	RP3	12,5	RP3	11,6
38	BEEP									
39	HI HAT DECAY CONTROL OUTPUT									
40	NO CONNECTION									

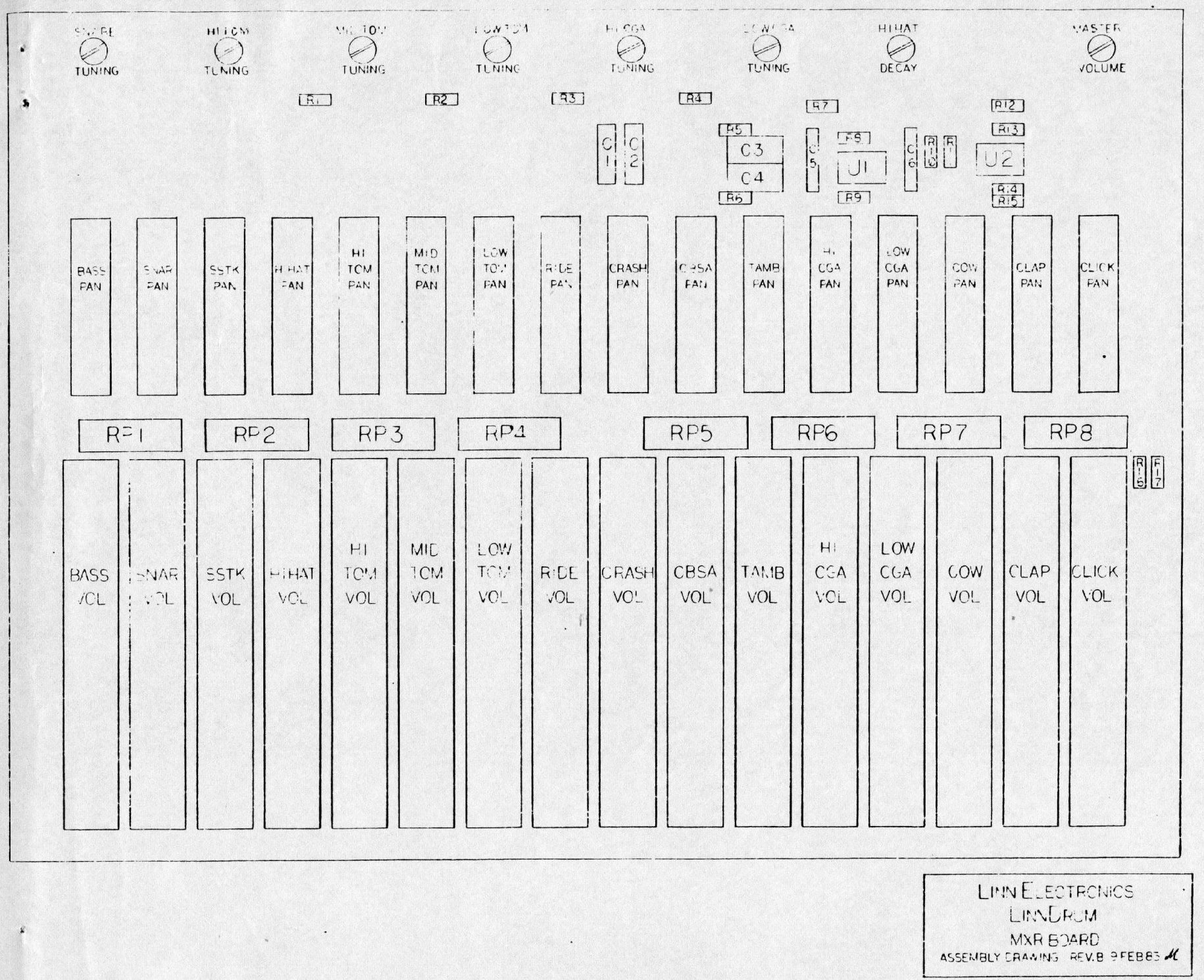
NOTES:

1. U1-U2 PIN 8 IS +15 VOLTS / PIN 4 IS -15 VOLTS.
2. R1-R2 ARE IN THE SAME RESISTOR PACK.
3. R3-R4 ARE IN THE SAME RESISTOR PACK.
4. RP1, RP3, RP5, RP7 ARE ALL 4116R-001-153.
5. RP2, RP4, RP6, RP8 ARE ALL 4116R-001-102
6. ALL RESISTORS ARE 5% UNLESS OTHERWISE NOTED.

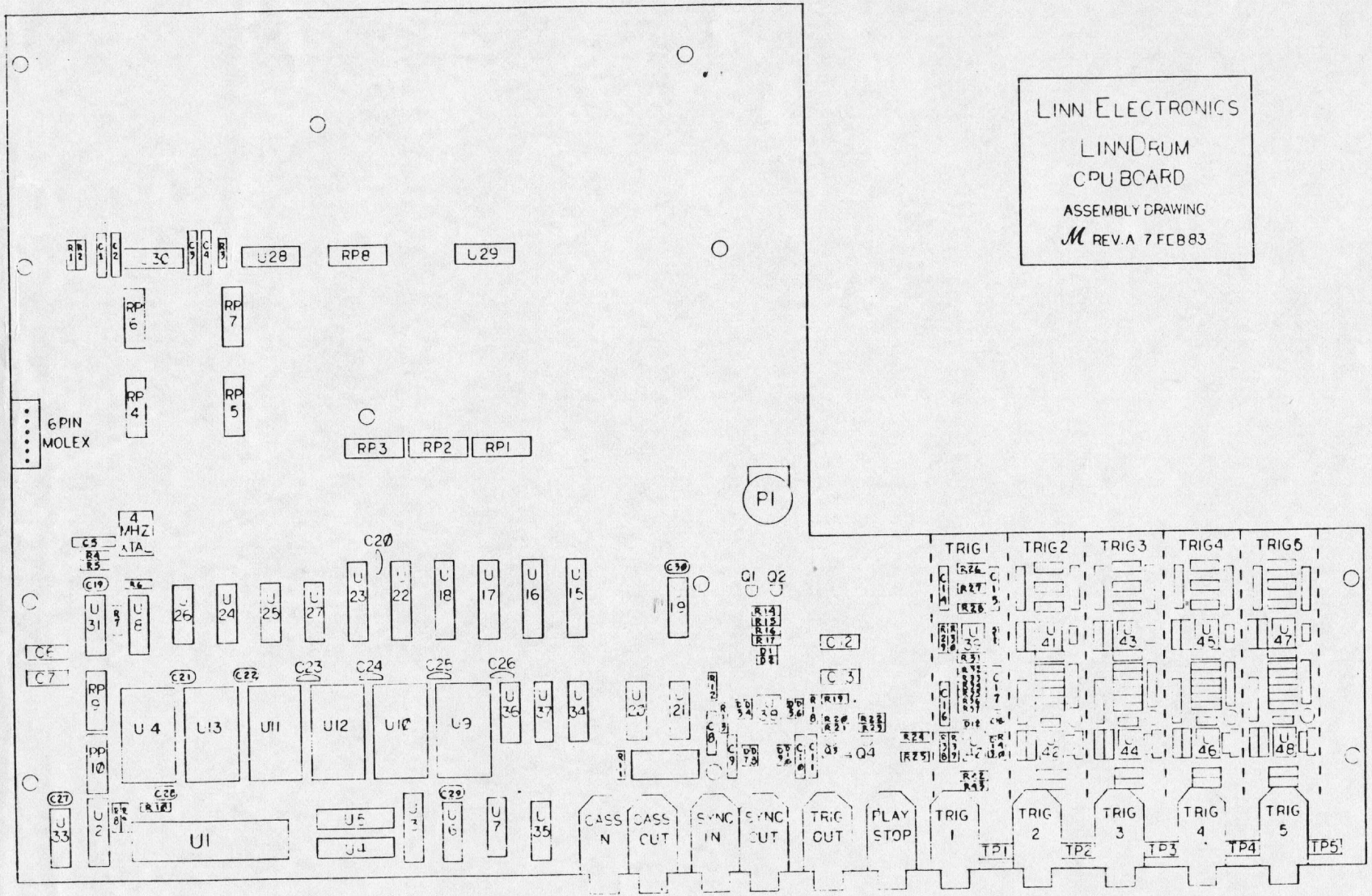


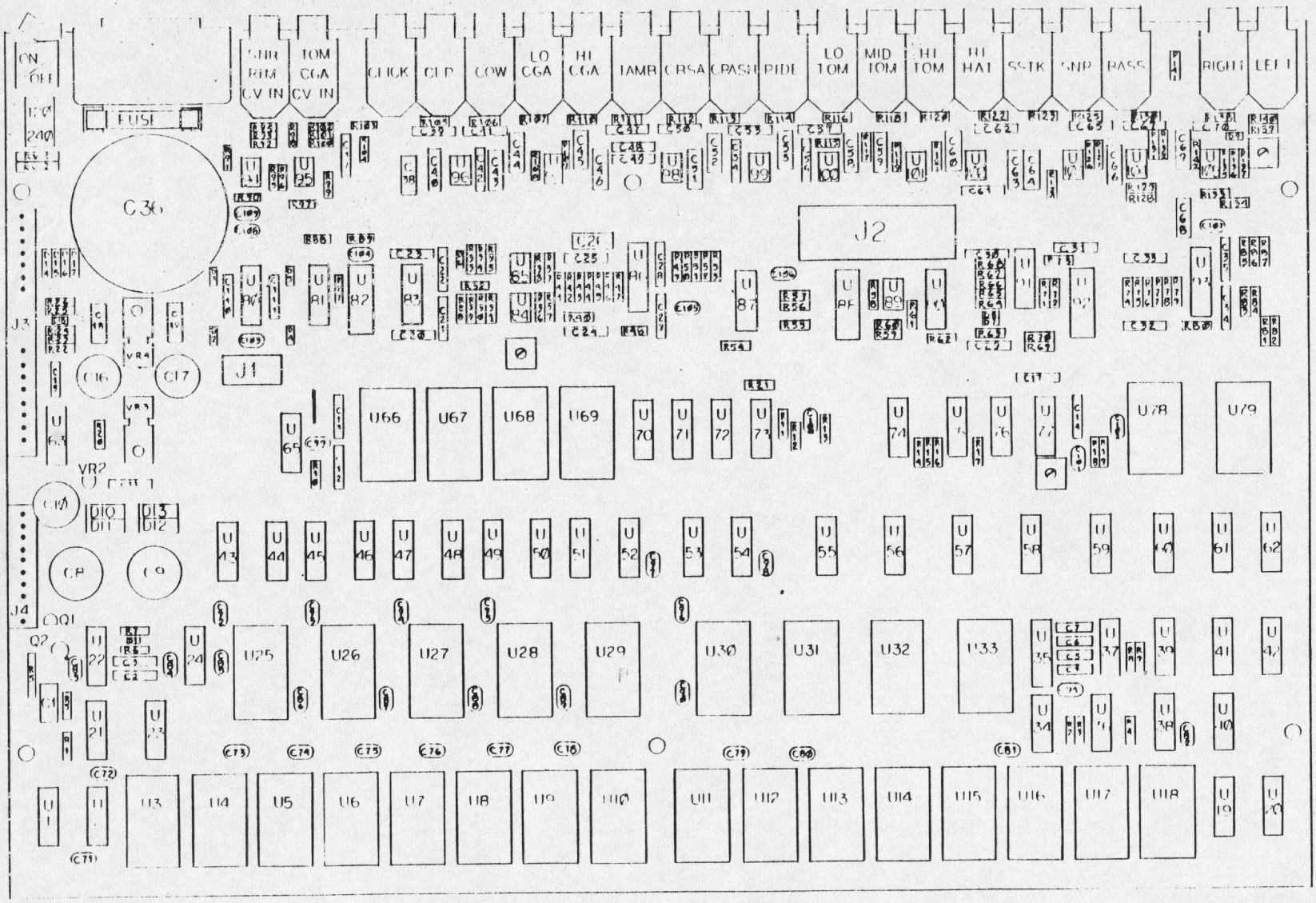


LINN ELECTRONICS
LINN DRUM
MXR BOARD
REV. E 27 JAN 83

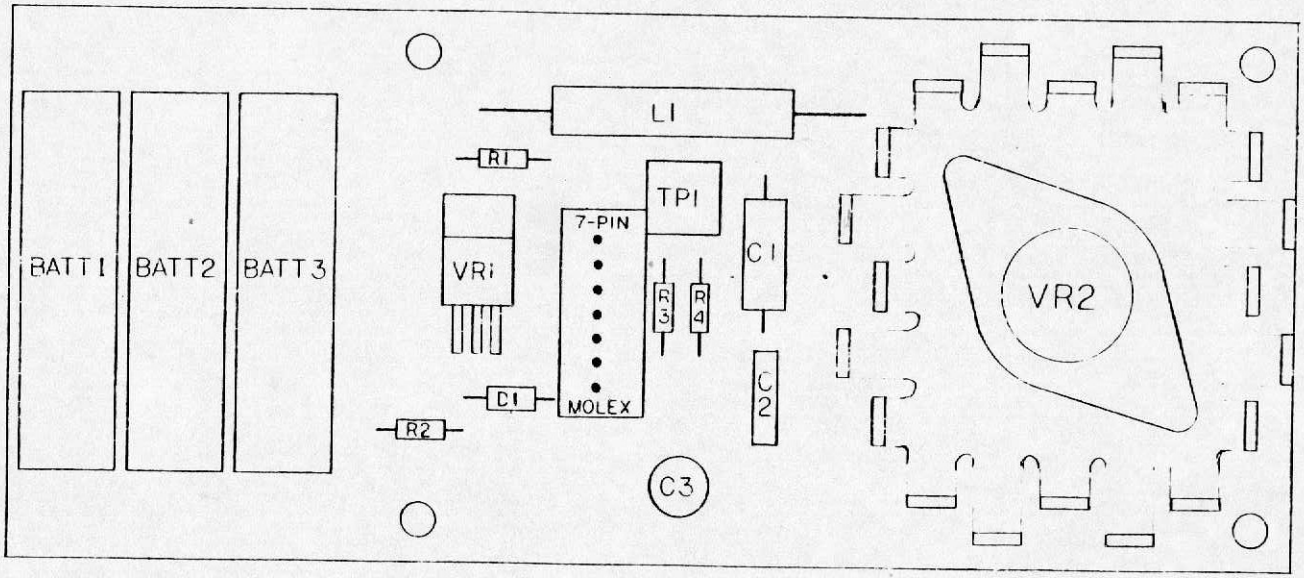


LINN ELECTRONICS
LINNDRUM
MXR BOARD
ASSEMBLY DRAWING REV.B 9FEB85


LINN ELECTRONICS
LINNDRUM
CPU BOARD
ASSEMBLY DRAWING
M REV.A 7 FEB 83
6 PIN MOLEX
4 MHZ XTAL
P1
TRIG 1
TRIG 2
TRIG 3
TRIG 4
TRIG 5
CASS IN
CASS OUT
SYNC IN
SYNC OUT
TRIG OUT
PLAY STOP
TP1
TP2
TP3
TP4
TP5



LINN ELECTRONICS
LINNDRUM
DRUM BOARD
ASSEMBLY DRAWING
REV.A 2FEB83



LINN ELECTRONICS

LINN DRUM

5 VSR BOARD

ASSEMBLY DRAWING

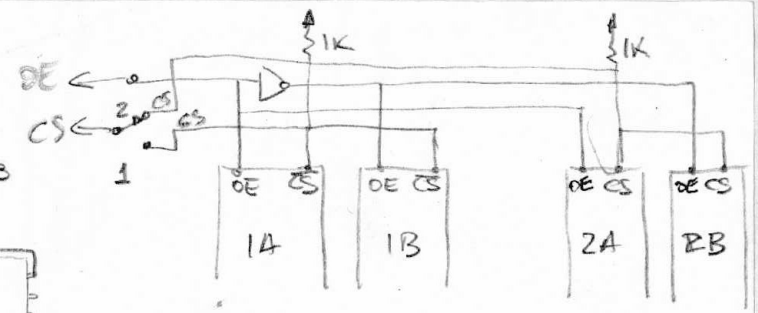
M REV A 8 FEB 83

MEMORIA
ADICIONAL
LINNDRUM

655
360
108

1123

TA TB



ANVERSO