XR3801 Circuit Description and Service Notes

Introduction

These notes are intended to assist maintenance and service of the XR3801 amplifier. It is recommended that reference is made to the relevant schematic diagrams and system diagram whilst reading this document.

The component references of the two amplifier channel electronics are appended “A” and “B” respectively. Shared circuitry (such as that of the protection system) has no suffix. This document will refer to channel A references only. Operation of channel B is identical except where explicitly noted. Voltage values in bold mentioned in the text are test voltages which may be used for diagnostic purposes, although attention is drawn to the surrounding text which explains circuit operation and may qualify such measurements.

Mechanical Construction

The mechanical structure of the unit is made up of two identical side panels, a rear panel, and a 3mm steel structural front panel. The rear panel is fixed to the side panels by means of six M5 screws (three each side) which also secure the two rear rack mounting brackets.

The front panel is fixed to the side panels by means of two side fixing brackets secured to the front by way of the handle screws and to the sides by three M5 screws each side.

The main circuit board is fixed to the two heatsinks by the power device fixing screws and is spaced from the circuit board by way of insulating bushes. The circuit board/heatsink assembly is fixed to the rear and side panels by a total of eight M5 screws.

The mains transformer is supported on the internal “transformer tray” which is fixed directly to the structural front panel.

The extruded cosmetic front panel is fixed directly to the structural front panel by two M5 screws.

Top and bottom covers complete the assembly each fixed in place by eight M4 screws.

Access to all the major components may be gained by removal of the top and bottom covers, further disassembly is rarely required.

Circuit description

Input Stage

The input stage is built around TL071 operational amplifier IC1A, configured as a unity-gain differential amplifier. Its correct operation is dependent upon both of its input terminals being correctly terminated and, therefore, any gain errors around this stage may be a result of a fault in the screened cable connection to the input PCB P1030. Preset potentiometer VR2A adjusts the gain of this stage and thereby provides adjustment to optimise the Common-Mode-Rejection of the input stage. This preset is factory set for optimum rejection and should not be re-adjusted unless it has been necessary to change any components around the input stage.

The trimming procedure is as follows :

Inject a common-mode test signal at 1kHz and +4dBu to the channel under test. The common-mode test signal of the Audio Precision test system is suitable, otherwise connect the signal to both pins 2 & 3 via 51 Ohm resistors. Observe the amplifier output and adjust VR2A for minimum output.

Power for the input stage is derived from the main $\pm$LT supply via 1W resistors R101A and R102A and shunt regulated to a nominal $\pm$18V by D22A and D23A.

The output of the input differential amplifier is fed via 1k “Build-out” resistor R57A and twin screen cable to the front panel level control and the returns via the “blue” core of the same cable to the main PCB to be fed to the power amplifier stage.

Power Amplifier

The power amplifier consists of a fairly conventional Class A driver stage driving a Class AB MOS-FET output stage with Class H supply rail modulation. Each stage will be dealt with individually.

Class A Driver

The input signal returned from the level control is fed via DC blocking capacitor C53A and R59A. DC bias current for the Class A input stage is supplied via R60A, whilst 330pF capacitor C54A prevents any extreme high frequency input signals from reaching the power amplifier and also provides a low source impedance at high frequencies to ensure frequency stability.

The first stage of the Class A driver consists of TR52A and TR53A configured as a long tailed pair differential amplifier. Emitter resistors R62A and R63A de-sensitise the performance of the input stage to parametric variations of the two input transistors. The quiescent current for the input stage is delivered by current source TR51A. Diodes D11A and D12A provide a reference voltage of approximately 1.3V which is applied to the base of TR51A. Approximately half of this **(0.65V) will then appear across R61A** (330R) which then sets the current sourced from TR51A collector at approximately 2mA. In the quiescent state half of this current is driven through TR52A and TR53A. Hence the **voltage dropped across emitter resistors R62A and R63A will be approximately equal at 100mV**.

The collector currents of TR52A and TR53A are fed via R67A and R68A to R69A and R70A respectively. Hence, in the quiescent state, **R69A and R70A should each exhibit a voltage drop of 2.7V** or so.

Overall voltage feedback of the amplifier is derived through R64A and R66A. R65A and C55A connected in parallel with R64A provide phase lead compensation to maintain good amplifier frequency stability, and a fault in either of these components may result in RF signals being present at the output, or in unusually high distortion. C56A connected in series with R66A gives 100% DC feedback to minimise any DC offset at the output. The resultant feedback signal is applied to the base of TR53A.

Under normal conditions the signals at the bases of TR52A and TR53A will be identical. However, under fault conditions, such as a DC offset at the output, the base voltages will become offset also. For example, in the event of a large DC offset of +50V at the output a positive DC voltage will appear at the feedback point and hence at the base of TR53A. Although this would, in theory, be the full +50V, owing to C56A being rated at only 25V, the voltage will, in practice, be somewhat lower. However, the important issue is that the voltage is **positive**. In the event the voltage is negative this indicates that the feedback network is faulty (most likely R64A itself).
The voltage at TR53A base being positive whilst the base of TR52A is close to 0V will then reverse bias TR53A base-emitter hence turning off the transistor. Hence, no voltage should appear across R63A and R70A whilst double the normal voltage will appear across R62A and R69A (200mV and 5.4V respectively). Should this not be the case, it indicates a fault in the input stage itself.

The output of the input long-tailed-pair (i.e. the voltages across R69A and R70A) are fed to a second long-tailed-pair TR56A and TR57A. The bias current for this stage is set by current source TR58A. The base current for TR58A is fed through R72A. TR59A senses the voltage across the emitter resistor of TR58A R77A and “robs” TR58A of base current to maintain approximately 650mV across R77A. Hence the collector current of TR58A is set at approximately 4.3mA which is shared equally between TR56A and TR57A. C58A and C62A provide Miller Feedback around TR56A and TR57A respectively. These capacitors set the dominant pole of the amplifier frequency response, and are therefore critical for amplifier stability. It should also be noted that either of these capacitors becoming “leaky” (difficult to measure in circuit) will result in a DC offset at the output.

The collector of TR57A drives the positive output more-or-less directly (more detail later) whilst the collector of TR56A drives current mirror TR54A/TR55A via R76A. In the quiescent state **R76A will show a voltage drop of around 22V**, and the current mirror emitter resistors **R74A R73A and will show equal voltage drops of 320mV**. Hence, for the same +50V DC offset, described earlier, one would expect no voltage drop across any of R76A, R73A or R74A, indicating that the feedback is attempting to correct the fault. Likewise, for a negative DC offset one would expect these voltages to be twice their usual value. If this is not the case then the second stage (TR54A-TR59A) is at fault.

The loads for TR57A and TR55A are formed by Bootstrapped current sources TR60A/TR61A and TR63A/TR64A respectively. Operation of the two current sources is, in principal, identical so the upper current source TR60A/TR61A only will de described. The load current is sourced from the collector of TR61A, its base being biased through R80A. The voltage across emitter resistor R79A is sensed by TR60A which then “robs” TR61A of base current to maintain a **voltage drop across R79A of approximately 650mV**. This sets the collector current of TR61A at approximately 4.3mA. The current source is connected to the +HT rail via R78A. The current through R78A is the sum of TR61A collector current (4.3mA) and the current through R80A (5mA) and, therefore, **43V will be developed across R80A**. Capacitors C63A and

C64A Bootstrap the current source end of R78A to the output. Therefore, with signal applied, the voltage at this point will be approximately 100V DC with the output signal superimposed upon it.

The outputs of the two current sources TR61A and TR63A are fed through D13A and D14A to vbe multiplier circuit TR62A, which sets the output stage bias. The bias voltage is defined by R81A, R82A and VR1A which is factory preset for the **correct bias setting of 350mV measured between the emitters of TR65A and TR66A**.

Diode/Zener clamps D15A-D18A limit the maximum gate to source voltage applied to the output stage thereby setting a current limit for protection of the output stage. Units fitted with P1042 re-entrant protection daughter boards connect transistors TR1 and TR2 across D16A and D17A respectively. The turn-on of these two transistors is controlled so as to reduce the allowed Gate to Source voltage as the Drain to Source voltage increases, thereby providing closer protection of the output stage.

Emitter followers TR65A and TR66A buffer the Class A driver stage in order to provide more current to drive the output stage. Although the MOS-FET output stage has very high input resistance, requiring little current, the parasitic capacitances will impair its performance without the addition drive current available.

Output Stage

The output stage consists of four tiers of seven output devices connected in parallel. TR8A-TR14A form the negative half of the Class AB output stage, whilst TR15A to TR21A form the positive half. Each device has a gate "stopper" resistor R8A-R21A and a Gate to Drain Miller capacitor C8A-C21A which prevent parasitic oscillation of the output stage.

The supply for the output stage is fed from the ±LT rails (approximately 70V) via D6A and D7A for the positive and negative halves respectively. In addition, the upper tiers of devices TR1A-TR7A and TR22A-TR28A modulate the supply to a voltage approximately 20V greater than the output voltage when the output approaches or exceeds the 70V LT supply. There are two important advantages to this system. Firstly, in the "Off" state the output stage is fed from a 70V supply, which reduces the breakdown voltage requirements for the output stage. Secondly, as the power dissipation in a Class AB output stage is proportional to the square of the supply voltage, for small (-6dB or lower) output signals, the power dissipation is a quarter of what it would be with a conventional design.

The upper tiers of the output stage are driven from TR29A-TR32A, TR37A and TR38A for the positive side, and from TR33A-TR36A, TR39A and TR40A for the negative side. The operation of each half is, in principal, identical so the positive driver only will be described.

The Class H driver consists of two current sources TR29A/TR30A and TR31A/TR32A. TR29A/TR30A operate from the +HT supply and are set to source approximately 2mA. TR31A /TR32A operate from the output signal and are set at 4.3mA. When operating correctly, **650mV will be developed across each of R32A and R33A**. Zener diode **ZD2A is connected between the two current sources and will normally show a voltage drop of 20V**. Zener diode ZD1A is connected between the Cathode of ZD2A and the output of the upper tier of output devices. Hence, in the quiescent state, the **Cathode voltage, with respect to 0V, of ZD1A will be approximately +70V**, and the **Anode to Cathode voltage will be approximately 650mV**. As the two current sources are unbalanced, the lower source will obtain 2mA of its 4.3mA from the upper current source and the remaining 2.3mA of current through ZD1A, thereby biasing the upper tier of the output stage into the off state. As the output voltage increases, less voltage will be dropped across TR32A as it maintains its 4.3mA of collector current. When the output voltage reaches approximately 20V below the +LT rail TR32A will become saturated and the voltage at the Cathode of ZD2A will begin to increase, biasing the upper tier of output devices into the on state. Transistors TR37A and TR38A are configured as emitter followers to increase the drive current available to the output stage. Hence the gate drive applied to the upper tier of devices will follow the output with an additional 20V of DC offset.

Faults in the Output Stage

Output device failure is usually in one of three modes.

A) Device short Drain to Source
B) Device short Gate to Source
C) Device open Drain to Source

Failure mode A) is usually exhibited as a DC offset at the output (or if the device is in the upper tier of devices as the modulated rail being "stuck" at the full ±140V). Such a fault will be revealed as a Drain to Source short circuit across the offending tier of devices. To identify which device(s) is faulty measure the resistance between Gate and Source of each device in the faulty tier with the multi-meter set to its 2kOhm range. A faulty device will show as a resistance measurement of less than 1k1 (usually 0-100 Ohms).

Failure modes B) and C) will be exhibited as premature clipping on one half-cycle of the output. This fault will not, however, be shown with the amplifier unloaded. In the event the fault persists with no load connected, the fault is likely to be elsewhere. Devices suffering from failure mode B) can be easily identified with the simple multi-meter test outlined above.

Failure mode C) is a little more difficult to identify. The simplest method is to connect a "wander" lead to the Source connection of the offending tier of devices. Touch each gate lead of that tier of devices with the "wander" lead in turn observing the output waveform. Each time a device is shorted Gate to Source the clipping will become more pronounced. A faulty device will be revealed by less dramatic additional clipping.

Multimeter Testing of Output Devices

Once a device has been removed from circuit it is comparatively simple to check whether it is operating correctly. The following routine is for an N-Channel (K1058) device. The routine for testing a P-Channel device is identical with Red and Black leads swapped.

Set the Multi-Meter to its 200 Ohm range. Connect the Black test lead to the (centre) Source lead of the device under test and the Red test lead to the (left) Gate lead of the device under test. The meter should show a high (>200 Ohm) resistance reading. Now move the Red test lead to the (right) Drain lead of the device under test. The meter should show a resistance reading <2 Ohms. Briefly touch the Black test lead on the (left) Gate lead of the device and then return it to the (centre) Source lead and check for a high (>200 Ohms) resistance reading. If any of these measurements are not achieved then the device is faulty.

Replacement of Output Devices

Attention is drawn to C Audio Technical Bulletin "MOS-FETs". Output devices date coded 4L3 and on exhibit slightly different self-protecting characteristics from previous production batches. In order to permit use of these devices in this unit a "re-entrant protection daughter board" has been developed (PCBA042). This PCB is fitted to the underside of the main circuit board in two positions (one for each channel). Where an output device of date code preceding 4L3 is replaced with a more recent part, this daughter board must be fitted to the affected channel(s). The fitting procedure is as follows:

1) Remove D16A, D17B, R87A from the circuit board (D16B, D17B, R87B for channel B). Clear the PCB holes of these components.
2) Fit the daughter board by inserting the leads of the vertically mounted 0 Ohm resistors into the PCB holes vacated by the above components, and solder in place. Trim the excess lead.
3) Connect the "flying" 0V lead from the daughter board to the main PCB 0v at R94A/B.
4) The unit may now be tested as usual.

Other Causes of apparent Output Stage Faults

Output DC offsets can be caused by faults outside of the output stage itself. In the event that no Drain to Source shorts are measured at the output stage, it is recommended that the driver stages are checked for correct operation. The fault-finding routine should start at the feedback point, checking the DC fault is reflected at this point, and then progress through the driver stages, checking that the relevant current sources are operating correctly, and that the feedback is attempting to correct the fault.

Premature clipping may also be caused by faults external to the output stage itself. Most often the fault lies within the current protection circuit D15A-D18A. This can easily be confirmed by removing D15A and D18A from the circuit board and observing if the fault clears. Note that, counter-intuitively, a fault D15A will show as a problem on the negative half-cycle, and a faulty D18A will show as a fault on the positive half cycle.

Premature clipping may also be caused by a fault in the Class H driver stage. It is usually difficult to distinguish whether the fault is caused in the Class AB stage or the Class H stage. It is usually best to confirm that all of the output devices are operating correctly, and then eliminate the current limit circuit as outlined above. If the problem persists it is likely to be in the Class H driver. Firstly, correct operation of the current sources should be confirmed by checking for the correct 650mV across the emitter resistors (R32A, 33A, 34A and 35A). It is usually best to also check all transistors for correct operation by measuring Base to Emitter and Base to Collector with a multi-meter set to the "diode check" setting. As both ZD1A and ZD2A can effectively limit the drive to the Class H stage either of these devices being faulty can result in premature clipping.

Output Connections

The commoned Source point of output MOS-FETs TR8A-TR21A is connected to Zobel Network R93A/C69A. This network presents a defined load impedance to the output stage at high frequencies to ensure stability. Either of R93A or C69A being faulty will result in the amplifier oscillating at high frequency, which may also be evidenced by mains "hum" and/or distortion at the output. This signal is fed via output choke L1 which isolates any load capacitance from the amplifier feedback to ensure stability.

The output is then fed through output relay RL1A and thence to the rear panel output connectors.

Protection System

The protection system is based around TR1-TR6. Under normal conditions TR4-6 will be off. At turn-on C116 will charge through R5 towards the +LT supply rail. The voltage is fed to the base of TR3 via D2. When the voltage across C116 reaches approximately 10V TR3 will turn on and thus turn on TR1. Resistor R3 connected between TR1 collector and TR3 base provides positive feedback in order to make the turn-on/turn-off of TR1 more defined. The collector of TR1 is connected via R6 to the coils of relays RLY1A and RLY1B, and is also fed to the soft start PCB in order to activate the soft start system.

Transistors TR4 and TR5 are connected in such a way that a voltage of -650mV applied to the emitter of TR4 will turn on TR4 and hence TR5. This will rapidly discharge C116 and hence turn off TR3 and TR1 thus opening the output relays. Similarly TR6 is connected such that a base voltage of +650mV will turn it on with the same resultant opening of the output relays.

The output of each channel is fed via resistors R112A and R112B into C112 and then via D4 and D5 to TR6 base and TR4 emitter respectively. The combination of C112 with R112A and R112B forms a low-pass filter, and so at signal frequencies C112 will have no voltage across it. In the event of a DC offset appearing at the output, however, C112 will charge to a DC voltage, turning on TR6 or TR4&5 depending upon the polarity, and hence opening the output relays.

The Network consisting of R9, R10 and C10 provides the rapid turn-off feature of the protection system. R10 is connected through the two 90 degree thermal switches to D6 and D7 which are connected to one of the secondaries of the mains transformer. The union of D6 and D7 will, therefore, show a half-wave rectified version of the secondary voltage. This is averaged by C10 to a **negative** DC voltage, reverse biasing D3 and, therefore, having no effect on the protection system. Should one of the thermal switches open, or the power be turned off, C10 will be rapidly charged towards the +LT rail via R9, forward biasing D3, turning TR6 on and opening the output relays.

Power Supply

The amplifier operates from nominal (off-load) $\pm$70V and $\pm$140V supplies. To generate the supplies, the mains transformer has two independent 50 - 0 - 50 secondaries each feeding a full-wave bridge rectifier (mounted immediately behind the mains transformer) and capacitor bank (C41A&B-C44A&B) to provide $\pm$70v outputs. The positive output of one supply is connected to the negative supply of the other to provide the required +140V, +70V, 0v, -70V, -140V supplies.

Cooling

Two cooling fans are provided one for each channel. The fans are 115V ac types and are powered from the transformer secondary feeding the negative supply via 55 degree normally open thermal switches. 1.5uF capacitors connected across the thermal switches provide some series impedance to drive the fans at slow speed before the thermal switches reach their closing temperature.

Soft Start System

The mains input to the unit is fed via the rear panel fuse holder to the "Live" and "Neutral" pins of the P1028 Soft-Start PCB, and thence to the wiper contacts of Relay 1 and Relay 2 respectively. The live feed is also connected to the "Switch" pin and through to the front panel mains switch. When the front panel switch is in the closed "on" position the live supply returns to the PCB and then Via C1 to full-wave bridge rectifier D4-D7 to provide a 80V supply across C3. This voltage is applied to the series load of Relay 1 coil, Relay 2 coil and R2, Q1 being turned on via R3 and R5, thereby bypassing Relay 3 coil, and Q2 being turned off via R4 and R5. Relays 1 and 2 close applying voltage to the transformer secondary via Fuse1 and R1. R1 limits the inrush current surge as the mains transformer core is magnetised.

When the amplifier's internal voltages become established the protection system's power-up delay will release sending a control signal of approximately 48V to the "+Cont" pin of the soft start PCB. This is applied via R7 to Darlington opto-coupler Opto1 whose output then becomes active, turning off Q1 and turning on Q2, thereby applying voltage to Relay 3 Coil. The contacts of Relay 3 close bypassing Fuse 1 and R1, thereby applying the mains supply directly to the mains transformer primary.

Fault-Finding Hints

When powering-up a unit after repair, there is always the possibility that undetected faults will result in further damage when the unit is retested. To minimise the risk of damage it is recommended that the following procedure is adopted.

1) Remove the "+Cont" connection to the Soft-Start PCB.
2) Remove the Soft-Start fuse Fuse 1, and connect a 100W mains lamp across the Fuse 1 position.
3) Power-up the unit in the normal way.

The lamp will initially glow brightly, and then dim down as the internal capacitances become charged. The unit may then be functionally tested with no load connected. Once satisfied that the unit is operating correctly, the mains supply may be applied to the unit as normal, and the unit load tested.

In the event that the lamp does not dim down, this indicates a major fault still exists, which must be remedied before full mains may be applied.

Locating Major faults

Major faults resulting in high current draw (as indicated by the series lamp refusing to dim) can be isolated as follows:

1) The power feeds to each channel are located on the solder side of the PCB, four connections (Red, Pink, Grey, Black) each to the left and right of the mains transformer. These connections should be removed. Should the fault persist, this indicates the fault to be with the mains transformer or bridge rectifiers.

2) The power feeds may now be reconnected to each channel in turn, thereby identifying which channel is at fault.

3) A faulty channel may be isolated to only a few possibilities

i) A faulty power supply capacitor
ii) A faulty output device
iii) A short circuit to the heatsink (either one of the power device cases, or one of the heatsink mounted power diodes.
iv) A short circuit from one of the output device leads or power diode leads to the heatsink.
v) Over-bias of the output stage-check for the correct 350mV between the emitters of TR65A and TR66A.

REAR PANEL MOUNTED

INPUT BOARD

XLR1

XLR2

BLUE

RED

SCR

TO STAR POINT

R50A 1K COAX2SYM

R51A 1K

R52A 9K1

R53A 9K1

C50A 220p

C51A 220p

C33A 10p

R56A 10K

CMOD 100n

R54A 9K76

VR2A 1K

CMRR ADJ

C52A 10p

IC1A TL071

+18

-18

R57A 1K

COAX2SYM

VOL1

20K LOG

C54A 330p

C53A 10u 63V

R59A 2K7

R60A 82K

D11A 1N4148

D12A 1N4148

R58A 39K/1W

GND

R61A 330R

TR51A BF423

R62A 100R

R63A 100R

TR52A 1085

TR53A 1085

R64A 47K

R66A 820R

R67A 10k

R68A 10k

C56A 100u 25V

R7A 22R

C57A 100n

BRIDGE RED

C55A 10p

R65A 1k

103B 47K

R76A 10K

C59A 100n

R73A 150

R74A 150

R75A 47R

C60A 10n

TR54A BF423

TR55A BF423

C58A 33p

C62A 33p

TR56A BF422

TR57A BF422

C61A 100n

R78A 4K7/1W

C63A 100n

C64A 47u 100V

TR60A BF423

R79A 150R

TR61A BF423

D13A 9V1

R80A 39K/ 1W

R81A 2K7

TR62A BF422

R82A 2K

VR1A 1K

IQ ADJ

D14A 9V1

TR63A BF422

TR64A BF422

C65A 47u 100V

C66A 100n

R84A 150R

R83A 4K7/1W

TR65A 2SA2238

TR66A 2SA968

D15A 1N4148

D16A 10V

D17A 12V

D18A 1N4148

R85A 680R

R86A 680R

R87A 1K

C34A 4n7

HT RAIL +

N DRIVE

FEEDBACK

P DRIVE

HT RAIL -

R69A 2K7

R70A 2K7

R72A 39K/1W

TR58A BF422

TR59A BF422

R77A 150R

LED MOUNTED ON FRONT PANEL

CN1/0

LED5 RED

CN1/1

BRIDGE SWITCH REAR PANEL MOUNTED

CN1/0

R13 12K/1W

LT RAIL +

B/O

COAX2SYM

B/I

CN1/1

GND

SMOOTHING AND +-18V SUPPLY

R101A 6K8/1W

+18V

HT RAIL +

D22A 18V

C71A 100u 35V

C73A 47u 160V

C75A 100n

TO STAR POINT

D23A 18V

C72A 100u 35V

C74A 47u 160V

C76A 100n

-18V

HT RAIL -

R102A 6K8/1W

LT RAIL -

FRONT PANEL MOUNT

COMMON

CN1/1

LED PEAK

CHANNEL A = CN1/2
CHANNEL B = CN1/5

D19A 1N4148

R92A 2K7

TR67A BF423

C68A 100n

R88 4K7/1W

R90A 1K

R91A 390K

TR68A BF422

R89A 4K7

C67A 10u/63V

LT RAIL -

FEEDBACK

LT RAIL+

R96A 510K

D20A 30V

C70A 1u/63V

R99A 1K5

TR70A BF423

R97A 10K

TR69A BF422

D21A 1N4148

R98A 10K

R100A 560R

CHANNEL A = CN1/3
CHANNEL B = CN1/4

SIG

CHANNEL A = CN1/3
CHANNEL B = CN1/4
MOUNTED ON FRONT PANEL

C69A 33n

R93A 10R/2.5W

10R R95A

L1A

R94A 220K

GREEN

GROUND

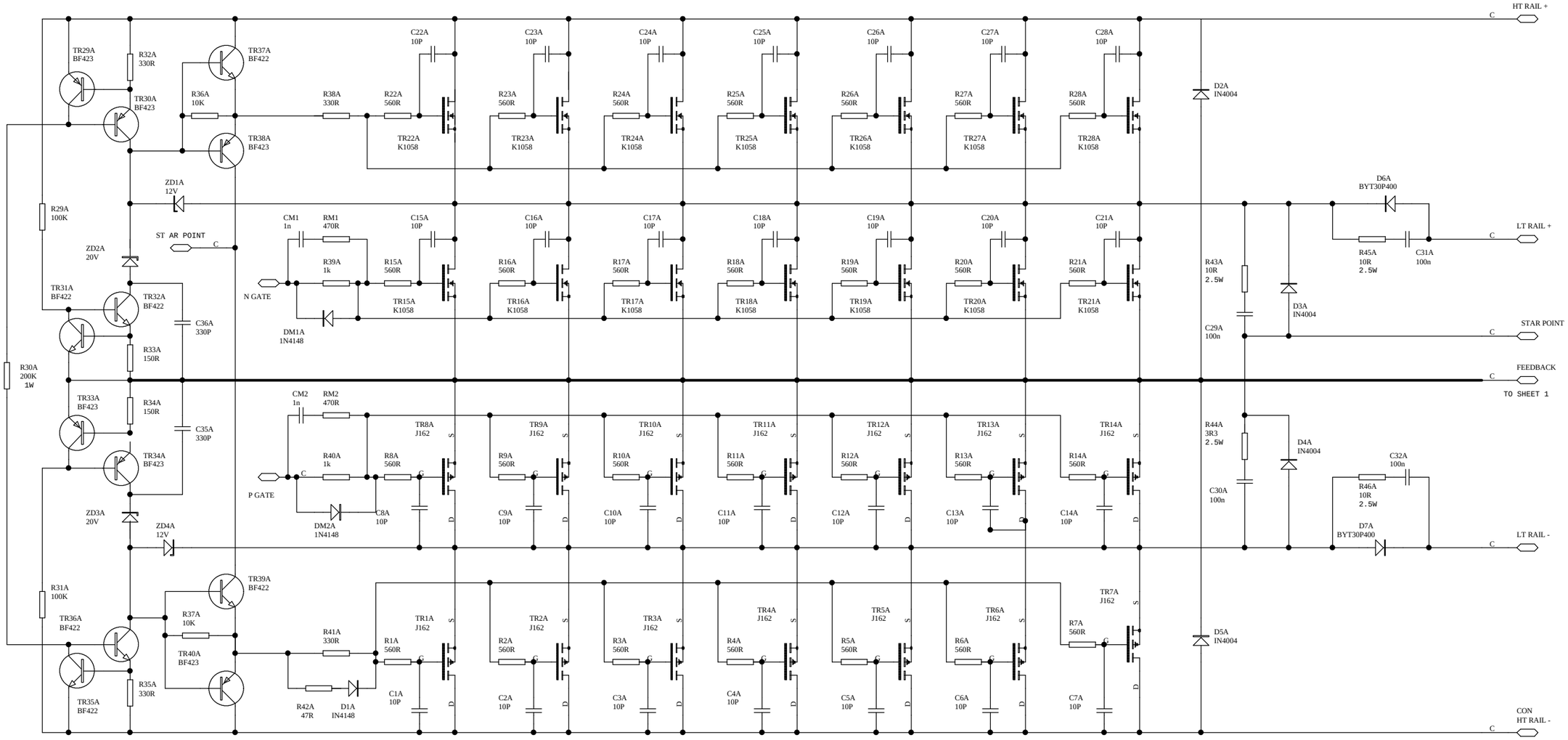
OUTPUT

YELLOW

XR3801 DRIVER CHANNEL A
CHANNEL B IS THE SAME EXCEPT FOR THE
COMPONENT DESIGNATOR WHICH IS SUFFIXED
A OR B ACCORDINGLY

SHEET 1

Title	**XR3801 DRIVER STAGE**		
Size A2	Number **C1027**		Revision 1
Date: 12-Jul-1999		Sheet of 1 4	
File: D:\PROTEL\XR3801\XR3801DR.S01		Drawn By: L BASHAM	



SHEET 2

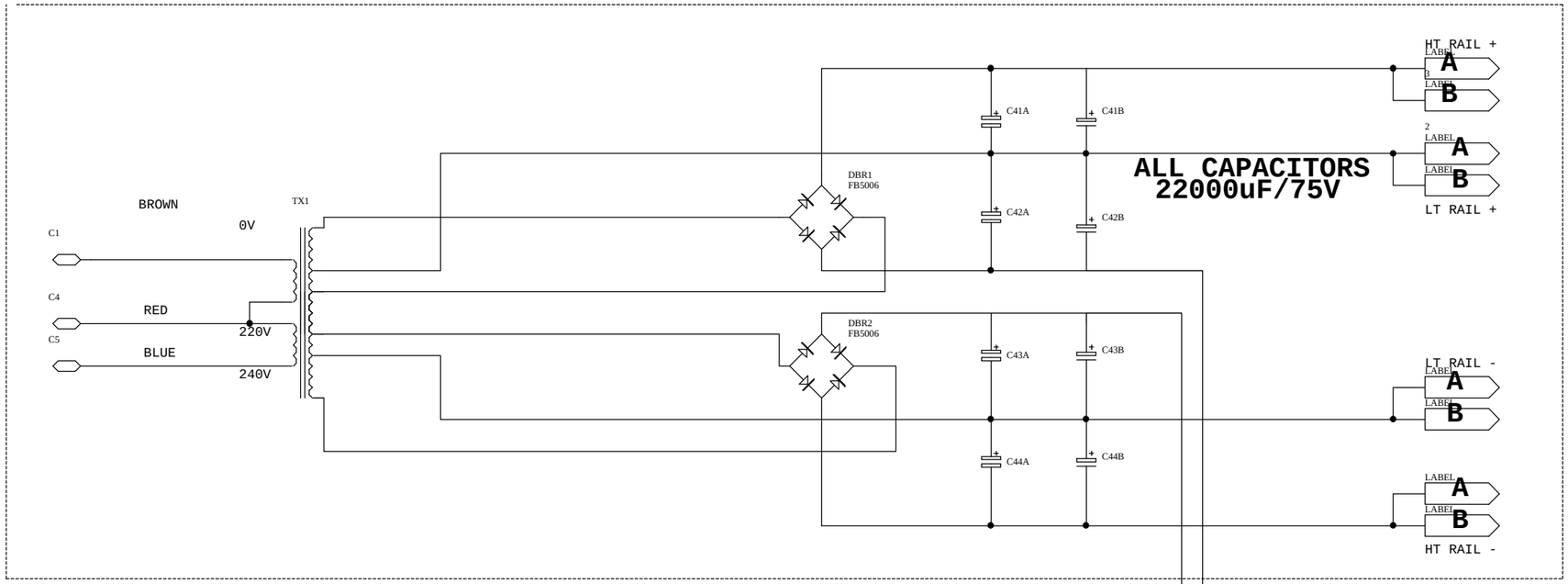
DRAWING SHOWS CHANNEL A OUTPUT STAGE

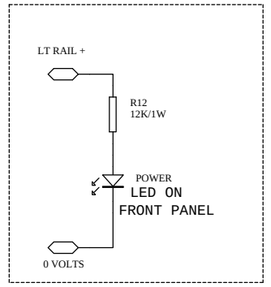
CHANNEL B HAS SAME COMPONENT NUMBERS

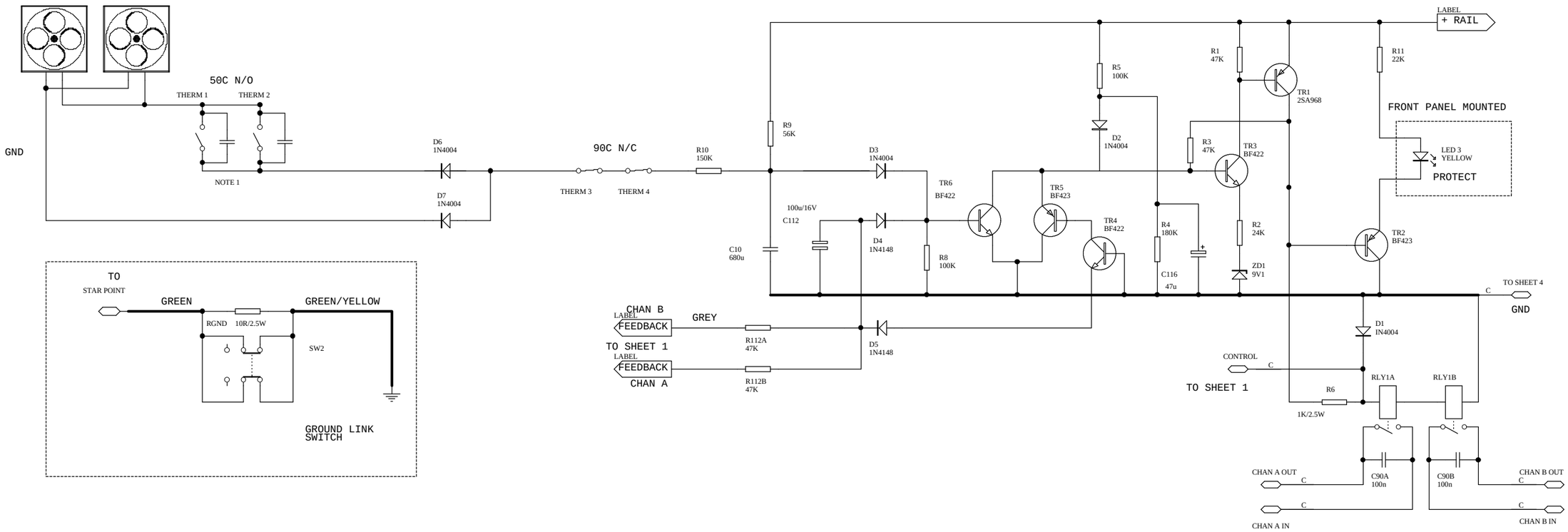
BUT WITH THE SUFFIX B

Title	XR3801 OUTPUT STAGE		
Size C	Number C1027		Revision 1
Date: 12-Jul-1999		Sheet of 2	4
File: D:\PROTEL\XR3801\XR3801OP.S01		Drawn By:	L BASHAM

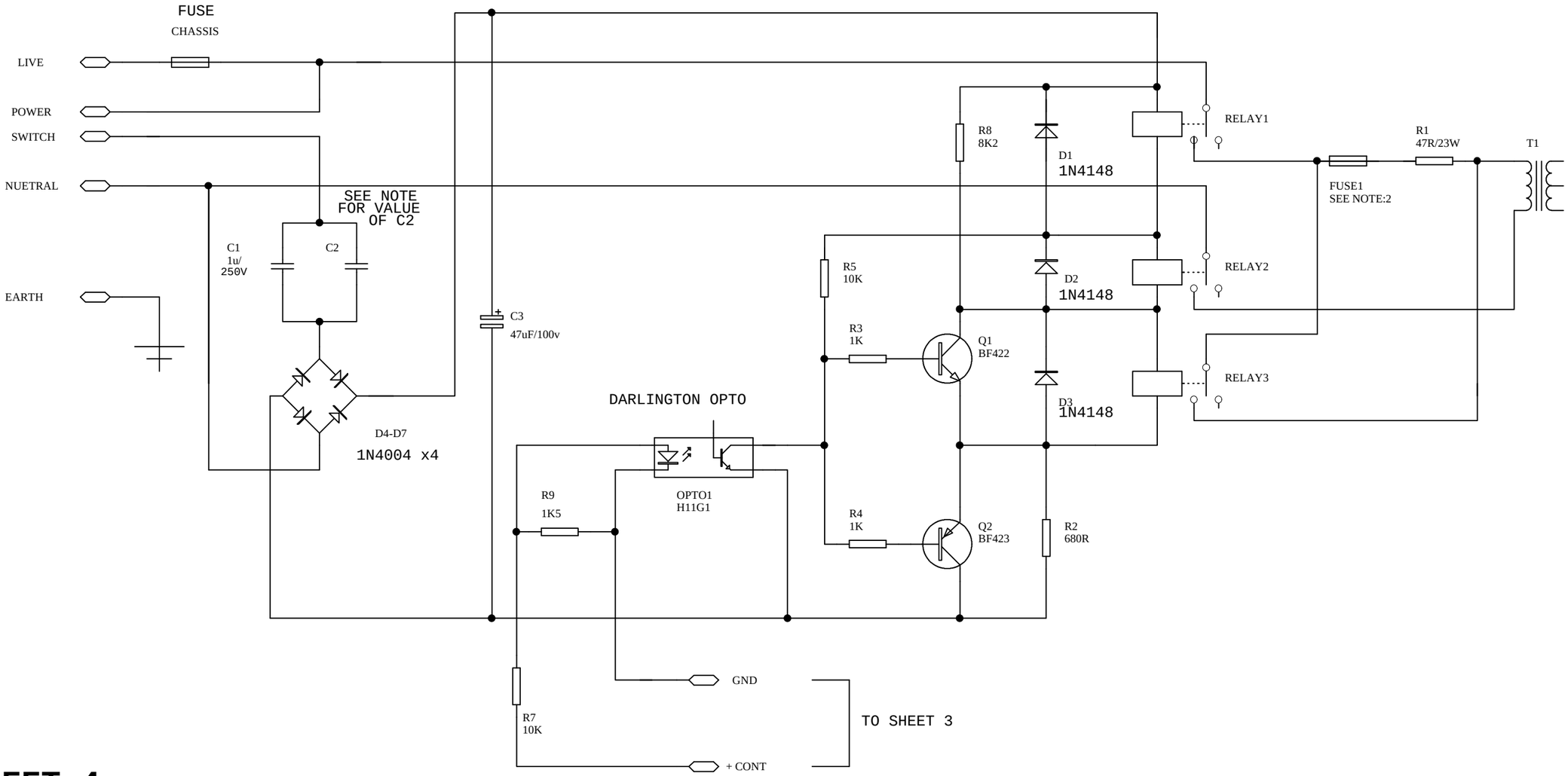
SHEET 3







Title:	XR3801 POWER/PROTECT		
Size: A2	Number: XR3801PWR	Revision: 1	
Date: 12-Jul-1999		Sheet of 3	4
File: D:\PROTEL\XR3801\XR3801PW.S01		Drawn By: L BASHAM	

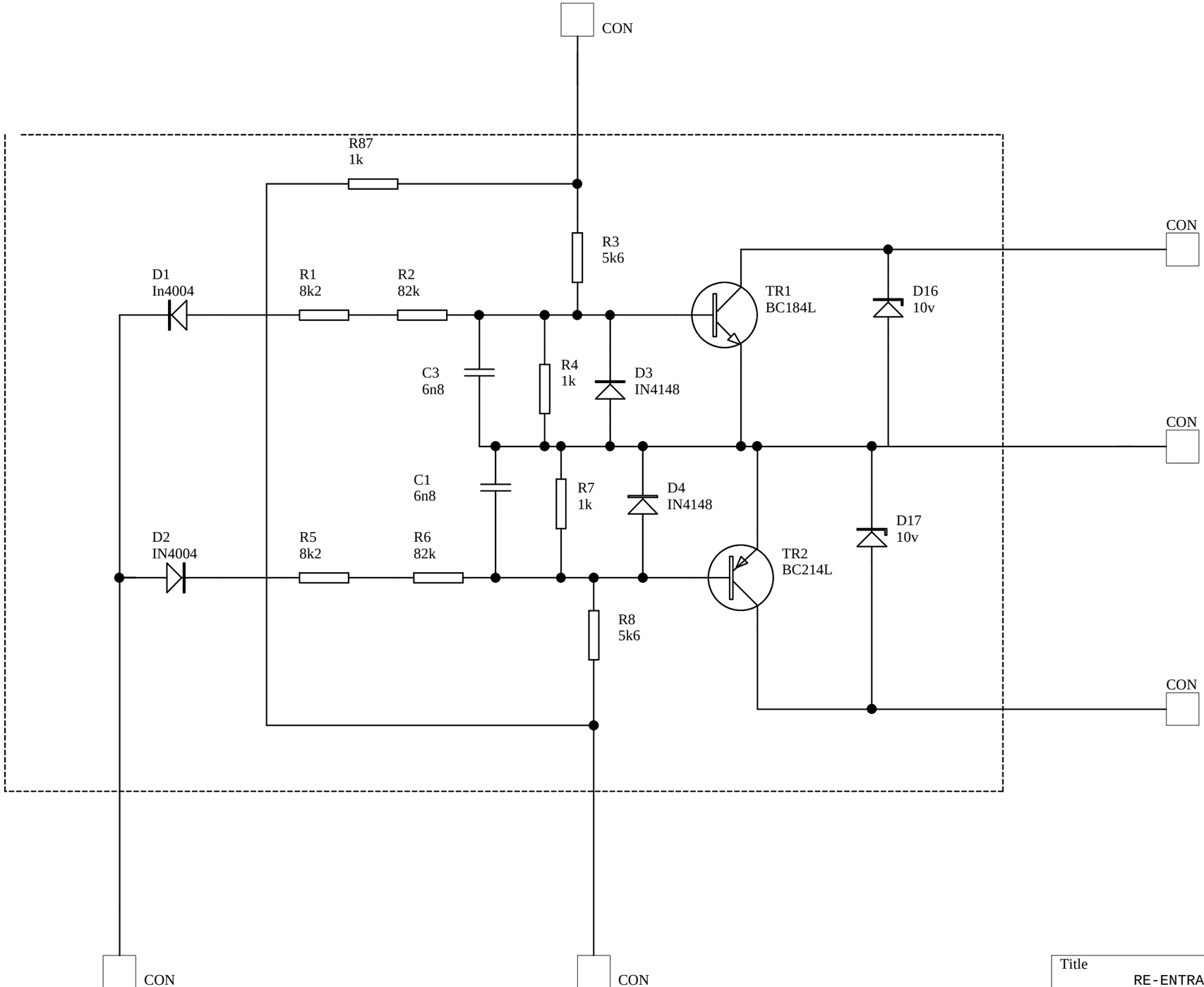


SHEET 4

NOTE:1
C2 IS ONLY FITTED WHEN UNIT IS USED ON 100/120V SUPPLY, ITS VALUE BEING
THE SAME AS C1 1u/250V

NOTE 2:
SOFT START FUSE = 1.6A FAST BLOW
WITH AN I^2t RATING OF 5.2
RS PART# 416-326

Title: C-AUDIO	XR3801 SOFT START		
Size: A3	Number: CA1027	Revision: 1	
Date: 12-Jul-1999	Sheet of 4 4		
File: D:\PROTEL\XR3801\XR3801SS.S01	Drawn By: L BASHAM		



Title	RE-ENTRANT PROTECT ION PCB		
Size A4	Number PCB1042/P1		Revision
Date:	12-Jul-1999	Sheet of	1 1
File:	D:\PROTEL\XR3801\XR3801MO.S01	Drawn By:	L BASHAM