ALESIS
MidiVerb 3 (M3)
Service Manual

P/N: 8-31-0014-A

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Preface

This document is intended to assist the service technician in the operation, maintenance and repair of the Alesis device. Together with the User Reference Manual, this document provides a complete description of the functionality and serviceability of the Device. Any comments or suggestions you may have pertaining to the document are welcome and encouraged.

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The arrowhead symbol on a lightning flash inside a triangle is intended to alert the user to the presence of un-insulated "dangerous voltage" within the enclosed product which may be of sufficient magnitude to constitute a risk of electric shock to persons.

The exclamation point inside a triangle is intended to alert the user to the presence of important operating, maintenance and servicing instructions in the literature which accompanies the product.

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CAUTION: The product under service may employ the use of a replaceable fuse. Danger of fire or electrocution if fuse is incorrectly replaced. Replace with only the same type or equivalent type recommended by the equipment manufacturer.

Regarding the Internal Battery

CAUTION: The product under service may employ the use of a internal battery. Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instruction.

Safety Instructions

Carefully read the applicable items of the operating instructions and these safety suggestions before using this product. Use extra care to follow the warnings written on the product itself and in the operating instructions. Keep the operating instructions and safety suggestions for reference in the future.

1. Power Source. The product should only be connected to a power supply which is described either in the operating instructions or in markings on the product.

2. Power Cord Protection. AC power supply cords should be placed such that no one is likely to step on the cords and such that nothing will be placed on or against them.

3. Periods of Non-use. If the product is not used for any significant period of time, the product's AC power supply cord should be unplugged from the AC outlet.

4. Foreign Objects and Liquids. Take care not to allow liquids to spill or objects to fall into any openings of the product.

5. Water or Moisture. The product should not be used near any water or in moisture.

6. Heat. Do not place the product near heat sources such as stoves, heat registers, radiators or other heat producing equipment.

7. Ventilation. When installing the product, make sure that the product has adequate ventilation. Improperly ventilating the product may cause overheating, which may damage the product.

8. Mounting. The product should only be used with a rack which the manufacturer recommends. The combination of the product and rack should be moved carefully. Quick movements, excessive force or uneven surfaces may overturn the combination which may damage the product and rack combination.

9. Cleaning. The product should only be cleaned as the manufacturer recommends.

10. Service. The user should only attempt the limited service or upkeep specifically described in the operating instructions for the user. For any other service required, the product should be taken to an authorized service center as described in the operating instructions.

11. Damage to the Product. Qualified service personnel should service the unit in certain situations including without limitation when:
    a. Liquid has spilled or objects have fallen into the product,
    b. The product is exposed to water or excessive moisture,
    c. The AC power supply plug or cord is damaged,
    d. The product shows an inappropriate change in performance or does not operate normally, or
    e. The enclosure of the product has been damaged.

1.0 M3 GENERAL DESCRIPTION

The M3, and other digital effects processors, achieve their results by slicing analog signals into segments, and then converting them to a numeric value, corresponding to the amplitude of the signal at that particular instant. These values are then mathematically manipulated, and stored at various locations in a memory "loop" for eventual playback. By varying the placement and amplitude of incoming samples, discrete time delays are achieved. When mixed together, and converted back into analog, these delays simulate the reflections associated with natural reverbs, and delays, as well as non natural effects such as reverse reverbs, and gated reverbs. The added capabilities of an 80C31 micro controller allow for user manipulation and storage of algorithm parameters, as well as effects such as chorus, and flange, that require real-time manipulation of algorithms. Please note that there are several different board revisions, so differences will be noticed from unit to unit.

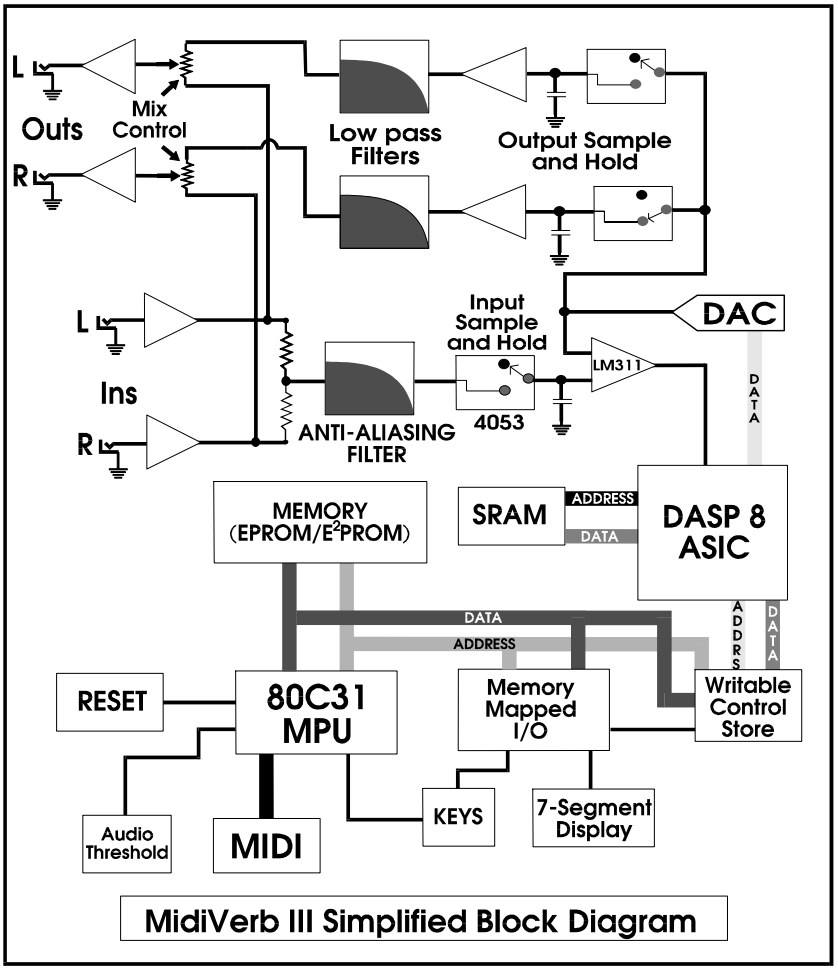


Diagram 1

2.0 POWER SUPPLY

The power supply begins with the 9 Volt, A.C., adapter. Input from J7 is R.F filtered (or bypassed in some units) by the large torroid and C68. From there it is split for the +12V, -12V, and +5V rails. The +12V rail consists of a voltage doubler (C69, C73, and 2 diodes), a filter cap (C81) a 7812 regulator (VR1), and filter capacitors (C7, C72, and C80). The -12V rail is a "mirror" of the +12V rail, consisting of voltage doubler (C70, C74, and 2 diodes), a filter cap (C83), a 7912 regulator (VR2), and filter capacitors (C6, C40, C71, and C82). The +5V rail consists of a rectifier diode, filter capacitors (C75-C78, and C84), a 7805 regulator (VR3), filter capacitor (C85), and many 0.1uF bypass capacitors.

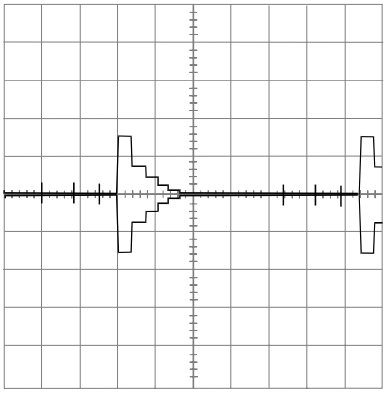
3.0 ANALOG SIGNAL PATHS

The inputs (stereo) from J1 and J2 pass through the small toroids for RF suppression (bypassed in some units), A.C. coupled (C1, C2) and have their impedances fixed at 1M by R2 and R3. While operating the unit monauraly, the input impedance fixed at 500K (R2, and R3, in parallel). From there, the inputs are buffered by U1, and passed through the input potentiometers. The stereo signal is then sent to a X10 gain stage (U1 etc.) and on to the dry side of the mix potentiometer, as well as summed to mono (Via R21, R22).

The summed stereo signal is sent to the anti-aliasing filter consisting of most of U4, and associated resistors and capacitors. There are several important features in the filter to be aware of. The first is the use of the LSTMSB (See section 4.5 for a description) signal from the ASIC. This signal is injected into the signal path at U4 pin 12. A signal diode at U4 pin 10 limits the incoming signal to 5V, preventing damage to the analog switch (U6). The output of U4 pin 8 has a tap running to R46, a 2N4401 transistor, etc., and eventually on to an 8031 input port (U27 pin 13) where it is used to detect the audio threshold level necessary for triggered flange and gated reverb.

The input sample and hold circuit consists of 1/3 of the 4053 analog switch (U6B), the input sample cap (C29), a buffer amplifier (U4), and a comparator (U5). Also note the differential amplifier (R44, R52, R53, 2 signal diodes, 2 NPN transistors) just prior to the comparator. This diff-amp speeds up the response time of the comparator.

The signal beyond this point is purely digital, until the DAC output cycle of the DASP 8. At the appropriate time, the DAC will output the processed left, and right signals. This action is coordinated with the two output sample and hold circuits (U6A&C, 2 op amps of U3, C22, C23), so that each receives the correct, separate signal for stereo output. After passing through low pass (anti aliasing) filters (2 op amps of U3, Misc. Resistors & Capacitors), the signals are buffered (2 op amps of U2), and sent through the output potentiometers. From here, they pass through unity gain amps (2 op amps of U2), through impedance fixing resistors (R5, R10) and R.F. suppression toroids, to the output jacks (J3, J4).



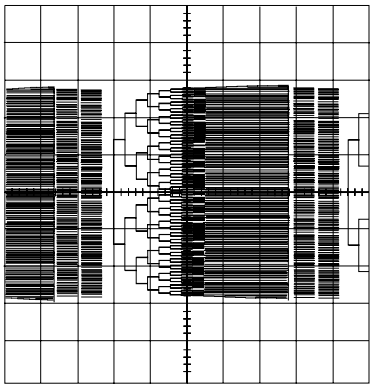
U10 pin 19/20 **1V/Div. 5uS/Div.**

M3 "Typical" DAC output w/ inactive SAR

Diagram 2

3.1 SUCCESSIVE APPROXIMATION

Successive approximation is an empirical approach to the process of analog to digital conversion. The idea is to divide the process into short, manageable sections. Each significant binary weight (starting with the Most Significant Bit) is taken in turn, thus requiring only 16 comparisons to achieve a final value.



1V/Div 5uS/Div **U7 Pin 20**

M3 "Typical" DAC output w/ fully active SAR

Diagram 3

The process begins with the input "sample and hold" circuit. 1/3 of the 4053 (U6B) is turned on, allowing the input sample capacitor (C44) to charge [or discharge] to the level of the current input signal. When the switch is turned off, the capacitor will hold that level indefinitely [barring internal leakage]. At this point, the SAR (Successive Approximation Register-part of the DASP 8 ASIC) will take over. Starting with the MSB, the SAR will set the bit, and compare the output of the DAC, to the level of the input sample capacitor (via comparator U5). The results of the comparison are stored in the register, and the next most significant bit is

compared. This process continues until a value is found for all 16 bits, and the data is ready for further processing by the ASIC. In order to see these signals properly on the scope, it will be necessary to use an external scope sync (use U6, pin 9 as the sync source). Diagrams 2, and 3, show the DAC output during a single SAR cycle, with no input, and full input.

4.0 DIGITAL SIGNAL PATHS

The digital portion of the M3 is somewhat complex, incorporating 2 data and address busses, as well as the control circuitry necessary for intercommunication.

4.1 80C31 MICRO CONTROLLER CIRCUIT

The 80C31 MPU controls all "user interface" functions of the M3. These functions range from handling the front panel buttons, to continuously updating algorithm information to the DASP 8 ASIC. Note that the 8031 data buss serves a dual purpose. This buss multiplexes between low order addresses (1st 8 bits), and data. Latch U26 is used to hold the low order address half, during 8031 read and write cycles. The EPROM (U25) is used to hold both program information, and algorithm data. The E^2PROM (U24) holds system variables, as well as user preset data. MIDI I/O is handled through the 8031's built in RXD (Read Serial Data), and TXD (Transmit Serial Data) ports. Front panel keypad decoding is handled through a combination of memory mapped I/O (see section 4.3), and the 8031's built in I/O ports.

4.2 RESET

The 8031 reset circuit is perhaps the single most important circuit in the M3. When this circuit is functioning incorrectly, a complete lock-up of the machine, will occur. A thorough knowledge of the operation of this circuit will greatly facilitate troubleshooting this unit. Note that the first units released did not incorporate the full reset circuit described below. These units used a simple resistor/capacitor circuit, and would occasionally fail to reset (particularly if the unit was turned off, and then back on rapidly). Most of these early units have been retrofitted with an extra board containing the newer reset circuit. The newest board revisions incorporate the reset on the board.

On power up, the 2N4401 transistor is off (the raw supply hasn't raised up far enough yet to bias the transistor on, through R202, R203, and the zener divider network). C100 is allowed to charge to +5V via R201 and the 1N914 signal diode. When the raw supply reaches approximately 7 volts, the transistor will turn on, discharging C100 through R200, and dropping the reset line low.

4.3 MEMORY MAPPED I/O

The M3 utilizes a memory mapped I/O system in order to deal with the wide variety of functions that the 8031 needs to access. During write cycles of the 8031, data on the 8031 data buss is made available to a series of latches (U12, U22, and U23). When A15 (address's most significant bit) is active, the 3 to 8 line demux (U35) is used to decode several other significant address lines, and send a strobe to the clock input of one of these latches. Consequently, data can be "stored" into a latch simply by writing a value into a nonexistent memory location. Memory mapped input works much the same. The address lines are again decoded when A15 is active. This time however, instead of strobing a clock line, the output enable of the selected latch is strobed, placing it's information on the data buss. The 8031 can then read the data for use as necessary.

4.4 WRITABLE CONTROL STORE

The writable control store is definitely the most complex circuit in the M3. The purpose of this circuit is to act as a mutually accessible (8031 and DASP 8) storage area for the DASP 8 "control" programs. This allows the 8031 to manipulate algorithms in real-time. Because the two devices operate asychronously a great deal of control logic is necessary to prevent buss conflicts. Timing is

so critical throughout this circuit that parts that are even slightly out of spec will cause failures. This is due to the fact that propagation delay times are not only significant, but inherently part of the design. If the logic seems a bit confusing at first, it helps to remember that many of the target signals are active low.

The M3 also utilizes a double buffering system to ensure smooth operation. (i.e. the ASIC reads it's instructions from bank A while the 8031 writes to bank B. At the end of the of the current sample period, the banks are switched.).The "FLIP" bit is used to keep track of this. Once the 8031 has finished writing a control program into the SRAM, it toggles the FLIP SeND (U21 pin 12) line. It can then poll FLIP ReCieVe (U20 pin 9) to determine when the flip actually takes place (the end of the current sample, when ASIC A7 goes from high to low, strobing the positive edge triggered clock of U21B {pin 11} via U18 {pins 1, 2, and 3 wired as Inverter}). All leftover SRAM space is used for the 8031 to store variables for it's own use.

There are three states of operation.

- ASIC Reads from memory
- 8031 Reads from memory
- 8031 Writes to memory

In all of these operations the DeLaYeD 6MHz clock determines which device will be controlling the SRAM. Any time that DLYD 6MHZ is low, the ASIC has control. When asic clock is high, the 8031 is allowed to access the SRAM. DLYD 6MHZ is derived from the 6MHz clock via U16 1A & 1B. In this configuration, the only difference between the 6MHz clock and DLYD 6MHZ is the propagation delay of U16. This is done to ensure that data and address lines have had time to settle before the SRAM is accessed. U13-U14 are used to multiplex between the ASIC and 8031 address busses and are switched directly by DLYD 6MHZ. Note that all access to the SRAM from the 8031 is memory mapped (see section 4.3 for a description of the process).

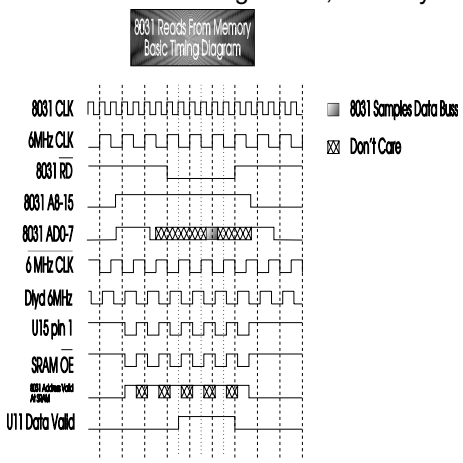


Diagram 4

4.4.1 ASIC Reads From Memory

Since the ASIC only needs to read memory, the logic is very simple. Anytime that DLYD 6MHZ is low, the SRAM's output enable (OE pin 20) is guaranteed to be low (when pin 5 of U18 goes low, it's output will go high, and U18 {pins 8,9, and 10} invert it to a low). At the same time The SRAM's Write Enable line (pin 21) is guaranteed to be high (U16 is always in the "A" position, and input 2A (pin 5) is tied high. A0-A7 are presented to the SRAM directly from the ASIC. At this point the U15 A/B select line (pin 1) is guaranteed to be high (via U16 4A) so that A9-A10 are guaranteed to be low (via U15 3B and 4B). A8 depends on the state of the FLIP bit arriving from U20 (pin 9) via U16 switch 3 (pins 9, 10, and 11), and determines which "bank" the ASIC is currently reading from. The SRAM data buss can now be read by the ASIC normally.

4.4.2 8031 Reads From Memory

8031 reads from memory begin as any normal read would. The 8031 sets up the address the address buss (see section 4.1 for details) and presents it to the SRAM via U26 (A0-A7) and U15 (A8-A10). If the address is memory map decoded by U17 to indicate access to the SRAM, it sets up a chain of events. Diagram 4 shows the basic timing of these events. U18 (pins 4, 5, and 6) ensures that the read assertion of the 8031 only passes through to the SRAM during the low half of DLYD 6MHZ (Diagram 4 SRAM OE). Latch U11 is output enabled as soon as 8031 ReaD is asserted, and now controls the 8031 data buss. The actual data on the buss however, won't be valid until the 6MHZ line goes high (Diagram 4 U11 Data Valid). The latch ensures that data is good when the 8031 samples the buss (latches the contents of the buss into itself) even though the SRAM itself may be busy with the ASIC.

4.4.3 8031 Writes to Memory

Writing to the SRAM from the 8031 is a little trickier. Diagram 5 shows the basic timing of these events. The process again begins as a normal 8031 write to memory. The address will be presented to the SRAM when appropriate. The write assertion from the 8031 will clock the data to be written into U12, but U12 will not be output enabled until allowed by DLYD 6MHZ. The complications arise when actually asserting the SRAM WE line. Observe that the WR WCS is not only used to latch the data from the 8031 into U12, but it is also sent to the D input of flip-flop U20A (pin 2). Normally the Q output of this device is high (as it is constantly being reset by DLYD 6MHZ), but when WR WCS goes high, it will be clocked into the flip-flop with the next low-high transition of DLYD 6MHZ (after a little propagation delay provided by U15/switch 2). At this point Q is low. This low signal then passes through U16 (pins 6 and 7) and on to the SRAM WE. This however doesn't last long, as the next high-low transition of the 6MHz clock switches the U16 to the A inputs. Since U16 switch 2A is tied high, the low signal to the SRAM WE is removed (allowing the ASIC control again). Shortly after this, the DLYD 6MHZ line will again go from high to low, resetting U20A and returning Q to it's normal state.

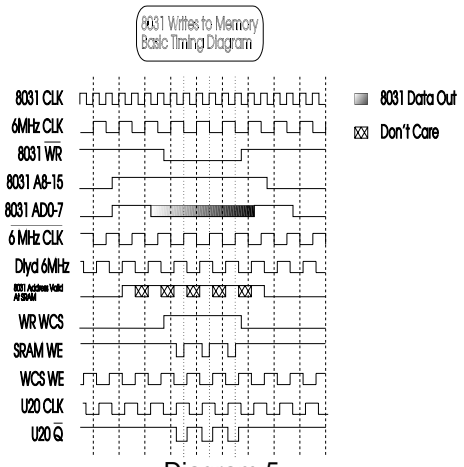


Diagram 5

4.5 DASP 8 ASIC

The DASP (Digital Audio Signal Processor) 8 ASIC (Application Specific Integrated Circuit), is a complex, LSI IC designed specifically to handle the specialized needs of digital effects processing. Obviously, a full discussion of this device is beyond the scope of this manual, however, a brief introduction to the device is definitely in order.

The DASP 8 contains a SAR (Successive Approximation Register), a writable control store (internal memory for algorithm storage), and a RISC (Reduced Instruction Set Computer) for use as an Arithmetic Logic Unit. Memory management hardware, and a variety of control hardware round out the package. Some important control signals are outlined below.

Signal	Pin	Function
OE	12	SRAM output enable.
CLK	51	- 6MHz clock
RST	50	- RESET
INH	46	- Controls sample and hold circuit timing.
LSTMSB	48	- This signal indicates the last state of the MSB (the sign bit in two's complement math). Note at this point that there are two different ASICs. One is made by Fujitsu, the other by AMI. The circuitry will vary depending on which manufacturers ASIC is used. This signal, in conjunction with either R250, or R57-R59, and the 2N4401 transistor, +C39 is used to bias the incoming analog signal slightly positive, or negative, depending on the result of the last DAC cycle (i.e. if the last DAC cycle started off with a negative value, LSTMSB will be 1, causing the input to the sample and hold circuit to pull slightly positive. On the next cycle, the reverse will occur). This reduces any audio pop during the attack portion of the input signal, and allows for a faster response to small signals.
ADC	49	- A/D comparison input.
OVFL	47	- This signal indicates a math overflow condition, and consequently turns on the clip LED circuit.
WE	11	- DRAM write enable

5.0 TEST PROCEDURES

If possible, user data should be saved (a DataDisk is recommended) prior to any servicing. This, of course, may not always be possible (i.e. dead power supply, bad reset signal, corrupt data, etc.). Saving user data may also be accomplished after unit functionality is restored (i.e. power supply, or reset line, is repaired), and prior to further servicing, and testing. The unit should always be reinitialized (power unit up while holding "INT PROG" and "STORE" buttons down) after changing the EPROM, or SRAM. To perform the M3's self diagnostics plug a MIDI cable between MIDI in, and MIDI out. Power up the unit while holding the "INT PROG", and "CONFIG", buttons down. The unit will then test ROM, RAM, Button LEDs, MIDI, and the clip LED. In the event of a #1 ROM, #2 RAM, or #3 MIDI failure, the unit will stop, and the display will show "ERROR #".

6.0 UPDATES AND CORRECTIONS

6.1 CABLES

Check all connector cables are firmly seated. In some cases, they can come 1/2 way off.

6.2 U17

If U17 (74HC139) is a type made by National semiconductor, it should be replaced with a type made by TI. Problems with this device range from distorted audio, to no display, or a complete system lockup.

6.3 RESET

The original design for the MidiVerb III called for a simple reset circuit cosisting simply of a resistor and a capacitor. Shortly after the release of the product, it was found that this simply wasn't enough (if the unit was turned off, and then turned back on rapidly, the unit would occasionally fail to reset). The circuit was redesigned to provide a more stable reset signal (see section 4.2). At this point, a small PC board was created to take the place of the orginal. These will be found screwed down to the regualtor heat sink (it makes for a convinient ground). Later, the circuit was incorporated into the main PC Board. We believe that most, if not all of the original boards that went out have been retrofitted, so their occurance in field should be extremely rare.

6.4 Power Choke

Two items regarding the R.F. chokes in the power supply. Some chokes were found to have broken loose during shipping. These should be affixed to the main PCB (we recomend using hot glue). It is also possible for the choke to short to the case top (which is grounded). A small piece of electrical tape on the case top, above the choke, or hot glue applied in a thin layer to the top of the choke should alleviate this situation.

7.0 HELPFUL HINTS & COMMON PROBLEMS

Troubleshooting a complex device, such as the M3, can range from the simplicity of looking, seeing, and reseating a loose cable, to examining complex timing relationships of data and control, and replacing the "slightly" bad latch. The chart on the following page was created in an effort to relieve the beleaguered technician from having to "discover" some of the common faults we have seen. Please note that we only cover the most likely causes, not all of them.

Customer Complaint	Possible Failure	Possible Action
No Power, No Lights, No Life	Blown DASP 8 ASIC.	If this IC is extremely hot, to the touch, then it is faulty.
	Bad +5V rectifier diode (D22)	The cathode should read roughly 10V (with some ripple). It has been noticed that 1N4001 seem to have problems, and since then have started using 1N4003 diodes exclusively.
Unit lights up, but there is no LCD Display. Unit locks up.	Bad Reset circuit.	Check reset (U32 pin 9), both during power up, and down. Troubleshoot if necessary.
	Bad 80C31.	Replace, and re-test.
	Bad 24MHz Crystal (Z1).	Some crystals are shock sensitive. Tapping on the crystal can sometimes reveal this.
	Bad LCD.	Replace and re-test.
	Bad LCD cable.	Replace and re-test.
No Memory.		
	Bad reset circuit.	Check reset (U32 pin 9), both during power up, and down. Troubleshoot if necessary.
Distorted audio.	Bad power supply rail.	Check PS rails, and troubleshoot if necessary.
	Faulty DASP-8 ASIC.	Replace and retest.
	Faulty trace, particularly between the DASP 8 ASIC, and the DAC, or analog switch (U19).	Troubleshoot, and replace if necessary.
	Faulty op-amp.	Troubleshoot, and replace if necessary.
	Faulty analog switch (U19).	Troubleshoot, and replace if necessary.
	Faulty power supply bypass capacitor, particularly the cap at the analog switch (U9).	Troubleshoot, and replace if necessary.
No MIDI in.	Faulty Opto-isolator (U28).	Replace and retest.
	Faulty 8031 (U32).	Replace and retest.
No MIDI out.	Faulty 8031 (U32).	Replace and retest.
	Faulty transistor (Q2, Q3).	Replace and retest.

A few final notes: The DAC output is an extremely important test point. Familiarity with the appearance of this signal on a scope, will greatly facilitate troubleshooting audio problems. Exercise caution when examining the output of comparator (U21). Accidentally shorting pins 7, and 8 together will instantly result in a dead ASIC. Other than there, and in the power supply, you really can't do any harm with a scope probe, so explore.

Be on the watch for user error. (I.E., if a user complains that it won't load from a DataDisk, check to be sure that SYSEX ENABLE is turned on.)

Remember to install ALL of the latest revisions, before returning the unit. This can help prevent many unhappy returns.

8.0 SOFTWARE HISTORY

DATE	VERSION	COMMENTS
10/9/89	1.00	First production release
10/25/90	1.01	1) MIDI system exclusive dump request (F0 00 00 0E 03 02 F7) was not being responded to properly. Receiving this command will now cause the MIDIVERB III to send out a complete sysex dump of its programs.

9.0 M3 MIDI IMPLEMENTATION (SYSTEM EXCLUSIVE)

SYSTEM EXCLUSIVE FORMAT

The Midiverb III MIDI System Exclusive message format is as follows:

F0	System exclusive status
00 00 0E	Alesis manufacturer id#
03	Midiverb III id#
cc	Opcode
dd	Data
:	:
:	:
F7	End-Of-Exclusive

OPCODES:

00 - Complete MIDI Data Dump F0 00 00 0E 03 00 <data> F7

<data> consists of 3500 transmitted bytes. This results in 1750 actual bytes, since every two transmitted bytes result in one data byte as follows:

0aaaaaaaB first byte (bits 0-6)
000000bB second byte (bit 7 in bit 0)

The first 3200 transmitted bytes (1600 actual bytes) consist of the 100 programs (100-199), each containing 16 bytes. The parameter locations in these bytes are as follows (0-1599):

0: INPUT EQ
1: EFFECT EQ
2: CHORUS ALGORITHM
3: CHORUS SPEED
4: DELAY TIME MSB
5: DELAY TIME LSB
6: DELAY REGEN
7: REVERB ALGORITHM
8: REVERB DECAY
9: REVERB MIX
10: DELAY MIX
11: CONFIGURATION
12: MOD ROUTING
13: MOD AMPLITUDE
14&15: spare

Bytes 1600-1615 consist of the same data as above, and relates to the current edit buffer. Bytes 1616 through 1621 are as follows:

1616: Current program number (000-199)
1617: Current edit buffer edited (0=no / dot off, 1=yes / dot on)
1618: Current program step displayed at MIDI PROG page
1619: MIDI echo off/on (0/1)
1620: MIDI channel (0-15)
1621: MIDI program change enable off/on (0/1)

Bytes 1622-1749 consist of the 128 byte MIDI program map table. Although these values can never be above 127, the two byte packed format is retained for consistency.

The Midiverb III will appear non-functional for approximately 10 seconds after receiving a complete memory dump, with the display showing "——". This is due to the relatively slow write time of the EEPROM.

01 - One Program MIDI Data Dump F0 00 00 0E 03 01 <program#> <data> F7

<program#> contains a value from 0-99, which relates to the user programs 100-199 in memory in which the data will be stored. If it contains 100-127, the data will be copied to the edit buffer, and not stored to any program location.

<data> consists of 32 transmitted bytes. This results in 16 actual bytes, since every two transmitted bytes result in one data byte as shown in the complete memory dump above. The 16 bytes are in the same format as a single program of a complete memory dump, shown above. Any MIDI data received within 300 milliseconds of the completion of this command may be ignored.

02 - Complete MIDI Dump Request

F0 00 00 0E 03 02 F7

When the Midiverb III receives this message, it initiates a complete MIDI data dump, and the display will show "——" until the dump is complete.

F0 00 00 0E 03 03 <parameter#> < value lsb> < value msb> F7

<parameter#> = 0000ppppB as follows:

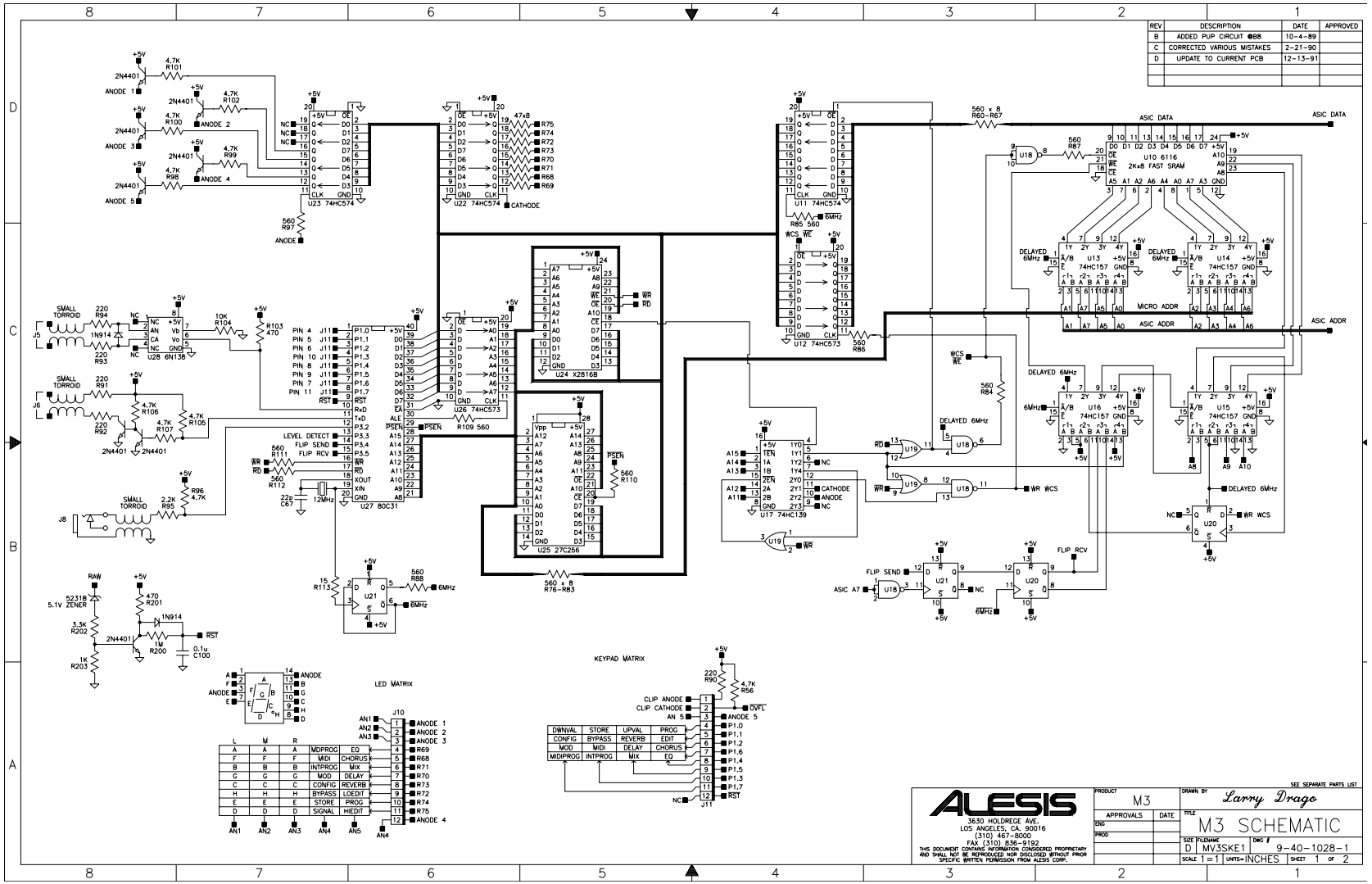
parameter	range	parameter	range
0=INPUT EQ	0-30	1=EFFECT EQ	0-30
2=CHORUS ALGORITHM	0-24	3=CHORUS SPEED	0-98
4=DELAY TIME	1-100*	5=DELAY REGEN	0-99
6=REVERB ALGORITHM	0-19	7=REVERB DECAY	0-99
8=REVERB MIX	0-99	9=DELAY MIX	0-99
10=CONFIGURATION	0-14	11=MOD ROUTING	0-48
12=MOD AMPLITUDE	0-198	13 & 14=spare	

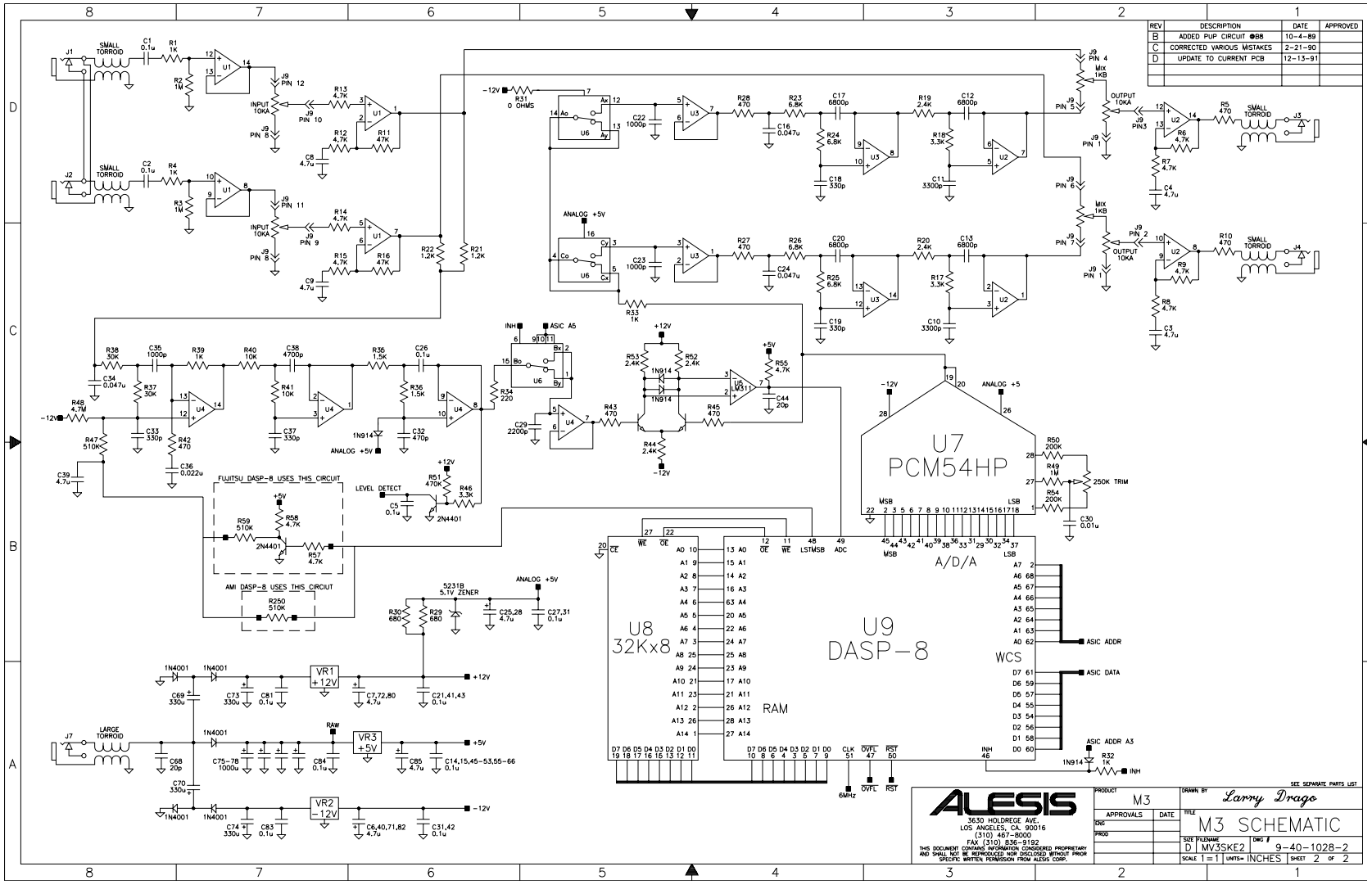
<value lsb> = 0aaaaaaaB = new parameter value lsb (bits 0-6)
<value msb> = 00000bbbB = new parameter value msb (bit 0-2),
resulting in 000000bbB baaaaaaaB. All parameters except 4 (delay time) are one byte values, so that only bit 0 of <value msb> may be relevant (if the parameter is valid above 127). The allowable range is shown above. The modulation amplitude is in offset binary, so the values 0 to 98 represent -99 to -1, 99 represents 00, and 100 to 198 represent 1 to 99. *The delay maximum value is 490 if the configuration is 13 or 14 (displayed as 14 & 15).

When the Midiverb III receives this message, it will edit the specified parameter to the new value and display it if it was on the relevant page. Any messages received via MIDI within 40 milliseconds after a parameter change may be ignored.

ALESIS
MidiVerb 3 (M3)

SCHEMATIC
AND
PCB
FILES


REV | DESCRIPTION | DATE | APPROVED
B | ADDED PUP CIRCUIT @88 | 10-4-89
C | CORRECTED VARIOUS MISTAKES | 2-21-90
D | UPDATE TO CURRENT PCB | 12-13-91
ASIC DATA
ASIC ADDR
MICRO ADDR
U10 6116 2Kx8 FAST SRAM
U24 X2816B
U25 27C256
U26 74HC573
U27 80C31
U28 6N138
U17 74HC139
U13 74HC157
U14 74HC157
U15 74HC157
U16 74HC157
KEYPAD MATRIX
LED MATRIX
DWNVAL | STORE | UPVAL | PROG
CONFIG | BYPASS | REVERB | EDIT
MOD | MIDI | DELAY | CHORUS
MIDIPROG | INTPROG | MIX | EQ
L | M | R | MIDPROG | EQ
MIDI | CHORUS
INTPROG | MIX
MOD | DELAY
CONFIG | REVERB
BYPASS | LOEDIT
STORE | PROG
SIGNAL | HIEDIT
ALESIS
3630 HOLDREGE AVE.
LOS ANGELES, CA. 90016
(310) 467-8000
FAX (310) 836-9192
THIS DOCUMENT CONTAINS INFORMATION CONSIDERED PROPRIETARY AND SHALL NOT BE REPRODUCED NOR DISCLOSED WITHOUT PRIOR SPECIFIC WRITTEN PERMISSION FROM ALESIS CORP.
PRODUCT M3
DRAWN BY Larry Drago
APPROVALS
DATE
ENG
PROD
TITLE M3 SCHEMATIC
SIZE D FILENAME M V3SKE1
DWG # 9-40-1028-1
SCALE 1=1 UNITS=INCHES
SHEET 1 OF 2
SEE SEPARATE PARTS LIST



REV	DESCRIPTION	DATE	APPROVED
B	ADDED PUP CIRCUIT @B8	10-4-89	
C	CORRECTED VARIOUS MISTAKES	2-21-90	
D	UPDATE TO CURRENT PCB	12-13-91	

ALESIS
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PRODUCT	M3
APPROVALS	DATE
ENG	
PROD	
DRAWN BY	Larry Drago
TITLE	M3 SCHEMATIC
SIZE	D
FILENAME	M V3SKE2
DWG #	9-40-1028-2
SCALE	1 = 1
UNITS=	INCHES
SHEET	2 OF 2

SEE SEPARATE PARTS LIST

ALESIS
MidiVerb 3 (M3)

BOM

10.0 M3 Service Parts List

GROUP	DESCRIPTION	PART#	QNTY	POSITION	PCB	MANUFACT	NOTES
ASS	PCB, M3 MAIN ASSY	8-20-0052	1	MAIN BOARD ASSEMBLY			
ASS	PCB, LED ASSY	8-20-0049	1	LED (FRONT PANEL) BOARD ASSEMBLY			
CAB	12 PIN SIL 3 0.1 CTR	4-19-0312	1		MAIN-F/P		
CAB	12 PIN SIL 7 0.1 CTR	4-19-0712	2		MAIN-F/P		
CAP	0.1 MF CERDISC	1-02-0104	32	C14,15,21,27,31,41-43,45-53,55-66,81,83,84	MAIN		0.25 SPC
CAP	1000 MF ELEC 16V 10x20	1-08-1000	4	C75-78	MAIN		10x20mm/0.2 SPC
CAP	330 MF ELEC 25V 10x13	1-09-0337	4	C69,70,73,74	MAIN		10x13mm/0.2 SPC
CAP	4.7 MF ELEC 50V 05x12	1-11-0475	15	C3,4,6,7-9,25,28,39,40,71,72,80,82,85	MAIN		05x12mm/0.1 SPC
CER	22 PF CERDISC	1-02-0220	3	C44,67,68	MAIN		0.25 SPC
FIL	1000 PF FILM	1-20-0102	3	C22,23,35	MAIN	WIMA	7x2mm/0.2 SPC
FIL	0.01 MF FILM	1-20-0103	1	C30	MAIN	WIMA	7x2mm/0.2 SPC
FIL	0.1 MF FILM	1-20-0104	5	C1,2,26,99,100	MAIN	WIMA	7x2mm/0.2 SPC
FIL	2200 PF FILM	1-20-0222	1	C29	MAIN	WIMA	7x2mm/0.2 SPC
FIL	0.022 MF FILM	1-20-0223	1	C36	MAIN	WIMA	7x2mm/0.2 SPC
FIL	330 PF FILM	1-20-0331	4	C18,19,33,37	MAIN	WIMA	7x2mm/0.2 SPC
FIL	3300 PF FILM	1-20-0332	2	C10,11	MAIN	WIMA	7x2mm/0.2 SPC
FIL	470 PF FILM	1-20-0471	1	C32	MAIN	WIMA	7x2mm/0.2 SPC
FIL	4700 PF FILM	1-20-0472	1	C38	MAIN	WIMA	7x2mm/0.2 SPC
FIL	0.047 MF FILM	1-20-0473	3	C16,24,34	MAIN	WIMA	7x2mm/0.2 SPC
FIL	6800 PF FILM	1-20-0682	4	C12,13,17,20	MAIN	WIMA	7x2mm/0.2 SPC
HDR	12 PIN SIL 0.1 CTR	4-15-0012	5	J9-11, F/P	MAIN/FP		LOCK
HDR	12 PIN SIL 90 0.1 CTR	4-15-0013	1	POT PCB	POT		RA LOCK
HDW	6-32x1/4 PF BLK UNC	5-00-0004	4	F/P			
HDW	6-32x1/4 PP BLK UNC	5-00-0003	29	CASE			
HDW	#6 INT STAR WASHER	5-01-0002	2	VR1,VR3			
HDW	0.095 NYLON SPACER	5-01-0007	10	F/P ASSY			
HDW	7/16 STAR WASHER	5-01-0008	2	J1,J8			
HDW	1/2 6-32 STANDOFF	5-02-0003	5	FP/HEATSINK			
HDW	6-32 KEP NUT	5-02-6320	8	F/P			
HDW	ANGLE BRACKET F/P	5-07-0001	3				
HDW	HEAT SINK	9-03-1008	1	VR1,VR3			
HDW	RUBBER STRIP 0.5x0.25	9-23-1003	2				
HDW	RUBBER STRIP 5 IN	9-23-1006	2				
IC	7805 +5 V T0220	2-11-7805	1	VR3	MAIN	NAT ONLY	
IC	7812 +12 V T0220	2-11-7812	1	VR1	MAIN	NAT ONLY	
IC	7912 -12 V T0220	2-11-7912	1	VR2	MAIN	NAT	
IC	74HC139 DEMUX	2-14-0139	1	U17	MAIN	TI ONLY - NO NAT	16 PIN DIP 0.3
IC	74HC157 QUAD 2-I/P MUX	2-14-0157	4	U13-16	MAIN	TI/NAT	16 PIN DIP 0.3
IC	74HC573 3-STATE LATCH	2-14-0573	2	U12,26	MAIN	TI/NAT	20 PIN DIP 0.3
IC	74HC574 OCTAL FF	2-14-0574	3	U11,22,23	MAIN	TI/NAT	20 PIN DIP 0.3
IC	74HC00 QUAD 2-IN NAND	2-14-7400	1	U18	MAIN	TI/NAT	14 PIN DIP 0.3
IC	74HC32 QUAD 2-I/P OR	2-14-7432	1	U19	MAIN	TI/NAT	14 PIN DIP 0.3
IC	74HC74 DUAL D FF	2-14-7474	2	U20,21	MAIN	TI/NAT	14 PIN DIP 0.3
IC	TL084 (LF347) 4 OP AMP	2-21-0084	4	U1-4	MAIN	TI/NAT	14 PIN DIP 0.3
GROUP	**DESCRIPTION**	**PART#**	**QNTY**	**POSITION**	**PCB**	**MANUFACT**	**NOTES**
IC	LM311 ANALOG COMP	2-22-0311	1	U5	MAIN	TI	8 PIN DIP 0.3

IC	4053 ANALOG SWITCH	2-23-4053	1	U6	MAIN	ST/HAR/RCA/SIG	16 PIN DIP 0.3
IC	6N138 OPTOISO	2-24-0138	1	U28	MAIN	SIEMANS/HP	8 PIN DIP 0.3
IC	2Kx8 SRAM 6116	2-17-0128	1	U10	MAIN	CYPRESS	24 PIN DIP 0.3
IC	32Kx8 SRAM	2-17-0257	1	U8 (LOW POWER)	MAIN	SONY	28 PIN DIP 0.6
IC	2Kx8 EEPROM X2816CP-20	2-19-0002	1	U24	MAIN	XICOR	24 PIN DIP 0.6
IC	27C256	2-19-0256	1	U25	MAIN	TI/NAT/INTEL	28 PIN DIP 0.6
IC	80C31 MPU	2-20-8031	1	U27	MAIN	SIG/INTEL	40 PIN DIP 0.6
IC	PCM54HP DAC	2-25-0054	1	U7	MAIN	BURR-BROWN	28 PIN DIP 0.6
IC	89Z ASIC (AMI)	2-27-0006	1	U9	MAIN	AMI	PLCC-68
JAC	5 PIN DIN JACK	4-00-0001	2	J5,6 (MIDI)	MAIN		
JAC	1/4 CLIFF (MONO)	4-02-0001	5	J1-4,8	MAIN	CLIFF	
JAC	3.5mm BAR JACK (P3)	4-16-0002	1	J7 (POWER)	MAIN		
ME	1N4148 SIGNAL DIODE	2-00-4148	6		MAIN		D0-41/0.3 SPC
ME	1N4003 POWER DIODE	2-02-4003	5		MAIN		DO-27/0.5 SPC
ME	1N5231B ZENER	2-02-5231	2		MAIN	MOT	DO-41/0.3 SPC
ME	2N4401 NPN TRANS	2-03-4401	11	Q1-9,11,12	MAIN	RCA/NAT/MOT/HAR	TO-92/0.1 SPC
ME	LED (GRN) LDG 1151 T1	3-00-0001	1		F/P		
ME	LED (RED) LDR 1102 T1	3-02-0001	16		F/P		
ME	7 SEG DISP 4710	3-04-0001	3		F/P		
ME	12 MHz CER RES	7-01-0003	1		MAIN		
ML	SIDE PANEL	9-03-1003	2				
ML	COVER PANEL	9-03-1005	2				
ML	REAR PANEL	9-03-1035	1				
MTL	FRONT PANEL	9-03-1032	1				
PCB	PCB, POT	9-40-1003	1				
PCB	PCB, M3 FRONT PANEL	9-40-1025	1				
PCB	PCB, M3 MAIN REVD	9-40-1028	1		REV D		
PLS	STANDARD KNOB	9-11-1001	3				15mm SKIRT
PLS	LED BUTTON	9-11-1017	13				
PLS	PLAIN BUTTON	9-11-1018	3				
PLS	RED BEZEL	9-11-1020	1				
POT	10 KA DUAL	0-09-1001	2	I/P,O/P	POT		
POT	1 KB DUAL	0-09-1002	1	MIX	POT		
RES	0 1/8W 5%	0-00-0000	5	R31,108,114-116	MAIN		
RES	1K 1/8W 5%	0-00-0102	6	R1,4,32,33,39,203	MAIN		
RES	10K 1/8W 5%	0-00-0103	3	R40,41,104	MAIN		
RES	1M 1/8W 5%	0-00-0105	4	R2,3,49,200	MAIN		
RES	1.2K 1/8W 5%	0-00-0122	2	R21,22	MAIN		
RES	15 1/8W 5%	0-00-0150	1	R113	MAIN		
RES	1.5K 1/8W 5%	0-00-0152	2	R35,36	MAIN		
RES	200K 1/8W 5%	0-00-0204	2	R50,54	MAIN		
RES	220 1/8W 5%	0-00-0221	6	R34,90-94	MAIN		
RES	2.2K 1/8W 5%	0-00-0222	1	R95	MAIN		
RES	2.4K 1/8W 5%	0-00-0242	5	R19,20,44,52,53	MAIN		
RES	30K 1/8W 5%	0-00-0303	2	R37,38	MAIN		
RES	3.3K 1/8W 5%	0-00-0332	4	R17,18,46,202	MAIN		
GROUP	**DESCRIPTION**	**PART#**	**QNTY**	**POSITION**	**PCB**	**MANUFACT**	**NOTES**
RES	47 1/8W 5%	0-00-0470	8	R68-75	MAIN		
RES	470 1/8W 5%	0-00-0471	9	R5,10,27,28,42,43,45,103,201	MAIN		
RES	4.7K 1/8W 5%	0-00-0472	19	R6-9,12-15,55,56,96,98-102,105-107	MAIN		

RES	47K 1/8W 5%	0-00-0473	2	R11,16	MAIN		
RES	470K 1/8W 5%	0-00-0474	1	R51	MAIN		
RES	4.7M 1/8W 5%	0-00-0475	1	R48	MAIN		
RES	510K 1/8W 5%	0-00-0514	2	R47,250	MAIN		
RES	560 1/8W 5%	0-00-0561	26	R60-67,76-88,97,109-112	MAIN		
RES	680 1/8W 5%	0-00-0681	2	R29,30	MAIN		
RES	6.8K 1/8W 5%	0-00-0682	4	R23-26	MAIN		
RES	250K TRIMPOT	0-08-0254	1		MAIN		
RUB	RUBBER KEYPAD	9-23-1027	1				
SOC	24 PIN DIP 0.3	4-04-0024	1	U10	MAIN		
SOC	24 PIN DIP 0.6	4-06-0024	1	U24	MAIN		
SOC	28 PIN DIP 0.6	4-06-0028	3	U7,8,25	MAIN		
SOC	40 PIN DIP 0.6	4-06-0040	1	U27	MAIN		
SOC	68 PIN ASIC SOCKET	4-12-0068	1	U9	MAIN		PLCC-68