

ICOM

SERVICE MANUAL

COMMUNICATIONS RECEIVER

IC-R2

INTRODUCTION

This service manual describes the latest service information for the **IC-R2** at the time of publication.

MODEL	VERSION	SYMBOL
IC-R2	Europe	EUR
	Italy	ITA
	Taiwan	TPE
	U.S.A.	USA
	Canada	CAN
	Other	OTH
		OTH-1

To upgrade quality, all electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

DANGER

NEVER connect the receiver to an AC outlet or to a DC power supply that uses more than 3.5 V. Such a connection could cause a fire hazard and/or electric.

DO NOT expose the receiver to rain, snow or any liquids.

DO NOT reverse the polarities of the power supply when connecting the receiver.

DO NOT apply an RF signal of more than 20 dBm (100mW) to the antenna connector. This could damage the receiver's front end.

ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

<SAMPLE ORDER>

8930046581	LCD Contact	IC-R2	LOGIC UNIT	5 pieces	
8810009560	Screw	PH BO M2x6 ZK	IC-R2	Chassis	10 pieces

Addresses are provided on the inside back cover for your convenience.



REPAIR NOTES

1. Make sure a problem is internal before disassembling the receiver.
2. **DO NOT** open the receiver until the receiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated turning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the receiver is defective.
6. **READ** the instructions of test equipment thoroughly before connecting equipment to the receiver.

TABLE OF CONTENTS

SECTION 1 SPECIFICATIONS**SECTION 2 INSIDE VIEWS****SECTION 3 DISASSEMBLY INSTRUCTIONS****SECTION 4 CIRCUIT DESCRIPTION**

4-1	RECEIVER CIRCUITS	4-1
4-2	PLL CIRCUITS	4-3
4-3	POWER SUPPLY CIRCUITS	4-4
4-4	PORT ALLOCATIONS	4-4

SECTION 5 ADJUSTMENT PROCEDURES

5-1	PREPARATION	5-1
5-2	PLL ADJUSTMENT	5-3
5-3	RECEIVER ADJUSTMENT	5-5

SECTION 6 PARTS LIST**SECTION 7 MECHANICAL PARTS AND DISASSEMBLY****SECTION 8 SEMI-CONDUCTOR INFORMATION****SECTION 9 BOARD LAYOUTS**

9-1	LOGIC UNIT	9-1
9-2	RF UNIT	9-3

SECTION 10 BLOCK DIAGRAM**SECTION 11 VOLTAGE DIAGRAM**

11-1	LOGIC UNIT	11-1
11-2	RF UNIT	11-2

SECTION 1 SPECIFICATIONS

■ GENERAL

- Frequency range : **Receive Frequencies (MHz)**

Version	Receive Frequencies (MHz)
EUR, U.K., CAN, OTH, OTH-1	0.495 – 1309.995
U.S.A.	0.495 – 823.995 849.000 – 868.995 894.000 – 1309.995

- Mode : FM, WFM, AM
- No. of memory channel : 450 channel
- Frequency stability : ± 6 ppm max.
(-10°C to $+60^{\circ}\text{C}$)
- Tuning steps : 5, 6.25, 10, 12.5, 15, 20, 25, 30, 50, and 100 kHz
- Antenna Impedance : 50Ω
- Power supply requirement : $2 \times \text{AA(R6)}$ Ni-Cd or alkaline cell
- Polarity : Negative ground
- Frequency resolution : 5 kHz, 6.25 kHz
- Current drain (at 3.0 V) :
 - Rated audio 170 mA typical
 - Standby 100 mA typical
 - Power saved 41 mA typical
- Usable temperature range : -10°C to $+60^{\circ}\text{C}$
(-14°F to $+140^{\circ}\text{F}$)
- Dimensions (projections not included) : $58(\text{W}) \times 86(\text{H}) \times 27(\text{D})$ mm;
 $29\frac{3}{8}(\text{W}) \times 3\frac{3}{8}(\text{H}) \times 1\frac{1}{16}(\text{D})$ in
- Weight (with antenna and battery) : 170 (g); 6 (oz)
- External SP connector : 3-conductor 3.5(d) mm ($1/8''$) / 8Ω

■ RECEIVER

- Receiver system : Triple super heterodyne
- Intermediate frequency : 1st 266.7 MHz
2nd 19.65 MHz
3rd 450 kHz
- Sensitivity* : (except spurious points)

Frequency (MHz)	FM	WFM	AM
0.495 – 1.625	—	0.4 μV	2.5 μV
1.625 – 5.0	0.56 μV		
5.0 – 30.0			
30.0 – 76.0			
76.0 – 108.0			
108.0 – 118.0			
118.0 – 136.0			
136.0 – 175.0			
175.0 – 222.0			
222.0 – 247.0			
247.0 – 330.0			
330.0 – 470.0			
470.0 – 770.0			
770.0 – 833.0			
833.0 – 1309.995	0.79 μV		

* FM and WFM are measured at 12 dB SINAD; AM is measured at 10 dB S/N.

- Squelch Sensitivity :

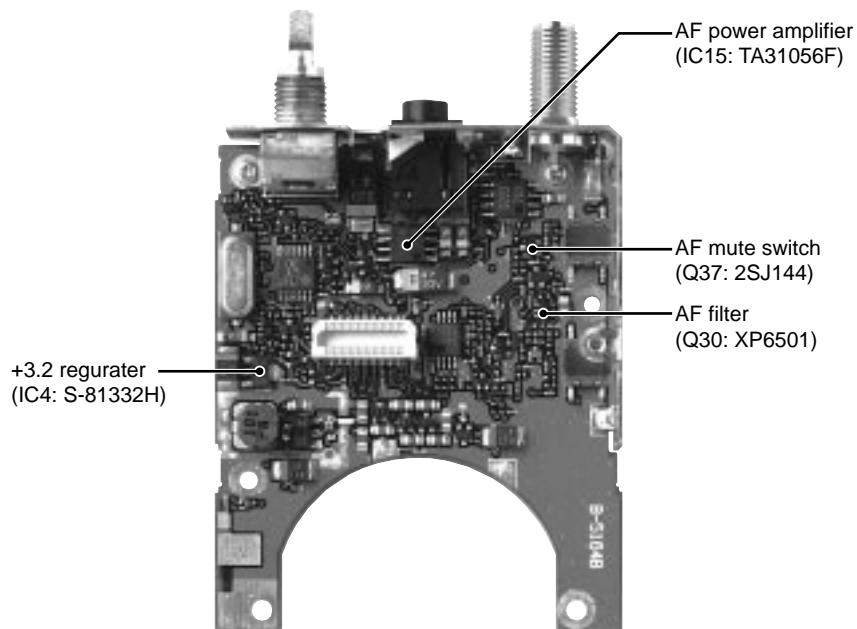
Frequency (MHz)	FM	WFM	AM
0.495 – 1.625	—	0.4 μV	2.5 μV
1.625 – 5.0	0.56 μV		
5.0 – 30.0			
30.0 – 76.0			
76.0 – 108.0			
108.0 – 118.0			
118.0 – 136.0			
136.0 – 175.0			
175.0 – 222.0			
222.0 – 247.0			
247.0 – 330.0			
330.0 – 470.0			
470.0 – 770.0			
770.0 – 833.0			
833.0 – 1309.995	0.79 μV		

- Selectivity :
 - AM / FM more than 15 kHz / -6 dB
 - WFM less than 30 kHz / -60 dB
 - more than 150 kHz / -6 dB
- Audio output power : 100 mW typical at 10 % distortion with an 8Ω load

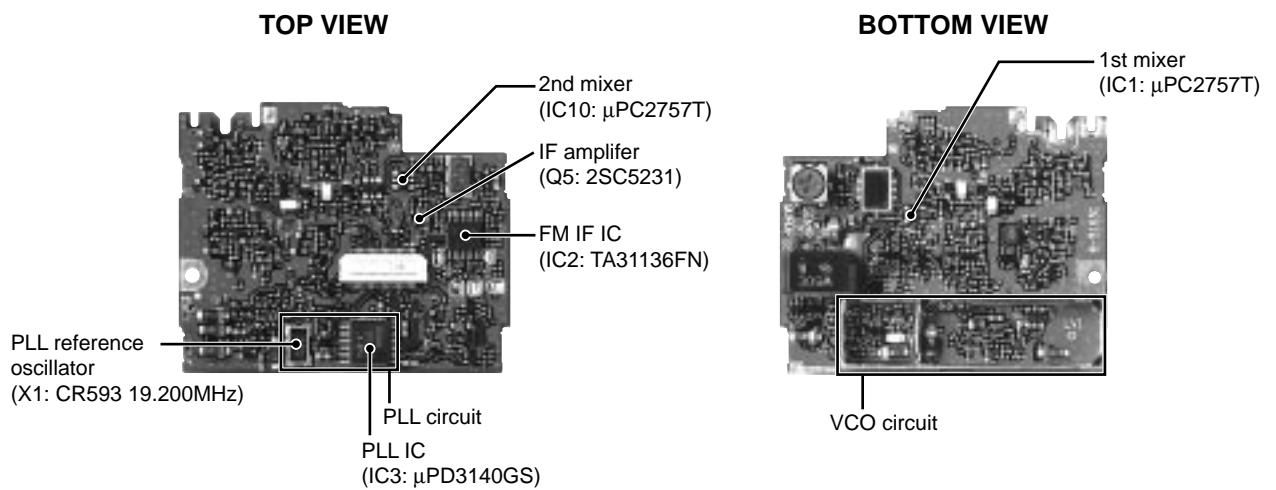
All stated specifications are subject to change without notice or obligation.

SECTION 2 INSIDE VIEWS

• LOGIC UNIT



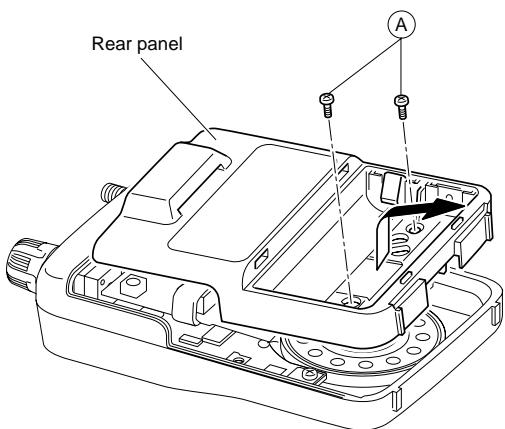
• RF UNIT



SECTION 3 DISASSEMBLY INSTRUCTIONS

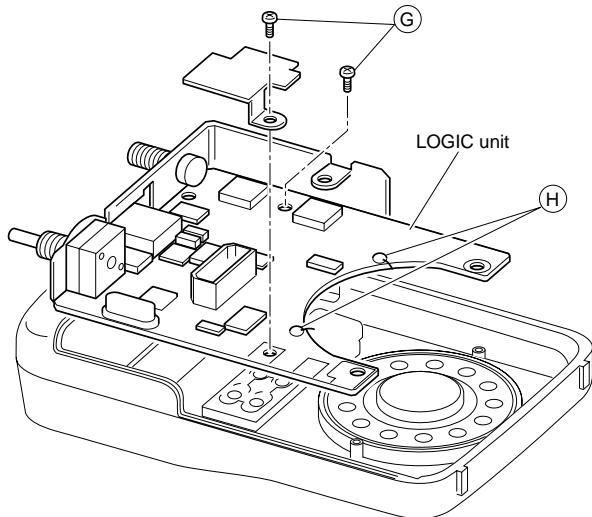
• REMOVING THE REAR PANEL

- ① Unscrew 2 screws, **A**.
- ② Remove the rear panel in the direction of the arrow.



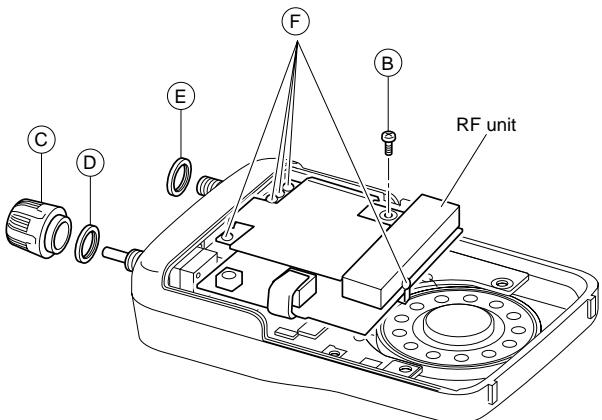
• REMOVING THE LOGIC UNIT

- ① Unscrew 2 screws, **G**.
- ② Unsolder 2 points, **H**, and then remove the LOGIC unit.



• REMOVING THE RF UNIT

- ① Unscrew 1 screw, **B**.
- ② Remove 1 knob, **C**.
- Unscrew 2 nuts, **D** and **E**.
- ③ Unsolder 5 points, **F**, and then remove the RF unit.



SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 ANTENNA SWITCHING CIRCUIT (RF UNIT)

The RF signals from the antenna connector pass through the limitter (D68) and an attenuator (D69). The signals are then applied to the RF circuit the antenna switching circuit (D13, D73, D75) which suppress out-of-band signals.

4-1-2 RF CIRCUIT (RF UNIT)

The RF circuit amplifies the received signals within the range of frequency coverage and filters out-of-band signals.

(1) 0.495 MHz–29.999 MHz

RF signals (0.495–29.999MHz) from an antenna switching circuit (D73) pass through a low-pass filter (C511–C515, L81, L82). The filtered signals are amplified at an RF amplifier (Q505) passing through each band-pass filter depending on the receiving frequency. The amplified signals are then applied to the 1st mixer circuit (IC1) after being amplified at another RF amplifier (IC11) via the band switching diode(D71).

The signals below 1.9 MHz pass through a low-pass filter (C534, C535, C657, C658, L88, L89) via the band switching diode (D66), and are then applied to the RF amplifier circuit (Q505) via the band switching diode (D67).

The 1.9 MHz–14.995 MHz signals pass through the band switching diode (D65) and band-pass filter (C522–C531, L85–L87, L91), and are then applied to the RF amplifier circuit (Q505) via the band switching diode (D70).

The 15 MHz–29.995 MHz signals pass through the band switching diode (D63) and high-pass filter (C516–C520, L83, L84) and are then applied to the RF amplifier circuit (Q505) via the band switching diode (D64).

(2) 118 MHz–174.995 MHz, 330 MHz–832.995 MHz

RF signals (118 MHz–174.995 MHz, 330 MHz–832.995 MHz) from an antenna switching diode (D75) are passed through each bandpass filter and RF amplifier, and are then applied to the 1st mixer circuit (IC1) via the band switching diode (D71) and RF amplifier (IC11).

The 118 MHz–174.995 MHz signals pass through the band switching diode (D74) and low-pass filter (C8–C13, C67, C416, L14, L57–L59, L70), and are then amplified at RF amplifier (Q14). The amplified signal passes through the tunable band-pass filters (D1, D2) and band switching diode (D25).

The 330 MHz–469.995 MHz signals are amplified at RF amplifier (Q35) via the band switching diode (D3) and band-pass filter (C19–C23, C216, L2–L5). The amplified signal passes through the tunable band-pass filters (D3, D4) and band switching diode (D29).

The 470 MHz–832.995 MHz signals are amplified at RF amplifier (Q24) via the band-pass filter (C32, C33, C35–C37, C39, C144, C145), between the band switching diode (D11, D32).

(3) 30–117.995 MHz, 175–329.995 MHz

The 30 MHz–117.95 MHz, 175 MHz–329.995 MHz signals pass through the low-pass filter (C40–C43, C665, C666, L9, L10, L92), and are then applied to the RF amplifier (Q36). The amplified signals are amplified at the RF amplifier (IC11) via band switching diodes (D34, D71). The amplified signals are applied to the 1st mixer circuit (IC1).

(4) 833 MHz–1309.995 MHz

The 833 MHz–1309.995 MHz signals pass through the bandpass filter (C5, C45–51, L11–L13, L43), and are then applied to the RF amplifier (Q26). The amplified signals are amplified at the RF amplifier (IC11) via band switching diodes (D36). The amplified signals are applied to 1st mixer circuit (IC1).

4-1-3 1ST MIXER CIRCUIT (RF UNIT)

The 1st mixer circuit converts the received RF signals to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will pass through the bandpass filters at the next stage of the 1st mixer.

The filtered RF signals are mixed with 1st LO signals at the 1st mixer circuit (IC1) to produce a 266.7 MHz 1st IF signal. The 1st IF signal is output from pin 6, and passed through the bandpass filter (F11) to suppress unwanted harmonic components. The filtered 1st IF signal is applied to the 2nd mixer circuit.

The 1st LO signals are generated at the 1st VCO (Q28, Q30, D45) and are applied to the 1st mixer (IC1, pin 3) directly or passing through the doubler circuit (Q31) after being amplified at the buffer amplifiers (IC4, Q40).

4-1-4 1ST IF AND 2ND MIXER CIRCUITS (RF UNIT)

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal.

The filtered 266.7 MHz 1st IF signal from the bandpass filter is mixed with the 2nd LO signal at the 2nd mixer circuit (IC10, pin 1) to produce a 19.65 MHz 2nd IF signal. The 2nd IF signal pass through (except WFM mode) or bypass (WFM mode) the bandpass filter (F13), and is then amplified at the 2nd IF amplifier (Q5). The amplified signal is applied to the demodulator circuit.

4-1-5 DEMODULATOR CIRCUITS (RF UNIT)

The demodulator circuit converts the 2nd IF signal into AF signals.

The 19.65 MHz 2nd IF signal from the 2nd IF amplifier (Q5) is applied to the 3rd mixer section of the FM IF IC (IC2, pin 16) and is then mixed with the 3rd LO signal for conversion into a 450 kHz 3rd IF signal.

IC2 contains the 3rd mixer, limiter amplifier, quadrature detector and S-meter detector, etc. A frequency from the PLL reference oscillator is used for the 3rd LO signal (19.20 MHz).

(1) FM mode

The 3rd IF signal is output from FM IF IC (IC2, pin 3) and passes through the ceramic bandpass filter (FI2). The filtered signal is fed back and amplified at the limiter amplifier section (pin 5), then demodulated AF signals at the quadrature detector section (pins 10, 11) and detector coil (L21). The demodulated AF signals are output from pin 9 and are applied to the AF circuit (LOGIC unit).

(2) WFM mode

The 3rd IF signal from the 3rd mixer bypasses the ceramic filter (FI2) and fed back to the limiter amplifier section (pin 5). The amplified signal is demodulated at the quadrature detector section (pins 10, 11) and detector coil (L21). The AF signals are output from pin 9 and are applied to the AF circuit (LOGIC unit).

By connecting R55 to R54 in parallel, the output characteristics of pin 12, "RSSI", change gradually. Therefore, the FM IF IC can detect WFM components.

(3) AM mode

The filtered 3rd IF signal from the bandpass filter (FI2) is amplified at the 3rd IF amplifier (Q1). The amplified IF signal is applied to the AM detector circuit (Q4) to converted into AF signals, and the signals are applied to the AF circuit (LOGIC unit).

4-1-6 AF AMPLIFIER CIRCUIT (LOGIC UNIT)

The AF amplifier circuit amplifies the demodulated AF signals to drive a speaker.

While in FM mode, AF signals from the demodulator circuit (RF unit) are passed through the de-emphasis circuit (R118, C66, C68) with frequency characteristics of -6 dB/octave, and are then applied to the pre-amplifier (Q31) via the band-pass filter (Q30).

While in AM mode, AF signals are pass through the band-pass filter and are then applied to the pre-amplifier (Q31).

While in WFM mode, AF signals are applied to the pre-amplifier (Q31) directly.

The pre-amplified AF signals pass through the AF mute circuit (Q37) and are then applied to the electronic volume control circuit (IC14, pin 6). The level controlled AF signals are output from pin 7 and applied to the AF power amplifier (IC15, pin 1) via the buffer amplifier (Q36). The power amplified AF signals are applied to the internal speaker via the [EXT SP] jack.

The electronic volume control circuit controls AF gain, therefore, the AF output level is according to the [VOL] setting and also the squelch conditions.

4-1-7 SQUELCH CIRCUIT (LOGIC AND RF UNITS)

• NOISE SQUELCH

The noise squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

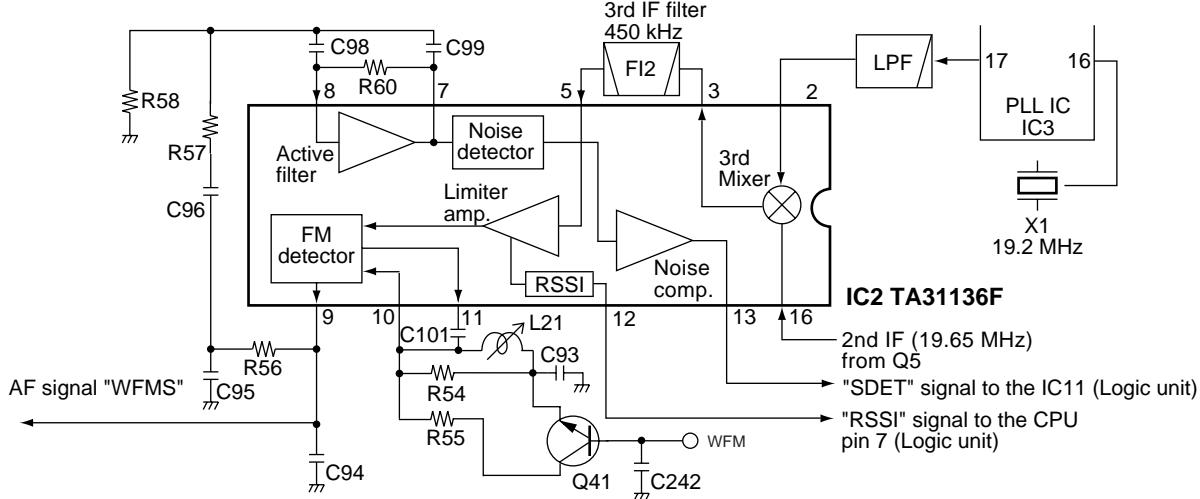
A portion of the AF signals from the FM IF IC (RF unit; IC2, pin 9) are applied to the active filter section (IC2, pin 8). The active filter section amplifies and filters noise components.

The filtered signals are applied to the noise detector section and output from IC2 (pin 13) as the "SDET" signal.

The "SDET" signal from IC2 (pin 13) passes through the noise detector (LOGIC unit; IC1), and is then applied to the CPU (LOGIC unit; IC11, pin 12) via the "SQL" line. The CPU analyzes the noise condition and outputs the "AMUTE" signal to the AF mute switch (Q37).

Even when the squelch is closed, the AF mute switch (Q37) opens at the moment of emitting beep tones.

• 2nd IF AND DEMODULATOR CIRCUITS



• TONE SQUELCH

The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the FM IF IC (IC2, pin 9) passes through the low-pass filter (LOGIC unit; IC9) via the "WFMS" line to remove AF (voice) signals and is applied to the CTCSS decoder inside the CPU (LOGIC unit; IC11, pin 8) via the "RTONE" line to control the AF mute switch.

4-2 PLL CIRCUITS

4-2-1 PLL CIRCUIT (RF UNIT)

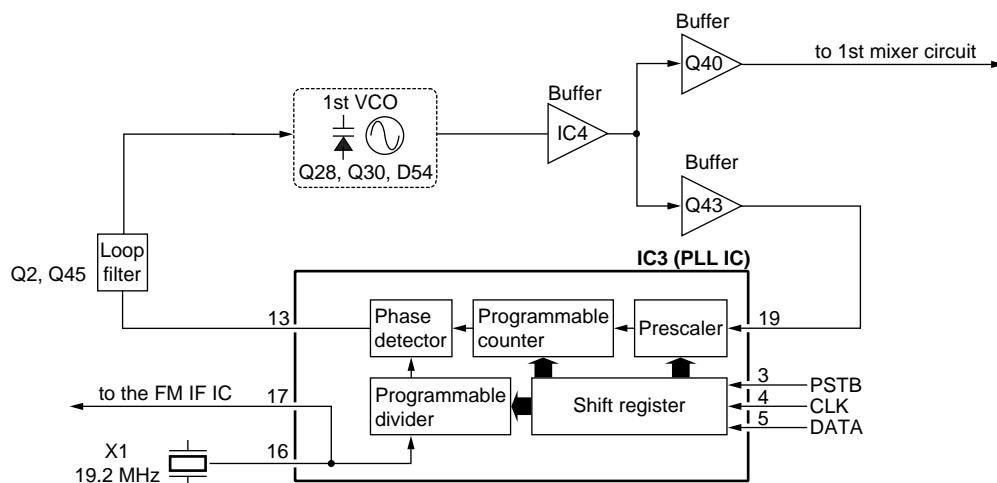
A PLL circuit provides stable oscillation of the receive 1st/2nd LO frequencies. The PLL circuit compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

An oscillated signal from the 1st VCO passes through the buffer amplifiers (IC4, Q43) is applied to the PLL IC (IC3, pin 19) and is prescaled in the PLL IC based on the divided ratio (N-data). The PLL IC detects the out-of-step phase using the reference frequency and outputs it from pin 13. The output signal is passed through the loop filter (Q2, Q45) and is then applied to the 1ST VCO circuit as the lock voltage.

4-2-2 REFERENCE OSCILLATOR CIRCUIT (RF UNIT)

The reference oscillator circuit (X1, IC3) generates a 19.2 MHz reference frequency which is stabilized within the temperature range -10°C ($+14^{\circ}\text{F}$) to $+60^{\circ}\text{C}$ ($+140^{\circ}\text{F}$). The reference frequency is applied to the PLL IC (IC3, pin 16) and the signal is output from the pin 17, and is then applied to the FM IF IC (IC2, pin 2) via the low-pass fileter.

• PLL circuit



4-2-3 1ST VCO CIRCUIT (RF UNIT)

The oscillated signal is applied to the buffer amplifiers (IC4, Q40). The amplified signal is applied to the 1st mixer circuit (IC1) via the RX LO switch circuit (D42–D44) and doubler circuit (Q31).

The 1st VCO circuit (Q28, Q30, D54) oscillates 267.2 MHz–380 MHz and 380 MHz–550 MHz by switching the SHIFT switch (Q29) "High" and "Low" respectively.

A portion of the signal from IC4 is amplified at the buffer amplifier (Q43) and is then fed back to the PLL IC (IC3, pin 2) as the comparison signal.

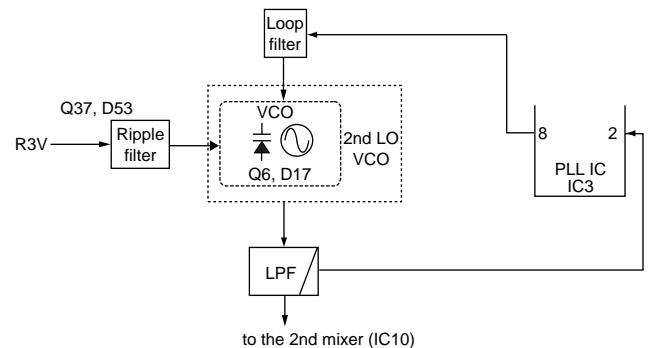
4-2-4 2nd VCO CIRCUIT (RF UNIT)

The 2nd LO circuit generates the 2nd LO frequencies, and the signals are applied to the 2nd mixer circuit.

The 2nd VCO circuit (Q6, L45, C80, C207, C208) oscillates 260 MHz. The oscillated signal is applied to the 2nd mixer (IC10, pin 3), and is then mixed with the 1st IF signal.

An oscillated signal from the 2nd VCO passes through the low-pass filter (C154, C250–C252, L69), and is applied to the PLL IC (IC3, pin 2), and is then output from pin 8.

• 2nd LO VCO circuit



4-3 POWER SUPPLY CIRCUITS

VOLTAGE LINE

LINE	DESCRIPTION
BATT	The voltage from the attached battery.
VP	Common 13 V converted from BATT line by the DC-DC convertors (IC10 and D3, D5, D15). The output voltage is applied to the PLL circuit (RF unit).
R3V	Receive 3V controlled by the R3V regulator circuit (Q4) using the "RX" signal from CPU (IC11).
+3S	Common 3V converted by the +3S regulator circuit (Q3, Q39) using the "+3SC" signal from CPU (IC11).
+3V	Common 3V converted by the +3V regulator circuit (Q6) using the "POWERC" signal from CPU (IC11).

4-4 PORT ALLOCATIONS

4-4-1 CPU (LOGIC UNIT IC11)

Pin number	Port name	Description
1	ADJ	Output control signal for the adjustment mode.
2	ATT	Outputs RF attenuator control signal to attenuator switch.
3	K2	Input port for [LOCK], [BAND], [V/M] switches.
4	K1	Input port for [UP], [DOWN] switches.
5	AMUTE	Output AF mute switch (LOGIC unit; Q37) control signal. LOW : While squelched.
6	BATT	Input port for the Low battery detection.
7	RSSI	Input port for the RSSI signal from the FM IF IC (RF unit; IC2, pin12) to detect receiving signal strength.
8	RTONE	Input port for the receiving tone signal.
9	TRC	Outputs control signal for the tunable band-pass filter.
10	FSET	Outputs control signal for the RIT frequency.
11	CTON	Outputs control signal for the CTCSS regulator circuit.
12	SQL	Pulse signal input port for the squelch.
13	KFUNC	Input port for the [FUNC] switch. Low : While [FUNC] switch is pushed.
14	KTS	Input port for the [TS] switch. Low : While [TS] switch is pushed.
15	VRC	Outputs level control signal for AF volume.
16	DCK	Input port for the DOWN signal from the [DIAL].
17	AM	Outputs AM mode select signals. Low : When AM is selected.
18	WFM	Outputs WFM mode select signals. Low : When WFM is selected.
21	BEEP	Outputs beep audio signals.
22	DUD	Input port for the UP signal from the [DIAL].
23	POWER	Input for the [POWER] switch. Low : While [POWER] switch is pushed
24	AFON	Outputs control signal for the AF amplifier regulator circuit. High : Activates the AF amplifier circuit.
25	DBL1	Outputs control signal for the 1st doubler circuit. Low : Activates the 1st doubler circuit.

Pin number	Port name	Description
26	LIGHT	Output LCD backlight control signal. High : Lights ON
27	+3SC	Outputs +3S regulator control signal for the receiver circuit. Low : Receiving.
28	POWERC	Outputs +3V regulator control signals.
29	B3	Outputs high-pass filter select signal. Low : When frequency 15 to 30 MHz are displayed.
30	B2	Outputs band-pass filter select signal. Low : When frequency 1.9 to 15 MHz are displayed.
31	B1	Outputs low-pass filter select signal. Low : When frequency 0.5 to 1.5 MHz are displayed.
32	KSQL	Input port for the [SQL] switch. High : While [SQL] switch is pushed.
33	RESET	Input port for the RESET signal.
39	EDA	Outputs data signals to the EEPROM IC (LOGIC unit; IC2).
42	PCK/IS	Outputs clock signal to both PLL IC (RF unit; IC3) and EEPROM IC (LOGIC unit; IC2).
43	ECK/I3	Outputs clock signal to EEPROM IC.
44, 45	I2, I1	Input ports for Initial matrix.
46	PSTB	Outputs strobe signals for the PLL IC.
47	PDA	Outputs data signals to the PLL IC. Input port for PLL unlock signal from PLL IC (RF unit; IC3).
48	DBL2	Output control signal for the doubler circuit. Low : Activates the 2nd doubler circuit.
50	300MC	Outputs low-pass filter select signal. Low : When frequencies 30 to 118 MHz or 175 to 330 MHz are displayed.
51	GC	Outputs band-pass filter select signal. Low : When frequencies 833 to 1309.995 MHz are displayed.
52	800MC	Outputs band-pass filter select signal. Low : When frequencies 470 to 1027 MHz are displayed.
53	UHFC	Outputs band-pass filter select signal. Low : When frequencies 330 to 470 MHz are displayed.
54	VHFC	Outputs band-pass filter select signal. Low : When frequencies 118 to 175 MHz are displayed.

Pin number	Port name	Description
55	SHIFT	Output port for 1st VCO SHIFT signals to the shift switch (RF unit; Q29). High : Shift ON (380 – 550 MHz). Low : Shift OFF (267.2 – 380 MHz).
56	HFC	Output control signal for the 0.5–30 MHz band RF amplifier. Low : Receiving 0.5–30 MHz bands.

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PREPARATION

The receiver (IC-R2) must be adjusted on the adjustment mode after programmed adjustment frequency data into memory channel. When you program adjustment frequency data into memory channel, optional CS-R2 PROGRAMMING SOFTWARE, OPC-478 CLONING CABLE are required.

■ REQUIRED TEST EQUIPMENT

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 3.0 V DC Current capacity : 1 A or more	Frequency counter	Frequency range : 0.1–600 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better
AC millivoltmeter	Measuring range : 10 mV–10 V		Frequency range : 0.1–1300 MHz Output level : 0.1 µV–32 mV (-127 to -17 dBm)
External speaker	Input impedance : 8 Ω Capacity : 1 W or more	Standard signal generator (SSG)	

■ SOFTWARE INSTALLATION

NOTE: Before using the program, make a backup copy of the original disk. After making a backup copy, keep the original disk in a safe place.

- ① Boot up DOS.
- ② Insert the backup disk into the floppy drive A.
- ③ Type the following to install the adjustment program:
A:>INSTALL A C:\CSR2 [Enter]

■ ADJUSTMENT FREQUENCY DATA

When program adjustment frequency data (at right) into memory channel, back up the original memory data using the optional CS-R2, OPC-478, and re-program it after adjustment.

CAUTION: When clone the adjustment frequency data to the receiver, the receiver's memory channel will be overwritten the data and deleted original memory data at same time.

■ ENTERING THE ADJUSTMENT MODE

- ① Connect a JIG (see illustration at CONNECTION) to the [SP] jack.
- ② Push and hold [FUNC], then turn power ON.
- ③ Disconnect the JIG and connect a PC with an OPC-478.
- ④ Boot up DOS.
- ⑤ Type the following to start up the adjustment program:
C:>CD CSR2 [Enter]
C:\CSR2>**CSR2** [Enter]

- Main menu appears at the top side of the cloning program, select the sub-menu "Screen"–"Memory CH"–"Bank 1", then input adjustment frequency (at right).
- ⑥ Select "Write → Receiver" of the Clone on the top menu.
 - Application writes adjustment frequency data to the connected receiver.
- ⑦ Disconnect the cloning cable and turn power OFF, then turn power ON to start adjustment.

• ADJUSTMENT FREQUENCY

Channel No.	Frequency [MHz]	Display ch. No.
0	280.100	FR
1	145.600	tk
2	435.600	tk
3	14.100	RS
4	145.100	RS
5	200.100	RS
6	435.100	RS
7	650.100	RS
8	1100.100	RS

NOTE: Adjustment frequency data must be programmed into proper channels, don't turn the order of channels, otherwise adjustment value will be wrong.

■ OPERATING ON THE ADJUSTMENT MODE

- Change the value : [DIAL]
Change the channel [UP] : [BAND]
Change the channel [DOWN] : [BAND]

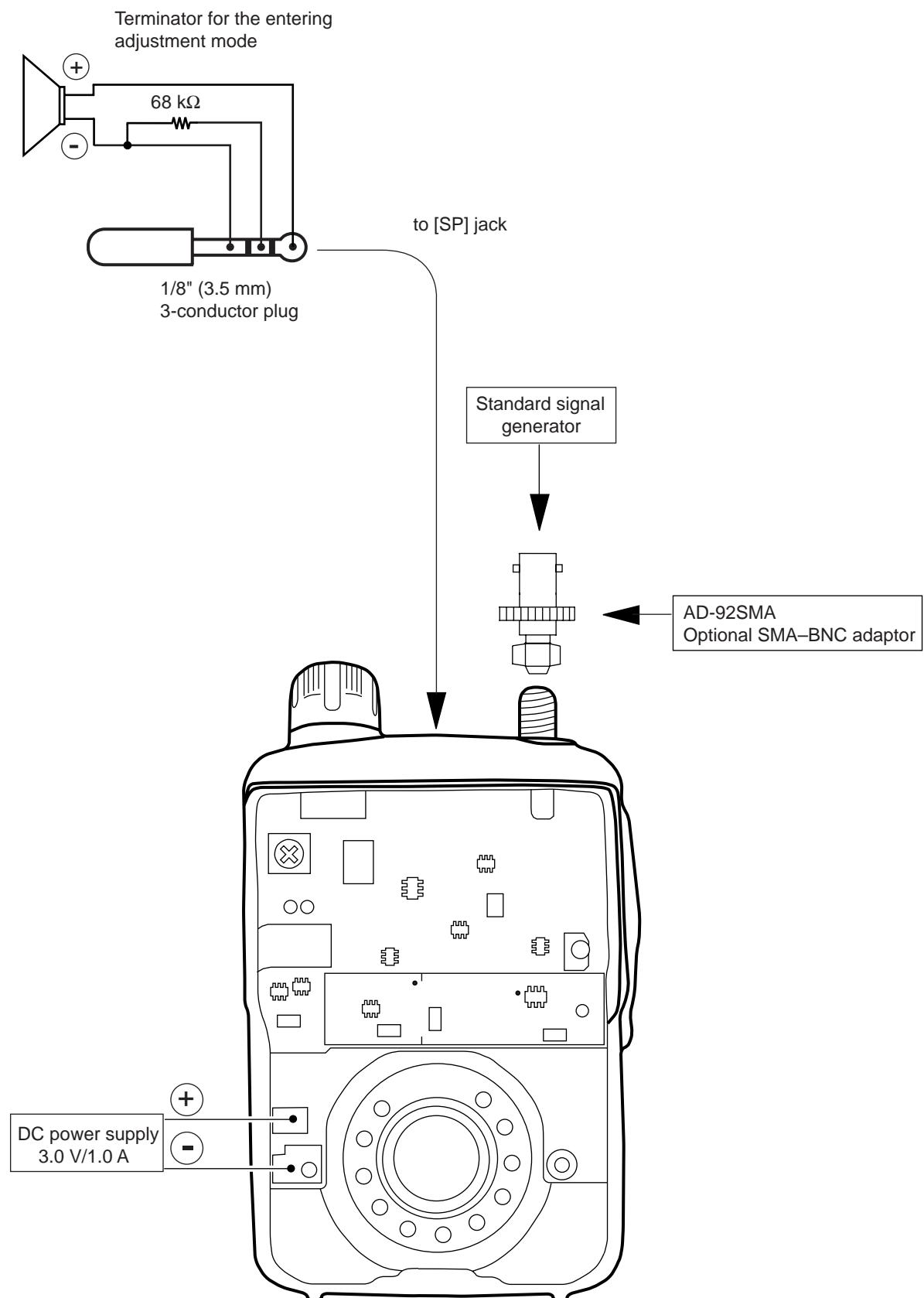
■ EXITING THE ADJUSTMENT MODE

When the adjustment is finished, the receiver must be cancelled adjustment mode to use normal operation, otherwise receiver does not work properly.

- ① Turn power OFF.
- ② Push and hold [FUNC] and [V/M], then turn power ON.

NOTE: All memory data except adjustment value will be cleared at this operation.

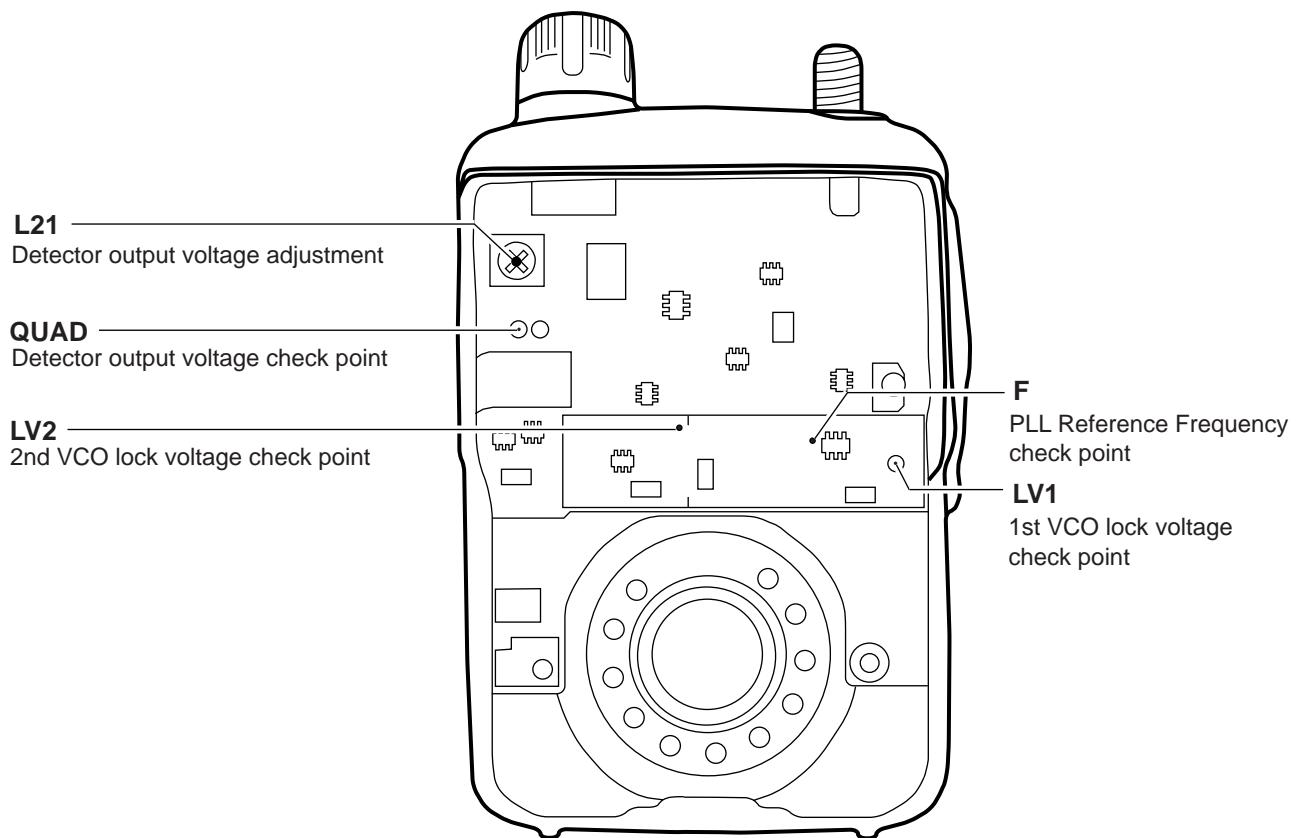
■ CONNECTION



5-2 PLL ADJUSTMENT

ADJUSTMENT	ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
		UNIT	LOCATION		UNIT	ADJUST
1ST VCO LOCK VOLTAGE (SHIFT ON)	1	• Displayed frequency : 493.300 MHz • Receiving	RF Connect the digital multi-meter to the check point LV1.	1.9 V – 2.9 V	Verify	
	2	• Displayed frequency : 282.900 MHz • Receiving		less than 12 V		
	1	• Displayed frequency : 0.495 MHz • Receiving		1.4 V – 2.4 V		
	2	• Displayed frequency : 493.295 MHz • Receiving		less than 12 V		
2ND VCO LOCK VOLTAGE	1	• Displayed frequency : 430.000 MHz • Receiving	RF Connect the digital multi-meter to the check point LV2.	0.4 V – 1.0 V	LOGIC	[DIAL]
	2	• Displayed frequency : 493.300 MHz • Receiving		less than 2.5 V		
REFERENCE FREQUENCY	1	• Displayed frequency : (FR ch) 280.100 MHz • Receiving	RF Connect the frequency counter to the check point F.	546.7999 MHz – 546.8001 MHz	LOGIC	[DIAL]
DETECTOR OUTPUT VOLTAGE	1	• Displayed frequency : (tk ch) 145.600 MHz • Connect an SSG to the antenna connector and set as: Level : 1 mV* (60 dB μ) Deviation : \pm 3.5 kHz Modulation : 1 kHz • Receiving	RF Connect the digital multi-meter to check point QUAD.	1.0 V	RF	L21

*This output level of the standard signal generator (SSG) is indicated as SSG's open circuit.

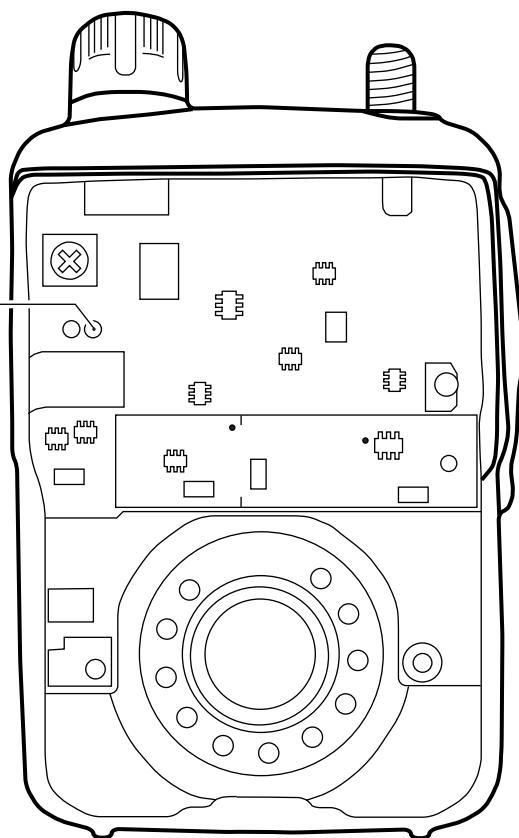


5-3 RECEIVER ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
			UNIT	LOCATION		UNIT	ADJUST
VHF SENSITIVITY	1	<ul style="list-style-type: none"> • Displayed frequency : (tk ch) 145.600 MHz • Connect an SSG to the antenna connector and set as : <ul style="list-style-type: none"> Level : 1 μV* (-107 dBm) Modulation : 1 kHz Deviation : \pm3.5 kHz • Receiving 	RF	Connect the DC voltmeter to the check point SEN.	Maximum DC voltage	LOGIC	[DIAL]
UHF SENSITIVITY	1	<ul style="list-style-type: none"> • Displayed frequency : (tk ch) 435.600 MHz • Connect an SSG to the antenna connector and set as : <ul style="list-style-type: none"> Level : 1 μV* (-107 dBm) Modulation : 1 kHz Deviation : \pm3.5 kHz • Receiving 	RF	Connect the DC voltmeter to the check point SEN.	Maximum DC voltage	LOGIC	[DIAL]
S-METER	1	<ul style="list-style-type: none"> • Displayed frequency : (RS ch) 14.100 MHz • Connect the SSG to the antenna connector and set as : <ul style="list-style-type: none"> Level : 0.5 μV* (-113 dBm) Modulation : 1 kHz Deviation : \pm 3.5 kHz • Receiving 			<ul style="list-style-type: none"> Push and hold the [MOD] key. • Verify that S-Meter shows S4 (3dots). 		
	2	<ul style="list-style-type: none"> • Displayed frequency : (RS ch) 145.100 MHz • Set the SSG as : <ul style="list-style-type: none"> Level : 0.5 μV* (-113 dBm) • Receiving 					
	3	<ul style="list-style-type: none"> • Displayed frequency : (RS ch) 200.100 MHz • Set the SSG as : <ul style="list-style-type: none"> Level : 0.5 μV* (-113 dBm) • Receiving 					
	4	<ul style="list-style-type: none"> • Displayed frequency : (RS ch) 435.100 MHz • Set the SSG as : <ul style="list-style-type: none"> Level : 0.5 μV* (-113 dBm) • Receiving 					
	5	<ul style="list-style-type: none"> • Displayed frequency : (RS ch) 650.100 MHz • Set the SSG as : <ul style="list-style-type: none"> Level : 0.5 μV* (-113 dBm) • Receiving 					
	6	<ul style="list-style-type: none"> • Displayed frequency : (RS ch) 1100.100 MHz • Set the SSG as : <ul style="list-style-type: none"> Level : 1 μV* (-107 dBμ) • Receiving 					

*This output level of the standard signal generator (SSG) is indicated as SSG's open circuit.

SEN
VHF and UHF sensitivity check point.



[RF UNIT]

REF NO.	ORDER NO.	DESCRIPTION	
C665	4030014200	S.CERAMIC	ECUE1H101JCQ
C666	4030014470	S.CERAMIC	ECUE1E391KBQ
C667	4030009820	S.CERAMIC	C1005 JB 1C 103K-T-A
J1	6510020550	S.CONNECTOR	AXK6S40445P
EP1	0910050763	PCB	B 5163C

S.=Surface mount

SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

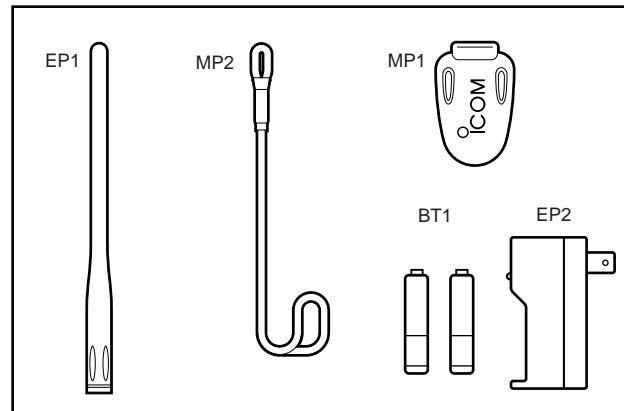
7-1 CABINET PARTS

[CHASSIS PARTS]

REF. NO.	ODER NO.	DESCRIPTION	QTY.
J1	6510020950	Connector SMA-R226	1
SP1	2510000960	Speaker K036NA500-26A27	1
MP1	8210015690	1995 Front panel (C)	1
MP2	8210014981	1995 Rear panel-1	1
MP3	8110006280	1995 BATT cover	1
MP4	8930044211	1995 7-Key-1	1
MP5	8930047620	2127 PTT rubber	1
MP6	8930047610	2127 Jack cap	1
MP7	8310044470	1995 Window plate (A)	1
MP8	8010017352	1995 Chassis-2	1
MP9	8930011900	Sheet SP net (A)	1
MP10	8830000570	Screw (A)	1
MP11	8830001090	Screw (D)	1
MP13	8110006290	1995 Lock cover	1
MP14	8610010520	Knob N-262	1
MP15	8930044250	1995 BATT seal	1
MP22	8810009790	Screw PH B0 1.7X4NI-ZU (BT)	3
MP23	8810009560	Screw PH B0 2X6ZK (BT)	2
MP26	8930047470	1995 Mic sheet	1
MP27	8930043440	Sponge (EY)	1

[ACCESSORIES]

REF. NO.	ODER NO.	DESCRIPTION	QTY.
BT1	3030000420	NICD CEL [EUR], [USA], [CAN]	2
	3030000450	NICD CEL [OTH] only	2
EP1	3310002150	Antenna FA-S270C	1
EP2	0800005090	Chager BC-127A ACC [USA], [CAN] only	1
	0800005100	Chager BC-127D ACC [EUR], [OTH] only	1
MP1	8930044191	1995 Belt clip-1	1
MP2	8010011960	Handstrap	1



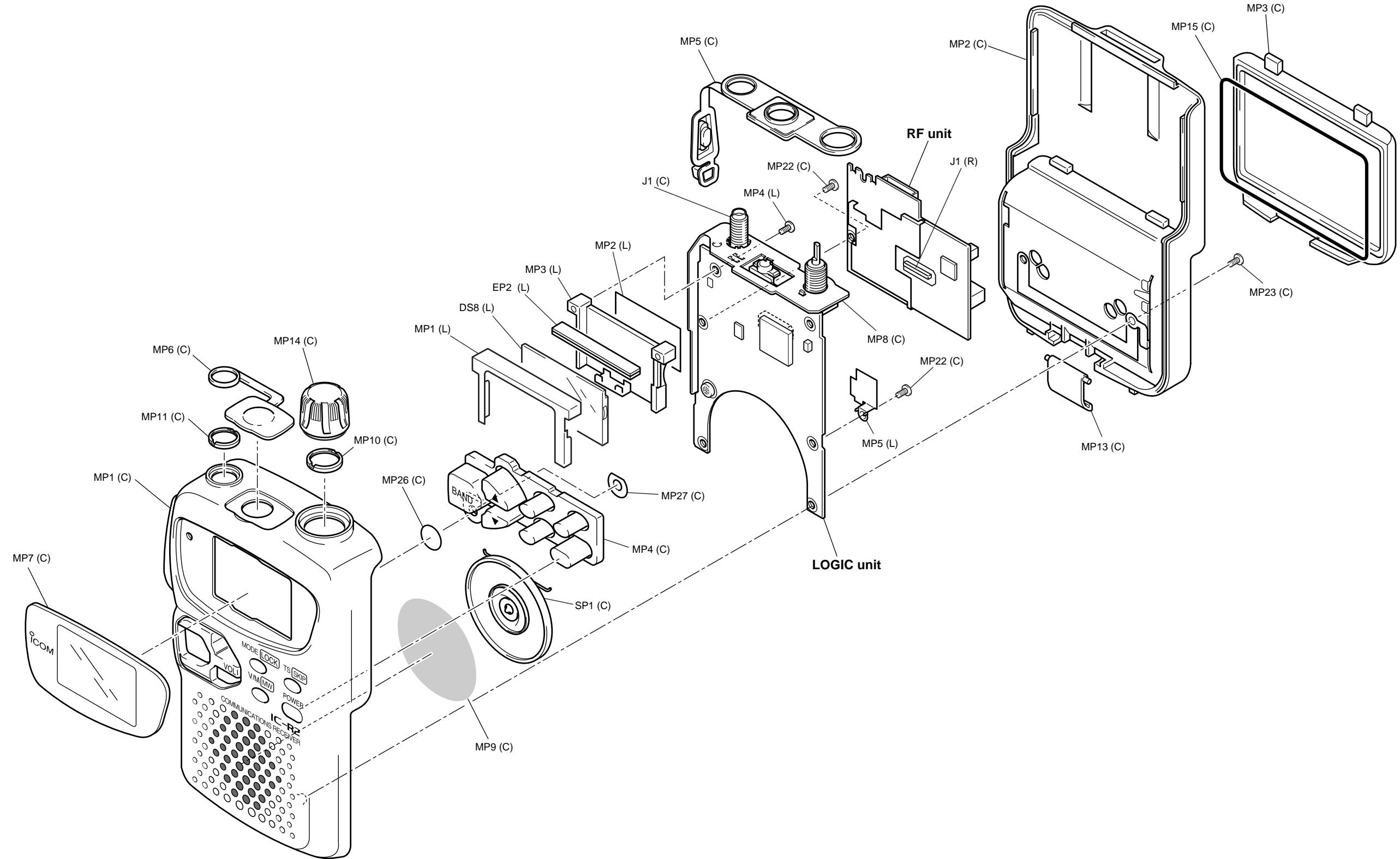
[LOGIC UNIT]

REF. NO.	ODER NO.	DESCRIPTION	QTY.
DS8	5030001610	LCD DLC-7995	1
EP2	8930046581	LCD contact	1
MP1	8930044290	1995 LCD holder	1
MP2	8930046400	1995 LCD sheet	1
MP3	8210015420	1995 Reflector	1
MP4	8810009790	Screw PH B0 1.7X4NI-ZU (BT)	2
MP5	8510012030	2127 Shield case	1

[RF UNIT]

REF. NO.	ODER NO.	DESCRIPTION	QTY.
J1	6510020550	S.Connector AXK6S40445P	1

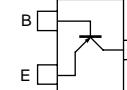
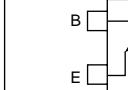
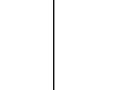
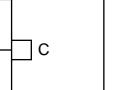
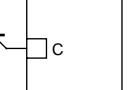
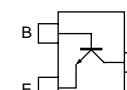
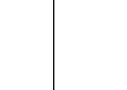
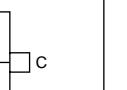
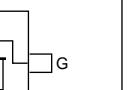
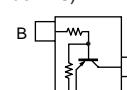
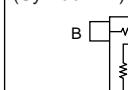
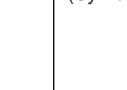
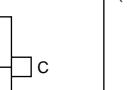
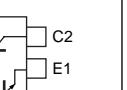
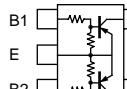
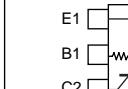
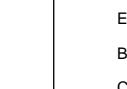
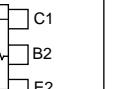
Screw abbreviations A, B0, BT: Self-tapping
PH: Pan head
FH: Flat head
BiH: Bind head
NI: Nickel
SUS: Stainless
ZK: Black



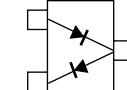
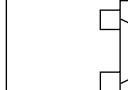
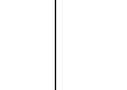
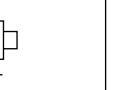
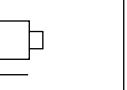
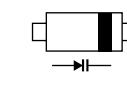
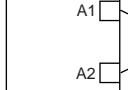
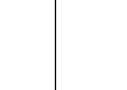
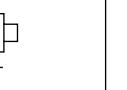
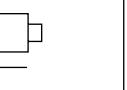
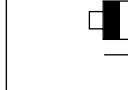
UNIT abbreviation (C): CHASSIS PARTS, (R): RF UNIT, (L): LOGIC UNIT

SECTION 8 SEMI-CONDUCTOR INFORMATION

• TRANSISTOR AND FET'S

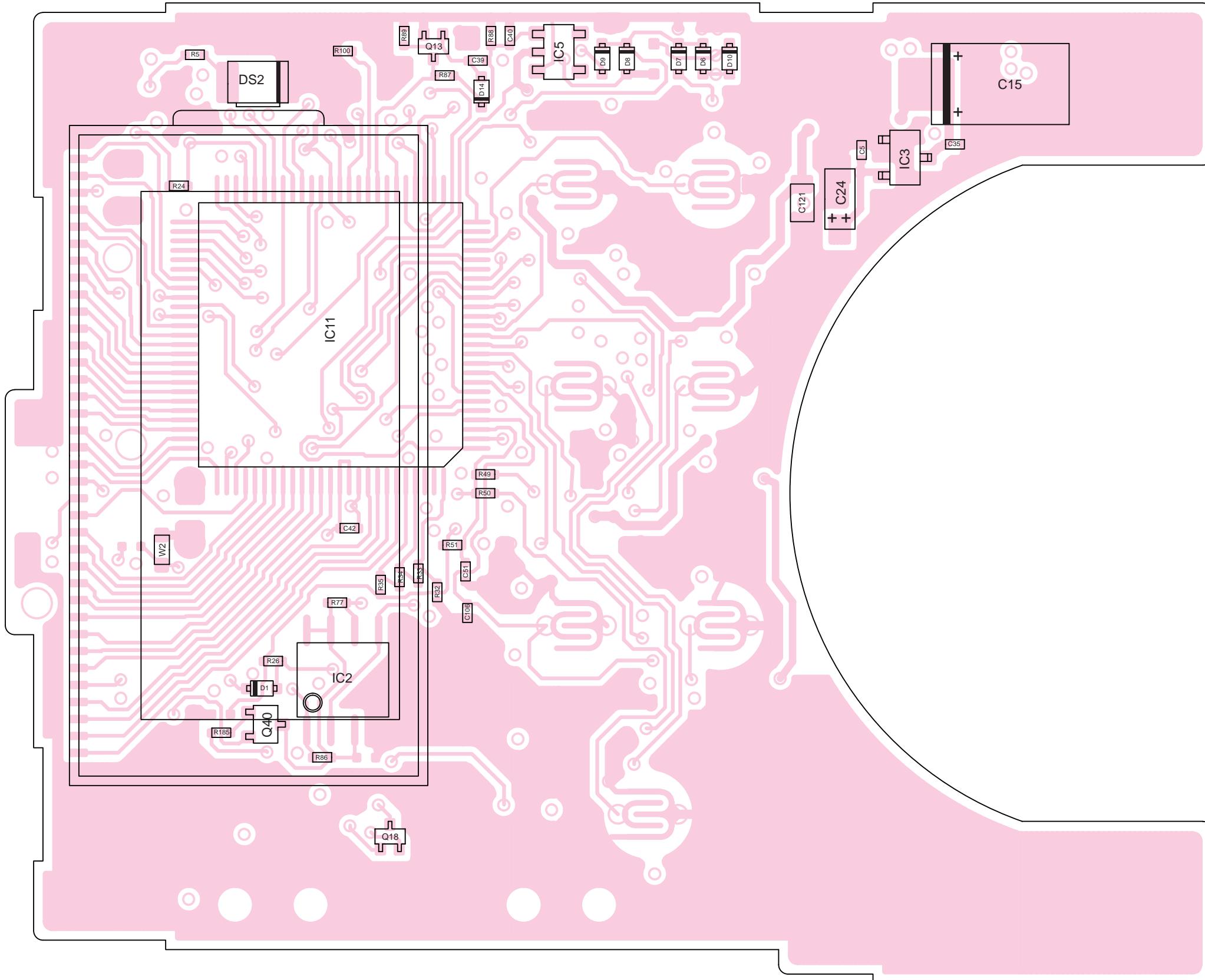
2SA1588 GR (Symbol: A6)	2SC4081 S (Symbol: BS)	2SC4117 GR (Symbol: DG)	2SC4215 O (Symbol: QO)	2SC4617 S (Symbol: BR)
				
2SC5006 (Symbol: 24)	2SC5231 C8 (Symbol: C8)	2SC5277 D2 (Symbol: D2)	2SJ144 Y (Symbol: VX)	2SK880 Y (Symbol: XY)
				
DTA144EE (Symbol: 16)	DTC114EE (Symbol: 24)	DTC144EE (Symbol: 26)	FH102 (Symbol: 102)	μPA805T (Symbol: T82)
				
XP1113 (Symbol: 7L)	XP4213 (Symbol: 8S)	XP4312 (Symbol: 7T)	XP6501 AB (Symbol: 5N)	
				

• DIODES

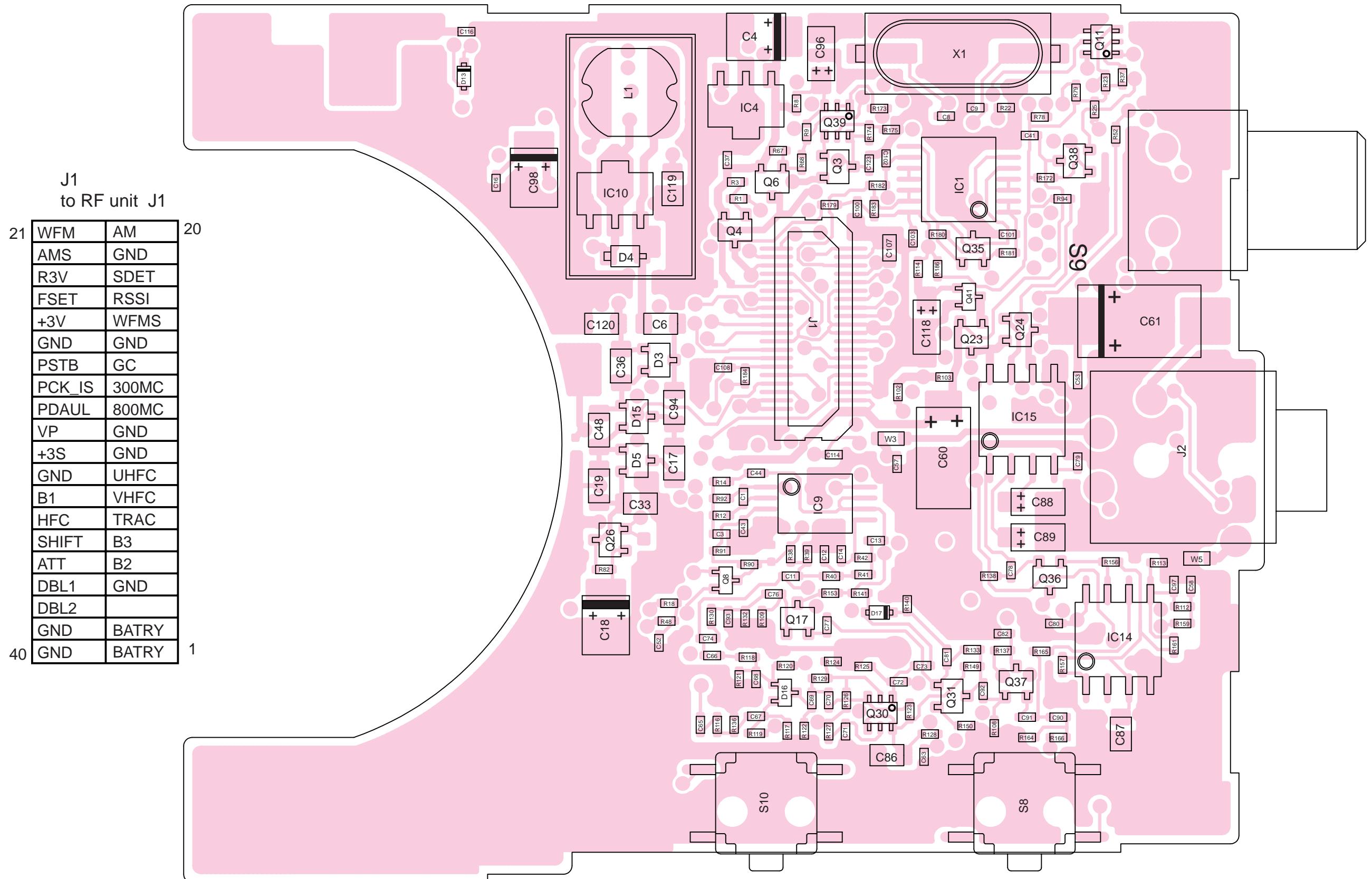
1SS372 (Symbol: N9)	1SV172 (Symbol: BE)	1SV286 (Symbol: T7)	1SV305 (Symbol: TV)	1SV308 (Symbol: TX)
				
HVU350 (Symbol: 4)	MA132WK (Symbol: MU)	MA2S077 (Symbol: S)	MA2S111 (Symbol: A)	MA6S718 (Symbol: M2N)
				
MA728 (Symbol: 2A)	MA729 (Symbol: 2B)			
				

SECTION 9 BOARD LAYOUTS

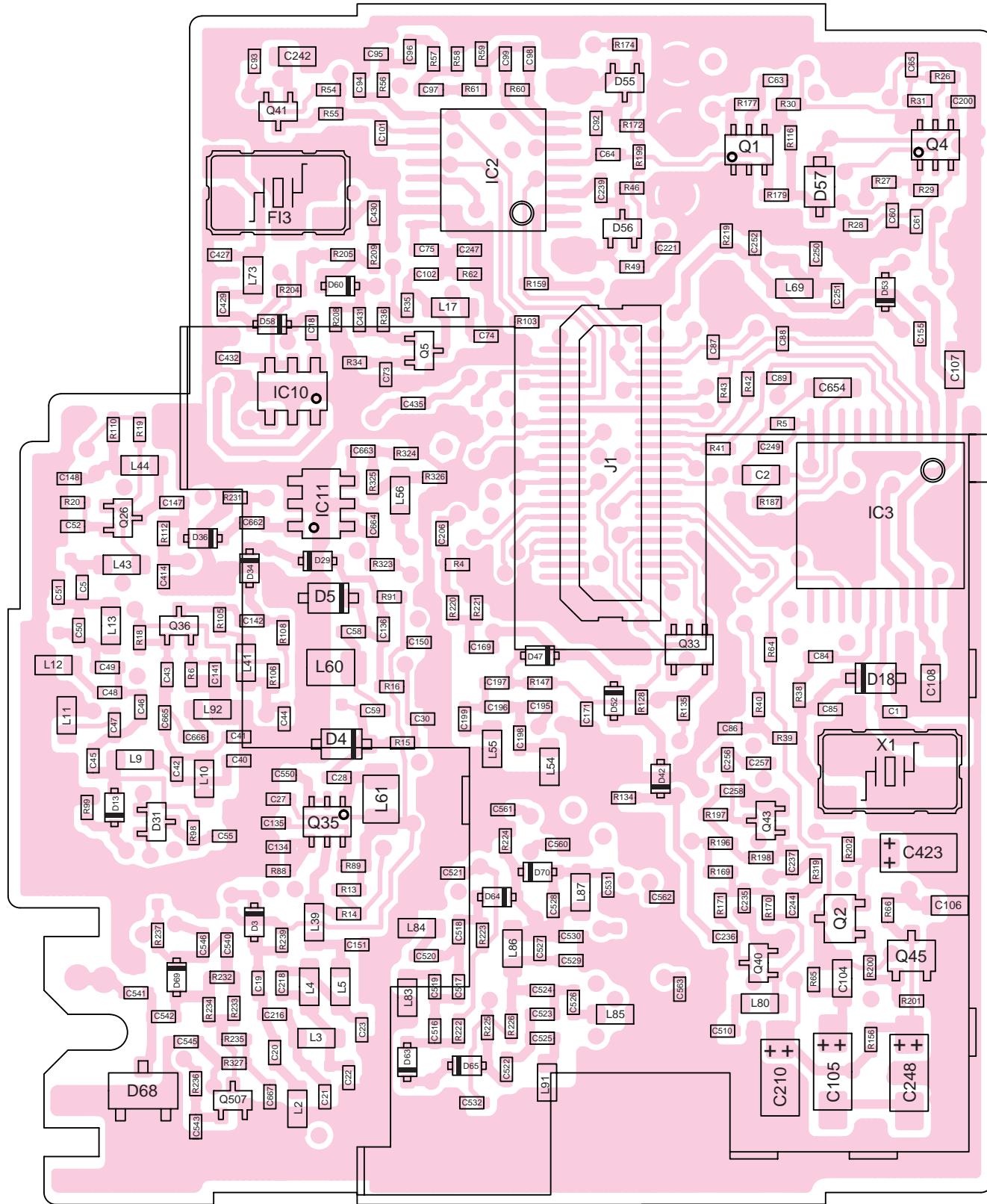
9 - 1 LOGIC UNIT • TOP VIEW



• BOTTOM VIEW



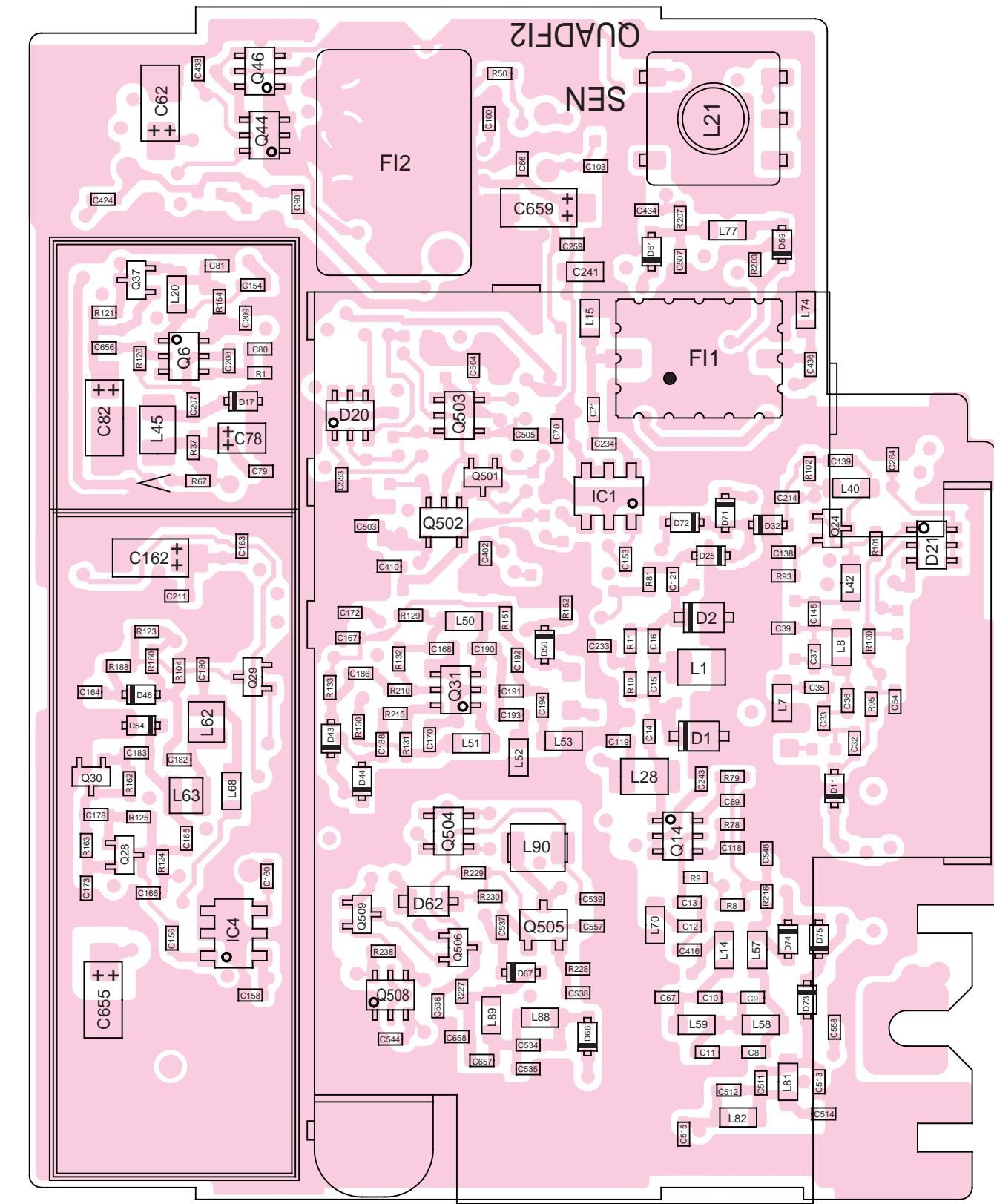
9 - 2 RF UNIT
• TOP VIEW



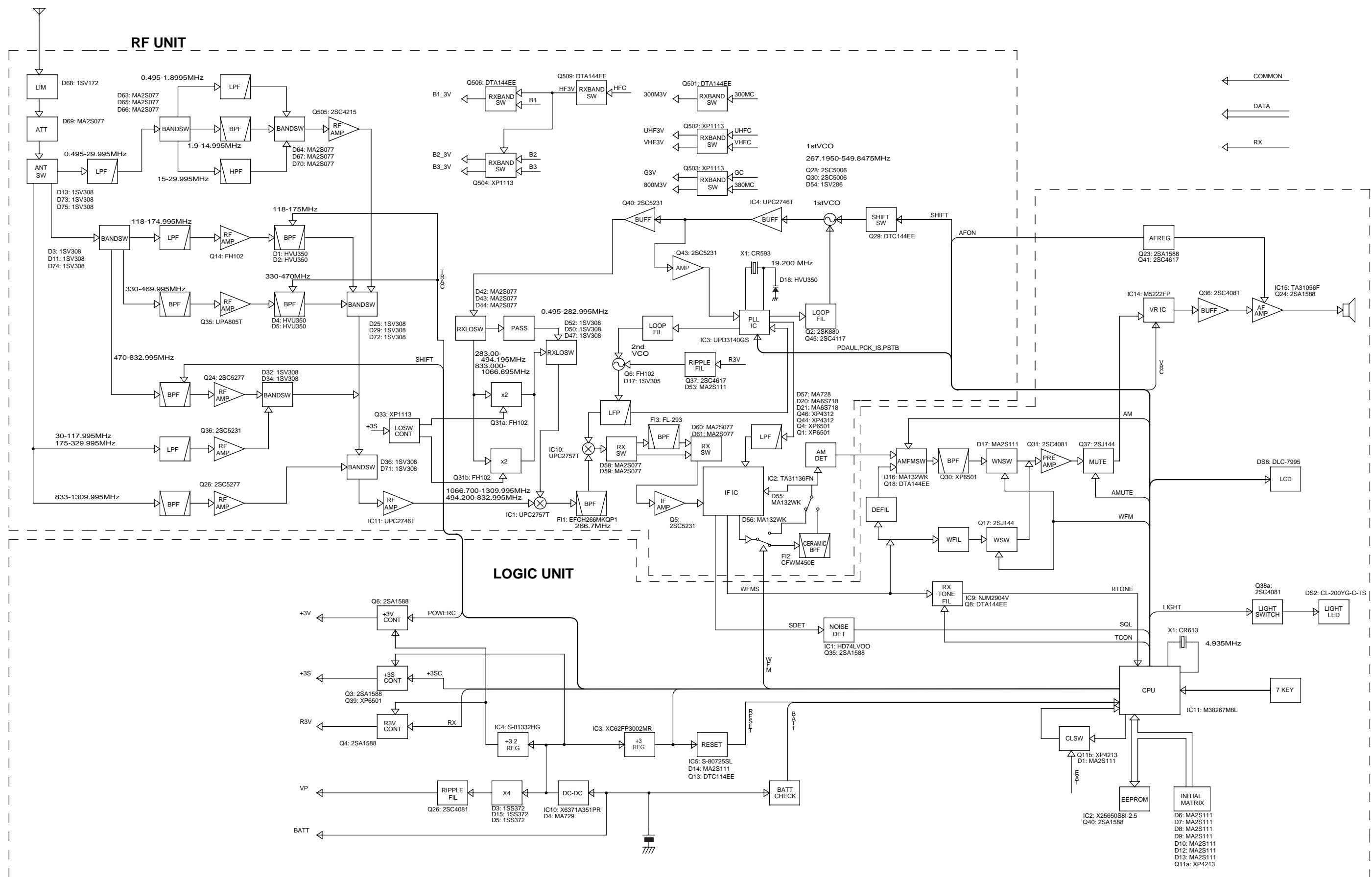
J1
to RF unit J1

20	AM	WFM	21
	GND	AMS	
SDET	R3V		
RSSI	FSET		
WFMS	+3V		
GND	GND		
GC	PSTB		
300MC	PCK_IS		
800MC	PDAUL		
GND	VP		
GND	+3S		
UHFC	GND		
VHFC	B1		
TRAC	HFC		
B3	SHIFT		
B2	ATT		
GND	DBL1		
GND	DBL2		
BATRY	GND		
1	BATRY	GND	40

• BOTTOM VIEW

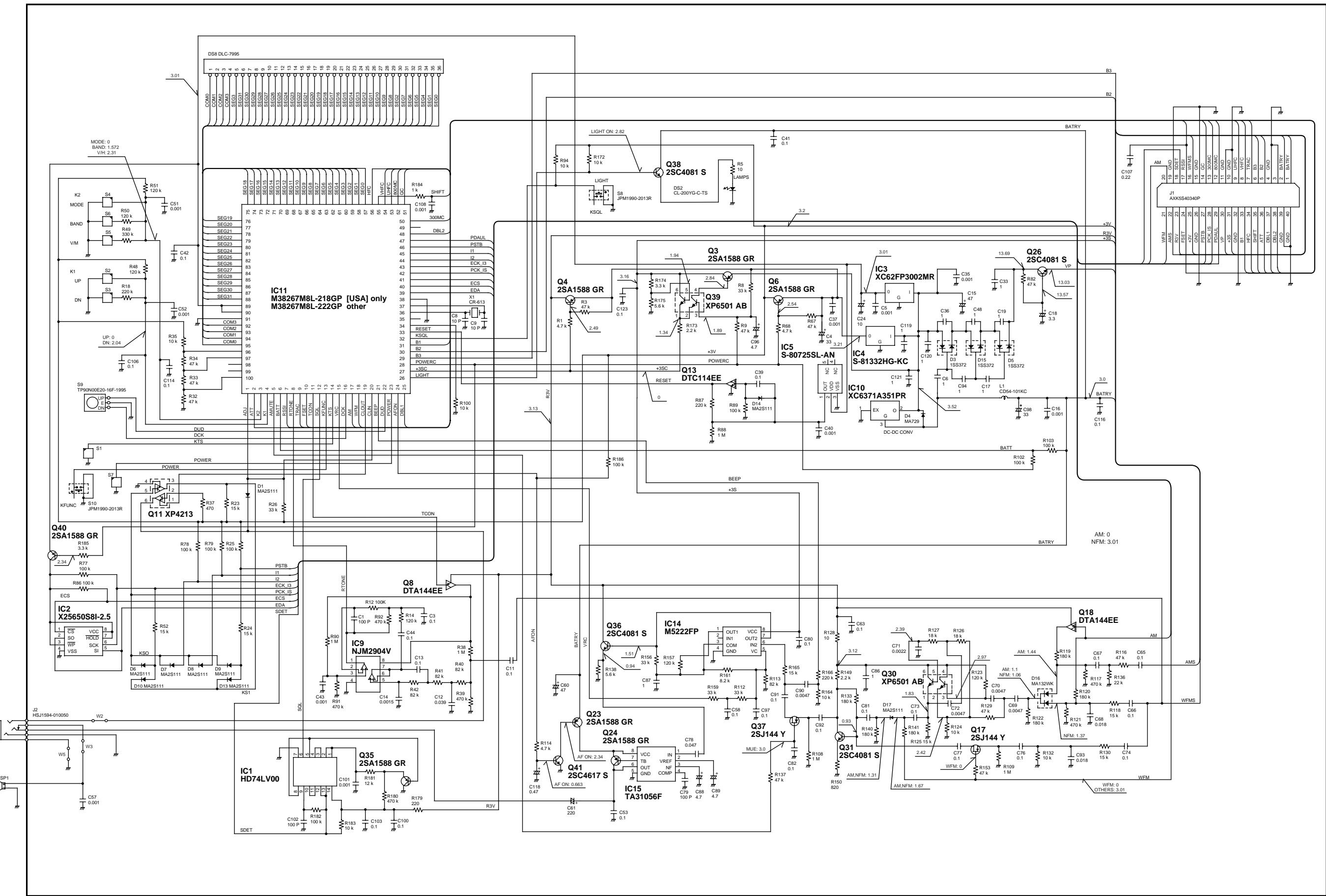


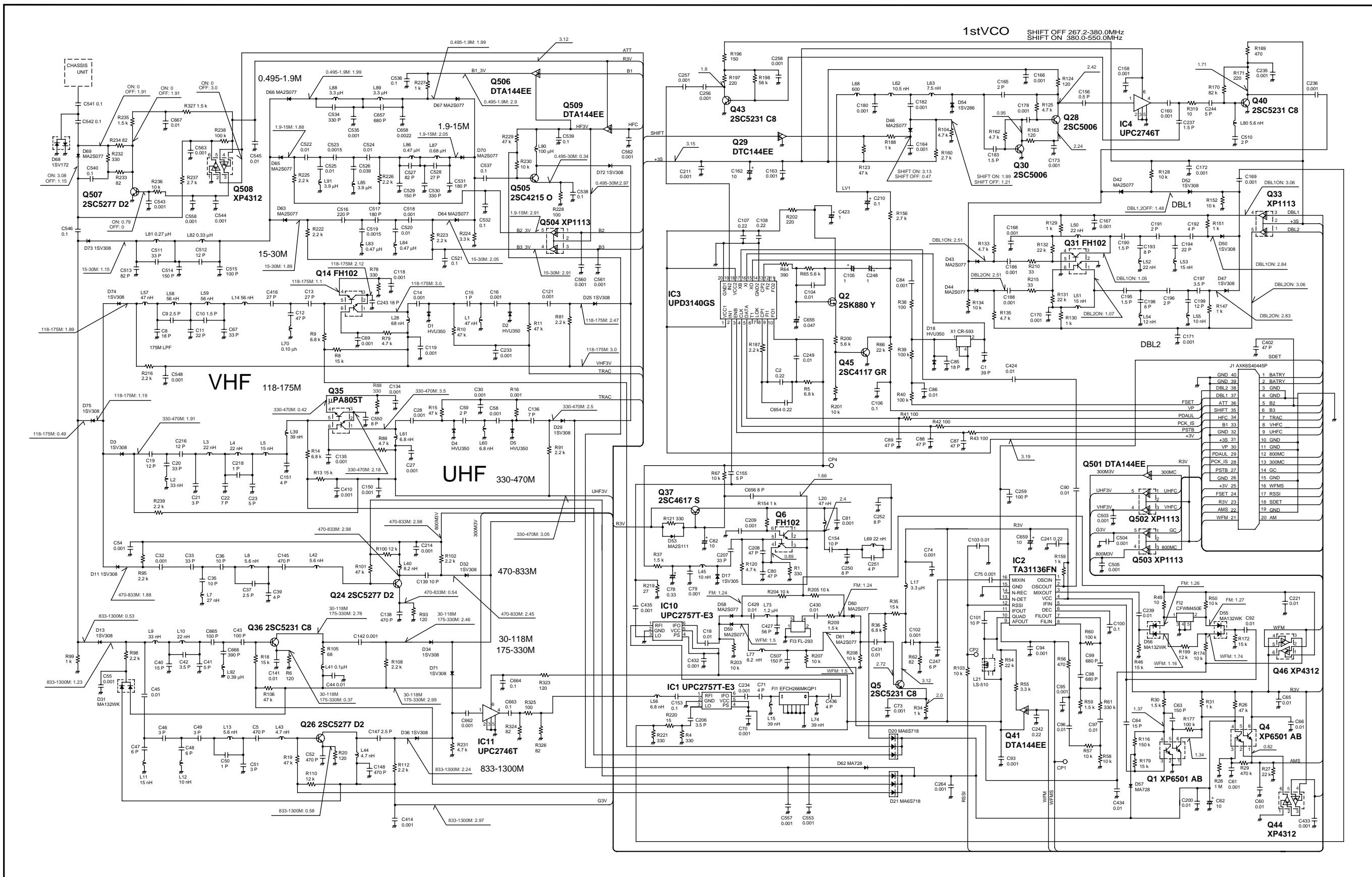
SECTION 10 BLOCK DIAGRAM



SECTION 11 VOLTAGE DIAGRAM

- LOGIC UNIT



• RF UNIT

Icom Inc.

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Fax : 06 6793 0013
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URL : <http://www.icomcanada.com>

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290-294 Albert Street, Brunswick, Victoria, 3056, Australia
Phone : 03 9387 0666 Fax : 03 9387 0022
URL : <http://www.icom.net.au>

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URL : <http://www.icomuk.co.uk>

Icom France S.a

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BP 5804, 31505 Toulouse Cedex, France
Phone : 561 36 03 03 Fax : 561 36 03 00
URL : <http://www.icom-france.com>

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