

 ICOM®

# SERVICE MANUAL

VHF TRANSCEIVER

**IC-V82**

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## INTRODUCTION

This service manual describes the latest service information for the **IC-V82 VHF TRANSCEIVER** at the time of publication.

MODEL	VERSION	SYMBOL	BATTERY PACK
IC-V82	USA	[USA-1]	BP-208N
		[USA-2]	BP-222N
		[USA-3]	BP-209N
	EUR	[EUR-1]	BP-208N
		[EUR-2]	BP-222N
		[EUR-3]	BP-209N
CSA	[CSA-1]	BP-208N	
	[CSA-2]	BP-222N	
	[CSA-3]	BP-209N	
	EXP	[EXP-1]	BP-208N
		[EXP-2]	BP-222N
		[EXP-3]	BP-209N
		[EXP-4]	BP-209N

To upgrade quality, any electrical or mechanical parts and internal circuits are subject to change without notice or obligation.

## DANGER

**NEVER** connect the transceiver to an AC outlet or a DC power supply that uses more than 10.3 V. This will ruin the transceiver.

**DO NOT** expose the transceiver to rain, snow or any liquids.

**DO NOT** reverse the polarities of the power supply when connecting the transceiver.

**DO NOT** apply an RF signal of more than 20 dBm (100 mW) to the antenna connector. This could damage the transceiver's front-end.

## ORDERING PARTS

Be sure to include the following four points when ordering replacement parts:

1. 10-digit order numbers
2. Component part number and name
3. Equipment model name and unit name
4. Quantity required

### <SAMPLE ORDER>

1110003490 S.IC TA31136FN IC-V82 MAIN UNIT 1 piece  
8210021290 2826 front panel IC-V82 CHASSIS 5 pieces

Addresses are provided on the inside back cover for your convenience.

## REPAIR NOTES

1. Make sure the problem is internal before disassembling the transceiver.
2. **DO NOT** open the transceiver until the transceiver is disconnected from its power source.
3. **DO NOT** force any of the variable components. Turn them slowly and smoothly.
4. **DO NOT** short any circuits or electronic parts. An insulated tuning tool **MUST** be used for all adjustments.
5. **DO NOT** keep power ON for a long time when the transceiver is defective.
6. **DO NOT** transmit power into a signal generator or a sweep generator.
7. **ALWAYS** connect a 40 dB or 50 dB attenuator between the transceiver and a deviation meter or spectrum analyzer when using such test equipment.
8. **READ** the instructions of test equipment thoroughly before connecting equipment to the transceiver.



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# SECTION 1 SPECIFICATIONS

## ■ GENERAL

• Frequency range	: TX 144.000–148.000 MHz 144.000–146.000 MHz 136.000–174.000 MHz*	[USA] [EUR] [EXP], [CSA]
	: RX 136.000–174.000 MHz* 144.000–146.000 MHz	[USA], [EXP], [CSA] [EUR]
*Specifications are guaranteed within 144.000 to 148.000 MHz range only.		
• Operating temperature range	: –10°C to 60°C; +14°F to +140°F	
• Operating mode	: F2D, F3E, F7W* (*with optional digital unit <b>UT-118</b> )	
• Frequency stability	: ±2.5 ppm (–10°C to +60°C; +14°F to +140°F)	
• Antenna impedance	: 50 Ω (BNC Type)	
• Power supply requirement	: Specified Icom's battery pack only (Operating voltage range; 6.0–10.3 V)	
• Number of memory channels	: 207 channels (Including 6 scan edges and 1 call channel)	
• Scan types	: Program/Memory/Skip/Priority/Tone scans	
• Tuning steps	: 5, 10, 12.5, 15, 20, 25, 30 and 50 kHz	
• Current drain (at 7.2 V DC; approx.)	: TX High 2.6 A Middle 2.0 A Low 1.0 A  RX Max. audio Less than 250 mA Stand-by Less than 80 mA Power save Less than 30 mA	
• Dimensions (Projections not included)	: 54.0 (W) × 139.0 (H) × 41.1 (D) mm; 2 1/8 (W) × 5 15/32 (H) × 1 5/8 (D) in.	
• Weight (except antenna, battery pack)	: Approx. 200 g (7 5/32 oz)	
• Data connector	: 3-conductor 2.5 (d) mm (1/10")	

## ■ TRANSMITTER

• Output power (at 7.2 V DC)	: 7.0 W (High), 4.0 W (Middle), 0.5 W (Low)
• Modulation system	: Variable reactance frequency modulation
• Maximum deviation	: ±2.5 kHz (Narrow), ±5.0 kHz (Wide)
• Spurious emissions	: Less than –60 dBc
• Ext. microphone connector	: 3-conductor 2.5 (d) mm (1/10")/2.2 kΩ

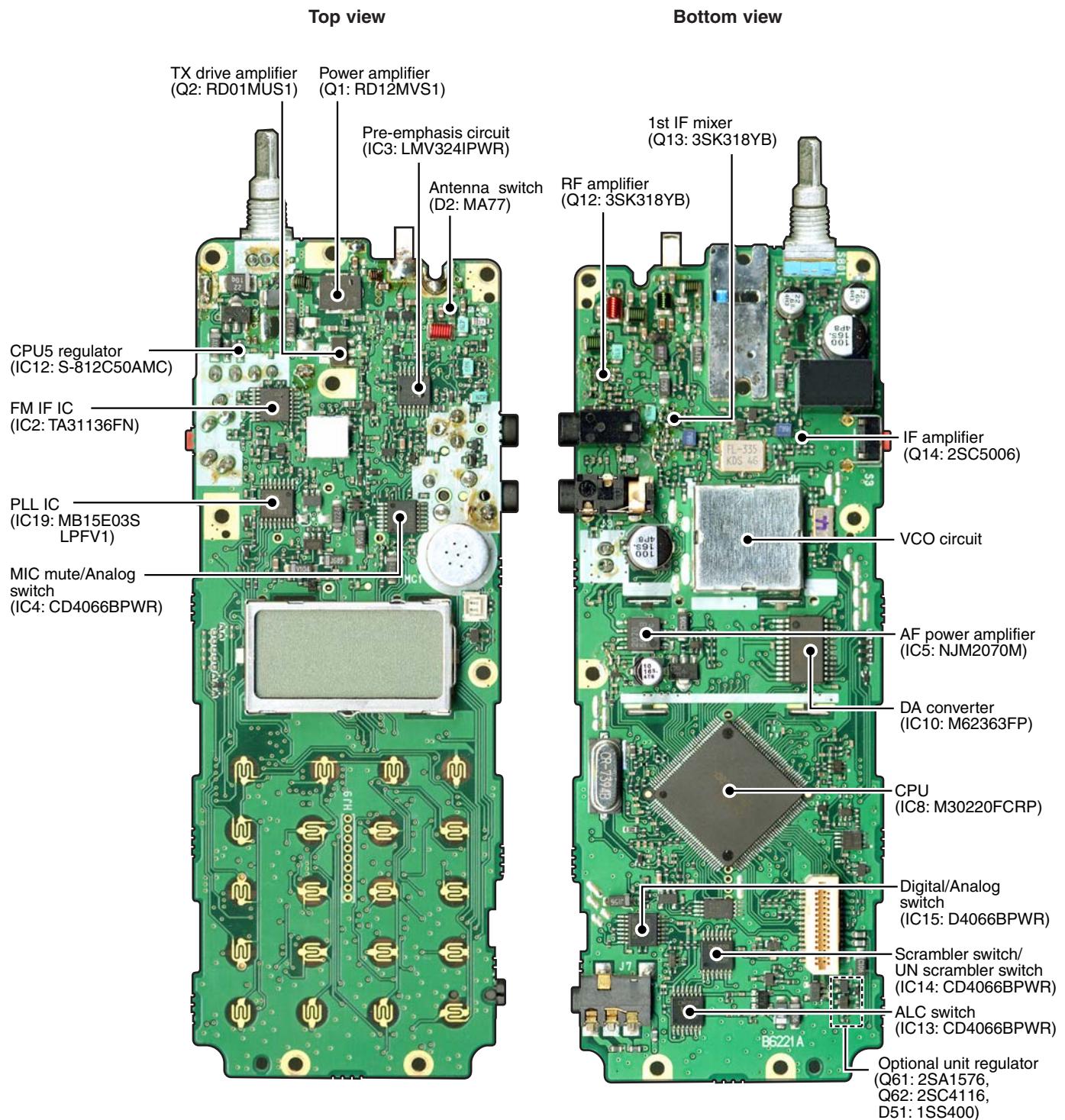
## ■ RECEIVER

• Receiving system	: Double conversion superheterodyne system
• Intermediate frequencies	: 1st; 46.35 MHz, 2nd; 450 kHz
• Sensitivity	: Less than –14 dBμ at 12 dB SINAD (0.16 μV typ.)
• Squelch sensitivity (at threshold)	: Less than –16 dBμ (0.11 μV typ.)
• Selectivity	: More than 55 dB (Wide; 65 dB typ.) More than 50 dB (Narrow)
• Intermodulation	: More than 55 dB (65 dB typ.)
• Spurious image rejection	: More than 60 dB (80 dB typ.)
• Audio output	: More than 300 mW at 10% distortion with an 8 Ω load
• Ext. speaker connector	: 3-conductor 3.5 (d) mm (1/8")/8 Ω

All stated specifications are subject to change without notice or obligation.

## SECTION 2 INSIDE VIEWS

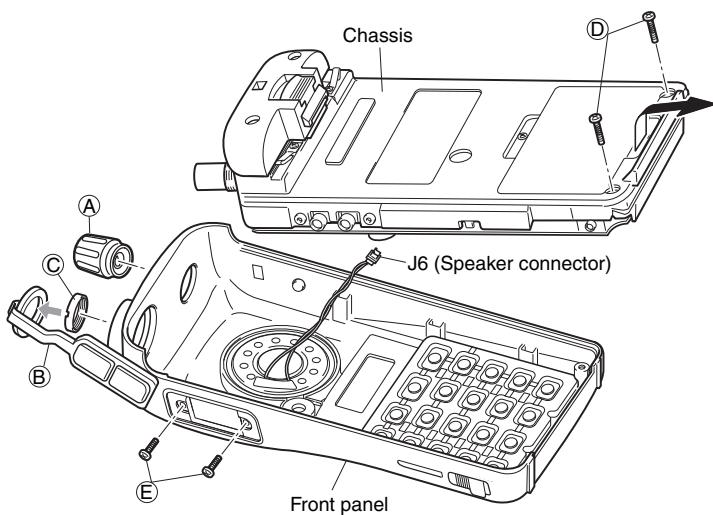
- MAIN UNIT



## SECTION 3 DISASSEMBLY INSTRUCTIONS

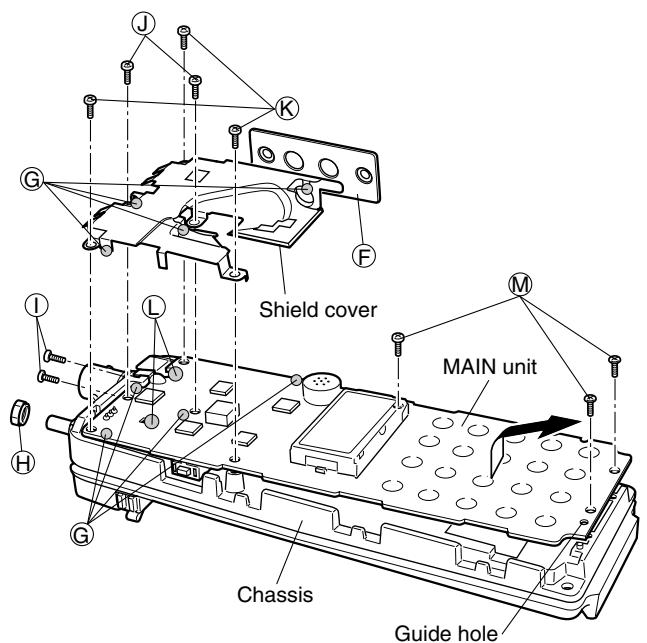
### 1. Removing the chassis panel

- ① Remove the knob (A) and jack cap (B).
- ② Unscrew 1 nut (C).
- ③ Unscrew 2 screws (D) ( $2 \times 10$  mm, black) and 2 screws (E) ( $2 \times 4$  mm, black) from the chassis.
- ④ Unplug the speaker connector (J6).
- ⑤ Take off the chassis in the direction of the arrow.



### 2. Removing the MAIN unit.

- ① Remove the Jack seal (F).
- ② Unsolder 4 points (G) of the shield cover.
- ③ Unscrew 1 nut (H) and 2 screws (I) ( $2 \times 4$  mm, black).
- ④ Unscrew 2 screws (J) ( $2 \times 4$  mm, black) and 3 screws (K) ( $2 \times 4$  mm, silver) and remove the shield cover.
- ⑤ Unsolder 2 points (L).
- ⑥ Unscrew 3 screws (M) ( $2 \times 4$  mm, silver).
- ⑦ Take off the MAIN unit in the direction of the arrow.



## SECTION 4 CIRCUIT DESCRIPTION

### 4-1 RECEIVER CIRCUITS

#### 4-1-1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit toggles receive line and transmit line. This circuit does not allow transmit signals to enter the receiver circuits.

Received signals from the antenna are passed through the low-pass filter (LPF: L1, L2, C1–C5) and applied to the  $\lambda/4$  type antenna switching circuit (D1, D2).

While receiving, no voltage is applied to D1 and D2. Thus, the receive line and the ground are disconnected and L15, L58, C52, C76 and C516 function as a two-stage LPF which leads received signals to the RF circuits via the limiter (D50).

#### 4-1-2 RF CIRCUITS

The RF circuits amplify received signals within the range of frequency coverage and filters off out-of-band signals.

The signals from the antenna switching circuit are passed through a tunable bandpass filter (BPF: D9, L16, C79, C81), then applied to the RF amplifier (Q12).

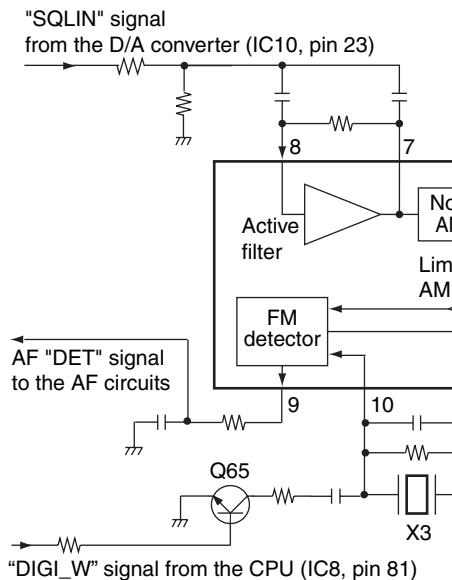
The amplified signals are passed through the limiter (D72) and another two-stage BPF (D11, D12, D65, L19, L57, C92, C94, C96, C97, C502–C505, C507) to suppress unwanted signals. The filtered signals are then applied to the 1st mixer circuit.

#### 4-1-3 1st MIXER AND 1st IF AMPLIFIER CIRCUITS

The 1st mixer circuit converts received signals into the 1st intermediate frequency (IF) signal by mixing with the local oscillator (LO) signal. The converted 1st IF signal is filtered at the 1st IF filter, then amplified at the 1st IF amplifier.

The signals from the two-stage BPF are converted into the 46.35 MHz 1st IF signal at the 1st mixer (Q13) by being mixed with the 1st LO signals generated at the VCO (Q76, D59, D60).

#### • 2ND IF AND DEMODULATOR CIRCUITS



The 1st IF signal from the 1st mixer is passed through the crystal filter (F11) to suppress unwanted signals, and the limiter (D63) and then applied to the 1st IF amplifier (Q14).

The amplified 1st IF signal is applied to the FM IF IC (IC2, pin 16).

#### 4-1-4 2nd IF AND DEMODULATOR CIRCUITS

The 1st IF signal is converted into the 2nd IF signal and demodulated by the FM IF IC. The FM IF IC contains 2nd mixer, limiter amplifier, quadrature detector, etc. in its package.

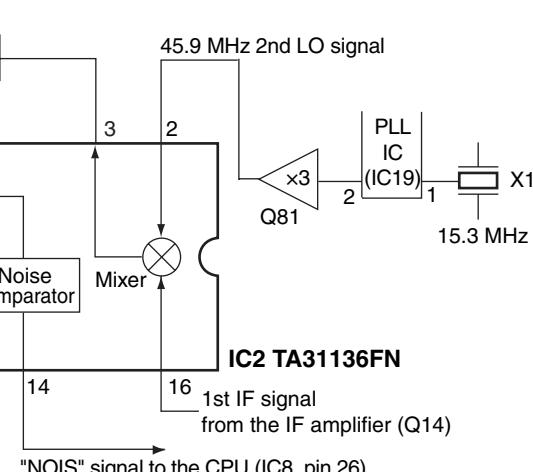
The 1st IF signal from the 1st IF amplifier is applied to the FM IF IC (IC2, pin 16), and mixed with the 45.9 MHz 2nd LO signal from the tripler (Q81) at the mixer section, to convert into the 450 kHz 2nd IF signal. The 2nd IF signal is output from pin 3 and is filtered by the ceramic filter (F12) to suppress the heterodyne noise. The filtered signal is applied to IC2 (pin 5) again and amplified at the limiter amplifier section and demodulated by the quadrature detector.

The quadrature detector is a detection method which uses a ceramic discriminator (X3). Q65 is a mode switch and toggles the detecting mode from wide and narrow, controlled by the "DIGI\_W" signal from CPU (IC8, pin 81).

The demodulated AF signals are output from pin 9.

#### 4-1-5 AF CIRCUITS

The AF signals from FM IF IC (IC2, pin 9) are passed through the AN switch (IC14, pins 10, 11), HPF (IC3, pins 6, 7), analog switch (IC4, pins 1, 2), the LPF (IC3, pins 13, 14) and analog switch (IC4, pins 10, 11). The signals from the analog switch are applied to the D/A converter (IC10, pins 11, 12) to adjust the AF output level, and then passed through the emphasis switch (Q73) which toggles the AF response characteristic according to the selected operating mode (analog/FM or digital). The AF signals from the emphasis switch are applied to the AF amplifier (IC5) to obtain 300 mW of AF output power. The amplified AF signals are applied to the internal speaker (SP1) via [SP] jack (J3).



## 4-1-6 SQUELCH CIRCUIT

Squelch circuit mutes AF output signal when no signals are received.

A portion of the AF signals from the FM IF IC (IC2, pin 9) are applied to the D/A converter (IC10, pin 24) to control its level. The level controlled signals are output from pin 23 and applied to the active filter (IC2, pins 7, 8; R86–R88, C121, C122). The filtered signals are applied to the noise amplifier section to amplify the noise components only.

The amplified noise components are detected at the noise detector section, and output from pin 13 as the "NOIS" signal and applied to the CPU (IC8, pin 26). Then the CPU outputs "AFON" signal from pin 71 according to the "NOIS" signal level to toggle the AF regulator (Q15, Q16) ON/OFF.

## 4-2 TRANSMITTER CIRCUITS

### 4-2-1 ALC AMPLIFIER AND PRE-EMPHASIS CIRCUIT

The ALC (Audio Level Control) amplifier maintains the level of the audio signals from the microphone constant. The pre-emphasis circuit amplifies the audio signals within +6 dB/oct pre-emphasis characteristic.

- When ALC function is ON.

The AF signals from the microphone are passed through the ALC switch (IC13, pins 3, 4) and applied to the ALC amplifier (IC17, pin 3) to limit its level.

The level limited signals are output from pin 5 and passed through the another ALC switch (IC13, pins 8, 9) and UN\_SEC switch (IC13, pins 10, 11). The signals from UN\_SEC switch are then applied to the pre-emphasis circuit (IC3, pins 8, 10) to obtain frequency characteristic of +6 dB/oct.

- When ALC function is OFF.

The audio signals from the microphone are passed through the ALC switch (IC13, pins 1, 2 and pins 10, 11) and UN\_SEC switch (IC13, pins 10, 11). The signals from UN\_SEC switch are then applied to the pre-emphasis circuit (IC3, pins 8, 10).

The signals from the pre-emphasis circuit are passed through the analog switch (IC4, pins 3, 4) and LPF (IC3, pins 13, 14). The signals from the LPF are passed through another analog switch (IC4, pins 8, 9), digital/analog switch (IC15, pins 8, 9 and pins 3, 4) and D/A converter (IC10, pins 21, 22) to adjust its level. The level adjusted signals from the D/A converter are applied to the modulator circuit (D61).

### 4-2-2 MODULATOR CIRCUIT

The modulation circuit modulates the VCO oscillating signal with the audio signals from the microphone.

AF signals from the D/A converter (IC10, pin 22) are applied to the modulation circuit (D61) to modulate the oscillated signal by changing the reactance of D61 at the VCO (Q76, D59, D60).

### 4-2-3 TRANSMIT AMPLIFIERS

The VCO output signal is amplified to transmit power level by the transmit amplifiers .

The VCO output signal is buffer-amplified by the buffer amplifiers (Q74, Q75) and passes through the TX/RX switch (D3). The signals from the TX/RX switch are applied to the pre-driver (Q3), driver (Q2) and power (Q1) amplifiers, to be amplified to the transmit output power level.

The power amplifier output is applied to the antenna connector (J1: CHASSIS UNIT) via the antenna switching circuit (D1), power detector (D32, D33), and two-stage LPFs.

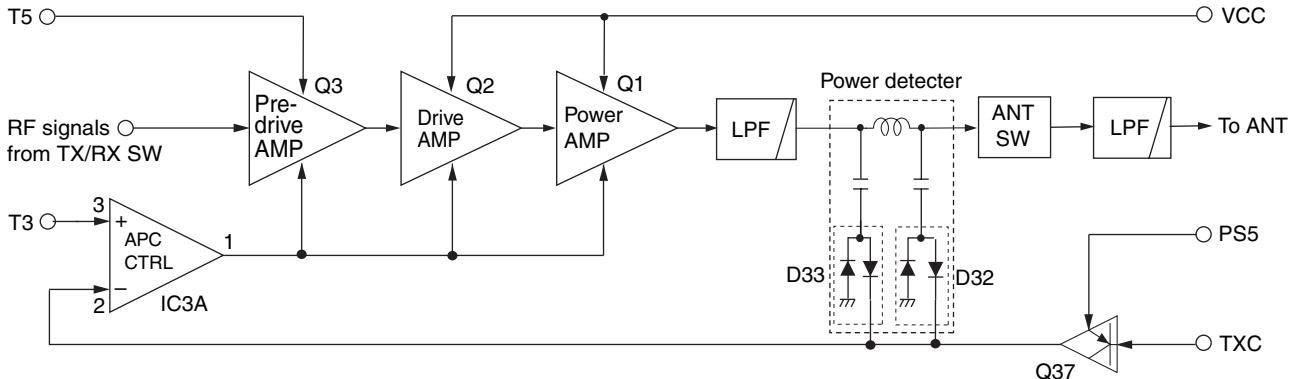
### 4-2-4 APC CIRCUIT

The APC (Automatic Power Control) circuit stabilizes transmit output power and controls transmit output power High, Middle and Low.

The RF output signal from the power amplifier (Q1) is detected at the power detector (D32, D33). The detector converts the RF signals into DC voltage, and the detected voltage is applied to the APC amplifier (IC3, pin 2).

The transmit output power setting voltage "T3" is applied to input terminal of the APC amplifier (IC3, pin 3) as the reference voltage. The APC amplifier controls the bias of the pre-driver (Q3), driver (Q2) and power amplifier (Q1) by comparing the detected voltage and the reference voltage. Thus the APC circuit maintains a constant output power.

## • APC CIRCUITS



## 4-3 PLL CIRCUITS

### 4-3-1 GENERAL

PLL circuits control the VCO circuit. IC19 is a PLL IC and contains prescaler, programmable counter, programmable divider, phase detector, charge pump in its package.

The VCO (Q76, D59, D60) directly generates both of the transmit frequency and the 1st LO frequency. The VCO shift circuit (Q77, D58) is used for switching the oscillating frequencies between transmit and receive.

While receiving, only L44 is connected to the VCO and the VCO generates the 1st LO frequency.

While transmitting, L44 and L45 are connected to the VCO to generate the transmit frequency.

The PLL sets the divided ratio based on the N-data from the CPU (IC8), and compares the phase of the VCO output with the reference frequency (15.3 MHz) generated by X4.

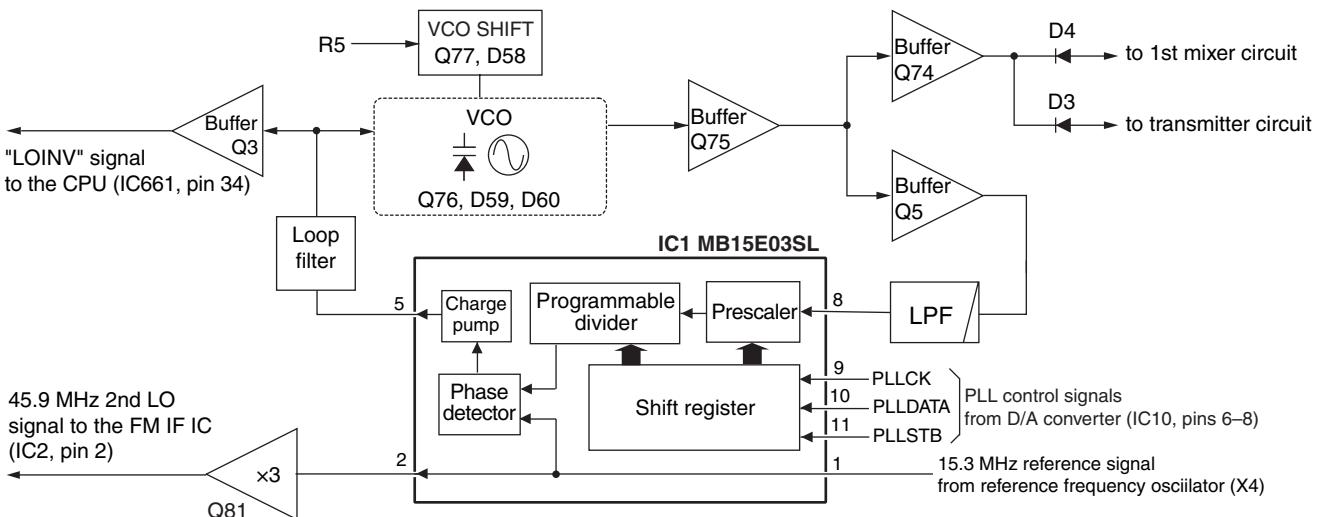
If the oscillated signal drifts, the phase of its frequency changes from the phase of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

### 4-3-2 TRANSMIT LOOP

A portion of the generated signal at the VCO (Q76, D59, D60) is applied to the PLL IC (IC19, pin 8) via buffer-amplifiers (Q5, Q75). The applied signal is divided at the prescaler section and programmable divider section, then applied to the phase detector section.

The phase detector compares the input signal with the reference frequency, and then outputs the control signal (pulse-type) from pin 5 via the charge pump section. The pulse-type signal is converted into DC voltage at the loop filter (R446-R448, C472-C474), and then applied to the VCO (Q76, D59, D60) as the lock voltage.

### • PLL CIRCUITS



### 4-3-3 RECEIVE LOOP

The generated 1st LO signal is applied to the PLL IC (IC19, pin 8) via the buffer-amplifiers (Q5, Q75) and is divided at the prescaler section and the programmable divider section, then applied to the phase detector section.

The phase detector compares the input signal with the reference frequency, and then outputs the control signal (pulse-type) from pin 5. The pulse-type signal is converted into DC voltage at the loop filter (R446-R448, C472-C474), and then applied to the VCO (Q76, D59, D60) as the lock voltage.

## 4-4 OTHER CIRCUITS

### 4-4-1 CTCSS/DTCS CIRCUIT (DECODING)

The CTCSS/DTCS signal from FM IF IC (IC2, pin 9) is filtered at the LPF (Q53). The filtered signal is then applied to the CPU (IC8, pin 5) to control the AF amplifier according to the received CTCSS/DTCS signal.

### 4-4-2 CTCSS/DTCS CIRCUIT (ENCODING)

#### • CTCSS

The CTCSS signal is generated by the CPU (IC8) and output from pin 139 and passed through the LPF (R224, C126, C129) and CTCSS switch (Q38). The CTCSS signal is then applied to the splatter filter (IC3, pin 13) to be mixed with the microphone audio signals. The filtered CTCSS signal is then output from pin 14 and applied to the digital/analog switch (IC15, pins 8, 9 and pins 3, 4) via the analog switch (IC4; pins 8, 9).

The CTCSS signal from the digital/analog switch (IC15, pin 3) is applied to the D/A converter (IC10, pin 21) to adjust its level. The level adjusted CTCSS signal is then applied to the modulator circuit (D61).

#### • DTCS

The DTCS signal is also generated by the CPU (IC8) and output from pin 139. The DTCS signal is applied to the DTCS amplifier (IC23, pin 3) via DTCS switch (IC16, pins 1, 7). The amplified DTCS signal is applied to the D/A converter (IC10, pin 13) to adjust its level. The level adjusted DTCS signal is then applied to both of the modulator circuit (D61) and the reference frequency oscillator (X4).

## 4-5 POWER SUPPLY CIRCUITS

### 4-5-1 VOLTAGE LINES

LINE	DESCRIPTION
VCC	The voltage from the attached battery pack.
CPU5	Common 5 V for the CPU (IC8) converted from the VCC line at the CPU5 regulator circuit (IC12).
SW5V	Common 5 V line converted from the VCC line at the SW5 regulator circuit (Q55–Q57, D39) controlled by the "PWRON" signal.
T5	5 V for the transmit circuits regulated from the SW5V line by the T5 regulator (Q22). The regulator is controlled by the "T5C" signal from the CPU (IC8, pin 80).
PS5	5 V for the power save line regulated from the SW5V line by the PS5 regulator (Q54). The regulator is controlled by the "PS5C" signal from the CPU (IC8, pin 92).
R5	5 V for the receive circuits regulated from the SW5V line by the R5 regulator (Q21). The regulator is controlled by the "R5C" signal from the CPU (IC8, pin 82).
VCO5	5 V for the VCO circuit regulated from the SW5V line by the VCO5 regulator (Q11). The regulator is controlled by the "PSVCO" signal from the CPU (IC8, pin 62).
+5V	5 V for the optional unit power supply regulated from the VCC line by the option power supply regulator (Q61, Q62, D51). The regulator is controlled by the "OP_PS" signal from the CPU (IC8, pin 59).

## 4-6 PORT ALLOCATION

### 4-6-1 CPU (IC8)

PIN NUMBER	PORT NAME	DESCRIPTION
1	LVIN	Input port for PLL lock voltage.
3	REMO	Input port for remote control microphone.
4	SD	Input port for receiving signal strength detect signal.
5	CTCIN	Input port for CTCSS/DTCS signals.
7	DET	Input port for weather alert tone detect signal.
8	LEDC	Outputs LCD backlight control signal. HIGH : Lights ON
9	PTT	Input port for [PTT].
10	MICS	Outputs AF filter switch (IC4) control signal. HIGH : While transmitting
11	AN	Output ports AN switch (IC14) control signal.
12	DIGITAL	Input port for UT-118 accept/refuse signal. LOW : Accept
13	UN_SEC	Output ports UN_SEC switch (IC14) control signal.
15	CSHIFT	Outputs CPU (IC8) clock control signal.
19	RESET	Input port for "RESET" signal.
25	PWRSW	Input port for [PWR]. LOW : While pushing [PWR]

PIN NUMBER	PORT NAME	DESCRIPTION
26	NOIS	Input port for "NOIS" signal.
28	ESDA	I/O port for EEPROM (IC7).
29	ESCK	Outputs clock signal for EEPROM (IC7).
30	CLIN	Input port for cloning data.
31	CLOUD	Output port for cloning data.
32	OPS0	Outputs serial data for optional unit.
33	SI	Input port for DTMF decode signal.
34	SECRET	Outputs secret switch (IC14) control signal.
35	BUSY	Outputs receive detection (busy) signal to UT-118.
40–42	OPT1–OPT3	I/O ports for optional unit.
43	ALC	Outputs ALC switch (IC13) control signal. HIGH : During digital mode operation.
44	THROUGH	Outputs ALC switch (IC13) control signal. HIGH : During analog mode operation.
45	DI_SEC	Outputs modulation/demodulation mode switching signal. HIGH : During digital mode operation
46	MMUTE	Outputs analog switch (IC4) control signal.
49	RMUTE	Outputs audio mute signal. HIGH : While muting
52–54	OPV1–OPV3	Input ports for optional unit type detect signal.
55	TX_DIGI	Outputs transmit audio frequency characteristic control signal. LOW : During digital mode operation.
56	PTTO	Input port for transmit request control signal from UT-118.
57	PTTI	Output port for transmit request control signal to UT-118.
58	D5VC	Output port for D5VC line (5 V power supply; IC22) control signal. HIGH : Power ON
59	OP_PS	Outputs option power supply (Q61, Q62, D51) control signal. HIGH : Power ON
60	OPSCK	Outputs clock signal for optional unit.
61	RX_MUTE	Input port for RX mute signal for digital mode operation.
62	PSVCO	Outputs PS5 regulator (Q22) control signal. LOW : Power ON
63	PLPS	Outputs power save control signal to the PLL IC (IC19). LOW : Power saved
64	DASTB	Outputs strobe signal to D/A converter (IC10).
66	DADATA	Outputs serial data to D/A converter (IC10).
67	PLLSW	Outputs PLL loop filter switch (IC20) control signal.
68	PLLCK	Outputs clock signal to PLL IC (IC19).
69	PLLDATA	Outputs serial data to the PLL IC (IC19).

PIN NUMBER	PORT NAME	DESCRIPTION
70	PLLSTB	Outputs PLL strobe signal.
71	AFON	Outputs AF regulator (Q15, Q16) control signal. HIGH : While emitting audio
72	DUSE	Outputs LPF cut-off frequency control signal to the CTCSS switch (Q38). LOW : When CTCSS or no signaling system is in use. HIGH : DTCS is in use.
73–76	KR0–KR3	Input ports for keypad.
78	UNLK	Input port for PLL unlock signal.
79	EMPHASIS	Outputs emphasis switch (Q73) control signal. HIGH : During FM mode operation.
80	T5C	Outputs T5 regulator (Q22) control signal. LOW : While transmitting
81	DEGI_W	Outputs detect circuit (Wide/Narrow) switch (Q53) control signal. HIGH : During narrow mode operation.
82	R5C	Outputs R5 regulator (Q21) control signal. LOW : During receive
83	TXC	Outputs RF output power control signal. LOW : During transmit
86–90	KS0–KS4	Output ports for keypad.
92	PS5C	Outputs PS5 regulator (Q54) control signal. LOW : Power saved
97, 98	DICK, DIUD	Input port for [VOL] control (S801).
141	TONE	Outputs DTMF, BEEP, 1750 Hz tone signals, etc.

#### 4-6-2 D/A CONVERTER (IC10)

PIN NUMBER	PORT NAME	DESCRIPTION
2	T1	Outputs the tunable BPF tuning signal. The output signal is applied to BPF (D9, D11, D12).
3	T2	Outputs the tunable BPF tuning signal. The output signal is applied to BPF (D11, D12).
10	T3	<ul style="list-style-type: none"> <li>Outputs the tunable BPF tuning signal. The output signal is applied to BPF (D65).</li> <li>Output port for transmit output power setting signal. The output signal is applied to the APC amplifier (IC3, pin 3).</li> </ul>
11	VOLOUT	Outputs AF output signals to the AF amplifier (IC5).
13	DTCS	Input port for DTCS signal from the DTCS amplifier (IC23).
15	FC	Outputs reference frequency control voltage.
22	MOD	Outputs modulating audio signal to the modulator circuit (D61).
23	SQLIN	Outputs squelch control signal to the noise active filter (IC2, pins 7, 8; R86–R88, C121, C122).

## 4-7 UT-118 CIRCUIT DESCRIPTION

### 4-7-1 RECEIVER CIRCUIT

The detected digital signals "FMDET" from the connected transceiver via the J301 (pin 22) are amplified at the buffer amplifier (IC251, pin 2). The amplified signals are applied to the GMSK modem circuit (IC252, pin 11), and are then applied to the CPU (IC204) as clock synchronizer digital signal. The digital signals from the CPU are applied to the AMBE voice CODEC IC (IC151) to press code extension, and are then applied to the linear CODEC IC (IC50) as 32 bits digital voice data. The applied digital signals are converted to the analog AF signals at the D/A converter section (IC50), and are then applied to the connected transceiver via the J301 (pin 21) as "DAFOUT" signal.

### 4-7-2 TRANSMITTER CIRCUIT

The analog AF signals "AMODIN" from the connected transceiver via the J301 (pin 4) are amplified at the buffer amplifier (IC251, pin 6). The amplified signals are applied to the linear CODEC IC (IC50, pin 5) to convert 32 bits digital voice data at the A/D converter section via the "ADIN" line. The digital signals are applied to the AMBE voice CODEC IC (IC151) to process code compression, and are then applied to the CPU (IC204). The digital signals from the CPU convert to the GMSK base band signal at the GMSK modem (IC252), and are then amplified at the buffer amplifier (IC253, pin 5). The amplified signals are applied to the connected transceiver via the J301 (pin 3).

### 4-7-3 RESET CIRCUIT

The UT-118 has the reset IC (IC203). The reset IC outputs "RES" signal to the CPU (IC204, pin 7) when more than 2.8 V of voltage is applied to the "VDD" port (pin 2).

### 4-7-4 RS-232C CIRCUIT

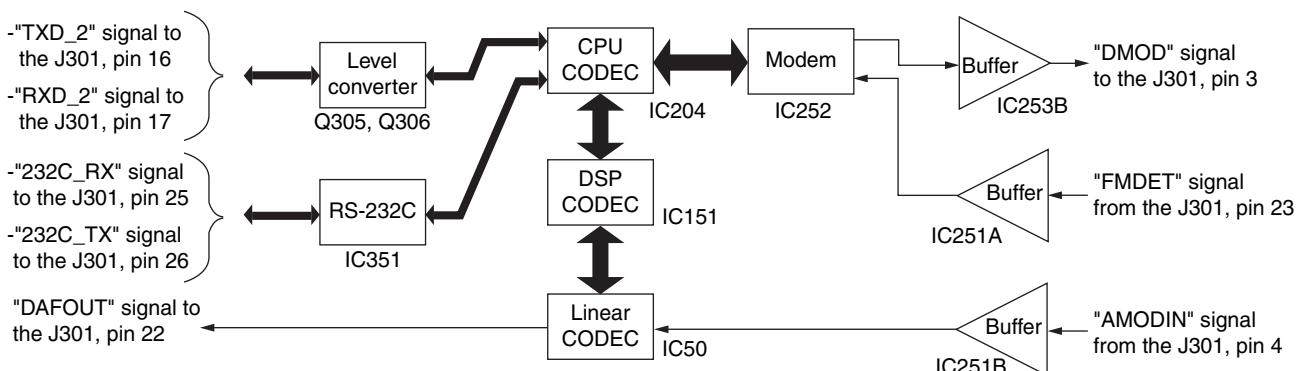
IC351 is a RS-232C compatible serial interface IC which converts data between the CPU and the external equipment (ex. Personal Computer).

### 4-7-5 LEVEL CONVERTER CIRCUIT

The level converter circuit (Q305 and Q306) converts communication data level between the CPU (IC204) and the connected transceiver's CPU.

Q301, Q302 and Q303 convert control signals level between the UT-118 and the IC-V82.

#### • UT-118 BLOCK DIAGRAM



## 4-8 UT-118 POWER SUPPLY CIRCUITS

### 4-8-1 VOLTAGE LINES

LINE	DESCRIPTION
5V	5 V from the connected transceiver via the J301 (pin 29). The 5V line is controlled by the +5 V control circuit (Q50 and Q51). The circuit is controlled by the "PSAVE" signal from the CPU (IC204, pin 58 and 59).
3.3V	Common 3.3 V converted from the 5V line by the 3.3V regulator circuit (IC1). One of the 3.3 V line is controlled by the +3V control circuit (Q400 and Q401). The circuit is controlled by the "PSAVE" signal from the CPU (IC204, pin 58 and 59).
3.2V	Common 3.2 V converted from the 4.5–8 V line by the 3.2V regulator circuit (IC2). The circuit is controlled by the "APWR" signal from the CPU (IC204, pin 16).

## 4-9 UT-118 PORT ALLOCATIONS

### 4-9-1 MODEM IC (IC252)

PIN NUMBER	PORT NAME	DESCRIPTION
2	MCLK	Outputs 2.4576 MHz clock signal to the CPU (IC151, pin 39).
7	ACQ	Outputs the PLL bandwidth control signal while receiving.
19	TXDT	Outputs transmitting data signal to the CPU (IC204, pin 54).
20	RXDT	Input port for receiving data signal from the CPU (IC204, pin 53).
21	RXCK	Input port for receive clock signal from the CPU (IC204, pin 52).
22	TXCK	Outputs transmit clock signal to the CPU (IC204, pin 51).

## SECTION 5 ADJUSTMENT PROCEDURES

### 5-1 PREPARATION

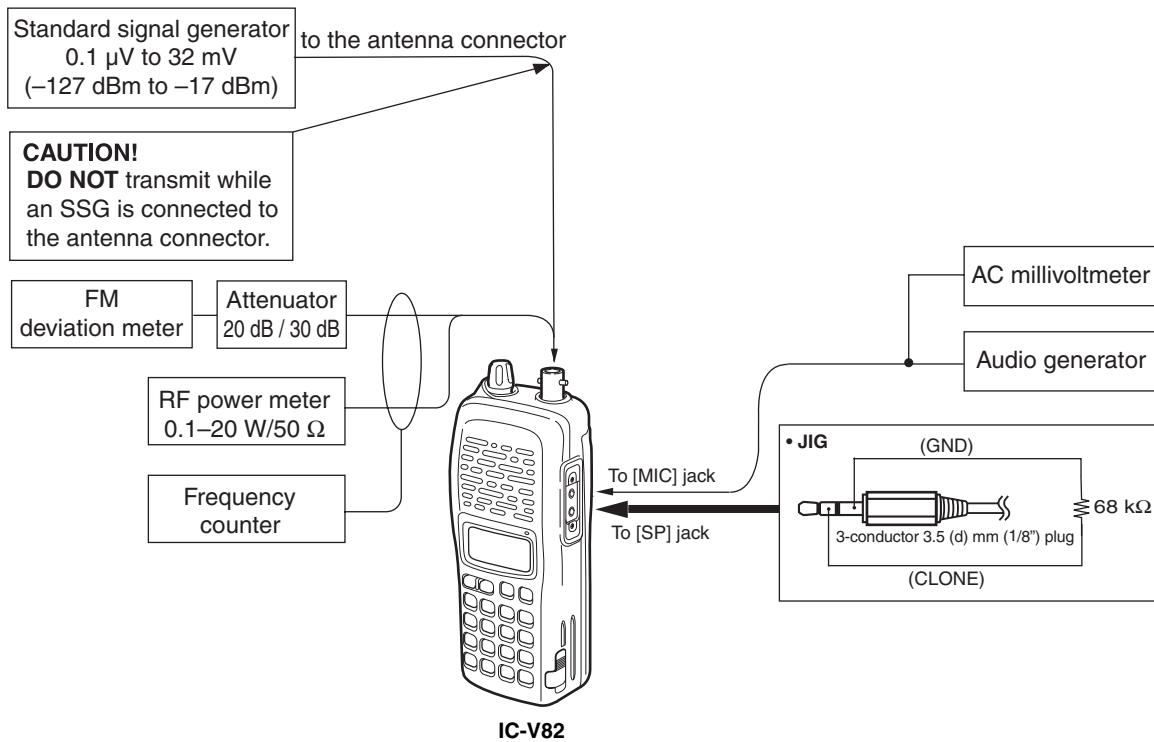
#### ■ REQUIRED TEST EQUIPMENTS

EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supplies*	Output voltage : 5.0 V DC 8.0 V DC Current capacity : 1 A or more	Standard signal generator (SSG)	Frequency range : 0.1–300 MHz Output level : 0.1 $\mu$ V to 32 mV (-127 to -17 dBm)
RF power meter (terminated type)	Measuring range : 0.1–20 W Frequency range : 100–300 MHz Impedance : 50 $\Omega$ SWR : Less than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–10 V
Frequency counter	Frequency range : 0.1–300 MHz Frequency accuracy: $\pm 1$ ppm or better Sensitivity : 100 mV or better	AC millivoltmeter	Measuring range : 10 mV to 10 V
Audio generator	Frequency range : 300–3000 Hz Output level : 1–500 mV	External speaker	Input impedance : 8 $\Omega$ Capacity : More than 0.5 W
FM deviation meter	Frequency range : 30–300 MHz Measuring range : 0 to $\pm 10$ kHz	Attenuator	Power attenuation : 20 or 30 dB Capacity : More than 5 W

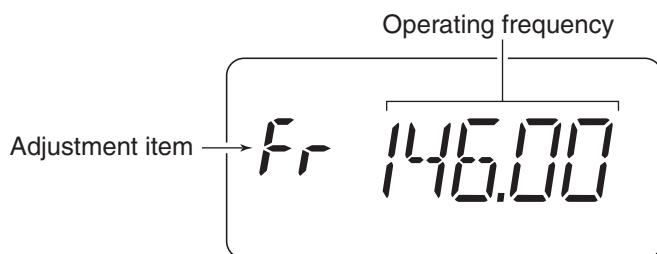
\*; For UT-118 adjustment only.

**CAUTION!:** BACK UP the originally programmed contents (Memory channels, Call signs, Common settings, etc.) in the transceiver using CS-V82 CLONING SOFTWARE before starting adjustment.  
When all adjustments are completed, these contents in the transceiver will be cleared.

#### • CONNECTION



#### • ADJUSTMENT MODE DISPLAY

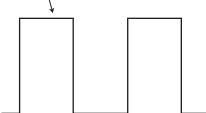


## 5-2 IC-V82 ADJUSTMENT

### 5-2-1 KEY OPERATION FOR THE ADJUSTMENT

- Rotate [VOL] to adjust the value.
- Push [D•CLR] key to store the adjustment value and move to next adjustment item.
- Push [ $\Delta$ ]/[ $\nabla$ ] key to move to next adjustment item without changing the value.

### 5-2-2 FREQUENCY AND TRANSMIT ADJUSTMENT

ADJUSTMENT	ADJUSTMENT CONDITION	OPERATION
ENTERING ADJUSTMENT MODE	• While pushing [ $\Delta$ ], [ $\nabla$ ] and [D•CLR] keys, turn power ON.	
REFERENCE FREQUENCY <i>Fr 146.00</i>	1 • Connect a frequency counter to the antenna connector through an attenuator. • Transmitting	• Rotate [VOL] to set to 146.000 MHz $\pm$ 100Hz. • Push [D•CLR] key.
TRANSMIT LOCK VOLTAGE <i>LV 146.00</i>	1 • Transmitting	• Push [D•CLR] key, then push [ $\nabla$ ] key. (Do not release [PTT] button when pushing [D•CLR] key.)
OUTPUT POWER (High) <i>P<sub>D</sub> 146.00</i>	1 • Connect an RF power meter to the antenna connector. • Transmitting	• Rotate [VOL] to set the transmit power to 7.0 W. • Push [D•CLR] key.
(Middle) <i>P<sub>D</sub> 146.00<sub>M</sub></i>	2 • Transmitting	• Rotate [VOL] to set the transmit power to 4.0 W. • Push [D•CLR] key.
(Low) <i>P<sub>D</sub> 146.00<sub>L</sub></i>	3 • Transmitting	• Rotate [VOL] to set the transmit power to 0.5 W. • Push [D•CLR] key.
FREQUENCY DEVIATION <i>DE 146.00</i>	1 • Mode : Wide • Connect an FM deviation meter to the antenna connector through an attenuator and set as : HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • Connect an audio generator to [MIC] jack and set as; Frequency : 1 kHz Level : 150 mV rms • Transmitting	• Rotate [VOL] to set to $\pm$ 4.2 kHz. • Push [D•CLR] key.
DIGITAL VCO FREQUENCY DEVIATION <i>DE 146.00<sub>DV</sub></i>	1 • Set the FM deviation meter as; HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • No audio input • Transmitting	• Rotate [VOL] to set to $\pm$ 1.20 kHz. • Push [D•CLR] key.
DTCS WAVE FORM <i>DE 146.00</i>	1 • Mode : Wide • Connect an oscilloscope and the FM deviation meter to the antenna connector. • Set the FM deviation meter as; HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • No audio input • Transmitting	• Rotate [VOL] to set to square wave form as shown below. • Push [D•CLR] key. Set to square wave form 
DIGITAL REFERENCE FREQUENCY DEVIATION <i>DE 146.00<sub>DV</sub></i>	1 • Set the FM deviation meter as; HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P-P)/2 • No audio input • Transmitting	• Rotate [VOL] to set to $\pm$ 1.20 kHz. • Push [D•CLR] key.

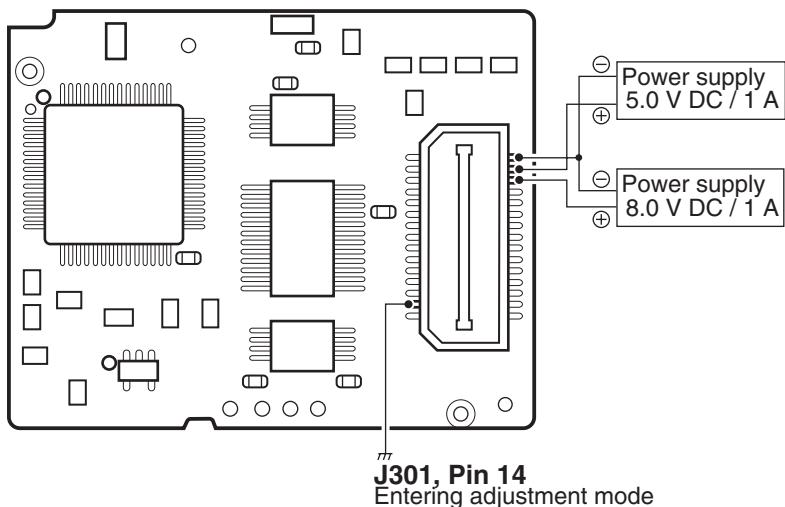
### 5-2-3 RECEIVE ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITION	OPERATION
<b>SENSITIVITY</b> <i>Er 145.02</i>	1	<ul style="list-style-type: none"> <li>• Connect an SSG to the antenna connector and set as;</li> <li>Frequency : 136.020 MHz</li> <li>Level : 0 dB<math>\mu</math>*</li> <li>Modulation : 1 kHz</li> <li>Deviation : <math>\pm</math> 3.5 kHz</li> <li>• Receiving</li> </ul>	• Push [D•CLR] key.
	2	<ul style="list-style-type: none"> <li>• Set the SSG as;</li> <li>Frequency : 147.980 MHz</li> <li>Level : 0 dB<math>\mu</math>*</li> <li>Modulation : 1 kHz</li> <li>Deviation : <math>\pm</math> 3.5 kHz</li> <li>• Receiving</li> </ul>	• Push [D•CLR] key.
	3	<ul style="list-style-type: none"> <li>• Set the SSG as;</li> <li>Frequency : 173.980 MHz</li> <li>Level : 0 dB<math>\mu</math>*</li> <li>Modulation : 1 kHz</li> <li>Deviation : <math>\pm</math> 3.5 kHz</li> <li>• Receiving</li> </ul>	• Push [D•CLR] key.
<b>SQUELCH</b> <i>Sq 145.02</i>	1	<ul style="list-style-type: none"> <li>• Set the SSG as;</li> <li>Frequency : 145.020 MHz</li> <li>Level : -19 dB<math>\mu</math>*</li> <li>Modulation : 1 kHz</li> <li>Deviation : <math>\pm</math> 3.5 kHz</li> <li>• Receiving</li> </ul>	• Close the squelch once, then set the squelch level at the point where the audio signals just appears.
<b>S-METER</b> <i>Sr 145.02</i>	1	<ul style="list-style-type: none"> <li>• Set the SSG as;</li> <li>Frequency : 145.020 MHz</li> <li>Level : -6 dB<math>\mu</math>*</li> <li>Modulation : 1 kHz</li> <li>Deviation : <math>\pm</math> 3.5 kHz</li> <li>• Receiving</li> </ul>	• Push [D•CLR] key.
<b>QUITING ADJUSTMENT MODE</b>	1	<ul style="list-style-type: none"> <li>• Turn power OFF.</li> </ul>	
	2	<ul style="list-style-type: none"> <li>• While pushing [MONI] and [D•CLR] keys, turn power ON.</li> </ul>	

\*; This output level of the standard signal generator (SSG) is indicated as SSG's terminated circuit.

## 5-3 UT-118 ADJUSTMENT

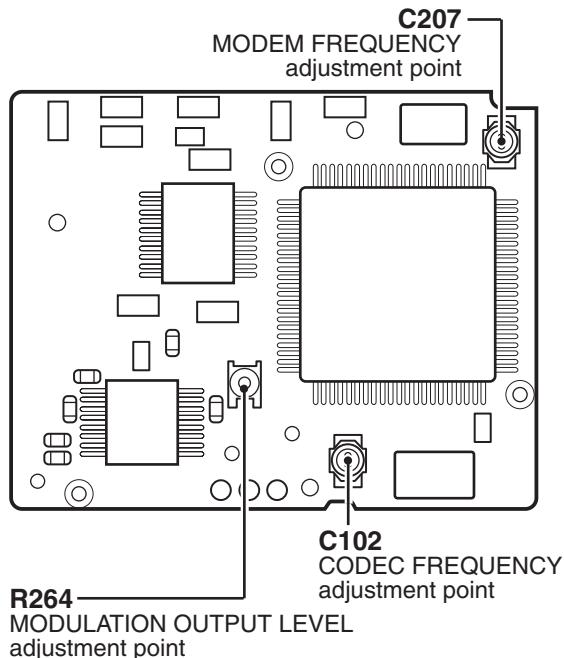
### • CONNECTION (BOTTOM VIEW)



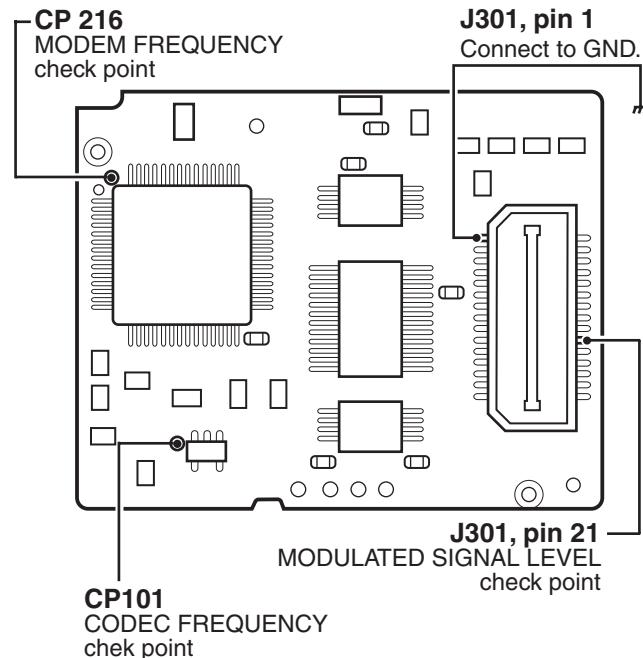
### • ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITION	OPERATION
ENTERING ADJUSTMENT MODE		• Connect the pin 14 of J301 to GND to enter the adjustment mode.	
CODEC FREQUENCY	1	• Connect the frequency counter to CP101 through a capacitor (1000 pF).	• Adjust C102 to set to 16.38400 MHz ±10 Hz.
MODEM FREQUENCY	1	• Connect the frequency counter to CP216 through a capacitor (1000 pF).	• Adjust C207 to set to 2.457600 MHz ±3 Hz.
MODULATION OUTPUT LEVEL	1	• Connect the pin 1 of J301 to GND to enter the transmit mode. • Connect the oscilloscope to pin 21 of J301.	• Adjust R264 to set to 350 mVp-p ±10 mV.
	2	• Disconnect the pin 1 of J301 from GND after the adjustment to quit the transmit mode.	
QUITING ADJUSTMENT MODE		• Disconnect the pin 14 of J301 from GND to quit the adjustment mode.	

### • UT-118 TOP VIEW



### • UT-118 BOTTOM VIEW













## SECTION 7 MECHANICAL PARTS AND DISASSEMBLY

### [CHASSIS PARTS]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
J1	6510022460	Connector BNC-R162	1
SP1	2510001280	Speaker SDRS-3650P-008A	1
W1	8900009640	Cable OPC-963	1
MP1	8210021290	2826 front panel	1
MP2	8930064470	2826 keyboard	1
MP3	8010019850	2826 chassis	1
MP4	8930064420	2826 D-cap	1
MP5	8930064440	2826 jack cap	1
MP6	8930064910	2826 S-jack seal	1
MP7	8930050870	2251 release button	1
MP9	8930064460	2826 PTT button	1
MP10	8210021300	2826 PTT panel	1
MP11	8930064450	2826 PTT rubber	1
MP12	8210021270	2826 rear panel	1
MP13	8210017091	2337 terminal holder-1	1
MP14	8310062510	2826 window plate	1
MP15	8930042350	1922 microphone sheet	1
MP16	8930051300	2251 microphone sponge	1
MP18	8610012170	Knob N-326	1
MP19	8810008640	Screw No.0-1 FH B0 2 × 4 NI-ZU (BT)	3
MP20	8930054881	2458 plus terminal-1	1
MP21	8930050840	2251 minus terminal	1
MP23	8830001340	1903 hex. Nut	1
MP24	8830001250	Nut ANT connector-101	1
MP25	8930036751	Spring (Y)-1	1
MP27	8810009510	Screw PH B0 2 × 4 NI-ZU (BT)	6
MP28	8810009560	Screw PH B0 2 × 6 ZK (BT)	4
MP29	8810000100	Screw PH M2 × 4 ZK	2
MP30	8810008990	Screw PH B0 2 × 10 ZK (BT)	2
MP31	8860001210	2251 antenna lug plate	1
MP32	8510016800	2826 shield cover	1
MP33	8510016790	2826 option plate	1
MP34	8930064880	2826 window sheet	1
MP35	8810005700	Screw No.0-1 PH M2 × 4 ZK	4
MP36	8930065490	Rubber sheet (BO)	1
MP37	8510016890	2826 U-shield cover	1

### [MAIN UNIT]

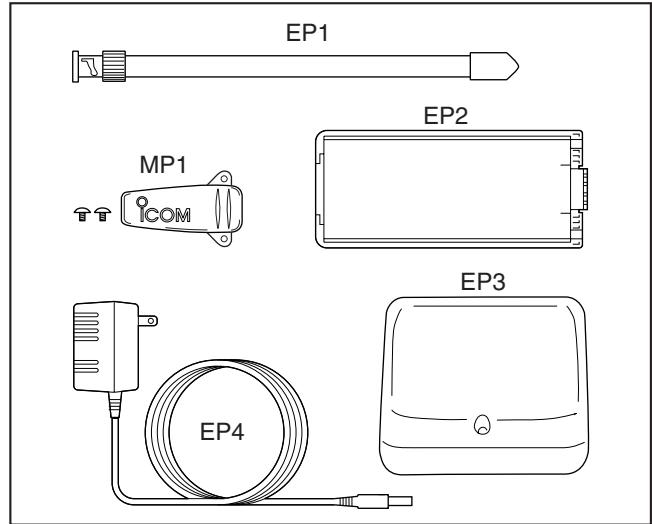
REF. NO.	ORDER NO.	DESCRIPTION	QTY.
DS4	5030002800	LCD A01B001X	1
MP1	8510016470	2775 VCO case	1
MP2	8510016470	2775 VCO cover	1
MP3	8210021280	2826 reflector	1
MP4	8930064560	2826 LCD holder	1
MP6	8930058840	Shield sponge	1

#### Screw abbreviations

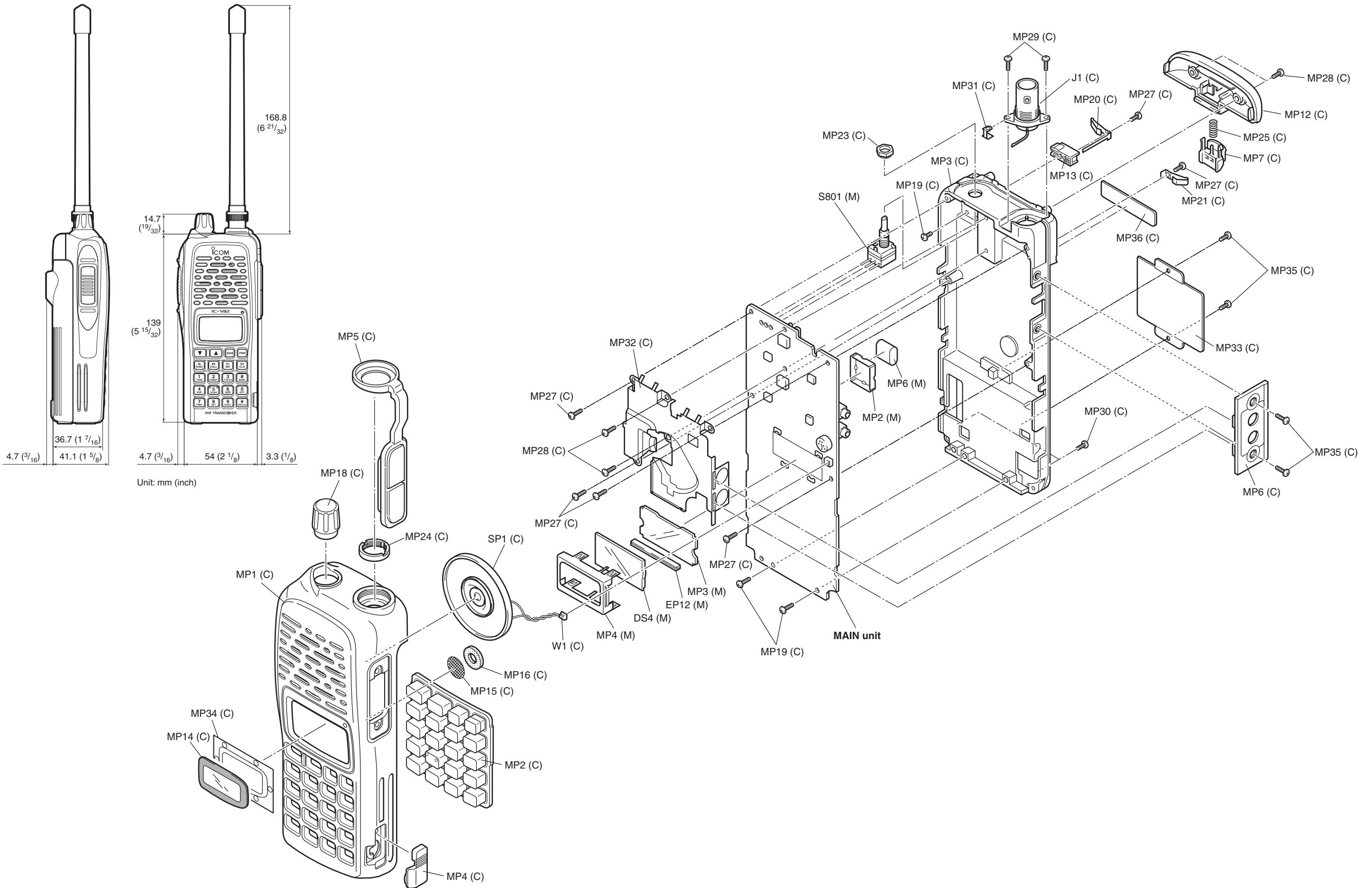
B0, BT: Self-tapping PH: Pan head  
NI-ZU: Nickel-Zinc ZK: Black

### [ACCESSORIES]

REF. NO.	ORDER NO.	DESCRIPTION	QTY.
EP1	Optional product	Antenna FA-B2E	1
EP2	Optional product	Battery BP-208N [EUR-1], [EXP-1], [USA-1], [CSA-1]	1
	Optional product	Battery BP-222N EXP [EUR-2], [EXP-2], [CSA-2]	1
	Optional product	Battery BP-222N RBRC [USA-2] only	1
	Optional product	Battery BP-209N EXP [CSA-3], [EUR-3], [EXP-4]	1
	Optional product	Battery BP-209N RBRC [USA-3] only	1
EP3	Optional product	AC adopter BC-146	1
EP4	Optional product	AC adopter BC-147E [EUR-2], [EXP-2], [EUR-3], [EXP-4]	1
	Optional product	AC adopter BC-147A [USA-2], [CSA-2], [USA-3]	1
MP1	Optional product	MB-103	1



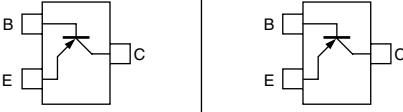
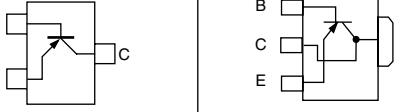
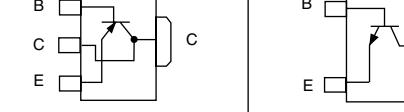
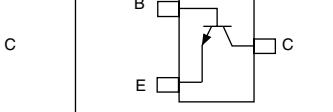
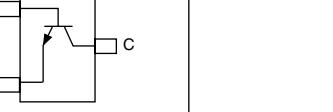
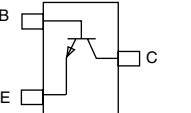
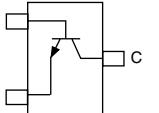
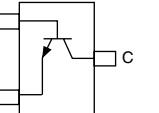
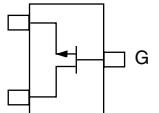
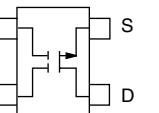
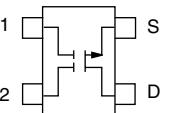
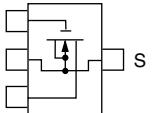
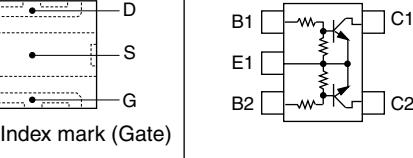
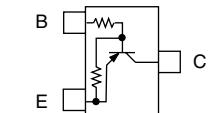
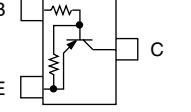
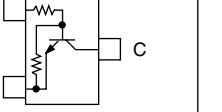
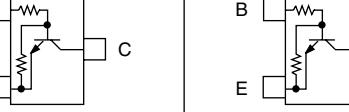
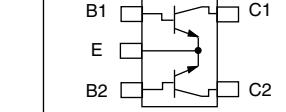
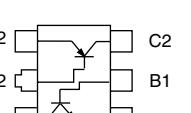
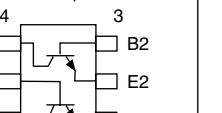
\* Design is depended on versions.



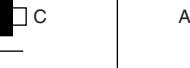
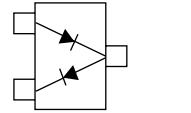
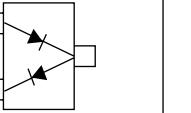
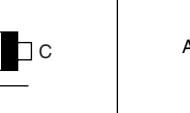
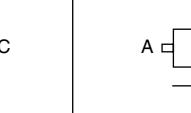
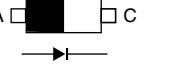
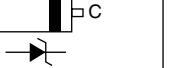
**UNIT abbreviations** (C): CHASSIS PARTS, (M): MAIN UNIT

## SECTION 8 SEMICONDUCTOR INFORMATION

### •TRANSISTORS AND FETS

2SA1576S (Symbol: FS)	2SA1576A (Symbol: FA)	2SB1132R (Symbol: BAR)	2SC4116BL (Symbol: LL)	2SC4617 TLS (Symbol: BS)
				
2SC5006-T1 (Symbol: 24)	2SC5085Y (Symbol: R6)	2SC5231 C8 (Symbol: C8)	2SK1069-4 (Symbol: FJ)	3SK299-U73 (Symbol: U73)
				
3SK318YB-TL-E (Symbol: YB)	RD01MUS1 (Symbol: K2)	RD12MVS1-T12 (Symbol: RD12MVS1)	UMG2N TL (Symbol: G2)	UNR911FJ (Symbol: 6O)
				
UNR9113J (Symbol: 6C)	UNR9210J (Symbol: 8L)	UNR9213J (Symbol: 8C)	UNR921NJ (Symbol: EX)	XP1501 AB (Symbol: 5R)
				
XP4601 (Symbol: 5C)	XP6501-AB (Symbol: 5N)			
				

### •DIODES

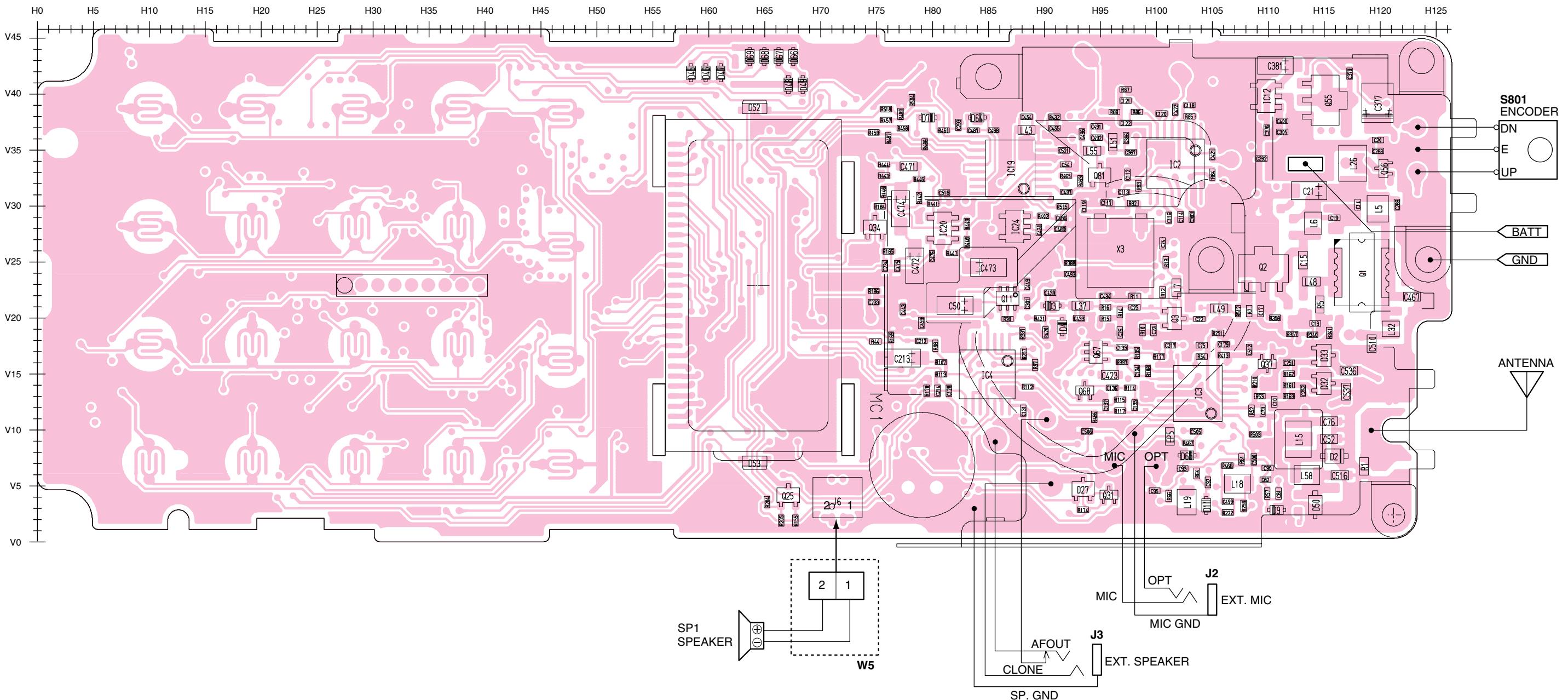
1SV286 (Symbol: T7)	1SV308 (Symbol: K)	MA2S30400L (Symbol: BAR)	HVC375BTRF (Symbol: B8)	1SS400 (Symbol: A)
				
DA221 TL (Symbol: K)	MA742 (Symbol: M1U)	HVU131TRF (Symbol: P1)	MA2S077 (Symbol: S)	MA728 (Symbol: 2A)
				
MA77 (Symbol: 4B)	MA8056-M (Symbol: 5-6)			
				

## SECTION 9 BOARD LAYOUTS

### MAIN UNIT

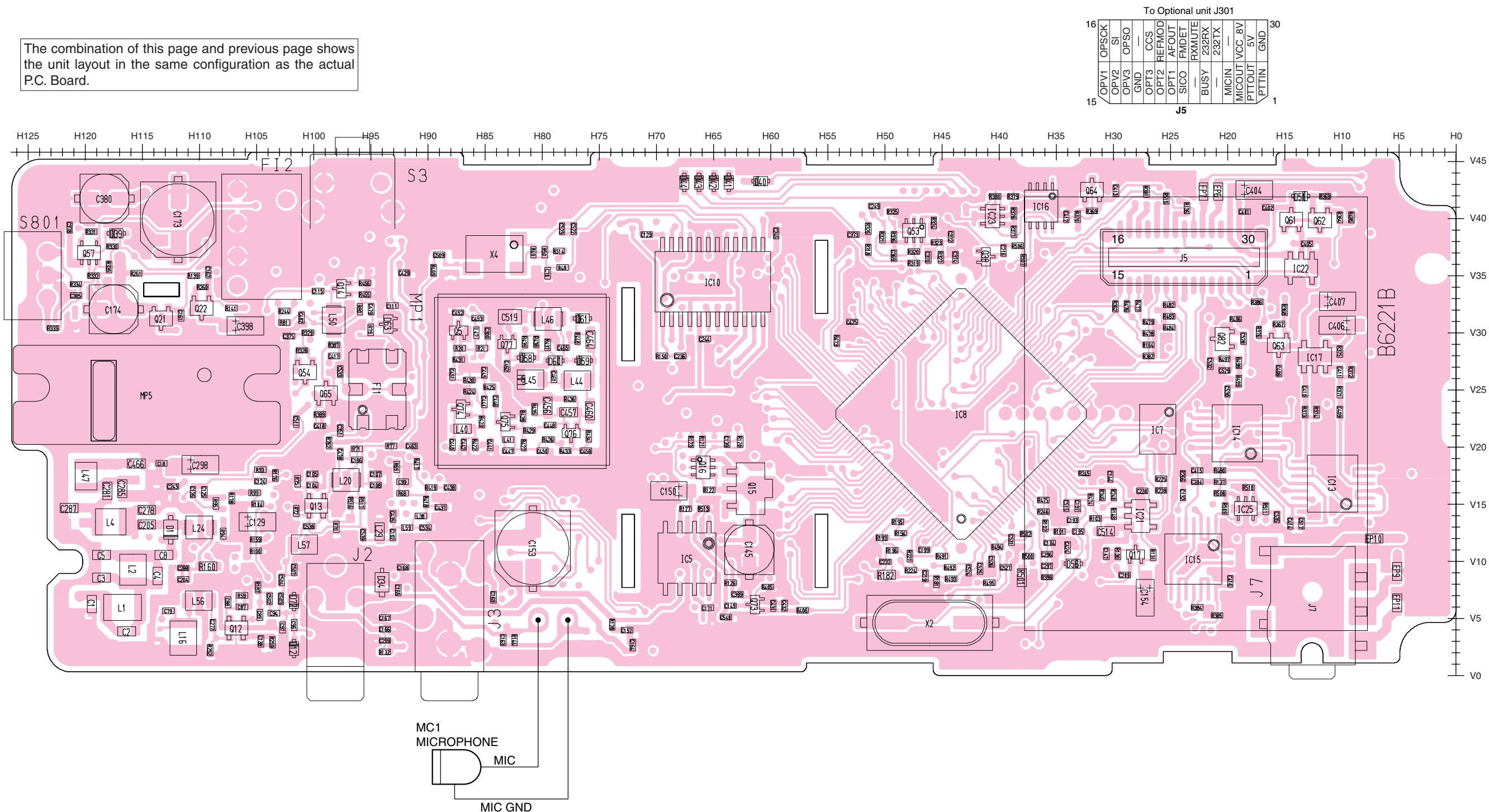
• TOP VIEW

The combination of this page and next page shows the unit layout in the same configuration as the actual P.C. Board.



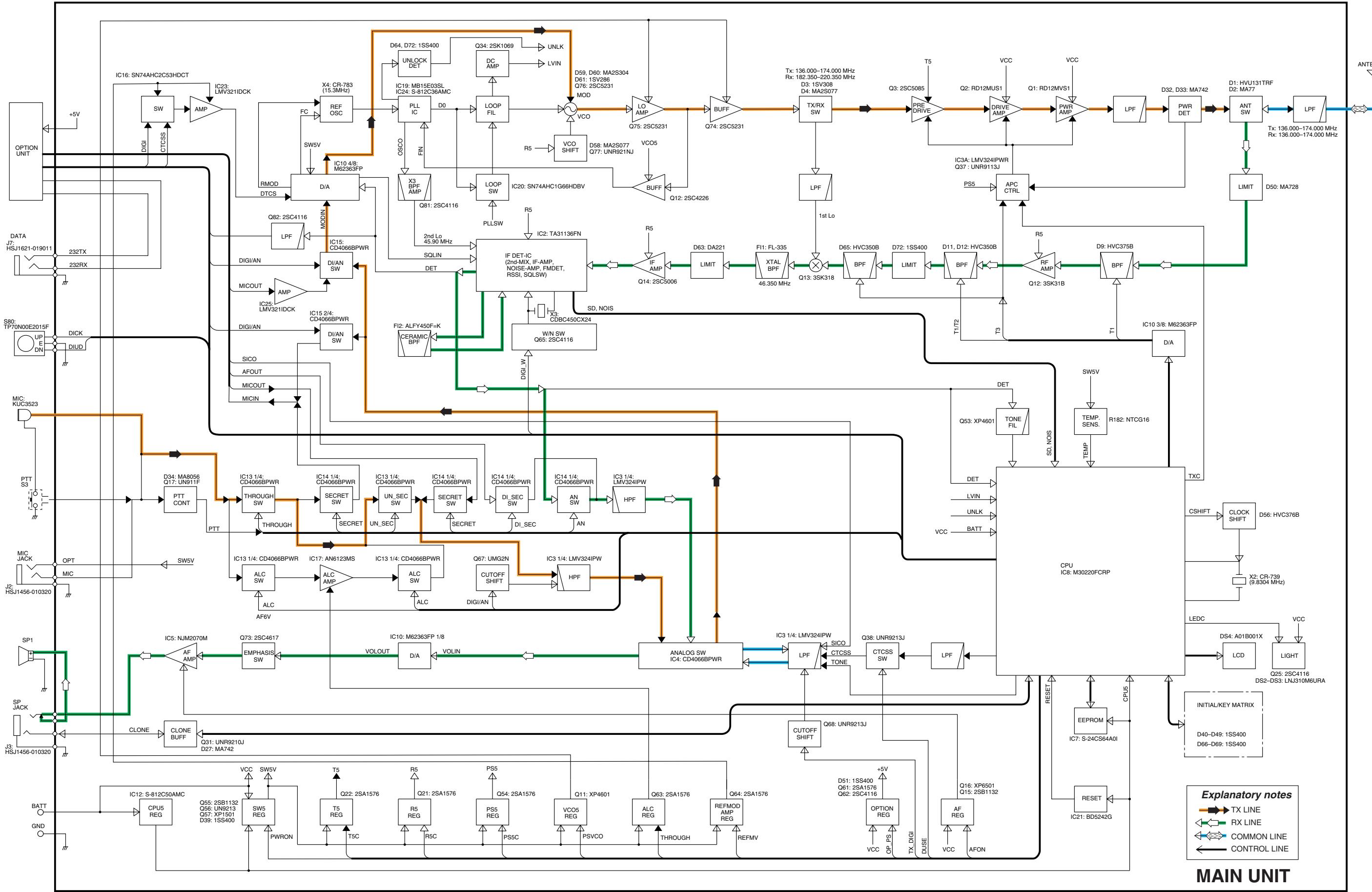
• BOTTOM VIEW

The combination of this page and previous page shows the unit layout in the same configuration as the actual P.C. Board.



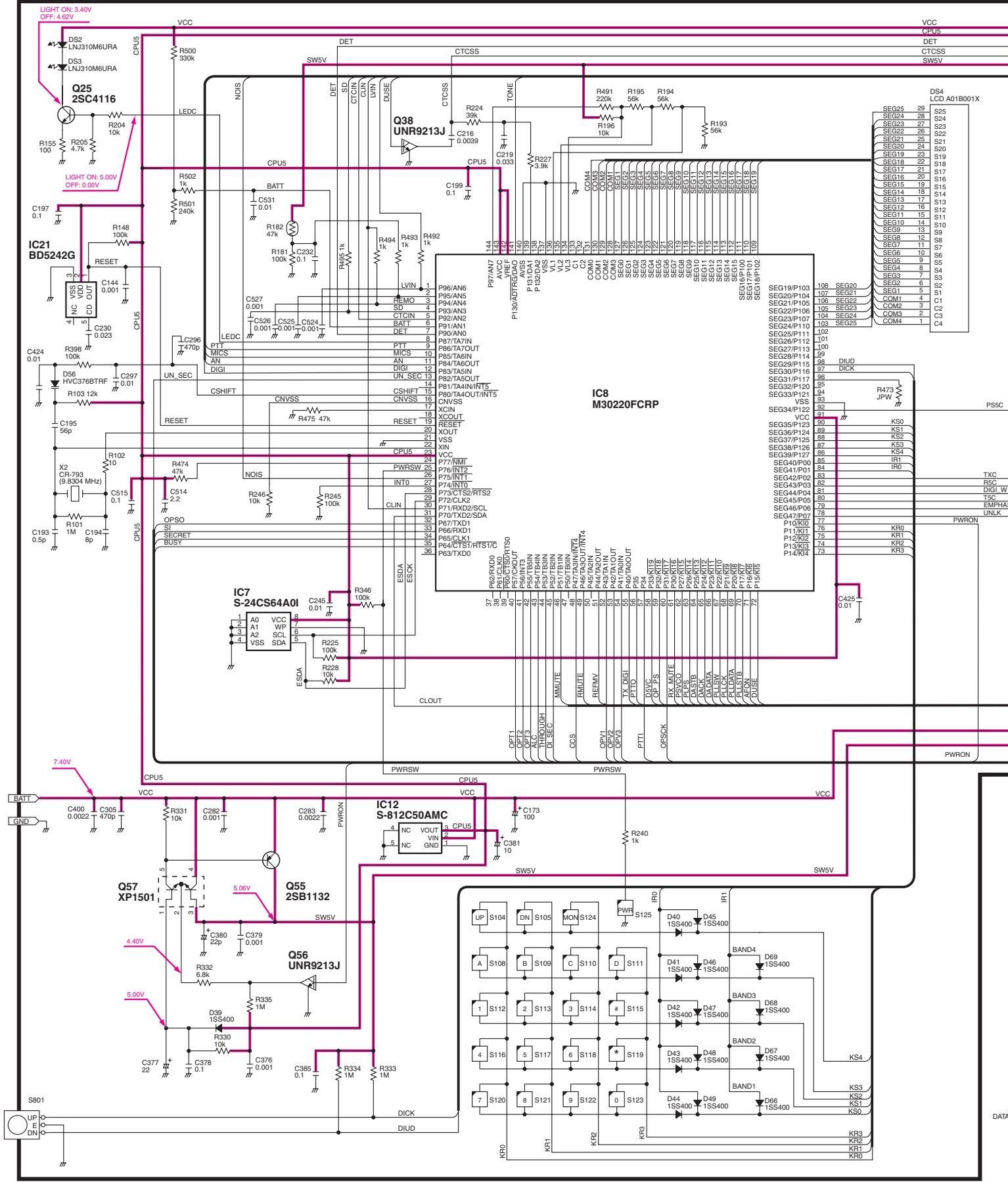
## SECTION 10 BLOCK DIAGRAM

### • MAIN UNIT



# SECTION 11 VOLTAGE DIAGRAM

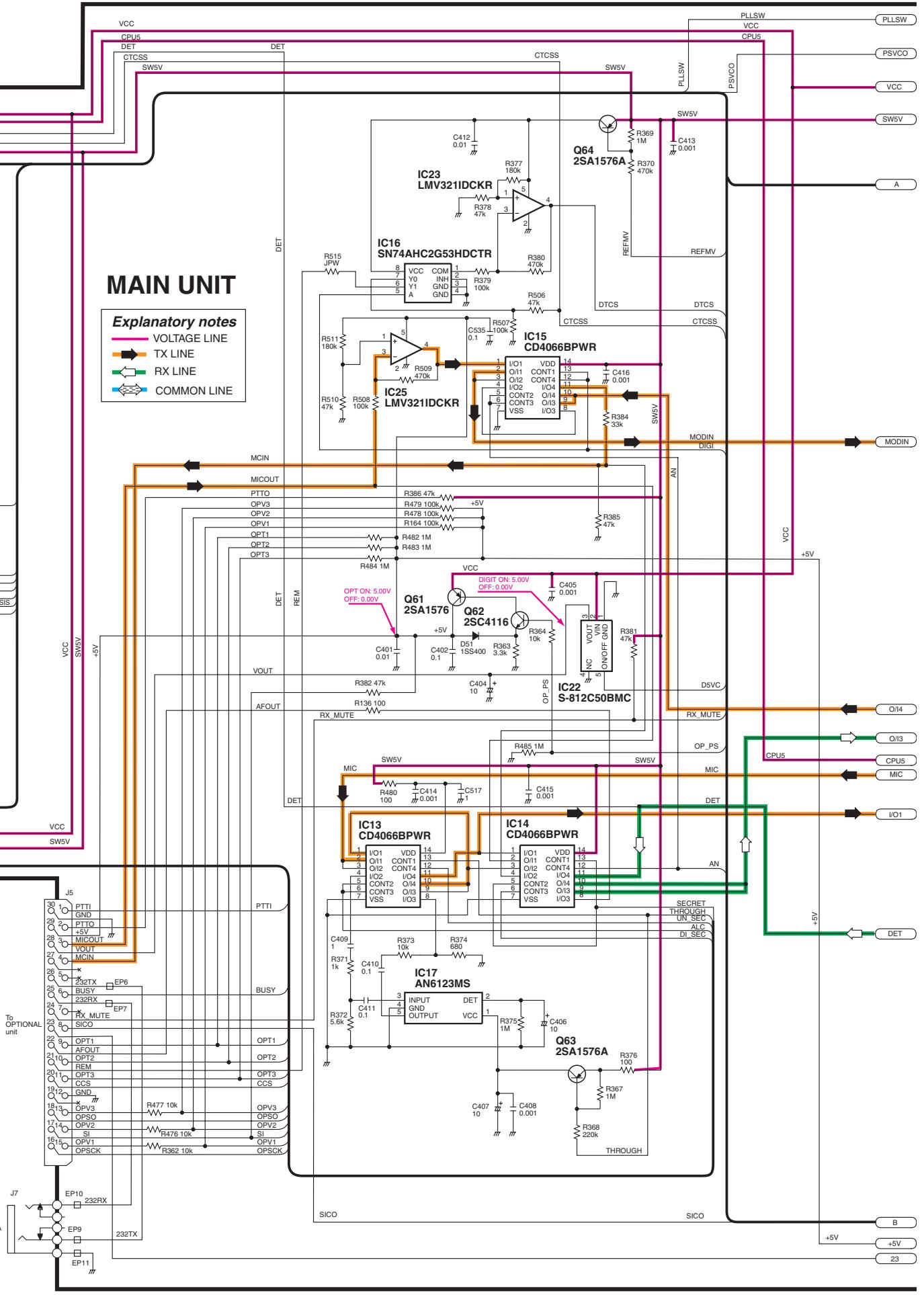
## • MAIN UNIT

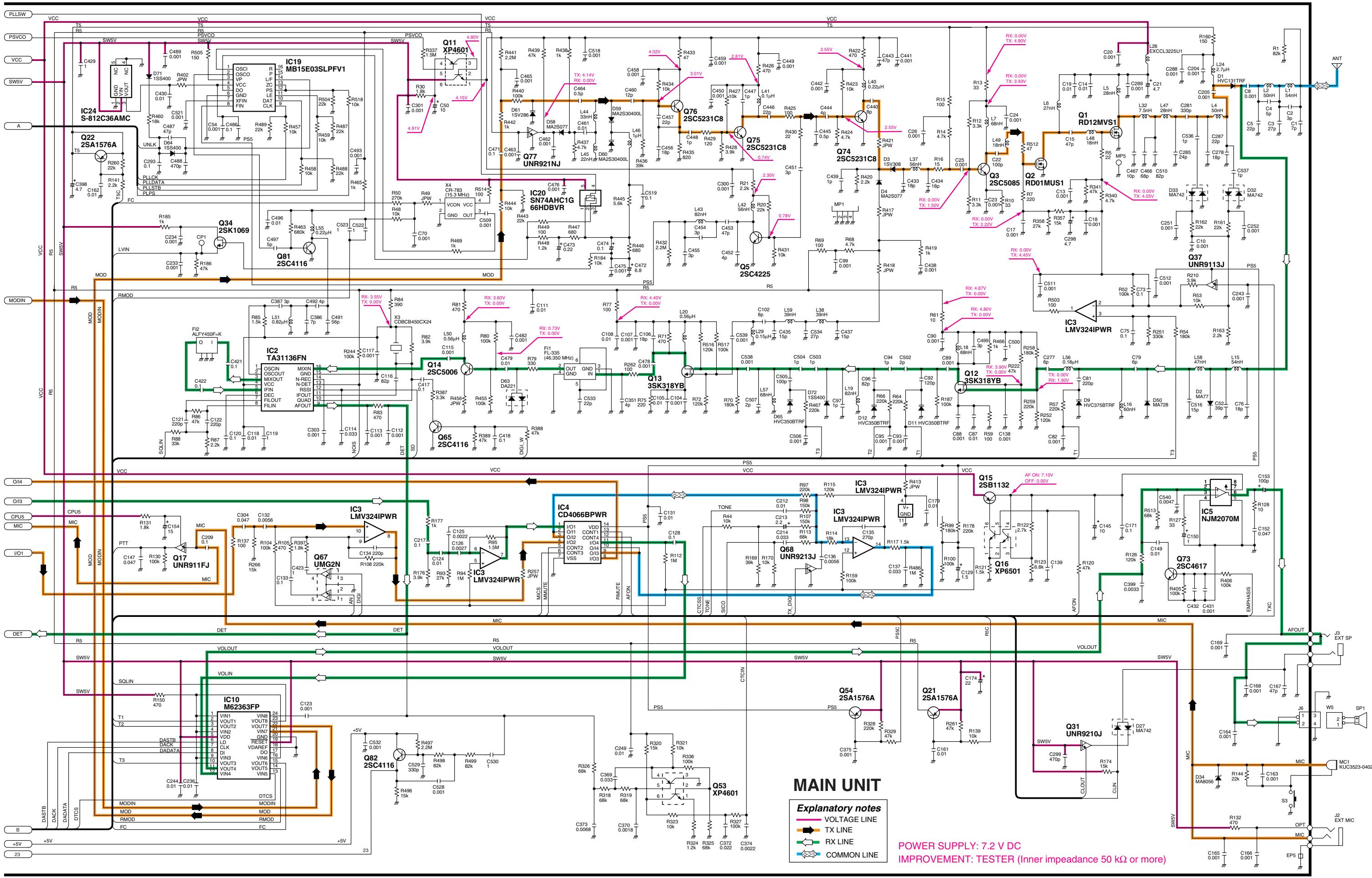


## MAIN UNIT

**Explanatory notes**

- VOLTAGE LINE (Pink line)
- TX LINE (Orange line)
- RX LINE (Green line)
- COMMON LINE (Blue line)

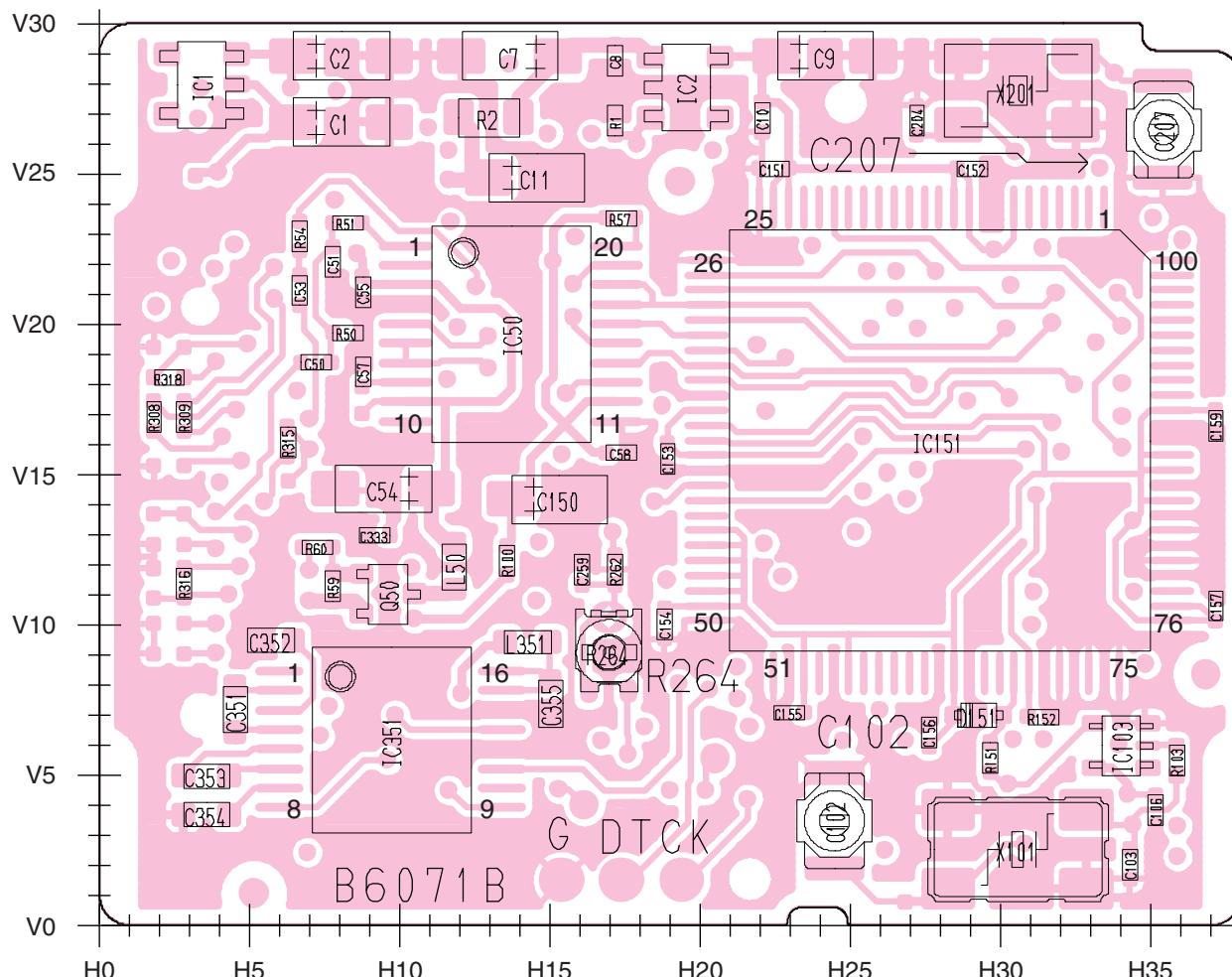




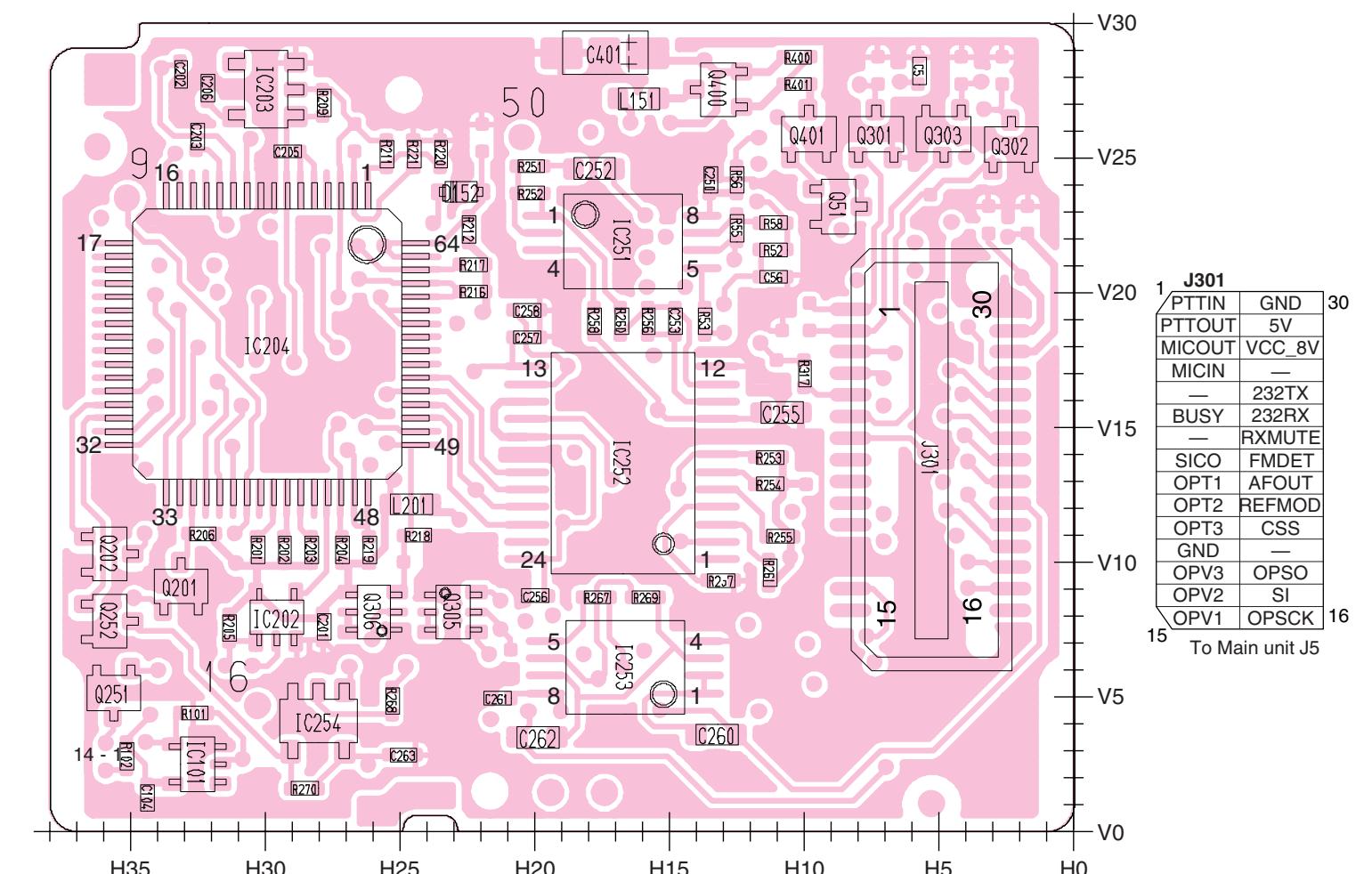
## SECTION 12 UT-118 DIGITAL UNIT (OPTIONAL UNIT)

### 12-1 UT-118 BOARD LAYOUT

• TOP VIEW

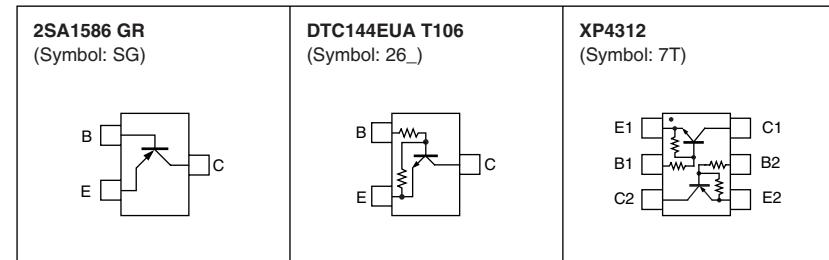


• BOTTOM VIEW

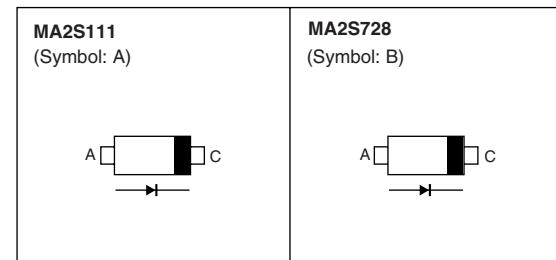


## 12-2 UT-118 SEMICONDUCTOR INFORMATION

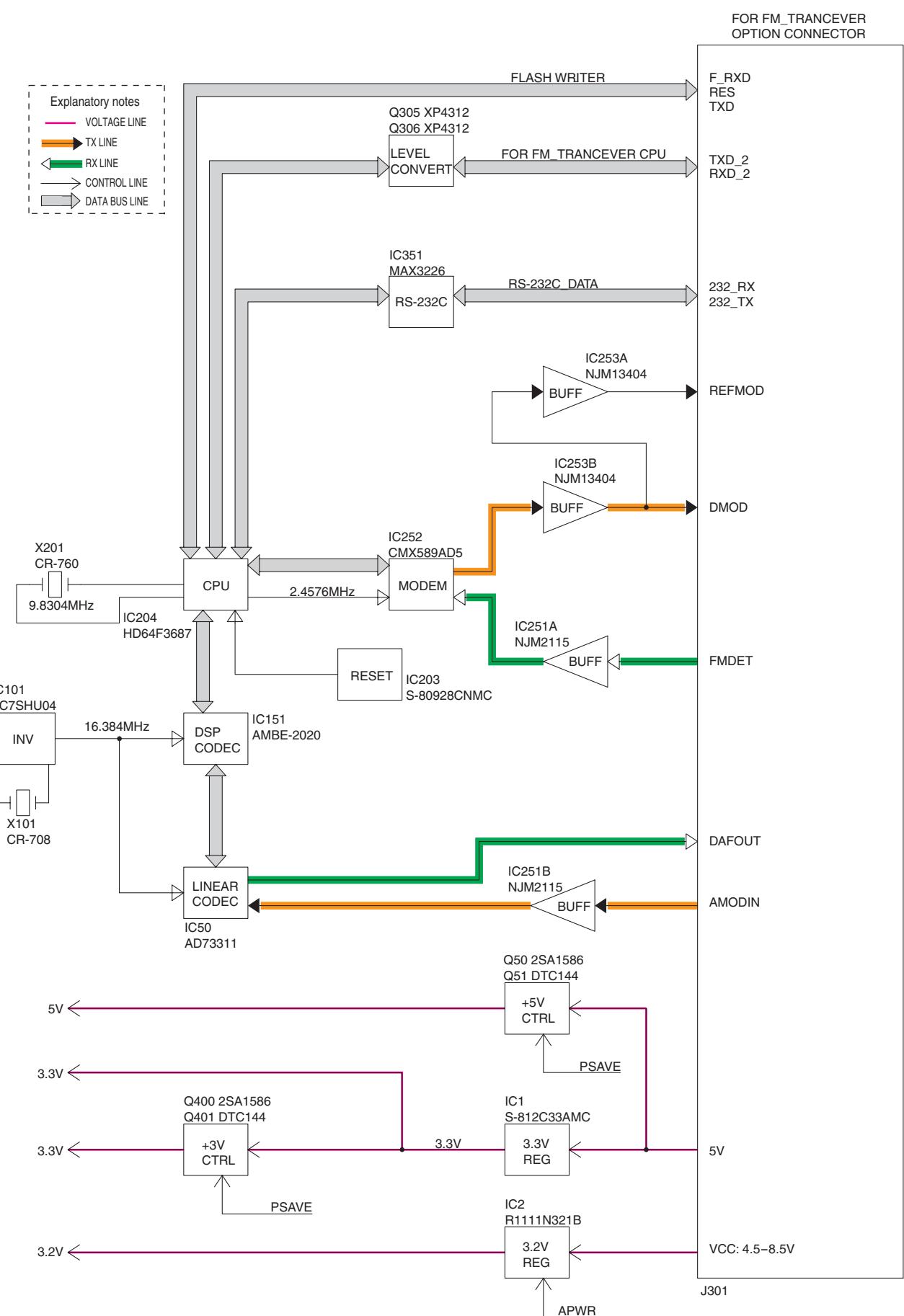
### • TRANSISTORS AND FET'S



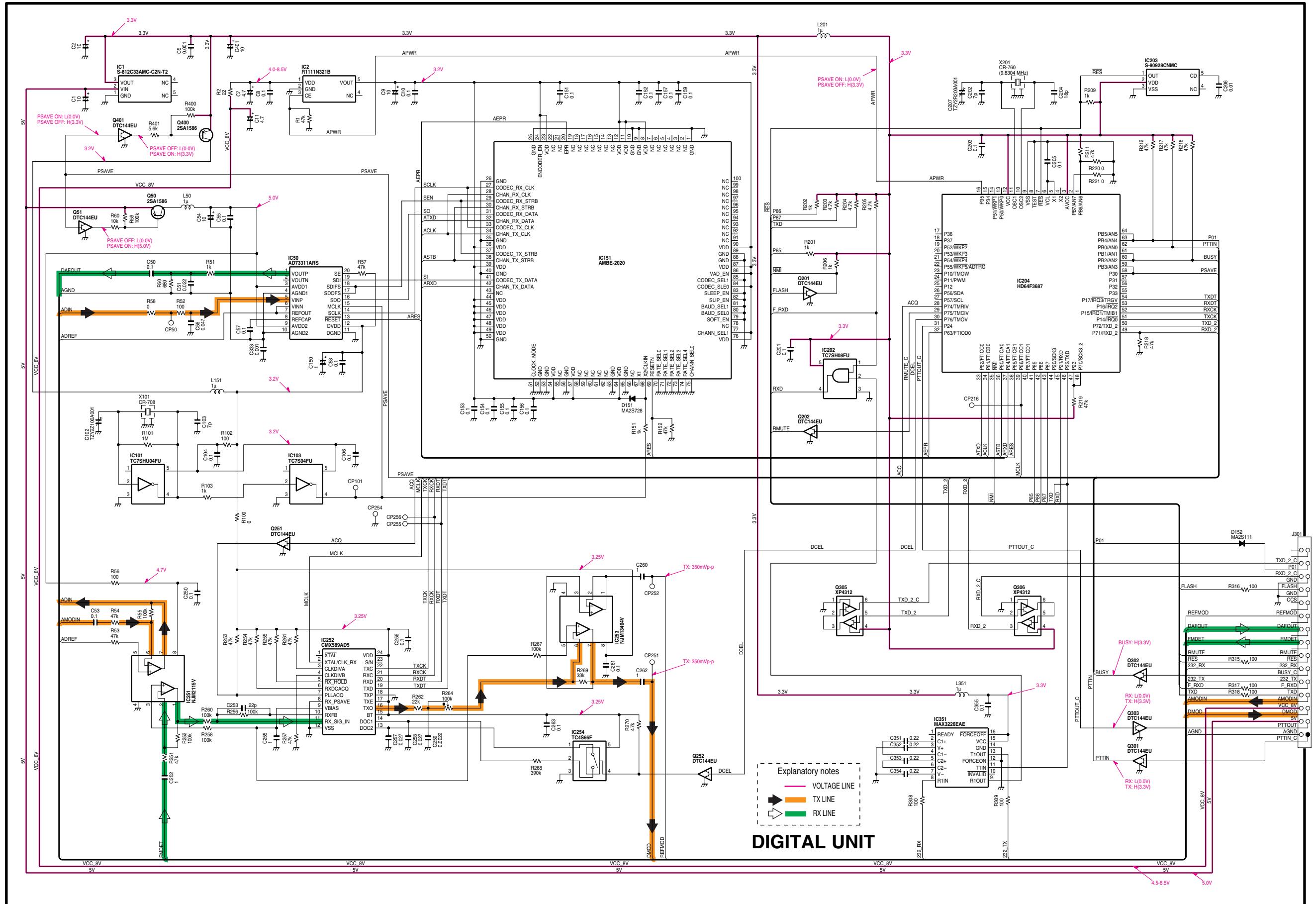
### • DIODES



## 12-3 UT-118 BLOCK DIAGRAM



## 12-4 UT-118 VOLTAGE DIAGRAM



DIGITAL UNIT

Explanatory notes

VOLTAGE LINE

TX LINE

RX LINE

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E-mail : [sales@icomamerica.com](mailto:sales@icomamerica.com)  
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**Count on us!**