

# DJ-V446

## Service Manual

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# SPECIFICATIONS

## General

Frequency range:	TX/RX 446.00625~446.09375MHz (12.5kHz step, 1~8ch)
Modulation:	8K50F3E (FM)
Memory channel:	200 channels
Ant. impedance:	50 Ω unbalanced
Frequency stability:	±2.5ppm
Mic impedance:	2k Ω
Supply voltage:	DC 7.0~16.0V (EXT DC-IN)
Current consumption:	600mA (typical) Transmit 250mA (typical) Receive at 500mW 70mA (typical) Standby 26mA (typical) Battery save on
Temperature range:	External DC: -10°C~+60°C (+14°F~+140°F) Battery packs: -10°C~+45°C (+14°F~+113°F)
Ground:	Negative ground
Dimension (projections excluded):	58(W) x 110(H) x 36.4(D)mm (2.28"(W) x 4.33"(H) x 1.43"(D)) (with EBP-65)
Weight:	Approx. 280g (9.9oz) (with EBP-65 and antenna)
Sub audible Tone (CTCSS):	encoder/decoder installed (39 tones)

## Transmitter

Power output:	Max. 500mW
Modulation:	Variable reactance
Spurious emission:	-60dB or less
Max deviation:	±2.5kHz
Mic. impedance:	2k Ω

## Receiver

System:	Double-conversion super heterodyne
Sensitivity:	-11.0dB μ (0.28 μ V)or less
Intermediate frequency:	1st IF 38.85MHz 2nd IF 450kHz
Selectivity:	-6dB: 6kHz or more -60dB: 13kHz or less
AF output:	500mW (MAX) 400mW (8 Ω, 10% distortion)

# CIRCUIT DESCRIPTION

## 1) Receiver System

The receiver system is a double superheterodyne system with a 38.85 MHz first IF and a 450 kHz second IF.

### 1. Front End

The received signal at any frequency in the 446.00625- to 446.09375-MHz (E version : 144.000- to 145.995-MHz) range is passed through the low-pass filter (L101, L102, L103, L113, C108, C120, C121, C124, C125, C126, C127 and C176) and ATT (Attenuator) circuit (Q120, R161, R187 and D112), and tuning circuit (C192, C193, C215, C216, D115, D116, L125 and L126), then amplified by the RF amplifier (Q114). The signal from Q114 is then passed through the tuning circuit (C200, C201, C219, C220, D117, D118, L128 and L129) and converted into 21.7 MHz by the mixer (Q116). The tuning circuit, which consists of C192, C193, C215, C216, L125, L126, variable capacitance diodes D115 and D116 and C200, C201, C219, C220, L128, L129, variable capacitance diodes D117 and D118, is controlled by the tracking voltage from the CPU so that it is optimized for the reception frequency. The local signal from the VCO is passed through the buffer (Q113), and supplied to the source of the mixer (Q116). The radio switches the lower and upper system at 420.000MHz : the lower side for the frequency up to 419.995 MHz and upper side for 420.000MHz and up.

### 2. ATT (Attenuator) Circuit

This circuit is used in case the receiving signal is disturbed by interfering signal(s), attenuating the receiving signal(s) to reduce the interference. CPU (IC109)'s pin 10 outputs a DC current to drive Q120, controlling D112's resistance to adjust the attenuation value.

### 3. IF Circuit

The mixer(Q116) mixes the received signal with the local signal to obtain the sum of and difference between them. The crystal filter (FL101) selects 38.85 MHz frequency from the results and eliminates the signals of the unwanted frequencies. The first IF amplifier (Q119) then amplifies the signal of the selected frequency. After the signal is amplified by the first IF amplifier (Q119), it is input to pin 16 of the demodulator IC (IC103). The second local signal of 38.85 MHz, which is oscillated by the internal oscillation circuit in IC103 and output of tripler circuit (L123, C202, C191, L122, Q115), is input through pin 1 of IC103. Then these two signals are mixed by the internal mixer in IC103 and the result is converted into the second IF signal with a frequency of 450kHz. The second IF signal is output from pin 3 of IC103 to the ceramic filter (FL103), where the unwanted frequency band of that signal is eliminated, and the resulting signal is sent back to the IC103 through 5 pins.

### 4. Demodulator Circuit

The second IF signal input via pin 5 is demodulated by the internal limiter amplifier and Quadrature detection circuit in IC103, and output as an audio signal through pin 9.

## **5. Audio Circuit**

The audio signal from pin 9 of IC103 is compensated to the audio frequency characteristics in the de-emphasis circuit (R223, R224, C241, C242) and amplified by the AF amplifier (Q196). The signal is then input to pin 1 of the electronic volume (IC107) for volume adjustment, and output from pin 2. The adjusted signal is sent to the audio power amplifier (IC106) through pin 2 to drive the speaker.

## **6. Squelch Circuit**

Part of the audio signal from pin 9 of IC103 is amplified by the noise filter amplifier and the internal noise amplifier in IC103. The desired noise of the signal is output through pin 14 of IC103 and input to pin 2 of CPU (IC109).

# **2) Transmitter System**

## **1. Modulator Circuit**

The audio signal is converted to an electric signal in either the internal or external microphone, and input to the microphone amplifier (IC102).

IC102 consists of four operational amplifiers; 1st amplifier (pins 1, 2, and 3) is composed of high-pass filter, 2nd amplifier (pins 12, 13, and 14) is composed of pre-emphasis and IDC circuits, 3rd amplifier (pins 8, 9, and 10) is composed of a splatter filter and 4th amplifier (pins 7, 6, and 5) is composed of a splatter filter. The maximum frequency deviation is determined to its optimal value by VR104 and input to the cathode of the variable capacitance diode of the VCO, to change the electric capacity in the oscillation circuit.

## **2. Power Amplifier Circuit**

The transmitted signal is oscillated by the VCO, amplified by the pre-drive amplifier (Q104) and drive amplifier (Q103), and input to the power amplifier (Q102). The signal is then amplified by the power amplifier (Q102) and led to the antenna switch (D101 and D103) and low-pass filter (L104, L103, L102, L101, C107, C108, C109, C110, C111, C120, C121, C124, C125, C126, and C127 ), where unwanted high harmonic signals are reduced as needed, and the resulting signal is supplied to the antenna.

## **3. APC Circuit**

Part of the transmission power from the low-pass filter is detected by D105, converted to DC, and then amplified by a differential amplifier ( Q111 ). The output voltage controls the bias voltage from the gate of Q102 and Q103 to maintain the transmission power constant.

### **3) PLL Synthesizer Circuit**

#### **1.CPU control**

The dividing ratio is obtained by sending data from the CPU (IC109) to pin 10, and sending clock pulses to pin 9 of the PLL IC (IC101). The oscillated signal from the VCO is amplified by the buffer (Q118), then input to pin 8 of IC101. Each programmable divider in IC101 divides the frequency of the input signal by N-value according to the frequency data, to generate a comparison frequency of 5 or 6.25 kHz.

#### **2. Reference Frequency Circuit**

The reference frequency appropriate for the channel steps is obtained by dividing the 12.8MHz reference oscillation (X102) by 2048 or 2560, according to the data from the CPU (IC109). When the resulting frequency is 5 kHz, channel steps of 5, 10, 15, 20, and 30 kHz are used. When it is 6.25 kHz, steps of 12.5, 25, and 50 kHz are used.

#### **3. Phase Comparator Circuit**

The PLL (IC101) uses the reference frequency, 5 or 6.25 kHz. The phase comparator in the IC101 compares the phase of the frequency from the VCO with that of the comparison frequency, 5 or 6.25 kHz, which is obtained by the internal divider in IC101.

#### **4. PLL Loop Fitter Circuit**

If a phase difference is found in the phase comparison between the reference frequency and VCO output frequency, the charge pump output (pin 5) of IC101 generates a pulse signal, which is converted to DC voltage by the PLL loop filter and input to the variable capacitance diode of the VCO unit for oscillation frequency control.

#### **5. VCO Circuit**

A Colpitts oscillation circuit driven by Q108 directly oscillates the desired frequency. The frequency control voltage determined in the CPU (IC109) and PLL circuit is input to the variable capacitance diodes (D109 and D110). This changes the oscillation frequency, which is amplified by the VCO buffer (Q110) and output from the VCO unit.

## **4) CPU and Peripheral Circuits**

#### **1. LCD Display Circuit**

The CPU turns ON the LCD via segment and common terminals with 1/3 the duty and 1/3 the bias, at the frame frequency of 112.5Hz.

#### **2. Display Lamp Circuit**

When the LAMP key is pressed, "L" is output from pin 42 of CPU (IC109) to the bases of Q152 then turns to ON and "H" is output from emitter of Q152 to the bases of Q146 to light LEDs (D131, D132).

### **3. Reset and Backup Circuits**

When the Output Voltage from pin 3 of IC110 drops to 4.5 V or below, the output signal from the reset IC (IC104), which has been input to pin 33 of the CPU (IC109), changes from "H" to "L" level. The CPU will then be in the backup state.

### **4. S(Signal)Meter Circuit**

The DC potential of pin 12 of IC103 is input to pin 1 of the CPU (IC109), converted from an analog to a digital signal, and displayed as the S-meter signal on the LCD.

### **5. Tone Encoder**

The CPU (IC109) is equipped with an internal tone encoder. The tone signal (67.0 to 250.3Hz) is output from pin 9 of the CPU to the variable capacitance diode of the VCO and 21.25MHz reference oscillation (X101) of the PLL IC (IC101) for modulation.

### **6. CTCSS Decoder**

The AF signal from the pin 9 of IC103 is filtered by an active filter (IC108) to eliminate the voice range of the signal then amplified and input to the pin 4 of the CPU (IC109). The signal is compared in the CPU with the pre-selected CTCSS values and the squelch opens in case the value matches.

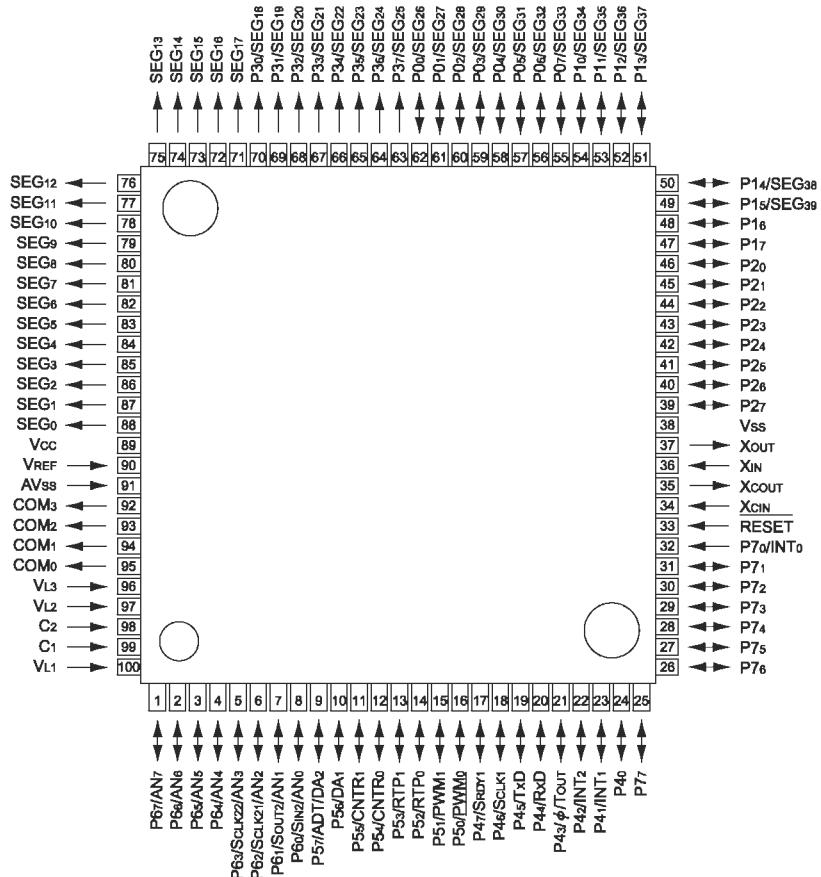
### **7. Clock Shift**

In case the selected frequency is disturbed by a CPU clock-noise, it may be eliminated by changing the CPU clock frequency. When the clock-shift is set, the pin 31 of the CPU (IC109) becomes Low turning ON the Q124. When Q124 becomes ON, X104's oscillation frequency shifts approximately by 200ppm.

## 5) M38268MCA-077GP ( XA1169 )

CPU

Terminal Connection  
( TOP VIEW )



No.	Terminal	Signal	I/O	Description
1	P67/AN7	SMT	I	S-meter input
2	P66/AN6	SQL	I	Noise level input for squelch
3	P65/AN5	BAT	I	Low battery detection input
4	P64/AN4	TIN	I	CTCSS tone input
5	P63/SCLK22/AN3	BP1	I	Band plan 1
6	P62/SCLK21/AN2	BP2	I	Band plan 2
7	P61/SOUT2/AN1		-	-
8	P60/SIN2/AN0	FKEY	I	Function / Monitor Key input
9	P57/ADT/DA2	CTOUT	O	CTCSS tone output
10	P56/DA1	DTOUT	O	ATT output
11	P55/CNTR1	SCL	O	Serial clock for EEPROM
12	P54/CNTR0	TBST	I/O	Tone burst output
13	P53/RTP1	BP4	I	Band plan 4
14	P52/RTP0	MUTE	I/O	Microphone mute
15	P51/PWM3	CLK	O	Serial clock output for PLL
16	P50/PWM0	DATA	I/O	Serial data output for PLL, CTCSS / PLL unlock signal input / EVR control output
17	P47/SROY1		-	-
18	P46/SCLK1	STBP	O	Strobe for PLL IC
19	P45/TXD	UTX	O	UART data transmission output
20	P44/RXD	URX	I	UART data reception input
21	P43/Φ TOUT	BEEP	I/O	Beep tone/Band plan 3 ( when the unit is turned on )
22	P42/INT2	RE2	I	Rotary encoder input
23	P41/INT1	RE1	I	
24	P40	CLO	O	CLONE ON/OFF output
25	P77	PTTK	I	PTT input
26	P76	CHG	I	Battery charge ON/OFF output
27	P75	P5C	O	PLL power ON/OFF output
28	P74	T5C	O	TX power ON/OFF output
29	P73	R5C	O	RX power ON/OFF output
30	P72	AFP	O	AF AMP power ON/OFF output
31	P71	CLSFT	O	CLOCK frequency shift
32	P70/INTO	BU	I	Backup signal detection input
33	RESET	RESET	I	Reset input
34	Xcin		-	-
35	Xcout		-	-
36	Xin	XIN	-	Main clock input
37	Xout	XOUT	-	Main clock output
38	Vss	GND	-	CPU GND
39	P27	PSW	I	Power switch input
40	P26	SDA	O	Serial data for EEPROM
41	P25	C5C	O	C5V power ON/OFF output
42	P24	LAMP	O	Lamp ON/OFF
43	P23	KI0	I	
44	P22	KI1	I	
45	P21	KI2	I	
46	P20	KI3	I	
47	P17	KO3	O	
48	P16	KO2	O	
49	P15/SEG39	KO1	O	
50	P14/SEG38	KO0	O	
51	P13/SEG37	DA3	O	DA converter for Tx output power
52	P12/SEG36	DA2	O	DA converter for Tx output power
53	P11/SEG35	DA1	O	DA converter for Tx output power
54	P10/SEG34	AFC/DA0	O	DA converter for Tx output power
				Voice Scrambler Board detection
55	P07/SEG33	EXP	I/O	(when the unit is turned on )
56	P06/SEG32	SD/PO	O	Signal detection output

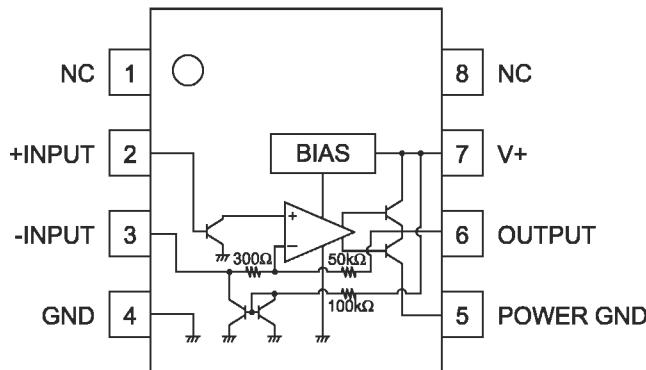
No.	Terminal	Signal	I/O	Description
57	P05/SEG31	SEG31	O	
58	P04/SEG30	SEG30	O	
59	P03/SEG29	SEG29	O	
60	P02/SEG28	SEG28	O	
61	P01/SEG27	SEG27	O	
62	P00/SEG26	SEG26	O	
63	P37/SEG25	SEG25	O	
64	P36/SEG24	SEG24	O	
65	P35/SEG23	SEG23	O	
66	P34/SEG22	SEG22	O	
67	P33/SEG21	SEG21	O	
68	P32/SEG20	SEG20	O	
69	P31/SEG19	SEG19	O	
70	P30/SEG18	SEG18	O	
71	SEG17	SEG17	O	
72	SEG16	SEG16	O	LCD segment signal
73	SEG15	SEG15	O	
74	SEG14	SEG14	O	
75	SEG13	SEG13	O	
76	SEG12	SEG12	O	
77	SEG11	SEG11	O	
78	SEG10	SEG10	O	
79	SEG9	SEG9	O	
80	SEG8	SEG8	O	
81	SEG7	SEG7	O	
82	SEG6	SEG6	O	
83	SEG5	SEG5	O	
84	SEG4	SEG4	O	
85	SEG3	SEG3	O	
86	SEG2	SEG2	O	
87	SEG1	SEG1	O	
88	SEG0	SEG0	O	
89	Vcc	VDD	-	CPU power terminal
90	Vref	Vref	-	AD converter power supply
91	Avss	Avss	-	AD converter GND
92	COM3	COM3	O	LCD COM3 output
93	COM2	COM2	O	LCD COM2 output
94	COM1	COM1	O	LCD COM1 output
95	COM0	COM0	O	LCD COM0 output
96	VL3	VL3	-	LCD power supply
97	VL2	VL2	-	
98	C2	C2	-	-
99	C1	C1	-	-
100	VL1	VL1	I	LCD power supply

# SEMICONDUCTOR DATA

## 1) NMJ2070MT1 ( XA0210 )

Low Voltage Power Amplifier

Equivalent Circuit

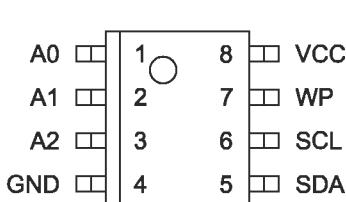


V+=6V, Ta=25±2°C

Parameter	Condition		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V+=		V+	1.8	-	15	V
Idle current	RL=		I <sub>Q</sub>	-	4	7	mA
Output voltage	V <sub>O</sub>		V <sub>O</sub>	-	2.7	-	V
Input bias current	I <sub>B</sub>		I <sub>B</sub>	-	200	-	nA
Output power	THD=10%, f=1kHz	V+=6V, RL=4	P <sub>O</sub>	0.5	0.6	-	W
		V+=4.5V, RL=4		-	0.32	-	W
		V+=3V, RL=4		-	120	-	mW
		V+=2V, RL=4		-	30	-	mW
	THD=10%, f=1kHz	V+=6V, RL=4		-	500	-	mW
		V+=4.5V, RL=4		-	250	-	mW
Distortion	Po=0.4W, RL=4 , f=1kHz		THD	-	0.25	-	%
Voltage gain	f=1kHz		A <sub>V</sub>	41	44	47	dB
Input impedance	f=1kHz		Z <sub>IN</sub>	100	-	-	k
Equivalent input noise voltage	R <sub>S</sub> =10k	A curve	V <sub>n1</sub>	-	2.5	-	μV
		B=22Hz to 22kHz	V <sub>n2</sub>	-	3	-	μV
Power supply voltage rejection ratio	f=100Hz, C <sub>x</sub> =100 μF		SVR	24	30	-	dB
Power gain band width (-3dB)	RL=8 , Po=250mW		P.B	-	200	-	kHz

## 2) S24CS64A01-J8T1G ( XA1117 )

16K bits CMOS Serial EEPROM

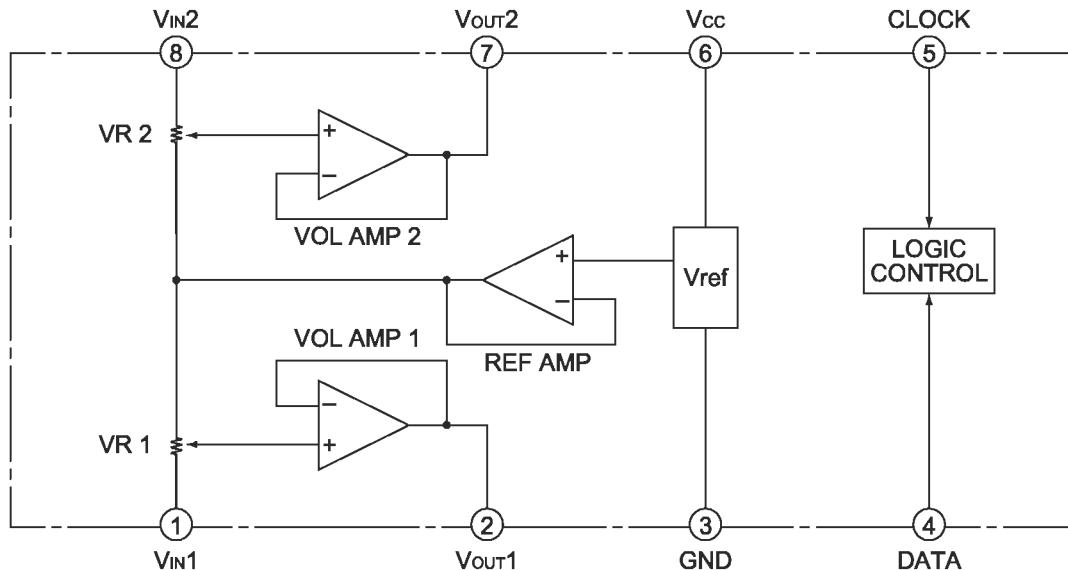
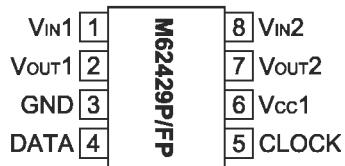


Pin Number	Pin Name	Function
1	A0	Slave address input
2	A1	Slave address input
3	A2	Slave address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to Vcc: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

Remark See Dimensions for details of the package drawings.

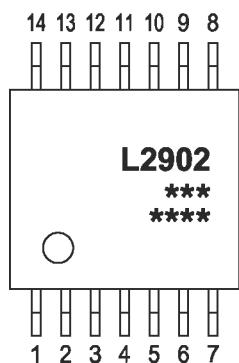
### 3) M62429FP/CF0J ( XA1118 )

Electronic Volume



### 4) LM2902PWR ( XA1106 )

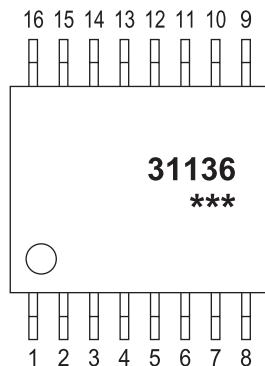
Quad Operational Amplifiers



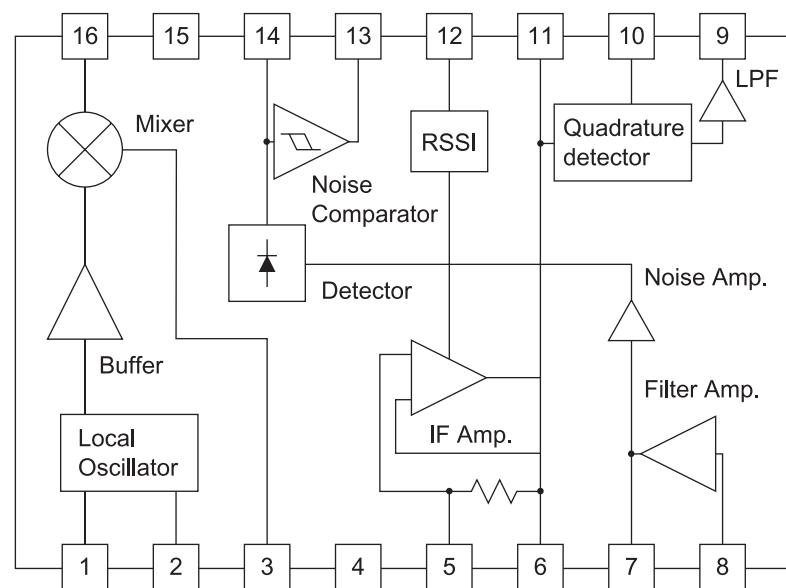
1. Output A
2. Inverting Input A
3. Non-inverting Input A
4. Vcc
5. Non-inverting Input B
6. Inverting Input B
7. Output B
8. Output C
9. Inverting Input C
10. Non-inverting Input C
11. GND
12. Non-inverting Input D
13. Inverting Input D
14. Output D

## 5) TA31136FN(EL) ( XA0404 )

Low Power FM IC

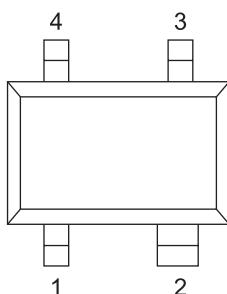


1. OSC IN	9. AF OUT
2. OSC OUT	10. QUAD
3. MIX OUT	11. IF OUT
4. Vcc	12. RSSI
5. IF IN	13. N-DET
6. DEC	14. N-REC
7. FIL OUT	15. GND
8. FIL IN	16. MIC IN



## 6) S80845CLNB-B66-T2G ( XA1120 )

C-MOS Voltage Detector

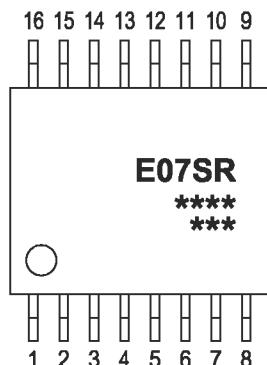


Pin No.	Pin name	Pin description
1	OUT	Voltage detection output pin
2	VDD	Voltage input pin
3	NC <sup>*1</sup>	No connection
4	VSS	GND pin

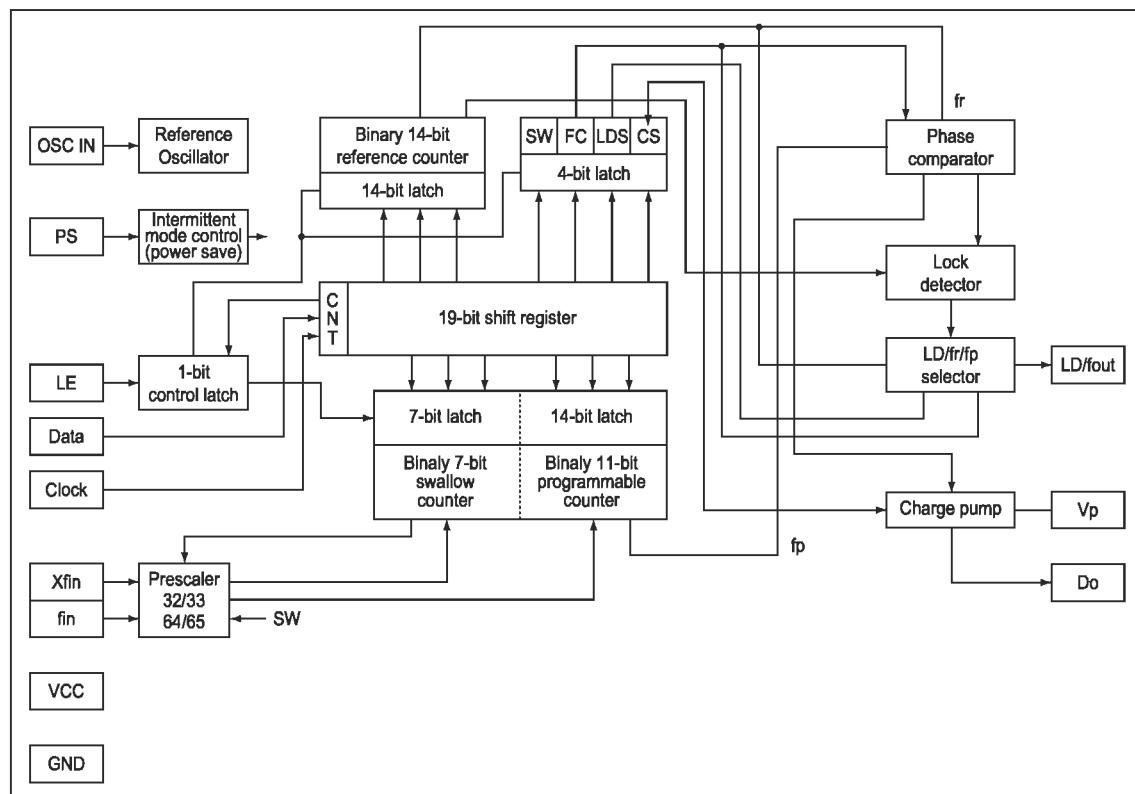
\*1. The NC pin is electrically open.  
The NC pin can be connected to VDD or VSS.

## 7) MB15E07SR ( XA1107 )

PLL Synthesizer



- |           |               |
|-----------|---------------|
| 1. OSC IN | 9. CLOCK      |
| 2. N. C.  | 10. Data      |
| 3. Vp     | 11. LE        |
| 4. Vcc    | 12. PS        |
| 5. Do     | 13. N. C.     |
| 6. GND    | 14. LD / fout |
| 7. Xfin   | 15. N. C.     |
| 8. fin    | 16. N. C.     |

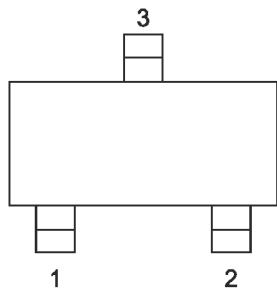


(Vcc=2.7 to 5.0V, Ta=-40°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	-	2.7	3.75	5.0	V
Power supply current	Icc	2500MHz Vcc=Vp=3.75V		8.0		mA
LPF supply voltage	Vp	-	Vcc	-	5.5	V
Local oscillator input level	Vfin	100MHz to 300MHz 300MHz to 2500MHz	-6 -15		+2 +2	dBm
Local oscillator input frequency	fin	-	100		2500	MHz
Xin input level	Vxin	-	0.5		Vcc	Vp-p
Xin input frequency	Fxin	-	3		40	MHz

## 8) XC6202P502MR ( XA1119 )

Voltage Regulator



Pin No.	Pin name	Function
1	VOUT	Regulated Voltage Output
2	VIN	Supply Voltage Input
3	VSS	Ground

### Absolute Maximum Ratings

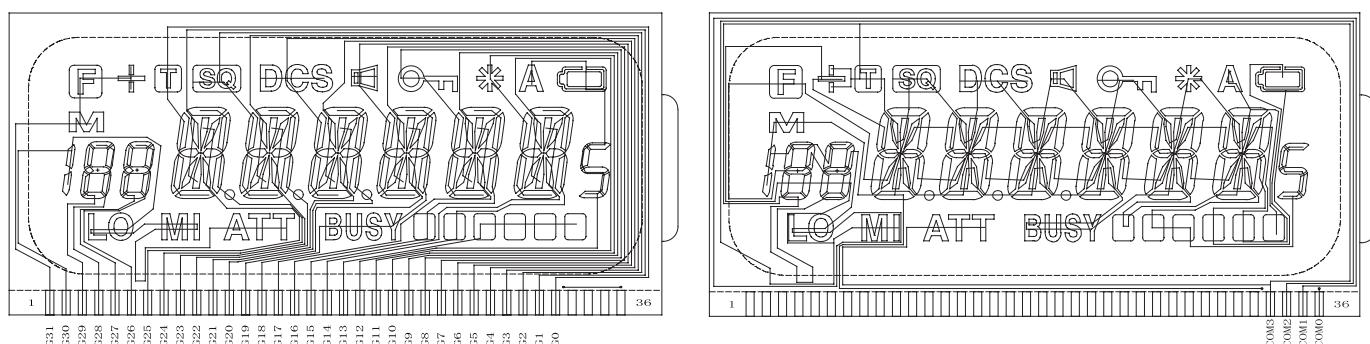
Parameter	Symbol	Rating	Units
Input Voltage	VIN	22	V
Output Current	IOUT	500	mA
Output Voltage	VOUT	VSS-0.3~VIN+0.3	V
Power Dissipation	Pd	150	mW
Operating Ambient Temperature	Topr	-40~+85	°C
Storage Temperature	Tstg	-55~+125	°C

## 9) Transistor, Diode and LED outline Drawings

Top View

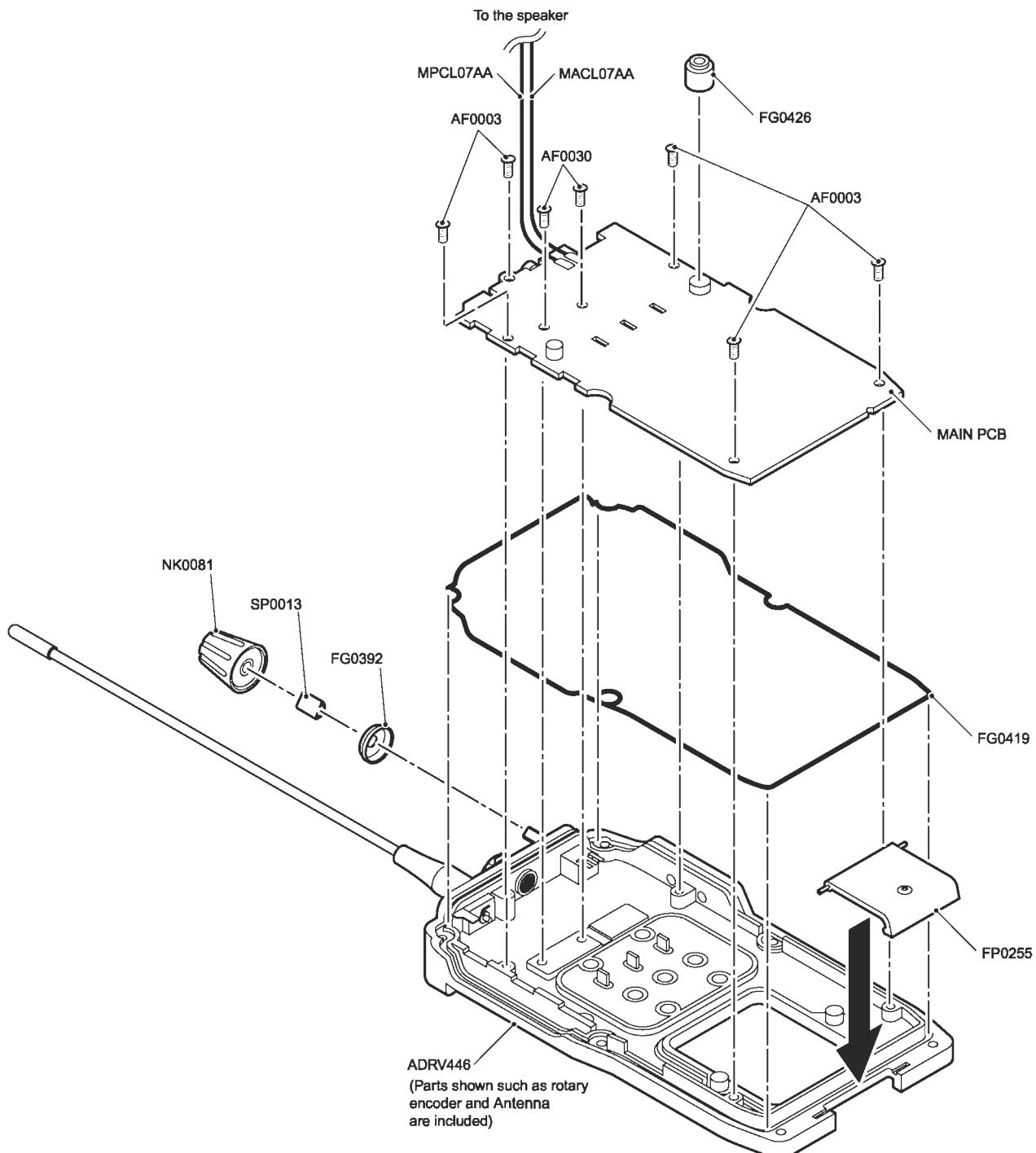
MA741WA-(TX) XD0251	1SS362(TE85L) XD0338	1SV308(TPH3) XD0339	MAZS0270HL XD0377	1SV314(TPH3,F) XD0403	1SS423(TE85L,F) XD0416	RB521S-30TE61 XD0418
1SS400TE61 XD0419	FA3J3STP XD0420	HSC277TRF-E XD0422	S3JB-T XD0424	SML-310MTT86 XL0036	SML-521MUWT86 XL0097	
3SK293 TE85L XE0053	SSM3K15FV(TPL) XE0069	2SK3475(TE12L,F) XE0070	2SK3476(TE12L,Q) XE0071	2SB766A-(TX)R XT0170	2SC5066FT-Y XT0180	2SC6026MFV XT0210
2SA1955FV-A(TPL3) XT0212	2SC5659T2L XT0213	HN2C01FE-GR(T5LF) XT0214	RN1107MFV(TPL3) XU0210	RN2107MFV(TPL3) XU0211	RN2115MFV(TPL3) XU0212	RN1111MFV(TPL3,F) XU0213
			Rb=10kohm Rbe=47kohm	Rb=10kohm Rbe=47kohm	Rb=2.2kohm Rbe=10kohm	Rb= min :7kohm typ. : 10kohm max :13kohm Rbe=none
RN2111MFV(TPL3) XU0220						

## 10) LCD Connection ( EL0059 )

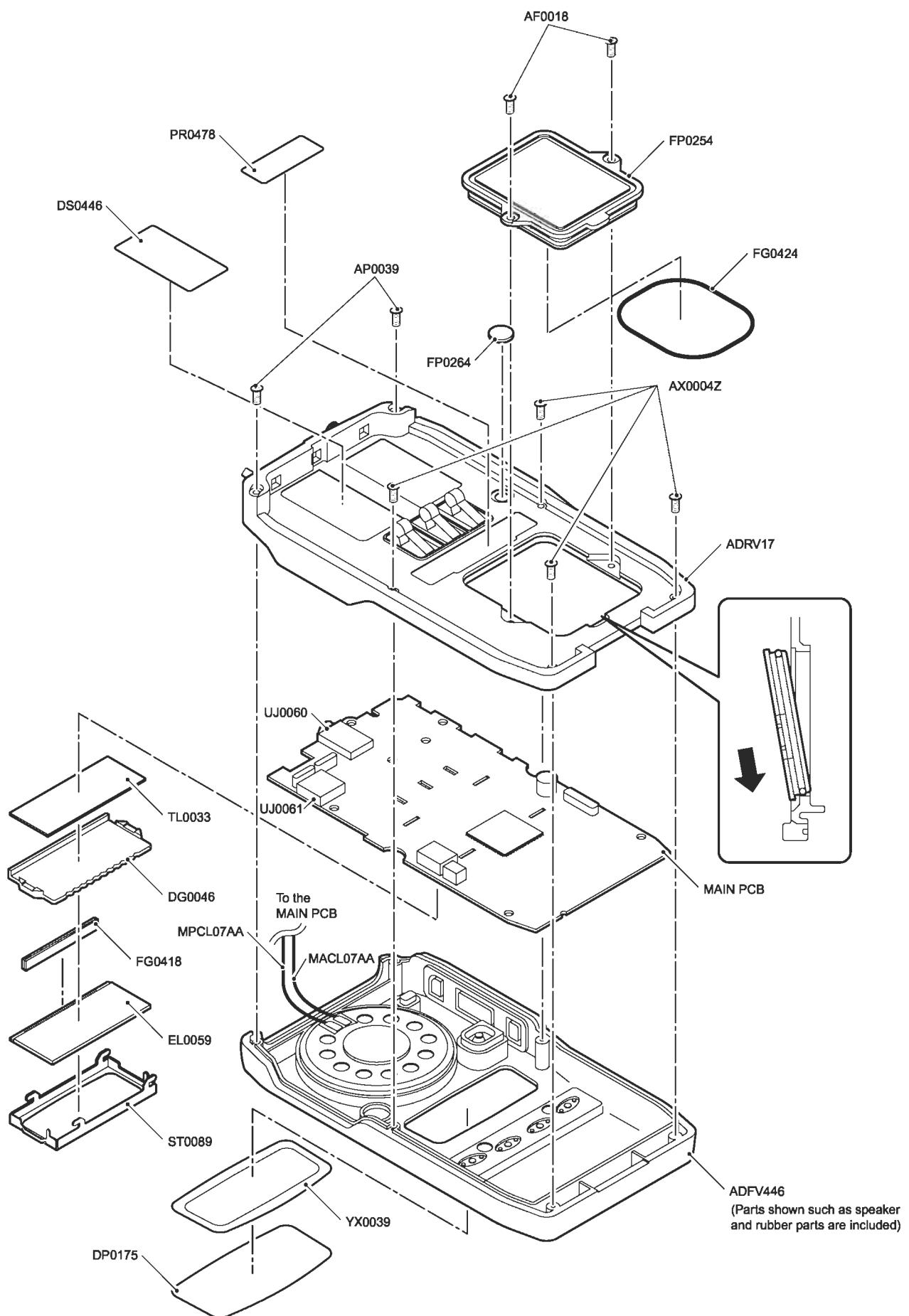


# EXPLODED VIEW

## 1) Front View



## 2) Rear View















Ref. No.	Parts No.	Description	Parts Name
	FP0254		REAR COVER
	FP0255		ROCK LEVER
	FP0264		BLIND SEAL
	NK0081		VOL KNOB
	SP0013		LECTRA #7800
	ST0089		LCD HOLDER
	TL0033		REFLECTIVE SHEET
	YX0039		LCD TAPE DJS45

## Packing Unit

Ref. No.	Parts No.	Description	Parts Name	Version
	EG0065	BATTERY	EBP-65A P BAG	
	EDC147	ADAPTOR	ADAPTOR 230V	
	EDC148	ADAPTOR	ADAPTOR 230V (UK)	EUK
	PR0478		SERIAL SEAL	
	DS0446		NITTO MODEL PLATE(S)	
	HU0238		INNER DJV446	
	PS0526	INSTRUCTION MANUAL	INSTRUCTION DJV446	
	PK0115		CIRCUIT DIAGRAM V446	
	HK0647		INDI PACKAGE DJV446	
	HP0034		PLA.BAG 5X125X400	
	BH0017	BELT CLIP	BELT CLIP	
	BB0009Y	HAND STRAP	HAND STRAP DJS41	
	AA0076		PH M3+6FE/B-ZN	
	HP0003		PLA.BAG 5X75X110	

**CAUTION:** RISK OF EXPLOSION IF BATTERY IS REPLACED BY AN INCORRECT TYPE. DISPOSE OF USED BATTERIES ACCORDING TO THE INSTRUCTIONS.

# ADJUSTMENTS

## 1) Required Test Equipment

The following items are required to adjust radio parameters

### 1. Regulated power supply

Supply voltage: 13.8 DC  
Current: 3A or more

### 2. Digital multimeter

Voltage range: FS = Approx. 20V  
Current: 10A or more  
Input resistance: High impedance

### 3. Oscilloscope

Measurable frequency: Audio frequency

### 4. Audio dummy load

Impedance: 8Ω  
Dissipation: 1W or more  
Jack: 3.5mm Φ

### 5. SSG

Output frequency: 500MHz or more  
Impedance: 50Ω, unbalanced  
Modulation: FM

### 6. Power meter

Measurable frequency: 500MHz or more  
Impedance: 50Ω, unbalanced  
Measuring range: 10W or more

### 7. Audio volmeter

Measurable frequency: Up to 100kHz  
Sensitivity: 1mV to 10V

### 8. Audio generator

Output frequency: 67Hz to 10kHz  
Output impedance: 600Ω, unbalanced

### 9. Distortion meter/SINAD meter

Measurable frequency: 1kHz  
Input level: Up to 40dB  
Distortion: 1%-100%

### 10. Frequency counter

Measurable frequency: 500MHz or more  
Measurable stability: Approx. ±0.1ppm

### 11. Linear detector

Measurable frequency: 500MHz or more  
Characteristics: Flat  
CN: 60dB or more

**Note:**

- (1). SSG initial setting
  - Modulation Frequency : 1kHz
  - Modulation Level : 1.5kHz
- (2). Necessary optional accessory : EDS-10 ( Microphone/Speaker Cable )
- (3). Reference sensitivity : 12dB SINAD
- (4). Specified audio output level : 500mW at 8Ω
- (5). Standard audio output level : 50mW at 8Ω
- (6). Use an RF cable ( 3D2W : 1M ) for test equipment.
- (7). Attach a fuse to the RF test equipment.
- (8). All SSG outputs are indicated by EMF
- (9). Supply voltage for the transceiver : 13.8VDC

**2)Preparation:**

1. Turn off the power of the adjusting unit (the unit hereafter).
2. Remove the screw ①.
3. Remove the rear cover ②.
4. Turn on the unit by pressing "F" key and "V/M" key together. The display will be blank out for 2 seconds then comes back normal.

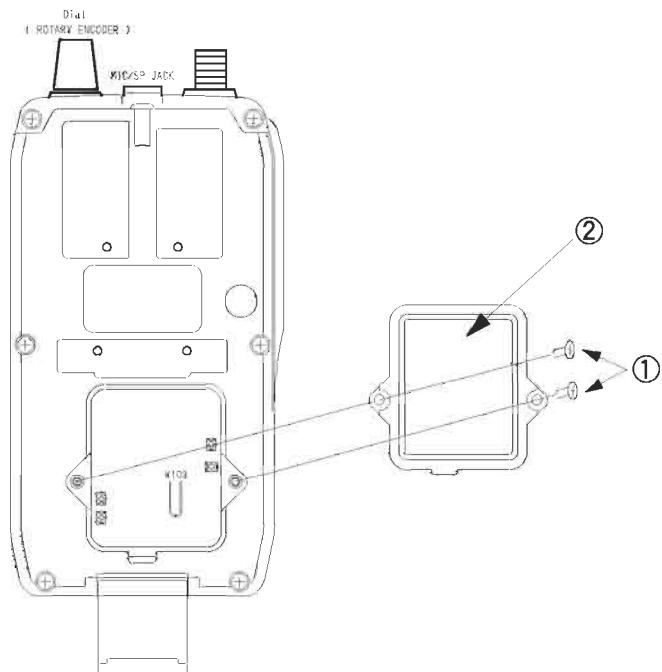


Chart 1 : Removing the rear cover

### 3) Adjustment mode

The adjustment should be operated in the Adjustment mode. Therefore except for the reference frequency, deviation and tone-deviation adjustments an operator won't touch the components on the board, but most of the adjustments should be done by operating the dial and keys on the unit. During such operation, memory channels are used temporary therefore it is required to program memories before the unit is set to the adjustment mod. Please refer the chart below for the programming channels. The channels may be varied depending on the RF environment around your work area, and refer the instruction manual for how to program the memories into the memory-channels.

To enter the adjustment mode, press "F" then "KL" to key-lock the unit. Then press the keys in order of "MONI", "V/M" 6 times, "SCAN" twice, "T SQL" twice and "V/M". Observe that decimal points appear on the display on both side of the channel number. To exit from the adjustment mode, repeat the whole sequence (key-lock then enter the code in order). NEVER RESET THE UNIT WHILE OPERATING IN THE SET MODE. This may reset whole adjustment values resulting the malfunction of the unit in the operating mode. The chart below shows the adjustment points and interface between the unit and instruments. Please use an attenuator in case the specifications of the linear-detector and frequency counter may exceed the requirement herein.

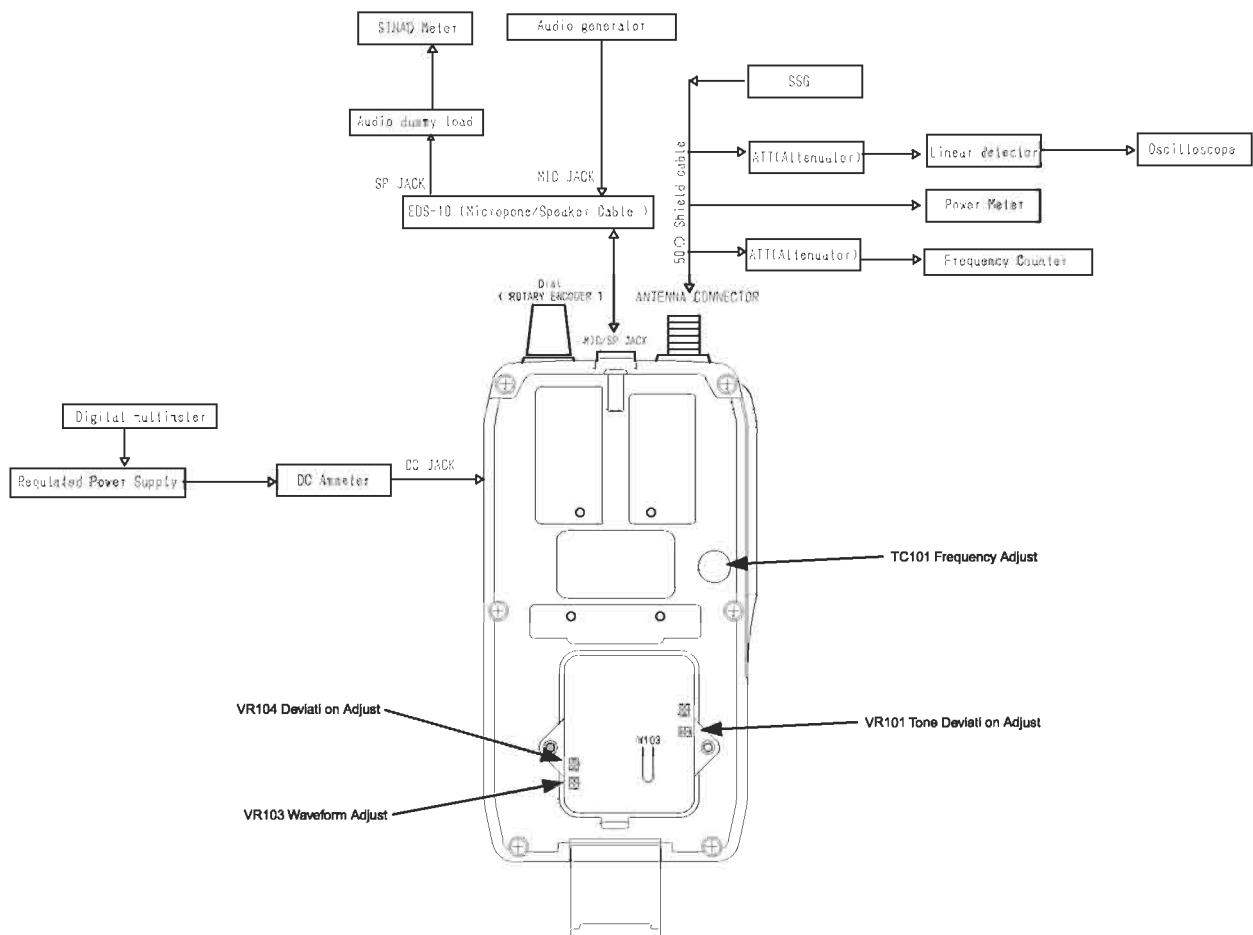


Chart 2 : Adjustment points and interface between the unit and instruments

Table 1: Memory programming for adjustment mode

\* Simply memory the frequencies only into the relative memory channels.

<b>Channel</b>	<b>Adjustment menu</b>	<b>Channel No.</b>
1	Frequency Adjustment	5-OF
3	TX-output	5-OF
4	Microphone deviation	5-OF
8	CTCSS tone deviation	5-OF
11	Check Tone-burst tone deviation	5-OF
13	Sensitivity adjustment	5-OF
15	Squelch adjustment (minimum)	5-OF
16	Squelch adjustment (maximum)	5-OF
17	S-meter adjustment (1)	5-OF
18	S-meter adjustment (Full)	5-OF
19	ATT (Attenuator) adjustment	5-OF
25	Low-battery icon appearance (Alkaline)	5-OF

## 1. Frequency adjustment

Select memory ch.1.

Press PTT on the unit to transmit and measure the TX frequency. Align TC101 to bring the value to the range specified below.

**Specification value : ±50Hz**

Necessary instrument : Frequency counter

## 2. TX output

Select memory ch.3.

Press PTT on the unit to transmit. One of digits 0-F should appear on the display where memory channel number was shown. Rotate the dial on the unit to adjust the TX power to meet the specification. Release the PTT to finish the adjustment. Be sure to check the consuming current value after the adjustment is completed.

**Specification :**

**TX-output power : 0.5 watts**

Necessary instrument : Power meter

### **3. Microphone deviation**

Select memory ch.4.

Input the signal as specified below from an Audio generator and transmit. Measure the deviation value using a Liner-detector. Align VR104 to bring the value to the range specified below.

**Specification :  $2.2 \pm 0.1$ kHz**

Measuring condition :

(1). Audio generator setting

Frequency : 1kHz

Output Level : 50mV

Necessary instrument : Audio generator / Linear detector

Optional accessory required : EDS-10

### **4. CTCSS tone 88.5Hz deviation and adjustment of the sign-wave**

Select memory ch.8.

Press PTT to automatically transmit 88.5Hz tone. Measure the deviation value using a Liner-detector. Align VR101 to bring the value to the range specified below. Use an oscilloscope to monitor the sign-wave then correct the wave shape (see the chart 3 below).

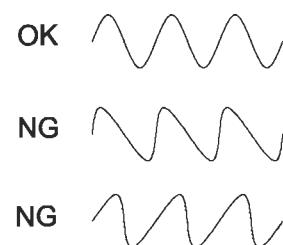


Chart 3: sign-wave correction

**Specification :  $0.50 \pm 0.05$ Hz**

Necessary instrument : Linear detector / Oscilloscope

### **5. Check Tone-burst tone 1750Hz deviation**

Select memory ch.11.

Press PTT to automatically transmit a tone-burst tone 1750Hz. Make sure the value is within the specification using a linear-detector.

**Specification :  $1.3 \sim 1.7$ kHz**

Necessary instrument : Linear detector

## **6. Receiver sensitivity adjustment**

Preparation : Set the speaker audio output level to 50mW.

Operation : Set the memory channels accordingly. Input an RF signal from the SSG to the antenna connector then measure output signal at the speaker jack using a SINAD meter.

Press "F" (FUNC) key on the unit. One of digits 0-FF should appear on the display where memory channel number was shown. Rotate the dial on the unit to bring the SINAD value to 12dB or better.

Condition :

(1). Memory Channel : 13

(2). SSG setting

Frequency : 446.05625MHz

RF Output Level : -4.0dB  $\mu$

Modulation Frequency : 1kHz

Modulation Level : 1.5kHz

Necessary instruments : Audio voltmeter/SSG/SINAD Meter/Audio dummy load

Optional accessory required : EDS-10

### **Note:**

Press "FUNC" key or leave the unit for 5 seconds to enter the new values and go to the next adjustment procedure. Memory number should appear on the display when the unit exits the sensitivity adjustment.

## **7. Squelch adjustments:**

Select the memory channel number accordingly to adjust the level Min and Max.

Input an RF signal to the antenna connector from SSG then press FUNC key on the unit. A beep ("pip") sounds and completes the adjustment.

### **a. Squelch level (Min.)**

Condition :

(1). Memory Channel : 15

(2). SSG setting

Frequency : 446.05625MHz

RF Output Level : -9.0dB  $\mu$

Modulation Frequency : 1kHz

Modulation Level : 1.5kHz

### **b. Squelch level (Max.)**

Condition :

(1). Memory Channel : 16

(2). SSG setting

Frequency : 446.05625MHz

RF Output Level : 0dB  $\mu$

Modulation Frequency : 1kHz

Modulation Level : 1.5kHz

Necessary instrument : SSG

## **8. S-meter adjustments**

Select the memory channel number accordingly to adjust the S-meter level 1 and full.

Input an RF signal to the antenna connector from SSG then press FUNC key on the unit. A beep ("pip") sounds and completes the adjustment.

### **a. S-meter level 1**

Condition :

(1). Memory Channel : 17

(2). SSG setting

Frequency : 446.05625MHz

RF Output Level : 0dB  $\mu$

Modulation Frequency : 1kHz

Modulation Level : 1.5kHz

### **b. S-meter level Full**

Condition :

(1). Memory Channel : 18

(2). SSG setting

Frequency : 446.05625MHz

RF Output Level : 20dB  $\mu$

Modulation Frequency : 1kHz

Modulation Level : 1.5kHz

Necessary instrument : SSG

## **9. Attenuator adjustment**

Select the memory ch.19.

Input an RF signal to the antenna connector from SSG then press FUNC key on the unit.

One of digits 0-FF should appear on the display where memory channel number was shown. Rotate the dial on the unit to adjust to the point that the S-meter shows 5th segment just from the 4th (OK even 5th may blinks).

Condition :

(1). SSG setting

Frequency : 446.05625MHz

RF Output Level : 20dB  $\mu$

Modulation Frequency : 1kHz

Modulation Level : 1.5kHz

Necessary instrument : SSG

### **Note:**

- (1) Press "FUNC" key or leave the unit for 5 seconds to go to the next adjustment procedure. Memory number should appear on the display when the unit exits this adjustment point.
- (2) The S-meter adjustment should be completed before you perform this operation.

## 10. Low-battery icon appearance ( Alkaline )

Select the memory ch.25.

Press "F" (FUNC) key on the unit. One of digits 0-FF should appear on the display where memory channel number was shown. Rotate the dial on the unit to select "6A". The value can be varied by rotating the dial, but select always 6A.

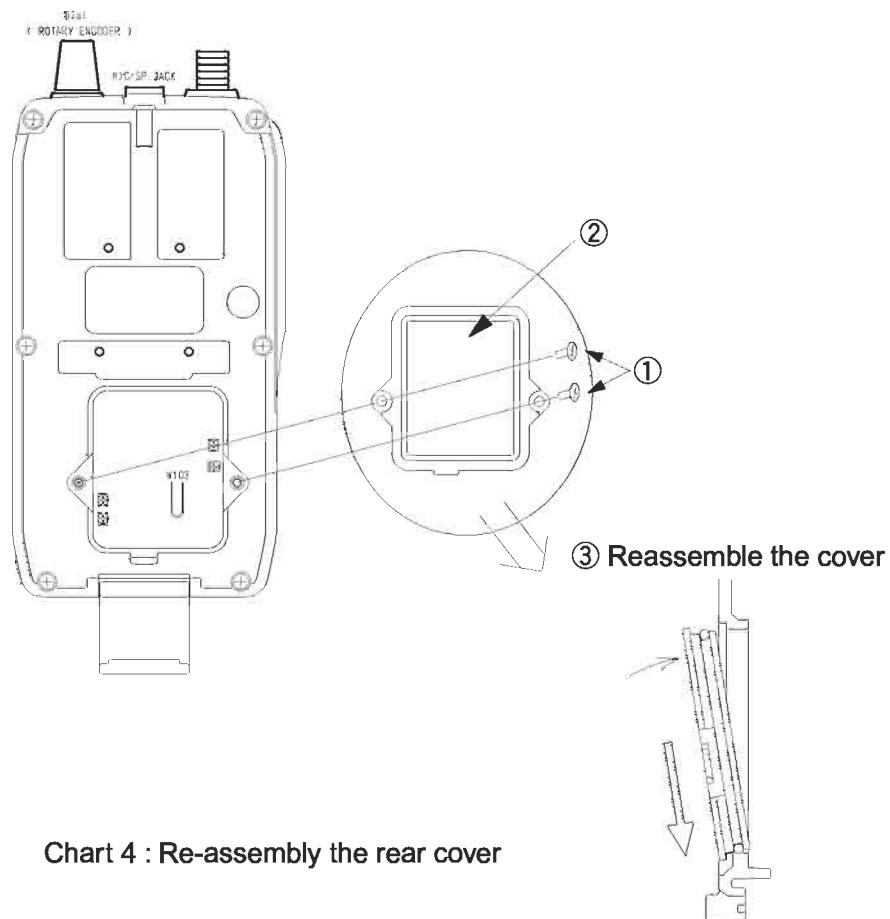
### Note:

Press "FUNC" key or leave the unit for 5 seconds to go to the next adjustment procedure.

Memory number should appear on the display when the unit exits this adjustment point.

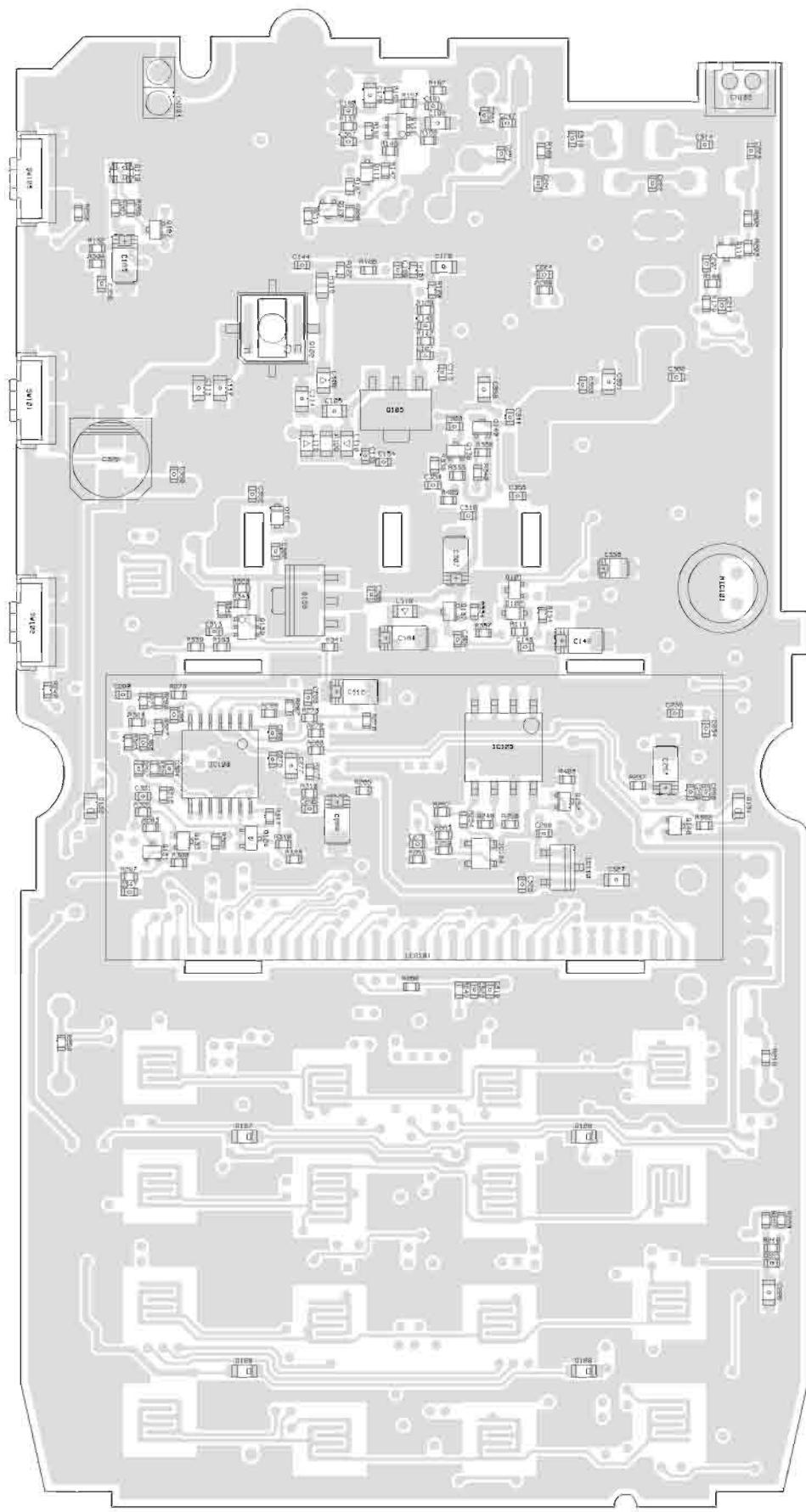
## 4) Re-assembly

1. Turn off the unit.
2. According to the instruction below ③, mount the rear-cover ②.
3. Securely screw ① to fix the cover.
4. Turn on the unit by pressing "F" key and "V/M" key together to reset the CPU. The display will be blank out for 2 seconds then comes back normal.

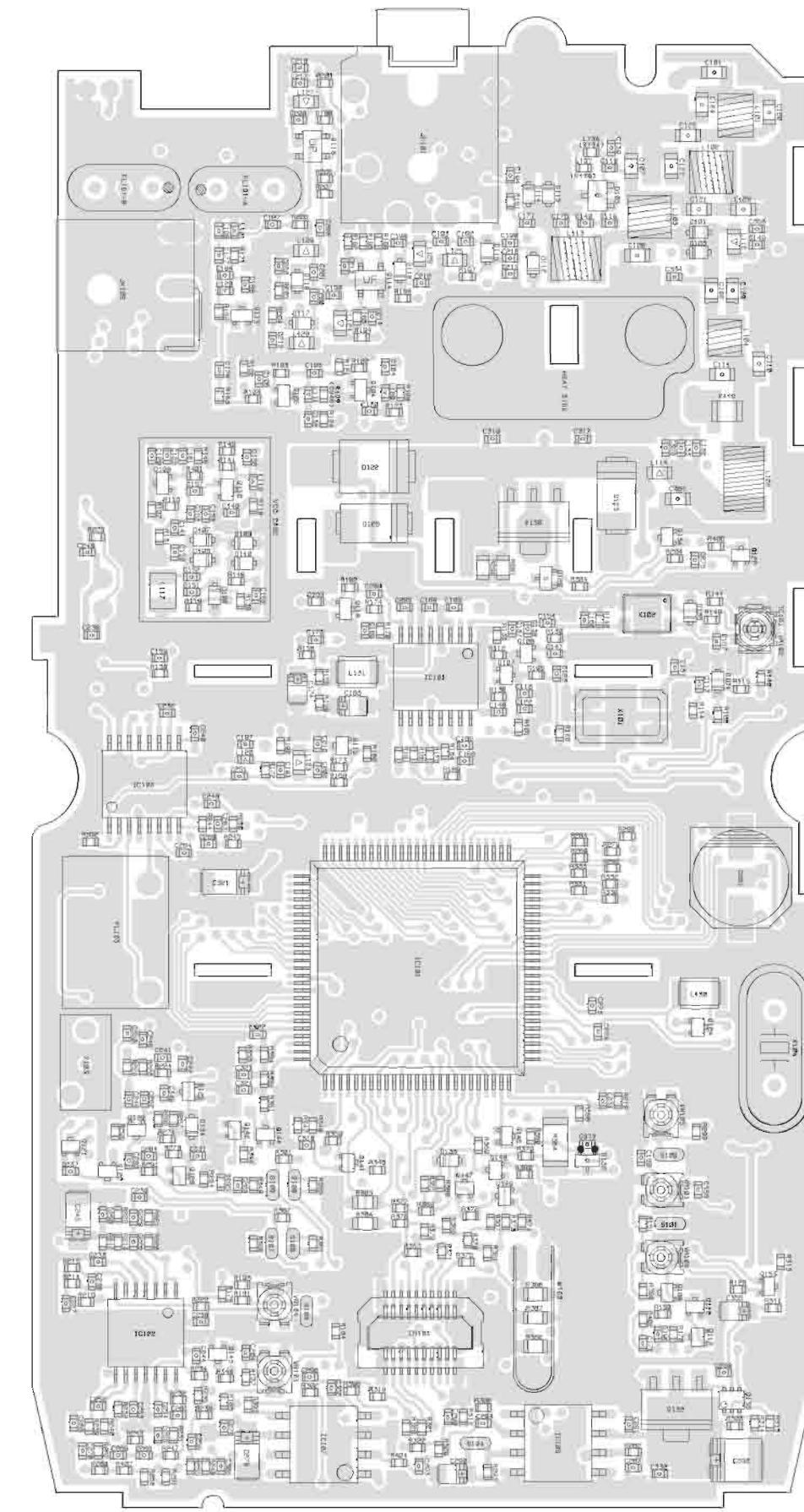


## PC BOARD VIEW

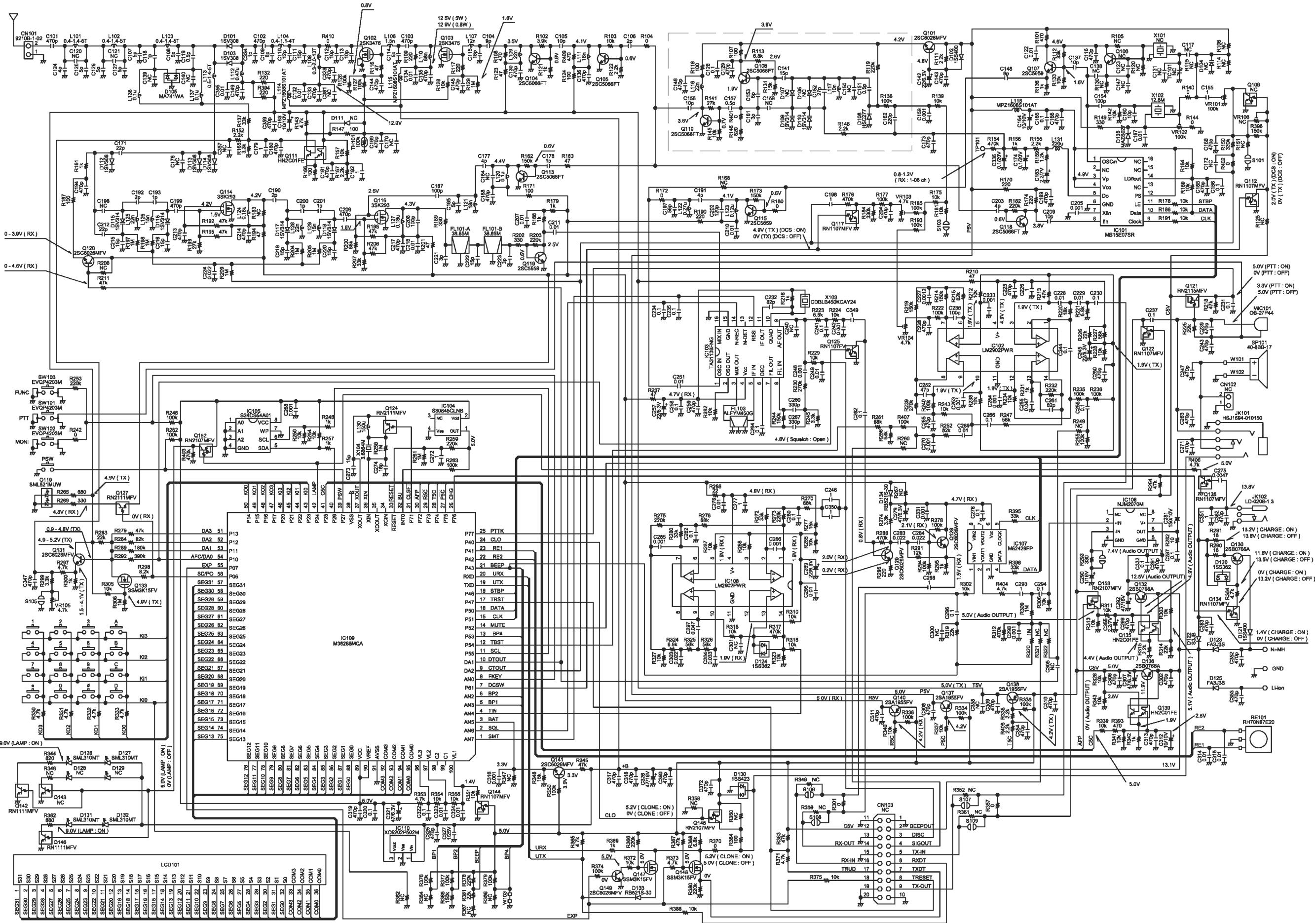
### MAIN SIDE A



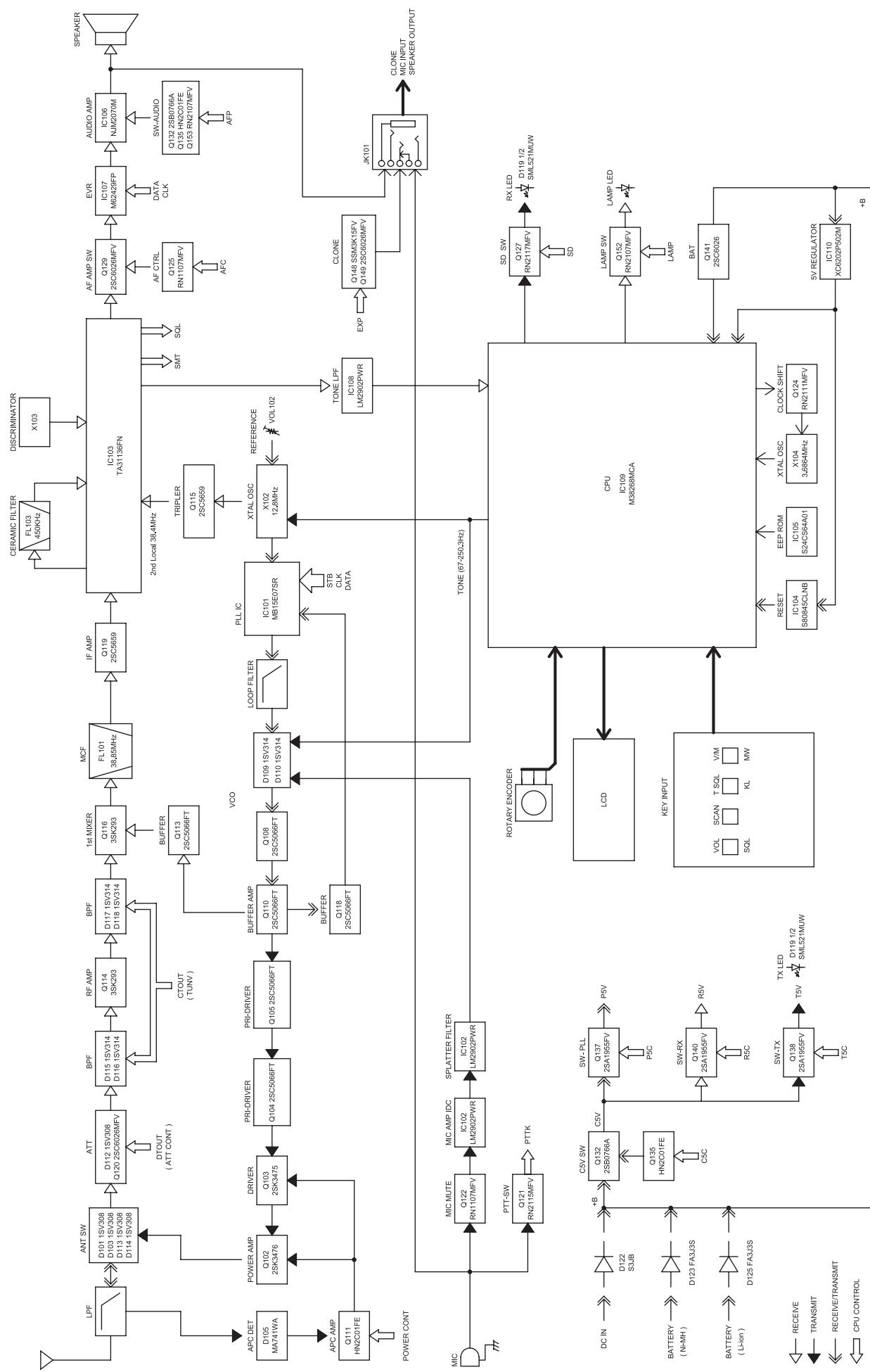
### MAIN SIDE B



# SCHEMATIC DIAGRAM



# BLOCK DIAGRAM



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