SOLID STATE DEVICES

Western Electric

HANDLING AND SELECTION GUIDE

SOLID STATE DEVICES

Handling and Selection Guide

EDITING COMMITTEE

Charles A. Bealer

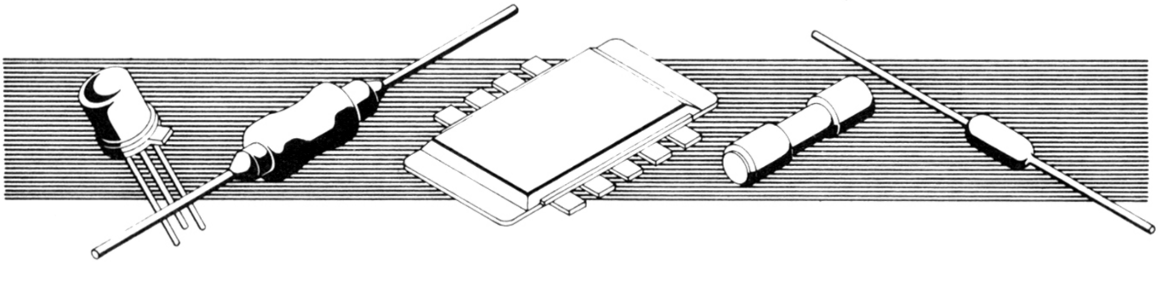
Allen R. Gerhard

John Krantz

John Mestishen

Richard L. Odenweller

Clem Tabor



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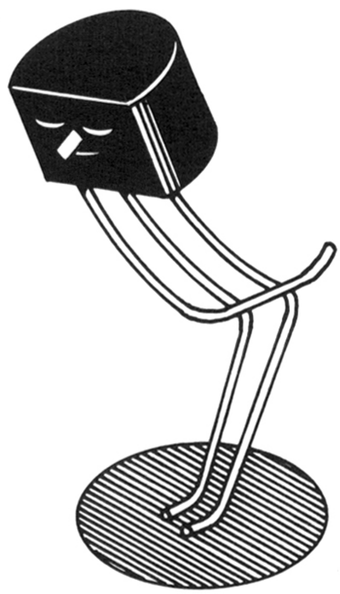

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Western Electric Company, Inc.
Bell System Printed Matter Organization
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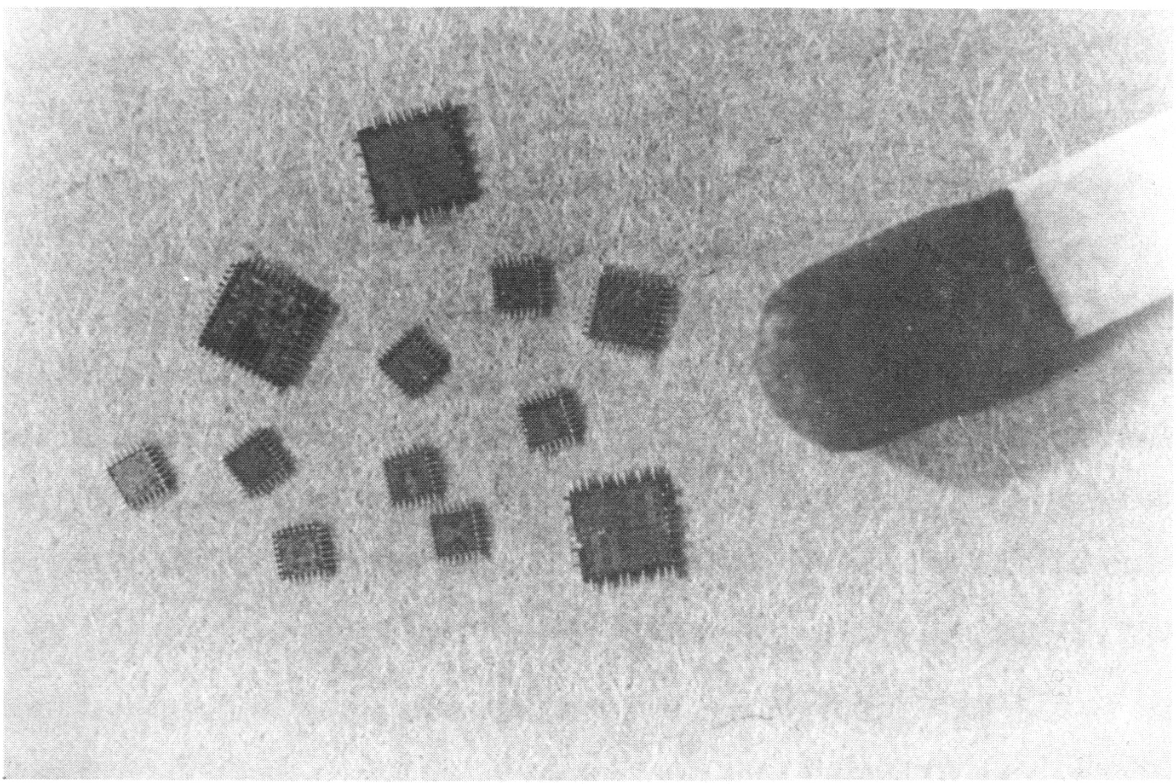
Introduction

The phenomenal success of the transistor, since it was announced by Bell Telephone Laboratories in 1948, and the ensuing development of microelectronic circuits has caused many changes in the electronics industry; large scale computers are an accepted part of our society, communications satellites form significant links in our communications systems, and the Picturephone® will supplement the telephone for personal communications. Many more of these tiny devices will be used as even more sophisticated communications systems are developed.



SOLID STATE DEVICES

The continued success of the telephone system will depend on having available semiconductors of high quality and good reliability at reasonable cost. The quality and reliability can be built into the devices during the manufacturing processes, but improper design or handling can negate all that the manufacturer does. The device user must, therefore, appreciate the sensitivity of these devices to electrical overloads and overheating or to mechanical abuse which could cause damage. Lack of such appreciation can lead to catastrophic failure of the devices or a slow degradation of their performance. In either case, there is the possibility of placing potentially defective devices into service and dooming a whole system to premature failure.

All of our present and future telephone systems are dependent on semiconductor devices and are expected to operate reliably for many decades. However, if only a few devices in a system should have a limited life because of improper manufacture, use, or assembly, the ultimate reliability of the total system is degraded. The primary purpose of this book is to help the device user protect the system reliability by explaining the proper handling and assembly procedures for semiconductor devices. The secondary purpose of this book is to provide the semiconductor device users with a better understanding of semiconductors and to serve as a source of information about common types in use in the Bell System.

The first section, a brief summary of the various device manufacturing techniques, points out that all semiconductors are not the same. The second and third sections are discussions of simple handling and testing precautions. The fourth section gives some insight into the more typical failure modes while the last section provides a quick source of information on the more common Bell System semiconductors.

Device Description

INTRODUCTION

After World War II, the Bell Telephone Laboratories at Murray Hill, New Jersey, applied considerable effort to the development of a solid state amplifying device using semiconductor materials such as germanium and silicon. It was known in the mid-forties that such materials possess mobile carriers of charge that move under the influence of an electric field resulting in a current. It was also known at this time that two different types of carriers were possible. For example, germanium and silicon atoms possess 4 electrons which could combine chemically (valence of 4). If some of their atoms were replaced by atoms that have a valence of 5 (for example, phosphorous or antimony), then the extra electrons would be loosely held in the crystal and be relatively free to move about. This forms the n-type crystal. If some atoms of the semiconductors were replaced by a valence 3 element such as aluminum or boron, then within the crystal structure, electrons would be missing. These are called holes which are easily filled by electrons from neighboring atoms. In the process of filling a hole, a new one is created. This is known as the p-type crystal. The process of adding controlled amounts of valence 3 or 5 elements to pure silicon or germanium is called "doping." Applying a voltage across a doped crystal causes movement of electrons or holes, producing an electric current.

Early experiments attempted to change the conductivity of a doped semiconductor by the action of a charged plate immediately above its surface. This is similar to the familiar electroscope or cat's fur experiments in elementary physics. It was hoped that a little power on the plate could control considerably more power by changing the conductivity of a semiconductor bar. The results with the charged plate were insignificant; but in trying to increase the effect of the field by using points instead of plates, a p-type region was created in the n-type material by the passage of current through a point containing valence 5 phosphorous, and the point contact transistor was born.

As a result of the experience gained from the point contact transistor and from a better understanding of junctions formed by n- and p-type regions, the junction transistor was developed two years later. Figure 1 shows the two junction-types which were developed at this time.

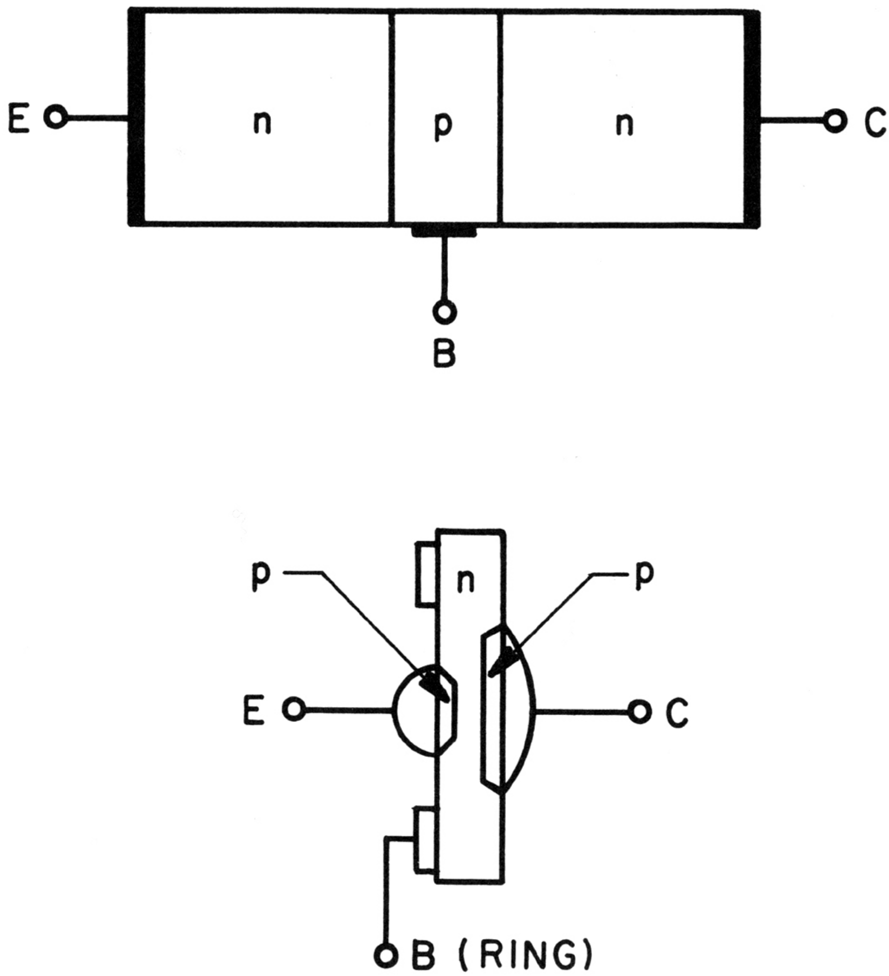


Figure 1

One type was grown by pulling a seed crystal out of a pool of molten semiconductor material which was alternately doped by n and p impurities. The other was alloyed by melting metal buttons on alternate sides of a wafer and doping the crystal in the resolidification process.

DEVICE DESCRIPTION

Although point contact transistors remained superior in frequency responses, these junction devices had definite advantages in that they were capable of handling larger power, were less noisy, were easier to handle in circuits, and had a more controllable manufacturing process.

Even though solid-state diodes have a much earlier history, going back before the turn of the century, the invention of the transistor led to a parallel improvement and development of the diode art. This naturally resulted from the intensive effort which went into the better understanding of device physics and materials and the development of fabrication techniques. Since the diode, with the exception of special types such as the tunnel diode, the gold bonded diode, the regulator diode, etc., is essentially a device possessing only two of the three regions of a transistor, it will not be treated as a separate device in this section.

The mid-fifties proved most important in the history of the transistor. In 1955, the diffusion technique was introduced in the junction transistor fabrication process, in which doped regions were formed by the application of heat in the presence of a gas or surface coating containing the proper impurities. These regions, which can be controlled to a depth of less than five millionths of an inch, then allowed for junction transistors to enter the 100 to 1000 megahertz range. The diffusion technique not only led to a breakthrough in the frequency response of junction transistors but also introduced a batch-type process which was to become the basis of modern transistor technology. Thus, thousands of transistor elements are handled simultaneously through most of the processing reducing greatly the need for individual operations. This also allows for greater uniformity in the product. Figure 2 shows a cutaway section of a diffused base mesa transistor element.

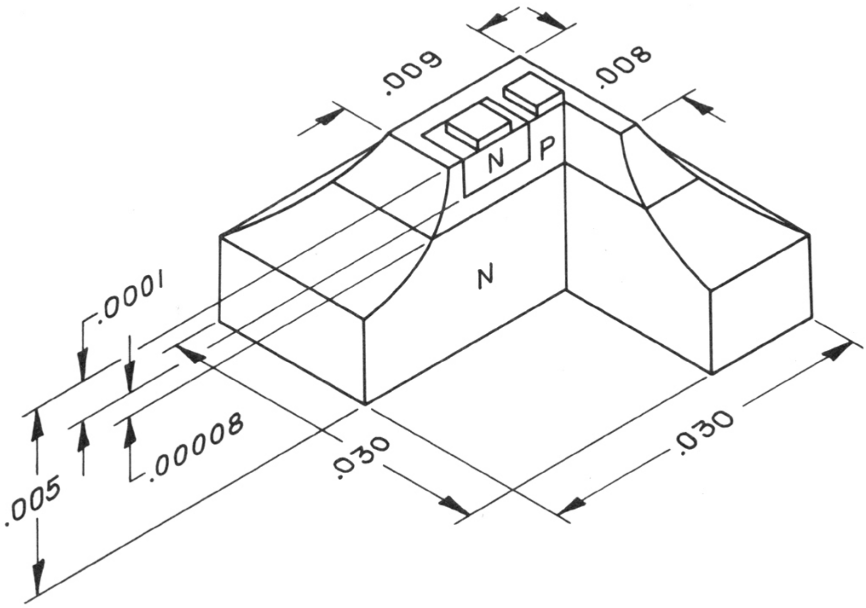


Figure 2

The next significant improvements took place at the end of the fifties with the introduction of the planar epitaxial transistor, in which the top surface is flat or planar, as shown in a cutaway representation in Figure 3. By growing the desired crystal on a heavily doped substrate, as shown by the n+ region, an improved device, particularly for switching applications, is formed. The new structure allows for many improvements, particularly higher voltages, while still retaining the desired low "on" voltage and switching times.

The planar technique, which eliminates the older mesa formation and provides protected junctions, also permits close control and reproducibility of junction regions through photographic techniques, so that hundreds of identical devices can be made on a slice with relative ease. As the planar process was improved, it became possible to drastically reduce the size of transistors and so increase their operating frequencies into the gigahertz range.

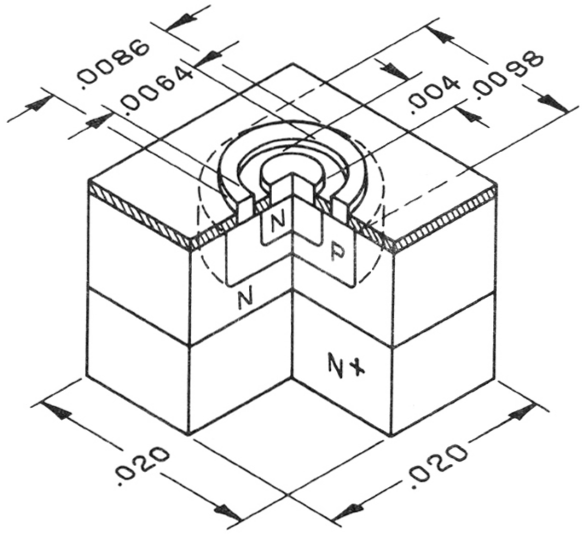


Figure 3

Components other than transistors can be made by the planar process--diodes, resistors, isolating junctions, and, to a limited degree, capacitors--all in the same semiconductor slice. It is not surprising, therefore, that the early sixties saw the development of the integrated circuit--a single chip containing active and passive components interconnected to form a complete functional linear or digital circuit. By the mid-sixties, new and improved processes made possible the sealed-junction beam-lead transistor (Figure 4) and integrated circuit (Figure 5) having smaller size, faster operating speeds, higher reliability, and lower cost than conventional devices. These chips can be bonded to ceramic substrates with other components to make complete systems and are available in separate Flatpack or Dual Inline Packages (DIP) as shown in Figure 6.

A new generation of Hybrid thin film Integrated Circuitry is beginning to see large usage in the Bell System. These HIC's consist of a ceramic or glass substrate on which thin film conductor patterns and, in some instances, resistors and capacitors have been generated, followed by the bonding of one or more beam-leaded

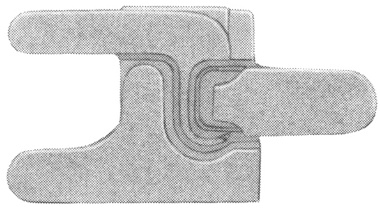


Figure 4

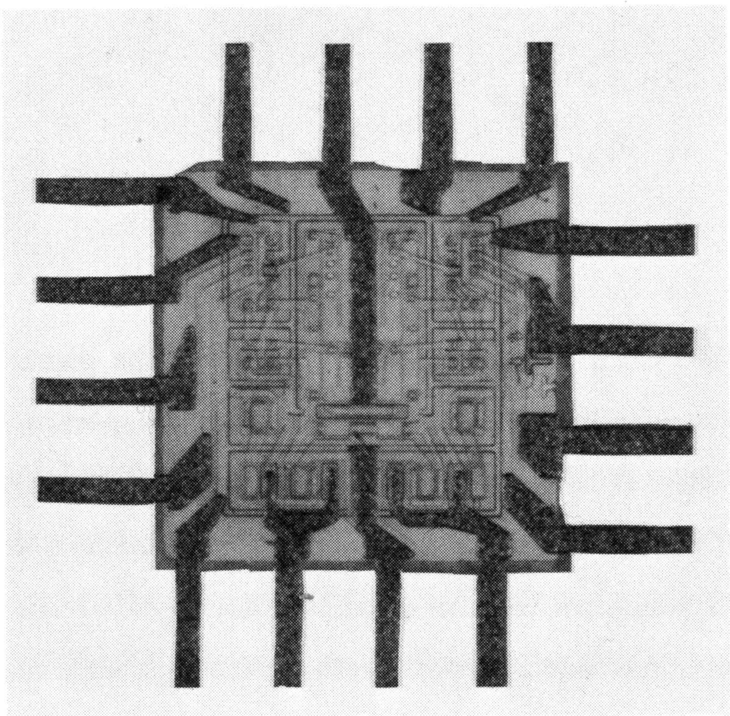
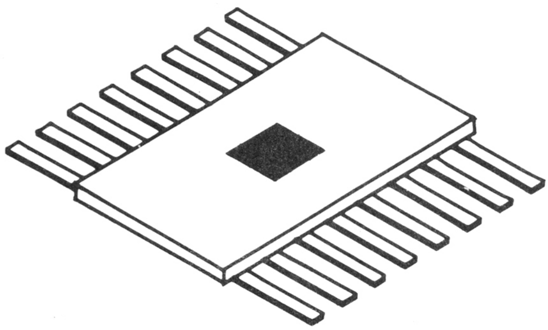
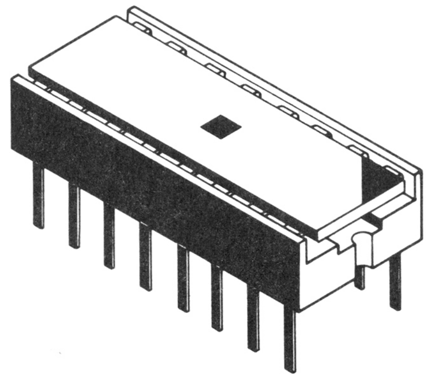


Figure 5

integrated circuits to the thin film conductors. As this new technology advances, such circuits are becoming more complex; a single substrate may now contain hundreds of narrow line-width conductors and more than 50 integrated circuit chips. This thin-film technology permits the inclusion of relatively high value resistors, none of which is now possible on the silicon chips. Because the processing of these circuits is dependent mainly on photolithographic batch techniques, they are highly reproducible and relatively low in cost.



FLATPACK



DIP

Figure 6

The following photos are examples of Hybrid Integrated Circuits. Figure 7 is an 810A PBX circuit containing 15 silicon chips, 10 tantalum resistors, and many conductors and crossovers on one substrate about 27 x 33-mm in size.

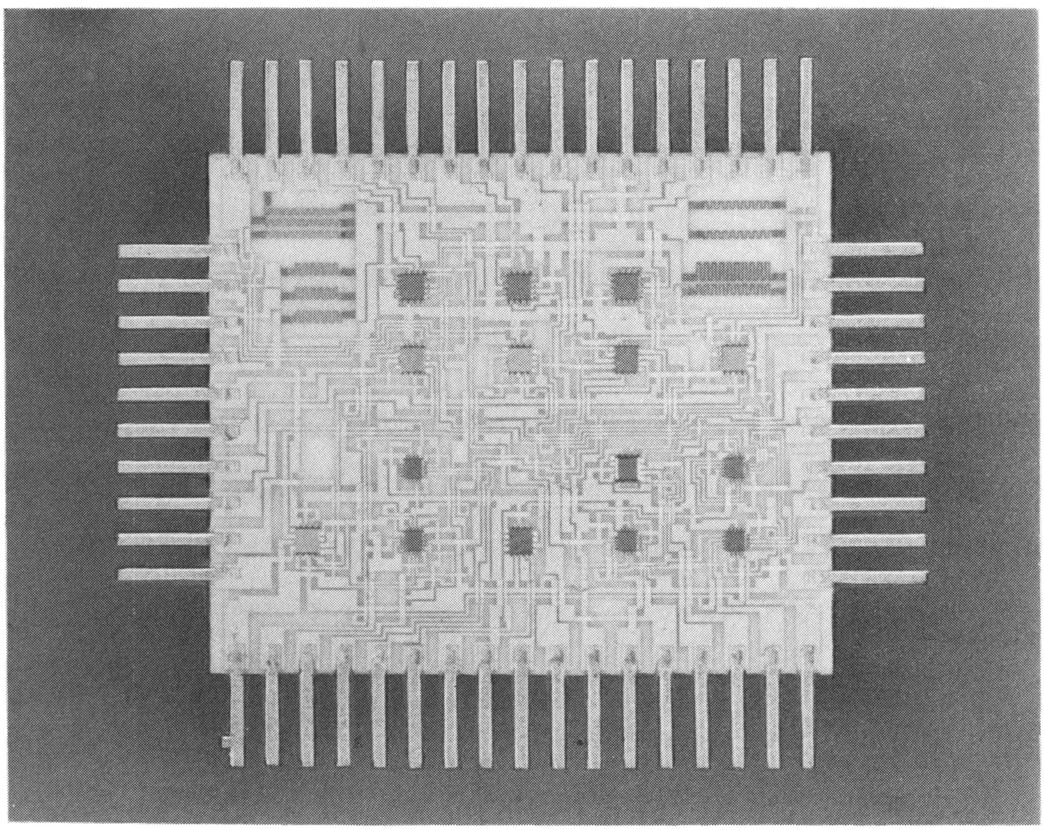


Figure 7

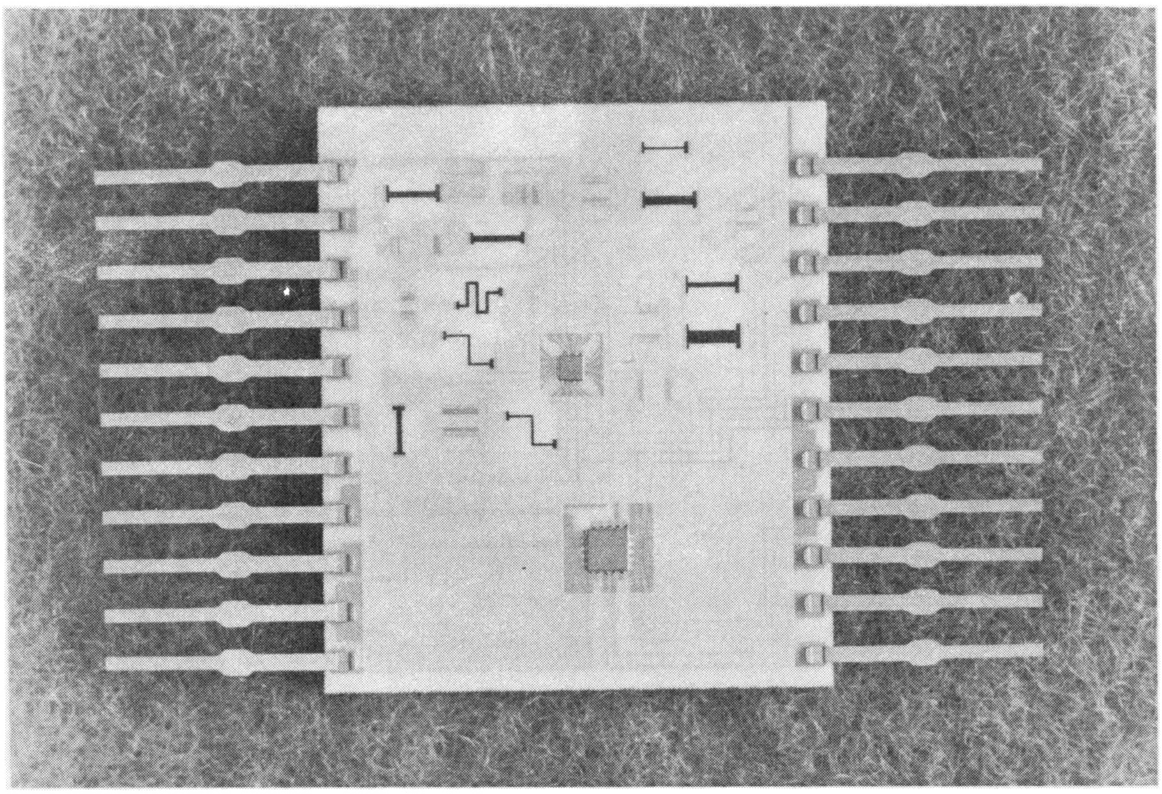


Figure 8

Figure 8 is the Video Processor Circuit for the Picturephone® and represents a circuit on which conductors, resistors, capacitors, and IC's all appear on a single ceramic substrate.

Figures 9 and 10 demonstrate the technique of placing capacitors on one substrate and the silicon chips and resistors on a second substrate attached above it. Figure 9 is the Touchtone® R-C Oscillator. Figure 10 is a circuit for the 208 Data Set.

Hybrid thin-film circuits, integrated circuits, and beam lead devices all have their place in the future. In some areas, a number of acceptable alternatives are possible. It is the mutual responsibility of the circuit designer and the device designer to understand the advantages and limitations of the various technologies and to make a choice based on the best interest of the Bell System.

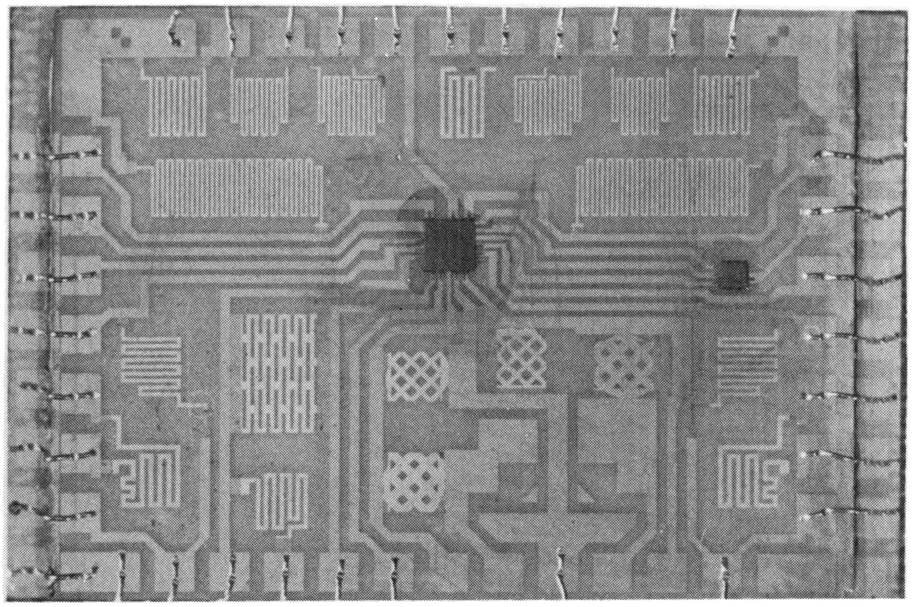


Figure 9

CHARACTERISTICS

The purpose of this section is to review, in general, the characteristics, ratings, and reliability which must be considered in selecting semiconductors for specific applications. Transistors and diodes, in general, would follow similar considerations and, therefore, diodes will not be treated separately.

In general, electronic circuits can be classified into switching or analog applications. A circuit is called upon to recognize the presence or absence of signals and transmit them at higher levels or recognize various levels and phases of signals and amplify them accordingly. Some applications such as high-level amplifiers, mixers, etc., could fall into both categories. The differences in the two circuit applications are reflected in the requirements of the transistors. Transistors are specified according to their ability to operate as a switch or as an amplifier. In switching applications, dc gain, "on" voltage, "off" voltage, input voltage, high-frequency response, and storage time play dominant roles. In amplifying applications, the high-frequency response, the power gain, power dissipation, input impedance, and noise figure contribute significantly.

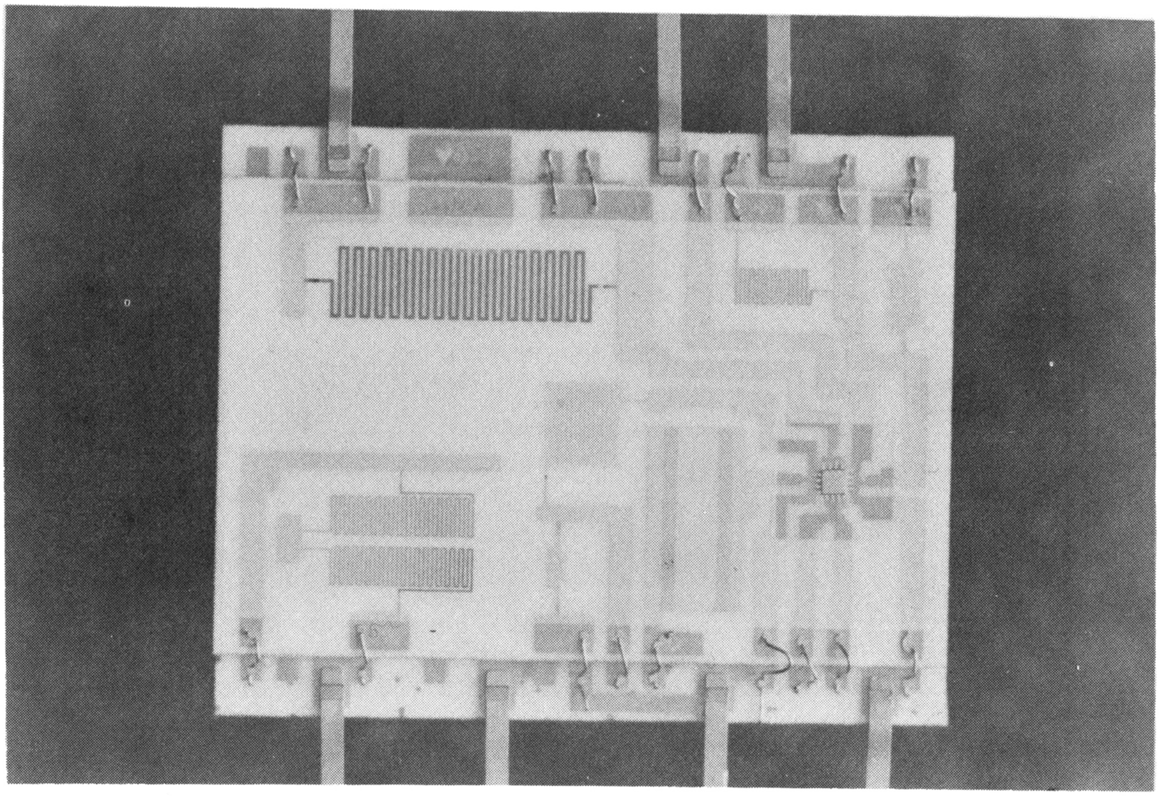


Figure 10

Since integrated circuits are complete circuits, the designer must consider other characteristics for proper selection. In logic applications, the logic type and function are of prime importance as are supply voltage, input and output loading (called fan-in and fan-out), power dissipation, propagation delay, and noise margin. Compatible logic families are available so that complete systems can be designed using the "building block" approach. Linear IC users must consider the circuit's function, supply voltage(s), gain, bandwidth, and impedances as well as special design characteristics. Obviously, the package type and its pin connections are important in any application.

SPECIFICATIONS AND DATA SHEETS

The objective of the specification is to assure that the product will satisfactorily function in the circuit. A single specification can guarantee performance, in many cases, in several circuits. The specification must not only assure operation at the beginning but also over the desired life of the equipment and over all necessary ambient conditions. Specifications are prepared for the use of manufacturing locations and data sheets for users. Data sheets supply characteristic curves and data that aid in the designing of circuits. The specification states manufacturing and testing requirements which control the quality of the product and provide the most economic balance of manufacturing and testing control to assure proper performance.

There is little doubt that the cost of manufacture and maintenance is of prime importance to every system designer. It is apparent that minimum costs will be achieved when the specification represents the optimum balance between system requirements, device design, and manufacturing skill. A weakness in any of the three areas can but add to the cost of the system. A mutual understanding between the three areas can greatly help in preventing unnecessary costs.

Some of the important considerations which follow a system from initial development to final manufacture and are necessary for optimum cost are the following:

a. Limit values on test specifications and data sheets must not only reflect temperature and aging variations but must also represent a balance between circuit complexity and performance and maximum device yield. Obviously, limits which are too tight increase costs by increased testing or reduced device yields, while excessively loose limits increase costs by reduced circuit efficiencies.

b. Device designs should reflect the latest achievable in electrical performance, reliability, and manufacturability. This can best be obtained by maintaining the areas of design and manufacture at the highest technical level possible and by a constant interchange of information and ideas on new and important product developments and system requirements.

RATINGS AND RELIABILITY

A rating is, by definition, a limit value for a device which, if exceeded, will impair the expected life of the device. In some cases, the failure can be catastrophic and take place immediately. This generally happens when voltage ratings are exceeded. In other cases, the increased degradation will not be immediately apparent but eventually will result in a higher failure rate. This usually results when junction temperature ratings are exceeded.

Therefore, precautions should be taken in every application to avoid excessive junction temperatures—including, if necessary, use of a suitable heat sink. (See discussion of heat sinks under Handling.)

Handling

The discrete solid state device so prevalent in electronic equipment of the 60's is gradually being supplanted by the microelectronic circuit of the 70's. As production techniques improve, devices such as beam-leaded transistors, field effect transistors, and integrated circuits are gaining much wider acceptance. Because of their minuteness and susceptibility to damage, it is essential that they are handled properly when installed in electronic assemblies. It is the purpose of this section to indicate the proper handling techniques for the assembly or replacement of various solid state devices in electronic equipment. Figure 11 illustrates the minuteness of a typical integrated circuit.

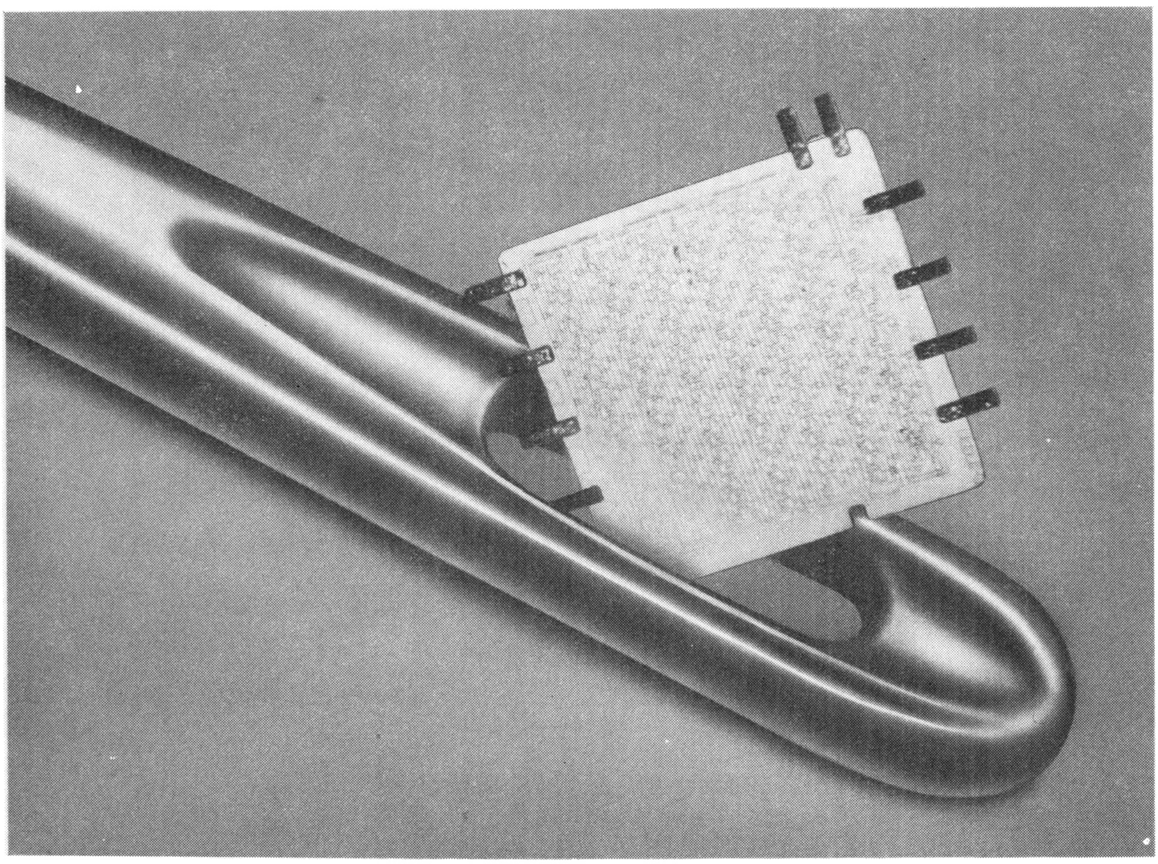


Figure 11

STORAGE

Solid state devices should be stored in the shipping containers whenever possible. These containers (Figure 12) are specially designed to protect the devices.

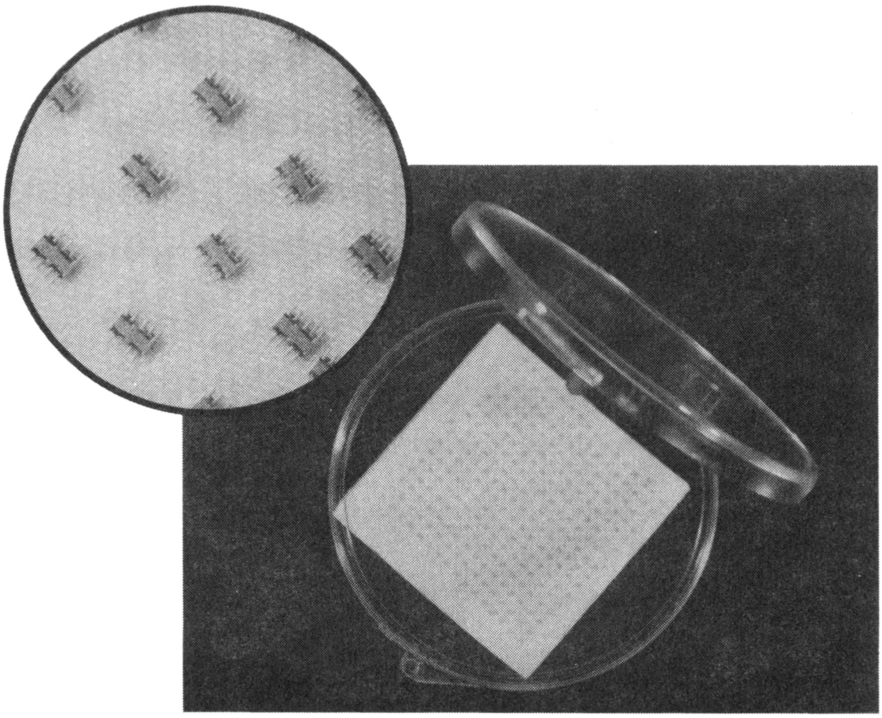
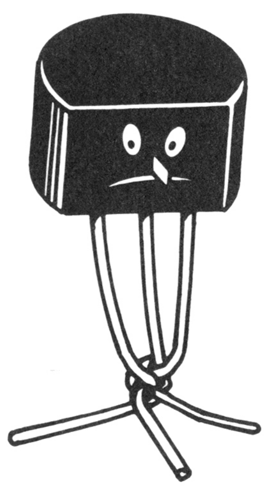


Figure 12

Avoid dumping devices from their containers. Physical shock may result in electrical or mechanical degradation.



HANDLING

Beam-leaded transistors and integrated circuits are often shipped in the "chip" form and are extremely susceptible to mechanical damage due to the multiplicity of components and fragile leads. When devices are shipped with mounting hardware, store it with the devices to insure its intended use. In general, all devices should be used on a "first in - first out" basis. Prolonged storage may cause oxides to form on the leads, necessitating special cleaning.

PACKING AND UNPACKING

Semiconductor devices may be received packaged in a number of ways depending on the device requirements, insertion requirements, or quantity ordered. To insure proper packing, the devices should be ordered by specifying standard multiple packaging where possible. For interworks locations employing automatic insertion equipment, lead tapes, plastic carriers, etc., may be available. For further information, contact the product engineer at the producer location.

When beam leaded transistors and integrated circuits are shipped in the "chip" form, the following packaging is presently employed:

a. They are shipped in plastic containers with the chips arranged on 100 mil centers in groups of 100 to 400 on glass disks.

b. The chips are imbedded on silicone resin applied to one side of the glass disk with a polyester pad as the compliant member to maintain device orientation. Note: The active side is down on the silicone.

c. Always open the plastic container from the top with the polyester pad up.

d. When using a vacuum pencil pickup, keep the pencil as vertical to the device as possible to prevent lead damage. Use as large a pencil pickup as possible to insure equal force distribution.

A promising approach for "chip" handling is presently under development where chips would be shipped in spool tapes for compliant bonding.

MECHANICAL DAMAGE

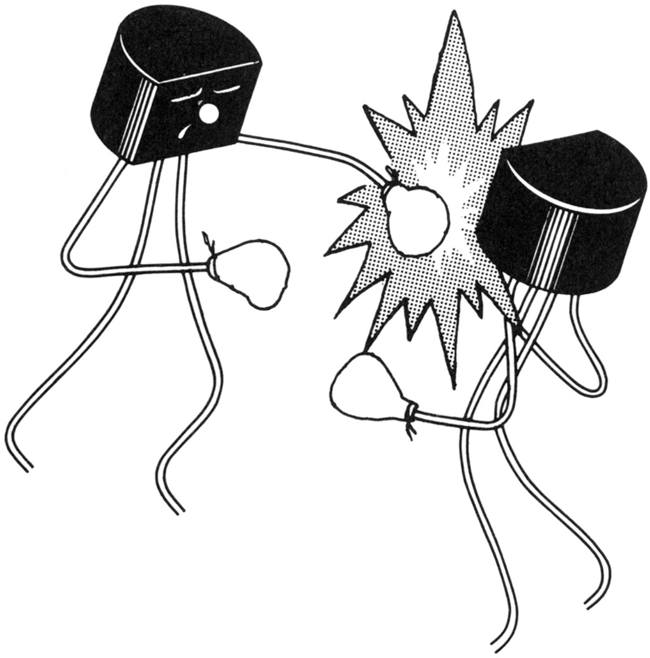
Semiconductor devices must be handled with care if the built-in reliability is to be assured. Rough handling may cause cracks in the seal, damage to the internal wafer, or opening of small wire bonds. Although these faults may not be immediately apparent, they may degrade the devices life expectancy. If mechanical damage such as cracks, dents, or scratches in the can or seal (metal encapsulated transistors with glass seals) is noted, it is recommended that the device not be used. In case of integrated circuits and beam-leaded transistors, the active side is coated with RTV rubber, but this affords little protection from mechanical damage. The slightest scratching of this area may easily destroy the device. In addition, only 20 grams of pressure can crack the chip.

In general, discrete solid-state devices are capable of withstanding shocks of the order of 2000g. Plastic encapsulated transistors are capable of withstanding even greater shocks due to the complete enclosure of the active area with plastic. Exposure of discrete devices to any single jolt or jar may not result in an immediate failure, but shocks in general should be avoided.

Microwave point contact diodes, alloy transistors, integrated circuits, thin-film circuits, and beam-leaded transistors are the most susceptible to shock due to their internal construction.

LEADS

Many discrete semiconductor devices employ a glass-to-metal seal. The leads of these devices are made with material such as Kovar and Rodar to match the thermal



expansion of glass. The following precautions should be observed when handling the leads of such devices:

a. Keep the number of bends to a minimum to assure the soundness of the seal. Forcing leads into alignment with terminals or posts, by twisting or pulling, may damage the seal.

b. All bends should be made not closer than 1/16 of an inch from the surface of the glass seal or, in the case of plastic encapsulated devices, from the body of the device. The flat leads of plastic transistors may be bent at 90° angles without any lead deterioration.

c. Handling of leads should be kept to a minimum, as residues from body oils are likely to cause soldering difficulties.

d. Improper cutting of semiconductor leads (such as with diagonal pliers), can result in a mechanical shock which may travel through the lead into the device and degrade its electrical properties. A shearing tool should be used to minimize the possibility of shock damage.

e. The wirewrapping of semiconductor device leads requires special consideration because of the residual tension and stress-corrosion effects which may develop. This is especially true of gold-plated Kovar or Rodar leaded devices.

f. The use of percussion welding is generally not recommended for semiconductor devices, because of the likelihood of damage due to the high currents generated. Resistance welding may be acceptable, provided care is taken to insure that no destructive transients are introduced into the devices. This is especially applicable to devices which usually have one element connected to the case. Low power devices, such as ultrahigh frequency and NPN alloy transistors, are especially susceptible.

Integrated circuits and beam-leaded transistors (of the chip form) are usually thermocompression bonded onto substrates. The leads being bonded in this process can be as small as 1 mil wide and 1/2 mil thick. Vacuum pickups are usually used for transfer of the chip during this process and could easily damage the leads if not carefully aligned.

HEAT SINKS

Heat sinks are classified under two types:

1. The temporary type (Figure 13) is used in soldering to prevent the introduction of excessive heat to the semiconductor device.

2. The permanent type (Figure 14) is installed with the device to allow a greater dissipation of heat generated within the device itself. This can be either a radiator fin-type, which surrounds and is part of the device, or the external type which is mounted to the stud of the device during circuit assembly. The temporary type will be discussed in the following section on Soldering.

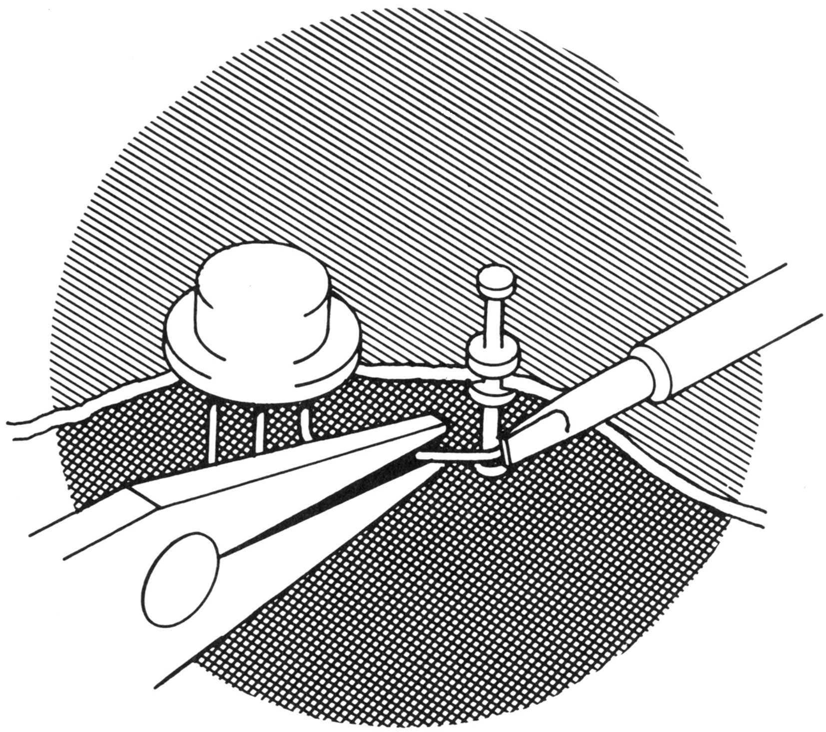


Figure 13

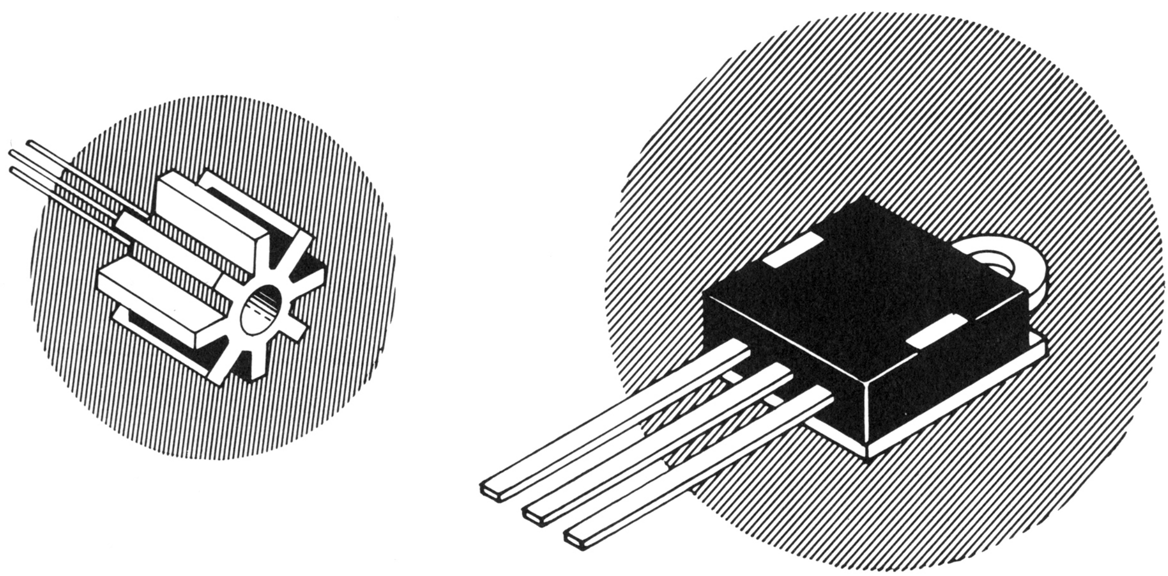


Figure 14

From the electrical standpoint, permanent type heat sinks are used to reduce junction temperature for increased power dissipation capability and reliability. The ability of a semiconductor device to dissipate its rated power is dependent upon: (1) internal thermal resistance of the device itself; and (2) external factors, such as the size of the heat sink, the thermal resistance between the heat sink and the device, the degree of ambient circulation, and the temperature of the ambient. Device data sheets often contain information concerning these external factors.

The bearing surface upon which a stud-mounted semiconductor device is installed must be flat, clean, and free of burrs. This is necessary to insure adequate contact between the heat sink and the device in order to obtain proper heat flow. Thermal contact is improved with a very thin film of silicone compound between the clamped surfaces. Care should be used to insure the torque recommended in the data sheets. When electrical isolation is required between the device and an external heat sink, a thin mica or other suitable washer, coated with silicone compound, can be used between the two. Care must be taken not to damage the insulating washer.

SOLDERING

A soldering iron, properly connected and grounded, may still have leakage voltages present on its tip in excess of 1 volt above ground. This voltage can cause damage, particularly to ultrahigh frequency transistors which have emitter-to-base breakdown voltages in the range of 1 volt. With such devices, it is desirable to use a working surface isolated from ground. Some soldering guns, even when adequately grounded, produce transient voltages each time the power is turned on or off. These are caused by the inductive reactance in the tool and ground lead.

Wave and dip soldering have an advantage over hand soldering because the entire circuit board is maintained at the electrical potential of the molten solder. Thus, destructive transients are not introduced into the devices. Care must be exercised to insure that solder bath temperatures are uniform, that the duration of immersion is timed properly, and that the devices are not immersed closer than 1/16 inch from the glass-to-metal seal. In the case of thin-film circuits, time and temperature must be properly controlled to prevent damage to previously soldered connections. Failure to follow these precautions can result in small changes in electrical characteristics which are not easily detected but which may cause failure of the device. The length of time a semiconductor device may safely remain in the molten solder is dependent upon the type (whether alloy or diffused), the temperature of the bath, and the distance heat must flow to reach the critical areas of the device.

Following are some additional recommended practices to use when soldering solid state devices:

1. Higher solder bath temperatures for a shorter time are preferred for better solder-wetting of the leads and to prevent long heat exposure from affecting the critical areas of the device.

2. Corrosive fluxes must not be used to facilitate soldering.

3. Diffused type devices can withstand higher temperatures for longer periods of time than can alloyed types which use lower temperatures in processing. As an example, diffused transistors can withstand a 575°F bath for a period of 1 minute when immersed to not more than 1/16 of an inch from the seal. The germanium alloy transistor can withstand a maximum of 460°F for a period of 30 seconds. In hand soldering, somewhat higher iron tip temperatures can be used if only one lead is heated at a time. For example, with the germanium transistor, the temperature of the iron tip should not exceed 930°F at a minimum distance of 1/16 inch away from the seal for a short duration.

4. Resoldering of thin-film circuits should be avoided since local stresses may be developed, resulting in cracked substrates.

5. Any soldering information which may be included in the device data sheets should be followed.

STATIC CHARGES AND TRANSIENTS

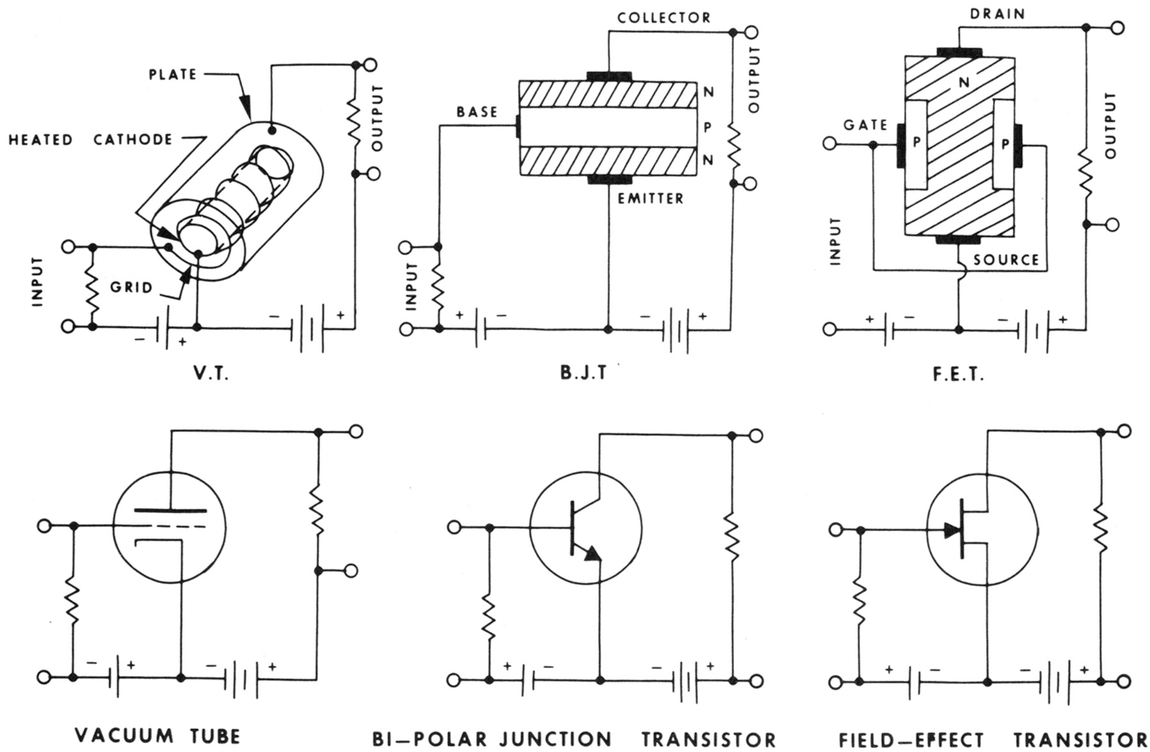
A static charge of several thousand volts can easily build up on your body from simply walking about on a nonconductive floor or moving around in a chair. This is particularly true in low humidity and when clothing made of wool or certain synthetic fibers, such as nylon, is worn. Ordinarily, this static charge may be high enough to send a damaging pulse through a semiconductor device when it is touched. Therefore, it is always good practice before handling semiconductor devices to be sure to ground static charges by touching some grounded metal object, such as the metal workbench. In extreme cases, sensitive devices may require handling in a completely shorted condition, and operators may require special grounding facilities.

Electric tools, such as screwdrivers and wirewrappers, are frequently used in the assembly of circuit boards containing semiconductor devices. Some devices can be damaged by transients generated by these tools. Air-operated tools are recommended for working on circuits subject to transient damage.

Electrical Testing

The long established procedures and equipment for testing electron tube circuits do not directly apply to circuits using semiconductor devices. This is true because parameters are greatly dependent on temperature and strict limits exist on the upper values of applied voltage. If voltage limits are exceeded, an abrupt change in impedance may take place which usually results in damage unless the circuits are designed to limit the current.

DEVICE ANALOGY — AMPLIFIERS



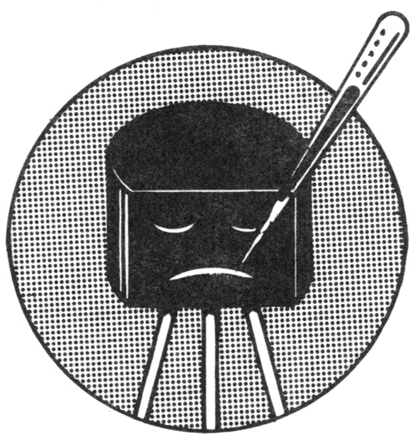
CIRCUIT TESTING

Performance tests on completed circuits must be made in such a way that ratings will not be exceeded for even very short periods of time. Exceeding these ratings may cause a sudden permanent change of characteristics or may start a long slow change resulting in eventual circuit failure.

Transient energy in the form of voltage spikes or current surges may be generated when sudden changes occur, such as turning a circuit on or off. Similar effects are produced by momentary shorts in live circuits or connection of a low-impedance probe for troubleshooting. These undesirable transients may exceed the maximum ratings of devices in the circuit and cause damage. Caution should be used to prevent or minimize their occurrence.

It is good practice to turn off the power when connecting or removing circuit boards from a test set. In some cases, it may be necessary to short the test set connector terminals in order to discharge the energy stored in wiring and other capacitance in the test set, even though all power supplies are disconnected.

After all necessary connections are made and test set connector short circuits removed, test voltages can be applied in a particular sequence. The Bell Labs circuit design engineer can provide this sequence.



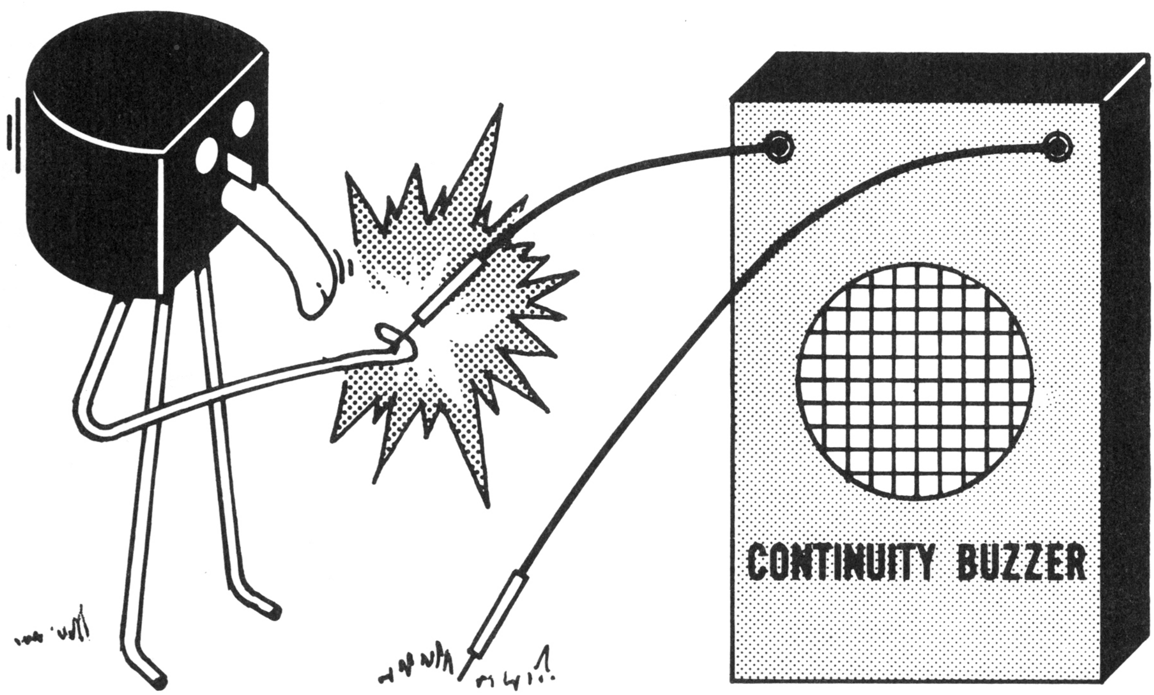
Consideration must be given to ambient temperature when testing solid state circuits, since some semiconductor device parameters can undergo a 2-to-1 change when the temperature is changed as little as 10°C.

Following the operating tests, all voltages should be returned to zero in a proper sequence. In the special case mentioned previously, the test set terminals must be shorted before the circuit under test is removed.

CIRCUIT TROUBLESHOOTING

When it is necessary to troubleshoot and repair an assembled circuit which does not operate properly, many approaches can be taken. It is not within the scope of this book to define methods of locating defects, but rather to offer precautionary suggestions which may apply.

"Buzzers" of the electromechanical type, often used as continuity testers, are prolific generators of high-energy transients. Destructive transients may be developed, even though the buzzer battery voltage is much lower than the normal voltage applied to the circuit under test. For this reason, such "buzzers" should never be used when troubleshooting circuits containing semiconductor devices.



Wiring continuity tests can be made safely by use of a selected ohmmeter or electronic buzzer, that is, one that does not exceed the current or voltage ratings of the devices in the circuits being tested.

Several good ohmmeters are available commercially which meet the "low power" requirements for testing solid state devices. A special "buzzer" developed at Western Electric, Omaha, is an excellent unit for continuity testing of circuits containing semiconductor devices. The Omaha "buzzer" (SID-321297) has a maximum short circuit current of 1 milliampere, a maximum open circuit voltage of 0.5 volts, and delivers a maximum of 0.25 milliwatts of power to the device under test.

It is always good practice to remove all power to a circuit when an ohmmeter is used. Even though power is removed, transients can result from connecting or disconnecting an ohmmeter across a transformer winding or other inductive element. Damage to a semiconductor device in an adjacent circuit may result.

Troubleshooting by bias measurement or signal tracing is, of necessity, performed with power on. Connecting or disconnecting test probes may cause damage to a semiconductor device by transients because of the effects of their low impedance or high input capacitance. Probe input capacitances may become charged at one point in the live circuit and then, at the next point of application, discharge destructive energy through a semiconductor device. The practice of using high impedance probes and, if necessary, shorting between readings will eliminate this problem.

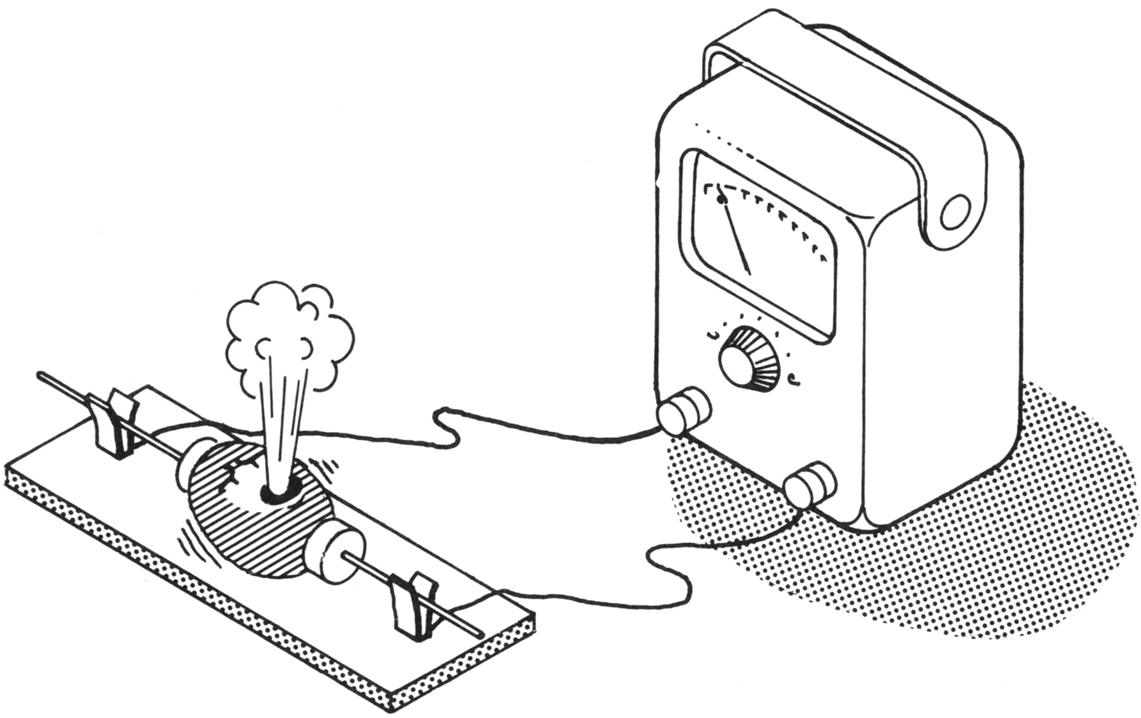
Improper grounding may cause leakage currents from ac-line-operated test equipment, which will result in damage to devices in the circuit under test.

High-voltage static charges which build up on clothing, particularly in low-humidity environments, can be injurious to some low-power semiconductor devices if discharged through them. This can be easily avoided by touching a grounded metal object before handling a semiconductor circuit. Use of conductive flooring and the wearing of suitable clothing and shoes may also be employed to prevent the buildup of static charges.

DEVICE TESTING

Transistors, diodes, and integrated circuits can be tested as individual units by removal from the system or while wired into a circuit. Precautions should be followed to avoid exceeding the device ratings as described in the sections on Circuit Testing and Troubleshooting.

Several general purpose semiconductor device testers are available commercially which will measure several of the functional parameters. Tests of dc parameters such as leakage current, breakdown voltage, and current gain (of transistors) will indicate the normal type of failures such as opens, shorts, or appreciable degradation since it was thoroughly tested by the manufacturer.

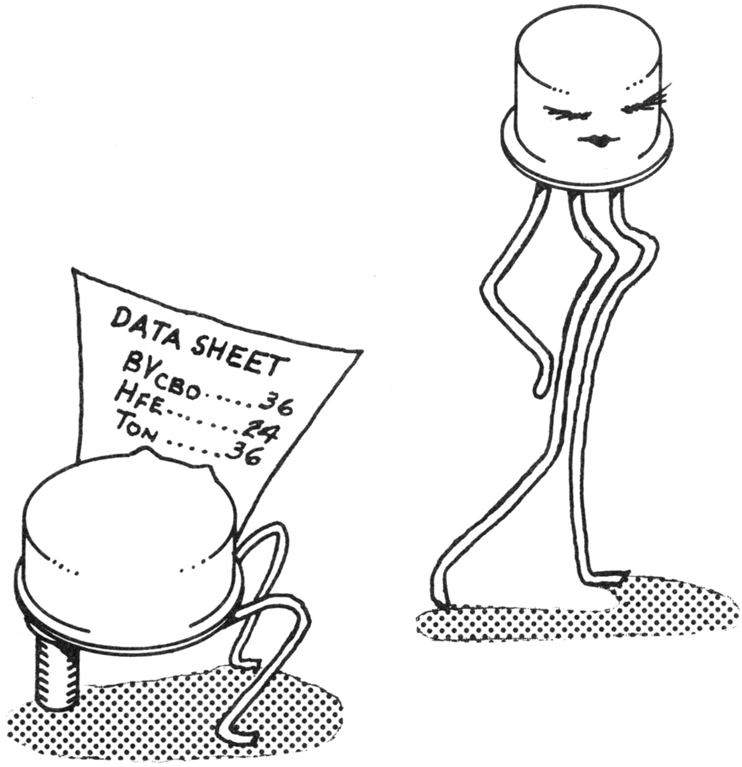


In some instances, an ohmmeter may be used to indicate opens or shorts. Any tester selected should be checked by the user to assure that it does not apply voltages or currents exceeding the ratings of the device being tested.

A common method of making a quick check of a semiconductor device or thin-film circuit believed to be dynamically defective is to insert it into a circuit or system known to be in working order. All power to the circuit should be removed before inserting the "doubtful" device to reduce transients. In some circuits, it may also be necessary to discharge circuit capacitances in order to eliminate harmful transients before inserting devices. A device known to be good should never be placed into a defective circuit since the device itself may become damaged. Units suspected of dynamic failure should be brought to the attention of the device manufacturer.

When testing a semiconductor wired into a circuit, refer to the precautions listed for Circuit Testing and Troubleshooting. There are several commercial "in-circuit" testers available which can make limited checks without removing a device soldered into the circuit.

Some device parameters are extremely dependent upon the temperature or bias conditions. Leakage currents may double when the temperature is increased about 10°C. Transistor current gain (common emitter) may vary more than 2-to-1, as the emitter current is varied within the ratings of the device. Consult the device data sheets for proper temperature and bias conditions when testing to specification limits.


DATA SHEET
BVCBO.....36
HFE.......24
TON.....36

Device Failures

INTRODUCTION

The reliability of a complex electronic system is completely dependent on the combined reliability of its component parts. A semiconductor device's intrinsic reliability is obtained through good design, careful processing, and manufacturing controls. If the reliability is to be maintained, the encapsulation or package must keep the environment of the active element constant with time.

The user can appreciably lower the intrinsic reliability of semiconductor devices through excessive exposure to thermal, electrical, or mechanical stresses. Disastrous results can be caused by test set transients, improper switching sequences, inductive surges, power line leakage currents, static discharges, capacitance discharges, and troubleshooting equipment and techniques by overloading the device junction for a brief instant. The effect of energy dissipated in a small volume is a rapid temperature rise (a hot spot) which destroys the junction causing an electrical short circuit. On occasion, the very fine connecting wires in a device package are vaporized causing an open circuit.

The integrity of the package seal may be degraded by shock or stress due to mishandling. A lead bent too close to a very thin metal-to-glass seal, or shock transmitted by lead clipping or pulling, may initiate a slow leak and allow the environment of the active element to change with time.

CAUSES OF FAILURES

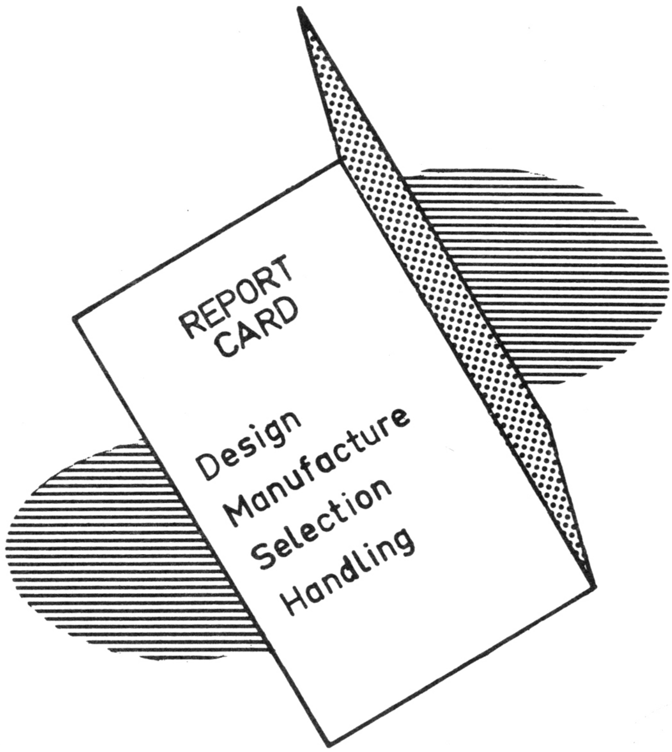
The causes of failures may, in general, be classified into four categories:

1. Device Design — Failure to meet reliability design objectives.

2. Device Manufacture — Improper device manufacturing techniques and workmanship.

3. System Design — Incompatibility between device selection and equipment specification.

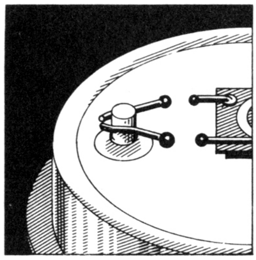
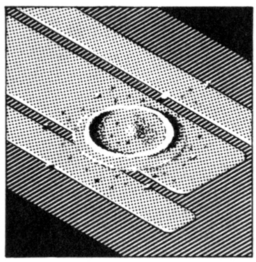
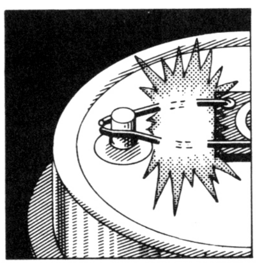
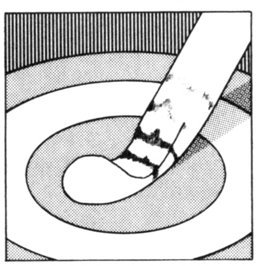
4. System Manufacturer or User — Improper techniques in handling and assembling of devices into circuits and systems.



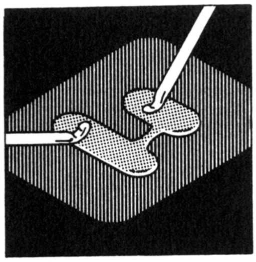
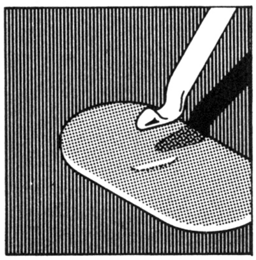
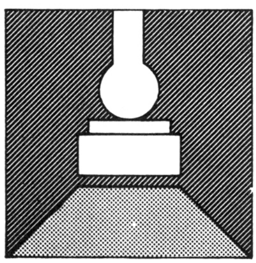
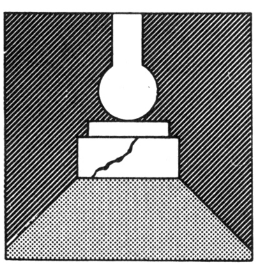
It is important to recognize the symptoms and understand the causes of failure so as to assign the failure to the proper category. When it becomes apparent that excessive numbers of failures are occurring either at the system manufacture or user area, careful analysis will allow corrective action to be taken in the shortest possible time. Experience has shown that during the early system testing period of a new device, most failures result from mishandling and improper testing.

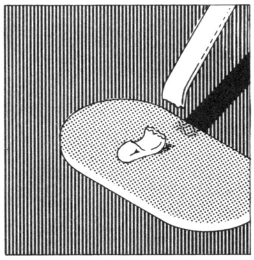
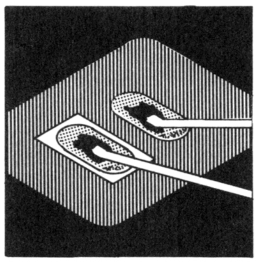
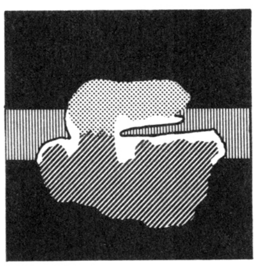
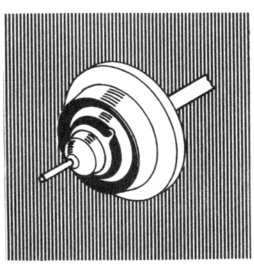
FAILURE CLASSIFICATION

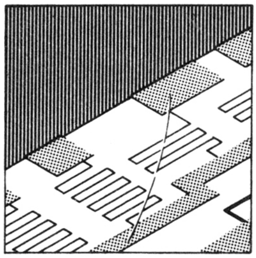
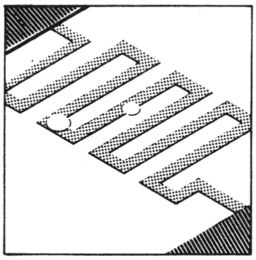
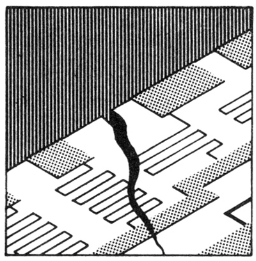
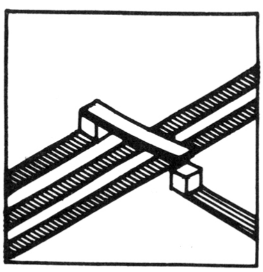
The low unit cost of most semiconductors does not justify establishment of a failure analysis engineering staff at the system manufacturing or user areas for analysis of failures. The procedures of C.I. 70.102-22 and C.I. 70.105-22 are quite adequate. However, when a new system is being developed or during its initial trials, it may be possible to expedite correction of failure problems if a responsible system engineer can do some failure analysis work. With this purpose in mind, the following chart of possible symptoms and causes of semiconductor device failures is provided. (The symptoms are shown for particular geometries; however, they apply equally well to all the various geometries used for solid state devices.)

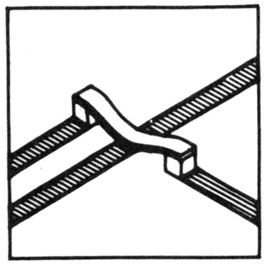
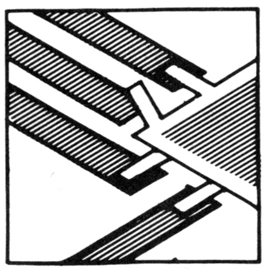
SYMPTONS		POSSIBLE CAUSE OF FAILURE
Balls on ends of open wires		Excessive current or voltage
Fused spot on wafer		Excessive current or voltage
Vaporized wire		Excessive current or voltage
Discoloration of wire or wafer and device shorted		Excessive current or voltage

DEVICE FAILURES

SYMPTOMS		POSSIBLE CAUSES OF FAILURE
Fused streak across wafer or spike between stripes		High voltage or static discharge
Wire lifted from stripe		Poor wire bond — Excessive mechanical shock
Wafer off header or melted wafer bond.		Poor wafer bond — Excessive mechanical shock or overheating
Cracked wafer		Severe shock

SYMPTOMS		POSSIBLE CAUSES OF FAILURE
Fractured wire at bond or weld		Poor bond or weld — Excessive vibration
Fractured end of wire at A1 stripe. Purple color present near wire		Migration of gold from wire to A1 stripe
No observable defect, but device is shorted internally		Static discharge, high voltage pulse, contamination, or overheating
Particle or thread-like foreign material across junction area		Physical defects due to poor assembly practices

SYMPTOMS		POSSIBLE CAUSES OF FAILURE
Open or high resistance		Scratch due to rough handling
Open or high resistance		"Pinhole" due to manufacturing defect
Open or high resistance. Broken substrate		Cracked substrate due to shock
Open circuit		Crossover beam detached or missing

SYMPTOMS		POSSIBLE CAUSE OF FAILURE
"Short" circuit		Crossover beam touching conductor
Inoperative circuit		IC lead bond open

Device Characteristics

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Code	Title	Page	Code	Title	Page
1A	Digital IC	72	9D	Transistor	51
1B	Digital IC	72	9E	Transistor	51
1C	Digital IC	72	15A	Transistor	53
1E	Digital IC	68	15B	Transistor	53
1F	Digital IC	68	15C	Transistor	53
1J	Digital IC	66	15D	Transistor	53
1K	Digital IC	66	20J	Transistor	49
1L	Digital IC	66	20K	Transistor	49
1M	Digital IC	66	20L	Transistor	49
1N	Digital IC	66	20M	Transistor	49
1P	Digital IC	66	20N	Transistor	49
1R	Digital IC	66	20P	Transistor	49
1S	Digital IC	66	20R	Transistor	49
1T	Linear IC	76	22B	Transistor	49
1U	Linear IC	76	22D	Transistor	49
1W	Digital IC	66	23B	Transistor	49
1Y	Digital IC	66	24C	Transistor	49
1AA	Digital IC	68	24D	Transistor	49
1AB	Digital IC	68	26A	Transistor	53
1AC	Digital IC	68	26B	Transistor	53
1AD	Digital IC	68	27A	PNPN Device	51
1AE	Digital IC	68	27B	PNPN Device	51
1AF	Digital IC	68	27C	PNPN Device	51
1AG	Digital IC	68	27D	PNPN Device	51
1AH	Linear IC	75	27E	PNPN Device	51
1AJ	Digital IC	68	27F	PNPN Device	51
1AK	Digital IC	68	27G	PNPN Device	51
1AL	Digital IC	68	27H	PNPN Device	51
1AM	Digital IC	68	34A	PNPN Device	51
1AN	Digital IC	68	34B	PNPN Device	51
1AP	Digital IC	68	34C	PNPN Device	51
1AR	Digital IC	68	36A	Linear IC	78
1AS	Digital IC	68	41A	Linear IC	76
1AT	Digital IC	68	41B	Linear IC	76
9A	Transistor	51	41C	Linear IC	76
9B	Transistor	51	41D	Linear IC	78

SOLID STATE DEVICES

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41E	Linear IC	76	41CP	Digital IC	66
41K	Linear IC	75	44A	Transistor	50
41N	Digital IC	70	44B	Transistor	50
41P	Digital IC	70	44C	Transistor	50
41R	Digital IC	70	44D	Transistor	50
41S	Digital IC	70	44E	Transistor	50
41T	Digital IC	70	44F	Transistor	50
41U	Digital IC	72	44G	Transistor	50
41W	Digital IC	72	45A	Linear IC	77
41Y	Digital IC	72	45A	Transistor	50
41AA	Digital IC	72	45B	Transistor	50
41AB	Digital IC	72	45C	Transistor	50
41AC	Digital IC	70	45D	Transistor	50
41AD	Digital IC	72	45E	Transistor	50
41AE	Digital IC	72	45F	Transistor	50
41AF	Digital IC	70	45G	Transistor	50
41AH	Linear IC	75	45H	Transistor	49
41AJ	Linear IC	76	45J	Transistor	49
41AK	Digital IC	66	45K	Transistor	50
41AL	Digital IC	66	45L	Transistor	50
41AM	Digital IC	66	45M	Transistor	50
41AN	Digital IC	66	45N	Transistor	50
41AR	Linear IC	76	46A	Linear IC	76
41AT	Linear IC	76	46A	Transistor	49
41AU	Digital IC	68	46C	Transistor	49
41AW	Digital IC	68	46D	Transistor	49
41AY	Digital IC	68	46E	Transistor	49
41BA	Digital IC	68	46F	Transistor	49
41BB	Digital IC	68	51A	Transistor	53
41BC	Digital IC	68	51B	Transistor	53
41BD	Digital IC	68	51C	Transistor	53
41BE	Digital IC	68	51D	Transistor	53
41BF	Digital IC	68	51E	Transistor	53
41BH	Digital IC	66	51F	Transistor	54
41BJ	Linear IC	76	51G	Transistor	54
41CB	Digital IC	70	51H	Transistor	53

DEVICE CHARACTERISTICS

SELECTION GUIDE

Code	Title	Page	Code	Title	Page
53A	Linear IC	76	68B	Transistor	50
53B	Linear IC	76	69A	Transistor	54
53C	Linear IC	76	69B	Transistor	54
55A	Transistor	50	70A	Transistor	53
55B	Transistor	53	71A	Transistor	53
56A	Transistor	53	72A	Transistor	50
56B	Transistor	53	73A	Transistor	53
58A	Transistor	53	75A	Transistor	53
58B	Transistor	53	76A	Transistor	49
59A	PNPN Device	51	76B	Transistor	49
60A	Transistor	53	77A	Transistor	49
61A	Transistor	52	77B	Transistor	49
61B	Transistor	52	77C	Transistor	49
61C	Transistor	52	77D	Transistor	49
61D	Transistor	52	79A	Transistor	50
61E	Transistor	52	100A	Multiple Diodes	62
62A	Transistor	49	100D	Multiple Diodes	62
62B	Transistor	49	100E	Multiple Diodes	62
62C	Transistor	49	100F	Multiple Diodes	62
65A	Linear IC	77	100G	Multiple Diodes	62
65A	Transistor	50	100H	Multiple Diodes	62
65B	Transistor	50	101A	Digital IC	74
66C	Transistor	50	101A	Multiple Diodes	62
66F	Transistor	50	101B	Digital IC	74
66G	Transistor	50	101C	Digital IC	74
66H	Transistor	50	101D	Digital IC	74
66J	Transistor	50	101E	Digital IC	74
66K	Transistor	50	101F	Digital IC	74
66L	Transistor	50	101G	Digital IC	74
66N	Transistor	50	101H	Digital IC	74
66P	Transistor	50	101J	Digital IC	74
66R	Transistor	50	101K	Digital IC	74
66S	Transistor	50	101L	Digital IC	74
66T	Transistor	50	101M	Digital IC	74
66U	Transistor	50	101N	Digital IC	74
68A	Transistor	50	101P	Digital IC	74

SOLID STATE DEVICES

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101R	Digital IC	74	426AB	1 Watt Volt. Reg.	57
101S	Digital IC	74	426AC	Rectifier	55
106A	Multiple Diodes	62	426AD	Rectifier	55
106B	Multiple Diodes	62	426AF	Rectifier	55
107A	Multiple Diodes	62	426AG	1 Watt Volt. Reg.	57
400A	Germanium Diode	61	426AH	1 Watt Volt. Reg.	57
400E	Germanium Diode	61	426AK	1 Watt Volt. Reg.	57
400F	Germanium Diode	61	426AM	1 Watt Volt. Reg.	57
400G	Germanium Diode	61	426AN	Special Use Diode	64
400H	Germanium Diode	61	426AP	Rectifier	55
400J	Germanium Diode	61	426AR	1 Watt Volt. Reg.	57
405B	Microwave Diode	62	426AS	1 Watt Volt. Reg.	57
405C	Microwave Diode	62	426AT	1 Watt Volt. Reg.	57
405E	Microwave Diode	62	426AU	1 Watt Volt. Reg.	57
406A	Microwave Diode	62	426AW	Rectifier	55
406B	Microwave Diode	62	440A	Rectifier	55
416C	Multiple Diodes	62	441A	Germanium Diode	61
424A	Germanium Diode	61	441F	Germanium Diode	61
426A	Rectifier	55	441H	Germanium Diode	61
426E	1 Watt Volt. Reg.	57	441J	Germanium Diode	61
426F	Rectifier	55	443E	PNPN Device	51
426G	Rectifier	55	446A	Switching Diode	60
426H	Rectifier	55	446B	0.4 Watt Volt. Reg.	58
426J	Rectifier	55	446C	0.4 Watt Volt. Reg.	58
426K	Rectifier	55	446D	0.4 Watt Volt. Reg.	58
426L	Rectifier	55	446E	0.4 Watt Volt. Reg.	58
426M	1 Watt Volt. Reg.	57	446F	Rectifier	55
426N	Special Use Diode	64	446G	0.4 Watt Volt. Reg.	58
426P	1 Watt Volt. Reg.	57	446H	0.4 Watt Volt. Reg.	58
426R	1 Watt Volt. Reg.	57	446K	Rectifier	55
426S	1 Watt Volt. Reg.	57	446L	0.4 Watt Volt. Reg.	58
426T	1 Watt Volt. Reg.	57	446M	0.4 Watt Volt. Reg.	58
426U	1 Watt Volt. Reg.	57	446N	0.4 Watt Volt. Reg.	58
426W	1 Watt Volt. Reg.	57	446P	Special Use Diode	64
426Y	1 Watt Volt. Reg.	57	446R	0.4 Watt Volt. Reg.	58
426AA	Special Use Diode	64	446S	0.4 Watt Volt. Reg.	58

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Code	Title	Page	Code	Title	Page
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446U	0.4 Watt Volt. Reg.	58	459D	0.25 Watt Volt. Reg.	59
446W	0.4 Watt Volt. Reg.	58	459E	0.25 Watt Volt. Reg.	59
446Y	0.4 Watt Volt. Reg.	58	459F	0.25 Watt Volt. Reg.	59
446AA	Special Use Diode	64	459G	0.25 Watt Volt. Reg.	59
446AB	Special Use Diode	64	459H	0.25 Watt Volt. Reg.	59
446AC	Special Use Diode	64	459J	0.25 Watt Volt. Reg.	59
446AD	0.4 Watt Volt. Reg.	58	459AA	0.25 Watt Volt. Reg.	59
446AE	Special Use Diode	64	459AB	0.25 Watt Volt. Reg.	59
446AF	Special Use Diode	64	459AC	0.25 Watt Volt. Reg.	59
446AG	Special Use Diode	64	459AD	0.25 Watt Volt. Reg.	59
446AH	Special Use Diode	64	459AE	0.25 Watt Volt. Reg.	59
446AJ	Special Use Diode	64	459AF	0.25 Watt Volt. Reg.	59
446AK	Special Use Diode	64	459AG	0.25 Watt Volt. Reg.	59
448A	0.4 Watt Volt. Reg.	58	459AH	0.25 Watt Volt. Reg.	59
448B	0.4 Watt Volt. Reg.	58	459AJ	0.25 Watt Volt. Reg.	59
448C	0.4 Watt Volt. Reg.	58	459BA	0.25 Watt Volt. Reg.	59
449A	Switching Diode	60	459BB	0.25 Watt Volt. Reg.	59
456A	Rectifier	55	459BC	0.25 Watt Volt. Reg.	59
456B	Rectifier	55	459BD	0.25 Watt Volt. Reg.	59
456C	Rectifier	55	459BE	0.25 Watt Volt. Reg.	59
456D	Rectifier	55	459BF	0.25 Watt Volt. Reg.	59
456E	Rectifier	55	459BG	0.25 Watt Volt. Reg.	59
457A	Special Use Diode	64	459BH	0.25 Watt Volt. Reg.	59
457F	Special Use Diode	64	459BJ	0.25 Watt Volt. Reg.	59
458A	Rectifier	55	459CA	0.25 Watt Volt. Reg.	59
458A	Switching Diode	60	459CB	0.25 Watt Volt. Reg.	59
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NPN SILICON PLANAR TRANSISTORS

Code	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)CES}$ (Min.)	$V_{(BR)CBO}$ (Min.)	$V_{(BR)EBO}$ (Min.)	$V_{CE(sus)}$	I_{CBO} µAdc (Max.)	h_{fe} (Min.)	h_{FE} (Min.)	f_T(Min.) (MHz)	f_T(Med) (MHz)	Mfg. Location
46A ●	P-19	P	4.0 ★	30		3.0	27	10		65-175	700		AL
46C ●	P-19	P	4.0 ★	30		3.0	32	10		25-250	650		AL
46D ●	P-19	R	4.0 ★	30		3.0	32	10		45-120	650		AL
46E ●	P-19	R	4.0 ★	30		3.0	27	10		30-90	600		AL
46F ●	P-19	R	4.0 ★	27		3.0	27	10		20	700		AL
62A ●	P-69	P	4.0 ★	30		3.0	27	10		65-175	700		AL
62B ●	P-69 ♦8	P	4.0 ★	30		3.0	27	10		65-175	700		AL
62C ●	P-69	P	4.0 ★	27		3.0	27	10		25-120	500		AL
20J	P-44	P	1.50	50		5.0	29	1.0	24			180	AL
20K	P-44	P	1.50	55		5.0	21	1.0	20			180	AL
20L ●	P-44	P	1.50	70		6.0	50	1.0		24		140	AL
20M	P-44	P	1.50	85		5.0	21	1.0	20			180	AL
20N ●	P-44	P	1.50	70		5.0	29	1.0		22		180	AL
20P	P-44	P	1.50	70		5.0	29	1.0	20			110	AL
20R	P-44	P	1.50	70		5.0	29	1.0		22		110	AL
76A ●	♦	P	1.50	20		3.0	20	10.0		60-150	1800-2250		AL
76B ●	♦	P	1.50	20		3.0	20	10.0		60-150	1850-2400		AL
77A ● ♣8	P-20	P	1.50	20		3.0	17	10.0		60-145	1600-1900		AL
77B ● ♣8	P-20	P	1.50	20		3.0	17	10.0		60-145	1850-2250		AL
77C ● ♣8	P-20	P	1.50	20		3.0	20	10.0		60-150	1850-2250		AL
77D ● ♣8	P-20	P	1.50	20		3.0	20	10.0		50-160	1800-2300		AL
24C	P-13	P	0.83	85		5.0	34	1.0	32-155			160	AL
24D ●	P-13	P	0.83	55		5.0	34	1.0	35-180			250	AL
23B	P-15	P	0.70	85		5.0	34	1.0	32-155			160	AL
45J ●	P-20	P	0.40	20		3.0	12	0.2		60-400	800		AL
22B	P-1 (2)	P	Two 16F's matched for V_{BE} and h_{FE}										AL
22D ▲1	P-1	P	0.40	55		6.0	18	1.0	h_{FB}=0.94			200	AL
45H ● ★4	P-20	P	0.400	20		3.0	12	1.0		60-400	800		AL

P = Preferred ● Epitaxial ★ With T_C at 25 C ♦8 Except the tab length is shorter ♦ Picture not available

R = Restricted (Check use with Applications Engineer) ▲1 Two transistors selected for individual t_{off} = 11-38 ns and combined t_{off} matched within 4.0 ns

★4 NF= 2.6 dB max. @ 30-70 MHz. R_G = 50 Ω ♦9 With infinite heat sink ♣10 Two Transistors paired for 10% h_{FE} match.

♣9 Two NPN transistors matched for ΔH_{FE} to within 25%. $\Delta V_{BE(ON)} \leq 5mV$, ΔC_{eb} (dir) <0.3 pF.

Care should be taken if any of the breakdown characteristics are exceeded. This is particularly true of epitaxial transistors which have low collector body resistance.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

NPN SILICON PLANAR TRANSISTORS

Code	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)CES}$ (Min.)	$V_{(BR)CBO}$ (Min.)	$V_{(BR)EBO}$ (Min.)	$V_{CE}(sus)$ (Min.)	I_{CBO} μAdc (Max.)	h_{fe} (Min.)	h_{FE} (Min.)	f_T(Min.) (MHz)	f_T(Med) (MHz)	Mfg. Location
66C	P-67	P	0.40	32		5.0	11	1.0	12.2			220	AL
66F	P-67	P	0.40	55		5.0	21	1.0	29-220			300	AL
66G ●	P-67	P	0.40	55		5.0	27	1.0	45-550			300	AL
66H	P-67	P	0.40	Same as 66F with 5 dB NF.									AL
66J ●	P-67	P	0.40	60		5.0	23	1.0				300	AL
66K	P-67	P	0.40	104		5.0	23	1.0	32-275			300	AL
66L	P-67	P	0.40	85		5.0	34	1.0	32-155			160	AL
66N	P-67	P	0.40	55		5.0	18	1.0		35-199			AL
66P ●	P-67	P	0.40	70		5.7	29	1.0				350	AL
66R ●	P-67	P	Same as 66G except h_{FE} (Min.) is 85.										
66S ●	P-67	P	0.40		35	5.7	29	1.0				350	AL
66T	P-67	P	0.40	32		5.0		1.0		40-185			AL
66U	P-67	P	0.40	85		5.0	55	1.0	32-155			160	AL
72A	P-62 (2)	R	Electrically two 66F's. The product of two h_{fe}'s is 3200 - 14,000.										AL
45B ●	P-20	P	0.330	20		3.0	12	0.3		30-330	800		AL
45C ●	P-20	P	0.330	20		3.0	12	0.5		30-330	800		AL
45D ●	P-20	P	0.330	20		3.0	16	1.0		60-330	800		AL
45E ●	P-20	P	0.330	20		3.0	12	0.3		60-330	800		AL
45F ●	P-20	P	0.330	20		3.0	12	0.5		60-330	850		AL
45G ● ★5	P-20	P	0.330	20		3.0	15	1.0		85-330	900		AL
45K ●	P-20	P	0.330	19		3.0	16	1.0		6.3(INV)			AL
45L ● ★4	P-20	P	0.330	20		3.0	15	1.0		85-330	900		AL
45M ●	P-20	P	0.330	19		3.0	15	1.0		60	400		AL
65A ●	P-20 (2)	P	Two 45E's matched for h_{FE} ratio ≤1.25										
65B	P-20	P	Two 45A's matched for V_{BE} (ON) ($\triangle V_{BE}$ (ON) ≤0.02 Vdc)										
45N ●	P-20	P	0.330	20		3.0	10	1.0		60	400		AL
44D ●	P-1	P	0.30	7.0		4.5	7.5	1.0		25-275	600		AL
44C ●	P-1	P	0.250	20		5.0	7.5	2.0		40-275	600		AL
68A ●	P-1 (2)	P	Two 44C's matched for storage time ($\triangle t_s$≤1.0 ns max.)										
68B ●	P-1	P	Two 44C's matched for storage time ($\triangle t_s$≤1.0 ns and V_{BE}(ON) ($\triangle V_{BE}$≤0.010 Vdc)										
44A ●	P-1	P	0.20	20		3.0	12	0.5		30-330	800		AL
44E ●	P-1	P	0.20	20		3.0	12	0.5		80-330	800		AL
44F ●	P-1	P	0.20	20		5.0	12	0.5		40			AL
44G ●	P-1	P	0.20	20		3.0	15	0.5		30-330	800		AL
45A ●	P-20	P	0.20	20		3.0	12	0.01		30-330	800		AL
55A	P-70	P	0.20 ◆9	20		3.0	12	1.0		25-275	400		AL
79A ♣9	◆	P	0.20 ◆9	14.0		5.5	12	0.05		30-250	450		AL
44B ●	P-1	P	0.10	6.0		4.5	6.5	0.5		25-275	600		AL

P = Preferred ● Epitaxial ★5 NF= 4.0 dB max. - @ 70 MHz. ★4 NF= 2.6 dB max. @ 30.70 MHz. R_G=50Ω ♣9 Two NPN Transistors matched for $\triangle H_{FE}$ to within 25% $\triangle V_{BE(ON)}$≤5 mV, $\triangle C_{eb}$(dir)<0.3pF.

R = Restricted (Check use with Applications Engineer) ◆9 With infinite heat sink.

Care should be taken if any of the breakdown characteristics are exceeded. This is particularly true of epitaxial transistors which have low collector body resistance.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

PNP GERMANIUM ALLOY TRANSISTORS

Code	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)CBO}$ (Min.)	$V_{(BR)EBO}$ (Min.)	$V_{(BR)CEV}$ (Min.)	$V_{CE(sus)}$ (Min.)	I_{CBO} μAdc (Max.)	$-h_{fb}$ (Min.)	$-h_{FB}$ (Min.)	f_T(Med) (MHz)	h_{fe} (Min.)	Mfg. Location
9A	P-68	P	30.0 ★	54	45	54		200				18.66	AL
9B	P-68	R	2.80	36	18			25				45-165	AL
9D	P-68	P	2.80	36	18			25				36-165	AL
9E	P-68	R	Same as 9A except for rise time of 2 μsec max.										AL

P-N-P-N DEVICES

Code	Description	Package	Status	I (Amps)	$V_{(BR)F}$ (Min.) ♠3	$V_{(BR)R}$ (Min.)	I_B (mAdc) (Max.)	@ $V_{(BR)F}$	I_H (mAdc) (Max.)	t_{rr} (ns) (Max.)	Mfg. Location
27A	3-Term PNPN Si	P-1	P	0.10	200	200	0.4	10	7.0 ♠3		AL
27B	3-Term PNPN Si	P-1	P	0.10	350	350	1.0	10	7.0 ♠3		AL
27C	3-Term PNPN Si	P-1	P	0.10	200	200	0.010	10	3.0 ♠3		AL
27D	3-Term PNPN Si	P-1	P	0.10	200	200	.05-.5	10	10.0 ♠4		AL
27E	3-Term PNPN Si	P-1	P	0.10	250	250	2.0	3	18●2 ♠3		AL
27F	3-Term PNPN Si	P-1	P	0.10	270	270	1.0	10	10.0 ♠3		AL
27G	3-Term PNPN Si	P-1	P	0.10	200	200	2.0	30	23●3 ♠8		AL
27H	3-Term PNPN Si	P-1	P	0.10	200	200	0.05-0.5	10	15 ♠4		AL
34A	3-Term PNPN Si	P-46	P	5.0	175	150	5.0	10	7.0 ♠3		AL
34B	3-Term PNPN Si	P-46	P	5.0	175	150	5.0	10	7.0 ♠3		AL
34C	3-Term PNPN Si	P-46 ◆13	P	5.0	175	150	5.0	10	7.0 ♠3		AL
59A	3-Term PNPN Si	P-44	P	1.0	185	185	0.5-7.0	10	2.0		AL
443E	2-Term PNPN Si	P-77	P	25 ●10	12-19.0	25			50		AL

P = Preferred ♠3 For 3 Terminal Devices with R_G = 1000 ohms. ●2 Minimum ●3 Minimum Value = 12 ♠8 R_G = 100 ohms.

R = Restricted (Check with Applications Engineer) ●10 Pulsed ♠4 For 3 terminal devices with R_G = 0 ohms. ◆13 Without crimped on-wire leads.

▲2 **Pinch-off voltage,** V_{GS}, @ I_{DS} = 10 nAdc, V_{DS} = 10 Vdc. ▲3 @ V_{GS} = 0, V_{DS} = 25 mV. ★ With T_C = 25 C

Care should be taken if any of the breakdown characteristics are exceeded. This is particularly true of epitaxial transistors which have low collector body resistance.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

N—CHANNEL SILICON JUNCTION FIELD EFFECT TRANSISTORS

Code	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)DGO}$ $V_{(BR)SGO}$ (Min.)	I_{DSS} mAdc (Min.)	V_P ▲2	I_{GSS} nAdc (Max.)	@ V_{GS} Vdc	C_{gss} ▲3 pF	r_{ds} ▲3 ohms (Max.)	g_{ds} ▲3 μmho	Mfg. Location
61A	P-1	P	0.25	20	20	6.5	5	10	20 Max.	250		RD
61B	P-1	P	0.25	20	20	2.5 - 7.5	5	10	33 Typ.		1.4k-2.8k	RD
61C	P-1	P	0.25	25	25	7.0 - 19.0	5	20	20 Max.	80		RD
61D	P-1	P	0.25	25	3-32	6.5	5	10	20 Max.			RD
61E	P-1	P	0.25	20		3.0 - 6.0	5	10	20 Max.	100-150		RD

P = Preferred ♠3 For 3 Terminal Devices with R_G = 1000 ohms. ●2 Minimum ●3 Minimum Value = 12 ♠8 R_G = 100 ohms.

R = Restricted (Check with Applications Engineer) ●10 Pulsed ♠4 For 3 terminal devices with R_G = 0 ohms. ♦13 Without crimped on-wire leads.

▲2 **Pinch-off voltage**, V_{GS}, @ I_{DS} = 10 nAdc, V_{DS} = 10 Vdc. ▲3 @ V_{GS} = 0, V_{DS} = 25 mV. ★ With T_C = 25 C

Care should be taken if any of the breakdown characteristics are exceeded. This is particularly true of epitaxial transistors which have low collector body resistance.
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

DEVICE CHARACTERISTICS

PNP DIFFUSED BASE GERMANIUM

Code	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)CBO}$ (Min.)	$V_{(BR)EBO}$ (Min.)	$V_{(BR)CEO}$ (Min.)	$V_{(BR)CES}$ (Min.)	$V_{CE}(sus)$ (Min.)	I_{CBO} μAdc (Max.)	h_{fe} (Min.)	h_{FE} (Min.)	f_T(Min.) (MHz)	Mfg. Location
15A	P-6	P	0.25	30	0.8	15			6.0	15-330		400	RD
15B	P-6	P	Same as 15A except V_{CE}(sat) = 1.5 Vdc Maximum										RD
15C	P-6	P	0.25	30	0.8	15			6.0	30-200		400	RD
15D	P-6	R	Same as 15C except NF = 31.0 dB max. at f = 1 kHz: V_{CE}(sat) = 3.0 Vdc max.										RD
26A	P-8	P	0.10	20	0.8	10			5.0	15-250(NF = 7.5 dB max. @ 70 MHz)			RD
26B	P-8	P	Same as 26A except NF = 6.0 dB max. @ 70 MHz										RD

BEAM LEAD TRANSISTORS

Code	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)CBO}$ (Min.)	$V_{(BR)EBO}$ (Min.)	$V_{(BR)CEO}$ (Min.)	$V_{(BR)CES}$ (Min.)	$V_{CE}(sus)$ (Min.)	I_{CBO} μAdc (Max.)	h_{fe} (Min.)	h_{FE} (Min.)	f_T(Min.) (MHz)	Mfg. Location
55A	P-70	P	0.20 ◆9		4.0		20	12	1.0		25-275	400	AL
55B	P-70	P	0.20 ◆9		4.0		30	26	1.0		25	200	AL
56A	P-71	P	—		4.0			12	2.0 ●11		25-275	400	AL
56B	P-71	P	—		4.0		20	12	1.0		25	300	AL
60A ▲	P-72	P	0.20 ◆9		5.5	30	40		0.1		30-300	100	AL
73A ♣9	◆	P	0.20 ◆9 Common Collectors		5.5		8.0	7.0 ▲6	0.05		40	450	AL
75A ♣9	◆	P	0.20 ◆9 Isolated Collectors		5.5		14.0	12	0.05		30-250	450	AL

PNP SILICON PLANAR TRANSISTORS

Code	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)CBO}$ (Min.)	$V_{(BR)EBO}$ (Min.)	$V_{(BR)CEO}$ (Min.)	$V_{(BR)CES}$ (Min.)	$V_{CE}(sus)$ (Min.)	I_{CBO} μAdc (Max.)	h_{fe} (Min.)	h_{FE} (Min.)	f_T(Min.) (MHz)	Mfg. Location
58A ●	P-44	P	1.5		5.5	30	40		0.1		25-140	100	AL
58B ●	P-44	P	1.5		5.5	45	45		0.1		30-220	100	AL
51A ●	P-67	P	0.250		5.5	30	40		0.03		30-210	100	AL
51B ●	P-67	P	0.250		5.5	53	54		0.03		30-210	100	AL
51C ●	P-67	P	0.250		30	30	30		0.03		30-210	10	AL
51D ●	P-67	P	0.250		5.5	30	40		0.03		25	100	AL
51E ●	P-67	P	0.250		5.5	30	40		0.03		38-210	100	AL
51H ●	P-67	P	0.250		5.5	95	95		0.1		40-250	100	AL
70A ●	P-67 (2)	P	Matched Pair of 51A's; $\Delta V_{BE} \leq 0.01$V										
71A ●	P-67 ▲5	P			5.5	30	40		0.03		45-135	100	AL

P = Preferred ◆9 With infinite heat sink ●11 I_{CES} ▲ 60A is PNP ● Epitaxial ▲5 Pair of P-67's held together with metal clip.

R = Restricted (Check use with Applications Engineer) ◆ Picture Not Available ▲6 Inverse V_{CE}(sat)≤.080 Vdc, collector to base reverse recovery ≤ 25 μs

♣9 Two NPN transistors matched for ΔH_{FE} to within 25% $\Delta V_{BF(ON)} \leq 5$ mV, ΔC_{eb} (dir) <0.3pF.

Care should be taken if any of the breakdown characteristics are exceeded. This is particularly true of epitaxial transistors which have low collector body resistance.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

SWITCHING TRANSISTORS

(DIFFUSED SILICON PLANAR NPN) ▲

Code	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)CBO}$	$V_{(BR)CES}$	t_r	t_{on}	t_s	t_{off}	t_s	f_T(Min.) (MHz)	f_T(Med) (MHz)	Mfg. Location
44B ●	P-1	P	0.10		6.5	6.0		4.5		4.5	600		AL
44C ●	P-1	P	0.250		21	6.0		4.5			600		AL
44D ●	P-1	P	0.30		8.0	6.0		4.5			600		AL
55A	P-70	P	0.20 ♦9		20			15		15	400		AL
69A ●	P-67	P	0.20	25				15		15		400	AL
56A	P-71	P						15			400		AL
56B	P-71	P						18			300		AL
69B ●	P-67	P	0.20	25				18				300	AL
51F ● ▲	P-67	P	0.250		54			200			100		AL
51G ● ▲	P-67	P	0.250		40			200-400			100		AL
20N ●	P-44	P	1.50		70		100	150				180	AL
20L ●	P-44	P	1.50		70		160	350				140	AL
20R	P-44	P	1.50		70		110	350				110	AL
66J ●	P-67	P	0.40		60			160				300	AL
66P ●	P-67	R	0.40		70		75		75				AL
66S ●	P-67	P	0.40		35		75	175				350	AL

P = Preferred ▲ 51G & 51F are PNP ● Epitaxial ♦9 With infinite heat sink

R = Restricted (Check use with Applications Engineer)

All units of time are nanoseconds.

Care should be taken if any of the breakdown characteristics are exceeded. This is particularly true of epitaxial transistors which have low collector body resistance.
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

RECTIFIERS

Code	Description	Package	Status	Power (Watts) T_A = 25 C	i_f (surge) (A pulse) (Max.)	I_O (Adc) (Max.)	t_{rr} (Max.) ns @	$I_F = I_R$ (mAdc)	$V_{(BR)}$ (Vdc) (Min.) @	I_R (μAdc)	V_F (Vdc) (Max.) @	I_F (Adc) (Min.)	I_S (μAdc) (Max.) @	V_R (Vdc)	Mfg. Location
485A	Si Diff	P-36	P	10.0 ★2	100	10.0			250	10	1.15	10.0	3.0	200	RD
485K	Si Diff	P-36	P	10.0 ★2	20	10.0	170	100	100	25	1.30	2.0	3.0	80	RD
485L	Si Diff	P-36	P	10.0 ★2	70	7.0	200	100	200	25	1.45	7.0	5.0	160	RD
485AB ♠7	Si Diff	P-36	P	10.0 ★2	100	10.0			250	10	1.15	10.0	3.0	200	RD
485AE	Si Diff	P-36	P	10.0 ★2	100	10.0	200	100	100	25	0.95	6.0	2.0	80	RD
485AL ♠7	Si Diff	P-36	P	10.0 ★2	70	7.0	200	100	200	25	1.45	7.0	5.0	160	RD
426A	Si Diff	P-63	P	1.0	20	1.0			250	10	1.05	1.0	1.0	200	RD
426F	Si Diff	P-63	P	1.0	20	1.0			500	10	1.05	1.0	1.0	400	RD
426G	Si Diff	P-63	R	1.0	12	.600			1200	25	2.1	0.60	3.0	1000	RD
426H	Si Diff	P-63	R	1.0	8.0	.400			1800	25	3.0	0.40	3.0	1500	RD
426J	Si Diff	P-63	R	1.0	6.0	.300			2400	25	3.7	0.30	3.0	2000	RD
426K	Si Diff	P-63	P	1.0	20	1.0			600	10	1.05	1.0	1.0	500	RD
426L ●9	Si Diff	P-63	P	1.0	12	.600	130	100	800	25	2.3	0.60	3.0	650	RD
426AC ●9	Si Diff	P-63	P	1.0	10	1.0	100	100	120	10	1.35 ●5	1.35 ●5	1.0	50	RD
426AD ●9	Si Diff	P-63	P	1.0	10	1.0	200	100	120	10	1.0	1.0	1.0	100	RD
426AF	Si Diff	P-63	R	1.0	10	1.0			600	10	1.05	1.0	.050	200	RD
426AP ●9	Si Diff	P-63	R	1.0		.30	100	100	1000	25	3.5	.300	3.0	800	RD
426AW	Si Diff	P-63	R	1.0	200	1.0			800	10	2.0	1.0	5.0	160	RD
440A	Si Diff	P-34	R	0.75	12	.750			100 ●4	1.0	1.15	0.75	1.0	100	RD
446F	Si Diff	P-39	P	0.40	3.0	.400			400-950	10	1.0	0.40	2.0	320	RD
446K	Si Diff	P-39	P	0.40	3.0	.400			600-950	10	1.0	0.40	2.0	480	RD
456A	Si Diff	P-30	P	0.20	1.0	.200 ■7			100	5.0	1.1	0.20	0.10	80	RD
456B	Si Diff	P-30	P	0.20	1.0	.200 ■7			200	5.0	1.1	0.20	0.10	160	RD
456C	Si Diff	P-30	P	0.10	1.0	.100 ■7			400	5.0	1.1	0.10	0.10	320	RD
456D	Si Diff	P-30	P	0.10	1.0	.100 ■7			600	5.0	1.1	0.10	0.10	480	RD
456E ★10	Si Diff	P-30	R	0.20		.200 ■7			75	5.0	0.51	0.001	0.200	40	RD
458A	Si Diff	P-30	P	0.10		.100			75	5.0	1.1	0.40	0.20	40	RD

P = Preferred ●9 **Medium speed rectifier. For switching time,use official Data Sheet and Switching Diode section of this Quick Selection List.** ●5 Peak pulse.

R = Restricted (Check use with Device Engineer.) ●4 P.I.V. ★2 With T_C at 65 C. ♠7 Reverse polarity; case is positive for reverse bias.

■7 Implied by power rating. ★10 z_f = 60 Ω max. @ I_F = 1.0 mAdc

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

10 WATT VOLTAGE REGULATORS ★2

Code	Description	Package	Status	$V_{(BR)}$ (Vdc) @	I_R (mAdc)	V_F (Vdc) (Max.) @	I_F (Adc) (Min.)	I_S (μAdc) (Max.) @	V_R (Vdc)	z_{br} (Ohms) (Max.) @	I_R (mAdc)	TCBV (%/°C) (Nom.)	Mfg. Location
485C	Si Diff	P-36	R	22 ± 3%	30	1.25	10	3.0	18	12	30	.080	RD
485D	Si Diff	P-36	P	18 ± 5%	100	1.25	10	3.0	14.5	4.0	100	.080	RD
485E	Si Diff	P-36	P	12 ± 5%	50	1.25	10	3.0	9.5	2.0	50	.060	RD
485F	Si Diff	P-36	P	15 ± 5%	100	1.25	10	3.0	12	2.0	100	.070	RD
485G ■3	Si Diff	P-36	P	8.65 ± 5%	10	—	—	50	5.0	20	10	.002	RD
485H ♣7	Si Diff	P-36	P	22 ± 5%	20	1.25	10	3.0	17.5	12	20	.080	RD
485J	Si Diff	P-36	P	22 ± 5%	20	1.25	10	3.0	17.5	12	20	.080	RD
485M	Si Diff	P-36	P	8.2 ± 5%	200	1.25	10	20	6.5	3.0	200	.050	RD
485N	Si Diff	P-36	P	27 ± 5%	50	1.25	10	4.0	21.5	8.0	50	.085	RD
485P ♣7	Si Diff	P-36	P	27 ± 5%	50	1.25	10	4.0	21.5	8.0	50	.085	RD
485R ♣7	Si Diff	P-36	P	18 ± 5%	100	1.25	10	3.0	14.5	4.0	100	.080	RD
485U ★7	Si Diff	P-36	R	12.4 ± 2%	1.0	1.25	10	3.0	9.5	3.0	50	.060	RD
485W	Si Diff	P-36	P	140 ± 5%	18	1.25	10	3.0	115	100	18	.100	RD
485Y ♣7	Si Diff	P-36	P	140 ± 5%	18	1.25	10	3.0	115	100	18	.100	RD
485AA	Si Diff	P-36	P	24 ± 5%	50	1.25	10	3.0	20	8.0	50	.085	RD
485AC ♣7	Si Diff	P-36	P	8.2 ± 5%	200	1.25	10	20	6.5	3.0	200	.050	RD
485AF ♣7	Si Diff	P-36	P	12 ± 5%	50	1.25	10	3.0	9.5	2.0	50	.080	RD
485AG	Si Diff	P-36	P	13 ± 5%	50	1.25	10	3.0	10.5	3.0	50	.080	RD
485AK ■7	Si Diff	P-36	R	18 ± 2%	60	1.25	10	3.0	14.5	2.0	60	.080	RD
485AM ♣7	Si Diff	P-36	R	18 ± 2%	60	1.25	10	3.0	14.5	2.0	60	.080	RD
485AN	Si Diff	P-36	R	27 ± 2%	50	1.25	10	4.0	21.5	8.0	50	.085	RD
485AP ♣7	Si Diff	P-36	R	27 ± 2%	50	1.25	10	4.0	21.5	8.0	50	.085	RD

P = Preferred ★2 With T_C at 65 C. ■3 Intended for low temperature coefficient voltage regulator applications - 1 Watt.

R = Restricted (Check use with Device Engineer) ♣7 Reverse polarity; case is positive for reverse bias. ★7 Also $V_{(BR)}$ = 13.2 Vdc max.@ I_R = 200 mAdc.

■7 45 amp lightning surge protector in reverse direction.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

1.0 WATT VOLTAGE REGULATORS

Code	Description	Package	Status	$V_{(BR)}$ (Vdc) @	I_R (mAdc)	V_F (Vdc) (Max.) @	I_F (Adc) (Min.)	I_S (μAdc) (Max.) @	V_R (Vdc)	z_{br} (Ohms) (Max.) @	I_R (mAdc)	TCBV (%/°C) (Nom.)	Mfg. Location
426E ■4	Si Diff	P-63	P	68 ± 5%	20	1.0	1.0	3.0	55	30	20	.090	RD
426M	Si Diff	P-63	P	22 ± 5%	10	1.0	1.0	1.0	18	30	10	.080	RD
426P	Si Diff	P-63	P	12 ± 5%	20	1.0	1.0	5.0	9.5	10	20	.060	RD
426R	Si Diff	P-63	P	18 ± 5%	10	1.0	1.0	1.0	14.5	25	10	.080	RD
426S	Si Diff	P-63	P	15 ± 5%	10	1.0	1.0	1.0	12	17	10	.070	RD
426T	Si Diff	P-63	P	8.2 ± 5%	20	1.0	1.0	5.0	6.5	5.0	20	.090	RD
426U ■5	Si Diff	P-63	P	18 ± 5%	10	1.0	1.0	3.0	14.5	15	10		RD
426W ●7	Si Diff	P-63	P	8.65 ± 5%	10	—	—	50	5.0	20	10	.005	RD
426Y ■6 ♁7	Si Diff	P-63	P	6.8 ± 10%	20	1.0	1.0	200	4.5	8.0	20	.05	RD
426AB ●7	Si Diff	P-63	R	8.65 ± 5%	10	—	—	50	5.0	20	10	.003	RD
426AG	Si Diff	P-63	P	27 ± 5%	5.0	1.0	1.0	2.0	21.5	50	5.0	.085	RD
426AH	Si Diff	P-63	P	75 ± 5%	2.0	1.0	1.0	2.0	60	175	2.0	.090	RD
426AK	Si Diff	P-63	P	33 ± 5%	10	—	—	2.0	26	75	10	.070	RD
426AM	Si Diff	P-63	P	105 ± 5%	2.0	1.0	1.0	2.0	85	350	2.0	.090	RD
426AR	Si Diff	P-63	P	6.8 ± 5%	20	1.0	1.0	200	4.6	6.0	20	.08	RD
426AS	Si Diff	P-63	P	13 ± 5%	10	1.0	1.0	3.0	10.5	20	10	.08	RD
426AT ■6	Si Diff	P-63	P	6.2 ± 5%	20	1.0	1.0	2000	4.5	—	—	.03	RD
426AU	Si Diff	P-63	R	7.6 ± 1.4%	20	—	—	200	45	10	75	.015	RD
470A ♁7	Si Alloy	P-63	P	4.7 ± 5%	50	1.0	0.5	400	3.0	7.0	50	.030	RD

P = Preferred

R = Restricted (Check use with Device Engineer)

■4 6 amp lightning surge protector in reverse direction.

■5 22 amp. lightning surge protector in reverse direction.

■6 60 amp. lightning surge protector in reverse direction.

♁7 Reverse polarity; case is positive for reverse bias.

●7 Temperature compensated V-R.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

0.4 WATT VOLTAGE REGULATORS

Code	Description	Package	Status	$V_{(BR)}$ (Vdc)	@ I_R (mAdc)	V_F (Vdc) (Max.)	@ I_F (Adc) (Min.)	I_S (μAdc) (Max.)	@ V_R (Vdc)	z_{br} (Ohms) (Max.)	@ I_R (mAdc)	TCBV (%/°C) (Nom.)	Mfg. Location
446B	Si Diff	P-39	P	6.2 ± 5%	10.0	1.0	0.40	200	4.5	6.0	10	.035	RD
446C	Si Diff	P-39	P	8.2 ± 10%	10.0	1.0	0.40	2.0	6.5	7.0	10	.060	RD
446D	Si Diff	P-39	P	12 ± 10%	10.0	1.0	0.40	1.0	9.5	10	10	.065	RD
446E	Si Diff	P-39	P	18 ± 5%	5.0	1.0	0.40	1.0	14.5	26	5.0	.085	RD
446G	Si Diff	P-39	P	27 ± 5%	5.0	1.0	0.40	1.0	21.5	35	5.0	.090	RD
446H	Si Diff	P-39	P	47 ± 5%	2.0	1.0	0.40	1.0	37.5	210	2.0	.105	RD
446L	Si Diff	P-39	P	10 ± 5%	10.0	1.0	0.40	2.0	8.0	9.0	10	.070	RD
446M	Si Diff	P-39	P	15 ± 5%	5.0	1.0	0.40	1.0	12	24	5.0	.075	RD
446N	Si Diff	P-39	P	22 ± 5%	5.0	1.0	0.40	1.0	17.5	30	5.0	.090	RD
446R	Si Diff	P-39	P	30 ± 5%	5.0	1.0	0.40	1.0	24	40	5.0	.095	RD
446S	Si Diff	P-39	P	100 ± 5%	1.0	1.0	0.40	1.0	80	350	1.0	.090	RD
446T	Si Diff	P-39	P	8.2 ± 5%	10.0	1.0	0.40	2.0	6.5	7.0	10	.065	RD
446U	Si Diff	P-39	P	62 ± 5%	1.0	1.0	0.40	1.0	49.5	285	1.0	.090	RD
446W	Si Diff	P-39	P	91 ± 5%	1.0	1.0	0.40	1.0	72.5	345	1.0	.090	RD
446Y	Si Diff	P-39	P	9.1 ± 5%	10.0	1.0	0.40	2.0	7.2	8.0	10	.065	RD
446AD	Si Diff	P-39	P	12 ± 5%	10.0	1.0	0.40	1.0	9.5	10	10	.065	RD
448A	Si Alloy	P-39	P	4.7 ± 10%	20.0	1.0	0.20	250	3.0	18	20	-.040	RD
448B	Si Alloy	P-39	P	4.3 ± 5%	20.0	1.0	0.20	1000	3.0	18	20	-.045●3	RD
448C	Si Alloy	P-39	R	4.7 ± 5%	20.0	1.0	0.20	250	3.0	18	20	-.040	RD

P = Preferred

●3 Maximum

R = Restricted (Check use with Device Engineer)

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

0.25 WATT VOLTAGE REGULATORS

Code	Description	Package	Status	$V_{(BR)}$ (Vdc)	@ I_R (mAdc)	V_F (Vdc) (Max.)	@ I_F (Adc) (Min.)	I_S (μAdc) (Max.)	@ V_R (Vdc)	z_{br} (Ohms) (Max.)	@ I_R (mAdc)	TCBV (%/°C) (Nom.)	Mfg. Location
459B	Si Diff	P-30	P	6.2 ± 5%	10.0	1.0	0.25	30.0	4.5	6.0	10		RD
459C	Si Diff	P-30	P	6.8 ± 5%	10.0	1.0	0.25	20.0	5.2	6.0	10		RD
459D	Si Diff	P-30	P	7.5 ± 5%	10.0	1.0	0.25	10.0	5.7	7.0	10		RD
459E	Si Diff	P-30	P	8.2 ± 5%	10.0	1.0	0.25	2.0	6.5	7.0	10	.060	RD
459F	Si Diff	P-30	P	9.1 ± 5%	10.0	1.1	0.20	1.0	7.2	10.0	10		RD
459G	Si Diff	P-30	P	10.0 ± 5%	10.0	1.1	0.20	0.5	8.0	15.0	10		RD
459H	Si Diff	P-30	P	11.0 ± 5%	10.0	1.1	0.20	0.1	8.8	18.0	10		RD
459J	Si Diff	P-30	P	12.0 ± 5%	10.0	1.1	0.20	0.05	9.5	20.0	10		RD
459AA	Si Diff	P-30	P	13.0 ± 5%	10.0	1.1	0.20	0.05	10.5	25.0	10		RD
459AB	Si Diff	P-30	P	15.0 ± 5%	5.0	1.1	0.20	0.02	12.0	25.0	5		RD
459AC	Si Diff	P-30	P	16.0 ± 5%	5.0	1.1	0.20	0.02	13.0	25.0	5		RD
459AD	Si Diff	P-30	P	18.0 ± 5%	5.0	1.1	0.20	0.02	14.5	26.0	5		RD
459AE	Si Diff	P-30	P	20.0 ± 5%	5.0	1.1	0.20	0.02	16.0	32.0	5		RD
459AF	Si Diff	P-30	P	22.0 ± 5%	5.0	1.1	0.20	0.02	17.5	36.0	5		RD
459AG	Si Diff	P-30	P	24.0 ± 5%	5.0	1.1	0.20	0.02	19.0	42.0	5		RD
459AH	Si Diff	P-30	P	27.0 ± 5%	5.0	1.1	0.20	0.02	21.5	48.0	5		RD
459AJ	Si Diff	P-30	P	30.0 ± 5%	5.0	1.1	0.20	0.02	24.0	56.0	5		RD
459BA	Si Diff	P-30	P	33.0 ± 5%	2.0	1.1	0.20	0.02	26.5	65	2		RD
459BB	Si Diff	P-30	P	36.0 ± 5%	2.0	1.1	0.20	0.02	29.0	75	2		RD
459BC	Si Diff	P-30	P	39.0 ± 5%	2.0	1.2	0.20	0.02	31.0	120	2		RD
459BD	Si Diff	P-30	P	43.0 ± 5%	2.0	1.2	0.20	0.02	34.5	160	2		RD
459BE	Si Diff	P-30	P	47.0 ± 5%	2.0	1.2	0.20	0.02	37.5	210	2		RD
459BF	Si Diff	P-30	P	51.0 ± 5%	2.0	1.2	0.20	0.02	41.0	260	2		RD
459BG	Si Diff	P-30	P	56.0 ± 5%	2.0	1.2	0.20	0.02	45.0	300	2		RD
459BH	Si Diff	P-30	P	62.0 ± 5%	2.0	1.2	0.20	0.02	49.5	340	2		RD
459BJ	Si Diff	P-30	P	68.0 ± 5%	2.0	1.2	0.20	0.02	54.0	400	2		RD
459CA	Si Diff	P-30	P	75.0 ± 5%	2.0	1.2	0.20	0.02	60.0	460	2		RD
459CB	Si Diff	P-30	P	82.0 ± 5%	1.0	1.2	0.20	0.02	65.0	570	1		RD
459CC	Si Diff	P-30	P	91.0 ± 5%	1.0	1.2	0.20	0.02	72.0	700	1		RD
459CD	Si Diff	P-30	P	100.0 ± 5%	1.0	1.2	0.20	0.02	80.0	850	1		RD
459CE	Si Diff	P-30	P	110.0 ± 5%	1.0	1.2	0.20	0.02	88.0	1000	1		RD
459CF	Si Diff	P-30	P	120.0 ± 5%	1.0	1.2	0.20	0.02	96.0	1200	1		RD
459CG	Si Diff	P-30	P	130.0 ± 5%	1.0	1.2	0.20	0.02	105.0	1400	1		RD
459CH	Si Diff	P-30	P	150.0 ± 5%	1.0	1.2	0.20	0.02	120.0	1700	1		RD

P - Preferred

R - Restricted (Check use with Device Engineer)

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

SWITCHING DIODES

Code	Description	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)}$ (Vdc) (Min.)	@ I_R (μAdc)	V_F (Vdc) (Max.)	@ I_F (Adc) (Min.)	I_S (μAdc) (Max.)	@ V_R (Vdc)	C ★8 (pF) (Max.)	t_{rr} (μS) (Max.)	@ $I_F = I_R$ (mAdc)	Mfg. Location
458C	Si Diff	P-30	P	0.10 ●6	40	5.0	1.0	0.01	0.015	20	4.0	0.004	10	RD
458D	Si Diff	P-30	R	0.10 ●6	40	5.0	.62-.72	0.002	0.015	20	4.0	0.004	10	RD
458G	Si Diff	P-30	R	0.10 ●6	40	5.0	1.0	0.01	0.025	20	1.5-2.0	0.004	10	RD
458E ●	Si Diff	P-30	R	0.10 ●6	50	5.0	1.0	0.100	0.050	20	4.0	0.005	10	RD
458H ●	Si Diff	P-30	P	0.10 ●6	55	5.0	1.15	0.250	0.050	20	4.0	0.005	10	RD
458J ● ★9	Si Diff	P-30	R	0.10 ●6	55	5.0	1.15	0.250	0.050	20	4.0	0.005	10	RD
458F	Si Diff	P-30	R	0.10 ●6	40	5.0	.30-.37	10^{-6}	0.025	20	5.0	0.005	10	RD
449A ■2	Si Diff	P-39	P	0.40			2.30	0.0025	2.0	150	15	0.04 ●2	2-10	RD
446A	Si Diff	P-39	P	0.40	120	5.0	1.1	0.40	2.0	100	25	0.05	100	RD
458A	Si Diff	P-30	P	0.10 ●6	75	5.0	1.10	0.40	0.200	40	30	0.050	100	RD
458B	Si Diff	P-30	R	0.10 ●6	75	5.0	.71-.84	0.10	0.200	40	30	0.050	100	RD
426AP	Si Diff	P-63	R	1.0	1000	25	2.3-3.5	0.300	3.0	800		0.100		RD
426AC	Si Diff	P-63	P	1.0	120	10	1.35 ●5	1.35 ●5	1.0	50	45	0.10	100	RD
485K	Si Diff	P-36	P	10.0 ★2	100	25.0	1.3	2.0	3.0	80	800	0.170	100	RD
426AD	Si Diff	P-63	P	1.0	120	10	1.0	1.0	1.0	100	100	0.20	100	RD
485L	Si Diff	P-36	P	10.0 ★2	200	25	1.45	7.0	5.0	160	400	0.200	100	RD
485AE	Si Diff	P-36	P	10.0 ★2	100	25	0.95	6.0	3.0	80	800	0.200	100	RD

P = Preferred ★2 With T_C at 65 C. ★8 @ V_R = 0 Vdc except 449A @ V_F = 1.0 Vdc, and 458G @ V_F = 3.0 Vdc.

R = Restricted (Check use with Device Engineer) ■2 Level Shifter; V_F = 1.53 Vdc Min. @ 70 μAdc. Stored Charge = 400 μCb @ i_f = 2 mAdc, i_r = 10 mAdc.

● Epitaxial ●2 Minimum ●5 Peak Pulse ●6 Switched Power ★9 Z_F = 15.5 — 20.5 ohms @ I_F = 3 mAdc.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

GERMANIUM DIODES

Code	Description	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)}$ (Vdc) (Min.) @	I_R (mAdc)	I_R (μAdc) (Max.) @	V_R (Vdc)	Mfg. Location
400A	Pt. Ct.	P-40	R	0.20	60		20/850	5/50	RD
400E	Pt. Ct.	P-40	R	0.20	140		500	50	RD
400F	Pt. Ct.	P-40	R	0.20	60		20/850	5/50	RD
400G	Pt. Ct.	P-40	R	0.20	60		1000	50	RD
400H	Pt. Ct.	P-40	R	0.20	60		20/850	5/50	RD
400J	Pt. Ct.	P-40	R	0.20	140		20/850	5/50	RD
424A	Pt. Ct.	P-34	R	0.20			3.5/35	5/25	RD
441A	Pt. Ct.	P-38	R	Same as 400A except axial leads					RD
441F	Pt. Ct.	P-38	R	Same as 400F except axial leads					RD
441H	Pt. Ct.	P-38	R	Same as 400H except axial leads					RD
441J	Pt. Ct.	P-38	R	Same as 400J except axial leads					RD

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

MICROWAVE DIODES

Code	Package	Status	Power (Watts) T_A = 25 C	$V_{(BR)}$ (Vdc) (Min.)	@ I_R (mAdc)	V_F (Vdc) (Max.)	@ I_F (Adc) (Min.)	I_R (μAdc) (Max.)	@ V_R (Vdc)	C_T (pF) (Max.)	Major Application	Mfg. Location
405B	P-22	R	0.40	∿3							Detector	RD
405C	P-22	R	0.02	∿3								RD
405E ■	P-22	R	0.03	∿3				100	1.0		Detector-Monitor	RD
406A	P-23	R	0.02	∿3							Converter	RD
406B	P-23	R	0.02	∿1		0.2	.0004	40	0.2		Converter	RD
471A ♠	P-28	R	0.13 ♠5	15 ♠6	0.01	1.1 ♠6	.100	0.1 ♠6	12	0.8-1.2 ♠6	Transmitter-Modulator	RD
473A	P-26	R	2.0 ★	60	0.01	1.1	.100	1.0	50	4.0-6.0	Harmonic Generator	RD
480A	P-29	R	0.03	15	0.01	1.00	.100	0.1	12	0.3-0.6	70 MHz Gates	RD
488A	P-29	R	0.05	∿3		1.0	.020	100	2.0		I. F. Detector	RD
497A ★6	P-28	R	0.05			0.95	.050	100	6.0	0.3-0.6	Down Converter	RD
498A	P-28	R	0.065	15	0.01	1.1	.100	0.1	12	0.8-1.2	Transmitter and Shift Modulator	RD
499A	P-65	R	0.03	∿3		1.0	.03	100	1.0	0.30-0.65	Detector	RD
509A ▲5	P-65	R	0.065	15	0.01	1.1	.100	0.1	12	0.8-1.2		RD

MULTIPLE DIODES

Code	Package	Status	Description	Mfg. Location
100A	P-35	P	0.90 Vdc Max. @ 100 mAdc; 0.20 Vdc Min. @ 0.01 mAdc in either direction	RD
100D	P-35	P	0.72 Vdc Max. @ 10 mAdc; 0.43 Vdc Min. @ 0.10 mAdc in either direction	RD
100E	P-35	P	Same as 100D except for addition of 50 amp. pulse test	RD
100F	P-35	P	Same as 100A except for addition of 50 amp. pulse test	RD
100G	P-35	P	0.74-0.80 Vdc @ 100 mAdc; 0.43 Vdc Min. @ 0.10 mAdc in either direction	RD
100H	P-35	P	Same as 100D, except C = 1500 pF Max. @ 1 MHz and V = 0	RD
101A	P-35	R	Seven 100 A's	RD
106A	P-61	R	2.50 Vdc Min., 3.00 Vdc Max. @ 10 mAdc; 1.30 Vdc Min. @ 0.01 mAdc in either direction	RD
106B	P-61	R	2.92 Vdc Max. @ 10 mAdc, 1.72 Vdc Min. @ 0.10 mAdc in either direction with 45 amp pulse test.	RD
107A	P-76	R	Symmetrical germanium fractional voltage limiter	RD
416C	P-22	R	Two 405's with overall NF = 10 dB max.	RD

P = Preferred ♠ Matched Pair - Unmounted ♠5 This rating applied to the pair. ▲5 R_S = 3.0 ohms max. @ V = 0.

R = Restricted (Check use with Device Engineer) ♠6 Applies for each diode of the pair.

★ With T_C at 25 C. ★6 NF = 7.3 dB Max. @ 3950 MHz. ■ Special vswr requirements.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

MULTIPLE DIODES

Code	Package	Status	Description	Mfg. Location
460A	P-10	P	Epi Si full-wave bridge in single encapsulation. (I_O = .250 Adc max. $V_{(BR)}$ = 200 Vdc min. at I_R = 10 μAdc)	RD
460B	P-10	P	Epi Si full-wave bridge in single encapsulation. (I_O = .200 Adc max.; $V_{(BR)}$ = 75 Vdc min. at I_R = 10 μAdc)	RD
460C	P-10 ◆4	R	Four Epi Si Diff diode elements in closed ring modulator configuration.	RD
460D	P-10	P	Epi Si full-wave bridge in single encapsulation.	RD
460E	P-10 ◆4	P	Same as 460C, except carrier leak = 6 mv max. at $i_{(sig)}$ = 15 ma	RD
460F	P-10	P	Same as 460D, except V_F = 1.0 Vdc max. at I_F = 100 mAdc and V (unbal) = ±4 mVdc max.	RD
460G	P-10 ◆5	P	Si full-wave bridge, with surge protector on input side in single encapsulation.	RD
460J	P-10	P	Same as 460F, except different input and output connections.	RD
460K	P-10	P	Same as 460G, except 22V surge protector.	RD
462A	P-8	P	Ge full-wave bridge in single encapsulation. Polarity guard.	RD
462B	P-8	P	Same as 462A, except P_T = 200 mW.	RD
475A	P-10	P	Matched pair of diode elements in a single encapsulation.	RD
475B	P-10	P	Matched pair of diode elements in a single encapsulation.	RD
482A	P-16	P	Eight diode elements with common cathodes in single encapsulation.	RD
482B	P-16	P	Eight diode elements with common anodes in single encapsulation.	RD

P = Preferred ◆4 Lead length is 0.190/0.155 inch. ◆5 Lead length is 0.650/0.550 inch. ◆7 Leads are located in positions 1, 3 & 4.

R = Restricted (Check use with Device Engineer) These diodes have been designed for specific applications. For further information, contact the appropriate Device Engineer.

ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

SPECIAL USE DIODES

Code	Package	Status	Description	Mfg. Location
426N	P-63	R	A68V ± 10% Regulator and 200 V Rectifier back-to-back.	RD
426AA	P-63	R	Variable capacitance diode, C = 800 - 1000 pF @ V_R = 1.0 Vdc	RD
426AN	P-63	P	Symmetrical surge protector, ± 18 volt limiter	RD
426AU	P-63	R	A 7.5 to 7.7 Vdc temperature compensated voltage regulator	RD
446P	P-39	P	Variable capacitance diode, C = 28 pF @ V_R = 4.0 Vdc	RD
446AA	P-39	P	Low capacitance diode	RD
446AB	P-39	R	Same as 446F except i_f (surge) = 30 A for 1 ms	RD
446AC	P-39	R	Same as 446T except 100% life tested for 1000 hours	RD
446AE	P-39	P	Symmetrical surge protector, ± 19.5 volt limiter	RD
446AF	P-39	P	Symmetrical surge protector, 18 volt ± 10% limiter	RD
446AG	P-39	R	Same as 446E, except additional noise requirement	RD
446AH	P-39	R	Symmetrical surge protector, 200 volt ± 10% limiter	RD
446AJ	P-39	R	Symmetrical surge protector, ± (6.55 to 7.25) volt limiter	RD
446AK	P-39	R	A 15V ± 5% Regulator intended for use as noise source.	RD
457A	P-30	R	Variable capacitance diode (High Q), C = 16 pF @ V_R = 5.0 Vdc	RD
457F	P-62	R	Series connected pair, $V_{(BR)}$ = 15.1 to 15.5 Vdc @ I_R = 10 mAdc	RD
474A	P-9	P	PIN Variolosser Diode in TO-18 type package	RD
476A to AK	P-24	R	Same as 446A to AK except electrically insulated body 476A – 0.410 476F – 0.411 476T – 0.543 476AL – 1.66 476B – 0.523 476K – 0.387 476AB – 0.464 476E – 0.469 476M – 0.484 476L – 0.491	RD
479A	P-7	R	Silicon ESBAR diode in three leaded package, $V_{(BR)}$ = 10 Vdc @ I_R = 10 μAdc	RD
479B	P-7	R	Silicon ESBAR diode in three leaded package, $V_{(BR)}$ = 20 Vdc @ I_R = 10 μAdc	RD
485S	P-36	R	A 250 V controlled charge switch, t_s = 3.5 μsec min., 5.0 μsec max. and t_f = 0.5 μsec max. @ I_F = I_R = 1.5 Adc	RD
485AD	P-36	R	Variable capacitance diode, C = 1378 = 1522 pF @ V_R = 7.0 Vdc, $V_{(BR)}$ = 15 Vdc min. at 50 mAdc	RD
485AJ	P-36	P	A 250 V controlled charge switch, t_s = 1.75 μsec min., 2.5 μsec max. and t_f = 0.25 μsec max. @ I_F = I_R = 1.5 Adc	RD
511A ■9	P-9	P	Ion-implanted, hyper-abrupt junction diode Vm* = 3.0 to 5.0 Vdc, Cm* = 7.0 to 9.0 pF, m* = 2.5 to 4.0	RD
511B ■9	P-9	P	Ion implanted, hyper-abrupt junction diode, C = 40 pF min. @ V_R = 0.1 Vdc & 5 pF max. @ V_R = 4.0 Vdc	RD
514A	P-9	R	Symmetrical surge protector ± 22.0 V ± 10% limiter.	RD

P = Preferred ◆4 Lead length is 0.190/0.155 inch. ◆5 Lead length is 0.650/0.550 inch. ◆7 Leads are located in positions 1, 3 & 4.

R = Restricted (Check use with Device Engineer) These diodes have been designed for specific applications. For further information, contact the appropriate Device Engineer.

■9 Epitaxial Schottky barrier

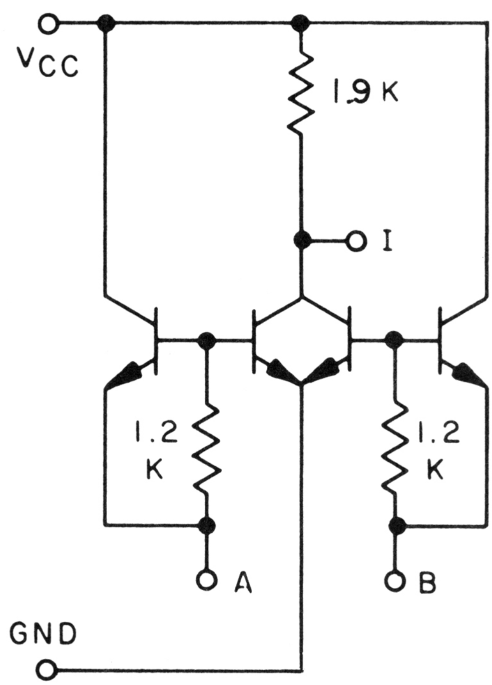
ABOVE QUICK SELECTION DATA NOT TO BE USED FOR CIRCUIT DESIGN—USE OFFICIAL DATA SHEET.

DEVICE CHARACTERISTICS

DIGITAL INTEGRATED CIRCUITS RTL (4.0V)

The RTL series is a family of resistor-transistor logic or direct-coupled-transistor logic available in 16-pin Dual Inline Packages and Ceramic Flatpacks. Input unit load is 300u amps. Noise margin is 500m volts. Logic "one" is 1.22V and logic "zero" is 0.25V (V_{cc} = 4.0V).

Basic Gate Schematic



DIGITAL INTEGRATED CIRCUITS RTL (4.0V)

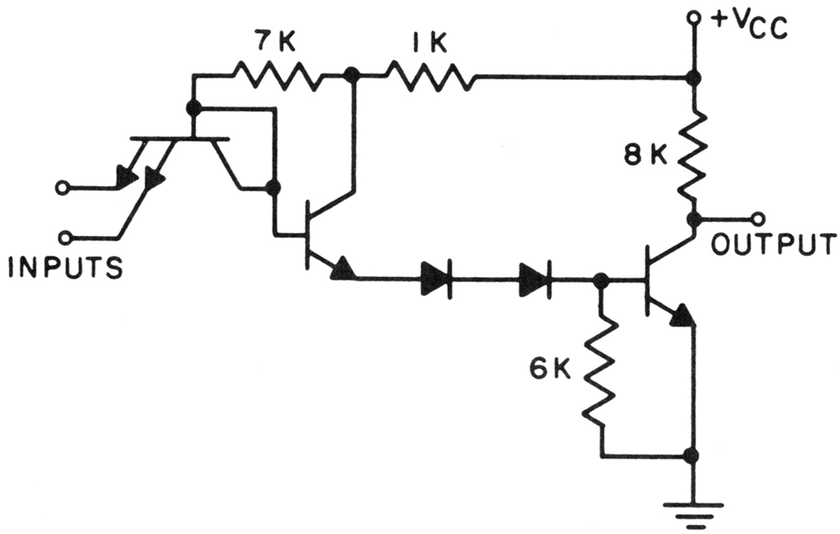
CODE		Description	Dia.	Fan Out	Avg. Prop Delay (nS)	Power Diss (mW)	Mfg. Location
Flat-pack	DIP						
1J	-	Replaced by 1N*					AL
1K	-	Replaced by 1P*					AL
1L	-	Replaced by 1R*					AL
1M	-	Replaced by 1S*					AL
1N	41AK	Quad 2 Input NOR	6	3	7	25	AL
1P	41AL	Dual 2-IN Driver	7	55	21	40	AL
1R	41AM	Dual Type D F/F	8	3	32	85	AL
1S	41AN	Dual Toggle F/F	9	3	32	85	AL
1W	41BH	Dual Exclusive NOR/OR	10	3	17	20	AL
1Y	41CP	Same as 1J	6	3	7	25	AL

*Not Recommended for New Designs

DIGITAL INTEGRATED CIRCUITS DTL (5.0V)

The DTL series is a family of medium-power, low-speed diode-transistor logic I.C.'s available in 16-lead Dual Inline Packages and Ceramic Flatpacks. Logic "one" is 2.4V and logic "zero" is 1.65V. Input unit load is 750ua (V_{cc} ± 5.0V). Noise margin is 1.0 volt. Near-equivalent 4.5 volt circuits are also available, but the 5 volt family is preferred for new design.

Basic Gate Schematic



DIGITAL INTEGRATED CIRCUITS DTL (5.0V & 4.5V)

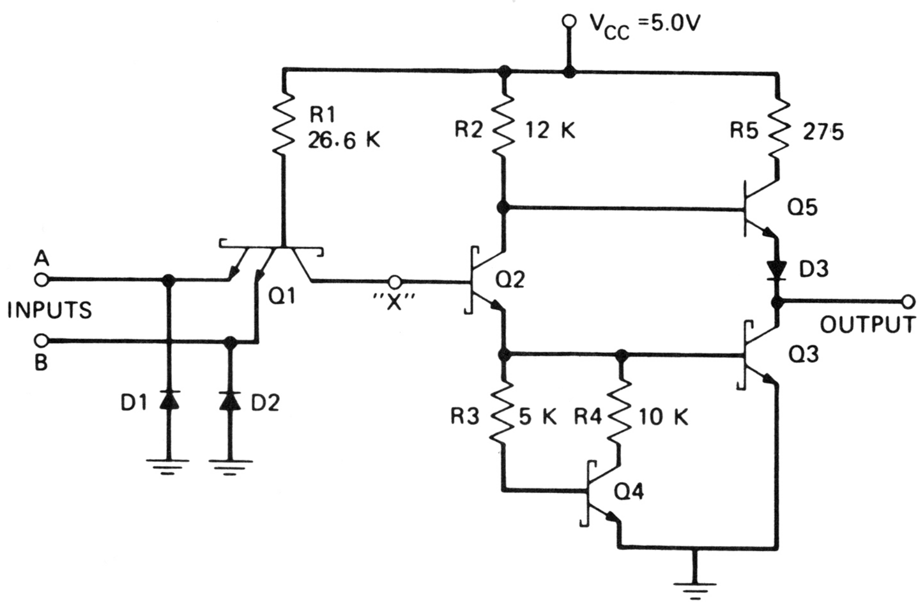
CODE								
4.5V Flat	5.0V Flat	5.0V DIP	Description	Dia.	Fan Out	Avg. Prop Delay (nS)	Total Power Diss (mW)	Mfg. Location
1E	1AJ	41AU	Triple (2-4-5 In)Nand	4	5	120	30	AL
1F	1AR	41AW	Expandable Nand	5	5	120	10	AL
1AA	1AL	41BA	Dual High F.O. Gate	11	50	120	71	AL
1AB	1AS	41BE	Dual Relay Driver	12	See Dia.	-	29	AL
1AC	1AM	41BB	Clocked J-K F/F	13	5	200KHz	72	AL
1AD	1AN	41BC	One-Shot	14	5	-	32	AL
1AE	1AP	41BD	Pulse Delay	15	5		44	AL
1AF	1AT	41BF	Dual Multiplying Gate	17			32	AL
1AG	1AK	41AY	Quad (2-2-2-3 In)Nand	16	5	120	40	AL

DEVICE CHARACTERISTICS

DIGITAL INTEGRATED CIRCUITS TTL(L) 5.0V

The TTL(L) series is a family of low-power, low-speed Schottky-clamped transistor logic I.C.'s available in 16-lead Dual Inline Packages. Input unit load is 240ua. Noise margin is 400mv. Logic "one" is 2.4V and logic "zero" is 0.4V (V_{cc} = 5.0V). All unused inputs should be connected to logic "one".

Basic Gate Schematic



DIGITAL INTEGRATED CIRCUITS TTL(L) 5.0V

Code	Description	Dia.	Fan Out	Avg. Prop Delay (nS)	Total Power Diss (mW)	Mfg. Location
41N	Quad (2-2-3-3) Input Nand	18	10	30	6	AL
41P	Quad (1-1-4-4) Input Nand	23	10	30	6	AL
41R	Dual 2 Wide-3 In A.O.I.	19	10	40	4.6	AL
41S	Dual J-K Flip Flop	24	10	3 MHz	14	AL
41T	8-BIT Shift Register	38	9	3 MHz	67	AL
41AC	Quad 2-Input Nand (O.C.)	20	10	60	6	AL
41AF	Dual 8-4 Input Nand	22	10	40	3	AL
41CB	Quad Type D Flip Flop	39	10	3 MHz	35	AL

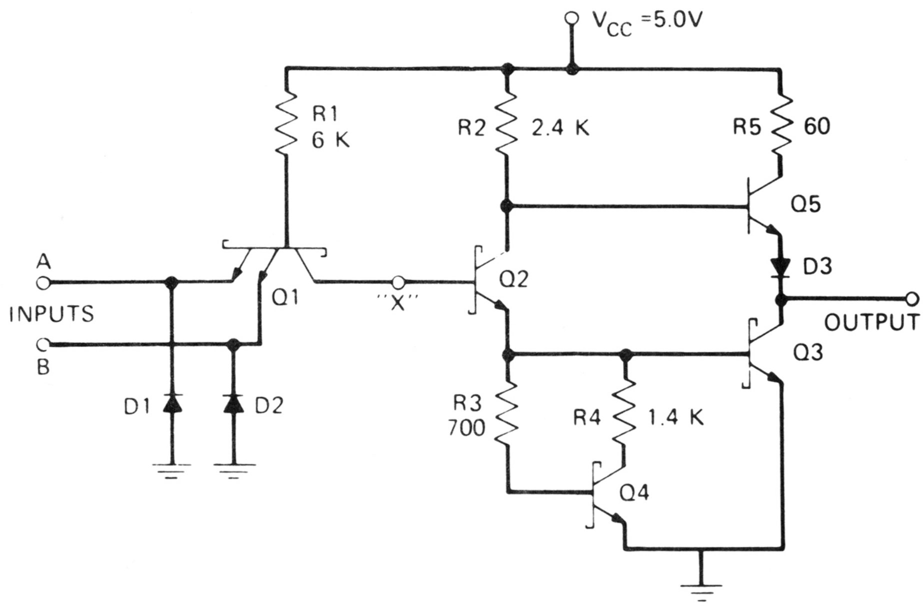
O.C. = Open Collector (See Data Sheet)

DEVICE CHARACTERISTICS

DIGITAL INTEGRATED CIRCUITS TTL(M) 5.0V

The TTL(M) series is a family of medium-power, medium-speed Schottky-clamped transistor-transistor logic I.C.'s available in 16-lead Dual Inline Packages. Input unit load is 980ua. Noise margin is 400mv. Logic "one" is 2.4V and logic "zero" is 0.4V (V_{cc} = 5.0V). All unused inputs should be connected to logic "one".

Basic Gate Schematic



DIGITAL INTEGRATED CIRCUITS TTL(M) 5.0V

Code	Description	Dia.	Fan Out	Avg. Prop Delay (nS)	Total Power Diss (mW)	Mfg. Location
1A	Dual 5-Input Gate*	1	12	14	50	AL
1B	Quad (2-2-3-3) Input Gate*	2	12	14	100	AL
1C	J-K Flip Flop*	3	12	25	100	AL
41U	Quad (2-2-3-3) Input Nand	18	10	8.5	30	AL
41W	Quad (1-1-4-4) Input Nand	23	10	8.5	30	AL
41Y	Dual 2 Wide-3 In A.O.I.	19	10	9.0	21	AL
41AA	Dual 8-4 Input Nand	22	10	12.0	15	AL
41AB	Dual J-K Flip Flop	24	10	20 MHz	60	AL
41AD	Quad 2-Input Nand (O.C.)	20	10	11.5	30	AL
41AE	Dual Type D Flip Flop	21	10	20 MHz	65	AL

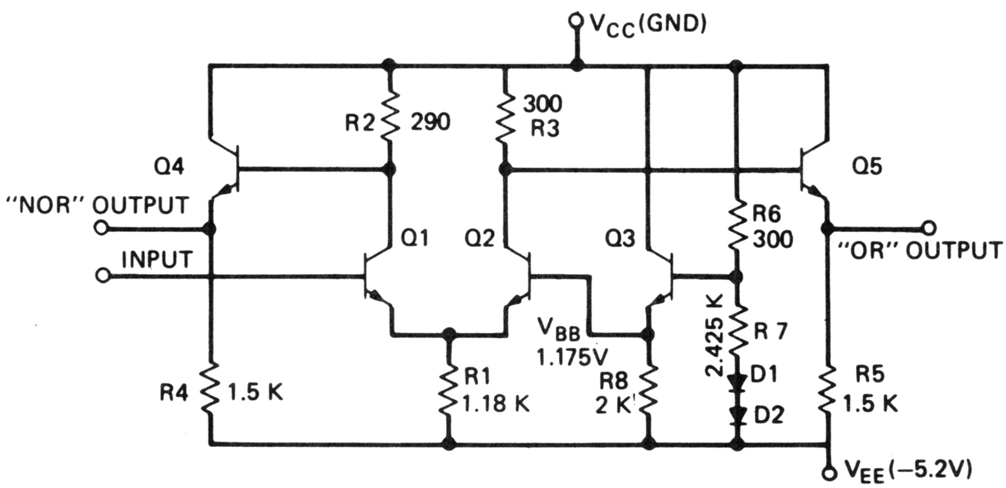
* = Flatpacks Only

O.C. = Open Collector (See Data Sheet)

DIGITAL INTEGRATED CIRCUITS ECL(−5.2V)

The ECL series is a family of high-speed, emitter-coupled logic I.C.'s available in 14-lead Dual Inline Packages. Input unit load is 100ua. Noise margin is 175mv. Logic "one" is −0.75V and logic "zero" is −1.6 volts when V_{cc} is at ground (V_{EE} = −5.2V). All unused inputs should be tied to V_{EE}, except the 101M, where unused inputs should be tied to V_{cc}.

Basic Gate Schematic



DIGITAL INTEGRATED CIRCUITS ECL (−5.2V)

Code	Description	Dia.	Fan Out	Avg. Prop Delay (nS)	Total Power Diss (mW)	Mfg. Location
101A	Quad 2-Input NOR	25	25	4.5	140	AL
101B	Triple 3-Input NOR	26	25	4.0	135	AL
101C	Dual 4-Input OR/NOR	27	25	4.0	95	AL
101D	Six-Input 3-OR, 3-NOR	28	25	4.0	115	AL
101E	Triple Diff. Amp.	29	25	5.0	140	AL
101F	Quad Line Receiver	30	25	4.0	115	AL
101G	J-K Flip Flop	31	25	6.0	125	AL
101H	Quad Exclusive OR	32	25	5.0	130	AL
101J	Quad Exclusive NOR	33	25	5.0	130	AL
101K	Full Adder	37	25	8.0	145	AL
101L	Dual R-S Flip Flop	34	25	6.0	140	AL
101M	Sat. Logic to ECL	35	25	15.0	150	AL
101N	ECL to Sat. Logic	36	10*	19.0	55	AL
101P	Quad 2-In NOR (N.R.)	25	25	4.5	65	AL
101R	Triple 3-In NOR (N.R.)	26	25	4.0	60	AL
101S	Dual 4-In OR/NOR (N.R.)	27	25	4.0	45	AL

* = TTL(M) Unit Load

(N.R.) = No Pulldown Resistor

LINEAR INTEGRATED CIRCUITS — COMPARATORS

Code	Package	Description	Mfg. Loc.
1AH	16 FLAT	Differential Voltage Comparator (High Speed)	AL
41K	16 DIP	Comparator (High Output Swing)	AL
41AH	16 DIP	Differential Voltage Comparator (High Speed)	AL
F-58465	16 DIP	Comparator (High Output Swing)	AL

Note 1: Leading Number in Package Column indicates number of Leads on Package.

Note 2: Detailed Information on the Above Linear Integrated Circuits has not been included in this Guide because of the complexity of these circuits. The official data sheets should be consulted for all pertinent information.

LINEAR INTEGRATED CIRCUITS – AMPLIFIERS

Code	Package	Description	Mfg. Loc.
1T	16 FLAT	Operational Amplifier (Minimum Offset)	AL
1U	16 FLAT	Operational Amplifier (50 MHz)	AL
41A	16 DIP	Operational Amplifier (High-Swing)	RD
41B	16 DIP	Operational Amplifier (High-Swing)	RD
41C	16 DIP	Operational Amplifier (High-Swing)	RD
41E	16 DIP	Operational Amplifier (High-Swing)	RD
41AJ	16 DIP	Operational Amplifier (Minimum Offset)	RD
41AR	16 DIP	Clock Extraction Circuit and Limiting Amplifier	AL
41AT	16 DIP	Line Receiver (Differential Input)	AL
41BJ	16 DIP	Operational Amplifier (Wide Band, Minimum Offset)	AL
46A	10 FLAT	Operational Amplifier (High Input Impedance)	AL
53A	TO 74	Power Amplifier (Speaker Driver)	RD
53B	TO 74	Power Amplifier (Ringing and Tone Plant)	RD
53C	TO 74	Power Amplifier (Speaker Driver)	RD
502A	16 DIP	Operational Amplifier (Voice Frequency)	RD
502B	16 DIP	Operational Amplifier (Voice Frequency)	RD
502F	16 DIP	Dual Operational Amplifier (Voice Frequency)	RD
502H	16 DIP	Dual Operational Amplifier (Voice Frequency)	RD
502S	16 DIP	Operational Amplifier (General Purpose)	RD
502T	16 DIP	Operational Amplifier (General Purpose)	RD
502U	16 DIP	Operational Amplifier (Low Supply Voltage)	RD
502W	16 DIP	Operational Amplifier (Internal Compensation)	RD
502Y	16 DIP	Operational Amplifier (Internal Compensation)	RD
502AK	16 DIP	Operational Amplifier (Internal or External Compensation)	RD
502AL	16 DIP	Operational Amplifier (Internal or External Compensation)	RD
502AM	16 DIP	Operational Amplifier (Internal or External Compensation)	RD
502AN	16 DIP	Operational Amplifier (Internal or External Compensation)	RD
502AR	16 DIP	Dual Operational Amplifier (General Purpose)	RD
503A	TO 76	Operational Amplifier (General Purpose)	RD
503B	TO 76	Operational Amplifier (General Purpose)	RD
532A	18 FLAT	2 Amplifiers and Voltage Regulator	RD
559A	16 DIP	Triple Operational Amplifier (General Purpose)	RD
F-58132	TO 74	Power Amplifier (Speaker Driver)	RD
F-58370	10 FLAT	Operational Amplifier (High Input Impedance)	RD

Note 1: Leading Number in Package Column indicates number of Leads on Package.

Note 2: Detailed Information on the Above Linear Integrated Circuits has not been included in this Guide because of the complexity of these circuits. The official data sheets should be consulted for all pertinent information.

LINEAR INTEGRATED CIRCUITS — REGULATORS

Code	Package	Description	Mfg. Loc.
45A	TO 74	Linear Voltage Regulator (12V)	RD
65A	TO 74	Linear Voltage Regulator (8V)	RD

Note 1: Leading Number in Package Column indicates number of Leads on Package.

Note 2: Detailed Information on the Above Linear Integrated Circuits has not been included in this Guide because of the complexity of these circuits. The official data sheets should be consulted for all pertinent information.

LINEAR INTEGRATED CIRCUITS – MISCELLANEOUS

Code	Package	Description	Mfg. Loc.
36A	14 FLAT	Threshold Detector and Relay Driver	RD
41D	16 DIP	Building Block (6 Transistors)	RD
502C	16 DIP	Three Input Comparator	RD
502D	16 DIP	Oscillator (External R-C Control)	RD
502E	16 DIP	Building Block (5 Transistors)	RD
502G	16 DIP	Building Block (5 Transistors)	RD
502J	16 DIP	Three Input Low Level Comparator	RD
502K	16 DIP	Three Input Low Level Rectifier	RD
502L	16 DIP	JFET Varilosser	RD
502M	16 DIP	Building Block (2 – 6 Diode Arrays; 2 Transistors)	RD
502N	16 DIP	Hybrid, Adder, and Talk-Down	RD
502P	16 DIP	Building Block (3 Darlington Pairs)	RD
502R	16 DIP	Building Block (3 Independent Differential Pairs)	RD
502AJ	16 DIP	Building Block (5 Transistors)	RD
502AS	16 DIP	Building Block (2 Darlington Pairs, 2 Transistors, 3 Diodes)	RD
502AT	16 DIP	Crystal Oscillator (External Crystal, Buffered Output)	RD
F58130	16 DIP	Hybrid, Adder, and Talk-Down	RD
F58131	16 DIP	Rectifier and Noise Guard	RD
F58790	24 DIP	Level Detector (Voltage and/or Current Sensing)	RD
F58935	24 DIP	Pulse Width Modulator (20kHz; 5% to 90%, Duty Cycle)	RD
F58936	24 DIP	Pulse Width Modulator (20kHz; 5% to 90%, Duty Cycle)	RD
F59059	24 DIP	Level Detector (Voltage and/or Current Sensing)	RD

Note 1: Leading Number in Package Column indicates number of Leads on Package.

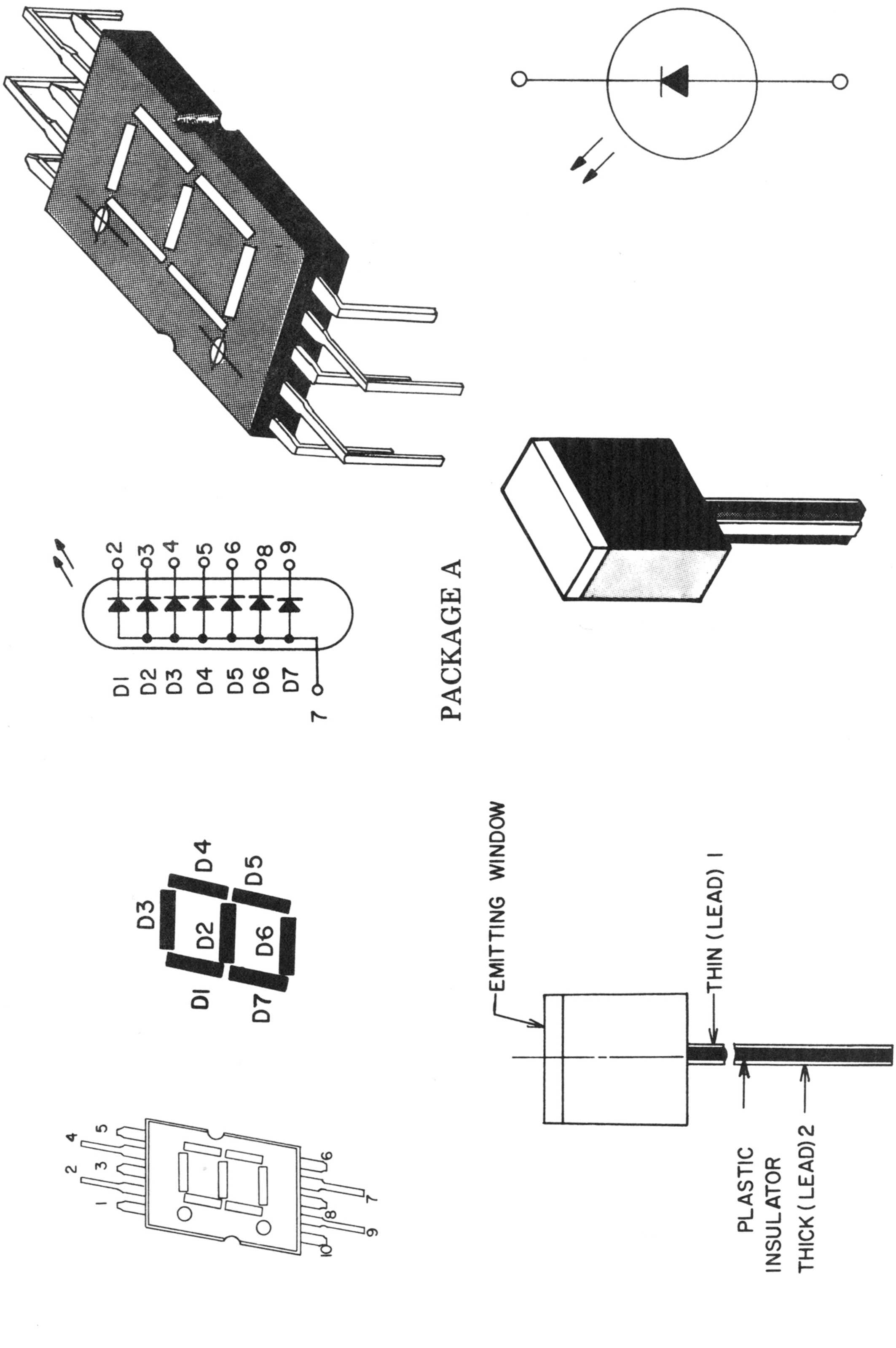
Note 2: Detailed Information on the Above Linear Integrated Circuits has not been included in this Guide because of the complexity of these circuits. The official data sheets should be consulted for all pertinent information.

LIGHT EMITTING DIODES

Code	Package	Description	Color	Output mlm @ IF = 10 ma	Mfg. Loc.
516A	A	7 Bar Numeric Display	Red	1.0	RD
516B	A	7 Bar Numeric Display	Green	1.0	RD
517A	B	Indicating Light	Red	3.0	RD
517B	B	Indicating Light	Green	3.0	RD
519A	C	Indicating Light	Red	4.0	RD
519B	C	Indicating Light	Green	4.0	RD
520A	D	Indicating Light	Red	3.0	RD
520B	D	Indicating Light	Green	3.0	RD

Note 1: Detailed Information on the Above Light Emitting Diodes has not been included in this Guide because of the complexity of these circuits. The official data sheets should be consulted for all pertinent information.

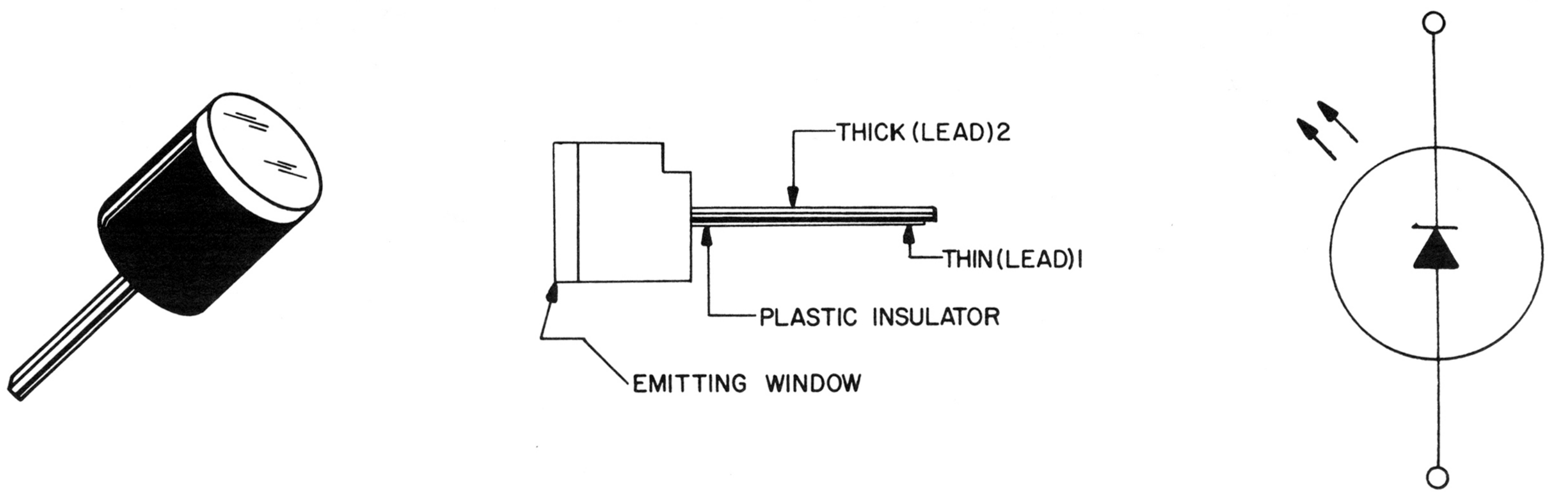
LIGHT EMITTING DIODE PACKAGES



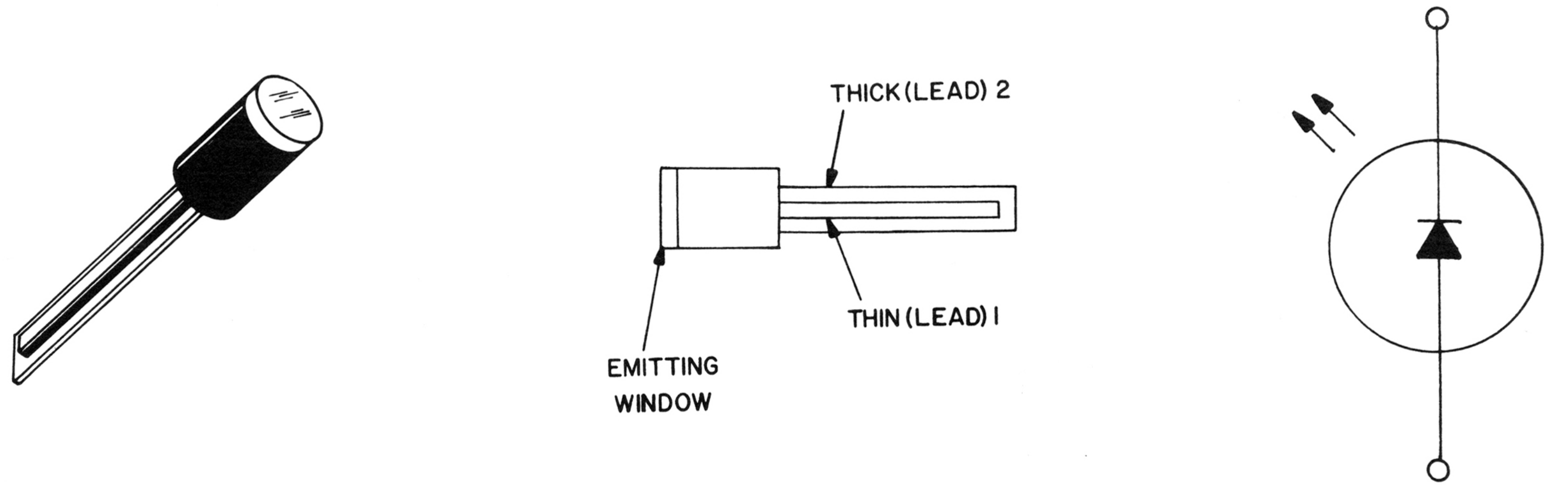
PACKAGE A

PACKAGE B

LIGHT EMITTING DIODE PACKAGES

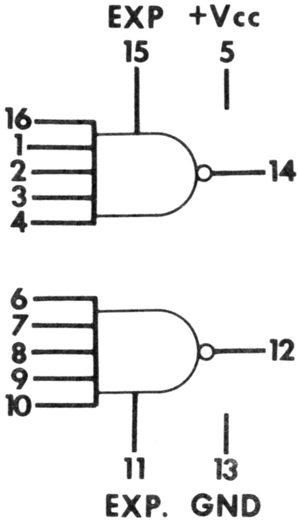


PACKAGE C



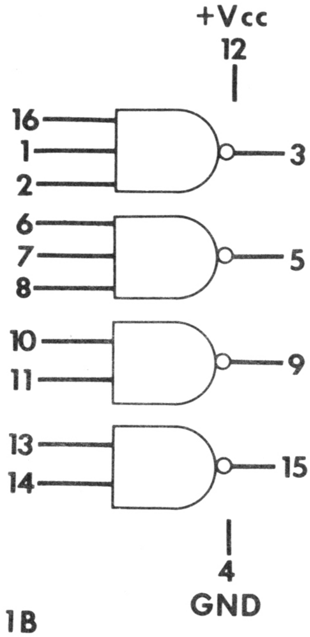
PACKAGE D

DEVICE LOGIC DIAGRAMS



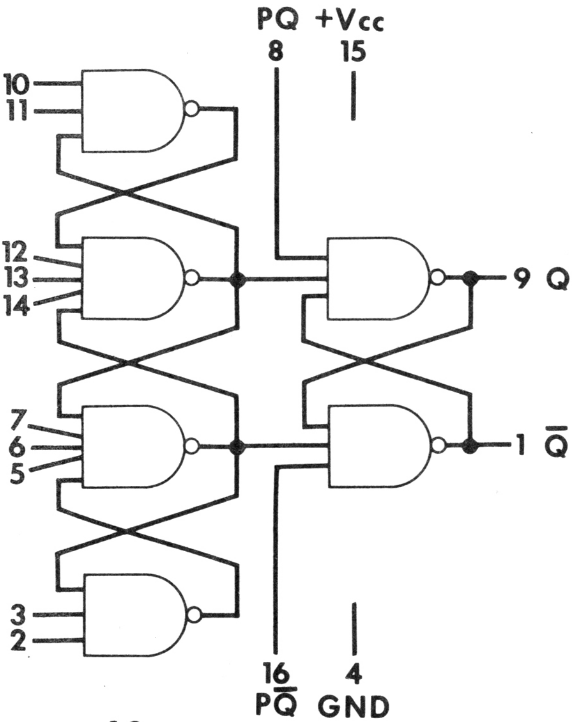
1A

DIA.1



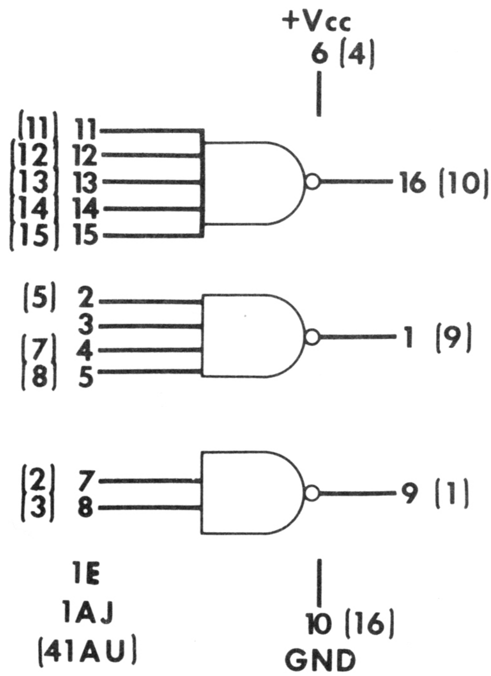
1B

DIA.2

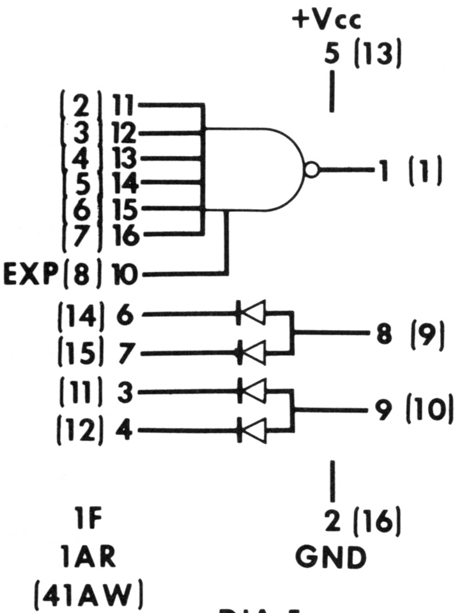


1C

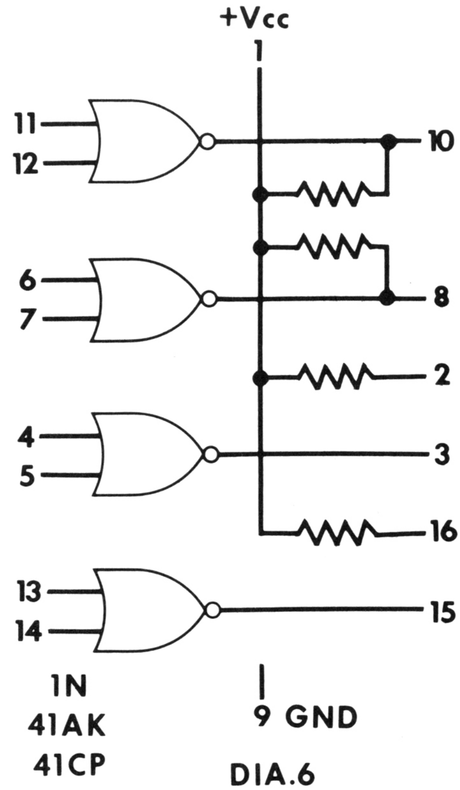
DIA.3



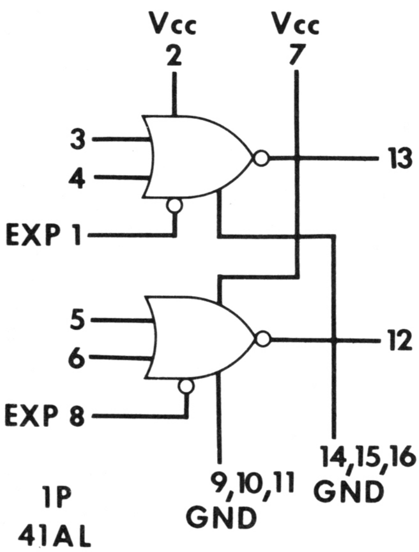
DIA.4



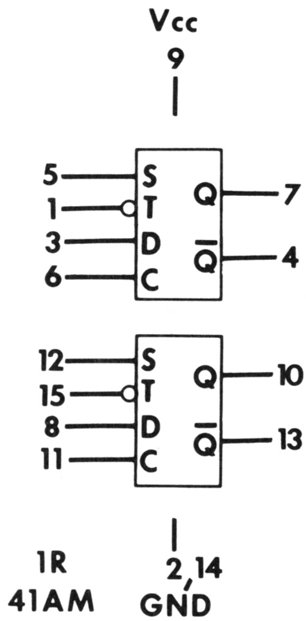
DIA.5



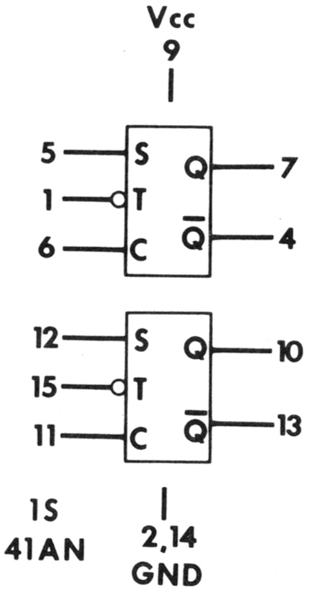
DIA.6



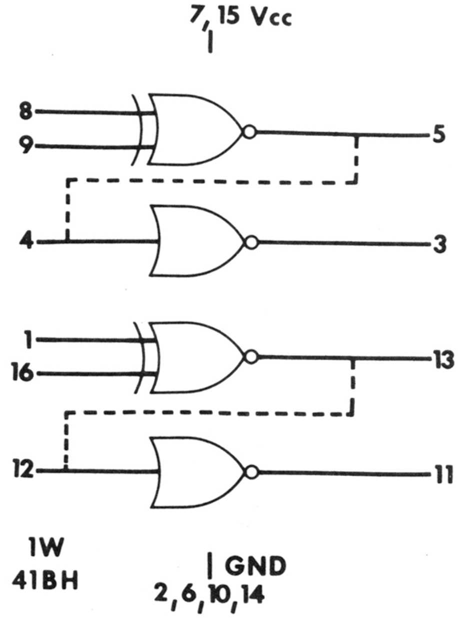
DIA.7



DIA.8

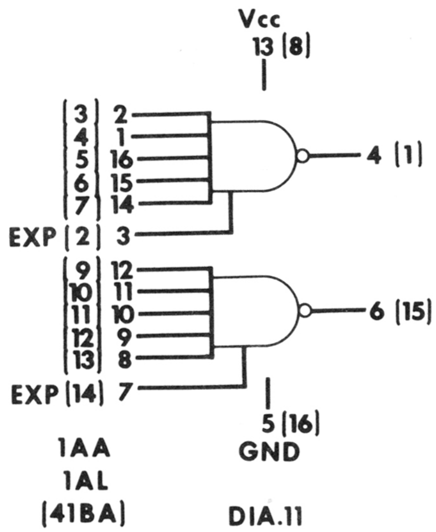


DIA.9

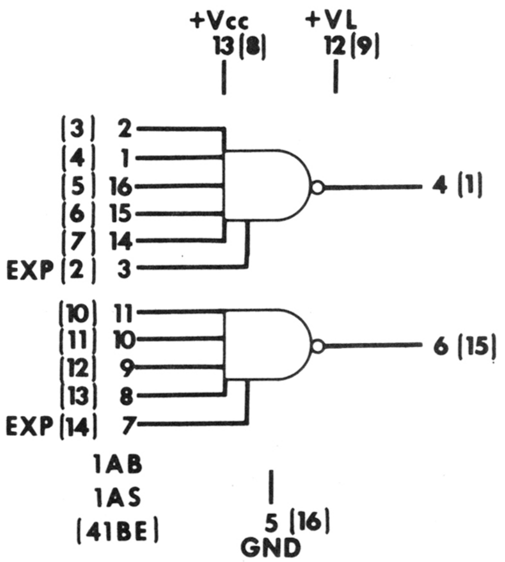


CONNECT DOTTED LINES FOR EX OR

DIA.10



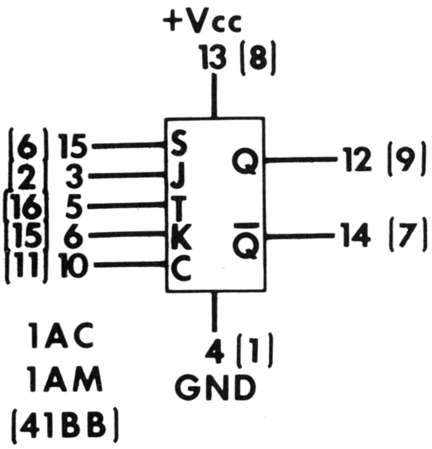
DIA.11



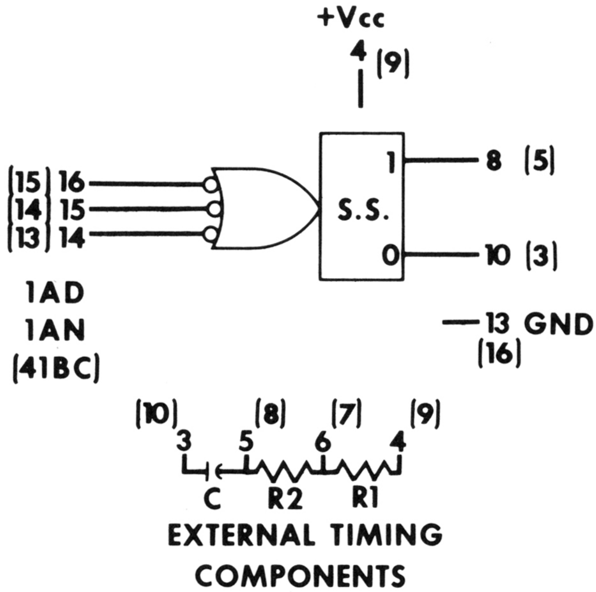
WILL DRIVE 51A LAMP OR BF/BG RELAY

(SEE DATA SHEET)

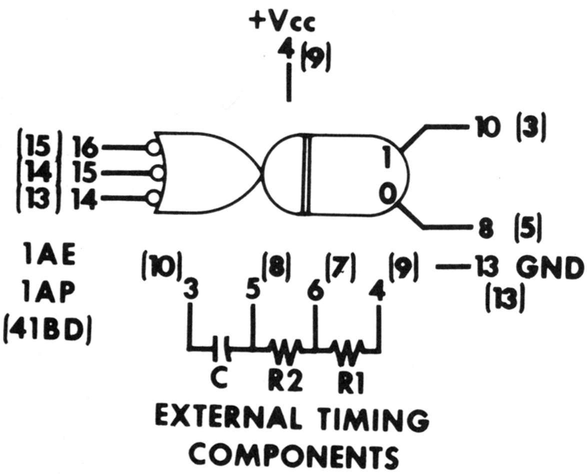
DIA.12



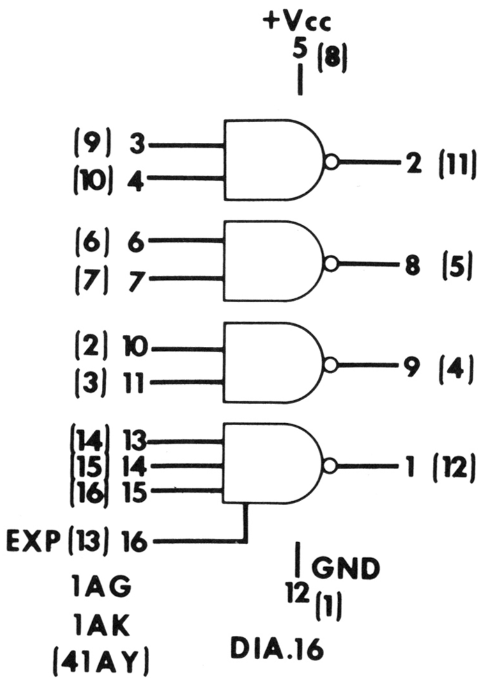
DIA.13



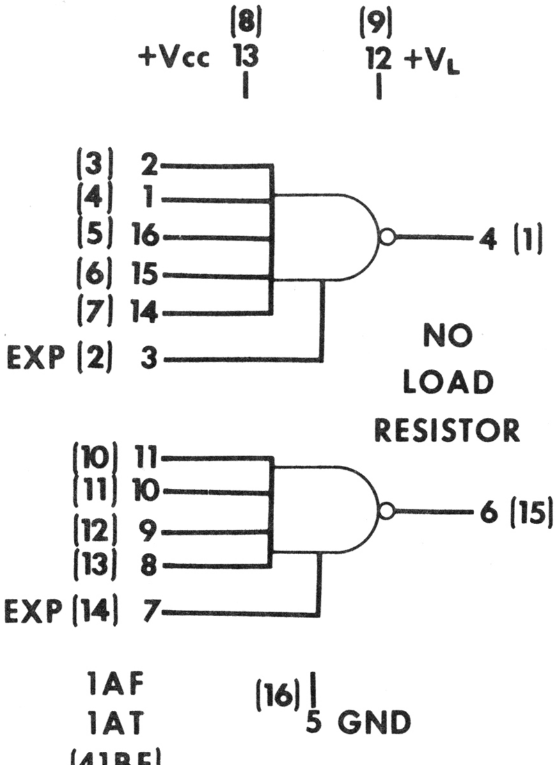
DIA.14



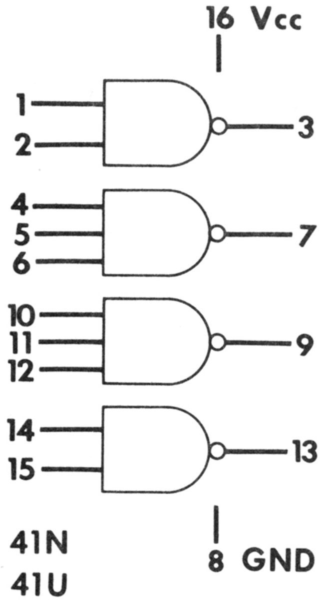
DIA.15



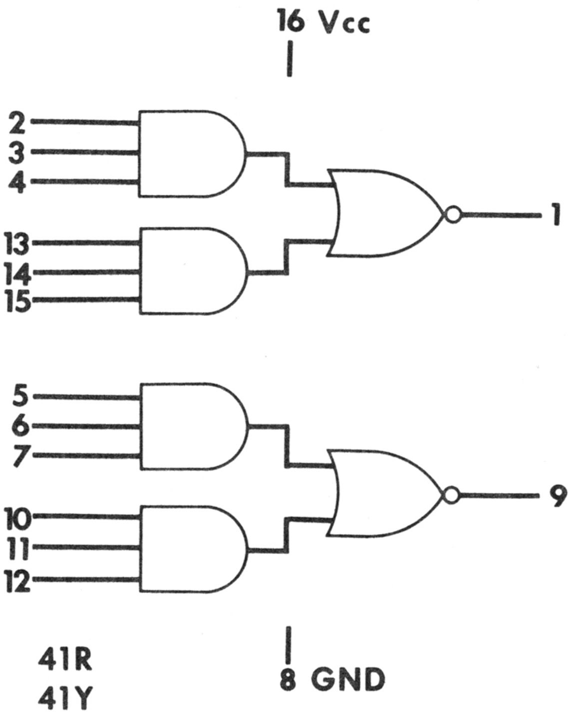
DIA.16



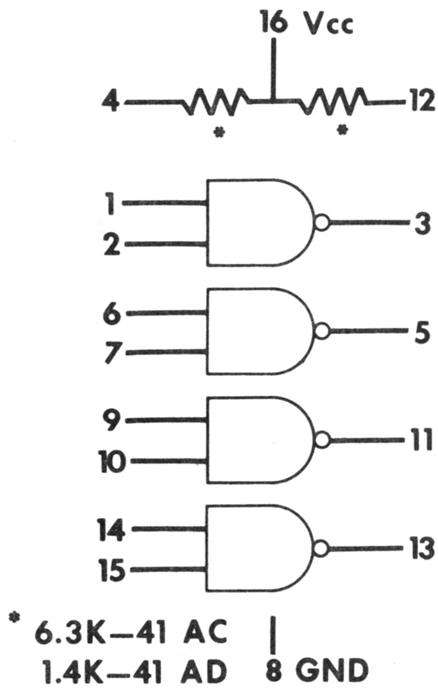
DIA.17



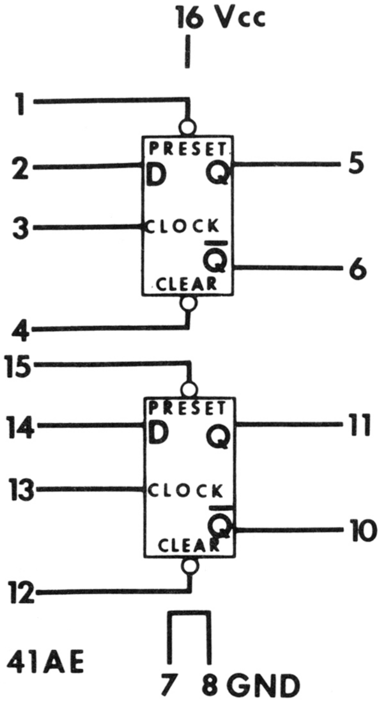
DIA.18



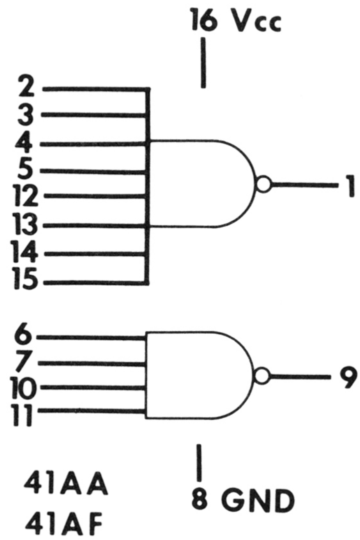
DIA.19



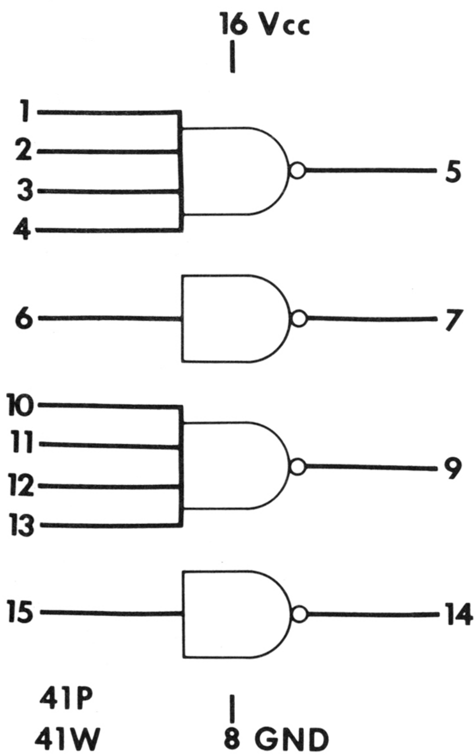
DIA.20



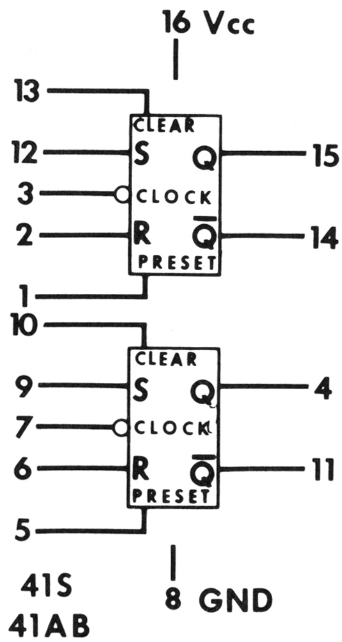
DIA.21



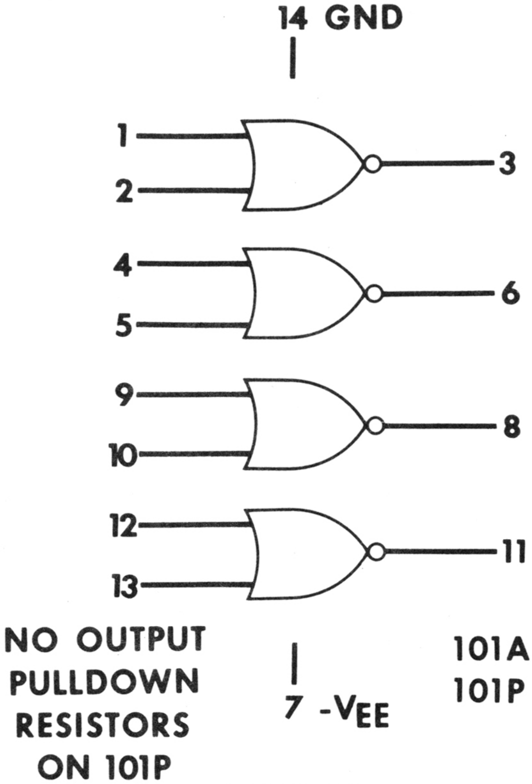
DIA.22



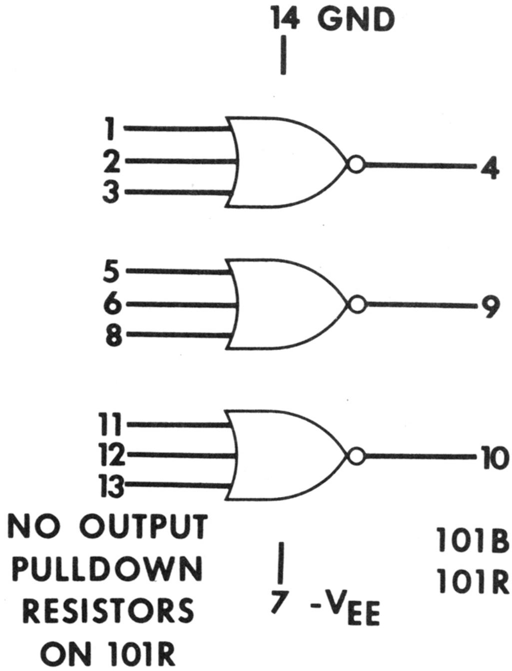
DIA.23



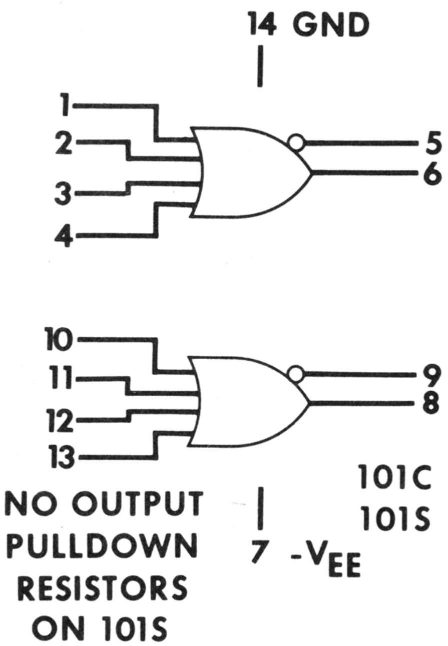
DIA.24



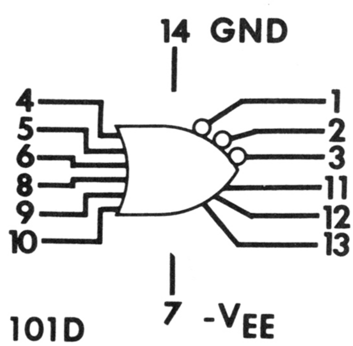
DIA.25



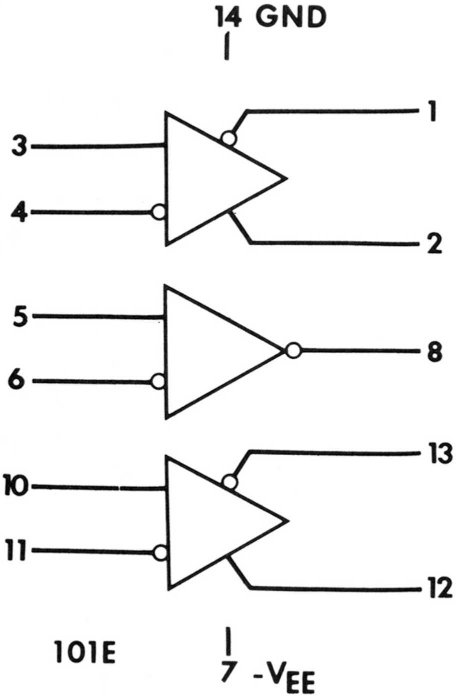
DIA.26



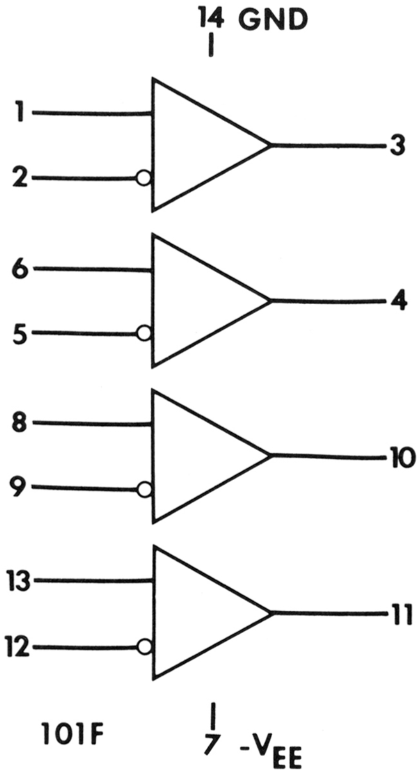
DIA.27



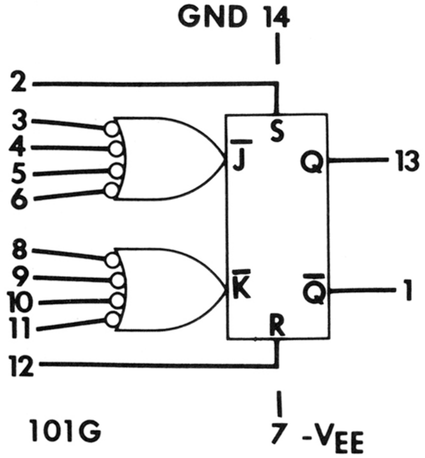
DIA.28



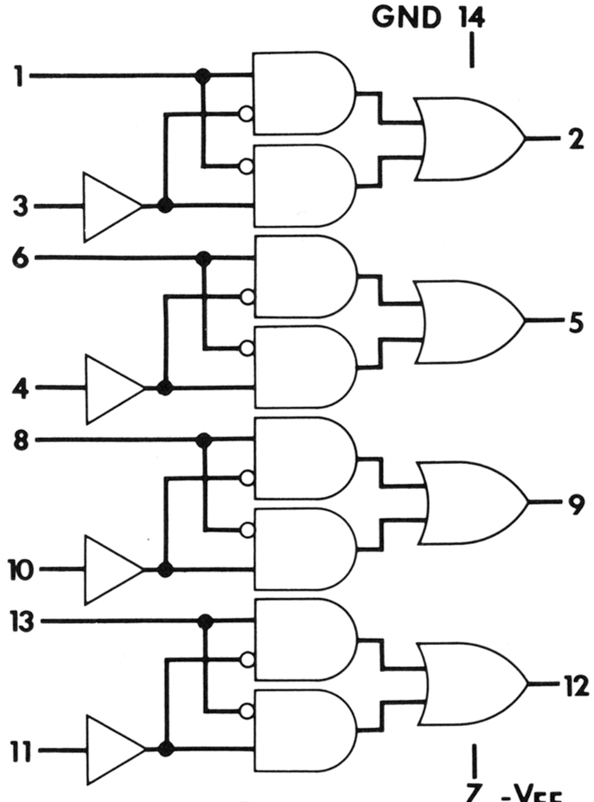
DIA.29



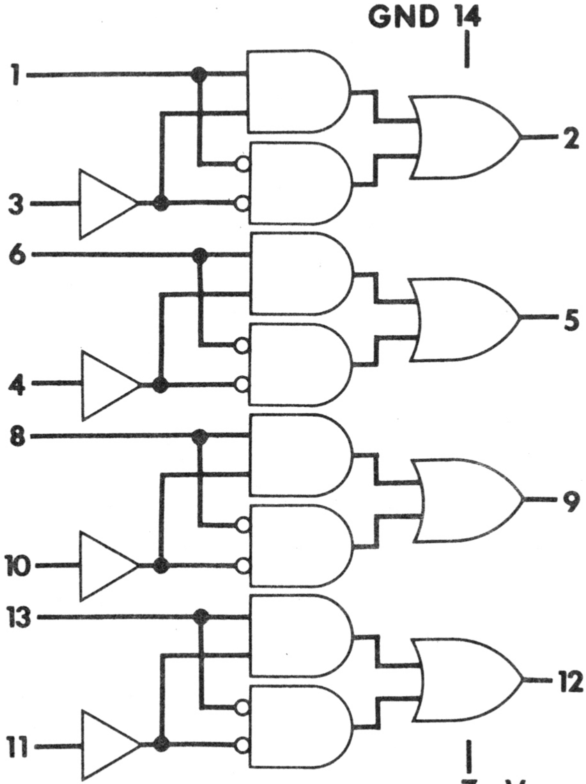
DIA.30



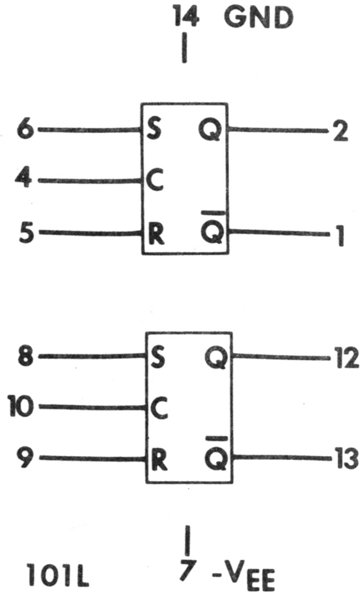
DIA.31



DIA.32

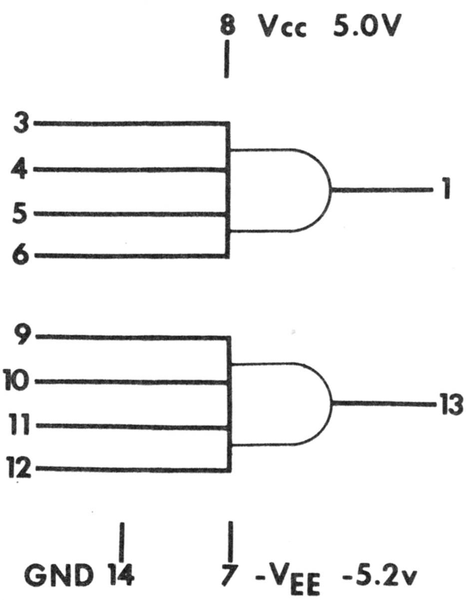


101J DIA.33

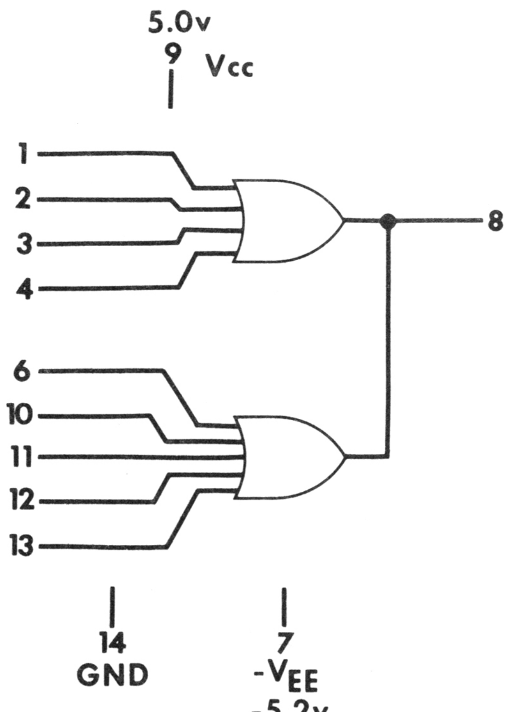


101L

DIA.34

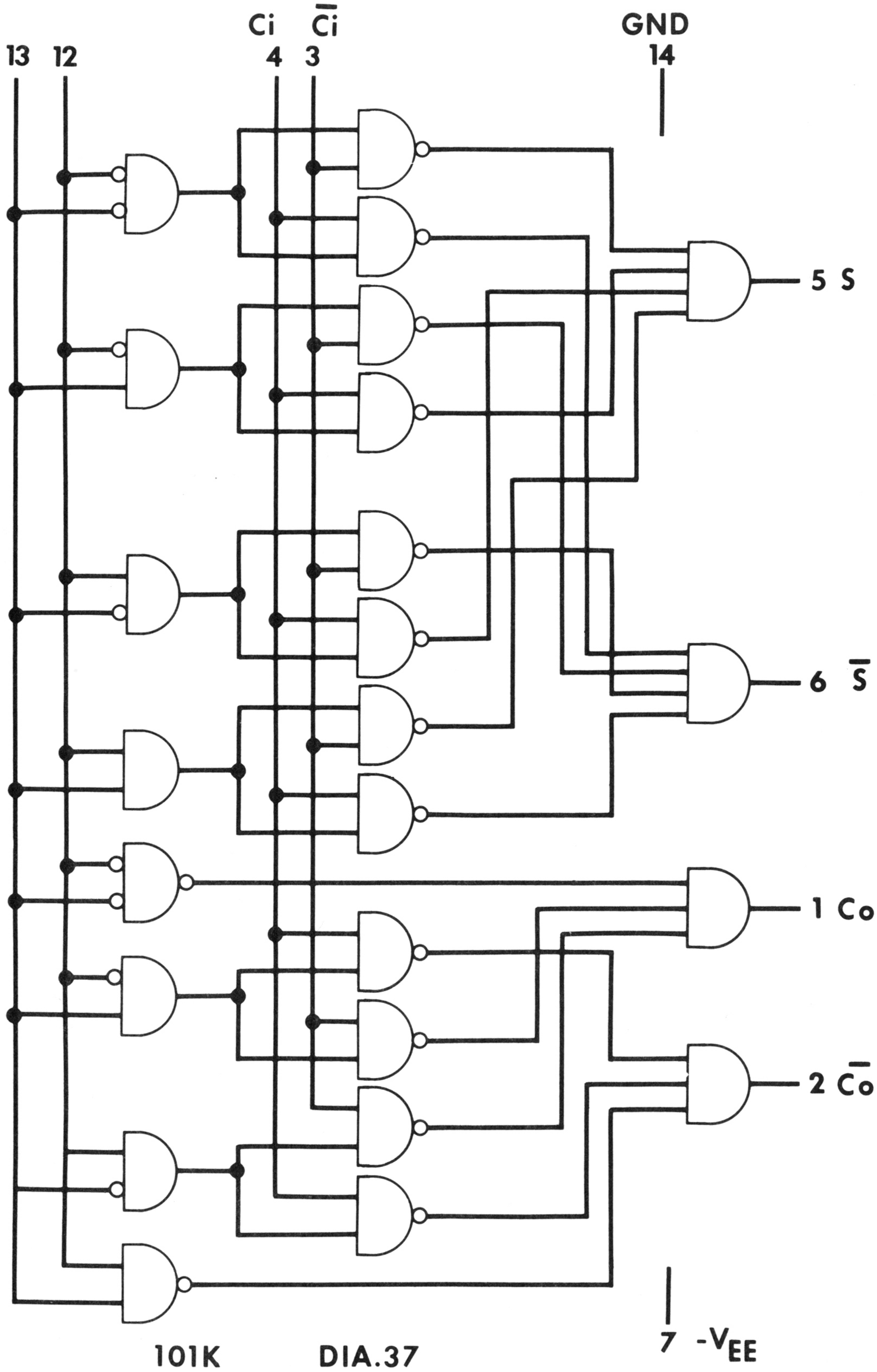


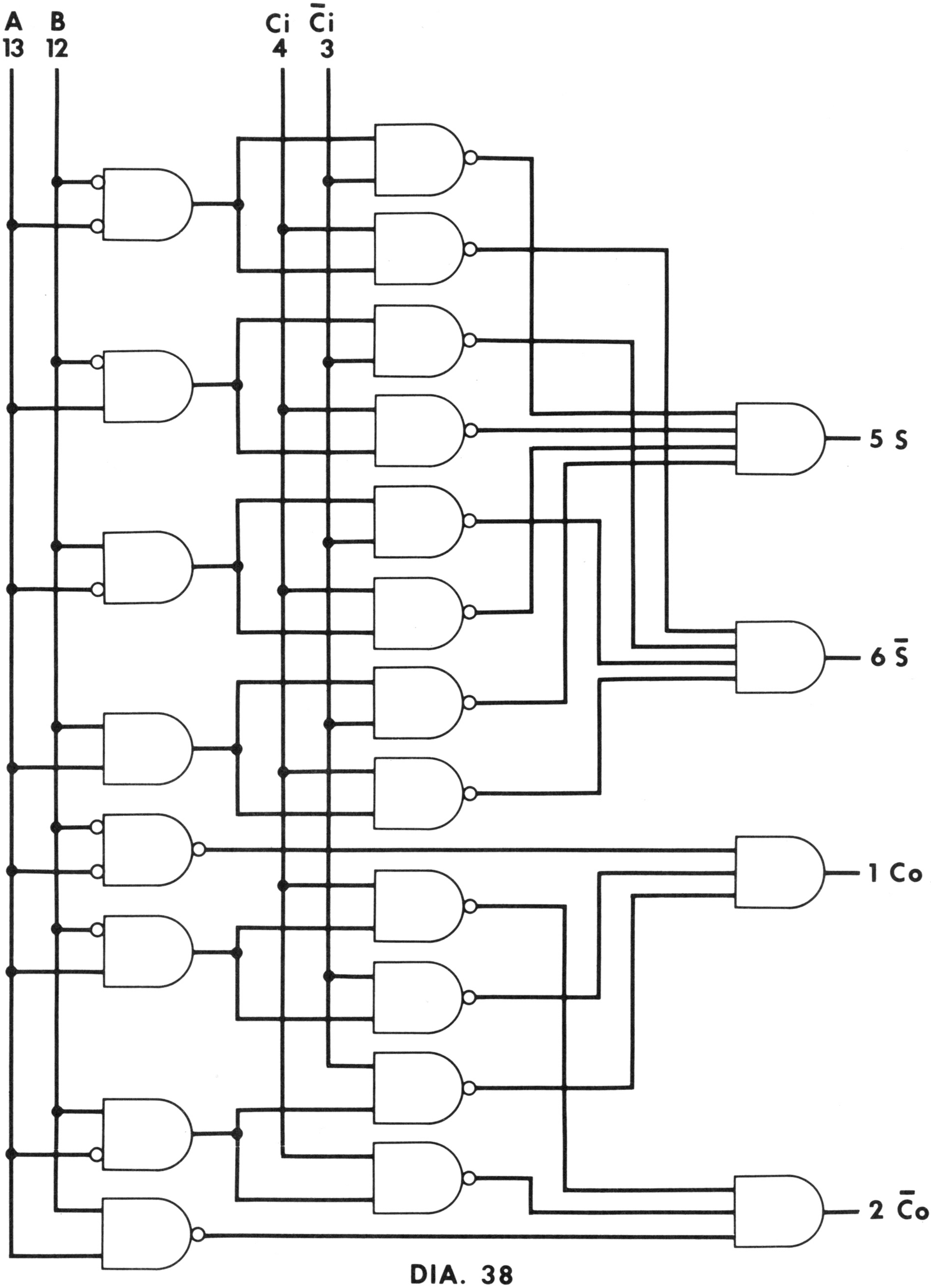
101M DIA.35



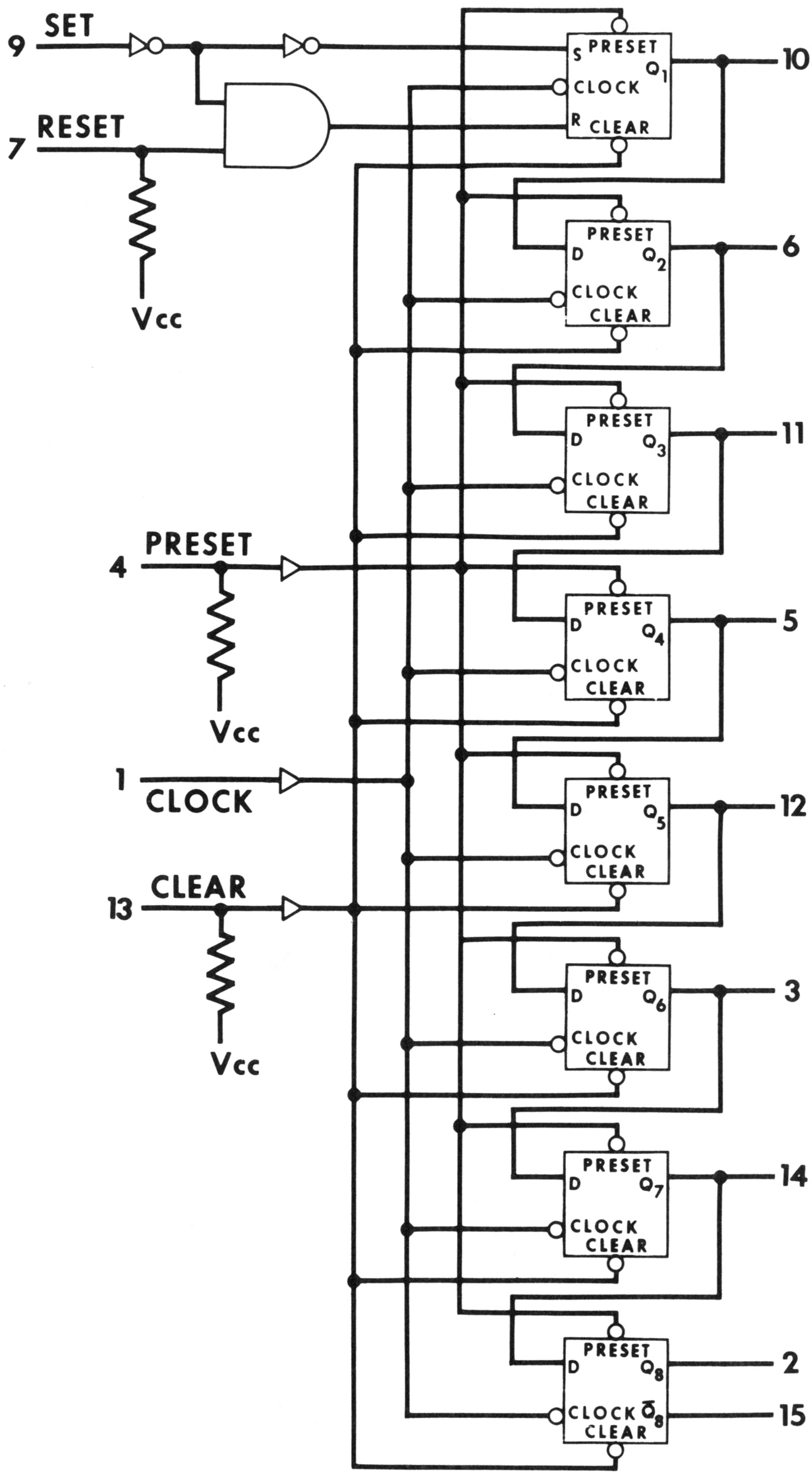
101N

DIA.36

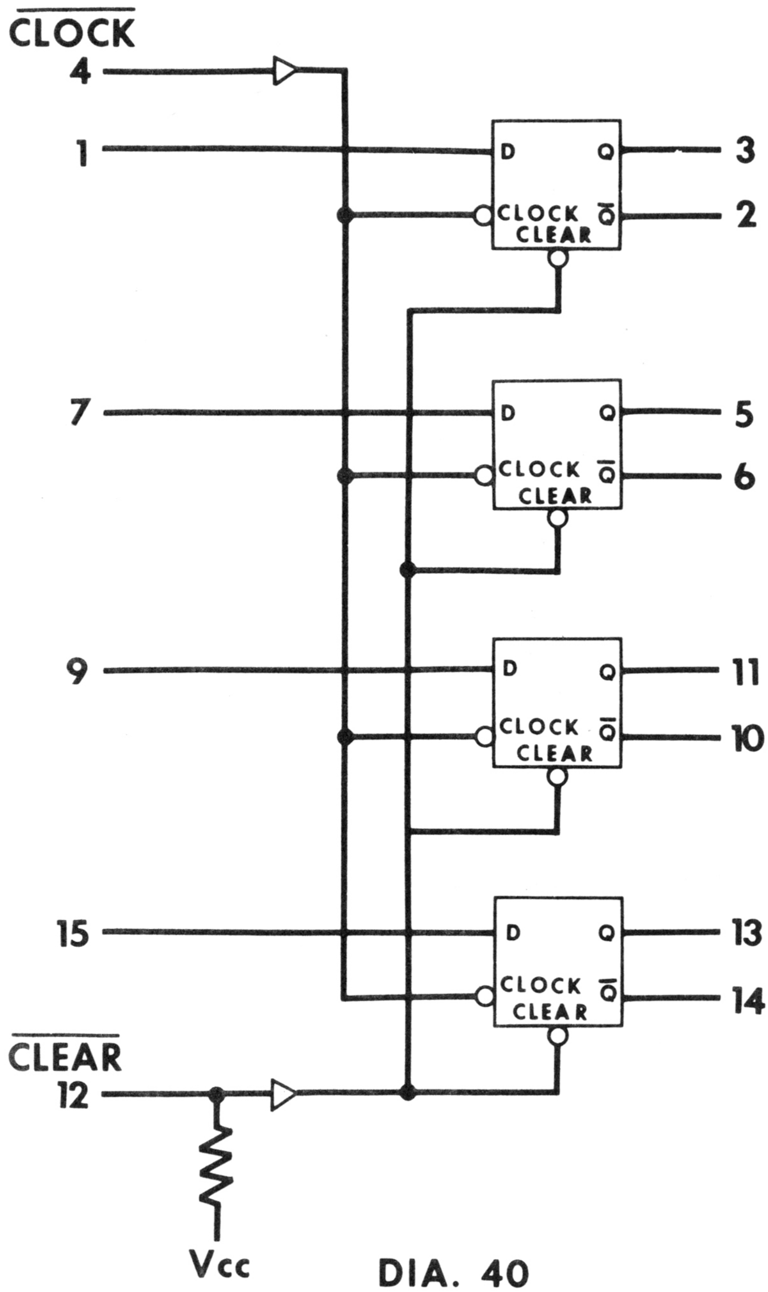

Ci
Ci
GND
13
12
4
3
14
5 S
6 S
1 Co
2 Co
7 -V_{EE}
101K
DIA.37



DIA. 38

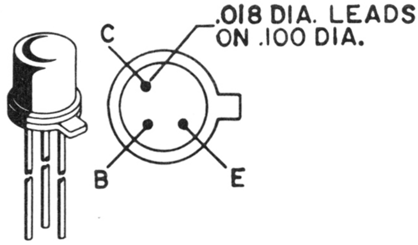

9
SET
7
RESET
Vcc
4
PRESET
Vcc
1
CLOCK
13
CLEAR
Vcc
S PRESET Q1
CLOCK
R CLEAR
10
PRESET
D Q2
CLOCK
CLEAR
6
PRESET
D Q3
CLOCK
CLEAR
11
PRESET
D Q4
CLOCK
CLEAR
5
PRESET
D Q5
CLOCK
CLEAR
12
PRESET
D Q6
CLOCK
CLEAR
3
PRESET
D Q7
CLOCK
CLEAR
14
PRESET
D Q8
CLOCK Q̄8
CLEAR
2
15

DIA. 39

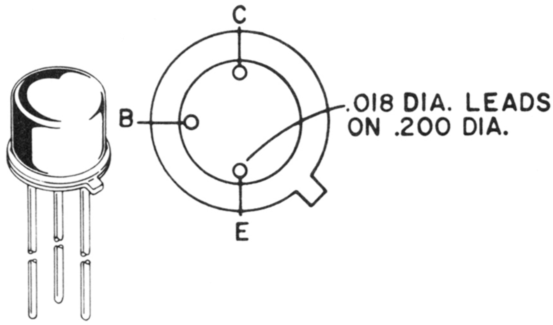

CLOCK
4
1
D
Q
3
CLOCK
Q̄
2
CLEAR
7
D
Q
5
CLOCK
Q̄
6
CLEAR
9
D
Q
11
CLOCK
Q̄
10
CLEAR
15
D
Q
13
CLOCK
Q̄
14
CLEAR
CLEAR
12
Vcc

DIA. 40

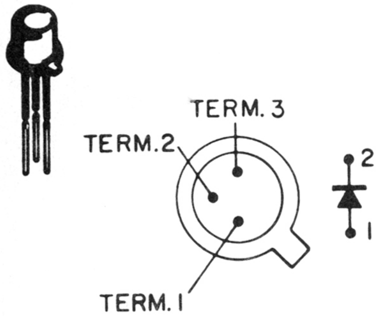
PACKAGE DRAWINGS



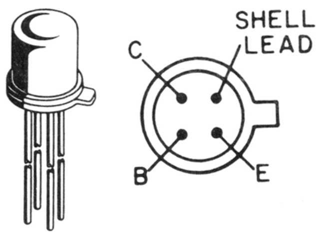
P—1



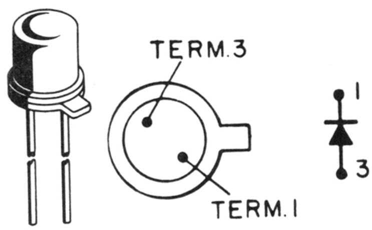
P—6



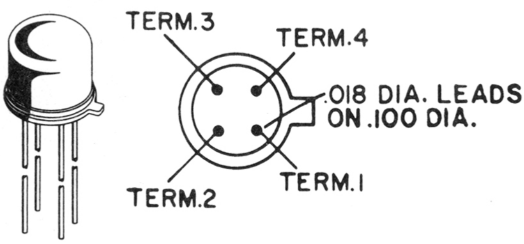
P—7



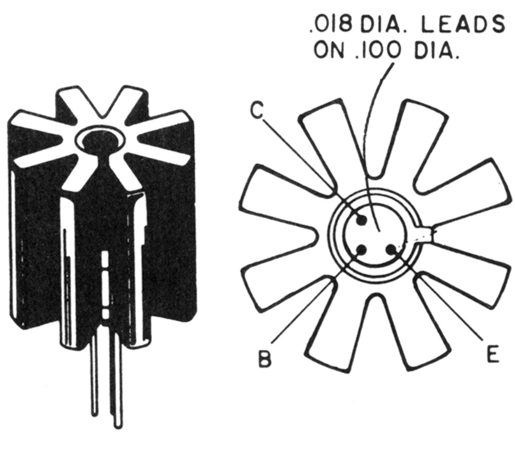
P—8



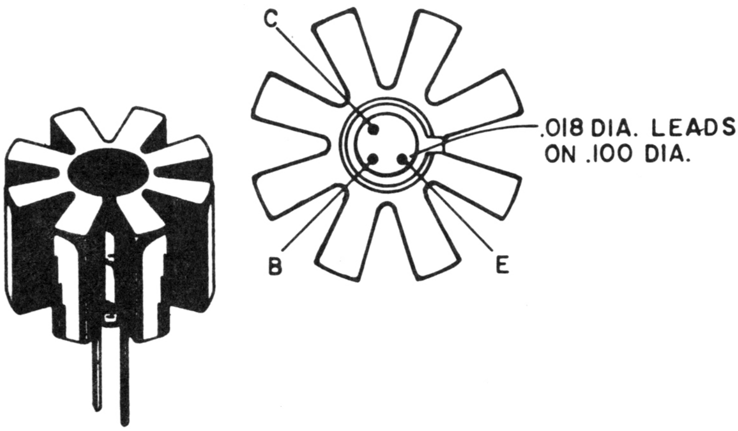
P—9



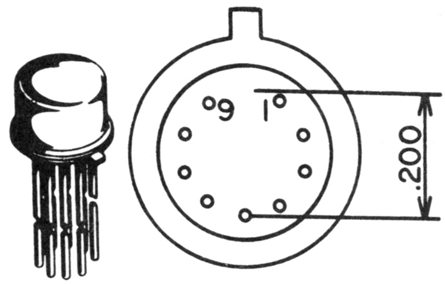
P—10



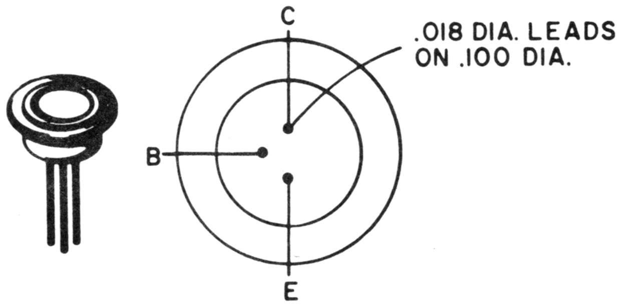
P—13



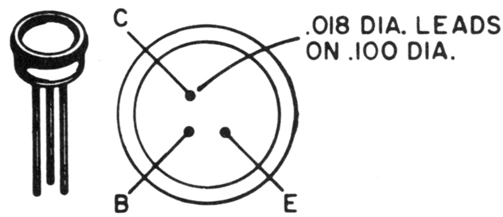
P—15



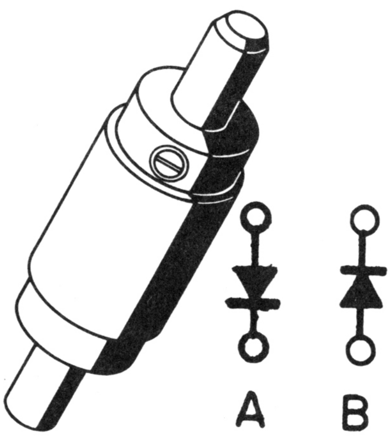
P—16



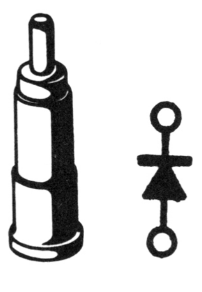
P—19



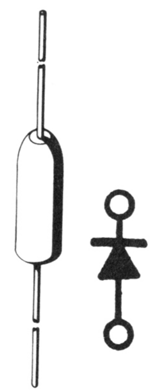
P—20



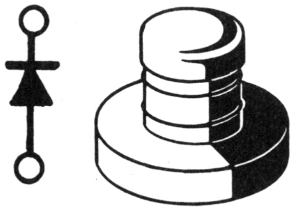
P—22



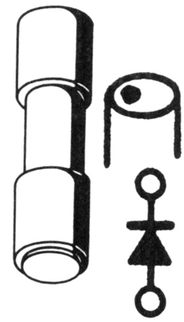
P—23



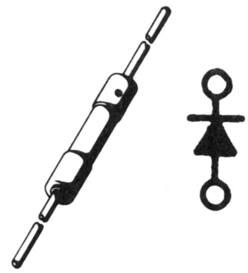
P—24



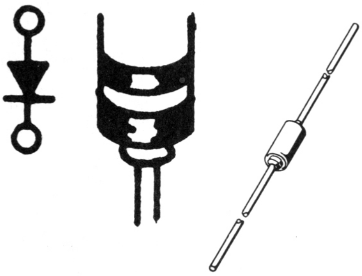
P—26



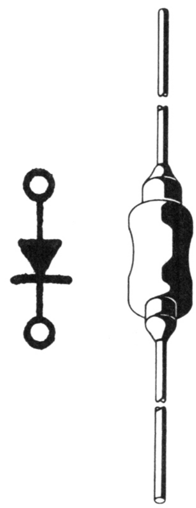
P—28



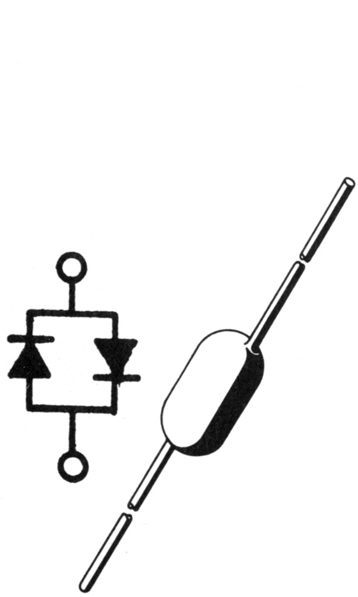
P—29



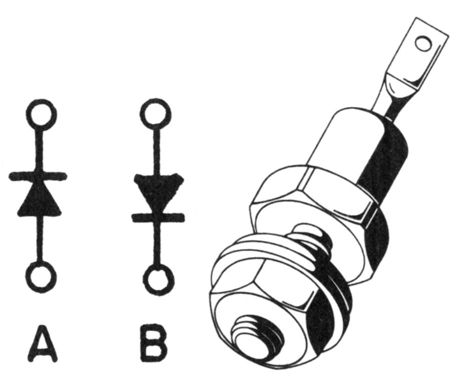
P—30



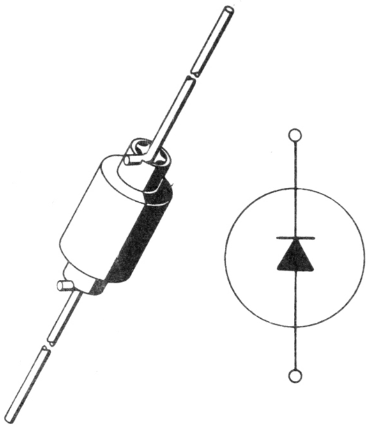
P—34



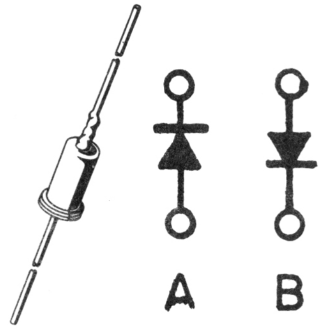
P—35



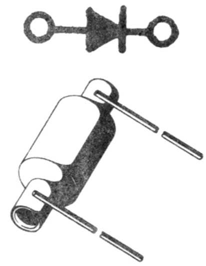
P—36



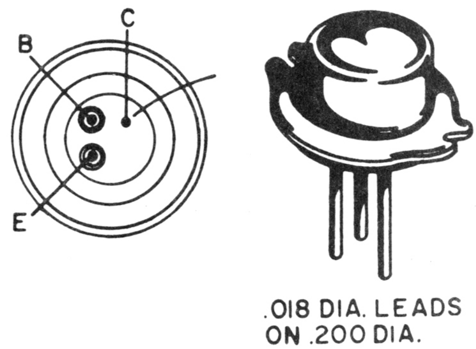
P—38



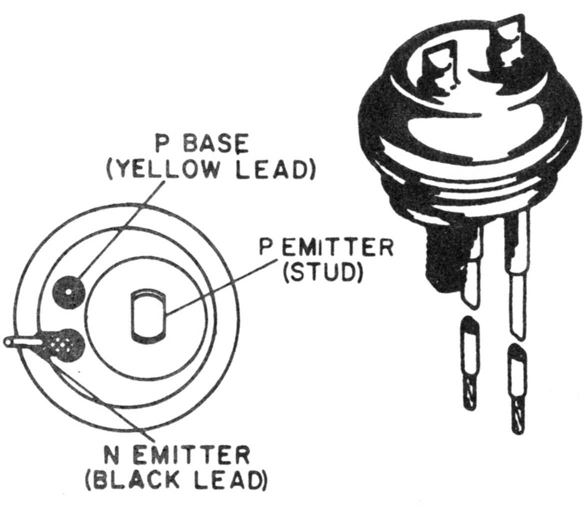
P—39



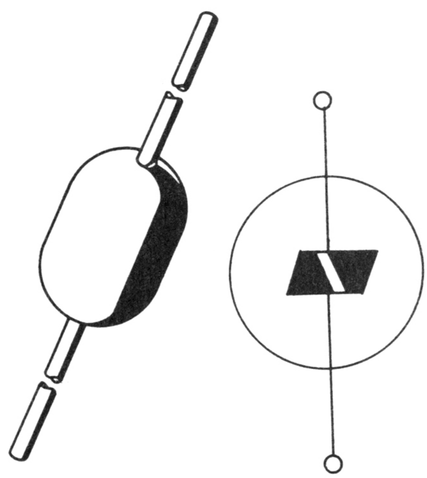
P—40



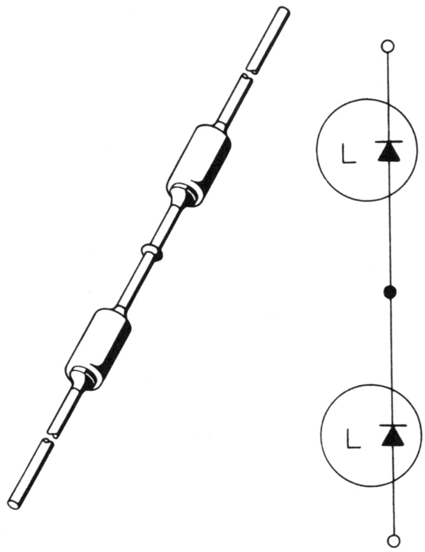
P—44



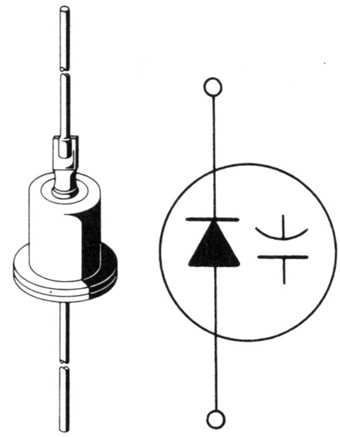
P—46



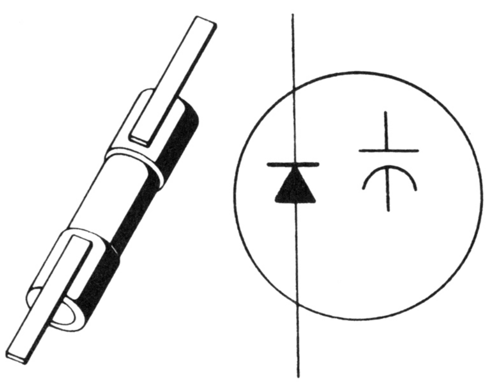
P—61



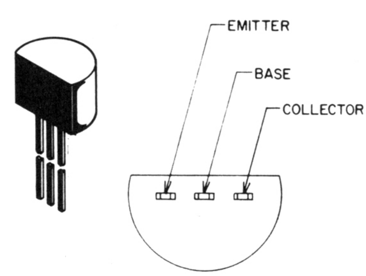
P—62



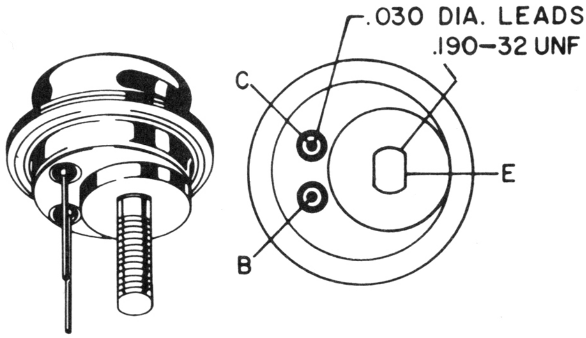
P—63



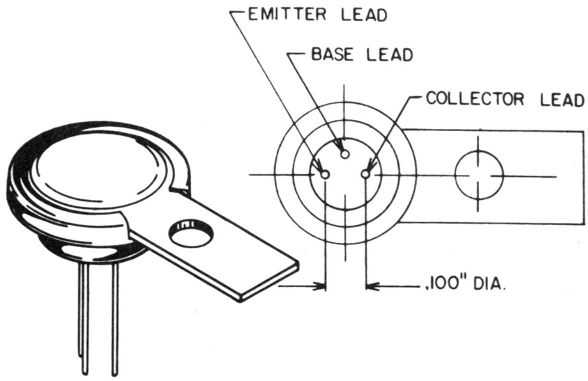
P—65



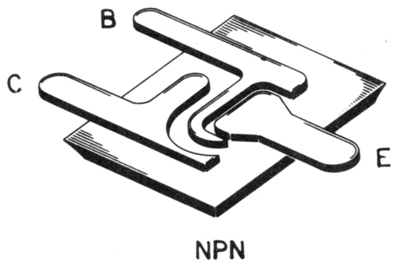
P—67



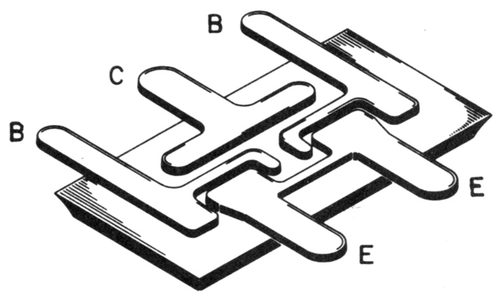
P—68



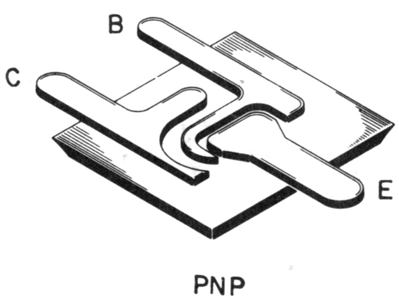
P—69



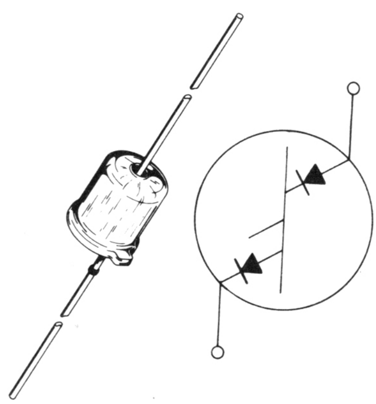
P—70



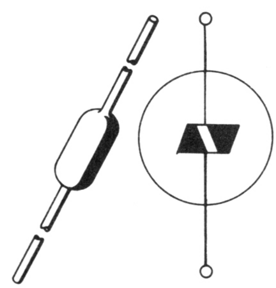
P—71



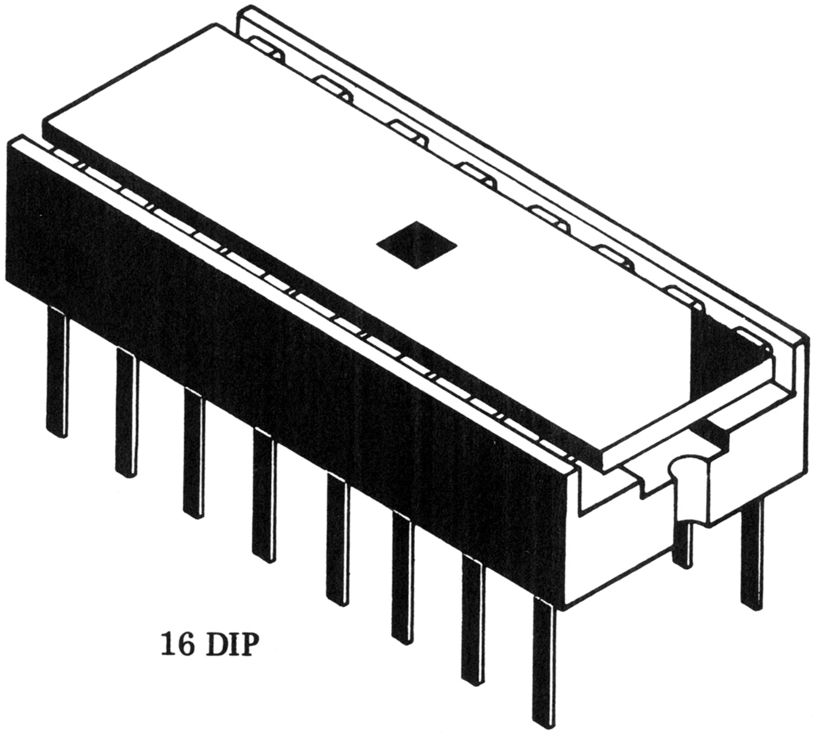
P—72



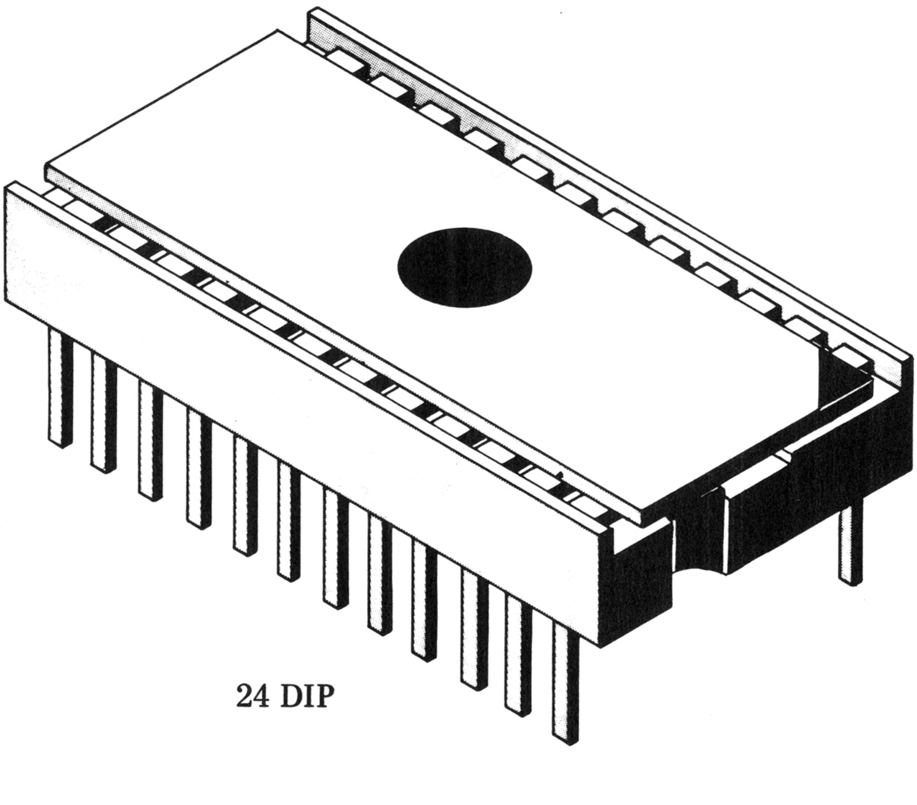
P—77



P—76



16 DIP



24 DIP

Glossary of Terms

DISCRETE DEVICES

BV. . . . . Breakdown voltage

Breakdown voltage — That value of reverse voltage which remains essentially constant over a considerable range of current values.

BV_{CBO}. . . . . Collector to base breakdown voltage, open emitter.

BV_{CES}. . . . . Collector to emitter breakdown voltage, base dc short circuited to emitter.

BV_{EBO}. . . . . Emitter to base breakdown voltage, open collector.

BV_F. . . . . Forward breakdown voltage for PNPN devices.

The maximum forward voltage between E_P and E_N attained before breakdown under base bias conditions specified.

BV_R. . . . . Reverse breakdown voltage for PNPN devices.

The maximum reverse voltage between E_P and E_N attained before breakdown is achieved or maximum specified reverse power is reached under base bias conditions specified.

C_O. . . . . Capacitance of a diode at zero direct current.

The capacitance at a specified applied ac voltage and frequency and zero direct current.

fh_{fb}. . . . . Small-signal short-circuit forward-current transfer ratio cutoff frequency.

The frequency at which the absolute value of the small-signal short-circuit forward-current transfer ratio is 0.70 times its value at the specified test frequency.

DISCRETE DEVICES (Continued)

f_T. . . . . Extrapolated unity gain frequency.

The frequency, obtained by extrapolation, at which h_{fe} becomes unity when reduced at a rate of 6 db/octave.

h_{fb}. . . . . Small-signal short-circuit forward-current transfer ratio.

Definition — The ratio of the ac output current to the ac input current.

h_{FB}. . . . . Static forward-current transfer ratio.

The ratio of the dc output current to the dc input current under the specified test conditions.

h_{fe}. . . . Small-signal short-circuit forward-current transfer ratio.

The ratio of the ac output current to the ac input current with zero ac output voltage.

I_{CBO}. . . . . Collector cutoff (saturation) current, open emitter.

The collector cutoff (saturation) current is the dc leakage current in the collector or base terminal when it is reversed biased by a voltage less than the breakdown voltage and with the emitter dc open-circuited.

I_B. . . . . Base Current, dc.

I_F. . . . . Forward current, dc.

I_H. . . . . Hold current for PNPN devices.

The forward current at which the negative resistance across the device becomes equal to a specified value during the transition from the low impedance to the high impedance state under specified base bias conditions.

I_R. . . . . Reverse current, dc.

DISCRETE DEVICES (Continued)

I_S. . . . . Saturation current.

The dc reverse current which flows through the semiconductor diode under the reverse voltage conditions specified (normally 80% or less of BV).

N_F. . . . . Noise figure.

At a selected input frequency, the noise figure is the ratio of the total noise power per unit bandwidth (at the corresponding output frequency) delivered to the output termination, to the portion produced at the input frequency by the thermal noise of the input termination, whose noise temperature is standard (290°K) at all frequencies.

Power Rating. . . . .

That power, which, when applied under specific conditions, yields the junction temperature acceptable for a particular application. In the case of the Quick Selection Guide, the rating for silicon is 125 to 150°C and for germanium is 85 to 100°C with the case at 25°C or ambient as required.

Status. . . . .

For convenience, the status is classified into two groups, as follows:

P. . . . . . Preferred.

R. . . . . . Restricted (check use with Applications Engineer).

t_W. . . . . Pulse average time.

The average pulse time of a pulse is the time duration from a point on the leading edge which is 50 percent of the maximum amplitude to a point on the trailing edge which is 50 percent of the maximum amplitude. (See Figure 1.)

DISCRETE DEVICES (Continued)

t_d. . . . . Pulse delay time.

The delay time of a pulse is the time interval from a point at which the leading edge of the input pulse has risen to 10 percent of its maximum amplitude to a point at which the leading edge of the output pulse has risen to 10 percent of its maximum amplitude.

t_f. . . . . Pulse fall time.

The fall time of a pulse is that time duration during which the amplitude of its trailing edge is decreasing from 90 to 10 percent of the maximum amplitude. (See Figure 1.)

t_r. . . . . Pulse rise time.

The rise time of a pulse is that time duration during which the amplitude of its leading edge is increasing from 10 to 90 percent of the maximum amplitude. (See Figure 1.)

t_s. . . . . Pulse storage time.

The storage time of a pulse is the time interval from a point 10 percent down from the maximum amplitude on the trailing edge of the input pulse to a point 10 percent down from the maximum amplitude on the trailing edge of the output pulse.

t_{rr}. . . . . Reverse recovery time.

The time between the instant current reversal from forward to reverse and the instant at which the specified reverse condition is reached.

V_{BE}. . . . . Base to emitter voltage.

DISCRETE DEVICES (Continued)

V_{CE}(sat). . . . . Saturation voltage, collector to emitter.

The dc voltage between the collector and emitter terminals for the specified saturation conditions (when the transistor output characteristic is essentially a constant voltage).

V_{CE}(sus). . . . . Sustain voltage, collector to emitter.

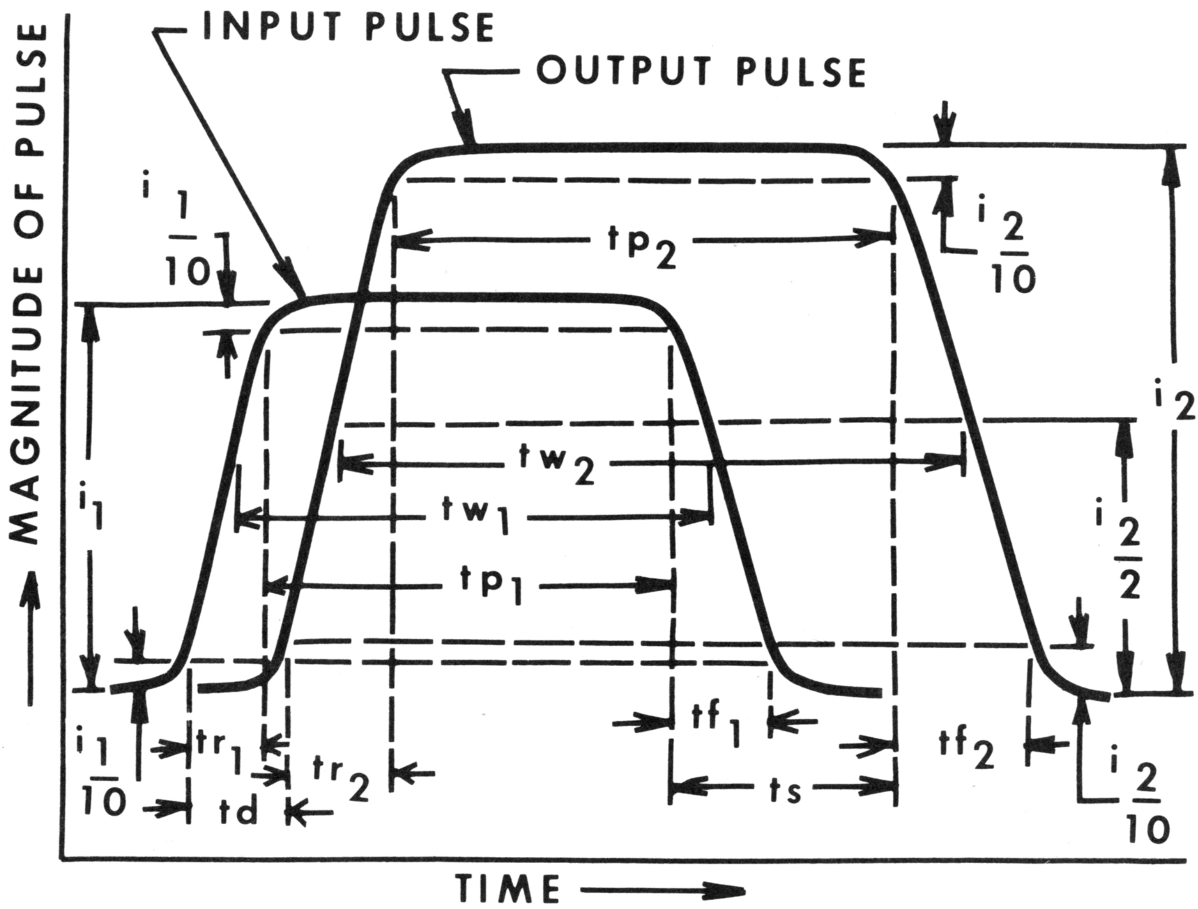
The voltage which appears between the collector and emitter terminals with specified input current or voltage and output current (LV_{CEO}).

V_F. . . . . Forward voltage, dc.

V_R. . . . . Reverse voltage, dc.

V_{RT}. . . . . Reach through voltage.

That value of reverse voltage for which the depletion layer spreads sufficiently to contact another junction or contact.



t_r = Pulse Rise Time

t_d = Pulse Delay Time

t_p = Pulse Time

t_s = Pulse Storage Time

t_f = Pulse Fall Time

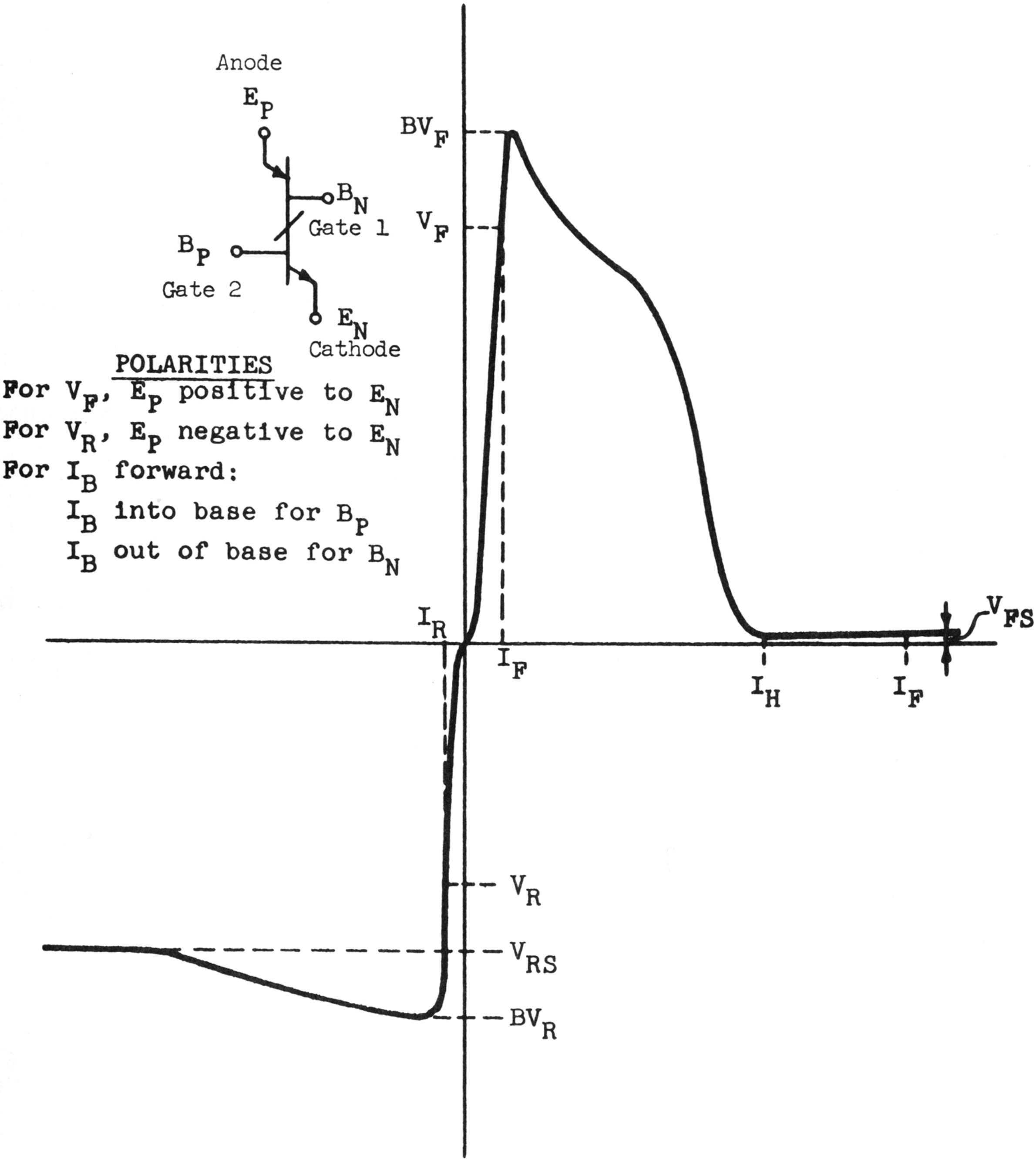
t_w = Pulse Average Time

i_1 = Input Pulse Amplitude

i_2 = Output Pulse Amplitude

PULSE CHARACTERISTICS

Following is a graphical presentation of symbols for multiple junction devices (SCR, PNPN, etc.):



DIGITAL MICROCIRCUITS

High Level. . . . .

The level which is the more positive of the two logic levels.

Low Level. . . .

The level which is the more negative of the two logic levels.

Negative Logic. . . . .

The logic is termed negative when logic ZERO state is assigned to the HIGH level and logic ONE state to the LOW level.

Positive Logic. . . . .

The logic is termed positive when logic ONE state is assigned to the HIGH level and logic ZERO state to the LOW level.

Noise Margin. . . . .

The voltage amplitude of extraneous signal which can be added to the noise-free worst-case input level before the output voltage deviates from the allowable level.

V_{CC}. . . . . Supply Voltage, Max (or Min) (V_{CC} max, V_{EE} min, etc.).

The maximum (or minimum) supply voltage that may be applied for which operation of the integrated circuit within specified limits is guaranteed.

V_{IL}. . . . . Input Voltage, Low Level.

The maximum voltage that may be applied to an input without changing the output from a HIGH to a LOW state.

DIGITAL MICROCIRCUITS (Continued)

V_{IH}. . . . . Input Voltage, High Level.

The minimum voltage that may be applied to an input without changing the output from a LOW to a HIGH state.

V_{OL}. . . . . Output Voltage, Low Level.

The voltage level at the output terminal for a specified output current with specified conditions applied to establish a LOW level output.

V_{OH}. . . . . Output Voltage, High Level.

The voltage level at the output terminal for a specified output current with specified conditions applied to establish a HIGH level output.

I_{LL}. . . . . Input Current, Low Level.

The current flowing into an input when the specified LOW level voltage is applied to that input.

I_{IH}. . . . . Input Current, High Level.

The current flowing into an input when the specified HIGH level voltage is applied to that input.

I_{OL}. . . . . Output Current, Low Level.

The current flowing into the output at the specified LOW level output voltage.

I_{OH}. . . . . Output Current, High Level.

The current flowing into the output at the specified HIGH level output voltage.

DIGITAL MICROCIRCUITS (Continued)

Fan-In. . . . .

The maximum number of independent input variables that can be used with a logic circuit.

Fan-Out. . . . .

The maximum number of logic circuits that can be driven by a logic circuit.

Unit Load. . . . .

The power required to drive the input of a simple gate of a device of the same family.

T_{PD}. . . . . Propagation Delay.

The time required for a logic signal to pass through a logic circuit or circuits.

Truth Table. . . . .

A tabulation relating all output logic states to all necessary or possible combinations of input logic states for sufficient successive time intervals to completely characterize the logic circuit.

LINEAR MICROCIRCUITS

Balanced Amplifier. . . . .

An amplifier whose quiesent dc output voltage is reduced to zero.

V_{IO}. . . . . Offset Voltage.

That voltage which must be applied between input terminals to obtain zero output voltage.

LINEAR MICROCIRCUITS (Continued)

I_{IO}. . . . . Offset Current.

The difference in the currents into the two input terminals of a balanced amplifier.

I_B. . . . . Bias Current.

The average of the two input currents.

A_{VD}. . . . .Voltage Gain — Differential.

The ratio of the change in output voltage to the change in differential input voltage.

A_{VC}. . . . . Voltage Gain — Common-Mode.

The ratio of the change in output voltage to the change in common-mode input voltage.

CMRR. . . . . Common-Mode Rejection Ratio.

The ratio of the differential voltage gain to the common-mode voltage gain.

Unity Gain Bandwidth. . . . .

The range of frequencies within which the circuit gain is greater than unity.

Cut-Off Frequency. . . . .

The frequency at which the gain is 3 dB below the gain at a specified frequency.

Phase Margin. . . . .

A figure equal to 180° minus the absolute value of phase shift at unity gain frequency.

LINEAR MICROCIRCUITS (Continued)

Slew Rate. . . . .

The time rate of change of the amplifier output voltage for a step signal input.

Total Harmonic Distortion. . . . .

The ratio, expressed in percent, of the rms voltage of all harmonics in the output to the rms voltage of the output for a pure sine wave input.

FIELD EFFECT TRANSISTORS

IGFET. . . . . . .

FET with gate area insulated from channel area. Insulated Gate Field Effect Transistor.

MOSFET. . . . . . .

Insulating gate area is oxide of basic silicon material. Thus Metal Oxide Silicon Field Effect Transistor.

Drain. . . . .

Equivalent to collector terminal of transistor.

Source. . . . .

Equivalent to emitter terminal of transistor.

Gate. . . . .

Equivalent to base terminal of transistor.

Channel. . . . .

Conducting region of FET.

FIELD EFFECT TRANSISTORS (Continued)

Unipolar. . . . .

FET uses only majority current carriers, unlike conventional bipolar transistors which use both majority and minority carriers.

Depletion Mode. . . . .

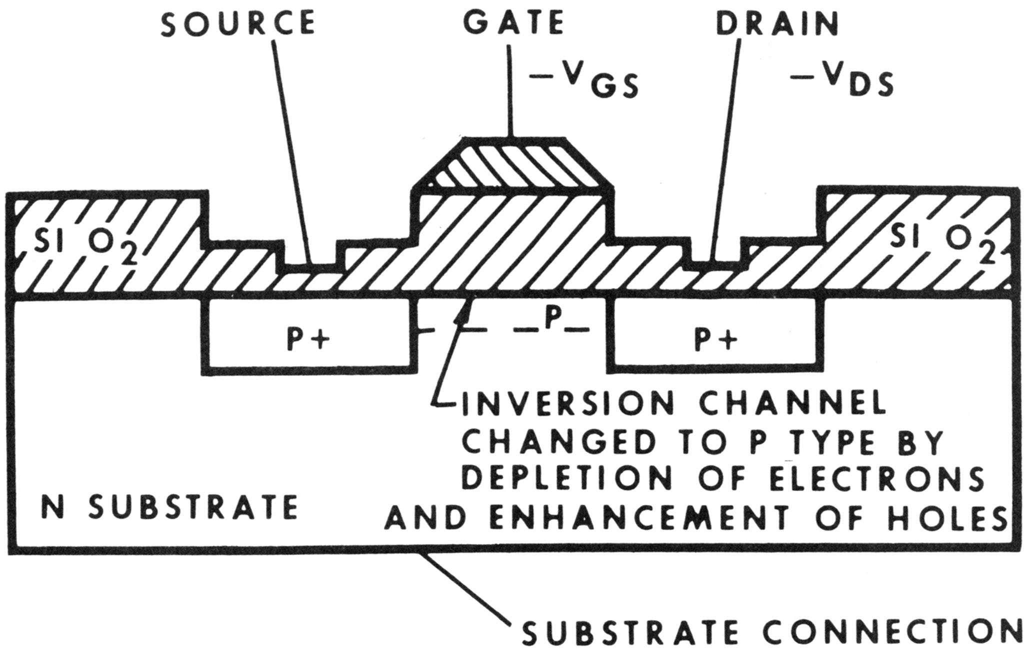
FET is normally "on." Reverse biasing the gate depletes the channel reducing drain current.

Enhancement Mode. . . . .

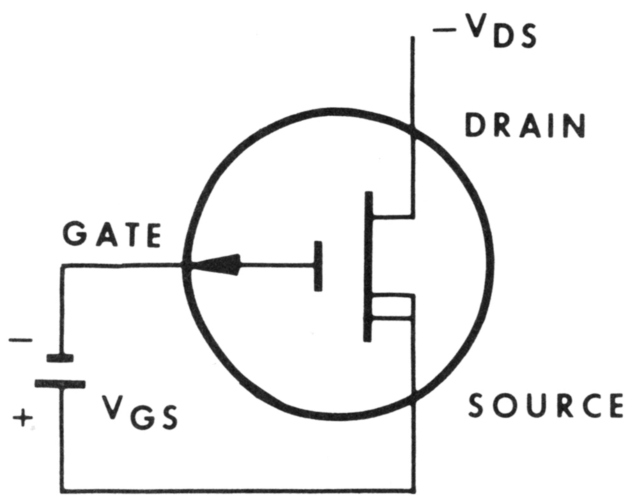
FET is normally "off." Forward biasing the gate enhances the channel increasing the drain current.

Characteristics of FET's. . . . .

1. Characteristics similar to a vacuum pentode tube.
2. Voltage controlled device.
3. Very high input impedance $\approx 10^{12}$ - 10^{14} ohms (IGFET).
4. High power gain.
5. Excellent temperature stability.
6. Enhancement mode IGFET's can be direct coupled because $V_{GS} = V_{DS}$.



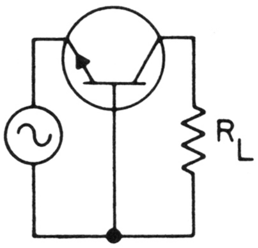
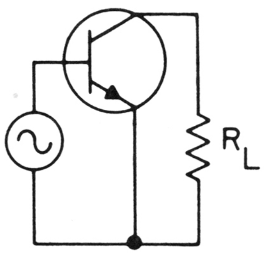
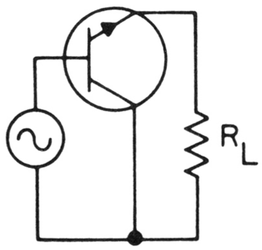
P-CHANNEL-IGFET
ENHANCEMENT MODE



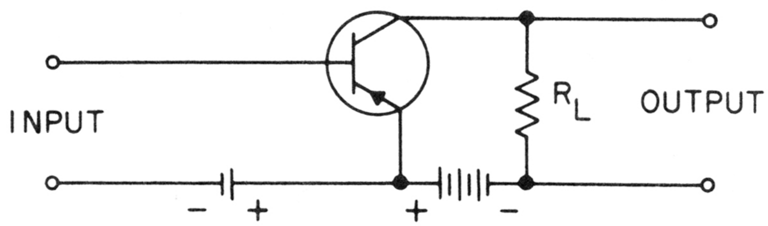
P-CHANNEL-IGFET

Appendix

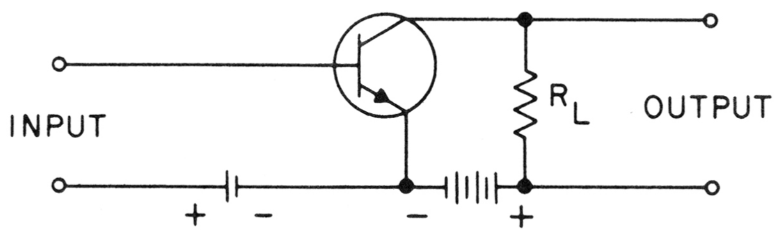
TRANSISTOR CIRCUIT CONFIGURATIONS

CIRCUIT	CHARACTERISTICS
 COMMON BASE (CB)	Lowest input impedance Highest output impedance Low current gain (<1) High voltage gain Moderate power gain
 COMMON EMITTER (CE)	Moderate input impedance Moderate output impedance High current gain High voltage gain Highest power gain
 COMMON COLLECTOR (CC) (EMITTER FOLLOWER)	Highest input impedance Lowest output impedance High current gain Unity voltage gain Lowest power gain

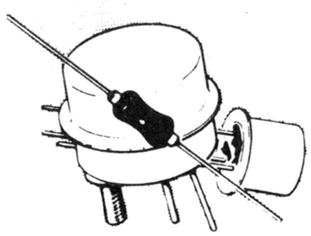
TRANSISTOR CIRCUIT CONFIGURATIONS (Continued)



COMMON EMITTER BIAS CIRCUIT - PNP



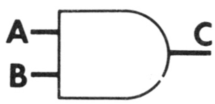
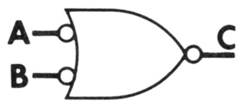
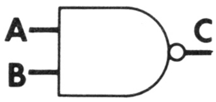
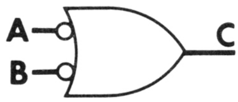
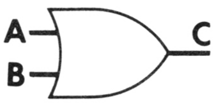
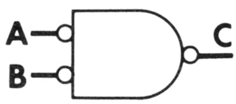
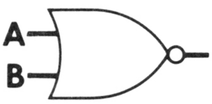
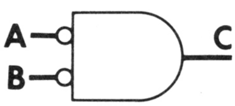
COMMON EMITTER BIAS CIRCUIT - NPN



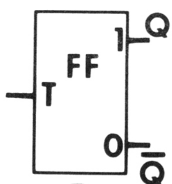
BASIC LOGIC DIAGRAMS

Positive Logic: HI=1=True ,LO=O=False,
Small circle= LO significant state

GATES

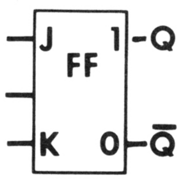
FUNCTION	BASIC	EQUIVALENT	TRUTH TABLE A B C
AND GATE			HI HI HI HI LO LO LO HI LO LO LO LO
NAND GATE			HI HI LO HI LO HI LO HI HI LO LO HI
OR GATE			HI HI HI HI LO HI LO HI HI LO LO LO
NOR GATE			HI HI LO HI LO LO LO HI LO LO LO HI

FLIP-FLOPS



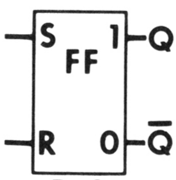
T

Input: Condition before trigger pulse Q	$\bar{Q}$	Output: Condition after trigger pulse Q	$\bar{Q}$
LO	HI	HI	LO
HI	LO	LO	HI



J-K

Input J	K	Output Q	$\bar{Q}$
LO	LO	No Change	
LO	HI	LO	HI
HI	LO	HI	LO
HI	HI	Comple	



R-S

Input R	S	Output Q	$\bar{Q}$
LO	LO	No change	
LO	HI	LO	HI
HI	LO	HI	LO
HI	HI	Undefined	

FLIP-FLOP INPUTS

SET.............Shown by the letter S
RESET........ Shown by the letter R
TOGGLE.....Shown by the letter T
J and K....Shown by the letters J and K

REFERENCE LIST

BASIC THEORY AND APPLICATION OF TRANSISTORS
TM 11-690, U. S. Government Printing Office

BELL SYSTEM PRACTICES (Data Sheets)
American Telephone and Telegraph Company

DEFINITIONS OF SEMICONDUCTOR TERMS
Proceedings of I.R.E., Volume 48, October, 1960

ELECTRONICS: BJTs, FETs, AND MICROCIRCUITS
E. James Angelo, Jr.
McGraw-Hill — 1969

HANDBOOK OF SEMICONDUCTOR ELECTRONICS
Lloyd P. Hunter
McGraw-Hill

POWER TRANSISTOR HANDBOOK
Motorola Semiconductor Products Division

TRANSISTOR CIRCUIT DESIGN
Texas Instruments Incorporated

TRANSISTOR MANUAL
General Electric Company

TRANSISTOR MANUAL (Tech. Series SC-10)
R.C.A. Semiconductor and Materials Division

ZENER DIODE HANDBOOK
International Rectifier Corporation