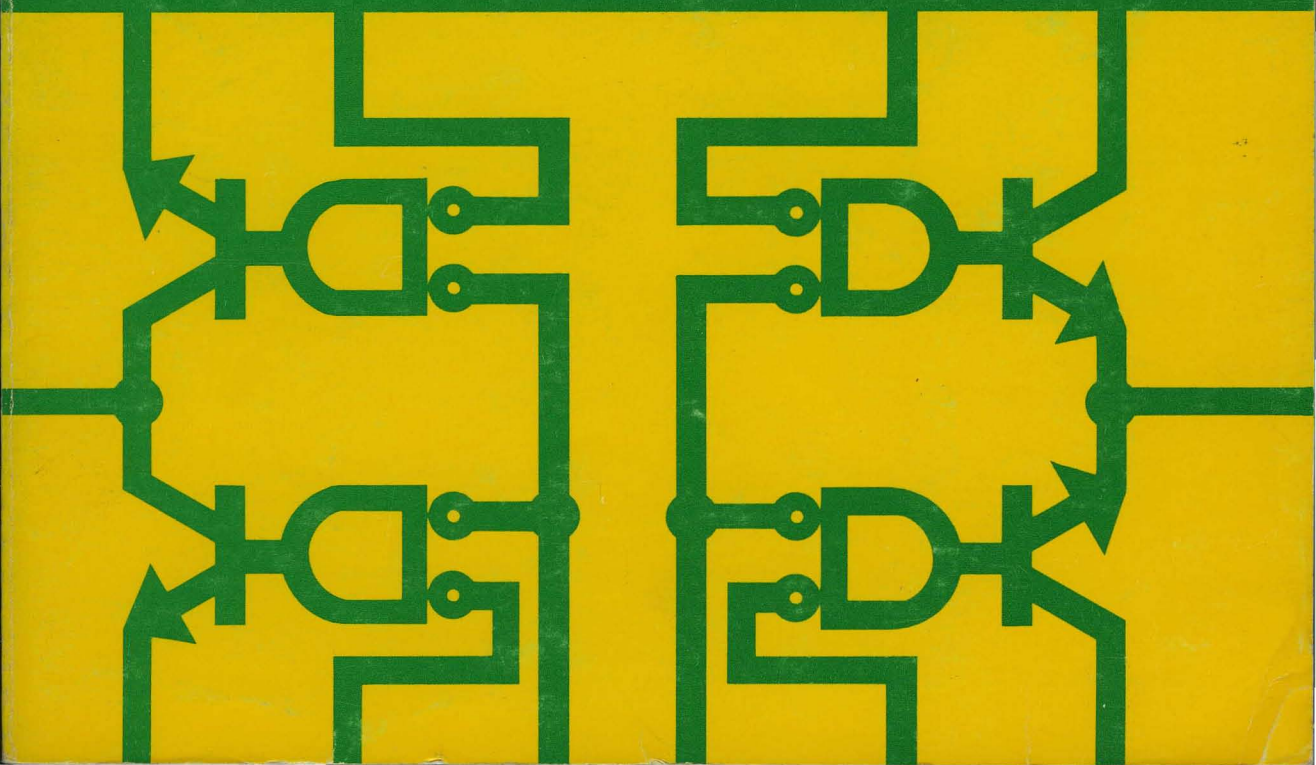
INTERFACE
INTEGRATED CIRCUITS

National

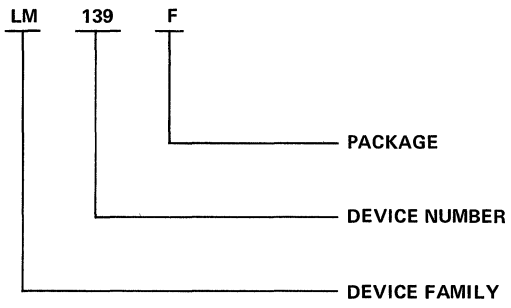


Edge Index by Product Family

Here is the new INTERFACE catalog from National Semiconductor Corporation. It contains complete information on all of National's INTERFACE products whether they be Linear, Digital, or MOS. It is the first such catalog in the industry and we hope it becomes your most important INTERFACE guide. For your convenience, two different Tables of Contents are provided. One lists the products by type—Line Driver, Sense Amplifier, etc.—and the other lists the products alphanumerically by part number. Product selection guides and a complete product applications section are also included.

Ordering Information

The ordering information for National devices covered in this catalog is as follows:



DEVICE FAMILY

AH – Analog Hybrid
AM – Analog Monolithic
DH – Digital Hybrids
DM – Digital Monolithic
LF – Linear FET
LH – Linear Hybrid
LM – Linear Monolithic
LX – Transducer
MH – MOS Hybrid
MM – MOS Monolithic

PACKAGE

D – Glass/Metal Dual-In-Line Package
F – Flat Package (0.25" wide)
G – TO-8 (12 lead) Metal Can
H – TO-5 (multi-lead) Metal Can
J – Glass/Glass Dual-In-Line Package
K – TO-3 Power Package
N – Molded Dual-In-Line Package
W – Flat Package (0.275" wide)

DEVICE NUMBER

3, 4 or 5 digit number.

Suffix Indicators:

A – Improved Electrical Specification
C – Reduced Temperature Range

Devices are listed in the table of contents alpha-numerically by device family (LH, LM, LX, etc.) and then by device number. **With most of National's proprietary linear circuits, a 1-2-3 numbering system is employed. The 1 denotes a Military temperature range device (–55°C to +125°C), the 2 denotes an Industrial temperature range device (–25°C to +85°C), and the 3 denotes a Commercial temperature range device (0°C to +70°C), i.e. LM111/LM211/LM311.**

Exceptions to this are some hybrid circuits which employ a "C" suffix to denote the commercial temperature range; and second-source products which follow the original manufacturers numbering system, i.e. LM710/LM710C or LM1414/LM1514.

Interface circuits and sense amplifiers employ a 55 as the first two digits for the military temperature range part, and a 75 for the commercial part, i.e. LM5520/LM7520. Display drivers and line drivers and receivers employ a 78/88 prefix. The 78 applies to the military part, and the 88 to the commercial part, i.e. DM7830/DM8830. And digital products employ a 54 as the first two digits for the military temperature range part, and a 74 for the commercial part, i.e. DM5406/DM7406.

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Alpha-Numerical Index

DEVICE NUMBER	NATIONAL PIN-FOR-PIN EQUIVALENT	NATIONAL FUNCTIONAL EQUIVALENT
Texas Instruments		
SN5500F		LM5524J
SN5524J	LM5524J	
SN5525J	LM5525J	
SN7500F		LM7524J
SN7501F		LM7524J
SN7502F		LM7524J
SN7520J	LM7520J	
SN7520N	LM7520N	
SN7521J	LM7521J	
SN7521N	LM7521N	
SN7522J	LM7522J	
SN7522N	LM7522N	
SN7523J	LM7523J	
SN7523N	LM7523N	
SN7524J	LM7524J	
SN7524N	LM7524N	
SN7525J	LM7525J	
SN7525N	LM7525N	
SN7528J	LM7528J	
SN7528N	LM7528N	
SN7529J	LM7529J	
SN7529N	LM7529N	
SN52710J		LM710H
SN52710L	LM710H	
SN52710N		LM710H
SN52710S		LM710H
SN52711J		LM711H
SN52711L	LM711H	
SN52711N		LM711H
SN52711S		LM711H
SN55107J	LM55107J	
SN55108J	LM55108J	
SN55109J	LM55109J	
SN55110J	LM55110J	
SN55182J	DM7820AJ	
SN55183J	DM7830J	
SN72710J		LM710CN
SN72710L	LM710CH	
SN72710N	LM710CN	
SN72710S		LM710CH
SN72711J		LM711CN
SN72711L	LM711CH	
SN72711N	LM711CN	
SN72720N	LM1414N	
SN72811S		LM711CH
SN75100L		DM8820D
SN75107J	LM75107J	
SN75107N	LM75107N	
SN75108J	LM75108J	
SN75108N	LM75108N	
SN75109J	LM75109J	
SN75109N	LM75109N	
SN75110J	LM75110J	
SN75110N	LM75110N	
SN75121J	LM75121J	
SN75121N	LM75121N	
SN75122J	LM75122J	
SN75122N	LM75122N	
SN75123J	LM75123J	
SN75123N	LM75123N	
SN75124J	LM75124J	
SN75124N	LM75124N	
SN75150J	LM75150J	
SN75150N	LM75150N	
SN75154J	LM75154J	
SN75154N	LM75154N	
SN75182J	DM8820AJ	
SN75182N	DM8820AN	
SN75183J	DM8830J	
SN75183N	DM8830N	
SN75324J	LM75324J	
SN75324N	LM75324N	
SN75325J	LM75325J	
SN75325N	LM75325N	
SN75450AN	LM75450N	
SN75450N	LM75450N	
SN75451AP	LM75451N	
SN75451P	LM75451N	
SN75452P	LM75452N	
SN75453P	LM75453N	
SN75454P	LM75454N	
SN75491N	DM75491N	
SN75492N	DM75492N	
SN75207J	LM75207J	
SN75207N	LM75207N	
SN75208J	LM75208J	
SN75208N	LM75208N	
Motorola		
MC1414L	LM1414J	
MC1440F		LM7524J
MC1440G		LM7524J
MC1440L		LM7524J
MC1441F		LM7524J
MC1441L		LM7524J
MC1488L	LM1488J	
MC1489AL	LM1489AJ	
MC1489L	LM1489J	
MC1514L	LM1514J	
MC1580L		DM7831J
MC1582L		DM7830J
MC1583L		DM7820J
MC1584L		DM7820AJ
MC1710CF		LM710CH
MC1710CG	LM710CH	
MC1710CL		LM710CH
MC1710F		LM710H
MC1710G	LM710H	
MC1710L		LM710H
MC1711CF		LM711CH
MC1711CG	LM711CH	
MC1711CL		LM711CH
MC1711F		LM711H
MC1711G	LM711H	
MC1711L		LM711H
Signetics		
DM8880N	DM8880N	
N5710A	LM710CN	
N5710T	LM710CH	
N5711A	LM711CN	
N5711K	LM711CH	
N7520B	LM7520N	
N7521B	LM7521N	
N7522B	LM7522N	
N7523B	LM7523N	
N7524B	LM7524N	
N7525B	LM7525N	
N8T13B	LM75121N	
N8T13F	LM75121J	
N8T14B	LM75122N	
N8T14F	LM75122J	
N8T23B	LM75123N	
N8T24B	LM75124N	
N8T25B	LM3625N	
NE518A		LM306H
NE518G		LM306H
NE518K		LM306H
NE526A		LM306H
NE526G		LM306H
NE526K		LM306H
NE529A	LM361N	
NE529K	LM361H	
S5710T	LM710H	
S5711K	LM711H	
S5711T		LM711H
SE518A		LM106H
SE518G		LM106H
SE518K		LM106H
SE526A		LM106H
SE526G		LM106H
SE526K		LM106H
SE529K	LM161H	
Fairchild		
U31962051X		DM7820D
U31962059X		DM8820N
U31962151X		DM7830D
U31962159X		DM8830N
U31962251X		DM7820D
U31962259X		DM8820N
U4L961451X		DM7830D
U4L961459X		DM8830D
U4L961551X		DM7820D
U4L961559X		DM8820N
U5B7710312	LM710AH	
U5B7710393	LM710CH	
U5F7711312	LM711H	
U5F7711393	LM711CH	
U5F7734312		LM111H
U5F7734393		LM311H
U6A7710312		LM710AH
U6A7710393	LM710CN	
U6A7711312		LM711H
U6A7711393	LM711CN	
U6A7750312		LM111H
U6A7750393		LM311H
U6A7760312	LM160J	
U6A7760393	LM360J	
U7B7524392	LM7524J	
U7B7525393	LM7525J	
U7B7761391		LM7524J
U7B7761392	LM7524J	
U7B7761393	LM7525J	
U7B961451X		DM7830D
U7B961459X		DM8830N
U7B961551X		DM7820D
U7B961559X		DM8820N
U7B961651X		LM1488J
U7B961659X		LM1488J
U7B961751X		LM1489AJ
U7B961759X		LM1489AJ
U7B964451X		DH0011H

Interface Cross Reference Guide

Voltage Comparator Guide

Device	Temperature Range*	DTL/TTL Fanout	Supply Voltage Typ (Volts)	Input Bias Current (+25°C) Max (μA)	Input Offset Current (+25°C) Max (μA)	Input Offset Voltage (+25°C) Max (mV)	Response Time† Typ (ns)	Voltage Gain Typ	Package Type	Comments
LM106	Military	10	$V^+ = +12$	20	3	2	40 max	40k	TO-5 F P	Single comparator with strobe, high speed and sensitivity, large fanout
LM206	Industrial	10	$V^- = -3$	20	3	2	40 max	40k	TO-5 F P	
LM306	Commercial	10	To −12	25	5	5	40 max	40k	TO-5 F P	
LM111 LH2111 (Note 1)	Military	5	±15	1	04	7	200	200k	TO-5 DIP F P	Single, with strobe, will work from single supply, low bias current
LM211 LH2211 (Note 1)	Industrial	5	To +5	1	04	7	200	200k	TO-5 DIP F P	
LM311 LH2311 (Note 1)	Commercial	5	And GND	25	06	2	200	200k	TO-5 DIP F P	
LM119	Military	2 (each side)	±15	5	075	4	80	40k	TO-5 DIP F P	High speed dual comparator
LM219	Industrial	2 (each side)	To +5	5	075	4	80	40k	TO-5 DIP F P	
LM319	Commercial	2 (each side)	And GND	1	2	8	80	40k	TO-5 DIP	
LM139	Military	1	±1	1	025	5	1 3 μs	200k	DIP F P	Quad comparator designed for single supply operation, input common mode range includes ground
LM239	Industrial	1	To ±18	25	050	5	1 3 μs	200k	DIP	
LM339	Commercial	1	Or From	25	050	5	1 3 μs	200k	DIP	
LM139A	Military	1	+2	1	025	2	1 3 μs	200k	DIP F P	Low offset voltage Quad comparator with DTL/TTL logic levels.
LM239A	Industrial	1	To +36	25	050	2	1 3 μs	200k	DIP	
LM339A	Commercial	1	And GND	25	050	2	1 3 μs	200k	DIP	
LM160	Military	2	±4 5	10	2	2	16	3k	TO-5 DIP F P	Very high speed, outputs compatible with DTL/TTL logic levels
LM260	Industrial	2	To	10	2	2	16	3k	TO-5 DIP	
LM360	Commercial	2	±6 5	15	4	4	16	3k	TO-5 DIP	
LM161	Military	2	±5	10	2	2	12	3k	TO-5 DIP F P	Very high speed, with individual strobes, DTL/TTL compatible
LM261	Industrial	2	To ±15	10	2	2	12	3k	TO-5 DIP	
LM361	Commercial	2	And +5	15	4	4	12	3k	TO-5 DIP	
LM710	Military	1	$V^+ = +12$	20	3	2	40	1750	TO-5	Single, differential in, single output
LM710C	Commercial	1	$V^- = -6$	25	5	5	40	1500	TO-5 DIP	
LM711	Military	1	$V^+ = +12$	75	10	3 5	40	1500	TO-5	Dual differential, common output, individual strobes
LM711C	Commercial	1	$V^- = -6$	100	15	5	40	1500	TO-5 DIP	
LM1514	Military	1	$V^+ = +14$	20	3	3	30	1250	DIP	Dual LM710 with separate strobes, individual outputs
LM1414	Commercial	1	$V^- = -7$	25	5	4	30	1000	DIP	

*Military −55°C to +125°C
Industrial −25°C to +85°C
Commercial 0°C to +70°C

†Response time is specified for 100 mV step input with 5 mV overdrive

Note 1 Dual version of device

DEVICE	DRIVER OR RECEIVER	COMMON MODE OR DIFFERENTIAL	INPUT THRESHOLD	OUTPUT LEVELS	POWER SUPPLY	DESCRIPTION AND COMMENTS
DM7820/DM8820	Receiver	Differential	200 mV	TTL	+5.0	Dual ±15V Common Mode Range
DM7820A/DM8820A	Receiver	Differential	200 mV	TTL	+5.0	High Performance DM7820
DM7822/DM8822	Receiver	Differential/Common Mode	−2.0 to +20	TTL	+5.0	Dual EIA Standard RS232
DM7830/DM8830	Driver	Differential	TTL	TTL	+5.0	Dual
DM7831/DM8831	Driver	Differential/Common Mode	TTL	TTL	+5.0	TRI-STATE® DM7830
DM7832/DM8832	Driver	Differential/Common Mode	TTL	TTL	+5.0	DM7831 Without V_{CC} Clamp Diodes
LM55107/LM75107	Receiver	Differential	25 mV	TTL	±5.0	10 mV Threshold LM55107 Dual
LM55207/LM75207	Receiver	Differential	10 mV	TTL	±5.0	10 mV Threshold LM55107
LM55108/LM75108	Receiver	Differential	25 mV	TTL	±5.0	Open Collector LM55107
LM55208/LM75208	Receiver	Differential	10 mV	TTL	±5.0	10 mV Threshold LM55108
LM163/LM363	Receiver	Differential	25 mV	TTL	±5.0	TRI-STATE® LM55107
LM163A/LM363A	Receiver	Differential	10 mV	TTL	±5.0	10 mV Threshold LM163
LM55109/LM75109	Driver	Differential	TTL	6.0 mA	±5.0	Dual
LM55110/LM75110	Driver	Differential	TTL	12 mA	±5.0	12 mA LM55109
LM55121/LM75121	Driver	Common Mode	TTL	TTL	+5.0	Dual 50Ω or Coax Driver
LM55122/LM75122	Receiver	Common Mode	0.8 to 2.0	TTL	+5.0	Triple with Hysteresis
LM55123/LM75123	Driver	Common Mode	TTL	TTL	+5.0	LM55121 for IBM Interface
LM55124/LM75124	Receiver	Common Mode	0.7 to 1.7	TTL	+5.0	LM55123 for IBM Interface
DM7834/DM8834	Transceiver	Common Mode	TTL	TTL	+5.0	Quad TRI-STATE® Hysteresis
DM7835/DM8835	Transceiver	Common Mode	TTL	TTL	+5.0	DM7834 with Strobed Receiver
DM7839/DM8839	Transceiver	Common Mode	TTL	TTL	+5.0	Non-inverting DM7834
DM7833/DM8833	Transceiver	Common Mode	TTL	TTL	+5.0	DM7839 with Strobed Receiver
DM7131/DM8131	Receiver	Common Mode	0.97 to 2.65	TTL	+5.0	6-Bit Comparator with Hysteresis
DM7136/DM8136	Receiver	Common Mode	0.97 to 2.65	TTL	+5.0	Expandable DM7131
LM1488	Driver	Common Mode	TTL	±7.0V	±9 0 to 15	Quad EIA Standard RS232
LM1489	Receiver	Common Mode	0.75 to 1.5	TTL	+5.0	Quad EIA Standard RS232 with Hysteresis
LM1489A	Receiver	Common Mode	0.75 to 2.25	TTL	+5.0	Higher Noise Immunity LM1489

Note: In applications devices grouped with Comparators and Sense Amplifiers may be used at line receivers. Also devices grouped with Peripheral drivers may be used as line drivers.

For additional application information reference:

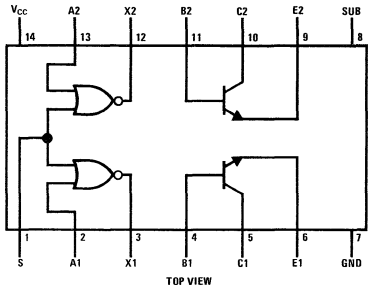
National Application Note 22, IC's for Digital Data Transmission
National Application Note 83, Data Bus and Differential Line Drivers and Receivers
National Application Note 108, Transmission Line Characteristics

Transmission Line Driver and Receiver Product Guide

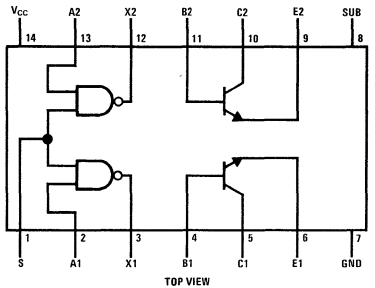
GENERAL DESCRIPTION

Series or Device Number	Nominal V_{CC} (Volts)	Output Breakdown Voltage (Volts)	Maximum Output Leakage Current (μA)	Maximum Output On Current (mA)	V_{OL} (Max) At Maximum Output Current (Volts)	Typical Propagation Delay (ns)
LM75450 Series (LM75450, LM350, LM75451, LM75452, LM75453, LM75454)	5.0	30	100	300	0.7	15
LM3611 Series (LM3611, LM3612, LM3613, LM3614)	5.0	80	100	300	0.7	130

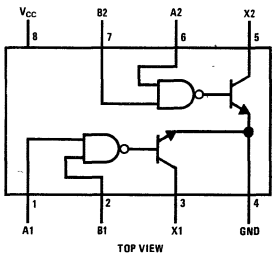
CONNECTION DIAGRAMS



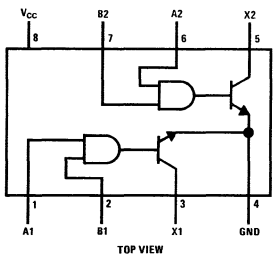
LM350



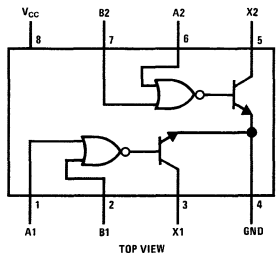
LM75450



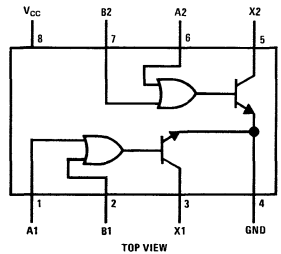
LM75451
LM3611



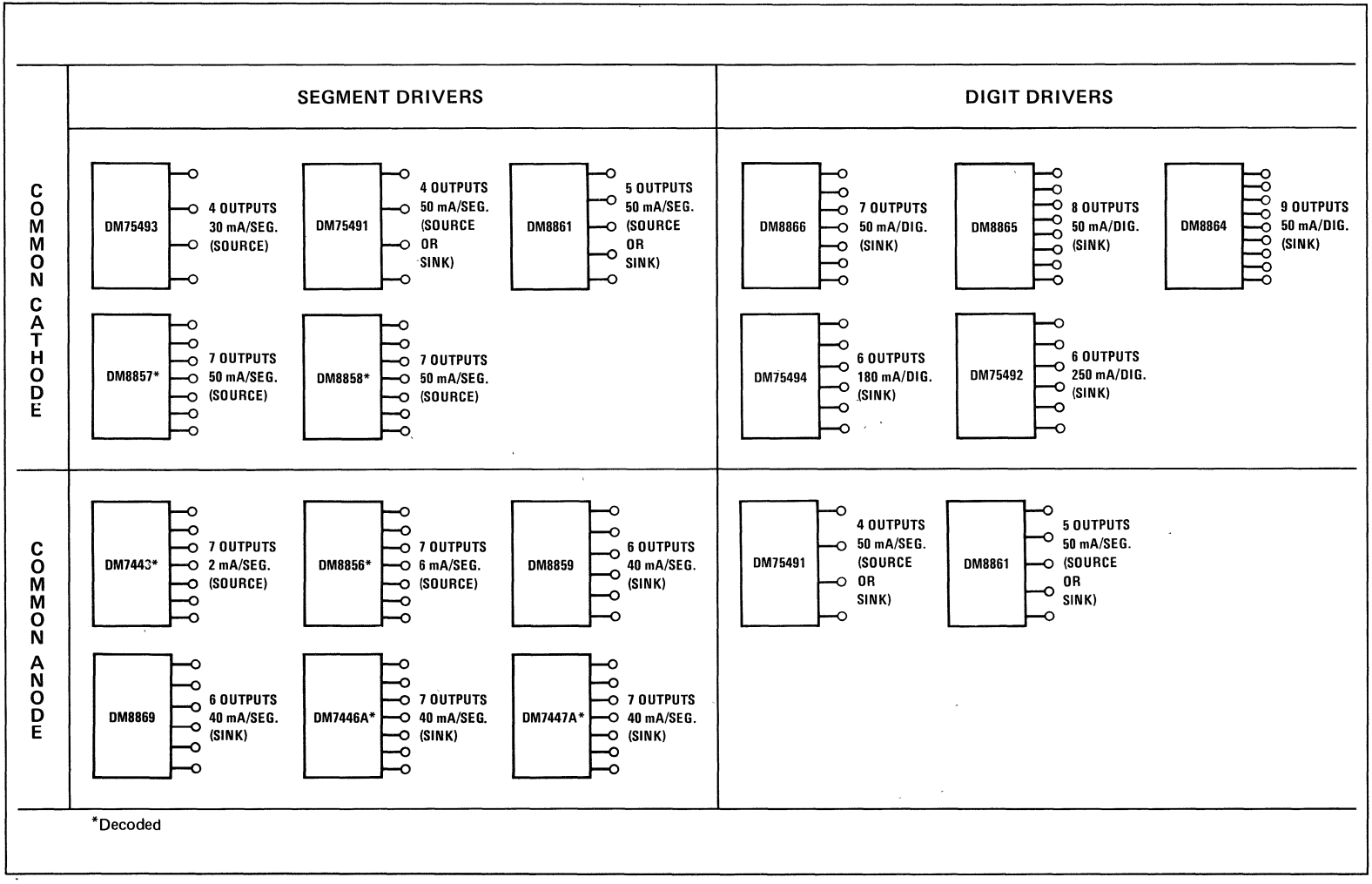
LM75452
LM3612



LM75453 (LM351)
LM3613



LM75454
LM3614



*Decoded

LED Driver Selection Guide

Analog Switch Cross Reference Guide

National also builds analog switches to custom or pin-for-pin second source requirements. Consult your local National sales office.

DEVICE NUMBER	FUNCTION	NATIONAL FUNCTIONAL EQUIVALENT
Dixon		
DAS2114	SPDT – 100 ohm	AH2114 (pin for pin)
DAS2126	SPDT – 50 ohm	AH0162
DAS2128	Quad SPST – 50 ohm	2-AH0152
DAS2132	Dual SPST – 50 ohm	AH0152
DAS2133	Dual SPST – 50 ohm	AH0152
DAS2136	Dual SPST – 50 ohm	AH0152
DAS2137	Dual SPST – 50 ohm	AH0152
Fairchild		
A3F3700 (xxx)	4CH MOS Switch	MM450 Series
A313701 (xxx)	6CH MOS MUX	AM2009
A6J3705 (xxx)	8CH MOS MUX	AM3705 (pin for pin)
A6J3708 (xxx)	8CH MOS MUX	AM3705 (pin for pin)
HAG3001 (1xx)	4PST (Obsolete)	AH0015
HAG3002 (xxx)	SPDT – 400 ohm	AH0014, AH0019
General Instrument		
MEM2009	6CH MOS MUX	AM2009 (pin for pin)
MEM2017	6CH MOS MUX	AM2009 (pin for pin)
MEM3705	8CH MUX with Decode	AM3705 (pin for pin)
NC450	Dual SPST – 500 ohm	AH0152
NC451	Dual SPST – 100 ohm	AH0134
NC2114	SPDT – 100 ohm	AH2114 (pin for pin)
NC2126	SPDT – 50 ohm	AH0162
NC2137	SPDT – 20 ohm	AH0146
Intersil		
IH5001	SPST – 30 ohm	1/2 AH0133
IH5002	SPST – 50 ohm	1/2 AH0152
IH5003	Dual SPST – 30 ohm	AH0133
IH5004	Dual SPST – 50 ohm	AH0152
IH5009 thru IH5024 Series	TTL Compatible – JFET Analog Current Switches	AH5009 thru AH5024 Series (pin for pin)
DG126 thru DG164 Series	TTL Compatible – JFET Analog Voltage Switches	AH0126 thru AH0164 Series (pin for pin – see note 1)
G114 thru G124 Series	Multiple P-MOS Transistors	MM450 thru MM454 Series and AM2009
Siliconix		
DG110	Dual SPST – 400 ohm	1/2 AH0015
DGM111	Dual SPST – 400 ohm	1/2 AH0015
DG112	Dual SPST – 400 ohm	1/2 AH0015
DG116	Obsolete – see DG172	1/2 AH0015
DG118	Obsolete – see DG172	AH0015
DG120	Obsolete – see DG502	AH0015
DG121	Obsolete – see DG502	2-AH0015
DGM122	Dual 2CH MUX – 400Ω	AH0015
DGM123	Obsolete – see DG501	AM3705

DEVICE NUMBER	FUNCTION	NATIONAL FUNCTIONAL EQUIVALENT
Siliconix (Con't)		
DG125	Obsolete – see DG501	AM3705
DG126 thru DG164 Series	TTL Compatible - JFET Analog Voltage Switches	AH0126 thru AH0164 Series (pin for pin – see note 1)
DG169	Obsolete – see DG173	AH0014
DG171	SPST – 100 ohm	AM1000
DG172	4CH MUX – 400 ohm	AH0015
DG173	DPDT – 400 ohm	AH0014
DG175	SPDT – 200 ohm	1/2 AH0015
DG181	Dual SPST – 30 ohm	AH0133
DG182	Dual SPST – 80 ohm	AH0134
DG184	Dual DPST – 30 ohm	AH0129
DG185	Dual DPST – 80 ohm	AH0126
DG187	SPDT – 30 ohm	AH0144
DG188	SPDT – 80 ohm	AH0143
DG190	Dual SPS1 – 30 ohm	2-AH0144
DG191	Dual SPDT – 80 ohm	2-AH0143
DG400 Series	Dual SPDT – 80 ohm	See note 2
DG501	8CH MUX – 200 ohm	AM3705
DG502	Dual 4CH MUX – 200 ohm	2-AH0015
DG503	8CH MUX – 400 ohm	AM3705
DG506	8CH MUX – 400 ohm	AM3705
DG507	8CH MUX – 400 ohm	AM3705
DG510	8CH MUX – 400 ohm	AM3705
DG511	Dual 4CH MUX – 400 ohm	2-AH0015
G114 thru G124 Series	Multiple P MOS Transistors	MM450 thru MM454 Series and AM2009
G125 thru G135 Series	Multiple J-FET Transistors	AH5009 thru AH5024 Series
SI3001	DPST – 500 ohm	1/2-AH0019
SI3002	SPDT – 500 ohm	1/2-AH0015
SI3705	8CH MUX – 400 ohm	AM3705 (pin for pin)
Teledyne – Crystalonics		
CAG6	SPST – 100 ohm	1/2-AH0134
CAG7	SPDT – 100 ohm	AH0143
CAG10	SPST – 500 ohm	AM1000
CAG13	Dual SPST – 500 ohm	AH0134, 1/2 AH0015
CAG14	SPST – 500 ohm	AM1000
CAG20	Dual SPST – 500 ohm	AH0134, 1/2 AH0015
CAG21	Dual DPST – 50 ohm	AH0154
CAG22	Dual DPST – 300 ohm	AH0154, AH0019
CAG23	Dual DPST – 500 ohm	AH0019
CAG24	Dual SPST – 300 ohm	AH0134, 1/2 AH0015
CAG27	Dual SPST – 100 ohm	AH0134
CAG30	SPST – 600 ohm	1/4 AH0015
CAG513	Dual SPST – 500 ohm	1/2 AH0015
CDA1	SPST – 100 ohm	1/2 AH0134
CDA2	Dual SPST – 300 ohm	1/2 AH0015
CDA4	SPST – 100 ohm	1/2 AH0134
CDA5	SPST – 200 ohm	1/2 AH0134
CDA6	SPST – 100 ohm	1/2 AH0134
CDA11	SPST – 100 ohm	1/2 AH0134
CDA18	SPST – 50 ohm	AM1000

DEVICE NUMBER	FUNCTION	NATIONAL FUNCTIONAL EQUIVALENT
Teledyne Semiconductor (Amelco)		
2107BE	SPST – 100 ohm	1/2 AH0126
2110BE	SPST – 500 ohm	1/2 AH0126
2114BF	SPDT – 100 ohm	AH2114 (pin for pin)
2126BG	SPDT – 500 ohm	AH0162
2127BG	DPST – 500 ohm	AH0152
2128BG	Quad SPST – 500 ohm	2-AH0152
2130BG	Dual SPST – 50 ohm	AH0152
2137BF	SPDT – 200 ohm	AH0146
2138BE	Dual SPST – 500 ohm	NS8035 (pin for pin)
2139BE	Dual SPST – 500 ohm	AH0152
2141BF/BH	Dual SPST – 500 ohm	AH0152
2145BE	Dual SPST – 50 ohm	AH0152
2147BE	Dual SPST – 500 ohm	AH0152
Texas Instrument		
TMS6000	10CH MOS MUX	AM3705
TMS6002	6CH MOS MUX	AM2009
TMS6005	6CH MOS MUX	AM2009
TMS6009	6CH MOS MUX	AM2009 (pin for pin)

Note 1: These devices have additional letter designations after part numbers. National's corresponding pkg and temp range codes are

Intersil & Siliconix Designations		National Designations
Letter "A"	= Military temperature range	= No letter
Letter "B"	= Industrial temperature range	= Letter "C"
Letter "L"	= Flatpack	= Letter "F"
Letter "P"	= Dual-In-Line	= Letter "D"

Examples

DG129AL	= AH0129F (pin for pin)
DG134BP	= AH0134CD (pin for pin)

Note 2. "400" series used to denote industrial temperature range product Coding was changed to use "100" series and letter "B"

Example DG426 ≡ DG126B ≡ AH0126C

Voltage Comparators

LF111/LF211/LF311 voltage comparators

general description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

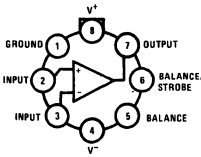
Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents.

advantages

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

connection diagrams*

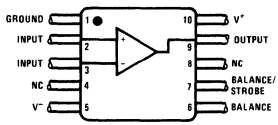
Metal Can Package



NOTE Pin 4 connected to case
TOP VIEW

Order Number LF111H, LF211H or LF311H
See Package 11

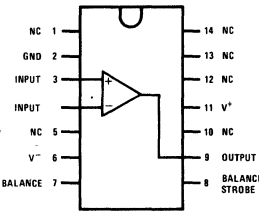
Flat Package



NOTE Pin 5 connected to bottom of package
TOP VIEW

Order Number LF111F
See Package 3

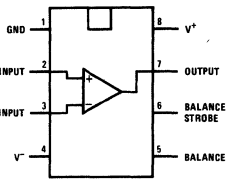
Dual-In-Line Package



Note Pin 6 connected to bottom of package
TOP VIEW

Order Number LF111D, LF211D or LF311D
See Package 1
Order Number LF311N-14
See Package 22

Dual-In-Line Package

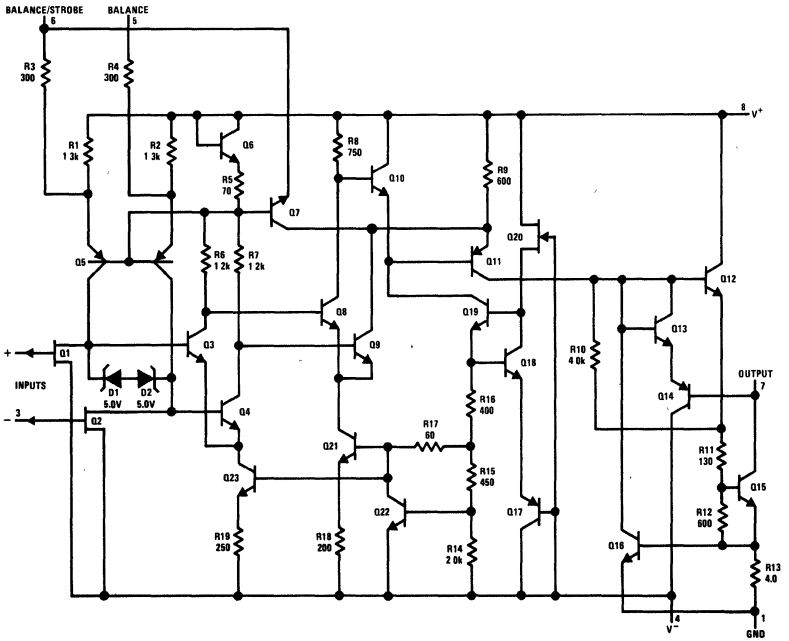


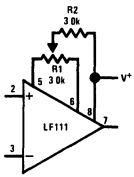
TOP VIEW

Order Number LF311N
See Package 20

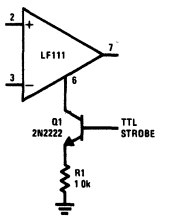
*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

schematic diagram and auxiliary circuits

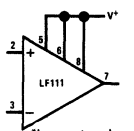




Offset Balancing



Strobing



*Increases typical common mode slew from 7.0V/μs to 18V/μs.

Increasing Input Stage Current*

absolute maximum ratings

	LF111/LF211	LF311
Total Supply Voltage (V_{84})	36V	36V
Output to Negative Supply Voltage (V_{74})	50V	40V
Ground to Negative Supply Voltage (V_{14})	30V	30V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 1)	±15V	±15V
Power Dissipation (Note 2)	500 mW	500 mW
Output Short Circuit Duration	10 seconds	10 seconds
Operating Temperature Range		
LF111	−55°C to +125°C	
LF211	−25°C to +85°C	
LF311		0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

electrical characteristics (LF111/LF211) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, R_S		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	25	pA
Input Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		20	50	pA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5.0$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5.0$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)				6.0	mV
Input Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		2.0	3.0	nA
Input Bias Current	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		5.0	7.0	nA
Input Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6.0$ mV, $I_{SINK} \leq 8.0$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5.0$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of +185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is +100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 mV supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

electrical characteristics (LF311) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
nput Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	10	mV
nput Offset Current (Note 4)	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		5.0	75	pA
nput Bias Current	$T_A = 25°C$, $V_{CM} = 0$ (Note 6)		25	150	pA
oltage Gain	$T_A = 25°C$		200		V/mV
esponse Time (Note 5)	$T_A = 25°C$		200		ns
aturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
trobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	10	nA
nput Offset Voltage (Note 4)	$R_S \leq 50k$			15	mV
nput Offset Current (Note 4)	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		1.0		nA
nput Bias Current	$V_S = \pm 15V$, $V_{CM} = 0$ (Note 6)		3.0		nA
nput Voltage Range			+14 −13.5		V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8.0$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit s equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is +150°C, the LF211 is +110°C and the LF311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of +185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is +100°C/W, junction to ambient.

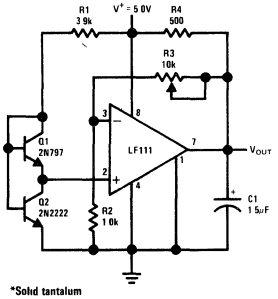
Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq +125°C$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and for the LF311 $0°C \leq T_A \leq +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 mV supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

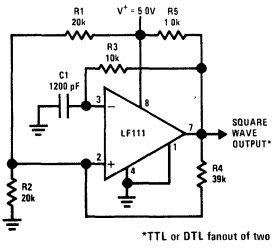
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

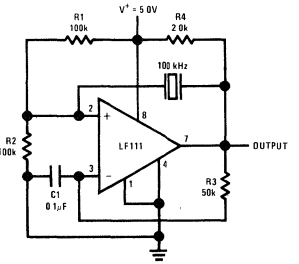
typical applications



Low Voltage Adjustable Reference Supply



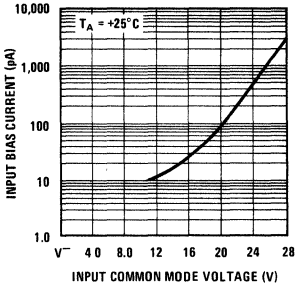
100 kHz Free Running Multivibrator



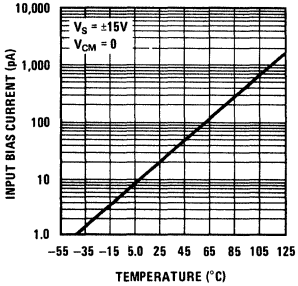
Crystal Oscillator

typical performance

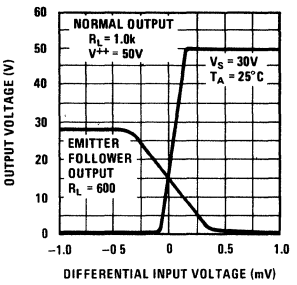
Input Bias Current vs Common Mode



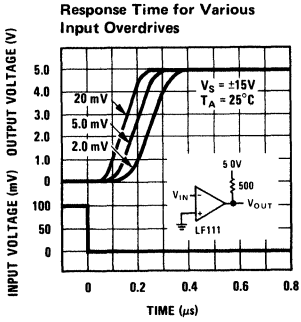
Input Bias Current vs Temperature



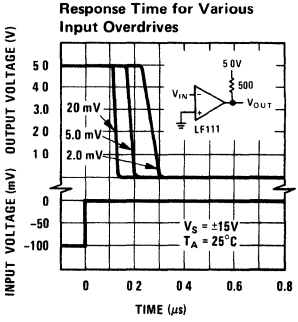
Transfer Function



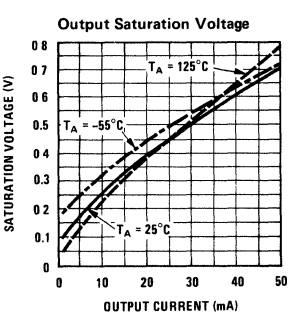
Response Time for Various Input Overdrives



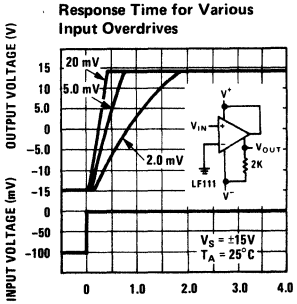
Response Time for Various Input Overdrives



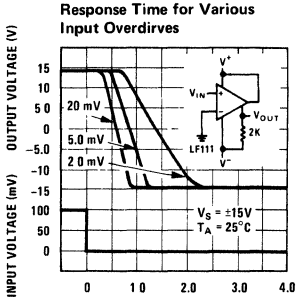
Output Saturation Voltage



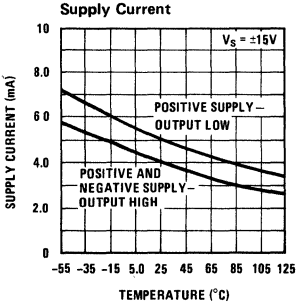
Response Time for Various Input Overdrives



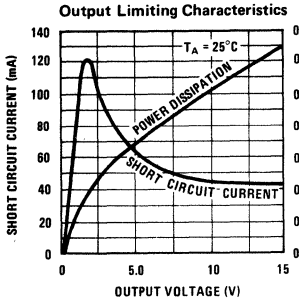
Response Time for Various Input Overdirves



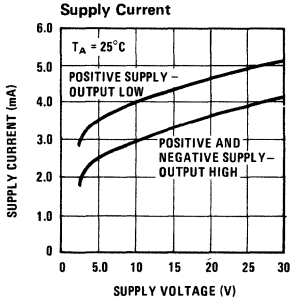
Supply Current



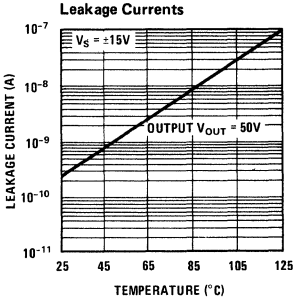
Output Limiting Characteristics



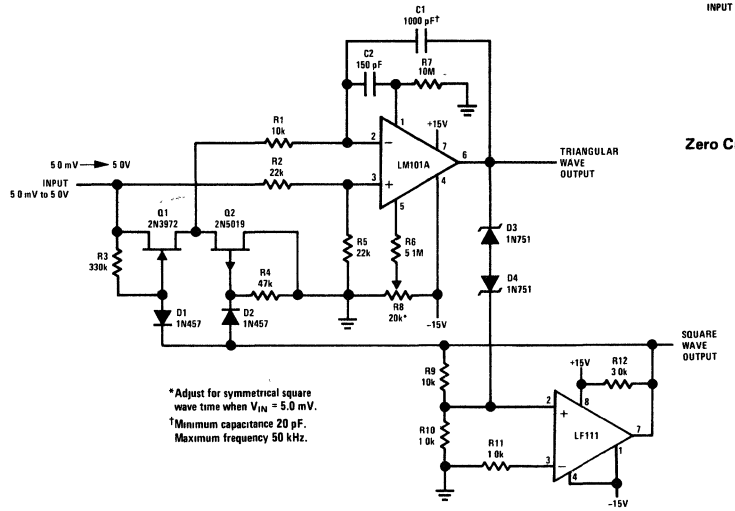
Supply Current



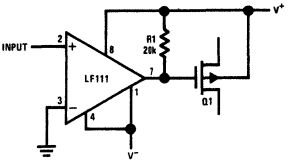
Leakage Currents



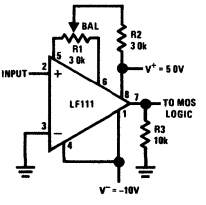
typical applications (con't)



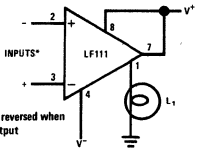
10 Hz to 10 kHz Voltage Controlled Oscillator



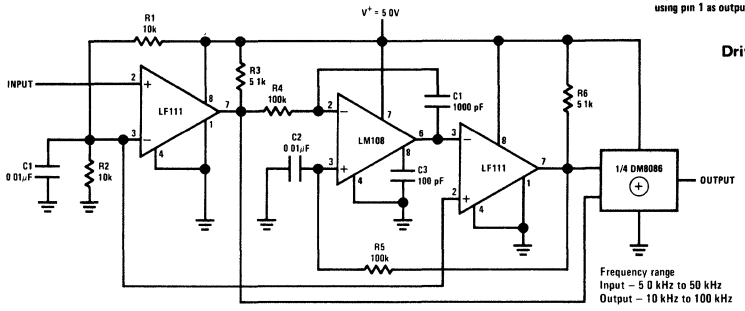
Zero Crossing Detector Driving MOS Switch



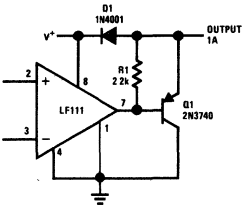
Zero Crossing Detector Driving MOS Logic



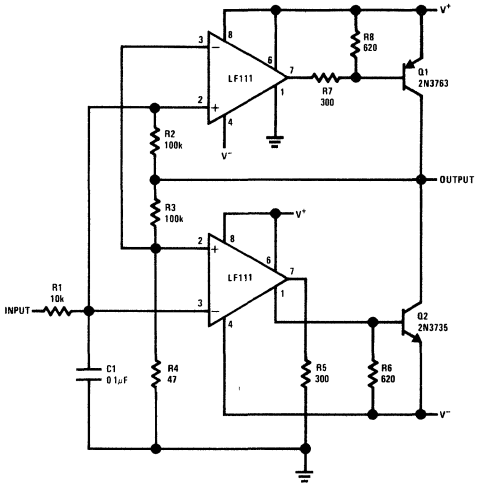
Driving Ground-Referred Load



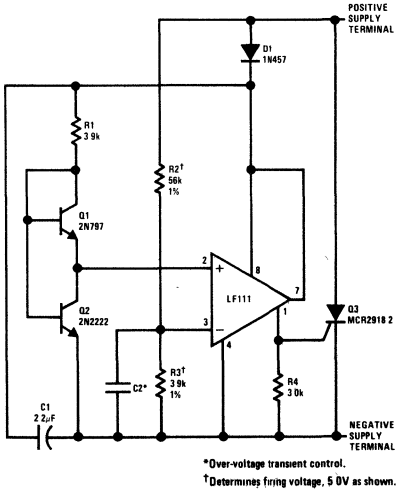
Frequency Doubler



Comparator and Solenoid Driver

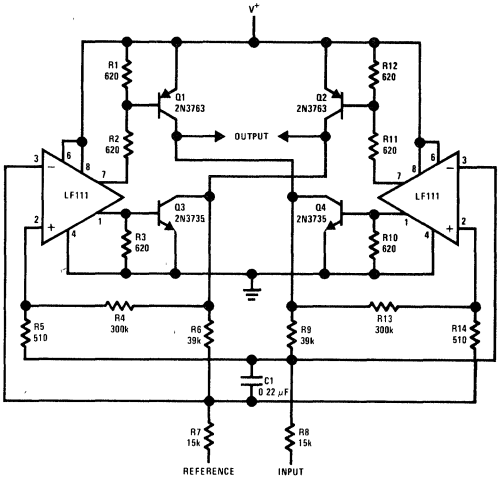


Switching Power Amplifier

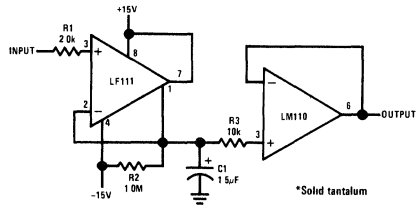


Crowbar Over-Voltage Protector

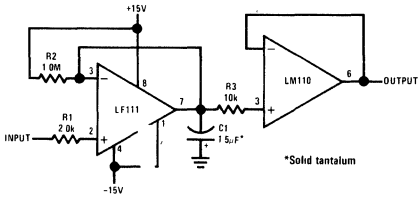
typical applications (con't)



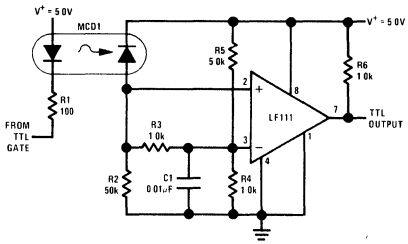
Switching Power Amplifier



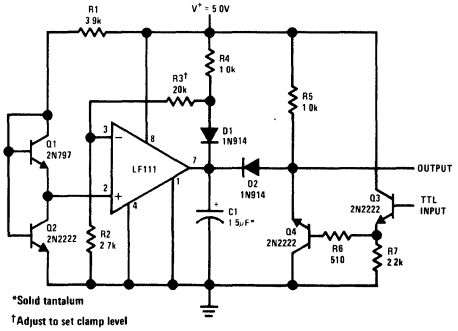
Positive Peak Detector



Negative Peak Detector

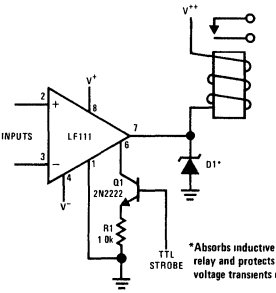


Digital Transmission Isolator



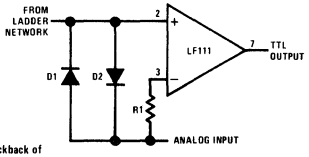
*Solid tantalum
†Adjust to set clamp level

Precision Squarer

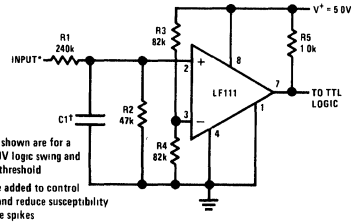


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line

Relay Driver with Strobe

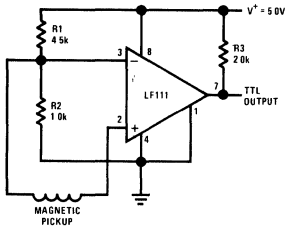


Using Clamp Diodes to Improve Response

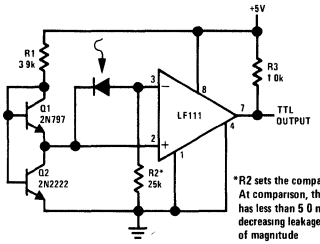


*Values shown are for a 0 to 30V logic swing and a 15V threshold
†May be added to control speed and reduce susceptibility to noise spikes

TTL Interface with High Level Logic

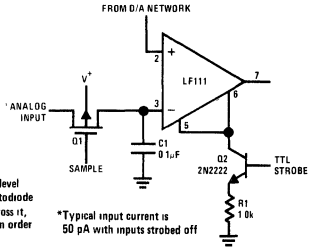


Detector for Magnetic Transducer



*R2 sets the comparison level At comparison, the photodiode has less than 5 0 mV across it, decreasing leakages by an order of magnitude

Precision Photodiode Comaprator



*Typical input current is 50 pA with inputs strobed off

Strobing Off Both Input* and Output Stages

Voltage Comparators

LH2111/LH2211/LH2311 dual voltage comparator

general description

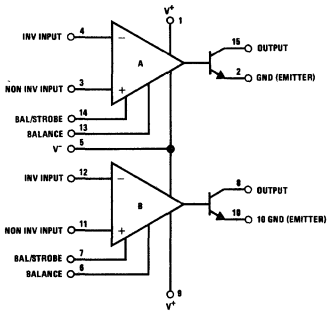
The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

The LH2111 is specified for operation over the −55°C to +125°C military temperature range. The LH2211 is specified for operation over the −25°C to +85°C temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

features

- Wide operating supply range — ±15V to a single +5V
- Low input currents — 6 nA
- High sensitivity — 10 μV
- Wide differential input range — ±30V
- High output drive — 50 mA, 50V

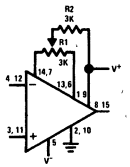
connection diagram



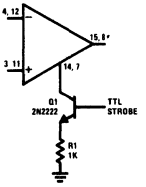
Order Number LH2111D, LH2211D or LH2311D
See Package 2

Order Number LH2111F, LH2211F or LH2311F
See Package 5

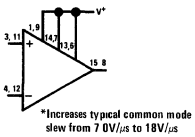
auxiliary circuits



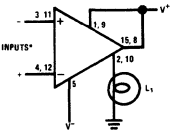
Offset Balancing



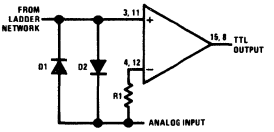
Strobing



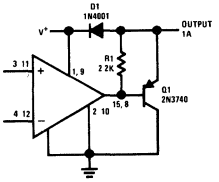
Increasing Input Stage Current*



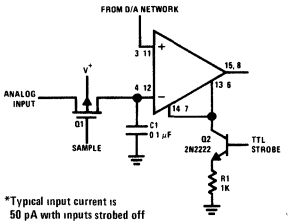
Driving Ground-Referred Load



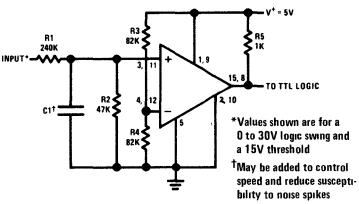
Using Clamp Diodes to Improve Responses



Comparator and Solenoid Driver



Strobing off Both Input* and Output Stages



TTL Interface with High Level Logic

absolute maximum ratings

Total Supply Voltage ($V^+ - V^-$)	36V	Output Short Circuit Duration	10 sec
Output to Negative Supply Voltage ($V_{OUT} - V^-$)	50V	Operating Temperature Range LH2111	−55°C to 125°C
Ground to Negative Supply Voltage (GND − V^-)	30V	LH2211	−25°C to 85°C
Differential Input Voltage	±30V	LH2311	0°C to 70°C
Input Voltage (Note 1)	±15V	Storage Temperature Range	−65°C to 150°C
Power Dissipation (Note 2)	500 mW	Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics — each side (Note 3)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2111	LH2211	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$	3.0	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	100	250	nA Max
Voltage Gain	$T_A = 25°C$	200	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	200	ns Typ
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$	1.5	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	3.0	n A Typ
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$	10	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leq 50k$	4.0	4.0	10	mV Max
Input Offset Current (Note 4)		20	20	70	nA Max
Input Bias Current		150	150	300	nA Max
Input Voltage Range		±14	±14	±14	V Typ
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -5$ mV, $I_{SINK} \leq 8$ mA	0.4	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	5.0	mA Max

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$ for the LH2111, $-25°C \leq T_A \leq 85°C$ for the LH2211, and $0°C \leq T_A \leq 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10$ mV.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Voltage Comparators

LM106/LM206 voltage comparator

general description

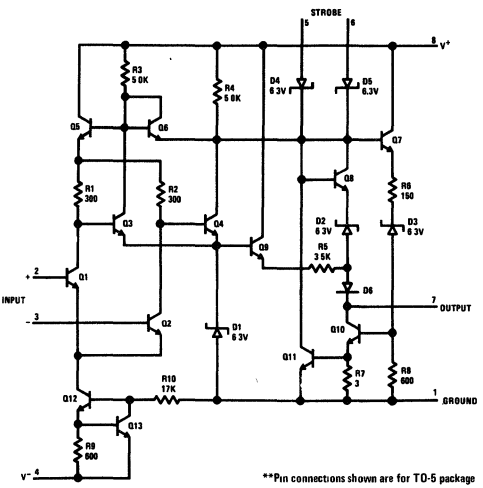
The LM106 and LM206 are high-speed voltage comparators designed to accurately detect low-level analog signals and drive a digital load. They are equivalent to an LM710, combined with a two input NAND gate and an output buffer. The circuits can drive RTL, DTL or TTL integrated circuits directly. Furthermore, their outputs can switch voltages up to 24V at currents as high as 100 mA. Other features include:

- Improved accuracy: 2 mV maximum worst case offset.
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710.
- 40 ns maximum response time

The devices have short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts to the positive supply. The speed is equivalent to that of an LM710. However, they are even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM106 and LM206. They can also be operated from any negative supply voltage between −3V and −12V with little effect on performance.

The LM106 is specified for operation over the −55°C to +125°C military temperature range. The LM206 is specified for operation over the −25°C to +85°C temperature range.

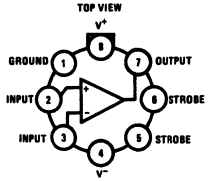
schematic and connection diagrams * *



**Pin connections shown are for TO-5 package

Metal Can

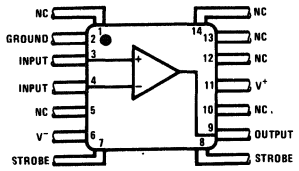
TOP VIEW



Note Pin 4 connected to case

Order Number LM106H or LM206H
See Package 11

Flat Package



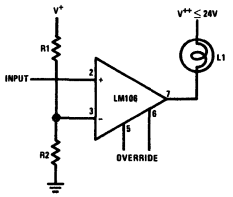
Note. Pin 6 connected to bottom of package

TOP VIEW

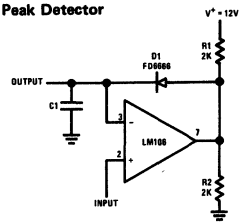
Order Number LM106F or LM206F
See Package 4

typical applications * *

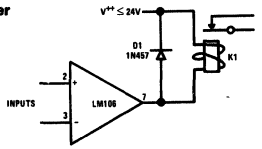
Level Detector and Lamp Driver



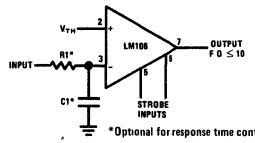
Fast Response Peak Detector



Relay Driver



Adjustable Threshold Line Receiver



*Optional for response time control

absolute maximum ratings

Positive Supply Voltage	15V	Power Dissipation (Note 1)	600 mW
Negative Supply Voltage	−15V	Output Short Circuit Duration	10 sec
Output Voltage	24V	Operating Temperature Range LM106	−55°C to 125°C
Output to Negative Supply Voltage	30V	LM206	−25°C to 85°C
Differential Input Voltage	±5V	Storage Temperature Range	−65°C to 150°C
Input Voltage	±7V	Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 3		0.5	2.0	mV
Input Offset Current	Note 3		0.7	3.0	μA
Input Bias Current			10	20	μA
Response Time	Note 4, R_L = 390Ω to +5V, C_L = 15 pF		28	40	ns
Saturation Voltage	$V_{IN} \leq -5$ mV, I_{OUT} = 100 mA		1 0	1.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8V \leq V_{OUT} \leq 24V$		0 02	1 0	μA

electrical characteristics

The following specifications apply for $T_L \leq T_A \leq T_H$ (Note 5)

Input Offset Voltage	Note 3			3 0	mV
Average Temperature Coefficient of Input Offset Voltage			3 0	10	μV/°C
Input Offset Current	Note 3, $T_L \leq T_A \leq 25°C$		1.8	7.0	μA
	$25°C \leq T_A \leq T_H$		0.25	3.0	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_H$		5.0	25	nA/°C
	$T_L \leq T_A \leq 25°C$		15	75	nA/°C
Input Bias Current	$T_L \leq T_A \leq 25°C$			45	μA
	$25°C \leq T_A \leq T_H$			20	μA
Input Voltage Range	$-7V \geq V^- \geq -12V$	±5.0			V
Differential Input Voltage Range		±5.0			V
Saturation Voltage	$V_{IN} \leq -5$ mV, I_{OUT} = 50 mA			1.0	V
Saturation Voltage	$V_{IN} \leq -5$ mV, I_{OUT} = 16 mA			0.4	V
Positive Output Level	$V_{IN} \geq 5$ mV, I_{OUT} = −400 μA	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8V \leq V_{OUT} \leq 24V$, $T_L \leq T_A \leq 25°C$			1 0	μA
	$25°C < T_A \leq T_H$			100	μA
Strobe Current	V_{strobe} = 0.4V		−1 7	−3.2	mA
Strobe ON Voltage		0.9	1.4		V
Strobe OFF Voltage	$I_{sink} \leq 16$ mA		1 4	2.2	V
Positive Supply Current	V_{IN} = −5 mV		5 5	10	mA
Negative Supply Current			−1.5	−3.6	mA

Note 1: The maximum junction temperature of the LM106 is +150°C, while that of the LM206 is +110°C For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of +185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0 03-inch-wide, 2-ounce copper conductors.

Note 2: These specifications apply for $-3.0V \geq V^- \geq -12V$, V^+ = 12V and T_A = +25°C unless otherwise specified All currents into device pins are considered positive.

Note 3: The offset voltages and offset currents given are the maximum values required to drive the output down to 0.5V or up to 5.0V. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain, specified supply voltage variations, and common mode voltage variations

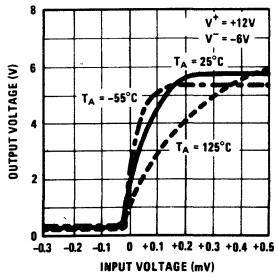
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 5: All currents into device pins are considered positive.

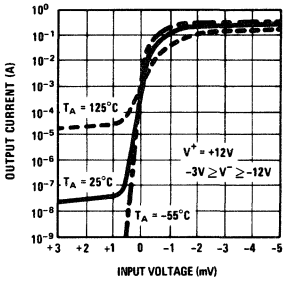
	T_L	T_H
LM106	−55°C	+125°C
LM206	−25°C	+85°C

typical performance characteristics

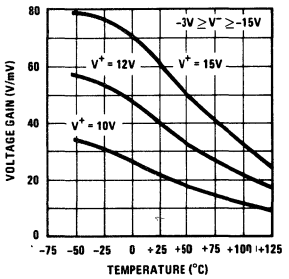
Transfer Function



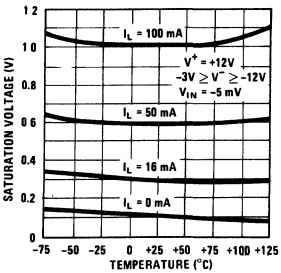
Transconductance



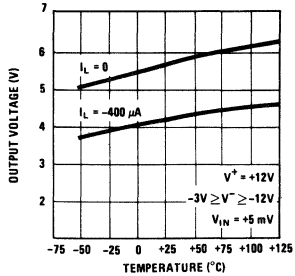
Voltage Gain



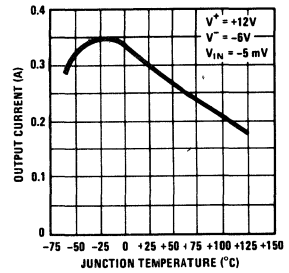
Saturation Voltage



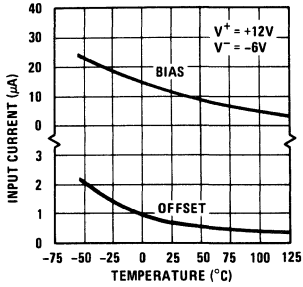
Positive Output Level



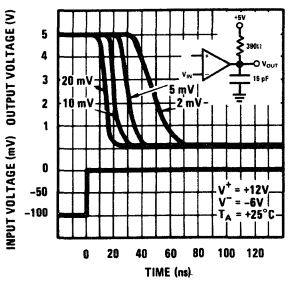
Short Circuit Output Current



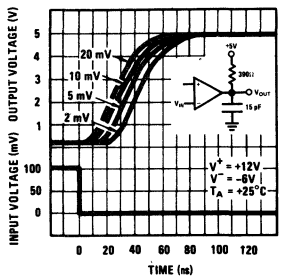
Input Current



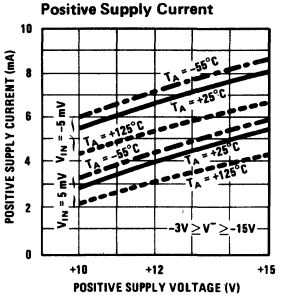
Response Time For Various Input Overdrives



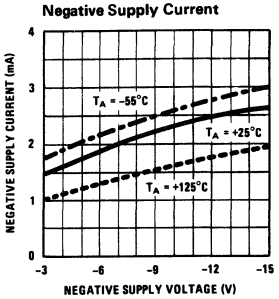
Response Time For Various Input Overdrives



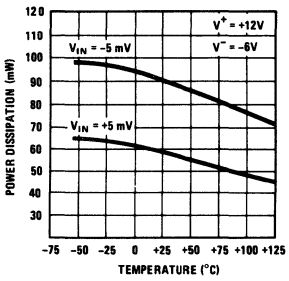
Positive Supply Current



Negative Supply Current



Power Consumption



Voltage Comparators

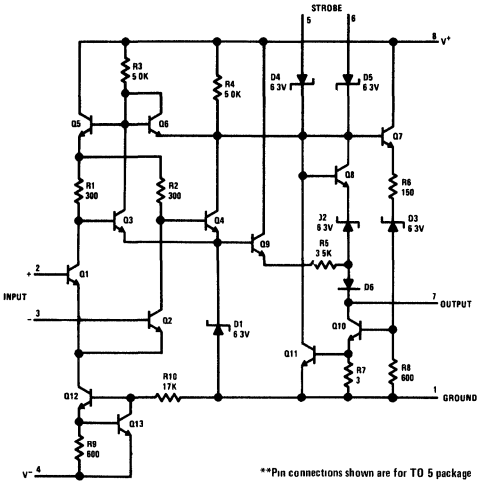
LM306 voltage comparator/buffer general description

The LM306 is a high-speed voltage comparator designed to accurately detect low-level analog signals and drive a digital load. It is equivalent to an LM710C, combined with a two input NAND gate and an output buffer. The circuit can drive RTL, DTL or TTL integrated circuits directly. Furthermore, the output can switch voltages up to 24V at currents as high as 100 mA. Other features include:

- Improved accuracy: 5 mV (max) offset
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710C.
- 40 ns maximum response time

The device has short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts. The speed is equivalent to that of an LM710C. However, it is even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM306. It can also be operated from any negative supply voltage between −3V and −12V with little effect on performance. The LM306 is identical to the LM106, except that it is specified over a 0°C to 70°C temperature range.

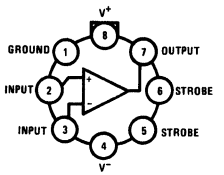
schematic and connection diagrams**



**Pin connections shown are for TO 5 package

Metal Can

TOP VIEW



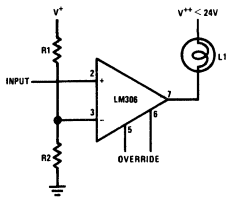
Note Pin 4 connected to case

Order Number LM306H

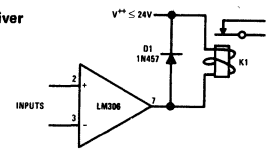
See Package 11

typical applications**

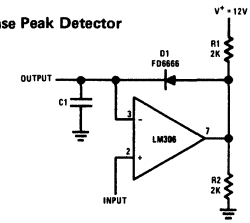
Level Detector and Lamp Driver



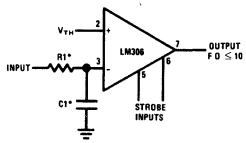
Relay Driver



Fast Response Peak Detector



Adjustable Threshold Line Receiver



*Optional for response time control

absolute maximum ratings

Positive Supply Voltage	15V
Negative Supply Voltage	−15V
Output Voltage	24V
Output to Negative Supply Voltage	30V
Differential Input Voltage	±5V
Input Voltage	±7V
Power Dissipation (Note 1)	600 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Note 3		1.6	5.0	mV
Input Offset Current	Note 3		1.8	5.0	μA
Input Bias Current			16	25	μA
Response Time	Note 4, R_L = 390Ω to +5V, C_L = 15 pF		28	40	ns
Saturation Voltage	$V_{IN} \leq -7$ mV, I_{OUT} = 100 mA		0.8	2.0	V
Output Leakage Current	$V_{IN} \geq 7$ mV, $8V \leq V_{OUT} \leq 24V$		0.02	2.0	μA

electrical characteristics

The following specifications apply for $0°C \leq T_A \leq 70°C$ (Note 5)

Input Offset Voltage	Note 3			6.5	mV
Average Temperature Coefficient of Input Offset Voltage			5	20	μV/°C
Input Offset Current	Note 3, $0°C \leq T_A < 25°C$		2 4	7.5	μA
	$25°C \leq T_A \leq 70°C$			5 0	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$		15	50	nA/°C
	$0°C \leq T_A \leq 25°C$		24	100	nA/°C
Input Bias Current	$0°C \leq T_A < 25°C$		25	40	μA
	$25°C \leq T_A \leq 70°C$			25	μA
Input Voltage Range	$-7V \geq V^- \geq -12V$	±5.0			V
Differential Input Voltage Range		±5 0			V
Saturation Voltage	$V_{IN} \leq -8$ mV, I_{OUT} = 50 mA			1.0	V
Saturation Voltage	$V_{IN} \leq -8$ mV, I_{OUT} = 16 mA			0.4	V
Positive Output Level	$V_{IN} \geq 8$ mV, $I_{OUT} = -400$ μA	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 8$ mV, $8V \leq V_{OUT} \leq 24V$				
	$0°C \leq T_A \leq 25°C$			2.0	μA
	$25°C < T_A \leq 70°C$			100	μA
Strobe Current	V_{strobe} = 0.4V		−1.7	−3.2	mA
Strobe ON Voltage		0.9	1.4		V
Strobe OFF Voltage	$I_{sink} \leq 16$ mA		1.4	2 2	V
Positive Supply Current	V_{IN} = −8 mV		5.5	10	mA
Negative Supply Current			−1.5	−3.6	mA

Note 1: For operating at elevated temperatures, the device must be derated based on a 85°C maximum junction temperature and a thermal resistance of 45°C/W junction to case or 150°C/W junction to ambient.

Note 2: These specifications apply for $-3V \geq V^- \geq -12V$, V^+ = 12V and T_A = 25°C unless otherwise specified All currents into pins are considered positive

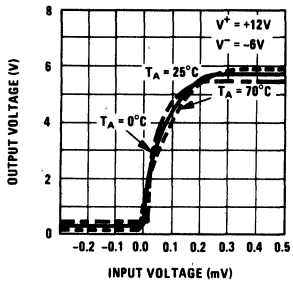
Note 3. The offset voltages and offset currents given are the maximum values required to drive the output down to 0 5V or up to 5 0V Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain, and input impedance, specified supply voltage variations, and common mode voltage variations

Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive

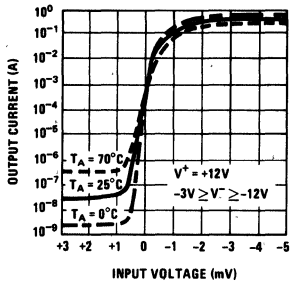
Note 5. All currents into device pins are considered positive

typical performance characteristics

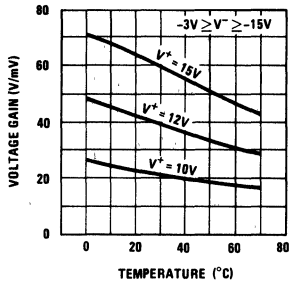
Transfer Function



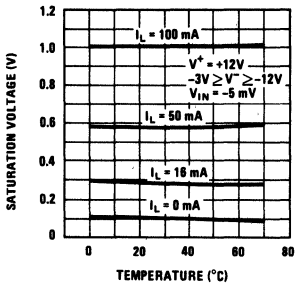
Transconductance



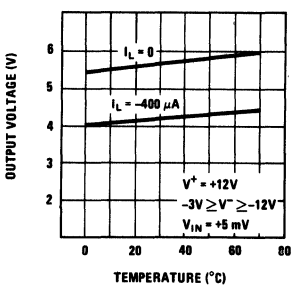
Voltage Gain



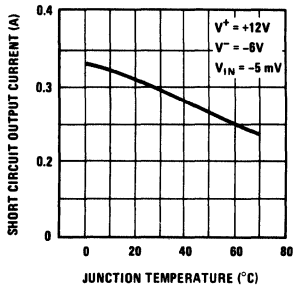
Saturation Voltage



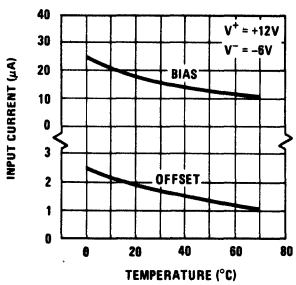
Positive Output Level



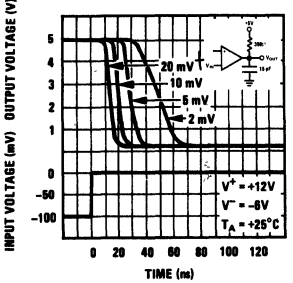
Short Circuit Output Current



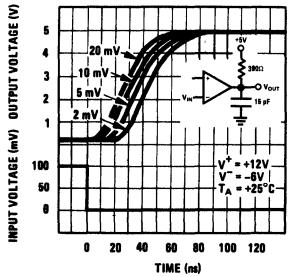
Input Current



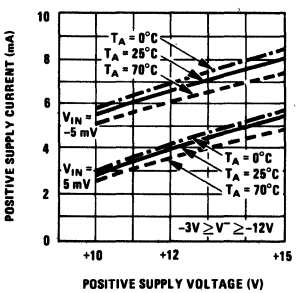
Response Time for Various Input Overdrives



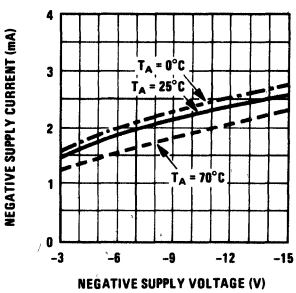
Response Time for Various Input Overdrives



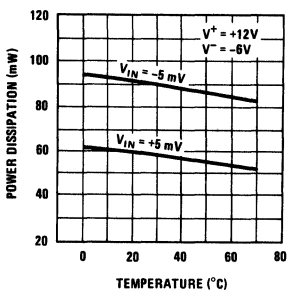
Positive Supply Current



Negative Supply Current



Power Dissipation



Voltage Comparators

LM111/LM211 voltage comparator

general description

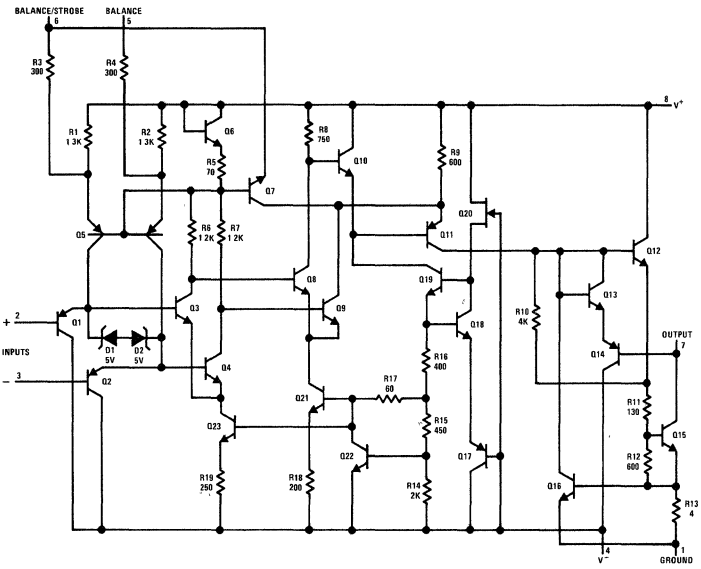
The LM111 and LM211 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA. Outstanding characteristics include:

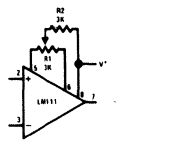
- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

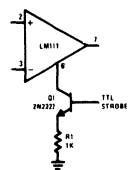
Both the inputs and the outputs of the LM111 or the LM211 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

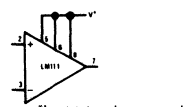
The LM211 is identical to the LM111, except that its performance is specified over a −25°C to 85°C temperature range instead of −55°C to 125°C.

schematic diagram and auxiliary circuits**



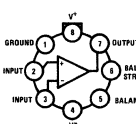






connection diagrams

Metal Can

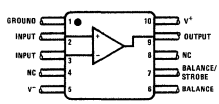


Note. Pin 4 connected to case

TOP VIEW

Order Number
LM111H or LM211H
See Package 11

Flat Package

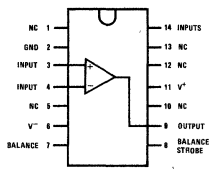


Note Pin 5 connected to bottom of package

TOP VIEW

Order Number
LM111F or LM211F
See Package 3

Dual-In-Line



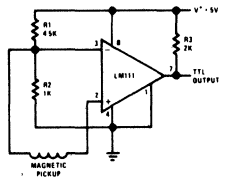
Note Pin 6 connected to bottom of package

TOP VIEW

Order Number
LM111D or LM211D
See Package 1

**Pin connections shown are for metal can

typical applications



Detector for Magnetic Transducer

absolute maximum ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LM111	−55°C to 125°C
LM211	−25°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10	nA
Input Bias Current	$T_A = 25°C$		60	100	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	10	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			4.0	mV
Input Offset Current (Note 4)				20	nA
Input Bias Current				150	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5	μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

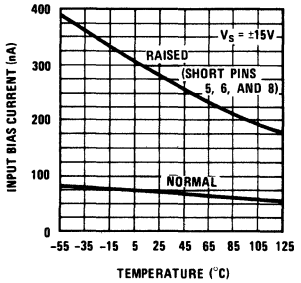
Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

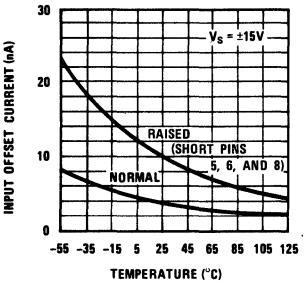
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

typical performance characteristics

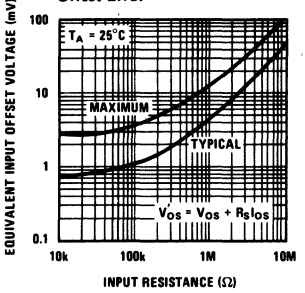
Input Bias Current



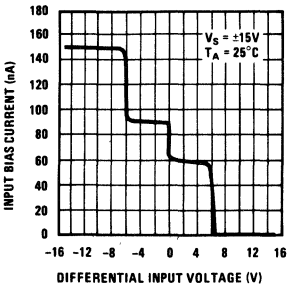
Input Offset Current



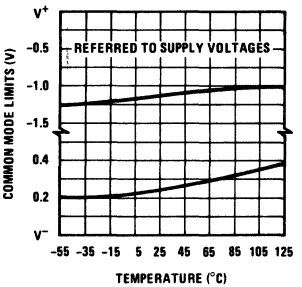
Offset Error



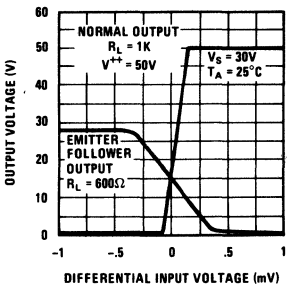
Input Characteristics



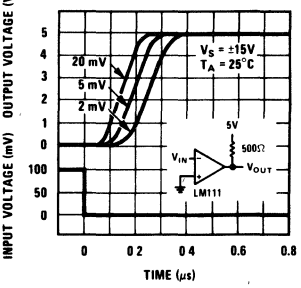
Common Mode Limits



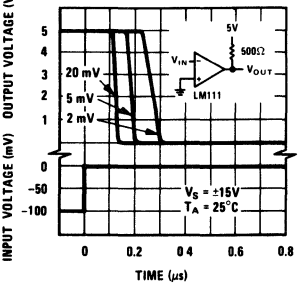
Transfer Function



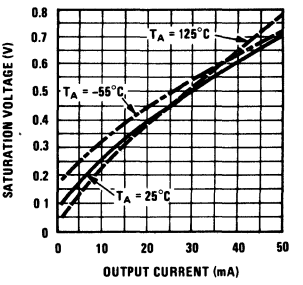
Response Time for Various Input Overdrives



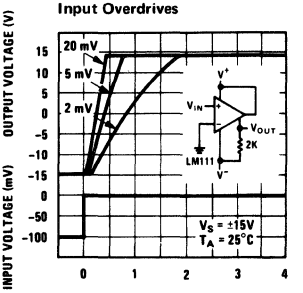
Response Time for Various Input Overdrives



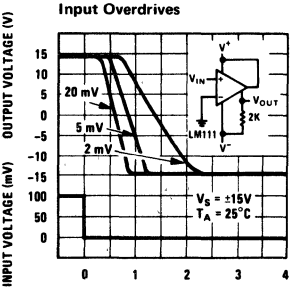
Output Saturation Voltage



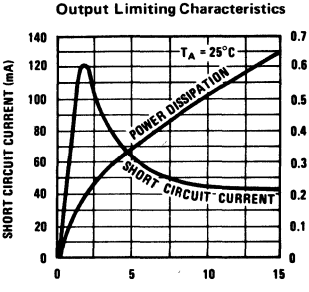
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

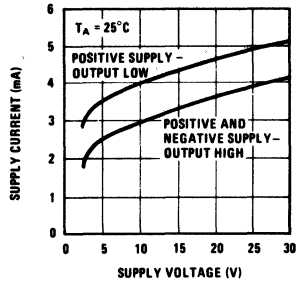


Output Limiting Characteristics

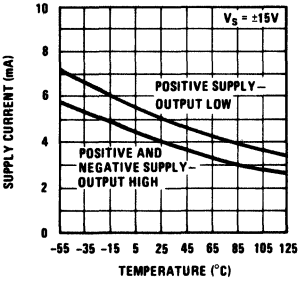


typical performance characteristics (con't)

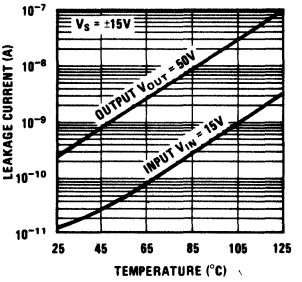
Supply Current



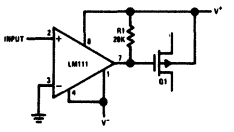
Supply Current



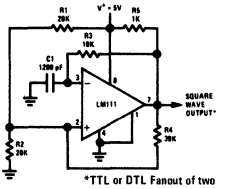
Leakage Currents



typical applications (con't)

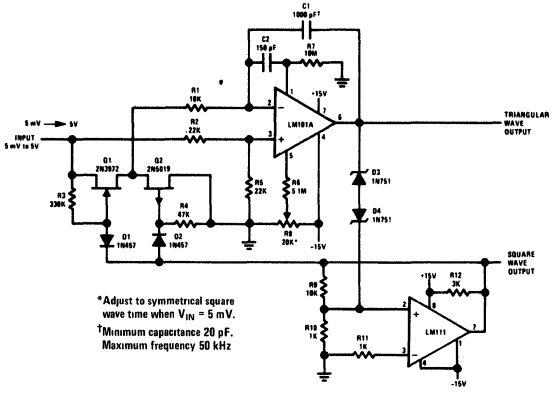


Zero Crossing Detector Driving MOS Switch



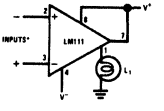
*TTL or DTL Fanout of two

100 kHz Free Running Multivibrator



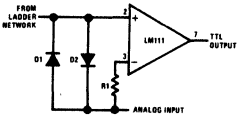
*Adjust to symmetrical square wave time when V_{IN} = 5 mV.
†Minimum capacitance 20 pF. Maximum frequency 50 kHz

10 Hz to 10 kHz Voltage Controlled Oscillator

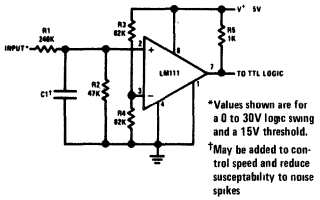


*Input polarity is reversed when using pin 1 as output

Driving Ground-Referred Load

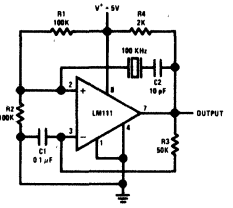


Using Clamp Diodes to Improve Response

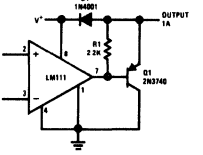


*Values shown are for a 0 to 30V logic swing and a 15V threshold.
†May be added to control speed and reduce susceptability to noise spikes

TTL Interface with High Level Logic

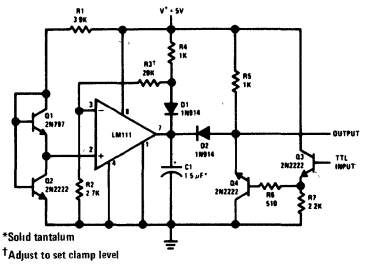


Crystal Oscillator



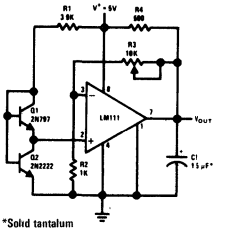
Comparator and Solenoid Driver

typical applications (con't)



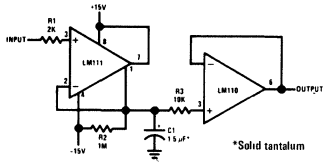
*Solid tantalum
†Adjust to set clamp level

Precision Squarer



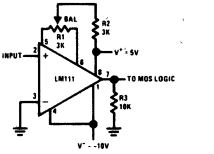
*Solid tantalum

Low Voltage Adjustable Reference Supply

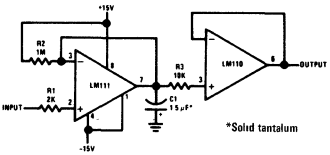


*Solid tantalum

Positive Peak Detector

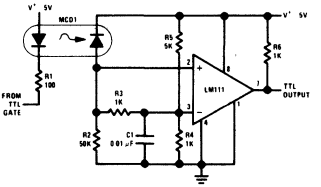


Zero Crossing Detector driving MOS logic

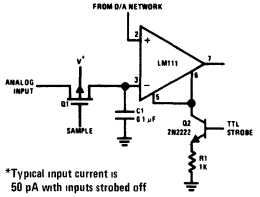


*Solid tantalum

Negative Peak Dectector

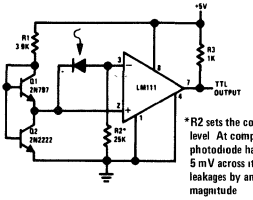


Digital Transmission Isolator



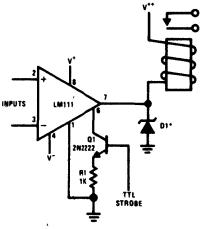
*Typical input current is 50 pA with inputs strobed off

Strobing off Both Input* and Output Stages



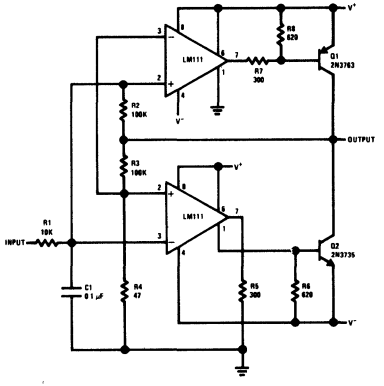
*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude

Precision Photodiode Comparator

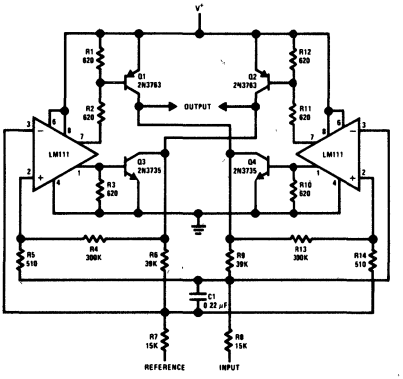


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line

Relay Driver with Strobe



Switching Power Amplifier



Switching Power Amplifier

Voltage Comparators

LM311 voltage comparator

general description

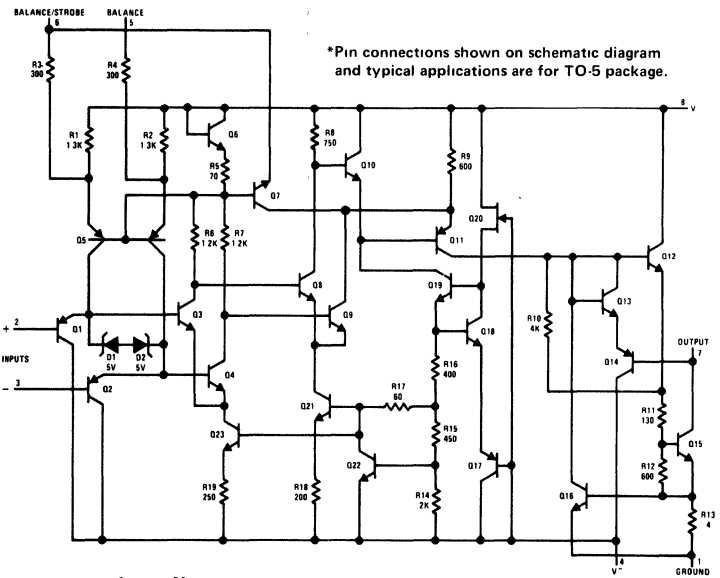
The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA

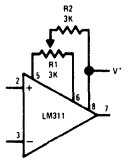
features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

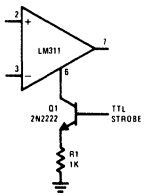
Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C.

schematic diagram and auxiliary circuits*

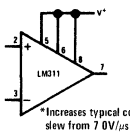




Offset Balancing



Strobing

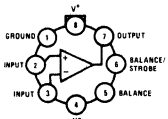


*Increases typical common mode slew from 7 0V/μs to 18V/μs

Increasing Input Stage Current*

connection diagrams

Metal Can

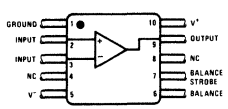


Note Pin 4 connected to case

TOP VIEW

Order Number LM311H
See Package 11

Flat Package

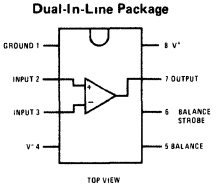


Note Pin 5 connected to bottom of package

TOP VIEW

Order Number LM311F
See Package 3

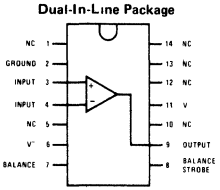
Dual-In-Line Package



TOP VIEW

Order Number LM311N
See Package 20

Dual-In-Line Package



Note Pin 6 connected to bottom of package

TOP VIEW

Order Number LM311D
See Package 1

Order Number LM311N-14
See Package 22

absolute maximum ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50K$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50K$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies The positive input voltage limit is 30V above the negative supply The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

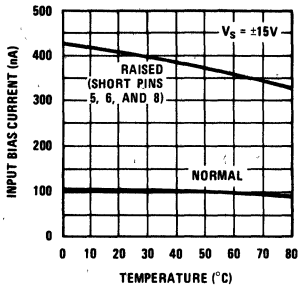
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C < T_A < 70°C$, unless otherwise specified The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

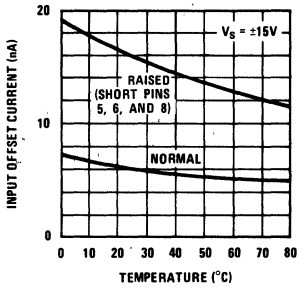
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

typical performance characteristics

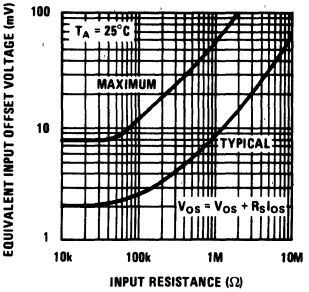
Input Bias Current



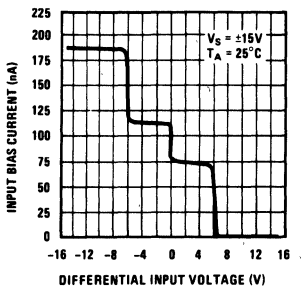
Input Offset Current



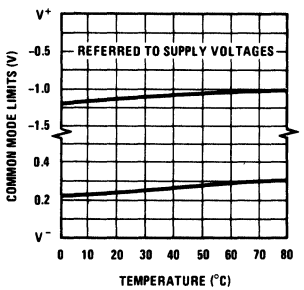
Offset Error



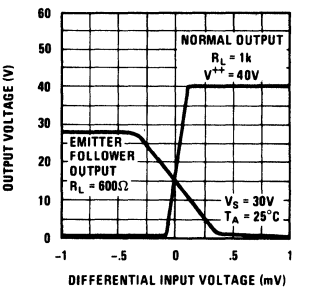
Input Characteristics



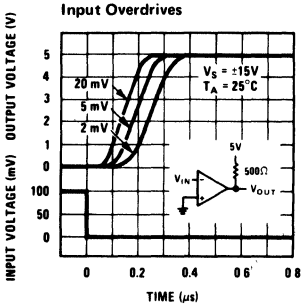
Common Mode Limits



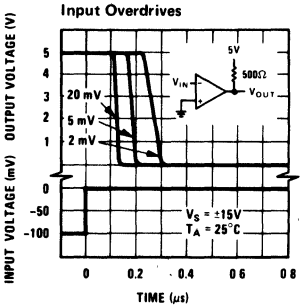
Transfer Function



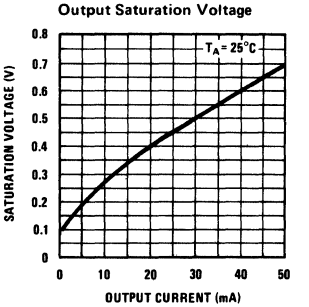
Response Time for Various Input Overdrives



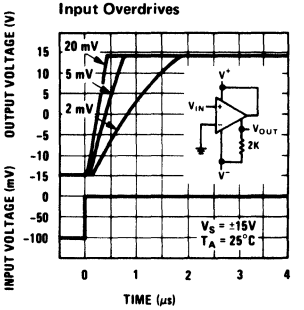
Response Time for Various Input Overdrives



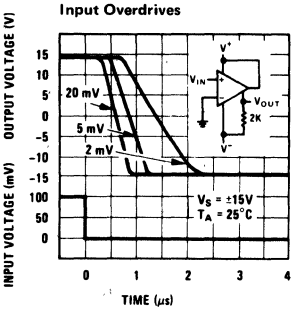
Output Saturation Voltage



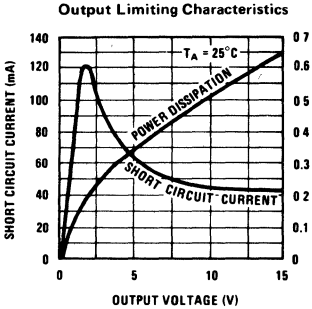
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

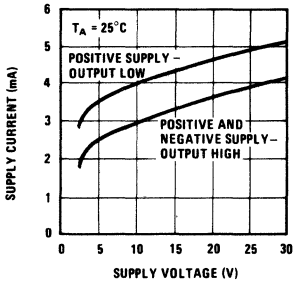


Output Limiting Characteristics

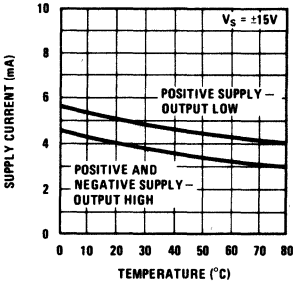


typical performance characteristics (con't)

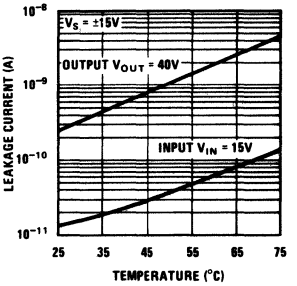
Supply Current



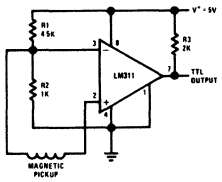
Supply Current



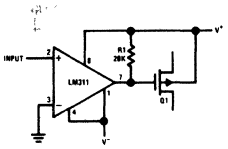
Leakage Currents



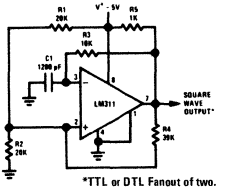
typical applications



Detector for Magnetic Transducer

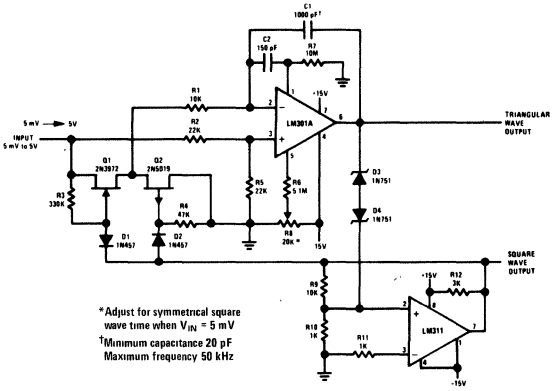


Zero Crossing Detector Driving MOS Switch



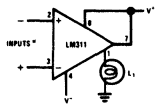
*TTL or DTL Fanout of two.

100 kHz Free Running Multivibrator



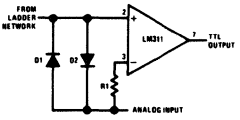
*Adjust for symmetrical square wave time when V_{IN} = 5 mV
†Minimum capacitance 20 pF
Maximum frequency 50 kHz

10 Hz to 10 kHz Voltage Controlled Oscillator

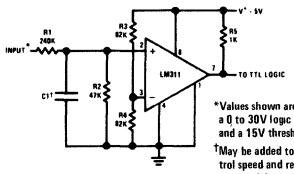


*Input polarity is reversed when using pin 1 as output

Driving Ground-Referred Load

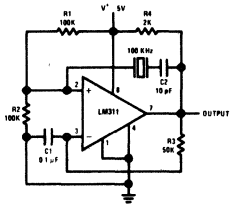


Using Clamp Diodes to Improve Response

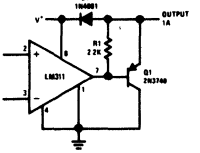


*Values shown are for a 0 to 30V logic swing and a 15V threshold.
†May be added to control speed and reduce susceptability to noise spikes

TTL Interface with High Level Logic

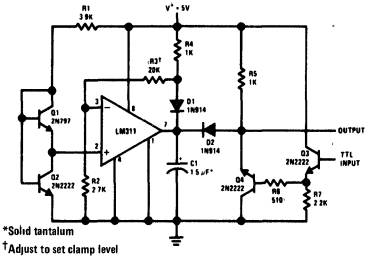


Crystal Oscillator



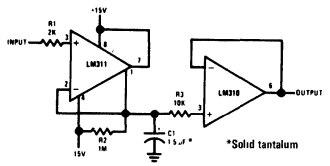
Comparator and Solenoid Driver

typical applications (con't)



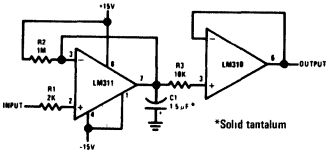
*Solid tantalum
†Adjust to set clamp level

Precision Squarer



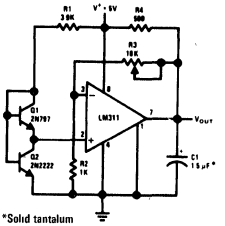
*Solid tantalum

Positive Peak Detector



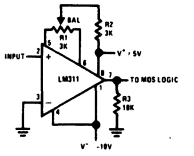
*Solid tantalum

Negative Peak Dectector

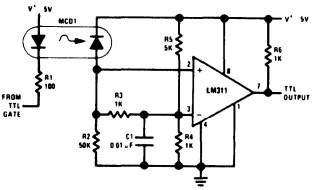


*Solid tantalum

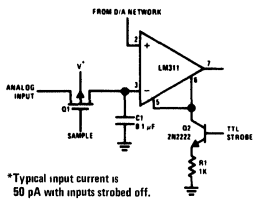
Low Voltage Adjustable Reference Supply



Zero Crossing Detector driving MOS logic

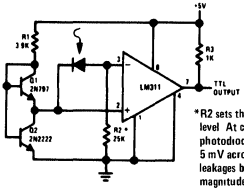


Digital Transmission Isolator



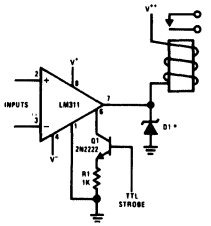
*Typical input current is 50 pA with inputs strobed off.

Strobing off Both Input* and Output Stages



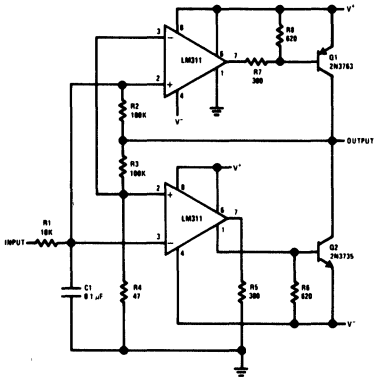
*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude

Precision Photodiode Comparator

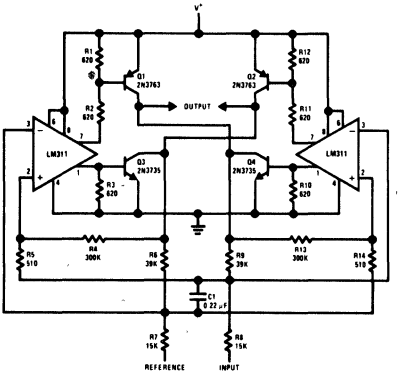


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line

Relay Driver with Strobe



Switching Power Amplifier



Switching Power Amplifier

Voltage Comparators

LM119/LM219 high speed dual comparator general description

The LM119/LM219 are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA. Outstanding features include:

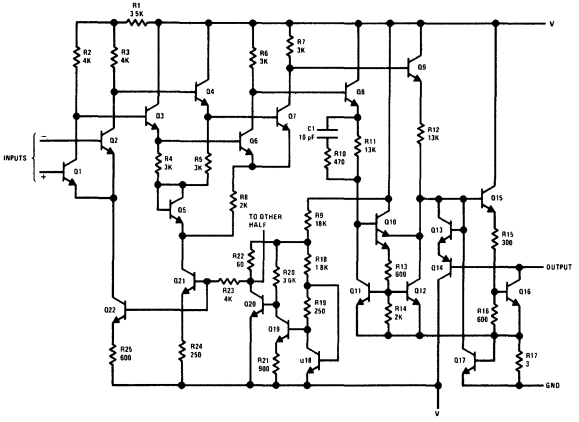
features

- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

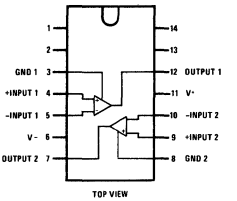
Although designed primarily for applications requiring operation from digital logic supplies, the LM119 is fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM219 is identical to the LM119, except that its performance is specified over a −25°C to 85°C temperature range instead of −55°C to 125°C.

schematic and connection diagrams

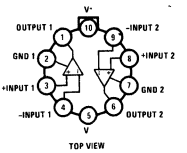


Dual-In-Line-Package



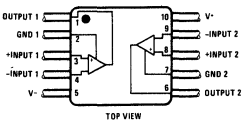
Order Number LM119D or LM219D
See Package 1

Metal Can Package



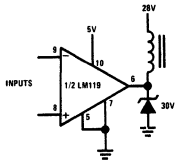
Order Number LM119H or LM219H
See Package 12

Flat Package

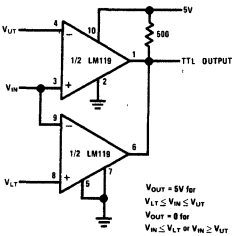


Order Number LM119F or LM219F
See Package 3

typical applications



Relay Driver



Window Detector

absolute maximum ratings

Total Supply Voltage	36V	Power Dissipation (Note 2)	500 mW
Output to Negative Supply Voltage	36V	Output Short Circuit Duration	10 sec
Ground to Negative Supply Voltage	25V	Operating Temperature Range LM119	−55°C to 125°C
Ground to Positive Supply Voltage	18V	LM219	−25°C to 85°C
Differential Input Voltage	±5V	Storage Temperature Range	−65°C to 150°C
Input Voltage (Note 1)	±15V	Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		0.7	4.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		30	75	nA
Input Bias Current	$T_A = 25°C$		150	500	nA
Voltage Gain	$T_A = 25°C$	10	40		V/mV
Response Time (Note 5)	$T_A = 25°C$ $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	2	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			7	mV
Input Offset Current (Note 4)				100	nA
Input Bias Current				1000	nA
Input Voltage Range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$	 1	±13	 3	V V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6$ mV, $I_{SINK} \leq 3.2$ mA $T_A \geq 0°C$ $T_A \leq 0°C$		 0.23	 0.4 0.6	 V V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		1	10	μA
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		8	11.5	mA
Negative Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		3	4.5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM119 is 150°C, while that of the LM219 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

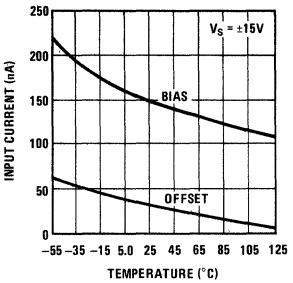
Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise stated. With the LM219, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

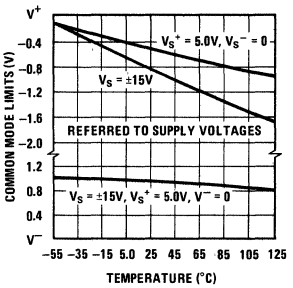
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

typical performance characteristics

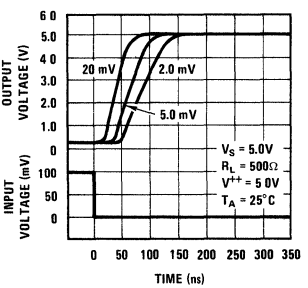
Input Currents



Common Mode Limits



Response Time for Various Input Overdrives



Voltage Comparators

LM319 high speed dual comparator

general description

The LM319 is a precision high speed dual comparator fabricated on a single monolithic chip. It is designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, it has higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM319 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

features

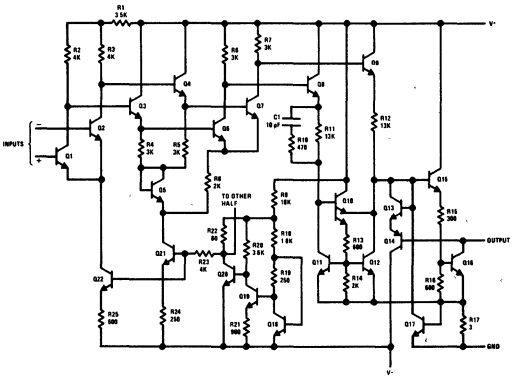
- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

Although designed primarily for applications requiring operation from digital logic supplies, the LM319 is fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM319 much more versatile than older devices like the LM711.

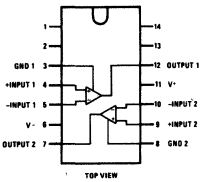
The LM319 has its performance specified over a 0°C to 70°C temperature range.

1

schematic and connection diagrams



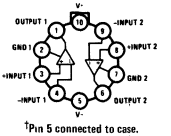
Dual In-Line-Package



Order Number LM319D
See package 1

LM319N
See Package 22

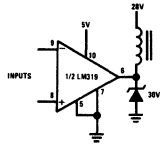
Metal Can Package†



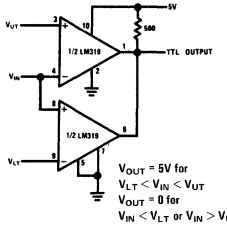
†Pin 5 connected to case.

Order Number LH319H
See Package 12

typical applications

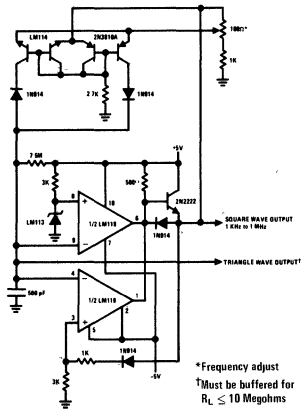


Relay Driver



V_{OUT} = 5V for
$V_{LT} < V_{IN} < V_{UT}$
V_{OUT} = 0 for
$V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

Window Detector



*Frequency adjust
†Must be buffered for $R_L \leq 10$ Megohms

Wide Range Variable Oscillator

absolute maximum ratings

Total Supply Voltage	36V	Power Dissipation (Note 2)	500 mW
Output to Negative Supply Voltage	36V	Output Short Circuit Duration	10 sec
Ground to Negative Supply Voltage	25V	Operating Temperature Range LM319	0°C to 70°C
Ground to Positive Supply Voltage	18V	Storage Temperature Range	−65°C to 150°C
Differential Input Voltage	±5V	Lead Temperature (Soldering, 10 sec)	300°C
Input Voltage (Note 1)	±15V		

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		2.0	8.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		80	200	nA
Input Bias Current	$T_A = 25°C$		250	1000	nA
Voltage Gain	$T_A = 25°C$	8	40		V/mV
Response Time (Note 5)	$T_A = 25°C$ $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	10	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			10	mV
Input Offset Current (Note 4)				300	nA
Input Bias Current				1200	nA
Input Voltage Range	$V_S = \pm 15V$		±13		V
	$V^+ = 5V$, $V^- = 0$	1		3	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$		0.3	0.4	V
	$V_{IN} \leq -10$ mV, $I_{SINK} \leq 3.2$ mA				
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		8	12.5	mA
Negative Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		3	5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage

Note 2: The maximum junction temperature of the LM319 is 85°C For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

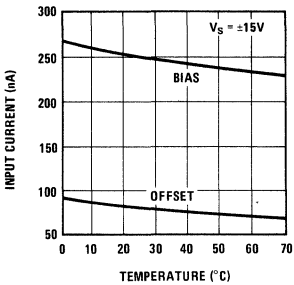
Note 3: These specifications apply for $V_S = \pm 15V$ and $-0°C \leq T_A \leq 70°C$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance

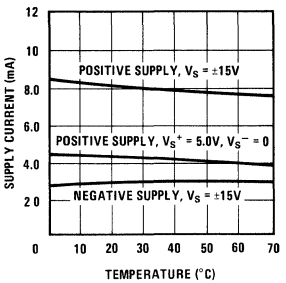
Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

typical performance characteristics

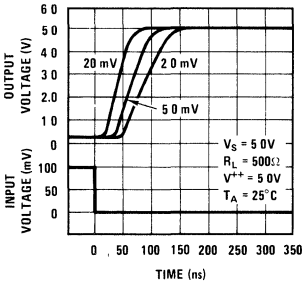
Input Currents



Supply Currents



Response Time for Various Input Overdrives



Voltage Comparators

LM139/LM239/LM339 quad comparators

general description

The LM139 series consists of four independent voltage comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM339 will directly interface with MOS logic — where the low power drain of the LM339 is a distinct advantage over standard comparators.

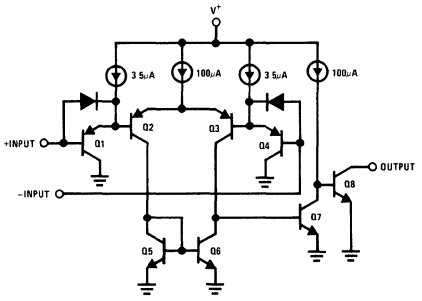
advantages

- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

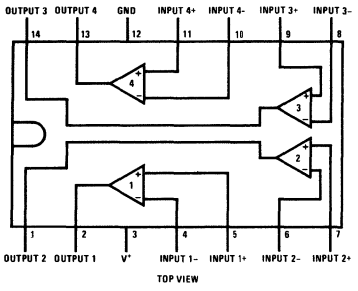
features

- Wide single supply
  Voltage range — $2\ V_{DC}$ to $36\ V_{DC}$
  or dual supplies — $\pm 1\ V_{DC}$ to $\pm 18\ V_{DC}$
- Very low supply current drain (0.8 mA) — independent of supply voltage (1 mW/comparator at $+5\ V_{DC}$)
- Low input biasing current — 35 nA
- Low input offset current — 3 nA
  and offset voltage — 3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output — 1 mV at 5μA
  saturation voltage — 70 mV at 1 mA
- Output voltage compatible with TTL (fanout of 2), DTL, ECL, MOS and CMOS logic systems

schematic and connection diagrams

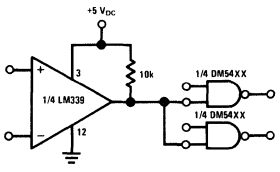


Dual-In-Line and Flat Package

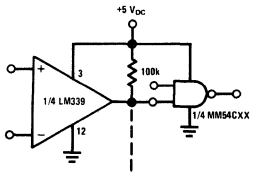


Order Number LM139F
See Package 4
Order Number LM139D, LM239D or LM339D
See Package 1
Order Number LM339N
See Package 22

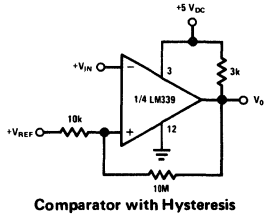
typical applications



Driving TTL



Driving CMOS



Comparator with Hysteresis

absolute maximum ratings

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Molded DIP (LM339N)	570 mW
Cavity DIP (LM139D, LM239D & LM339D)	900 mW
Flat Pack (LM139F)	800 mW
Output Short-Circuit to GND (Note 2)	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$)(Note 3)	50 mA
Operating Temperature Range	
LM339	0°C to +70°C
LM239	−25°C to +85°C
LM139	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics ($V^+ = +5.0\ V_{DC}$, see Note 4)

PARAMETER	CONDITIONS	LM139			LM239, LM339			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = +25°C$ (Note 9)		±2	±5.0		±2	±5.0	mV_{DC}
Input Bias Current (Note 5)	$I_{IN(+)}$ or $I_{IN(-)}$ With Output in Linear Range, $T_A = +25°C$		25	100		25	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = +25°C$		±3	±25		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 6)	$T_A = +25°C$	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	$R_L = \infty$ On All Comparators $T_A = +25°C$		0.8	2.0		0.8	2.0	mA_{DC}
Voltage Gain	$R_L \geq 15 k\Omega$, $T_A = +25°C$		200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = +1.4\ V_{DC}$, $V_{RL} = 5.0\ V_{DC}$ and $R_L = 5.1\ k\Omega$		300			300		ns
Response Time (Note 7)	$V_{RL} = 5.0\ V_{DC}$ and $R_L = 5.1\ k\Omega$, $T_A = +25°C$		1.3			1.3		µs
Output Sink Current	$V_{IN(-)} \geq +1.0\ V_{DC}$, $V_{IN(+)} = 0$ and $V_O \leq +1.5\ V_{DC}$, $T_A = +25°C$	6	16		6	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq +1.0\ V_{DC}$, $V_{IN(+)} = 0$ and $I_{SINK} \leq 4.0\ mA$, $T_A = +25°C$		250	500		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq +1.0\ V_{DC}$, $V_{IN(-)} = 0$ and $V_{OUT} = 5.0\ V_{DC}$, $T_A = +25°C$		0.1			0.1		nA_{DC}
Input Offset Voltage	(Note 9)			9.0			9.0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ With Output in Linear Range			300			400	nA_{DC}
Input Common-Mode Voltage Range		0		V^+−2.0	0		V^+−2.0	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq +1.0\ V_{DC}$, $V_{IN(+)} = 0$ and $I_{SINK} \leq 4.0\ mA$			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq +1.0\ V_{DC}$, $V_{IN(-)} = 0$ and $V_{OUT} = 30\ V_{DC}$			1.0			1.0	μA_{DC}
Differential Input Voltage (Note 8)	Keep All V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used)			36			36	V_{DC}

Note 1: For operating at high temperatures, the LM339 must be derated based on +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC}.

Note 4: These specifications apply for $V^+ = +5.0\ V_{DC}$ and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM239, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C and the LM339 temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ − 1.5V, but either or both inputs can go to +30 V_{DC} without damage.

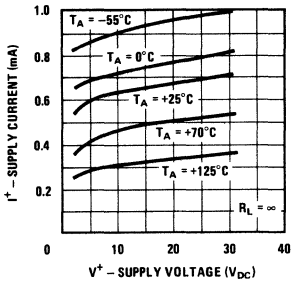
Note 7: The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: The positive excursions of the input can exceed the power supply voltage level, and if the other input voltage remains within the common-mode voltage range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply voltage, if used).

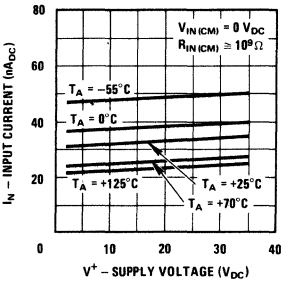
Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}, and over the full input common mode range (0 V_{DC} to V^+ ±1.5 V_{DC}).

typical performance characteristics

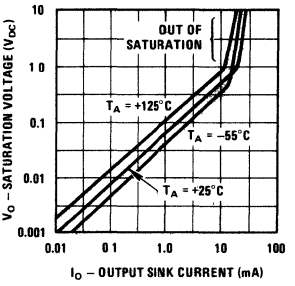
Supply Current



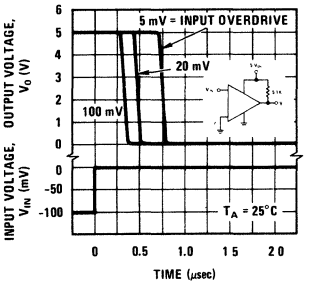
Input Current



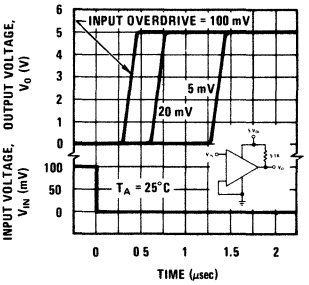
Output Saturation Voltage



Response Time for Various Input Overdrives – Negative Transition



Response Time for Various Input Overdrives – Positive Transition



application hints

The LM139 is a high gain, wide bandwidth device; which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $<10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

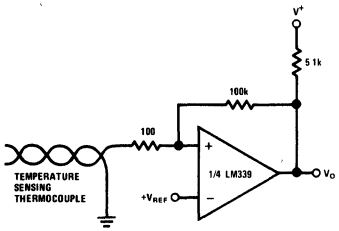
The bias network of the LM139 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $2V_{DC}$ to $30\ V_{DC}$.

It is usually unnecessary to use a bypass capacitor across the power supply line.

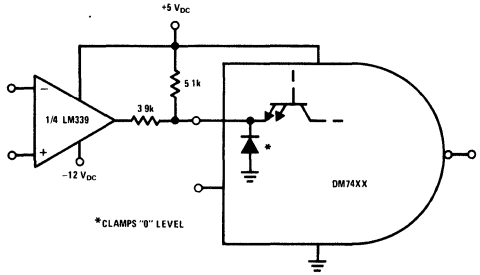
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode and input resistor can be used as shown in the applications section.

The output of the LM139 is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139 package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

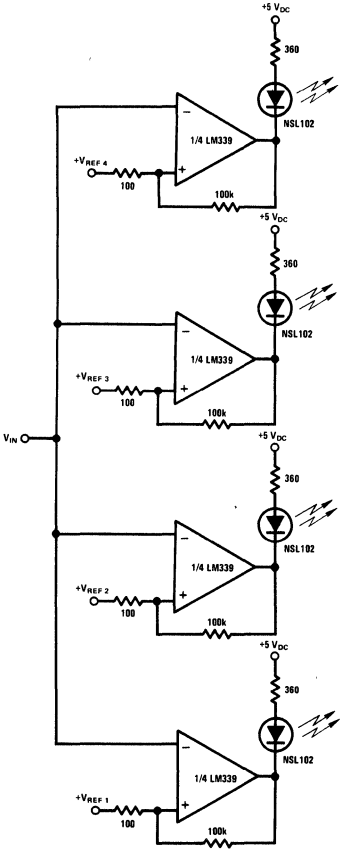
typical applications (con't)



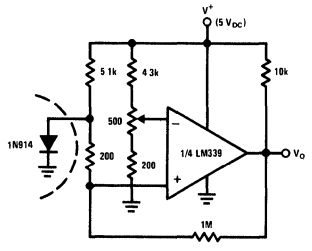
Ground Referenced Thermocouple in Single Supply System



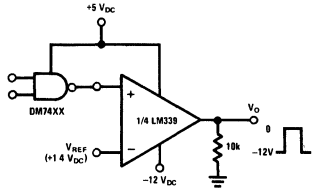
MOS to TTL Logic Translator



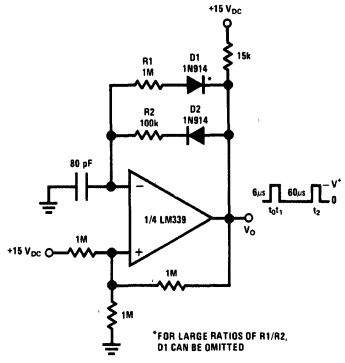
Visible Voltage Indicator



Remote Temperature Sensing

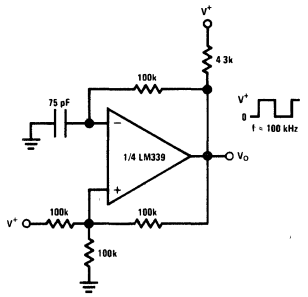


TTL to MOS Logic Converter

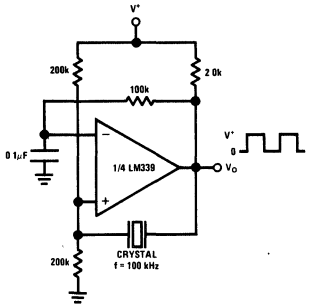


Pulse Generator

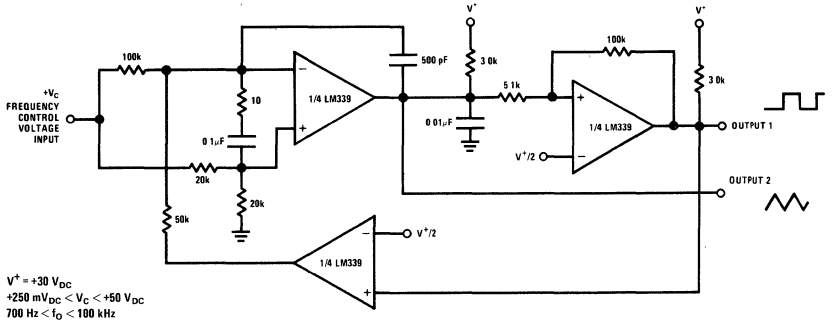
typical applications (con't)



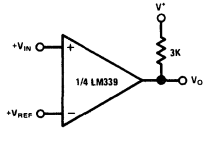
Squarewave Oscillator



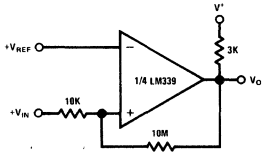
Crystal Controlled Oscillator



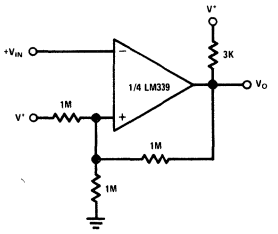
Two-Decade High-Frequency VCO



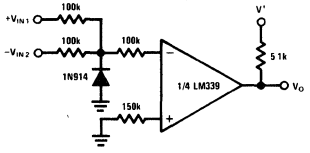
Basic Comparator



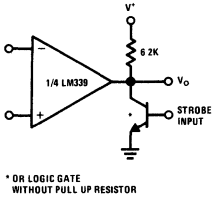
Non-Inverting Comparator with Hysteresis



Inverting Comparator with Hysteresis



Comparing Input Voltages
of Opposite Polarity



* OR LOGIC GATE
WITHOUT PULL UP RESISTOR

Output Strobing

Voltage Comparators

LM139A/LM239A/LM339A low offset voltage quad comparators

general description

The LM139A series consists of four independent precision voltage comparators with an offset voltage specification of 2 mV max. for all four comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139A series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM339A will directly interface with MOS logic—where the low power drain of the LM339A is a distinct advantage over standard comparators.

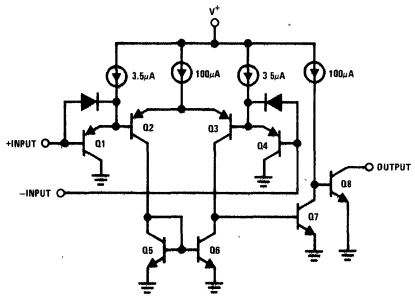
advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

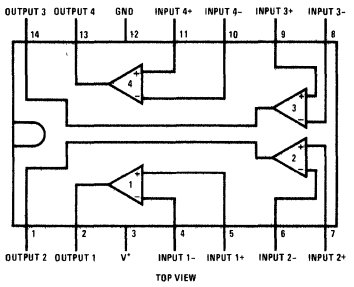
features

- Wide single supply
  Voltage range $2\,V_{DC}$ to $36\,V_{DC}$
  or dual supplies $\pm1\,V_{DC}$ to $\pm18\,V_{DC}$
- Very low supply current drain (0.8 mA)—independent of supply voltage (1 mW/comparator at $+5\,V_{DC}$)
- Low input biasing current 35 nA
- Low input offset current 3 nA
  and maximum offset voltage 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output 1 mV at 5μA
  saturation voltage 70 mV at 1 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

schematic and connection diagrams

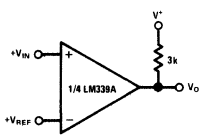


Dual-In-Line and Flat Package

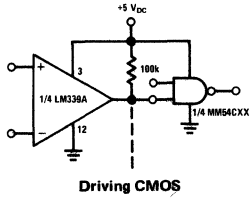


Order Number LM139AF
See Package 4
Order Number LM139AD, LM239AD or LM339AD
See Package 1
Order Number LM339AN
See Package 22

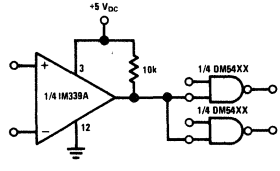
typical applications ($V^+ = 5.0\,V_{DC}$)



Basic Comparator



Driving CMOS



Driving TTL

absolute maximum ratings

Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	36 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}
Power Dissipation (Note 1)	
Molded DIP (LM339AN)	570 mW
Cavity DIP (LM139AD, LM239AD, and LM339AD)	900 mW
Flat Pack (LM139AF)	800 mW
Output Short-Circuit to GND (Note 2)	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA
Operating Temperature Range	
LM339A	0°C to +70°C
LM239A	−25°C to +85°C
LM139A	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics ($V^+ = +5.0\ V_{DC}$, see Note 4)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = +25°C$ (Note 9)		±1	±2 0		±1	±2.0	mV_{DC}
Input Bias Current (Note 5)	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $T_A = +25°C$		25	100		25	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = +25°C$		±3	±25		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 6)	$T_A = +25°C$	0		V^+−1 5	0		V^+−1.5	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators $T_A = +25°C$		0 8	2.0		0 8	2.0	mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, $T_A = +25°C$, $V^+ = 15\ V_{DC}$ (To Support Large V_O Swing)	50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = +1.4\ V_{DC}$, $V_{\overline{R}_L} = 5\ V_{DC}$, $R_L = 5\ 1\ k\Omega$ and $T_A = +25°C$		300			300		ns
Response Time (Note 7)	$V_{R_L} = 5\ V_{DC}$ and $R_L = 5\ 1\ k\Omega$, $T_A = +25°C$		1 3			1 3		µs
Output Sink Current	$V_{IN(-)} \geq +1\ V_{DC}$, $V_{IN(+)} = 0$, and $V_O \leq +1.5\ V_{DC}$, $T_A = +25°C$	6 0	16		6 0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq +1\ V_{DC}$, $V_{IN(+)} = 0$, and $I_{SINK} \leq 4\ mA$, $T_A = +25°C$		250	500		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq +1\ V_{DC}$, $V_{IN(-)} = 0$ and $V_O = 5\ V_{DC}$, $T_A = +25°C$		0 1			0 1		nA_{DC}
Input Offset Voltage	(Note 9)			4 0			4 0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400	nA_{DC}
Input Common-Mode Voltage Range		0		V^+−2 0	0		V^+−2.0	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq +1\ V_{DC}$, $V_{IN(+)} = 0$ and $I_{SINK} \leq 4\ mA$			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq +1\ V_{DC}$, $V_{IN(-)} = 0$ and $V_O = 30\ V_{DC}$			1 0			1 0	μA_{DC}
Differential Input Voltage (Note 8)	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used)			V^+			V^+	V_{DC}

Note 1: For operating at high temperatures, the LM339A must be derated based on a +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient The LM239A and LM139A must be derated based on a +150°C maximum junction temperature The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output transistors are allowed to saturate

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction The maximum output current is approximately 20 mA independent of the magnitude of V^+

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0 3 V_{DC}.

Note 4: These specifications apply for $V^+ = +5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated With the LM239A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$

Note 5. The direction of the input current is out of the IC due to the PNP input stage This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines

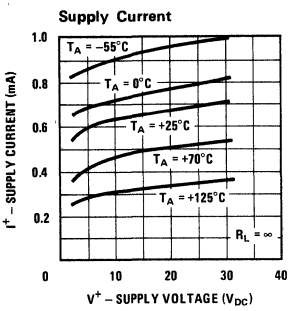
Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V The upper end of the common-mode voltage range is V^+ −1.5V, but either or both inputs can go to +30 V_{DC} without damage

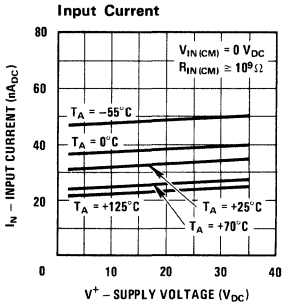
Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section

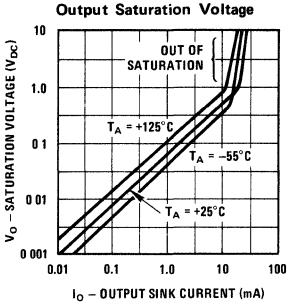
Note 8. If the voltage applied to any input exceeds V^+, all four comparator outputs will go to the high voltage level The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used)

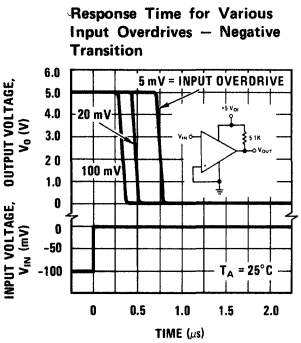
Note 9: At output switch point, $V_O \cong 1\ 4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}, and over the full input common mode range (0 V_{DC} to V^+ −1.5 V_{DC})

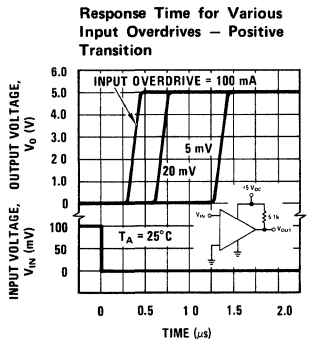
typical performance characteristics











application hints

The LM139A is a high gain, wide bandwidth device; which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10\ k\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139A establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than $-0.3\ V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139A is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Voltage Comparators

LM160/LM260/LM360 high speed differential comparator

general description

The LM160/LM260/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 500 mV.

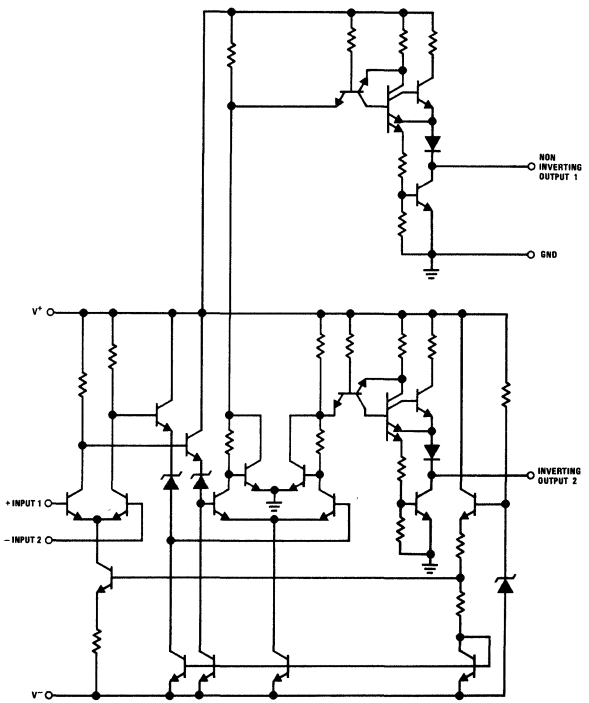
Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disc file systems.

features

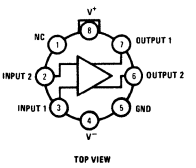
- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

1

schematic and connection diagrams

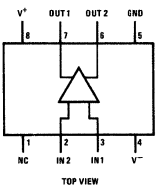


Metal Can Package



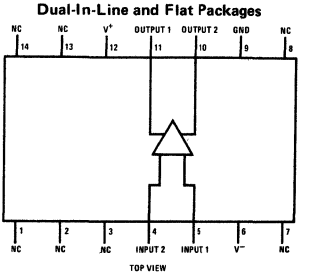
Order Number LM160H, LM260H, or LM360H
See Package 11

Dual-In-Line Package



Order Number LM360N
See Package 20

Dual-In-Line and Flat Packages



Order Number LM160D, LM260D or LM360D
See Package 1

Order Number LM160F
See Package 4

absolute maximum ratings

Positive Supply Voltage	+8V	Operating Temperature Range	
Negative Supply Voltage	−8V	LM160	−55°C to +125°C
Peak Output Current	20 mA	LM260	−25°C to +85°C
Differential Input Voltage	±5V	LM360	0°C to +70°C
Input Voltage	$V^+ \geq V_{IN} \geq V^-$	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Conditions					
Supply Voltage V_{CC}^+		4.5	5	6.5	V
Supply Voltage V_{CC}^-		−4.5	−5	−6.5	V
Input Offset Voltage	$R_S \leq 200\Omega$		2	5	mV
Input Offset Current			.5	3	μA
Input Bias Current			5	20	μA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	$T_A = 25°C$, $V_S = \pm5V$ (Note 1)		13	25	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Note 2)		12	20	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Note 3)		14		ns
Response Time Difference Between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$, (Note 1)		2		ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		μV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	$V_S = \pm6.5V$	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	$I_{OUT} = -320\mu A$, $V_S = \pm4.5V$	2.4	3		V
Output Low Voltage (Either Output)	$I_{SINK} = 6.4$ mA		.25	.4	V
Positive Supply Current	$V_S = \pm6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm6.5V$		−9	−16	mA

Note 1: Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
Note 2: Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.
Note 3: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Voltage Comparators

LM161/LM261/LM361 high speed differential comparators

general description

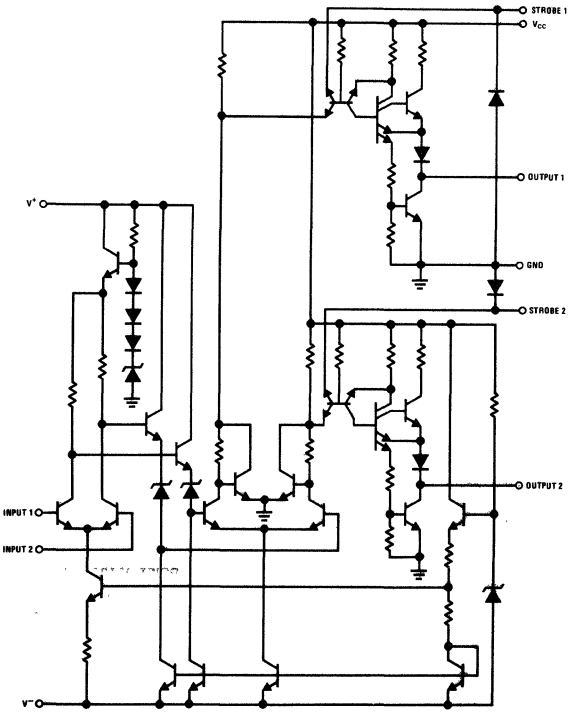
The LM161/LM261/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disc file systems.

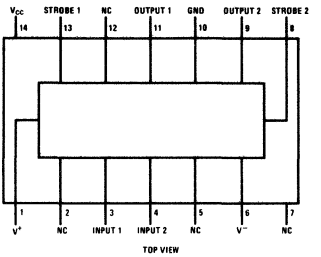
features

- Independent strobes
- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

schematic and connection diagrams

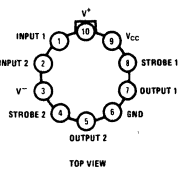


Dual-In-Line and Flat Package



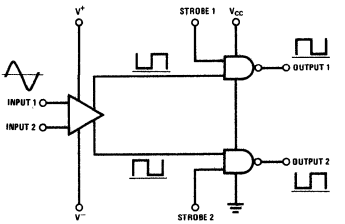
Order Number LM361N
See Package 22
Order Number LM161D, LM261D or LM361D
See Package 1
Order Number LM161F
See Package 4

Metal Can Package



Order Number LM161H or LM261H
See Package 12

logic diagram



absolute maximum ratings

Positive Supply Voltage, V^+	+16V
Negative Supply Voltage, V^-	−16V
Gate Supply Voltage, V_{CC}	+7V
Output Voltage	+7V
Differential Input Voltage	±5V
Input Common Mode Voltage	±6V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LM161	−55°C to +125°C
LM261	−25°C to +85°C
LM361	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	TYP	MAX
Supply Voltage V^+			
LM161/LM261	5V		15V
LM361	5V		15V
Supply Voltage V^-			
LM161/LM261	−6V		−15V
LM361	−6V		−15V
Supply Voltage V_{CC}			
LM161/LM261	4.5V	5V	5.5V
LM361	4.75V	5V	5.25V

electrical characteristics

($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless noted)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM161/LM261			LM361			
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			1	3		1	5	mV
Input Bias Current	$T_A = 25°C$		5	20		10	30	µA µA
Input Offset Current	$T_A = 25°C$		2	3		2	5	µA µA
Voltage Gain	$T_A = 25°C$		3			3		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		20			20		kΩ
Logical "1" Output Voltage	$V_{CC} = 4.75V$, $I_{SOURCE} = -5$ mA	2.4	3.3		2.4	3.3		V
Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{SINK} = 6.4$ mA			4			4	V
Strobe Input "1" Current	$V_{CC} = 5.25V$, $V_{STROBE} = 2.4V$			200			200	µA
Strobe Input "0" Current	$V_{CC} = 5.25V$, $V_{STROBE} = 4V$			−1.6			−1.6	mA
Strobe Input "0" Voltage	$V_{CC} = 4.75V$			8			8	V
Strobe Input "1" Voltage	$V_{CC} = 4.75V$	2			2			V
Output Short Circuit Current	$V_{CC} = 5.25V$, $V_{OUT} = 0V$	−18		−55	−18		−55	mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			4.5				mA
Supply Current I^+	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						5	mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			10				mA
Supply Current I^-	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						10	mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $-55°C \leq T_A \leq 125°C$			18				mA
Supply Current I_{CC}	$V^+ = 10V$, $V^- = -10V$, $V_{CC} = 5.25V$, $0°C \leq T_A \leq 70°C$						20	mA
TRANSIENT RESPONSE	$V_{IN} = 50$ mV Overdrive							
Propagation Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		14	20		14	20	ns
Propagation Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		14	20		14	20	ns
Delay Between Output A and B	$T_A = 25°C$		2	5		2	5	ns
Strobe Delay Time ($t_{pd(0)}$)	$T_A = 25°C$		8			8		ns
Strobe Delay Time ($t_{pd(1)}$)	$T_A = 25°C$		8			8		ns

Voltage Comparators

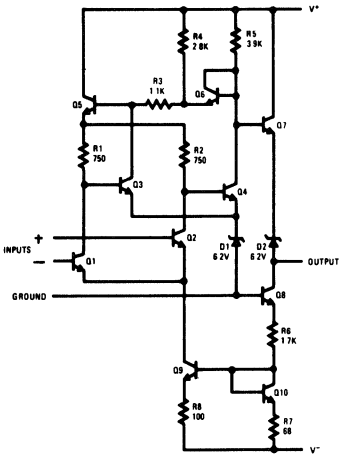
LM710 voltage comparator general description

The LM710 is a high-speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

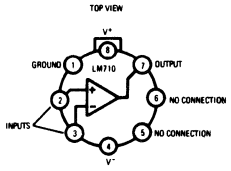
The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

The LM710 is useful as a pulse height discriminator, a voltage comparator in high-speed A/D converters or a go, no-go detector in automatic test equipment. It also has applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the unit suggests it for applications replacing relatively simple discrete component circuitry.

schematic* and connection diagrams



Metal Can

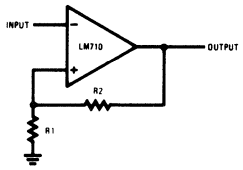


Note Pin 4 connected to case

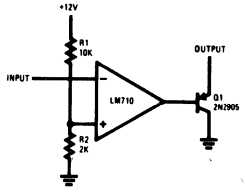
Order Number LM710H
See Package 11

typical applications*

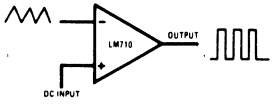
Schmidt Trigger



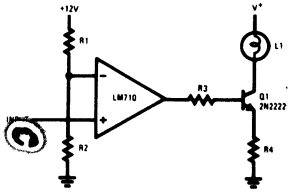
Line Receiver With Increased Output Sink Current



Pulse Width Modulator



Level Detector With Lamp Driver



*Pin connections shown are for metal can.

absolute maximum ratings

Positive Supply Voltage	14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	10 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Power Dissipation	
TO-99 (Note 1)	300 mW
Flat Package (Note 2)	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP.	MAX.	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 200\Omega$ $V_{CM} = 0V$		0.6	2.0	mV
Input Offset Current	$T_A = 25°C$, $V_{OUT} = 1.4V$		0.75	3.0	μA
Input Bias Current	$T_A = 25°C$		13	20	μA
Voltage Gain	$T_A = 25°C$	1250	1700		
Output Resistance	$T_A = 25°C$		200		Ω
Output Sink Current	$T_A = 25°C$, $V_{IN} \leq -5$ mV $V_{OUT} = 0$	2.0	2.5		mA
Response Time (Note 4)	$T_A = 25°C$		40		ns
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$-55°C \leq T_A \leq 125°C$ $R_S \leq 50\Omega$		3.0	10	μV/°C
Input Offset Current	$T_A = 125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$		5.0	25	nA/°C
	$-55°C \leq T_A \leq 25°C$		15	75	nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		dB
Differential Input Voltage Range		±5.0V			V
Voltage Gain		1000			
Positive Output Level	$V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq -5$ mA	2.5	3.2	4.0	V
Negative Output Level	$V_{IN} \leq -5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = 125°C$, $V_{IN} \leq -5$ mV $V_{OUT} = 0V$	0.5	1.7		mA
	$T_A = -55°C$, $V_{IN} \leq -5$ mV $V_{OUT} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{IN} \leq -5$ mV		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption	$V_{IN} \leq -5$ mV $I_{OUT} = 0$ mA		90	150	mW

Note 1: Rating applies for case temperatures to +125°C, derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

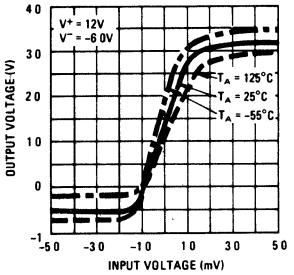
Note 2: Derate linearly at 4.4 mW/°C for ambient temperatures above +100°C.

Note 3: These specifications apply for $V^+ = 12V$, $V^- = -6.0V$, $-55°C \leq T_A \leq +125°C$ unless otherwise specified. The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C, and 1.0V at +125°C.

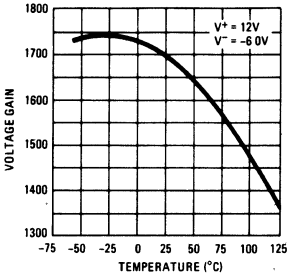
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

typical performance characteristics

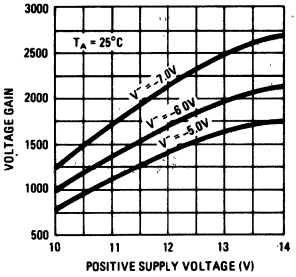
Transfer Function



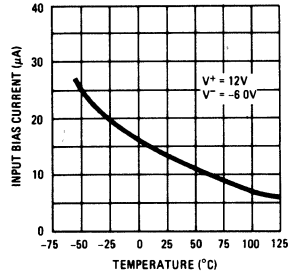
Voltage Gain



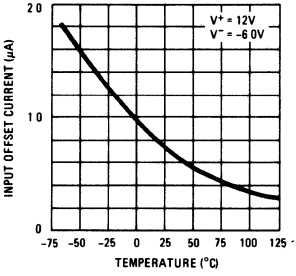
Voltage Gain



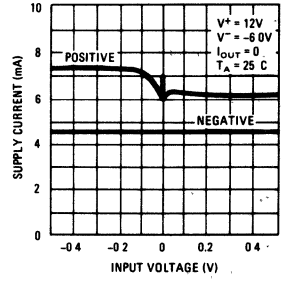
Input Bias Current



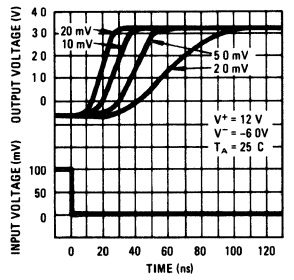
Input Offset Current



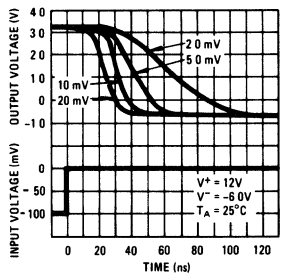
Supply Current



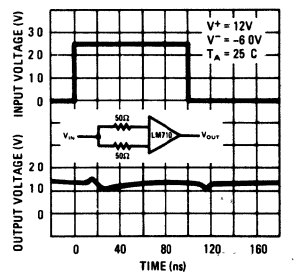
Response Time For Various Input Overdrives



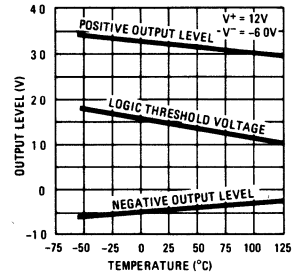
Response Time For Various Input Overdrives



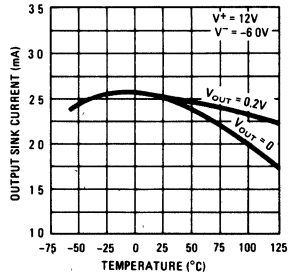
Common Mode Pulse Response



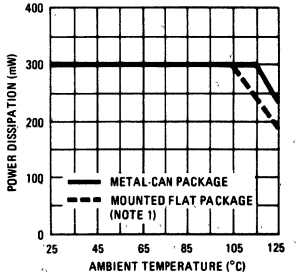
Output Voltage Level



Output Sink Current



Maximum Power Dissipation



Voltage Comparators

LM710C voltage comparator

general description

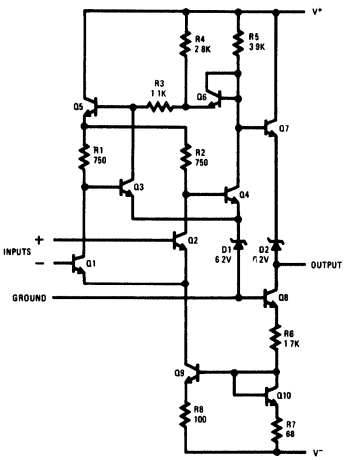
The LM710C is a high-speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

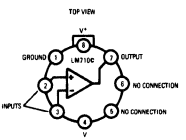
The LM710C is useful as a pulse height discriminator, a voltage comparator in high-speed A/D converters or a go, no-go detector in automatic test equipment. It also has applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the unit suggests it for applications replacing relatively simple discrete component circuitry.

The LM710C is the commercial/industrial version of the LM710. It is identical to the LM710 except that operation is specified over a 0°C to +70°C temperature range.

schematic* and connection diagrams



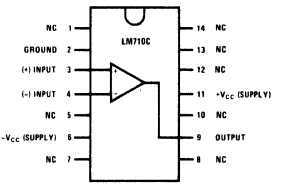
Metal Can Package



Note Pin 4 connected to case.

Order Number LM710CH
See Package 11

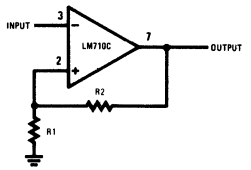
Dual-In-Line Package



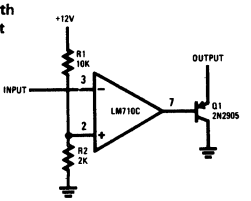
Order Number LM710CN
See Package 22

typical applications*

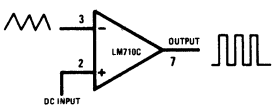
Schmidt Trigger



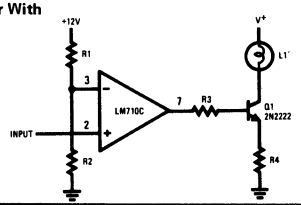
Line Receiver With Increased Output Sink Current



Pulse Width Modulator



Level Detector With Lamp Driver



*Pin connections shown are for metal can.

absolute maximum ratings

Positive Supply Voltage	14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	10 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Power Dissipation (Note 1)	
TO-99	300 mW
Flat Package	200 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S < 200\Omega$ $V_{CM} = 0V$		1 6	5 0	mV
Input Offset Current	$T_A = 25°C$, $V_{OUT} = 1.4V$		1 8	5 0	μA
Input Bias Current	$T_A = 25°C$		16	25	μA
Voltage Gain	$T_A = 25°C$	1000	1500		
Output Resistance	$T_A = 25°C$		200		Ω
Output Sink Current	$T_A = 25°C$, $\Delta V_{IN} \geq 10$ mV $V_{OUT} = 0$	1.6	2 5		mA
Response Time (Note 3)	$T_A = 25°C$		40		ns
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$			6 5	mV
Average Temperature Coefficient of Input Offset Voltage	$0°C \leq T_A \leq 70°C$ $R_S \leq 50\Omega$		5 0	20	μV/°C
Input Offset Current				7 5	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Positive Output Level	$V_{IN} \geq 10$ mV $0 \leq I_{OUT} \leq -5$ mA	2 5	3.2	4 0	V
Negative Output Level	$V_{IN} \leq -10$ mV	−1.0	−0.5	0	V
Output Sink Current	$V_{IN} \leq -10$ mV, $V_{OUT} = 0V$	0.5			mA
Positive Supply Current	$V_{IN} \leq -10$ mV		5.2	9 0	mA
Negative Supply Current			4.6	7 0	mA
Power Consumption				150	mW

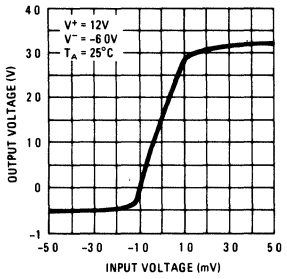
Note 1: Ratings apply for ambient temperatures to +70°C

Note 2: These specifications apply for $V^+ = 12V$, $V^- = 6.0V$, $0°C \leq T_A \leq +70°C$ unless otherwise specified. The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

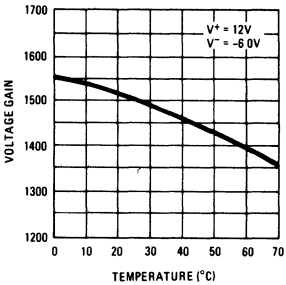
Note 3: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

typical performance characteristics

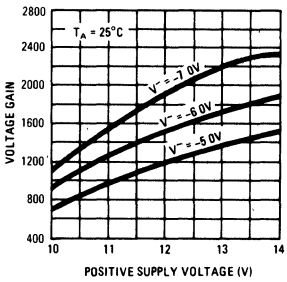
Transfer Function



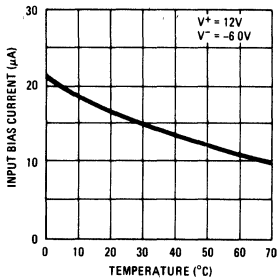
Voltage Gain



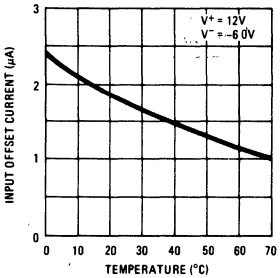
Voltage Gain



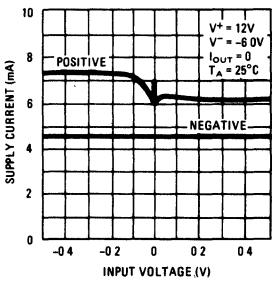
Input Bias Current



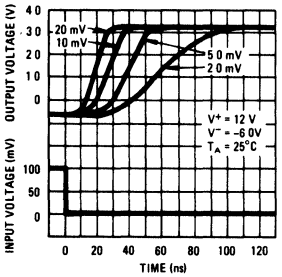
Input Offset Current



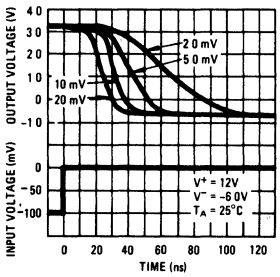
Supply Current



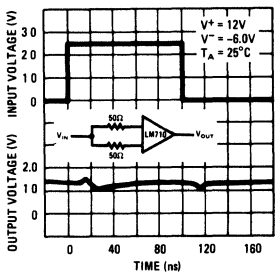
Response Time For Various Input Overdrives



Response Time For Various Input Overdrives



Common Mode Pulse Response



Voltage Comparators

LM711 dual comparator

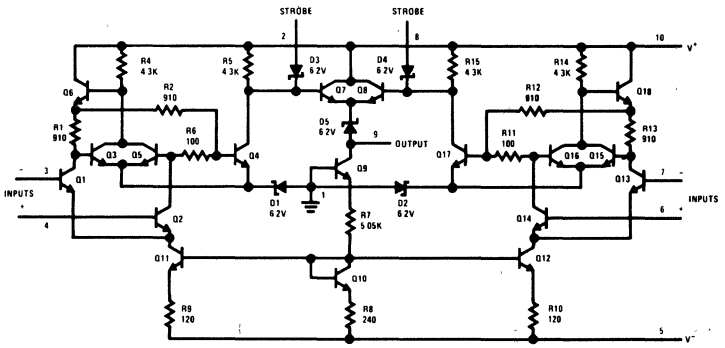
general description

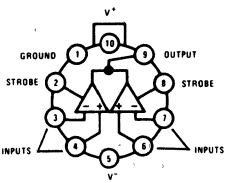
The LM711 contains two voltage comparators with separate differential inputs, a common output and provision for strobing each side independently. Similar to the LM710, the device features low offset and thermal drift, a large input voltage range, low power consumption, fast recovery from large overloads and compatibility with most integrated logic circuits.

With the addition of an external resistor network, the LM711 can be used as a sense amplifier for core memories. The input thresholding, combined with the high gain of the comparator, eliminates many of the inaccuracies encountered with conventional sense amplifier designs. Further, it has the speed and accuracy needed for reliably detecting the outputs of cores as small as 20 mils.

The LM711 is also useful in other applications where a dual comparator with OR'ed outputs is required, such as a double-ended limit detector. By using common circuitry for both halves, the device can provide high speed with lower power dissipation than two single comparators. The LM711 is available in either an 10-lead low profile TO-5 header or a 1/4" by 1/4" metal flat package.

schematic** and connection diagrams



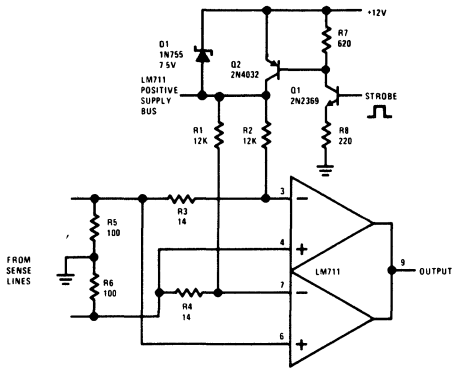


Note Pin 5 connected to case

Order Number LM711H
See Package 14

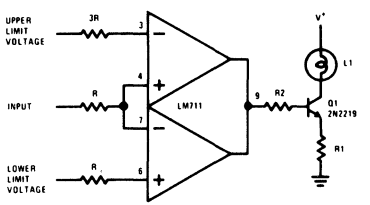
typical applications**

Sense Amplifier With Supply Strobing for Reduced Power Consumption*



*Standby dissipation is about 40 mW

Double-Ended Limit Detector With Lamp Driver



**Pin connections shown are for metal can

absolute maximum ratings

Positive Supply Voltage	+14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	25 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Strobe Voltage	0 to +6.0V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (These specifications apply for $T_A = 25°C$, $V^+ = 12V$, $V^- = -6V$)

PARAMETER	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0$		1.0	3.5	mV
	$R_S \leq 200\Omega$, $-5V \leq V_{CM} \leq +5V$		1.0	5.0	mV
Input Offset Current			0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 3)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{IN} \geq 10$ mV, $I_{OUT} = -5$ mA	2.5	3.5		V
Negative Output Level	$V_{IN} \leq -10$ mV	−1.0		0	V
Strobed Output Level	$V_{STROBE} \leq 0.3V$	−1.0		0	V
Output Sink Current	$V_{IN} \leq -10$ mV, $V_{OUT} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{STROBE} = 100$ mV		1.2	2.5	mA
Positive Supply Current	$V_{IN} \leq -10$ mV		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\Omega$			6.0	mV
Input Offset Current				20	μA
Input Bias Current				150	μA
Average Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

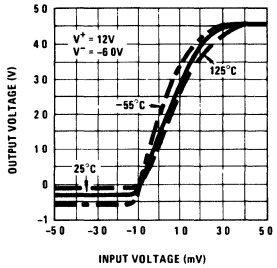
Note 1: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

Note 2: The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C, and 1.0V at +125°C.

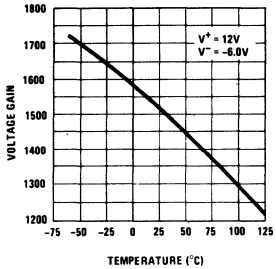
Note 3: The response time specified is for a 100 mV input step with 5 mV overdrive (see definitions).

typical performance characteristics

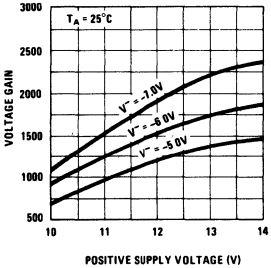
Transfer Function



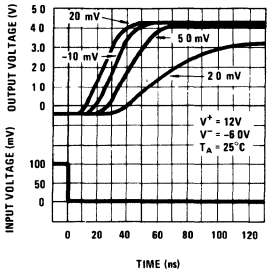
Voltage Gain



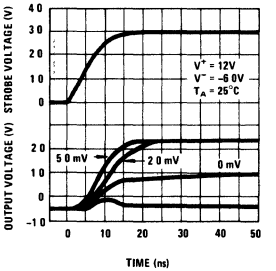
Voltage Gain



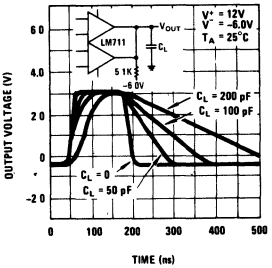
Response Time for Various Input Overdrives



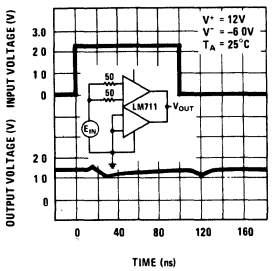
Strobe Release Time for Various Input Overdrives



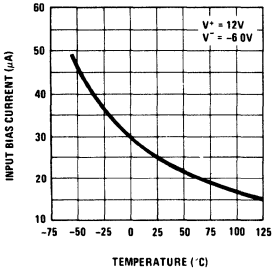
Output Pulse Stretching With Capacitive Loading



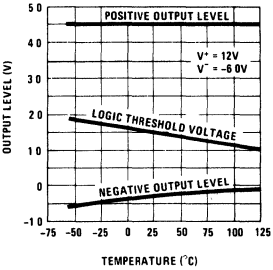
Common Mode Pulse Response



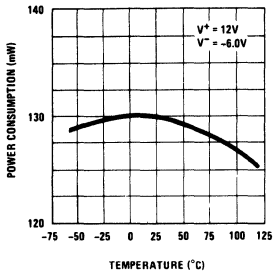
Input Bias Current



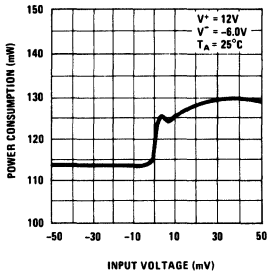
Output Voltage Level



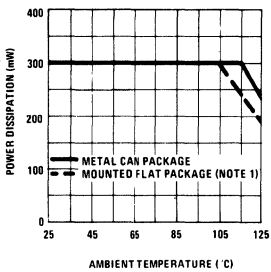
Power Consumption



Power Consumption



Maximum Power Dissipation



Voltage Comparators

LM711C dual comparator

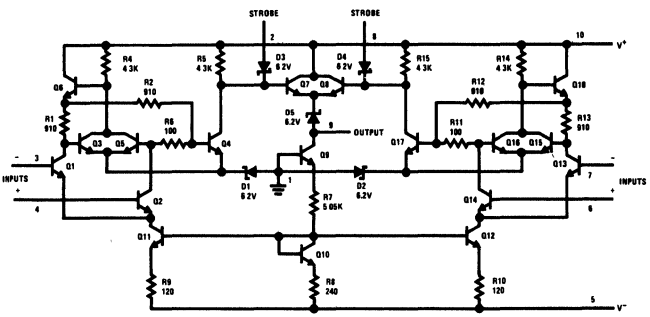
general description

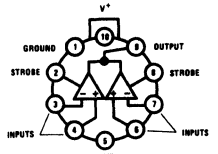
The LM711C contains two voltage comparators with separate differential inputs, a common output and provision for strobing each side independently. Similar to the LM710C, the device features low offset and thermal drift, a large input voltage range, low power consumption, fast recovery from large overloads and compatibility with most integrated logic circuits.

With the addition of an external resistor network, the LM711C can be used as a sense amplifier for core memories. The input thresholding, combined with the high gain of the comparator, eliminates many of the inaccuracies encountered with conventional sense amplifier designs. Further, it has the speed and accuracy needed for reliably detecting the outputs of cores as small as 20 mils.

The LM711C is also useful in other applications where a dual comparator with OR'ed outputs is required, such as a double-ended limit detector. By using common circuitry for both halves, the device can provide high speed with lower power dissipation than two single comparators. The LM711C is the commercial/industrial version of the LM711. It is identical to the LM711, except that operation is specified over a 0°C to 70°C temperature range.

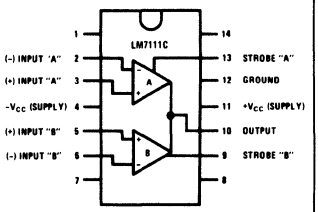
schematic** and connection diagrams





Note Pin 5 connected to case

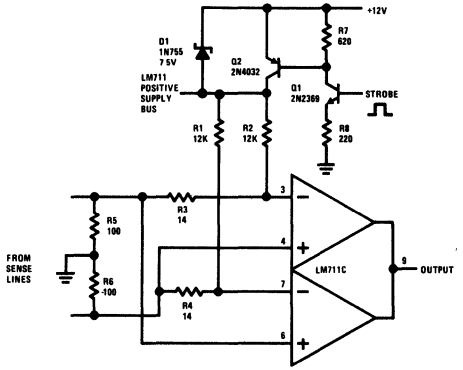
Order Number LM711CH
See Package 14



Order Number LM711CN
See Package 22

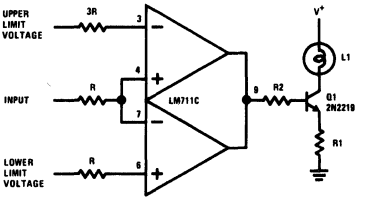
typical applications**

Sense Amplifier With Supply Strobing for Reduced Power Consumption*



*Standby dissipation is about 40 mW

Double-Ended Limit Detector With Lamp Driver



**Pin connections shown are for metal can.

absolute maximum ratings

Positive Supply Voltage	+14.0V
Negative Supply Voltage	-7.0V
Peak Output Current	25 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Strobe Voltage	0 to +6.0V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

(The following specfications apply for $T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0$		1.0	5.0	mV
	$R_S \leq 200\Omega$, $-5V \leq V_{CM} \leq +5V$		1.0	7.5	mV
Input Offset Current			0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 3)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{IN} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{IN} \geq 10$ mV, $I_{OUT} = -5$ mA	2.5	3.5		V
Negative Output Level	$V_{IN} \leq -10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{STROBE} \leq 0.3V$	-1.0		0	V
Output Sink Current	$V_{IN} \leq -10$ mV, $V_{OUT} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{STROBE} = 100$ mV		1.2	2.5	mA
Positive Supply Current	$V_{IN} \leq -10$ mV		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	230	mW
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0$			6.0	mV
	$R_S \leq 200\Omega$, $-5V \leq V_{CM} \leq +5V$			10	mV
Input Offset Current				25	μA
Input Bias Current				150	μA
Average Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

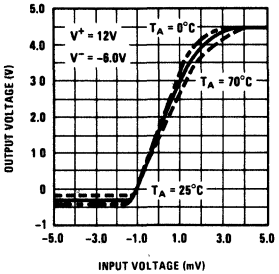
Note 1: Ratings apply for ambient temperatures to 70°C.

Note 2: The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at 25°C, and 1.2V at +70°C.

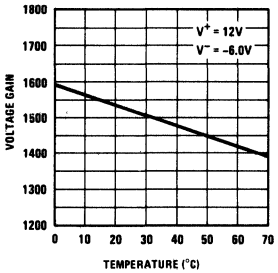
Note 3: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

typical performance characteristics

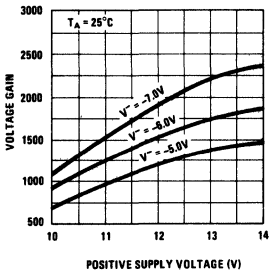
Transfer Function



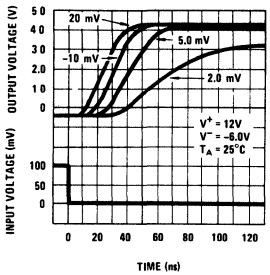
Voltage Gain



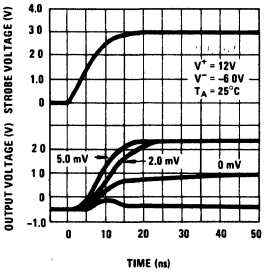
Voltage Gain



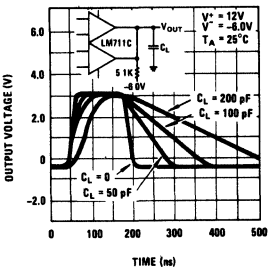
Response Time for Various Input Overdrives



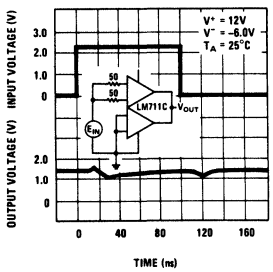
Strobe Release Time for Various Input Overdrives



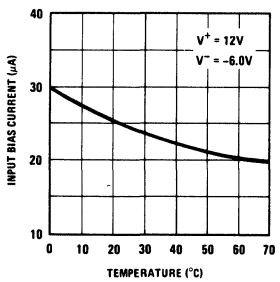
Output Pulse Stretching With Capacitive Loading



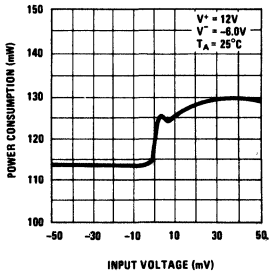
Common Mode Pulse Response



Input Bias Current



Power Consumption



Voltage Comparators

LM1514/LM1414 dual differential voltage comparator

general description

The LM1514/LM1414 is a dual differential voltage comparator intended for applications requiring high accuracy and fast response times. The device is constructed on a single monolithic silicon chip.

The LM1514/LM1414 is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms. The LM1514/LM1414 meet or exceed the specifications for the MC1514/MC1414 and are pin-for-pin replacements. The LM1514 is available in the ceramic dual-in-line package. The LM1414 is available in either the ceramic or molded dual-in-line package.

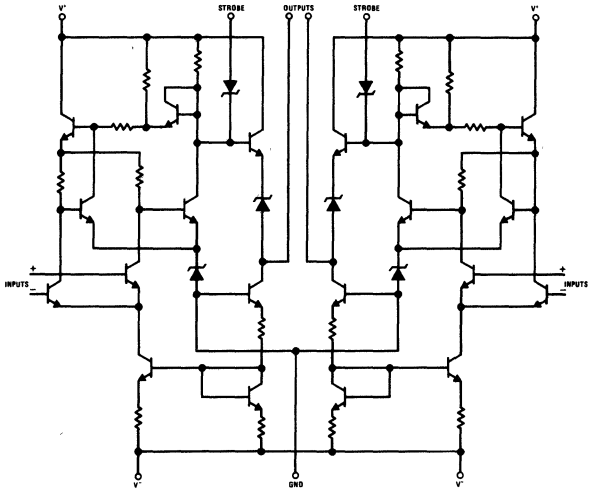
The LM1514 is specified for operation over the −55°C to +125°C military temperature range. The LM1414 is specified for operation over the 0°C to +70°C temperature range.

features

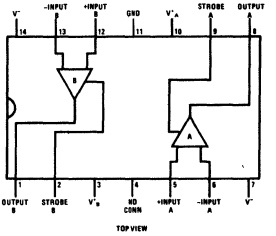
- Two totally separate comparators per package
- Independent strobe capability
- High speed 30 ns typ
- Low input offset voltage and current
- High output sink current over temperature
- Output compatible with TTL/DTL logic
- Molded or ceramic dual-in-line package

1

schematic and connection diagram



Dual-In-Line Package



Order Number LM1414J or LM1514J
See Package 16

Order Number LM1414N
See Package 22

absolute maximum ratings (Note 1)

Positive supply voltage	+14 0V	Power dissipation (Note 2)		600 mW
Negative supply voltage	−7 0V	Operating temperature Range	LM1514	−55°C to +125°C
Peak output current	10 mA		LM1414	0°C to +70°C
Differential input voltage	±5.0V	Storage temperature range		−65°C to +150°C
Input voltage	±7.0V	Lead temperature (soldering, 10 sec)		300°C

electrical characteristics for $T_A = 25°C$, $V^+ = +12V$, $V^- = -6V$, unless otherwise specified

PARAMETER	CONDITIONS	LM1514			LM1414			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$, $V_{OUT} = 1.4V$		0.6	2 0		1.0	5.0	mV
Input Offset Current	$V_{CM} = 0V$, $V_{OUT} = 1\ 4V$		0 8	3 0		1 2	5 0	μA
Input Bias Current				20			25	μA
Voltage Gain		1250			1000			
Output Resistance			200			200		Ω
Differential Input Voltage Range		±5 0			±5.0			V
Input Voltage Range	$V^- = -7.0V$	±5 0			±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$, $V^- = -7\ 0V$	80	100		70	100		dB
Positive Output Voltage	$V_{IN} \geq 7.0$ mV, $0 \leq I_{OUT} \leq -5\ 0$ mA	2.5	3.2	4.0	2 5	3.2	4 0	V
Negative Output Voltage	$V_{IN} \leq -7\ 0$ mV	−1.0	−0.5	0	−1.0	−0.5	0	V
Strobed Output Voltage	$V_{STROBE} \leq 0.3V$	−1.0	−0.5	0	−1 0	−0.5	0	V
Strobe "0" Current	$V_{STROBE} = 100$ mV		−1 2	−2.5		−1.2	−2.5	mA
Positive Supply Current	$V_{IN} \leq -7$ mV			18			18	mA
Negative Supply Current	$V_{IN} \leq -7$ mV			−14			−14	mA
Power Consumption			180	300		180	300	mW
Response Time	(Note 3)		30			30		ns
LM1514/LM1414: The following apply for $T_L \leq T_A \leq T_H$ (Note 4) unless otherwise specified								
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{OUT} = 1.8V$ for $T_A = T_L$			3.0			6.5	mV
	$V_{CM} = 0V$, $V_{OUT} = 1.0V$ for $T_A = T_H$			3 0			6.5	mV
Input Bias Current				45			40	μA
Temperature Coefficient of Input Offset Voltage			3.0			5 0		μV/°C
Input Offset Current	$V_{CM} = 0V$, $V_{OUT} = 1.8V$, $T_A = T_L$			7.0			7 5	μA
	$V_{CM} = 0V$, $V_{OUT} = 1\ 0V$, $T_A = T_H$			3.0			7.5	μA
Voltage Gain		1000			800			
Output Sink Current	$V_{IN} \leq -9\ 0$ mV, $V_{OUT} \geq 0V$	2.8	4.0		1.6	2 5		mA

Note 1: Voltage values are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

Note 2: LM1514 ceramic package: The maximum junction temperature is +150°C, for operating at elevated temperatures, devices must be derated linearly at 12 5 mW/°C LM1414 ceramic package: The maximum junction temperature is +95°C for operating at elevated temperatures, devices must be derated linearly at 12.5 mW/°C. LM1414 molded package: The maximum junction temperature is +115°C, for operating at elevated temperatures, devices must be derated linearly at 6.7 mW/°C.

Note 3: The response time specified (see Definitions) for a 100 mV input step with 5 mV overdrive.

Note 4: For LM1514, $T_L = -55°C$, $T_H = +125°C$. For LM1414, $T_L = 0°C$, $T_H = +70°C$.

Level Translators/Buffers

DH0034/DH0034C high speed dual level translator

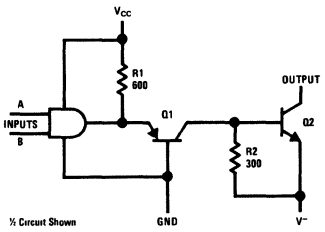
general description

The DH0034/DH0034C is a high speed level translator suitable for interfacing to MOS or junction FET analog switches. It may also be used as a universal logic level shifter capable of accepting TTL/DTL input levels and shifting to CML, MOS, or SLT levels.

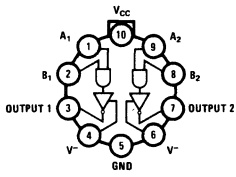
features

- Fast switching, t_{pd0}: typically 15 ns; t_{pd1}: typically 35 ns
- Large output voltage range: 25V
- Input is TTL/DTL compatible
- Low output leakage: typically 0.1 μA
- High output currents: up to ±100 mA

schematic and connection diagrams

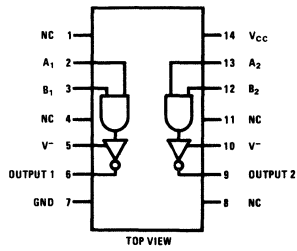


Metal Can Package



Order Number DH0034H
or DH0034CH
See Package 12

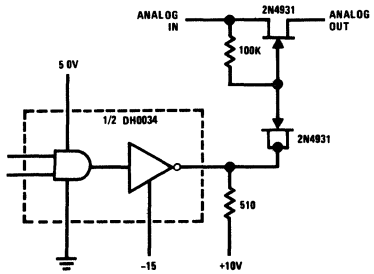
Dual-in-Line Package



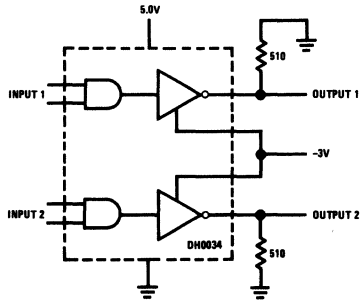
Order Number DH0034D
or DH0034CD
See Package 1

typical applications

5 MHz Analog Switch



TTL to IBM (SLT) Logic Levels



absolute maximum ratings

V_{CC} Supply Voltage		7.0V
Negative Supply Voltage		−30V
Positive Supply Voltage		+25V
Differential Supply Voltage		25V
Maximum Output Current		100 mA
Input Voltage		+5.5V
Operating Temperature Range:	DH0034	−55°C to +125°C
	DH0034C	0°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (See Notes 1 & 2)

PARAMETER	CONDITIONS	DH0034			DH0034C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Logical "1" Input Voltage	V_{CC} = 4.5V V_{CC} = 4.75V	2.0			2.0			V
Logical "0" Input Voltage	V_{CC} = 5.5V V_{CC} = 4.75V			0.8			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 2.4V V_{CC} = 5.25V, V_{IN} = 2.4V			40			40	μA
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V V_{CC} = 5.25V, V_{IN} = 5.5V			1.0			1.0	mA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V V_{CC} = 5.25V, V_{IN} = 0.4V			1.6			1.6	mA
Power Supply Current Logic "0"	(Note 3) V_{CC} = 5.5V, V_{IN} = 4.5V V_{CC} = 5.25V, V_{IN} = 4.5V		30	38		30	38	mA
Power Supply Current Logic "1"	(Note 3) V_{CC} = 5.5V, V_{IN} = 0V V_{CC} = 5.25V, V_{IN} = 0V		37	48		37	48	mA
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 100 mA V_{CC} = 4.5V, I_{OUT} = 50 mA		V^- + .50 V^- + .3	V^- + .75 V^- + .50		V^- + .50 V^- + .3	V^- + .80 V^- + .65	V V
Output Leakage Current	V_{CC} = 5.5V, V_{IN} = 0.8V $V^+ - V^-$ = 25V		0.1	5		0.1	5	μA
Transition Time to Logical "0"	V_{CC} = 5.0V, V_3 = 0V, T_A = 25°C V^- = −25V, R_L = 510Ω		15	25		15	35	ns
Transition Time to Logical "1"	V_{CC} = 5.0V, T_A = 25°C V^- = −25V, R_L = 510Ω		35	60		35	65	ns

Note 1: These specifications apply over the temperature range −55°C to +125°C for the DH0034 and 0°C to +85°C for the DH0034C with a 510 ohm resistor connected between output and ground, and V^- connected to −25V, unless otherwise specified.

Note 2: All typical values are for T_A = 25°C.

Note 3: Current measured is total drawn from V_{CC} supply.

theory of operation

When both inputs of the DH0034 are raised to logic "1", the input AND gate is turned "on" allowing Q1's emitter to become forward biased. Q1 provides a level shift and constant output current. The collector current is essentially the same as the emitter which is given by $\frac{V_{CC} - V_{BE}}{R1}$ Approximately 7.0 mA flows out of Q1's collector.

About 2 mA of Q1's collector current is drawn off by pull down resistor, R2. The balance, 5 mA, is available as base drive to Q2 and to charge its associated Miller capacitance. The output is pulled to within a V_{SAT} of V^-. When either (or both) input to the DH0034 is lowered to logic "0," the AND gate output drops to 0.2V turning Q1 off. Deprived of base drive Q2 rapidly turns off causing the output to rise to the V_3 supply voltage. Since Q2's emitter operates between 0.6V and 0.2V, the speed of the DH0034 is greatly enhanced.

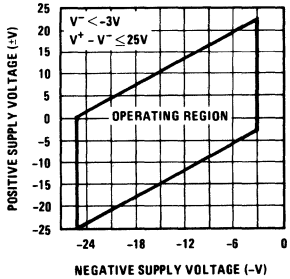
applications information

1. Paralleling the Outputs

The outputs of the DH0034 may be paralleled to increase output drive capability or to accomplish the "wire OR". In order to prevent current hogging by one output transistor or the other, resistors of 2 ohms/100 mA value should be inserted between the emitters of the output transistors and the minus supply.

2. Recommended Output Voltage Swing

The graph shows boundary conditions which govern proper operation of the DH0034. The range of operation for the negative supply is shown on the X axis and must be between −3V and −25V. The allowable range for the positive supply is governed by the value chosen for V^-. V^+ may be selected by drawing a vertical line through the selected value for V^- and terminated by the boundaries of the operating region. For example, a value of V^- equal to −6V would dictate values of



V^+ between −5V and +19V. In general, it is desirable to maintain at least 5V difference between the supplies.

Level Translators/Buffers

DM5406/DM7406,DM5416/DM7416
hex inverter buffers/drivers

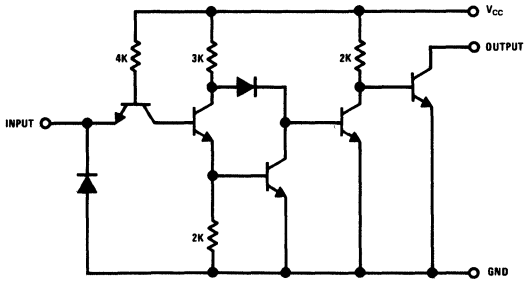
general description

These TTL hex inverter buffers/drivers are fully compatible for use with TTL and DTL logic circuits. Each inverter features high-voltage, open-collector outputs (DM5406/DM7406 30 volts minimum breakdown and DM5416/DM7416 15 volts minimum breakdown). These inverters also feature high sink current capability. (DM5406, DM5416 30 mA and DM7406, DM7416 40 mA).

features

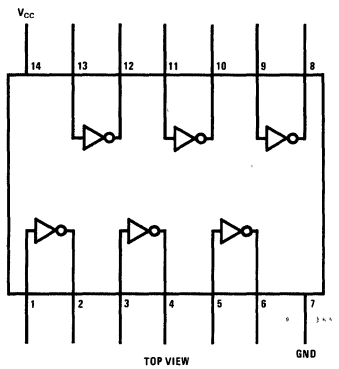
- Input clamp diodes
- High voltage open-collector outputs
  - DM5406/DM7406 30V
  - DM5416/DM7416 15V
- High sink current capability
  - DM5406, DM5416 30 mA
  - DM7406, DM7416 40 mA
- 15 ns typical propagation delay time

schematic and connection diagrams



Note Component values shown are nominal

Dual-In-Line and Flat Package



TOP VIEW

Order Number DM5406J, DM7406J, DM5416J or DM7416J
See Package 16

Order Number DM5406N, DM7406N, DM5416N or DM7416N
See Package 22

Order Number DM5406W or DM5616W
See Package 27

absolute maximum ratings (Note 1)

Supply Voltage		7.0V
Input Voltage		5.5V
Output Voltage	DM5406/DM7406	30V
	DM5416/DM7416	15V
Storage Temperature Range		−65°C to +150°C
Lead Temperature, (Soldering, 10 Sec)		300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
DM5406,DM5416	4.5	5.5	V
DM7406,DM7416	4.75	5.25	V
Temperature (T_A)			
DM5406,DM5416	−55	+125	°C
DM7406,DM7416	0	70	°C
Output Sink Current			
DM5406,DM5416		30	mA
DM7406,DM7416		40	mA

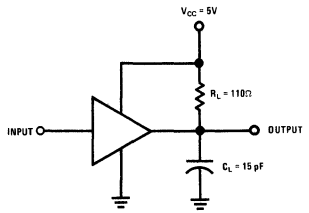
electrical characteristics (Note 2)

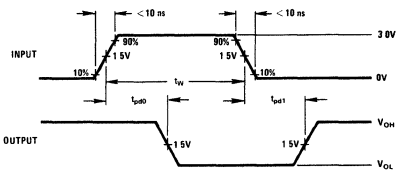
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2			V
Logical "0" Input Voltage				0.8	V
Output Breakdown Voltage					
DM5406/DM7406	V_{CC} = Max, I_{OFF} = 250 μA, V_{IN} = 0.8V	30			V
DM5416/DM7416	V_{CC} = Max, I_{OFF} = 250 μA, V_{IN} = 0.8V	15			V
Logical "1" Output Current					
DM5406/DM7406	V_{CC} = Max, V_{OH} = 30V, V_{IN} = 0.8V			250	μA
DM5416/DM7416	V_{CC} = Max, V_{OH} = 15V, V_{IN} = 0.8V			250	μA
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2V, I_{OUT} = Max			0.7	V
	V_{CC} = Min, V_{IN} = 2V, I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Supply Current — Logical "1"	V_{CC} = Max, V_{IN} = 0V		30	42	mA
Logical "0"	V_{CC} = Max, V_{IN} = 5V		27	38	mA
Input Clamp Voltage	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C			−1.5	V
Propagation Delay to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 110Ω		15	23	ns
Propagation Delay to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 110Ω		10	15	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the operation of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5406, DM5416 and across the 0°C to 70°C range for the DM7406,DM7416. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

ac test circuit and switching time waveforms





Level Translators/Buffers

DM5407/DM7407,DM5417/DM7417
hex buffers/drivers

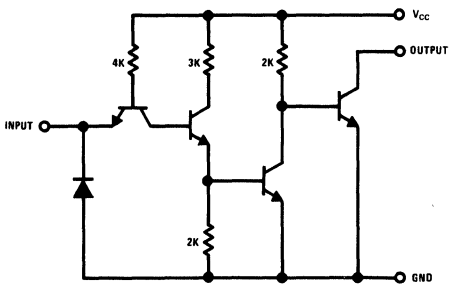
general description

These TTL hex buffers/drivers are fully compatible for use with TTL and DTL logic circuits. Each buffer features high-voltage, open-collector outputs (DM5407/DM7407 30V minimum breakdown and DM5417/DM7417 15V minimum breakdown). These buffers also feature high sink current capability (DM5407, DM5417 30 mA and DM7407, DM7417 40 mA).

features

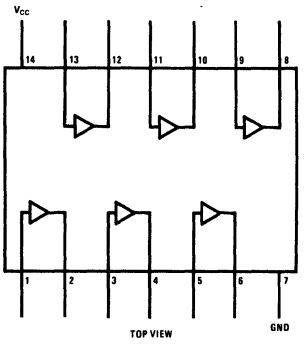
- Input clamp diodes
- High voltage open-collector outputs
  - DM5407/DM7407 30V
  - DM5417/DM7417 15V
- High sink current capability
  - DM5407,DM5417 30 mA
  - DM7407,DM7417 40 mA
- 14 ns typical propagation delay time
- 145 mW typical power dissipation

schematic and connection diagrams



Note Component values shown are nominal

Dual-In-Line and Flat Package



TOP VIEW

Order Number DM5407J, DM7407J, DM5417J or DM7417J
See Package 16

Order Number DM5407N, DM7407N, DM5417N or DM7417N
See Package 22

Order Number DM5407W or DM5417W
See Package 27

absolute maximum ratings (Note 1)

Supply Voltage		7.0V
Input Voltage		5.5V
Output Voltage	DM5407/DM7407	30V
	DM5417/DM7417	15V
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5407,DM5417	4.5	5 5	V
DM7407,DM7417	4.75	5.25	V
Temperature (T_A)			
DM5407,DM5417	−55	+125	°C
DM7407,DM7417	0	70	°C
Output Sink Current			
DM5407,DM5417		30	mA
DM7407,DM7417		40	mA

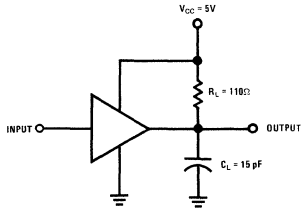
electrical characteristics (Note 2)

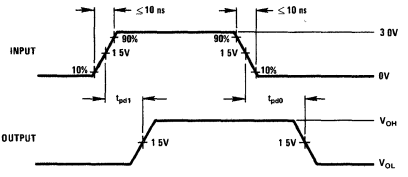
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2			V
Logical "0" Input Voltage				0.8	V
Output Breakdown Voltage					
DM5407/DM7407	V_{CC} = Max, I_{OFF} = 250μA, V_{IN} = 2.0V	30			V
DM5417/DM7417	V_{CC} = Max, I_{OFF} = 250μA, V_{IN} = 2 0V	15			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0 8V, I_{OUT} = Max			0.7	V
	V_{CC} = Min, V_{IN} = 0 8V, I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max V_{IN} = 2 4V			40	μA
	V_{CC} = Max V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max V_{IN} = 0.4V			-1.6	mA
Supply Current – Logical "1"	V_{CC} = Max V_{IN} = 5.0V		29	41	mA
Logical "0"	V_{CC} = Max V_{IN} = 0V		21	30	mA
Input Clamp Voltage	V_{CC} = 5.0V I_{IN} = −12 mA, T_A = 25°C			-1.5	V
Propagation Delay to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 110Ω		20	30	ns
Propagation Delay to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 110Ω		6	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the operation of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5407, DM5417 and across the 0°C to 70°C range for the DM7407, DM7417. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

ac test circuit and switching time waveforms





Level Translators/Buffers

DM5426/DM7426
quad 2-input TTL-MOS interface gate

general description

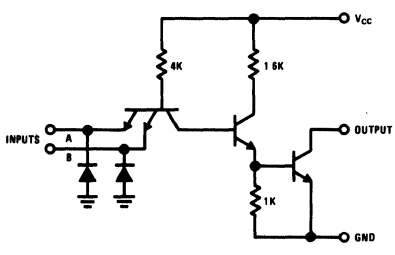
These Series 54/74 compatible gates are high output voltage versions of the DM5403 (SN5403), DM7403 (SN7403). Their open-collector outputs may be "pulled-up" to +15 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

In addition the devices may be used in applications where it is desirable to drive low current relays or lamps that require up to 15 volts.

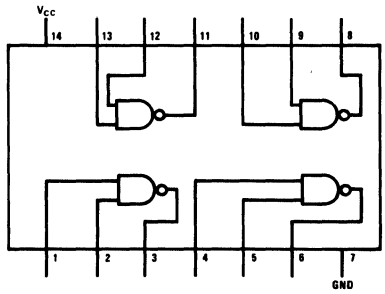
features

- 15V standoff voltage
- Pin compatible with DM5403/DM7403

schematic and connection diagrams



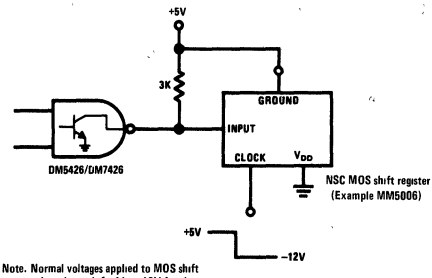
Dual-In-Line Package



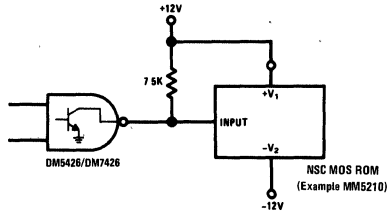
TOP VIEW

Order Number DM5426J or DM7426J
See Package 16
Order Number DM5426N or DM7426N
See Package 22

typical applications



Note. Normal voltages applied to MOS shift registers have been shifted by +10V for this application



absolute maximum ratings

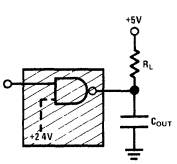
V_{CC}	7V
Input Voltage	5.5V
Output Voltage	15V
Operating Temperature Range	
DM5426	−55°C to 125°C
DM7426	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

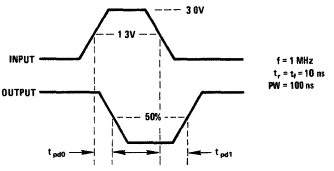
electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	$V_{CC} = \frac{4.5V}{4.75V}$	2.0			V
Logical "0" Input Voltage	$V_{CC} = \frac{4.5V}{4.75V}$			0.8	V
Logical "1" Output Current	$V_{CC} = \frac{4.5V}{4.75V}$ V_{IN} = 0.8V V_{OUT} = 12V			50	μA
Logical "1" Output Breakdown Voltage	$V_{CC} = \frac{4.5V}{4.75V}$ V_{IN} = 0V I_{OUT} = 1 mA	15			V
Logical "0" Output Voltage	$V_{CC} = \frac{4.5V}{4.75V}$ V_{IN} = 2.0V I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 2.4V			40	μA
Logical "1" Input Current	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 5.5V			1	mA
Logical "0" Input Current	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 0.4V			−1.6	mA
Supply Current — Logical "0" (Each Gate)	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 5.0V		3.0	5.1	mA
Supply Current — Logical "1" (Each Gate)	$V_{CC} = \frac{5.5V}{5.25V}$ V_{IN} = 0V		1.0	1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k		8	17	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k		14	24	ns

Note 1: Min/Max units apply across the guaranteed temperature range −25°C to +125°C for the DM5426 and across the 0°C to +70°C for the DM7426 unless otherwise specified. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

ac test circuit and switching time waveforms





Level Translators/Buffers

DM7800/DM8800 dual voltage translator

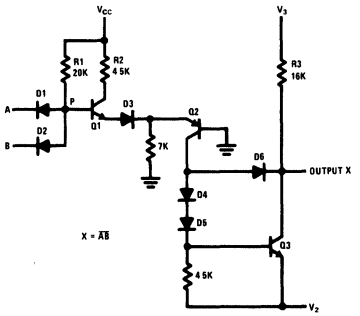
general description

The DM7800/DM8800 are dual voltage translators designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with high impedance junction or MOS FET-type devices. The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

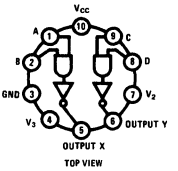
features

- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:
  DM7800 −55°C to +125°C
  DM8800 0°C to +70°C
- Compatible with all MOS devices

schematic and connection diagrams



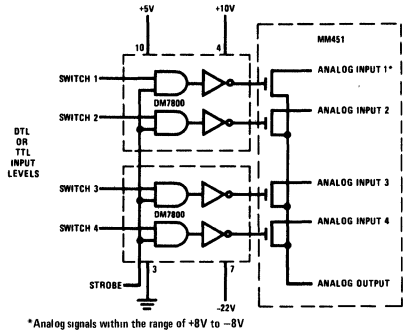
Metal Can Package



Order Number DM7800H
or DM8800H
See Package 12

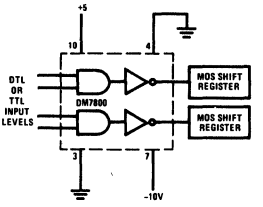
typical applications

4-Channel Analog Switch



*Analog signals within the range of +8V to −8V

Bipolar to MOS Interfacing



absolute maximum ratings

V_{CC} Supply Voltage	7.0V
V_2 Supply Voltage	−30V
V_3 Supply Voltage	+30V
V_3-V_2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
DM7800	−55°C to +125°C
DM8800	0°C to 70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP (Note 4)	MAX	UNITS
Logical "1" Input Voltage	DM7800	V_{CC} = 4.5V	2.0			V
	DM8800	V_{CC} = 4.75V				
Logical "0" Input Voltage	DM7800	V_{CC} = 4.5V			0.8	V
	DM8800	V_{CC} = 4.75V				
Logical "1" Input Current	DM7800	V_{CC} = 5.5V			5	μA
	DM8800	V_{CC} = 5.25V V_{IN} = 2.4V				
Logical "1" Input Current	DM7800	V_{CC} = 5.5V			1	mA
	DM8800	V_{CC} = 5.25V V_{IN} = 5.5V				
Logical "0" Input Current	DM7800	V_{CC} = 5.5V		−0.2	−0.4	mA
	DM8800	V_{CC} = 5.25V V_{IN} = 0.4V				
Output Leakage Current (Note 2)	DM7800	V_{CC} = 5.5V			10	μA
	DM8800	V_{CC} = 5.25V V_{IN} = 0.8V (Note 5)				
Output Collector Resistor		T_A = 25°C	11.5	16.0	20.0	kΩ
Logical "0" Output Voltage	DM7800	V_{CC} = 4.5V			V_2 + 2.0	V
	DM8800	V_{CC} = 4.75V V_{IN} = 2.0V (Note 5)				
Power Supply Current Logical "0" (Note 3) (Each Gate)	DM7800	V_{CC} = 5.5V		0.85	1.6	mA
	DM8800	V_{CC} = 5.25V V_{IN} = 4.5V				
Power Supply Current Logical "1" (Note 3) (Each Gate)	DM7800	V_{CC} = 5.5V		0.22	0.41	mA
	DM8800	V_{CC} = 5.25V V_{IN} = 0V				
Transition Time to Logical "0" Output		T_A = 25°C C = 15 pF (Note 6)	25	70	125	ns
Transition Time to Logical "1" Output		T_A = 25°C C = 15 pF (Note 7)	25	62	125	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for the DM7800 and 0°C to +70°C for the DM8800 unless otherwise specified.
Note 2: Current measured is drawn from V_3 supply.
Note 3: Current measured is drawn from V_{CC} supply.
Note 4: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.
Note 5: Specification applies for all allowable values of V_2 and V_3.
Note 6: Measured from 1.5V on input to 50% level on output.
Note 7: Measured from 1.5V on input to logic "0" voltage, plus 1V.

theory of operation

The two input diodes perform the AND function on TTL or DTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2. The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL and DTL, the interfacing with these types of circuits is achieved.

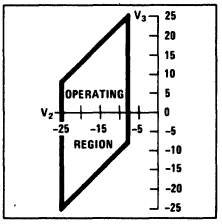
Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2. Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and to Q_3. And when Q_3 turns on the output voltage drops to the logical "0" level.

The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to −25V can be applied to V_2. Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3.

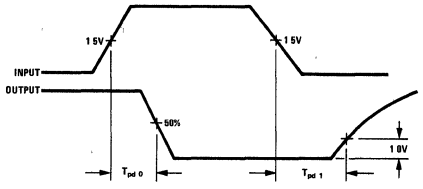
Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the output voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.

selecting power supply voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V_2 is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V_3 is governed by supply V_2. With a value chosen for V_2, V_3 may be selected as any value along a vertical line passing through the V_2 value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



switching time waveforms



Level Translators/Buffers

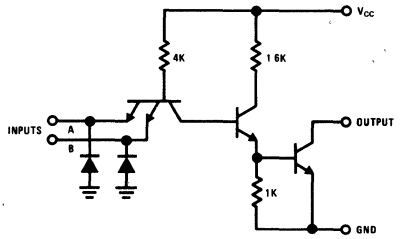
DM7810/DM8810 quad 2-input TTL-MOS interface gate
DM7811/DM8811 quad 2-input TTL-MOS interface gate
DM7812/DM8812 TTL-MOS hex inverter

general description

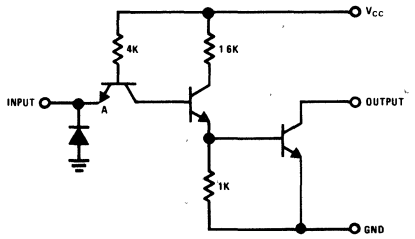
These Series 54/74 compatible gates are high output voltage versions of the DM5401/DM7401 (SN5401/SN7401), DM5403/DM7403 (SN5403/SN7403), and DM5405/DM7405 (SN5405/SN7405). Their open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

In addition the devices may be used in applications where it is desirable to drive low current relays or lamps that require up to 14 volts.

schematic and connection diagrams

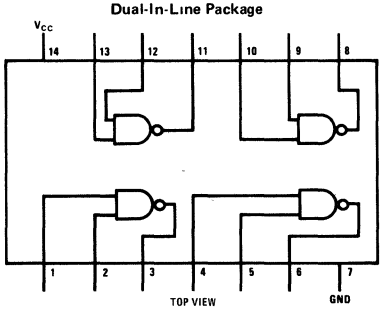


DM7810/DM8810, DM7811/DM8811



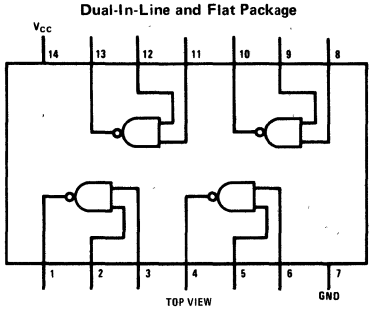
DM7812/DM8812

Dual-In-Line Package



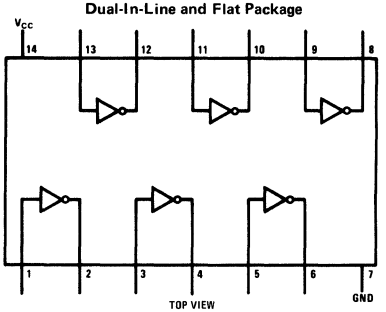
DM7810/DM8810

Dual-In-Line and Flat Package



DM7811/DM8811

Dual-In-Line and Flat Package



DM7812/DM8812

ORDER NUMBER	SEE PKG	ORDER NUMBER	SEE PKG	ORDER NUMBER	SEE PKG
DM7810J	16	DM7810N	22	DM7811W	27
DM7811J	16	DM7811N	22	DM7812W	27
DM7812J	16	DM7812N	22	DM8811W	27
DM8810J	16	DM8810N	22	DM8812W	27
DM8811J	16	DM8811N	22		
DM8812J	16	DM8812N	22		

absolute maximum ratings

V_{CC}	7V
Input Voltage	5.5V
Output Voltage	14V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

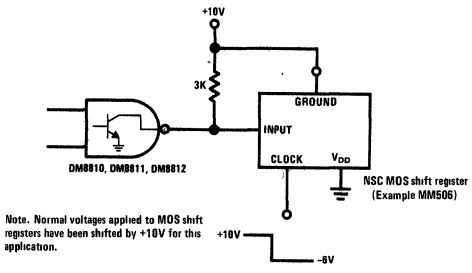
	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM78XX	4.75	5.25	V
DM88XX	4.75	5.25	V
Temperature (T_A)			
DM78XX	−55	+125	°C
DM88XX	0	+70	°C

electrical characteristics (Note 1)

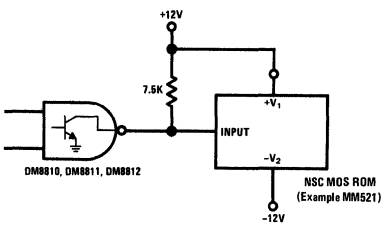
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C I_{IN} = −12 mA			−1.5	V
Logical "1" Input Voltage	V_{CC} = Min	2.0			V
Logical "0" Input Voltage	V_{CC} = Min			0.8	V
Logical "1" Output Current	V_{CC} = Min V_{IN} = 0.8V V_{OUT} = 10V V_{IN} = 0.0V			250 40	μA μA
Logical "1" Output Breakdown Voltage	V_{CC} = Min, V_{IN} = 0V I_{OUT} = 1 mA	14			V
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V I_{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Supply Current — Logical "0" (Each Gate)	V_{CC} = Max, V_{IN} = 5.0V		3.0	5.1	mA
Supply Current — Logical "1" (Each Gate)	V_{CC} = Max, V_{IN} = 0V		1.0	1.8	mA
Propagation Delay Time to a Logical "0", t_{pd0}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	4	12	18	ns
Propagation Delay Time to a Logical "1", t_{pd1}	V_{CC} = 5.0V, T_A = 25°C C_{OUT} = 15 pF, R_L = 1k	18	29	45	ns

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM78XX and across the 0°C to 70°C range for the DM88XX. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

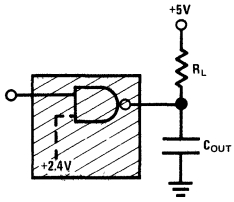
typical applications

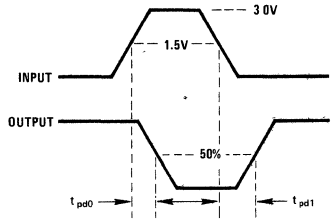


Note. Normal voltages applied to MOS shift registers have been shifted by +10V for this application.



ac test circuit and switching time waveforms





f = 1 MHz
$t_r = t_f$ = 10 ns
PW = 100 ns

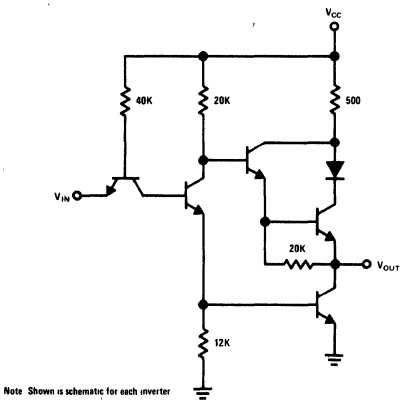
Level Translators/Buffers

DM88L12 TTL-MOS hex inverter/ interface gate

general description

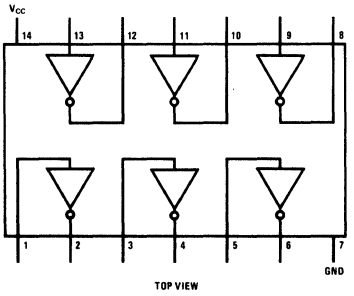
The DM88L12 is a low power TTL to MOS hex inverter element. The outputs may be "pulled up" to +14V in the logical "1" state, thus providing guaranteed interface between TTL and MOS logic levels. The gate may also be operated with V_{CC} levels up to +14V without resistive pull-ups at the outputs and still providing a guaranteed logical "1" level of V_{CC} – 2.2V with an output current of –200 μA.

schematic and connection diagrams



Note Shown is schematic for each inverter

Dual-In-Line and Flat Package

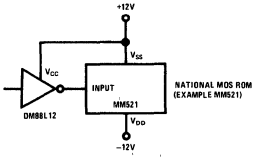


TOP VIEW

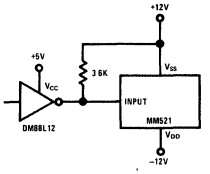
Order Number DM88L12F
See Package 4
Order Number DM88L12J
See Package 16
Order Number DM88L12N
See Package 22

typical applications

TTL Interface to MOS ROM Without Resistive Pull-Up



TTL Interface to MOS ROM With Resistive Pull-Up



ac test circuits

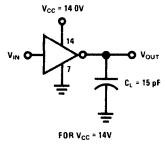


Figure 1

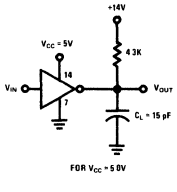
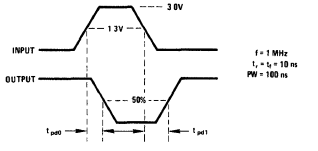


Figure 2

switching time waveforms



absolute maximum ratings (Note 1)

Supply Voltage	15V
Input Voltage	5.5V
Output Voltage.	15V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
DM78L12	4.5	5.5	V
DM88L12	4.75	5.25	V
Temperature			
DM78L12	−55	125	°C
DM88L12	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 14.0V			2.0	1.3		V
	V_{CC} = Min			2.0	1.3		V
Logical "0" Input Voltage	V_{CC} = 14.0V				1 3	0 7	V
	V_{CC} = Min				1.3	0.7	V
Logical "1" Output Voltage	V_{CC} = 14 0V	V_{IN} = 0.7V	I_{OUT} = −200 μA	11 8	12.0		V
	V_{CC} = Min	V_{IN} = 0.7V	I_{OUT} = +200 μA	14 5	15.0		V
	V_{CC} = Min	V_{IN} = 0V	I_{OUT} = −5.0μA	V_{CC} = 1.1V			V
Logical "0" Output Voltage	V_{CC} = 14.0V	V_{IN} = 2.0V	I_{OUT} = 12 mA		0.5	1.0	V
	V_{CC} = Min	V_{IN} = 2.0V	I_{OUT} = 3.6 mA		0.2	0.4	V
Logical "1" Input Current	V_{CC} = 14 0V	V_{IN} = 2.4V			<1	20	μA
	V_{CC} = Max	V_{IN} = 2.4V			<1	10	μA
	V_{CC} = 14.0V	V_{IN} = 5.5V			<1	100	μA
	V_{CC} = Max	V_{IN} = 5.5V			<1	100	μA
Logical "0" Input Current	V_{CC} = 14.0V	V_{IN} = 0.4V			−320	−500	μA
	V_{CC} = Max	V_{IN} = 0.4V			−100	−180	μA
Output Short Circuit Current (Note 3)	V_{CC} = 14.0V	V_{OUT} = 0V		−10	−25	−50	mA
	V_{CC} = Max	V_{OUT} = 0V		−3	−8	−15	mA
Supply Current — Logical "1" (Each Inverter)	V_{CC} = 14.0V	V_{IN} = 0V			0.32	0 50	mA
	V_{CC} = Max	V_{IN} = 0V			0.11	0.16	mA
Logical "0"	V_{CC} = 14.0V	V_{IN} = 5.25V			1 0	1 5	mA
	V_{CC} = Max	V_{IN} = 5.25V			0.3	0.5	mA
Propagation Delay to a Logical "0" from Input to Output, t_{pd0}	V_{CC} = 5.0V, T_A = 25°C	See Figure 2			27	45	ns
Propagation Delay to a Logical "0" from Input to Output, t_{pd0}	V_{CC} = 14.0V, T_A = 25°C	See Figure 1			11	20	ns
Propagation Delay to a Logical "1" from Input to Output, t_{pd1} (Note 4)	V_{CC} = 5.0V, T_A = 25°C	See Figure 2			79	100	ns
Propagation Delay to a Logical "1" from Input to Output, t_{pd1}	V_{CC} = 14.0V, T_A = 25°C	See Figure 1			34	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM78L12 and across the 0°C to +70°C range for the DM88L12. All typicals are given for V_{CC} = 5.0V and T_A = 25°C, or for V_{CC} = 14.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

Note 4: t_{pd1} for V_{CC} = 5.0V is dependent upon the resistance and capacitance used.

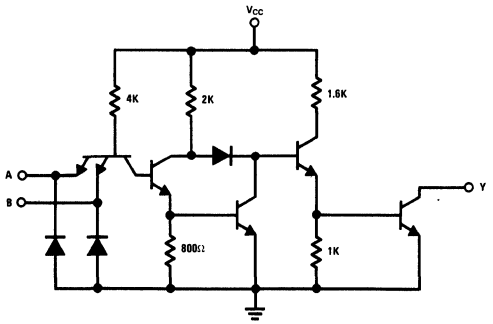
Level Translators/Buffers

DM7819/DM8819 quad 2-input TTL-MOS AND gate

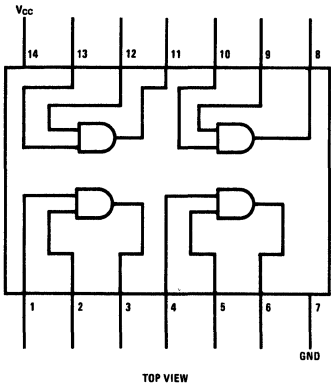
general description

The DM7819 is the high output voltage version of the SN5409. Its open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

schematic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

Order Number DM7819J or DM8819J
See Package 16
Order Number DM7819N or DM8819N
See Package 22
Order Number DM7819W or DM8819W
See Package 27

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7819	4.5	5.5	V
DM8819	4.75	5.25	V
Temperature (T_A)			
DM7819	−55	+125	°C
DM8819	0	70	°C

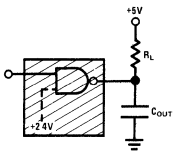
electrical characteristics (Note 2)

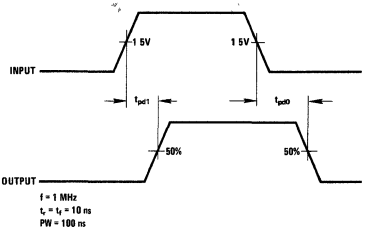
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = Min	2 0			V
Logical "0" Input Voltage	V_{CC} = Min			0 8	V
Logical "1" Output Current	V_{CC} = Min, V_{IN} = 2 0V, V_{OUT} = 10V			40.0	μA
	V_{CC} = Min, V_{IN} = 4.5V, V_{OUT} = 14V			1.0	mA
Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OUT} = 16 mA			0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V			40.0	μA
	V_{CC} = Max, V_{IN} = 5.5V			1 0	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Supply Current — Logical "1"	V_{CC} = Max, V_{IN} = 5V		11 0	21.0	mA
Logical "0"	V_{CC} = Max, V_{IN} = 0V		20 0	33.0	mA
Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V
Propagation Delay to a Logical "0" t_{pd0}					
DM7819 / DM8819	V_{CC} = 5.0V, T_A = 25°C		16.0	24.0	ns
Propagation Delay to a Logical "1" t_{pd1}					
DM7819 / DM8819	V_{CC} = 5.0V, T_A = 25°C		16.0	32.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7819 and across the 0°C to 70°C range for the DM8819 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

ac test circuit and switching time waveforms





f = 1 MHz
$t_r = t_f$ = 10 ns
PW = 100 ns

Memory/Clock Drivers

DH3467C quad PNP core driver

general description

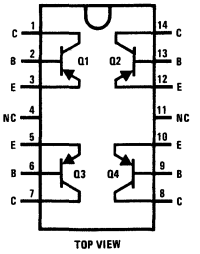
The DH3467C consists of four 2N3467 type PNP transistors mounted in a 14-pin molded dual-in-line package. The device is primarily intended for core memory application requiring operating currents in the ampere range, high stand-off voltage, and fast turn-on and turn-off times.

typical characteristics

Turn-ON Time	18 ns
Turn-OFF Time	45 ns
Collector Current	1A
Collector-Base Breakdown Voltage	120V typ.
Collector Saturation Voltage at I_C = 1A	0.55V
Collector Saturation Voltage at I_C = 0.5A	0.31V

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DH3467CD
See Package 1
Order Number DH3467CN
See Package 22

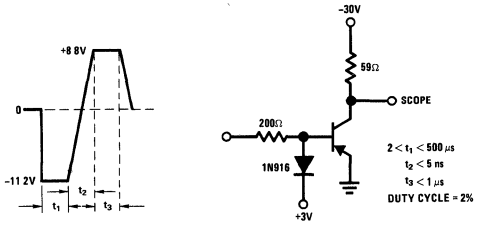


FIGURE 1. Turn-On Equivalent Test Circuit

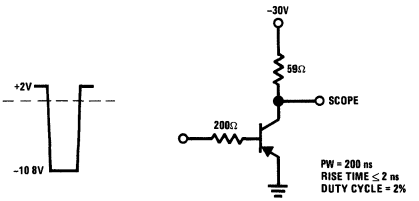


FIGURE 2. Turn-Off Equivalent Test Circuit

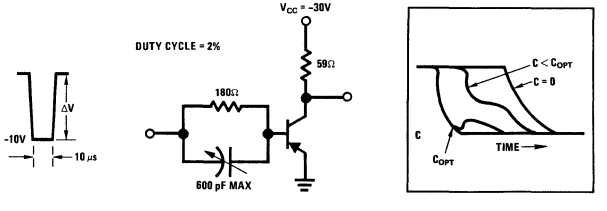


FIGURE 3. Q_T Test Circuit

absolute maximum ratings

Collector to Base Voltage	40V
Collector to Emitter Voltage	40V
Collector to Emitter Voltage (Note 1)	40V
Emitter to Base Voltage	5V
Collector Current – Continuous	1.0A
Power Dissipation (T_A = 25°C) (each device)	0.85W
Power Dissipation (T_A = 25°C) (total package)	2.5W
Operating Junction Temperature	150°C Max
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics (T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Collector to Base Breakdown Voltage (BV_{CBO})	I_C = 10 μA I_E = 0	−40		V
Emitter to Base Breakdown Voltage (BV_{EBO})	I_E = 10 μA I_C = 0	−5 0		V
Collector to Emitter Breakdown Voltage (Note 1) (BV_{CEO})	I_C = 10 mA I_B = 0	−40		V
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 150 mA V_{CE} = −1.0V	40		
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 500 mA V_{CE} = −1 0V	40	120	
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 1.0A V_{CE} = −5 0V	40		
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 150 mA I_B = 15 mA		−0.30	V
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 500 mA I_B = 50 mA		−0.50	V
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 1 0A I_B = 100 mA		−1.0	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 150 mA I_B = 15 mA		−1.0	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 500 mA I_B = 50 mA	−0.8	−1.2	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 1.0A I_B = 100 mA		−1.6	V
Collector Cutoff Current (I_{CBO})	V_{CB} = −30V I_B = 0		100	nA
Collector Cutoff Current ($I_{CBO(100°C)}$)	V_{CB} = −30V I_B = 0		15	μA
Collector Cutoff Current (I_{CEX})	V_{CB} = −30V V_{EB} = −3.0V		100	nA
Base Cutoff Current (I_{BL})	V_{CB} = −30V V_{EB} = −3.0V		120	nA
Total Control Charge (Figure 3) (Q_T)	I_C = 500 mA I_B = 50 mA		6 0	nC
Turn On Delay Time (Figure 1) (t_d)	I_C = 500 mA I_{B1} = 50 mA		10	ns
Rise Time (Figure 1) (t_r)	I_C = 500 mA I_{B1} = 50 mA		30	ns
Storage Time (Figure 2) (t_s)	I_C = 500 mA I_{B1} = I_{B2} = 50 mA		60	ns
Fall Time (Figure 2) (t_f)	I_C = 500 mA I_{B1} = I_{B2} = 50 mA		30	ns
Output Capacitance (f = 100 kHz) (C_{ob})	I_E = 0 V_{CB} = −10V		25	pF
Input Capacitance (f = 100 kHz) (C_{ib})	I_C = 0 V_{CB} = −0 5V		100	pF
High Frequency Current Gain (f = 100 MHz) (h_{fe})	I_C = 50 mA V_{CE} = 10V	1.75		

Note 1: Pulsed test, PW = 300μs, duty cycle = 1%

Memory/Clock Drivers

DH3725C quad NPN core driver

general description

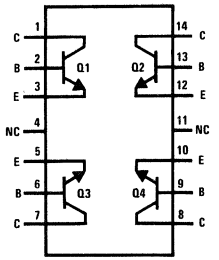
The DH3725C consists of four 2N3725 type NPN transistors mounted in a 14-pin molded dual-in-line package. The device is primarily intended for core memory application requiring operating currents in the ampere range, high stand-off voltage, and fast turn-on and turn-off times.

typical characteristics

Turn-ON Time	18 ns
Turn-OFF Time	45 ns
Collector Current	1A
Collector-Base Breakdown Voltage	120V typ.
Collector Saturation Voltage at I_C = 1A	0.55V
Collector Saturation Voltage at I_C = 0.5A	0.31V

connection diagram

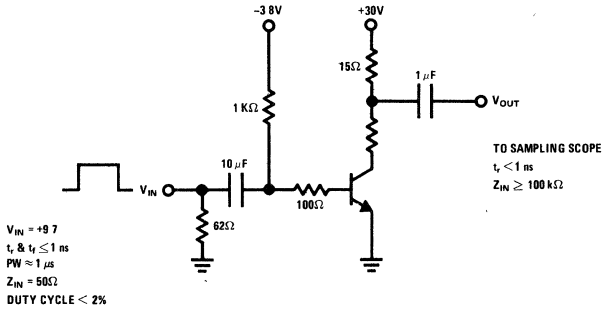
Dual-In-Line Package



TOP VIEW

Order Number DH3725CD
See Package 1
Order Number DH3725CN
See Package 22

switching time test circuit



$I_C \approx 500$ mA, $I_{B1} \approx 50$ mA, $I_{B2} \approx -50$ mA

absolute maximum ratings

Collector to Base Voltage	80V
Collector to Emitter Voltage	80V
Collector to Emitter Voltage (Note 1)	50V
Emitter to Base Voltage	6V
Collector Current – Continuous	1.0A
Power Dissipation (T_A = 25°C)	0.6W
Power Dissipation (T_C = 25°C)	1.5W
Operating Junction Temperature	150°C Max
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics – Each transistor (T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector to Emitter Sustaining Voltage (V_{CEO} (sust)	I_C = 10 mA, I_B = 0	50			V
Collector to Emitter Breakdown Voltage (BV_{CES})	I_C = 10 μA, V_{BE} = 0	80			V
Collector to Base Breakdown Voltage (BV_{CBO})	I_C = 10 μA, I_E = 0	80			V
Emitter to Base Breakdown Voltage (BV_{EBO})	I_C = 0, I_E = 10 μA	6.0			V
Collector Saturation Voltage ($V_{CE\ (Sat)}$) (Note 2)	I_C = 1A, I_B = 100 mA		0.55	0.95	V
	I_C = 0.5A, I_B = 50 mA		0.31	0.52	V
	I_C = 0.1A, I_B = 10 mA		0.19	0.26	V
DC Pulse Current Gain (h_{FE}) (Note 2)	I_C = 1A, V_{CE} = 5V	25	65		
	I_C = 0.5A, V_{CE} = 1V	35	45		
	I_C = 0.1A, V_{CE} = 1V	60	90	150	
Base Saturation Voltage (V_{BE} (Sat) (Note 2)	I_C = 1A, I_B = 100 mA		1.10	1.70	V
	I_C = 0.5A, I_B = 50 mA		0.95	1.20	V
	I_C = 0.1A, I_B = 10 mA		0.75	0.86	V
Collector Cutoff Current (I_{CBO})	I_E = 0, V_{CB} = 60V		0.33	1.70	μA
Turn-ON Time	I_C = 0.5A, I_{B1} = 50 mA (See test circuit)		18	30	ns
Turn-OFF Time	I_C = 0.5A, I_{B1} = 50 mA I_{B2} = 50 mA (See test circuit)		45	60	ns
High Frequency Current Gain	f = 100 MHz, I_C = 50 mA, V_{CE} = 10V	2.5	4.5		
Common Base, Open Circuit, Output Capacitance	I_E = 0, V_{CB} = 10V		4.8	10	pF
Common Base, Open Circuit, Input Capacitance	I_C = 0, V_{BE} = 0.5V		40	55	pF

Note 1: Ratings refer to a high-current point where collector-to-emitter voltage is lowest.
Note 2: Pulse conditions. Length = 300 μs, duty cycle = 1%.

Memory/Clock Drivers

LM75324 memory driver with decode inputs

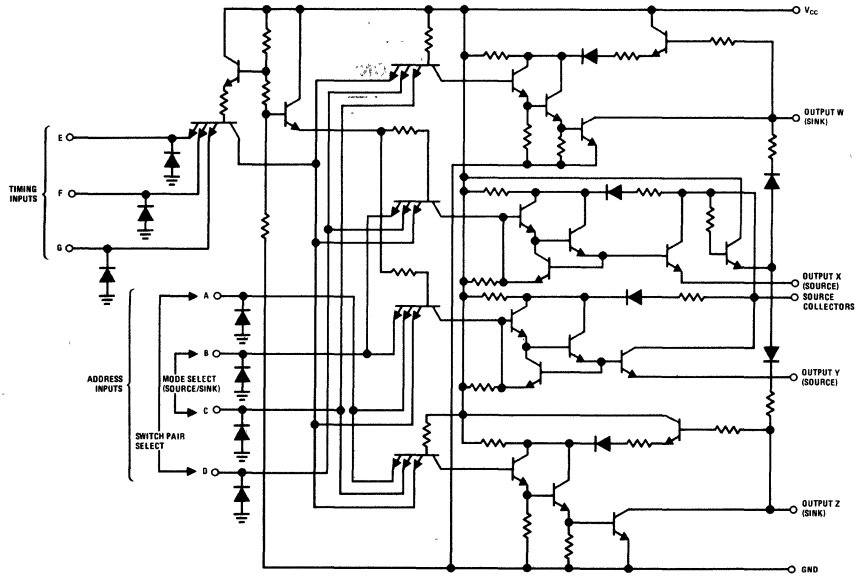
general description

The LM75324 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X)

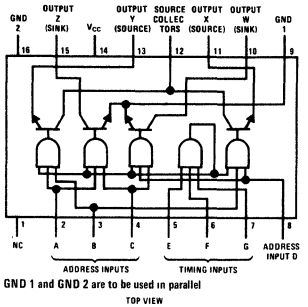
features

- Output capability 400 mA
- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- Fast switching times
- Operation 0°C to +70°C
- DTL/TTL compatible
- Input clamping diodes

schematic and connection diagrams



Dual-In-Line Package (J)

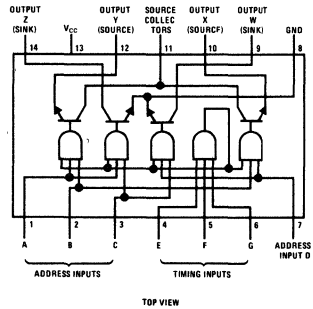


GND 1 and GND 2 are to be used in parallel

TOP VIEW

Order Number LM75324J
See Package 17

Dual-In-Line Package (N)



TOP VIEW

Order Number LM75324N
See Package 22

absolute maximum ratings

Supply Voltage V_{CC} (Note 1)	17V
Input Voltage (Note 2)	5.5V
Operating Case Temperature Range	0°C to +70°C
Continuous Total Power Dissipation at (or Below) +70°C Case Temperature	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics (V_{CC} = 14V, T_C = 0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Required to Insure Logical "1" At Any Input ($V_{IN(1)}$)	Figure 1	3.5			V
Input Voltage Required to Insure Logical "0" At Any Input ($V_{IN(0)}$)	Figure 1			0.8	V
Logical "1" Level Address Input Current ($I_{IN(1)}$)	V_{IN} = 5V, Figure 1			200	μA
Logical "1" Level Timing Input Current ($I_{IN(1)}$)	V_{IN} = 5V, Figure 1			100	μA
Logical "0" Level Address Input Current ($I_{IN(0)}$)	V_{IN} = 0V, Figure 1			−6	mA
Logical "0" Level Timing Input Current ($I_{IN(0)}$)	V_{IN} = 0V, Figure 1			−12	mA
Sink Saturation Voltage (V_{sat})	$I_{SINK} \simeq$ 420 mA, R_L = 53Ω, Figure 2		0.75	0.85	V
Source Saturation Voltage (V_{sat})	$I_{SOURCE} \simeq$ −420 mA, R_L = 47.5Ω, Figure 2		0.75	0.85	V
Output Reverse Current (Off State) (I_{OFF})	V_{IN} = 0V, Figure 1		125	200	μA
Supply Current, All Sources and Sinks Off (I_{CC})	V_{IN} = 0V, Figure 3		12.5	15	mA
Supply Current, Either Sink Selected (I_{CC})	Figure 4		30	40	mA
Supply Current, Either Source Selected (I_{CC})	Figure 4		25	35	mA
Input Clamp Voltage (V_1)	I_{IN} = −12 mA, T_A = 25°C			−1 5	V

ac switching characteristics (V_{CC} = 14V, T_C = 25°C)

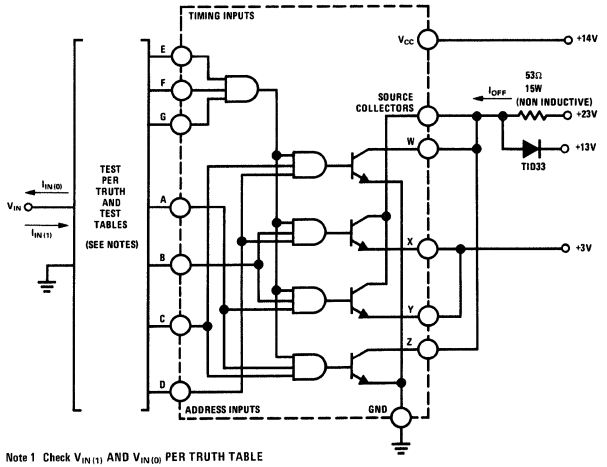
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" Level, Source Output (t_{pd1})	R_{L1} = 53Ω, R_{L2} = 500Ω, C_L = 20 pF, Figure 5			90	ns
Propagation Delay Time to Logical "0" Level, Source Output (t_{pd0})				50	ns
Propagation Delay Time to Logical "1" Level, Sink Output (t_{pd1})	R_L = 53Ω, C_L = 20 pF, Figure 6			110	ns
Propagation Delay Time to Logical "0" Level, Sink Output (t_{pd0})				40	ns
Sink Storage Time (t_s)				70	ns

Note 1: Voltage values are with respect to network ground terminal.
Note 2: Input signals must be zero or positive with respect to network ground terminal.

truth table

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

test circuits and switching time waveforms



Note 1 Check $V_{IN(1)}$ AND $V_{IN(0)}$ PER TRUTH TABLE

Note 2 Measure $I_{IN(0)}$ per test table

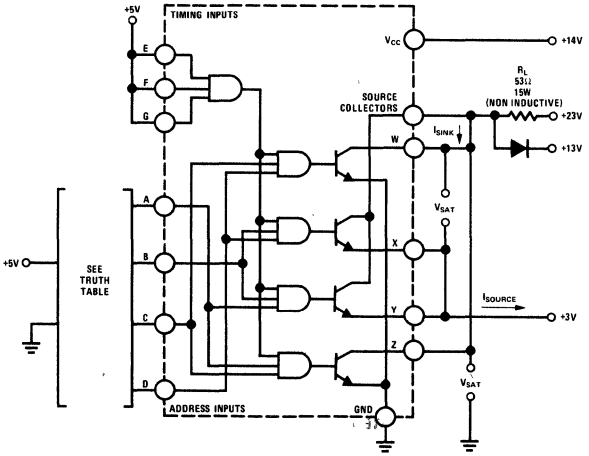
Note 3 When measuring $I_{IN(1)}$, all other inputs are at GND Each input is tested separately

TEST TABLE FOR $I_{IN(0)}$

APPLY 3.5V	GROUND	TEST $I_{IN(0)}$
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

FIGURE 1. $V_{IN(0)}$, $V_{IN(1)}$, $I_{IN(0)}$, $I_{IN(1)}$, and I_{OFF}

test circuits and switching time waveforms (con't)



Note This parameter must be measured using pulse techniques
t_P = 500 ns, duty cycle ≤ 1%

FIGURE 2. $V_{(SAT)}$

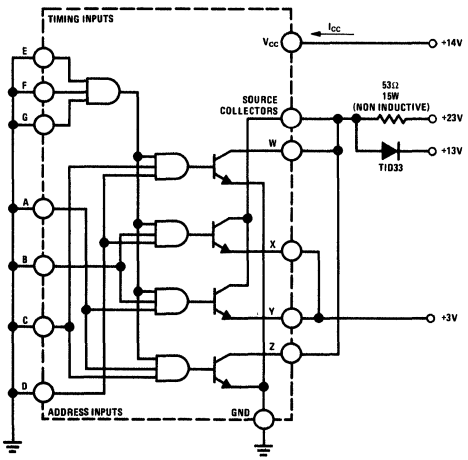
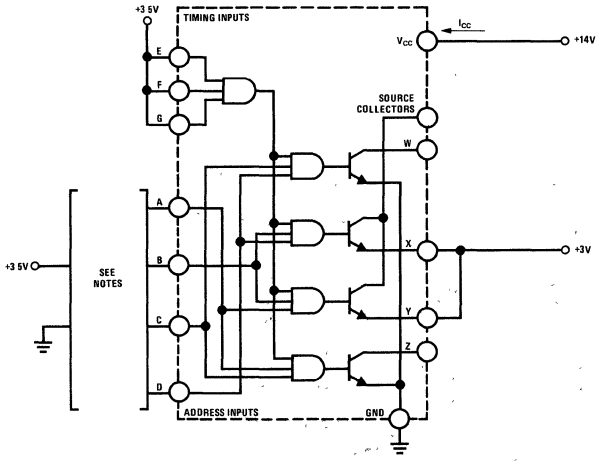


FIGURE 3. I_{CC} (All Outputs Off)

test circuits and switching time waveforms (con't)



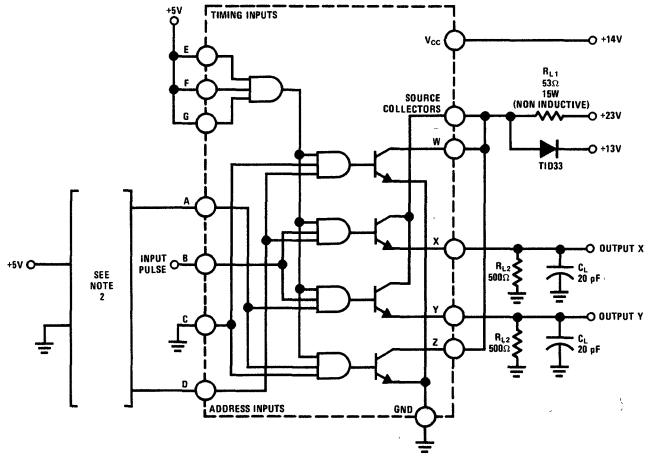
Note 1 GND A and B, apply +3.5V to C and D, and measure I_{CC} (output W is on)

Note 2 GND B and D, apply +3.5V to A and C, and measure I_{CC} (output Z is on)

Note 3 GND A and C, apply +3.5V to B and D, and measure I_{CC} (output X is on)

Note 4 GND C and D, apply +3.5V to A and B, and measure I_{CC} (output Y is on)

FIGURE 4. I_{CC} (One Output On)



Note 1 The input waveform is supplied by a generator with the following characteristics $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, and $Z_{OUT} \approx 50\Omega$

Note 2 When measuring delay times at output X, apply +5V to input D, and GND A. When measuring delay times at output Y, apply +5V to input A, and GND D

Note 3 C_L includes probe and jig capacitance

Note 4 Unless otherwise noted all resistors are 0.5W

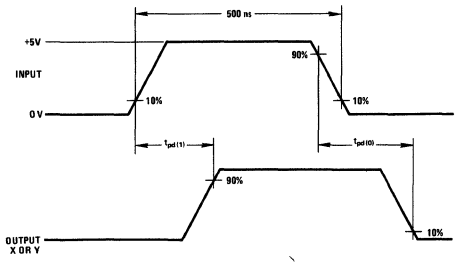
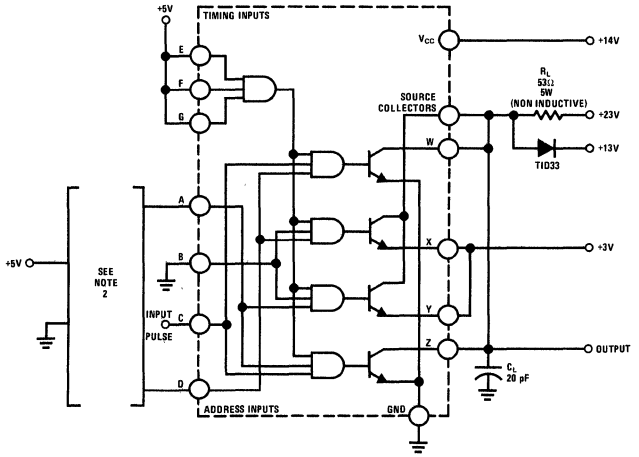


FIGURE 5. Source-Output Switching Times

test circuits and switching time waveforms (con't)



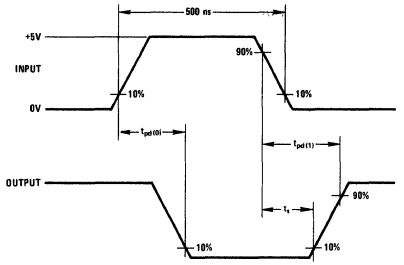


FIGURE 6. Sink-Output Switching Times

Note 1 The input waveform is supplied by a generator with the following characteristics. $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, $Z_{OUT} \approx 50\Omega$.

Note 2 When measuring delay times at output W, apply +5V to input D, and GND A When measuring delay times at output Z, apply +5V to input A, and GND D

Note 3 C_L includes probe and jig capacitance

Memory/Clock Drivers

LM55325/LM75325 memory drivers general description

The LM55325 and LM75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs These circuits are designed for use with magnetic memories

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs Inputs A and B determine source selection while the source strobe (S_1) allows the selected source turn on In the same manner, inputs C and D determine sink selection while the sink strobe (S_2) allows the selected sink turn on

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2} This protects the outputs from voltage surges associated with switching inductive loads

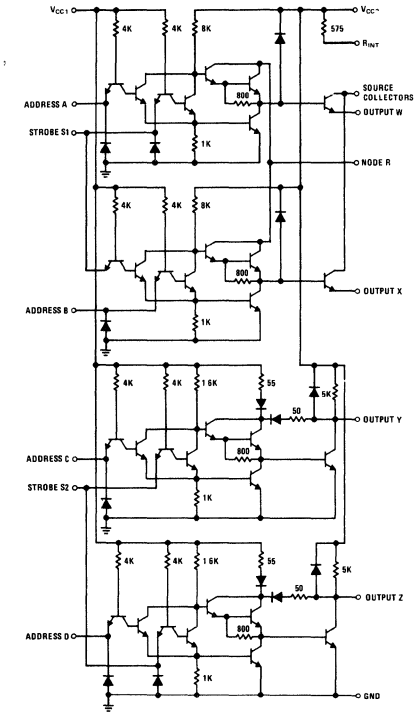
The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally activating an internal resistor connected from V_{CC2} to Node R This provides adequate base drive for source currents up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V

The LM55325 operates over the full military temperature range of -55°C to +125°C, while the LM75325 operates from 0°C to +70°C

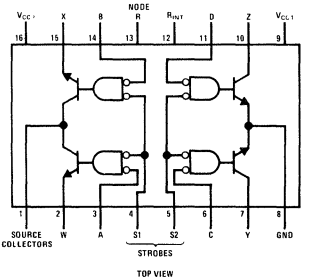
features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- DTL/TTL compatible

schematic and connection diagrams



Dual-In-Line Package



Order Number LM55325J or LM75325J
See Package 17

Order Number LM75325N
See Package 23

truth table

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE Not more than one output is to be on at any one time

absolute maximum ratings

Supply Voltage V_{CC1} (Note 1)		7V
Supply Voltage V_{CC2} (Note 1)		25V
Input Voltage (Any Address or Strobe Input)		5.5V
Continuous Total Dissipation at (or Below) +70°C Free-Air Temperature (Note 2)		800 mW
Operating Temperature Range	LM55325	−55°C to +125°C
	LM75325	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55325			LM75325			
		MIN	TYP*	MAX	MIN	TYP*	MAX	
High Level Input Voltage (V_{IH})	Figure 1 and 2	2			2			V
Low Level Input Voltage (V_{IL})	Figure 3 and 4			0.8			0.8	V
Input Clamp Voltage (V_I)	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{IN} = −12 mA, T_A = 25°C, Figure 5		−1.3	−1.7		−1.3	−1.7	V
Source Collectors Terminal Off State Current (I_{OFF})	V_{CC1} = 4.5V, V_{CC2} = 24V, Full Range, Figure 1			500			200	μA
Source Collectors Terminal Off State Current (I_{OFF})	V_{CC1} = 4.5V, V_{CC2} = 24V, T_A = 25°C, Figure 1		3	150		3	200	μA
High Level Sink Output Voltage (V_{OH})	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{OUT} = 0V, Figure 2	19	23		19	23		V
Saturation Voltage Source Outputs** (V_{SAT})	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SOURCE} ≈ −600 mA, Full Range, (Note 3) Figure 3			0.9			0.9	V
Saturation Voltage Source Outputs** (V_{SAT})	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SOURCE} ≈ −600 mA, T_A = 25°C, (Note 3) Figure 3		0.43	0.7		0.43	0.75	V
Saturation Voltage Sink Outputs** (V_{SAT})	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SINK} ≈ 600 mA, Full Range, (Note 3) Figure 4			0.9			0.9	V
Saturation Voltage Sink Outputs** (V_{SAT})	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SINK} ≈ 600 mA, T_A = 25°C, (Note 3) Figure 4		0.43	0.7		0.43	0.75	V
Input Current at Maximum Input Voltage Address Inputs (I_I)	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 5.5V, Figure 5			1			1	mA
Input Current at Maximum Input Voltage Strobe Inputs (I_I)	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 5.5V, Figure 5			2			2	mA
High Level Input Current Address Inputs (I_{IH})	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 2.4V, Figure 5		3	40		3	40	μA
High Level Input Current Strobe Inputs (I_{IH})	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 2.4V, Figure 5		6	80		6	80	μA
Low Level Input Current Address Inputs (I_{IL})	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 0.4V, Figure 5		−1	−1.6		−1	−1.6	mA
Low Level Input Current Strobe Inputs (I_{IL})	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 0.4V, Figure 5		−2	−3.2		−2	−3.2	mA
Supply Current, All Sources and Sinks Off From V_{CC1} ($I_{CC\,OFF}$)	V_{CC1} = 5.5V, V_{CC2} = 24V, T_A = 25°C, Figure 6		14	22		14	22	mA
Supply Current, All Sources and Sinks Off From V_{CC2} ($I_{CC\,OFF}$)	V_{CC1} = 5.5V, V_{CC2} = 24V, T_A = 25°C, Figure 6		7.5	20		7.5	20	mA
Supply Current From V_{CC1}, Either Sink On (I_{CC1})	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SINK} = 50 mA, T_A = 25°C, Figure 7		55	70		55	70	mA
Supply Current From V_{CC2}, Either Source On (I_{CC2})	V_{CC1} = 5.5V, V_{CC} = 24V, I_{SOURCE} = −50 mA, T_A = 25°C, Figure 8		32	50		32	50	mA

Note 1: Voltage values are with respect to network ground terminal.

Note 2: For operation of LM55325 above +70°C free-air temperature, refer to Dissipation Derating Curve (Figure 12).

Note 3: These parameters must be measured using pulse techniques. t_W = 200μs, duty cycle ≤ 2%.

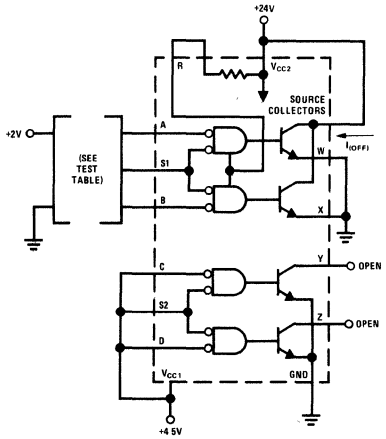
*All typical values are at T_A = 25°C.

**Not more than one output is to be on at any one time.

ac switching characteristics (V_{CC1} = 5V, T_A = 25°C)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Propagation Delay Time, Low to High Level Output to Source Collectors (t_{PLH})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		25	50	ns
Propagation Delay Time, High to Low Level Output to Source Collectors (t_{PHL})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		25	50	ns
Transition Time, Low to High Level Output to Source Outputs (t_{TLH})	V_{CC2} = 20V, R_L = 1 kΩ, C_L = 25 pF, Figure 10		55		ns
Transition Time, High to Low Level Output to Source Outputs (t_{THL})	V_{CC2} = 20V, R_L = 1 kΩ, C_L = 25 pF, Figure 10		7		ns
Propagation Delay Time, Low to High Level Output to Sink Outputs (t_{PLH})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		20	45	ns
Propagation Delay Time, High to Low Level Output to Sink Outputs (t_{PHL})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		20	45	ns
Transition Time, Low to High Level Output to Sink Outputs (t_{TLH})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		7	15	ns
Transition Time, High to Low Level Output to Sink Outputs (t_{THL})	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		9	20	ns
Storage Time, Sink Outputs (t_S)	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, Figure 9		15	30	ns

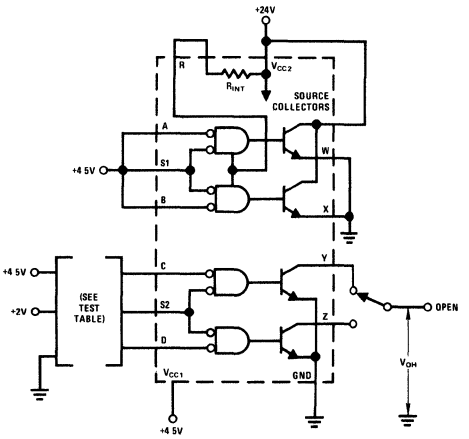
dc test circuits



TEST TABLE

A	B	S1
GND	GND	2V
2V	2V	GND

FIGURE 1. I_{OFF}

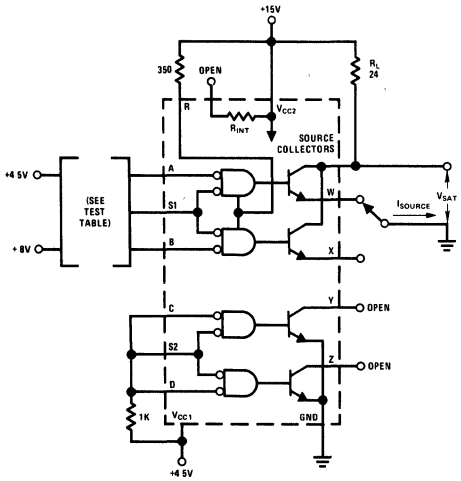


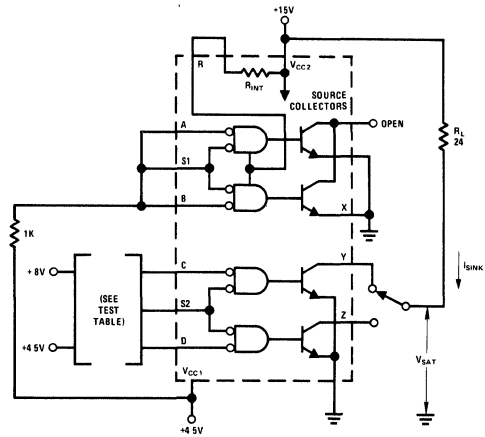
TEST TABLE

C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}

FIGURE 2. V_{IH} and V_{OH}

dc test circuits(con't)





Note 1. Figures 3 and 4 parameters must be measured using pulse techniques $t_W = 200\mu s$, duty cycle $\leq 2\%$

TEST TABLE

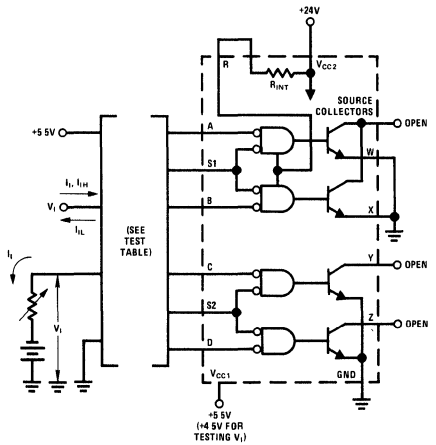
A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

FIGURE 3. V_{IL} and Source V_{SAT}

TEST TABLE

C	D	S2	Y	Z
0.8V	4.5V	0.8V	R_L	OPEN
4.5V	0.8V	0.8V	OPEN	R_L

FIGURE 4. V_{IL} and Sink V_{SAT}



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5V MEASURE I_I / APPLY V_I = 2.4V MEASURE I_{IH}	GROUND	APPLY 5.5V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4V, MEASURE I_{IL} / APPLY I_I = −10 mA, MEASURE V_I	APPLY 5.5V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5. V_I, I_I, I_{IH}, and I_{IL}

dc test circuits(con't)

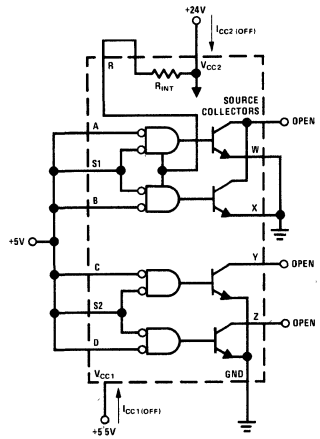
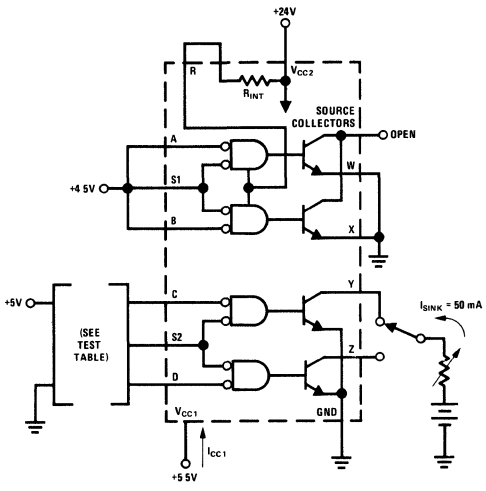


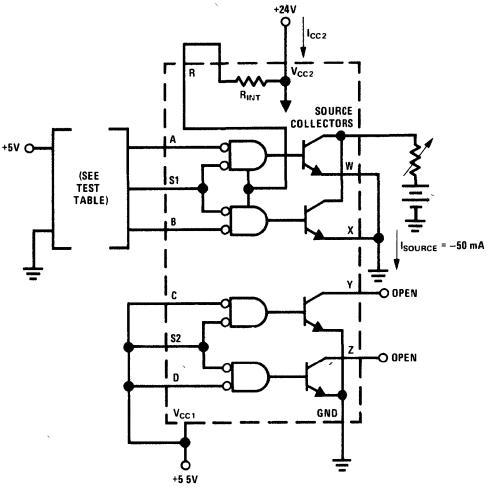
FIGURE 6. $I_{CC1(OFF)}$ and $I_{CC2(OFF)}$



TEST TABLE

C	D	S2	Y	Z
GND	5V	GND	$I_{(SINK)}$	OPEN
5V	GND	GND	OPEN	$I_{(SINK)}$

FIGURE 7. I_{CC1}, Either Sink On

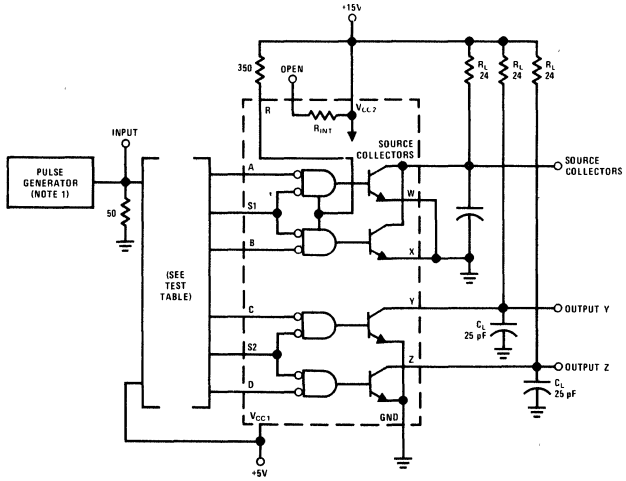


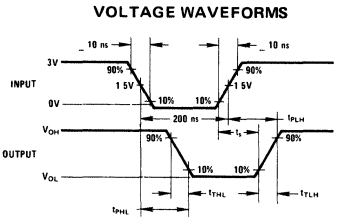
TEST TABLE

A	B	S1
GND	5V	GND
5V	GND	GND

FIGURE 8. I_{CC2}, Either Source On

dc test circuits(con't)





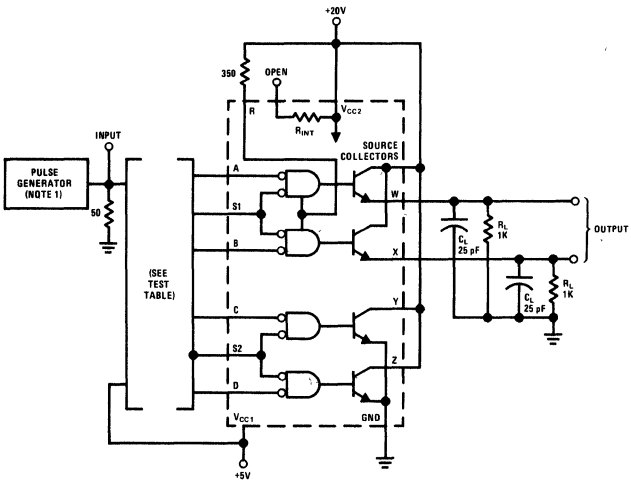
Note 1 The pulse generator has the followng characteristics $Z_{OUT} = 50\Omega$, duty cycle $\leq 1\%$.

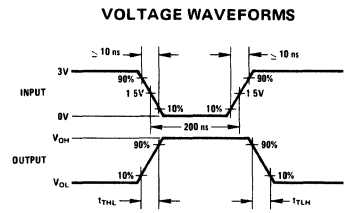
Note 2 C_L includes probe and jig capacitance

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1

FIGURE 9. Switching Times





Note 1 The pulse generator has the followng characteristics $Z_{OUT} = 50\Omega$, duty cycle $\leq 1\%$

Note 2 C_L includes probe and jig capacitance

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2

FIGURE 10. Transition Times of Source Outputs

applications

External Resistor Calculation

A typical magnetic-memory word drive requirement is shown in Figure 11. A source-output transistor of one LM75325 delivers load current (I_L). The sink-output transistor of another LM75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \quad (1)$$

where: R_{ext} is in kΩ,

$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts, V_S is the source output voltage in volts with respect to ground, I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \quad (2)$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\ I_L \quad (3)$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)}$ = 20V and V_L = 3V while I_L of 500 mA flows. Using Equation 1:

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

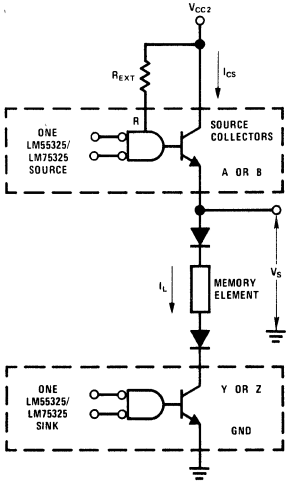
and from Equation 2:

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.



Note 1 For clarity, partial logic diagrams of two LM55325's are shown
Note 2 Source and sink shown are in different packages

FIGURE 11. Typical Application Data

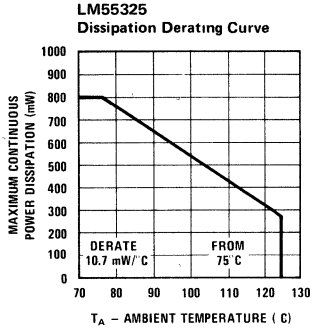


FIGURE 12. Thermal Information

Memory/Clock Drivers

MH0007/MH0007C dc coupled MOS clock driver

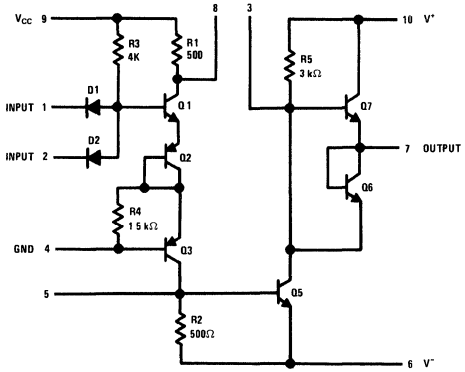
general description

The MH0007 is a voltage translator and power booster designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with inputs or clocks of MOS FET type devices. The design allows the user a wide latitude in selection of supply voltages, and is especially useful in normally "off" applications, since power dissipation is typically only 5 milliwatts in the "off" state.

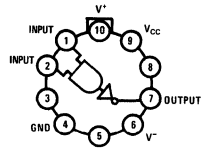
features

- 30 volts (max) output swing
- Standard 5V power supply
- Peak currents in excess of ±300 mA available
- Compatible with all MOS devices
- High speed: 5 MHz with nominal load
- External trimming possible for increased performance

schematic and connection diagram



10 Pin TO-100 Package

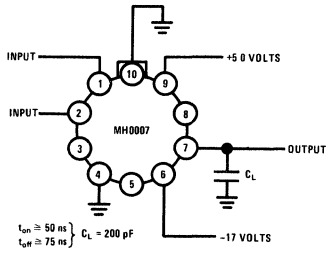


TOP VIEW

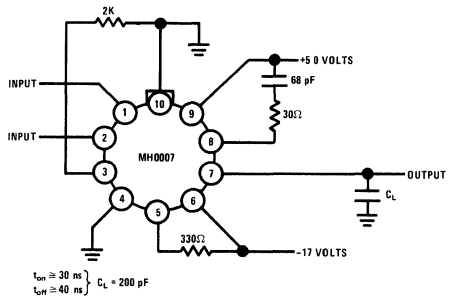
Order Number MH0007H
or MH0007CH
See Package 13

typical applications

Switching Time Test Configuration



High Speed Operation



absolute maximum ratings

V_{CC} Supply Voltage	8V
V^- Supply Voltage	−40V
V^+ Supply Voltage	+28V
$(V^+ - V^-)$ Voltage Differential	30V
Input Voltage	5.5V
Power Dissipation (T_A = 25°C)	800 mW
Peak Output Current	±500 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range MH0007	−55°C to +125°C
MH0007C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

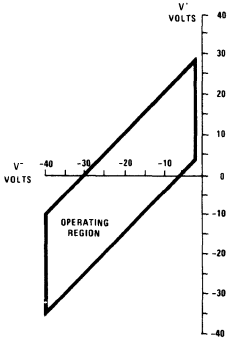
PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.2			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			100	μA
Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V		1.0	1.5	mA
Logical "1" Output Voltage	V_{CC} = 5.5V, I_{OUT} = 30 mA, V_{IN} = 0.8V	$V^+ - 4.0$			V
	V_{CC} = 5.5V, I_{OUT} = 1 mA, V_{IN} = 0.8V	$V^+ - 2.0$			V
Logical "0" Output Voltage	V_{CC} = 4.5V, I_{OUT} = 30 mA, V_{IN} = 2.2V			$V^- + 2.0$	V
Transition Time to Logical "0" Output	C_L = 200 pF (Note 3)		50		ns
Transition Time to Logical "1" Output	C_L = 200 pF (Note 3)		75		ns

Note 1: Min/max limits apply across the guaranteed range of −55°C to +125°C for the MH0007, and from 0°C to +85°C for the MH0007C, for all allowable values of V^- and V^+

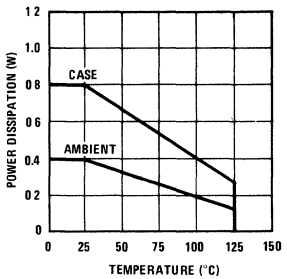
Note 2: All typical values measured at T_A = 25°C with V_{CC} = 5.0 volts, V^- = −25 volts, V^+ = 0 volts.

Note 3: Transition time measured from time V_{IN} = 50% value until V_{OUT} has reached 80% of final value.

Allowable Values for V^- and V^+



Maximum Power Dissipation



3

Memory/Clock Drivers

MH0009/MH0009C dc coupled two phase MOS clock driver

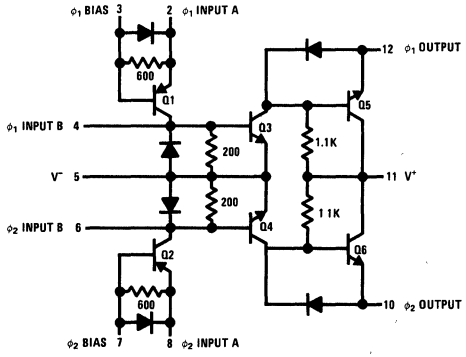
general description

The MH0009/MH0009C is high speed, DC coupled, dual MOS clock driver designed to operate in conjunction with high speed line drivers such as the DM8830, DM7440, or DM7093. The transition from TTL/DTL to MOS logic level is accomplished by PNP input transistors which also assure accurate control of the output pulse width.

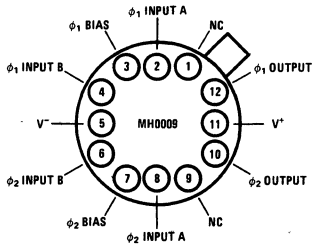
features

- DC logically controlled operation
- Output Swings – to 30V
- Output Currents – in excess of ±500 mA
- High rep rate – in excess of 2 MHz
- Low standby power

schematic and connection diagrams



12-Lead TO-8 Package



$V^+ = +5.0V$

V^- V^+ −12V

Order Number MH0009G or MH0009CG
See Package 6

typical application

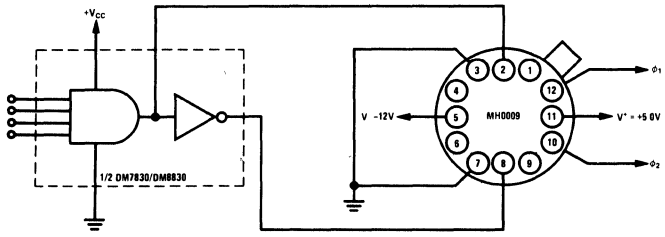


FIGURE 1

absolute maximum ratings

V^- Supply Voltage: Differential (Pin 5 to Pin 3) or (Pin 5 to Pin 7)	-40V
V^+ Supply Voltage: Differential (Pin 11 to Pin 5)	30V
Input Current. (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±500 mA
Power Dissipation (Note 2 and Figure 2)	1.5W
Storage Temperature	-65°C to +150°C
Operating Temperature: MH0009	-55°C to +125°C
MH0009C	0°C to 85°C
Lead Temperature (Soldering, 10 Sec.)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ON}	C_{IN} = .0022 μF C_L = 001 μF		10	35	ns
t_{rise}	C_{IN} = .0022 μF C_L = 001 μF		40	50	ns
Pulse Width (50% to 50%)	C_{IN} = 0022 μF C_L = .001 μF	340	400	440	ns
t_{fall}	C_{IN} = 0022 μF C_L = .001 μF		80	120	ns
t_{delay}	C_{IN} = 600 pF C_L = 200 pF		10		ns
t_{rise}	C_{IN} = 600 pF C_L = 200 pF		15		ns
Pulse Width (50% to 50%)	C_{IN} = 600 pF C_L = 200 pF	40	70	120	ns
t_{fall}	C_{IN} = 600 pF C_L = 200 pF		40		ns

Note 1: Characteristics apply for circuit of Figure 1 With V^- = -20 volts; V^+ = 0 volts; V_{CC} = 5 0 volts. Minimum and maximum limits apply from -55°C to +125°C for the MH0009 and from 0°C to +85°C for the MH0009C Typical values are for T_A = 25°C

Note 2: Transient power is given by $P = fC_L (V^+ - V^-)^2$ watts, where f = repetition rate, C_L = load capacitance, and $(V^+ - V^-)$ = output swing

Note 3: For typical performance data see the MH0013/MH0013C data sheet.

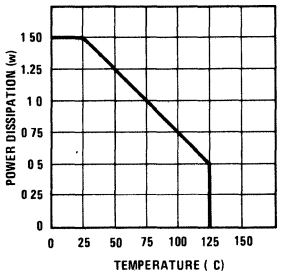


FIGURE 2. Maximum Power Dissipation

Memory/Clock Drivers

MH0012/MH0012C high speed MOS clock driver

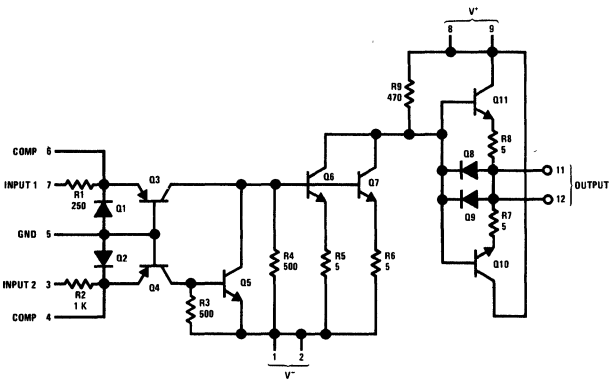
general description

The MH0012/MH0012C is a high performance clock driver that is designed to be driven by the DM7830/DM8830 or other line drivers or buffers with high output current capability. It will provide a fixed width pulse suitable for driving MOS shift registers and other clocked MOS devices.

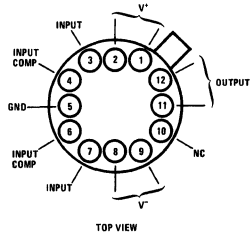
features

- High output voltage swings—12 to 30 volts
- High output current drive capability—1000 mA peak
- High repetition rate—10 MHz at 18 volts into 100 pF
- Low standby power—less than 30 mW

schematic and connection diagrams

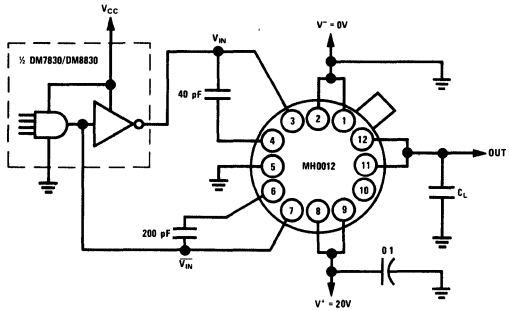


12-lead TO-8 Package

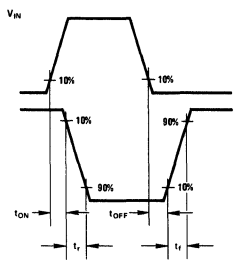


Order Number MH0012G
or MH0012CG
See Package 6

typical application (ac test circuit)



timing diagram



absolute maximum ratings

V^- Supply Voltage	Differential (Pin 1 or 2 to Pin 5)	−40V
V^+ Supply Voltage	Differential (Pin 8 or 9 to Pin 1 or 2)	30V
Input Current (Pin 3 or 7)		±75 mA
Peak Output Current		±1000 mA

Maximum Output Load – See Figure 2	
Power Dissipation – See Figure 1	1 5W
Storage Temperature	−65°C to +150°C
Operating Temperature MH0012	−55°C to +125°C
MH0012C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} \leq V^- + 2V$		1 0	2 0	V
Logic "0" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} \geq V^+ - 1\,5V$	0 4	0 6		V
Logic "1" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = 1mA$, $V_{IN} = 2\,0V$		V^- + 1 0	V^- + 2 0	V
Logic "0" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = -1mA$, $V_{IN} = 0\,4V$	$V^+ - 1\,5$	$V^+ - 0\,7$		V
I_{DC} (V^- Supply)	$V^+ - V^- = 20V$, $V_{IN} = 2\,0V$		34	60	mA

ac electrical characteristics

PARAMETER	CONDITIONS (Note 3)	MIN	TYP	MAX	UNITS
Turn-On Delay (t_{ON})	$V^+ - V^- = 20V$, $V_{CC} = 5\,0V$ $C_L = 200$ pF, f = 1 0 MHz $T_A = 25°C$		10	15	ns
Rise Time (t_r)			5	10	ns
Turn-Off Delay (t_{OFF})			35	50	ns
Fall Time (t_f)			35	45	ns

Note 1: Characteristics apply for circuit of Figure 1. Min and max limits apply from −55°C to +125°C for the MH0012 and from 0°C to +85°C for the MH0012C. Typical values are for T_A = +25°C.

Note 2: Due to the very fast rise and fall times, and the high currents involved, extremely short connections and good by passing techniques are required.

Note 3: All conditions apply for each parameter.

Power Dissipation

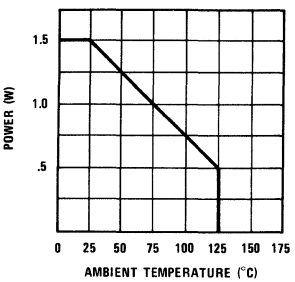


Figure 1.

Maximum Output Load vs Voltage Swing vs Rise Times

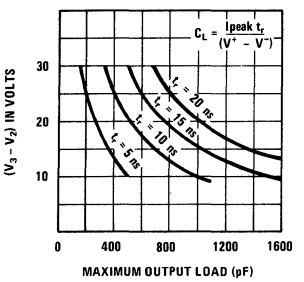
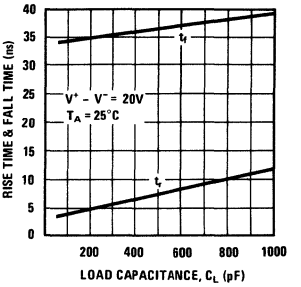


Figure 2.

Rise and Fall Times vs Load Capacitance



applications information

Power Dissipation Considerations

The power dissipated by the MH0012 may be divided into three areas of operation = ON, OFF and switching. The OFF power is approximately 30 mW and is dissipated by R_2 when Pin 3 is in the logic "1" state The OFF power is neglible and will be ignored in the subsequent discussion. The ON power is dissipated primarily by Q_3 and R_9 and is given by:

$$P_{ON} \cong [V^- I_{IN} + \frac{(V^+ - V^-)^2}{R_9}] \text{ DC} \quad (1)$$

Where

$$\text{DC} = \text{Duty Cycle} = \frac{\text{ON Time}}{\text{ON Time \& OFF Time}}$$

I_{IN} is given by $\frac{V_{IN} - V_{BE3}}{R_1}$ and equation (1) becomes

$$P_{ON} = \left[\frac{(V_{IN} - V_{BE3})|V^-|}{R_1} + \frac{(V^+ - V^-)^2}{R_9}\right] \text{DC} \quad (2)$$

For V_{IN} = 2 5V, V_{BE3} = 0 7V, V^+ = 0V, V^- = −20V, and DC = 20%, $P_{ON} \cong$ 200 mW

The transient power incurred during switching is given by:

$$P_{AC} = (V^+ - V^-)^2\, C_L f \quad (3)$$

For V^+ = 0V, V^- = −20V, C_L = 200 pF, and f = 5.0 MHz, P_{AC} = 400 mW.

The total power is given by

$$P_T = P_{AC} + P_{ON} \quad (4)$$

$$P_T \leq P_{MAX}$$

For the above example, P_T = 600 mW.

Memory/Clock Drivers

MH0013/MH0013C two phase MOS clock driver

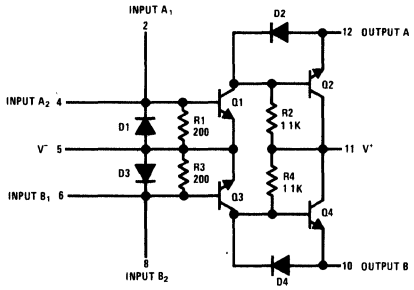
general description

The MH0013/MH0013C is a general purpose clock driver that is designed to be driven by DTL or TTL line drivers or buffers with high output current capability. It will provide fixed width clock pulses for both high threshold and low threshold MOS devices. Two external input coupling capacitors set the pulse width maximum, below which the output pulse width will closely follow the input pulse width or logic control of output pulse width may be obtained by using larger value input capacitors and no input resistors.

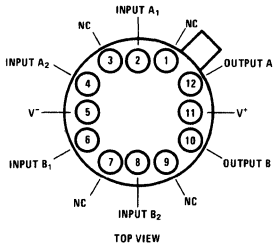
features

- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 500 mA
- High Repetition Rate—up to 5.0 MHz
- Pin Compatible with the MH0009/MH0009C
- "Zero" Quiescent Power

schematic and connection diagrams

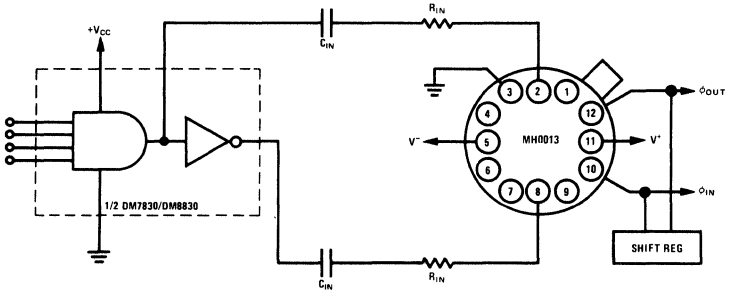


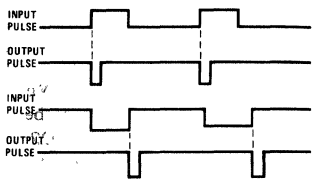
12-Lead TO-8 Package



Order Number MH0013G or MH0013CG
See Package 6

typical applications





absolute maximum ratings

$(V^+ - V^-)$ Voltage Differential	30V
Input Current (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±600 mA
Power Dissipation (Figure 7)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature MH0013	−55°C to +125°C
MH0013C	0°C to +85°C
Lead Temperature (Soldering, 10 sec 1/16" from Case)	300°C

electrical characteristics (Note 1 and Figure 8)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "0" Output Voltage	I_{OUT} = −50 mA I_{IN} = 1.0 mA	$V^+ - 3.0$	$V^+ - 1.0$		V
	I_{OUT} = −10 mA I_{IN} = 1.0 mA		$V^+ - 0.7$	$V^+ - 0.5$	V
Logical "1" Output Voltage	I_{OUT} = 50 mA I_{IN} = 10 mA		$V^- + 1.5$	$V^- + 2.0$	V
					V
Power Supply Leakage Current	$(V^+ - V^-)$ = 30V $I_{OUT} = I_{IN}$ = 0 mA		1.0	100	μA
Negative Input Voltage Clamp	I_{IN} = −10 mA	$V^- - 1.2$	$V^- - 0.8$		V
$t_{d\,ON}$			20	35	ns
t_{rise}			35	50	ns
$t_{d\,OFF}$ (Note 2)	C_{IN} = 0.0022 μF R_{IN} = 0Ω		30	60	ns
t_{fall} (Note 2)	C_L = 0.001 μF	40	50	80	ns
t_{fall} (Note 3)		40	70	120	ns
Pulse Width (50% to 50%) (Note 3)		340	420	490	ns
t_{rise}	C_{IN} = 500 pF		15		ns
t_{fall}	R_{IN} = 0Ω		20		ns
Pulse Width (50% to 50%) (Note 3)	C_L = 200 pF		110		ns
Positive Output Voltage Swing			$V^+ - 0.7V$		V
Negative Output Voltage Swing			$V^- + 0.7V$		V

Note 1: Min/Max limits apply over guaranteed operating temperature range of −55°C to +125°C for MH0013 and 0°C to +85°C for MH0013C, with V^- = −20V and V^+ = 0V unless otherwise specified. Typical values are for 25°C

Note 2: Parameter values apply for clock pulse width determined by input pulse width.

Note 3: Parameter values apply for input pulse width greater than output clock pulse width

TABLE I. Typical Drive Capability of One Half MH0013 at 70°C Ambient

$(V_2 - V_3)$ VOLTS	FREQUENCY MHz	PULSE WIDTH ns	TYPICAL R_{IN} Ω	TYPICAL C_{IN} pF	OUTPUT DRIVE CAPABILITY IN pF[1]	RISE TIME LIMIT ns[2]
28					50	–
20	4.0	100	0	750	200	7
16					350	10
28					100	5
20	2.0	200	10	1600	400	14
16					700	19
28					400	19
20	1.0	200	0	2300	1000	34
16					1700	45
28					2800	130
20	0.5	500	10	4000	5500	183
16					9300	248

Note 1: Output load is the maximum load that can be driven at 70°C without exceeding the package rating under the given conditions.

Note 2: The rise time given is the minimum that can be used without exceeding the peak transient output current for the full rated output load.

circuit operation

Input current forced into the base of Q1 through the coupling capacitor C_{IN} causes Q1 to be driven into saturation, swinging the output to $V^- + V_{CE}(SAT) + V_{DIODE}$.

When the input current has decayed, or has been switched, such that Q1 turns off, Q2 receives base drive through R2, turning Q2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q1 always switches off before Q2 begins to supply current; hence, high internal transient currents from V^+ to V^- cannot occur.

typical performance characteristics

FIGURE 1. Output Load vs Voltage Swing

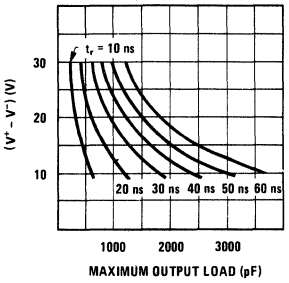


FIGURE 2. Transient Power vs Rep. Rate vs C_L

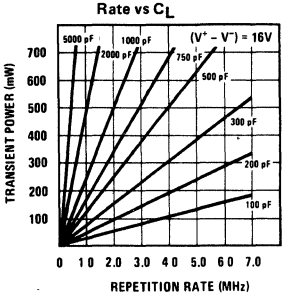


FIGURE 3. Transient Power vs Rep. Rate vs C_L

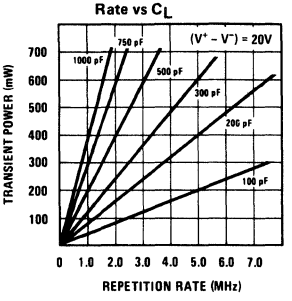


FIGURE 4. Average Internal Power vs Output Swing vs Duty Cycle

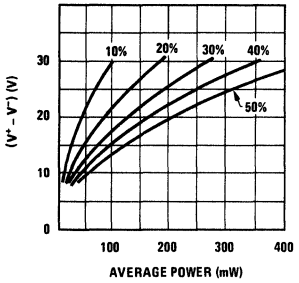


FIGURE 5. Typical Clock Pulse Variations vs Ambient Temperature

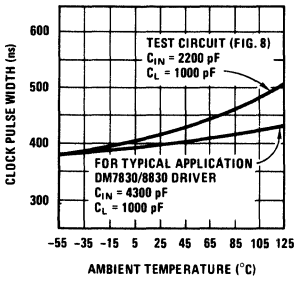


FIGURE 6. R_{IN} vs C_{IN} vs Pulse Width

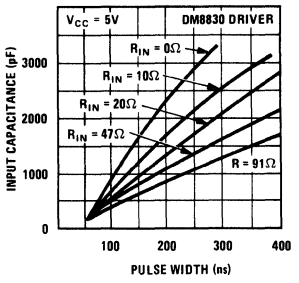
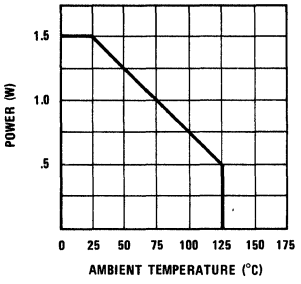
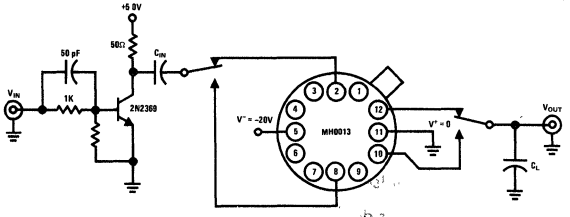


FIGURE 7. Package Power Derating



ac test circuit



V_{IN} = 0 to 5V pulse, f = 500 kHz, DC = 50%, t_r and $t_f \lesssim 10$ ns

timing diagram

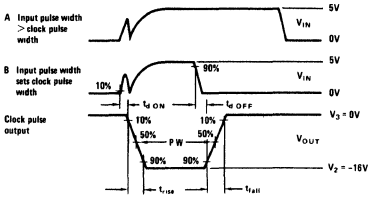


Figure 8

pulse width

Maximum output pulse width is a function of the input driver characteristics and the coupling capacitance and resistance. After being turned on, the input current must fall from its initial value I_{IN} peak to below the input threshold current I_{IN} min $\simeq V_{BE}/R1$ for the clock driver to turn off. For example, referring to the test circuit of Figure 8, the output pulse width, 50% to 50%, is given by

$$pw_{OUT} \cong \frac{1}{2}(t_{rise} + t_{fall}) + R_O C_{IN} \ln \frac{I_{IN}\ peak}{I_{IN}\ min} \cong 400\ ns.$$

For operation with the input pulse shorter than the above maximum pulse width, the output pulse width will be directly determined by the input pulse width.

$$pw_{OUT} = pw_{IN} + t_{d\,OFF} + t_{d\,ON} + \frac{1}{2}(t_{fall} + t_{rise})$$

Typical maximum pulse width for various C_{IN} and R_{IN} values are given in Figure 6.

fan-out calculation

The drive capability of the MH0013 is a function of system requirements, i.e., speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition. Some typical fan-outs for conditions are given in Table 1.

Transient Current

The maximum peak output current of the MH0013 is given as 600 mA. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{T_R} \qquad (1)$$

This can give a maximum limit to the load.

Figure 1 shows maximum voltage swing and capacitive load for various rise times

1. *Transient Output Power*

The average transient power (P_{AC}) dissipated is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (F)

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times F \qquad (2)$$

Figures 2 and 3 show transient power for two different values of $(V^+ - V^-)$ versus output load and frequency.

2. *Internal Power*

"0" State

Negligible (<3 mW)

"1" State

$$P_{INT} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle.} \qquad (3)$$

Figure 4 gives various values of internal power versus ouptut voltage and duty cycle.

3 *Input Power*

The average input power is a function of the input current and duty cycle. Due to input voltage clamping, this power contribution is small and can therefore be neglected. At maximum duty cycle of 50%, at 25°C, the average input power is less than 10 mW per phase for $R_{IN}C_{IN}$ controlled pulse widths For pulse widths much shorter than $R_{IN}C_{IN}$, and maximum duty cycle of 50%, input power could be as high as 30 mW, since I_{IN} peak is maintained for the full duration of the pulse width

4 *Package Power Dissipation*

Total Average Power = Transient Output Power + Internal Power + Input Power

Typical Example *Calculation for One Half MH0013C*

How many MM506 shift registers can be driven by an MH0013C driver at 1 MHz using a clock pulse width of 400 ns, rise time 30–50 ns and 16 volts amplitude over the temperature range 0–70°C?

Power Dissipation

From the graph of power dissipation versus temperature, Figure 7, it can be seen that an MH0013C at 70°C can dissipate 1W without a heat sink, therefore, each half can dissipate 500 mW.

Transient Peak Current Limitation

From Figure 1 (equation 1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 1140 pF.

Average Internal Power

Figure 4 (equation 3) gives an average power of 102 mW at 16V 40% duty cycle.

Input power will be a maximum of 8 mW

Transient Output Power

For one half of the MH0013C

500 mW = 102 mW + 8 mW + transient output power

390 mW = transient output power

Using Figure 2 (equation 2) at 16V, 1 MHz and 390 mW, each half of the MH0013C can drive a 1520 pF load. This is, however, in excess of the load derived from the transient current limitation (Figure 1, equation 1), and so a maximum load of 1140 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{1140}{80}$ or 14 registers.

For nonsymmetrical clock widths, drive capability is improved.

Memory/Clock Drivers

MH0025/MH0025C two phase MOS clock driver

general description

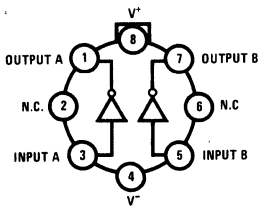
The MH0025/MH0025C is monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL/DTL line drivers or buffers such as the DM932, DM8830, or DM7440. Two input coupling capacitors are used to perform the level shift from TTL/DTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse widths may be set by selection of the input capacitors eliminating the need for tight input pulse control.

features

- 8-lead TO-5 or 8-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DM932, DM8830, DM7440(SN7440)
- "Zero" Quiescent Power

connection diagrams

Metal Can Package

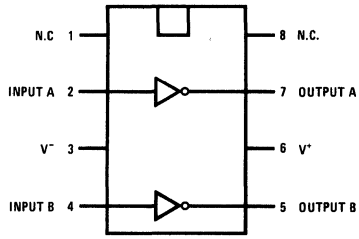


Note: Pin 4 connected to case.

TOP VIEW

Order Number MH0025H or MH0025CH
See Package 11

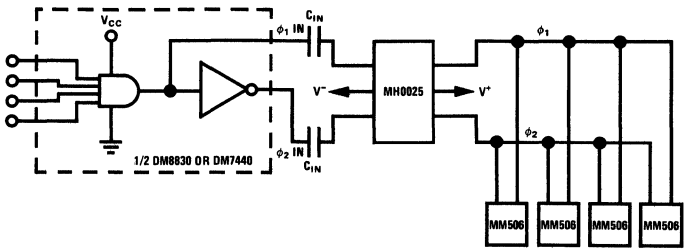
Dual-In-Line Package



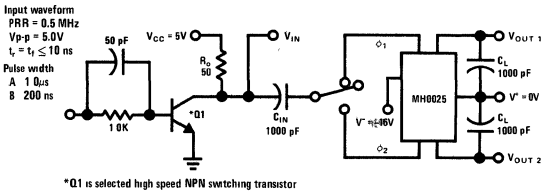
TOP VIEW

Order Number MH0025CN
See Package 20

typical application

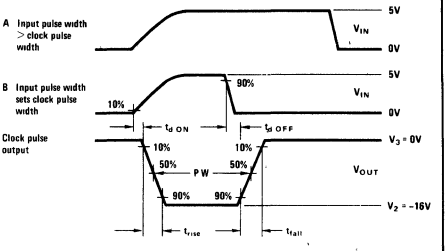


ac test circuit



*Q1 is selected high speed NPN switching transistor

timing diagram



absolute maximum ratings

$(V^+ - V^-)$ Voltage Differential	30V
Input Current	100 mA
Peak Output Current	1.5A
Power Dissipation	See Curves
Storage Temperature	−65°C to +150°C
Operating Temperature MH0025	−55°C to +125°C
MH0025C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1) See test circuit.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$T_{d_{ON}}$	C_{IN} = .001 μF, R_{IN} = 0Ω, C_L = .001 μF		15	30	ns
T_{rise}			25	50	ns
$T_{d_{OFF}}$ (Note 2)			30	60	ns
T_{fall} (Note 2)		60	90	120	ns
T_{fall} (Note 3)		100	150	250	ns
P.W. (50% to 50%) (Note 3)			500		ns
Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA	$V^+ - 1.0$	$V^+ - 0.7V$		V
Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA		$V^- + 0.7V$	$V^- + 1.5V$	V

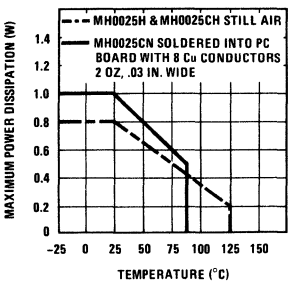
Note 1. Min/Max limits apply across the guaranteed operating temperature range of −55°C to +125°C for MH0025 and 0°C to 85°C for MH0025C. Typical values are for +25°C.

Note 2. Parameter values apply for clock pulse width determined by input pulse width.

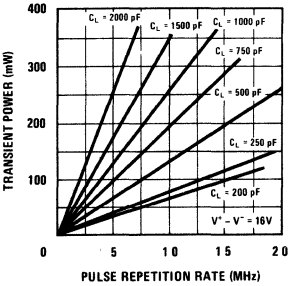
Note 3. Parameter values apply for input pulse width greater than output clock pulse width.

typical performance

Package Power Derating

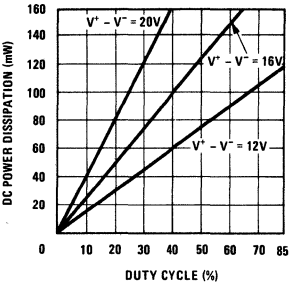


Transient Power vs Rep. Rate



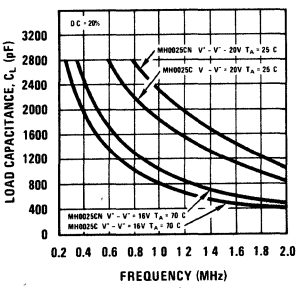
$P_{AC} = (V^+ - V^-)^2 f C_L$

DC Power (P_{DC}) vs Duty Cycle



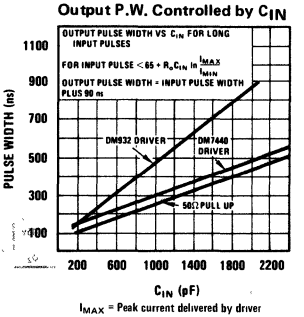
$P_{DC} = \frac{(V^+ - V^-)^2 (DC)}{1k}$

Maximum Load Capacitance



$$C_L \leq \frac{(P_{MAX})(1k) - (V^+ - V^-)^2 (DC)}{(f)(1k)(V^+ - V^-)^2} \leq \frac{(I_{pk})(t_r)}{V^+ - V^-}$$

Output P.W. Controlled by C_{IN}



I_{MAX} = Peak current delivered by driver

$I_{MIN} \cong \frac{V_{BE}}{R1} = \frac{0.6}{1k}$

applications information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents form V^- to V^+ cannot occur.

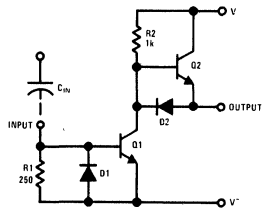


FIGURE 1. MH0025 Schematic (One-Half Circuit)

Fan-Out Calculation

The drive capability of the MH0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the MH0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns For $V^+ - V^- = 20V$, I = 0.8A.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, f = 1.0 MHz, C_L = 1000 pF, P_{AC} = 400 mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

= 80 mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power

example calculation

How many MM506 shift registers can be driven by an MH0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30-50 ns and 16V amplitude over the temperature range 0-70°C?

Power Dissipation:

At 70°C the MH0025CN can dissipate 630 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one half of the MH0025C, 630 mW ÷ 2 can be dissipated.

315 mW = 50 mW + transient output power

265 mW = transient output power

Using equation (2) at 16V, 1 MHz and 250 mW, each half of the MH0025CN can drive a 975 pF load. This is, less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 975 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{975}{80}$ or 12 registers.

Memory/Clock Drivers

MH0026/MH0026C 5 MHz two phase MOS clock driver

general description

The MH0026/MH0026C is a low cost monolithic high speed two phase MOS clock driver and interface circuit. Unique circuit design along with advanced processing provide both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 series gates and flip-flops or from drivers such as the DM8830 or DM7440. The MH0026 is intended for applications in which the output pulse width is logically controlled: i.e., the output pulse width is equal to the input pulse width.

features

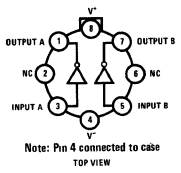
- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on load
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

The MH0026 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16 bit MM1103 RAM memory system. Information on the correct usage of the MH0026 in these as well as other systems is included in the application section starting on page 5. A thorough understanding of its usage will insure optimum performance of the device.

The device is available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt TO-8 packages.

connection diagrams

Metal Can Package

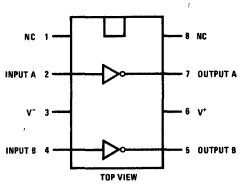


Note: Pin 4 connected to case

TOP VIEW

Order Number MH0026H or MH0026CH See Package 11

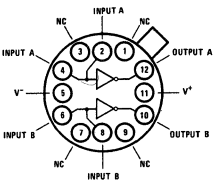
Dual-In-Line Package



TOP VIEW

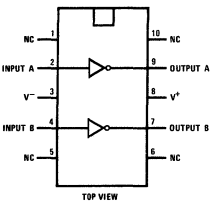
Order Number MH0026CN See Package 20

Metal Can Package



Order Number MH0026G or MH0026CG See Package 6

Flat Package

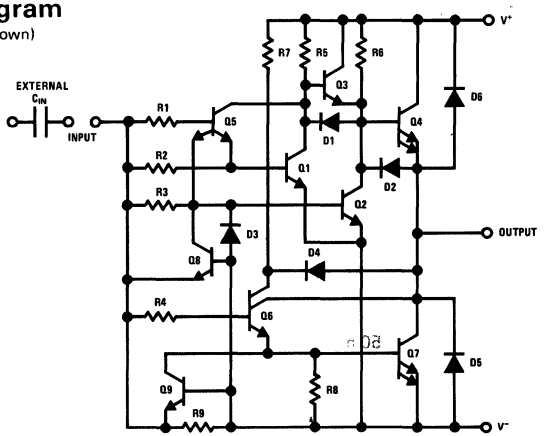


TOP VIEW

Order Number MH0026F or MH0026CF See Package 3

schematic diagram

(1/2 of Circuit Shown)



absolute maximum ratings

$V^+ - V^-$ Differential Voltage		22V
Input Current		100 mA
Input Voltage ($V_{IN} - V^-$)		5.5V
Peak Output Current		1.5A
Power Dissipation		See curves
Operating Temperature Range	MH0026	−55°C to +125°C
	MH0026C	0°C to 85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics (Notes 1 & 2)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Logic "1" Input Voltage	$V_{OUT} = V^- + 1.0V$	2.5	1.5		V
Logic "1" Input Current	$V_{IN} - V^- = 2.5V$, $V_{OUT} = V^- + 1.0V$		10	15	mA
Logic "0" Input Voltage	$V_{OUT} = V^+ - 1.0V$		0.6	0.4	V
Logic "0" Input Current	$V_{IN} - V^- = 0V$, $V_{OUT} = V^+ - 1.0V$		−0.005	−10	μA
Logic "0" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$ $V_{IN} = -11.6$	4.0	4.3		V
Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$	$V^+ - 1.0$	$V^+ - 0.7$		V
Logic "1" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$ $V_{IN} = -9.5V$		−11.5	−11.0	V
Logic "1" Output Voltage	$V_{IN} - V^- = 2.5V$		$V^- + 0.5$	$V^- + 1.0$	V
"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.5V$		30	40	mA
"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0.0V$		10	100	μA

ac electrical characteristics (Notes 1 & 2, AC test circuit, $T_A = 25°C$)

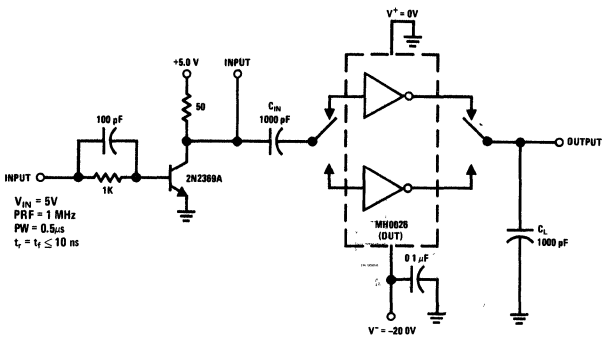
Turn-On Delay (t_{ON})		5.0	7.5	12	ns
Turn-Off Delay (t_{OFF})		5.0	12	15	ns
Rise time (t_r) — Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		12		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		15	18	ns
	$C_L = 1000$ pF		20	35	ns
Falltime (t_f) — Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		10		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		12	16	ns
	$C_L = 1000$ pF		17	25	ns

Note 1: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range −55°C to +125°C for the MH0026 and 0°C to +85°C for the MH0026C, unless otherwise specified.

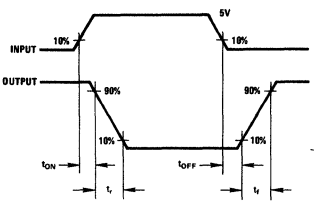
Note 2: All typical values for the $T_A = 25°C$.

Note 3: Rise and fall time are given for MOS logic levels; i.e., rise time is transistion from logic "0" to logic "1" which is voltage fall. See waveforms on the following pages.

ac test circuit

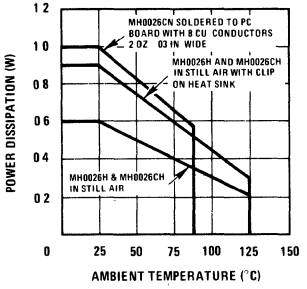


switching time waveforms

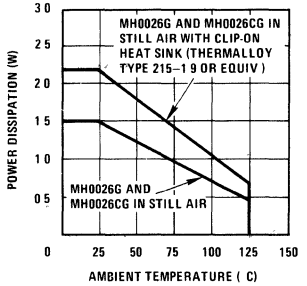


typical performance characteristics

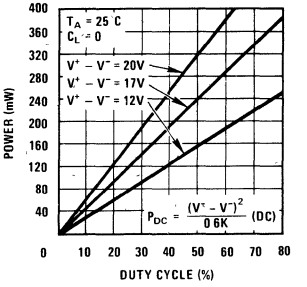
TO-5 & DIP Power Ratings



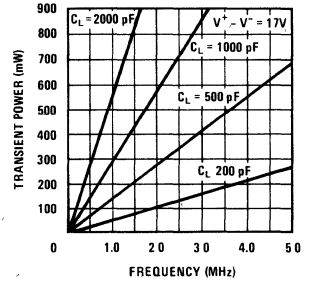
TO-8 Package Power Rating



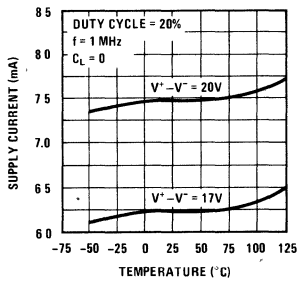
DC Power (P_{DC}) vs Duty Cycle



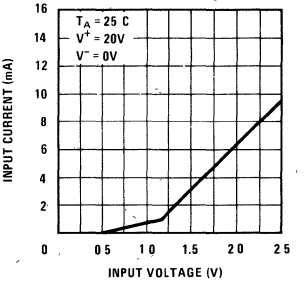
Transient Power (P_{AC}) vs Frequency



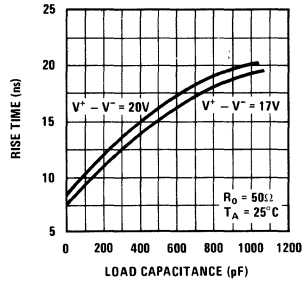
Supply Current vs Temperature



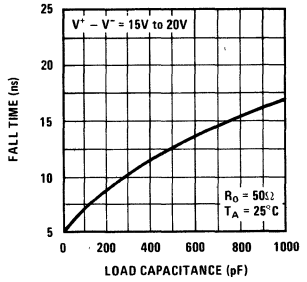
Input Current vs Input Voltage



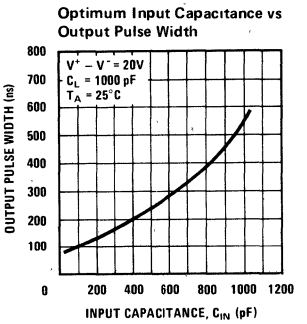
Rise Time vs Load Capacitance



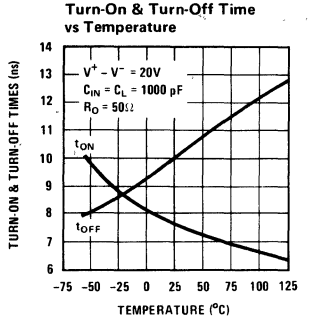
Fall Time vs Load Capacitance



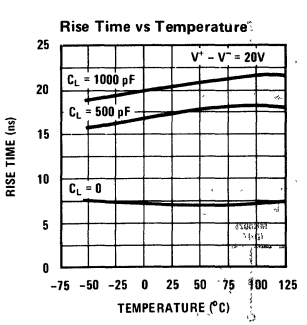
Optimum Input Capacitance vs Output Pulse Width



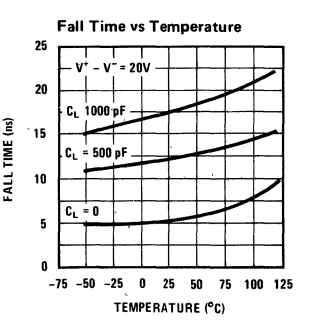
Turn-On & Turn-Off Time vs Temperature



Rise Time vs Temperature



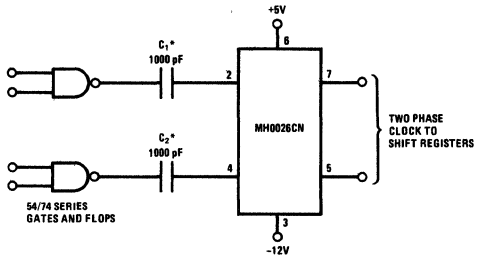
Fall Time vs Temperature



3

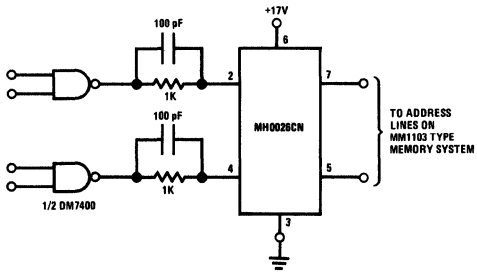
typical applications (cont.)

AC Coupled MOS Clock Driver

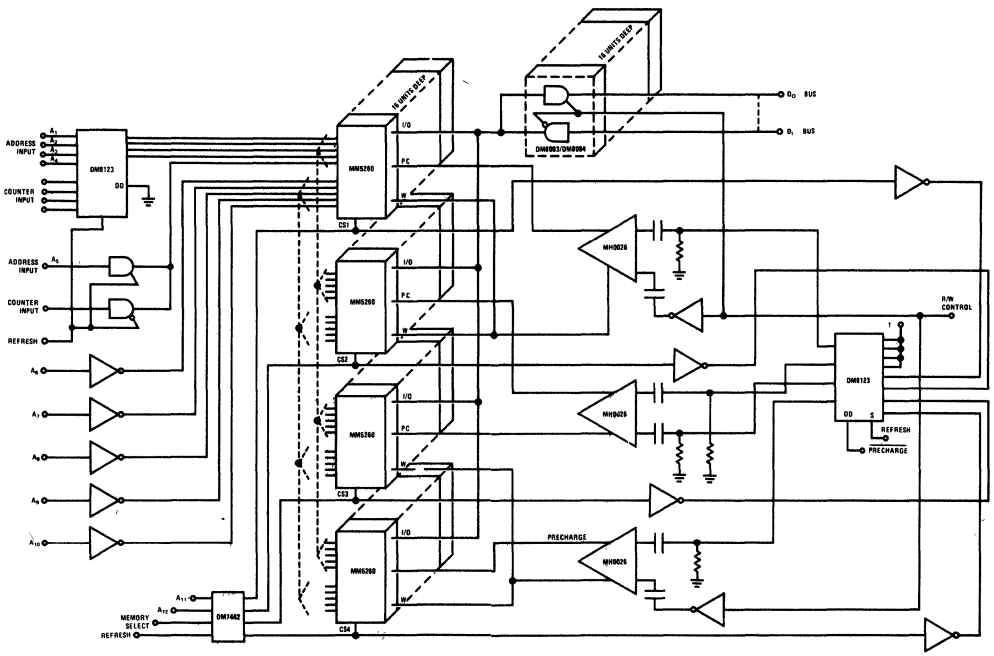


*See applications section for detailed information on input/output design criterion.

DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

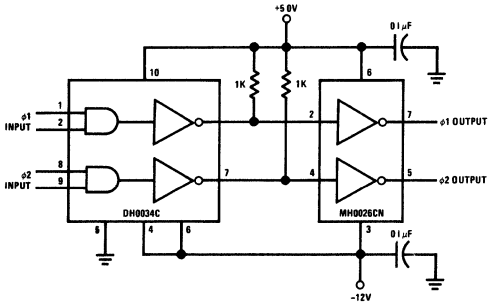


Precharge Driver for MOS RAM Memories

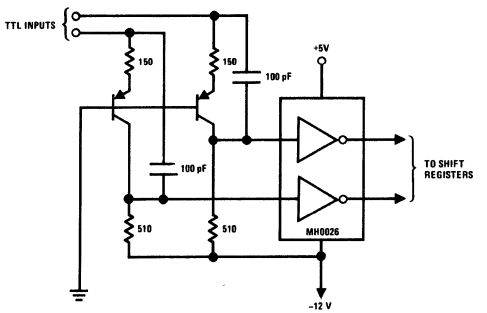


typical applications

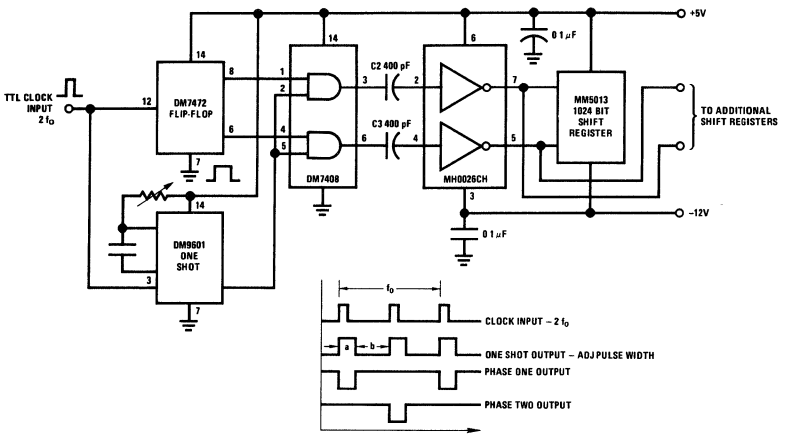
DC Coupled MOS Clock Driver



Transistor Coupled MOS Clock Driver



Logically Controlled AC Coupled Clock Driver



application information

1.0 Introduction

The MH0026 is capable of delivering 30 watts peak power (1.5 amps at 20V needed to rapidly charge large capacitative loads) while its package is limited to the watt range. This section describes the operation of the circuit and how to obtain optimum system performance. If additional design information is required, please contact your local National field application engineer.

2.0 Theory of Operation

Conventional MOS clock drivers like the MH0013 and similar devices have relied on the circuit configuration in Figure 1. The AC coupling of an input pulse allows the device to work over a wide range of supplies while the output pulse width may be controlled by the time constant $-R_1 \times C_1$.

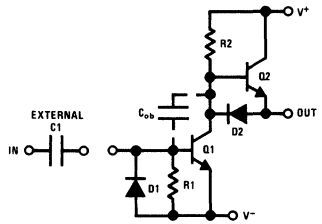


FIGURE 1. Conventional MOS Clock Drive

D_2 provides 0.7V of dead-zone thus preventing Q_1 and Q_2 from conducting at the same time. In order to drive large capacitive loads, Q_1 and Q_2 are large geometry devices but C_{ob} now limits useful output rise time. A high voltage TTL output stage (Figure 2) could be used; however, during switching until the stored charge is removed from Q_1, both output devices conduct at the same time. This is familiar in TTL with supply line glitches in the order of 60 to 100 mA. A clock driver built this way would introduce 1.5 amp spikes into the supply lines.

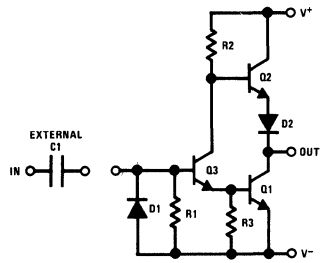


FIGURE 2. Alternate MOS Clock Drive

Unique circuit design and advanced semiconductor processing overcome these clasic problems allowing the high volume manufacture of a device, the MH0026, that delivers 1.5A peak output currents with 20ns rise and fall times into 1000pF loads. In a simplified diagram, D_1 (Figure 3) provides 0.7V dead zone so that Q_3 is turned ON for a rising input pulse and Q_2 OFF prior to Q_1 turning ON a few nanoseconds later. D_2 prevents zenering of the emitter-base junction of Q_2 and provides an initial discharge path for the load via Q_3. During a falling input, the stored charge in Q_3 is used beneficially to keep Q_3 ON thus preventing Q_2 from conducting until Q_1 is OFF. Q_1 stored charge is quickly discharged by means of common-base transistor Q_4.

The complete circuit of the MH0026 (see schematic on page 1) basically makes Darlingtons out of each of the transistors in Figure 3.

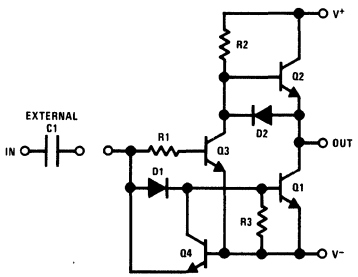


FIGURE 3. Simplified MH0026

When the output of the TTL input element (not shown) goes to the logic "1" state, current is supplied through C_{IN} to the base of Q_1 and Q_2 turning them ON, and Q_3 and Q_4 OFF when the input voltages reaches 0.7V. Initial discharge of the load as well as E-B protection for Q_3 and Q_4 are provided by D_1 and D_2. When the input voltage reaches about 1.5V, Q_6 and Q_7 begin to conduct and the load is rapidly discharged by Q_7. As the input goes low, the input side of C_{IN} goes negative with respect to V^- causing Q_8 and Q_9 to conduct momentarily to assure rapid turn-off of Q_2 and Q_7 respectively. When Q_1 and Q_2 turn OFF, Darlington connected Q_3 and Q_4 rapidly charge the load toward V^+ volts. R_6 assures that the output will reach to within one V_{BE} of the V^+ supply.

The real secret of the device's performance is proper selection of transistor geometries and resistor values so that Q_4 and Q_7 do not conduct at the same time while minimizing delay from input to output.

3.0 Power Dissipation Considerations

There are four considerations in determining power dissipations.

1. Average DC power
2. Average AC power
3. Package and heat sink selection
4. Remember—2 drivers per package

application information (cont.)

The total average power dissipated by the MH0026 is the sum of the DC power and AC transient power. The total must be less than given package power ratings.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Since the device dissipates only 2mW with output voltage high (MOS logic "0"), the dominating factor in average DC power is duty cycle or the percent of time in output voltage low state (MOS logic "1"). Percent of total power contributed by P_{DC} is usually neglible in shift register applications where duty cycle is less than 25%. P_{DC} dominates in RAM address line driver applications where duty cycle can exceed 50%.

3.1 DC Power (per driver)

DC Power is given by:

$$P_{DC} = (V^+ - V^-) \times (I_{S(Low)}) \times \left(\frac{\text{ON time}}{\text{OFF time–ON time}}\right)$$

or P_{DC} = (Output Low Power) X (Duty Cycle)

where: $I_{S(LOW)} = I_S$ @ $(V^+ - V^-)$

Example 1: (V^+ = +5V, V^- = −12V)

a) Duty cycle = 25%, therefore

P_{DC} = 17V X 40mA X 17/20 X 25%

P_{DC} = 145mW worst-case, each side

P_{DC} = 109mW typically

b) Duty cycle = 5%

P_{DC} = 21mW

c) See graph on page 3

The above illustrates that for shift register applications, the minimum clock width allowable for the given type of shift register should be used in order to drive the largest number of registers per clock driver.

Example 2: (V^+ = +17V, V^- = GND):

a) Duty cycle = 50%

P_{DC} = 290mW worst-case

P_{DC} = 218mW typically

b) Duty cycle = 100%

P_{DC} = 580mW

Thus for RAM address line applications, package type and heat sink technique will limit drive capability rather than AC power.

3.2 AC Transient Power (per driver)

AC Transient power is given by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L$$

where: f = frequency of operation

C_L = Load capacitance (including all strays and wiring)

Example 3: (V^+ = +5V, V^- = −12V)

$$P_{AC} = 17 \times 17 \times f(MHz) \times 10^6 \times C_L(nF) \times 10^{-9}$$

P_{AC} = 290mW per MHz per 1000pF

Thus at 5MHz, a 1000pF load will cause any driver to dissipate one and one half watts. For long shift registers, a driver with the highest package power rating will drive the largest number of bits for the lowest cost per bit.

3.3 Package Selection

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs on page 3 illustrate derating for various operating temperatures.

3.31 TO-5 ("H") Package: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 900mW with clip on heat sink (derate at 6.0mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving capability by 50%.

3.32 8-Pin ("N") Molded Mini-DIP: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 1.0 watt soldered to PC board (derate at 6.6mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600mW when mounted in a socket and not one watt until it is soldered down.)

3.33 TO-8 ("G") Package: Rated at 1.5 watts still air (derate at 10mW/°C above 25°C) and 2.3 watts with clip on heat sink (Wakefield type 215-1.9 or equivalent–derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

application information (cont.)

3.4 Summary—Package Power Considerations

The maximum capacitative load that the MH0026 can drive is thus determined by package type, heat sink technique, ambient temperature, AC power (which is proportional to frequency and capacitive load) and DC power (which is principally determined by duty cycle). Combining equations previously given, the following formula is valid for any clock driver with negligible input power and negligible power in output high state:

$$C_L \text{ (max in pF)} = \frac{10^{-3}}{n} \times \frac{P_{max(mW)}(T_A, pkg) \times R_{eq} - (V^+ - V^-)^2 \times (Dc) \times 10^3}{(V^+ - V^-)^2 \times R_{eq} \times f(MHz)}$$

or:

$$C_L \text{ (max in pF)} = .5 \times 10^{-3} \times \frac{P_{max}(mW) \times 500 - V_S^2 \times Dc \times 10^3}{V_S^2 \times 500 \times f(MHz)}$$

Where: n = number of drivers per pkg. (2 for the MH0026)

$P_{max(mW)}(T_A,$ pkg) = Package power rating in milliwatts for given package, heat sink, and max, ambient temperature (See graphs)

R_{eq} = equivalent internal resistance

$R_{eq} = (V^+ - V^-)/I_{S(Low)}$ = 500 ohms (worst case over temperature for the MH0026 or 660 ohms typically)

$V_S = (V^+ - V^-)$ = total supply voltage across device

Dc = Duty Cycle =

$$\frac{\text{Time in output low state}}{\text{Time in output low} + \text{Time in output high state}}$$

Table I illustrates MH0026 drive capability under various system conditions.

4.0 Pulse Width Control

The MH0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + \frac{t_r + t_f}{2} = PW_{IN} + 25ns$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the MH0026 discharges to just above the devices threshold (about 1.5V). If the input is allowed to discharge below the threshold, t_{OFF} and t_f will be degraded. The graph on page 3 shows optimum values for C_{IN} vs desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN} = (2 \times 10^{-3})\,(PW)_{OUT}$$

For an output pulse width of 500ns, the optimum value for C_{IN} is:

$$C_{IN} = (2 \times 10^{-3})(500 \times 10^{-9}) \cong 1000pF$$

TABLE 1. Worst Case Maximum Drive Capability for MH0026*

PACKAGE TYPE		TO-8 WITH HEAT SINK		TO-8 FREE AIR		MINI-DIP SOLDERED DOWN		TO-5 AND MINI-DIP FREE AIR	
Max. Operating Frequency	Max. Ambient Temp. ↓ / → Duty Cycle	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C
100kHz	5%	30 k	24 k	19 k	15 k	13 k	10k	7.5k	5.8k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2.7k	2k	1.5k	1.1k
1MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	430
2MHz	25%	1.4k	1.1k	850	650	550	400	280	190
5MHz	25%	620	470	380	290	240	170	120	80
10MHz	25%	280	220	170	130	110	79	–	–

*Note: Values in pF and assume both sides in use as non-overlaping 2 phase driver, each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$. For loads greater than 1200 pF, rise and fall times will be limited by output current, see Section 5.0

application information (cont.)

5.0 Rise & Fall Time Considerations(Note 3)

The MH0026's peak output current is limited to 1.5A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leqslant 1.5A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V)(250 \times 10^{-12} + C_L)$$

Where: ΔV = The change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

For $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20V)(250 \times 10^{-12} + 10^{-12})$$
$$= 25ns$$

For small values of C_L, equation above predicts optimistic values for t_r. The graph on page 3 shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2R\left(C_S + \frac{C_L}{h_{FE} + 1}\right)$$

6.0 Clock Overshoot

The output waveform of the MH0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the ouput of the MH0026. The critical valve for $R_s = 2\sqrt{L/C\ell}$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_s is readily determined emperically, and values typically range between 10 and 51 ohms. R_s does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2R_S C_L$$

7.0 Clock Line Cross Talk

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the MH0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output has to drop at least 2 V_{BE} before Q_3 and Q_4 come on and pull the output back to V^+. A simple method for eliminating or minimizing this effect is to add bleed resistors between the MH0026 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2k and 10k ohms.

8.0 Power Supply Decoupling

Power supply decoupling is a widespread and accepted practice. Decoupling of V^+ to V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each MH0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.

Memory/Clock Drivers

MH7803/MH8803 two phase oscillator/clock driver

general description

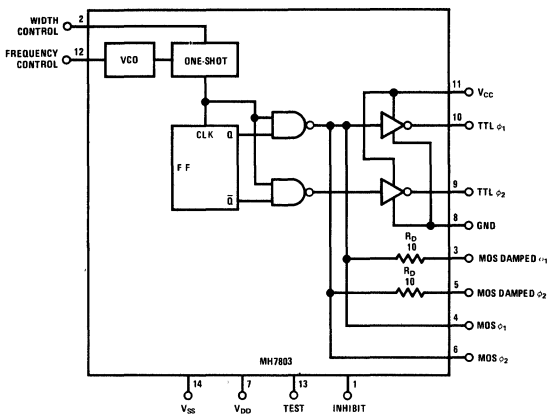
The MH7803 is a self contained two phase oscillator/clock driver. It requires no external components to generate one of three primary oscillator frequencies and pulse widths. Other frequencies can easily be obtained by programming input voltages. Three sets of outputs are provided: damped and un-damped MOS outputs and TTL monitor outputs. The MOS outputs easily drive 500 pF loads with less than 150 ns rise and fall times. In addition the outputs have current limiting to protect against momentary shorts to the supplies.

The MH7803 and MH8803 are available in a 14 lead cavity DIP. The MH8803 is also available in a 14 pin molded DIP.

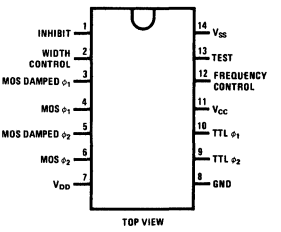
features

- Two phase non-overlapping outputs
- No external timing components required
- Frequency adjustable from 100 kHz to 500 kHz
- Pulse width adjustable from 260 ns to 1.4μs
- Damped and un-damped MOS outputs
- TTL monitor outputs

block and connection diagrams



Dual-In-Line Package



Order Number MH7803J or MH8803J
See Package 16
Order Number MH8803N
See Package 22

absolute maximum ratings

$V_{SS} - V_{DD}$	22V	Operating Temperature Range	
$V_{CC} - GND$	7.0V	MH7803	−55°C to +125°C
Pulse Width Adjust Voltage	V_{SS} + 0.5V	MH8803	0°C to +70°C
Frequency Adjust Voltage	V_{SS} + 0.5V	Storage Temperature Range	−65°C to +150°C
$V_{SS} - V_{DD}$ Minimum	14V	Lead Temperature (Soldering, 10 seconds)	300°C
Test and Inhibit Input Voltages	V_{SS}		

electrical characteristics (Note 1)

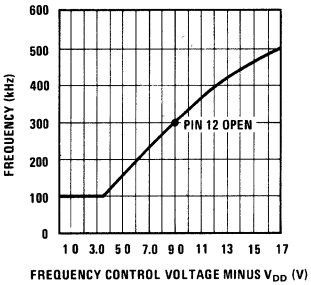
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	Pin 12 at 17V, T_A = 25°C	300	500	600	kHz
	Pin 12 Open, T_A = 25°C	175	300	350	kHz
	Pin 12 at 0V, T_A = 25°C	60	100	150	kHz
Frequency Change from 25°C					
MH7803	Pin 12 at 17V		±20	±30	%
MH8803	Pin 12 at 17V		±10	±15	%
Pulse Width (Note 2)	Pin 2 at 17V, T_A = 25°C	0 2	0.26	0.4	μs
	Pin 2 Open, T_A = 25°C	0.5	0.75	1.3	μs
	Pin 2 at 0V, T_A = 25°C	1.0	1.4	2.6	μs
Pulse Width Change from 25°C					
MH7803	Pin 2 at 17V		±20	±30	%
MH8803	Pin 2 at 17V		±10	±15	%
MOS V_{OH}	I_{OH} = −100μA	V_{SS}−1 1	V_{SS}−0.8		V
MOS V_{OL}	I_{OL} = 2.0 mA		V_{DD}+0.15	V_{DD}+0.5	V
TTL V_{OH}	I_{OH} = −200μA	2.4	3 7		V
TTL V_{OL}					
MH7803	I_{OL} = 2.0 mA		0.17	0.3	V
MH8803	I_{OL} = 3 2 mA		0 2	0.4	V
TTL I_{OS}		3.0	8.0	15	mA
MOS Output Current Limit			70		mA
I_{SS}	Pins 2, 12, 13 at 0V, and Pin 1 at −0.3V		10	17	mA
I_{CC}	Pins 2, 12, at 0V, and Pin 1 at −0.3V		0.75	1.1	mA
R_D					
MH7803		7.0	10	13	Ω
MH8803		5.0	10	15	Ω
MOS t_R, t_f	C_L = 500 pF, T_A = 25°C		100	150	ns
	C_L = 50 pF, T_A = 25°C		20	30	ns

Note 1: These specifications apply for the MH7803 at $V_{SS} - V_{DD}$ = 17V ±10% and over −55°C to +125°C; for the MH8803 at $V_{SS} - V_{DD}$ = 17V ±5% and over 0°C to +70°C unless otherwise specified.

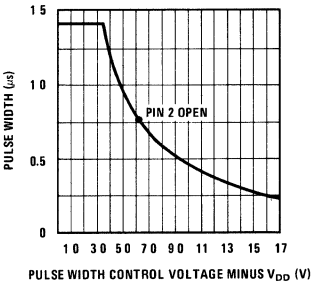
Note 2: The duty cycle can not physically exceed 50% at any output. At high frequencies the frequency adjust pin will affect the pulse width by limiting the duty cycle to slightly less than 50%. Under this condition the pulse width spec does not apply.

typical performance characteristics

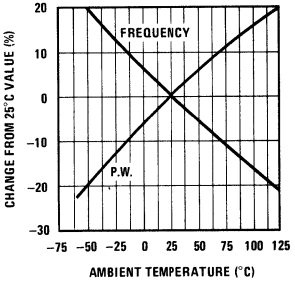
Frequency Control Voltage



Pulse Width Control Voltage

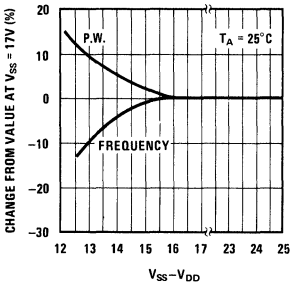


Frequency and Pulse Width vs Temperature

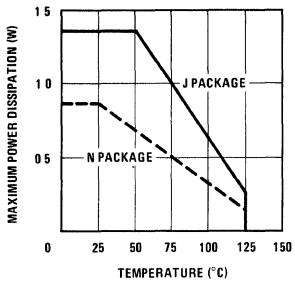


typical performance characteristics (con't)

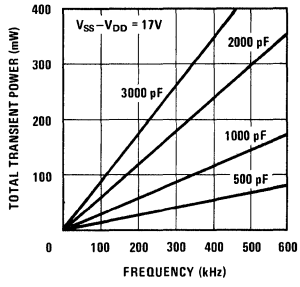
Frequency and Pulse Width vs $V_{SS}-V_{DD}$



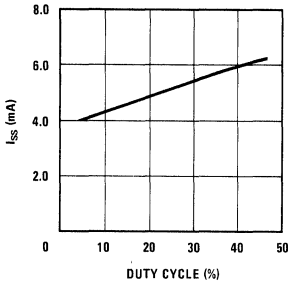
Maximum Package Dissipation



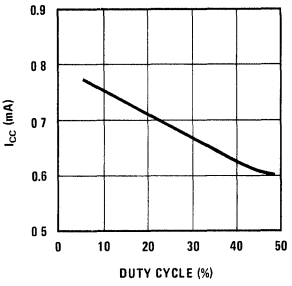
Total Transient Power vs Frequency vs Total C_L



I_{SS} vs Duty Cycle



I_{CC} vs Duty Cycle



applications information

TTL MONITOR OUTPUTS

The TTL outputs are extra functions provided for monitor or synchronization applications. In some systems these outputs may not be required. For these cases the V_{CC} pin may be left open and the TTL circuitry power consumption will be virtually zero.

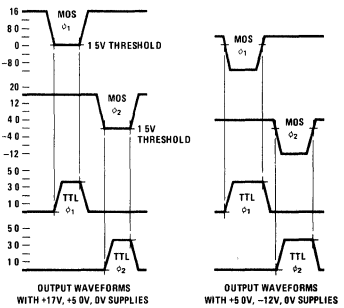
The TTL outputs are slaved to the MOS outputs. Thus the TTL outputs start to switch when the MOS outputs cross the TTL threshold voltage (about 1.5V above ground). Figure 1 depicts the effect of different supply voltages on the TTL waveform when the MOS outputs are driving capacitive loads.

DAMPED MOS OUTPUTS

An extra set of MOS outputs provides a 10 ohm resistor in series with each output line. These resistors give the output pulses an R-C rolloff which tends to minimize ringing or peaking problems associated with board layout.

INHIBIT AND TEST INPUTS

The INHIBIT and TEST inputs are designed to facilitate testing of the device. They were not included in the IC for system use.



(A) (B)

FIGURE 1.

Typically they perform as follows:

INHIBIT Input: in the low state prevents pulses from being initiated on either phase output.

High Level Input:

$$V_{IH} \geq V_{DD} + 2.0V$$

Low Level Input:

$$V_{DD} + 0.2V \geq V_{IL} \geq V_{DD} - 0.5V$$

applications information (con't)

TEST Input: in the low state forces a ONE state on all outputs. The test input should only be used with the INHIBIT input also in the low state.

High Level:

$$V_{IH} \geq V_{DD} + 8.0V$$

Low Level:

$$V_{DD} + 0.5V \geq V_{IL} \geq V_{DD}$$

A pull-up resistor is connected from the TEST pin to V_{SS} internally.

POWER CONSIDERATIONS

Internal power dissipation is affected by three factors:

- dc power
- ac power
- package dissipation capability

The total average power dissipation is the summation of the dc power and ac power. This sum must be less than the maximum package dissipation capability at the particular operating temperature to insure safe operation, i.e.:

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Where

$$P_{AC} = P_{AC\,TTL} + P_{AC\,MOS}$$

$$P_{AC} = [(V_{CC} - GND)^2 \times f \times C_L]_{TTL} + [(V_{SS} - V_{DD})^2 \times f \times C_L]_{MOS}$$

And

$$P_{DC} = (I_{CC}) \times (V_{CC} - GND) + (I_{SS}) \times (V_{SS} - V_{DD})$$

for I_{CC} and I_{SS} selected at the appropriate duty cycle.

For practical cases the $P_{AC\,TTL}$ can be neglected as being very small compared to $P_{AC\,MOS}$.

Thus P_{DISS} is the sum of the MOS transient power (total for both sides of the MH7803) and the standby power of the TTL and MOS sections of the MH7803.

DECOUPLING

It is recommended that each device be decoupled with a 0.1μF capacitor from V_{SS} to V_{DD}. If there is noise on the supply lines, better frequency and pulse width stability can be obtained by connecting a 0.001μF capacitor from the frequency control pin to V_{DD} and another 0.001μF capacitor from the pulse width control pin to V_{DD}.

Memory/Clock Drivers

MH8808 dual high speed MOS clock driver

general description

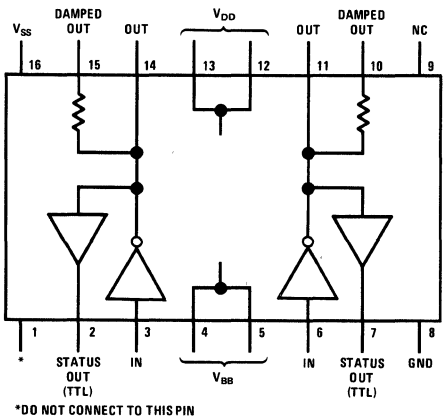
The MH8808 is a high speed dual MOS clock driver intended to drive the two phases of a memory array of 500 pF per phase at rates up to 4 MHz. The design includes output current limiting for controlled rise and fall times, and thermal shutdown which protects the chip against excessive power dissipation or accidental output shorts. Two DTL/TTL compatible status outputs monitor clock outputs and provide a corresponding TTL logic level for status indication. Both direct and internally damped outputs are available for each phase to suit the particular application. It is ideally suited for driving MM5262 2k RAMs.

features

- High Speed: 18 ns typ delay and 20 ns typ rise and fall times with 500 pF load
- Current limited outputs ±450 mA typ
- Direct and damped outputs available
- Thermal shutdown protection
- TTL compatible status outputs
- 1W dissipation capability at 25°C T_A
- 16 pin cavity dual-in-line package
- Output high level clamped to +5V

connection diagram

Dual-In-Line Package



*DO NOT CONNECT TO THIS PIN

TOP VIEW

Order Number MH8808J
See Package 17

Order Number MH8808N
See Package 23

absolute maximum ratings

V_{SS}	+7V
$V_{BB} - V_{DD}$	26V
Total Power Dissipation (Note 1)	1W
Operating Temperature Range	0°C to +70°C

electrical characteristics

The following apply for V_{BB} = +7V, V_{SS} = +5V, V_{DD} = −15V, T_A = 25°C unless otherwise stated

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Input Current	V_{IN} = −9V (Note 2)		10	mA
Output Low Voltage	I_{OUT} = +1 mA, V_{IN} = −10V (Note 2)	−14		V
Output High Voltage	I_{OUT} = −1 mA, V_{IN} = −14V	4 5	5 3	V
Status "1" Voltage	I_{OUT} = −250 μA, V_{IN} = −14V	3		V
Status "0" Voltage	I_{OUT} = 20 mA, V_{IN} = −10V (Note 2)		0 5	V
Output Leakage Current	V_{BB} = +8 5V, V_{SS} = 5V V_{DD} = −17 5V, V_{OUT} = +8 5V V_{IN} = open		100	μA
Damping Resistor		4		Ω
I_{BB}	V_{IN} = −11 5V V_{SS} = +6 5V, V_{DD} = −17 5V V_{BB} = +8 5V (Note 2)		32	mA
I_{SS}	V_{IN} = −11 5V V_{SS} = +6 5V, V_{DD} = −17 5V V_{BB} = +8 5V (Note 2)		23	mA
I_{DD}	V_{IN} = −11 5V V_{SS} = +6 5V, V_{DD} = −17 5V V_{BB} = +8 5V (Note 2)		−55	mA
Output Rise Time	C_L = 500 pF		26	ns
Output Fall Time	C_L = 500 pF		26	ns
Delay to Negative-Going Output	C_L = 500 pF	7	22	ns
Delay to Positive-Going Output	C_L = 500 pF	10	25	ns

Note 1: Maximum junction temperature is +125°C. For operation above +25°C derate at +80°C/W θ_{JA} for still air.
Note 2: Test only one input high (more positive) at a time.

Line Drivers/Receivers

DM7820/DM8820 dual line receiver

general description

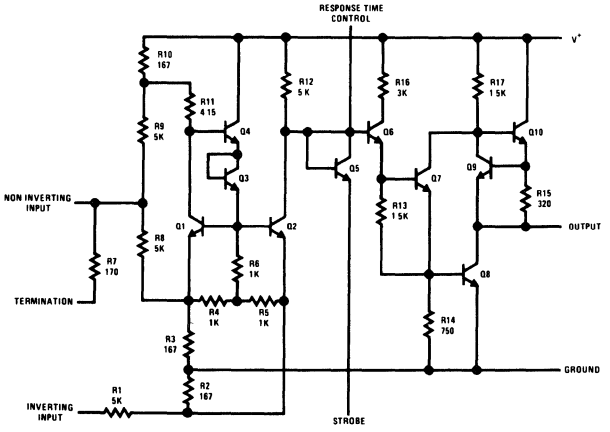
The DM7820, specified from -55°C to 125°C, and the DM8820, specified from 0°C to 70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

features

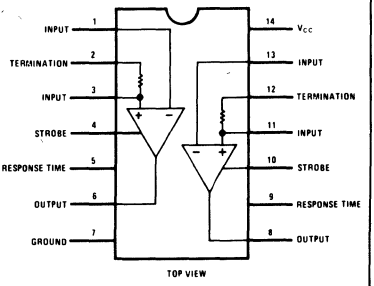
- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Each channel can be strobed independently
- High input resistance
- Fanout of two with either DTL or TTL integrated circuits

The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DM7820 and the DM8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

schematic and connection diagrams

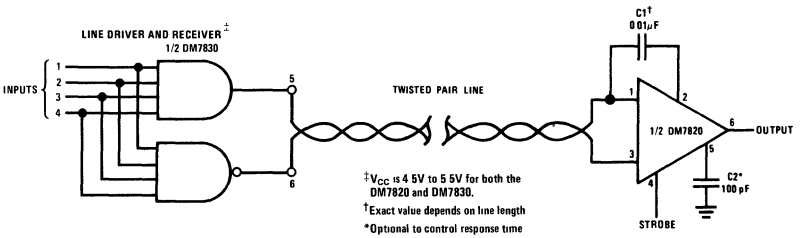


Dual-In-Line and Flat Package



Order Number DM7820J or DM8820J
See Package 16
Order Number DM8820N
See Package 22
Order Number DM7820W or DM8820W
See Package 27

typical application



absolute maximum ratings

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25 mA
Power Dissipation (Note 1)	600 mW
Operating Temperature Range	
DM7820	−55°C to +125°C
DM8820	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 2 & 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Threshold Voltage	$V_{IN} = 0$	−0.5	0	0.5	V
	$-15V \leq V_{IN} \leq 15V$	−1.0	0	1.0	V
High Output Level	$I_{OUT} \leq 0.2$ mA	2.5		5.5	V
Low Output Level	$I_{sink} \leq 3.5$ mA	0		0.4	V
Inverting Input Resistance		3.6	5.0		kΩ
Non-inverting Input Resistance		1.8	2.5		kΩ
Line Termination Resistance	$T_A = 25°C$	120	170	250	Ω
Response Time	$C_{delay} = 0$		40		ns
	$C_{delay} = 100$ pF		150		ns
Strobe Current	$V_{strobe} = 0.4V$		1.0	1.4	mA
	$V_{strobe} = 5.5V$			−5.0	μA
Power Supply Current	$V_{IN} = 15V$		3.2	6.0	mA
	$V_{IN} = 0$		5.8	10.2	mA
	$V_{IN} = -15V$		8.3	15.0	mA
Non-inverting Input Current	$V_{IN} = 15V$		5.0	7.0	mA
	$V_{IN} = 0$	−1.6	−1.0		mA
	$V_{IN} = -15V$	−9.8	−7.0		mA
Inverting Input Current	$V_{IN} = 15V$		3.0	4.2	mA
	$V_{IN} = 0$		0	−0.5	mA
	$V_{IN} = -15V$	−4.2	−3.0		mA

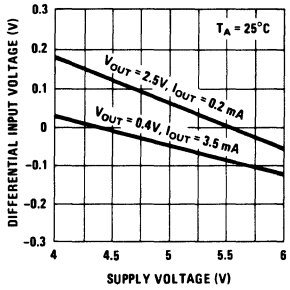
Note 1: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 100°C/W and a maximum junction temperature of 160°C for the DM7820 or 105°C for the DM8820.

Note 2: These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq 125°C$ for the DM7820 or $0°C \leq T_A \leq 70°C$ for the DM8820 unless otherwise specified; typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0$ unless stated differently.

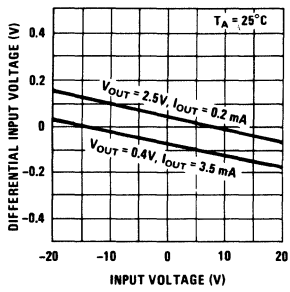
Note 3: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

typical performance characteristics (Note 3)

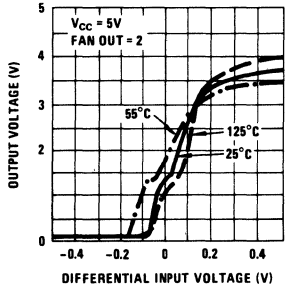
Supply Voltage Sensitivity



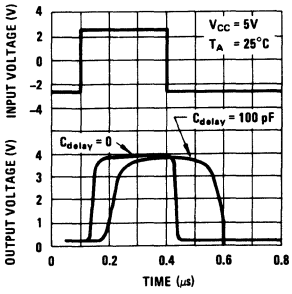
Common Mode Rejection



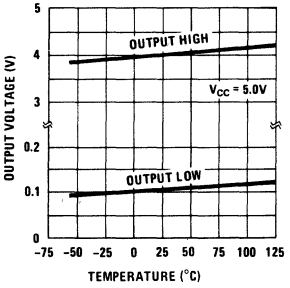
Transfer Function



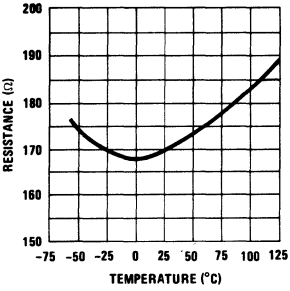
Response Time



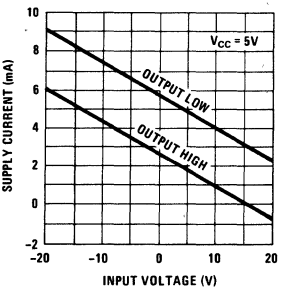
Output Voltage Levels



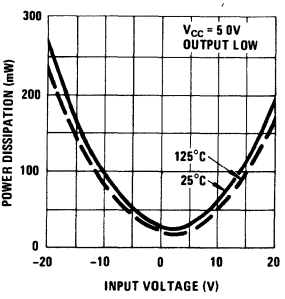
Termination Resistance



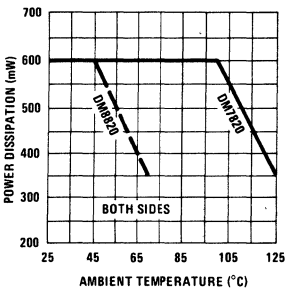
Positive Supply Current



Internal Power Dissipation



Maximum Power Dissipation



4

Line Drivers/Receivers

DM7820A/DM8820A dual line receiver

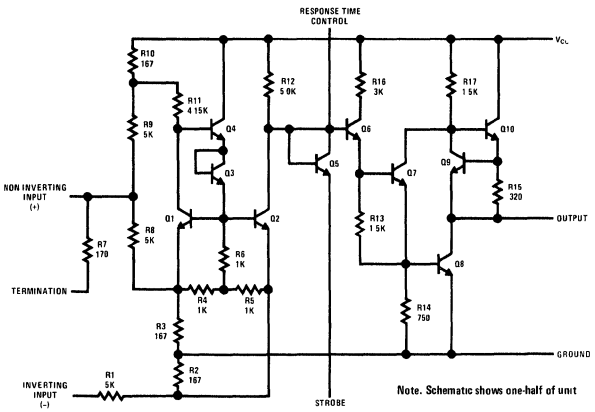
general description

The DM7820A and the DM8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits. Some important design features include:

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with either DTL or TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

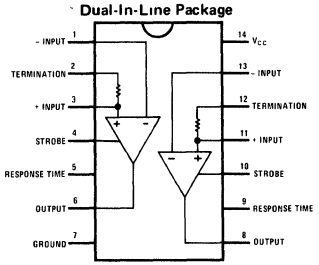
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DM7820A and the DM8820A are specified, worst case, over their full operating temperature range (−55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

schematic and connection diagrams



Note. Schematic shows one-half of unit

Dual-In-Line Package



Note Pin 7 connected to bottom of cavity package.

TOP VIEW

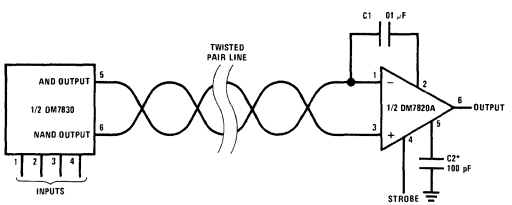
Order Number DM7820AJ or DM8820AJ
See Package 16

Order Number DM8820AN
See Package 22

Order Number DM7820AW or DM8820AW
See Package 27

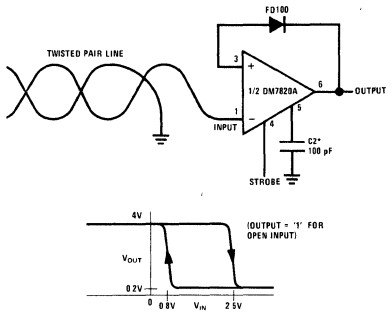
typical applications

Differential Line Driver and Receiver



*Optional to control response time

Single Ended (EIA-RS232C) Receiver with Hysteresis



absolute maximum ratings

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Power Dissipation (Note 1)	600 mW
Operating Temperature Range	
DM7820A	−55°C to 125°C
DM8820A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 2, 3 & 4)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
	V_{CM}	OUTPUT	OTHER				
Differential Threshold Voltage	$-3V \le V_{CM} \le +3V$	−400 μA	$V_{OUT} \ge 2.5V$		+0.06	+0.5	V
	$-15V \le V_{CM} \le +15V$	−400 μA	$V_{OUT} \ge 2.5V$		+0.06	+1.0	V
	$-3V \le V_{CM} \le +3V$	+16 mA	$V_{OUT} \le 0.4V$		−0.08	−0.5	V
	$-15V \le V_{CM} \le +15V$	+16 mA	$V_{OUT} \le 0.4V$		−0.08	−1.0	V
Inverting Input Resistance	$-15V \le V_{CM} \le +15V$			3.6	5		kΩ
Non-Inverting Input Resistance	$-15V \le V_{CM} \le +15V$			1.8	2.5		kΩ
Line Termination Resistance			$T_A = 25°C$	120	170	250	Ω
Inverting Input Current	+15V				+3.0	+4.2	mA
	0V				0	−0.5	mA
	−15V				−3.0	−4.2	mA
Non-Inverting Input Current	+15V				+5.0	+7.0	mA
	0V				−1.0	−1.6	mA
	−15V				−7.0	−9.8	mA
Power Supply Current	+15V	Logic "0"	$V_{DIFF} = -1V$		+3.9	+6.0	mA
	0V	Logic "0"	$V_{DIFF} = -0.5V$		+6.5	+10.2	mA
	−15V	Logic "0"	$V_{DIFF} = -1V$		+9.2	+14.0	mA
Logical "1" Output Voltage		−400 μA	$V_{DIFF} = +1V$	2.5	4.0	5.5	V
Logical "0" Output Voltage		+16 mA	$V_{DIFF} = -1V$	0	0.22	0.4	V
Logical "1" Strobe Input Voltage		+16 mA	$V_{OUT} \le 0.4V$, $V_{DIFF} = -3V$	2.1			V
Logical "0" Strobe Input Voltage		−400 μA	$V_{OUT} \ge 2.5V$, $V_{DIFF} = -3V$			0.9	V
Logical "1" Strobe Input Current			$V_{STROBE} = 5.5V$, $V_{DIFF} = +3V$		0.01	5.0	μA
Logical "0" Strobe Input Current			$V_{STROBE} = 0.4V$, $V_{DIFF} = -3V$		−1.0	−1.4	mA
Output Short Circuit Current		0V	$V_{CC} = 5.5V$, $V_{STROBE} = 0V$	−2.8	−4.5	−6.7	mA
Propagation Delays (see waveforms)							
Differential Input to "0" Output			$V_{CC} = 5V$, $T_A = 25°C$		30	45	ns
Differential Input to "1" Output			$V_{CC} = 5V$, $T_A = 25°C$		35	55	ns
Strobe Input to "0" Output			$V_{CC} = 5V$, $T_A = 25°C$		16	25	ns
Strobe Input to "1" Output			$V_{CC} = 5V$, $T_A = 25°C$		18	30	ns

Note 1: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 100°C/W and a maximum junction temperature of 160°C for the DM7820A, or 150°C/W and 115°C maximum junction temperature for the DM8820A.

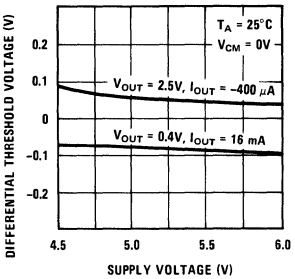
Note 2: These specifications apply for $4.5V \le V_{CC} \le 5.5V$, $-15V \le V_{CM} \le 15V$ and $-55°C \le T_A \le 125°C$ for the DM7820A or $0°C \le T_A \le 70°C$ for the DM8820A unless otherwise specified. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently

Note 3: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

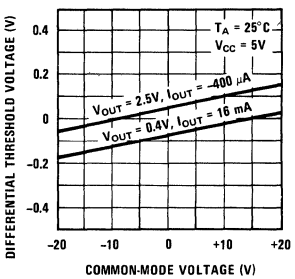
Note 4: Min and max limits apply to absolute values.

typical performance characteristics (Note 3)

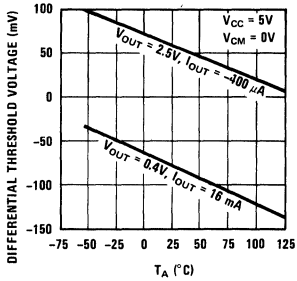
Supply Voltage Sensitivity



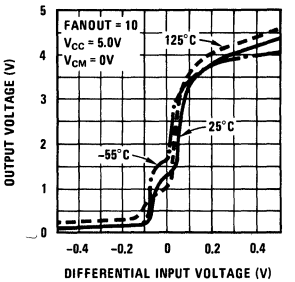
Common-Mode Voltage Sensitivity



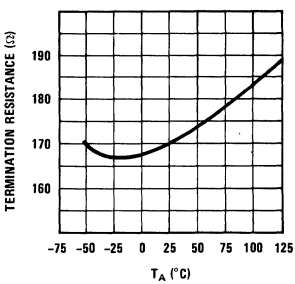
Temperature Sensitivity



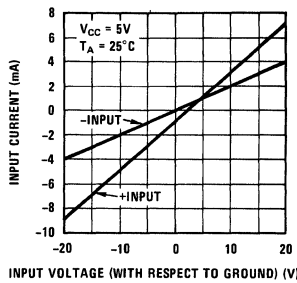
Transfer Function



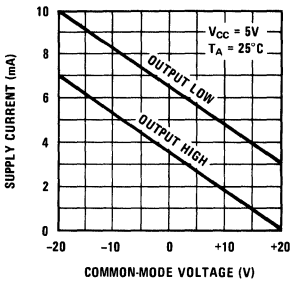
Termination Resistance



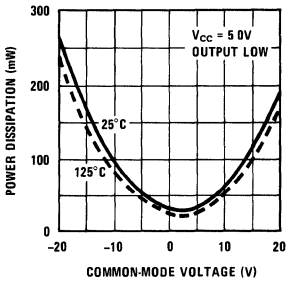
Input Characteristics



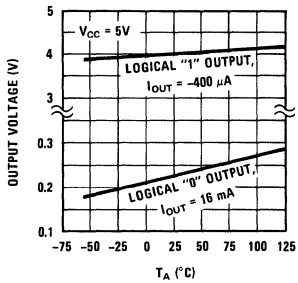
Power Supply Current



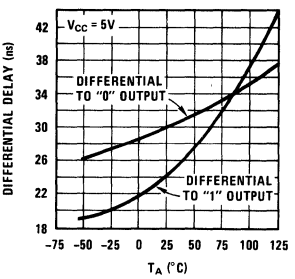
Internal Power Dissipation



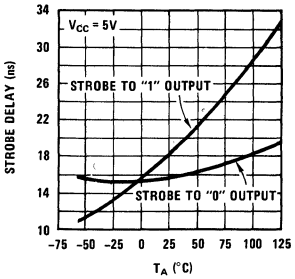
Output Voltage Levels



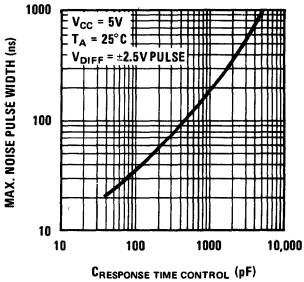
Differential Input Delays



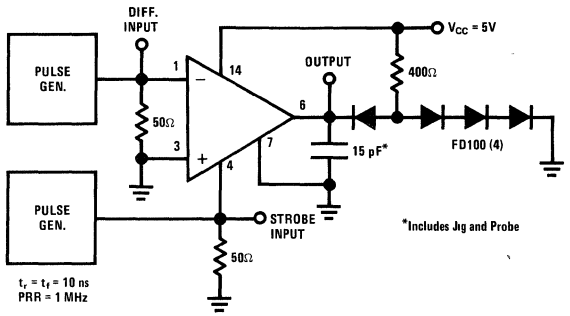
Strobe Delays

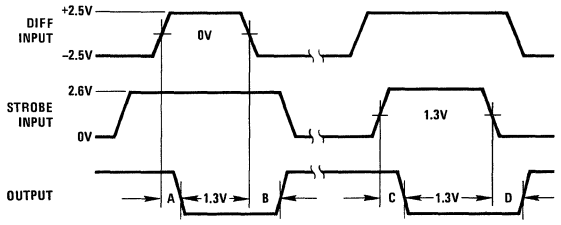


Noise Rejection



ac test circuit and waveforms





A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

4

Line Drivers /Receivers

DM7822/DM8822 dual line receiver

general description

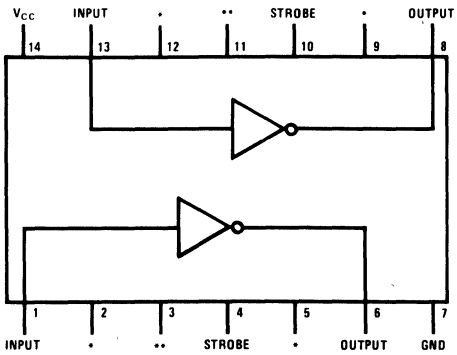
The DM7822/DM8822 is a dual inverting line receiver which meets the requirements of EIA specification RS232 Revision B. The device contains both receivers on a single monolithic silicon chip. The receivers share common power supply and ground connections, otherwise their operation is fully independent.

In addition to meeting the requirements of RS232, the DM7822/DM8822 also has independent strobe inputs which allow the receiver to be placed in the high state independent of the information being received at the input.

The output of the DM7822/DM8822 is completely compatible with five volt DTL and TTL logic families

The DM7822 is specified for operation over the −55°C to +125°C military temperature range. The DM8822 is specified for operation over the 0°C to +70°C temperature range.

connection diagram



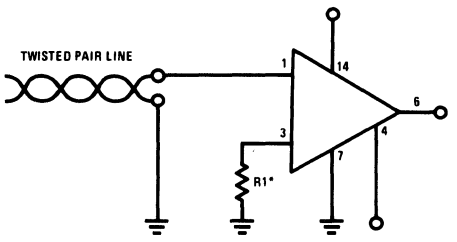
*Make no connection to these pins

**For operation requiring "Mark Hold" with the input open connect a 470Ω resistors from each of these pins to ground

Order Number DM7822J
See Package 16

Order Number DM8822N
See Package 22

typical connection



*For Mark Hold R1 = 470Ω, otherwise connect pin 3 to ground

absolute maximum ratings

Supply Voltage		8.0V
Input Voltage		±30V
Strobe Voltage		8.0V
Output Sink Current		25 mA
Power Dissipation (Note 1)		600 mW
Operating Temperature Range	DM7822	−55°C to +125°C
	DM8822	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER	PARAGRAPH IN RS-232	CONDITIONS	MIN	TYP	MAX	UNITS
Negative Input Threshold Voltage	4.8 (8)	$V_{OUT} \geq 2.5V$	−2.0			V
Positive Input Threshold Voltage (Note 3)		$V_{OUT} \leq 0.4V$			2.0	V
Input Resistance	4.5 and 4.8 (5)		3.0	5.0	7.0	kΩ
Input Current		$V_{IN} = 25V$	3.57	5	8.33	mA
		$V_{IN} = 0V$		0		mA
		$V_{IN} = -25V$	−8.33	−5	−3.57	mA
Open Circuit Input Voltage	4.5 and 4.8 (4)	$V_{IN} = 0V$		.03	0.5	V
Logical "1" Output Voltage		$I_{OUT} \leq -0.2$ mA	2.5			V
Logical "0" Output Voltage		$I_{OUT} = 3.5$ mA			0.4	V
Strobe Current		$V_{STROBE} = 0.4V$		1.0	1.4	mA
		$V_{STROBE} = 5.5V$		−5.0 μA	−1.0 mA	
Power Supply Current (Both Receivers)		$-25V \leq V_{IN} \leq 25V$			24.0	mA
Response Time, t_1 or t_2		$T_A = 25°C$ $V_{CC} = 5.0V$ Input Ramp Rate $\leq$ 10 ns		65	125	ns

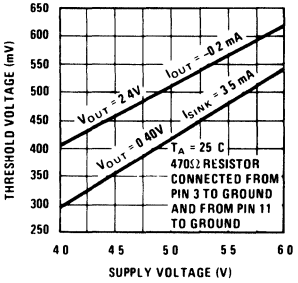
Note 1. For operating at elevated temperatures, the device must be derated in accordance with the "Maximum Power Dissipation" curve

Note 2. Min/Max limits apply across the guaranteed temperature range of −55°C to +125°C for the DM7822 and 0°C to 70°C for the DM8822 unless otherwise specified Likewise the limits apply across the guaranteed V_{CC} range of 4.5V to 5.5V for the DM7822 and 4.75V to 5.25V for the DM8822 unless otherwise specified. Typical values are given for $V_{CC} = 5.0V$ and $T_A = 25°C$

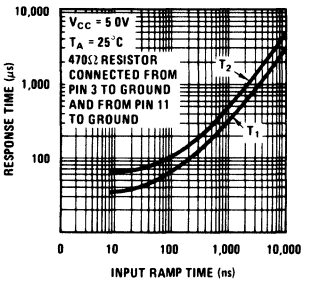
Note 3. Since the EIA RS-232 specification requires the threshold to be between −3V and +3V, the immunity limits shown here guarantee 1 volt additional noise immunity

typical performance characteristics

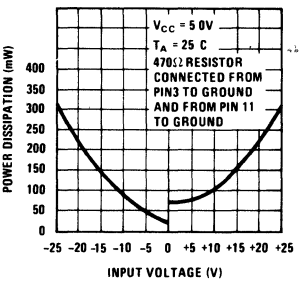
Threshold Voltage vs Supply Voltage



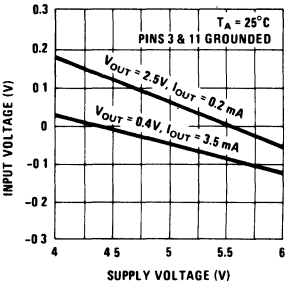
Response Time vs Input Ramp Time



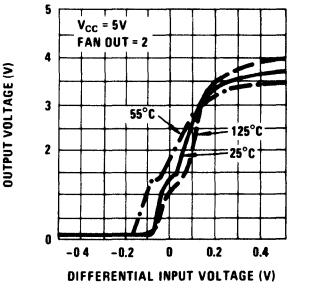
Internal Power Dissipation



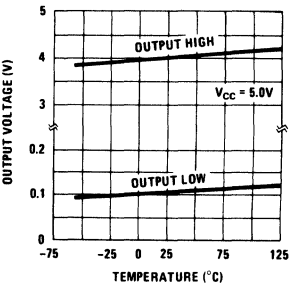
Threshold Voltage vs Supply Voltage



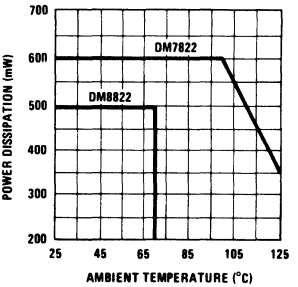
Transfer Function



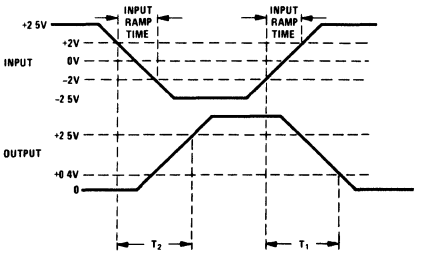
Output Voltage Levels



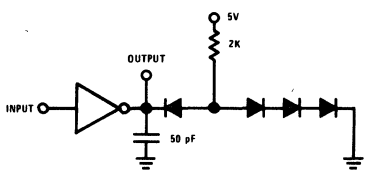
Maximum Power Dissipation



switching time waveforms



ac test circuit



Line Drivers/Receivers

DM7830/DM8830 dual differential line driver

general description

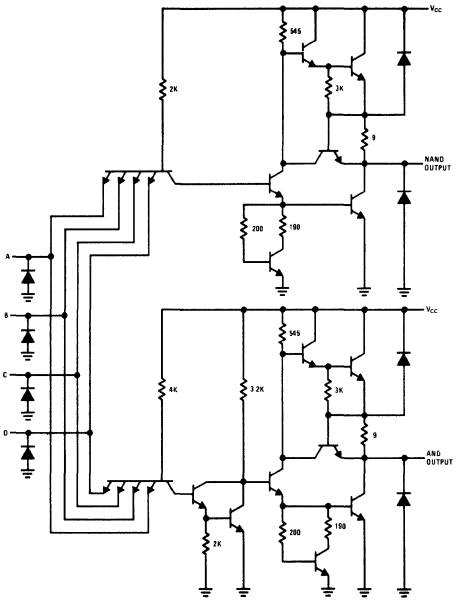
The DM7830/DM8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

features

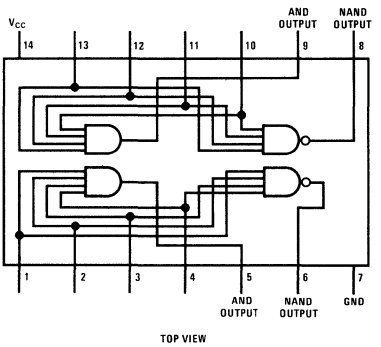
- Single 5 volt power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High Speed
- Short Circuit Protection

schematic* and connection diagrams



*2 PER PACKAGE.

Dual-In-Line and Flat Package



TOP VIEW

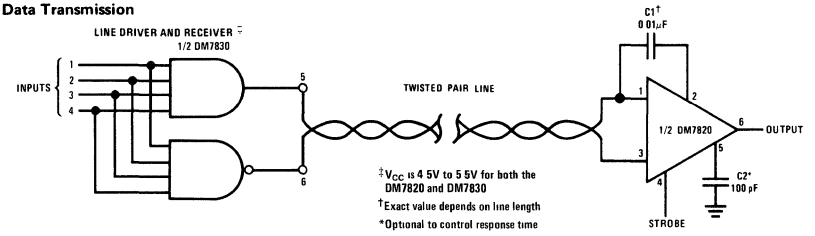
Order Number DM7830J or DM8830J
See Package 16

Order Number DM8830N
See Package 22

Order Number DM7830W or DM8830W
See Package 27

typical application

Digital Data Transmission



‡V_{CC} is 4.5V to 5.5V for both the DM7820 and DM7830

†Exact value depends on line length

*Optional to control response time

absolute maximum ratings

V_{CC}		7.0V
Input Voltage		5.5V
Operating Temperature	DM7830	−55°C to +125°C
	DM8830	0°C to 70°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C
Output Short Circuit Duration (125°C)		1 second

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2.0			V
Logical "0" Input Voltage				0.8	V
Logical "1" Output Voltage	V_{IN} = 0.8V I_{OUT} = −0.8 mA	2.4			V
Logical "1"Output Voltage	V_{IN} = 0.8V I_{OUT} = 40 mA	1.8	3.3		V
Logical "0" Output Voltage	V_{IN} = 2.0V I_{OUT} = +32 mA		0.2	0.4	V
Logical "0" Output Voltage	V_{IN} = 2.0V I_{OUT} = +40 mA		0.22	0.5	V
Logical "1" Input Current	V_{IN} = +2.4V			120	μA
Logical "1" Input Current	V_{IN} = 5.5V			2	mA
Logical "0" Input Current	V_{IN} = 0.4V			4.8	mA
Output Short Circuit Current	V_{CC} = 5.0V T_A = 125°C	40	100	120	mA
Supply Current	V_{IN} = 5.0V (Each Driver)		11	18	mA
Propagation Delay AND Gate t_{pd1}	T_A = 25°C		8	12	ns
t_{pd0}	V_{CC} = 5.0V		11	18	ns
Propagation Delay NAND Gate t_{pd1}	C_L = 15 pF		8	12	ns
t_{pd0}	See Figure 1		5	8	ns
Differential Delay t_1	Load, 100Ω and 5000 pF		12	16	ns
Differential Delay t_2	See Figure 2		12	16	ns

Note 1: Specifications apply for DM7830 −55°C ≤ T_A ≤ +125°C, V_{CC} = +5V ±10%, DM8830 0°C ≤ T_A ≤ 70°C, V_{CC} = +5V ±5% unless otherwise stated. Typical values given are for T_A = 25°C, V_{CC} = 5.0V.

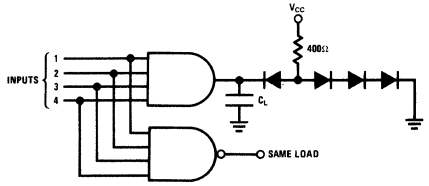


FIGURE 1.

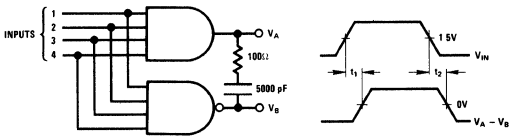
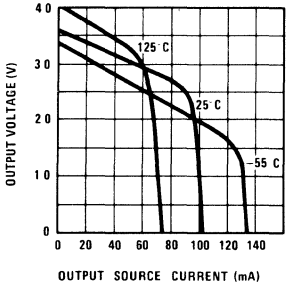


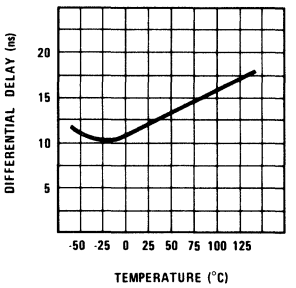
FIGURE 2.

typical performance characteristics

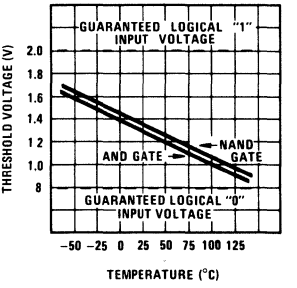
Output High Voltage (Logical "1") Vs Output Current



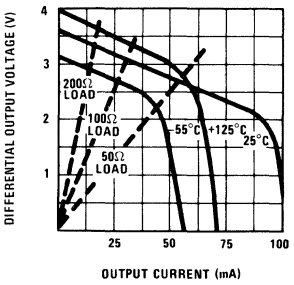
Differential Delay Vs Temperature



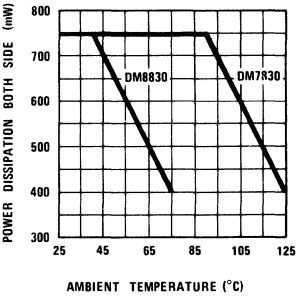
Threshold Voltage Vs Temperature



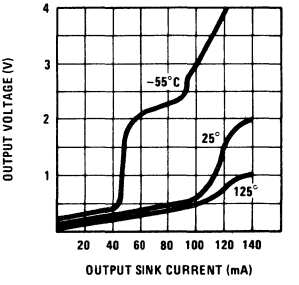
Differential Output Voltage ($|V_{AND} - V_{NAND}|$) Vs Differential Output Current



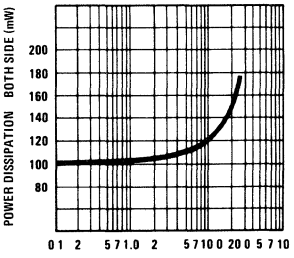
Maximum Power Dissipation



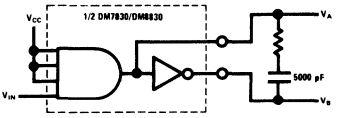
Output Low Voltage (Logical "0") Vs Output Current



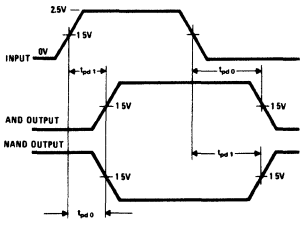
Power Dissipation (No Load) Vs Data Input Frequency

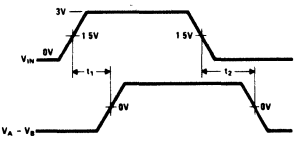


ac test circuit



switching time waveforms





Line Drivers/Receivers

DM7831/DM8831,DM7832/DM8832 TRI-STATE™ line driver

general description

Through simple logic control, the DM7831/DM8831, DM7832/DM8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DM7832/DM8832 does not have the V_{CC} clamp diodes found on the DM7831/DM8831.

The DM7831 & DM7832 are specified for operation over the −55°C to +125°C military temperature range. The DM8831 & DM8832 are specified for operation over the 0°C to +70°C temperature range.

features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line.

mode of operation

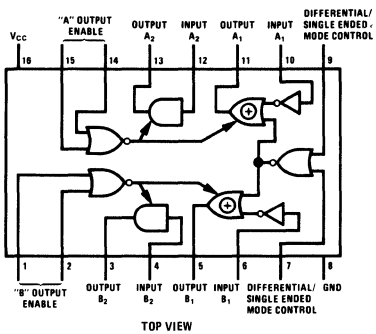
To operate as a quad single-ended line driver apply logical "0"s to the Output Disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"'s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs. The inputs to the A channels should be connected together and the inputs to the B channels should be connected to-In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

When operating in a bus-organized system with outputs tied directly to outputs of other

(continued)

connection and logic diagram



TOP VIEW

Order Number DM7831J, DM8831J, DM7832J or DM8832J
See Package 17
Order Number DM8831N or DM8832N
See Package 23
Order Number DM7831W, DM8831W, DM7832W or DM8832W
See Package 28

truth table (Shown for A Channels Only)

"A" OUTPUT DISABLE		DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL		INPUT A_1	OUTPUT A_1	INPUT A_2	OUTPUT A_2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A_1	Logical "1" or Logical "0"	Same as Input A_2
0	0	X 1	1 X	Logical "1" or Logical "0"	Opposite of Input A_1	Logical "1" or Logical "0"	Same as Input A_2
1 X	X 1	X	X	X	High impedance state	X	High impedance state

X = Don't Care

absolute maximum ratings

Supply Voltage		7V
Input Voltage		5 5V
Output Voltage		5 5V
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	DM7831, DM7832	−55°C to +125°C
	DM8831, DM8832	0°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C
Time that 2 bus-connected devices may be in opposite low impedance states simultaneously		10 ms

electrical characteristics (Note 1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM7831,DM7832	V_{CC} = 4 5V	2 0			V
	DM8831,DM8832	V_{CC} = 4 75V				
Logical "0" Input Voltage	DM7831,DM7832	V_{CC} = 4 5V			0 8	V
	DM8831,DM8832	V_{CC} = 4 75V				
Logical "1" Output Voltage	DM7831,DM7832	V_{CC} = 4.5V, I_O = −40 mA	1 8	2 3		V
		V_{CC} = 4.5V, I_O = −2 mA	2 4	2 7		V
	DM8831,DM8832	V_{CC} = 4.75V, I_O = −40 mA	1 8	2 5		V
		V_{CC} = 4.75V, I_O = −5 2 mA	2 4	2 9		V
Logical "0" Output Voltage	DM7831,DM7832	I_O = 40 mA		0 29	0 50	V
		I_O = 32 mA			.40	V
	DM8831,DM8832	I_O = 40 mA		0 29	0 50	V
		I_O = 32 mA			.40	V
Logical "1" Input Current	DM7831,DM7832	V_{CC} = 5 5V, V_{IN} = 5 5V			1	mA
	DM8831,DM8832	V_{CC} = 5 25V, V_{IN} = 2 4V			40	μA
Logical "0" Input Current	DM7831,DM7832	V_{CC} = 5 5V, V_{IN} = 0.4V		−1.0	−1 6	mA
	DM8831,DM8832	V_{CC} = 5 25V				
Output Disable Current	DM7831,DM7832	V_{CC} = 5 5V, V_O = 2.4V or 0 4V	−40		40	μA
	DM8831,DM8832	V_{CC} = 5.25V				
Output Short Circuit Current	DM7831,DM7832	V_{CC} = 5 5V	−40	−100	−120	mA
	DM8831,DM8832	V_{CC} 5.25V	(Note 2)		(Note 2)	
Supply Current	DM7831,DM7832	V_{CC} = 5.5V		65	90	mA
	DM8831,DM8832	V_{CC} = 5 25V				
Input Diode Clamp Voltage		V_{CC} = 5 0V, T_A = 25°C, I_{IN} = −12 mA			−1 5	V
Output Diode Clamp Voltage	DM7831, DM8831 DM7832, DM8832	I_{OUT} = −12 mA, V_{CC} = 5 0V, T_A = 25°C			−1 5	V
	DM7831, DM8831	I_{OUT} = +12 mA, V_{CC} = 5 0V, T_A = 25°C			V_{CC}+1 5	V
Propagation Delay to a Logical "0" from Inputs A_1, A_2, B_1, B_2 Differential Single-ended Mode Control to Outputs, t_{pd0}		V_{CC} = 5 0V, T_A = 25°C		13	25	ns
Propagation Delay to a Logical "1" from Inputs A_1, A_2, B_1, B_2 Differential Single-ended Mode Control to Outputs, t_{pd1}		V_{CC} = 5.0V, T_A = 25°C		13	25	ns
Delay from Disable Inputs to High Impedance State (from Logical "1" Level), t_{1H}		V_{CC} = 5 0V, T_A = 25°C		6	12	ns
Delay from Disable Inputs to High Impedance State (from Logical "0" Level), t_{0H}		V_{CC} = 5 0V, T_A = 25°C		14	22	ns
Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State), t_{H1}		V_{CC} = 5.0V, T_A = 25°C		14	22	ns
Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State), t_{HO}		V_{CC} = 5 0V, T_A = 25°C		18	27	ns

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7831, DM7832 and across the 0°C to 70°C temperature range for the DM8831, DM8832 All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Applies for T_A = 125°C only Only one output should be shorted at a time

mode of operation (cont.)

DM7831/DM8831's, DM7832/DM8832's (Figure 1), all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DM7831/DM8831's, DM7832/DM8832's (Figure 2).

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DM7831/DM8831's, DM7832/DM8832's and still have available drive for the bus line (Figure 3).

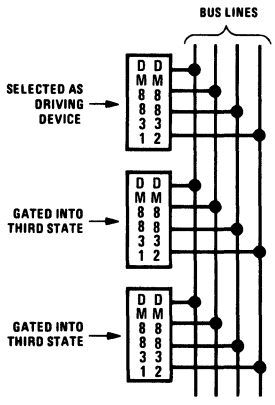


Figure 1

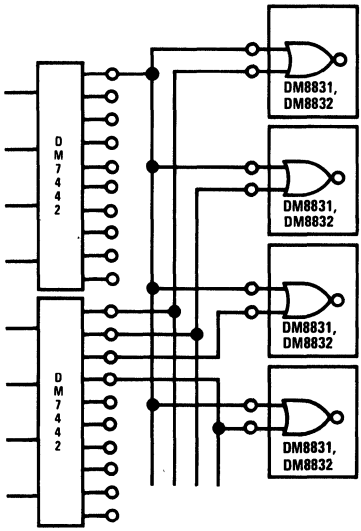


Figure 2

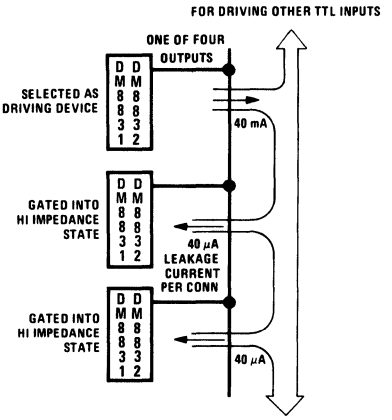
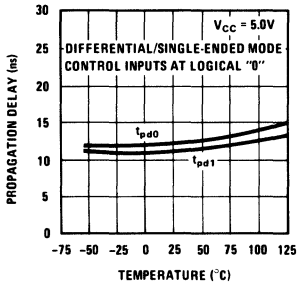


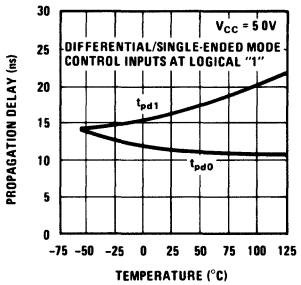
Figure 3

typical performance characteristics

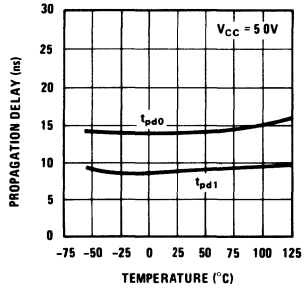
Propagation Delay from Input to Output (Channel 1)



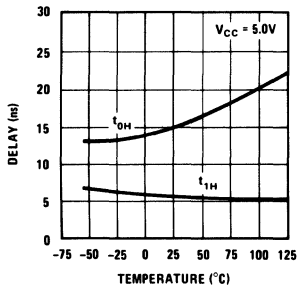
Propagation Delay from Input to Output (Channel 1)



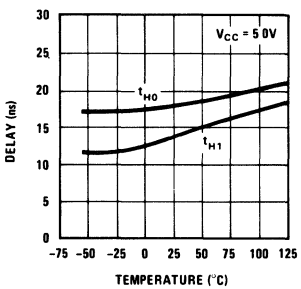
Propagation Delay from Input to Output (Channel 2)



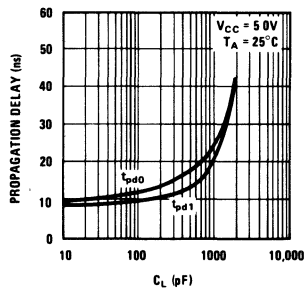
Delay from Disable to High Impedance State



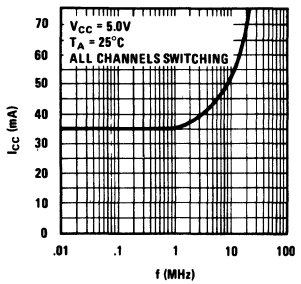
Delay from Disable to Low Impedance State



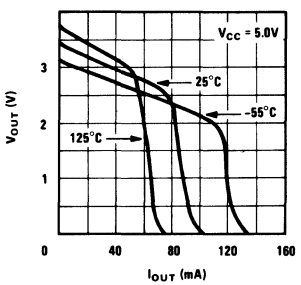
Propagation Delay vs Load Capacitance



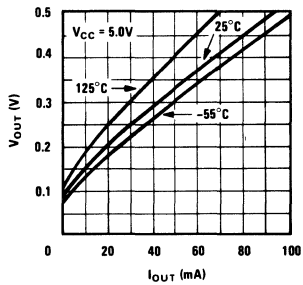
Total Supply Current vs Frequency



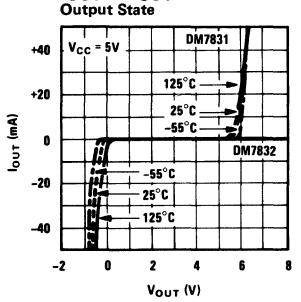
Logical "1" Output Voltage vs Source Current



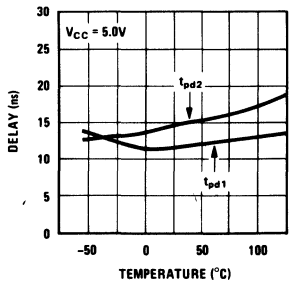
Logical "0" Output Voltage vs Sink Current

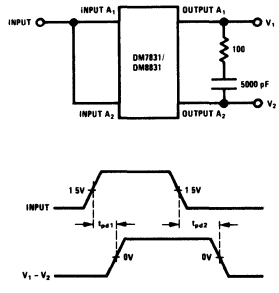


I_{OUT} vs V_{OUT} High Impedance Output State



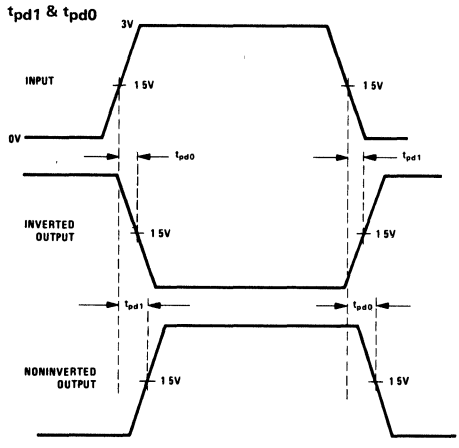
Propagation Delay in Differential Mode





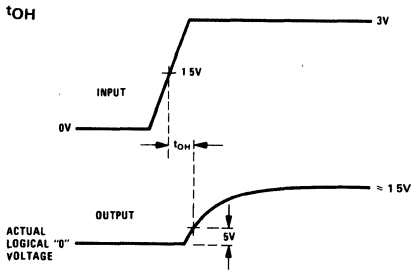
4

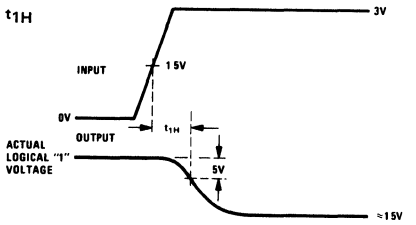
switching time waveforms

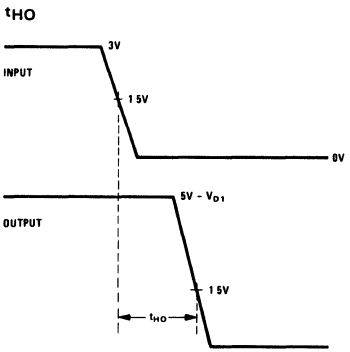


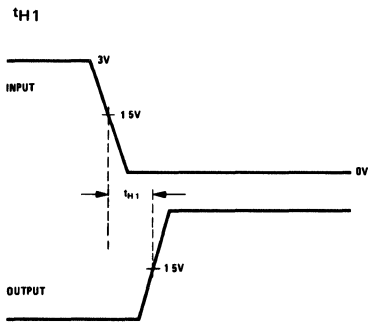
Input characteristic

Amplitude = 3.0V
Frequency = 1.0 MHz, 50% duty cycle
$t_r = t_f \leq 10$ ns (10% to 90%)

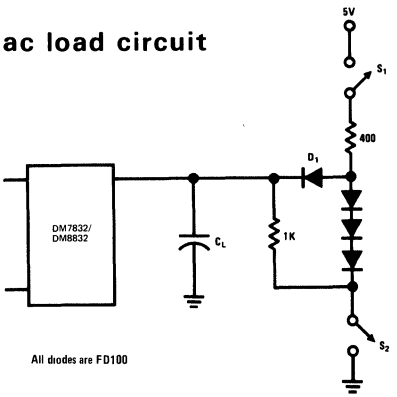








ac load circuit



All diodes are FD100

	Switch S_1	Switch S_2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{OH}	closed	closed	*5 pF
t_{1H}	closed	closed	*5 pF
t_{HO}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*Jig capacitance.

Line Drivers/Receivers

DM7836/DM8836 quad NOR unified bus receiver

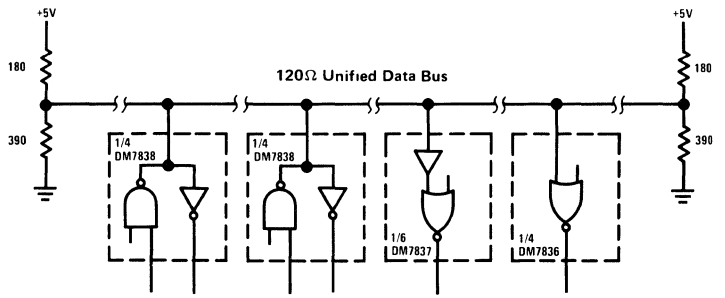
general description

The DM7836/DM8836 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. This receiver has been specifically configured to replace the SP380 gate pin-for-pin to provide the distinct advantages of the DM7837 receiver design in existing systems. Performance is optimized for systems with bus rise and fall times $\leq 10\mu s$.

features

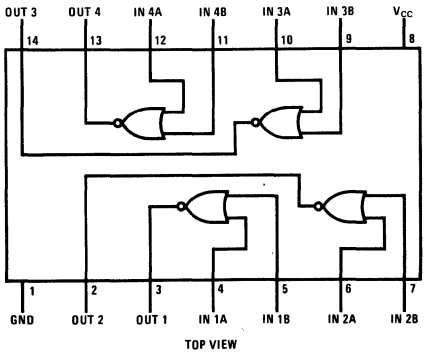
- Plug-in replacement for SP380 gate
- Low input current with normal V_{CC} or $V_{CC} = 0V$ (15 μA typ)
- Built-in input hysteresis (1V typ)
- High noise immunity (2V typ)
- Temperature-insensitive input thresholds track bus logic levels
- DTL/TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (18 ns typ)

typical application



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

Order Number DM7836J or DM8836J
See Package 16

Order Number DM8836N
See Package 22

Order Number DM7836W or DM8836W
See Package 27

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Power Dissipation	600 mW
Operating temperature range:	
DM7836	−55°C to +125°C
DM8836	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

The following apply for $V_L \leq V_{CC} \leq V_H$, $T_L \leq T_A \leq T_H$, unless otherwise specified (Note 2)

PARAMETER	INPUT	OUTPUT	COMMENTS	MIN	TYP	MAX	UNIT
High Level Input Threshold							
DM7836	V_{TH}	16 mA	Output < 0 4V	1.65	2 25	2 65	V
DM8836	V_{TH}	16 mA	Output < 0 4V	1.80	2.25	2 50	V
Low Level Input Threshold							
DM7836	V_{TH}	−400 μA	Output > 2 4V	0.97	1 30	1 63	V
DM8836	V_{TH}	−400 μA	Output > 2 4V	1.05	1.30	1.55	V
Maximum Input Current	4V		$V_{CC} = V_H$		15	50	μA
Maximum Input Current	4V		$V_{CC} = 0V$		1	50	μA
Logic "1" Output Voltage	0 5V	−400 μA		2 4			V
Logic "0" Output Voltage	4V	16 mA			0 25	0 4	V
Output Short Circuit Current	0 5V	0V	$V_{CC} = V_H$	−18		−55	mA
Power Supply Current	4V		Per Package		25	40	mA
Input Clamp Diode Voltage	−12 mA		$T_A = 25°C$		−1	−1.5	V
The following apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified							
Propagation Delays							
Input to Logic "1" Output			Note 3		20	30	ns
Input to Logic "0" Output			Note 4		18	30	ns

Note 1: Voltage values are with respect to network ground terminal. Positive current is defined as current into the reference pin.
Note 2: For DM7836: $V_L = 4.5V$, $V_H = 5.5V$, $T_L = -55°C$, $T_H = +125°C$.
For DM8836: $V_L = 4.75V$, $V_H = 5.25V$, $T_L = 0°C$, $T_H = +70°C$.
Note 3: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.
Note 4: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Line Drivers/Receivers

DM7837/DM8837 hex unified bus receiver

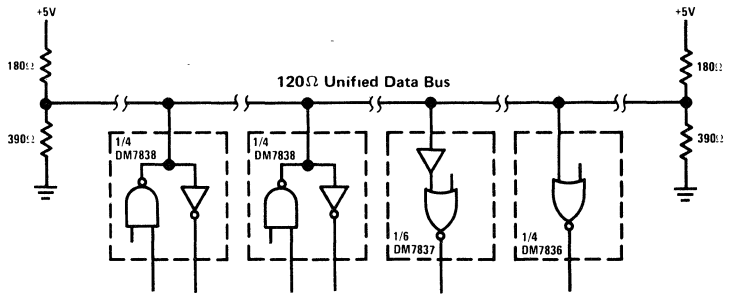
general description

The DM7837/DM8837 are high speed receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The receiver design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Disable inputs provide time discrimination. Disable inputs and receiver outputs are DTL/TTL compatible. Performance is optimized for systems with bus rise and fall times $\leq 10\mu s$.

features

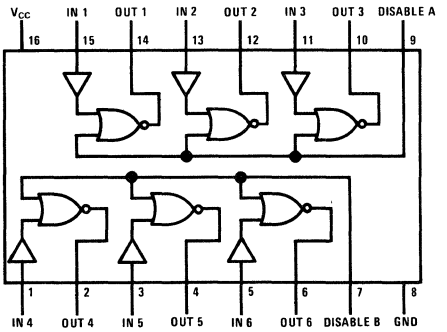
- Low receiver input current for normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Six separate receivers per package
- Built-in receiver input hysteresis (1V typ)
- High receiver noise immunity (2V typ)
- Temperature insensitive receiver input thresholds track bus logic levels
- DTL/TTL compatible disable and output
- Molded or cavity dual-in-line or flat package
- High speed

typical application



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

Order Number DM7837J or DM8837J
See Package 17

Order Number DM8837N
See Package 23

Order Number DM7837W or DM8837W
See Package 28

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Power Dissipation	600 mW
Operating Temperature Range	
DM7837	−55°C to +125°C
DM8837	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

The following apply for $V_L \leq V_{CC} \leq V_H$, $T_L \leq T_A \leq T_H$, unless otherwise specified (Note 2)

PARAMETER	RECEIVER INPUT	DISABLE INPUT	OUTPUT	COMMENTS	MIN	TYP	MAX	UNIT
High Level Receiver Threshold DM7837	V_{TH}	0 8V	16 mA	Output < 0 4V	1 65	2 25	2 65	V
High Level Receiver Threshold DM8837	V_{TH}	0 8V	16 mA	Output < 0 4V	1 80	2 25	2 50	V
Low Level Receiver Threshold DM7837	V_{TH}	0 8V	−400 mA	Output > 2 4V	0.97	1 30	1 63	V
Low Level Receiver Threshold DM8837	V_{TH}	0 8V	−400 mA	Output > 2 4V	1.05	1 30	1 55	V
Maximum Receiver Input Current	4V			V_{CC} · V_H		15 0	50 0	μA
Maximum Receiver Input Current	4V			V_{CC} 0V		1 0	50 0	μA
Logic "1" Input Voltage Disable	0 5V	V_{IN}	16 mA	Output < 0 4V	2 0			V
Logic "0" Input Voltage Disable	0 5V	V_{IN}	−400 μA	Output > 2 4V			0 8	V
Logic "1" Output Voltage	0 5V	0 8V	−400 μA		2 4			V
Logic "0" Output Voltage	4V	0 8V	16 mA			0 25	0 4	V
Logic "1" Input Current Disable		2 4V					80 0	μA
Logic "1" Input Current Disable		5 5V					2 0	mA
Logic "0" Input Current Disable	4V	0 4V					−3 2	mA
Output Short Circuit Current	0 5V	0V	0V	$V_{CC} = V_H$	−18 0		−55 0	mA
Power Supply Current	4V	0V		Per Package		45.0	60 0	mA
Input Clamp Diode	−12 mA	−12 mA		$T_A = 25°C$		−1 0	−1 5	V
The following apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified								
Propagation Delays								
Receiver Input to Logic "1" Output		0V		Note 3		20	30	ns
Receiver Input to Logic "0" Output		0V		Note 4		18	30	ns
Disable Input to Logic "1" Output	0V			Note 5		9	15	ns
Disable Input to Logic "0" Output	0V			Note 5		4	10	ns

Note 1: Voltage values are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
Note 2: For DM7837: $V_L = 4.5V$, $V_H = 5.5V$, $T_L = -55°C$, $T_H = +125°C$
For DM8837: $V_L = 4.75V$, $V_H = 5.25V$, $T_L = 0°C$, $T_H = +70°C$
Note 3: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.
Note 4: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.
Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Line Drivers /Receivers

DM7838/DM8838 quad unified bus transceiver

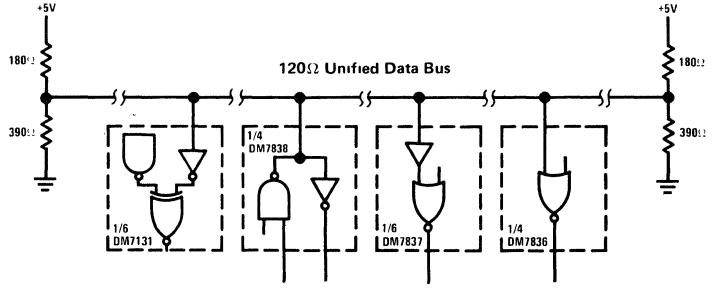
general description

The DM7838/DM8838 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times $\leq 10\mu s$.

features

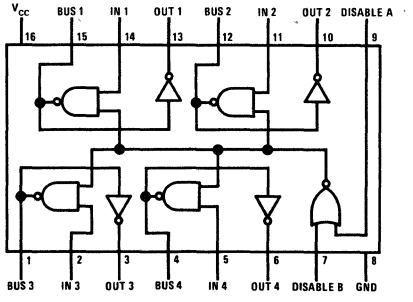
- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

typical application



connection diagram

Dual In-Line and Flat Package



TOP VIEW

Order Number DM7838J or DM8838J
See Package 17

Order Number DM7838W or DM8838W
See Package 28

Order Number DM8838N
See Package 23

absolute maximum ratings

Supply Voltage	7V	Operating Temperature Range	
Input and Output Voltage	5 5V	DM7838	−55 C to +125 C
Power Dissipation	600 mW	DM8838	0 C to +70 C
		Storage Temperature Range	−65 C to +150 C
		Lead Temperature (Soldering, 10 sec)	300 C

electrical characteristics

DM7838/DM8838 The following apply for $V_L \leq V_{CC} \leq V_H$, $T_L \leq T_A \leq T_H$ unless otherwise specified (Note 2)

PARAMETER	DISABLE INPUT	DRIVER INPUT	BUS PIN	RECEIVER OUTPUT	COMMENTS	MIN	TYP	MAX	UNIT
Logic "1" Input Voltage Disable	V_{IN}	2V	4V		Bus < 100 μA	2 0			V
Logic "0" Input Voltage Disable	V_{IN}	2V	50 mA		Bus < 0 7V			0 8	V
Logic "1" Input Voltage Driver	0 8V	V_{IN}	50 mA		Bus < 0 7V	2 0			V
Logic "0" Input Voltage Driver	0 8V	V_{IN}	4V		Bus < 100 μA			0 8	V
High Level Receiver Threshold DM7838		0 8V	V_{TH}	16 mA	Receiver output < 0 4V	1 65	2 25	2 65	V
High Level Receiver Threshold DM8838		0 8V	V_{TH}	16 mA	Receiver output < 0 4V	1 80	2 25	2 50	V
Low Level Receiver Threshold DM7838		0 8V	V_{TH}	−400 μA	Receiver output > 2 4V	0 97	1 30	1 63	V
Low Level Receiver Threshold DM8838		0 8V	V_{TH}	−400 μA	Receiver output > 2 4V	1 05	1 30	1 55	V
Logic "1" Input Current Disable and Driver	5 5V	5 5V						1	mA
Logic "1" Input Current Disable and Driver	2 4V	2 4V						40	μA
Logic "0" Input Current Disable and Driver	0 4V	0 4V						−1 6	mA
Maximum Bus Current	0 8V	0 8V	4V		$V_{CC} = V_H$		20	100	μA
Maximum Bus Current	0 8V	0 8V	4V		$V_{CC} = 0V$		2	100	μA
Low Level Bus Voltage	0 8V	2V	50 mA				0 4	0 7	V
Logic "1" Output Voltage Receiver	0 8V	0 8V	0 5V	−400 μA		2 4			V
Logic "0" Output Voltage Receiver	0 8V	0 8V	4V	16 mA			0 25	0 4	V
Output Short Circuit Current Receiver	0 8V	0 8V	0 5V	0V	$V_{CC} = V_H$	−18		−55	mA
Supply Current	0V	2V			Per Package		50	70	mA
Input Diode Clamp Voltage	−12 mA	−12 mA	−12 mA		$T_A = 25°C$		−1	−1 5	V
The following apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified									
Propagation Delays									
Disable to Bus "1"					Note 3		19	30	ns
Disable to Bus "0"					Note 3		15	23	ns
Driver Input to Bus "1"					Note 3		17	25	ns
Driver Input to Bus "0"					Note 3		9	15	ns
Bus to Logic "1" Receiver Output					Note 4		20	30	ns
Bus to Logic "0" Receiver Output					Note 5		18	30	ns

Note 1: Voltage values are with respect to network ground terminal Positive current is defined as current into the referenced pin.

Note 2: For DM7838. $V_L = 4.5V$, $V_H = 5.5V$, $T_L = -55°C$, $T_H = +125°C$
For DM8838. $V_L = 4.75V$, $V_H = 5.25V$, $T_L = 0°C$, $T_H = +70°C$

Note 3: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, $C_{LOAD} = 15$ pF total Measured from $V_{IN} = 1.5V$ to $V_{BUS} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 4: Fan-out of 10 load, $C_{LOAD} = 15$ pF total Measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1\ 5V$, $V_{IN} = 0V$ to 3.0V pulse

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total Measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1\ 5V$, $V_{IN} = 0V$ to 3 0V pulse.

Line Drivers/Receivers

LM1488 quad line driver

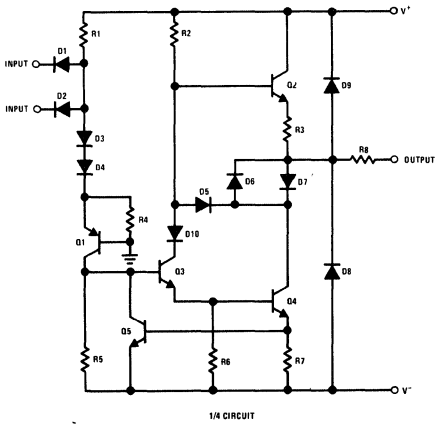
general description

The LM1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V. 24.

features

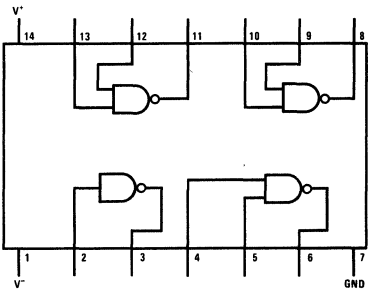
- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

schematic and connection diagrams



1/4 CIRCUIT

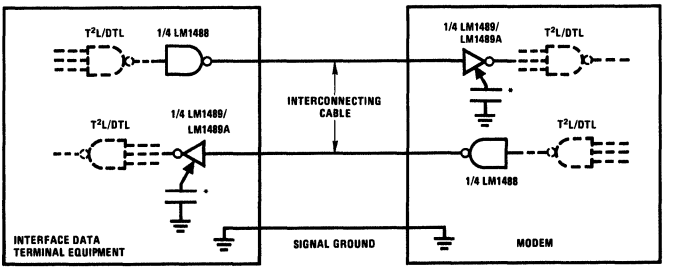
Dual-In-Line Package



TOP VIEW
Order Number LM1488J
See Package 16

typical applications

RS232C Data Transmission



*OPTIONAL FOR NOISE FILTERING

absolute maximum ratings (Note 1)

Supply Voltage	
V^+	+15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \leq V_{IN} \leq 7.0V$
Output Voltage	±15V
Power Derating (Note 2)	
(Package Limitation, J Package)	1000 mW
Derating above T_A = +25°C ($1/\theta_{JA}$)	6.7 mW/°C
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "0" Input Current	V_{IN} = 0V		−1.0	−1.3	mA
Logic "1" Input Current	V_{IN} = +5.0V		.005	10.0	μA
High Level Output Voltage	R_L = 3.0kΩ, V_{IN} = 0.8V; V^+ = 9.0V, V^- = −9.0V	6.0	7.0		V
	R_L = 3.0kΩ, V_{IN} = 0.8V; V^+ = 13.2V, V^- = −13.2V	9.0	10.5		V
Low Level Output Voltage	R_L = 3.0kΩ, V_{IN} = 1.9V; V^+ = 9.0V, V^- = −9.0V	−6.0	−6.8		V
	R_L = 3.0kΩ, V_{IN} = 1.9V; V^+ = 13.2V, V^- = −13.2V	−9.0	−10.5		V
High Level Output Short-Circuit Current	V_{OUT} = 0V, V_{IN} = 0.8V	−6.0	−10.0	−12.0	mA
Low Level Output Short-Circuit Current	V_{OUT} = 0V, V_{IN} = 1.9V	6.0	10.0	12.0	mA
Output Resistance	$V^+ = V^- = 0V$, V_{OUT} = ±2V	300			Ω
Positive Supply Current (Output Open)	V_{IN} = 1.9V; V^+ = 9.0V, V^- = −9.0V		15.0	20.0	mA
	V_{IN} = 1.9V; V^+ = 12V, V^- = −12V		19.0	25.0	mA
	V_{IN} = 1.9V; V^+ = 15V, V^- = −15V		25.0	34.0	mA
	V_{IN} = 0.8V; V^+ = 9.0V, V^- = −9.0V		4.5	6.0	mA
	V_{IN} = 0.8V; V^+ = 12V, V^- = −12V		5.5	7.0	mA
	V_{IN} = 0.8V; V^+ = 15V, V^- = −15V		8.0	12.0	mA
Negative Supply Current (Output Open)	V_{IN} = 1.9V; V^+ = 9.0V, V^- = −9.0V		−13.0	−17.0	mA
	V_{IN} = 1.9V; V^+ = 12V, V^- = −12V		−18.0	−23.0	mA
	V_{IN} = 1.9V; V^+ = 15V, V^- = −15V		−25.0	−34.0	mA
	V_{IN} = 0.8V; V^+ = 9.0V, V^- = −9.0V		−.001	−1.0	mA
	V_{IN} = 0.8V; V^+ = 12V, V^- = −12V		−.001	−1.0	mA
	V_{IN} = 0.8V; V^+ = 15V, V^- = −15V		−.01	−2.5	mA
Power Dissipation	V^+ = 9.0V, V^- = −9.0V		252	333	mW
	V^+ = 12V, V^- = −12V		444	576	mW
Propagation Delay to "1" (t_{pd1})	R_L = 3.0 kΩ C_L = 15 pF, T_A = 25°C		230	350	ns
Propagation Delay to "0" (t_{pd0})	R_L = 3.0 kΩ C_L = 15 pF, T_A = 25°C		70	175	ns
Rise Time (t_r)	R_L = 3.0 kΩ C_L = 15 pF, T_A = 25°C		75	100	ns
Fall Time (t_f)	R_L = 3.0 kΩ C_L = 15 pF, T_A = 25°C		40	75	ns

Note 1: Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

Note 2: The maximum junction temperature of the LM1488 is 150°C. For operating at elevated temperatures the cavity Dual-In-Line Package (J) must be derated based on a thermal resistance of 85°C/W, junction to ambient.

Note 3: These specifications apply for V^+ = +9.0V ± 1%, V^- = −9.0V ± 1%, T_A = 0°C to +75°C unless otherwise noted. All typicals are for V^+ = 9.0V, V^- = −9.0V, and T_A = 25°C.

applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the LM1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship,

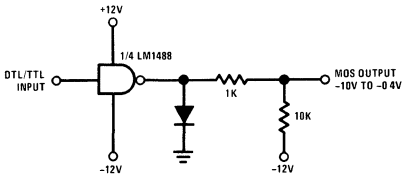
$$C = I_{SC}\,(\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

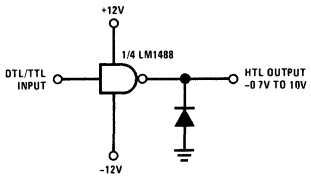
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

typical applications (con't)

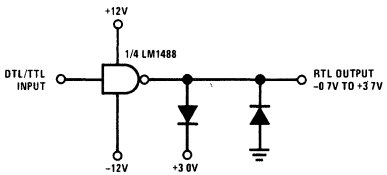
DTL/TTL-to-MOS Translator



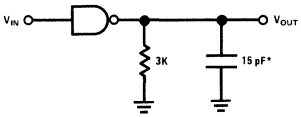
DTL/TTL-to-HTL Translator



DTL/TTL-to-RTL Translator

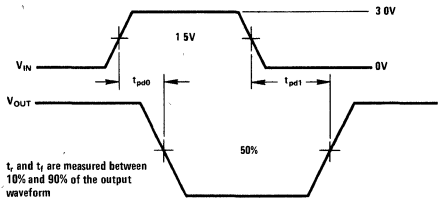


ac load circuit



*C_L includes probe and jig capacitance

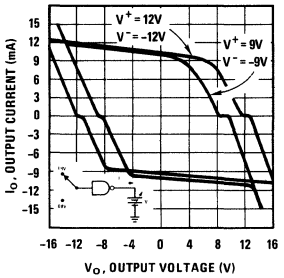
switching time waveforms



t_r and t_f are measured between 10% and 90% of the output waveform

typical performance characteristics

Output Voltage and Current-Limiting Characteristics



Line Drivers/Receivers

LM1489/LM1489A quad line receiver

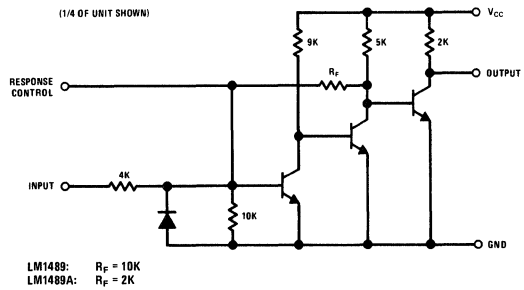
general description

The LM1489/LM1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C. The LM1489/LM1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements. The LM1489/LM1489A are available in 14 lead ceramic dual-in-line package.

features

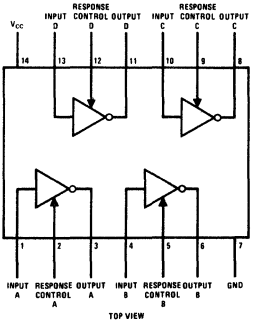
- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

schematic and connection diagrams



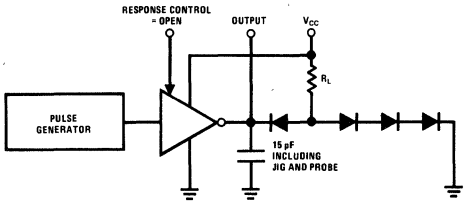
LM1489: R_F = 10K
LM1489A: R_F = 2K

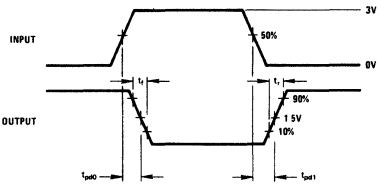
Dual-In-Line Package



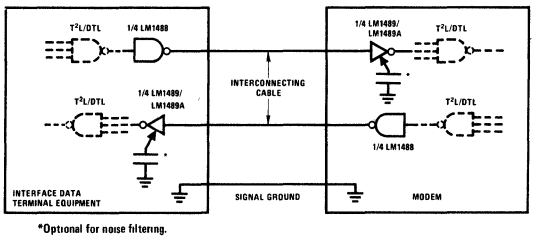
Order Number LM1489J or LM1489AJ
See Package 16

ac test circuit and voltage waveforms



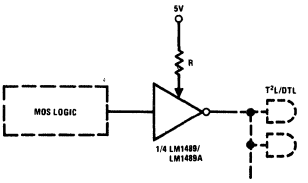


typical applications



*Optional for noise filtering.

RS232C Data Transmission



MOS to T^2L/DTL Translator

absolute maximum ratings (Note 1)

The following apply for $T_A = 25°C$ unless otherwise specified.

Power Supply Voltage	10V	Power Dissipation (Note 2)	1W
Input Voltage Range	±30V	Operating Temperature Range	0°C to +75°C
Output Load Current	20 mA	Storage Temperature Range	-65°C to +175°C

electrical characteristics (Note 3)

LM1489/LM1489A The following apply for $V_{CC} = 5.0V \pm 1\%$, $0°C \leq T_A \leq +75°C$ unless otherwise specified

PARAMETER	CONDITIONS	LM1489			LM1489A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input High Threshold Voltage	$T_A = 25°C$, $V_{OUT} \leq 0.45V$, $I_{OUT} = 10$ mA	1.0		1.5	1.75		2.25	V
Input Low Threshold Voltage	$T_A = 25°C$, $V_{OUT} \geq 2.5V$, $I_{OUT} = -0.5$ mA	0.75		1.25	0.75		1.25	V
Input Current	$V_{IN} = +25V$	+3.6	+5.6	+8.3	+3.6	+5.6	+8.3	mA
	$V_{IN} = -25V$	-3.6	-5.6	-8.3	-3.6	-5.6	-8.3	
	$V_{IN} = +3V$	+0.43	+0.53		+0.43	+0.53		mA
	$V_{IN} = -3V$	-0.43	-0.53		-0.43	-0.53		
Output High Voltage	$V_{IN} = 0.75V$, $I_{OUT} = -0.5$ mA	2.6	3.8	5.0	2.6	3.8	5.0	V
	Input = Open, $I_{OUT} = -0.5$ mA	2.6	3.8	5.0	2.6	3.8	5.0	V
Output Low Voltage	$V_{IN} = 3.0V$, $I_{OUT} = 10$ mA		0.33	0.45		0.33	0.45	V
Output Short Circuit Current	$V_{IN} = 0.75V$		3.0			3.0		mA
Supply Current	$V_{IN} = 5.0V$		14	26		14	26	mA
Power Dissipation	$V_{IN} = 5.0V$		70	130		70	130	mW
LM1489/LM1489A: The following apply for $V_{CC} = 5.0V \pm 1\%$, $T_A = 25°C$								
Input to Output "High" Propagation Delay (t_{pd1})	$R_L = 3.9k$ (Figure 1) (AC Test Circuit)		28	85		28	85	ns
Input to Output "Low" Propagation Delay (t_{pd0})	$R_L = 390\Omega$ (Figure 1) (AC Test Circuit)		20	50		20	50	ns
Output Rise Time	$R_L = 3.9k$ (Figure 1) (AC Test Circuit)		110	175		110	175	ns
Output Fall Time	$R_L = 390\Omega$ (Figure 1) (AC Test Circuit)		9	20		9	20	ns

Note 1: Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

Note 2: For operation at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 85°C/W junction to case.

Note 3: These specifications apply for response control pin = open.

Line Drivers/Receivers

LM55107A/LM75107A,LM55108A/LM75108A, LM163/LM363 dual line receivers LM75207,LM75208,LM363A dual MOS sense amplifiers

general description

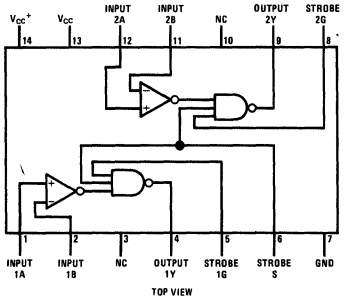
The nine products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers or MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the LM55109/LM75109 and LM55110/LM75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the LM75207, LM75208 and LM363A make them ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators. TRI-STATE® products enhance bused organizations.

features

- High speed 17 ns typ
- TTL compatible
- Input sensitivity ±10 mV or ±25 mV
- Input common-mode range ±3V
- High input impedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- TRI-STATE outputs for high speed buses
- Dual circuits
- Sensitivity guaranteed over full common-mode range
- Logic input clamp diodes
- 14 pin cavity or molded dual-in-line package
- Standard supply voltages ±5V

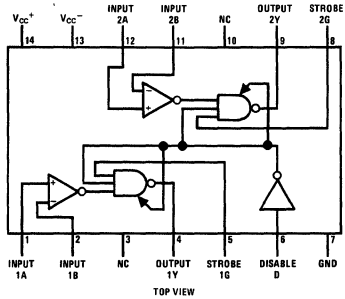
connection diagrams

Dual-In-Line Package



Order Number LM55107AF or LM55108AF
See Package 4
Order Number LM55107AJ, LM75107AJ, LM55108AJ, LM75108AJ, LM75207J or LM75208J
See Package 16
Order Number LM75107AN, LM75108AN, LM75207N or LM75208N
See Package 22

Dual-In-Line Package



Order Number LM163J, LM363J, or LM363AJ
See Package 16
Order Number LM363N or LM363AN
See Package 22

product selection guide

TEMPERATURE→ / PACKAGE→	$-55°C \leq T_A \leq +125°C$ CAVITY DIP	$0°C \leq T_A \leq +70°C$ CAVITY OR MOLDED DIP	
INPUT SENSITIVITY→ / OUTPUT LOGIC↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-up TTL Open Collector TTL TRI-STATE	LM55107A LM55108A LM163	LM75107A LM75108A LM363	LM75207 LM75208 LM363A

absolute maximum ratings

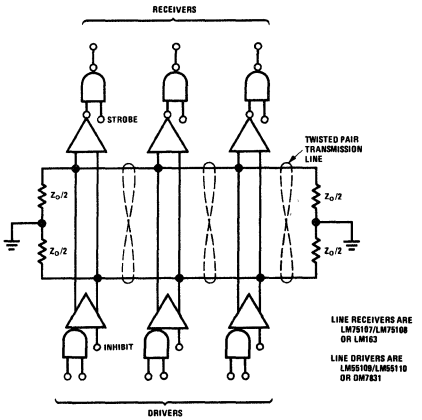
Supply Voltage, V_{CC}^+	7V	Strobe Input Voltage	5.5V
Supply Voltage, V_{CC}^-	−7V	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	±6V	Power Dissipation	600 mW
Common Mode Input Voltage	±5V	Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

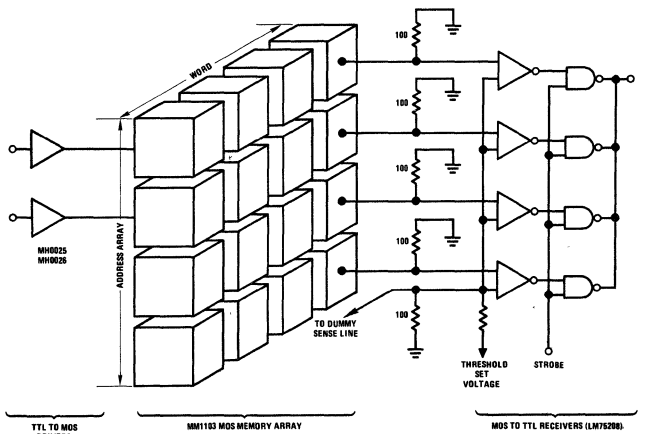
	LM55107A, LM55108A, LM163			LM75107A, LM75207 LM75108A, LM75208 LM363, LM363A		
	MIN	NOM	MAX	MIN	NOM	MAX
Supply Voltage V_{CC}^+	4 5V	5V	5.5V	4 75V	5V	5 25V
Supply Voltage V_{CC}^-	−4 5V	−5V	−5 5V	−4 75V	−5V	−5 25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

typical applications

Line Receiver Used in a Party-Line or Data-Bus System

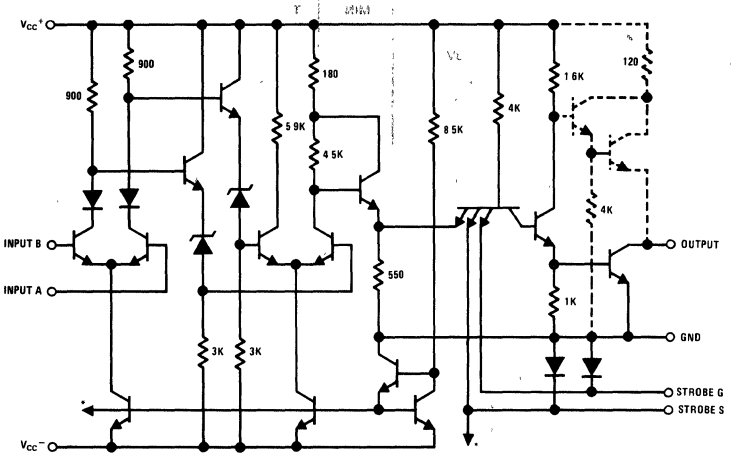


Line Receiver Used in MOS Memory System



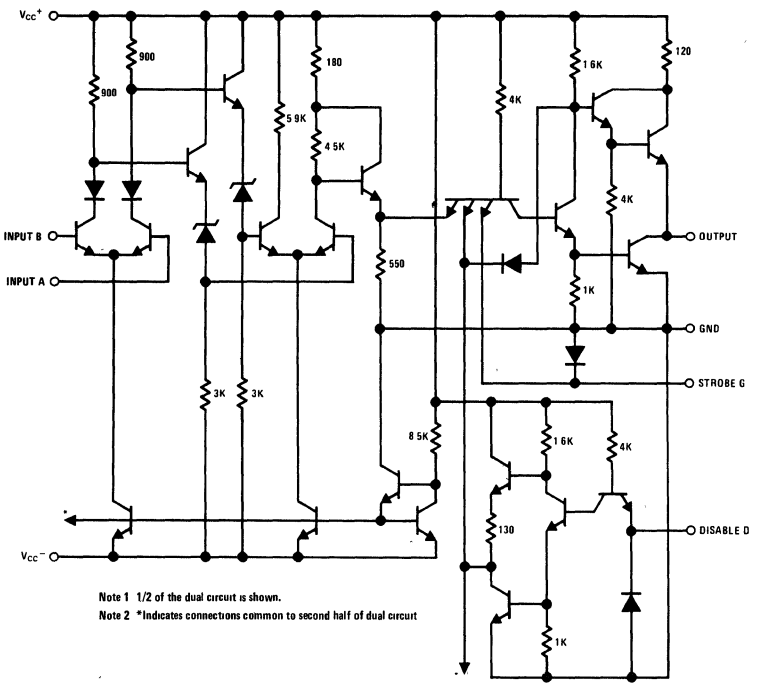
schematic diagrams

LM55107A/LM75107A, LM75207
LM55108A/LM75108A, LM75208



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit.
Note 3: Components shown with dash lines are applicable to the LM55107A, LM75107A, and LM75207 only.

LM163/LM363, LM363A



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit

LM55107A/LM75107A, LM55108A/LM75108A

dc electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55107A/LM75107A			LM55108A/LM75108A			
		MIN	TYP	MAX	MIN	TYP	MAX	
High Level Input Current Into 1A, 1B, 2A or 2B (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0 5V, V_{IC} = −3V to 3V		30	75		30	75	μA
Low Level Input Current Into 1A, 1B, 2A or 2B (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = −3V to 3V			−10			−10	μA
High Level Input Current Into 1G or 2G (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2 4V			40			40	μA
High Level Input Current Into 1G or 2G (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			1			1	mA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(S)}$ = 0 4V			−1 6			−1 6	mA
High Level Input Current Into S (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2 4V			80			80	μA
High Level Input Current Into S (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			2			2	mA
Low Level Input Current Into S (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(S)}$ = 0 4V			−3 2			−3 2	mA
High Level Output Voltage (V_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −400μA, V_{ID} = 25 mV, V_{IC} = −3V to 3V	2 4						V
Low Level Output Voltage (V_{OL})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, V_{IC} = −3V to 3V			0 4			0 4	V
High Level Output Current (I_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min V_{OH} = Max V_{CC}^+						250	μA
Short Circuit Output Current (I_{OS})	V_{CC}^+ = Max, V_{CC}^- = Max	−18		−70				mA
High Logic Level Supply Current From V_{CC} (I_{CCH}^+)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C		18	30		18	30	mA
High Logic Level Supply Current From V_{CC} (I_{CCH}^-)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C		−8 4	−15		−8 4	−15	mA
Input Clamp Voltage on G or S (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1 5		−1	−1 5	V

ac switching characteristics (V_{CC}^+ = 5V, V_{CC}^- = −5V, T_A = 25°C)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55107A/LM75107A			LM55108A/LM75108A			
		MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 390Ω, C_L = 50 pF		17	25				ns
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 390Ω, C_L = 15 pF					19	25	ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 390Ω, C_L = 50 pF		17	25				ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 390Ω, C_L = 15 pF					19	25	ns
Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output ($t_{PLH(S)}$)	R_L = 390Ω, C_L = 50 pF		10	15				ns
Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output ($t_{PLH(S)}$)	R_L = 390Ω, C_L = 15 pF					13	20	ns
Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output ($t_{PHL(S)}$)	R_L = 390Ω, C_L = 50 pF		8	15				ns
Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output ($t_{PHL(S)}$)	R_L = 390Ω, C_L = 15 pF					13	20	ns

Note 1: Differential input is +100 mV to -100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

LM75207, LM75208

dc electrical characteristics ($0°C \leq T_A \leq +70°C$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM75207			LM75208			
		MIN	TYP	MAX	MIN	TYP	MAX	
High Level Input Current Into 1A, 1B, 2A or 2B (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0 5V, V_{IC} = -3V to 3V		30	75		30	75	μA
Low Level Input Current Into 1A, 1B, 2A or 2B (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = -3V to 3V			−10			−10	μA
High Level Input Current Into 1G or 2G (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2 4V			40			40	μA
High Level Input Current Into 1G or 2G (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			1			1	mA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(S)}$ = 0 4V			−1 6			−1 6	mA
High Level Input Current Into S (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2 4V			80			80	μA
High Level Input Current Into S (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			2			2	mA
Low Level Input Current Into S (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(S)}$ = 0 4V			-3 2			−3 2	mA
High Level Output Voltage (V_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −400μA, V_{ID} = 10 mV, V_{IC} = −3V to 3V	2 4						V
Low Level Output Voltage (V_{OL})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, V_{IC} = −3V to 3V			0 4			0 4	V
High Level Output Current (I_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min V_{OH} = Max V_{CC}^+						250	μA
Short Circuit Output Current (I_{OS})	V_{CC}^+ = Max, V_{CC}^- = Max	−18		−70				mA
High Logic Level Supply Current From V_{CC} (I_{CCH}^+)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 10 mV, T_A = 25°C		18	30		18	30	mA
High Logic Level Supply Current From V_{CC} (I_{CCH}^-)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 10 mV, T_A = 25°C		−8 4	−15		−8 4	−15	mA
Input Clamp Voltage on G or S (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1 5		−1	−1 5	V

ac switching characteristics ($V_{CC}^+ = 5V$, $V_{CC}^- = -5V$, $T_A = 25°C$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM75207			LM75208			
		MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 470Ω, C_L = 15 pF			35				ns
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 470Ω, C_L = 15 pF						35	ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to output (Note 1) ($t_{PHL(D)}$)	R_L = 470Ω, C_L = 15 pF			20				ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 470Ω, C_L = 15 pF						20	ns
Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output ($t_{PLH(S)}$)	R_L = 470Ω, C_L = 15 pF			17				ns
Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output ($t_{PLH(S)}$)	R_L = 470Ω, C_L = 15 pF						17	ns
Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output ($t_{PHL(S)}$)	R_L = 470Ω, C_L = 15 pF			17				ns
Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output ($t_{PHL(S)}$)	R_L = 470Ω, C_L = 15 pF						17	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.

LM163/LM363

dc electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	LIMITS LM163/LM363 MIN	TYP	MAX	UNITS
High Level Input Current Into 1A, 1B, 2A or 2B (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0 5V, V_{IC} = −3V to 3V		30	75	μA
Low Level Input Current Into 1A, 1B, 2A or 2B (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = −3V to 3V			−10	μA
High Level Input Current Into 1G, 2G or D (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2 4V			40	μA
High Level Input Current Into 1G, 2G or D (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			1	mA
Low Level Input Current Into D (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0 4V			−1 6	mA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, $V_{IL(G)}$ = 0 4V			−40	μA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0 8V, $V_{IL(G)}$ = 0 4V			−1 6	mA
High Level Output Voltage (V_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −2 mA, V_{ID} = 25 mV, $V_{IL(D)}$ = 0 8V, V_{IC} = −3V to 3V	2 4			V
Low Level Output Voltage (V_{OL})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, $V_{IL(D)}$ = 0 8V, V_{IC} = −3V to 3V			0 4	V
Output Disable Current (I_{OD})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, V_{OUT} = 2 4V			40	μA
Output Disable Current (I_{OD})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, V_{OUT} = 0 4V			−40	μA
Short Circuit Output Current (I_{OS})	V_{CC}^+ = Max, $V_{IL(D)}$ = 0 8V, V_{CC}^- = Max	−18		−70	mA
High Logic Level Supply Current From V_{CC}^+ (I_{CCH}^+)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C		28	40	mA
High Logic Level Supply Current From V_{CC}^- (I_{CCH}^-)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C		−8 4	−15	mA
Input Clamp Voltage on G or D (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1 5	V

ac switching characteristics (V_{CC}^+ = 5V, V_{CC}^- = −5V, T_A = 25°C)

PARAMETER	CONDITIONS	LIMITS LM163/LM363 MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 390Ω, C_L = 50 pF		17	25	ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 390Ω, C_L = 50 pF		17	25	ns
Propagation Delay Time, Low to High Level, From Strobe Input G to Output ($t_{PLH(S)}$)	R_L = 390Ω, C_L = 50 pF		10	15	ns
Propagation Delay Time, High to Low Level, From Strobe Input G to Output ($t_{PHL(S)}$)	R_L = 390Ω, C_L = 50 pF		8	15	ns
Disable Low to High to Output High to Off (t_{1H})	R_L = 390Ω, C_L = 5 pF			20	ns
Disable Low to High to Output Low to Off (t_{0H})	R_L = 390Ω, C_L = 5 pF			30	ns
Disable High to Low to Output Off to High (t_{H1})	R_L = 1k to 0V, C_L = 50 pF			25	ns
Disable High to Low to Output Off to Low (t_{H0})	R_L = 390Ω C_L = 50 pF			25	ns

Note 1: Differential input is +100 mV to −100 mV pulse Delays read from 0 mV on input to 1 5V on output

LM363A
dc electrical characteristics ($0°C \leq T_A \leq +70°C$)

PARAMETER	CONDITIONS	LIMITS LM363A MIN	LIMITS LM363A TYP	LIMITS LM363A MAX	UNITS
High Level Input Current Into 1A, 1B, 2A or 2B (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0 5V, V_{IC} = −3V to 3V		30	75	μA
Low Level Input Current Into 1A, 1B, 2A or 2B (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = −3V to 3V			−10	μA
High Level Input Current Into 1G, 2G or D (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = 2 4V			40	μA
High Level Input Current Into 1G, 2G or D (I_{IH})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(S)}$ = Max V_{CC}^+			1	mA
Low Level Input Current Into D (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0 4V			−1 6	mA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, $V_{IL(G)}$ = 0 4V			−40	μA
Low Level Input Current Into 1G or 2G (I_{IL})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0 8V, $V_{IL(G)}$ = 0 4V			−1 6	mA
High Level Output Voltage (V_{OH})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −2 mA, V_{ID} = 10 mV, $V_{IL(D)}$ = 0 8V, V_{IC} = −3V to 3V	2 4			V
Low Level Output Voltage (V_{OL})	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, $V_{IL(D)}$ = 0 8V, V_{IC} = −3V to 3V			0 4	V
Output Disable Current (I_{OD})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, V_{OUT} = 2 4V			40	μA
Output Disable Current (I_{OD})	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V, V_{OUT} = 0 4V			−40	μA
Short Circuit Output Current (I_{OS})	V_{CC}^+ = Max, $V_{IL(D)}$ = 0 8V, V_{CC}^- = Max	−18		−70	mA
High Logic Level Supply Current From V_{CC}^+ (I_{CCH}^+)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 10 mV, T_A = 25°C		28	40	mA
High Logic Level Supply Current From V_{CC}^- (I_{CCH}^-)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 10 mV, T_A = 25°C		−8 4	−15	mA
Input Clamp Voltage on G or D (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1 5	V

ac switching characteristics ($V_{CC}^+ = 5V$, $V_{CC}^- = -5V$, $T_A = 25°C$)

PARAMETER	CONDITIONS	LIMITS LM363A MIN	LIMITS LM363A TYP	LIMITS LM363A MAX	UNITS
Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output (Note 1) ($t_{PLH(D)}$)	R_L = 470Ω, C_L = 15 pF			35	ns
Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output (Note 1) ($t_{PHL(D)}$)	R_L = 470Ω, C_L = 15 pF			20	ns
Propagation Delay Time, Low to High Level, From Strobe Input G to Output ($t_{PLH(S)}$)	R_L = 470Ω, C_L = 15 pF			17	ns
Propagation Delay Time, High to Low Level, From Strobe Input G to Output ($t_{PHL(S)}$)	R_L = 470Ω, C_L = 15 pF			17	ns
Disable Low to High to Output High to Off (t_{1H})	R_L = 470Ω, C_L = 5 pF			20	ns
Disable Low to High to Output Low to Off (t_{0H})	R_L = 470Ω, C_L = 5 pF			30	ns
Disable High to Low to Output Off to High (t_{H1})	R_L = 1k to 0V, C_L = 15 pF			25	ns
Disable High to Low to Output Off to Low (t_{H0})	R_L = 470Ω, C_L = 15 pF			25	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Line Drivers/Receivers

LM55109/LM75109, LM55110/LM75110 dual line drivers

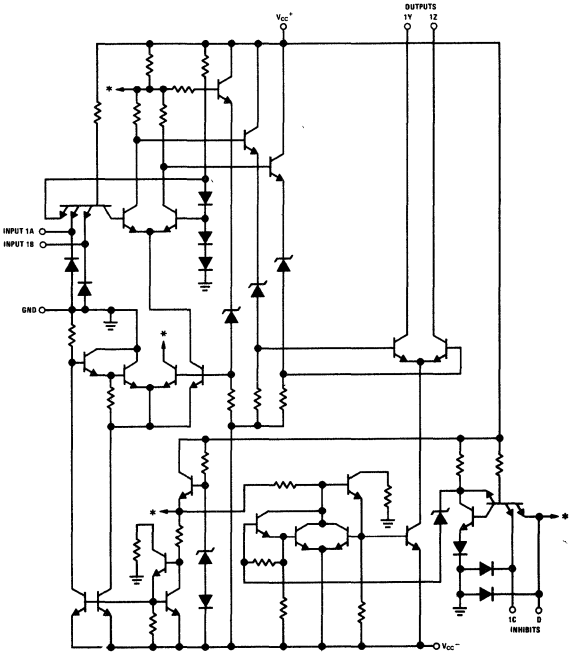
general description

These products are TTL compatible high speed differential line drivers intended for use in terminated twisted-pair party-line data transmission systems. They may also be used for level shifting since output common-mode range is −3V to +10V. An internal current sink is switched to either output dependent on input logic conditions. The current sink may be turned off by appropriate inhibit input conditions.

features

- Tightly controlled output currents over temperature, V_{CC}, and common-mode variations
- High speed 15 ns max
- Wide output common-mode range
- High output impedance
- Inhibits for party-line applications
- Current sink outputs 6 or 12 mA
- Dual circuits
- Standard supply voltages ±5V
- Input clamp diodes
- 14 pin cavity or molded DIP

schematic diagram

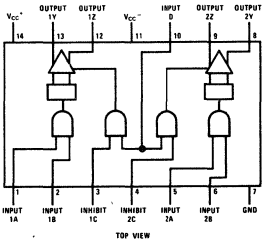


Note 1. 1/2 of the dual circuit shown

Note 2: *Indicates connections common to second half of circuit.

connection diagram

Dual-In-Line Package

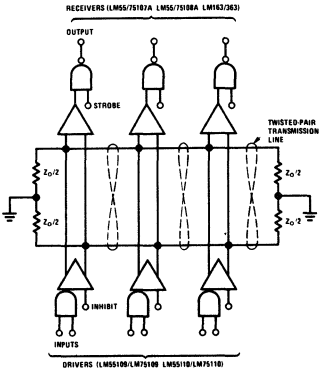


Order Number LM55109J, LM55110J, LM75109J, or LM75110J
See Package 16

Order Number LM75109N or LM75110N
See Package 22

typical application

Party-Line Data Transmission System



absolute maximum ratings

Supply Voltage, V_{CC}^+	7V
Supply Voltage, V_{CC}^-	−7V
Logic and Inhibitor Input Voltages	5 5V
Common-mode Output Voltage	−5V to 12V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	600 mW
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
LM55109, LM55110	4.5	5.5	V
LM75109, LM75110	4.75	5.25	V
Temperature (T_A)			
LM55109, LM55110	−55	+125	°C
LM75109, LM75110	0	+70	°C

dc electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55109/LM75109			LM55110/LM75110			
		MIN	TYP	MAX	MIN	TYP	MAX	
Positive Common Mode Output Voltage		0		10	0		10	V
Negative Common Mode Output Voltage		0		−3	0		−3	V
High Level Input Current Into 1A, 1B, 2A or 2B ($I_{IH(L)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(L)}$ = 2 4V			40			40	µA
High Level Input Current Into 1A, 1B, 2A or 2B ($I_{IH(L)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(L)}$ = Max V_{CC}^+			1			1	mA
Low Level Input Current Into 1A, 1B, 2A or 2B ($I_{IL(L)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(L)}$ = 0 4V			−3			−3	mA
High Level Input Current Into 1C or 2C ($I_{IH(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(I)}$ = 2 4V			40			40	µA
High Level Input Current Into 1C or 2C ($I_{IH(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(I)}$ = Max V_{CC}^+			1			1	mA
Low Level Input Current Into 1C or 2C ($I_{IL(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(I)}$ = 0 4V			−3			−3	mA
High Level Input Current Into D ($I_{IH(I)}$)	V_{CC}^+ = Max V_{CC}^- = Max, $V_{IH(I)}$ = 2 4V			80			80	µA
High Level Input Current Into D ($I_{IH(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(I)}$ = Max V_{CC}^+			2			2	mA
Low Level Input Current Into D ($I_{IL(I)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(I)}$ = 0 4V			−6			−6	mA
On State Output Current ($I_{O(ON)}$)	V_{CC}^+ = Max, V_{CC}^- = Max, V_{CC}^+ = Min, V_{CC}^- = Max	3 5		7	6 5		15	mA mA
Off State Output Current ($I_{O(OFF)}$)	V_{CC}^+ = Min, V_{CC}^- = Min			100			100	µA
Supply Current From V_{CC}^+ With Driver Enabled ($I_{CC^+(ON)}$)	$V_{IL(L)}$ = 0 4V, $V_{IH(I)}$ = 2V		18	30		23	35	mA
Supply Current From V_{CC}^- With Driver Enabled ($I_{CC^-(ON)}$)	$V_{IL(L)}$ = 0.4V, $V_{IH(I)}$ = 2V		−18	−30		−34	−50	mA
Supply Current From V_{CC}^+ With Driver Inhibited ($I_{CC^+(OFF)}$)	$V_{IL(L)}$ = 0.4V, $V_{IL(I)}$ = 0 4V		18			21		mA
Supply Current From V_{CC}^- With Driver Inhibited ($I_{CC^-(OFF)}$)	$V_{IL(L)}$ = 0.4V, $V_{IL(I)}$ = 0 4V		−10			−17		mA
Input Clamp Voltage on Inputs or Inhibits (V_I)	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C		−1	−1.5		−1	−1 5	V

ac switching characteristics ($V_{CC}^+ = 5V$, $V_{CC}^- = 5V$, $T_A = 25°C$)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM55109/LM75109			LM55110/LM75110			
		MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time, Low to High Level, From Logic Input A or B to Output Y or Z ($t_{PLH(L)}$)	$R_L = 50\Omega$, $C_L = 40$ pF		9	15		9	15	ns
Propagation Delay Time, High to Low Level, From Logic Input A or B to Output Y or Z ($t_{PHL(L)}$)	$R_L = 50\Omega$, $C_L = 40$ pF		9	15		9	15	ns
Propagation Delay Time, Low to High Level, From Inhibitor Input C or D to Output Y or Z ($t_{PLH(I)}$)	$R_L = 50\Omega$, $C_L = 40$ pF		16	25		16	25	ns
Propagation Delay Time, High to Low Level, From Inhibitor Input C or D to Output Y or Z ($t_{PHL(I)}$)	$R_L = 50\Omega$, $C_L = 40$ pF		13	25		13	25	ns

Line Drivers/Receivers

LM55121/LM75121 dual line drivers

general description

The LM55121/LM75121 are monolithic dual line drivers designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines having impedances from 50 to 500 ohms. Both are compatible with standard TTL logic and supply voltage levels.

The LM55121/LM75121 will drive terminated low impedance lines due to the low-impedance emitter-follower outputs. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

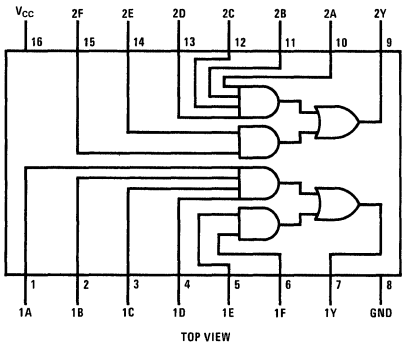
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

features

- Designed for digital data transmission over 50 to 500 ohms coaxial cable, strip line, or twisted pair transmission lines
- TTL compatible
- Open emitter-follower output structure for party-line operation
- Short-circuit protection
- AND-OR logic configuration
- High speed (max propagation delay time 20 ns)
- Plug-in replacement for the SN55121 and the 8T13

connection diagram

Dual-In-Line Package



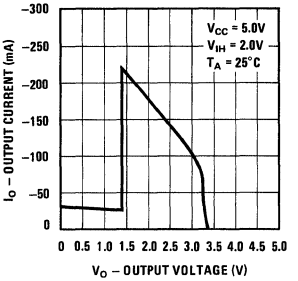
TOP VIEW

Order Number LM55121J or LM75121J
See Package 17

Order Number LM75121N
See Package 23

typical performance characteristics

Output Current vs Output Voltage

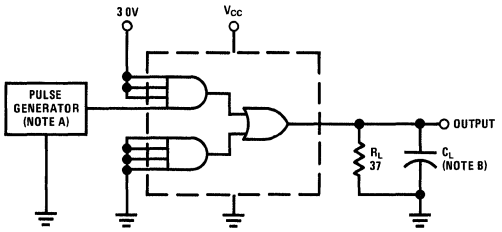


truth table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

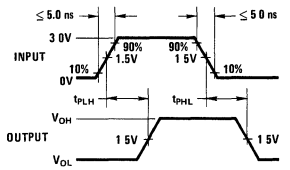
H = high level, L = low level, X = irrelevant

ac test circuit and switching time waveforms



Note A: The pulse generators have the following characteristics $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%, $t_r = t_f = 5.0$ ns

Note B: C_L includes probe and jig capacitance



absolute maximum ratings

(Notes 1 and 2)

Supply Voltage, V_{CC}	6.0V
Input Voltage	6.0V
Output Voltage	6.0V
Output Current	−75 mA
Continuous Total Dissipation at (or below) 25°C Free-Air Temperature (Note 5)	800 mW
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A			
LM55121	−55	+125	°C
LM75121	0	+75	°C

electrical characteristics (Note 3) V_{CC} = 4.75V to 5.25V (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})		2.0			V
Low Level Input Voltage (V_{IL})				0.8	V
Input Clamp Voltage (V_I)	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
Input Breakdown Voltage $V_{(BR)I}$	V_{CC} = 5.0V, I_I = 10 mA	5.5			V
High Level Output Voltage (V_{OH})	V_{IH} = 2.0V, I_{OH} = −75 mA (Note 4)	2.4			V
High Level Output Current (I_{OH})	V_{CC} = 5.0V, V_{IH} = 4.75V, V_{OH} = 2.0V, T_A = 25°C (Note 4)	−100		−250	mA
Low Level Output Current (I_{OL})	V_{IL} = 0.8V, V_{OL} = 0.4V (Note 4)			−800	μA
Off State Output Current ($I_{O(OFF)}$)	V_{CC} = 0V, V_O = 3.0V			500	μA
High Level Input Current (I_{IH})	V_I = 4.5V			40	μA
Low Level Input Current (I_{IL})	V_I = 0.4V	−0 1		−1 6	mA
Short Circuit Output Current (I_{OS})	V_{CC} = 5.0V, T_A = 25°C			−30	mA
Supply Current, Outputs High (I_{CCH})	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open			28	mA
Supply Current, Outputs Low (I_{CCL})	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open			60	mA

switching characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (t_{PLH})	R_L = 37Ω, C_L = 15 pF (See AC Test Circuit and Switching Time Waveforms)		11	20	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})			8 0	20	ns
Propagation Delay Time, Low to High Level Output (t_{PLH})	R_L = 37Ω, C_L = 1000 pF (See AC Test Circuit and Switching Time Waveforms)		22	50	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})			20	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for LM55121 and 0°C to +75°C for LM75121, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: For operating at elevated temperatures, the cavity DIP package (J) must be derated based on a thermal resistance of +85°C/W, junction to ambient. The molded DIP package (N) must be derated based on a thermal resistance of +150°C/W, junction to ambient.

Line Drivers/Receivers

LM55122/LM75122 triple line receivers

general description

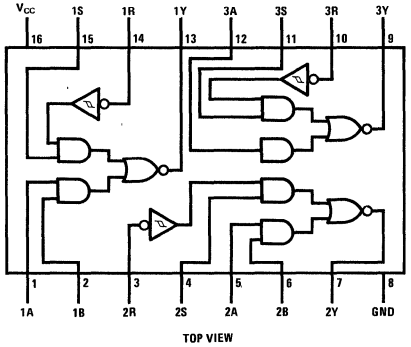
The LM55122/LM75122 are triple line receivers designed for digital data transmission with line impedances from 50Ω to 500Ω. Each receiver has one input with built-in hysteresis which provides a large noise margin. The other inputs on each receiver are in a standard TTL configuration. The LM55122/LM75122 are compatible with standard TTL logic and supply voltage levels.

features

- Built-in input threshold hysteresis
- High speed . . . typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Fanout to 10 series 54/74 standard loads
- Plug-in replacement for the SN55122 and the 8T14

connection diagram

Dual-In-Line Package



TOP VIEW

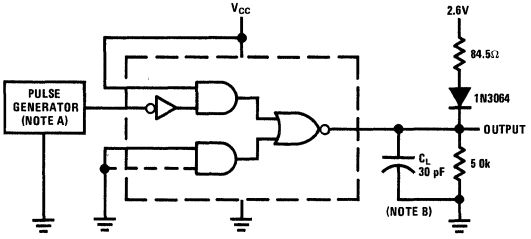
Order Number LM55122J, LM75122J
See Package 17
Order Number LM75122N
See Package 23

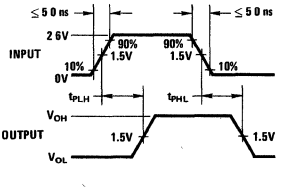
truth table

INPUTS A	INPUTS B†	INPUTS R	INPUTS S	OUTPUT Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant
†B input and last two lines of the truth table are applicable to receivers 1 and 2 only

ac test circuit and switching time waveforms





Note A. The pulse generator has the following characteristics $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%, $t_r = t_f = 5.0$ ns.
Note B C_L includes probe and jig capacitance

absolute maximum ratings

(Notes 1 and 2)

Supply Voltage, V_{CC}	6.0V
Input Voltage	
R Input	6.0V
A, B, or S Input	5.5V
Output Voltage	6.0V
Output Current	±100 mA
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (Note 5)	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A			
LM55122	−55	+125	°C
LM75122	0	+75	°C
High Level Output Current, I_{OH}		−500	μA
Low Level Output Current, I_{OL}		16	mA

electrical characteristics (Note 3) V_{CC} = 4.75V to 5.25V (unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})					
A, B, R, or S		2.0			V
Low Level Input Voltage (V_{IL})					
A, B, R, or S				0.8	V
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V, T_A = 25°C				
R	(Note 7)	0.3	0.6		V
Input Clamp Voltage (V_I)					
A, B, or S	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
Input Breakdown Voltage ($V_{(BR)I}$)					
A, B, or S	V_{CC} = 5.0V, I_I = 10 mA	5.5			V
High Level Output Voltage (V_{OH})	V_{IH} = 0V, V_{IL} = 0.8V, I_{OH} = −500μA, (Note 4)	2.6			V
	$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(S)}$ = 2.0V, $V_{I(R)}$ = 1.45V, (Note 8), I_{OH} = −500μA	2.6			V
Low Level Output Voltage (V_{OL})	V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 16 mA, (Note 4)			0.4	V
	$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(S)}$ = 2.0V, $V_{I(R)}$ = 1.45V, (Note 9), I_{OL} = 16 mA			0.4	V
High Level Input Current (I_{IH})					
A, B, or S	V_I = 4.5V			40	μA
R	V_I = 3.8V			170	μA
Low Level Input Current (I_{IL})					
A, B, or S	V_I = 0.4V	−0.1		−1.6	mA
Short Circuit Output Current (I_{OS})	V_{CC} = 5.0V, T_A = 25°C, (Note 6)	−50		−100	mA
Supply Current (I_{CC})	V_{CC} = 5.25V			72	mA

switching characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output from R Input (t_{PLH})	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns
Propagation Delay Time, High to Low Level Output from R Input (t_{PHL})			20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for LM55122 and 0°C to +75°C for LM75122, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: For operating at elevated temperatures, the cavity DIP package (J) has a maximum junction temperature of +150°C and must be derated based on a thermal resistance of +85°C/W, junction to ambient. The molded DIP package (N) has a maximum junction temperature of +150°C and must be derated based on a thermal resistance of +150°C/W, junction to ambient.

Note 6: Not more than one output should be shorted at a time.

Note 7: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

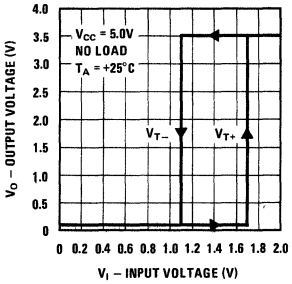
Note 8: Receiver input was at a high level immediately before being reduced to 1.45V.

Note 9: Receiver input was at a low level immediately before being raised to 1.45V.

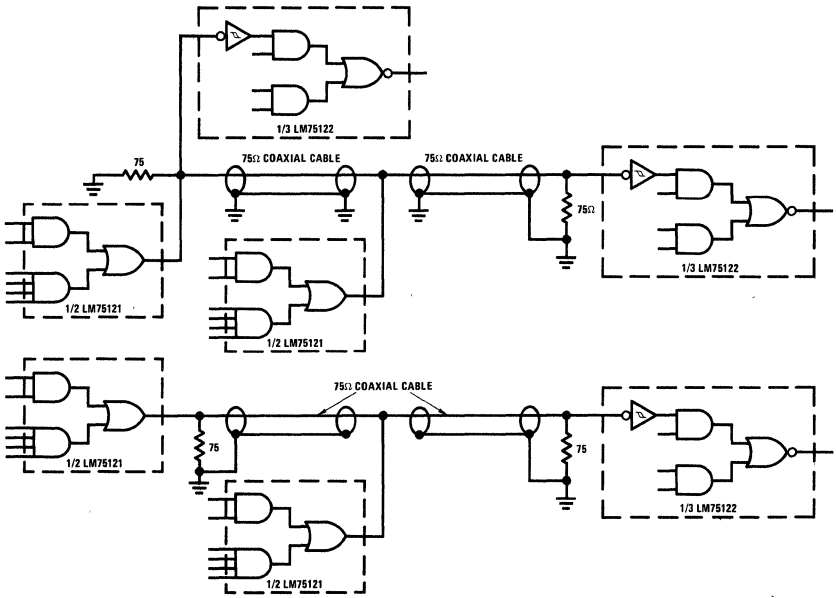
4

typical performance characteristics

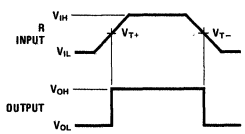
Output Voltage vs Receiver Input Voltage



typical applications



Single-Ended Party Line Circuits



THE HIGH GAIN AND BUILT IN HYSTERESIS OF THE LM55122/ LM75122 LINE RECEIVERS ENABLE THEM TO BE USED AS SCHMITT TRIGGERS IN SQUARING UP PULSES

Pulse Squaring

Line Drivers/Receivers

LM75123 dual line driver

general description

The LM75123 is a monolithic dual line driver designed specifically to meet the I/O interface specifications for IBM System 360. It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the LM75123 enable driving terminated low impedance lines. In addition the outputs are uncommited allowing two or more drivers to drive the same line.

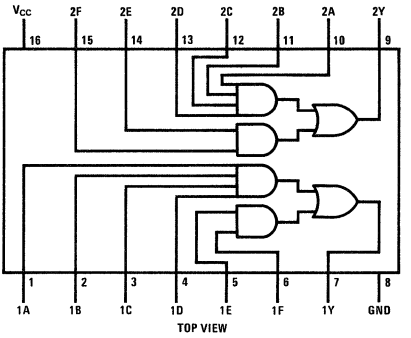
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

features

- Meet IBM System 360 I/O interface specifications for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or terminated pair transmission lines
- TTL compatible with single 5.0V supply
- 3.11V output at I_{OH} = −59.3 mA
- Open emitter-follower output structure for party-line operation
- Short circuit protection
- AND-OR logic configuration
- Plug-in replacement for the SN75123 and the 8T23

connection diagram

Dual-In-Line Package

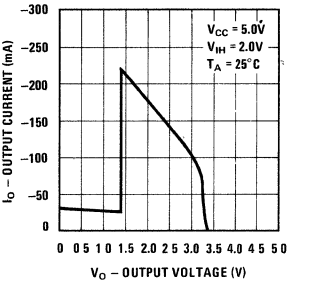


Order Number LM75123J
See Package 17

Order Number LM75123N
See Package 23

typical performance characteristics

Output Current vs Output Voltage

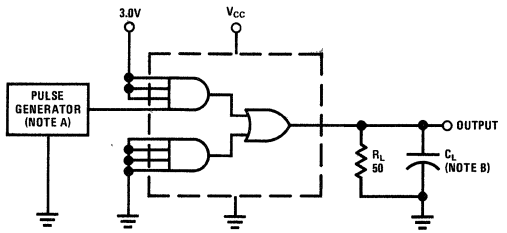


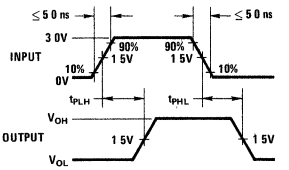
truth table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = high level, L = low level, X = irrelevant

ac test circuit and switching time waveforms





NOTE A. THE PULSE GENERATORS HAVE THE FOLLOWING CHARACTERISTICS $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, DUTY CYCLE = 50%

NOTE B C_L INCLUDES PROBE AND JIG CAPACITANCE

absolute maximum ratings
(Notes 1 and 2)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	7.0V
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (Note 5)	800 mW
Operating Free-Air Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−100	mA
Temperature, T_A	0	+75	°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})		2.0			V
Low Level Input Voltage (V_{IL})				0.8	V
Input Clamp Voltage (V_I)	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
Input Breakdown Voltage ($V_{(BR)I}$)	V_{CC} = 5.0V, I_I = 10 mA	5.5			V
High Level Output Voltage (V_{OH})	V_{CC} = 5.0V, V_{IH} = 2.0V, I_{OH} = −59.3 mA, (Note 4)				
	T_A = 25°C	3.11			V
	T_A = 0°C to +75°C	2.9			V
High Level Output Current (I_{OH})	V_{CC} = 5.0V, V_{IH} = 4.5V, T_A = 25°C, (Note 4) V_{OH} = 2.0V	−100		−250	mA
Low Level Output Voltage (V_{OL})	V_{IL} = 0.8V, I_{OL} = −240μA, (Note 4)			0.15	V
Off State Output Current ($I_{O\ OFF}$)	V_{CC} = 0, V_O = 3.0V			40	μA
High Level Input Current (I_{IH})	V_I = 4.5V			40	μA
Low Level Input Current (I_{IL})	V_I = 0.4V	−0 1		−1.6	mA
Short Circuit Output Current (I_{OS})	V_{CC} = 5.0V, T_A = 25°C			−30	mA
Supply Current, Outputs High (I_{CCH})	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open			28	mA
Supply Current, Outputs Low (I_{CCL})	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open			60	mA

switching characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (t_{PLH})	R_L = 50Ω, C_L = 15 pF (See AC Test Circuit and Switching Time Waveforms)		12	20	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})			12	20	ns
Propagation Delay Time, Low to High Level Output (t_{PLH})	R_L = 50Ω, C_L = 100 pF (See AC Test Circuit and Switching Time Waveforms)		20	35	ns
Propagation Delay Time, High to Low Level Output (t_{PHL})			15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for LM75123, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: For operating at elevated temperatures, the cavity DIP package (J) has a maximum junction temperature of +150°C and must be derated based on a thermal resistance of +85°C/W, junction to ambient. The molded DIP package (N) has a maximum junction temperature of +150°C and must be derated based on a thermal resistance of +150°C/W, junction to ambient.

Line Drivers/Receivers

LM75124 triple line receivers

general description

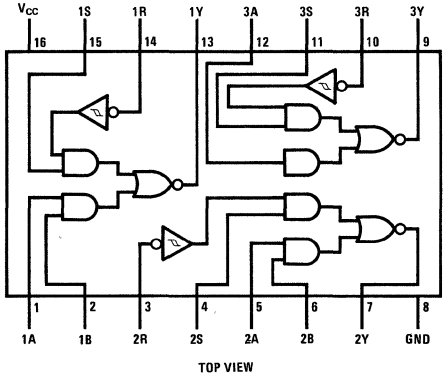
The LM75124 is designed to meet the input/output interface specifications for IBM System 360. It has built-in hysteresis on one input on each of the three receivers to provide large noise margin. The other inputs on each receiver are in a standard TTL configuration. The LM75124 is compatible with standard TTL logic and supply voltage levels.

features

- Built-in input threshold hysteresis
- High speed . . typ propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Plug-in replacement for the SN75124 and the 8T24

connection diagram and truth table

Dual-In-Line Package



TOP VIEW

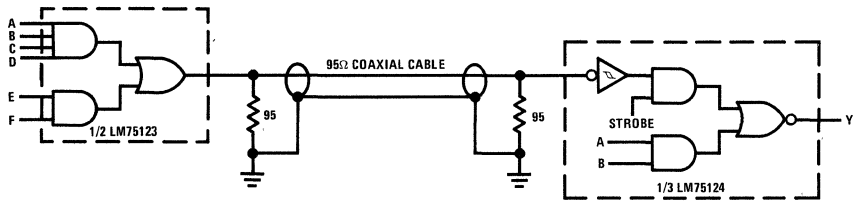
INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant
†B input and last two lines of the truth table are applicable to receivers 1 and 2 only

Order Number LM75124J
See Package 17

Order Number LM75124N
See Package 23

typical application



absolute maximum ratings

(Notes 1 and 2)

Supply Voltage, V_{CC}	7.0V
Input Voltage	
R Input with V_{CC} Applied	7.0V
R Input with V_{CC} not Applied	6.0V
A, B, or S Input	5.5V
Output Voltage	7.0V
Output Current	±100 mA
Continuous Total Power Dissipation at (or below) 25°C Free-Air Temperature (Note 5)	800 mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−800	μA
Low Level Output Current, I_{OL}		16	mA
Operating Temperature, T_A	0	+75	°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High Level Input Voltage (V_{IH})					
A, B, or S		2.0			V
R		1.7			V
Low Level Input Voltage (V_{IL})					
A, B, or S				0.8	V
R				0.7	V
Hysteresis ($V_{T+} - V_{T-}$)	(Note 7)				
R	V_{CC} = 5.0V, T_A = 25°C	0.2	0.4		V
Input Clamp Voltage (V_I)					
A, B, or S	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
Input Breakdown Voltage ($V_{(BR)I}$)					
A, B, or S	V_{CC} = 5.0V, I_I = 10 mA	5.5			V
High Level Output Voltage (V_{OH})	$V_{IH} = V_{IH\,MIN}$, $V_{IL} = V_{IL\,MAX}$, I_{OH} = −800μA (Note 4)	2.6			V
Low Level Output Voltage (V_{OL})	$V_{IH} = V_{IN\,MIN}$, $V_{IL} = V_{IL\,MAX}$, I_{OL} = 16 mA (Note 4)			0.4	V
Input Current at Maximum Input Voltage (I_I) R	V_I = 7.0V			5.0	mA
	V_I = 6.0V, V_{CC} = 0			5.0	mA
High Level Input Current (I_{IH})					
A, B, or S	V_I = 4.5V			40	μA
R	V_I = 3.11V			170	μA
Low Level Input Current (I_{IL})					
A, B, or S	V_I = 0.4V	−0.1		−1.6	mA
Short Circuit Output Current (I_{OS})	V_{CC} = 5.0V, T_A = 25°C, (Note 6)	−50		−100	mA
Supply Current (I_{CC})	V_{CC} = 5.25V			72	mA

switching characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output from R Input (t_{PLH})	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns
Propagation Delay Time, High to Low Level Output from R Input (t_{PHL})			20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for LM75124, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

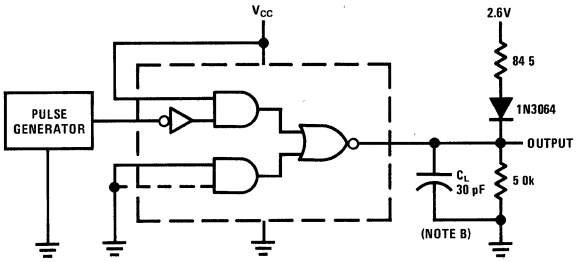
Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: For operating at elevated temperatures, the cavity DIP package (J) must be derated based on a thermal resistance of +85°C/W, junction to ambient. The molded DIP package (N) must be derated based on a thermal resistance of +150°C/W, junction to ambient.

Note 6: Note more than one output should be shorted at a time.

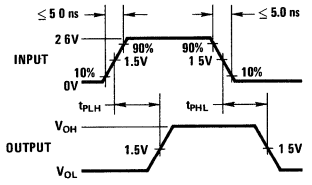
Note 7: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

ac test circuit and switching time waveforms

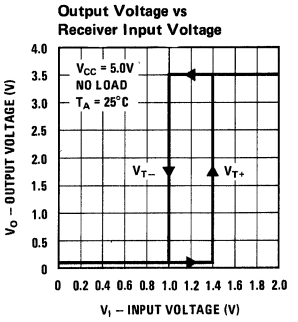


NOTE A. THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, DUTY CYCLE = 50%.

NOTE B C_L INCLUDES PROBE AND JIG CAPACITANCE.



typical performance characteristics



Peripheral/Power Drivers

DH0006/DH0006C*current driver

general description

The DH0006/DH0006C is an integrated high voltage, high current driver designed to accept standard DTL or TTL logic levels and drive a load of up to 400 mA at 28 volts. AND inputs are provided along with an Expander connection, should additional gating be required. The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are driven.

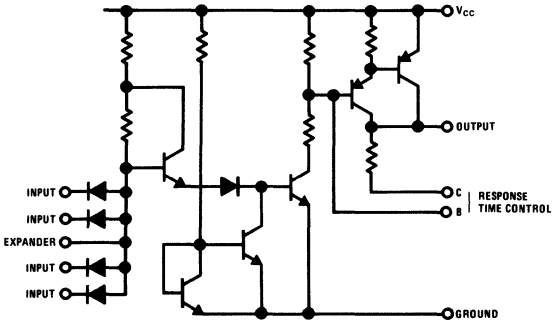
Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

*Previously called NH0006/NH0006C

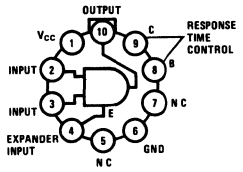
features

- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply.
- 1.5A, 50 ms, Pulse Current Capability.

schematic and connection diagrams



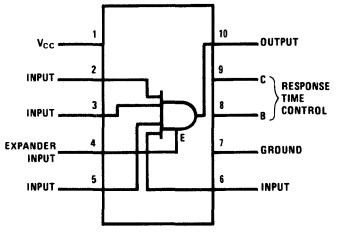
Metal Can Package



TOP VIEW

Order Number DH0006H or DH0006CH
See Package 13

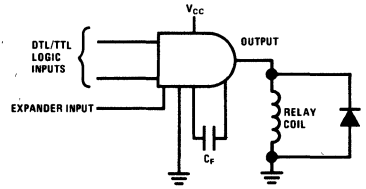
Dual-In-Line Package



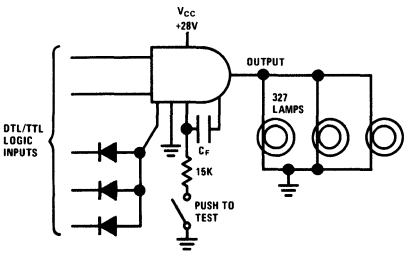
Order Number DH0006CN
See Package 21

typical applications

Relay Driver



Lamp Driver with Expanded Inputs



absolute maximum ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current (50 ms On/1 sec Off)	1.5A
Operating Temperature	
DH0006	−55°C to +125°C
DH0006C, DH0006CN	0°C to +70°C
Storage Temperature	−65°C to +150°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 400 mA	26.5	27.0		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1K		.001	.01	V
Logical "1" Output Voltage	V_{CC} = 10V, V_{IN} = 2.0V, I_{OUT} = 150 mA	8.8	9.2		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = .4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0.8V		1.6	2.0	mA
"On" Power Supply Current	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 0 mA			8	mA
Rise Time	V_{CC} = 28V, R_L = 82Ω		0.10		μs
Fall Time	V_{CC} = 28V, R_L = 82Ω		0.8		μs
T_{on}	V_{CC} = 28V, R_L = 82Ω		0.26		μs
T_{off}	V_{CC} = 28V, R_L = 82Ω		2.2		μs

Note 1: Unless otherwise specified, limits shown apply from −55°C to 125°C for **DH0006** and 0°C to 70°C for DH0006C.

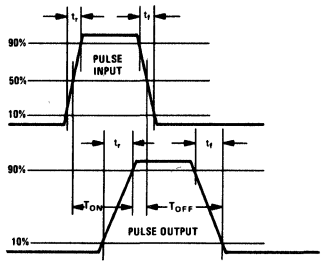
Note 2: Typical values are for 25°C ambient.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a ϕ_{JA} of 210°C/W

Note 4: Power rating for the **DH0006CN** Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 175°C/W when mounted in a standard DIP socket

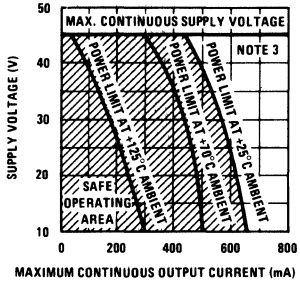
Note 5: Power rating for the **DH0006CN** Molded DIP based on a maximum junction temperature of +150°C and a thermal resistance of 150°C/W when mounted on a 1/16 inch thick, epoxy-glass board with ten 0 03 inch wide 2 ounce copper conductors.

switching time waveforms

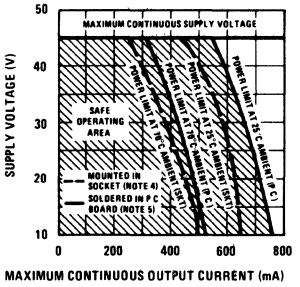


typical performance

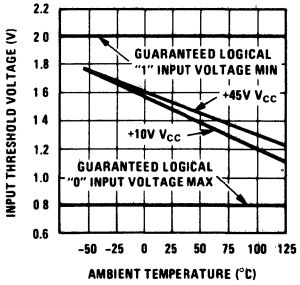
Maximum Continuous Output Current For TO-5



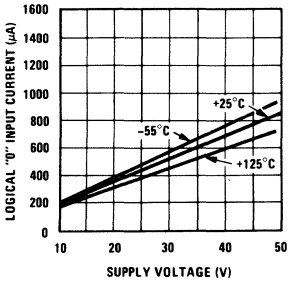
Maximum Continuous Output Current For Molded DIP



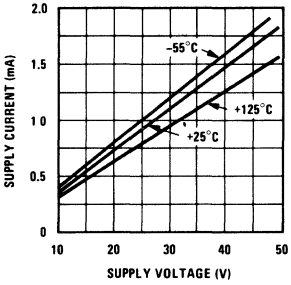
Input Threshold Voltage vs Temperature



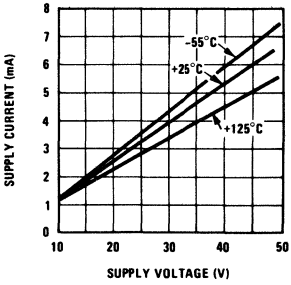
Logical "0" Input Current



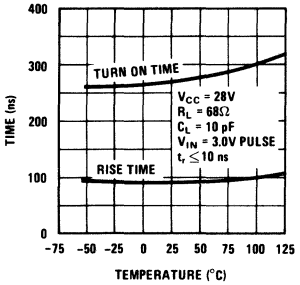
"OFF" Supply Current Drain



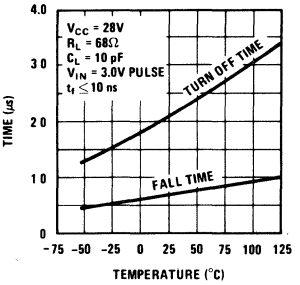
"ON" Supply Current Drain



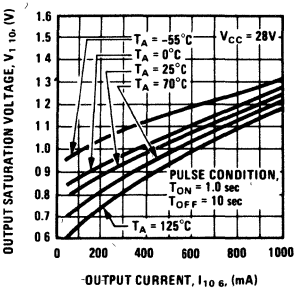
Turn On And Rise Time



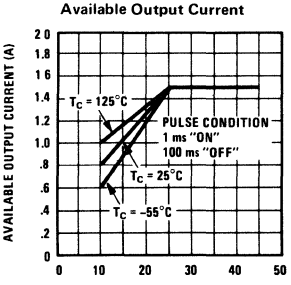
Turn Off and Fall Time



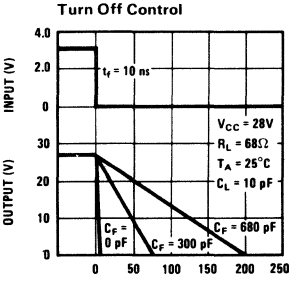
Output Saturation Voltage



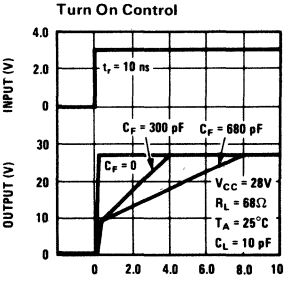
Available Output Current



Turn Off Control



Turn On Control



5

Peripheral/Power Drivers

DH0008/DH0008C*
high voltage, high current driver

general description

The DH0008/DH0008C is an integrated high voltage, high current driver, designed to accept standard DTL or TTL input levels and provide a pulsed load of up to 3A from a continuous supply voltage up to 45V. AND inputs are provided with an EXPANDER connection, should additional gating be required.

Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

The high pulse current capability makes the DH0008/DH0008C ideal for driving nonlinear resistive loads such as incandescent lamps. The

*Previously called NH0008/NH0008C

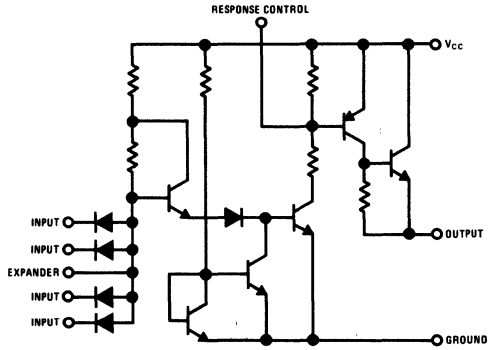
circuit also requires only one power supply for circuit functional operation.

The DH0008 is available in a 10-pin TO-5 package; the DH0008C is also available in a 10-pin TO-5, in addition to a 10-lead molded dual-in-line package.

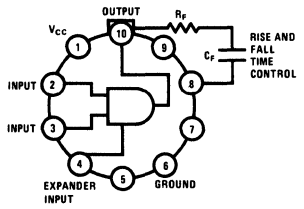
features

- Operation from a Single +10V to +45V Power Supply.
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply.
- 3.0A, 50 ms, Pulse Current Capability.

schematic and connection diagrams

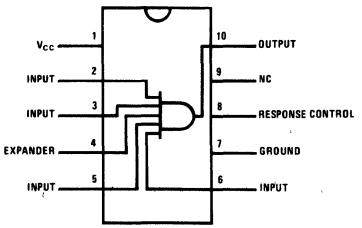


Metal Can Package



Order Number DH0008H or DH0008CH
See Package 13

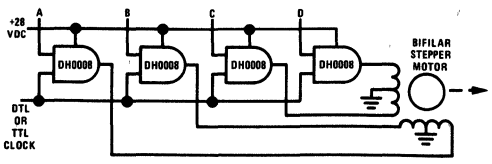
Dual-In-Line Package



Order Number DH0008CN
See Package 21

typical application

Controller for Closed Loop Stepper Motor



Switching Sequence

Step	A	B	C	D
1	1	0	1	0
2	1	0	0	1
3	0	1	0	1
4	0	1	1	0
1	1	0	1	0

To reverse the direction use a 4, 3, 2, 1 sequence

absolute maximum ratings

Peak Power Supply Voltage (for 0.1 sec)	60V
Continuous Supply Voltage	45V
Input Voltage	5.5V
Input Extender Current	5.0 mA
Peak Output Current	
(50 msec On/1 sec Off)	3.0 Amp
Continuous Output Current	
(See continuous operating curves.)	
Operating Temperature	
DH0008	−55°C to +125°C
DH0008C	0°C to +70°C
Storage Temperature	−65°C to +150°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 45V to 10V	2.0			V
Logical "0" Input Voltage	V_{CC} = 45V to 10V			0.8	V
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2.0V, I_{OUT} = 1.6A 50 ms On/1 sec Off	43	43.5		V
Logical "0" Output Voltage	V_{CC} = 45V, V_{IN} = 0.8V, R_L = 1K		0.02	0.1	V
Logical "1" Output Voltage	V_{CC} = 28V, V_{IN} = 2.0V, I_{OUT} = 0.8A 50 ms On/1 sec Off	26.5	27.1		V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0.4V		−0.8	−1.0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2.4V		0.5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5.5V			100	μA
"Off" Power Supply Current	V_{CC} = 45V, V_{IN} = 0V		1.6	2.0	mA
Rise Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.2		μs
Fall Time	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		3.0		μs
T_{ON}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		0.4		μs
T_{OFF}	V_{CC} = 28V, R_L = 39Ω, V_{IN} = 5.0V		7.0		μs

Note 1: Unless otherwise specified limits shown apply from −55°C to 125°C for **DH0008** and 0°C to 70°C for **DH0008C.**

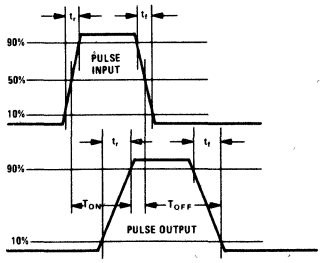
Note 2: Typical values are 25°C ambient

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and a ϕ JA of 210°C/w

Note 4: Power ratings for the **DH0008CN** Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 150°C/w when mounted in a standard DIP socket

Note 5: Power ratings for the **DH0008CN** Molded DIP based on a maximum junction temperature of 150°C and a thermal resistance of 115°C/w when mounted on a 1/16 inch thick, epoxy-glass board with ten 0.03 inch wide 2 ounce copper conductors.

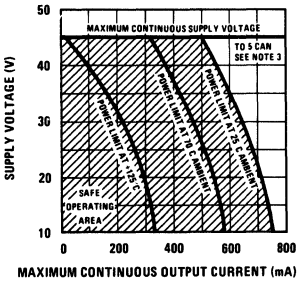
switching time waveforms



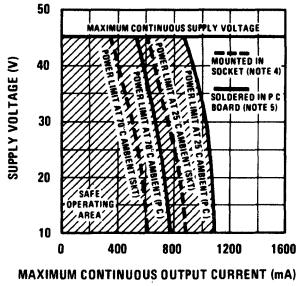
5

typical performance

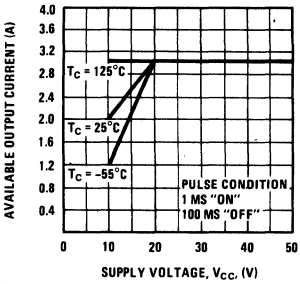
Maximum Continuous Output Current for TO-5 Package



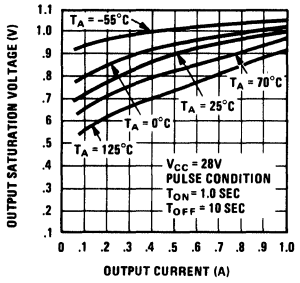
Maximum Continuous Output Current for Molded DIP



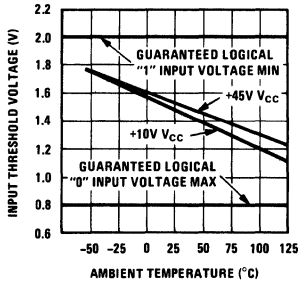
Available Output Current



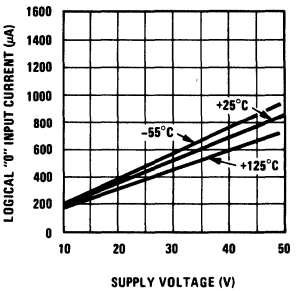
Output Saturation Voltage



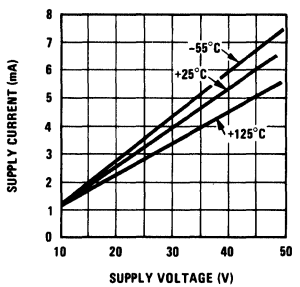
Input Threshold Voltage vs Temperature



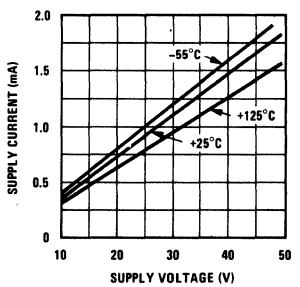
Logical "0" Input Current



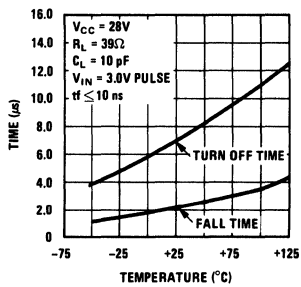
ON Supply Current Drain



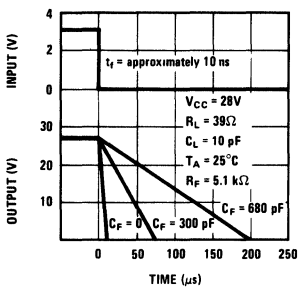
OFF Supply Current Drain



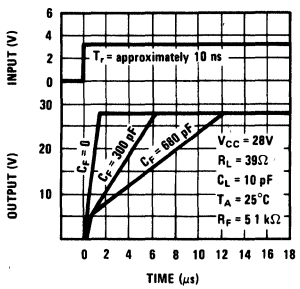
Turn OFF and Fall Times



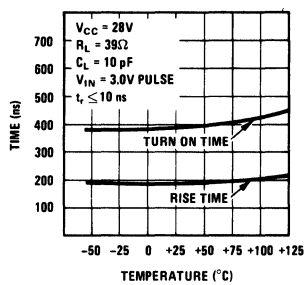
Turn ON Control



Turn OFF Control



Turn ON and Rise Time



Peripheral/Power Drivers

DH0011*(SH2001)
DH0011C*(SH2002)
DH0011CN*(SH2002P)

high voltage high current drivers

general description

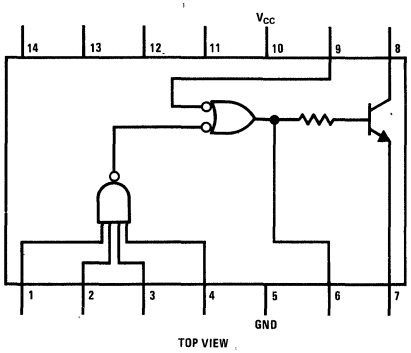
The DH0011 high voltage, high current driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability. A summary of the variations is listed below.

Applications include driving lamps, relays, cores, and other devices requiring several hundred milliamp currents at voltages up to 40V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects the base of the output transistor.

*Previously called NH0011, NH0011C, NH0011CN

logic diagram

Dual-In-Line Package*



TOP VIEW

ordering information

NSC DESIGNATION	SH DESIGNATION	SEE PACKAGE	TEMPERATURE RANGE	OUTPUT CURRENT CAPABILITY
DH0011H	SH2001	12	−55°C to +125°C	250 mA
DH0011CH	SH2002	12	0°C to +70°C	150 mA
DH0011CN	SH2002P	22	0°C to +70°C	150 mA

*Metal can pin numbers are the same as the dual-in-line pin numbers.

absolute maximum ratings

V_{CC}		8V
Collector Voltage (Output)		40V
Input Reverse Current		1.0 mA
Power Dissipation		800 mW
Operating Temperature Range	DH0011H	−55°C to +125°C
	DH0011CH/DH0011CN	0°C to +70°C
Storage Temperature		−65°C to 150°C

electrical characteristics

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	MIN	MAX
1	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CCL}	V_8		V_{OL}
2	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CCL}	V_8		V_{OL}
3	V_{IL}				GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
4		V_{IL}			GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
5			V_{IL}		GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
6				V_{IL}	GND	I_{OL2}				V_{CCL}	V_6		V_{OL2}
7				GND	GND	I_{OL2}			V_{IH}	V_{CCL}	V_6		V_{OL2}
8	V_R	GND	GND	GND	GND					V_{CCH}	I_1		I_R
9	GND	V_R	GND	GND	GND					V_{CCH}	I_2		I_R
10	GND	GND	V_R	GND	GND					V_{CCH}	I_3		I_R
11	GND	GND	GND	V_R	GND					V_{CCH}	I_4		I_R
12					GND				V_R	V_{CCH}	I_9		I_R
13	V_F	V_R	V_R	V_R	GND					V_{CCH}	I_1		$-I_F$
14	V_R	V_F	V_R	V_R	GND					V_{CCH}	I_2		$-I_F$
15	V_R	V_R	V_F	V_R	GND					V_{CCH}	I_3		$-I_F$
16	V_R	V_R	V_R	V_F	GND					V_{CCH}	I_4		$-I_F$
17				GND	GND				V_F	V_{CCH}	I_9		$-I_F$
18					GND		GND			V_{CCL}	V_6	V_{OH}	
19	GND				GND		GND	V_{OX}		V_{CCL}	I_8		I_{OX}
20					GND		GND			V_{PD}	I_{10}		I_{PDH}
21	GND				GND					V_{MAX}	I_{10}		I_{MAX}
22*					GND					V_{PD}			t_{ON}
23*					GND					V_{PD}			t_{OFF}

*See Test Circuits and Waveforms on Page 4.

forcing functions (Note 1) DH0011

PARAMETER	−55°C	+25°C	+125°C	UNITS
V_{CCL}	4.5	4.5	4.5	V
V_{CCH}	5.5	5.5	5.5	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.4	1.1	0.8	V
V_{IH}	2.1	1.9	1.7	V
V_R	4.0	4.0	4.0	V
V_F	0.0	0.0	0.0	V
I_{OL1}	250	250	250	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.0	40.0	40.0	V

Note 1: Temperature Range −55°C to +125°C

forcing functions (Note 2) DH0011C, DH0011CN

PARAMETER	0°C	+25°C	+70°C	UNITS
V_{CCL}	5.00	5.0	5.0	V
V_{CCH}	5.00	5.0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	1.20	1.1	.95	V
V_{IH}	2.00	1.9	1.8	V
V_R	4.00	4.0	4.0	V
V_F	0.45	0.45	0.5	V
I_{OL1}	150	150	150	mA
I_{OL2}	8.0	8.0	7.5	mA
V_{OX}	40.00	40.0	40.0	V

test limits (Note 1) DH0011

PARAMETER	-55°C		+25°C		+125°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.4		0.45	V
V_{OL2}		0.45		0.4		0.45	V
V_{OH}	2.20		2.00		1.80		V
I_R				2.0		5.0	μA
$-I_F$		1.60		1.6		1.5	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				29.6			mA
t_{ON}				160			ns
t_{OFF}				220			ns

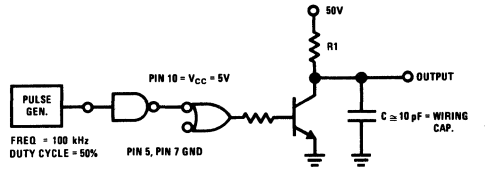
test limits (Note 2) DH0011C, DH0011CN

PARAMETER	0°C		+25°C		+70°C		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OL1}		0.45		0.45		0.5	V
V_{OL2}		0.45		0.45		0.5	V
V_{OH}	2.05		1.95		1.85		V
I_R				5.0		10.0	μA
$-I_F$		1.40		1.4		1.35	mA
I_{OX}				5.0		200	μA
I_{PDH}				30.6			mA
I_{MAX}				34.0			mA

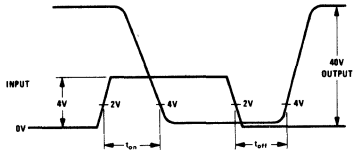
Note 1: Temperature Range −55°C to +125°C

Note 2: Temperature Range 0°C to +70°C

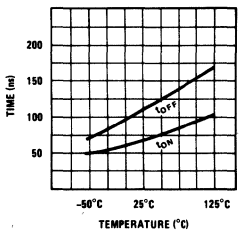
switching time test circuit



switching time waveforms



Typical Switching Times



5

Peripheral/Power Drivers

DH0016CN*
DH0017CN*(SH2200P)
DH0018CN*

high voltage high current drivers

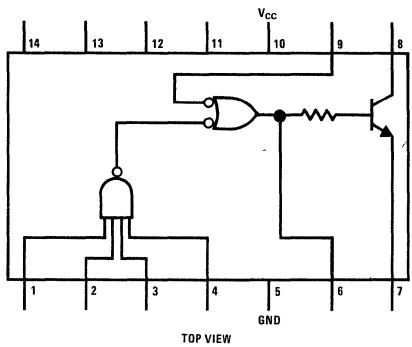
general description

This high-voltage, high-current driver family consists of hybrid integrated circuits which provide a wide range of output currents and output voltages. Applications include driving lamps, relays, cores, and other devices requiring up to 500 mA and withstanding voltages up to 100V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects to the base of the output transistor.

*Previously called NH0016CN, NH0017CN, NH0018CN

logic diagram

Dual-In-Line Package



TOP VIEW

ordering information

NSC DESIGNATION	SH DESIGNATION	SEE PACKAGE	OUTPUT CHARACTERISTICS	
			Maximum Standoff Voltage	Current
DH0016CN	N/A	21	70V	250 mA
DH0017CN	SH2200P	21	50V	500 mA
DH0018CN	N/A	21	100V	500 mA

absolute maximum ratings

V_{CC}		8V
Input Voltage		8V
Collector Voltage	DH0016CN	70V
	DH0017CN	50V
	DH0018CN	100V
Output Surge Current	DH0016CN	1.0A
	DH0017CN & DH0018CN	2.0A
Power Dissipation		455mW
Operating Temperature Range		0°C to +70°C
Storage Temperature		−65°C to +150°C

electrical characteristics

TEST NO.	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	SENSE	LIMITS MIN	LIMITS MAX
2	V_{IH}	V_{IH}	V_{IH}	V_{IH}	GND		GND	I_{OL1}		V_{CC}	V_8		V_{OL1}
3	V_{IL}				GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
4		V_{IL}			GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
5			V_{IL}		GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
6				V_{IL}	GND		GND	I_{OL1}	V_{IL}	V_{CC}	V_8		V_{OL1}
7	V_{IL}				GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
8		V_{IL}			GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
9			V_{IL}		GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
10				V_{IL}	GND	I_{OL2}				V_{CC}	V_6		V_{OL2}
11				GND	GND	I_{OL2}			V_{IH}	V_{CC}	V_6		V_{OL2}
12	V_R	GND	GND	GND	GND					V_{CC}	I_1		I_R
13	GND	V_R	GND	GND	GND					V_{CC}	I_2		I_R
14	GND	GND	V_R	GND	GND					V_{CC}	I_3		I_R
15	GND	GND	GND	V_R	GND					V_{CC}	I_4		I_R
16					GND				V_R	V_{CC}	I_9		I_R
17	V_F	V_R	V_R	V_R	GND					V_{CC}	I_1		$-I_F$
18	V_R	V_F	V_R	V_R	GND					V_{CC}	I_2		$-I_F$
19	V_R	V_R	V_F	V_R	GND					V_{CC}	I_3		$-I_F$
20	V_R	V_R	V_R	V_F	GND					V_{CC}	I_4		$-I_F$
21				GND	GND				V_F	V_{CC}	I_9		$-I_F$
22					GND		GND			V_{CC}	V_6	V_{OH1}	
23	GND				GND	I_{OL3}	GND	V_{OX}		V_{CC}	I_8		I_{OX}
24					GND					V_{PD}	I_{10}		I_{PD}
25	GND				GND				GND	V_{MAX}	I_{10}		I_{MAX}

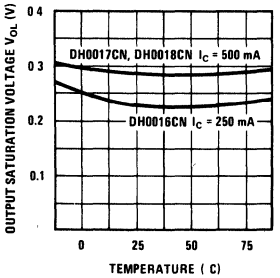
forcing functions

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{CC}	5.0	5 0	5.0	V
V_{PD}		5.0		V
V_{MAX}		8.0		V
V_{IL}	0.85	0.85	0.85	V
V_{IH}	1 9	1.8	1.6	V
V_R	4.5	4.5	4.5	V
V_F	0.45	0.45	0.45	V
V_{OX} (DH0016CN)		70	70	V
V_{OX} (DH0017CN)		50	50	V
V_{OX} (DH0018CN)		100	100	V
I_{OL1} (DH0017CN, DH0018CN)	500	500	500	mA
I_{OL1} (DH0016CN)	250	250	250	mA
I_{OL2}	16	16	16	mA
I_{OL3}		8.0		mA

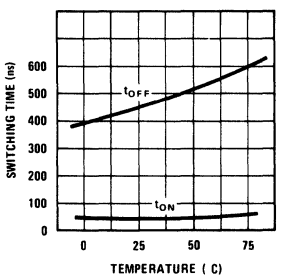
test limits

SYMBOL	0°C	+25°C	+70°C	UNITS
V_{OL1}	0.6	0.6	0.6	V
V_{OL2}	0.45	0.45	0.45	V
V_{OHI}	1.95	1.85	1.65	V
I_R		60	60	μA
$-I_F$	1.6	1.6	1.6	mA
I_{OX}		5.0	200	μA
I_{PD}		12.2		mA
I_{MAX}		10		mA

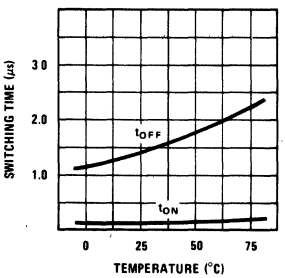
Typical Output Voltages vs Temperature



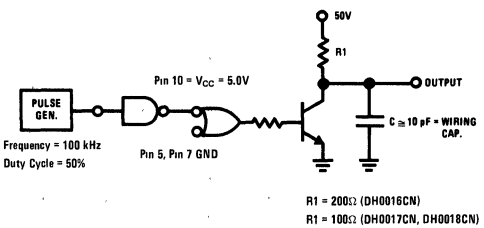
Typical Switching Times I_C = 250 mA
DH0016CN



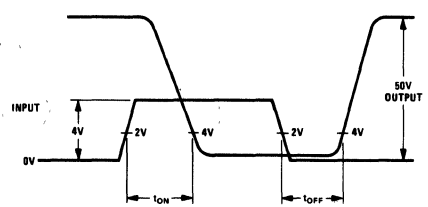
Typical Switching Times I_C = 500 mA
DH0017CN, DH0018CN



switching time test circuit



switching time waveform



Peripheral/Power Drivers

DH0028C/DH0028CN* hammer driver

general description

The DH0028C/DH0028CN is a high current hammer driver designed for utilization in a wide variety of printer applications. The device is capable of driving 6 amp pulsed loads at duty cycles up to 10% (1 ms ON/10 ms OFF). The input is DTL/TTL compatible and requires only a single voltage supply in the range of 10V to 45V.

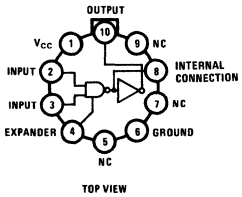
features

- Low standby power: 45 mW at V_{CC} = 36V, 35 mW at V_{CC} = 28V.
- AND input with expander affords logic flexibility.
- Fast turn-on, typically 200 ns.

*Previously called NH0028C/NH0028CN

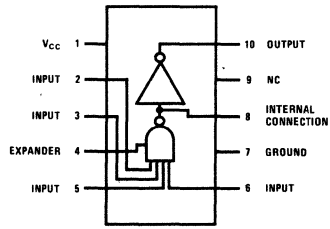
connection diagrams

Metal Can Package



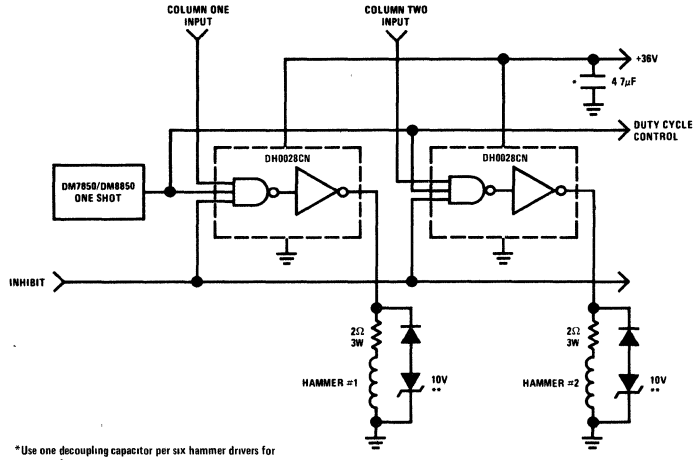
Order Number DH0028CH
See Package 13

Molded Dual-In-Line Package



Order Number DH0028CN
See Package 21

typical application



*Use one decoupling capacitor per six hammer drivers for improved ac noise immunity

**Zener is used to control the dynamics of the hammer

absolute maximum ratings

Continuous Supply Voltage	45V
Instantaneous Peak Supply Voltage (Pin 1 to Ground for 0.1 sec)	60V
Input Voltage	5.5V
Expander Input Current	5.0 mA
Peak Otuput Current (1 ms ON/10 ms OFF)	6.5A
Continuous Output Current DH0028C at 25°C	750 mA
DH0028CN at 25°C	1000 mA
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +175°C
Lead Soldering Temperature (10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 10V to 45V	2 0			V
Logical "0" Input Voltage	V_{CC} = 10V to 45V			0.8	V
Logical "0" Input Current	V_{CC} = 45V, V_{IN} = 0 4V		0 8	1 0	mA
Logical "1" Input Current	V_{CC} = 45V, V_{IN} = 2 4V		0 5	5.0	μA
	V_{CC} = 45V, V_{IN} = 5 5V			100 0	μA
Logical "1" Output Voltage	V_{CC} = 45V, V_{IN} = 2 0V, I_{OUT} = 1 6A	43 0	43 5		V
	V_{CC} = 36V, V_{IN} = 2 0V, I_{OUT} = 5A (Note 2)	33 5	34 0		V
Logical "0" Output Voltage	V_{CC} = 45V, R_L = 1k, V_{IN} = 0 8V		020	100	V
OFF Power Supply Current	V_{CC} = 45V, V_{IN} = 0 0V		1 6	2 0	mA
Rise Time (10% to 90%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5 0V peak, PRF = 1 kHz		0 2		μs
Fall Time (90% to 10%)	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5 0V peak, PRF = 1 kHz		3 0		μs
T_{ON}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5 0V peak, PRF = 1 kHz		0 4		μs
T_{OFF}	V_{CC} = 45V, R_L = 39Ω, V_{IN} = 5 0V peak, PRF = 1 kHz		7 0		μs

Note 1. These specifications apply for ambient temperatures from 0°C to 70°C unless otherwise specified. All typical values are for 25°C ambient.

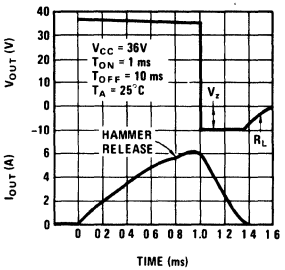
Note 2: Measurement made at 1 ms ON and 10 ms OFF.

Note 3: Power ratings for the DH0028C are based on a maximum junction temperature of 175°C and a thermal resistance of 210°C/W.

Note 4: Power ratings for the DH0028CN are based on a maximum junction temperature of 175°C and a thermal resistance of 150°C/W.

typical performance characteristics

Waveforms for Typical Drum Printer Hammer



Peripheral/Power Drivers

DH0035/DH0035C PIN diode switch driver

general description

The DH0035/DH0035C is a high speed digital driver designed to drive PIN diodes in RF modulators and switches. The device is used in conjunction with an input buffer such as the DM7830/DM8830 or DM5440/DM7440.

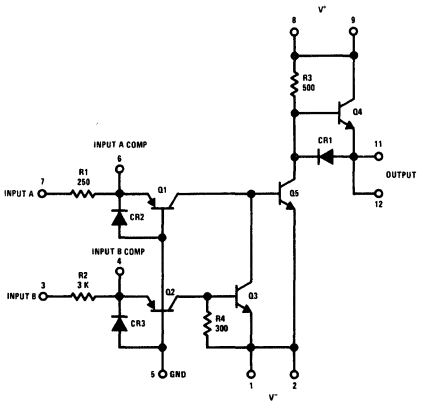
features

- Large output voltage swing – 30V
- Peak output current in excess of 1 Amp
- Inputs TTL/DTL compatible
- Short propogation delay – 10 ns
- High repetition rate – 5 MHz

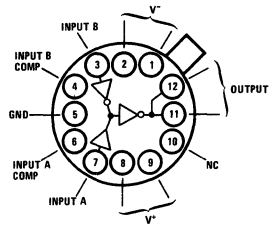
The DH0035/DH0035C is capable of driving a variety of PIN diode types including parallel, serial, anode grounded and cathode grounded. For additional information, see *AN-49 PIN Diode Drivers*.

The DH0035 is guaranteed over the temperature range −55°C to +125°C whereas the DH0035C is guaranteed from 0°C to 85°C.

schematic and connection diagrams



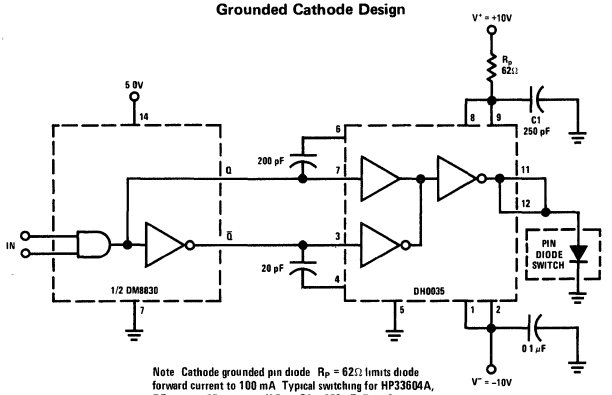
Metal Can Package



Order Number DH0035G or DH0035CG
See Package 6

typical applications

Grounded Cathode Design



Note Cathode grounded pin diode $R_P = 62\Omega$ limits diode forward current to 100 mA Typical switching for HP33604A, RF turn-on 25 ns, turn-off 5 ns C2 = 250 pF, $R_P = 0\Omega$, C1 = 0 1F

5

absolute maximum ratings

V^- Supply Voltage Differential (Pin 5 to Pin 1 or 2)	40V
V^+ Supply Voltage Differential (Pin 1 or 2 to Pin 8 or 9)	30V
Input Current (Pin 3 or 7)	±75 mA
Peak Output Current	±1 0 Amps
Power Dissipation (Note 3)	1 5W

Storage Temperature Range	−65°C to +150°C
Operating Temperature Range DH0035	−55°C to +125°C
DH0035C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1, 2)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Logic "1" Threshold	V_{OUT} = −8V, R_L = 100Ω	1 5			V
Input Logic "0" Threshold	V_{OUT} = +8V, R_L = 100Ω			0 4	V
Positive Output Swing	I_{OUT} = 100 mA	7 0	+8.0		V
Negative Output Swing	I_{OUT} = 100 mA		−8.0	−7.0	V
Positive Short Circuit Current	V_{IN} = 0V, R_L = 0Ω (Pulse Test; Duty Cycle ≤ 3%)	400	800		mA
Negative Short Circuit Current	V_{IN} = 1.5V, I_{IN} = 50 mA, R_L = 0Ω (Pulse Test, Duty Cycle ≤ 3%)	800	−1000		mA
Turn-On Delay	V_{IN} = 1.5V, V_{OUT} = −3V		10	15	ns
Turn-Off Delay	V_{IN} = 1 5V, V_{OUT} = +3V		15	30	ns
On Supply Current	V_{IN} = 1 5V		45	60	mA

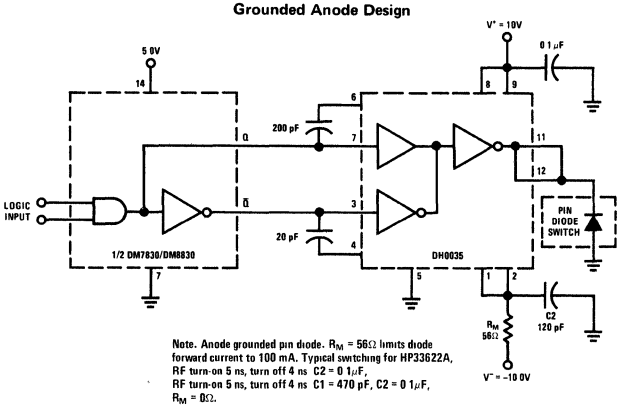
Note 1: Unless otherwise specified, these specifications apply for V^+ = 10.0V, V^- = −10.0V, pin 5 grounded, over the temperature range −55°C to +125°C for the DH0035, and 0°C to 85°C for the DH0035C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 10 mW/°C for ambient temperatures above 25°C.

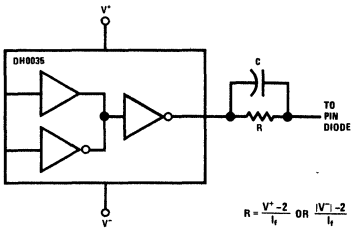
typical applications (cont.)

Grounded Anode Design



Note. Anode grounded pin diode. R_M = 56Ω limits diode forward current to 100 mA. Typical switching for HP33622A, RF turn-on 5 ns, turn off 4 ns C2 = 0 1µF; RF turn-on 5 ns, turn off 4 ns C1 = 470 pF, C2 = 0 1µF, R_M = 0Ω.

Alternate Current Limiting



Peripheral/Power Drivers

LM3611, LM3612, LM3613, LM3614 dual peripheral drivers

general description

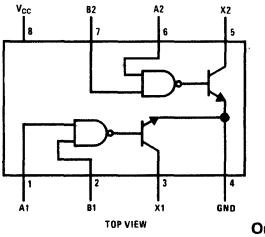
The LM3611 series of dual peripheral drivers was designed for those applications where a higher breakdown voltage is required than that provided by the LM75451 series. The pin outs for the circuits are identical to those of the LM75451 to LM75454. The LM3611 series parts feature high voltage outputs (80V breakdown in the "off" state) as well as high current (300 mA in the "on" state). Typical applications include power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers.

features

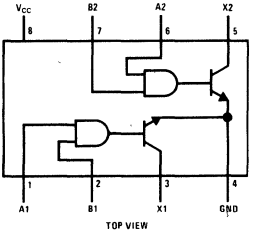
- 300 mA output current capability per driver
- High-voltage outputs 80V
- TTL or DTL compatible
- Input clamping diodes
- Choice of logic function

connection diagrams and truth tables

LM3611



LM3612



Order Number LM3611N or LM3612N
See Package 20

Positive logic AB=X

A	B	OUTPUT X*
0	0	0
1	0	0
0	1	0
1	1	1

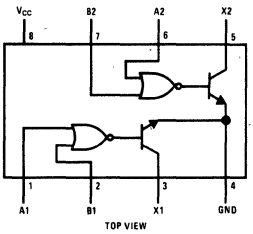
*"0" Output ≤ 0.7V
"1" Output ≤ 100μA

Positive logic $\overline{AB}$=X

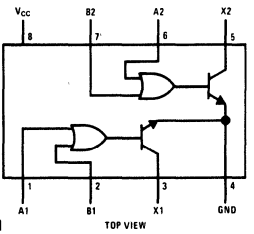
A	B	OUTPUT X*
0	0	1
1	0	1
0	1	1
1	1	0

*"0" Output ≤ 0.7V
"1" Output ≤ 100μA

LM3613



LM3614



Order Number LM3613N or LM3614N
See Package 20

Positive logic A + B = X

A	B	OUTPUT X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output ≤ 0.7V
"1" Output ≤ 100μA

Positive logic A + B = X

A	B	OUTPUT X*
0	0	1
1	0	0
0	1	0
1	1	0

*"0" Output ≤ 0,7V
"1" Output ≤ 100μA

5

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage (Note 3)	80V
Continuous Output Current	300 mA
Continuous Total Power Dissipation (Note 2)	800 mW
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (LM3611 Dual AND Peripheral Driver)

The following apply at $0°C \leqq T_A \leqq +70°C$, V_{CC} = 5.0V +5% unless otherwise specified.

PARAMETER	LOGIC INPUT	OUTPUT	SUPPLY VOLTAGE	COMMENTS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IN}		4 75V	Figure 1	2 0			V
Logical "0" Input Voltage	V_{IN}		4 75V	Figure 1			0 8	V
Logical "1" Input Current	2 4V		5.25V	Figure 2			40	μA
	5.5V		5.25V	Figure 2			1 0	mA
Logical "0" Input Current	0 4V		5 25V	Figure 3		−1.0	−1 6	mA
Output Low Voltage	0 8V	100 mA	4 75V	Figure 1		0 25	0 4	V
	0 8V	300 mA	4.75V	Figure 1		0 5	0 7	V
Output Leakage Current	2 0V	100μA	4.75V	Figure 1	80			V
	2 0V	100μA	0V	Figure 1	80			V
Supply Currents								
Output Low	0V		5 25V	Per Package Figure 4			69	mA
Output High	5 0V		5 25V	Per Package Figure 4			11	mA
Input Clamp Diode Voltage	−12 mA		5 0V	T_A = +25°C Figure 3			−1 5	V
Propagation Delay Times. The following apply for V_{CC} = 5 0V, T_A = 25°C								
Propagation to "1" (t_{pd1})			(Note 4)	Figure 6		130		ns
Propagation to "0" (t_{pd0})			(Note 4)	Figure 6		125		ns

electrical characteristics (LM3612 Dual NAND Peripheral Driver)

The following apply at $0°C \leqq T_A \leqq +70°C$, V_{CC} = 5.0V +5% unless otherwise specified.

PARAMETER	LOGIC INPUT	OUTPUT	SUPPLY VOLTAGE	COMMENTS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IN}		4 75V	Figure 1	2 0			V
Logical "0" Input Voltage	V_{IN}		4 75V	Figure 1			0.8	V
Logical "1" Input Current	2 4V		5.25V	Figure 2			40	μA
	5.5V		5 25V	Figure 2			1.0	mA
Logical "0" Input Current	0 4V		5 25V	Figure 3		−1.0	−1 6	mA
Output Low Voltage	2 0V	100 mA	4 75V	Figure 1		0.25	0 4	V
	2 0V	300 mA	4 75V	Figure 1		0 5	0 7	V
Output Leakage Current	0 8V	100μA	4 75V	Figure 1	80			V
	0 8V	100μA	0V	Figure 1	80			V
Supply Currents								
Output Low	5 0V		5.25V	Per Package Figure 4			71	mA
Output High	0V		5 25V	Per Package Figure 4			14	mA
Input Clamp Diode Voltage	−12 mA		5 0V	T_A = +25°C Figure 3			−1.5	V
Propagation Delay Times The following apply for V_{CC} = 5 0V, T_A = +25°C								
Propagation to "1" (t_{pd1})			(Note 4)	Figure 6		110		ns
Propagation to "0" (t_{pd0})			(Note 4)	Figure 6		110		ns

electrical characteristics (LM3613 Dual OR Peripheral Driver)

The following apply at $0°C \leq T_A \leq +70°C$, V_{CC} = 5.0V +5% unless otherwise specified.

PARAMETER	LOGIC INPUT	OUTPUT	SUPPLY VOLTAGE	COMMENTS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IN}		4 75V	Figure 1	2 0			V
Logical "0" Input Voltage	V_{IN}		4.75V	Figure 1			0 8	V
Logical "1" Input Current	2 4V		5.25V	Figure 2			40	μA
	5.5V		5 25V	Figure 2			1 0	mA
Logical "0" Input Current	0.4V		5.25V	Figure 3		−1.0	−1 6	mA
Output Low Voltage	0 8V	100 mA	4 75V	Figure 1		0 25	0 4	V
	0.8V	300 mA	4 75V	Figure 1		0 5	0 7	V
Output Leakage Current	2 0V	100μA	4 75V	Figure 1	80			V
	2 0V	100μA	0V	Figure 1	80			V
Supply Currents								
Output Low	0V		5 25V	Per Package Figure 5			73	mA
Output High	5.0V		5 25V	Per Package Figure 5			14	mA
Input Clamp Diode Voltage	−12 mA		5 0V	T_A = +25°C			−1 5	V
Propagation Delay Times The following apply for V_{CC} = 5 0V, T_A = +25°C								
Propagation to "1" (t_{pd1})			(Note 4)	Figure 6		125		ns
Propagation to "0" (t_{pd0})			(Note 4)	Figure 6		125		ns

electrical characteristics (LM3614 Dual NOR Peripheral Driver)

The following apply at $0°C \leq T_A \leq +70°C$, V_{CC} = 5.0V +5% unless otherwise specified.

PARAMETER	LOGIC INPUT	OUTPUT	SUPPLY VOLTAGE	COMMENTS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage	V_{IN}		4.75V	Figure 1	2 0			V
Logical "0" Input Voltage	V_{IN}		4 75V	Figure 1			0 8	V
Logical "1" Input Current	2 4V		5 25V	Figure 2			40	μA
	5 5V		5.25V	Figure 2			1.0	mA
Logical "0" Input Current	0 4V		5 25V	Figure 3		−1.0	−1 6	mA
Output Low Voltage	2 0V	100 mA	4 75V	Figure 1		0.25	0 4	V
	2.0V	300 mA	4 75V	Figure 1		0 5	0.7	V
Output Leakage Current	0 8V	100μA	4 75V	Figure 1	80			V
	0 8V	100μA	0V	Figure 1	80			V
Supply Currents								
Output Low	5 0V		5.25V	Per Package Figure 5			79	mA
Output High	0V		5 25V	Per Package Figure 5			17	mA
Input Clamp Diode Voltage	−12 mA		5.0V	T_A = +25°C Figure 3			−1 5	V
Propagation Delay Times The following apply for V_{CC} = 5.0V, T_A = +25°C								
Propagation to "1" (t_{pd1})			(Note 4)	Figure 6		220		ns
Propagation to "0" (t_{pd0})			(Note 4)	Figure 6		150		ns

Note 1: All voltage values are with respect to ground. Positive current is defined to be current into referenced pin.

Note 2: Maximum junction temperature is 150°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance, θ_{JA}, of 110°C/W.

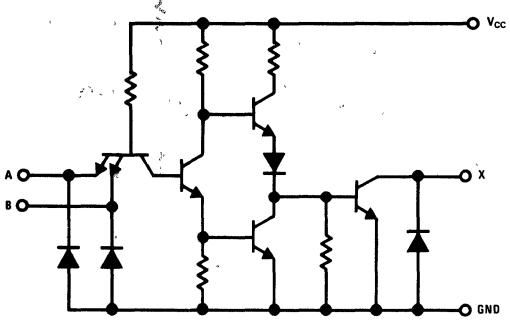
Note 3: Maximum voltage to be applied to either output in the off state.

Note 4: Delay is measured with a 50Ω load to 10V, 15 pF load capacitance, measured from 1.5V input to 50% point on output.

5

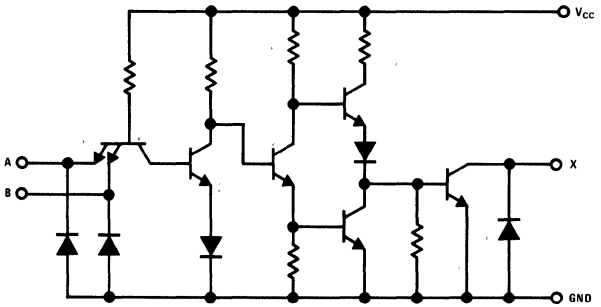
schematic diagrams (each driver)

LM3611 Dual AND Peripheral Driver



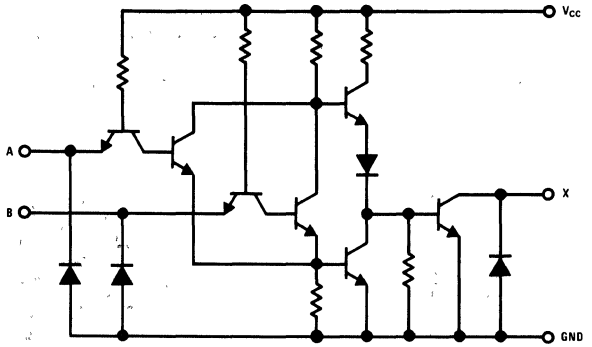
NOTE 1/2 OF UNIT SHOWN

LM3612 Dual NAND Peripheral Driver



NOTE 1/2 OF UNIT SHOWN

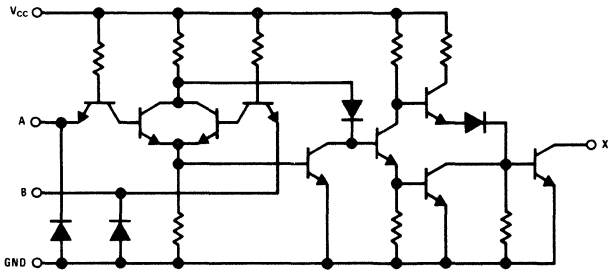
LM3613 Dual OR Peripheral Driver



NOTE 1/2 OF UNIT SHOWN

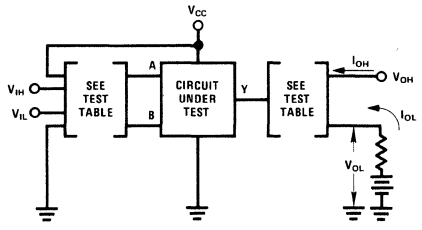
schematic diagrams (con't)

LM3614 Dual NOR Peripheral Driver



NOTE 1/2 OF UNIT SHOWN

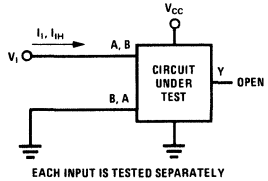
test circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
LM3611	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OH} I_{OL}	V_{OH} V_{OL}
LM3612	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} I_{OH}	V_{OL} V_{OH}
LM3613	V_{IH} V_{IL}	GND V_{IL}	I_{OH} I_{OL}	V_{OH} V_{OL}
LM3614	V_{IH} V_{IL}	GND V_{IL}	I_{OL} I_{OH}	V_{OL} V_{OH}

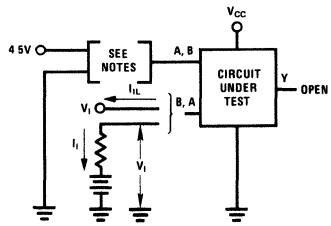
NOTE: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, I_{OH}, V_{OL}



EACH INPUT IS TESTED SEPARATELY

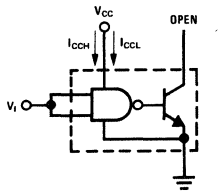
FIGURE 2. I_I, I_{IH}



NOTE A EACH INPUT IS TESTED SEPARATELY.

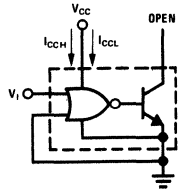
NOTE B WHEN TESTING LM3613 AND LM3614 INPUT NOT UNDER TEST IS GROUNDED. FOR ALL OTHER CIRCUITS IT IS AT 4.5V

FIGURE 3. V_I, I_{IL}



BOTH GATES ARE TESTED SIMULTANEOUSLY

FIGURE 4. I_{CCH}, I_{CCL} for AND, NAND Circuits

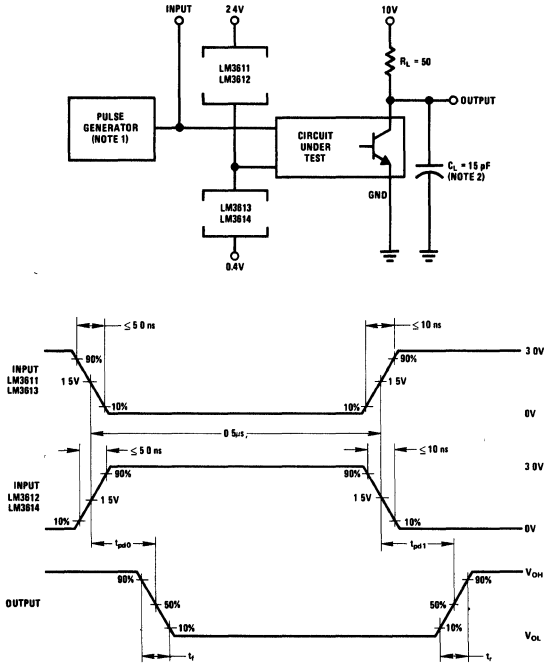


BOTH GATES ARE TESTED SIMULTANEOUSLY.

FIGURE 5. I_{CCH}, I_{CCL} for OR, NOR Circuits

5

test circuit and switching time waveforms



NOTE 1 THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$

NOTE 2 C_L INCLUDES PROBE AND JIG CAPACITANCE

FIGURE 6. Switching Times of Complete Drivers

Peripheral/Power Drivers

LM75450, LM350 dual peripheral driver

general description

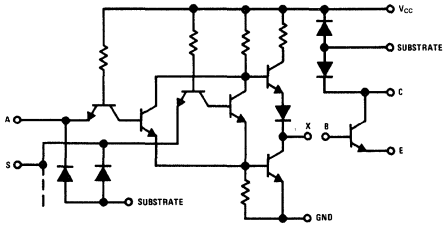
The LM75450 and LM350 are general purpose dual peripheral drivers. The design employs two standard TTL gates (NOR in LM350, NAND in LM75450) and two totally uncommitted, high-voltage, high-current NPN transistors. These transistors are capable of sinking 300 mA and will withstand 30V in the OFF state. Inputs are fully DTL/TTL compatible. The LM75450 meets or exceeds the specifications for both the SN75450 and the SN75450A and is a pin-for-pin replacement.

features

- High speed
- High sink current 300 mA
- Separate gates and transistors
- Both transistors can sink 300 mA simultaneously
- Transistors withstand 30V collector to emitter in the OFF state
- Input clamp diodes

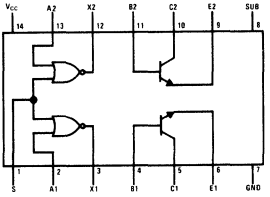
schematic and connection diagrams

LM350



Note 1/2 of unit shown

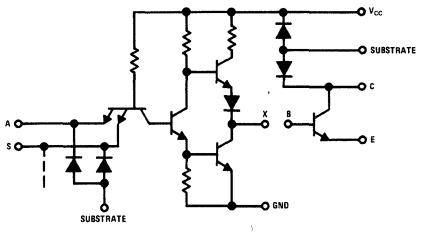
LM350



Positive Logic: $\overline{A+S} = X$

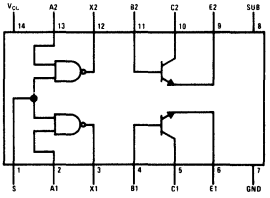
Order Number LM350N
See Package 22

LM75450



Note 1/2 of unit shown

LM75450



Positive Logic: $\overline{A \cdot S} = X$

Order Number LM75450N
See Package 22

5

absolute maximum ratings (Note 1)

Supply Voltage V_{CC}	7V	Emitter-Base Voltage	5V
Input Voltage	5.5V	Continuous Collector Current	300 mA
V_{CC} -to-Substrate Voltage	35V	Continuous Total Power Dissipation (Note 3)	800 mW
Collector-to-Substrate Voltage	35V	Operating Free-Air Temperature Range	0°C to 70°C
Collector-Base Voltage	35V	Storage Temperature Range	−65°C to 150°C
Collector-Emitter Voltage (Note 2)	30V		

electrical characteristics

The following apply for $0°C \leq T_A \leq 70°C$, V_{CC} = 5V ±5%, for LM75450 and LM350 unless otherwise specified.

TTL GATES

PARAMETER	COMMENTS	LOGIC INPUT	LOGIC OUTPUT	SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	Logic Output ≤ 0.4V	V_{IN}	16 mA	4.75V	2			V
Logical "0" Input Voltage	Logic Output ≥ 2.4V	V_{IN}	−400 μA	4.75V			0.8	V
Logical "1" Output Voltage		0.8V	−400 μA	4.75V	2.4			V
Logical "0" Output Voltage		2V	16 mA	4.75V			0.4	V
Logical "1" Input Current	A Input	2.4V		5.25V			40	μA
	S Input	2.4V		5.25V			80	μA
	A Input	5.5V		5.25V			1	mA
	S Input	5.5V		5.25V			2	mA
Logical "0" Input Current	A Input	0.4V		5.25V			−1.6	mA
	S Input	0.4V		5.25V			−3.2	mA
Output Short Circuit Current	Note 4	0V	0V	5.25V	−18		−55	mA
Supply Current								
Output Low								
LM350	Per Package	5V		5.25V		8	14	mA
LM75450	Per Package	5V		5.25V		6	11	mA
Output High								
LM350	Per Package	0V		5.25V		4	7	mA
LM75450	Per Package	0V		5.25V		2	4	mA
Input Diode Clamp Voltage	T_A = 25°C, V_{SUB} = 0V	−1.2 mA		5V			−1.5	V

TRANSISTORS

PARAMETER	COMMENTS	BASE	EMITTER	COLLECTOR	MIN	TYP	MAX	UNIT
BV_{CBO}		0V		100 μA	35			V
BV_{CER}	$R_{BE} \leq 500\Omega$		0V	100 μA	30			V
BV_{EBO}		0V	100 μA		5			V
V_{BE}		10 mA	0V	100 mA		0.85	1	V
		30 mA	0V	300 mA		1.05	1.2	V
$V_{CE(sat)}$		10 mA	0V	100 mA		0.25	0.4	V
		30 mA	0V	300 mA		0.5	0.7	V
h_{FE}	V_{CE} = 3V, T_A = 0°C, Note 5	I_B	0V	100 mA	20			
	V_{CE} = 3V, T_A = 0°C Note 5	I_B	0V	300 mA	25			
	V_{CE} = 3V, T_A = 25°C, Note 5	I_B	0V	100 mA	25			
	V_{CE} = 3V, T_A = 25°C, Note 5	I_B	0V	300 mA	30			

The following apply for V_{CC} = 5V, T_A = 25°C

TTL GATES (Note 6)

PARAMETER	TYP	MAX
t_{pd1}	10 ns	22 ns
t_{pd0}	5 ns	15 ns

TRANSISTORS

PARAMETER	TYP	MAX
t_d	6 ns	15 ns
t_r	12 ns	20 ns
t_s	6 ns	15 ns
t_f	8 ns	15 ns

GATES AND TRANSISTORS (Note 7)

PARAMETER	TYP
t_{pd1}	30 ns
t_{pd0}	30 ns
t_r	12 ns
t_f	15 ns

Note 1: All voltage values are with respect to ground terminal. Positive current is defined to be current into referenced pin.

Note 2: With base-emitter resistance ≤ 500Ω.

Note 3: The maximum junction temperature is 150°C. For operating at elevated temperatures the package must be derated based on a thermal resistance of 150°C/W θ_{JA}.

Note 4: Only one output should be shorted at a time.

Note 5: These parameters are to be measured with less than 2% duty cycle.

Note 6: Delays measured with fanout of 10, 15 pF total load capacitance; measured from 1.5V input to 1.5V output.

Note 7: Delays measured with 50Ω load to 10V, 15 pF total load capacitance; measured from 1.5V input to 50% of output.

Peripheral/Power Drivers

LM75451, LM75452, LM75453, LM351 dual peripheral driver

general description

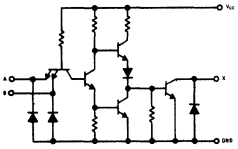
These devices are general purpose dual peripheral drivers, each capable of sinking two independent 300 mA loads to ground. In the off state (or with V_{CC} = 0V) the outputs will withstand 30V. Inputs are fully DTL/TTL compatible. The LM75451 meets or exceeds the specifications for the SN75451 and is a pin-for-pin replacement. The LM75452 and LM75453 meet or exceed the specifications for SN75452 and SN75453, respectively, and are pin-for-pin replacements.

features

- High speed
- Both outputs can sink 300 mA simultaneously
- Withstands 30V on output with V_{CC} = 0V for power strobing applications
- Input clamp diodes
- Two separate drivers per package

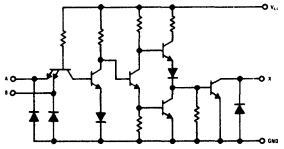
schematic diagrams

LM75451



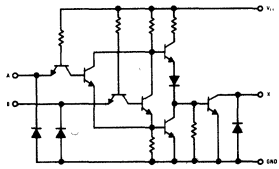
Note 1/2 of unit shown

LM75452



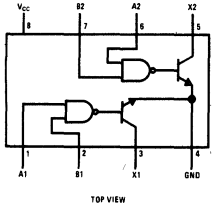
Note 1/2 of unit shown

LM351, LM75453



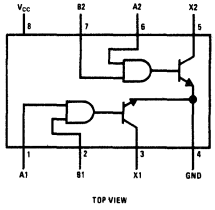
Note 1/2 of unit shown

connection diagrams



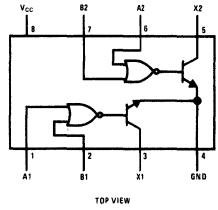
TOP VIEW

Order Number LM75451N
See Package 20



TOP VIEW

Order Number LM75452N
See Package 20



TOP VIEW

Order Number LM75453N or LM351
See Package 20

truth tables

Positive logic: AB=X

A	B	OUTPUT X*
0	0	0
1	0	0
0	1	0
1	1	1

*"0" Output ≤ 0.7V
"1" Output ≤ 100 μA

Positive logic: $\overline{AB}$=X

A	B	OUTPUT X*
0	0	1
1	0	1
0	1	1
1	1	0

*"0" Output ≤ 0.7V
"1" Output ≤ 100 μA

Positive logic: A + B = X

A	B	OUTPUT X*
0	0	0
1	0	1
0	1	1
1	1	1

*"0" Output ≤ 0.7V
"1" Output ≤ 100 μA

5

absolute maximum ratings (Note 1)

Supply Voltage V_{CC}	7V	Continuous Total Power Dissipation (Note 3)	800 mW
Input Voltage	5 5V	Operating Free Air Temperature Range	0°C to 70°C
Output Voltage (Note 2)	30V	Storage Temperature Range	−65°C to 150°C
Continuous Output Current	300 mA	Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics

The following apply for $0°C \leq T_A \leq 70°C$, V_{CC} = 5V ±5%, unless otherwise specified (Note 4)

PARAMETER	LOGIC INPUT	OUTPUT	SUPPLY VOLTAGE	COMMENTS	MIN	TYP	MAX	UNIT
Logic "1" Input Voltage	V_{IN}	30V (300 mA)	4 75V	Output $\leq$ 100 μA ($\leq$0.7V)	2			V
Logic "0" Input Voltage	V_{IN}	300 mA (30V)	4 75V	Output $\leq$ 0.7V ($\leq$100 μA)			0 8	V
Output Leakage Currents	2V (0.8V)	30V	4 75V				100	μA
		30V	0V				100	μA
Output LOW Voltages	0 8V (2V)	100 mA	4.75V			0 25	0 4	V
	0 8V (2V)	300 mA	4 75V			0.5	0 7	V
Logic "1" Input Currents	2.4V		5.25V				40	μA
	5 5V		5.25V				1	mA
Logic "0" Input Current	0.4V		5.25V			−1	−1 6	mA
Supply Currents.								
Output Low								
LM75451	0V		5.25V	Per Package		48	65	mA
LM75452	5V		5.25V	Per Package		51	71	mA
LM75453	0V		5 25V	Per Package		50	68	mA
Output High								
LM75451	5V		5.25V	Per Package		7	11	mA
LM75452	0V		5 25V	Per Package		9	14	mA
LM75453	5V		5.25V	Per Package		9	11	mA
Input Diode Clamp Voltage	−12 mA		5V	T_A = 25°C			−1 5	V
The following apply for V_{CC} = 5V, T_A = 25°C								
Propagation Delay Times								
Input to Output HIGH								
LM75451& LM75453			(Note 5)			11	25	ns
LM75452			(Note 5)			13	35	ns
Input to Output LOW								
LM75451& LM75453			(Note 5)			16	25	ns
LM75452			(Note 5)			19	35	ns
Output Risetime						4		ns
Output Falltime						10		ns

Note 1: All voltage values are with respect to ground terminal. Positive current is defined to be current into referenced pin.

Note 2: Maximum voltage to be applied to either output in the off state.

Note 3: The maximum junction temperature is 150°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance of 110°C/W θ_{JA}.

Note 4: Test conditions in parentheses pertain to LM75452, other test conditions pertain to LM75451A and LM75453.

Note 5: Delays measured with 50Ω load to 10V, 15 pF total load capacitance; measured from 1.5V input to 50% of output.

Peripheral/Power Drivers

LM75454 dual peripheral driver

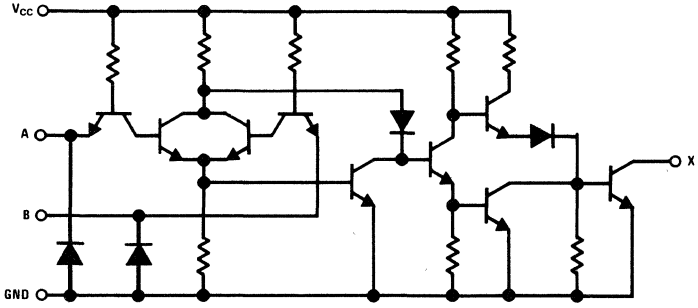
general description

The LM75454 is a dual NOR peripheral line driver with output transistors rated up to 300mA continuous current. Both output transistors can sink this current at the same time, bringing maximum chip power dissipation to 820mW. Switching speeds are compatible with standard TTL and logic levels interface directly with TTL, DTL, and LPTTL logic families. The overall input to output NOR function allows pin for pin replacement with TI's SN75454 positive logic NOR driver.

features

- High speed
- Both outputs can sink 300 mA simultaneously
- Withstands 30V on outputs
- Input clamp diodes
- Maximum package power dissipation at maximum current rating $\leq$ 820 mW

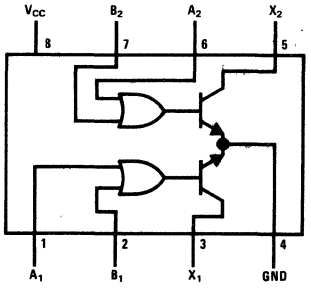
schematic diagram



NOTE: 1/2 SCHEMATIC SHOWN

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number LM75454N
See Package 20

truth table

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Voltage (Note 4)	30V
Continuous Output Current	300mA
Continuous Total Power Dissipation (Note 2)	820mW
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics The following apply at $0°C \leq T_A \leq +70°C$, V_{CC} = 5V + 5% unless otherwise noted.

PARAMETER	LOGIC INPUT	OUTPUT	SUPPLY VOLTAGE	COMMENTS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IN}	300mA	4 75V	Output $\leq$ 0 7V	2 0			V
Logical "0" Input Voltage	V_{IN}	30V	4 75V	Output $\leq$ 100μA			0 8	V
Logical "1" Input Current	2.4V		5 25V				40	μA
	5.5V		5 25V				1	mA
Logical "0" Input Current	0.4V		5 25V			−1.0	−1 6	mA
Output Low Voltage	2.0V	100mA	4 75V			0 25	0 4	V
	2 0V	300mA	4 75V			0 5	0 7	V
Output Leakage Current	0 8V	30V	4 75V				100	μA
	0.8V	30V	0V				100	μA
Supply Currents:								
Output Low	A_1 = 5V, B_1 = 0V		5 25V	Per Package		61	79	mA
Output High	$A_1 = B_1$ = 0V		5 25V	Per Package		13	17	mA
Input Clamp Diode Voltage	−12mA		5V	T_A = 25°C			−1 5	V
Propagation Delay Times. The following Apply for V_{CC} = 5V, T_A = 25°C								
t_{pd1}, Input "0" to Output "1"			(Note 3)			13	35	ns
t_{pd1}, Input "1" to Output "0"			(Note 3)			19	35	ns
Output Risetime								ns
Output Falltime								ns

Note 1: All voltage values are with respect to ground. Positive current is defined to be current into referenced pin.

Note 2: Maximum junction temperature is 150°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance, θ_{JA}, of 110°C/W.

Note 3: Delay is measured with a 50Ω load to 10V, 15pF load capacitance, measured from 1.5V input to 50% point on output. Unused inputs should be grounded for this test.

Note 4: Maximum voltage to be applied to either output in the off state.

Display Drivers

DM5441A/DM7441A
BCD to decimal decoder/nixie* driver

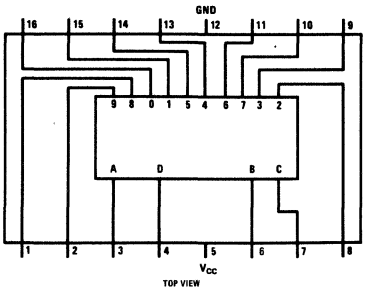
general description

The DM5441A/DM7441A is monolithic binary-coded-decimal to decimal decoder. The BCD number to be decoded is applied to the four input lines; and the unique output corresponding to the decimal equivalent of the input number falls to a logical 0 level. Outputs are designed to drive gas-filled-readout (Nixie*) tubes but are also able to operate with other low current lamps and relays.

An over-range feature provides that if binary numbers between 10 and 15 are applied to the input the least significant bit of these numbers (0 through 5) will be decoded on the output.

connection diagram

Dual-In-Line and Flat Package



Order Number DM5441AJ or DM7441AJ
See Package 17

Order Number DM7441N
See Package 23

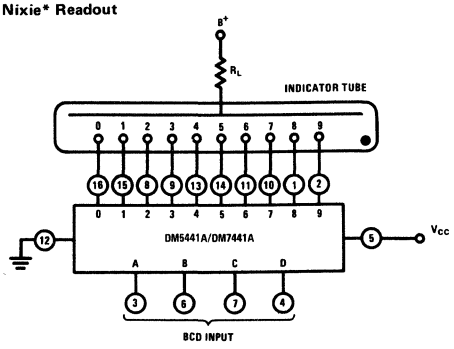
Order Number DM5441AW
See Package 28

logic table

INPUT D	C	B	A	LOW OUTPUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
(OVER RANGE)				
1	0	1	0	0
1	0	1	1	1
1	1	0	0	2
1	1	0	1	3
1	1	1	0	4
1	1	1	1	5

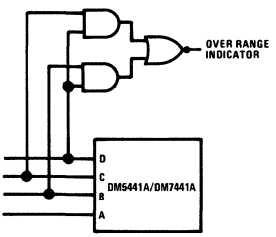
typical applications

Nixie* Readout



Note: Values for B+ and R_L are as specified by the tube manufacturer.

Over-Range Decoding



*Trademark of Burroughs Corporation

absolute maximum ratings

Supply Voltage (V_{CC})		7.0V
Output Voltage		70V
Input Voltage		5.5V
Operating Temperature Range	DM5441A	−55°C to +125°C
	DM7441A	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER		CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
Logical 1 Input Voltage	DM5441A	V_{CC} = 4.5V			2.0			V
	DM7441A	V_{CC} = 4.75V						
Logical 0 Input Voltage	DM5441A	V_{CC} = 4.5V					0.8	V
	DM7441A	V_{CC} = 4.75V						
Logical 1 Input Current (all inputs)	DM5441A	V_{CC} = 5.5V	V_{IN} = 2.4V			3	40	μA
	DM7441A	V_{CC} = 5.25V						
Logical 1 Input Current	DM5441A	V_{CC} = 5.5V	V_{IN} = 5.5V				1	mA
	DM7441A	V_{CC} = 5.25V						
Logical 0 Input Current	DM5441A	V_{CC} = 5.5V	V_{IN} = 0.4V			−1.0	−1.6	mA
	DM7441A	V_{CC} = 5.25V						
Supply Current	DM5441A	V_{CC} = 5.5V	V_{IN} = 0.0V			21	36	mA
	DM7441A	V_{CC} = 5.25V						
Logical 1 Output Breakdown	DM5441A	V_{CC} = 5.5V	I_{OUT} = 1.0 mA		70	85		V
	DM7441A	V_{CC} = 5.25V						
Logical 1 Output Current	DM5441A	V_{CC} = 5.5V	V_{OUT} = 50V	125°			60	μA
				70°			40	
	DM7441A	V_{CC} = 5.25V		25°			1.8	
				0°			1.8	
				−55°			1.8	
Logical 0 Output Voltage	DM5441A	V_{CC} = 4.5V	I_{OUT} = 7 mA	125°			3.0	V
				70°			2.5	
	DM7441A	V_{CC} = 4.75V		25°		1.4	2.5	
				0°			2.5	
				−55°			2.5	

Note 1: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5441A, and the 0°C to +70°C temperature range for the DM7441A.

Note 2: All typicals apply at 25°C for V_{CC} = 5V.

Display Drivers

DM5445/DM7445
DM54145/DM74145
BCD-to-decimal decoder/drivers

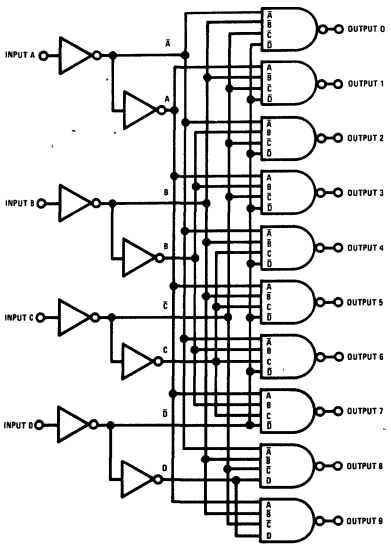
general description

The DM5442/DM7442 and DM54145/DM74145 BCD-to-decimal decoder/drivers are fully compatible for use with TTL or DTL logic circuits. Each circuit features full decoding of all valid BCD input conditions (0 to 9) ensuring that all outputs will be off for any invalid input condition. Each output transistor is capable of sinking 80 mA. In the off condition each transistor can withstand high breakdown voltages (DM5445/DM7445 = 30V and DM54145/DM74145 = 15V).

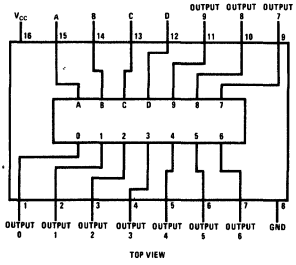
features

- 210 mW typical power dissipation
- 30 ns maximum propagation delay
- Series 54/74 compatible

logic and connection diagrams



Dual-In-Line and Flat Package



Order Number DM5445J, DM7445J, DM54145J or DM74145J
See Package 17
Order Number DM7445N or DM74145N
See Package 23
Order Number DM5445W, DM7445W, DM54145W or DM74145W
See Package 28

truth table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

6

absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5 5V
Output Voltage	DM5445/DM7445	30V
	DM54145/DM74145	15V
Operating Temperature Range		
	DM5445,DM54145	−55°C to +125°C
	DM7445,DM74145	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5445,DM54145	4.5	5.5	V
DM7445,DM74145	4 75	5.25	V

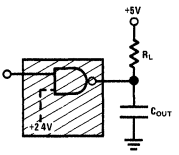
electrical characteristics (Note 2)

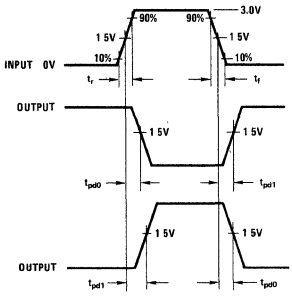
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage		2			V
Logic "0" Input Voltage				0 8	
Output Breakdown Voltage	V_{CC} = Max, I_{OFF} = 250 μA	30			V
	V_{CC} = Max, I_{OFF} = 250 μA	15			V
Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 80 mA		0 5	0 9	V
	V_{CC} = Min, I_{OUT} = 20 mA		0 2	0 4	V
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V			40	μA
	V_{CC} = Max, V_{IN} = 5 5V			1	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1 6	mA
Supply Current	V_{CC} = Max DM5445/DM54145		42	62	mA
	V_{CC} = Max DM7445/DM74145		42	70	mA
Input Clamp Voltage	V_{CC} = 5 0, T_A = 25°C, I_{IN} = −12 mA			−1 5	V
Propagation Delay to a Logical "0", t_{pd0}	V_{CC} = 5 0, T_A = 25°C, C_L = 15 pF, R_L = 100Ω		17	30	ns
Propagation Delay to a Logical "1"	V_{CC} = 5 0, T_A = 25°C, C_L = 15 pF, R_L = 100Ω		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM5445, DM54145 and across the 0°C to 70°C range for the DM7445,DM74145 All typicals are given for V_{CC} = 5 0V and T_A = 25°C

ac test circuit and switching time waveforms





FREQUENCY = 1 MHz
DUTY CYCLE = 50%
$t_r = t_f$ = 10 ns

DM5446A/DM7446A
DM5447A/DM7447A
DM5448/DM7448
BCD-to-7-segment decoder/drivers

general description

This versatile series of 7-segment display drivers fulfills a wide variety of requirements for most active high (common cathode) and active low (common anode) Light Emitting Diodes (LED) or lamp displays. Each device fully decodes a 4-bit BCD input into a number from 0 through 9 in the standard 7-segment display format, and BCD numbers above 9 into unique patterns that verify operation. All circuits operate from a single 5.0V supply.

The DM5446A/DM7446A has active-low, open-collector outputs that will drive segments requiring up to 40 mA of current. The outputs are capable of withstanding 30V at a maximum leakage current of 250μA. This configuration is particularly well suited for common anode LED displays or higher voltage lamp displays. The high sink current capability also allows this circuit to be used in the multiplex or nonmultiplex mode of display drive. In addition, the device may be used to drive logic circuits since its normalized fanout is 25.

The DM5447A/DM7447A has the same output characteristics as the DM5446A/DM7446A except that the outputs withstand 15V at a maximum leakage current of 250μA. Since its output configuration is the same as the DM5446A/DM7446A its applications will also be the same, the only restriction is that a lower voltage type display be used because of the reduced output voltage limit of 15V.

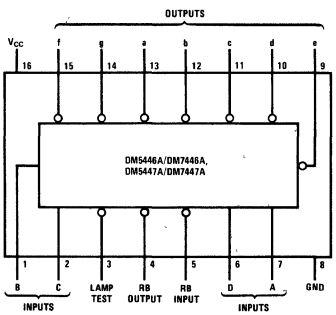
The DM5448/DM7448 has active-high, passive-pull up outputs with a fanout of 4. Typical source current is 2.0 mA at an output voltage of 0.85V. The sink capability is 6.4 mA at a maximum voltage of 0.4V. It is normally used to drive logic circuits, operate high-voltage loads such as electroluminescent displays through buffer transistors or SCR switches, and in low current common cathode Non-Multiplex LED applications.

features

- Lamp-test input
- Leading/trailing zero suppression (RBI and RBO)
- Blanking input that may be used to modulate lamp intensity or inhibit output
- TTL and DTL compatible
- Input clamping diodes

connection diagrams

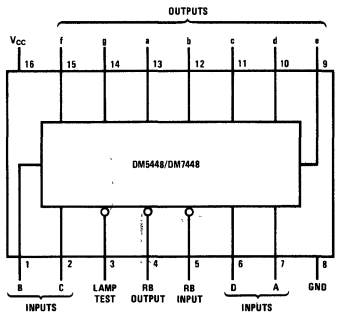
Dual-In-Line and Flat Package



TOP VIEW

Order Number DM5446AJ, DM7446AJ, DM5447AJ, DM7447AJ, DM5448J, or DM7448J
See Package 17

Dual-In-Line and Flat Package



TOP VIEW

Order Number DM5446AN, DM7446AN, DM5447AN, DM7447AN, DM5448N, or DM7448N
See Package 23

Order Number DM5446AW, DM7446AW, DM5447AW, DM7447AW, DM5448W or DM7448W
See Package 28

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absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5446A, DM5447A, DM5448	4.5	5.5	V
DM7446A, DM7447, DM7448	4.75	5.25	V
Temperature (T_A)			
DM5446A, DM5447A, DM5448	−55	+125	°C
DM7446A, DM7447A, DM7448	0	+70	°C
Output Voltage			
DM5446A, DM7446A		30	V
DM5447A, DM7447A		15	V
DM5448, DM7448		5.5	V
Output Sink Current (per segment)			
DM5446A, DM7446A,		40	mA
DM5447A, DM7447A		40	mA
DM5448, DM7448		6.4	mA

electrical characteristics (Note 2) The following is applicable to all parts.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2.0			V
Logical "0" Input Votlage				0.8	V
Logical "1" Output Voltage BI/RBO Node	V_{CC} = Min, I_{OUT} = −200μA	2.4	3 7		V
Logical "0" Output Voltage at BI/RBO Node	V_{CC} = Min, I_{IN} = 8.0 mA		0.3	0.4	V
Logical "1" Input Current at any Input Except BI/RBO Node	V_{CC} = Max, V_{IN} = 2.4V V_{CC} = Max, V_{IN} = 5.5V			40 1.0	μA mA
Logical "0" Input Current (Except BI/RBO Node)	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Logical "0" Input Current BI/RBO Node	V_{CC} = Max, V_{IN} = 0.4V			−4.2	mA
Output Short Circuit Current at BI/RBO Node	V_{CC} = Max			−4.0	mA
Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V

output characteristics and supply current

DM5446A/DM7446A, DM5447A/DM7447A (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Output Voltage Outputs a through g					
DM5446A, DM7446A	V_{CC} = Max, I_{OUT} = 250μA	30			V
DM5447A, DM7447A		15			V
Logical "0" Output Voltage Outputs a through g	V_{CC} = Min, I_{OUT} = 40 mA		0 3	0 4	V
Supply Current					
DM5446A, DM5447A	V_{CC} = Max		60	85	mA
DM7446A, DM7447A			60	103	mA

output characteristics and supply current

DM5448/DM7448 (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Output Voltage Outputs a through g DM5448, DM7448	V_{CC} = Min, I_{OUT} = −400μA	2.4	3.2		V
Logical "0" Output Voltage Outputs a through g	V_{CC} = Min, I_{OUT} = 6.4 mA		0.25	0.4	V
Logical "1" Load Current Available, Outputs a through g	V_{CC} = Min, V_{OUT} = 0.85V	−1.3	−2.0		mA
Output Short Circuit Current Outputs a through g (Note 3)	V_{CC} = Max		−3.0	−4.0	mA
Supply Current DM5448	V_{CC} = Max		50	76	mA
DM7448			50	90	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM5446A, DM5447A, and DM5448, and across the 0°C to +70°C range for DM7446A, DM7447A, and DM7448. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

switching characteristics

DM5446A/DM7446A, DM5447A/DM7447A, DM5448/DM7448 (V_{CC} = 5.0V, T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a Logical "0" from A Input to any Output (t_{pd0})					
DM5446A/DM7446A	C_L = 15 pF, R_L = 120Ω			100	ns
DM5447A/DM7447A	C_L = 15 pF, R_L = 120Ω			100	ns
DM5448	C_L = 15 pF, R_L = 1kΩ			100	ns
DM7448	C_L = 15 pF, R_L = 667Ω			100	ns
Propagation Delay to a Logical "0" from RBI to any Output (t_{pd0})					
DM5446A/DM7446A	C_L = 15 pF, R_L = 120Ω			100	ns
DM5447A/DM7447A	C_L = 15 pF, R_L = 120Ω			100	ns
DM5448	C_L = 15 pF, R_L = 1kΩ			100	ns
DM7448	C_L = 15 pF, R_L = 667Ω			100	ns
Propagation Delay to a Logical "1" from A Input to any Output (t_{pd1})					
DM5446A/DM7446A	C_L = 15 pF, R_L = 120Ω			100	ns
DM5447A/DM7447A	C_L = 15 pF, R_L = 120Ω			100	ns
DM5448	C_L = 15 pF, R_L = 1kΩ			100	ns
DM7448	C_L = 15 pF, R_L = 667Ω			100	ns
Propagation Delay to a Logical "1" from RBI to any Output (t_{pd1})					
DM5446A/DM7446A	C_L = 15 pF, R_L = 120Ω			100	ns
DM5447A/DM7447A	C_L = 15 pF, R_L = 120Ω			100	ns
DM5448	C_L = 15 pF, R_L = 1kΩ			100	ns
DM7448	C_L = 15 pF, R_L = 667Ω			100	ns

truth tables

DM5446A/DM7446A, DM5447A/DM7447A

DECIMAL OR FUNCTION	INPUTS LT	RBI	D	C	B	A	BI/RBO	OUTPUTS a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1	
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0	4

Note 1: BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical 1 when output functions 0 through 15 are desired, and the ripple-blanking input (RBI) must be open or at a logical 1 if blanking of a decimal 0 is not desired. X = input may be high or low.

Note 2: When a logical 0 is applied directly to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition

Note 3: When the ripple-blanking input (RBI) and inputs A, B, C, and D are at logical 0, with the lamp test input at logical 1, all segment outputs go to a logical 1 and the ripple-blanking output (RBO) goes to a logical 0 (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical 1, and a logical 0 is applied to the lamp-test input, all segment outputs go to a logical 0.

DM5448/DM7448

DECIMAL OR FUNCTION	INPUTS LT	RBI	D	C	B	A	BI/RBO	OUTPUTS a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

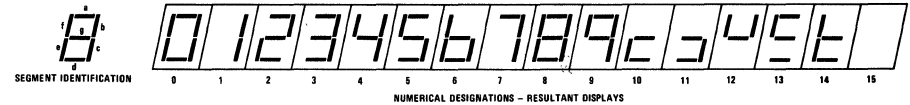
Note 1: BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical 1 when output functions 0 through 15 are desired, and the ripple-blanking input (RBI) must be open or at a logical 1 if blanking of a decimal 0 is not desired. X = input may be high or low.

Note 2: When a logical 0 is applied directly to the blanking input (forced condition) all segment outputs go to a logical 0 regardless of the state of any other input condition.

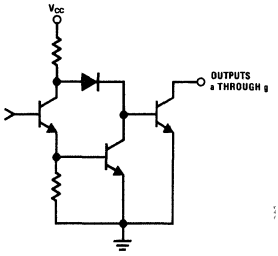
Note 3: When the ripple-blanking input (RBI) and inputs A, B, C, and D are at logical 0, with the lamp test at logical 1 all segment outputs go to the logical 0 and the ripple blanking output (RBO) goes to a logical 0 (response condition).

Note 4: When the blanking input/ripple-blanking output (RI/RBO) is open or held at a logical 1, and a logical 0 is applied to the lamp-test input, all segment outputs go to a logical 1.

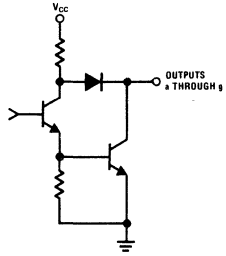
output display



output stage schematics

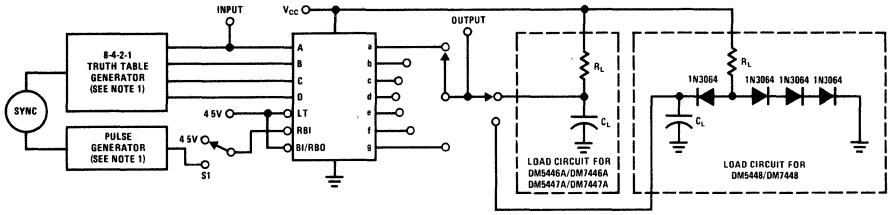


DM5446A/DM7446A
DM5447A/DM7447A

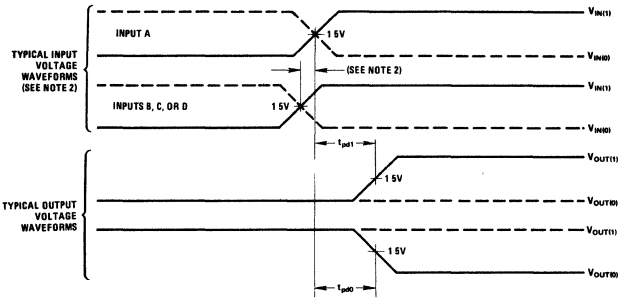


DM5448/DM7448

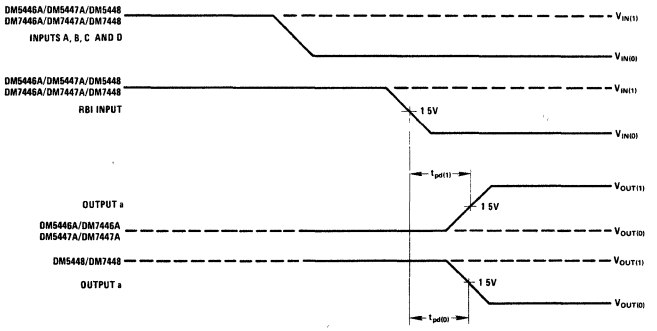
ac test circuit



switching time waveforms



A Input to Outputs



RBI Input to Outputs

Note 1 The truth table generator and pulse generator have the following characteristics: $V_{OUT(1)} \geq 2.4V$, $V_{OUT(0)} \leq 0.4V$, t_r and $t_f \leq 10$ ns, and PRR = 1.0 MHz

Note 2 Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions RBI = 4.5V.

Note 3 C_L includes probe and jig capacitance.

6

Display Drivers

DM54141/DM74141
BCD to decimal decoder/driver

general description

The DM54141/DM74141 is a second-generation BCD to decimal decoder designed specifically to drive cold cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

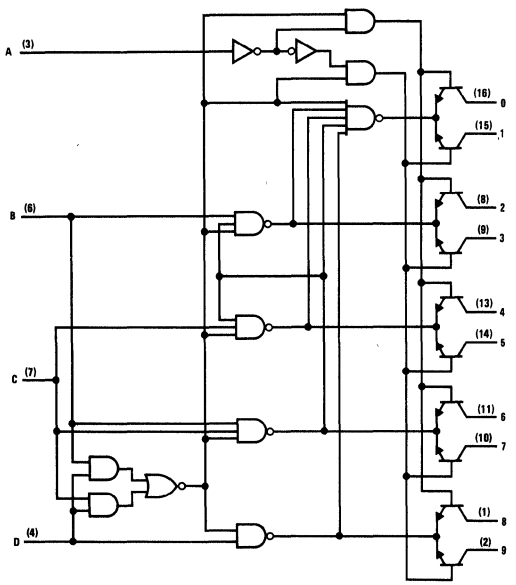
Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the DM54141/DM74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The ten high-performance NPN output transistors have a maximum reverse current of 50μA at 55V.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 mW, which is about one-half the power requirement of earlier designs.

features

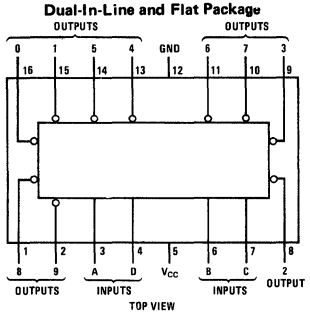
- Drives cold cathode numeric indicator tubes directly
- Low leakage current at 55V 50μA max
- Low power dissipation of 55 mW typ
- Fully decoded inputs ensure all outputs off for invalid codes
- Input clamp diodes for minimizing transmission line effects

logic diagram



connection diagram

Dual-In-Line and Flat Package



Order Number DM54141J or DM74141J
See Package 17
Order Number DM74141N
See Package 23
Order Number DM54141W or DM74141W
See Package 28

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	60V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM74141	4.75	5.25	V
DM54141	4.5	5.5	V
Temperature, T_A			
DM74141	0	+70	°C
DM54141	−55	+125	°C

electrical characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})	V_{CC} = Min	2 0			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max, V_{IH} = 5 5V			0.1	mA
A Input	V_{CC} = Max, V_{IH} = 2.4V			40	μA
B, C, or D Input	V_{CC} = Max, V_{IH} = 2 4V			80	μA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Min			0 8	V
Logical "0" Input Current (I_{IL})					
A Input	V_{CC} = Max, V_{IL} = 0.4V			−1 6	mA
B, C, or D Input	V_{CC} = Max, V_{IL} = 0.4V			−3.2	mA
Input Clamp Voltage (V_{CD})	V_{CC} = Min, I_{CD} = −12 mA			−1 5	V
Logical "1" Output Voltage (V_{OH})	V_{CC} = Max, I_{OH} = 0 5 mA	60			V
Logical "1" Output Current (I_{OH})	V_{CC} = Max, V_O = 55V			50	μA
	V_{CC} = Max, V_O = 30V Input States 10–15			5 0	μA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OL} = 7.0 mA			2 5	V
Supply Current (I_{CC})	V_{CC} = Max, All Inputs GND, All Outputs Open		11	25	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54141 and across the 0°C to +70°C range for the DM74141. All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

truth table

INPUT D	C	B	A	OUTPUT ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level

†All other outputs are off

Display Drivers

DM75491 MOS-to-LED quad segment driver
DM75492 MOS-to-LED hex digit driver

general description

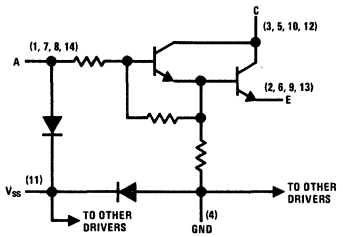
The DM75491 and DM75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

features

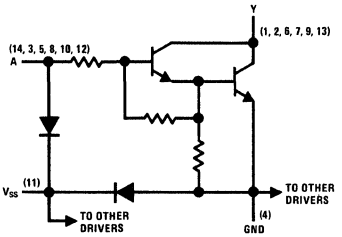
- Source or sink capability per driver (DM75491) 50 mA
- Sink capability per driver (DM75492) 250 mA
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

schematic and connection diagrams

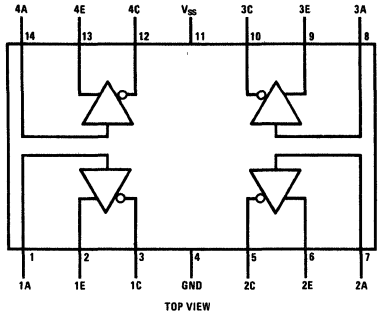
DM75491 (each driver)



DM75492 (each driver)

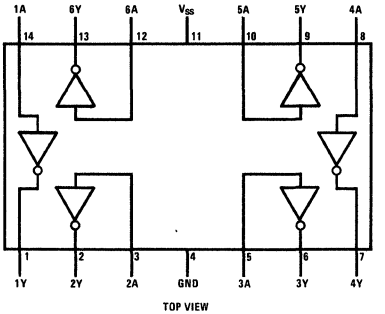


DM75491 Dual-In-Line Package



TOP VIEW

DM75492 Dual-In-Line Package



TOP VIEW

Order Number DM75491J or DM75492J
See Package 16
Order Number DM75491N or DM75492N
See Package 22

absolute maximum ratings

	DM75491	DM75492
Input Voltage Range (Note 1)	−5V to V_{SS}	−5V to V_{SS}
Collector Output Voltage (Note 2)	10V	10V
Collector Output to Input Voltage	10V	10V
Emitter to Ground Voltage ($V_I \geq 5V$)	10V	
Emitter to Input Voltage	5V	
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V
Collector Output Current		
Each Collector Output	50 mA	250 mA
All Collector Outputs	200 mA	600 mA
Continuous Total Dissipation	800 mW	800 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C

dc electrical characteristics

DM75491 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On State Collector Emitter Voltage ($V_{CE\ ON}$)	Input = 8 5V through 1 kΩ, V_E = 5V, I_C = 50 mA, T_A = 25°C		.9	1 2	V
On State Collector Emitter Voltage ($V_{CE\ ON}$)	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA			1.5	V
Off State Collector Current ($I_{C\ OFF}$)	V_C = 10V, V_E = 0, I_{IN} = 40μA			100	μA
Off State Collector Current ($I_{C\ OFF}$)	V_C = 10V, V_E = 0, V_{IN} = .7V			100	μA
Input Current at Maximum Input Voltage (I_I)	V_{IN} = 10V, V_E = 0, I_C = 20 mA		2.2	3.3	mA
Emitter Reverse Current (I_E)	V_{IN} = 0, V_E = 5V, I_C = 0			100	μA
Current Into V_{SS} Terminal (I_{SS})				1	mA

DM75492 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Level Output Voltage (V_{OL})	Input = 6 5V through 1 kΩ, I_{OUT} = 250 mA T_A = 25°C		.9	1.2	V
Low Level Output Voltage (V_{OL})	Input = 6 5V through 1 kΩ, I_{OUT} = 250 mA			1.5	V
High Level Output Current (I_{OH})	V_{OH} = 10V, I_{IN} = 40μA			200	μA
High Level Output Current (I_{OH})	V_{OH} = 10V, V_{IN} = .5V			200	μA
Input Current at Maximum Input Voltage (I_I)	V_{IN} = 10V, I_{OL} = 20 mA		2.2	3.3	mA
Current Into V_{SS} Terminal (I_{SS})				1	mA

ac switching characteristics

DM75491 (V_{SS} = 7.5V, T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (Collector) (t_{PLH})	V_{IH} = 4 5V, V_E = 0,		100		ns
Propagation Delay Time, High to Low Level Output (Collector) (t_{PHL})	R_L = 200Ω, C_L = 15 pF		20		ns

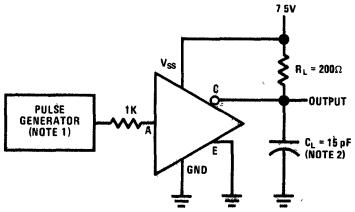
DM75492 (V_{SS} = 7.5V, T_A = 25°C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level Output (t_{PLH})	V_{IH} = 7.5V, R_L = 39Ω,		300		ns
Propagation Delay Time, High to Low Level Output (t_{PHL})	C_L = 15 pF		30		ns

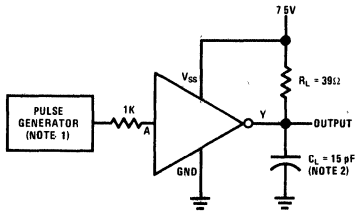
Note 1: The input is the only device terminal which may be negative with respect to ground.
Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

6

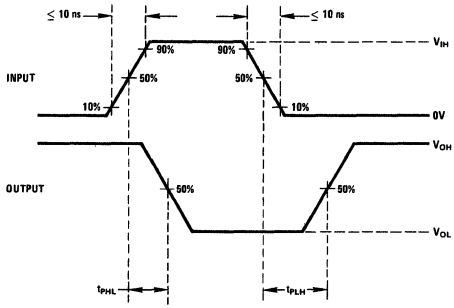
ac test circuits and switching time waveforms



DM75491



DM75492



NOTE 1 THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS Z_{OUT} = 50Ω, PRR = 100 KHz, t_W = 1 μs.

NOTE 2: C_L INCLUDES PROBE AND JIG CAPACITANCE

Display Drivers

DM75493 quad LED segment driver

general description

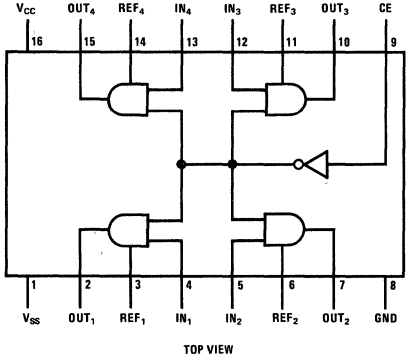
The DM75493 is a quad LED segment driver. It is designed to interface between MOS IC's and LED's. An external resistor is required for each segment to drive the output current which is approximately equal to $0.7V/R_L$ and is relatively constant, independent of supply variations. Blanking can be achieved by taking the chip enable (CE) to a logical "1" level.

features

- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Output current regulation
- Quad high gain circuits

logic and connection diagram

Dual-In-Line Package

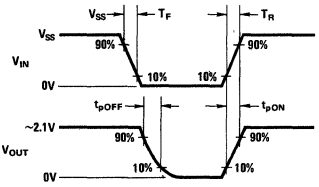


TOP VIEW

Order Number DM75493J
See Package 17

Order Number DM75493N
See Package 23

switching time waveforms



truth table

CE	V_{IN}	I_{OUT}
0	1	ON
0	0	OFF
1	X	OFF

X = Don't care

absolute maximum ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	V_{CC}
Storage Temperature Range	+65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC}	3.2	8.8	V
V_{SS}	6.5	8.8	V
Temperature, T_A	0	+70	°C

electrical characteristics ($V_{SS} \geq V_{CC}$)

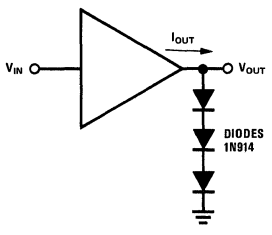
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current into V_{CC} Terminal (I_{CC})	V_{CC} = 8.8V, V_{SS} = 8.8V, All Other Pins to GND			40	μA
Current into V_{SS} Terminal (I_{SS})	V_{SS} = 8.8V, All Other Pins to GND			40	μA
	V_{REF} = 2.15V, V_{IN} = 8 8V, V_{CE} = 8.8V through 100kΩ, R_L = 50Ω		0 5	1.5	mA
	V_{REF} = Open, V_{OUT} = Open, R_L = 50Ω, V_{CC} = 3.2V, V_{CE} = 0V, V_{IN} = 8.8V			1.4	mA
Chip Enable Current (I_{CE})	V_{CE} = 8.8V, V_{CC} = 8.8V, V_{SS} = 8.8V, All Other Pins to GND			2.1	mA
Input Current (I_{IN})	V_{IN} = 8 8V, V_{CE} = 0V, V_{REF} = 0V, V_{OUT} = 0V			3.2	mA
	V_{IN} = 8.8V, V_{CE} = 8 8V, V_{REF} = 0V, V_{OUT} = 0V			3 6	mA
Output Leakage Current (I_{OL})	V_{CE} = 0V, V_{REF} = 0V, V_{OUT} = 0V, V_{IN} = 8 8V through 100kΩ, Measure Current to GND			100	μA
	V_{CE} = 6.5V through 1.0kΩ, V_{IN} = 3 8V, V_{REF} = 0V, V_{OUT} = 0V, Measure Current to GND			200	μA
Current into Reference Terminal (I_{REF})	V_{SS} = 6.5V, V_{REF} = 2.15V, R_L = 50Ω, I_{CE} = 80μA, V_{IN} = 6.5V through 1.0kΩ, V_{CC} = 3.2V	−8.0	13		mA
	V_{REF} = 2.15V, V_{CE} = 0V, R_L = 50Ω, V_{IN} = 8 8V		16	−20	mA
Propagation Delay to a Logical "0" from Input to Output ($t_{pd\,OFF}$)	T_A = 25°C, See AC Test Circuits		170	300	ns
Propagation Delay to a Logical "1" from Input to Output ($t_{pd\,ON}$)	T_A = 25°C, See AC Test Circuits		11	100	ns

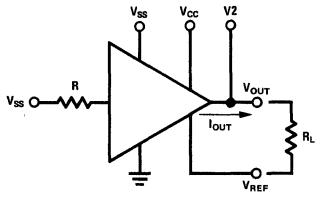
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DM75493. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

ac test circuits





Display Drivers

DM75494 hex digit driver

general description

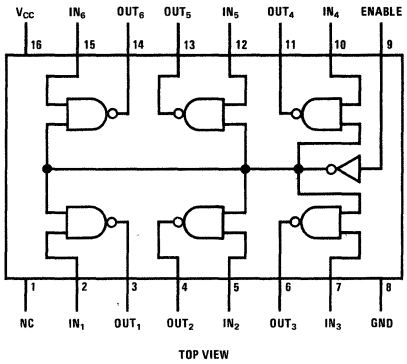
The DM75494 is a hex digit driver. It is designed to interface between most MOS devices and common cathodes configured LED's with a low output voltage at high operating currents. The enable input disables all the outputs when taken high.

features

- 150 mA sink capability
- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Low voltage saturating outputs
- Hex high gain circuits

logic and connection diagram

Dual-In-Line Package

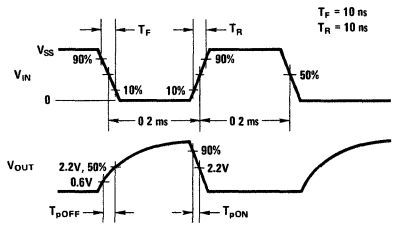


TOP VIEW

Order Number DM75494J
See Package 17

Order Number DM75494N
See Package 23

switching time waveforms



truth table

ENABLE	V_{IN}	V_{OUT}
0	0	1
0	1	0
1	X	1

X = don't care

6

absolute maximum ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	3.2	8.8	V
Temperature, T_A	0	+70	°C

electrical characteristics (Notes 2 and 3)

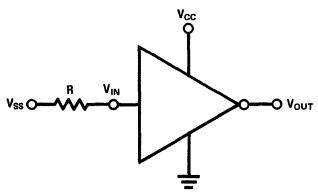
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Current (I_{IH})	V_{CC} = Min, V_{IN} = 8.8V, V_{CE} = 8.8V through 100k			2.0	mA
	V_{CC} = Min, V_{IN} = 8.8V, V_{CE} = 8.8V			2.7	mA
Logical "0" Input Current (I_{IL})	V_{CC} = Max, V_{IN} = −5.5V			−20	μA
Logical "1" Output Current (I_{OH})	V_{CC} = Max, V_{IN} = 8.8V through 100k, V_{OH} = 8.8V, V_{CE} = 0V			400	μA
	V_{CC} = Max, V_{IN} = 8.8V, V_{OH} = 8.8V, V_{CE} = 6.5V through 1.0k			400	μA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OL} = 150 mA, V_{IN} = 6.5V through 1.0k, V_{CE} = 8.8V through 100k		0.25	0.35	V
Supply Current (I_{CC})	V_{CC} = Max, One Driver ON, V_{IN} = 8.8V			8.0	mA
	V_{CC} = Max, V_{CE} = 6.5V through 1.0k All Other Pins to GND			100	μA
	V_{CC} = Max, All Pins to GND			40	μA
	V_{CC} = Max, V_{IN} = 8.8V through 100k All Other Pins to GND			100	μA
t_{OFF}	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits		0.04	1.2	μs
t_{ON}	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See AC Test Circuits		13	100	ns

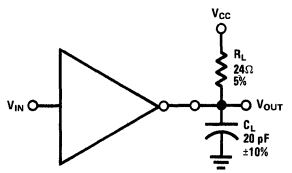
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DM75494.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

ac test circuits





DM7856/DM8856, DM8857, DM7858/DM8858
BCD-to-7-segment LED drivers

general description

This series of 7-segment display drivers fulfills a wide variety of requirements for most active high (common cathode) Light Emitting Diodes (LEDs). Each device fully decodes a 4-bit BCD input into a number from 0 through 9 in the standard 7-segment display format, and BCD numbers above 9 into unique patterns that verify operation. All circuits operate off of a single 5.0V supply.

The DM7856/DM8856 has active-high, passive pull-up outputs which provide a typical source current of 6.0 mA at an output voltage of 1.7V. The applications are the same as for the DM5448/DM7448 except that more design freedom is allowed with higher source current levels. This circuit was designed to drive the MAN-4 or equivalent type display directly without the use of external current limit resistors.

The DM8857 has active-high outputs and is designed to be used with common cathode LED's in the multiplex mode. It provides a typical source current of 50 mA at an output voltage of 2.3V.

In addition, with the use of an external current limit resistor per segment, this circuit can be used in higher current nonmultiplex LED applications.

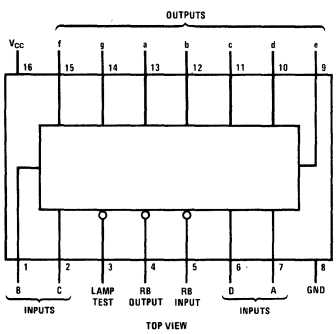
The DM7858/DM8858 has active high outputs with source current adjustable with the use of external current limit resistors, one per segment. This feature allows extreme flexibility in source current value selection for either multiplex or non-multiplex common cathode LED drive applications. It allows the system designer freedom to tailor the drive current for his particular applications.

features

- Lamp-test input
- Leading/trailing zero suppression (RBI and RBO)
- Blanking input that may be used to modulate lamp intensity or inhibit output
- TTL and DTL compatible
- Input clamping diodes

connection diagram

Dual-In-Line and Flat Package



Order Number DM7856J, DM8856J, DM8857J, DM7858J, DM8858J
See Package 17

Order Number DM7856N, DM8856N, DM7858N or DM8858N
See Package 23

Order Number DM7856W, DM8856W, DM7858W or DM8858W
See Package 28

output display

6

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7856, DM7858	4.5	5.5	V
DM8856, DM8857, DM8858	4.75	5.25	V
Temperature (T_A)			
DM7856, DM7858	−55	+125	°C
DM8856, DM8857, DM8858	0	+70	°C
Output Voltage			
All Circuits		5.5	V
Output Sink Current (per Segment)			
DM7856, DM8856		6.4	mA
Output Source Current (per Segment)			
DM8857		60	mA
DM7858, DM8858		50	mA

electrical characteristics (Note 2) The following is applicable to all parts.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2.0			V
Logical "0" Input Votlage				0.8	V
Logical "1" Output Voltage BI/RBO Node	V_{CC} = Min, I_{OUT} = −200μA	2 4	3 7		V
Logical "0" Output Voltage at BI/RBO Node	V_{CC} = Min, I_{IN} = 8.0 mA		0.3	0.4	V
Logical "1" Input Current at any Input Except BI/RBO Node	V_{CC} = Max, V_{IN} = 2.4V V_{CC} = Max, V_{IN} = 5.5V			40 1.0	μA mA
Logical "0" Input Current (Except BI/RBO Node)	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Logical "0" Input Current BI/RBO Node	V_{CC} = Max, V_{IN} = 0.4V			−4.2	mA
Output Short Circuit Current at BI/RBO Node	V_{CC} = Max			−4.0	mA
Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA			−1.5	V

output characteristics and supply current

DM7856/DM8856 (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "0" Output Voltage Outputs a through g	V_{CC} = Min, I_{OUT} = 6.4 mA		0.25	0.4	V
Logical "1" Load Current Available, Outputs a through g	V_{CC} = 5 0V, V_{OUT} = 1.7V	−4.7	−6 0	−7.5	mA
Output Short Circuit Current Outputs a through g (Note 3)	V_{CC} = Max		−12	−15	mA
Supply Current					
DM7856	V_{CC} = Max		90	120	mA
DM8856			90	130	mA

output characteristics and supply current (con't)

DM8857, DM7858/DM8858 (Notes 2 and 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Load Current Available, Outputs a through g					
DM8857	V_{CC} = 5.0V, V_{OUT} = 2 3V	−40		−60	mA
DM7858 (Note 4)	V_{CC} = 5 0V, I_{OUT} = −50 mA	2 7	3 2		V
DM8858 (Note 4)	V_{CC} = 5 0V, I_{OUT} = −50 mA	2.9	3 2		V
Supply Current	V_{CC} = Max			60	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM7856, and DM7858 and across the 0°C to +70°C range for DM8856, DM8857, and DM8858. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Care must be taken in not shorting the outputs to ground while they are in the "1" state because excessive current flow would result from the Darlington upper stages.

Note 4: Special care must be taken in the use of the DM7858 ceramic (J) and the DM8858 plastic (N) DIP's with regard to not exceeding the maximum operating junction temperature of the devices. The maximum junction temperature of the DM7858J is 150°C and must be derated based on a thermal resistance of 80°C/watt, junction to ambient. The maximum junction temperature for the DM8858N is 150°C and must be derated based on a thermal resistance of 140°C/watt junction to ambient.

truth table

INPUTS								OUTPUTS							
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

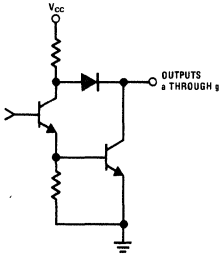
Note 1: BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical 1 when output functions 0 through 15 are desired, and the ripple-blanking input (RBI) must be open or at a logical 1 if blanking of a decimal 0 is not desired. X = input may be high or low.

Note 2: When a logical 0 is applied directly to the blanking input (forced condition) all segment outputs go to a logical 1 regardless of the state of any other input condition

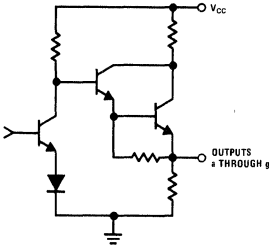
Note 3: When the ripple-blanking input (RBI) and inputs A, B, C, and D are at logical 0, with the lamp test input at logical 1, all segment outputs go to a logical 1 and the ripple-blanking output (RBO) goes to a logical 0 (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical 1, and a logical 0 is applied to the lamp-test input, all segment outputs go to a logical 0.

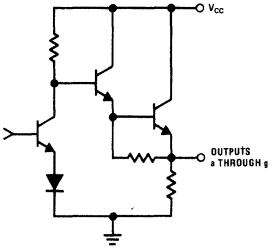
output stage schematics



DM7856/DM8856



DM8857



DM7858/DM8858

Display Drivers

DM8859, DM8869 TTL compatible hex LED drivers

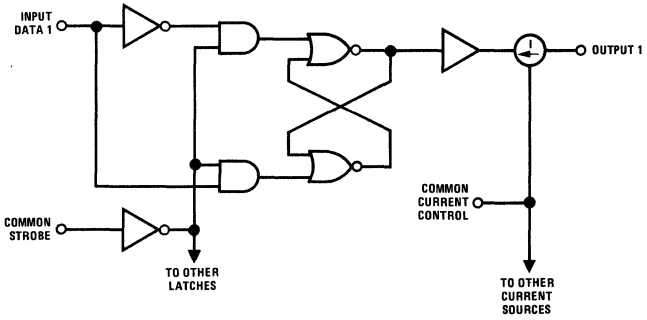
general description

The DM8859, DM8869 are TTL compatible hex LED drivers with programmable current source outputs. The current sources are nominally set at 20 mA but may be adjusted by external resistors for any value between 0–50 mA. Each device contains six latches which may be set by input data terminals. A strobe common to all six latches enables the data input terminals. The DM8859 current source outputs are switched on by entering a high level into the latches and the DM8869 current source outputs are switched on by entering a low level into the latches.

The devices are available in either a molded or cavity package. In order not to damage the devices there is a limit placed on the power dissipation allowable for each package type. This information is shown in the graph on the back page.

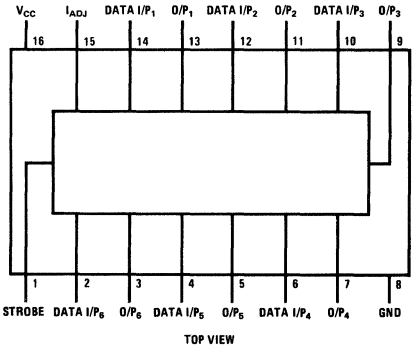
schematic diagram

DM8859



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM8859J or DM8869J
See Package 17

Order Number DM8859N or DM8869N
See Package 23

truth table

COMMON STROBE	I/P	DM8859 O/P (t+1)	DM8869 O/P (t+1)
0	0	OFF	ON
0	1	ON	OFF
1	X	O/P (t)	O/P (t)

6

absolute maximum ratings (Note 1)

Supply Voltage	+7.0V
Input Voltage	+5.5V
Output Voltage	+5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM8859, DM8869	4.75	5.25	V
Temperature (T_A)			
DM8859, DM8869	0	+70	°C

electrical characteristics (Note 2)

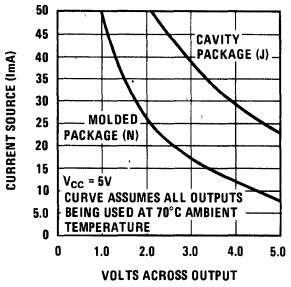
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.75V	2 0			V
Logical "0" Input Voltage	V_{CC} = 4.75V			0 8	V
Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V			40	μA
Logical "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V		−1 0	−1 6	mA
Typical Output Current	V_{CC} = 5.0V, I_{ADJ} Pin Open, 25°C		20		mA
Supply Current (each device)	V_{CC} = 5.25V, Current Sources "Off"			50	mA
Input Clamp Voltage	I_{IN} = −12 mA		−1.1	−1.5	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

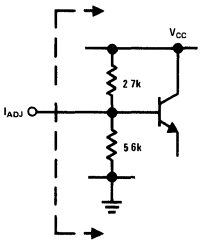
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DM8859 and the DM8869. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

typical performance characteristics

Max Power Dissipation Curves



test circuit



I_{ADJ} may be programmed by a voltage source or by resistors.

Display Drivers

DM8861 MOS-to-LED 5-segment driver

general description

The DM8861 is designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays.

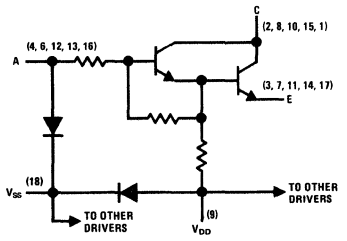
The DM8861 is a 5-segment driver capable of sinking or sourcing up to 50 mA from each driver.

features

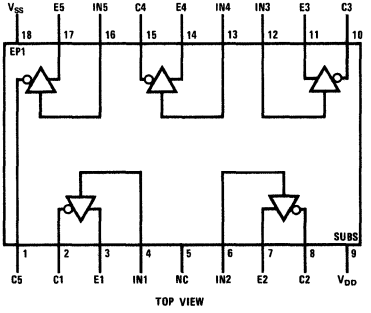
- Source or sink capability per driver 50 mA
- MOS compatibility (low input current)
- Low standby power
- High gain Darlington circuits

schematic and connection diagrams

DM8861



Dual-In-Line Package



TOP VIEW

Order Number DM8861N
See Package 25

absolute maximum ratings

Input Voltage Range (Note 1)	−5V to V_{SS}
Collector (Output) Voltage (Note 2)	10V
Collector (Output)-to-Input Voltage	10V
Emitter-to-Ground Voltage ($V_I \geq 5V$)	10V
Emitter-to-Input Voltage	5V
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V
Collector (Output) Current	
Each Collector (Output)	50 mA
All Collectors (Output)	200 mA
Continuous Total Dissipation	800 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics

DM8861 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
On State Collector Emitter Voltage ($V_{CE\ ON}$)	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA, T_A = 25°C		.9	1.2	V
On State Collector Emitter Voltage ($V_{CE\ ON}$)	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA			1.5	V
Off State Collector Current ($I_{C\ OFF}$)	V_C = 10V, V_E = 0, I_{IN} = 40μA			100	μA
Off Set Collector Current ($I_{C\ OFF}$)	V_C = 10V, V_E = 0, V_{IN} = .7V			100	μA
Input Current at Maximum Input Voltage (I_I)	V_{IN} = 10V, V_E = 0, I_C = 20 mA		2.2	3.3	mA
Emitter Reverse Current (I_E)	V_{IN} = 0, V_E = 5V, I_C = 0			100	μA
Current Into V_{SS} Terminal (I_{SS})				1	mA

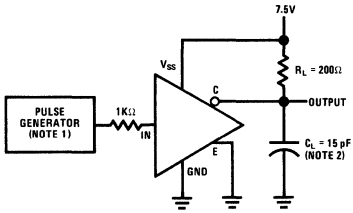
ac switching characteristics

DM8861 (V_{SS} = 7.5V, T_A = 25°C)

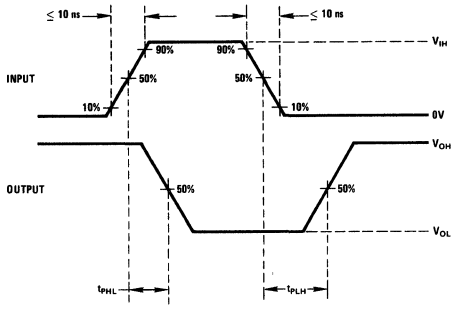
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time, Low to High Level Output (Collector) (t_{PLH})	V_{IH} = 4.5V, V_E = 0		100		ns
Propagation Delay Time, High to Low Level Output (Collector) (t_{PHL})	R_L = 200Ω, C_L = 15 pF		20		ns

Note 1: The input is the only device terminal which may be negative with respect to ground.
Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

ac test circuits and waveforms



DM8861



NOTE 1 THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS Z_{OUT} = 50Ω, PRR = 100 KHz, t_W = 1μs

NOTE 2 C_L INCLUDES PROBE AND JIG CAPACITANCE

Display Drivers

DM8864, DM8865, DM8866 LED cathode drivers

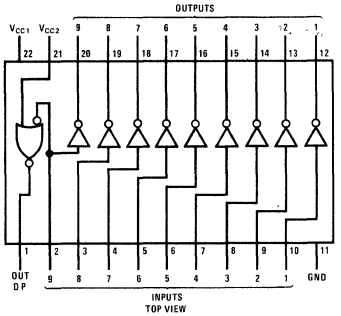
general description

The DM8864, DM8865 and DM8866 are cathode drivers for 9, 8, and 7 digit LED displays respectively. They are designed to interface between MOS calculator or clock circuits supplying 2.0 mA, and LED displays operating up to 50 mA in a multiplex mode. The DM8864 and DM8866 feature a "low battery" indicator driver which will light a decimal point whenever a 9.0V battery drops below 6.5V typical.

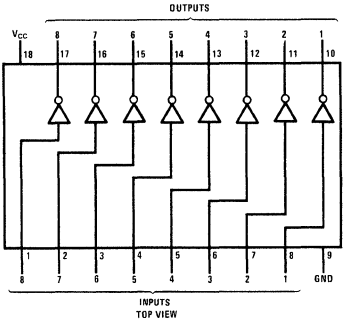
features

- Used with 50 mA LED displays
- "Low battery voltage" indicator
- Directly interfaced from MOS
- Inputs and outputs clustered for easy wiring
- Drivers consume no standby power

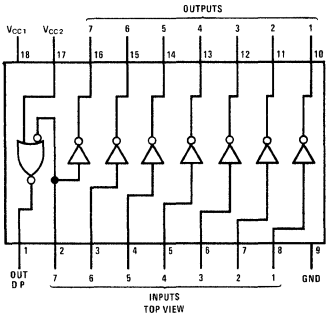
connection diagrams (Dual-In-Line Packages)



Order Number DM8864N
See Package 29

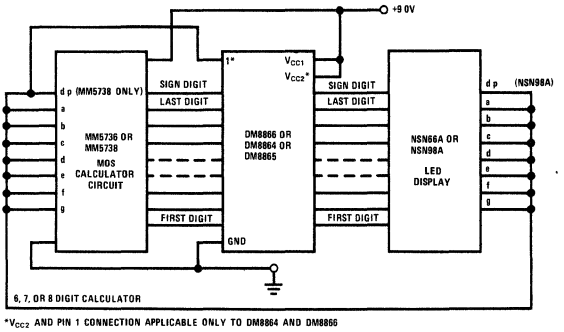


Order Number DM8865N
See Package 25



Order Number DM8866N
See Package 25

typical application



*V_{CC2} AND PIN 1 CONNECTION APPLICABLE ONLY TO DM8864 AND DM8866

absolute maximum ratings (Note 1)

Supply Voltage	11V
Input Voltage	11V
Output Voltage	8.0V
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	5.0	9.5	V
Temperature, T_A	0	+70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})	V_{CC} = Max	4.5			V
Logical "1" Input Current (I_{IH})	V_{CC} = Max, V_{IN} = 6.5V			2.0	mA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Max			0 4	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max, V_{IN} = 0.4V			60	μA
Decimal Point Output Current (Pin 1) ($I_{DP\,ON}$) (Note 3)	V_{CC} = 6.25V, V_{DP} = 3.3V, V_{IN9} = 4.5V		6 0		mA
Decimal Point Output Current (Pin 1) ($I_{DP\,OFF}$) (Note 3)	V_{CC} = 7.0V, V_{DP} = 1 0V, V_{IN9} = 4 5V		−1 0		μA
Output Leakage Current (I_{CEX})	V_{CC} = Max, V_{OH} = 6.0V, I_{IN} = 40μA			40	μA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, V_{IN} = 4 5V, I_{OL} = 50 mA			1 5	V
Supply Current (I_{CC1} or I_{CC})	V_{CC} = Max, V_{IN} = 0			0 1	mA
Supply Current (I_{CC2})	V_{CC} = Max, V_{IN9} = 4.5V			1 3	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Apply over 0°C to +70°C operating temperature range.

Note 3: Note applicable to DM8865.

Display Drivers

DM7880/DM8880 high voltage 7-segment decoder/driver (for driving Sperry and Panaplex II™ displays)

general description

The DM7880/DM8880 is custom designed to decode four lines of BCD and drive a gas-filled seven-segment display tube.

The design employs a 112-bit read-only memory which provides BCD input to full hexadecimal output decoding in the standard DM7880/DM8880 product. For applications desiring other fonts, or not using standard BCD coding, the ROM contents can be custom modified to produce any 16 output displays for the 16 binary input combinations.

Each output constitutes a switchable, adjustable current sink which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sinks have a voltage compliance from 3V to at least 80V; typically the output current varies 1% for output voltage changes of 3 to 50V. Each bit line of the ROM switches a current sink on or off as prescribed by the input code. Each current sink is ratioed to the b-output current as required for even illumination of all segments.

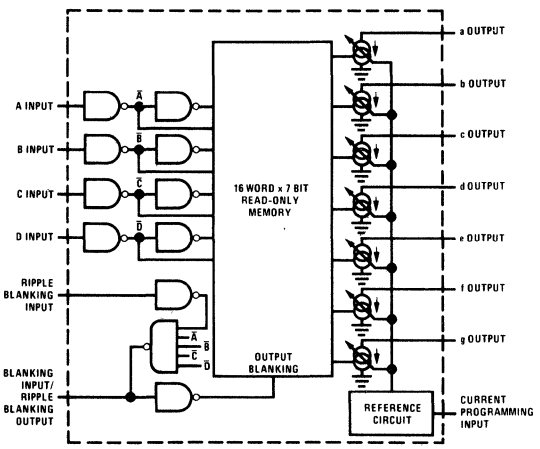
Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the Program input in accordance with the programming curve. The circuit design provides a one-to-one correlation between program input current and b-segment output current.

The Blanking Input provides unconditional blanking of any output display, while the Ripple Blanking pins allow simple leading- or trailing-zero blanking.

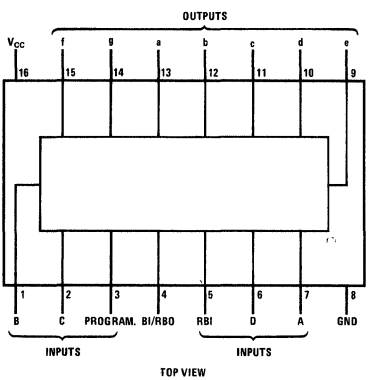
features

- Current sink outputs
- Adjustable output current – 0.2 to 1.5 mA
- High output breakdown voltage – 110V typ
- Suitable for multiplex operation
- Blanking and Ripple Blanking provisions
- Low fan-in and low power

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DM7880J or DM8880J
See Package 17
Order Number DM8880N
See Package 23

absolute maximum ratings

V_{CC}	7V
Input Voltage (Except BI)	6V
Input Voltage (BI)	V_{CC}
Segment Output Voltage	80V
Power Dissipation (Note 1)	600 mW
Transient Segment Output Current (Note 2)	50 mA
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7880	4 5	5 5	V
DM8880	4 75	5 25	V
Temperature (T_A)			
DM7880	−55	+125	C
DM8880	0	+70	C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage	V_{CC} = Min	2 0			V
Logic "0" Input Voltage	V_{CC} = Min			0 8	V
Logic "1" Output Voltage (RBO)	V_{CC} = Min, I_{OUT} = −200 μA	2 4	3 7		V
Logic "0" Output Voltage (RBO)	V_{CC} = Min, I_{OUT} = 8 mA		0 13	0 4	V
Logic "1" Input Current (Except BI)	V_{CC} = Max, V_{IN} = 2 4V		2	15	μA
	V_{CC} = Max, V_{IN} = 5 5V		4	400	μA
Logic "0" Input Current (Except BI)	V_{CC} = Max, V_{IN} = 0 4V		−300	−600	μA
Logic "0" Input Current (BI)	V_{CC} = Max, V_{IN} = 0 4V		−1 2	−2 0	mA
Power Supply Current	V_{CC} = Max, R_P = 2 2k All Inputs = 0V		27	43	mA
Input Diode Clamp Voltage	V_{CC} = Max, T_A = 25°C I_{IN} = −12 mA		-0 9	−1 5	V
Segment Outputs					
Outputs a, f, g ON Current Ratio	All Outputs = 50V Output b Curr = Ref	0 84	0 93	1 02	
Output c ON Current Ratio	All Outputs = 50V, Output b Curr = Ref	1.12	1 25	1 38	
Output d ON Current Ratio	All Outputs = 50V Output b Curr = Ref	0 90	1 00	1 10	
Output e ON Current Ratio	All Outputs = 50V Output b Curr = Ref	0 99	1 10	1.21	
Output b ON Current	V_{CC} = 5V, V_{OUT} b = 50V T_A = 25°C, R_P = 18 1k	0 18	0 20	0 22	mA
	V_{CC} = 5V, V_{OUT} b = 50V T_A = 25°C, R_P = 7.03k	0 45	0 50	0 55	mA
	V_{CC} = 5V, V_{OUT} b = 50V T_A = 25°C, R_P = 3 40k	0 90	1.00	1 10	mA
	V_{CC} = 5V, V_{OUT} b = 50V T_A = 25°C, R_P = 2 20k	1 35	1.50	1 65	mA
Output Saturation Voltage	V_{CC} = Min, R_P = 1k±5% I_{OUT} b = 2 mA (Note 4)		0.8	2.5	V
Output Leakage Current	V_{OUT} = 75V, BI = 0V		.003	3	μA
Output Breakdown Voltage	I_{OUT} = 250 μA, BI = 0V	80	110		V
Propagation Delays					
BCD Input to Segment Output	V_{CC} = 5V, T_A = 25°C		0 4	10	μs
BI to Segment Output	V_{CC} = 5V, T_A = 25°C		0 4	10	μs
RBI to Segment Output	V_{CC} = 5V, T_A = 25°C		0.7	10	μs
RBI to RBO	V_{CC} = 5V, T_A = 25°C		0 4	10	μs

Note 1: Maximum junction temperature for DM7880 is +150°C whereas that for DM8880 is +130°C. For operating at elevated temperatures the device must be derated based on a thermal resistance of 85°C/W Θ_{JA} for DM8880.

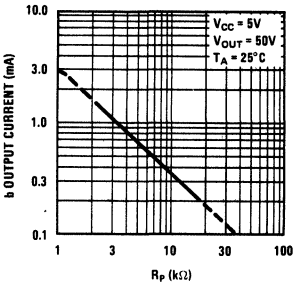
Note 2: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

Note 3. Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for DM7880 and 0°C to +70°C for DM8880, unless otherwise specified Typicals are for V_{CC} = 5 0V, T_A = +25°C. Positive current is defined as current into the referenced pin.

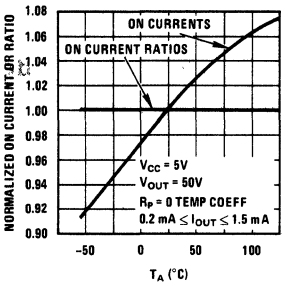
Note 4: For saturation mode the segment output currents are externally limited and ratioed

typical performance characteristics

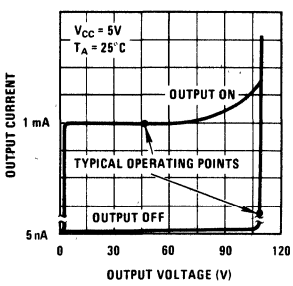
Output Current Programming



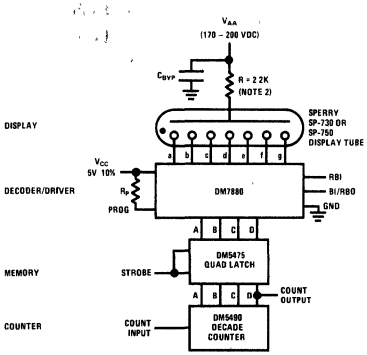
On Currents vs Temperature



Output Characteristic

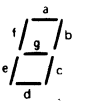


typical application



truth table

DECIMAL OR FUNCTION	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0
1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	X	0	0	1	0	1	0	0	1	0	0	1	0	2
3	X	0	0	1	1	1	0	0	0	0	1	1	0	3
4	X	0	1	0	0	1	1	0	0	1	1	0	0	4
5	X	0	1	0	1	1	0	1	0	0	1	0	0	5
6	X	0	1	1	0	1	0	1	0	0	0	0	0	6
7	X	0	1	1	1	1	0	0	0	1	1	1	1	7
8	X	1	0	0	0	1	0	0	0	0	0	0	0	8
9	X	1	0	0	1	1	0	0	0	0	1	0	0	9
10	X	1	0	1	0	1	0	0	0	1	0	0	0	A
11	X	1	0	1	1	1	1	1	0	0	0	0	0	b
12	X	1	1	0	0	1	0	1	1	0	0	0	1	C
13	X	1	1	0	1	1	1	0	0	0	0	1	0	d
14	X	1	1	1	0	1	0	1	1	0	0	0	0	E
15	X	1	1	1	1	1	0	1	1	1	0	0	0	F
BI	X	X	X	X	X	0	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	



SEGMENT IDENTIFICATION

Display Drivers

DM8884A high voltage cathode decoder/driver (for driving Panaplex II™ and Sperry displays)

general description

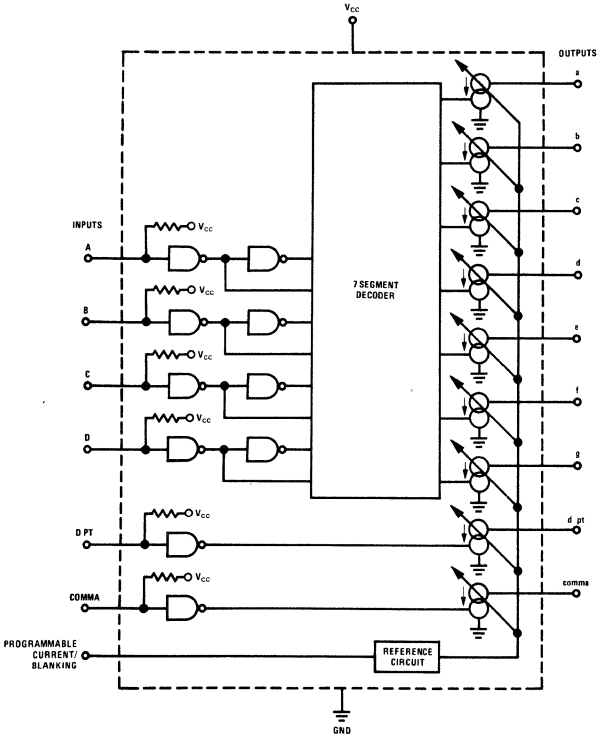
The DM8884A is designed to decode four lines of BCD input and drive seven-segment digits of gas-filled readout displays. Two separate inputs are provided for driving the decimal point and comma cathodes.

All outputs consist of switchable and programmable current sinks which provide constant current to the tube cathodes, even with high tube anode supply tolerance. Output currents may be varied over the 0.2 to 1.2 mA range for multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the program input in accordance with the programming curve.

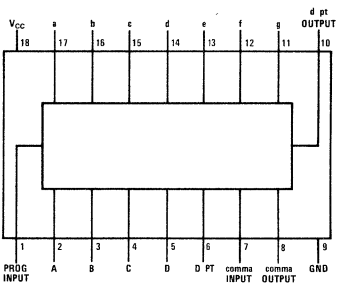
features

- Usable with AC or DC input coupling
- Current sink outputs
- High output breakdown voltage
- Low input load current
- Intended for multiplex operation.
- Input pullups increase noise immunity

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DM8884AN

See Package 25

6

absolute maximum ratings

V_{CC}	7V
Input Voltage (Note 1)	V_{CC}
Segment Output Voltage	80V
Power Dissipation (Note 2)	600 mW
Transient Segment Output Current (Note 3)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

electrical characteristics ($0°C \leq T_A \leq 70°C$ – Unless otherwise noted), $V_{CC} = 5V \pm 5\%$.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
Logic "1" Input Voltage	V_{CC} = 4.75V	2 0		V
Logic "0" Input Voltage	V_{CC} = 4.75V		1.0	V
Logic "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V		15	μA
Positive Input Clamp Voltage	V_{CC} = 4.75, I_{IN} = 1 mA	5.0		V
Logic "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V		−250	μA
Power Supply Current	V_{CC} = 5.25V, R_P = 2.8k, All Inputs = 5V		40	mA
Negative Input Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C		−1 5	V
Segment Outputs:				
All Outputs ON Current Ratio	All Outputs = 50V, Output b Current = Ref	0 9	1 1	
Output b ON Current	V_{CC} = 5V, V_{OUT} b = 50V,			
	T_A = 25°C, R_P = 18.1k	0.18	0.22	mA
	R_P = 7.03k	0 45	0.55	mA
	R_P = 3.40k	0.90	1.10	mA
	R_P = 2.80k	1 08	1.32	mA
Output Leakage Current	V_{OUT} = 75V		5	μA
Output Breakdown Voltage	I_{OUT} = 250 μA	80		V
Propagation Delay:				
Any Input to Segment Output	V_{CC} = 5V, T_A = 25°C		10	μs

Note 1: This limit can be higher for a current limiting voltage source

Note 2: The maximum junction temperature is 140°C For operation at elevated temperatures, the device must be derated based on a thermal resistance of 140°C/W θ_{JA}

Note 3: In all applications transient segment output current must be limited to 50 mA This may be accomplished in DC applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications

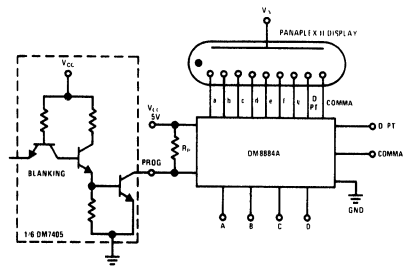
truth table

FUNCTION	D PT	COMMA	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	1	1	0	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	1	1	0	0	1	1	1	1	
2	1	1	0	0	1	0	0	0	1	0	0	1	0	
3	1	1	0	0	1	1	0	0	0	0	1	1	0	
4	1	1	0	1	0	0	1	0	0	1	1	0	0	
5	1	1	0	1	0	1	0	1	0	0	1	0	0	
6	1	1	0	1	1	0	0	1	0	0	0	0	0	
7	1	1	0	1	1	1	0	0	0	1	1	1	1	
8	1	1	1	0	0	0	0	0	0	0	0	0	0	
9	1	1	1	0	0	1	0	0	0	0	1	0	0	
10	1	1	1	0	1	0	1	1	0	0	0	1	1	
11	1	1	1	0	1	1	1	1	0	0	1	1	0	
12	1	1	1	1	0	0	0	0	1	1	1	0	0	
13	1	1	1	1	0	1	1	0	1	1	0	0	0	
14	1	1	1	1	1	0	1	1	1	1	1	1	0	
15	1	1	1	1	1	1	1	1	1	1	1	1	1	
*D PT	0	1	X	X	X	X	X	X	X	X	X	X	X	.
*Comma	0	0	X	X	X	X	X	X	X	X	X	X	X	,

□ Decimal Point
, Comma

*Decimal point and comma can be displayed with or without any numeral.

typical application



typical performance characteristics (see DM7880 data sheet)

Display Drivers

DM8885 MOS to high voltage cathode buffer

general discription

The DM8885 interfaces MOS calculator or counter-latch-decoder-driver circuits directly to seven-segment high-voltage gas-filled displays. The six inputs A, B, D, E, F, G are decoded to drive the seven segments of the tube.

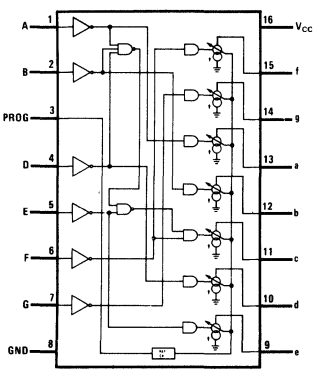
Each output constitutes a switchable, adjustable current source which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sources have a voltage compliance from 3V to at least 80V. Each current source is ratioed to the b-output current as required for even illumination of all segments. Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation The output current is adjusted by connecting a program resistor (R_P) from V_{CC} to the program input.

features

- Current source outputs
- Adjustable output currents 0.2 to 1.5 mA
- High output breakdown voltage 80V min
- Suitable for multiplex operation
- Low fan-in and low power
- Blanking via program input
- Also drives overrange, polarity, decimal point cathodes

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DM8885J
See Package 17

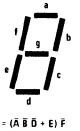
Order Number DM8885N
See Package 23

truth tables

A	B	D	E	F	G	DISPLAY
1	1	1	1	1	0	0
0	1	0	0	0	0	1
1	1	1	1	0	1	2
1	1	1	0	0	1	3
0	1	0	0	1	1	4
1	0	1	0	1	1	5
1	0	1	1	1	1	6
1	1	0	0	0	0	7
1	1	1	1	1	1	8
1	1	1	0	1	1	9
0	0	1	1	1	1	b
1	1	0	0	1	1	c
1	1	0	1	1	1	A
0	1	0	1	1	1	H
0	1	1	1	1	0	J
0	0	0	0	0	1	E
0	0	0	0	0	0	

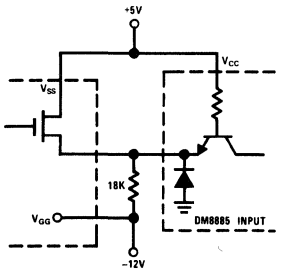
INPUT*	OUTPUT*
0	1 (OFF)
1	0 (ON)

*Positive Logic

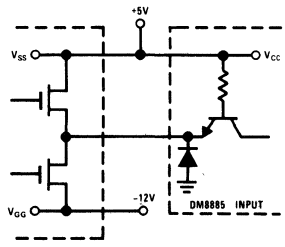


$C = (\bar{A}\,\bar{B}\,\bar{D} + E)\,\bar{F}$

typical applications



Open-Drain MOS Output



Push-Pull MOS Output

absolute maximum ratings

V_{CC}	7V
Input Voltage	6V
Segment Output Voltage	80V
Power Dissipation (Note 1)	600 mW
Transient Segment Output Current (Note 2)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage	V_{CC} = 4 75V	2 0			V
Logic "0" Input Voltage	V_{CC} = 4 75V			0 8	V
Logic "1" Input Current	V_{CC} = 5 25V, V_{IN} = 2 4V		2	15	μA
	V_{CC} = 5 25V, V_{IN} = 5 5V		4	400	μA
Logic "0" Input Current	V_{CC} = 5 25V, V_{IN} = 0 4V		-300	-600	μA
Power Supply Current	V_{CC} = 5 25V, All Inputs = 0V, R_P = 2 2k		22	31	mA
Input Diode Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C		-0 9	-1 5	V
Segment Outputs					
Outputs a, f, g On Current Ratio	All Outputs = 50V, Output b Curr = Ref	0 84	0 93	1 02	
Output c On Current Ratio	All Outputs = 50V, Output b Curr = Ref	1 12	1 25	1 38	
Output d On Current Ratio	All Outputs = 50V, Output b Curr = Ref	0 90	1 00	1 10	
Output e On Current Ratio	All Outputs = 50V, Output b Curr = Ref	0 99	1 10	1 21	
Output b On Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 18 1k	0 18	0 20	0 22	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 7 03k	0 45	0 50	0 55	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 3 40k	0 90	1 00	1 10	mA
	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C, R_P = 2 20k	1 35	1 50	1 65	mA
Output Saturation Voltage	V_{CC} = 4 75V, I_{OUT} b = 2 mA, R_P = 1k ± 5% (Note 4)		0 8	2 5	V
Output Leakage Current	V_{OUT} = 75V, V_{IN} = 0 8V, R_P = 1k		0 003	3	μA
	V_{OUT} = 75V, V_{PROG} = 0 4V		0 003	3	μA
Output Breakdown Voltage	I_{OUT} = 250 μA, V_{IN} = 0 8V	80	110		V
Propagation Delays					
Input to Segment Output	V_{CC} = 5V, T_A = 25°C		0 4	10	μs

Note 1: Maximum junction temperature is 130°C. For operating at elevated temperatures, the device must be derated based on a thermal resistance of 150°C/W θ_{JA}.

Note 2: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in DC applications by connecting a 2 2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +70°C, unless otherwise specified Typicals are for V_{CC} = 5V, T_A = 25°C. Positive current is defined as current into the referenced pin

Note 4: For saturation mode the segment output currents are externally limited and ratioed

typical performance characteristics (see DM7880 data sheet)

Display Drivers

DM7887/DM8887 8-digit high voltage anode driver (active-high inputs)

DM7889/DM8889 8-digit high voltage cathode driver (active-high inputs)

DM7897/DM8897 8-digit high voltage anode driver (active-low inputs)

general description

The DM7887/DM8887 and DM7897/DM8897 are designed to drive the individual anodes of a seven segment (cathodes) high-voltage gas discharge panel in a time multiplexed fashion.

When driven with appropriate input signals, the driver will switch voltage and impedance levels at the anode. This will allow or prevent ionization of gas around selected cathode in order to form a numeric display. Their main application will be to act as buffers between MOS outputs (fully-decoded) and the anodes of a gas-discharge panel, since the devices can source up to 16 mA at a low impedance and can tolerate more than 55V in the off state.

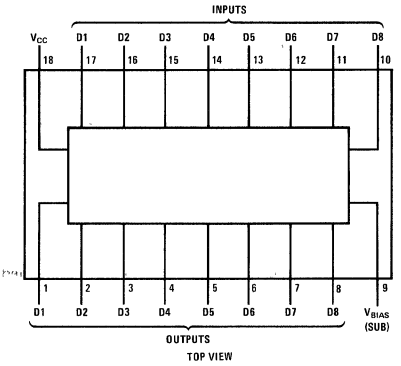
DM7889/DM8889 is capable of driving eight segments of a high-voltage display tube with a constant output sink current, which can be adjusted by external program resistor, R_P. The program current is half that of output on current. In the "OFF" state the outputs can tolerate more than 80V. The ratio of "ON" output currents is within ±10%. Inputs have negative clamp diodes. Active high input logic. The main application of the device is to interface MOS circuits to high-voltage displays. The total power dissipation in the package is low.

features

- Versatile circuits for a wide range of display applications
- High breakdown voltages
- Low power dissipation

connection diagrams (dual-in-line packages)

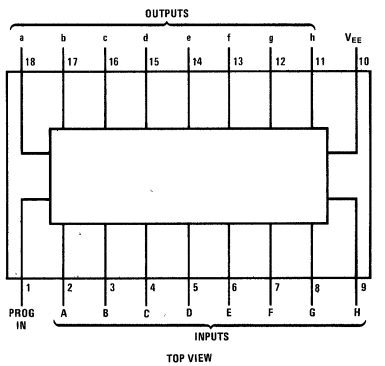
DM7887/DM8887, DM7897/DM8897



Order Number DM7887J or DM8887J
See Package 24
Order Number DM8887N
See Package 25

Order Number DM7897J or DM8897J
See Package 24
Order Number DM8897N
See Package 25

DM7889/DM8889



Order Number DM7889J or DM8889J
See Package 24
Order Number DM8889N
See Package 25

6

absolute maximum ratings (Note 1)

Supply Voltage ($V_{CC} - V_{BIAS}$) (Note 2)	
DM7887/DM8887, DM7897/DM8897	−60V
Package Power	
DM7889/DM8889	600 mW
Input Voltage	
DM7887/DM8887, DM7897/DM8897	−20V
DM7889/DM8889 (Note 3)	35V
Output Voltage	
DM7887/DM8887, DM7897/DM8897	−65V
DM7889/DM8889	85V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage ($V_{CC} - V_{BIAS}$)			
DM7887/DM8887, DM7897/DM8897	−40	−60	V
Temperature (T_A)			
DM7887, DM7889, DM7897	−55	+125	°C
DM8887, DM8889, DM8897	0	+70	°C

dc electrical characteristics (Notes 2, 3 and 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DM8887, DM8897					
Logical "1" Input Voltage					
DM8887	$V_{OUT} = -1.4V$, $I_{OUT} = -16$ mA	−2.0			V
Logical "0" Input Voltage					
DM8887	$V_{OUT} = -60V$, $I_{OUT} = -100\mu A$			−5.5	V
Logical "1" Input Current					
DM8897	$V_{OUT} = -1.4$, $I_{OUT} = -16$ mA	−300			μA
Logical "0" Input Current					
DM8897	$V_{OUT} = -60V$, $I_{OUT} = -100\mu A$			−10	μA
Input Current					
DM8887	$V_{IN} = -1$ 0V		335	550	μA
	$V_{IN} = -6.0V$		−0.2	−25	μA
DM8897	$V_{IN} = -12V$	−0.30		−0.65	mA
	$V_{IN} = -12V$	−0 6		−1.5	mA
Output Off Voltage	$I_{OUT} = -100\mu A$, $I_{IN} = 0\mu A$	−60	−77		V
Output Off Current	$V_{OUT} = -55V$, $I_{IN} = 0\mu A$		−0.03	−5.0	μA
Output On Voltage					
DM8887	$V_{IN} = -2.0V$, $I_{OUT} = -16$ mA		−1.0	−1.4	V
DM8897	$I_{IN} = -300\mu A$, $I_{OUT} = -16$ mA			−1 4	V
Supply Current					
DM8887 (Note 5)	$V_{IN} = -1.0V$, $I_{OUT} = -16$ mA, $V_{BIAS} = -60V$		−2.2	−4.0	mA
DM8897	$I_{IN} = -300\mu A$, $I_{OUT} = -16$ mA, $V_{BIAS} = -60V$, (One Driver Only)			−100	μA
DM7889/DM8889					
Input Current	$V_{IN} = 6$ 0V	150	250	350	μA
Logical "0" Input Current	$I_{OUT} = 5.0\mu A$, $V_{OUT} = 75V$			7 0	μA
Logical "1" Input Current	$I_{OUT} = 1$ 4 mA, $I_{IP} = 850\mu A$, $V_{OUT} = 50V$	80			μA
Input Clamp Voltage	$I_{IN} = -1.0$ mA, $T_A = 25°C$		−0 68	−0 85	V
Output Breakdown Voltage	$I_{OUT} = 100\mu A$, $I_{IN} = 0\mu A$	80			V
Output Leakage Current	$V_{OUT} = 75V$, -1 0 mA $\leq I_{IN} \leq 7$ 0μA		0 02	5 0	μA
Prog. Input Voltage	$I_{IP} = 150\mu A$	1 8	2 3		V
	$I_{IP} = 850\mu A$		4 0	4.5	V
Logical "0" Output Current	$V_{OUT} = 50V$, $80\mu A \leq I_{IN} \leq I_{IP}$				
DM7889	$I_{IP} = 150\mu A$	210	300	390	μA
DM8889	$I_{IP} = 150\mu A$	240	300	360	μA
DM7889	$I_{IP} = 400\mu A$	660	800	940	μA
DM8889	$I_{IP} = 400\mu A$	680	800	920	μA
DM7889	$I_{IP} = 850\mu A$	1.45	1 7	1.95	mA
DM8889	$I_{IP} = 850\mu A$	1 53	1 7	1 87	mA
Output Current Ratio	I_{OUT} 'b' Ref = 1.7 mA, $V_{OUT} = 50V$	0.9	1 0	1 1	

ac electrical characteristics $T_A = 25°C$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DM8887					
Propagation Delay from Input to Output "ON" (t_{ON})	(See AC Test Circuit and Switching Time Waveforms)			5 0	μs
Propagation Delay from Input to Output "ON" (t_{RISE})				1 0	μs
DM7889/DM8889					
Propagation Delay to a Logical "0" from Input to Output (t_{pd0})	R_P = 6.0k to 6 0V, R_{OUT} = 1 0k to 6 0V		37	100	ns
Propagation Delay to a Logical "1" from Input to Output (t_{pd1})	Input Ramp Rate ≤ 15 ns, Freq = 1 0 MHz, DC = 50%, Amplitude = 6 0V		92	200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits The table of "Electrical Characteristics" provides conditions for actual device operation

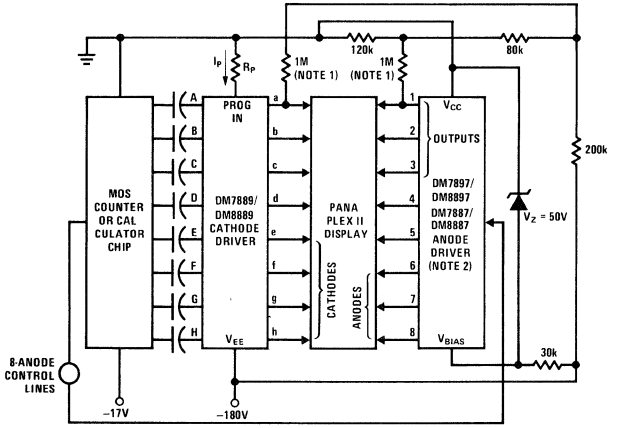
Note 2: All voltages shown for DM7887/DM8887, DM7897/DM8897 W R T V_{CC} = 0V All currents into device pins shown as positive, out of device pins as negative All values shown as max or min on absolute value basis

Note 3: All voltages for DM7889/DM8889 with respect to V_{EE} = 0V

Note 4: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7889 and across the 0°C to +70°C range for the DM8887, DM8889 and DM8897 All typicals are given for $T_A = 25°C$

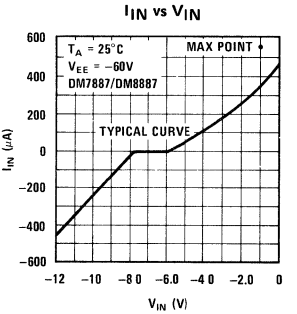
Note 5: Supply currents specified for any one input = −1 0V All other inputs = −5 5V and selected output having 16 mA load

typical application

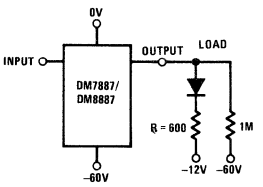


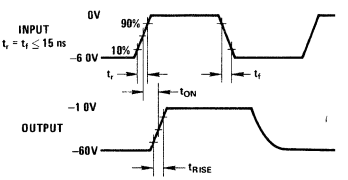
NOTE 1 ALL OUTPUTS OF BOTH CATHODE AND ANODE DRIVER HAVE LOADS AS SHOWN FOR OUTPUT a
NOTE 2 USE DM7887/DM8887 FOR ACTIVE HIGH INPUTS AND DM7897/DM8897 FOR ACTIVE LOW INPUTS

typical performance characteristics



ac test circuit and switching time waveforms

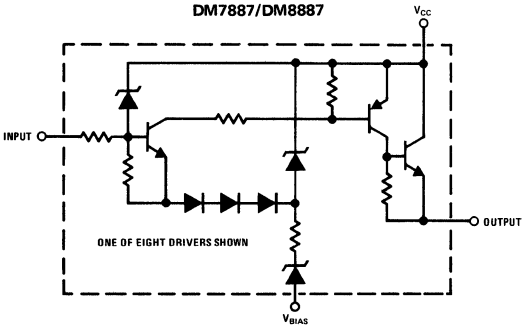




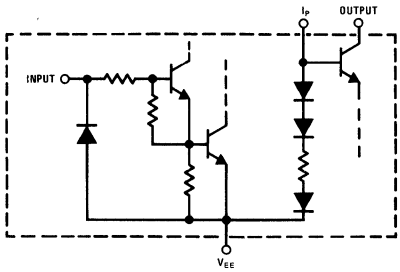
6

logic diagrams

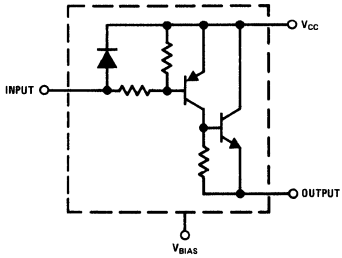
DM7887/DM8887



DM7889/DM8889



DM7897/DM8897



Sense Amplifiers

DM7802/DM8802, DM7806/DM8806
high speed MOS to TTL level converters

general description*

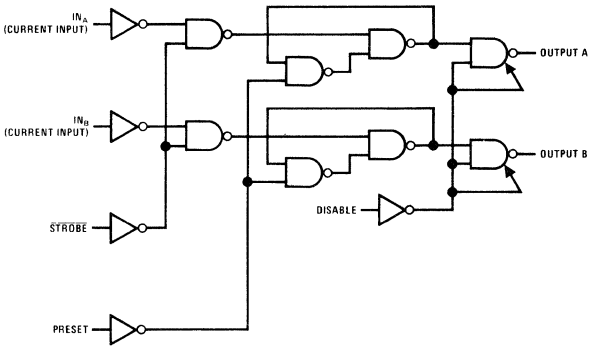
The DM7802/DM8802, DM7806/DM8806 are high speed MOS to TTL level converters. These circuits act as an interface level converter between MOS and TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE® output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

*Also see LM3625.

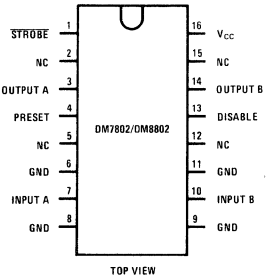
features

- Very low output impedance – high drive ability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter

logic and connection diagrams

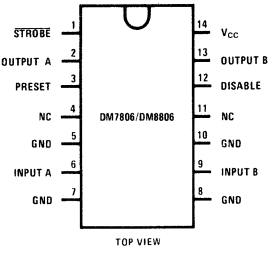


Dual-In-Line Package



Order Number DM7802J or DM8802J
See Package 17
Order Number DM8802N
See Package 23

Dual-In-Line and Flat Package



Order Number DM7806J or DM8806J
See Package 16
Order Number DM8806N
See Package 22
Order Number DM7806W or DM8806W
See Package 27

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5 5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM7802, DM7806	4.5	5 5	V
DM8802, DM8806	4.75	5.25	V
Temperature (T_A)			
DM7802, DM7806	−55	+125	°C
DM8802, DM8806	0	+70	°C

electrical characteristics (Note 2)

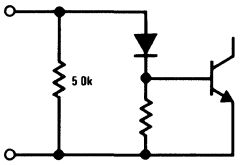
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Current (I_{INA}, I_{INB})	V_{CC} = Min	500			μA
Logical "0" Input Current (I_{INA}, I_{INB})	V_{CC} = Min			200	μA
Logical "1" Input Voltage, Strobe, Preset, Disable	V_{CC} = Min	2 0			V
Logical "0" Input Voltage, Strobe, Preset, Disable	V_{CC} = Min			0 8	V
Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = 1 5 mA	2 4			V
Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA			0 4	V
Third State Output Current	V_{CC} = Max, V_O = 2 4V			40	μA
	V_{CC} = Max, V_O = 0 4V			-40	μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V			40	μA
	V_{CC} = Max, V_{IN} = 5 5V			1 0	mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			-1 6	mA
Supply Current	V_{CC} = Max, $V_{IN(DISABLE)}$ = 2 Other Inputs = ϕV			40	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = 12 mA			-1 5	V
Output Short Circuit Current (Note 3)	V_{CC} = Max, V_O = 0V				
	DM7802, DM7806	20		70	mA
	DM8802, DM8806	-18		-70	mA
Propagation Delay to a Logical "0" From STROBE to Output (t_{ds})	V_{CC} = 5 0V (See waveforms) T_A = 25°C		17	25	ns
Propagation Delay to a Logical "1" From Preset to Output (t_{dp})	V_{CC} = 5 0V (See waveforms) T_A = 25°C		22	32	ns
Delay From Disable Input to High Impedance State (From Logical "1" Level)(t_{1H})	V_{CC} = 5 0V (See ac test circuit) T_A = 25°C		7 0	11	ns
Delay From Disable Input to High Impedance State (From Logical "0" Level)(t_{0H})	V_{CC} = 5 0V (See ac test circuit) T_A = 25°C		17	25	ns
Delay From Disable Input to Logical "1" Level (From High Impedance State)(t_{H1})	V_{CC} = 5 0V (See ac test circuit) T_A = 25°C		9 0	14	ns
Delay From Disable Input to Logical "0" Level (From High Impedance State)(t_{H0})	V_{CC} = 5 0V (See ac test circuit) T_A = 25°C		13 5	16	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM7802, DM7806 and across the 0°C to +70°C range for the DM8802, DM8806. All typicals are given for V_{CC} = 5.0V, T_A = 25°C.

Note 3: Only one output at a time should be shorted.

typical input circuit

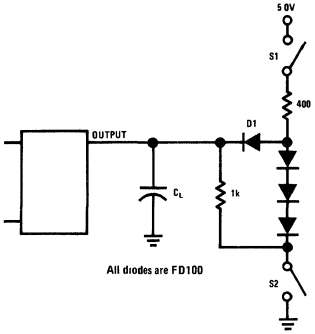


truth table

IN A OR B	ST	P	D	Q_A OR Q_B
0	1	1	0	1
1	1	1	0	1
0	0	1	0	0
1	0	1	0	1
X	X	X	1	Hi-Z

X = Don't care

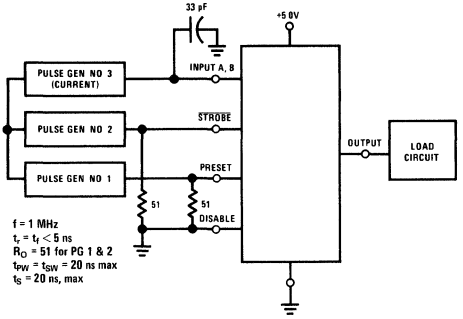
ac test circuits



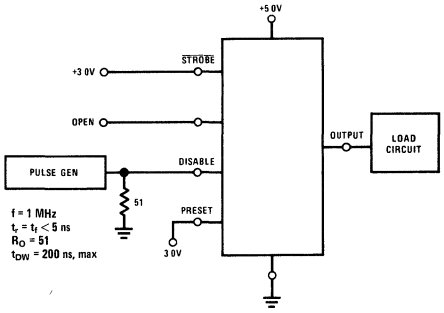
	SWITCH S_1	SWITCH S_2	C_L
t_{dp}	Closed	Closed	50 pF
t_{ds}	Closed	Closed	50 pF
t_{0H}	Closed	Closed	*5 pF
t_{1H}	Closed	Closed	*5 pF
t_{H0}	Closed	Open	50 pF
t_{H1}	Open	Closed	50 pF

*Jig capacitance

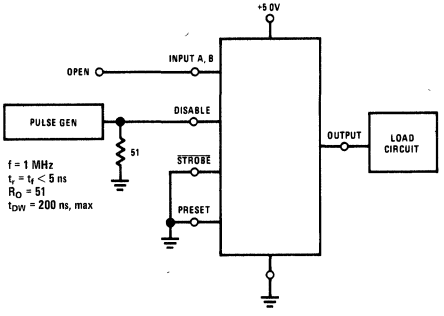
(a)



(b)



(c)



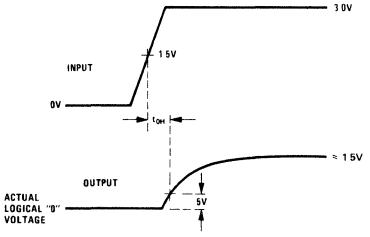
(d)

Test Circuit 20

7

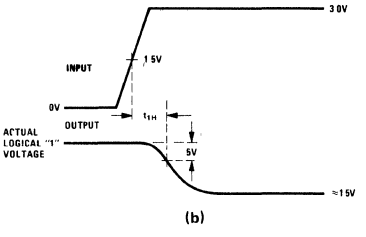
switching time waveforms

t_{0H}



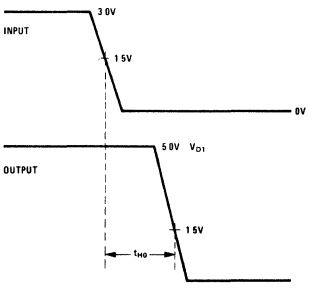
(a)

t_{1H}



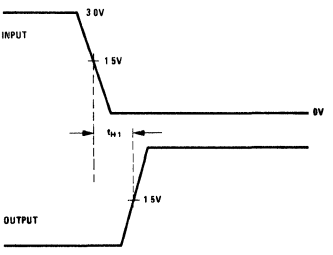
(b)

t_{H0}

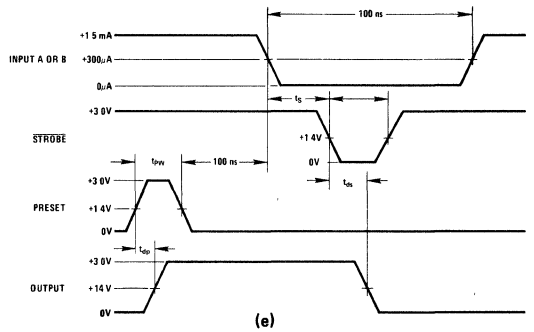


(c)

t_{H1}



(d)



(e)

Sense Amplifiers

LM5520/LM7520 series
dual core memory sense amplifiers
general description

The devices in this series of dual core sense amplifiers convert bipolar millivolt-level memory sense signals to saturated logic levels. The design employs a common reference input which allows the input threshold voltage level of both amplifiers to be adjusted. Separate strobe inputs provide time discrimination for each channel. Logic inputs and outputs are DTL/TTL compatible. All devices of the series have identical preamplifier configurations, while various logic connections are provided to suit the specific application.

The LM5520/LM7520 has output latch capability and provides sense, strobe, and memory function for two sense lines. The LM5522/LM7522 contains a single open collector output which may be used to expand the number of inputs of the LM5520/LM7520, or to drive an external Memory Data Register (MDR). Intended for small memories, the two channels of the LM5524/LM7524 are independent with two separate outputs. The LM5534/LM7534 is similar to the LM5524/LM7524 but has uncommitted, wire-ORable outputs. The LM5528/LM7528 has the same logic configuration of the LM5524/LM7524 and in addition provides separate low impedance Test Points at each preamplifier output. A similar device having uncommitted, wire-ORable outputs is the LM5538/LM7538.

features

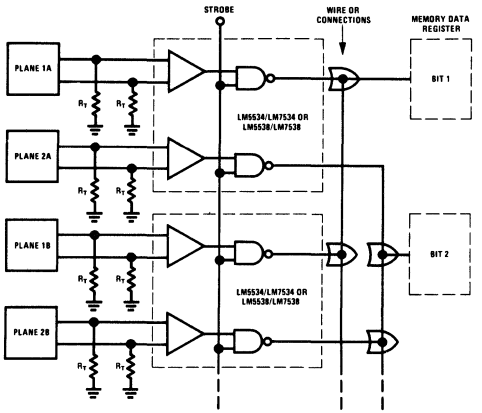
- High speed
- Guaranteed narrow threshold uncertainty over temperature
- Adjustable input threshold voltage
- Fast overload recovery times
- Two amplifiers per package
- Molded or cavity dual-in-line package
- Six logic configurations

The part number ending with an even number (e.g., LM5520) designates a tighter guaranteed input threshold uncertainty than the subsequent odd number ending (e.g., LM5521). The remaining specifications for the two are identical. All devices meet or exceed the specifications for the corresponding device (where applicable) in the SN5520/SN7520 series and are pin-for-pin replacements.

absolute maximum ratings

Supply Voltage	±7V
Differential or Reference Input Voltage	±5V
Logic Input Voltage	+5.5V
Operating Temperature Range	
LM55XX	−55°C to +125°C
LM75XX	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

typical application



Expanded Small Memory System

LM5520/LM7520 and LM5521/LM7521 electrical characteristics

LM5520/LM5521: The following apply for $-55°C \leq T_A \leq 125°C$

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF. INPUT	STROBE INPUT	GATE Q INPUT	GATE $\bar{Q}$ INPUT	LOGIC OUTPUT (NOTE 3)	SUPPLY VOLT.	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V		+16 mA(Q)	±5V	Logic Output <0 4V
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V		−400 μA(Q)	±5V	Logic Output >2.4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V		+16 mA(Q)	±5V	Logic Output <0 4V
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V		−400 μA(Q)	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V	+5 25V	+5 25V		±5.25V	
LM7520/LM7521: The following apply for $0°C \leq T_A \leq 70°C$												
Differential Input Threshold Voltage (V_{TH}) (Note 4)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V		+16 mA(Q)	±5V	Logic Output <0 4V
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V		−400 μA(Q)	±5V	Logic Output >2 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V		+16 mA(Q)	±5V	Logic Output <0.4V
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V		−400 μA(Q)	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V	+5 25V	+5 25V		±5 25V	
LM5520/LM5521: The following apply for $-55°C \leq T_A \leq 125°C$ LM7520/LM7521: The following apply for $0°C \leq T_A \leq 70°C$												
Differential Input Offset Current		0 5		μA	0V	0V	+5 25V	+5 25V	+5 25V		±5 25V	
Logic "1" Input Voltage												
(Strobes)	2			V	40 mV	20 mV	+2V	+4 75V		−400 μA(Q)	±5V	Logic Output >2 4V
(Gate Q)	2			V	40 mV	20 mV	0V	+2V		+16 mA(Q)	±5V	Logic Output <0.4V
(Gate $\bar{Q}$)	2			V	40 mV	20 mV	0V	0V	+2V	+16 mA($\bar{Q}$)	±5V	Logic Output <0 4V
Logic "0" Input Voltage												
(Strobes)			0 8	V	40 mV	20 mV	+0 8V	+4.75V		+16 mA(Q)	±5V	Logic Output <0.4V
(Gate Q)			0 8	V	40 mV	20 mV	0V	+0.8V		−400 μA(Q)	±5V	Logic Output >2 4V
(Gate $\bar{Q}$)			0 8	V	40 mV	20 mV	0V	0V	+0 8V	−400 μA($\bar{Q}$)	±5V	Logic Output >2 4V
Logic "0" Input Current		-1	-1 6	mA	40 mV	20 mV	+0 4V	+0 4V	+0 4V		±5 25V	Each Input
Logic "1" Input Current		5	40	μA	0V	20 mV	+2 4V	+5 25V	+2 4V		±5 25V	Each Input
(Strobe & Gate $\bar{Q}$)		02	1	mA	0V	20 mV	+5 25V	+5 25V	+5 25V		±5 25V	Each Input
(Gate Q)		5	40	μA	40 mV	20 mV	+5 25V	+2 4V			±5 25V	
		02	1	mA	40 mV	20 mV	+5 25V	+5 25V			±5 25V	
Logic "1" Output Voltage												
(Strobe)	2 4	3 9		V	40 mV	20 mV	+2 0V	+5 25V		−400 μA(Q)	±4 75V	
(Gate Q)	2 4	3 9		V	40 mV	20 mV	0V	+0 8V		−400 μA(Q)	±4 75V	
(Gate $\bar{Q}$)	2 4	3 9		V	40 mV	20 mV	+4.75V	0V	+0 8V	−400 μA($\bar{Q}$)	±4 75V	
Logic "0" Output Voltage												
(Strobe)		0 25	0 40	V	40 mV	20 mV	+0.8V	+4 75V		+16 mA(Q)	±4 75V	
(Gate Q)		0 25	0 40	V	0V	20 mV	0V	+2V		+16 mA(Q)	±4 75V	
(Gate $\bar{Q}$)		0 25	0 40	V	0V	20 mV	0V	0V	+2V	+16 mA($\bar{Q}$)	±4 75V	
Q Output Short Circuit Current	-3	-4	-5	mA	0V	20 mV	0V	0V		0 V(Q)	±5 25V	
$\bar{Q}$ Output Short Circuit Current	-2 1	-2 8	-3 5	mA	0V	20 mV	0V	0V	0V	0 V($\bar{Q}$)	±5 25V	
V+ Supply Current		21	35	mA	0V	20 mV	0V	0V	0V		±5 25V	
V− Supply Current		-13	-18	mA	0V	20 mV	0V	0V	0V		±5 25V	

Note 1: For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5520 and LM5521 are guaranteed the same as LM7520 and LM7521, respectively.

Note 2: Limits in parentheses pertain to LM5521, other limits pertain to LM5520.

Note 3: Q or $\bar{Q}$ in parentheses indicate Q or $\bar{Q}$ logic output, respectively.

Note 4: Limits in parentheses pertain to LM7521, other limits pertain to LM7520.

Note 5: Positive current is defined as current into the referenced pin.

Note 6: Pin 1 to have $\geq$100 pF capacitor connected to ground.

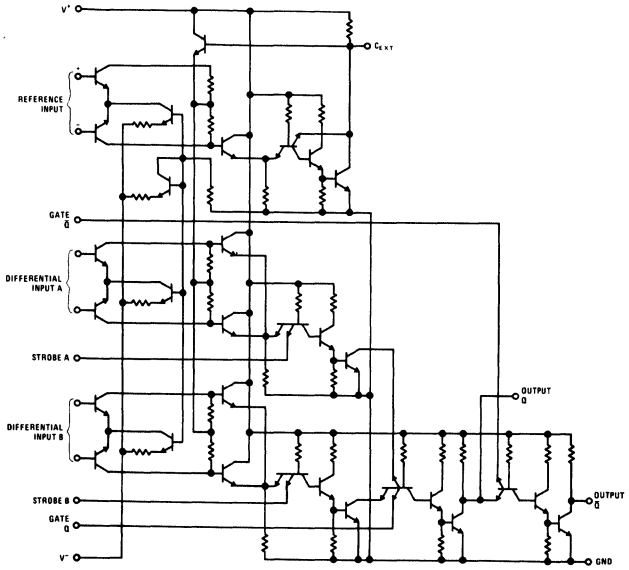
LM5520/LM7520 and LM5521/LM7521 electrical characteristics

LM5520/LM5521 and LM7520/LM7521: The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$

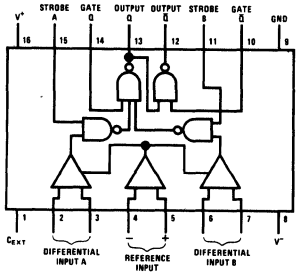
PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS				
					DIFF. INPUT	REF. INPUT	STROBE AND GATE INPUTS	Q LOGIC OUTPUT	AC TEST CIRCUIT
AC Common-Mode Input Firing Voltage		±2 5		V	PULSE	20 mV	+5V	SCOPE	
Propagation Delays									
Differential Input to Logical "1" Q Output		20	40	ns		20 mV			1
Differential Input to Logical "0" Q Output		28		ns		20 mV			1
Differential Input to Logical "1" $\overline{Q}$ Output		36		ns		20 mV			1
Differential Input to Logical "0" $\overline{Q}$ Output		28	55	ns		20 mV			1
Strobe Input to Logical "1" Q Output		10	30	ns		20 mV			1
Strobe Input to Logical "0" Q Output		20		ns		20 mV			1
Strobe Input to Logical "1" $\overline{Q}$ Output		33		ns		20 mV			1
Strobe Input to Logical "0" $\overline{Q}$ Output		16	55	ns		20 mV			1
Gate Q Input to Logical "1" Q Output		12	20	ns		20 mV			2
Gate Q Input to Logical "0" Q Output		6		ns		20 mV			2
Gate Q Input to Logical "1" $\overline{Q}$ Output		17		ns		20 mV			2
Gate Q Input to Logical "0" $\overline{Q}$ Output		19	30	ns		20 mV			2
Gate $\overline{Q}$ Input to Logical "1" $\overline{Q}$ Output		12		ns		20 mV			2
Gate $\overline{Q}$ Input to Logical "0" $\overline{Q}$ Output		6	20	ns		20 mV			2
Diff Input Overload Recovery Time		10		ns					
Common-Mode Input Overload Recovery Time		5		ns					
Min Cycle Time		200		ns					

LM5520/LM7520 and LM5521/LM7521

schematic diagram



connection diagram



TOP VIEW

Order Number LM5520J or LM7520J
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Order Number LM7520N
See Package 23
Order Number LM5521J or LM7521J
See Package 17
Order Number LM7521N
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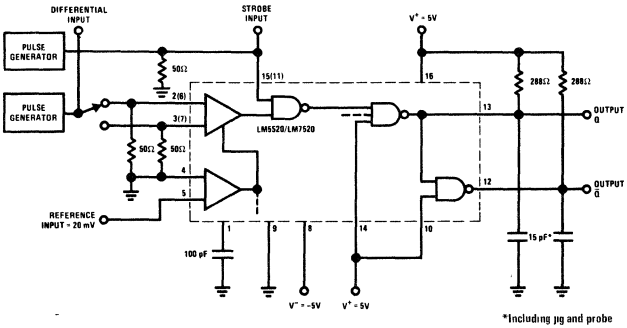
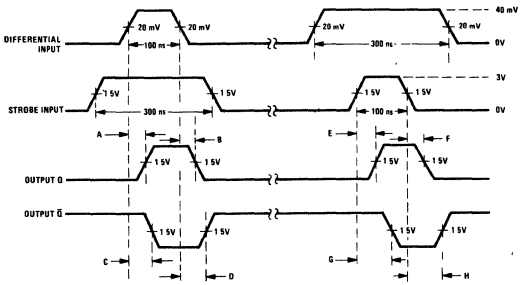
LM5520/LM7520 and LM5521/LM7521

AC test circuit (1)



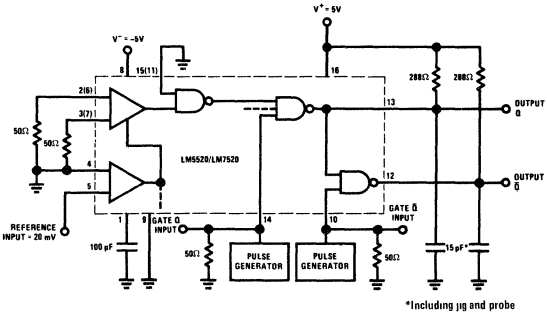
*Including jig and probe

voltage waveforms (1)



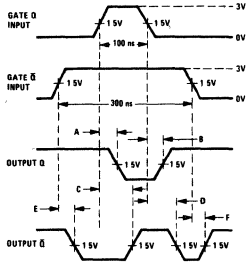
1 Pulse generator characteristics
$Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2 Propagation delays
A = Differential input to logical "1" output Q
B = Differential input to logical "0" output Q
C = Differential input to logical "0" output Q̄
D = Differential input to logical "1" output Q̄
E = Strobe input to logical "1" output Q
F = Strobe input to logical "0" output Q
G = Strobe input to logical "0" output Q̄
H = Strobe input to logical "1" output Q̄

AC test circuit (2)



*Including jig and probe

voltage waveforms (2)



1 Pulse generator characteristics
$Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2 Propagation delays.
A = Gate Q input to logical "0" output Q
B = Gate Q input to logical "1" output Q̄
C = Gate Q input to logical "1" output Q
D = Gate Q̄ input to logical "0" output Q̄
E = Gate Q̄ input to logical "0" output Q
F = Gate Q̄ input to logical "1" output Q̄

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LM5522/LM7522 and LM5523/LM7523 electrical characteristics

LM5522/LM5523: The following apply for $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF. INPUT	STROBE INPUT	GATE INPUT	LOGIC OUTPUT	SUPPLY VOLT.	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V	−400 μA	±5V	Logic Output >2 4V
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V	+16 mA	±5V	Logic Output <0 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V	−400 μA	±5V	Logic Output >2 4V
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V	+16 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V	+5 25V		±5.25V	
LM7522/LM7523: The following apply for $0^{\circ}C \leq T_A \leq 70^{\circ}C$											
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5V	−400 μA	±5V	Logic Output >2.4V
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+5V	+16 mA	±5V	Logic Output <0.4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5V	−400 μA	±5V	Logic Output >2.4V
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+5V	+16 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V	+5.25V		±5 25V	
LM5522/LM5523: The following apply for $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ LM7522/LM7523: The following apply for $0^{\circ}C \leq T_A \leq 70^{\circ}C$											
Diff Input Offset Current		0 5		μA	0V	0V	+5.25V	+5 25V		±5 25V	
Logic "1" Input Voltage (Strobes)	2			V	40 mV	20 mV	+2V	+4 75V	+16 mA	±5V	Logic Output <0 4V
(Gate)	2			V	40 mV	20 mV	0V	+2V	−400 μA	±5V	Logic Output >2 4V
Logic "0" Input Voltage (Strobes)			0 8	V	40 mV	20 mV	+0 8V	+4.75V	−400 μA	±5V	Logic Output >2.4V
(Gate)			0.8	V	40 mV	20 mV	0V	+0.8V	+16 mA	±5V	Logic Output <0.4V
Logic "0" Input Current		−1	−1 6	mA	40 mV	20 mV	+0 4V	+0 4V		±5.25V	Each Input
Logic "1" Input Current (Strobes)			40	μA	0V	20 mV	+2.4V	+5.25V		±5.25V	
			1	mA	0V	20 mV	+5 25V	+5 25V		±5.25V	
(Gate)			40	μA	40 mV	20 mV	+5 25V	+2.4V		±5.25V	
			1	mA	40 mV	20 mV	+5 25V	+5.25V		±5 25V	
Logic "1" Output Voltage	2.4	3 9		V	40 mV	20 mV	+0 8V	+2V	−400 μA	±4.75V	
Logic "0" Output Voltage (Strobes)		0 25	0.40	V	40 mV	20 mV	+2V	+4.75V	+16 mA	±4.75V	Tie Pins 10 and 12
(Gate)		0 25	0.40	V	40 mV	20 mV	0V	+0.8V	+16 mA	±4.75V	Tie Pins 10 and 12
Output Short Circuit Current	−2 1	−2 8	−3.5	mA	40 mV	20 mV	0V	+5.25V	0V	±5.25V	Tie Pins 10 and 12
Output Leakage Current		0.01	250	μA	0V	20 mV	0V	+2V	+5.25V	±4 75V	
V^+ Supply Current		23	36	mA	0V	20 mV	0V	0V		±5.25V	
V^- Supply Current		−13	−18	mA	0V	20 mV	0V	0V		±5.25V	
LM5522/LM5523 and LM7522/LM7523: The following apply for $T_A = 25^{\circ}C$, $V^+ = 5V$, $V^- = -5V$											
AC Common Mode Input Firing Voltage		±2 5		V	PULSE	20 mV	+5V	+5V	SCOPE		
Propagation Delays Differential Input to Logical "1" Output		26		ns		20 mV					AC Test Circuit
Differential Input to Logical "0" Output		21	45	ns		20 mV					AC Test Circuit
Strobe Input to Logical "1" Output		22		ns		20 mV					AC Test Circuit
Strobe Input to Logical "0" Output		12	40	ns		20 mV					AC Test Circuit
Gate Input to Logical "1" Output		4		ns		20 mV					AC Test Circuit
Gate Input to Logical "0" Output		15	25	ns		20 mV					AC Test Circuit
Differential Input Overload Recovery Time		10		ns							
Common Mode Input Overload Recovery Time		5		ns							
Min Cycle Time		200		ns							

Note 1. For $0^{\circ}C \leq T_A \leq 70^{\circ}C$ operation, electrical characteristics for LM5522 and LM5523 are guaranteed the same as LM7522 and LM7523, respectively

Note 2: Limits in parentheses pertain to LM5523, other limits pertain to LM5522

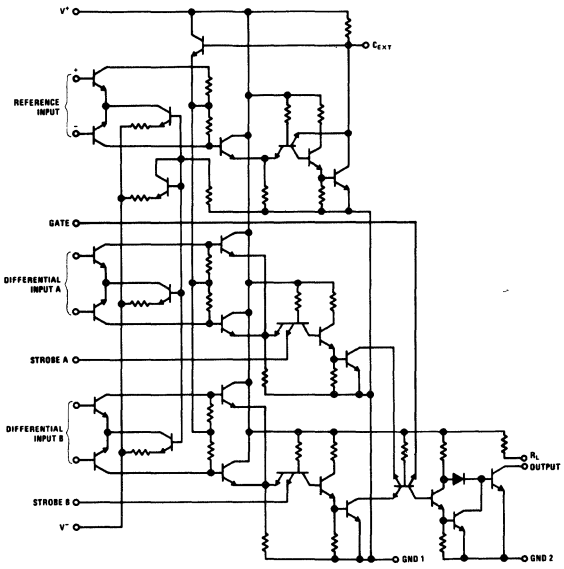
Note 3. Limits in parentheses pertain to LM7523, other limits pertain to LM7522

Note.4 Positive current is defined as current into the referenced pin

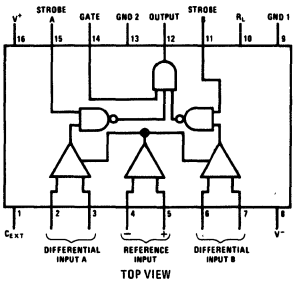
Note 5: Pin 1 to have $\geq$ 100 pF capacitor connected to ground

LM5522/LM7522 and LM5523/LM7523

schematic diagram



connection diagram



TOP VIEW

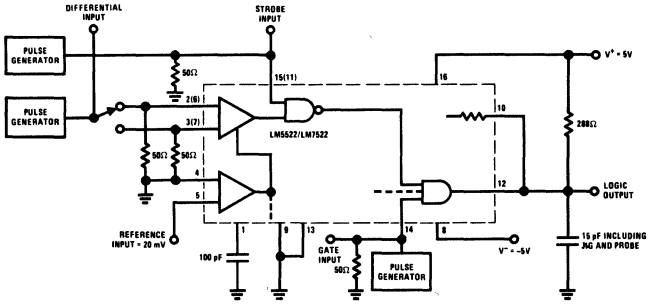
Order Number LM5522J or LM7522J
See Package 17

Order Number LM7522N
See Package 23

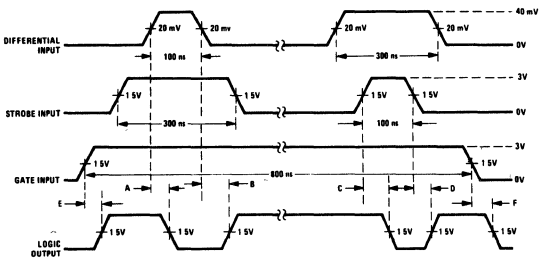
Order Number LM5523J or LM7523J
See Package 17

Order Number LM7523N
See Package 23

AC test circuit



voltage waveforms



1. One strobe is grounded when the other side is being tested
2. Pulse generator characteristics.
   $Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
3. Propagation delays:
   A = Differential input to logical "0" output
   B = Differential input to logical "1" output
   C = Strobe input to logical "0" output
   D = Strobe input to logical "1" output
   E = Gate input to logical "1" output
   F = Gate input to logical "0" output

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LM5524/LM7524 and LM5525/LM7525 electrical characteristics

LM5524/LM5525: The following apply for $-55°C \leq T_A \leq 125°C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF. INPUT	STROBE INPUT	LOGIC OUTPUT	SUPPLY VOLT.	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	−400 μA	±5V	Logic Output >2 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	−400 μA	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V		±5 25V	
LM7524/LM7525: The following apply for $0°C \leq T_A \leq 70°C$										
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+16 mA	±5V ±5%	Logic Output <0 4V
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	−400 μA	±5V ±5%	Logic Output >2 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+16 mA	±5V ±5%	Logic Output <0 4V
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	−400 μA	±5V ±5%	Logic Output >2 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V		±5 25V	
LM5524/LM5525: The following apply for $-55°C \leq T_A \leq 125°C$ LM7524/LM7525: The following apply for $0°C \leq T_A \leq 70°C$										
Diff Input Offset Current		0.5		μA	0V	0V	+5 25V		±5 25V	
Logic "1" Input Voltage	2			V	40 mV	20 mV	+2V	−400 μA	±5V	Logic Output >2 4V
Logic "0" Input Voltage			0 8	V	40 mV	20 mV	+0.8V	+16 mA	±5V	Logic Output <0.4V
Logic "0" Input Current		−1	−1 6	mA	40 mV	20 mV	+0.4V		±5 25V	
Logic "1" Input Current		5	40	μA	0V	20 mV	+2 4V		±5 25V	
		0.02	1	mA	0V	20 mV	+5.25V		±5.25V	
Logic "1" Output Voltage	2.4	3.9		V	40 mV	20 mV	+2 0V	−400 μA	±4 75V	
Logic "0" Output Voltage		0 25	0.40	V	40 mV	20 mV	+0.8V	+16 mA	±4 75V	
Output Short Circuit Current	−2 1	−2 8	−3.5	mA	40 mV	20 mV	+5 25V	0V	±5.25V	
V^+ Supply Current		29	40	mA	0V	20 mV	0V		±5 25V	
V^- Supply Current		−13	−18	mA	0V	20 mV	0V		±5 25V	
LM5524/LM5525 and LM7524/LM7525: The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$										
AC Common-Mode Input Firing Voltage		±2.5		V	PULSE	20 mV	+5V	SCOPE		
Propagation Delays										
Differential Input to Logical "1" Output		20	40	ns		20 mV				AC Test Circuit
Differential Input to Logical "0" Output		28		ns		20 mV				AC Test Circuit
Strobe Input to Logical "1" Output		10	30	ns		20 mV				AC Test Circuit
Strobe Input to Logical "0" Output		20		ns		20 mV				AC Test Circuit
Differential Input Overload Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time		5		ns						
Min Cycle Time		200		ns						

Note 1: For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5524 and LM5525 are guaranteed the same as LM7524 and LM7525 respectively.

Note 2: Limits in parentheses pertain to LM5525, other limits pertain to LM5524.

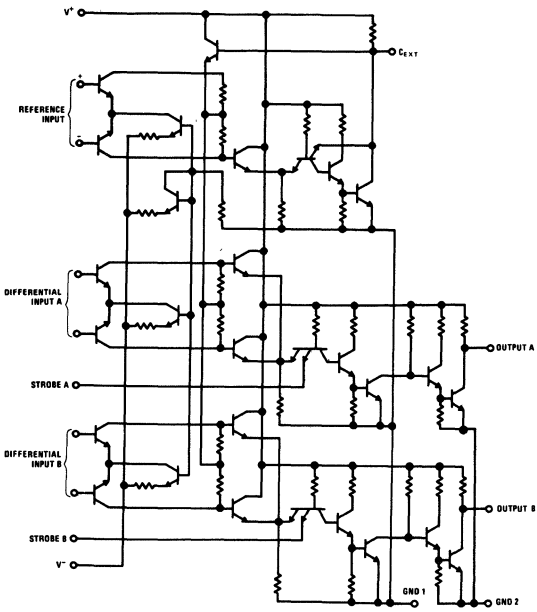
Note 3: Limits in parentheses pertain to LM7525, other limits pertain to LM7524.

Note 4: Positive current is defined as current into the referenced pin.

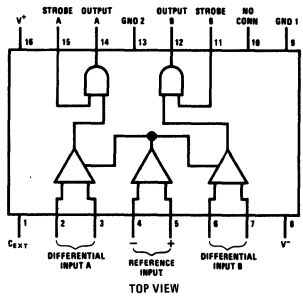
Note 5: Pin 1 to have $\geq$100 pF capacitor connected to ground.

LM5524/LM7524 and LM5525/LM7525

schematic diagram



connection diagram



TOP VIEW

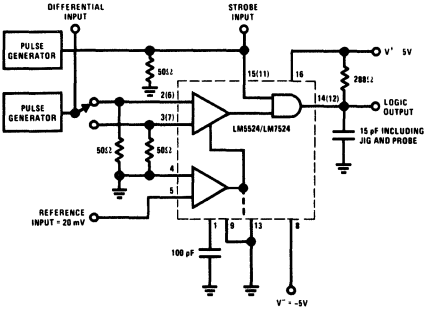
Order Number LM5524J or LM7524J
See Package 17

Order Number LM7524N
See Package 23

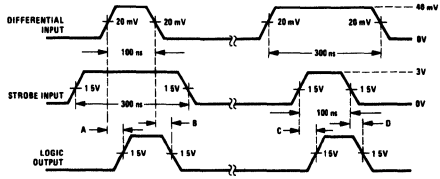
Order Number LM5525J or LM7525J
See Package 17

Order Number LM7525N
See Package 23

AC test circuit



voltage waveforms



1. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ±5 ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "1" output
   B = Differential input to logical "0" output
   C = Strobe input to logical "1" output
   D = Strobe input to logical "0" output

7

LM5528/LM7528 and LM5529/LM7529 electrical characteristics

LM5528/LM5529: The following apply for $-55°C \leq T_A \leq 125°C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF. INPUT	STROBE INPUT	LOGIC OUTPUT	SUPPLY VOLT.	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	-400 μA	±5V	Logic Output >2 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	-400 μA	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5.25V		±5 25V	
LM7528/LM7529: The following apply for $0°C \leq T_A \leq 70°C$										
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	-400 μA	±5V	Logic Output >2 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+16 mA	±5V	Logic Output <0 4V
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	-400 μA	±5V	Logic Output >2 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V		±5 25V	
LM5528/LM5529: The following apply for $-55°C \leq T_A \leq 125°C$ LM7528/LM7529: The following apply for $0°C \leq T_A \leq 70°C$										
Diff Input Offset Current		0 5		μA	0V	0V	+5 25V		±5 25V	
Logic "1" Input Voltage	2			V	40 mV	20 mV	+2V	-400 μA	±5V	Logic Output >2 4V
Logic "0" Input Voltage			0 8	V	40 mV	20 mV	+0 8V	+16 mA	±5V	Logic Output <0 4V
Logic "0" Input Current		-1	-1.6	mA	40 mV	20 mV	+0 4V		±5 25V	
Logic "1" Input Current		5 0.02	40 1	μA mA	0V 0V	20 mV 20 mV	+2 4V +5.25V		±5.25V ±5 25V	
Logic "1" Output Voltage	2.4	3.9		V	40 mV	20 mV	+2 0V	-400 μA	±4 75V	
Logic "0" Output Voltage		0.25	0 40	V	40 mV	20 mV	+0 8V	+16 mA	±4 75V	
Output Short Circuit Current	-2 1	-2 8	-3 5	mA	40 mV	20 mV	+5 25V	0V	±5 25V	
V^+ Supply Current		29	40	mA	0V	20 mV	0V		±5 25V	
V^- Supply Current		-13	-18	mA	0V	20 mV	0V		±5.25V	
LM5528/LM5529 and LM7528/LM7529: The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$										
AC Common-Mode Input Firing Voltage		±2 5		V	PULSE	20 mV	+5V	SCOPE		
Propagation Delays										
Differential Input to Logical "1" Output		20	40	ns		20 mV				AC Test Circuit
Differential Input to Logical "0" Output		28		ns		20 mV				AC Test Circuit
Strobe Input to Logical "1" Output		10	30	ns		20 mV				AC Test Circuit
Strobe Input to Logical "0" Output		20		ns		20 mV				AC Test Circuit
Differential Input Overload Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time		5		ns						
Min. Cycle Time		200		ns						

Note 1: For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5528 and LM5529 are guaranteed the same as LM7528 and LM7529 respectively.

Note 2: Limits in parentheses pertain to LM5529, other limits pertain to LM5528.

Note 3: Limits in parentheses pertain to LM7529, other limits pertain to LM7528.

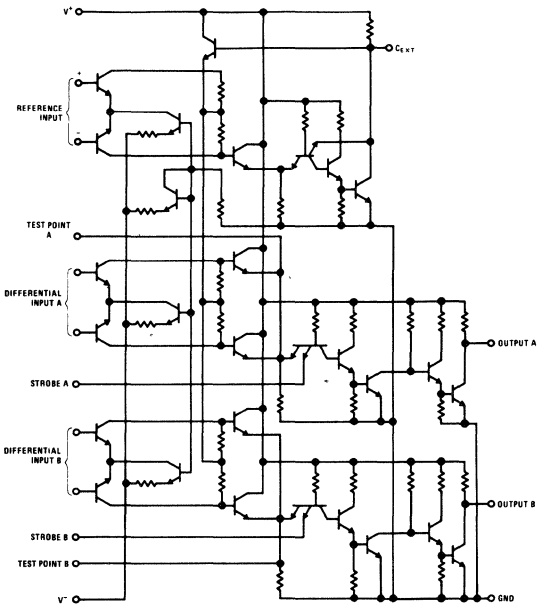
Note 4: Positive current is defined as current into the referenced pin.

Note 5: Pin 1 to have $\geq$100 pF capacitor connected to ground.

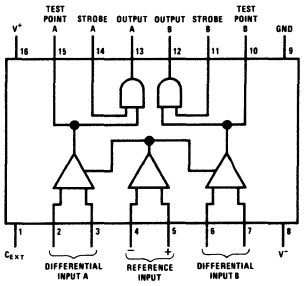
Note 6: Each test point to have $\leq$15 pF capacitive load to ground.

LM5528/LM7528 and LM5529/LM7529

schematic diagram



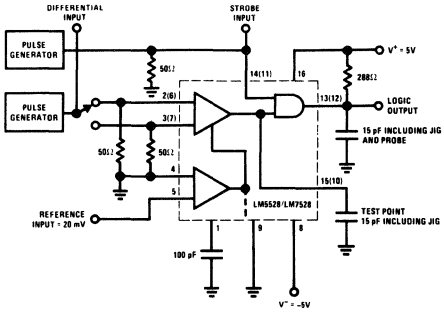
connection diagram



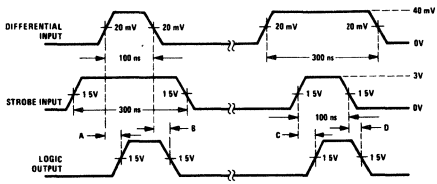
TOP VIEW

Order Number LM5528J or LM7528J
See Package 17
Order Number LM7528N
See Package 23
Order Number LM5529J or LM7529J
See Package 17
Order Number LM7529N
See Package 23

AC test circuit



voltage waveforms



1 Pulse generator characteristics
$Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2 Propagation delays
A = Differential input to logical "1" output
B = Differential input to logical "0" output
C = Strobe input to logical "1" output
D = Strobe input to logical "0" output

7

LM5534/LM7534 and LM5535/LM7535 electrical characteristics

LM5534/LM5535: The following apply for $-55°C \leq T_A \leq 125°C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF. INPUT	STROBE INPUT	LOGIC OUTPUT	SUPPLY VOLT.	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	+20 mA	±5V	Logic Output <0 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V		±5 25V	
LM7534/LM7535: The following apply for $0°C \leq T_A \leq 70°C$										
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5.25V	±5V	Logic Output <250 μA
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+20 mA	±5V	Logic Output <0 4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5 25V		±5 25V	
LM5534/LM5535: The following apply for $-55°C \leq T_A \leq 125°C$ **LM7534/LM7535: The following apply for $0°C \leq T_A \leq 70°C$**										
Diff Input Offset Current		0 5		μA	0V	0V	+5 25V		±5 25V	
Logic "0" Input Voltage			0.8	V	40 mV	20 mV	+0 8V	+5.25V	±5V	Logic Output <250 μA
Logic "1" Input Voltage	2.0			V	40 mV	20 mV	+2.0V	+20 mA	±5V	Logic Output <0.4V
Logic "0" Input Current		-1	-1.6	mA	40 mV	20 mV	+0.4V		±5.25V	
Logic "1" Input Current		5	40	μA	0V	20 mV	+2.4V		±5 25V	
		0.02	1	mA	0V	20 mV	+5 25V		±5 25V	
Logic "0" Output Voltage		0.25	0.40	V	40 mV	20 mV	+2V	+20 mA	±4.75V	
Output Leakage Current		0.01	250	μA	40 mV	20 mV	+0.8V	+5 25V	±4 75V	
V^+ Supply Current		28	38	mA	0V	20 mV	0V		±5 25V	
V^- Supply Current		-13	-18	mA	0V	20 mV	0V		±5 25V	
LM5534/LM5535 and LM7534/LM7535: The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$										
AC Common-Mode Input Firing Voltage		±2.5		V	PULSE	20 mV	+5V	SCOPE		
Propagation Delays										
Differential Input to Logical "1" Output		24		ns		20 mV				AC Test Circuit
Differential Input to Logical "0" Output		20	40	ns		20 mV				AC Test Circuit
Strobe Input to Logical "1" Output		16		ns		20 mV				AC Test Circuit
Strobe Input to Logical "0" Output		10	30	ns		20 mV				AC Test Circuit
Differential Input Overload Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time		5		ns						
Min. Cycle Time		200		ns						

Note 1: For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5534 and LM5535 are guaranteed the same as LM7534 and LM7535 respectively

Note 2: Limits in parentheses pertain to LM5535, other limits pertain to LM5534.

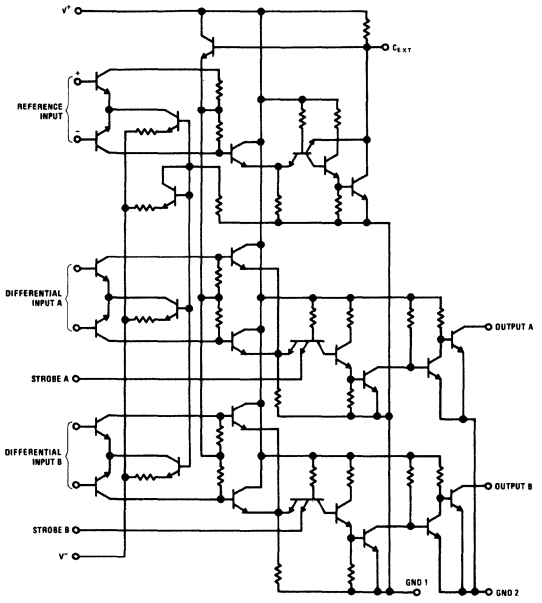
Note 3: Limits in parentheses pertain to LM7535, other limits pertain to LM7534.

Note 4: Positive current is defined as current into the referenced pin.

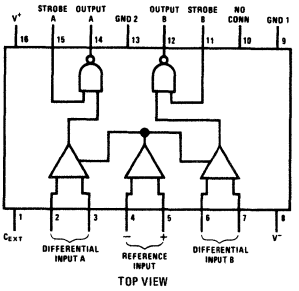
Note 5: Pin 1 to have $\geq$ 100 pF capacitor connected to ground.

LM5534/LM7534 and LM5535/LM7535

schematic diagram



connection diagram



TOP VIEW

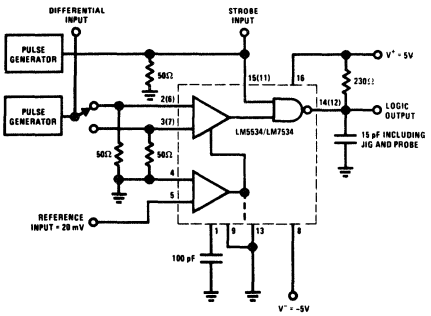
Order Number LM5534J or LM7534J
See Package 17

Order Number LM7534N
See Package 23

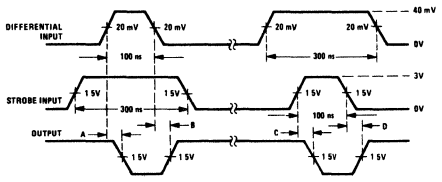
Order Number LM5535J or LM5535J
See Package 17

Order Number LM7535N
See Package 23

AC test circuit



voltage waveforms



1. Pulse generator characteristics
   Z_{OUT} = 50Ω, t_r = t_f = 15 ±5 ns, PRR = 1 MHz
2. Propagation delays.
   A = Differential input to logical "0" output
   B = Differential input to logical "1" output
   C = Strobe input to logical "0" output
   D = Strobe input to logical "1" output

7

LM5538/LM7538 and LM5539/LM7539 electrical characteristics

LM5538/LM5539: The following apply for $-55°C \leq T_A \leq 125°C$ (Note 1)

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS (EACH AMPLIFIER) DIFF. INPUT	REF. INPUT	STROBE INPUT	LOGIC OUTPUT	SUPPLY VOLT.	COMMENTS
Differential Input Threshold Voltage (V_{TH}) (Note 2)	10(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		15	20(22)	mV	$\pm V_{TH}$	15 mV	+5V	+20 mA	±5V	Logic Output <0 4V
	35(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5 25V	±5V	Logic Output <250 μA
		40	45(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V	Logic Output <0 4V
Differential & Reference Input Bias Current		30	100	μA	0V	0V	+5 25V		±5.25V	
LM7538/LM7539: The following apply for $0°C \leq T_A \leq 70°C$										
Differential Input Threshold Voltage (V_{TH}) (Note 3)	11(8)	15		mV	$\pm V_{TH}$	15 mV	+5V	+5.25V	±5V	Logic Output <250 μA
		15	19(22)	mV	$\pm V_{TH}$	15 mV	+5V	+20 mA	±5V	Logic Output <0.4V
	36(33)	40		mV	$\pm V_{TH}$	40 mV	+5V	+5.25V	±5V	Logic Output <250 μA
		40	44(47)	mV	$\pm V_{TH}$	40 mV	+5V	+20 mA	±5V	Logic Output <0.4V
Differential & Reference Input Bias Current		30	75	μA	0V	0V	+5.25V		±5 25V	
LM5538/LM5539: The following apply for $-55°C \leq T_A \leq 125°C$ LM7538/LM7539: The following apply for $0°C \leq T_A \leq 70°C$										
Diff. Input Offset Current		0.5		μA	0V	0V	+5.25V		±5 25V	
Logic "1" Input Voltage	2			V	40 mV	20 mV	+2V	+20 mA	±5V	Logic Output <0 4V
Logic "0" Input Voltage			0.8	V	40 mV	20 mV	+0.8V	+5 25V	±5V	Logic Output <250 μA
Logic "0" Input Current		-1	-1.6	mA	40 mV	20 mV	+0.4V		±5 25V	
Logic "1" Input Current		5	40	μA	0V	20 mV	+2.4V		±5.25V	
		0.02	1	mA	0V	20 mV	+5.25V		±5.25V	
Logic "0" Output Voltage		0.25	0.40	V	40 mV	20 mV	+2.0V	+20 mA	±4 75V	
Output Leakage Current		0.01	250	μA	40 mV	20 mV	+0.8V	+5.25V	±4.75V	
V^+ Supply Current		28	38	mA	0V	20 mV	0V		±5.25V	
V^- Supply Current		-13	-18	mA	0V	20 mV	0V		±5.25V	
LM5538/LM5539 and LM7538/LM7539: The following apply for $T_A = 25°C$, $V^+ = 5V$, $V^- = -5V$										
AC Common-Mode Input Firing Voltage		±2.5		V	PULSE	20 mV	+5V	SCOPE		
Propagation Delays										
Differential Input to Logical "1" Output		24		ns		20 mV				AC Test Circuit
Differential Input to Logical "0" Output		20	40	ns		20 mV				AC Test Circuit
Strobe Input to Logical "1" Output		16		ns		20 mV				AC Test Circuit
Strobe Input to Logical "0" Output		10	30	ns		20 mV				AC Test Circuit
Differential Input Overload Recovery Time		10		ns						
Common-Mode Input Overload Recovery Time		5		ns						
Min. Cycle Time		200		ns						

Note 1: For $0°C \leq T_A \leq 70°C$ operation, electrical characteristics for LM5538 and LM5539 are guaranteed the same as LM7538 and LM7539 respectively.

Note 2: Limits in parentheses pertain to LM5539, other limits pertain to LM5538.

Note 3: Limits in parentheses pertain to LM7539, other limits pertain to LM7538.

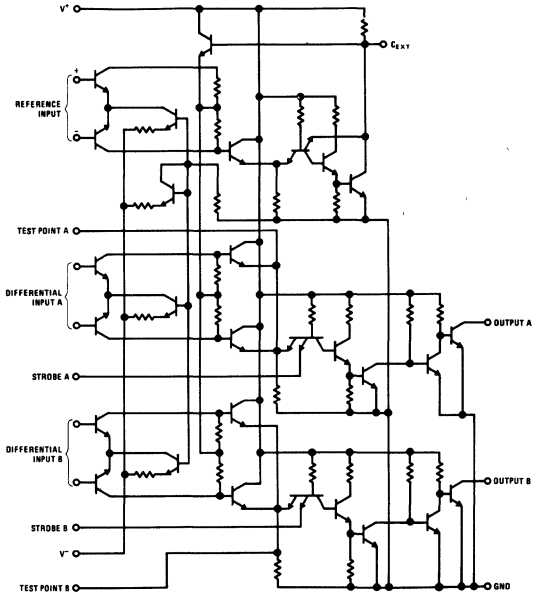
Note 4: Positive current is defined as current into the referenced pin.

Note 5: Pin 1 to have $\geq$100 pF capacitor connected to ground.

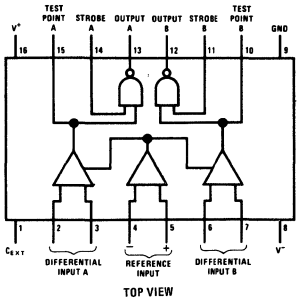
Note 6: Each test point to have $\leq$15 pF capacitive load to ground.

LM5538/LM7538 and LM5539/LM7539

schematic diagram



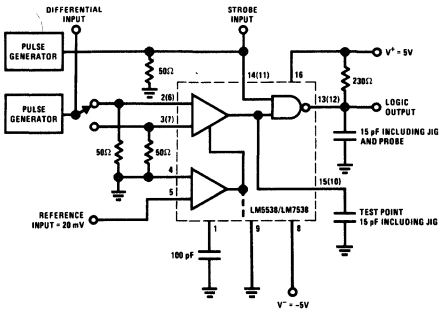
connection diagram



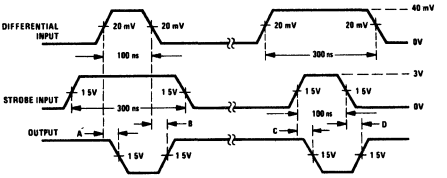
TOP VIEW

Order Number LM5538J or LM5538J
See Package 17
Order Number LM7538N
See Package 23
Order Number LM5539J or LM7539J
See Package 17
Order Number LM7539N
See Package 23

AC test circuit



voltage waveforms

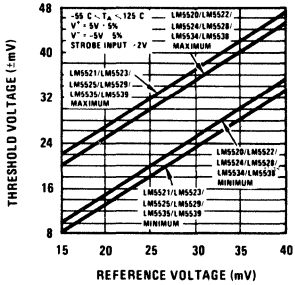


1 Pulse generator characteristics
$Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2 Propagation delays
A = Differential input to logical "0" output
B = Differential input to logical "1" output
C = Strobe input to logical "0" output
D = Strobe input to logical "1" output

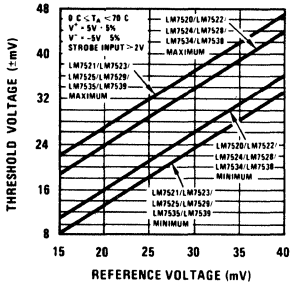
7

guaranteed performance characteristics

Differential Input Threshold Voltage

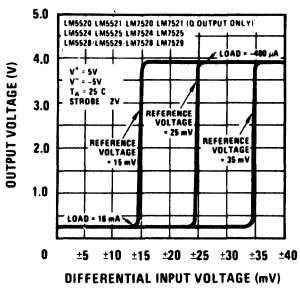


Differential Input Threshold Voltage

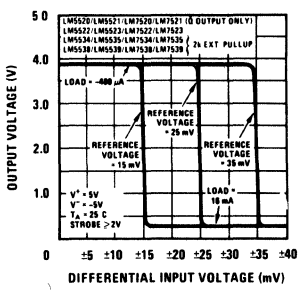


typical performance characteristics

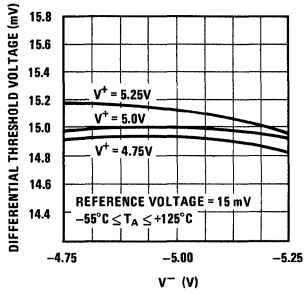
Transfer Characteristics



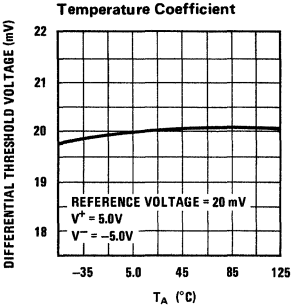
Transfer Characteristics



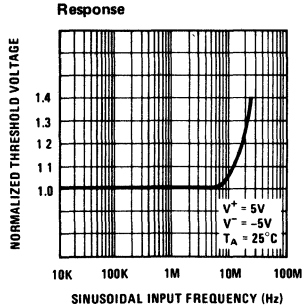
Power Supply Rejection



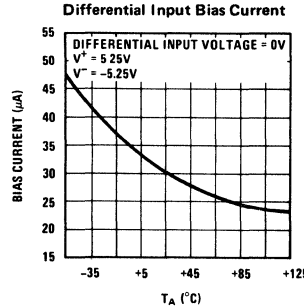
Temperature Coefficient



Differential Input Frequency Response

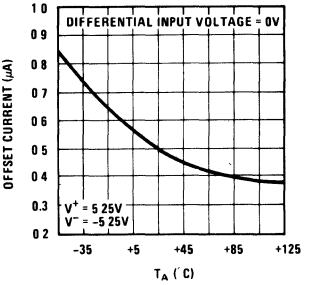


Differential Input Bias Current

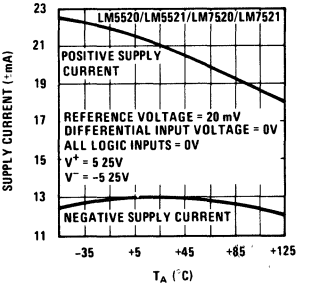


typical performance characteristics (cont.)

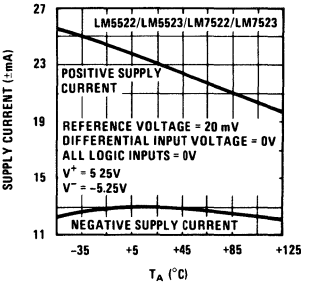
Differential Input Offset Current



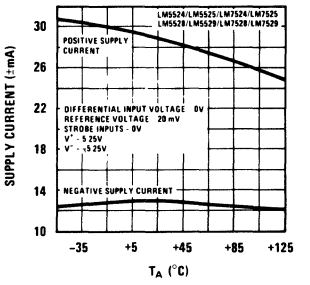
Power Supply Currents



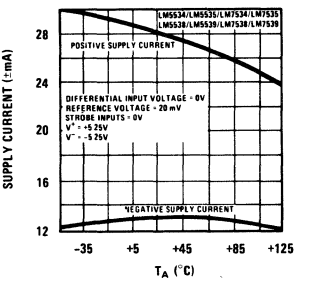
Power Supply Currents



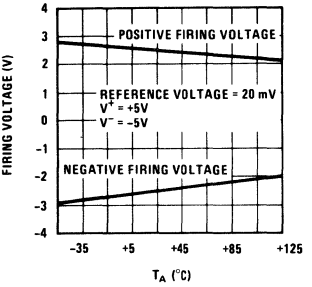
Power Supply Currents



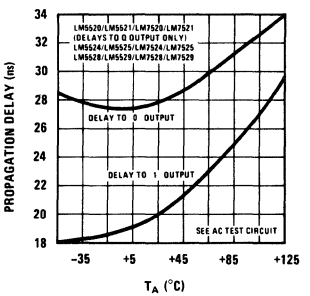
Power Supply Currents



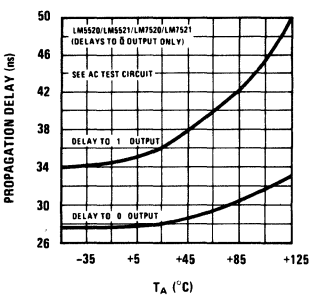
AC Common-Mode Firing Voltage



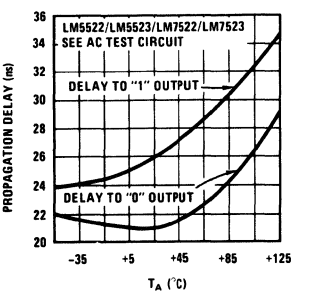
Differential Input to Output Propagation Delays



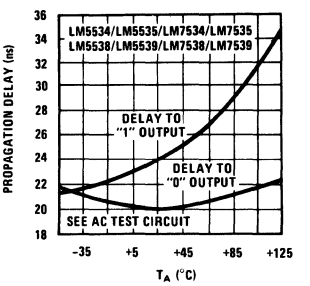
Differential Input to Output Propagation Delays



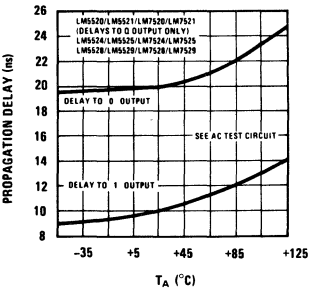
Differential Input to Output Propagation Delays



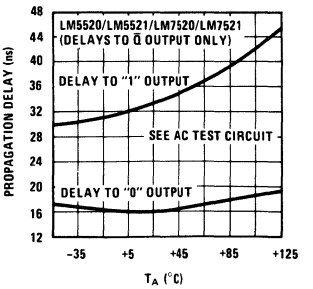
Differential Input to Output Propagation Delays



Strobe to Output Propagation Delays



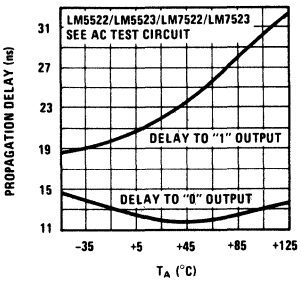
Strobe to Output Propagation Delays



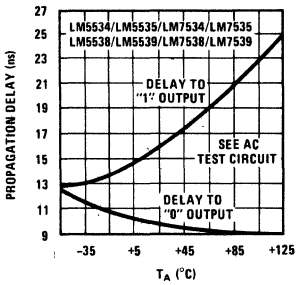
7

typical performance characteristics (cont.)

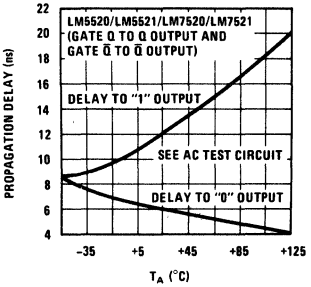
Strobe to Output Propagation Delays



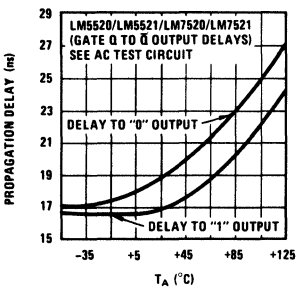
Strobe to Output Propagation Delays



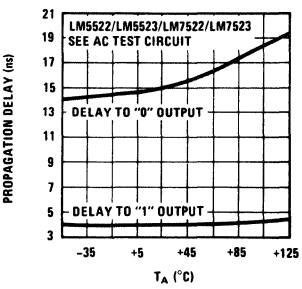
Gate to Output Propagation Delays



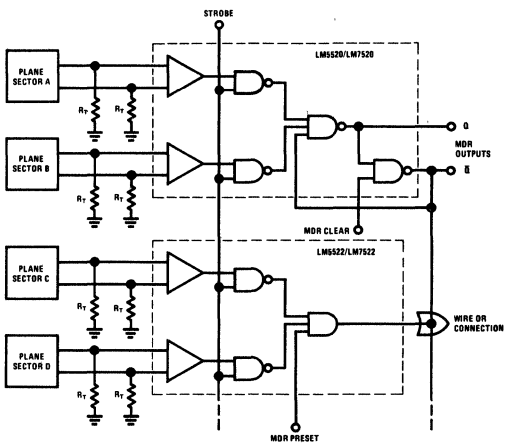
Gate to Output Propagation Delays



Gate to Output Propagation Delays

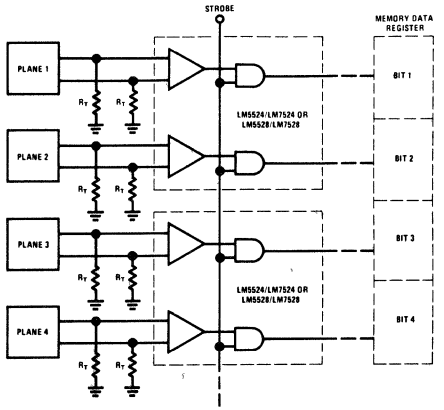


typical applications

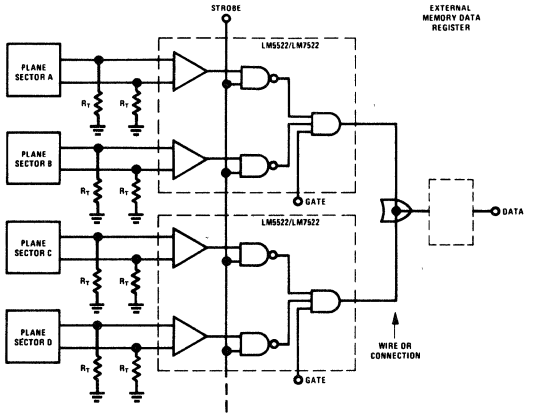


Large Memory System with Sectored Core Planes

typical applications (cont.)



Small Memory System



Large Memory System

Analog Switches

AH0014/AH0014C* DPDT, AH0015/AH0015C quad SPST, AH0019/AH0019C* dual DPST-TTL/DTL compatible MOS analog switches

general description

This series of TTL/DTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors; the second chip is a bipolar I.C. gate and level shifter. The series is available in both hermetic dual-in-line package and flatpack.

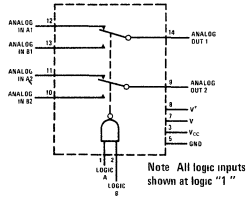
features

- Large analog voltage switching ±10V
- Fast switching speed 500 ns
- Operation over wide range of power supplies
- Low ON resistance 200Ω
- High OFF resistance $10^{11}\Omega$
- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

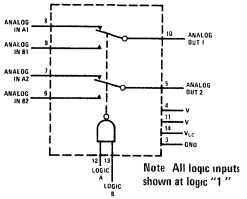
These switches are particularly suited for use in both military and industrial applications such as commutators in data acquisition systems, multiplexers, A/D and D/A converters, long time constant integrators, sample and hold circuits, modulators/demodulators, and other analog signal switching applications. For information on other National analog switches and analog interface elements, see listing on last page.

The AH0014, AH0015 and AH0019 are specified for operation over the −55°C to +125°C military temperature range. The AH0014C, AH0015C and AH0019C are specified for operation over the −25°C to +85°C temperature range.

block and connection diagrams

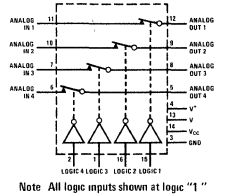


Order Number AH0014F or AH0014CF
See Package 4



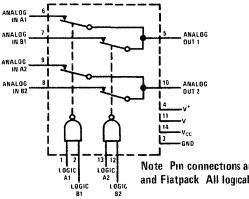
Order Number AH0014D or AH0014CD
See Package 1

Quad SPST



Order Number AH0015D or AH0015CD
See Package 2

Dual DPST

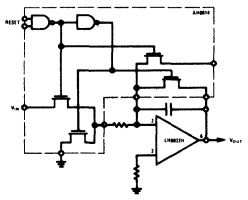


Order Number AH0019F or AH0019CF
See Package 4

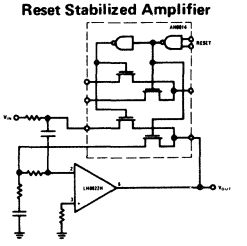
Order Number AH0019D or AH0019CD
See Package 1

typical applications

Integrator



Reset Stabilized Amplifier



*Previously called NH0014/NH0014C and NH0019/NH0019C

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absolute maximum ratings

V_{CC} Supply Voltage	7.0V
V^- Supply Voltage	−30V
V^+ Supply Voltage	+30V
V^+/V^- Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
AH0014, AH0015, AH0019	−55°C to +125°C
AH0014C, AH0015C, AH0019C	−25°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 0.4V		0.2	0.4	mA
Power Supply Current Logical "1" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" Input – each gate (Note 3)	V_{CC} = 5.5V V_{IN} = 0V				
AH0014, AH0014C			1.5	3.0	mA
AH0015, AH0015C			0.22	0.41	mA
AH0019, AH0019C			0.22	0.41	mA
Analog Switch ON Resistance – each gate	V_{IN} (Analog) = +10V		75	200	Ω
	V_{IN} (Analog) = −10V		150	600	Ω
Analog Switch OFF Resistance			10^{11}		Ω
Analog Switch Input Leakage Current – each input (Note 4)	V_{IN} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		25	200	pA
	T_A = 125°C		25	200	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.1	10	nA
	T_A = 70°C		30	100	nA
Analog Switch Output Leakage Current – each output (Note 4)	V_{OUT} = −10V				
AH0014, AH0015, AH0019	T_A = 25°C		40	400	pA
	T_A = 125°C		40	400	nA
AH0014C, AH0015C, AH0019C	T_A = 25°C		0.05	10	nA
	T_A = 70°C		4	50	nA
Analog Input (Drain) Capacitance	1 MHz @ Zero Bias		8	10	pF
Output Source Capacitance	1 MHz @ Zero Bias		11	13	pF
Analog Turn-OFF Time – t_{OFF}	See test circuit; T_A = 25°C		400	500	ns
Analog Turn-ON Time – t_{ON}	See test circuit; T_A = 25°C				
AH0014, AH0014C			350	425	ns
AH0015, AH0015C			100	150	ns
AH0019, AH0019C			100	150	ns

Note 1: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for AH0014, AH0015, AH0019 and −25°C to +85°C for AH0014C, AH0015C, AH0019C. V^- = −20V. V^+ = +10V and an analog test current of 1 mA unless otherwise specified.

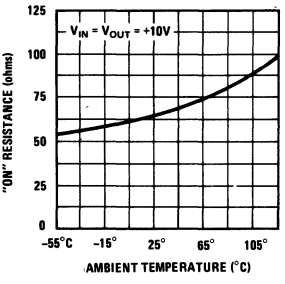
Note 2: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V. V^+ = +10V, V^- = −22V.

Note 3: Current measured is drawn from V_{CC} supply.

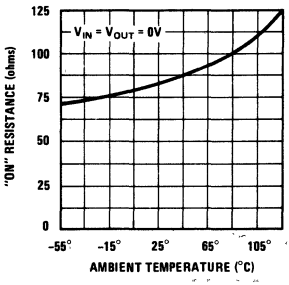
Note 4: All analog switch pins except measurement pin are tied to V^+

analog switch characteristics (Note 2)

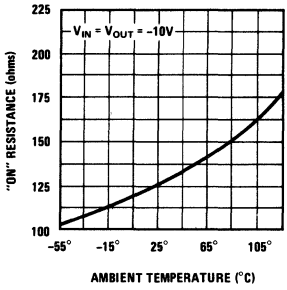
R_{ON} vs Temperature



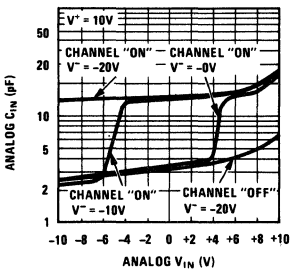
R_{ON} vs Temperature



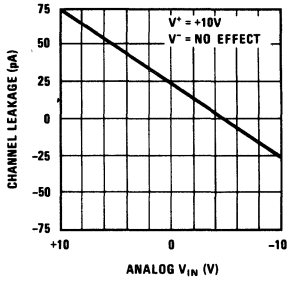
R_{ON} vs Temperature



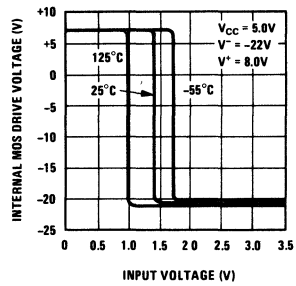
C_{IN} vs V_{IN}



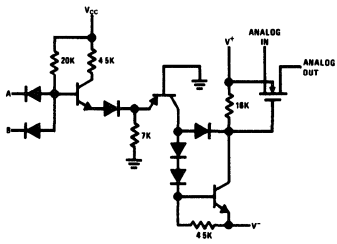
Leakage vs V_{IN} (Channel "OFF")



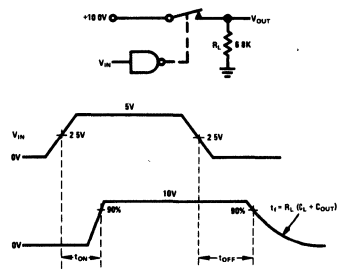
Driver Gate V_{IN} vs V_{OUT}



Schematic (Single Driver Gate and MOS Switch Shown)

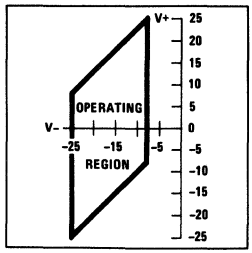


Analog Switching Time Test Circuit



selecting power supply voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V^- is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V^+ is governed by supply V^-. With a value chosen for V^-, V^+ may be selected as any value along a vertical line passing through the V^- value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



8

Analog Switches

AH0120/AH0130/AH0140/AH0150/AH0160 series analog switches

general description

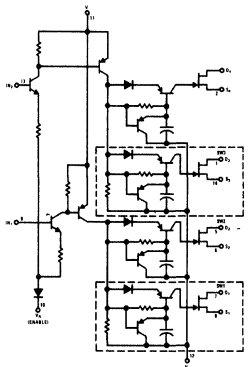
The AH0100 series represents a complete family of junction FET analog switches. The inherent flexibility of the family allows the designer to tailor the device selection to the particular application. Switch configurations available include dual DPST, dual SPST, DPDT, and SPDT. $r_{ds(ON)}$ ranges from 10 ohms through 100 ohms. The series is available in both 14 lead flat pack and 14 lead cavity DIP. Important design features include:

- TTL/DTL and RTL compatible logic inputs
- Up to 20V p-p analog input signal
- $r_{ds(ON)}$ less than 10Ω (AH0140, AH0141, AH0145, AH0146)
- Analog signals in excess of 1 MHz
- "OFF" power less than 1 mW
- Gate to drain bleed resistors eliminated
- Fast switching, t_{ON} is typically .4 μs, t_{OFF} is 1.0 μs
- Operation from standard op amp supply voltages, ±15V, available (AH0150/AH0160 series)
- Pin compatible with the popular DG 100 series.

The AH0100 series is designed to fulfill a wide variety of analog switching applications including commutators, multiplexers, D/A converters, sample and hold circuits, and modulators/demodulators. The AH0100 series is guaranteed over the temperature range −55°C to +125°C; whereas, the AH0100C series is guaranteed over the temperature range −25°C to +85°C.

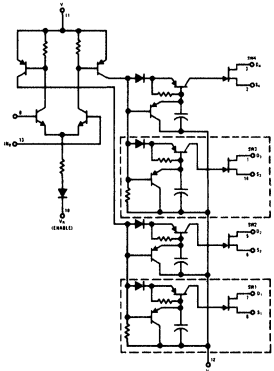
schematic diagrams

DUAL DPST and DUAL SPST



Note Dotted line portions are not applicable to the dual SPST.

DPDT (diff.) and SPDT (diff.)

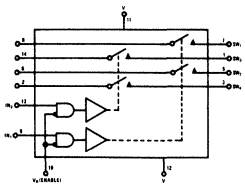


Note Dotted line portions are not applicable to the SPDT (differential)

logic and connection diagrams

Order any of the devices below using the part number with a D or F suffix. See Packages 1 and 4.

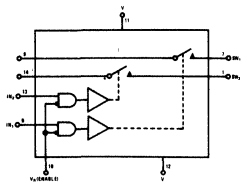
DUAL DPST



HIGH LEVEL (±10V)
AH0140 (10Ω)
AH0129 (30Ω)
AH0126 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0153 (15Ω)
AH0154 (50Ω)

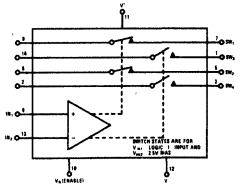
DUAL SPST



HIGH LEVEL (±10V)
AH0141 (10Ω)
AH0133 (30Ω)
AH0134 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0151 (15Ω)
AH0152 (50Ω)

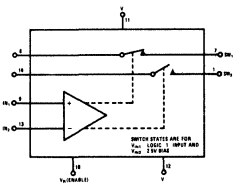
DPDT (Diff)



HIGH LEVEL (±10V)
AH0145 (10Ω)
AH0139 (30Ω)
AH0142 (80Ω)

MEDIUM LEVEL (±7.5)
AH0163 (15Ω)
AH0164 (50Ω)

SPDT (Diff)



HIGH LEVEL (±10V)
AH0146 (10Ω)
AH0144 (30Ω)
AH0143 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0161 (15Ω)
AH0162 (50Ω)

absolute maximum ratings

	High Level	Medium Level
Total Supply Voltage ($V^+ - V^-$)	36V	34V
Analog Signal Voltage ($V^+ - V_A$ or $V_A - V^-$)	30V	25V
Positive Supply Voltage to Reference ($V^+ - V_R$)	25V	25V
Negative Supply Voltage to Reference ($V_R - V^-$)	22V	22V
Positive Supply Voltage to Input ($V^+ - V_{IN}$)	25V	25V
Input Voltage to Reference ($V_{IN} - V_R$)	±6V	±6V
Differential Input Voltage ($V_{IN} - V_{IN2}$)	±6V	±6V
Input Current, Any Terminal	30 mA	30 mA
Power Dissipation		See Curve
Operating Temperature Range AH0100 Series		−55°C to +125°C
AH0100C Series		−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics for "HIGH LEVEL" Switches (Note 1)

PARAMETER	SYMBOL	DEVICE TYPE: DUAL DPST	DUAL SPST	DPDT (DIFF)	SPDT (DIFF)	CONDITIONS (V^+ = 12.0V, V^- = −18.0V, V_R = 0.0V)		LIMITS: TYP	MAX	UNITS
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	T_A = 25°C	2.0	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	T_A = 25°C	0.1	.1	µA
							Over Temp. Range		2.0	µA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	−1.0	−1.8	mA
							Over Temp. Range		−2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	−1.0	−1.4	mA
							Over Temp. Range		−1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2}$ = 0.8V	T_A = 25°C	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2}$ = 0.8V	T_A = 25°C	−1.0	−10	µA
							Over Temp. Range		−25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				$V_{IN1} = V_{IN2}$ = 0.8V	T_A = 25°C	−1.0	−10	µA
							Over Temp. Range		−25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0126	AH0134	AH0142	AH0143	V_D = 10V, I_D = 1 mA	T_A = 25°C	45	80	Ω
							Over Temp. Range		150	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0129	AH0133	AH0139	AH0144	V_D = 10V, I_D = 1 mA	T_A = 25°C	25	30	Ω
							Over Temp. Range		60	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0140	AH0141	AH0145	AH0146	V_D = 10V, I_F = 1 mA	T_A = 25°C	8.0	10	Ω
							Over Temp. Range		20	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S$ = −10V	T_A = 25°C	0.1	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0126, AH0129	AH0134, AH0133	AH0142, AH0139	AH0143, AH0144	V_{DS} = ±20V	T_A = 25°C	0.8	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0140	AH0141	AH0145	AH0146	V_{DS} = ±20V	T_A = 25°C	4.0	10	nA
							Over Temp. Range		1.0	µA
Switch Turn-ON Time	t_{ON}	AH0126, AH0129	AH0134, AH0133	AH0142, AH0139	AH0143, AH0144	See Test Circuit, V_A = ±10V, T_A = 25°C		0.5	0.8	µs
Switch Turn-ON Time	t_{ON}	AH0140	AH0141	AH0145	AH0146	See Test Circuit, V_A = ±10V, T_A = 25°C		0.8	1.0	µs
Switch Turn-OFF Time	t_{OFF}	AH0126, AH0129	AH0134, AH0133	AH0142, AH0139	AH0143, AH0144	See Test Circuit, V_A = ±10V, T_A = 25°C		0.9	1.6	µs
Switch Turn-OFF Time	t_{OFF}	AH0140	AH0141	AH0145	AH0146	See Test Circuit, V_A = ±10V, T_A = 25°C		1.1	2.5	µs

Note 1: Unless otherwise specified these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for T_A = 25°C.

Note 2: For the DPST and Dual DPST, the ON condition is for V_{IN} = 2.5V; the OFF condition is for V_{IN} = 0.8V. For the differential switches and SW1 and 2 ON, V_{IN2} = 2.5V, V_{IN1} = 3.0V. For SW3 and 4 ON, V_{IN2} = 2.5V, V_{IN1} = 2.0V.

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electrical characteristics for "MEDIUM LEVEL" Switches (Note 1)

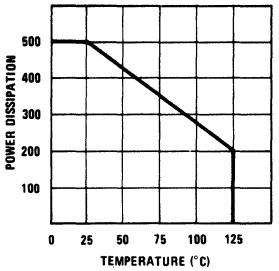
PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DUAL DPDT	SPDT (DIFF)	V^+ = +15 0V, V^- = −15V, V_R = 0V		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	T_A = 25°C	20	60	µA
							Over Temp Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	T_A = 25°C	01	0 1	µA
							Over Temp Range		2	µA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	2 2	3 0	mA
							Over Temp Range		3 3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	−1 0	−1 8	mA
							Over Temp Range		−2 0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	T_A = 25°C	−1 0	−1 4	mA
							Over Temp Range		−1 6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				V_{IN1} = V_{IN2} = 0 8V	T_A = 25°C	1 0	10	µA
							Over Temp Range		25	µA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				V_{IN1} = V_{IN2} = 0 8V	T_A = 25°C	−1 0	−10	µA
							Over Temp Range		−25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				V_{IN1} = V_{IN2} = 0 8V	T_A = 25°C	−1 0	−10	µA
							Over Temp Range		−25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0153	AH0151	AH0163	AH0161	V_D = 7 5V, I_D = 1 mA	T_A = 25°C	10	15	Ω
							Over Temp Range		30	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0154	AH0152	AH0164	AH0162	V_D = 7 5V, I_D = 1 mA	T_A = 25°C	45	50	Ω
							Over Temp Range		100	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				V_D = V_S = −7 5V	T_A = 25°C	01	2	nA
							Over Temp Range		500	nA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0153	AH0151	AH0163	AH0161	V_{DS} = ±15V	T_A = 25°C	5	10	nA
							Over Temp Range		1 0	µA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0154	AH0152	AH0164	AH0162	V_{DS} = ±15 0V	T_A = 25°C	1 0	2 0	nA
							Over Temp Range		200	nA
Switch Turn-ON Time	t_{ON}	AH0153	AH0151	AH0163	AH0161	See Test Circuit, V_A = ±7 5V, T_A = 25°C		0 8	1 0	µs
Switch Turn-ON Time	t_{ON}	AH0154	AH0152	AH0164	AH0162	See Test Circuit, V_A = ±7 5V, T_A = 25°C		0 5	0 8	µs
Switch Turn-OFF Time	t_{OFF}	AH0153	AH0151	AH0163	AH0161	See Test Circuit, V_A = ±7 5V, T_A = 25°C		1 1	2 5	µs
Switch Turn-OFF Time	t_{OFF}	AH0154	AH0152	AH0164	AH0162	See Test Circuit, V_A = ±7 5V, T_A = 25°C		0 9	1 5	µs

Note 1: Unless otherwise specified, these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for T_A = 25°C.

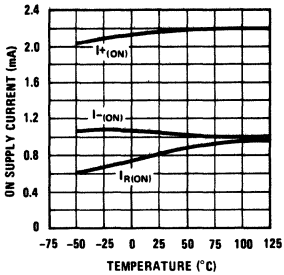
Note 2: For the DPST and Dual DPST, the ON condition is for V_{IN} = 2.5V; the OFF condition is for V_{IN} = 0.8V. For the differential switches and SW1 and 2 ON, V_{IN2} = 2.5V, V_{IN1} = 3.0V. For SW3 and 4 ON, V_{IN2} = 2.5V, V_{IN1} = 2.0V.

typical performance characteristics

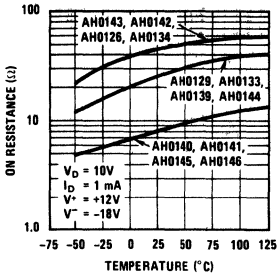
Power Dissipation vs Temperature



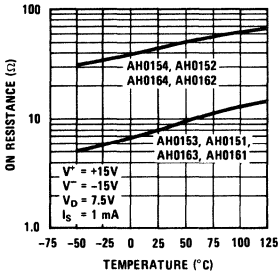
ON Supply Current vs Temperature



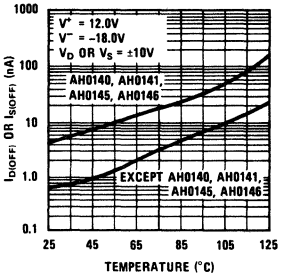
rds(ON) vs Temperature AH0120 thru AH0140 Series



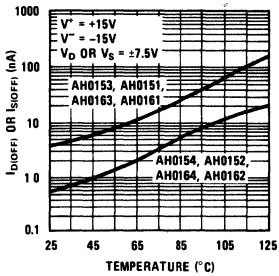
rds(ON) vs Temperature AH0150/AH0160 Series



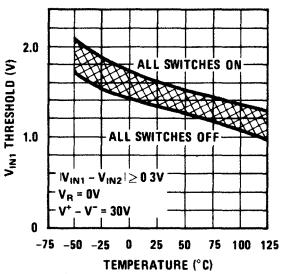
Leakage Current vs Temperature AH0120, AH0130, & AH0140



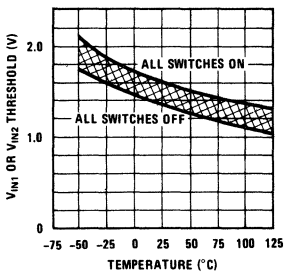
Leakage Current vs Temperature AH0150 & AH0160



Single Ended Switch Input Threshold vs Temperature

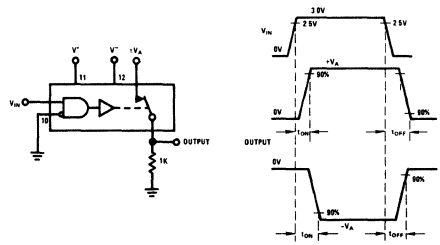


Differential Switch Input Threshold vs Temperature

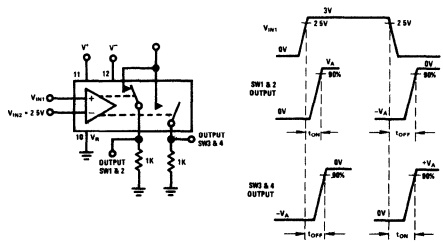


switching time test circuits

Single Ended Input



Differential Input



applications information

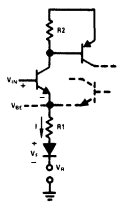
1. INPUT LOGIC COMPATIBILITY

A. Voltage Considerations

In general, the AH0100 series is compatible with most DTL, TTL, and RTL logic families. The ON-input threshold is determined by the V_{BE} of the input transistor plus the V_f of the diode in the emitter leg, plus I x R_1, plus V_R. At room temperature and V_R = 0V, the nominal ON threshold is: 0.7V+0.7V+0.2V$_f$=1.6V. Over temperature and manufacturing tolerances, the threshold may be as high as 2.5V and as low as 0.8V. The rules for proper operation are:

$V_{IN} - V_R \geq 2.5V$ All switches ON

$V_{IN} - V_R \leq 0.8V$ All switches OFF



B. Input Current Considerations

$I_{IN(ON)}$, the current drawn by the driver with V_{IN} = 2.5V is typically 20 μA at 25°C and is guaranteed less than 120 μA over temperature. DTL, such as the DM930 series can supply 180 μA at logic "1" voltages in excess of 2.5V. TTL output levels are comparable at 400 μA. The DTL and TTL can drive the AH0100 series directly. However, at low temperature, DC noise margin in the logic "1" state is eroded with DTL. A pull-up resistor of 10 kΩ is recommended when using DTL over military temperature range.

If more than one driver is to be driven by a DM930 series (6K) gate, an external pull-up resistor should be added. The value is given by:

$$R_P = \frac{11}{N-1} \text{ for } N > 2$$

where:

R_P = value of the pull-up resistor in kΩ

N = number of drivers.

C. Input Slew Rate

The slew rate of the logic input must be in excess of 0.3V/μs in order to assure proper operation of the analog switch. DTL, TTL, and RTL output rise times are far in excess of the minimum slew rate requirements. Discrete logic designs, however, should include consideration of input rise time.

2. ENABLE CONTROL

The application of a positive signal at the V_R terminal will open all switches. The V_R (ENABLE) signal must be capable of rising to within 0.8V of $V_{IN(ON)}$ in the OFF state and of sinking $I_{R(ON)}$ milliamps in the ON state (at $V_{IN(ON)} - V_R >$ 2.5V). The V_R terminal can be driven from most TTL and DTL gates.

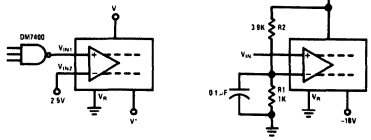
3. DIFFERENTIAL INPUT CONSIDERATIONS

The differential switch driver is essentially a differential amplifier. The input requirements for proper operation are:

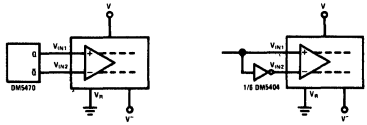
$$|V_{IN1} - V_{IN2}| \geq 0.3V$$

$$2.5 \leq (V_{IN1} \text{ or } V_{IN2}) - V_R \leq 5V$$

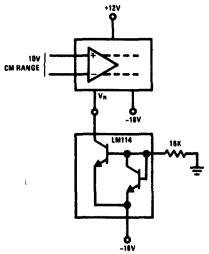
The differential driver may be furnished by a DC level as shown below. The level may be derived from a voltage divider to V^+ or the 5V V_{CC} of the DTL logic. In order to assure proper operation, the divider should be "stiff" with respect to I_{IN2}. Bypassing R1 with a 0.1 μF disc capacitor will prevent degradation of t_{ON} and t_{OFF}.



Alternatively, the differential driver may be driven from a TTL flip-flop or inverter.



Connection of a 1 mA current source between V_R and V^- will allow operation over a ±10V common mode range. Differential input voltage must be less than the 6V breakdown, and input threshold of 2.5V and 300mV differential overdrive still prevail.



4. ANALOG VOLTAGE CONSIDERATIONS

The rules for operating the AH0100 series at supply voltages other than those specified essentially breakdown into OFF and ON considerations. The OFF considerations are dictated by the maximum negative swing of the analog signal and the pinch off of the JFET switch. In the OFF state, the gate of the FET is at $V^- + V_{BE} + V_{SAT}$ or about 1.0V above the V^- potential. The maximum V_P of the FET switches is 7V. The most negative analog voltage, V_A, swing which can be accomodated for any given supply voltage is:

$$|V_A| \leq |V^-| - V_P - V_{BE} - V_{SAT} \text{ or}$$

$$|V_A| \leq |V^-| - 8.0 \text{ or } |V^-| \geq |V_A| + 8.0V$$

For the standard high level switches, $V_A \leq |-18| + 8 = -10V$. The value for V^+ is dictated by the maximum positive swing of the analog input voltage. Essentially the collector to base junction of the turn-on PNP must remain reversed biased for all positive value of analog input voltage. The base of the PNP is at $V^+ - V_{SAT} - V_{BE}$ or $V^+ - 1.0V$. The PNP's collector base junction should have at least 1.0V reverse bias. Hence, the most positive analog voltage swing which may be accommodated for a given value of V^+ is:

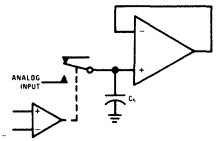
$$V_A \leq V^+ - V_{SAT} - V_{BE} - 1.0V \text{ or}$$

$$V_A \leq V^+ - 2.0V \text{ or } V^+ \geq V_A + 2.0V$$

For the standard high level switches, $V_A = 12 - 2.0V = +10V$.

5. SWITCHING TRANSIENTS

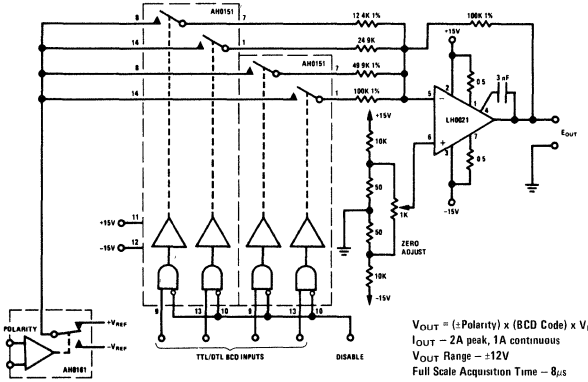
Due to charge stored in the gate-to-source and gate-to-drain capacitances of the FET switch, transients may appear in the output during switching. This is particularly true during the OFF to ON transition. The magnitude and duration of the transient may be minimized by making source and load impedance levels as small as practical.



Furthermore, transients may be minimized by operating the switches in the differential mode; i.e., the charge delivered to the load during the ON to OFF transition is, to a large extent, cancelled by the OFF to ON transition.

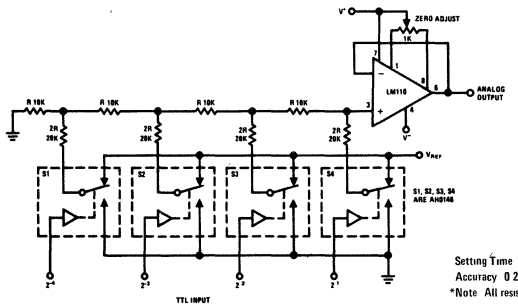
typical applications

Programmable One Amp Power Supply



V_{OUT} = (±Polarity) x (BCD Code) x V_{REF}
I_{OUT} – 2A peak, 1A continuous
V_{OUT} Range – ±12V
Full Scale Acquisition Time – 8 μs

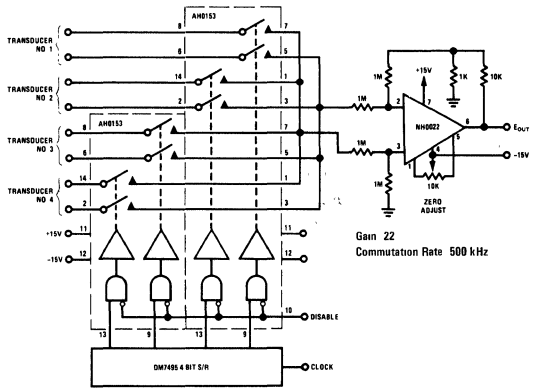
Four to Ten Bit D to A Converter (4 Bits Shown)



Setting Time 1 μs
Accuracy 0.2%
*Note All resistors are 0.1%

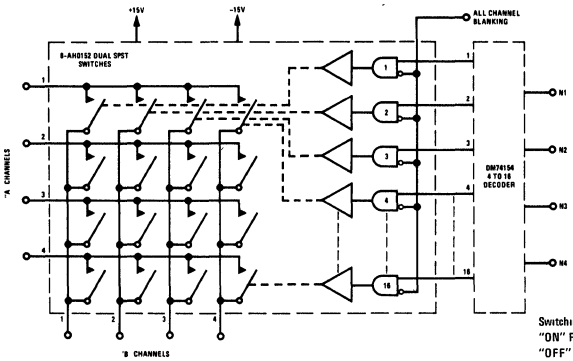
typical applications (con't)

Four Channel Differential Transducer Commutator



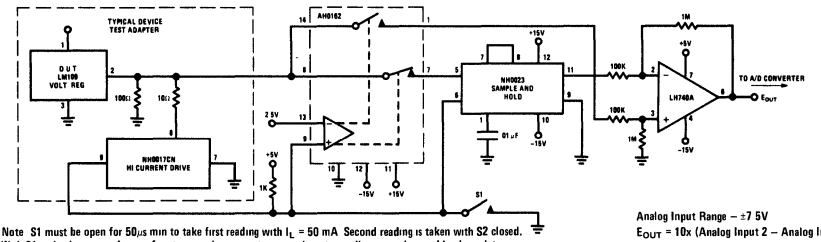
Gain 22
Commutation Rate 500 kHz

4 x 4 Cross Point Analog Switch



Switching Time – 800 ns
"ON" Resistance – 45Ω
"OFF" Resistance – $10^{10}\Omega$

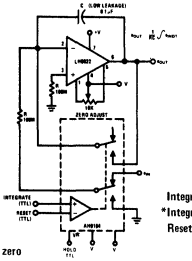
Delta Measurement System for Automatic Linear Circuit Tester



Note S1 must be open for 50μs min to take first reading with I_L = 50 mA. Second reading is taken with S2 closed. With S1 and other set-up forcing functions under computer control, system will measure line and load regulation on voltage regulators, voltage gain, offset current, CMRR and PSRR on op amps as well as other circuits requiring measurement of the change of a parameter with the change of a forcing function

Analog Input Range – ±7.5V
E_{OUT} = 10x (Analog Input 2 – Analog Input 1)
Error Rate – 0.01% F.S./sec

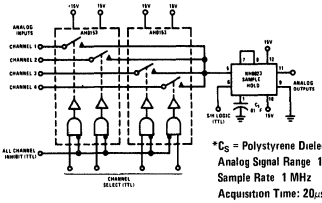
Precision Long Time Constant Integrator with Reset



Integration Internal = 10 sec
*Integration Error = 100μV
Reset Time 30μs

*Note: V_{OS} adjusted to zero

Four Channel Commutator



*C_S = Polystyrene Dielectric
Analog Signal Range 15 Vp-p
Sample Rate 1 MHz
Acquisition Time: 20μs
Drift Rate 0.5 mV/sec

Analog Switches

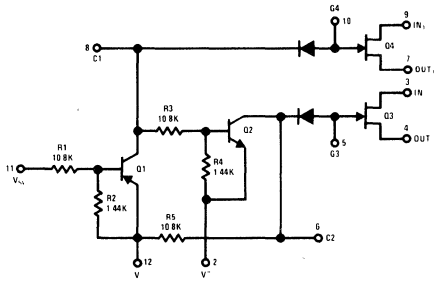
AH2114/AH2114C DPST analog switch general description

The AH2114 is a DPST analog switch circuit comprised of two junction FET switches and their associated driver. The AH2114 is designed to fulfill a wide variety of high level analog switching applications including multiplexers, A to D Converters, integrators, and choppers. Design features include:

- Low ON resistance, typically 75Ω
- High OFF resistance, typically $10^{11}\Omega$
- Large output voltage swing, typically ±10V
- Powered from standard op-amp supply voltages of ±15V
- Input signals in excess of 1 MHz
- Turn-ON and turn-OFF times typically 1 μs

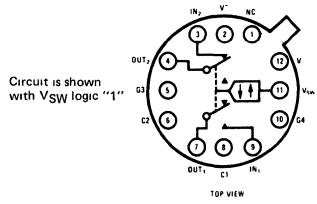
The AH2114 is guaranteed over the temperature range −55°C to +125°C whereas the AH2114C is guaranteed over the temperature range 0°C to +85°C.

schematic and connection diagrams



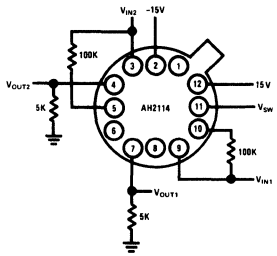
Metal Can Package

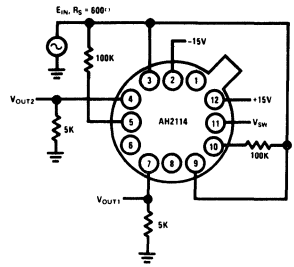
Circuit is shown with V_{SW} logic "1"

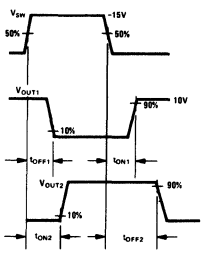


Order Number AH2114G or AH2114CG
See Package 6A

ac test circuit and waveforms







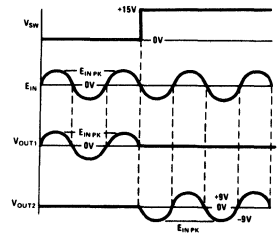


FIGURE 1.

FIGURE 2.

absolute maximum ratings

Vplus Supply Voltage	+25V
Vminus Supply Voltage	-25V
Vplus–Vminus Differential Voltage	40V
Logic Input Voltage	25V
Power Dissipation (Note 3)	1 36W
Operating Temperature Range	
AH2114	-55°C to +125°C
AH2114C	0°C to +85°C
Storage Temperature Range	-65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	AH2114			AH2114C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Static Drain-Source "On" Resistance	I_D = 1 0 mA, V_{GS} = 0V, T_A = 25°C		75	100		75	125	Ω
	I_D = 1 0 mA, V_{GS} = 0V			150			160	Ω
Drain-Gate Leakage Current	V_{DS} = 20V, V_{GS} = -7V, T_A = 25°C		0 2	1 0		0.2	5 0	nA
				60			60	nA
FET Gate-Source Breakdown Voltage	I_G = 1 0 μA V_{DS} = 0V	35			35			V
Drain-Gate Capacitance	V_{DG} = 20V, I_S = 0 f = 1.0 MHz, T_A = 25°C		4.0	5.0		4 0	5 0	pF
Source-Gate Capacitance	V_{DG} = 20V, I_D = 0 f = 1 0 MHz, T_A = 25°C		4 0	5 0		4 0	5 0	pF
Input 1 Turn-ON Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		35	60		35	60	ns
Input 2 Turn-ON Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		1 2	1 5		1 2	1 2	μs
Input 1 Turn-OFF Time	V_{IN1} = 10V, T_A = 25°C (See Figure 1)		0 6	0.75		0 6	0.75	μs
Input 2 Turn-OFF Time	V_{IN2} = 10V, T_A = 25°C (See Figure 1)		50	80		50	80	ns
DC Voltage Range	T_A = 25°C (See Figure 2)	±9 0	±10 0		±9.0	±10 0		V
AC Voltage Range	T_A = 25°C (See Figure 2)	±9 0	±10 0		±9 0	±10 0		V

Note 1: Unless otherwise specified these specifications apply for pin 12 connected to +15V, pin 2 connected to -15V, -55°C to 125°C for the AH2114, and 0°C to 85°C for the AH2114C.

Note 2: All typical values are for T_A = 25°C.

Note 3: Derate linearly at 100°C/W above 25°C.

Analog Switches

AH5009 series low cost analog current switches

general description

The AH5009 series is a versatile family of analog switches designed to economically fulfill a wide variety of multiplexing and analog switching applications.

Even numbered switches (AH5010, AH5012, AH5014, etc.,) may be driven directly from standard (5V) TTL; whereas the odd numbered switches (AH5009, AH5011, AH5013, etc.,) are intended for applications utilizing open-collector (15V) structures.

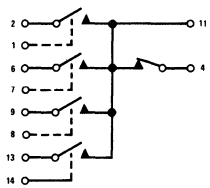
features

- Large analog signal range ±10V peak
- Excellent isolation between channels 80 dB at 1 kHz
- Very low leakage 50 pA
- High switching speed 150 ns
- Low on resistance 100Ω
- Interfaces with standard TTL

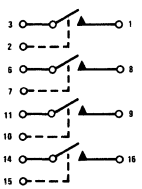
functional and schematic diagrams

(See additional types on page 6.)

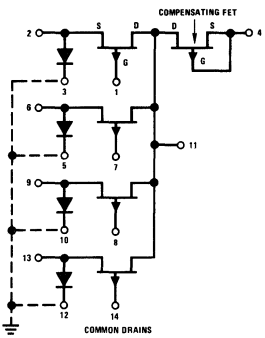
MUX Switches (4 channel version shown)



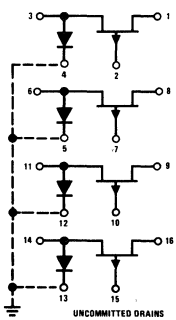
SPST Switches (quad version shown)



MUX Switches (4 channel version shown)

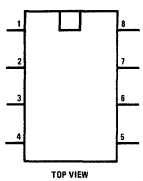


SPST Switches (quad version shown)



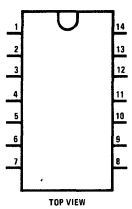
connection diagrams

Dual-In-Line Package



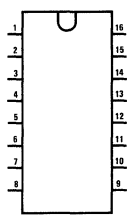
Order Number AH5017CN, AH5018CN, AH5019CN, AH5020CN, AH5021CN, AH5022CN, AH5023CN, or AH5024CN
See Package 20

Dual-In-Line Package



Order Number AH5009CN, AH5010CN, AH5013CN, or AH5014CN
See Package 22

Dual-In-Line Package



Order Number AH5011CN, AH5012CN, AH5015CN, or AH5016CN
See Package 23

8

absolute maximum ratings

Input Voltage (V_{IN})	±30V
Positive Analog Signal Voltage (V_A)	30V
Negative Analog Signal Voltage (V_A)	−15V
Diode Current	10 mA
Drain Current (I_D)	30 mA
Power Dissipation (see graph)	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics (each channel)

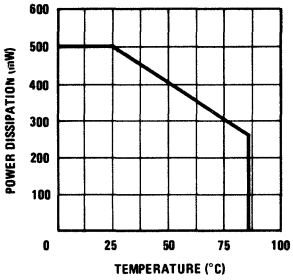
PARAMETER (Note 2)	CIRCUIT TYPE	CONDITIONS (Note 1)	TYP	MAX	UNITS
Input Current "ON" ($I_{IN(ON)}$)	All	V_{IN} = 0V, I_D = 2 mA, T_A = 25°C V_{IN} = 0V, I_D = 2 mA	.01	.1 100	µA µA
Input Current "OFF" ($I_{IN(OFF)}$)	5VTTL	V_{IN} = 4.5V, V_A = ±10V, T_A = 25°C V_{IN} = 4.5V, V_A = ±10V	.04	.2 10	nA nA
Input Current "OFF" ($I_{IN(OFF)}$)	15VTTL	V_{IN} = 11V, V_A = ±10V, T_A = 25°C	.04	.2 10	nA nA
Channel Control Voltage "ON" ($V_{IN(ON)}$)	5VTTL 15VTTL	V_A = ±10V, I_D = 1 mA V_A = ±10V, I_D = 1 mA		.5 1.5	V V
Channel Control Voltage "OFF" ($V_{IN(OFF)}$)	5VTTL 15VTTL	V_A = ±10V V_A = ±10V		4.5 11	V V
Leakage Current "OFF" ($I_{D(OFF)}$)	5VTTL	V_{IN} = 4.5V, V_A = ±10V, T_A = 25°C V_{IN} = 4.5V, V_A = ±10V	.02	.2 10	nA nA
Leakage Current "OFF" ($I_{D(OFF)}$)	15VTTL	V_{IN} = +11V, V_A = ±10V, T_A = 25°C V_{IN} = +11V, V_A = ±10V	.02	.2 10	nA nA
Leakage Current "ON" ($I_{D(ON)}$)	5VTTL	V_{IN} = 0V, I_S = 1mA, T_A = 25°C V_{IN} = 0V, I_S = 1 mA	.3	1 .2	nA µA
Leakage Current "ON" ($I_{D(ON)}$)	15VTTL	V_{IN} = 0V, I_S = 1 mA, T_A = 25°C V_{IN} = 0V, I_S = 1 mA	.1	.5 .1	nA µA
Leakage Current "ON" ($I_{D(ON)}$	5VTTL	V_{IN} = 0V, I_S = 2 mA, T_A = 25°C V_{IN} = 0V, I_S = 2 mA		1 10	µA µA
Leakage Current "ON" ($I_{D(ON)}$)	15VTTL	V_{IN} = 0V, I_S = 2 mA, T_A = 25°C V_{IN} = 0V, I_S = 2 mA		2 1	nA µA
Drain-Source Resistance "ON" ($r_{DS(ON)}$)	5VTTL	V_{IN} = 0.5V, I_D = 2 mA, T_A = 25°C V_{IN} = 0.5V, I_D = 2 mA	90	150 240	Ω Ω
Drain-Source Resistance "ON" ($r_{DS(ON)}$)	15VTTL	V_{IN} = 1.5V, I_D = 2 mA, T_A = 25°C V_{IN} = 1.5V, I_D = 2 mA	60	100 160	Ω Ω
$r_{DS(ON)}$ Match (Effective $r_{DS(ON)}$)($r_{DS(ON)}$ EFF.)	15VTTL MUX 5VTTL MUX	V_{IN} = 1.5V, I_D = 2 mA V_{IN} = 0.5V, I_D = 2 mA		50	Ω
Turn-On Time ($t_{(ON)}$)	All	See AC Test Circuits, T_A = 25°C	150	500	ns
Turn-Off Time ($t_{(OFF)}$)	All	See AC Test Circuits, T_A = 25°C	300	500	ns
Cross Talk (CT)	All	See AC Test Circuits, T_A = 25°C	120		dB

Note 1: Unless otherwise noted, these specifications apply for −25°C to +85°C for AH5009C through AH5012C.

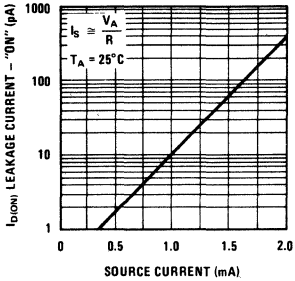
Note 2: "OFF" and "ON" notation refers to the conduction state of the FET switch.

typical performance characteristics

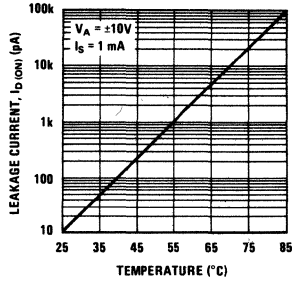
Maximum Power Dissipation



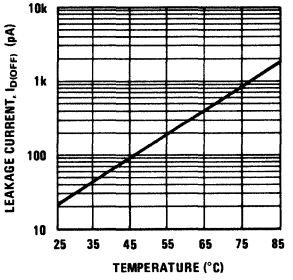
Leakage Current, $I_{D(ON)}$ vs I_S



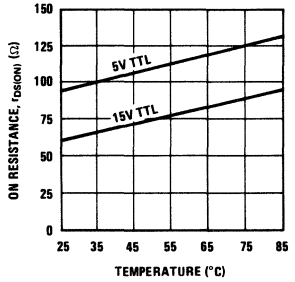
Leakage Current, $I_{D(ON)}$ vs Temperature



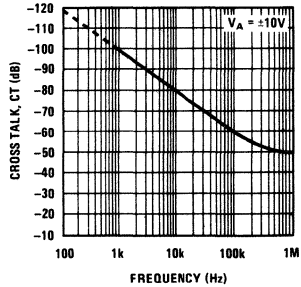
Leakage Current, $I_{D(OFF)}$ vs Temperature



On Resistance, $r_{DS(ON)}$ vs Temperature

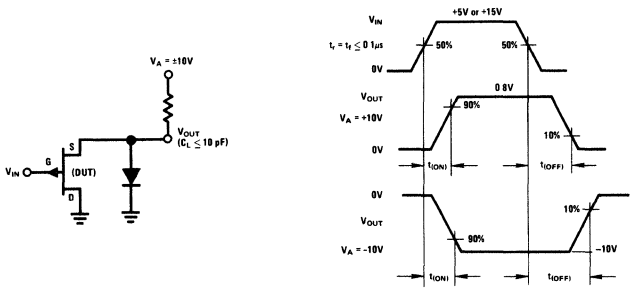


Cross Talk, CT vs Frequency

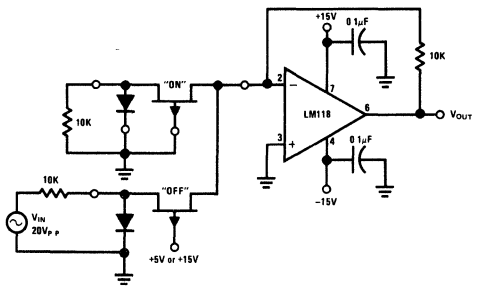


test circuits

AC Switching Test Circuits



Cross Talk Test Circuit



applications information

Theory of Operation

The AH5009 series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred mV eliminates the need for a special gate driver. Thus, the switch may be controlled with conventional TTL elements (5V) or with the open collector (15V) structures.

Two basic switch configurations are available: multiple independent switches (N by SPST) and multiple pole switches used for multiplexing (NPST-MUX). The MUX versions such as the AH5009 offer common drains and include a series FET operated at V_{GS} = 0V. The additional FET is placed in feedback path in order to compensate for the "ON" resistance of the switch FET as shown in Figure 1.

The closed-loop gain of Figure 1 is:

$$A_{VCL} = \frac{R_2 + r_{DS(ON)Q2}}{R_1 + r_{DS(ON)Q1}}$$

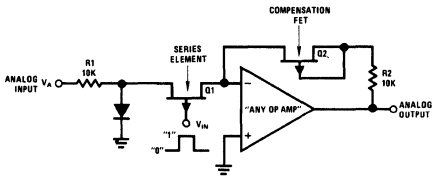


FIGURE 1. Use of Compensation FET

For $R_1 = R_2$, gain accuracy is determined by the $r_{DS(ON)}$ match between Q_1 and Q_2. Standard match between Q_1 and Q_2 is 50Ω resulting in a gain accuracy of 0.5% (for $R_1 = R_2$ = 10k). Tighter $r_{DS(ON)}$ match versions are available.

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = +10V, the source of Q_1 is clamped to about 0.6V by the diode (V_{GS} = 14.4V). The "ON" impedance of the diode is about 26Ω ensuring that AC signals imposed on the +10V will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AH5009 series of analog switches are operated current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the gate to channel (source) diode resulting in leakage across the diode. This leakage, $I_{D(ON)}$, increases exponentially with increasing I_S. As shown in Figure 2, $I_{D(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

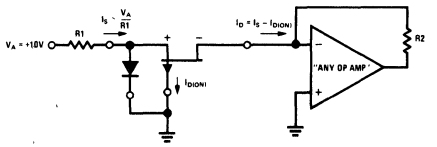


FIGURE 2. On Leakage Current, $I_{D(ON)}$

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R_{1(MIN)} \geq \frac{V_{A(MAX)}\ A_D}{I_{D(ON)}} \qquad (2a)$$

or:

$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \qquad (2b)$$

which ever is worse.

Where: $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{D(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch

≅ 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, $0°C \leq T_A \leq 85°C$. The criterion of equation (2b) predicts:

$$R_{1(MIN)} \geq \frac{10V}{\frac{20MA}{10}} = 5k\Omega$$

For R_1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{D(ON)} \leq 1\mu A$ at 85°C for the AH5010C. Per the criterion of equation (2a):

$$R_{1(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

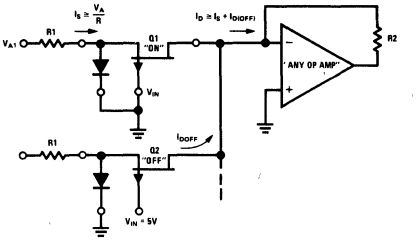


FIGURE 3.

The "OFF" condition of the FET also effects gain accuracy. As shown in Figure 3, the leakage across Q_2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

applications information (con't)

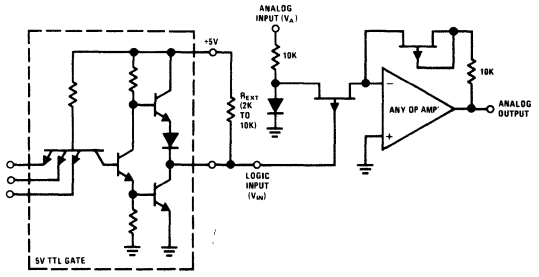


FIGURE 4. Interfacing with +5V Logic

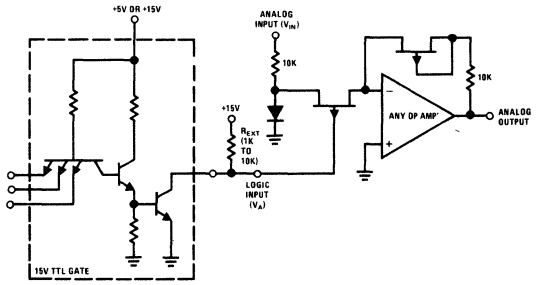


FIGURE 5. Interfacing with +15V Open Collector Logic

Accordingly:

$$R_{1(MAX)} \leq \frac{V_{A(MIN)}\ A_D}{(N)\ I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value for the analog input signal

A_D = Desired accuracy

N = Number of channels

$I_{D(OFF)}$ = OFF leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)} \leq$ 10 nA at 85°C for the AH5009C, $R_{1(MAX)}$ is:

$$R_{1(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R_2, of course, depends on the gain desired and for unity gain $R_1 = R_2$.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp — all of which should be considered in setting the overall gain accuracy of the circuit.

TTL Compatibility

Two input logic drive versions of AH5009 series are available: the even numbered part types are specified to be driven from standard 5V-TTL logic and the odd numbered types from 15V open collector TTL.

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AH5010, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in Figure 4.

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in Figure 5. In both cases, $t_{(OFF)}$ is improved for lower values of R_{EXT} and the expense of power dissipation in the low state.

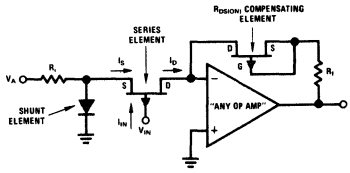


FIGURE 6. Definition of Terms

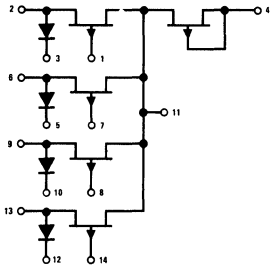
Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in Figure 6.

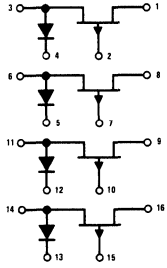
device schematics and pin connections

FOUR CHANNEL

AH5009CN ($R_{DS(ON)} \leq 100\Omega$ 15V - TTL)
AH5010CN ($R_{DS(ON)} \leq 150\Omega$ 5V - TTL)
14 PIN DIP

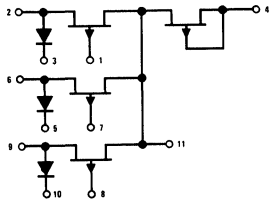


AH5011CN ($R_{DS(ON)} \leq 100\Omega$ 15V - TTL)
AH5012CN ($R_{DS(ON)} \leq 150\Omega$ 5V - TTL)
16 PIN DIP

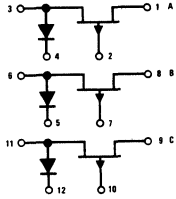


THREE CHANNEL

AH5013CN ($R_{DS(ON)} \leq 100\Omega$ 15V - TTL)
AH5014CN ($R_{DS(ON)} \leq 150\Omega$ 5V - TTL)
14 PIN DIP

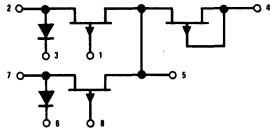


AH5015CN ($R_{DS(ON)} \leq 100\Omega$ 15V - TTL)
AH5016CN ($R_{DS(ON)} \leq 150\Omega$ 5V - TTL)
16 PIN DIP

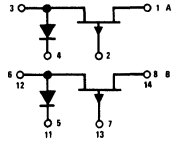


TWO CHANNEL

AH5017CN ($R_{DS(ON)} \leq 100\Omega$ 15V - TTL)
AH5018CN ($R_{DS(ON)} \leq 150\Omega$ 5V - TTL)
8 PIN DIP

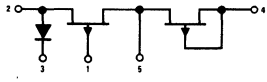


AH5019CN ($R_{DS(ON)} \leq 100\Omega$ 15V - TTL)
AH5020CN ($R_{DS(ON)} \leq 150\Omega$ 5V - TTL)
8 PIN DIP

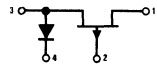


SINGLE CHANNEL

AH5021CN ($R_{DS(ON)} \leq 100\Omega$ 15V - TTL)
AH5022CN ($R_{DS(ON)} \leq 150\Omega$ 5V - TTL)
8 PIN DIP



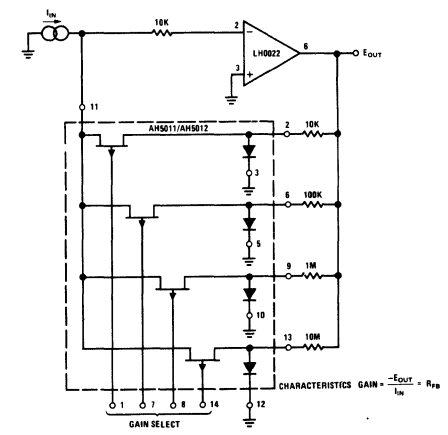
AH5023CN ($R_{DS(ON)} \leq 100\Omega$ 15V - TTL)
AH5024CN ($R_{DS(ON)} \leq 150\Omega$ 5V - TTL)
8 PIN DIP



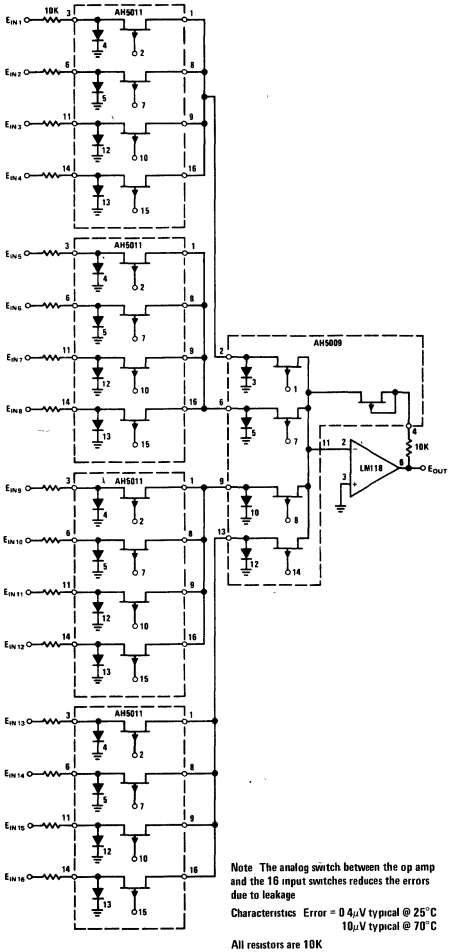
Package Types – 8, 14, 16 pin epoxy "B"

typical applications

Gain Programmable Amplifier



16-Channel Multiplexer

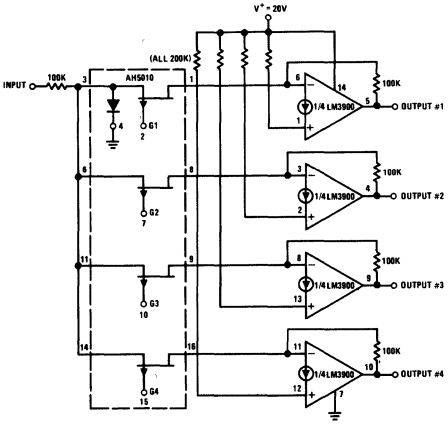


Note The analog switch between the op amp and the 16 input switches reduces the errors due to leakage

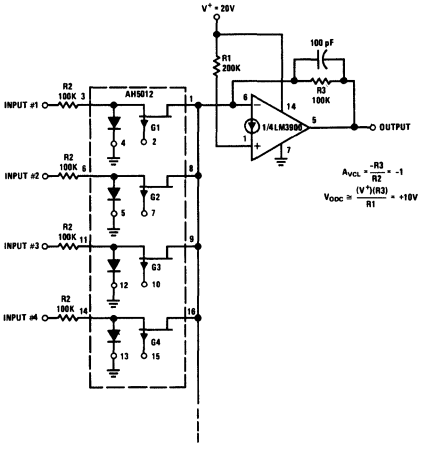
Characteristics Error = 0.4μV typical @ 25°C
10μV typical @ 70°C

All resistors are 10K

Low Cost Demultiplexer



Low Cost Multiplexer/Mixer



Analog Switches

AM1000,AM1001,AM1002 silicon N-channel high speed analog switch

general description

The AM1000 series are junction FET integrated circuit analog switches. These devices commutate faster and with less voltage spiking than any other analog switch presently available. By comparison, discrete JFET switches require elaborate drive circuits to obtain reasonable performance for high toggle rates. Encapsulated in a four pin TO-72 package, these units require a minimum of circuit board area. Switching transients are greatly reduced by a monolithic integrated circuit process. The resulting analog switch device provides the following features:

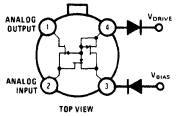
- Low ON Resistance 30Ω
- High Analog Signal Frequency 100 MHz
- High Toggle Rate 4 MHz
- Low Leakage Current 250 pA
- Large Analog Signal Swing ±15V
- Break Before Make Action

The AM1000 series of analog switches are particularly suitable for the following applications:

- High Speed Commutators
- Multiplexers
- Sample and Hold Circuits
- Reset Switching
- Video Switching

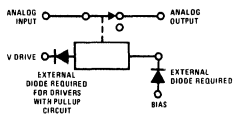
schematic and connection diagram

TO-72 Package



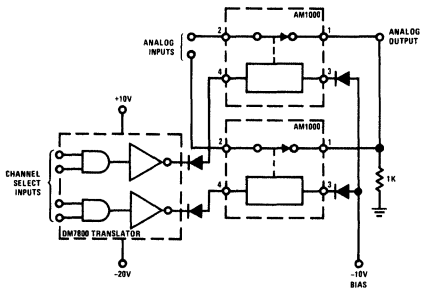
Order Number AM1000H, AM1001H or AM1002H
See Package 9A

equivalent circuit

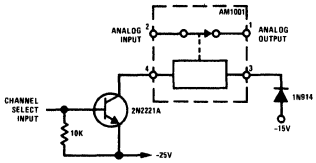


typical applications

±10 Volt Swing Analog Switch 0.5% Accuracy



±15 Volt Swing Analog Switch



absolute maximum ratings

	AM1001	AM1000 AM1002
V_{IN} (Note 1)	+50V	+40V
V_{OUT} (Note 1)	+50V	+40V
V_{DRIVE} (Note 1)	-50V	-40V
V_{BIAS} (Note 1)	+50V	+40V

Power Dissipation @ T_A = 25°C	300 mW
Linear Derating Factor	1.7 mW/°C
Power Dissipation @ T_C = 125°C	150 mW
Linear Derating Factor	6 mW/°C
Maximum Junction Operating Temperature	-55°C to +150°C
Storage Temperature	+200°C
Lead Temperature (Soldering, 10 sec)	+300°C

electrical characteristics

ON CHARACTERISTICS (Note 2)

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
R_{ON}	V_{DRIVE} = +15V, V_{BIAS} = -15V I_{IN} = 1 mA, V_{OUT} = 0V	AM1001	20	40	50	Ω
R_{ON}	V_{DRIVE} = +10V V_{BIAS} = -10V I_{IN} 1 mA, V_{OUT} = 0V	AM1000 AM1002	20 20	25 50	30 100	Ω Ω

OFF CHARACTERISTICS

PARAMETER	CONDITION	AM1000 AM1001			AM1002			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$I_{OUT(OFF)}$	V_{DRIVE} = -20V, V_{BIAS} = -10V V_{IN} = -10V, V_{OUT} +10V							
	T_A = +25°C		05	25		0.5	1	nA
	T_A = +125°C		025	25		0.2	1	μA
$I_{OUT(OFF)}$	V_{DRIVE} = -20V, V_{BIAS} = -10V V_{IN} = +10V, V_{OUT} = -10V							
	T_A = +25 C		05	25		0.5	1	nA
	T_A = +125 C		05	25		0.2	1	μA

DRIVE CHARACTERISTICS (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
I_{DRIVE} (Switch OFF)	V_{DRIVE} = -20V, V_{BIAS} = -10V AM1000, 1001, 1002 V_{IN} = ±10V, V_{OUT} = ±10V		5	10	mA

SWITCHING CHARACTERISTICS

PARAMETER	CONDITION	AM1000 MAX	AM1001 MAX	AM1002 MAX	UNITS
t_{ON}	See Switching Time Test Circuit	100	150	200	ns
t_{OFF}		100	100	100	ns

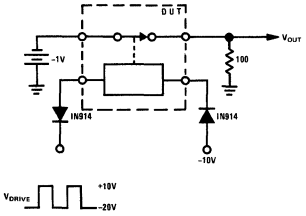
Note 1: The maximum voltage ratings may be applied between any pin or pins simultaneously. Power dissipation may be exceeded in some modes if the voltage pulse exceeds 10 ms. Normal operation will not cause excessive power dissipation even in a dc switching application.

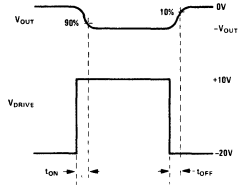
Note 2: All parameters are measured with external silicon diodes. See electrical connection diagram for proper diode placement

Note 3: I_{BIAS} (Switch OFF) is equal to I_{DRIVE} (Switch OFF). $I_{(BIAS)}$ (Switch ON), is equal to external diode leakage.

Note 4: Rise and fall times of V_{DRIVE} shall be 15 ns maximum for switching time testing.

switching time test circuit and waveforms





8

Analog Switches

AM2009/AM2009C/MM4504/MM5504
six channel MOS multiplex switches

general description

The AM2009/AM2009C/MM4504/MM5504 are six channel multiplex switches constructed on a single silicon chip using low threshold P-channel MOS process. The gate of each MOS device is protected by a diode circuit.

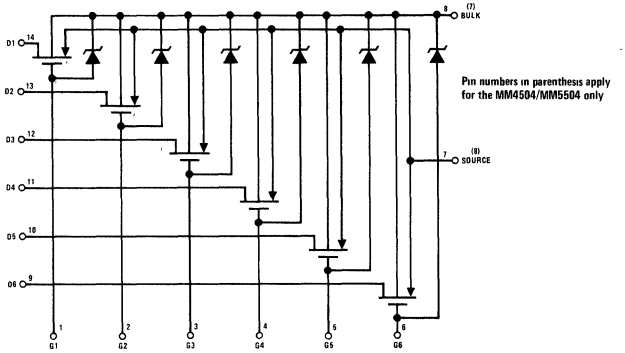
The AM2009/AM2009C/MM4504/MM5504 are designed for applications such as time division multiplexing of analog or digital signals. Switching speeds are primarily determined by conditions external to the device such as signal source impedance, capacitive loading and the total number of channels used in parallel.

The AM2009/MM4504 are specified for operation over the -55°C to +125°C military temperature range. The AM2009C/MM5504 are specified for operation over the -25°C to +85°C temperature range.

features

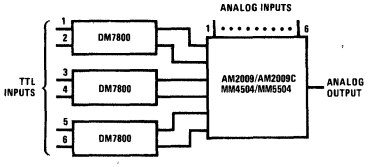
- Typical low "on" resistance 150Ω
- Typical low "off" leakage 100 pA
- Typical large analog voltage range ±10V
- Zero inherent offset voltage
- Normally off with zero gate voltage

schematic diagram

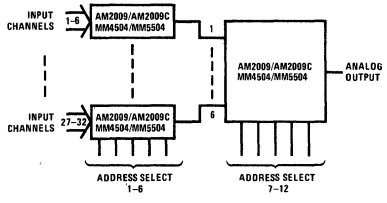


Order Number AM2009F, AM2009CF, MM4504F or MM5504F
See Package 4
Order Number AM2009D, AM2009CD, MM4504D or MM5504D
See Package 1

typical applications



TTL Compatible 6 Channel MUX



32 Channel MUX

absolute maximum ratings (V_{BULK} = 0V)

Voltage on Any Source or Drain	-30V	Total Power Dissipation (at T_A = 25°C)	900 mW
Voltage on Any Gate	-35V	Power Dissipation — each gate circuit	150 mW
Positive Voltage on Any Pin	+0 3V	Operating Temperature Range AM2009	-55°C to +125°C
Source or Drain Current	50 mA	AM2009C	-25°C to +85°C
Gate Current (forward direction of zener clamp)	0 1 mA	Storage Temperature Range	-65°C to +150°C
		Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Threshold Voltage	$V_{GS} = V_{DS}$, $I_{DS} = -1\ \mu A$	-1 0		-3 0	V
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		150	250	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$, $T_A = 25°C$		500	1250	Ω
DC ON Resistance	$V_{GS} = -20V$, $I_{DS} = -100\ \mu A$			325	Ω
DC ON Resistance	$V_{GS} = -10V$, $V_{SB} = -20V$, $I_{DS} = -100\ \mu A$			1500	Ω
Gate Leakage	$V_{GS} = -20V$, Note 2 $V_{GS} = -20V$, Note 2, $T_A = 25°C$		 100	1 0	μA pA
Input Leakage	$V_{DS} = -20V$, Note 2 $V_{DS} = -20V$, Note 2, $T_A = 25°C$		 100	1 0	μA pA
Output Leakage	$V_{SD} = -20V$, Note 2 $V_{SD} = -20V$, Note 2, $T_A = 25°C$		 500	3 0	μA pA
Gate-Bulk Breakdown Voltage	$I_{GB} = -10\ \mu A$, Note 2	-35			V
Source-Drain Breakdown Voltage	$I_{SD} = -10\ \mu A$, $V_{GD} = 0$, Note 2	-30			V
Drain-Source Breakdown Voltage	$I_{DS} = -10\ \mu A$, $V_{GS} = 0$, Note 2	-30			V
Transconductance			4000		mhos
Gate Capacitance	Note 3, f = 1 MHz		4 7	8	pF
Input Capacitance	Note 3, f = 1 MHz		4 6	8	pF
Output Capacitance	Note 3, f = 1 MHz		16	20	pF

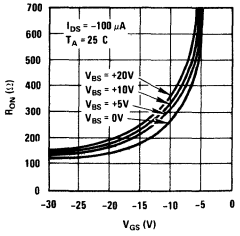
Note 1: Ratings apply over the specified temperature range and V_{BULK} = 0 unless otherwise specified.

Note 2: All other pins grounded.

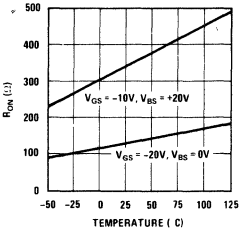
Note 3: Capacitance measured on dual-in-line package between pin under measurement to all other pins. Capacitances are guaranteed by design.

typical performance characteristics

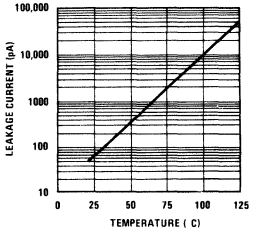
"ON" Resistance vs Gate-to-Source Voltage



"ON" Resistance vs T Temperature



Input Leakage Current vs Temperature



8

Analog Switches

AM3705/AM3705C 8-channel MOS analog multiplexer general description

The AM3705/AM3705C is an eight-channel MOS analog multiplex switch. TTL compatible logic inputs that require no level shifting or input pull-up resistors and operation over a wide range of supply voltages is obtained by constructing the device with low threshold P-channel enhancement MOS technology. To simplify external logic requirements, a one-of-eight decoder and an output enable are included in the device.

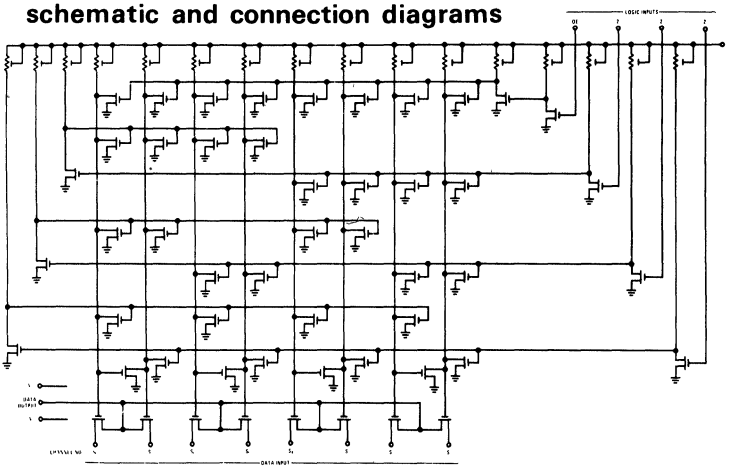
Important design features include:

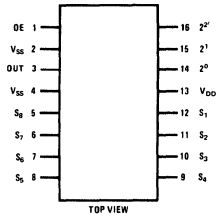
- TTL/DTL compatible input logic levels
- Operation from standard +5V and −15V supplies
- Wide analog voltage range — ±5V
- One-of-eight decoder on chip
- Output enable control
- Low ON resistance — 150Ω
- Input gate protection
- Low leakage currents — 0.5 nA

The AM3705/AM3705C is designed as a low cost analog multiplex switch to fulfill a wide variety of data acquisition and data distribution applications including cross-point switching, MUX front ends for A/D converters, process controllers, automatic test gear, programmable power supplies and other military or industrial instrumentation applications.

The AM3705 is specified for operation over the −55°C to +125°C military temperature range. The AM3705C is specified for operation over the −25°C to +85°C temperature range.

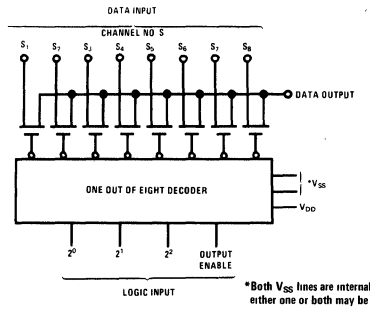
schematic and connection diagrams





Order Number
AM3705D or AM3705CD
See Package 2

block diagram (MIL-STD-806B)



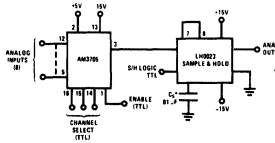
*Both V_{SS} lines are internally connected, either one or both may be used

truth table

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

typical application

Buffered 8-Channel Multiplex, Sample and Hold



*Polystyrene Dielectric
Analog Signal Range — +5V
Acquisition Time — 25 ns
Drift Rate — 0 5 mV/sec
Aperature Time — 250 ns

absolute maximum ratings

Positive Voltage on Any Pin (Note 1)		+0 3V
Negative Voltage on Any Pin (Note 1)		−35V
Source to Drain Current		±30 mA
Logic Input Current		±0 1 mA
Power Dissipation (Note 2)		500 mW
Operating Temperature Range	AM3705	−55°C to +125°C
	AM3705C	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 3)

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
ON Resistance	R_{ON}	$V_{IN} = V_{SS}$, $I_{OUT} = 100\ \mu A$		80	250	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$, $I_{OUT} = -100\ \mu A$		160	400	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$, $I_{OUT} = -100\ \mu A$				
AM3705		$T_A = +125°C$			400	Ω
AM3705C		$T_A = +70°C$			400	Ω
ON Resistance	R_{ON}	$V_{IN} = +5V$, $V_{DD} = -15V$, $I_{OUT} = 100\ \mu A$		100		Ω
ON Resistance	R_{ON}	$V_{IN} = 0V$, $V_{DD} = -15V$, $I_{OUT} = -100\ \mu A$		150		Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$, $V_{DD} = -15V$, $I_{OUT} = -100\ \mu A$		250		Ω
OFF Resistance	R_{OFF}			10^{10}		Ω
Output Leakage Current	I_{LO}	$V_{SS} - V_{OUT} = 15V$		0 5	10	nA
AM3705	I_{LO}	$V_{SS} - V_{OUT} = 15V$, $T_A = 125°C$		150	500	nA
AM3705C	I_{LO}	$V_{SS} - V_{OUT} = 15V$, $T_A = 70°C$		35	500	nA
Data Input Leakage Current	I_{LDI}	$V_{SS} - V_{IN} = 15V$		0 1	3 0	nA
AM3705	I_{LDI}	$V_{SS} - V_{IN} = 15V$, $T_A = 125°C$		25	500	nA
AM3705C	I_{LDI}	$V_{SS} - V_{IN} = 15V$, $T_A = 70°C$		0 5	500	nA
Logic Input Leakage Current	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$		001	1	μA
AM3705	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$, $T_A = 125°C$		.05	10	μA
AM3705C	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$, $T_A = 70°C$		05	10	μA
Logic Input LOW Level	V_{IL}	$V_{SS} = +5\ 0V$		0 5	1.0	V
Logic Input LOW Level	V_{IL}		V_{DD}		$V_{SS} - 4.0$	V
Logic Input HIGH Level	V_{IH}	$V_{SS} = +5\ 0V$	3.0	3.5		V
Logic Input HIGH Level	V_{IH}		$V_{SS} - 2.0$		$V_{SS} + 0\ 3$	V
Channel Switching Time-Positive	t^+	Switching Time Test Circuit		300		ns
Channel Switching Time-Negative	t^-			600		ns
Channel Separation		f = 1 kHz		62		dB
Output Capacitance	C_{db}	$V_{SS} - V_{OUT} = 0$, f = 1 MHz		35		pF
Data Input Capacitance	C_{sb}	$V_{SS} - V_{DIP} = 0$, f = 1 MHz		6.0		pF
Logic Input Capacitance	C_{cg}	$V_{SS} - V_{Logic\ In} = 0$, f = 1 MHz		6 0		pF
Power Dissipation	P_D	$V_{DD} = -31V$, $V_{SS} = 0V$		125	175	mW

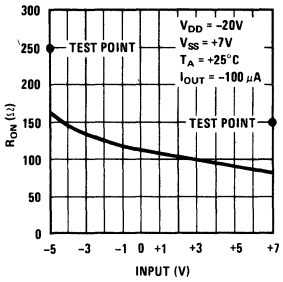
Note 1: All voltages referenced to V_{SS}.

Note 2: Rating applies for ambient temperatures to +25°C, derate linearly at 3 mW/°C for ambient temperatures above +25°C.

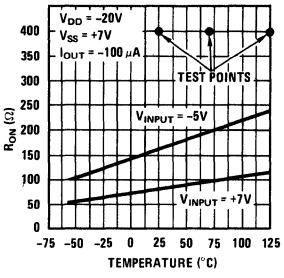
Note 3: Specifications apply for $T_A = 25°C$, $-24V \leq V_{DD} \leq -20V$, and $+5.0V \leq V_{SS} \leq +7.0V$; unless otherwise specified (all voltages are referenced to ground).

typical performance characteristics

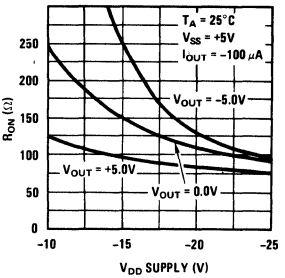
ON Resistance vs Analog Input Voltage



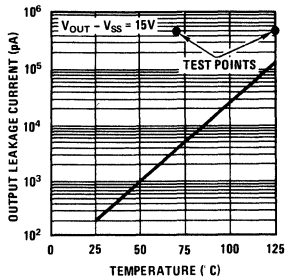
ON Resistance vs Ambient Temperature



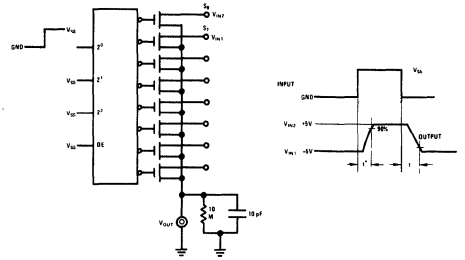
ON Resistance vs V_{DD} Supply Voltage



Output Leakage Current vs Ambient Temperature

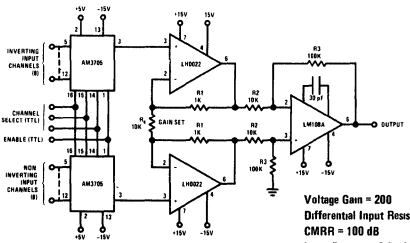


switching time test circuit



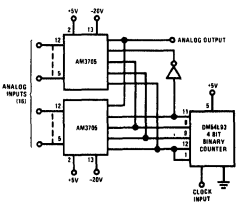
typical applications (con't.)

Differential Input MUX

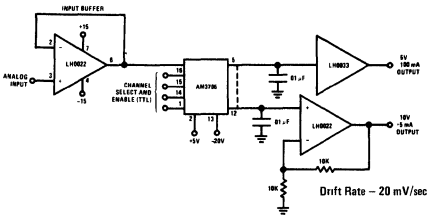


Voltage Gain = 200
Differential Input Resistance = $10^{10}\Omega$
CMRR = 100 dB
Input Current = 0 5 nA

16-Channel Commutator

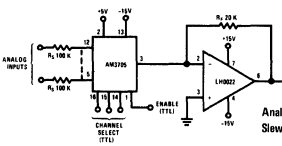


8-Channel Demultiplexer with Sample and Hold



Drift Rate – 20 mV/sec

Wide Input Range Analog Switch



Analog Input Range – 25V
Slew Rate – 5 V/μs

Analog Switches

LF1650/LF2650/LF3650 quad JFET analog switch

general description

The LF1650/LF2650/LF3650 is a monolithic combination of bipolar and JFET technology producing the industry's first one chip quad FET switch. A unique circuit technique is employed to maintain a constant R_{ON} over the analog voltage range. The input is designed to operate from minimum TTL levels, and switch operation also ensures a break before make action.

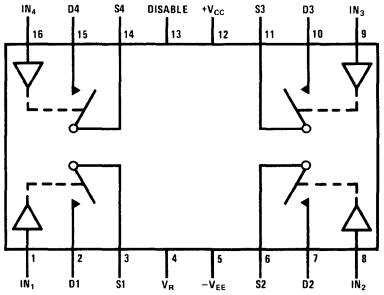
features

- Constant ON resistance for signals ±10V and 100 kHz
- $t_{OFF} < t_{ON}$, break before make action
- Open switch isolation at 1.0 MHz —50 dB
- < 1.0 nA leakage in OFF state
- TTL, DTL, RTL direct drive compatibility
- Single disable pin turns all switches in package OFF

The LF1650/LF2650/LF3650 is designed to operate from ±15V supplies and swing a ±10V analog signal. The FET switches can be used wherever a dc to medium frequency analog signal needs to be controlled.

connection diagram

Dual-In-Line Package
(Logic "0" In).



TOP VIEW

Order Number LF1650D, LF2650D or LF3650D
See Package 2

Order Number LF3650N
See Package 23

typical circuit and schematic diagrams

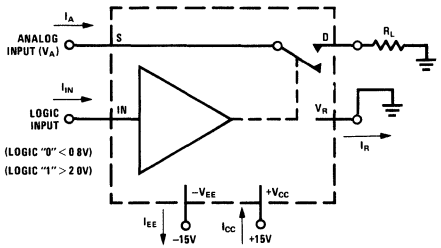


FIGURE 1.

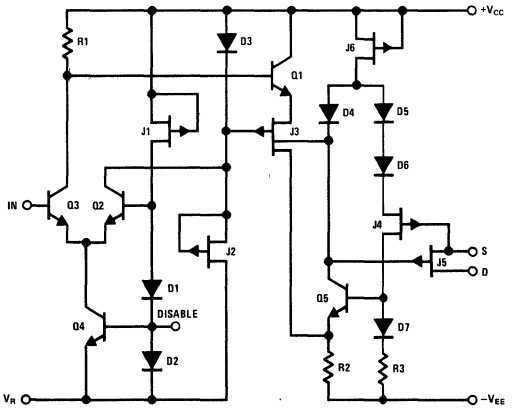


FIGURE 2.

absolute maximum ratings

Positive Supply – Negative Supply	36V
Positive Supply – Reference Supply	36V
Input Voltage	V_{CC} – 2.5V
Reference Voltage	V_{CC} – 5.0V ≥ V_R ≥ – V_{EE}
Input Voltage + Reference Voltage	–4.0V
Input Voltage – Reference Voltage	6.0V
Positive Analog Voltage	V_{CC}
Negative Analog Voltage	V_{EE}
Analog Current	$\|I_A\|$ < 20 mA
Power Dissipation (Note 1)	
Molded DIP (LF3650N)	570 mW
Cavity DIP (LF1650D, LF2650D, LF3650D)	800 mW
Operating Temperature Range	
LF1650	–55°C to +125°C
LF2650	–25°C to +85°C
LF3650	0°C to +70°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics ($+V_{CC}$ = 15V, $-V_{EE}$ = –15V, T_A = 25°C, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ON Resistance (R_{ON})	V_A = 0V, I_D = 1.0 mA		150		Ω
Maximum Analog Swing (V_{AMAX}) (Figure 1)			+11 –12		V V
Analog Current Loss ($I_{S(ON)}$ + $I_{D(ON)}$)	Switch ON, Source and Drain Connect to +10V		0.3		nA
Source Current OFF ($I_{S(OFF)}$)	Switch OFF, Source at +10V, Drain at –10V		0.4		nA
Drain Current OFF ($I_{D(OFF)}$)	Switch OFF, Source at +10V, Drain at –10V		0.1		nA
Logic Input Bias Current (I_{INH})	V_{IN} at +5.0V		3.6		μA
Delay Time ON (t_{ON}) (Figures 3 and 4)	Source at –10V		500		ns
Delay Time OFF (t_{OFF}) (Figures 3 and 4)	Source at +10V		90		ns
Source Capacitance ($C_{S(OFF)}$)	Switch OFF Source at –10V		4.0		pF
Drain Capacitance ($C_{D(OFF)}$)	Switch OFF Drain at –10V		3.0		pF
Active Source and Drain Capacitance ($C_{S(ON)}$ and $C_{D(ON)}$)	Switch ON Source and Drain at 0V		5.0		pF
OFF Isolation	Switch OFF, 1 0 MHz Signal on Source (Figure 5)		–50		dB
Crosstalk	One Switch OFF Another Switch ON with 1.0 Vrms @ 1.0 MHz at Source (Figure 5)		–65		dB
Positive Supply Current (I_{CC})	All Switches OFF		5.0		mA
Negative Supply Current (I_{EE})	All Switches OFF		–3.0		mA
Reference Supply Current (I_R)	All Switches OFF		–2.0		mA
V_{IN} Logic "0"				0.8	V
V_{IN} Logic "1"		2.0			V
Signal Path Slew Rate			50		V/μs

Note 1: For operating at high temperatures the molded DIP products must be derated based on a +125°C maximum junction temperature and a thermal resistance of +175°C/W, devices in the cavity DIP are based on a +150°C maximum junction temperature and are derated at +100°C/W.

est circuits

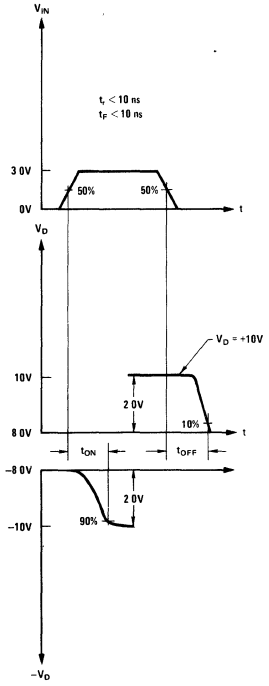


FIGURE 3. t_{ON}, t_{OFF}, Test

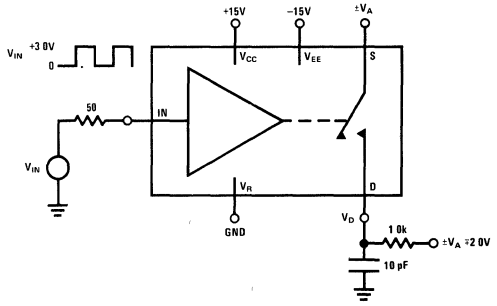


FIGURE 4. t_{ON}, t_{OFF} Test Circuit

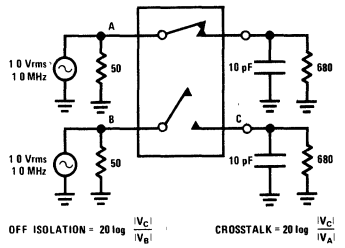
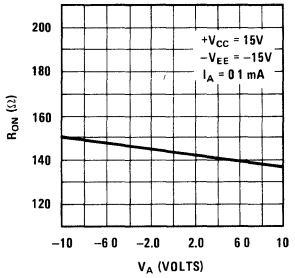


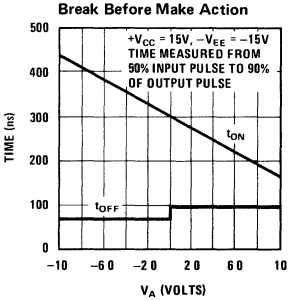
FIGURE 5. OFF Isolation and Crosstalk

ypical performance characteristics

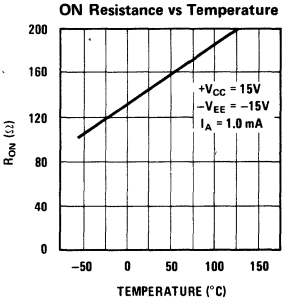
ON Resistance vs Analog Voltage



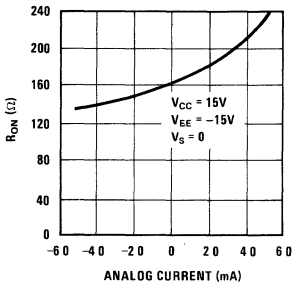
Break Before Make Action



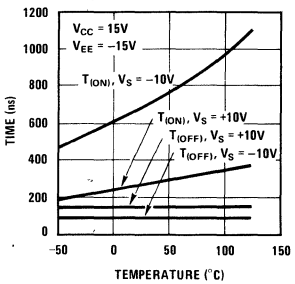
ON Resistance vs Temperature



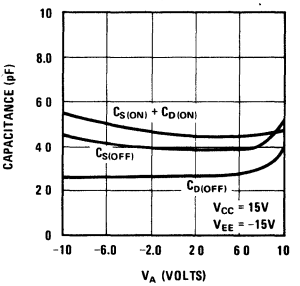
On Resistance vs Analog Current



Switching Times vs Temperature



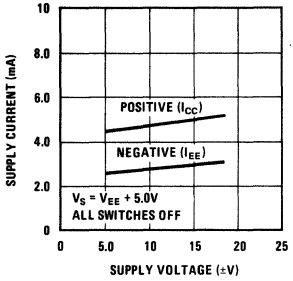
Switch Capacitances vs Analog Voltage



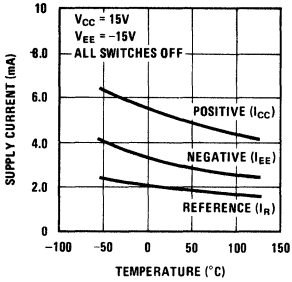
8

typical performance characteristics (con't)

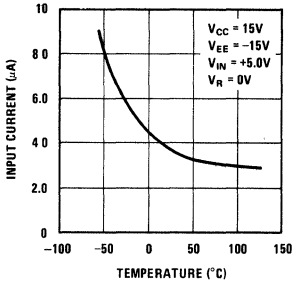
Supply Current vs Supply Voltage



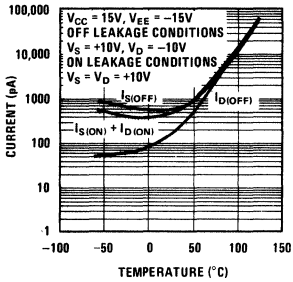
Supply Current vs Temperature



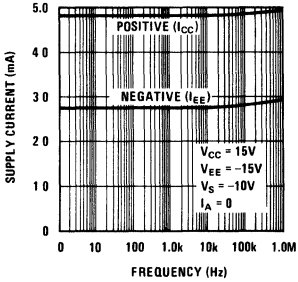
Logic "1" Input Bias Current vs Temperature



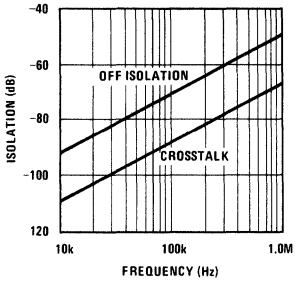
Switch Leakage Currents vs Temperature



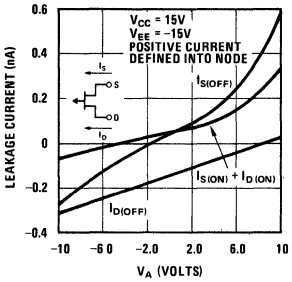
Supply Current vs Toggle Rate



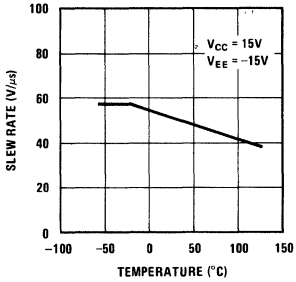
Crosstalk and OFF Isolation vs Frequency Using Test Circuit of Figure 5



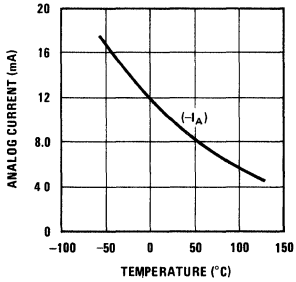
Leakage Currents vs Analog Voltage



Slew Rate of Analog Voltage Above Which Signal Loading Occurs



*See Note



***Note:** The above graph indicates the analog current at which 1% of the analog current is lost.

When the drain of the analog switch is positive with respect to the source the drain gate junction tends to forward bias and the output FET becomes a PNP transistor with base and substrate current losses. Operation in this mode allows much higher analog currents while maintaining a minimum R_{ON}.

Analog Switches

MM450/MM550, MM451/MM551
MM452/MM552, MM455/MM555 MOS analog switches

general description

The MM450, and MM550 series each contain four p channel MOS enhancement mode transistors built on a single monolithic chip. The four transistors are arranged as follows:

MM450, MM550	Dual Differential Switch
MM451, MM551	Four Channel Switch
MM452, MM552	Four MOS Transistor Package
MM455, MM555	Three MOS Transistor Package

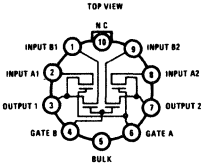
These devices are useful in many airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors (V_{TH} = 2 volts) permits operations with large analog input swings (± 10 volts) at low gate voltages (−20 volts). Significant features, then, include:

- Large Analog Input Swing ±10 Volts
- Low Supply Voltage V_{BULK} = +10 Volts, V_{GG} = −20 Volts
- Low ON Resistance V_{IN} = −10V 150Ω; V_{IN} = +10V 75Ω
- Low Leakage Current 200 pA @ 25°C
- Input Gate Protection
- Zero Offset Voltage

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

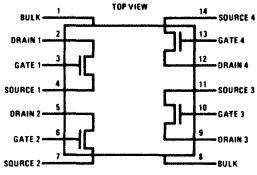
The MM450, MM451, MM452 and MM455 are specified for operation over the −55°C to +125°C military temperature range. The MM550, MM551, MM552 and MM555 are specified for operation over the −25°C to +70°C temperature range.

schematic and connection diagrams



Note Pin 5 connected to case and device bulk. MM450, MM550

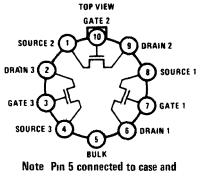
Order Number MM450H or MM550H
See Package 12



Note 1 Pins 1 and 8 connected to case and device bulk Drain and Source may be interchanged MM452F, MM552F
Note 2 MM452D and MM552D (dual-in-line packages) have same pin connections as MM452F and MM552F shown above

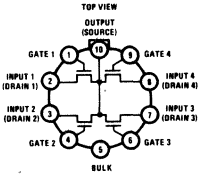
Order Number MM452F or MM552F
See Package 4

Order Number MM452D or MM552D
See Package 1



Note Pin 5 connected to case and device bulk Drain and Source may be interchanged MM455, MM555

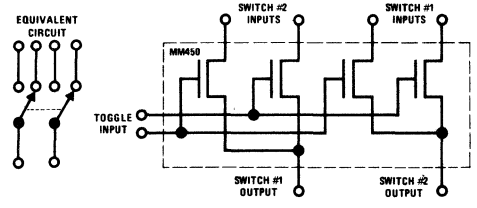
Order Number MM455H or MM555H
See Package 12



Note Pin 5 connected to case and device bulk MM451, MM551

Order Number MM451H or MM551H
See Package 12

typical applications



DPDT Analog Switch

8

absolute maximum ratings

	MM450, MM451, MM452, MM455	MM550, MM551, MM552, MM555
Gate Voltage (V_{GG})	+10V to -30V	+10V to -30V
Bulk Voltage (V_{BULK})	+10V	+10V
Analog Input (V_{IN})	+10V to -20V	+10V to -20V
Power Dissipation	200 mW	200 mW
Operating Temperature	-55°C to +125°C	-25°C to 70°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C

electrical characteristics

STATIC CHARACTERISTICS (Note 1)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage				±10	V
Threshold Voltage ($V_{GS(T)}$)	V_{DG} = 0, I_D = 1 μA	1.0	2.2	3.0	V
ON Resistance	V_{IN} = -10V		150	600	Ω
ON Resistance	V_{IN} = V_{SS}		75	200	Ω
OFF Resistance			10^{10}		Ω
Gate Leakage Current (I_{GSB})	V_{GS} = -25V, V_{BS} = 0, T_A = 25°C		20		pA
Input (Drain) Leakage Current					
MM450, MM451, MM452, MM455	T_A = 25°C		.025	100	nA
	T_A = 85°C		.002	1.0	μA
	T_A = 125°C		.025	1.0	μA
Input (Drain) Leakage Current					
MM550, MM551, MM552, MM555	T_A = 25°C		0.1	100	nA
	T_A = 70°C		.030	1.0	μA
Output (Source) Leakage Current					
MM450, MM451, MM452, MM455	T_A = 25°C		.040	100	nA
Output (Source) Leakage Current					
MM450	T_A = 85°C			1.0	μA
MM451	T_A = 85°C			1.0	μA
MM452, MM455	T_A = 85°C			1.0	μA
MM450, MM451, MM452, MM455	T_A = 125°C			1.0	μA
Output (Source) Leakage Current					
MM550	T_A = 70°C			1.0	μA
MM551	T_A = 70°C			1.0	μA
MM552, MM555	T_A = 70°C			1.0	μA
DYNAMIC CHARACTERISTICS					
Large Signal Transconductance	V_{DS} = -10V, I_D = 10 mA f = 1 kHz		4000		μmhos

CAPACITANCE CHARACTERISTICS (Note 2)

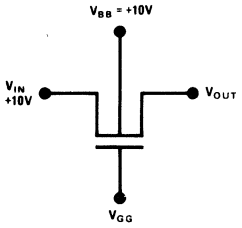
PARAMETER	DEVICE TYPE	MIN	TYP	MAX	UNITS
Analog Input (Drain) Capacitance (C_{DB})	ALL		8	10	pF
Output (Source) Capacitance (C_{SB})	MM450, MM550		11	14	pF
	MM451, MM551		20	24	pF
	MM452, MM552		7.5	11	pF
	MM455, MM555		7.5	11	pF
Gate Input Capacitance (C_{GB})	MM450, MM550		10	13	pF
	MM451, MM551		5.5	8	pF
	MM452, MM552		5.5	9	pF
	MM455, MM555		5.5	9	pF
Gate to Output Capacitance (C_{GS})	ALL		3.0	5	pF

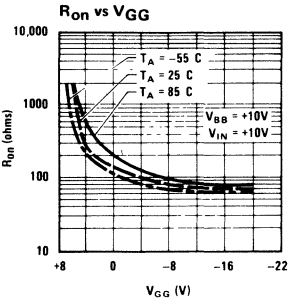
Note 1: The resistance specifications apply for -55°C $\leq T_A \leq$ + 85°C, V_{GG} = -20V, V_{BULK} = +10V, and a test current of 1 mA. Leakage current is measured with all pins held at ground except the pin being measured which is biased at -25V.

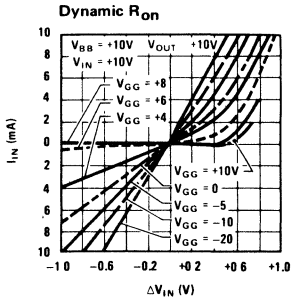
Note 2: All capacitance measurements are made at 0 volts bias at 1 MHz.

typical dynamic input characteristics (T_A = 25°C Unless Otherwise Noted)

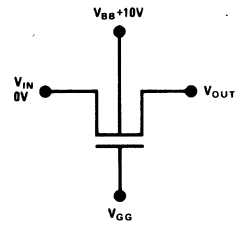
CONDITION 1
ANALOG INPUT VOLTAGE
AT +10 VOLTS

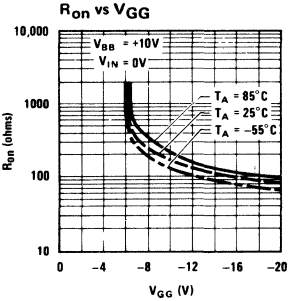


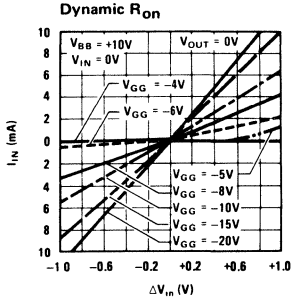




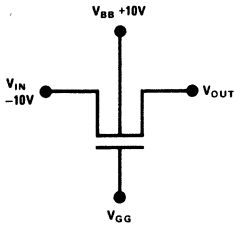
CONDITION 2
ANALOG INPUT VOLTAGE
AT 0 VOLTS

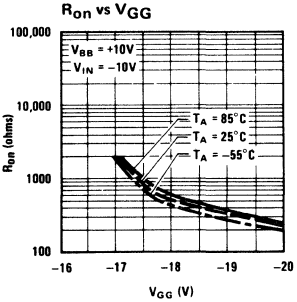


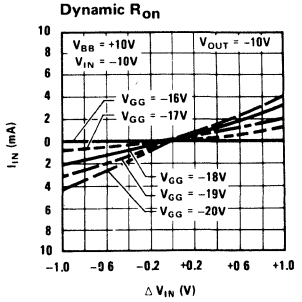


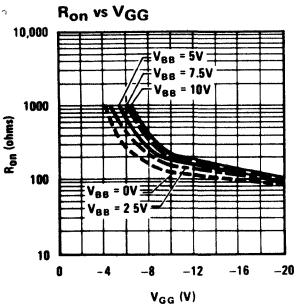


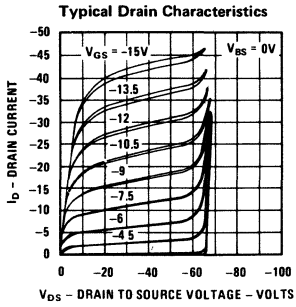
CONDITION 3:
ANALOG INPUT VOLTAGE
AT −10 VOLTS

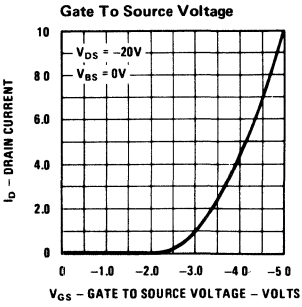








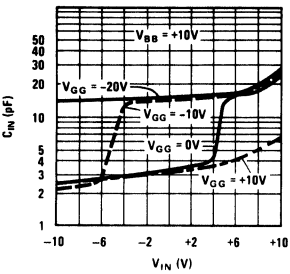




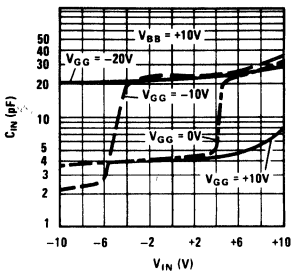
8

typical input capacitance characteristics

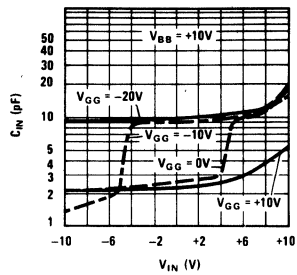
MM450, MM550
C_{IN} vs V_{IN}



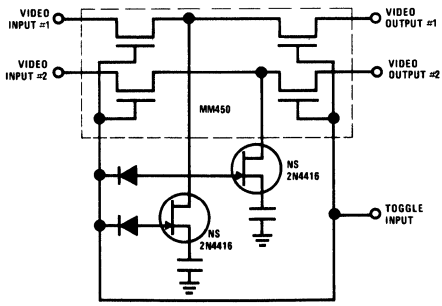
MM451, MM551
C_{IN} vs V_{IN}



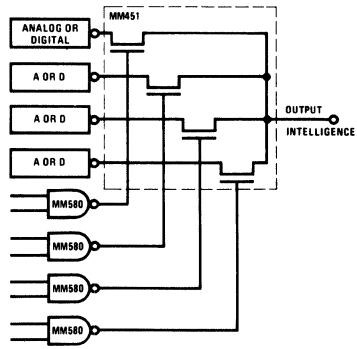
MM452, MM552, MM455, MM555
C_{IN} vs V_{IN}



typical applications (con't)



DPST High-Frequency Switch



4-Channel Multiplexer*

*Expansion in the number of data input lines is possible by using multiple level series switches allowing the same decode gates to be used for all lower rank decoding.

Analog Switches

MM454/MM554 four-channel commutator

general description

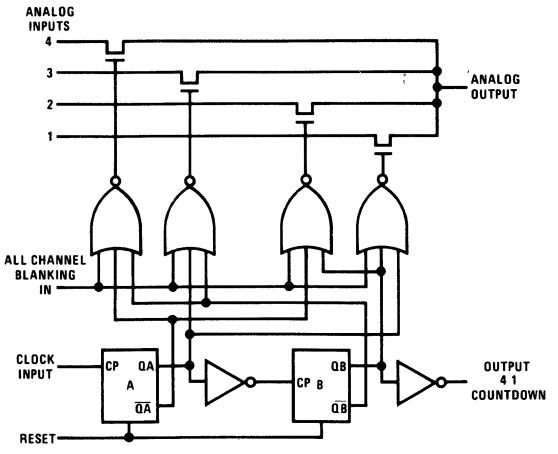
The MM454/MM554 is a four-channel analog commutator capable of switching four analog input channels sequentially onto an output line. The device is constructed on a single silicon chip using MOS P Channel enhancement transistors; it contains all the digital circuitry necessary to sequentially turn ON the four analog switch transistors permitting multiplexing of the analog input data. The device features:

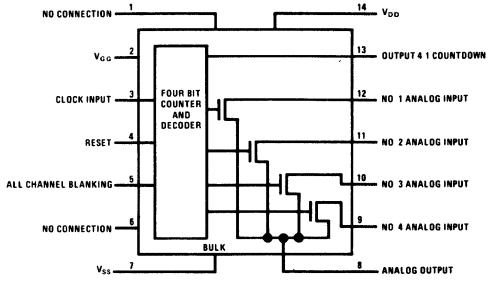
- High Analog Voltage Handling ±10V
- High Commutating Rate 500 kHz
- Low Leakage Current (T_A = 25°C) 200 pA
  (T_A = 85°C) 50 nA
- All Channel Blanking input provided
- Reset capability provided
- Low ON Resistance 200Ω

In addition, the MM454/MM554 can easily be applied where submultiplexing is required since a 4:1 clock countdown signal is provided which can drive the clock input of subsequent MM454/MM554 units.

The MM454 is specified for operation over the −55°C to +125°C military temperature range. The MM554 is specified for operation over the −25°C to +70°C temperature range.

schematic and connection diagrams





Note: Pin 7 connected to case and to device bulk. Nominal Operating Voltages
V_{GG} = −24V, V_{DD} = 0V; V_{SS} = +12V, RESET BIAS = +12V (0V for RESET)
ALL CHANNEL BLANKING BIAS = +12V (0V for BLANKING)

Order Number MM454F or MM554F
See Package 4

absolute maximum ratings (Note 1)

Gate Voltage (V_{GG})	+10V to −30V
Bulk Voltage (V_{SS})	+10V
Analog Input (V_{IN})	+10V to −20V
Power Dissipation	200 mW
Operating Temperature MM454	−55°C to +125°C
MM554	−25°C to +70°C
Storage Temperature	−65°C to +150°C

static characteristics (Note 2)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage					±10	V
ON Resistance		V_{IN} = −10V		170	600	Ω
ON Resistance		V_{IN} = V_{SS}		90	200	Ω
OFF Resistance				10^{10}		Ω
Analog Input Leakage Current	MM454	T_A = 25°C		050	100	nA
	MM454	T_A = 85°C		006	1.0	μA
	MM554	T_A = 25°C		0001	100	nA
	MM554	T_A = 70°C		.030	1.0	μA
Analog Output Leakage Current	MM454	T_A = 25°C		0 100	100	nA
	MM454	T_A = 85°C		30	1.0	μA
	MM554	T_A = 25°C		0001	100	nA
	MM554	T_A = 70°C		.030	1.0	μA
V_{SS} Supply Current Drain		V_{SS} = +12V		3.8	5.5	mA
V_{GG} Supply Current Drain		V_{GG} = −24V		2.4	3.5	mA

capacitance characteristics

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Analog Input Capacitance Channel OFF	I_{IN} = 0		4	6	pF
Analog Input Capacitance Channel ON	I_{IN} = 0		20	24	pF
Analog Output Capacitance	I_{IN} = 0		20	24	pF
Clock Input	V_{CL} = +12V		2.0		pF
Reset Input	V_{RESET} = +12V		2 0		pF
Blanking Input	V_{BLANK} = +12V		2 0		pF

clock characteristics (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Clock Input (HIGH)[4]		V_{SS} − 2		V_{SS}	V
Clock Input (LOW)		−5	0	+5	V
Clock Input Rise Time (POS GOING)			No requirement		
Clock Input Fall Time (NEG GOING)				20	μsec
Countdown Output (POS) V_{OH}		V_{SS} −2		V_{SS}	V
Countdown Output (NEG) V_{OL}			0		V
Maximum Commutation Rate		0 5	2.0		MHz
V_{SS}		+10 0	+12	+14	V

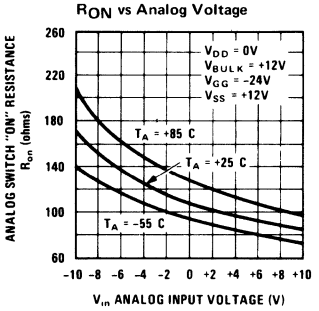
Note 1: Maximum ratings are limiting values above which the device may be damaged. All voltages referenced to V_{DD} = 0.

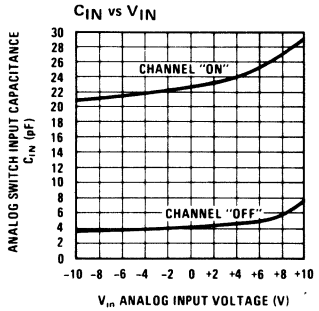
Note 2: These specifications apply over the indicated operating temperature range for V_{GG} = −24V, V_{DD} = 0V, V_{SS} = +12V, V_{RESET} = +12V, V_{BLANK} = +12V ON resistance measured at 1 mA, OFF resistance and leakage measured with all analog inputs and output common. Capacitance measured at 1 MHz.

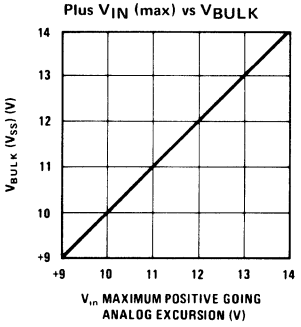
Note 3: Operating conditions in Note 2 apply. V_{SS} to V_{DD} (0V) voltage is applied to counting and gating circuits. V_{GG} is required only for analog switch biasing. All logic inputs are high resistance and are essentially capacitive.

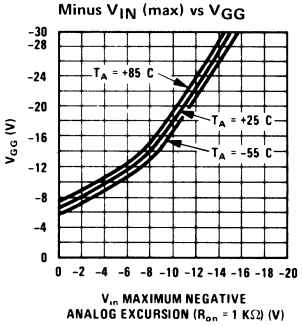
Note 4: Logic input voltage must not be more positive than V_{SS}.

typical performance characteristics

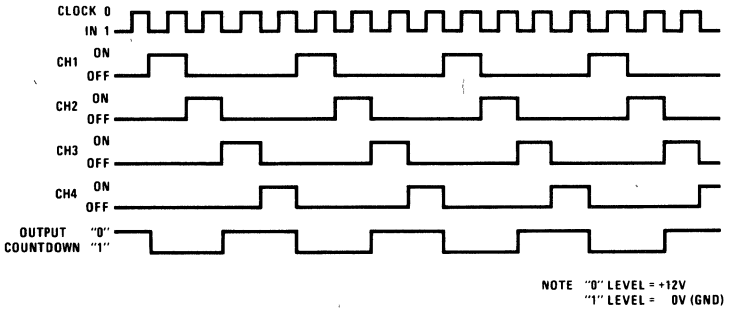








timing diagram



NOTE "0" LEVEL = +12V
"1" LEVEL = 0V (GND)

8

New Products

DM7833/DM8833, DM7834/DM8834, DM7835/DM8835, DM7839/DM8839 quad TRI-STATE® transceivers

general description

This family of TRI-STATE® party line transceivers offer extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DM7833/DM8833 and DM7835/DM8835 employ TRI-STATE outputs on the receiver also, while on the DM7834/DM8834 and DM7839/DM8839 the receiver outputs are standard active pull up T^2L.

The DM7833/DM8833 are non-inverting quad transceivers with a common driver disable control and a common receiver disable control.

The DM7839/DM8839 are non-inverting quad transceivers with a common two-input driver disable control.

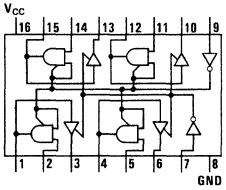
The DM7834/DM8834 are inverting quad transceivers with a common two input driver disable control.

The DM7835/DM8835 are inverting quad transceivers with a common driver disable control and a common receiver disable control.

features

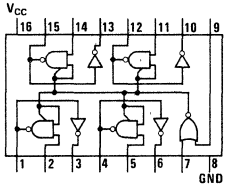
- Receiver hysteresis 450 mV (typ)
- Receiver noise immunity 1.4V (typ)
- Receiver input current for normal V_{CC} or V_{CC} = 0V 50 μA (max)
- Receivers
  - Sink 16 mA at 0.4V (max)
  - Source 2.0 mA (mil), 5.2 mA (com) at 2.4V (min)
- Drivers
  - Sink 50 mA at 0.5V (max) or 32 mA at 0.4V (max)
  - Source 10.4 mA at 2.4V (min)
- Drivers have TRI-STATE outputs
- DM7833/DM8833 and DM7835/DM8835 receivers have TRI-STATE outputs
- Capable of driving 100Ω DC terminated buses
- 74 series TTL compatible

connection diagrams



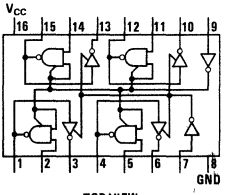
TOP VIEW

DM7833/DM8833



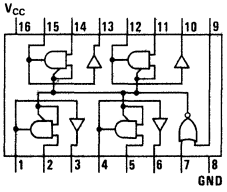
TOP VIEW

DM7834/DM8834



TOP VIEW

DM7835/DM8835



TOP VIEW

DM7839/DM8839

New Products

LM165/LM365, LM166/LM366, LM167/LM367, LM168/LM368 MOS sense amplifiers (MOS to TTL converters)

general description

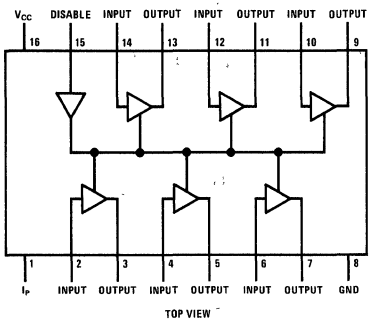
This is a new series of hex sense amplifiers. The LM165/LM365 and LM166/LM366 have TRI-STATE outputs. The LM167/LM367 and LM168/LM363 have both TRI-STATE inputs and outputs. High impedance states are controlled by an enable input.

The current threshold at which the outputs change state is determined by the current at the programming pin. The current threshold is 100μA with the programming pin grounded and 350μA with the pin unconnected. It can be set from 100μA to 350μA by connecting a resistor from the pin to ground, and set above 350μA by connecting a resistor from the pin to the positive supply.

The outputs are high current drivers capable of sinking 50 mA in the low state and sourcing 5.0 mA in the high state. The circuits feature high speed direct MOS sense capability with high impedance states to allow use of a common bus line.

connection diagram

Dual-In-Line Package



TOP VIEW

truth tables

LM165/LM365

I_{IN}	D_{IS}	OUT
X	H	Hi-z
$>I_t$	L	H
$<I_t$	L	L

LM166/LM366

I_{IN}	D_{IS}	OUT
X	H	Hi-z
$>I_t$	L	L
$<I_t$	L	H

LM167/LM367

I_{IN}	D_{IS}	OUT
X	H	Hi-z
$>I_t$	L	L
$<I_t$	L	H

LM168/LM368

I_{IN}	D_{IS}	OUT
X	H	Hi-z
$>I_t$	L	H
$<I_t$	L	L

ıbsolute maximum ratings (Note 1)

upply Voltage	7.0V
ıput Voltage	5.5V
utput Voltage	5.5V
torage Temperature Range	−65°C to +150°C
ead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
LM165,LM166,LM167,LM168	4.5	5.5	V
LM365,LM366,LM367,LM368	4.75	5.25	V
Temperature (T_A)			
LM165,LM166,LM167,LM168	−55	+125	°C
LM365,LM366,LM367,LM368	0	+70	°C

ılectrical characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage (V_{IH})	V_{CC} = Min	2.0			V
Logical "1" Input Current Disable (I_{IH})	V_{CC} = Max, V_{IN} = 2.4V			40	μA
Input Threshold (I_t)	I_P = 0.0μA		400		μA
Logical "0" Input Voltage (V_{IL})	V_{CC} = Min			0.8	V
Logical "0" Input Current (I_{IL})	V_{CC} = Max, V_{IN} = 0.4V			−1.6	mA
Input Clamp Voltage (V_{CO})	V_{CC} = Min, I_{OUT} = −12 mA		1.0		V
Logical "1" Output Voltage (V_{OH})	V_{CC} = Min, I_{OUT} = −5.0 mA	2.4			V
Output Short Circuit Current (I_{OS}) (Note 4)	V_{CC} = Max, V_{OUT} = 0.0V	−20		−100	mA
Logical "0" Output Voltage (V_{OL})	V_{CC} = Min, I_{OUT} = 50 mA		0.3		V
Supply Current (I_{CC})					
LM165/LM365, LM166/LM366	V_{CC} = Max		70		mA
LM167/LM367, LM168/LM368	V_{CC} = Max		80		mA
Input and Output Disable Current (I_{DIS})	V_{CC} = Max, 0.4V ≤ V ≤ 2.4V		±5.0		μA

ıwitching characteristics T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, Low to High Level (t_{pdLH})	C_L = 50 pF, R_L = 80Ω				
LM165/LM365, LM168/LM368			12		ns
LM166/LM366, LM167/LM367			15		ns
Propagation Delay Time, High to Low Level (t_{pdHL})	C_L = 50 pF, R_L = 80Ω				
LM165/LM365			10		ns
LM166/LM366, LM167/LM367			15		ns
LM168/LM368			12		ns

ote 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating emperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" rovides conditions for actual device operation.

ote 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the LM165, LM166, LM167, LM168 ıd across the 0°C to +70°C range for the LM365, LM366, LM367, LM368. All typicals are given for V_{CC} = 7.0V and T_A = 25°C.

ote 3: All currents into device pins shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted. All ılues shown as max or min on absolute value basis.

ote 4: Only one output at a time should be shorted.

New Products

LM3625 dual high speed MOS sense amp

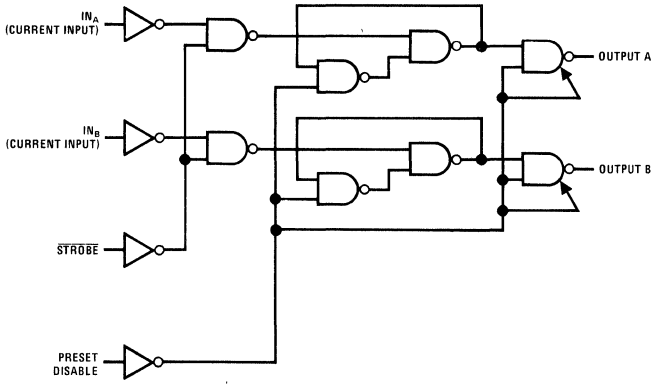
general description

The LM3625 is a dual high speed MOS to TTL level converter. It acts as an interface level converter between MOS and TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE® output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

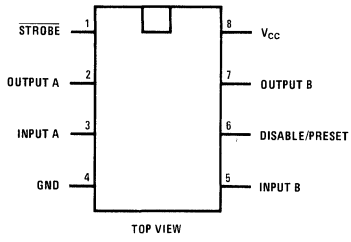
features

- Easily interfaces with most popular 1k and 2k dynamic MOS RAMs
- Pin-for-pin replacement for the 8T25
- Very low output impedance – high drive ability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter

logic and connection diagrams



Dual-In-Line Package



Order Number LM3625N
See Package 20

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Current (I_{INA}, I_{INB})	V_{CC} = Min	400			μA
Logical "0" Input Current (I_{INA}, I_{INB})	V_{CC} = Min			200	μA
Logical "1" Input Voltage, Strobe, Preset/Disable	V_{CC} = Min	2 0			V
Logical "0" Input Voltage; Strobe, Preset/Disable	V_{CC} = Min			0 8	V
Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −1 5 mA	2 8			V
Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA			0 4	V
Third State Output Current	V_{CC} = Max, V_O = 3 9V V_{CC} = Max, V_O = 0 0V			100 −100	μA μA
Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2 4V V_{CC} = Max, V_{IN} = 5 5V			40 1 0	μA mA
Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0 4V			−1 6	mA
Supply Current	V_{CC} = Max, $V_{IN(PRE/DIS)}$ = 2 0V Other Inputs = 0V			40	mA
Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			1 5	V
Output Short Circuit Current (Note 3)	V_{CC} = Max, V_O = 0V	−20		−70	mA
Propagation Delay to a Logical "0" from STROBE to Output (t_{ds})	V_{CC} = 5 0V, T_A = 25°C		17	25	ns
Delay from Disable Input to High Impedance State (from Logical "1" Level)(t_{1H})	V_{CC} = 5 0V, T_A = 25°C		7.0	11	ns
Delay from Disable Input to High Impedance State (from Logical "0" Level)(t_{0H})	V_{CC} = 5 0V, T_A = 25°C		17	25	ns
Delay from Disable Input to Logical "1" Level (from High Impedance State)(t_{H1})	V_{CC} = 5 0V, T_A = 25°C		9 0	14	ns
Delay from Disable Input to Logical "0" Level (from High Impedance State)(t_{H0})	V_{CC} = 5 0V, T_A = 25°C		13.5	16	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC} = 5.0V, T_A = 25°C.

Note 3: Only one output at a time should be shorted.

New Products

LM75150 dual line driver

general description

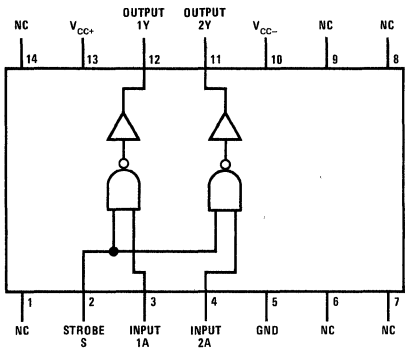
The LM75150 is a monolithic dual line driver designed to interface with data communication equipment. The device satisfies the specifications of EIA standard RS232C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12V and −12V power supplies. The LM75150 is characterized for operation from 0°C to +70°C.

features

- Withstands sustained output short-circuit to any low-impedance voltage between −25V and +25V
- 2.0 μs max transition time through the +3.0V to −3.0V transition region under full 2500 pF load
- Inputs are DTL/TTL compatible
- Common strobe input
- Inverting output
- Slew rate control with external capacitor

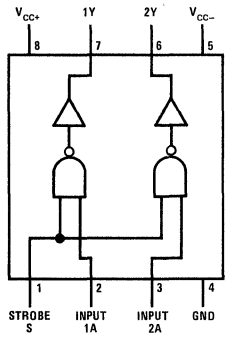
connection diagrams

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

New Products

LM75154 quad line receiver

general description

The LM75154 is a quad line receiver designed to interface with data communications equipment. This device satisfies the specifications of EIA standard RS232C. The LM75154 can also be used for short, single-line, point-to-point transmission and for level translators.

In normal operation, the threshold-control terminals are connected to pin 15, the V_{CC1} terminal. This provides a wider hysteresis loop. When the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

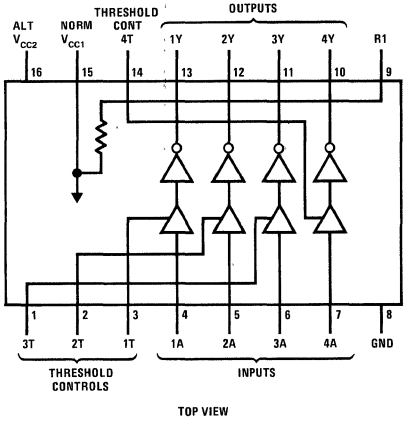
For fail-safe operation, the threshold-control terminals are open. This narrows the hysteresis loop by causing the negative-going threshold voltage to be above zero. When the input voltage goes to zero, the output will go to the high level independent of the previous input condition. This guarantees that the output will be in the high level if the input voltage goes to zero or an open-circuit.

features

- Input resistance . . . 3.0 kΩ to 7.0 kΩ over full RS232C voltage range
- Input threshold adjustable to meet "Fail-Safe" requirements without using external components
- Built-in hysteresis for increase noise immunity
- Inverting output compatible with DTL or TTL
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage 5.0V
- Can also operate with 12V supply

connection diagram

Dual-In-Line Package



TOP VIEW

New Products

MH7807/MH8807 oscillator/clock drivers

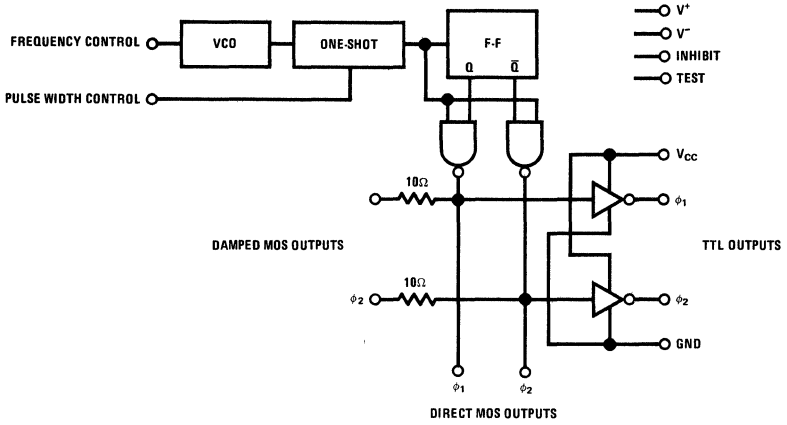
general description

The MH7807/MH8807 is a complete self-contained two-phase oscillators and clock driver subsystems for MOS micro-computer, calculator and shift register systems.

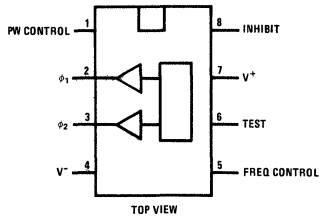
features

- No external timing components
- Two non-overlapping outputs
- Both frequency and pulse width are voltage controlled
- Frequency adjustable from 400 kHz to 2 MHz
- Pulse width adjustable from 300 ns to 2μs
- Low power for battery operation
- TTL outputs for verification and synchronization
- Both direct and damped MOS outputs

logic diagram



connection diagram



New Products

MH8804 quad MOS memory driver
MH8805 dual MOS memory driver

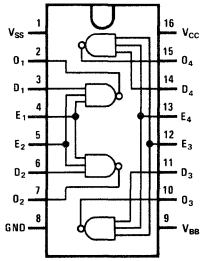
general description

The quad MH8804 and the dual MH8805 are bipolar to MOS drivers specifically designed to drive input address lines for MOS memory arrays using MM1103 type RAMs. The MH8804 is pin compatible with the 13207 and the MH8805 with the SN75361.

features

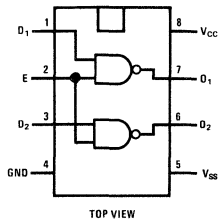
- Current mode output drive ±500 mA
- Rise and fall times 20 ns
- Delay times 15 ns
- High output voltage $V_{SS} - 1.0V$
- Low output voltage 0.3V
- Input levels TTL/DTL

connection diagrams



TOP VIEW

MH8804



TOP VIEW

MH8805

INTEGRATED CIRCUITS FOR DIGITAL DATA TRANSMISSION

INTRODUCTION

It is frequently necessary to transmit digital data in a high-noise environment where ordinary integrated logic circuits cannot be used because they do not have sufficient noise immunity. One solution to this problem, of course, is to use high-noise-immunity logic. In many cases, this approach would require worst case logic swings of 30V, requiring high power-supply voltages. Further, considerable power would be needed to transmit these voltage levels at high speed. This is especially true if the lines must be terminated to eliminate reflections, since practical transmission lines have a low characteristic impedance.

A much better solution is to convert the ground referred digital data at the transmission end into a differential signal and transmit this down a balanced, twisted-pair line. At the receiving end, any induced noise, or voltage due to ground-loop currents, appears equally on both ends of the twisted-pair line. Hence, a receiver which responds only to the differential signal from the line will reject the undesired signals even with moderate voltage swings from the transmitter.

Figure 1 illustrates this situation more clearly. When ground is used as a signal return as in Figure 1a, the voltage seen at the receiving end will be the output voltage of the transmitter plus any noise voltage induced in the signal line. Hence, the noise immunity of the transmitter-receiver combination must be equal to the maximum expected noise from both sources.

The differential transmission scheme diagrammed in Figure 1b solves this problem. Any ground noise or voltage induced on the transmission lines will appear equally on both inputs of the receiver. The receiver responds only to the differential signal coming out of the twisted-pair line and delivers a single-ended output signal referred to the ground

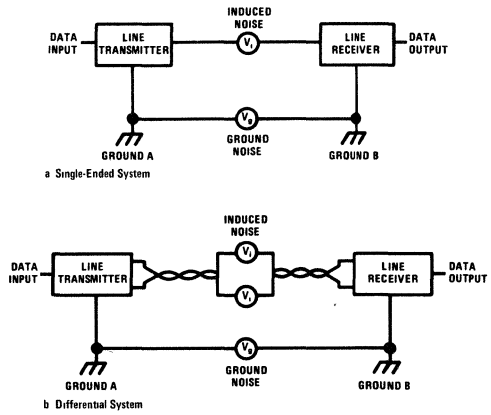


FIGURE 1. Comparing Differential and Single-Ended Data Transmission

at the receiving end. Therefore, extremely high noise immunities are not needed; and the transmitter and receiver can be operated from the same supplies as standard integrated logic circuits.

This article describes the operation and use of a line driver and line receiver for transmission systems using twisted-pair lines. The transmitter provides a buffered differential output from a DTL or TTL input signal. A four-input gate is included on the input so that the circuit can also perform logic. The receiver detects a zero crossing in the differential input voltage and can directly drive DTL or TTL integrated circuits at the receiving end. It also has strobe capability to blank out unwanted input signals. Both the transmitter and the receiver incorporate two independent units on a single silicon chip.

LINE DRIVER

Figure 2 shows a schematic diagram of the line transmitter. The circuit has a marked resemblance to a standard TTL buffer. In fact, it is possible to use a standard dual buffer as a transmitter. However, the DM7830 incorporates additional features. For one, the output is current limited to protect the driver from accidental shorts in the transmission lines. Secondly, diodes on the output clamp severe voltage transients that may be induced into the transmission lines. Finally, the circuit has internal inversion to produce a differential output signal, reducing the skew between the outputs and making the output state independent of loading.

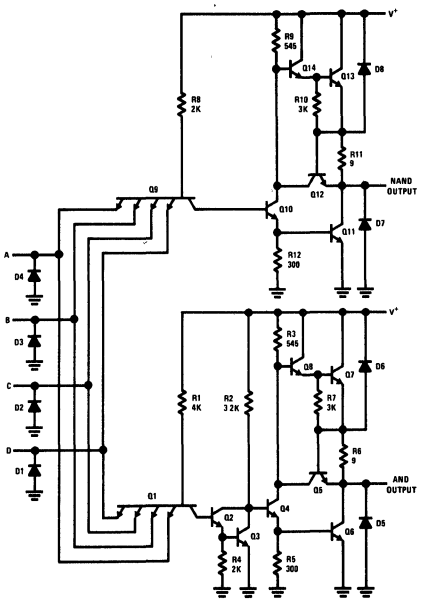


FIGURE 2. Schematic Diagram of the DM7830 Line Driver

As can be seen from the upper half of Figure 2, a quadruple-emitter input transistor, Q9, provides four logic inputs to the transmitter. This transistor drives the inverter stage formed by Q10 and Q11 to give a NAND output. A low state logic input on any of the emitters of Q9 will cause the base drive to be removed from Q10, since Q9 will be saturated by current from R8, holding the base of Q10 near ground. Hence, Q10 and Q11 will be turned off; and the output will be in a high state. When all the emitters of Q9 are at a one logic level, Q10 receives base drive from R8 through the forward biased collector-base junction of Q9. This saturates Q10 and also Q11, giving a low output state. The input voltage at which the transition occurs is equal to the sum of the emitter-base turn on voltages of Q10 and Q11 minus the saturation voltage of Q9. This is about 1.4V at 25°C.

A standard "totem-pole" arrangement is used on the output stage. When the output is switched to the high state, with Q10 and Q11 cut off, current is supplied to the load by Q13 and Q14 which are connected in a modified Darlington configuration. Because of the high compound current gain of these transistors, the output resistance is quite low and a large load current can be supplied. R10 is included across the emitter-base junction of Q13 both to drain off any collector-base leakage current in Q13 and to discharge the collector-base capacitance of Q13 when the output is switched to the low state. In the high state, the output level is approximately two diode drops below the positive supply, or roughly 3.6V at 25°C with a 5.0V supply.

With the output switched into the low state, Q10 saturates, holding the base of Q14 about one diode drop above ground. This cuts off Q13. Further, both the base current and the collector current of Q10 are driven into the base of Q11 saturating it and giving a low-state output of about 0.1V. The circuit is designed so that the base of Q11 is supplied 6 mA, so the collector can drive considerable load current before it is pulled out of saturation.

The primary purpose of R12 is to provide current to remove the stored charge in Q11 and charge its collector-base capacitance when the circuit is switched to the high state. Its value is also made enough less than R9 to prevent supply current transients which might otherwise occur* when the power supply is coming up to voltage.

*J. Kalb, "Design Considerations for a TTL Gate," *"National Semiconductor* TP-6, May, 1968.

The lower half of the transmitter in Figure 2 is identical to the upper, except that an inverter stage has been added. This is needed so that an input signal which drives the output of the upper half positive will drive the lower half negative, and vice versa, producing a differential output signal. Transistors Q2 and Q3 produce the inversion. Even though the current gain is not necessarily needed, the modified Darlington connection is used to produce the proper logic transition voltage on the input of the transmitter. Because of the low load capacitance that the inverter sees when it is completely within the integrated circuit, it is extremely fast, with a typical delay of 3 ns. This minimizes the skew between the outputs.

One of the schemes used when dual buffers are employed as a differential line driver is to obtain the NAND output in the normal fashion and provide the AND output by connecting the input of the second buffer to the NAND output. Using an internal inverter has some distinct advantages over this: for one, capacitive loads which slow down the response of the NAND output will not introduce a time skew between the two outputs; secondly, line transients on the NAND output will not cause an unwanted change of state on the AND output.

Clamp diodes, D1 through D4, are added on all inputs to clamp undershoot. This undershoot and ringing can occur in TTL systems because the rise and fall times are extremely short.

Output-current limiting is provided by adding a resistor and transistor to each of the complementary outputs. Referring again to Figure 2, when the current on the NAND output increases to a value where the voltage drop across R11 is sufficient to turn on Q12, the short circuit protection comes into effect. This happens because further increases in output current flow into the base of Q12 causing it to remove base drive from Q14 and, therefore, Q13. Any substantial increase in output current will then cause the output voltage to collapse to zero. Since the magnitude of the short circuit depends on the emitter base turn-on voltage of Q12, this current has a negative temperature coefficient. As the chip temperature increases from power dissipation, the available short circuit current is reduced. The current limiting also serves to control the current transient that occurs when the output is going through a transition with both Q11 and Q13 turned on.

The AND output is similarly protected by R6 and Q5, which limit the maximum output current to about 100 mA, preventing damage to the circuit from shorts between the outputs and ground.

The current limiting transistors also serve to increase the low state output current capability under severe transient conditions. For example, when the current into the NAND output becomes so high as to pull Q11 out of saturation, the output voltage will rise to two diode drops above ground. At this voltage, the collector-base junction of Q12 becomes forward biased and supplies additional base drive to Q11 through Q10 which is saturated. This minimizes any further increase in output voltage.

When either of the outputs are in the high state, they can drive a large current towards ground without a significant change in output voltage. However, noise induced on the transmission line which tries to drive the output positive will cut it off since it cannot sink current in this state. For this reason, D6 and D8 are included to clamp the output and keep it from being driven much above the supply voltage, as this could damage the circuit.

When the output is in a low state, it can sink a lot of current to clamp positive-going induced voltages on the transmission line. However, it cannot source enough current to eliminate negative-going transients so D5 and D7 are included to clamp those voltages to ground.

It is interesting to note that the voltage swing produced on one of the outputs when the clamp diodes go into conduction actually increases the diffferential noise immunity. For example with no induced common mode current, the low-state output will be a saturation voltage above ground while the high output will be two diode drops below the positive supply voltage. With positive-going common mode noise on the line, the low output remains in saturation; and the high output is clamped at a diode drop above the positive supply. Hence, in this case, the common mode noise increases the differential swing by three diode drops.

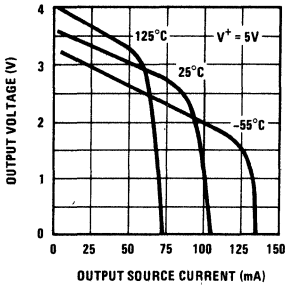


FIGURE 3. High State Output Voltage as a Function of Output Current

Having explained the operation of the line driver, it is appropriate to look at the performance in more detail. Figure 3 shows the high-state output characteristics under load. Over the normal range of output currents, the output resistance is about 10Ω. With higher output currents, the short circuit protection is activated, causing the output voltage to drop to zero. As can be seen from the figure, the short-circuit current decreases at higher temperatures to minimize the possibility of overheating the integrated circuit.

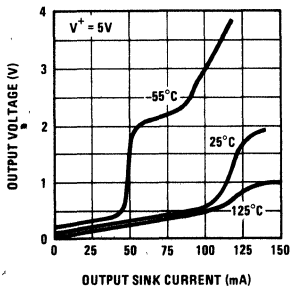


FIGURE 4. Low-State Output Current as a Function of Output Current

Figure 4 is a similar graph of the low-state output characteristics. Here, the output resistance is about 5Ω with normal values of output current. With larger currents, the output transistor is pulled out of saturation; and the output voltage increases. This is most pronounced at –55°C where the transistor current gain is the lowest. However, when the output voltage rises about two diode drops above ground, the collector-base junction of the current-limit transistor becomes forward biased, providing additional base drive for the output transistor. This roughly doubles the current available for clamping positive common-mode transients on the twisted-pair line. It is interesting to note that even though the output level increases to about 2V under this condition, the differential noise immunity does not suffer because the high-state output also increases by about 3V with positive going common-mode transients.

It is clear from the figure that the low state output current is not effectively limited. Therefore, the device can be damaged by shorts between the output and the 5V supply. However, protection against shorts between outputs or from the outputs to ground is provided by limiting the high-state current.

The curves in Figures 3 and 4 demonstrate the performance of the line driver with large, capacitively-coupled common-mode transients, or under

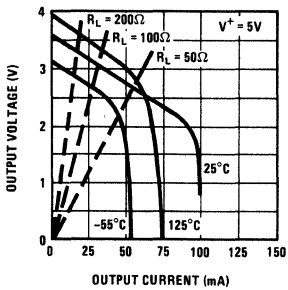


FIGURE 5. Differential Output Voltage as a Function of Differential Output Current

gross overload conditions. Figure 5 shows the ability of the circuit to drive a differential load: that is, the transmission line. It can be seen that for output currents less than 35 mA, the output resistance is approximately 15Ω. At both temperature extremes, the output falls off at high currents. At high temperatures, this is caused by current limiting of the high output state. At low temperatures, the falloff of current gain in the low-state output transistor produces this result.

Load lines have been included on the figure to show the differential output with various load resistances. The output swing can be read off from the intersection of the output characteristic with the load line. The figure shows that the driver can easily handle load resistances greater than 100Ω.

This is more than adequate for practical, twisted-pair lines.

Figure 6 shows the no load power dissipation, for one-half of the dual line driver, as a function of frequency. This information is important for two reasons. First, the increase in power dissipation at high frequencies must be added to the excess power dissipation caused by the load to determine the total package dissipation. Second, and more important, it is a measure of the "glitch" current which flows from the positive supply to ground through the output transistors when the circuit is going through a transition. If the output stage is

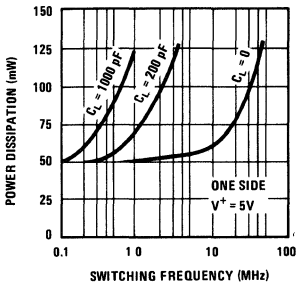


FIGURE 6. Power Dissipation as a Function of Switching Frequency

not properly designed, the current spikes in the power supplies can become quite large; and the power dissipation can increase by as much as a factor of five between 100 KHz and 10 MHz. The figure shows that, with no capacitive loading, the power increase with frequencies as high as 10 MHz is almost negligible. However, with large capacitive loads, more power is required.

The line receiver is designed to detect a zero crossing in the differential output of the line driver. Therefore, the propagation time of the driver is measured as the time difference between the application of a step input and the point where the differential output voltage crosses zero. A plot of the propagation time over temperature is shown in Figure 7. This delay is added directly to the propagation time of the transmission line and the delay of the line receiver to determine the total data-propagation time. However, in most cases, the delay of the driver is small, even by comparison to the uncertainties in the other delays.

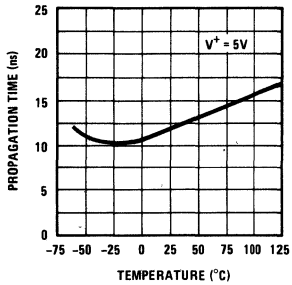


FIGURE 7. Propagation Time as a Function of Temperature

To summarize the characteristics of the DM7830 line driver, the input interfaces directly with standard DTL or TTL circuits. It presents a load which is equivalent to a fan out of 3 to the circuit driving it, and it operates from the 5.0V, ±10% logic supplies. The output can drive low impedance lines down to 50Ω and capacitive loads up to 5000 pF. The time skew between the outputs is minimized to reduce radiation from the twisted-pair lines, and the circuit is designed to clamp common mode transients coupled into the line. Short circuit protection is also provided. The integrated circuit consists of two independent drivers fabricated on a 41 x 53 mil-square die using the standard TTL process. A photomicrograph of the chip is shown in Figure 8.

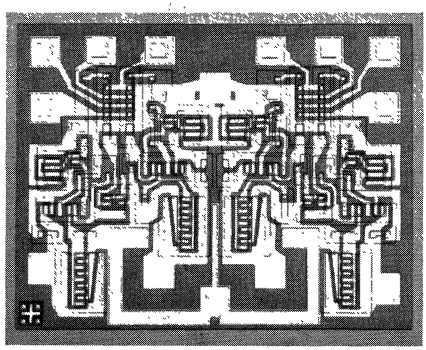


FIGURE 8. Photomicrograph of the DM7830 Dual Line Driver

LINE RECEIVER

As mentioned previously, the function of the line receiver is to convert the differential output signal of the line driver into a single ended, ground-referred signal to drive standard digital circuits on the receiving end. At the same time it must reject the common mode and induced noise on the transmission line.

Normally this would not be too difficult a task because of the large signal swings involved. However, it was considered important that the receiver operate from the +5V logic supply without requiring additional supply voltages, as do most other line receiver designs. This complicates the situation because the receiver must operate with ±15V input signals which are considerably greater than the operating supply voltage.

The large common mode range over which the circuit must work can be reduced with an attenuator on the input of the receiver. In this design, the input signal is attenuated by a factor of 30. Hence, the ±15V common mode voltage is reduced to ±0.5V, which can be handled easily by circuitry operating from a 5V supply. However, the differential input signal, which can go down as low as ±2.4V in the worst case, is also reduced to ±80 mV. Hence, it is necessary to employ a fairly accurate zero crossing detector in the receiver.

System requirements dictated that the threshold inaccuracy introduced by the zero crossing detector be less than 17 mV. In principle, this accuracy requirement should not pose insurmountable problems because it is a simple matter to make well matched parts in an integrated circuit.

Figure 9 shows a simplified schematic diagram of the circuit configuration used for the line receiver. The input signal is attenuated by the resistive dividers R1-R2 and R8-R3. This attenuated signal is fed into a balanced dc amplifier, operating in the common base configuration. This input amplifier, consisting of Q1 and Q2, removes the common mode component of the input signal. Further, it delivers an output signal at the collector of Q2, which is nearly equal in amplitude to the original differential input signal. This output signal is buffered by Q6 and drives an output amplifier, Q8. The output stage drives the logic load directly.

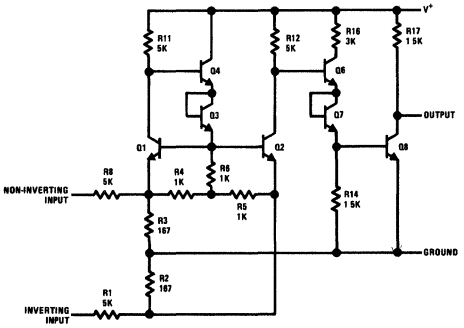


FIGURE 9. Simplified Schematic of the Line Receiver

An understanding of the circuit can be obtained by first considering the input stage. Assuming high current gains and neglecting the voltage drop across R3, the collector current of Q1 will be:

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R11}. \qquad (1)$$

With equal emitter-base voltages for all transistors, this becomes:

$$I_{C1} = \frac{V^+ - 3V_{BE}}{R11}. \qquad (2)$$

The output voltage at the collector of Q2 will be:

$$V_{C2} = V^+ - I_{C2}R12. \qquad (3)$$

When the differential input voltage to the receiver is zero, the voltages presented to the emitters of Q1 and Q2 will be equal. If Q1 and Q2 are matched devices, which is easy to arrange when they are fabricated close together on a single silicon chip, their collector currents will be equal with zero input voltage. Hence, the output voltage from Q2 can be determined by substituting (2) into (3):

$$V_{C2} = V^+ - \frac{R12}{R11}(V^+ - 3V_{BE}). \qquad (4)$$

For R11 = R12, this becomes:

$$V_{C2} = 3V_{BE}.$$

The voltage on the base of Q6 will likewise be $3V_{BE}$ when the output is on the verge of switching from a zero to a one state. A differential input signal which causes Q2 to conduct more heavily will then make the output go high, while an input signal in the opposite direction will cause the output to saturate.

It should be noted that the balance of the circuit is not affected by absolute values of components—only by how well they match. Nor is it affected by variations in the positive supply voltage, so it will perform well with standard logic supply voltages between 4.5V and 5.5V. In addition, component values are chosen so that the collector currents of Q4 and Q6 are equal. As a result, the base currents of Q4 and Q6 do not upset the balance of the input stage. This means that circuit performance is not greatly affected by production or temperature variations in transistor current gain.

A complete schematic of the line receiver, shown in Figure 10, shows several refinements of the basic circuit which are needed to secure proper operation under all conditions. For one, the explanation of the simplified circuit ignores the fact that the collector current of Q1 will be affected by common mode voltage developed across R3. This can give a 0.5V threshold error at the extremes of the ±15V common mode range. To compensate for this, a separate divider, R9 and R10, is used to maintain a constant collector current in Q1 with varying common mode signals. With an increasing common mode voltage on the non-inverting input, the voltage on the emitter of Q1 will increase. Normally, this would cause the voltage across R11 to decrease, reducing the collector current of Q1. However, the increasing common mode signal also drives the top end of R11 through R9 and R10 so as to hold the voltage drop across R11 constant.

In addition to improving the common mode rejection, R9 also forces the output of the receiver into the high state when nothing is connected to the input lines. This means that the output will be in a pre-determined state when the transmission cables are disconnected.

A diode connected transistor, Q5, is also added in the complete circuit to provide strobe capability. With a logic zero on the strobe terminal, the out-

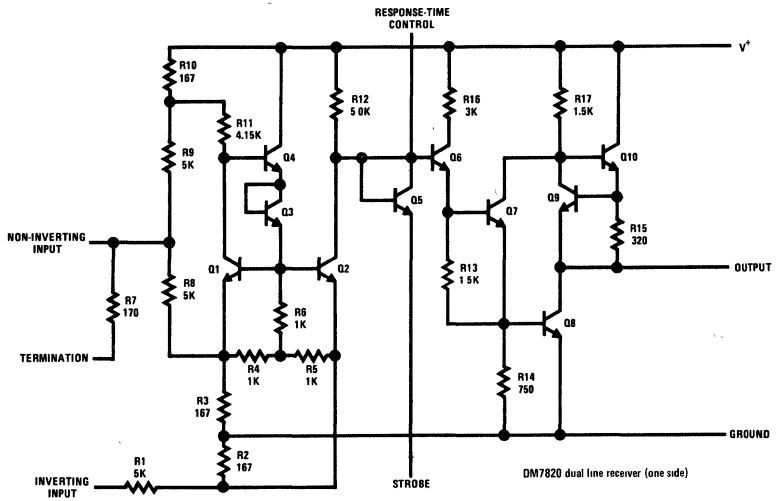


FIGURE 10. Complete Schematic of the Line Receiver

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put will be high no matter what the input signal is. With the strobe, the receiver can be made immune to any noise signals during intervals where no digital information is expected. The output state with the strobe on is also the same as the output state with the input terminals open.

The collector of Q2 is brought out so that an external capacitor can be used to slow down the receiver to where it will not respond to fast noise spikes. This capacitor, which is connected between the response-time-control terminal and ground, does not give exactly-symmetrical delays. The delay for input signals which produce a positive-going output will be less than for input signals of opposite polarity. This happens because the impedance on the collector of Q2 drops as Q6 goes into saturation, reducing the effectiveness of the capacitor.

Another difference in the complete circuit is that the output stage is improved both to provide more gain and to reduce the output resistance in the high output state. This was accomplished by adding Q9 and Q10. When the output stage is operating in the linear region, that is, on the verge of switching to either the high or the low state, Q9 and Q10 form sort of an active collector load for Q8. The current through R15 is constant at approximately 2 mA as the output voltage changes through the active region. Hence, the percentage change in the collector current of Q8 due to the voltage change across R17 is made smaller by this pre-bias current; and the effective stage gain is increased.

With the output in the high state (Q8 cut off), the output resistance is equal to R15, as long as the load current is less than 2 mA. When the load current goes above this value, Q9 turns on; and the output resistance increases to 1.5K, the value of R17.

This particular output configuration gives a higher gain than either a standard DTL or TTL output stage. It can also drive enough current in the high state to make it compatible with TTL, yet outputs can be wire OR'ed as with DTL.

Remaining details of the circuit are that Q7 is connected as an emitter follower to make the circuit even less sensitive to transistor current gains. R16 limits the base drive to Q7 with the output saturated, while R17 limits the base drive to the output transistor, Q8. A resistor, R7, which can be used to terminate the twisted-pair line is also included on the chip. It is not connected directly across the inputs. Instead, one end is left open so that a capacitor can be inserted in series with the resistor. The capacitor significantly reduces the power dissipation in both the line transmitter and receiver, especially in low-duty-cycle applications, by terminating the line at high frequencies but blocking steady-state current flow in the terminating resistor.

Since line receivers are generally used repetitively in a system, the DM7820 has been designed with two independent receivers on a single silicon chip. The device is fabricated on a 41 x 49 mil-square die using the standard six mask planar-epitaxial process. The processing employed is identical to that used on TTL circuits, and the design does not impose any unusual demands on the processing. It is only required that various parts within the circuit match well, but this is easily accomplished in a monolithic integrated circuit without any special effort in manufacturing. A photomicrograph of the integrated circuit chip is shown in Figure 11.

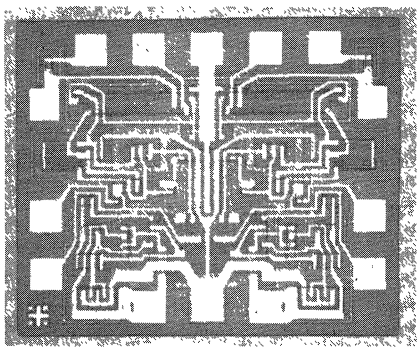

FIGURE 11. Photomicrograph of the DM7820 Dual Line Receiver

The only components in the circuit which see voltages higher than standard logic circuits are the resistors used to attenuate the input signal. These resistors, R1, R7, R8 and R9, are diffused into a separate, floating, N-type isolation tub, so that the higher voltage is not seen by any of the transistors. For a ±15V input voltage range, the breakdown voltages required for the collector-isolation and collector-base diodes are only 15V and 19V, respectively. These breakdown voltages can be achieved readily with standard digital processing.

The purpose of the foregoing was to provide some insight into circuit operation. A more exact mathematical analysis of the device is developed in Appendix A.

RECEIVER PERFORMANCE

The characteristics of the line receiver are described graphically in Figures 12 through 18. Figure 12 illustrates the effect of supply voltage variations on the threshold accuracy. The upper curve gives the differential input voltage required to hold the output at 2.5V while it is supplying 200 μA to the digital load. The lower curve shows the differential input needed to hold the output at 0.4V while it sinks 3.5 mA from the digital load. This load corresponds to a worst case fanout of 2 with either DTL or TTL integrated circuits. The data shows that the threshold accuracy is only affected by ±60 mV for a ±10% change in supply voltage. Proper operation can be secured over a wider range of supply voltages, although the error becomes excessive at voltages below 4V.

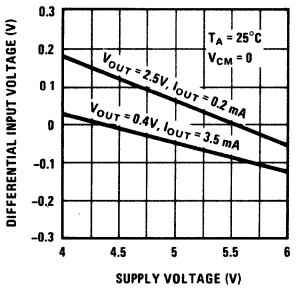

FIGURE 12. Differential Input Voltage Required for High or Low Output as a Function of Supply Voltage

Figure 13 is a similar plot for varying common mode input voltage. Again the differential input voltages are given for high and low states on the output with a worst case fanout of 2. With precisely matched components within the integrated circuit, the threshold voltage will not change with common mode voltage. The mismatches typically encountered give a threshold voltage change of ±100 mV over a ±20V common mode range. This change can have either a positive slope or a negative slope.

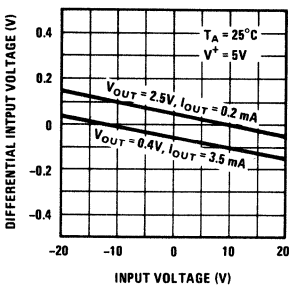

FIGURE 13. Differential Input Voltage Required for High or Low Output as a Function of Common Mode Voltage

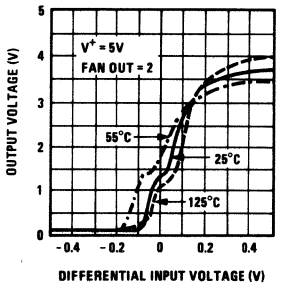

FIGURE 14. Voltage Transfer Function

The transfer function of the circuit is given in Figure 14. The loading is for a worst case fanout of 2. The digital load is not linear, and this is reflected as a non-linearity in the transfer function which occurs with the output around 1.5V. These transfer characteristics show that the only significant effect of temperature is a reduction in the positive swing at –55°C. However, the voltage available remains well above the 2.5V required by digital logic.

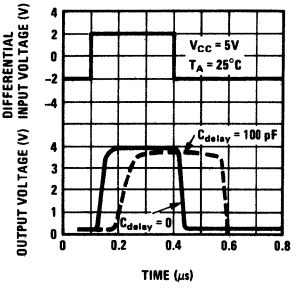

FIGURE 15. Response Time With and Without an External Delay Capacitor

Figure 15 gives the response time, or propagation delay, of the receiver. Normally, the delay through the circuit is about 40 ns. As shown, the delay can be increased, by the addition of a capacitor between the response-time terminal and ground, to make the device immune to fast noise spikes on the input. The delay will generally be longer for negative going outputs than for positive going outputs.

Under normal conditions, the power dissipated in the receiver is relatively low. However, with large common mode input voltages, dissipation increases markedly, as shown in Figure 16. This is of little consequence with common mode transients, but the increased dissipation must be taken into account when there is a dc difference between the grounds of the transmitter and the receiver. It is important to note that Figure 16 gives the dissipation for one half the dual receiver. The total package dissipation will be twice the values given when both sides are operated under identical conditions.

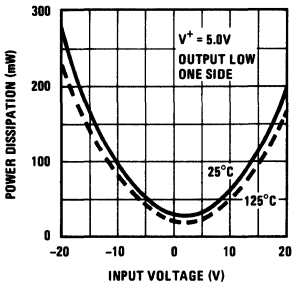

FIGURE 16. Internal Power Dissipation as a Function of Common Mode Input Voltage

Figure 17 shows that the power supply current also changes with common mode input voltage due to the current drawn out of or fed into the supply through R9. The supply current reaches a maximum with negative input voltages and can actually reverse with large positive input voltages. The figure also shows that the supply current with the output switched into the low state is about 3 mA higher than with a high output.

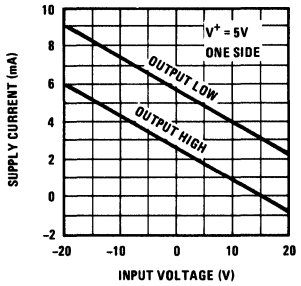

FIGURE 17. Power Supply Current as a Function of Common Mode Input Voltage

The variation of the internal termination resistance with temperature is illustrated in Figure 18.Taking into account the initial tolerance as well as the change with temperature, the termination resistance is by no means precise. Fortunately, in most cases, the termination resistance can vary appreciably without greatly affecting the characteristics of the transmission line. If the resistor tolerance is a problem, however, an external resistor can be used in place of the one provided within the integrated circuit.

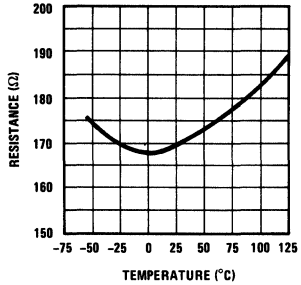

FIGURE 18. Variation of Termination Resistance With Temperature

DATA TRANSMISSION

The interconnection of the DM7830 line driver with the DM7820 line receiver is shown in Figure 19. With the exception of the transmission line, the design is rather straightforward. Connections on the input of the driver and the output or strobe of the receiver follow standard design rules for DTL or TTL integrated logic circuits. The load presented by the driver inputs is equal to 3 standard digital loads, while the receiver can drive a worst-case fanout of 2. The load presented by the receiver strobe is equal to one standard load.

The purpose of C1 on the receiver is to provide dc isolation of the termination resistor for the transmission line. This capacitor can both increase the differential noise immunity, by reducing attenuation on the line, and reduce power dissipation in both the transmitter and receiver. In some applications, C1 can be replaced with a short between Pins 1 and 2, which connects the internal termination resistor of the DM7820 directly across the line. C2 may be included, if necessary, to control the response time of the receiver, making it immune to noise spikes that may be coupled differentially into the transmission lines.

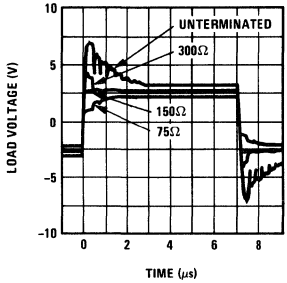

FIGURE 20. Transmission Line Response With Various Termination Resistances

The effect of termination mismatches on the transmission line is shown in Figure 20. The line was constructed of a twisted pair of No. 22 copper conductors with a characteristic impedance of approximately 170Ω. The line length was about 150 ns and it was driven directly from a DM7830 line driver. The data shows that termination resistances which are a factor of two off the nominal value do not cause significant reflections on the line. The lower termination resistors do, however, increase the attenuation.

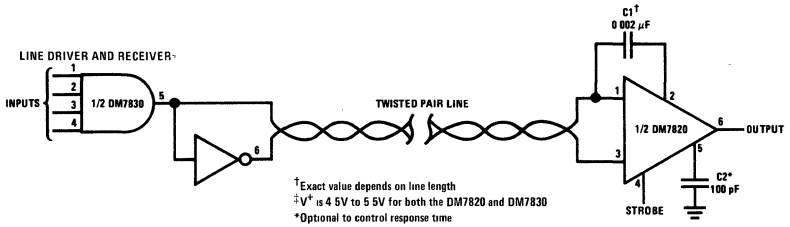

FIGURE 19. Interconnection of the Line Driver and Line Receiver

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Figure 21 gives the line-transmission characteristics with various termination resistances when a dc isolation capacitor is used. The line is identical to that used in the previous example. It can be seen that the transient response is nearly the same as a dc terminated line. The attenuation, on the other hand, is considerably lower, being the same as an unterminated line. An added advantage of using the isolation capacitor is that the dc signal current is blocked from the termination resistor which reduces the average power drain of the driver and the power dissipation in both the driver and receiver.

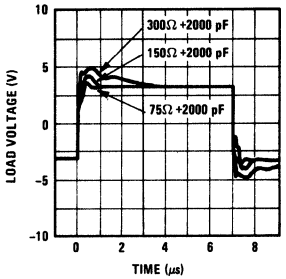


FIGURE 21. Line Response for Various Termination Resistances With a DC Isolation Capacitor

The effect of different values of dc isolation capacitors is illustrated in Figure 22. This shows that the RC time constant of the termination resistor/isolation capacitor combination should be 2 to 3 times the line delay. As before, this data was taken for a 150 ns long line.

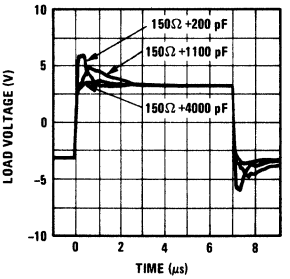
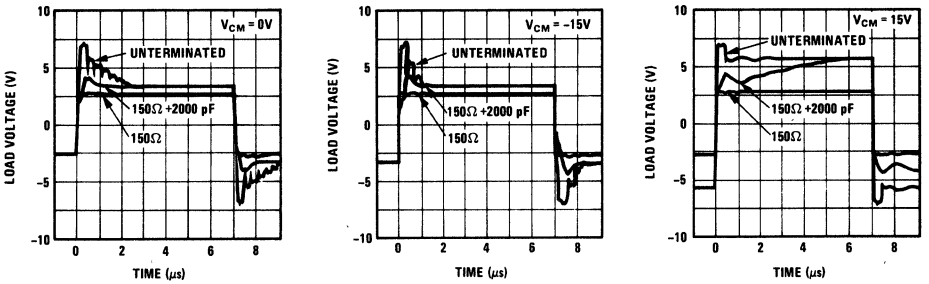


FIGURE 22. Response of Terminated Line With Different DC Isolation Capacitors

In Figure 23, the influence of a varying ground voltage between the transmitter and the receiver is shown. The difference in the characteristics arises because the source resistance of the driver is not constant under all conditions. The high output of



a. V_{CM} = 0V b. V_{CM} = −15V c. V_{CM} = 15V

FIGURE 23. Line Response With Different Terminations and Common Mode Input Voltages

the transmitter looks like an open circuit to voltages reflected from the receiving end of the transmission line which try to drive it higher than its normal dc state. This condition exists until the voltage at the transmitting end becomes high enough to forward bias the clamp diode on the 5V supply. Much of the phenomena which does not follow simple transmission-line theory is caused by this. For example, with an unterminated line, the overshoot comes from the reflected signal charging the line capacitance to where the clamp diodes are forward biased. The overshoot then decays at a rate determined by the total line capacitance and the input resistance of the receiver.

When the ground on the receiver is 15V more negative than the ground at the transmitting end, the decay with an unterminated line is faster, as shown in Figure 23b. This occurs because there is more current from the input resistor of the receiver to discharge the line capacitance. With a terminated line, however, the transmission characteristics are the same as for equal ground voltages because the terminating resistor keeps the line from getting charged.

Figure 23c gives the transmission characteristics when the receiver ground is 15V more positive than the transmitter ground. When the line is not terminated, the differential voltage swing is increased because the high output of the driver will be pulled against the clamp diodes by the common mode input current of the receiver. With a dc isolation capacitor, the differential swing will reach this same value with a time constant determined by the isolation capacitor and the input resistance of the receiver. With a dc coupled termination, the characteristics are unchanged because the differential load current is large by comparison to the common mode current so that the output transistors of the driver are always conducting.

The low output of the driver can also be pulled below ground to where the lower clamp diode conducts, giving effects which are similar to those described for the high output. However, a current of about 9 mA is required to do this, so it does not happen under normal operating conditions.

To summarize, the best termination is an RC combination with a time constant approximately equal to 3 times the transmission-line delay. Even though its value is not precisely determined, the internal termination resistor of the integrated circuit can be used because the line characteristics are not greatly affected by the termination resistor.

The only place that an RC termination can cause problems is when the data transmission rate approaches the line delay and the attenuation down the line (terminated) is greater than 3 dB. This would correspond to more than 1000 ft. of twisted-pair cable with No. 22 copper conductors. Under these conditions, the noise margin can disappear with low-duty-cycle signals. If this is the case, it is best to operate the twisted-pair line without a termination to minimize transmission losses. Reflections should not be a problem as they will be absorbed by the line losses.

CONCLUSION

A method of transmitting digital information in high-noise environments has been described. The technique is a much more attractive solution than high-noise-immunity logic as it has lower power consumption, provides more noise rejection, operates from standard 5V supplies, and is fully compatible with almost all integrated logic circuits. An additional advantage is that the circuits can be fabricated with integrated circuit processes used for standard logic circuits.

APPENDIX A

LINE RECEIVER

Design Analysis

The purpose of this appendix is to derive mathematical expressions describing the operation of the line receiver. It will be shown that the performance of the circuit is not greatly affected by the absolute value of the components within the integrated circuit or by the supply voltage. Instead, it depends mostly on how well the various parts match.

The analysis will assume that all the resistors are well matched in ratio and that the transistors are likewise matched, since this is easily accomplished over a broad temperature range with monolithic construction. However, the effects of component mismatching will be discussed where important. Further, large transistor current gains will be assumed, but it will be pointed out later that this is valid for current gains greater than about 10.

A schematic diagram of the DM7820 line receiver is shown in Figure A-1. Referring to this circuit, the collector current of the input transistor is given by

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} - \frac{\frac{R3}{R4 + 2R6 + R3} V_{BE1} - \frac{R3 \,//\, R11}{R8 + R3 \,//\, R1} V_{IN}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} + \frac{(V_{IN} - V^+) \frac{R10 \,//\, R11}{R9 + R10 \,//\, R11}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} \quad \text{(A. 1)}$$

where V_{IN} is the common mode input voltage and $R_a//R_b$ denotes the parallel connection of the two resistors. In Equation (A. 1), R8 = R9, R3 = R10, R10 << R11, R9 >> R10, R3 << R11, R8>>R3 and $\frac{R3}{R4 + 2R6 + R3}$ <<3 so it can be reduced to

$$I_{C1} = \frac{V^+ - 3V_{BE} - \frac{R10}{R9} V^+}{R10 + R11 + R3} \quad \text{(A. 2)}$$

which shows that the collector current of Q1 is not affected by the common mode voltage.

The output voltage on the collector of Q2 is

$$V_{C2} = V^+ - I_{C2} R12 \quad \text{(A. 3)}$$

For zero differential input voltage, the collector currents of Q1 and Q2 will be equal so Equation (A. 3) becomes

$$V_{C2} = V^+ - \frac{R12 \left(V^+ - 3V_{BE} - \frac{R10}{R9} V^+\right)}{R10 + R11 + R3} \quad \text{(A. 4)}$$

It is desired that this voltage be $3V_{BE}$ so that the output stage is just on the verge of switching with zero input. Forcing this condition and solving for R12 yields

$$R12 = (R10 + R11 + R3) \frac{V^+ - 3V_{BE}}{V^+ - 3V_{BE} - \frac{R10}{R9} V^+} \quad \text{(A. 5)}$$

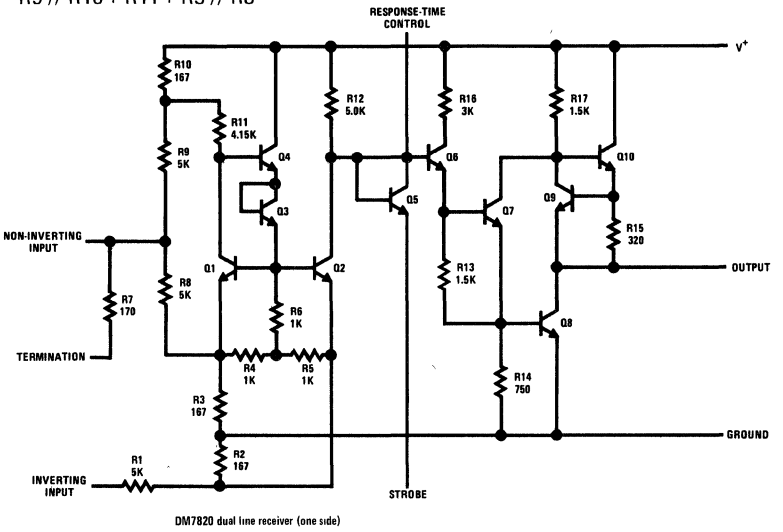


FIGURE A-1. Schematic Diagram of the DM7820 Line Receiver

This shows that the optimum value of R12 is dependent on supply voltage. For a 5V supply it has a value of 4.7 kΩ. Substituting this and the other component values into (A. 4),

$$V_{C2} = 2.83V_{BE} + 0.081V^{+}, \qquad \text{(A. 6)}$$

which shows that the voltage on the collector of Q2 will vary by about 80 mV for a 1V change in supply voltage.

The next step in the analysis is to obtain an expression for the voltage gain of the input stage.

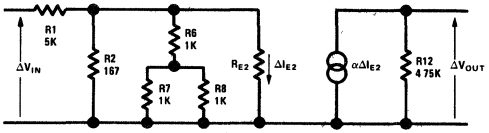


FIGURE A-2. Equivalent Circuit Used to Calculate Input Stage Gain

An equivalent circuit of the input stage is given in Figure A-2. Noting that R6 = R7 = R8 and R2 ≅ 0.1 (R6 + R7//R8), the change in the emitter current of Q1 for a change in input voltage is

$$\Delta I_{E2} = \frac{0.9\ R2}{R1\ (0.9\ R2 + R_{E2})}\ \Delta V_{IN}\ . \qquad \text{(A. 7)}$$

Hence, the change in output voltage will be

$$\Delta V_{OUT} = \alpha I_{E2} R12$$

$$= \frac{0.9\ \alpha\ R2\ R12}{R1\ (0.9\ R2 + R_{E2})}\ \Delta V_{IN}\ . \qquad \text{(A. 8)}$$

Since $\alpha \cong 1$, the voltage gain is

$$A_{V1} = \frac{0.9\ R2\ R12}{R1\ (0.9\ R2 + R_{E2})} \qquad \text{(A. 9)}$$

The emitter resistance of Q2 is given by

$$R_{E2} = \frac{kT}{qI_{C2}}, \qquad \text{(A. 10)}$$

where

$$I_{C2} = \frac{V^{+} - 3V_{BE}}{R12} \qquad \text{(A. 11)}$$

so

$$R_{E2} = \frac{kT\ R12}{q\ (V^{+} - 3V_{BE})} \qquad \text{(A. 12)}$$

Therefore, at 25°C where V_{BE} = 670 mV and kT/q = 26 mV, the computed value for gain is 0.745. The gain is not greatly affected by temperature as the gain at −55°C where V_{BE} = 810 mV and kT/q = 18 mV is 0.774, and the gain at 125°C where V_{BE} = 480 mV and kT/q = 34 mV is 0.730.

With a voltage gain of 0.75, the results of Equation (A. 6) show that the input referred threshold voltage will change by 0.11V for a 1V change in supply voltage. With the standard ±10-percent supplies used for logic circuits, this means that the threshold voltage will change by less than ±60 mV.

Finally, the threshold error due to finite gain in the output stage can be considered. The collector current of Q7 from the bleeder resistor R14, is large by comparison to the base current of Q8, if Q8 has a reasonable current gain. Hence, the collector current of Q7 does not change appreciably when the output switches from a logic one to a logic zero. This is even more true for Q6, an emitter follower which drives Q7. Therefore, it is safe to presume that Q6 does not load the output of the first-stage amplifier, because of the compounded current gain of the three transistors, and that Q8 is driven from a low resistance source.

It follows that the gain of the output stage can be determined from the change in the emitter-base voltage of Q8 required to swing the output from a logic one state to a logic zero state. The expression

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \qquad \text{(A. 13)}$$

describes the change in emitter-base voltage required to vary the collector current from one value, I_{C1}, to a second, I_{C2}. With the output of the receiver in the low state, the collector current of Q8 is

$$I_{OL} = \frac{V^{+} - V_{OL} - V_{BE9} - V_{BE10}}{R17}$$

$$+ \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} + I_{SINK}\ , \qquad \text{(A. 14)}$$

where V_{OL} is the low state output voltage and I_{SINK} is the current load from the logic that the receiver is driving. Noting that R13 = 2R14 and figuring that all the emitter-base voltages are the same, this becomes

$$I_{OL} = \frac{V^{+} - V_{OL} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15}$$

$$- \frac{V_{BE}}{2R14} + I_{SINK}\ . \qquad \text{(A. 15)}$$

Similarly, with the output in the high state, the collector current of Q8 is

$$I_{OH} = \frac{V^{+} - V_{OH} - V_{BE9} - V_{BE10}}{R17}$$

$$+ \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14}$$

$$+ \frac{V_{BE7}}{R13} - I_{SOURCE}\ , \qquad \text{(A. 16)}$$

where V_{OH} is the high-level output voltage and I_{SOURCE} is the current needed to supply the input leakage of the digital circuits loading the comparator.

With the same conditions used in arriving at (A. 15), this becomes

$$I_{OH} = \frac{V^+ - V_{OH} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} - I_{SOURCE} \cdot \quad \text{(A. 17)}$$

From (A. 13) the change in the emitter-base voltage of Q8 in going from the high output level to the low output level is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{OL}}{I_{OH}} \quad \text{(A. 18)}$$

providing that Q8 is not quite in saturation, although it may be on the verge of saturation.

The change of input threshold voltage is then

$$\Delta V_{TH} = \frac{kT}{qA_{V1}} \log_e \frac{I_{OL}}{I_{OH}} \quad \text{(A. 19)}$$

where A_{V1} is the input stage gain. With a worst case fanout of 2, where V_{OH} = 2.5V, V_{OL} = 0.4V, I_{SOURCE} = 40 μA and I_{SINK} = 3.2 mA, the calculated change in threshold is 37 mV at 25°C, 24 mV at –55°C and 52 mV at 125°C.

The measured values of overall gain differ by about a factor of two from the calculated gain. This is not too surprising because a number of assumptions were made which introduce small errors, and all these errors lower the gain. It is also not too important because the gain is high enough where another factor of two reduction would not cause the circuit to stop working.

The main contributors to this discrepancy are the non-ideal behavior of the emitter-base voltage of Q8 due to current crowding under the emitter and the variation in the emitter base voltage of Q7 and Q8 with changes in collector-emitter voltage (h_{RE}).

Although these parameters can vary considerably with different manufacturing methods, they are relatively fixed for a given process. The ΔV_{BE} errors introduced by these quantities, if known, can be added directly into Equation (A. 18) to give a more accurate gain expression.

The most stringent matching requirement in the receiver is the matching of the input stage divider resistors: R1 with R8 and R2 with R3. As little as 1% mismatch in one of these pairs can cause a threshold shift of 150 mV at the extremes of the ±15V common mode range. Because of this, it is necessary to make the resistors absolutely identical and locate them close together. In addition, since R1 and R8 do dissipate a reasonable amount of power, they have to be located to minimize the thermal gradient between them. To do this, R9 was located between R1 and R8 so that it would heat both of these resistors equally. There are not serious heating problems with R2 and R3; however, because of their low resistance value, it was necessary even to match the lengths of the aluminum interconnects, as the resistance of the aluminum is high enough to cause intolerable mismatches. Of secondary importance is the matching of Q1 and Q2 and the matching of ratios between R11 and R12. A 1 mV difference in the emitter-base voltages of Q1 and Q2 causes a 30 mV input offset voltage as does a 1% mismatch in the ratio of R11 to R12.

The circuit is indeed insensitive to transistor current gains as long as they are above 10. The collector currents of Q4 and Q6 are made equal so that their base currents load the collectors of Q1 and Q2 equally. Hence, the input threshold voltage is affected only by how well the current gains match. Low current gain in the output transistor, Q8, can cause a reduction in gain. But even with a current gain of 10, the error produced in the input threshold voltage is less than 50 mV.

ANALOG-SIGNAL COMMUTATION

INTRODUCTION

Telemetry and other data-acquisition systems have become very compact and efficient, particularly when built with integrated circuits. To keep in step, small, low-power commutators are needed to multiplex large numbers of analog signals. Metal-oxide-semiconductor field-effect transistors do the job well.

MOS IC's containing several MOSFET switching channels are presently available in production quantities and perform excellently as low-level analog commutators if the system designer understands their limitations and exploits their advantages. This report will describe the DC characteristics involved in switching analog signals when the signal input range varies between −10V and +10V.

MOSFET's size up very well against earlier switching devices when their overall characteristics are considered (see Table 1 and the discussion of competitive devices). In addition to being fabricated easily as multichannel IC's—in some cases, complete with switching-control circuitry on the chip—MOSFET's have several significant electrical advantages:

- Power dissipation is essentially zero in most applications. No DC power is consumed in the control gate, and practically no signal power is dissipated in the switch.
- Offset voltage is zero in a well-designed switch.
- Resistance is reasonably low when the channel is conducting.
- Resistance of an OFF channel is practically open-circuit (R_{OFF} is on the order of 10^{12} ohms and leakage currents are very small, about 100 pA).
- Analog signals are well isolated from the switch-control signals.

With all of these things in their favor, MOS analog-switching IC's will come into much wider use, especially in large, multichannel instrumentation and data-transmission systems.

	Mechanical Switch	Bipolar Transistor	Photocell	N Junction FET	P MOS FET
"On" Resistance	$10^{-2}\Omega$	10Ω	1 KΩ	30Ω	100Ω
"Off" Leakage	10 pA	100 pA	10 nA	100 pA	100 pA
Offset Voltage	0	10^{-2}V	0	0	0
Commutation Rate	1 KHz	100 KHz	100 Hz	10 MHz	50 MHz

Table 1

Comparison of Switches

MOS IC STRUCTURE

MOS IC's generally provide four or more channels in a monolithic chip, but two are enough to illustrate the basic construction that governs switch operation. The cutaway view of Figure 1 shows two complete MOSFET's, one of which may be on while the other is off. Figure 2 is the schematic.

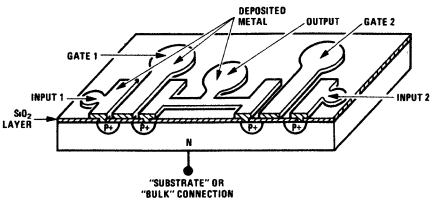


FIGURE 1. Cross-section of Two MOSFET's in an Integrated Circuit.

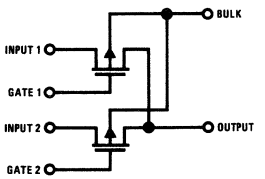


FIGURE 2. Schematic Diagram of Two-Channel Analog Switch.

Both MOSFET's have a common substrate, the "bulk" consisting of lightly doped N type silicon. Thermally grown silicon oxide covers the entire chip surface, except where the oxide was etched away to allow ohmic connections of input and output electrodes to stripes diffused with P+ dopants. These stripes are the MOSFET drain and source regions. Each gate is defined by the gate electrode, which lies over a channel region and is isolated from it by the oxide (hence, MOSFET's are sometimes called insulated-gate FET's or IGFET's).

All electrodes are etched from a thin film of deposited aluminum. Each MOSFET has separate input and gate electrodes, but the output electrodes may be paired as shown, connected to a common output pin, or connected to separate output pins on the package. The same basic MOSFET

structure can be used, whether the circuit is a differential switch, a multiplexer, or independent switches in a single package (see Figure 3).

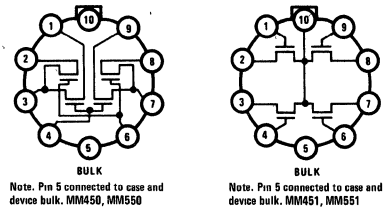


FIGURE 3. Connection Diagrams of Dual Differential Switch, Four-Channel Switch and Quad MOS Transistor.

MOSFET's are, for practical purposes, bilaterally symmetrical. The drain (or source) can be either the input or output. By strict definition, the drain is the electrode to which majority-carrier current flows. The majority carriers are "holes" in the channel of P-channel MOSFET's (N-channel MOSFET's are not commonly used in MOS IC's). In most analog switching applications, the signal contains AC components, so the direction of current flow frequently alternates.

SWITCHING AND ISOLATION

A P-channel MOSFET turns on when negative voltage is applied between gate and source. The gate is biased negative with respect to the bulk. Electrons accumulate on the gate, creating positive charges in the channel region. This inverts the electric charge thus creating an "enhanced" P type channel in the n-type semiconductor. When the gate is several volts more negative than threshold, a conducting channel is formed, allowing majority carrier current (holes) to flow freely between source and drain. The channel is said to be "enhanced," so these MOSFET's are called P-channel enhancement MOSFET's.

Operating voltages in a typical switching channel are illustrated in Figure 4. In most schematics, the bulk connection would not be shown.

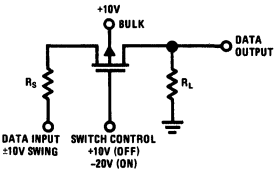


FIGURE 4. Biases on Single MOS Channel at Maximum Signal Range of ±10V.

The applied biases are those that would be used at an analog signal range of ±10V. At any signal range, the following guidelines apply:

1. Bulk bias V_{BB} must equal or be more positive than the most positive excursion of the analog signal. This bias must be maintained at all times, so is taken from a DC supply.
2. To turn the switch ON and make R_{ON} low, the voltage applied to the gate should be *at least* 5V more negative than the most negative excursion of the analog signal (10V is desirable). The actual gate voltage is V_{GG} and the gate bias is $-V_{GB}$.
3. To ensure that the switch turns OFF fully, V_{GG} should be as positive as V_{BB} making $V_{GB} = 0$.

The first rule must be followed to get good performance from the switch. With V_{BB} most positive, the p-n junctions are kept reverse-biased. When the channel is OFF, this condition isolates the drain from the source. When the switch is turned ON and the P-channel is enhanced, the drain-channel-source region is isolated by the p-n junction from the substrate because the substrate is "reverse biased" from all of these regions at all times.

The voltage across the switch, from drain to source, is caused by IR drop whether the switch is on or off. The MOS analog switch does not have any inherent offset voltage. To get $V_{out} = V_{in}$ in a MOSFET switch merely requires that load resistance R_L be much larger than the resistance in the conducting channel, R_{ON}. Since R_L is generally about 100 kilohms in most high-accuracy analog commutator applications, the requirement is easily met.

Figure 5 helps clarify rules (2) and (3). This curve shows how the gate-source threshold voltage changes with bulk-source bias voltage. Channel resistance is high and current flow at the output can only be a few microamperes. A forward bias higher than threshold is needed to enhance the channel. Making gate bias much more negative than V_{TH} at turn-ON does this. Then, at turn-OFF, the gate bias becomes more positive than V_{TH} when $V_{GG} = V_{BB}$. The channel must revert to N-type silicon thus preventing majority carrier current flow.

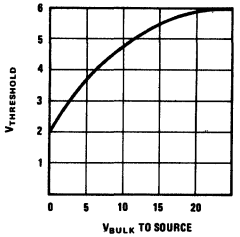
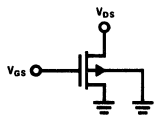


FIGURE 5. Variation in Switching-Threshold Voltage with Changes in Bulk-to-Source Bias Voltage.

The circuit designer must use biases that prevent the drain from having a positive potential when the switch is OFF. For example, V_{in} = +10V and V_{BB} = +9V should not be allowed. Operating with V_{DS} = +1V won't harm the MOSFET, but some of the signal will appear at the output. Effects of improper biasing can be seen in Figure 6. With the source and bulk grounded while V_{DS} varies, output currents at different gate biases are measured to produce the "drain family of curves." The normal family looks like Figure 6b (the drain family of National Semiconductor's MM450/MM550 MOS switching IC's). The "bipolar" family in Figure 6c shows what happens when V_{DS} is allowed to go positive.



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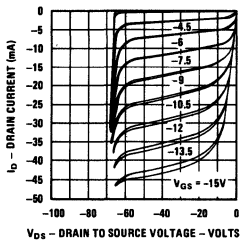

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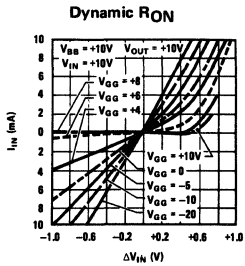

6c

FIGURE 6. Drain-Current Measuring Circuit, Normal Drain Family of Curves, and "Bipolar" Drain Family of Curves.

During small excursions of V_{DS}, the MOSFET acts as a voltage-variable resistor. But when V_{DS} rises to about +0.6V, there is an abrupt increase in drain current. At this point, the diode drop is exceeded and the drain-bulk junction becomes forward biased. Minority carriers are injected into the n-type channel region, causing grounded-base pnp bipolar transistor action (note in Figure 1 that a MOSFET resembles a lateral pnp transistor in the OFF condition). Output current will be α times the input current. In most MOS devices, the amplification factor will be 0.5 to 0.9.

It is absolutely mandatory that the $V_{DS} \geq$+0.6V be avoided. Otherwise the effective R_{OFF} will be poor and the channel will seem to have abnormally high leakage current.

Only the upper right corner of the graph in Figure 6b, detailed in the third quadrant of Figure 6c, is useful in practical circuit designs. The useful characteristics are to the right of $-V_{DS} = -1$ and above a load line at about I_D = 0.5 mA.

ON AND OFF RESISTANCE

Both R_{ON} and R_{OFF} normally vary with signal voltage and operating temperature. A positive signal voltage improves channel enhancement by making the gate more negative with respect to drain and source.

R_{ON} is minimum at the most positive signal level. It will increase slowly with temperature, since high temperatures reduce the mobility of majority carriers. Neverthless, R_{ON} will have little effect on signal quality if R_L is much larger. R_{ON} does vary nonlinearly, though, so we investigated its effect upon signal quality. Figure 7 proves that the effect is negligible provided that the biasing rules are observed.

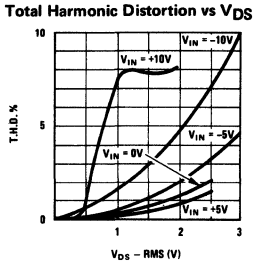

FIGURE 7. Small-Signal Harmonic Distortion (Measured with Only About 100 Ohms Load Resistance).

The curves of small-signal harmonic distortion in Figure 7 were measured with practically no load resistance. AC signals at various voltages were

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applied to the MOSFET input and the current flow was measured at the output with the help of a 100-ohm current-sensing resistor. Distortion levels less than 0.1% could not be measured with available instruments. The anomaly in the +10V curve is due to diode distortion of the type illustrated in Figure 6c. The input signal's AC plus DC components exceeded the bulk voltage, V_{BB} = +10V, by more than the +0.6V diode drop.

The harmonic distortion is amply low for practical applications. With a 1-kilohm load, the small-signal distortion typically would be less than 0.5%, with V_{in} = ±10V and V_{DS} almost ±1V. A load of 1 kilohm is unusually small. Small signal distortion would be almost unmeasurable with a 10-kilohm load. When signal accuracy must be very high, 100 kilohms are used by some designers.

Worst-case R_{ON} can be expected at a –10V input. Figure 8 gives the change in R_{ON} of the MM450/MM550 series devices when the analog input is at +10V, 0V and –10V. If lower impedance is essential, the gate can be biased more negative. For instance, at V_{BB} = +10V, V_{GG} can be made –25V or –30V instead of –20V, increasing $-V_{GB}$ to –35V or –40V. Don't go over the specificed maximum bias, which is usually –45V, because excessive bias could reduce the device operating life.

Conversely, all biases can be reduced if the signal voltage range is less than ±10V. The gate-drive circuit will not have to swing as far, the switch can be operated faster, and switching transients will be smaller. Or, the bulk bias can be reduced and the gate bias maintained at the previous ON level. This

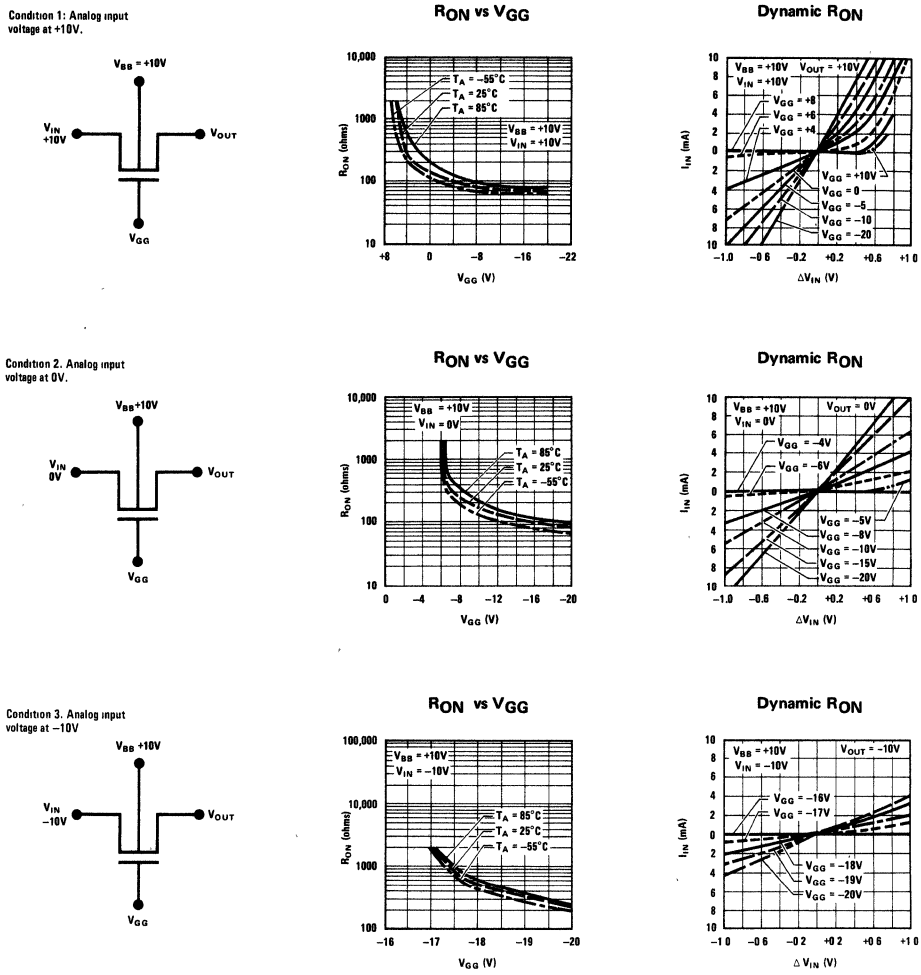


FIGURE 8. Typical R_{ON} Characteristics of MM450/MM550 MOS Devices at Most Positive, Zero and Most Negative Signal Voltages.

will give the effect shown in Figure 9—an improvement in channel enhancement and reductions in R_{ON} at the various signal levels.

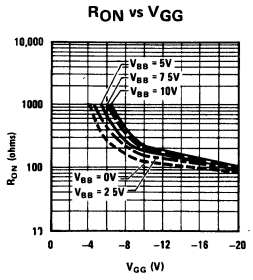


FIGURE 9. Bulk Bias Effect on R_{ON}.

When the gate is turned OFF, impedance between source and drain becomes very high ($R_{OFF} \approx 10^{12}$ ohms). A MOSFET's only significant DC conduction is leakage current. Total leakage in MM450/MM550 devices is typically less than 100 pA at 25°C. It rises more rapidly than R_{ON} with increasing temperature, approximately doubling with every 10°C rise in temperature. However, the MM450 devices are low-leakage types that are specified for use to 125°C. At the maximum temperature, leakage will usually be less than 100 nA. (At very high signal frequencies, another conduction mechanism may occur—analog signal feedthrough in the device capacitances, which can be prevented by making the gate-driver impedance low when the switch is OFF.)

The two significant forms of DC leakage are leakage from source and drain to bulk, and leakage through the channel from input to output. When all channels in the multiplexer are OFF, and the outputs of each MOSFET are connected to a common package pin, total leakage will be the sum of the bulk and channel leakages.

Worst-case leakage is measured with the circuit in Figure 10. The pin at which the leakage current is measured is biased to –25V and all other pins are grounded. This is equivalent to the bulk being biased at +10V, all gates at +10V, and all analog-signal inputs at +10V, with the output at –15V.

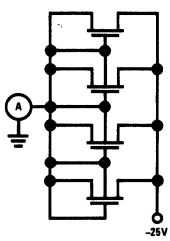


FIGURE 10. Worst-Case Leakage Test Circuit and Typical Worst-Case Total Leakage of MM451 at 25°C.

Channel leakage is measured with the test circuit in Figure 11a. At V_{in} = +10V, the leakage at the output is at its maximum positive value. As V_{in} goes more negative than +10V, channel leakage decreases, goes through zero, and becomes negative, as in Figure 11b.

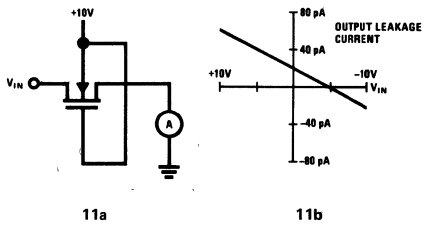


FIGURE 11. Channel-Leakage Test Circuit and Variation in Leakage with Signal Voltage.

The designer of switching systems that require very high R_{OFF} values under all signal conditions should anticipate the possibility of worst-case leakage. But average leakage will generally be considerably less than worst case. First, leakage currents in each switch are voltage-sensitive, and will be less than maximum at signal voltages less than +10V. Secondly, when the analog signals on some channels are positive and those on other channels are negative, the negative currents will subtract from the positive currents, further reducing the total leakage at the output. Also, when a switch is ON, it would not be contributing to the leakage. Assuming signal voltages vary randomly between +10 and –10V, total leakage will run about half that of worst case. Of course, leakage will be still less if the analog signal limits are less than ±10V.

CONCLUSION

Integrated MOSFET switching circuits make excellent low-level analog commutators. Power dissipation is essentially zero, capacitance is reasonably low (typically 8 pF at the analog input), the R_{OFF}/R_{ON} ratio is high, and the control signal is isolated from the input. MOS IC's with four or more switching channels are readily available in production quantities.

Conventional bipolar drive circuitry can control channel switching at rates in the megahertz range. Hybrid integrated circuits containing monolithic MOS multiplexers and bipolar drivers are being manufactured for medium-speed applications (NH0014 and NH0019). Level-changing circuits in these devices allow external TTL or DTL IC's to control the commutator at analog signal levels to ±10V. MOS commutator systems can be built with building-block circuits such as the MM454F in Figure 12. This monolithic IC can commutate at rates to 1 MHz, depending on the range of signal voltages. The control logic on the chip includes a clock-countdown chain that facilitates submultiplexing.

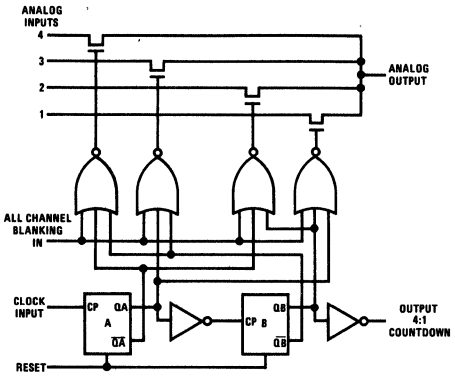


FIGURE 12. Logic Diagram of MM454F Four-Channel MOS Multiplexer. Switches and Control Circuitry Are Fabricated in the Same Monolithic Chip.

MOSFET switches are generally used to commutate low-frequency analog signals. Today, the preferred device for RF-signal multiplexing is the N-channel junction FET, which can handle signal frequencies in the VHF range. MOS IC's have operated successfully, however, in some RF application. The high-frequency capabilities of MOS IC's are being investigated by the author and will be the subject of a future report.

Although the most outstanding feature of MOSFET's is the ease with which they can be fabricated as multichannel monolithic IC's, their electrical characteristics compare quite favorably with those of other switching components. An "order of magnitude" comparison of MOSFET's and other devices that could be used for low-level analog switching is given by Table 1. Better characteristics might be obtained in each case, but these values are typical.

Each type of analog switch has advantages and limitations that must be considered for practical use. No switch is perfect. If a switch were perfect, it would have zero resistance when ON, infinite resistance when OFF, and be 100% efficient—that is, it would consume no power.

Electrically, the mechanical switch comes close to this ideal. It has the highest R_{OFF}/R_{ON} ratio and totally isolates the analog signal from the switching-control function. However, it has mechanical drawbacks that make it noisy and unsuitable for low-level commutation: contact bounce, contact pitting, susceptibility to vibration, and the necessity to move a physical mass to turn the switch on or off. It cannot commutate very fast and consumes more power than a solid-state switch, as a rule.

Bipolar transistors make excellent digital switches, the fastest ever developed, but they are usually a poor choice for multiplexing low-level analog signals. Their main disadvantages are an inherent offset voltage and the impossibility of isolating the switching control signal from the analog signal being switched. Furthermore, analog switching rates are slower than FET's. Their R_{on} is low, though—typically 10 ohms in analog switches (versus milliohms in power transistors). Bipolar transistors fare much better in high-level switching, where DC offset is not a problem.

Photocells make fairly good analog switches. Because light is used as the control signal, the control is completely isolated from the analog electrical signal. However, R_{ON} is high and the R_{OFF}/R_{ON} ratio is relatively poor. Even at moderate R_{OFF}/R_{ON} ratios, photocells cannot commutate much faster than 100 Hz. After exposure to intense light, a photocell made with a semiconductor such as cadmium sulfide or cadmium selenide exhibits a long turn-off decay time. Photocell turn-off time constants may stretch out for many seconds before R_{OFF} reaches an acceptable level. Faster switches can be made with combinations of electroluminescent diodes and phototransistors, but these devices are still very expensive.

Some N-channel junction FET's come close to being ideal switches. Offset voltage is zero, and the admittance-to-input capacitance ratio Y_{fs}/C_{iss} is the highest of any contemporary device. These two parameters govern commutation rate, which can be very high if the impedances of the signal source and the load are made very low. Theoretically, the high majority-carrier mobility in an N-channel J-FET enables it to operate at a frequency higher than any other type of FET. A good example is the 2N4391: R_{OFF}/R_{ON} is about 10^9, $R_{ds\ (on)}$ is a maximum of 30 ohms, and maximum leakage at 25°C is 100 pA. The one major disadvantage of N-channel J-FET's is that they are extremely difficult to make in the form of multichannel IC's. For high-frequency commutation, the P-channel type of J-FET is a poor choice because its majority carrier mobility is lower than N channel J-FET's.

APPLICATIONS OF MOS ANALOG SWITCHES

ABSTRACT

This discussion begins with some basic commutation circuits, then describes some uses in linear amplifier applications such as reset functions and chopper applications. The use of MOS switches as a suppressed carrier double-sideband modulator and a double-sideband demodulator is then covered; followed by a circuit proposal for a phase-locked loop AM-FM detector without tuned circuits.

THE MOS DIFFERENTIAL SWITCH—DC TO RF

The dual differential switch is a particular switch connection scheme which at first glance prompts one to say—so what? It is, however, one of those simple circuit configurations which can find a wide variety of uses in electronic circuits. The dual differential switch could also be called a DPDT switch or two SPDT switches—depending on how they are toggled.

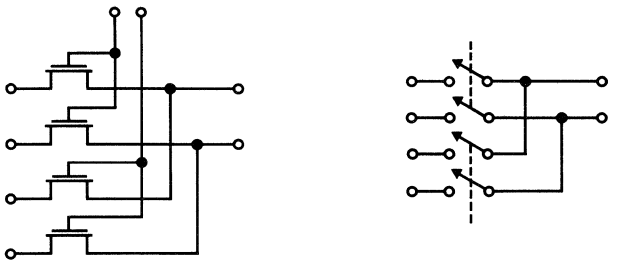
MOS switches have some unique features which make them very useful for data switching[1,2,3]: no offset voltage, high R_{OFF}/R_{ON} ratios, low leakage, fast operation, and matched "on" resistance. Within definite bounds, MOS switches exhibit good isolation between the switching drive and signal path.

MOS switches do have somewhat unique driving requirements. In order to solve this problem, National manufactures a hybrid integrated circuit which provides DTL-TTL drive compatibility with the dual differential switch. These devices use the DM7801 chip with an MM450 chip for the NH0014 and the DM7800 chip with an MM450 chip for the NH0019. The NH0014 is basically a DPDT switch while the NH0019 is two SPDT switches in the same package. Each connection has its particular advantages and disadvantages.

COMMUTATION CIRCUITS

The NH0014 may be used as a two channel commutator only, because two of its four channels are always on. The NH0019 may be used for systems with any number of channels since it can shut all channels off on command.

Figure 3 shows a six channel commutator which may be easily expanded. Data sampling may be done on any format which the user chooses. Sampling format is easily controlled by DTL or TTL logic design independent of the NH0019. Since each buffer-driver of the NH0019 has a dual input gate, all channel blanking is readily achieved. If desired, the format shown in Figure 3 may be



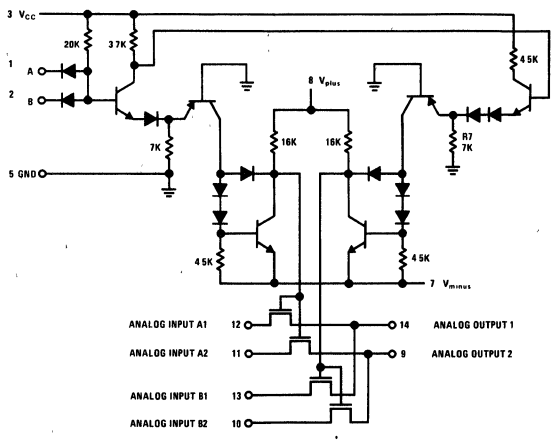
(a) MOS Configuration

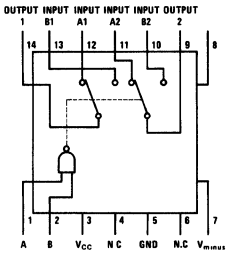
(b) Schematic Configuration

FIGURE 1. MM450/MM550 MOS Dual Differential Switch

modified so as to use the NH0019 logic inputs as binary gates which can reduce the command logic complexity if the blanking function is not required.

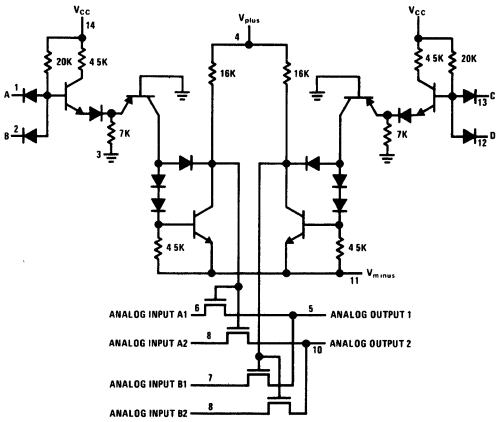
Since the multiplexed information is in differential form, common mode noise is greatly reduced. Also, the MOS gate drive spiking is drastically reduced because of the differential channel configuration. Demultiplexing may be accomplished by using a circuit identical to the multiplexer because the MOS device is a true bilateral switch. In hard-wired systems where the multiplex "outputs" are electrically connected as in Figure 4, the signal may be transmitted in either direction. For non-hardwired systems, the modulation-demodulation sequence is still bilateral, but provisions must be made for transmit/receive function control.

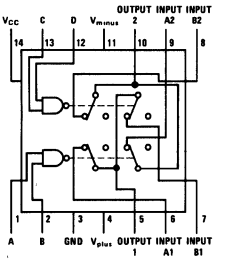




Note: All inputs "HIGH."

(a) NH0014





Note: All inputs "HIGH."

(b) NH0019

FIGURE 2. NH0014 and NH0019 DTL-TTL Compatible MOS Analog Switches

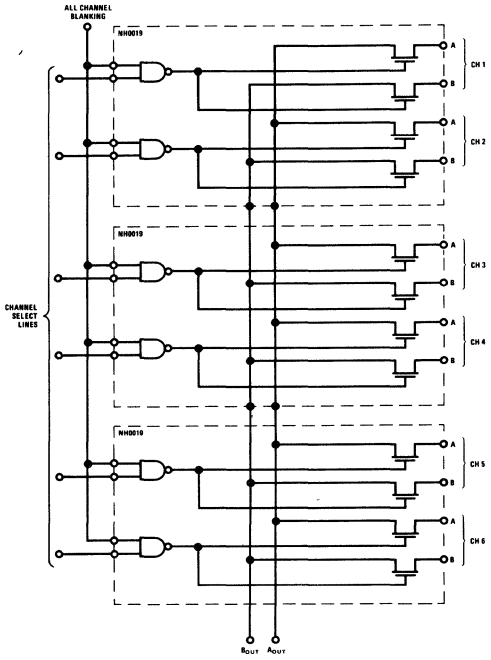


FIGURE 3. Differential Signal Commutator–NH0019

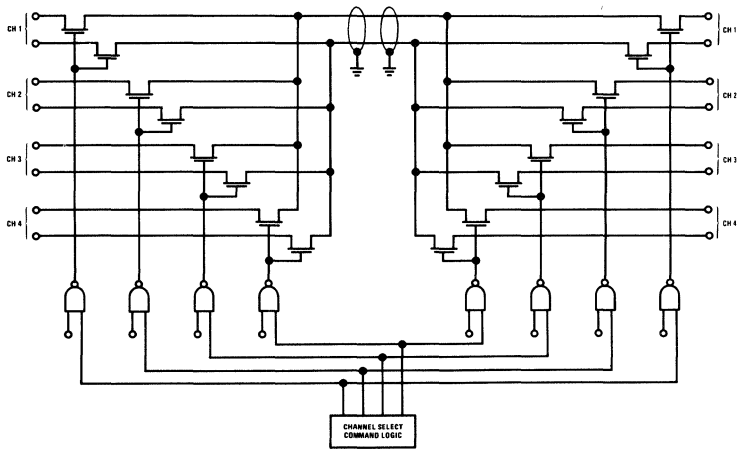


FIGURE 4. Commutation-Modulation and Demodulation

USAGE IN LINEAR AMPLIFIER CIRCUITS

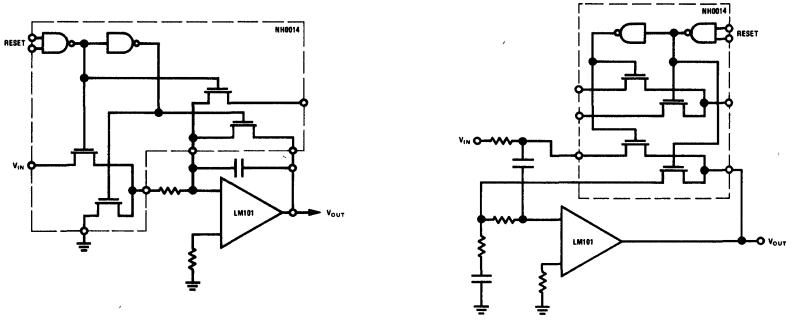
The NH0014 and NH0019 devices are useful for switching functions in linear circuit applications because of high off/on resistance ratio and ease of switching control using logic elements. Sample and hold circuits, integrator reset switching, and reset stabilized amplifiers are a few examples (Figure 5). More detailed information on this type of circuitry is available in National Semiconductor applications notes AN-4, AN-5, AN-20, and AN-29[4-7].

An obvious use of the NH0014 and NH0019 are in chopper stabilized amplifiers (Figure 6). One of the better forms of chopper stabilized amplifiers is the series shunt chopper with sample and hold type of output. The NH0014 does a good job at this because it contains the complete set of switches plus proper drive for the switches. The NH0014 can greatly reduce component count for chopper stabilized amplifiers.

DOUBLE SIDEBAND MODULATOR

The NH0019 can be used as a double sideband modulator. In modulator applications, the NH0019 functions as a DPDT switch which alternately reverses the polarity of the modulating signal at the chopper frequency. MOS switches work quite well at this application because of zero offset voltage and large signal handling ability.

In order to build a double sideband balanced modulator[8,9], one of the two modulating inputs must be applied as a balanced input. For the circuit shown in Figure 7, an LM102 and LM107 were used for an audio phase splitter.



(a) Integrator

(b) Reset Stabilized Amplifier

FIGURE 5. Switching Applications With Linear Circuits

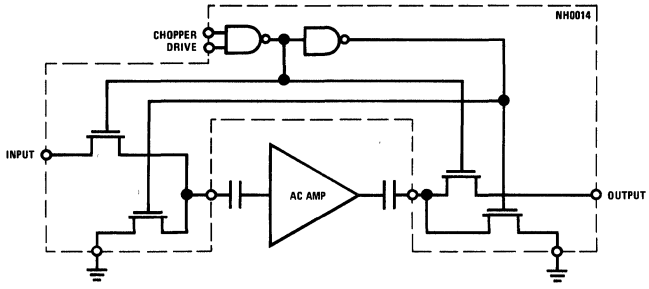


FIGURE 6. Series-Shunt Chopper Stabilized Amplifier

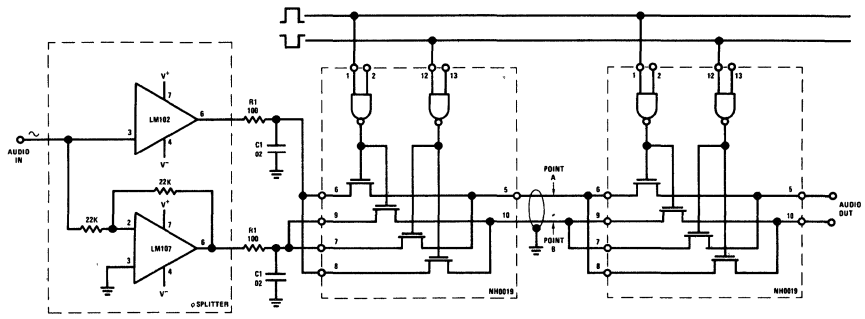


FIGURE 7. Double Sideband Modulator-Demodulator

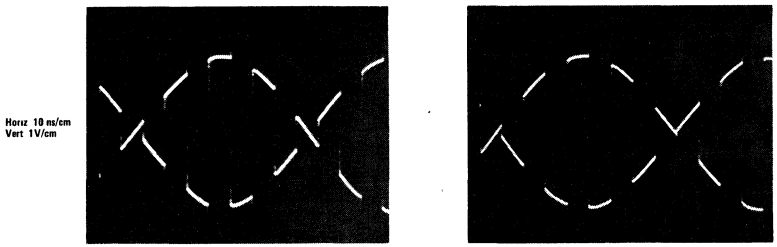
Both point A and point B in Figure 7 are DSB modulated outputs; so, technically, you could get by with only one. The waveform at point A is illustrated in Figure 8a for a carrier frequency of 100 kHz and an audio frequency of 12.5 kHz. Point B is equal and out of phase.

One type of spurious response encountered with MOS switching devices is output spikes caused by a charge being dumped into the channel by the gate drive through gate-channel capacitance. By adding C1, part of the charge can be absorbed, thus reducing the voltage amplitude of the spikes. The R1C1 combination has its 3 dB point at about 80 kc, so output from the phase splitter was not attenuated in the audio range.

The astute observer will notice switching transients on the waveform in Figure 8a. By taking the output in differential form at points A and B, these transients are greatly reduced because the desired signals are equal but of opposite polarity, while the switching transients are an "in phase" or "common mode" error.

To better illustrate the improvement by using a balanced output, the audio signal was reduced to zero volts and the points A, B, and A-B were measured as shown in Figure 9. The improvement operating in the differential mode is obvious.

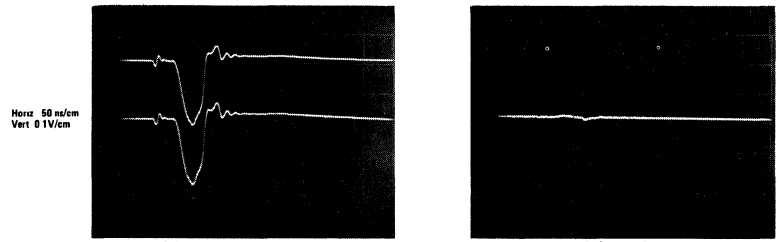
The circuit drive requirements for Figure 7 may be simplified by using the NH0014 since it provides an inverting function internally. Only one phase of toggle drive to the NH0014 is required.



(a) V_a (b) V_a-V_b

FIGURE 8. Double Sideband Signal

The modulation will be distorted more due to the phase lag created by the internal inverter of the NH0014. Figure 10a shows the switching performance of the NH0019 while Figure 10b shows the switching performance of the NH0014. In applications which do not require high carrier frequencies, the NH0014 is adequate, but for carrier frequencies above 100 kHz, the NH0019 provides improved performance because of its symmetrical switching behavior.



(a) Upper Trace - V_a
Lower Trace - V_b

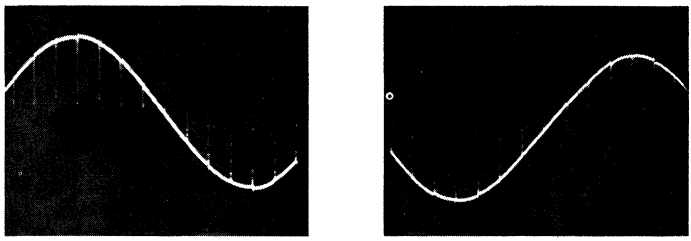
(b) V_a-V_b

FIGURE 9. MOS Switching Transients

(a) NH0019 50 ns/cm

(b) NH0014 50 ns/cm

FIGURE 10. Channel Switching–NH0019 vs NH0014



(a) Single Ended Output

(b) Differential Output

FIGURE 11. Demodulator Recovered Output

DOUBLE SIDEBAND DEMODULATOR

The major requirement of double sideband signal demodulation is proper carrier reinsertion. For maximum output, the carrier must be reinserted exactly in phase or exactly 180° out of phase with respect to the signal. Any departure from this optimum phase relationship will reduce the recovered signal amplitude. By applying the double sideband signal to a second NH0019, as shown in Figure 7, the original modulating waveform may be recovered, along with some switching transients (Figure 11).

These switching transients may be filtered out quite easily. It is, however, instructive to compare the recovered audio signal with the original. The modulating signal had less than 0.1% distortion at 1 kHz. Figure 12 shows the distortion of the recovered signal vs. signal amplitude.

Carrier frequency was 100 Hz for the upper curve and 10 kHz for the lower. These curves indicate that most of the distortion is due to switching transients, especially at low modulation levels. Output filtering will significantly reduce the recovered signal distortion.

Figure 13 emphasizes the affect that switching transients have on harmonic distortion. At carrier frequencies below 10 kHz, the RMS value of the transients is reduced to a point where distortion of the MOS switches themselves can be seen.

The NH0014 and NH0019 data sheet suggests a V plus supply value of 10 volts and a V minus supply value of −20 volts. However, switching transients may be reduced by using different power supply voltages. Figure 14 and Figure 15 show what happens to harmonic distortion caused by spiking versus power supply level. Figure 14 is plotted for V minus with V plus at 10 volts. Figure 15 shows what happens as V plus is varied. All of the previous data was taken at V plus at 14 volts and V minus at −12 volts.

AM-FM DEMODULATOR

Although an AM-FM demodulator was not physically constructed, the previously discussed "double sideband demodulator" performance implies that a very interesting phase detector can be built. The interesting features of this type of a detector are large dynamic range, recovery of both in-phase (amplitude modulated) and quadrature-phase (frequency modulated) signals plus the feasibility of not using any inductors for tuning.

Figure 16 shows the proposed circuit block diagram which uses a phase-locked loop for phase reference signal. The voltage controlled oscillator (VCO) is operated at 4 f_o. Flip Flop #1 provides a two phase output which is fed into FF #2 and FF #3. The outputs of FF #2 and FF #3 are exactly 90° out of phase regardless of the frequency of the VCO. This kind of performance is awfully hard to achieve using tuned circuits. For a 455 kHz detector, the VCO would operate at 1820 kHz. TTL flip flops will operate quite nicely at that frequency and should hold phase shift errors to practically zero. The LM107 provides DC gain to close the phase-locked loop, it forces the VCO to a frequency and phase angle which causes the "FM out" port to zero volts DC; this port is then operating exactly in quadrature with the applied signal. This part of the detector is then insensitive to amplitude modulation and sensitive to frequency modulation. Since the AM detector portion is operating exactly 90° out of phase with the FM portion, its output is insensitive to FM and sensitive to AM.

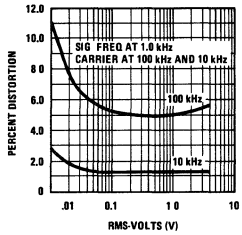
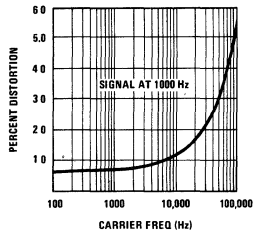


FIGURE 12. Recovered Signal Harmonic Distortion vs Audio Modulation Level



There was little significant difference in distortion at signal amplitudes of 3.0V, 1.0V, 0.3V, 0.1V RMS

FIGURE 13. Recovered Signal Harmonic Distortion vs Carrier Frequency

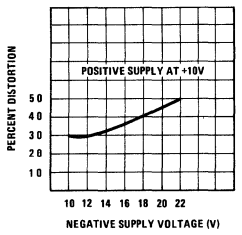


FIGURE 14. Harmonic Distortion vs Negative Power Supply Voltage

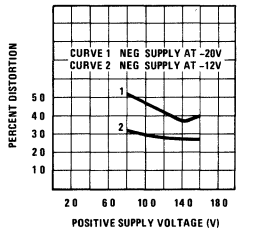


FIGURE 15. Harmonic Distortion vs Positive Supply Voltage

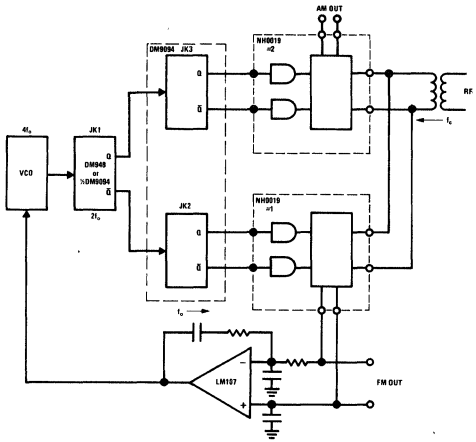


FIGURE 16. AM-FM Demodulator

CONCLUSION

The most obvious use of the NH0014 and NH0019 is in commutator applications, and it indeed is a very useful device for that purpose. The use of these switches in linear circuit applications is also very attractive because of DTL-TTL control compatibility. There are many more uses of these switches possible than the few examples described here.

The unusual application of these devices as suppressed carrier double-sideband modulators and demodulators suggests applications in servo systems and even communications systems due to their high speed operation. The final circuit suggestion, a phase-locked loop AM-FM demodulator without tuned circuits should be very useful in communications systems. The NH0019 will operate quite well at an IF frequency of 455 kHz or less.

These basic capabilities of the MOS dual differential switch should encourage much greater usage of this type of device in new product designs.

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PIN DIODE DRIVERS

INTRODUCTION

The DH0035/DH0035C is a TTL/DTL compatible, DC coupled, high speed PIN diode driver. It is capable of delivering peak currents in excess of one ampere at speeds up to 10 MHz. This article demonstrates how the DH0035 may be applied to driving PIN diodes and comparable loads which require high peak currents at high repetition rates. The salient characteristics of the device are summarized in Table I.

PARAMETER	CONDITIONS	VALUE
Differential Supply Voltage ($V^+ - V^-$)		30V Max.
Output Current		1000 mA
Maximum Power		1.5W
t_{delay}	PRF = 5.0 MHz	10 ns
t_{rise}	$V^+ - V^- = 20V$ 10% to 90%	15 ns
t_{fall}	$V^+ - V^- = 20V$ 90% to 10%	10 ns

Table I DH0035 Characteristics

PIN DIODE SWITCHING REQUIREMENTS

Figure 1 shows a simplified schematic of a PIN diode switch. Typically, the PIN diode is used in RF through microwave frequency modulators and switches. Since the diode is in shunt with the RF path, the RF signal is attenuated when the diode is forward biased ("ON"), and is passed unattenuated when the diode is reversed biased ("OFF"). There are essentially two considerations of interest in the "ON" condition. First, the amount of "ON" control current must be sufficient such that RF signal current will not significantly modulate the "ON" impedance of the diode. Secondly, the time required to achieve the "ON" condition must be minimized.

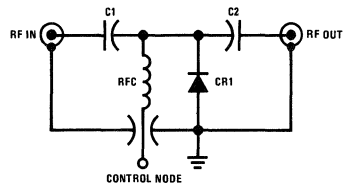

FIGURE 1. Simplified PIN Diode Switch

The charge control model of a diode[1,2] leads to the charge continuity equation given in equation (1).

$$i = \frac{dQ}{dt} + \frac{Q}{\tau} \qquad (1)$$

where: Q = charge due excess minority carriers
τ = mean life time of the minority carriers

Equation (1) implies a circuit model shown in Figure 2. Under steady conditions $\frac{dQ}{dt} = 0$, hence:

$$I_{DC} = \frac{Q}{\tau} \text{ or } Q = I_{DC}\tau \qquad (2)$$

where: I = steady state "ON" current.

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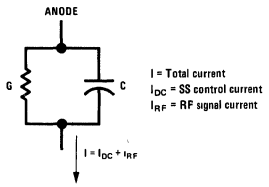

FIGURE 2. Circuit Model for PIN Switch

The conductance is proportional to the current, I; hence, in order to minimize modulation due to the RF signal, $I_{DC} >> i_{RF}$. Typical values for I_{DC} range from 50 mA to 200 mA depending on PIN diode type, and the amount of modulation that can be tolerated.

The time response of the excess charge, Q, may be evaluated by taking the Laplace transform of equation (1) and solving for Q:

$$Q(s) = \frac{\tau I(s)}{1 + s\tau} \qquad (3)$$

Solving equation (3) for Q(t) yields:

$$Q(t) = L^{-1}[Q(s)] = I\tau(1 - \epsilon^{-t/\tau}) \qquad (4)$$

The time response of Q is shown in Figure 3a. As can be seen, several carrier lifetimes are required to achieve the steady state "ON" condition ($Q = I_{DC} \cdot \tau$).

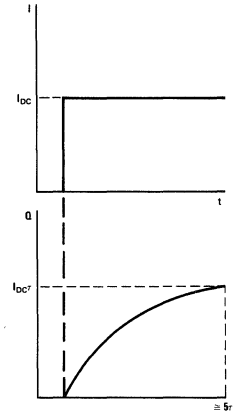

FIGURE 3a.

The time response of the charge, hence the time for the diode to achieve the "ON" state could be shortened by applying a current spike, Ipk, to the diode and then dropping the current to the steady state value, I_{DC}, as shown in Figure 3b. The optimum response would be dictated by:

$$(Ipk)(t) = \tau \cdot I_{DC} \qquad (5)$$

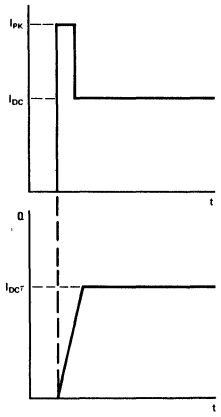

FIGURE 3b.

The turn off requirements for the PIN diode are quite similar to the turn on, except that in the "OFF" condition, the steady current drops to the diode's reverse leakage current.

A charge, $I_{DC} \cdot \tau$, was stored in the diode in the "ON" condition and in order to achieve the "OFF" state this charge must be removed. Again, in order to remove the charge rapidly, a large peak current (in the opposite direction) must be applied to the PIN diode:

$$-Ipk >> \frac{Q}{\tau} \qquad (6)$$

It is interesting to note an implication of equation (5). If the peak turn on current were maintained for a period of time, say equal to τ, then the diode would acquire an excess charge equal to Ipk·T. This same charge must be removed at turn off, instead of a charge $I_{DC} \cdot \tau$, resulting in a considerably slower turn off. Accordingly, control of the width of turn on current peak is critical in achieving rapid turn off.

APPLICATION OF THE DH0035 AS A PIN DIODE DRIVER

The DH0035 is specifically designed to provide both the current levels and timing intervals required to optimally drive PIN diode switches. Its

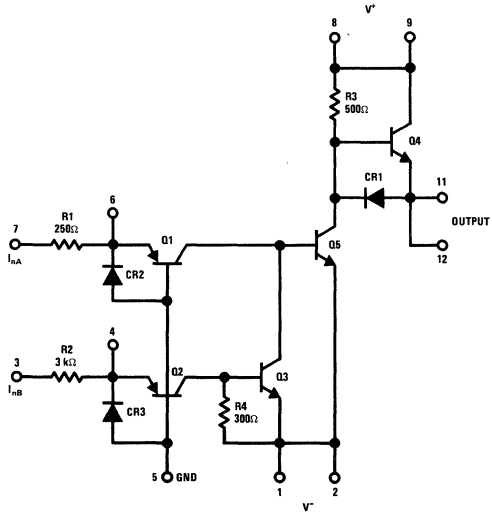

FIGURE 4. DH0035 Schematic Diagram

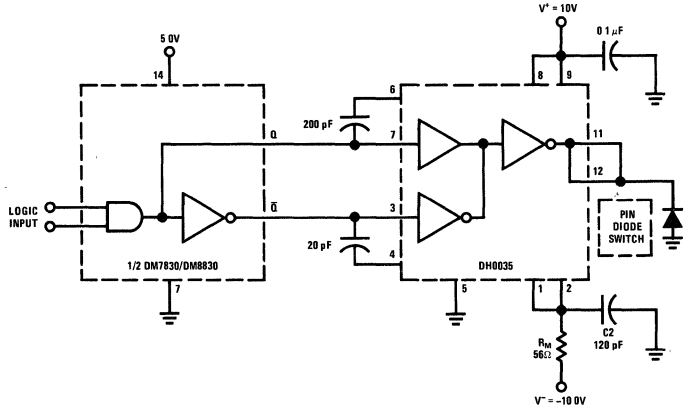

FIGURE 5. Anode Grounded Driver

schematic is shown in Figure 4. The device utilizes a complementary TTL input buffer such as the DM7830/DM8830 or DM5440/DM7440 for its input signals.

Two configurations of PIN diode switch are possible: cathode grounded and anode grounded. The design procedures for the two configurations will be considered separately.

ANODE GROUND DESIGN

Selection of power supply voltages is the first consideration. Table I reveals that the DH0035 can withstand a total of 30V differentially. The supply voltage may be divided symmetrically at ±15V, for example. Or asymmetrically at +20V and −10V. The PIN diode driver shown in Figure 5, uses ±10V supplies.

When the Q output of the DM8830 goes high a transient current of approximately 50 mA is applied to the emitter of Q_1 and in turn to the base of Q_5.

Q_5 has an h_{fe} = 20, and the collector current is h_{fe} x 50 or 1000 mA. This peak current, for the most part, is delivered to the PIN diode turning it "ON" (RF is "OFF").

Ipk flows until C_2 is nearly charged. This time is given by:

$$t = \frac{C2\,\Delta V}{Ipk} \qquad (7)$$

where: ΔV = the change in voltage across C_2.

Prior to Q_5's turn on, C_2 was charged to the minus supply voltage of −10V. C_2's voltage will rise to within two diode drops plus a V_{sat} of ground:

$$V = |V^-| - Vf(\text{PIN Diode}) - Vf_{CR1} - V_{sat_{Q5}} \qquad (8)$$

for V^- = −10V, ΔV = 8V.

Once C_2 is charged, the current will drop to the steady state value, I_{DC}, which is given by:

$$I_{DC} = \frac{V}{R_M} - \frac{V^+}{R_3} - \frac{V_{CC}}{R_1} \qquad (9)$$

where: V_{CC} = 5.0V
R_1 = 250Ω
R_3 = 500Ω

$$\therefore R_M = \frac{(R_3)\,(\Delta V)\,(R_1)}{R_1 V+ + I_{DC}R_3R_1 + V_{CC}R_3} \qquad (9a)$$

For the driver of Figure 5, and I_{DC} = 100 mA, R_M is 56 ohms (nearest standard value).

Returning to equation (7) and combining it with equation (5) we obtain:

$$t = \frac{\tau I_{DC}}{Ipk} = \frac{C_2 V}{Ipk} \qquad (10)$$

Solving equation (10) for C_2 gives:

$$C_2 = \frac{I_{DC}\tau}{V} \qquad (11)$$

For τ = 10 ns, C_2 = 120 pF.

One last consideration should be made with the diode in the "ON" state. The power dissipated by the DH0035 is limited to 1.5W (see Table I). The DH0035 dissipates the maximum power with Q_5 "ON". With Q_5 "OFF", neglible power is dissipated by the device. Power dissipation is given by:

$$P\,\text{diss} \cong \left[I_{DC}\,(|V^-| - \Delta V) + \frac{(V^+ - V^-)^2}{R3}\right] \times (\text{D.C.}) \leq P_{max} \qquad (12)$$

where: D.C. = Duty Cycle =

$$\frac{(\text{"ON" time})}{(\text{"ON" time} + \text{"OFF" time})}$$

Pmax = 1.5W

In terms of I_{DC}:

$$I_{DC} \leq \frac{\left[\frac{(Pmax)}{(D.C.)} - \frac{(V^+ - V^-)^2}{500}\right]}{|V^-| - \Delta V} \qquad (12a)$$

For the circuit of Figure 5 and a 50% duty cycle, P diss = 0.5W.

Turn-off of the PIN diode begins when the Q output of the DM8830 returns to logic "0" and the $\overline{Q}$ output goes to logic "1". Q_2 turns "ON", and in turn, causes Q_3 to saturate. Simultaneously, Q_1 is turned "OFF" stopping the base drive to Q_5. Q_3 absorbs the stored base charge of Q_5 facilitating its rapid turn-off. As Q_5's collector begins to rise, Q_4 turns "ON". At this instant, the PIN diode is still in conduction and the emitter of Q_4 is held at approximately −0.7V. The instantaneous current available to clear stored charge out of the PIN diode is:

$$Ipk = \frac{V^+ - V_{BE\,Q4} + V_{f(PIN)}}{\frac{R_3}{h_{fe}+1}} \cong \frac{(h_{fe}+1)\,(V^+)}{R_3} \qquad (13)$$

where:

h_{fe} + 1 = current gain of Q_4 = 20

$V_{BE\,Q4}$ = base-emitter drop of Q_4 = 0.7V

$V_{f(PIN)}$ = forward drop of the PIN diode = 0.7V

For typical values given, Ipk = 400 mA. Increasing V^+ above 10V will improve turn-off time of the diode, but at the expense of power dissipation in the DH0035. Once turn-off of the diode has been achieved, the DH0035 output current drops to the reverse leakage of the PIN diode. The attendant power dissipation is reduced to about 35 mW.

CATHODE GROUND DESIGN

Figure 6 shows the DH0035 driving a cathode grounded PIN diode switch. The peak turn-on current is given by:

$$Ipk \cong \frac{(V^+ - V^-)\,(h_{fe}+1)}{R_3} \qquad (14)$$

= 800 mA for the values shown.

The steady state current, I_{DC}, is set by Rp and is given by:

$$I_{DC} = \frac{V^+ - 2V_{BE}}{\frac{R_3}{h_{fe}+1} + R_P} \qquad (15)$$

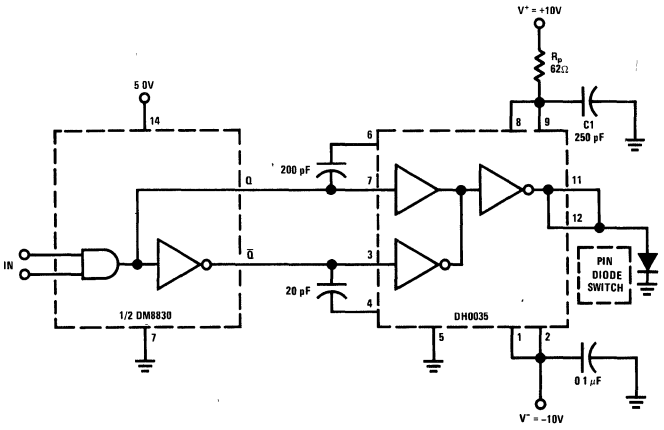

FIGURE 6. Cathode Grounded Design

where: $2V_{BE}$ = forward drop of Q_4 base emitter junction plus V_f of the PIN diode = 1.4V.

In terms of Rp, equation (15) becomes:

$$R_P = \frac{(h_{fe}+1)\,(V^+ - 2V_{BE}) - I_{DC}\,R_3}{(h_{fe}+1)\,I_{DC}} \qquad (15a)$$

For the circuit of Figure 6, and I_{DC} = 100 mA, Rp is 62 ohms (nearest standard value).

It now remains to select the value of C_1. To do this, the change in voltage across C_1 must be evaluated. In the "ON" state, the voltage across C_1, Vc, is given by:

$$(Vc)_{ON} = \frac{V^+R_3 + Rp(h_{fe}+1)\,(2V_{BE})}{R_3 + (h_{fe}+1)\,Rp} \qquad (16)$$

For the values indicated above, $(Vc)_{ON}$ = 3.8V.

In the "OFF" state, Vc is given by:

$$(Vc)_{OFF} = \frac{V^+R_3 - |V^-|Rp}{Rp + R_3} \qquad (17)$$

= 8.0V for the circuit of Figure 6.

Hence, the change in voltage across C_1 is:

$$\begin{aligned} V &= (Vc)_{OFF} - (Vc)_{ON} \qquad (18)\\ &= 8.0 - 3.8\\ &= 4.2V \end{aligned}$$

The value of C_4 is given, as before, by equation (11):

$$C_1 = \frac{I_{DC}\tau}{V^-} \qquad (19)$$

For a diode with τ = 10 ns and I_{DC} = 100 mA, C_1 = 250 pF.

Again, the power dissipated by the DH0035 must be considered. In the "OFF" state, the power dissipation is given by:

$$P_{OFF} = \left[\frac{(V^+ - V^-)^2}{R_3}\right](D.C.) \qquad (20)$$

where: D.C. = duty cycle =

$$\frac{\text{"OFF" time}}{\text{"OFF" time} + \text{"ON" time}}$$

The "ON" power dissipation is given by:

$$P_{ON} = \left[\frac{(Vc)_{ON}^2}{R_3} + I_{DC} \times (Vc)_{ON}\right](1 - D.C.) \qquad (21)$$

where: $(Vc)_{ON}$ is defined by equation (16).

Total power dissipated by the DH0035 is simply $P_{ON} + P_{OFF}$. For a 50% duty cycle and the circuit of Figure 6, P diss = 616 mW.

The peak turn-off current is, as indicated earlier, equal to 50 mA x h_{fe} which is about 1000 mA. Once the excess stored charge is removed, the current through Q_5 drops to the diodes leakage current. Reverse bias across the diode = $V^- - V_{sat} \cong -10V$ for the circuit of Figure 6.

REPETITION RATE CONSIDERATIONS

Although ignored until now, the PRF, in particular, the "OFF" time of the PIN diode is important in selection of C_2, R_M, and C_1, Rp. The capacitors must recharge completely during the diode "OFF" time. In short:

$$4\,R_MC_2 \leq t_{OFF} \qquad (22a)$$

$$4\,RpC_1 \leq t_{OFF} \qquad (22b)$$

10

FIGURE 7. RF Turn-On (10 ns/cm)

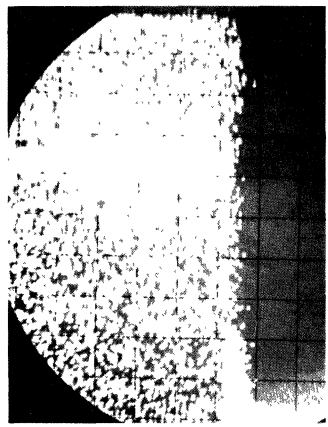

FIGURE 8. RF Turn-Off (10 ns/cm)

CONCLUSION

The circuit of Figure 6 was breadboarded and tested in conjunction with a Hewlett-Packard 33622A PIN diode.

I_{DC} was set at 100 mA, V^+ = 10.0V, V^- = 10V. Input signal to the DM8830 was a 5V peak, 100 kHz, 5 μs wide pulse train. RF turn-on was accomplished in 10-12 ns while turn-off took approximately 5 ns, as shown in Figures 7 and 8.

In practice, adjustment C_2 (C_1) may be required to accommodate the particular PIN diode minority carrier life time.

SUMMARY

A unique circuit utilized in the driving of PIN diodes has been presented. Further a technique has been demonstrated which enable the designer to tailor the DH0035 driver to the PIN diode application.

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HIGH SPEED ANALOG SWITCHES

SUMMARY

In the past, many factors combined to make precision, high speed analog switching circuits complex and expensive, if not impossible. A unique monolithic J-FET family opens new analog switching applications which require high toggle rates, high frequency signal handling ability, and high level analog signals with broad dynamic range.

Called the AM1000, AM1001 and AM1002 analog switches, these devices were developed specifically for high speed analog switching applications. The AM1000 series overcomes the problem of slow switching speed normally associated with junction FET analog switches. While MOS analog switches are noted for their high speed, they have the peculiar problem of their ON resistance being modulated by the analog signal level. The AM1000 series eliminates this problem too.

National's AM1000 series analog switches are simple N-channel monolithic integrated circuit J-FETs. They are packaged in TO-72 (4-pin TO-18) headers to reduce circuit board space and yet retain the advantages of a hermetically sealed package.

WHAT IS AN ANALOG SIGNAL?

An analog signal is an electrical voltage (or current) whose level is an analog of certain information. This information can be an electrical level itself, a voice signal, an electrical analog of a pressure, temperature, position, etc., or any other data source. The analog information may also be preconditioned by logarithmic compression or expansion, or other desired "distortion." If the analog information does not vary quickly with time and if many analog signals have to be handled in a system, the analog information may be sampled periodically rather than monitored continuously. Sampled data systems can dramatically reduce cost and weight by proper utilization of available information channel bandwidth where the cost of additional data channels becomes expensive.

The telephone companies are probably the most adept at signal multiplexing, but other applications are beginning to appear. Modern aircraft are using multiplexing to reduce weight in wire harnesses. Any applications requiring long multiconductor cable runs are prime targets for economic use of analog signal multiplexing.

TIME DOMAIN MULTIPLEXING

There are two basic types of multiplexing: frequency domain multiplexing and time domain multiplexing. Frequency domain multiplexing is common in RF communications, it uses a number of subcarriers on a data channel, each subcarrier being modulated in some manner. An example would be FM radio standard broadcast which has home stereo multiplex information (a suppressed carrier double sideband subcarrier) and the SCA commercial "background music" multiplex information (an FM modulated subcarrier). When the number of data channels becomes great, frequency domain multiplexing becomes difficult to implement.

In time domain multiplexing, a certain time slot is allowed for sampling of a particular data line. Thus, if you sample some analog information during a 10 μs time slot at a 10 kHz rate, you have time "left over" to sample nine other signals at 10 μs intervals at a 10 kHz rate. If you can improve the analog switch device to execute a suitable sample in only 1 μs, you have made a tenfold improvement and you have the choice of increasing system channel capability to 100 channels (with no change in analog signal bandwidth), increasing analog signal frequency bandwidth by 10 times (with no increase in channels), or a compromise between increasing signal bandwidth and increasing the number of data channels. This is what the AM1000 family of analog switches is all about; they allow shorter sampling times for a given signal accuracy.

WHAT MAKES A GOOD ANALOG SWITCH?

There are five principle parameters which determine how good an analog switch is:

ON resistance
ON resistance modulation
OFF resistance
Offset voltage
Commutation rate

There are other considerations which may also be significant for special cases, but these five will almost always have significant bearing on a system design. For most applications, there are two devices which are the most popular—MOS switches and J-FET switches. Relays normally would be a good choice but they won't toggle very fast. In general, the MOS switches have had a speed advantage, and ease of fabrication advantage, whereas the J-FET switches have an advantage of lower ON resistance, no ON resistance modulation, higher voltage capability.[4,5,6] The AM1000 family of analog switches have all of the advantages of the J-FET plus high speed which makes it superior to any MOS switch in a precision system.

WHAT MAKES THE AM1000 FAST?

Figure 1 shows a typical J-FET circuit used in analog switching. Diode D_1 allows the gate drive signal to drive the gate negative thus turning off the J-FET switch. When the gate drive signal goes positive, diode D_1 decouples the drive from the gate and resistor R_g discharges the gate-source capacitance. R_g must be large so it doesn't load the analog signal, typical values for R_g are 100 kΩ and up; thus the gate capacitance—R_g time constant is large which precludes high switching rates. If C_{iss} of the J-FET is 15 pF nominal and R_g is 100 kΩ, the time constant is 1.5 μs thus making megacycle toggle rates impossible.

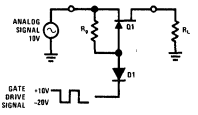

FIGURE 1. Typical J-FET Analog Switch

The AM1000 consists of three J-FETs. One large and two small ones. The large one acts as the analog signal pass transistor. The two smaller FETs act as a turn-on circuit which reduces switching transients.

The pinchoff voltage of all these FETs are almost identical and are all less than 10V. In Figure 3 (ignoring diode drops), the gates of all three FETs are at -20V and the AM1000 is turned off. There is at least -10V from gate to source of Q_1 so it is pinched off and leakage from input to output is in the pA range. Q_2 has -10V from gate to source so it is also pinched off and its current which shunts the input signal is in the pA range.

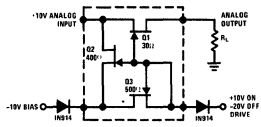

FIGURE 2. AM1000 Circuit

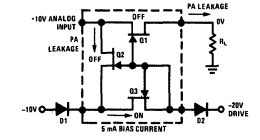

FIGURE 3. AM1000 Turned Off

Q_3 is operated at 0V gate-source so it draws saturation current, I_{DSS}. The bias supply for D_1 must be 10V more positive than the negative drive signal.

During turn-on, the drive signal ideally makes a step function change from -20V to +10V thus turning D_2 off. The gates of Q_1, Q_2 and Q_3 are then driven positive by the saturation current of Q_3 through diode D_1. The rate that this voltage slews is dependent on gate capacitance and I_{DSS} of Q_3. $C_{iss(off)}$ of the AM1000 is about 10 pF so the voltage slews at:

$$\frac{dv}{dt} = \frac{I_{DSS}}{C_{iss}} = \frac{5 \times 10^{-3}}{10^{-11}} = 5 \times 10^{8}\ \text{V/sec}$$

Within 5V of rise (about 10 ns), Q_2 begins to turn on and D_1 turns off. The remainder of the gate capacitance charge is discharged into the input (or source) of Q_1 via the ON resistance of Q_2 and Q_3. During this time interval the average series resistance of Q_2 and Q_3 is about 2 kΩ and the gate capacitance is changing from about 10 pF to about 25 pF. The approximate RC time constant is 20 pF and 2 kΩ, or 40 ns, depending on the level of the analog signal. Total turn on time is therefore about 50 ns. For a +10V analog signal, the correct analysis is a little more complex, but the AM1000 will turn on in about 70 ns for this circuit condition. The reason that the turn-on transient at R_L is drastically reduced is that the discharge path of gate capacitance does *not* flow through R_L. The small transient that may appear at R_L is due to the time that D_1 is on during turn-on.

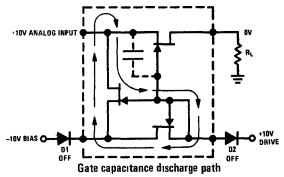

FIGURE 4. AM1000 Turning On

So, the AM1000 achieves its high switching speed because its R_g (see Figure 1) is very low during turn on, yet its R_g during the OFF state is in the G ohm range and thus doesn't load the signal.

TOGGLE RATE

The toggle rate (how fast the switch can be turned on and off) of an analog switch is not a simple straightforward parameter for a real system design. The reason is that most analog switches are specified at a ridiculously low impedance level; this is done in order to show the highest speed that the device can possibly go. This speed is not normally realistic for most systems designs. In order to demonstrate a realistic comparison, the AM1000 will be pitted against an MOS analog switch for a system with a ±10V analog signal swing.

TABLE 1: AM1000 – MOS Parameter Comparison

PARAMETER	AM1000	MOS ANALOG SWITCH
$R_{DS(on)}$ (Max)	30Ω	400Ω
$R_{DS(on)}$ (Min)	20Ω	150Ω
$R_{DS(on)}$ (Nom)	25Ω	275Ω
C_{iss} (Nom)	15 pF	7 pF
Breakdown Volts	40V	35V

$R_{DS(on)}$ and C_{iss} indicate the basic speed capability of the devices assuming low source and load impedance, here the AM1000 has a speed advantage of about 5:1 over the MOS switch.

The parameter that affects toggle rate the most, however is $R_{DS(on)}$ variation with analog signal level. At an analog signal of +10V, the MOS switch has an $R_{DS(on)}$ of 150Ω and for a -10V analog signal it has an on resistance of 400Ω. This variation of ON resistance is caused by the bulk gate to channel voltage modulating the ON resistance of the MOS switch.[5] Thus, the MOS switch has a design on resistance characteristic of 275Ω ±125Ω. The AM1000 has an $R_{DS(on)}$ of 25Ω ±5Ω and its resistance *does not* vary with analog signal level.

For a system of a given accuracy, the load impedance is determined by the variations expected in channel resistance. Assuming a system accuracy of ±0.5%, the AM1000 load resistance could be as low as 1 kΩ; the MOS switch load resistance would have to be 25 kΩ (±125Ω being 0.5% of 25 kΩ).

The capacitance of the AM1000 is about twice that of the MOS switch but the system load resistance is 25 times lower thus giving the AM1000 a toggle rate advantage of about 12 times over the MOS "high speed" analog switch. In order to graphically illustrate the superiority of the AM1000, two simple series switches were constructed; one with the MOS switch and one with an AM1000. The MOS analog switch was set up to sample a +10V DC signal, after being switched off, the output returns to ground level. The AM1000 was set up to sample a portion of the turn off transient of the MOS analog switch, each switch with a 0.5% system accuracy! Figure 5 shows the circuit used to obtain the oscillograph shown in Figure 6A.

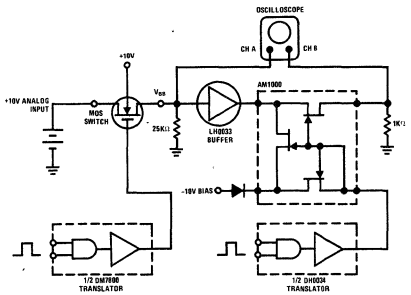

FIGURE 5. Analog Switch Comparison Circuit

A National LH0033 high speed buffer was used to sense the analog voltage at the load resistor of the MOS switch and drive the analog input of the AM1000. Figure 6A shows the oscillogram; the upper trace is the MOS switch turning off; its load voltage heading toward ground; the lower trace (oscilloscope vertical gain reduced slightly for photo clarity) shows the AM1000 sampling this switching transient. Figure 6B shows the timing pulses, the upper trace being the MOS drive timing and the lower is the AM1000 drive timing (positive indicating off for both devices). It is interesting to note that the turn-on delay or "aperture time" of the AM1000 is primarily caused by the DH0034 translator. Maximum specified turn on time is 100 ns and turn off time is specified at 100 ns for the AM1000. Figure 6 shows absolute superiority of the AM1000 in switching ability for a given system accuracy.

AM1000 DRIVE CIRCUITS

Normally, analog switches will be selected by some digital control means which will usually mean 0V add +5V power supply levels. The AM1000 needs a driver capable of handling the full analog voltage swing, plus 10V. Therefore a circuit known as an analog switch translator is normally requried. There are several types available. All of the following circuits feature "break before make" action which is desirable for multiplexing.

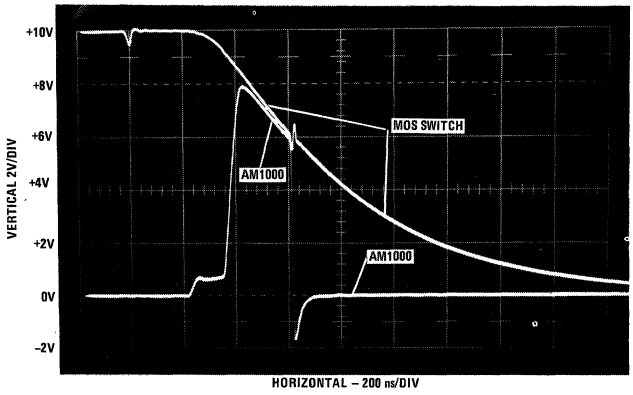

FIGURE 6A. AM1000 Sampling the Switching Transient of an MOS Analog Switch

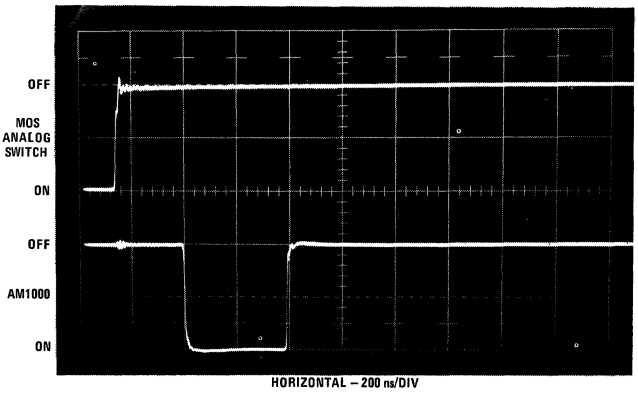

FIGURE 6B. Analog Switch Drive Timing

Analog switch translator-drivers fall into two basic categories. Those with pullups and those without. If the translator-driver has a pullup, such as the National DM7800, then a switching diode must be used to decouple the driver from the AM1000 when the driver goes positive.

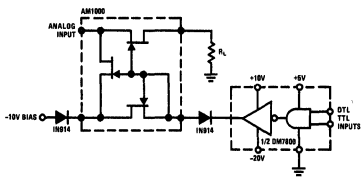

FIGURE 7. Translator-Driver with Voltage Pullup

The AM1000 does not require a driver with a pullup. Figure 8 shows the circuit for this configuration. Note that the driver decoupling diode is not required. This configuration eliminates one power supply but adds the capacitance of the driver which the AM1000 must charge. Usually this additional capacitance is not excessive.

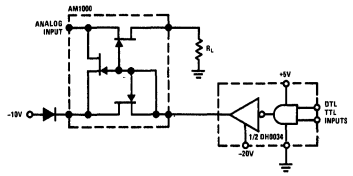

FIGURE 8. Translator-Driver without Pullup

In some systems, the cost of monolithic or hybrid drivers is not worth the space they save. Figure 9 shows a four channel driver using low cost discrete components. The ON channel is selected by binary coding and is DTL-TTL compatible. If A and B are "high" then drive is removed from Q_5 allowing channel 1 AM1001 to pull up and turn on. Q_6, Q_7 and Q_8 have drive applied which pull down on CH2, 3 and 4 thus turning them off. The voltages and devices indicated in Figure 9 allow ±15V analog signals to be handled.

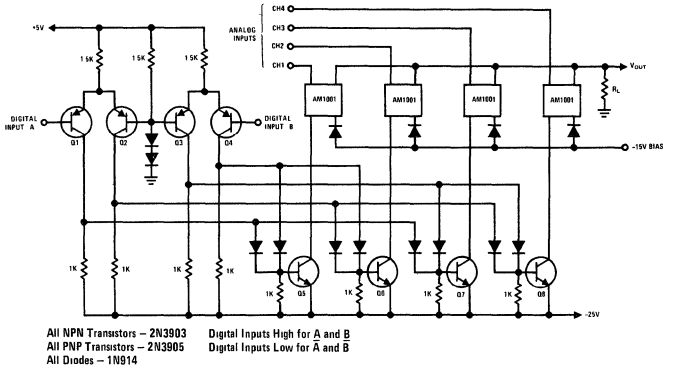

FIGURE 9. Binary Controlled Four Channel Multiplexer

CURRENT MODE MULTIPLEXING

So far, the discussion of multiplexing circuits has been confined to sampling various analog input voltages. Voltage mode analog switching allows maximum toggle rates but limited voltage range (±10V for AM1000, AM1002 and ±15V for AM1001).

If large analog voltages must be handled, current mode multiplexing must be used; toggle rate is reduced because accurate current-voltage converters are not as fast as non-inverting voltage amplifiers. Analog signal loading can also be a problem. Nevertheless current mode multiplexing allows sampling of very high analog voltages. This is accomplished by using scaling resistors and bound limit diodes at the input of the analog switch. Also, in this case the current to voltage converter should be the lowest impedance point in the system, so the AM1000 must be "turned around", so its analog "output" is used for the signal input and *vice versa.*

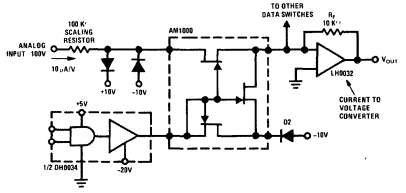

FIGURE 10. Current Mode Multiplexing

The system sensitivity in Figure 10 is determined by R_f in the current to voltage converter op amp. The LH0032 J-FET input op amp is selected because of its high slew rate and low input current.

The 10 kΩ feedback resistor shown results in 10V output for 1 mA input. Thus the scaling resistor at the input is selected for 1 mA for 100V input, or 10 μA/V. A 1000V analog signal would use a 1 MΩ scaling resistor. For lower voltage signals, the R_{on} of the AM1000 would have to be considered for precision systems. The bound limit diodes connected to +10V and -10V prevents excessive voltage from appearing at the AM1000. Input impedance to the current to voltage converter is R_f divided by the open loop op amp gain (5000 for the LH0032); the input impedance would be 2Ω in Figure 10.

OTHER APPLICATIONS

Analog computer circuits can make good use of analog switches. A few examples are sample and hold circuits, reset stabilized circuits, integrator reset switches, and chopper stabilized amplifiers.[4]

Video signal switching can be done with a minimum of switching transients. More unusual applications such as double sideband suppressed carrier modulators can be constructed plus double sideband suppressed carrier demodulation and FM quadrature demodulators.[5]

CONCLUSION

Where precision, high speed analog switching is required, the AM1000 series of analog switches "rewrites the book."

Time domain multiplexing can be dramatically improved in channel capability and/or analog signal bandwidth capability. Sample and hold circuits can be improved, chopper stabilized amplifiers can be improved and virtually any other circuit which requires precision, high level, high speed analog switching can be improved.

10

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APPLYING MODERN CLOCK DRIVERS TO MOS MEMORIES

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input wave forms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAM's (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, two new monolithic integrated circuit drivers, the MH0025 and MH0026 are selected as examples because of their low cost.

The MH0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage-gold doped process utilizing a collector sinker to minimize $V_{CE\ SAT}$.

The MH0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Of course each of us is careful of details but reminders such as "turn on the power supplies" or "don't reverse supply polarity" sometimes solve a not-so-obvious problem. This section is intended to review and answer design questions like "how much should I decouple supplies?"

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking

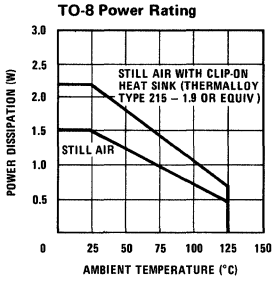
TABLE I. MH0025 Characteristics

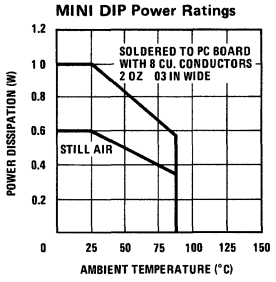
PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0022μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0001μF, R_0 = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	V^+ - 0 7	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	V^- + 1 0	V
On Supply Current (V^+)	I_{IN} = 10mA	17	mA

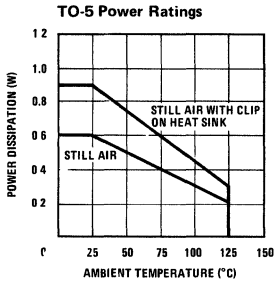
TABLE II. MH0026 Characteristics

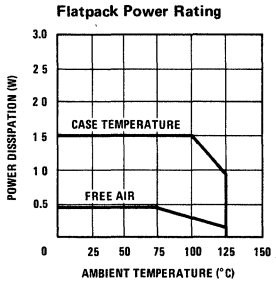
PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		7 5	ns
t_{OFF}	C_{IN} = 001μF, R_{IN} = 0Ω	7 5	ns
t_r	R_0 = 50Ω, C_L = 1000pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = -1mA	V^+ - 0 7	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	V^- + 0.5	V
On Supply Current (V^+)	I_{IN} = 10mA	28	mA

TABLE III. Package Power Ratings









required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

The TO-5 ("H") package is rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 900mW with clip on heat sink (derate at 6.0mW/°C above 25°C). This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on-heat sink increases driving capability by 50%.

The 8 pin ("N") molded mini-DIP is rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 1.0W soldered to P.C. board (derate at 6.6mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600mW when mounted in a socket and not one watt until it is soldered down.)

The TO-8 ("G") package is rated at 1.5W still air (derate at 10mW/°C above 25°C) and 2.3W with with clip on heat sink (Wakefield type 215-1.9 or equivalent-derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

The 14 pin cavity DIP is rated at 600mW free air. While some rate this package at 1W *case* temperature, National does not recommend its use for clock drivers. This is because from a user point of view, it is impossible to get more than 400 to 500mW rating under normal system conditions; i.e., there is no practical way to conduct heat away from the device other than air.

Other package types range in size and power handling capability. Most have the disadvantage of being in non-standard sizes and are difficult to mount in a system.

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

- Package and heat sink selection
- Average DC power, P_{DC}
- Average AC power, P_{AC}
- Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of DC power and AC power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \qquad (1)$$

Average DC power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \quad (2)$$

For most types of clock drivers, the first two terms are neglible (less than 10mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

Req = Equivalent device resistance in the "ON" state

$= V^+ - V^-/I_{S(ON)}$ (3)

DC = Duty Cycle

$$= \frac{\text{"ON" Time}}{\text{"ON" Time + "OFF" Time}}$$

For the MH0025, Req is typically 1kΩ while Req is typically 600Ω for the MH0026. Graphical solutions for P_{DC} appear in Figure 1. For example if $V^+ = +5V$, $V^- = -12V$, Req = 500Ω, and DC = 25%, then P_{DC} = 145mW. However, if the duty cycle was only 5%, P_{DC} = 29mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

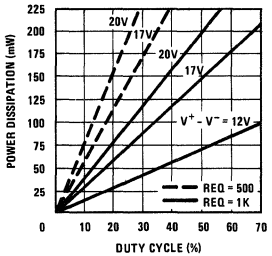


FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \quad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in Figure 2. Thus, any type of clock driver will dissipate internally 290mW per MHz per thousand pF of load. At 5MHz, this would be 1.5W for a 1000pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

Combining equations (1), (2), (3), and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

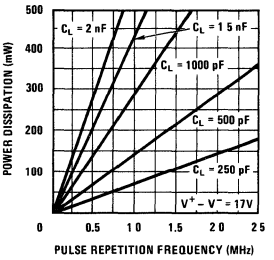


FIGURE 2. P_{AC} vs PRF

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \quad (5)$$

As an example, the MH0025CN can dissipate 630mW at $T_A = 70°C$ when soldered to a printed circuit board. Req is approximately equal to 1k. For $V^+ = 5V$, $V^- = -12V$, f = 1MHz, and DC = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(630 \times 10^{-3})}{(2)(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$$C_L \leq 880pF \text{ (each driver)}$$

A typical application might involve driving an MM5013 triple 64-bit shift register with the MH0025. Using the conditions above and the clock line capacitance of the MM5013 of 60pF, a single MH0025 can drive 880pF/60pF, or 14 MM5013's.

Similarly, the MH0026CG can dissipate 1.0W at 75°C. For $V^+ = 5V$, $V^- = -12V$, f = 2MHz, and DC = 20%, the maximum load capacitance which may be driven is:

$$C_L \leq 2 \times \frac{1}{10^6}\left[\frac{(1.0)}{(2)(17)^2} - \frac{0.2}{600}\right]$$

$$C_L \leq 700pF \text{ (each driver)}$$

10

TABLE IV. Worst Case Maximum Drive Capability for MH0026*

PACKAGE TYPE		TO-8 WITH HEAT SINK		TO-8 FREE AIR		MINI-DIP SOLDERED DOWN		TO-5 AND MINI-DIP FREE AIR	
Max Operating Frequency	Max. Ambient Temp. → / ↓ Duty Cycle	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C
100kHz	5%	30 k	24 k	19 k	15 k	13 k	10k	7 5k	5 8k
500kHz	10%	6.5k	5 1k	4 1k	3.2k	2 7k	2k	1 5k	1.1k
1MHz	20%	2 9k	2 2k	1 8k	1 4k	1 1k	840	600	430
2MHz	25%	1 4k	1 1k	850	650	550	400	280	190
5MHz	25%	620	470	380	290	240	170	120	80
10MHz	25%	280	220	170	130	110	79	–	–

*Note: Values in pF and assume both sides in use as non-overlaping 2 phase driver, each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$ For loads greater than 1200 pF, rise and fall times will be limited by output current

Returning to the MM5013 example, a single MH0026 can drive 700pF/60pF, or 11 5013's. Using the above equations, Table IV has been calculated for quick reference. In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, AC power (which depends on frequency, voltage across the device, and capacitive load) and DC power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (c) peak transient current available. Details of these are included in Appendixes I and II. Figures AI-3, AI-4, AII-2, and AIII-3 illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver, and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ peak}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this app. note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vise versa for fall times. Since MOS logic is inverted from normal TTL, "risetime" as used in this note is "voltage fall" and "fall time" is "voltage rise."

Power Supply Decoupling

Although power supply decoupling is a wide spread and accepted practice, the question often arises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in Figure 3. In this instance, a small damping resistor is inserted

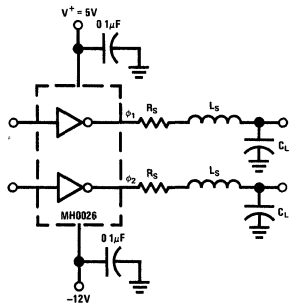


FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r\,(max)} = t_{f\,(max)} \leq 2.2\, R_S\, C_L \qquad (7)$$

One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2 f C_L$ and accordingly the resistor wattage rating will generally be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. Figure 4

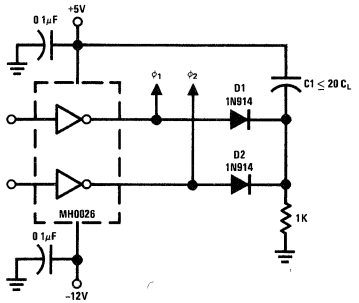


FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vise-versa) during the transition of ϕ_1 to MOS logic "1." The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Figure 5 illustrates the problem.

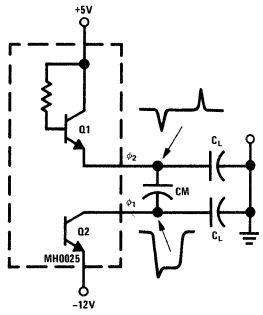


FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q_1 is "OFF" since only μA are drawn from the device. A simple method of minimizing cross-talk is shown in Figure 6.

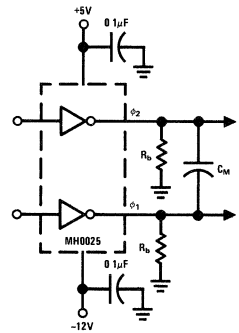


FIGURE 6. Use of Bleed Resistors to Minimize Clock-Line Crosstalk

Bleed resistors are connected between the clock driver and ground causing a current of a few mA to flow. The output impedance of the clock driver is reduced and the negative spike is thus minimized. Values for R_b depend on layout and the number of registers being driven. Typical values are between 1k and 10kΩ.

A major point should be emphasized with regard to clock-line crosstalk, i.e., even if the output impedance of the driver is zero ohms, self inductance between the clock driver and registers will cause the clock lines to spike on the transitions. Hence, the technique shown in Figure 6 works reasonably well for small systems.

For large systems, the circuit of Figure 7 is recommended. In this instance, Q_1 and Q_2 are turned "ON" just prior to the clocks transition to logic "1." The spike is therefore clamped by the $V_{CE\ (sat)}$ of Q_1 and Q_2. A key feature of the circuit is that the clamps are physically placed adjacent the register thus minimizing the inductance between the clamp and the load.

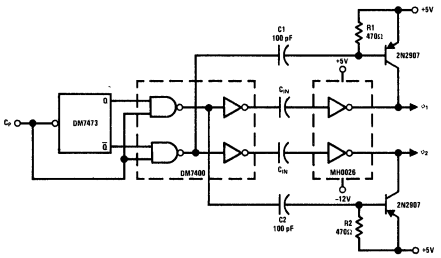


FIGURE 7. Cross Talk Minimization Circuit

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to DC level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the MH0025 and MH0026 utilize input capacitors when level shifting from TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of both the MH0025 and MH0026.

CONCLUSION

The practical aspects of driving MOS memories with new low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the MH0025 and MH0026 provide superior performance for most MOS input interface applications.

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1. Bert Mitchell, *"New MOS Clock Driver for MOS Shift Registers,"* National Semiconductor, AN-18, March 1969.

2. John Vennard, *"MOS Clock Drivers,"* National Semiconductor, MB-9, December 1969.

3. Dale Mrazek, *"MOS Delay Lines,"* National Semiconductor, AN-25, April 1969.

4. Dale Mrazek, *"MOS Clock Savers,"* National Semiconductor, MB-5.

5. Dale Mrazek, *"Silicon Disc's Challenge Magnetic Disc Memories,"* EDN/EEE Magazine, Sept. 1971.

6. Richard Percival, *"Dynamic MOS Shift Registers can also simulate Stack and Silo Memories,"* Electronics Magazine, Nov. 8, 1971.

7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, Aug. 1971.

8. Don Femling, *"Using the MM5704 Keyboard Interface in Keyboard Systems,"* National Semiconductor, AN-52.

APPENDIX I

MH0025 Circuit Operation

The schematic diagram of the MH0025 is shown in Figure AI-1. With the TTL driver in the logic "0" state Q_1 is "OFF" and Q_2 is "ON" and the output is at approximately one V_{BE} below the V^+ supply.

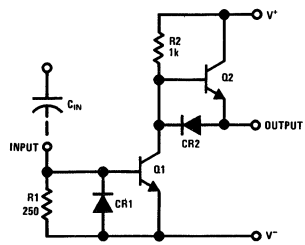


FIGURE AI-1. MH0026 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q_1, through C_{IN}, turning it "ON." As the collector of Q_1 goes negative, Q_2 turns OFF. Diode CR_2 assures turn-on of Q_1 prior to Q_2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q_2's base emitter junction.

The negative voltage transistion (to MOS logic "1") will be quite linear since the capacitive load will force Q_1 into its linear region until the load is discharged and Q_1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q_1 turns "OFF" and Q_2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the MH0025 is primarily a function of the AC load, C_L, the available input current and total voltage swing. As shown in Figure AI-2, the input current must

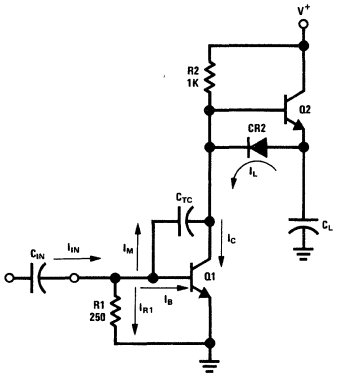


FIGURE AI-2. Rise Time Model for the MH0025

charge the Miller capacitance of Q_1, C_{TC}, as well as supply sufficient base drive to Q_1 to discharge C_L rapidly. By inspection:

$$I_{IN} = I_M + I_B + I_{R1} \qquad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M >> I_{R1} \text{ \& } I_B >> I_{R1}$$

$$I_B = I_{IN} - C_{TC}\frac{\Delta V}{\Delta t} \qquad \text{(AI-2)}$$

If the current through R_2 is ignored,

$$I_C = I_B h_{FEQ1} = I_L + I_M \qquad \text{(AI-3)}$$

where:

$$I_L = C_L \frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, AI-3 yields:

$$\frac{\Delta V}{\Delta t}\left[C_L + C_{TC}(h_{FEQ1}+1)\right] = h_{FEQ1} I_{IN} \qquad \text{(AI-4)}$$

or

$$t_r \cong \frac{[C_L + (h_{FEQ1}+1)C_{TC}]\ \Delta V}{h_{FEQ1} I_{IN}} \qquad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a MH0025 loaded with 1000 pF, rise times of:

$$\frac{(1000pF + 250pF)\ (17V)}{(50mA)\ (20)}$$

or 21ns may be expected for V^+=5.0V, V^-=-12V. Figure AI-3 gives rise time for various values of C_L.

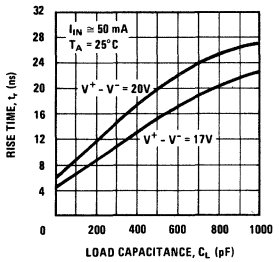


FIGURE AI-3. Rise Time vs C_L for the MH0025

Fall Time Considerations

The MOS logic fall time (voltage rise) of the MH0025 is dictated by the load, C_L, and the output capacitance of Q_1. The fall time equivalent circuit of MH0025 may be approximated with the circuit of Figure AI-4. In actual practice, the base

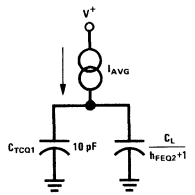


FIGURE AI-4. Fall Time Equivalent Circuit

drive to Q_2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic

values at the end. Figure AI-5 shows t_f as function of C_L.

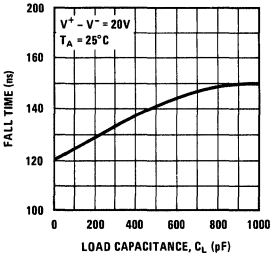


FIGURE AI-5. MH0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R_2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \qquad \text{(AI-6)}$$

or

$$t_f \cong 2R_2 \left(C_{TCQ1} + \frac{C_L}{h_{FEQ1+1}}\right) \qquad \text{(AI-7)}$$

MH0025 Input Drive Requirements

Since the MH0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50 to 60 mA region. It is therefore a good idea to drive the MH0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the MH0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The MH0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output

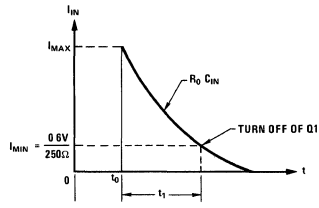


FIGURE AI-6. MH0025 Input Current Waveform

pulse width. In the latter mode a long pulse is supplied to the MH0025. The input current is of the general shape as shown in Figure AI-6. I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50 to 60 mA). Q_1 will begin to turn-off when I_{IN} decays below V_{BE}/R_1 or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R_0 C_{IN}} \qquad \text{(AI-8)}$$

Where:

R_0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \frac{V_{BE}}{R_1}$ and solving for t_1 yields:

$$t_1 = R_0 C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R_0 C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-10)}$$

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200pF is:

$$t_{PW} \cong \frac{25ns + 150ns}{2} + (65\Omega)(2{,}200pF) \ln \frac{50mA}{2.5mA} = 517ns$$

A plot of pulse width for various types of drivers is shown in Figure AI-7. For applications in which

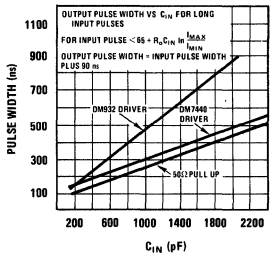


FIGURE AI-7. Output PW Controlled by C_{IN}

the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

The MH0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and plus 20V. The MH0025 is shown in Figure AI-8 driving the address or precharge line in the logically controlled mode.

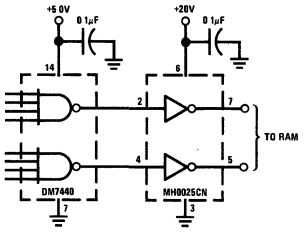


FIGURE AI-8. DC Coupled MH0025 Driving 1103 RAM.

If DC operation to a negative level is desired, a level translator such as the DM7800 or DH0034 may be employed as shown in Figure AI-9. Finally, the level shift may be accomplished using PNP transistors are shown in Figure AI-10.

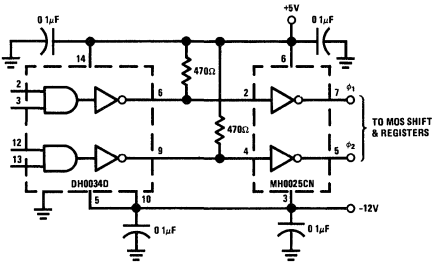


FIGURE AI-9. DC Coupled Clock Driver Using DH0034.

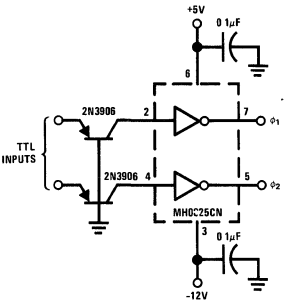


FIGURE AI-10. Transistor Coupled MH0025 Clock Driver.

APPENDIX II

MH0026 Circuit Operation

The schematic of the MH0026 is shown in Figure AII-1. The device is typically AC coupled on the input and responds to input current as does the MH0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q_1, Q_2, Q_5, Q_6, and Q_7 are "OFF" allowing Q_3 and Q_4 to come "ON." R_6 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q_1 and Q_2 turning them "ON." Simultaneously, Q_3 and Q_4 are snapped "OFF." As the input voltage rises (to about 1.2V), Q_5 and Q_6 turn-on. Multiple emitter transistor Q_5 provides additional base drive to Q_1 and Q_2 assuring their complete and rapid turn-on. Since Q_3 and Q_4 were rapidly turned OFF minimal power supply current spiking will occur when Q_7 comes "ON."

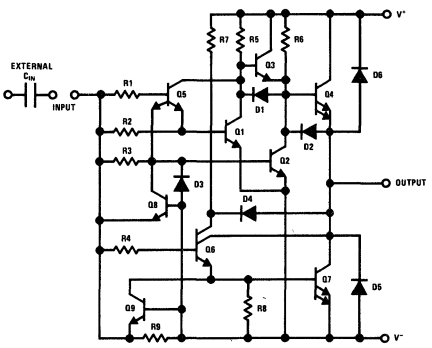


FIGURE AII-1. MH0025 Schematic (One-Half Circuit)

Q_6 now provides sufficient base drive to Q_7 to turn it "ON." The load capacitance is then rapidly discharged toward V^-. Diode D_4 affords a low impedance path to Q_6's collector which provides additional drive to the load through current gain of Q_7. Diodes D_1 and D_2 prevent avalanching Q_3's and Q_4's base-emitter junction as the collectors of Q_1 and Q_2 go negative. The output of the MH0026 continues negative stopping about 0.5V more positive than V^-.

When the TTL input returns to logic "0," the input voltage to the MH0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q_8 and Q_9 turn-on, pulling stored base charge out of Q_7 and Q_2 assuring their rapid turn-off. With Q_1, Q_2, Q_6 and Q_7 off, Darlington connected Q_3 and Q_4 turn-on and rapidly charge the load to within a V_{BE} of V^+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the MH0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\ \Delta V \qquad \text{(AII-1)}$$

For C_L = 1000pF, V^+ = 5.0V, V^- = -12V, $t_r \cong$ 21ns. Figure AII-2 shows MH0026 rise times vs. C_L.

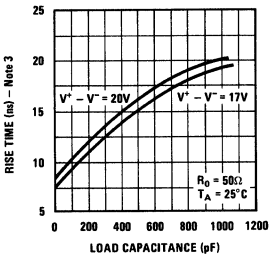


FIGURE AII-2. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the MH0026 is determined primarily by the capacitance Miller capacitance of Q_5 and Q_1 and R_5. The fall time may be predicted by:

$$t_f \cong (2.2)(R_5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q_3
= 2pF

$h_{FE}{}^2 = (h_{FEQ3}+1)(h_{FEQ4}+1)$
$\cong$ 500

For the values given and C_L = 1000pF, $t_f \cong$ 17.5ns. Figure AII-3 gives t_f for various values of C_L.

MH0026 Input Drive Requirements

The MH0026 was designed to be driven by standard 54/74 elements. The device's input characteristics

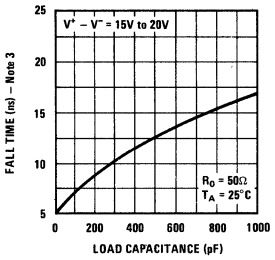


FIGURE AII-3. Fall Time vs Load Capacitance

are shown in Figure AII-4. There is breakpoint at $V_{IN} \cong$ 0.6V which corresponds to turn-on of Q_1 and Q_2. The input current then rises with a slope of about 600Ω ($R_2 \parallel R_3$) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q_5 and Q_6. The slope at this point is about 150Ω ($R_1 \parallel R_2 \parallel R_3 \parallel R_4$).

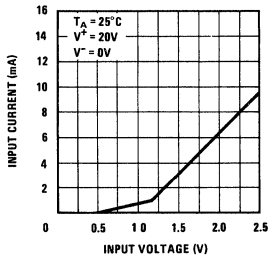


FIGURE AII-4. Input Current vs Input Voltage

The current demanded by the input is in the 5 to 10mA region. A standard 54/74 gate can source currents in excess of 20mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a MH0026. As far as the MH0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the MH0025 and MH0026 is that the MH0026 requires that the output pulse width be logically controlled. In short, the input pulse width $\cong$ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the MH0026 "ON." As before:

$$t_1 = R_0 C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AII-3)}$$

or

$$C_{IN} = \frac{t_1}{R_0 \ln \frac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

In this case R_0 equals the sum of the TTL gate output impedance plus the input impedance of the MH0026 (about 150Ω). I_{MIN} from Figure AII-5 is about 1mA. A standard 54/74 series gate has an high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20mA into 1.2V. For an output pulse width of 500ns,

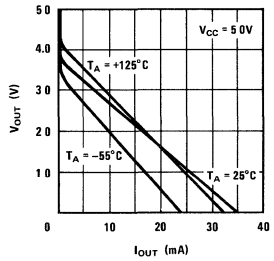


FIGURE AII-5. Logical "1" Output Voltage vs Source Current

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega)\ln \frac{20mA}{1mA}} = 560pF$$

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, MH0026, and temperature variations.

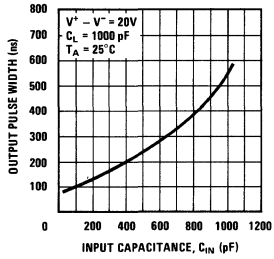


FIGURE AII-6. Optimum Input Capacitance vs Output Pulse Width

A plot of optimum value for C_{IN} vs desired output pulse width is shown in Figure AII-6.

DC Coupled Applications

The MH0026 may be applied in direct coupled applications. Figure AII-7 shows the device driving address or pre-charge lines on an MM1103 RAM.

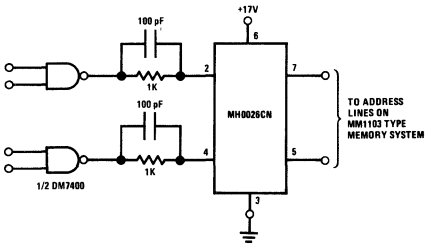


FIGURE AII-7. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a DC level shift, the circuit of Figure AII-8 or AII-9 are recommended.

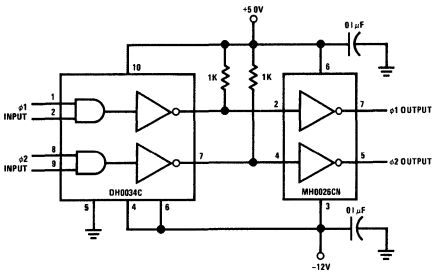


FIGURE AII-8. Transistor Coupled MOS Clock Driver

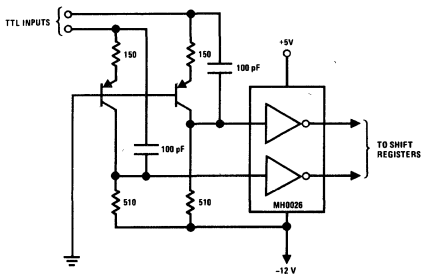


FIGURE AII-9. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007 Direct coupled, single phase, TTL compatible clock driver.

MH0009 Two phase, direct or AC coupled clock driver.

MH0012 10MHz, single phase direct coupled clock driver.

MH0013 Two phase, AC coupled clock driver.

MH0025 Low cost, two phase clock driver.

MH0026 Low cost, two phase, high speed clock driver.

MH8808 Dual clock driver for MM5262 2k RAM.

MOS Oscillator/Clock Drivers

MH7803/MH7807 — Complete two phase clock system for MOS micro-processors and calculators.

MOS RAM Memory Address and Precharge Drivers

MH8804 Quad TTL to 1103 address driver.

MH8805 Dual TTL to 1103 address driver.

MH0025 Dual address and precharge driver.

MH0026 Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034 Dual high speed TTL to negative level converter.

DM7800 Dual TTL to negative level converter.

DM7810/DM7812/DM7819 — Open collector TTL to positive high level MOS converter gates.

DM78L12 Active pull-up TTL to positive high level MOS converter gates.

MOS to TTL Level Converters and Sense Amps

DM7802/DM7806* — Dual sense amp for MM5262 2k MOS RAM memory.

LM165 Series* — Hex sense amp MOS to TTL.

LM163/LM75107/LM75207* — Dual sense amp for MM1103 1k MOS RAM memory.

Voltage Regulators for MOS Systems

LM109/LM140 Series — Positive regulators.

LM120 Series — Negative regulators.

LM125 Series* — Dual +/— regulators.

*To be announced.

DATA BUS AND DIFFERENTIAL LINE DRIVERS AND RECEIVERS

INTRODUCTION

Monolithic circuits designed specifically to transmit and receive digital data via buses and differential cables have been available for two or three years. But important changes in transmission concepts and IC designs have been made recently. This note will bring designers up to data on circuits developed at National Semiconductor. Table I and Figure 1 outline the devices to be discussed.

In general, the new bus circuits offer these advances: self-isolation of powered-down receivers; much lower input currents, permitting more driver/receivers pairs per bus line; input hysteresis to raise noise immunity; higher speed with better control of bus levels; and eliminating of terminating pull-up resistors by the TRI-STATE® designs.

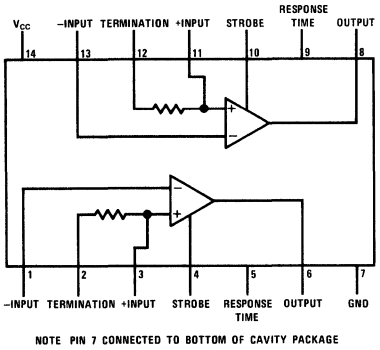
The DM7820/DM8820 and DM7830/DM8830 were described in Application Note AN-22. This note adds to the previous discussion of termination techniques and reports on new tests of their long-lines drive capability and crosstalk immunity.

TABLE I. Table of Devices Discussed

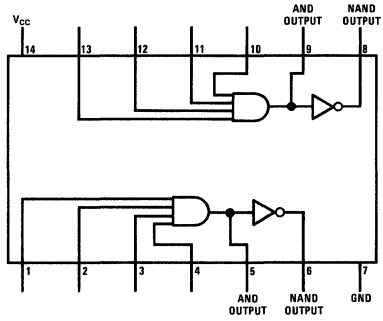
LINE DRIVERS DEVICE NO.	LINE RECEIVERS DEVICE NO.	DESCRIPTION	POWER SUPPLY	COMMENTS
LM1488	LM1489/LM1489A	Communication to EIA standard RS 232C.	±12V LM1489A +5 0V	Twisted pair single ended Unidirectional
DM7830/DM8830	DM7820A/DM8820A	Dual differential line driver and receiver	+5 0V	True differential. ±15V common mode rejection Unidirectional Use of internal receiver termination recommended up to 100 feet
DM7831/DM8831	DM7820A/DM8820A	Dual differential line driver and receiver	+5.0V	True differential, bidirectional. Driver includes upper and lower level clamps to combat transients Use of internal receiver termination optional
DM7832/DM8832	DM7820A/DM8820A	Dual differential line driver and receiver	+5.0V	As above, but without upper level clamping, so party line busses may be used, even with some peripherals powered down
DM7831/DM8831	DM7837/DM8837 (hex) or DM7836/ DM8836 (quad)	Quad single-ended line driver and hex receiver, or a quad 2 input NOR receiver	+5.0V	If used unidirectionally, receiver should be terminated In party line applications disabled driver clamps line Receiver input current is 15μA typical, has 1.0V hysteresis.
TRANSCEIVER DEVICE NO.		**DESCRIPTION**	**POWER SUPPLY**	**COMMENTS**
DM7838/DM8838		Quad open collector transceiver	+5 0V	Receiver has typical 15μA input current 1 0V hysteresis. Driver will pull down double terminated 120Ω line
DM7839/DM8839		Quad TRI-STATE® transceiver Four transmitters all disabled by control NOR gate	+5.0V	Drivers have 10 4 mA forward drive at 2 4V, sink 32 mA at 0 4V Receivers have 1.0V hysteresis, input current is 15μA typical Disabled driver clamps undershoots A transceiver on the bus may be powered down without affecting bus logic levels
DM7833/DM8833		Quad TRI-STATE transceiver One control disables all transmitters, one control disables all receiver outputs	+5.0V	
DM7834/DM8834		Quad TRI-STATE transceiver Controls same as DM7839 but driver and receiver are inverting	+5.0V	
DM7835/DM8835		Quad TRI-STATE transceiver Controls same as DM7833 but driver and receiver are inverting	+5.0V	

10

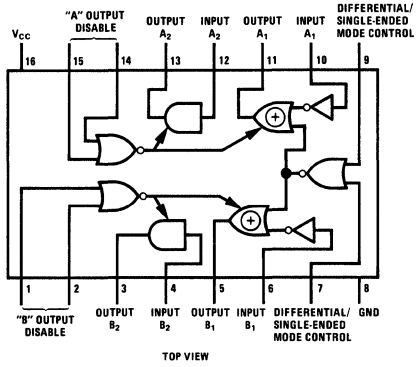
DM7820/DM8820, DM7820A/DM8820A



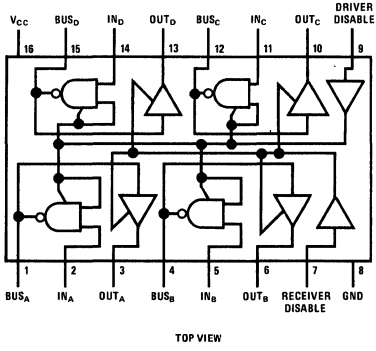
DM7830/DM8830



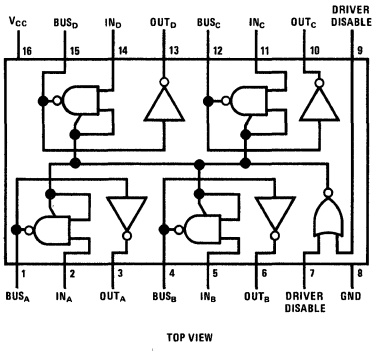
DM7831/DM8831, DM7832/DM8832



DM7833/DM8833



DM7834/DM8834



DM7835/DM8835

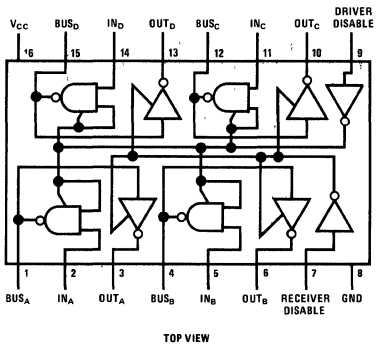
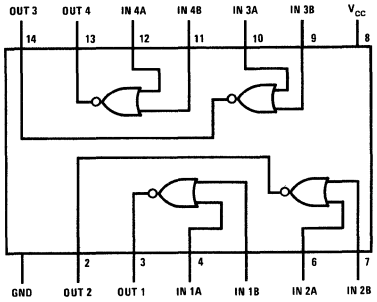


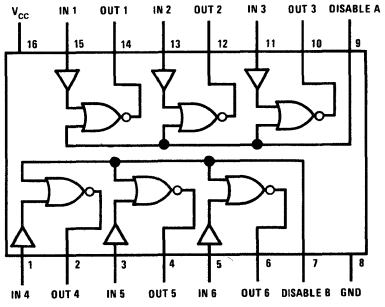
FIGURE 1.

DM7836/DM8836



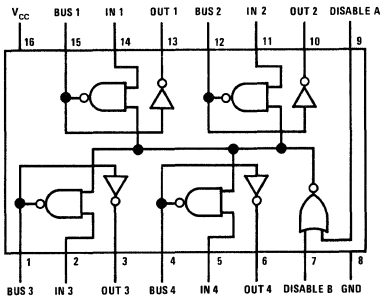
TOP VIEW

DM7837/DM8837



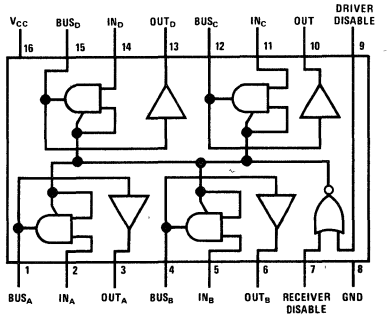
TOP VIEW

DM7838/DM8838



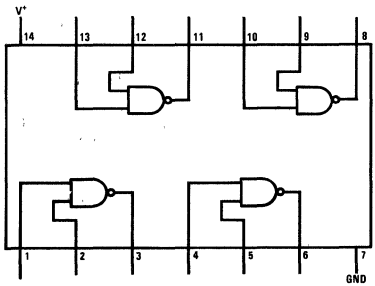
TOP VIEW

DM7839/DM8839



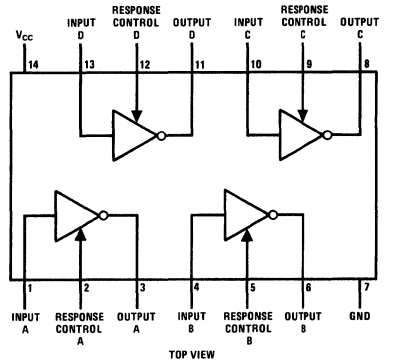
TOP VIEW

LM1488/LM1588



TOP VIEW

LM1489/LM1489A



TOP VIEW

FIGURE 1. (Con't)

Not much need be said about the EIA RS232C designs. They meet or exceed a standard which is below today's attainable performance levels.

UNIFIED BUS

A typical unified bus is a flat, multiconductor cable interconnecting the CPU and peripherals of a minicomputer (Figure 2). The lines are single-ended (non-differential), ground-referenced, bi-directional, and terminated at each end in 120Ω to 3.2V. The line level is high except when an open-collector driver pulls the line low. Drivers take turns transmitting, as controlled by "polling" or other control sequences.

Single-ended communications are susceptible to common mode voltage induced by ground currents between chassis. In a computer room, the problem is usually minimized by linking the chassis with heavy-gauge grounding cables. Communications with remote points go through differential transmission links, or modems coupled to phone lines.

In early unified bus designs, open-collector TTL buffers were used as drivers, and standard gates as receivers. However, the low threshold voltage of the receiving gate (it can be as low as 1.0V) is too close to ground potential, which can itself be carrying transients of almost a volt. In addition, the gate's input current can be as high as 1.6 mA, severely limiting the number of receivers which can be controlled by one driver. This is true particularly if the driver has an open collector output, and must also be sinking the current from a 120Ω termination at each end of the unified bus.

That problem was solved by the SP380 gate. Its signal input is the base of an NPN emitter-follower, giving a higher threshold and lower input current. Unfortunately, the input transistor's collector-base junction becomes forward-biased when V_{CC} goes down. If a peripheral is shut off, the bus lines are clamped near ground unless the bus cable is disconnected manually.

The new unified bus designs in Table I have a receiver that is self-isolating when power is down. The main bus is still usable if peripherals are turned off.

Other improvements include: very low input current, typically 15μA whether V_{CC} is 5.0V or zero; input hysteresis of 1.0V, providing 1.8V noise immunity; thresholds of 1.3V and 2.3V; and temperature compensation to keep thresholds and noise immunity constant.

The DM7836/DM8836 is pin-compatible with the SP380. Each receiver trio in the DM7837/DM8837 has an enable control, so the system can force receiver outputs to zero whether the bus is pulled down or not. The four drivers in the DM7838/DM8838 transceiver are disabled by a NOR gate control.

Each open-collector driver in the transceiver sinks 50 mA at 0.7V. It has the power to pull down the double-terminated bus and drive 20 of the low-current receivers.

TRI-STATE BUS

TRI-STATE logic (or TSL) outputs are active in both the "1" and "0" state. This greatly improves risetimes and allows many more driver/receiver pairs to be connected to a bus since power is not wasted in terminations. Switching delays can be halved during certain data exchanges.

A disabled output switches into a third, high-impedance state. Only small leakage currents flow in the output in this state, virtually disconnecting the output from the bus. TSL outputs do not "wire-OR" – the bus is operated by one set of outputs at a time.

Figure 3 is a TSL bus line. Although there are no terminations, reflections are less of a problem than in a unified bus. The bus is tightly controlled without terminations because the disabled drivers actually clamp undershoots.

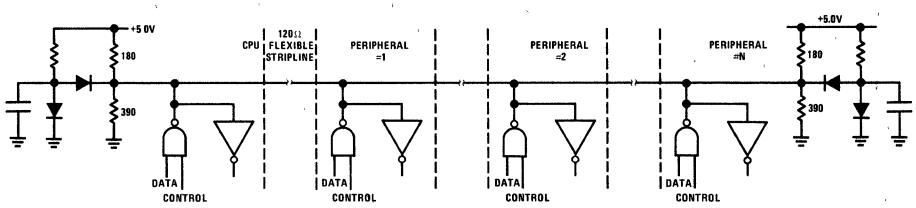


FIGURE 2. Unified Open Collector Bus

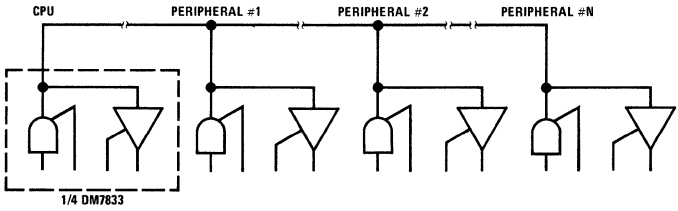


FIGURE 3. TRI-STATE Bus

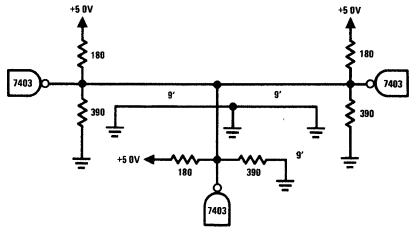


FIGURE 4. Open Collector Line With Stub

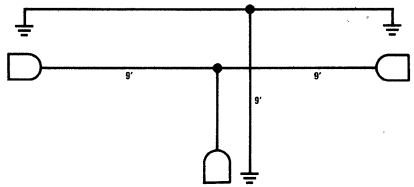


FIGURE 5. TRI-STATE Line With Stub

Tests indicate the transceivers can drive bus lines longer than 25 feet. They are guaranteed to source 10.4 mA at the minimum "one" level of 2.4V. Small-signal source impedance is typically 50Ω to 5.0V compared with 120Ω to 3.2V on the unified bus. That explains TSL's higher speed — the active-pull-up output charges the line capacitance much faster. If even greater source current capability is needed, the DM7831/DM8831 and DM7832/DM8832 are available. As quad single-ended drivers they can source and sink at least 40 mA (and have a source impedance of only 11Ω). They can drive lines with characteristic impedance down to 40Ω.

When a peripheral equipped with a transceiver is powered down or disabled, no current (apart from microamps of leakage) will flow in the input/output while the data levels move between ground and +5.0V. Other peripherals can still use the bus without their signals being shunted or degraded. The receivers are isolated like the unified bus designs. (The DM7832/DM8832 has the same degree of freedom. However, the DM7831/DM8831 has an output diode to V_{CC} to control transients when used in its differential mode. It will clamp the bus lines when powered-down, so it is not recommended for use in a peripheral which might be switched off in isolation from the rest of the system).

In the TSL transceiver family, typical receiver input characteristics are 17μA current, 400 mV hysteresis, and 1.4V noise immunity. All types are completely compatible with standard TTL.

Figure 4 shows a line with a stub (actually a branch of equal length, to ease analysis). It is terminated in the line's characteristic impedance at all three ends.

Figure 5 shows an identical hook-up, this time "terminated" only by a disabled TRI-STATE gate at the receiving end and the stub end.

The result of driving the circuit of Figure 4 is seen in Figure 6. The current pulled from the line by the driver (top trace) was determined by the effective impedance of the termination in parallel with the 120Ω line charged to 3.2V. When this wavefront reached the fork, half the current was drawn from each leg. So when the half-current front arrives at the stub only half the voltage pull-down results (Figure 6 lower trace).

A series of these timed halvings and quarterings produces the bathtub effect shown. The duty cycle distortion experienced by a receiver at the stub termination is obvious. If we take off the stub termination network, the situation gets no better. Figure 7 shows it (time base and sensitivity unchanged). The undershoot in the lower trace is followed by an overshoot which reaches 1.0V above ground: and the stub continues to ring (which isn't surprising since its two ends have terminations in 60Ω and infinity respectively). A receiver at the end of the stub would have to be ignored until the ringing had decayed, and its output had become valid.

Contrast this with Figure 8, demonstrating the results of the TRI-STATE driver of Figure 5. The same rapid falling edge at the receiving end is brought to a halt very sharply, and instead of reflective overshoots, there is a shallow series of level adjustments which never cross the maximum zero level of 0.4V above ground.

How is this achieved?

Figure 9 shows the schematic of the output stage of a TRI-STATE transceiver. Now if the output is disabled, point A is held by the TRI-STATE control at $V_{CE}sat + V_{BE}$, or 1.0V at 25°C.

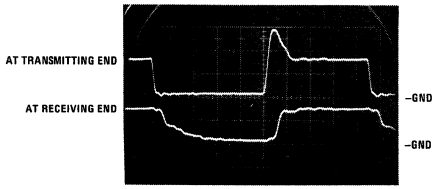


FIGURE 6. Open Collector Bus With Two Terminated Stubs 2.0V/div 20 ns/div

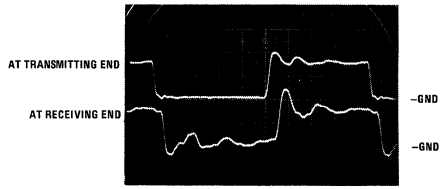


FIGURE 7. Open Collector Bus at an Unterminated Stub

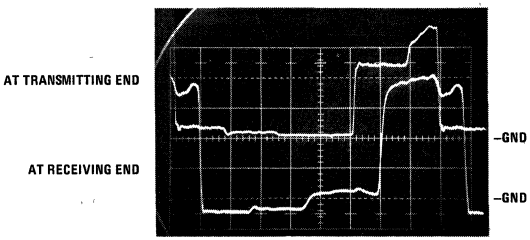


FIGURE 8. TRI-STATE® Bus at a Stub – Demonstration of the TSL Non-Linear Termination

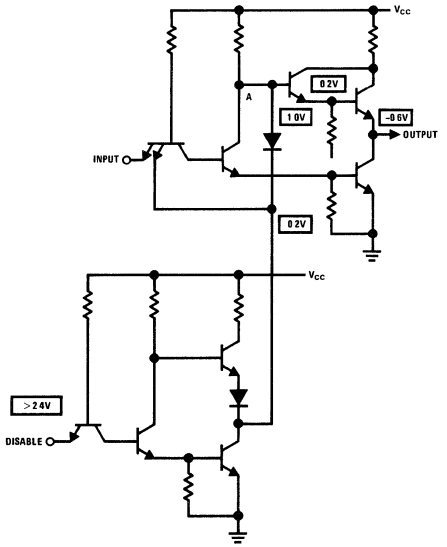


FIGURE 9. DC Levels in a Disabled TRI-STATE Element

So to turn on the Darlington pull-up stage will take an undershoot below ground on the bus line of 2 V_{BE} lower than point A. Or at 25°C, 1.0 − 1.6, = −0.6V. Allowing for a chip temperature somewhat above ambient, the output will begin to clamp at -0.4V. Figure 10 shows a typical result of

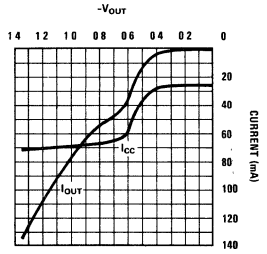


FIGURE 10. Current Available as a Function of Bus Voltage at a Disabled TRI-STATE Output

a test of pulling current out of a disabled TRI-STATE output.

O. A. Horna* has pointed out the effectiveness of a non-linear termination in emitter-coupled logic transmission lines. The ability of the disabled TSL output to turn on very hard in a precisely similar way in an otherwise uncontrollable situation has been conclusively demonstrated.

A further advantage for an unterminated line appears under certain special conditions of architecture. Figures 11 and 12 compare two test circuits, simulating two peripherals one on each

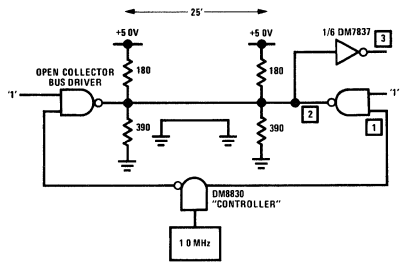


FIGURE 11. Central Controller in an Open Collector Environment

*O. A. Horna – *"Non-Linear Termination of Transmission Lines"* IEEE Transactions on Computers, Sept. 1972, pp. 1011-1-15.

10

side of a CPU, linked by, in the first case an open collector terminated bus; in the second case a TRI-STATE bus.

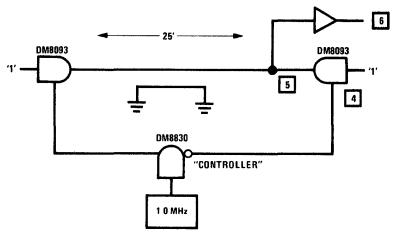


FIGURE 12. Central Controller in a TRI-STATE Environment

In both cases, the bus drivers are holding the bus in one state, and not switching data during the experiment.

Looking at Figure 13, in the open collector case, relinquishment by one driver and immediate taking up by the other at the low state still leaves the termination to pull the bus high for two line delays. And the receiver, waiting for data from the far end, must obviously be ignored until a safe amount of time after the glitch seen in Figure 13 trace 3 has died down. Contrast this with the TRI-STATE case shown in Figure 14. The relinquished bus, seeing only extremely low leakage current, does not move. It may be safely assumed that very shortly after the changeover, a change on the line will be a signal being propagated on the bus.

TRUE DIFFERENTIAL TRANSMISISON

Often, a zero ground reference can't be established between remote subsystems. One can overwhelm the ground difference with a high-amplitude, single-ended transmission. But a differential transmission not referenced to ground is more efficient (Figure 15). The data is complemented at normal logic levels, transmitted over a twisted-pair cable, and received with a comparator sensitive enough to overcome signal degradations, yet rejecting common mode voltages.

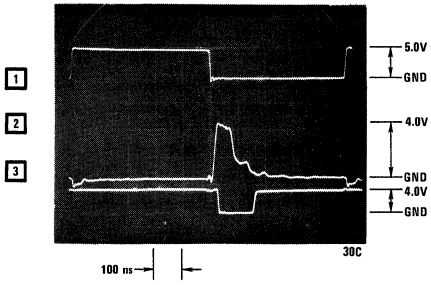


FIGURE 13. Open Collector Bus Signals With Central Controller

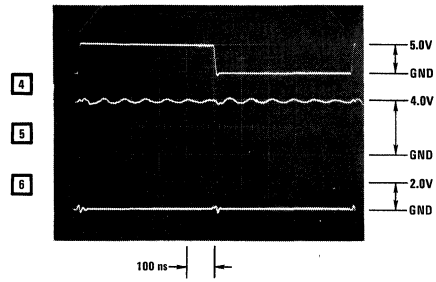


FIGURE 14. TRI-STATE Bus Signals With Central Controller

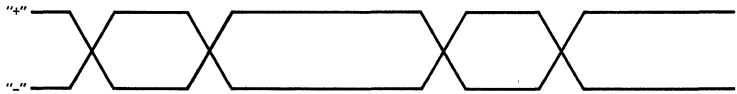


FIGURE 15. Differential Drive — Ideal

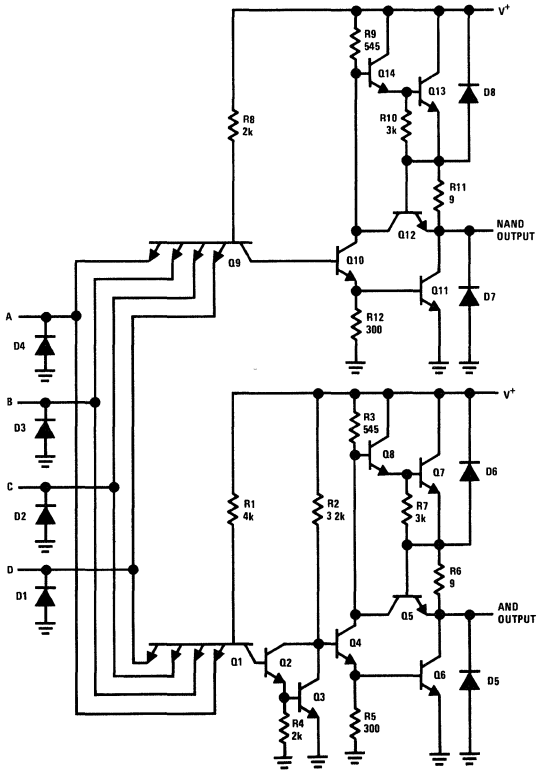


FIGURE 16. DM8830 Schematic

We implemented the differential concept several years ago with the DM7830/DM8830 driver and DM7820/DM8820 receiver. More recently, the two TRI-STATE drivers have been used in such applications. DM7831 output characteristics in the differential driving mode are shown in Figure 17.

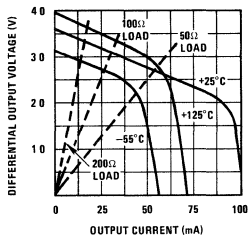


FIGURE 17. Differential Output Voltage as a Function of Differential Output Current in the DM7831

The DM7820 and DM7830 designs were explained in AN-22. Rather than repeat the information in that note, the following sections will answer questions frequently asked by users.

First, how does the new DM7820A differ from the DM7820? They both have the same schematic. One of the two receivers on the chip is shown in Figure 18. However, the "A" version's fanout is 10 TTL or DTL loads rather than 2, the strobe input is specified fully and is guaranteed to be driven by saturated logic, and the speeds are guaranteed.

Second, what establishes the driver current requirement? The receiver's non-inverting input is at the center of a voltage divider between V_{CC} and ground. This sets the voltage into the terminal at 1/2 V_{CC}, or 2.5V in a 5.0V system. The small-signal input impedance is the parallel combination of the two 5.0 kΩ +167Ω paths, or about 2.5 kΩ. When the input swings from high to ground, the current transient is about 1.0 mA. A similar analysis shows the driver must source about 1/2 mA to bring the inverting input up to 2.4V.

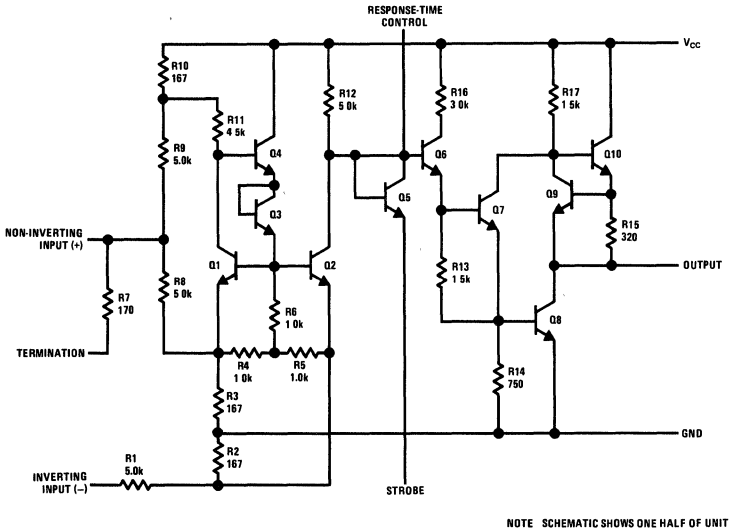


FIGURE 18. DM7820 Schematic

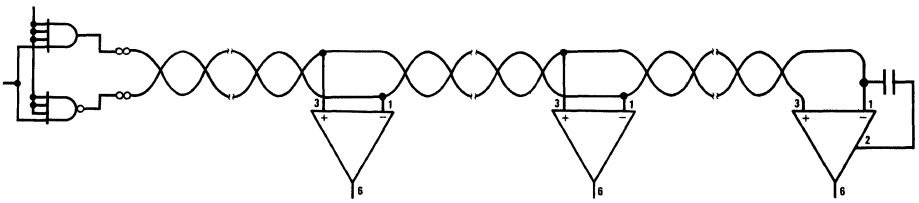


FIGURE 19. DM7830 Driving Daisy-Chained DM7820's

The DM7830 and DM7831 output curves are similar. Either can drive up to 12 DM7820 receivers strung along a cable, as in Figure 19, and have ample overdrive at the last receiver.

TERMINATING THE DIFFERENTIAL LINE

There are three modes of operation of the differential line, each of which demands a different answer to the commonly asked question of how to terminate the line. AN-22 only went into one case, namely, terminating a short line where data period exceeds two line lengths. The second case covers those lines where the period is less than two line lengths, and the third the case where the line is long.

Why is two line delay times significant? It's a question of power dissipation only. When the line is short, so that effectively no voltage is lost in the copper of the cable, running without a termination, where the differential capability of the driver exceeds 3.5V will produce reflections of 7.0V magnitude in the line.

This situation is best avoided, so a termination in the characteristic impedance of the line is advisable. When data rates are slow, this means that the driver, if the termination is dc, will continue to dissipate the power plotted on the load line of Figure 17, quite unnecessarily. If instead a capacitor is included in series with the dc termination, at the leading edge the termination appears dc, so Radio Frequency Interference (RFI) doesn't get generated. But as the capacitor charges, the voltage on the higher line rises, and the current in the driver drops, until at one V_{BE} below V_{CC}, line power ceases to be dissipated.

So long as the rise is controlled, RFI won't be a problem. And the rule of thumb of $R_1C = 3$ line lengths works very well. Where the driver is running so fast as never to be waiting for the reflection, it will be continuously dissipating the power indicated by the load line continuously.

As the line gets longer, the loop resistance gets up to the same order as the terminating resistor. That translates into an attenuation of the differential drive voltage at the receiver. Once the leading edge of the received voltage gets below 2.5V, the reflection ceases to have RFI significance, and a progressively worse mismatch is acceptable as the line gets longer, since the higher the termination resistor value, the more signal is available. For a typical cable, 1000 feet marks the point where any termination serves only to weaken the signal and narrow the channel bandwidth.

The bandwidth of the DM7820 receiver may be reduced by use of a shunt capacitor. The response curve is shown in Figure 20.

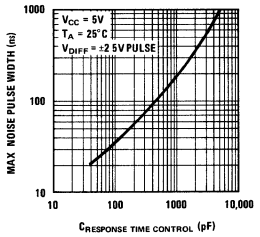


FIGURE 20. Noise Rejection in the DM7820A

MAXIMUM LINE LENGTHS

The tests in Table II were made with a DM7820 and DM7830 to settle questions about maximum line lengths and frequencies. Characteristics of the test cable were: 24 AWG gauge; 110Ω impedance; 5.6Ω/100 ft loop resistance; and 14 pF/ft capacitance (D-200 multi-pair cable made by Dynatronic Engineering Corp., Los Angeles).

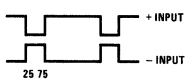
Receiver inputs were complementary pulses with 25/75% duty cycles. These simulate a string of alternating ones and zeros in an RZ (return to zero) format. The first results column indicates safe maximum data rates. The second column shows the rates at which attenuation reached a point where the signal could not switch the line receiver. These are typical, not maximum or safe rates.

Figure 21 illustrates the weaker signals which will switch the receiver. There is obviously no noise margin. For maximum performance, a single twisted-pair line should meet all three of these criteria:

1. High characteristic impedance (to maximize initial voltage step and voltage across the termination at the receiver)
2. Low capacitance (minimizes the "line charging" effect, which attenuates the signal's high-frequency components and makes dc loss worse by degrading the response to fast transients)
3. Low resistance to dc (use heavier-gauge cable for long runs driven at high frequency)

TABLE II. DM8830A/DM8820A 24 Gauge 110Ω

Line Length	Point of Duty Cycle Distortion	Point of Failure To Invert
25'	10 MHz	25 MHz
200'	5 0 MHz	12 MHz
1000'	1 25 MHz	3.2 MHz
5000'	0.125 MHz	0.275 MHz



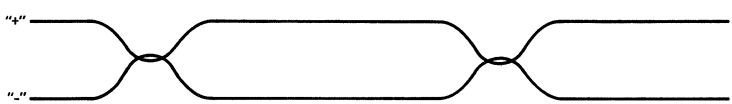


FIGURE 21. Differential Drive Long Distance

CROSSTALK IMMUNITY

One more question concerns crosstalk in multi-pair cables. The tests reported in Table III indicate that the individual pairs rarely, if ever, need individual shielding. One shield over all the pairs in the sheath should be adequate.

TABLE III.

NOISE THRESHOLD AT POINT A (VOLTS)		FREQUENCY
LOWER	UPPER	
1.22	1 26	500 kHz
1.22	1 27	100 kHz
1 24	1.30	10 kHz
1.24	1.30	1.0 kHz

Two side-by-side runs of twisted pairs in D-200 cable were selected to provide two 800-foot lengths adjacent to each other in the bundle for their whole length. A DM7830 driver and a DM7820 receiver were connected to each pair. One driver's input was a pulse train and the other driver's input was a dc voltage. Tests were made to determine the susceptibility of the receiver on the dc line to signals cross-coupled into it from the pulsed line.

This driver/cable/receiver combination is susceptible in a transition region about 60 mV wide between the "1" and "0" states, indicated by the tabulated thresholds for the dc line. Signals from the ac side coupled-in sufficiently to trip the dc pair's receiver.

However, in a real system both driver outputs will swing through this region rapidly. The minimum swing is 2.0V. Therefore, the sensitive region is 60 mV/2,000 mV, or 3% of the swing and of the logic switching time. The minimum risetime of a non-damped DM7820 receiver output is 50 ns. Assuming this is the result of a straight voltage/time ramp input, the receiver is susceptible to crosstalk only if it is being driven with transition times greater than 50 ns/3%, or 1.6 ms.

In fact, the longest driver risetimes observed when the DM7830 was driving the longest cable in the previous test (Table II) were always less than 10 ns. We can conclude that a twisted pair with the driver and receiver is immune to crosstalk from another DM7830-DM7820 combination operating with any adjacent twisted pair.

EIA STANDARD CIRCUITS

The drivers and receivers listed as EIA RS232C circuits in Table I meet the specifications of that standard. It might be noted, however, that the standard's provisions antedate the availability of integrated circuits for such communications. Thus, it tends to restrict further development.

Compare the results in Table II, for example, with paragraph 1.3 of the standard. The standard indicates 20 kilobits/second is a nominal data transfer rate. And paragraph 1.4 requires single-ended, ground-referenced links even though true differential communications are demonstratedly more efficient in data exchanges between chassis.

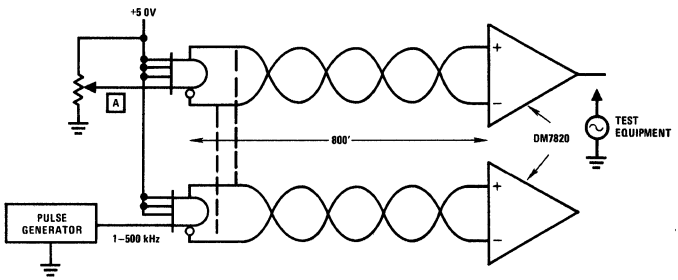


FIGURE 22. Crosstalk Between Close Twisted Pairs

DRIVING 7-SEGMENT GAS DISCHARGE DISPLAY TUBES WITH NATIONAL SEMICONDUCTOR CIRCUITS

INTRODUCTION

Circuitry for driving high voltage cold cathode gas discharge 7-segment displays, such as Sperry Information Displays and Burroughs Panaplex II, is greatly simplified by a complete new line of monolithic integrated circuits from National Semiconductor. The new products also make possible reduced cost of system implementation. They are: DM7880/DM8880 high voltage cathode decoder/driver; DM8884A high voltage cathode decoder/driver; DM8885 MOS to high voltage cathode buffer; DM8889 low power cathode driver; and DM8887 8-digit anode driver.

In addition to satisfying all the displays' parameter requirements, including high output breakdown voltage, the new circuits have capability of programming segment current, and providing constant current sinking for the display segments. This feature alleviates the problem of achieving uniformity of brightness with unregulated display anode voltage. The National circuits can drive the displays directly.

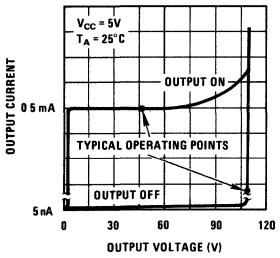
Sperry Information Displays and Burroughs Panaplex II are used principally in calculators and digital instruments. These 7-segment, multi-digit displays form characters by passing controlled currents through the appropriate anode/segment combinations. The cathode in any digit will glow when a voltage greater than the ionization voltage is applied between it (the cathode) and the anode for that digit. In the multiplexed mode of operation, a digit position is selected by driving the anode for that digit with a positive voltage pulse. At the same time, the selected cathode segments are driven with a negative current pulse. This causes the potential between the anode and the selected cathodes to exceed the ionization level, causing a visible glow discharge.

Generally, these displays exhibit the following characteristics: low "on" current per segment—from 200μA (in DC mode) to 1.2 mA (in multiplex mode); high tube anode supply voltage—180V to 200V; and moderate ionization voltage—170V. Once the element fires, operating voltage drops to approximately 150V and light output becomes a direct function of current, which is controlled by current limiting or current regulating cathode circuits. Current regulation therefore is most desirable since brightness will then be constant for large anode voltage changes. Tube anode to cathode "off" voltage is approximately 100V; and maximum "off" cathode leakage is 3μA to 5μA.

Correspondingly, specifications for the cathode driver must be complimentary, approximately as follows: A high "off" output breakdown voltage 80V minimum; typical "on" output voltage of 50V; maximum "on" output current of 1.5 mA per segment; and maximum "off" leakage current of 3μA to 5μA.

To allow operation without anode voltage regulation, the cathode driver must be able to sink a constant current in each output, with the output

(a) Cathode Driver Output Characteristic



(b) On Currents vs Temperature

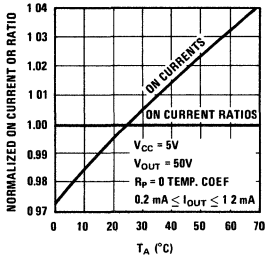


FIGURE 1.

"on" voltage ranging from 5V to 50V (see Figure 1). The following is a brief description of the circuits now offered by National:

DM7880/DM8880 High Voltage Cathode Decoder/Driver

The DM7880/DM8880 offers 7-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs; and programmable output current from 0.2 mA to 1.5 mA.

Application

The circuit has a built-in BCD decoder and can interface directly to Sperry and Panaplex II displays, minimizing external components (Figure 2). The inputs can be driven by TTL or MOS outputs directly. It is optimized for use in systems with 5V supplies.

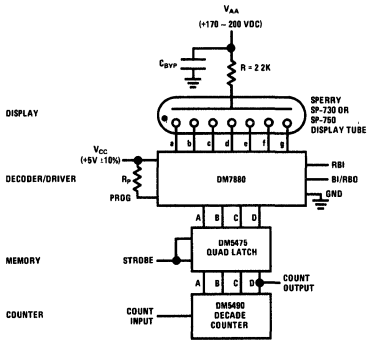


FIGURE 2. DC Operation From TTL

The DM7880/DM8880 decoder/driver provides for unconditional as well as leading and trailing zero blanking. It utilizes negative input voltage clamp diodes. Typically, output current varies only 1% for output voltage changes of 3V to 50V. Operating power supply voltage is 5V. The device can be used for multiplexed or DC operation.

Available in 16-pin cavity DIP packages, the DM7880 is guaranteed over the full military operating temperature range of −55°C to +125°C; the DM8880 in molded DIP over the industrial range of 0°C to +70°C.

DM8884A High Voltage Cathode Decoder/Driver

The DM8884A offers 9-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs, programmable from 0.2 mA to 1.2 mA. It also offers input negative and positive voltage clamp diodes for DC restoring, and low input load current of −0.25 mA maximum.

Application

DM8884A decodes four lines of BCD input and drives 7-segment digits of gas-filled displays. There are two separate inputs and two additional outputs for direct control of decimal point and comma cathodes. The inputs can be DC coupled to TTL (Figure 3) or MOS outputs (Figure 4), or AC-coupled to TTL or MOS outputs (Figure 5) using only a capacitor. This means the device is useful in applications where level shifting is required. It can be used in multiplexed operation, and is available in an 18-pin molded DIP package.

Other advantages of the DM8884A are: typical output current variation of 1% for output voltage changes of 3V to 50V; and operating power supply

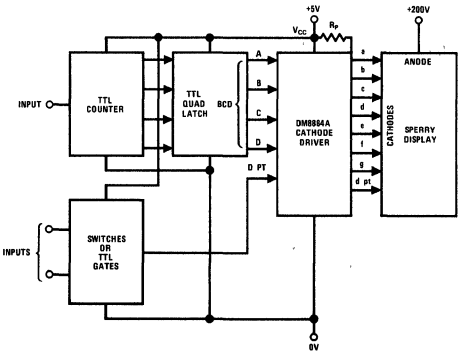


FIGURE 3. Interfacing Directly With TTL Output

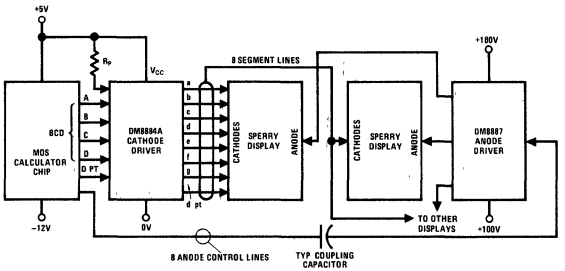


FIGURE 4. BCD Data Interfacing Directly With MOS Output

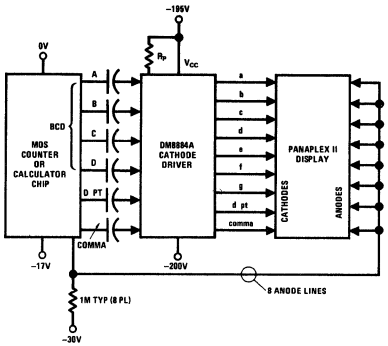


FIGURE 5. Cathode BCD Data AC Coupled From MOS Output

voltage of 5V. Inputs have pull-up resistors to increase noise immunity in AC coupled applications.

The DM8884A is guaranteed over the 0°C to +70°C operating temperature range.

DM8885 MOS to High Voltage Cathode Buffer

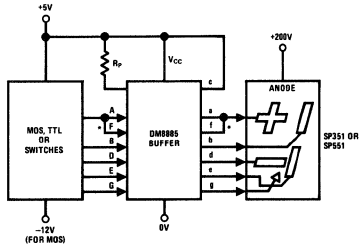
The DM8885 features seven constant current-sink outputs; programmable output current of 0.2 mA to 1.5 mA; high output breakdown voltage of 80V minimum; and capability for blanking through program current input. It operates from a +5V supply.

Application

DM8885 is best suited for interfacing 7-segment fully decoded MOS chips to digit displays. It is also useful for driving polarity, overrange, and decimal point segments.

DM8885 has 6 inputs and 7 outputs. Output c is decoded internally; the other 6 outputs are directly controlled by the 6 corresponding inputs. A typical application of this device is interfacing between an MOS calculator chip with 7-segment decoded outputs (open-drain or push-pull) and Sperry/ Panaplex II displays (Figure 6).

When the DM8885 is used to drive minus and plus (polarity) cathodes, overrange, and decimal points, output c should be tied to V_{CC} so it does not saturate (Figure 7). This leaves 6 inputs and 6 outputs related one-to-one. The inputs can be driven directly from TTL or MOS outputs.



*Output may be paralleled for cathodes requiring more current, providing the corresponding inputs are also paralleled

FIGURE 7. Polarity, Overrange, Decimal Point Driving

The DM8885 is available in 16-pin molded DIP package, and is guaranteed over the operating temperature range of 0°C to +70°C.

DM8889 Low Power Cathode Driver

The DM8889 requires no power supply since power is derived from program current. It offers extremely low standby power—only 1 mW internally. Features include programmable output currents 0.3 mA to 1.7 mA; 8 constant current-sink outputs; and input negative voltage clamp diodes for DC restoring. Outputs have 80V minimum breakdown voltage.

The device is suitable for multiplexed operation from fully decoded chips and is capable of driving decimal point segments simultaneously with numeric segments.

Application

The DM8889 has 8 inputs and 8 outputs, and interfaces directly between 7-segment decoded MOS outputs and numeric display tubes (Figures 8 and 9). It is optimized for use in systems with a limited number of power supplies.

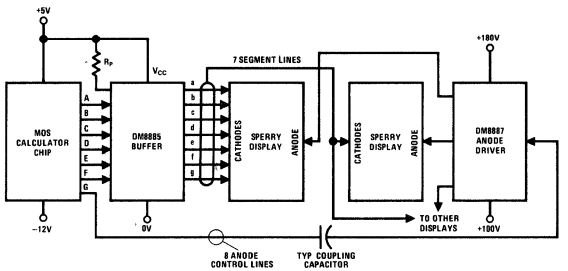


FIGURE 6. Fully Decoded MOS Cathode Outputs

The program input is characterized in terms of input current, therefore any supply (greater than 5V) can provide proper operation by connecting a single resistor to the program pin from the supply.

The DM8889, guaranteed for the 0°C to +70°C operating temperature range, is offered in the 18-pin molded DIP.

DM8887 8-Digit Anode Driver

The DM8887 interfaces directly to MOS chips and operates from a −40V to −80V power supply.

The DM8887 can operate virtually any multiplex display system requiring more output performance from the MOS chip than is available (Figures 4, 6, 8 and 9). It has low input current and voltage swing requirements but can drive up to 16 mA, and exhibits -55V minimum output breakdown voltage.

The DM8887 is available in the 18-pin molded DIP package; and is guaranteed over the operating temperature range of 0°C to +70°C.

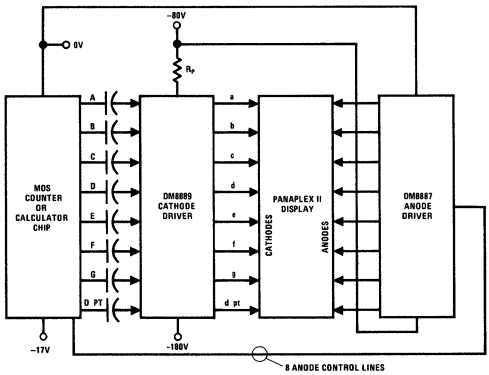


FIGURE 8. Decoded Cathode Data AC Coupled From MOS Output

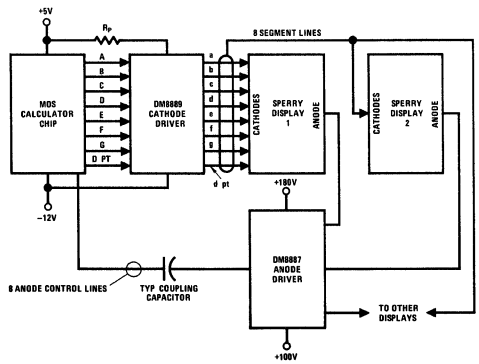


FIGURE 9. Decoded Cathode Data Direct Coupled From MOS Output

COMPARING THE HIGH SPEED COMPARATORS

INTRODUCTION

Several integrated circuit voltage comparators exist which were designed with high speed and complementary TTL outputs as the main objectives. The more common applications for these devices are high speed analog to digital (A to D) converters, tape and disk-file read channels, fast zero-crossing detectors, and high speed differential line receivers. This note compares the National Semiconductor devices to similar devices from other manufacturers.

The product philosophy at National was to create pin-for-pin replacement circuits that could be considered as second-sources to the other comparators, while simultaneously containing the improvements necessary to make a more optimum device for the intended usage. Optimized parameters include speed, input accuracy and impedance, supply voltage range, fanout, and reliability. The LM160/LM260/LM360 are replacement devices for the μA760, while the LM161/LM261/LM361 replace the SE/NE529. Tables I and II compare the critical parameters of the National commercial range devices to their respective counterparts.

SPEED

Throughout the universe the subject of speed must be approached with caution; the same holds true here. Speed (propagation delay time) is a function

TABLE I. LM360/μA760C Comparison $0^\circ \leq T_A \leq +70^\circ C$, $V^+ = +5.0V$, $V^- = -5.0V$

PARAMETER	LM360	μA760C	UNITS
Input Offset Voltage	5.0	6.0	mV max
Input Offset Current	3.0	7.5	μA max
Input Bias Current	20	60	μA max
Input Capacitance	4.0	8.0	pF typ
Input Impedance	17	5.0	kΩ typ @ 1 MHz 25°C
Differential Voltage Range	±5.0	±5.0	V typ
Common Mode Voltage Range	±4.0	±4.0	V typ
Gain	3.0	3.0	V/mV typ 25°
Fanout	4.0	2.0	74 Series TTL Loads
Propagation Delays:			
(1) 30 mV_{P-P} 10 MHz Sinewave in	25	30	ns max 25°
(2) 2.0 V_{P-P} 10 MHz Sinewave in	20	25	ns max 25°
(3) 100 mV Step + 5.0 mV Overdrive	14	22	ns typ 25°

TABLE II. LM261/NE529 Comparison $0^\circ \leq T_A \leq +70^\circ C$, $V^+ = +10V$, $V^- = -10V$, $V_{CC} = +5.0V$

PARAMETER	LM261	NE529	UNITS
Input Offset Voltage	3.0	10	mV max
Input Offset Current	3.0	15	μA max
Input Bias Current	20	50	μA max
Input Impedance	17	5.0	kΩ typ @ 1 MHz 25°C
Differential Voltage Range	±5.0	±5.0	V typ
Common Mode Voltage Range	±6.0	±6.0	V typ
Gain	3.0	4.0	V/mV typ 25°
Fanout	4.0	6.0	74 Series TTL Loads
Propagation Delay – 50 mV Overdrive	20	22	ns max 25°

of the measurement technique. The earlier "standard" of using a 100 mV input step with 5.0 mV overdrive has given way to seemingly endless variations. To be meaningful, speed comparisons must be made with identical conditions. It is for this reason that the speed conditions specified for the National parts are the same as those of the parts replaced.

Probably the most impressive speed characteristic of the six National parts is the fact that propagation delay is essentially independent of input overdrive (Figure 1); a highly desirable characteristic in A to D applications. Their delay typically

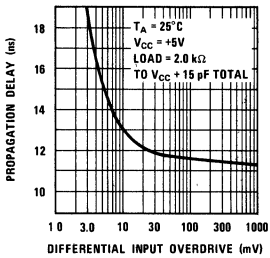


FIGURE 1. Delay vs Overdrive

varies only 3 ns for overdrive variations of 5.0 mV to 500 mV, whereas the other parts have a corresponding delay variation of two to one. As can be seen in Tables I and II, the National parts have an improved maximum delay specification. Further, the 20 ns maximum delay is meaningful since it is specified with a representative load: a 2.0 kΩ resistor to +5.0V and 15 pF total load capacitance. Figure 2 shows typical delay variation with temperature.

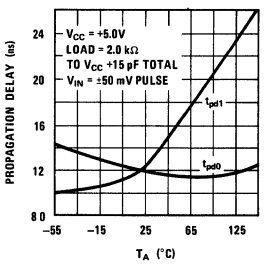


FIGURE 2. Delay vs Temperature

INPUT PARAMETERS

The A to D, level detector, and line receiver applications of these devices require good input accuracy and impedance. In all these cases the differential input voltage is relatively large, resulting in a complete switch of input bias current as the input signal traverses the reference voltage level. This effect can give rise to reduced gain and threshold inaccuracy, dependent on input source impedances and comparator input bias currents. Tables I and II show that the National parts have a substantially lower maximum bias current to ease this problem. This was done without resorting to Darlington input stages whose price is higher offset voltages and longer delay times. The lower bias currents also raise input resistance in the threshold region. Lower input capacitance and higher input resistance result in higher input impedance at high frequencies.

Even with low source impedances, input accuracy is still dependent on offset voltage. Since none of the devices under discussion has internal offset null capability, ultimate accuracy was improved by designing and specifying lower maximum offset voltage. Refer to Figure 3 for typical offset voltage drift with temperature.

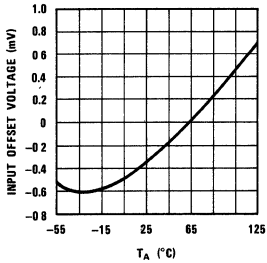


FIGURE 3. Offset Temperature Coefficient

OTHER PERFORMANCE AREAS

In the case of the LM160/LM260/LM360, fanout was doubled over the previous device. For the LM161/LM261/LM361, operating supply voltage range was extended to ±15V op amp supplies

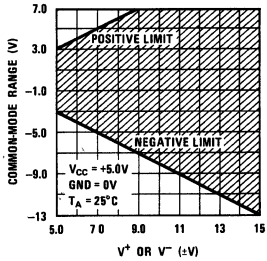


FIGURE 4. LM161 Common Mode Range

which are often readily available where such a comparator is used. Figure 4 reveals the common mode range of the latter device.

The performance improvements previously mentioned were a result of circuit design (Figures 5 and 6) and device processing. Schottky clamping, which can give rise to reliability problems, was not used. Gold doping, which results in processing dependent speeds and low transistor beta, was not used. Instead a non-gold-doped process with high breakdown voltage, high beta, and high f_T ($\approx$ 1.5 GHz) was selected which produced remarkably consistent performance independent of normal process variation. The higher breakdown voltage allows the LM161/LM261/LM361 to operate on ±15V supplies and results in lower transistor capacitance; higher beta provides lower input bias currents; and higher f_T helps reduce propagation time.

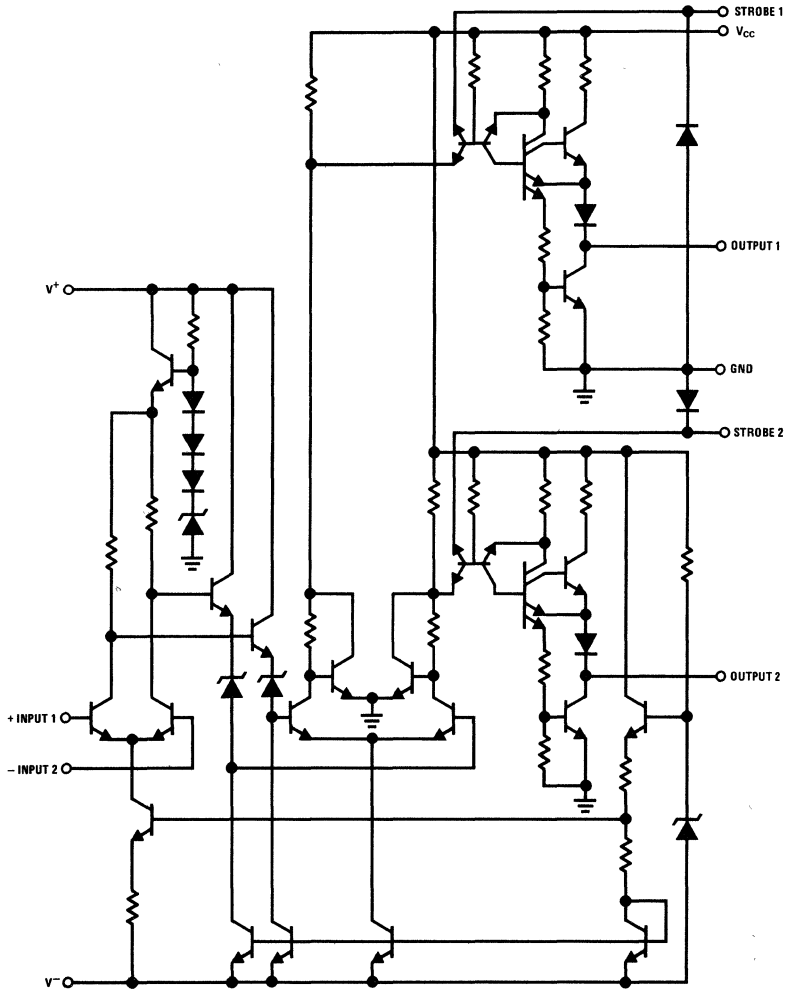


FIGURE 5. LM161 Schematic Diagram

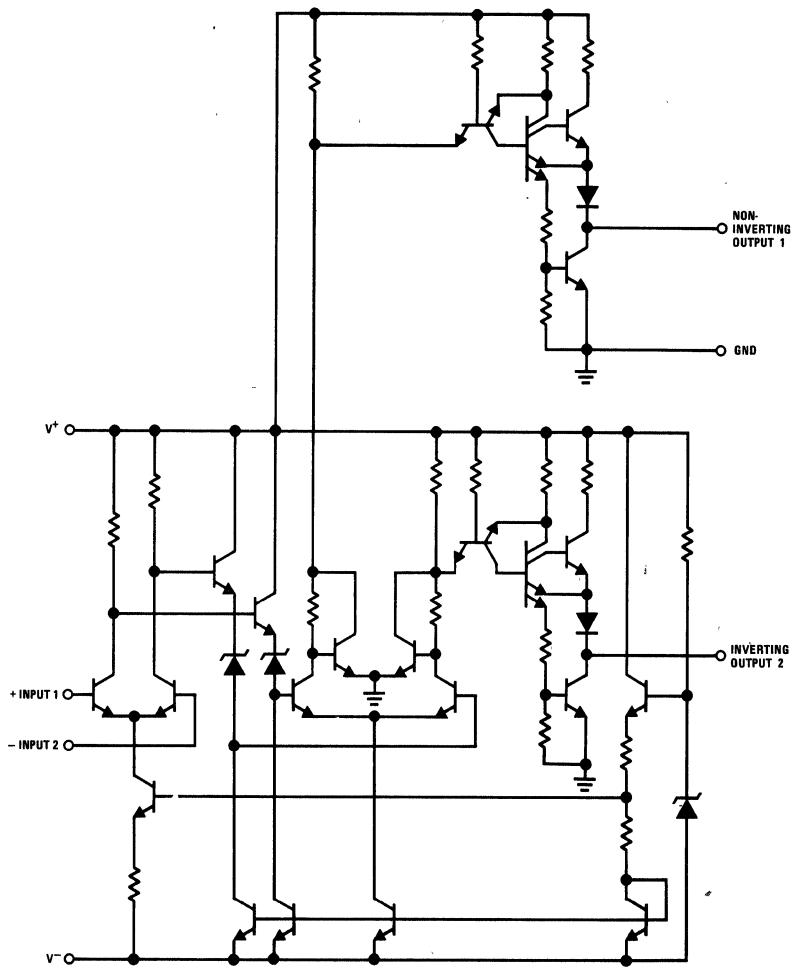


FIGURE 6. LM160 Schematic Diagram

APPLICATIONS

Typical applications have been mentioned previously. The LM160 and LM161 may be combined as in Figure 7 to create a fast, accurate peak detector for use in tape and disk-file read channels. A 3-bit A to D converter with 21 ns typical conversion time is shown in Figure 8. Although primarily intended for interfacing to TTL logic, direct connection may be made to ECL logic from the LM161 by the technique shown in Figure 9. When used this way the common mode range is shifted from that of the TTL configuration. Finally level detectors or line receivers may be implemented with hysteresis in the transfer characteristic as seen in Figure 10.

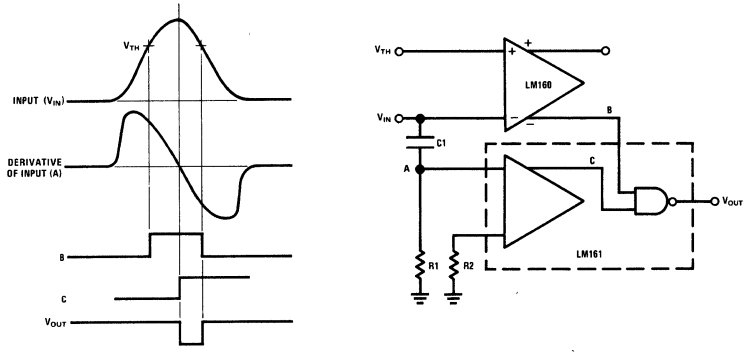


FIGURE 7. Peak Detector

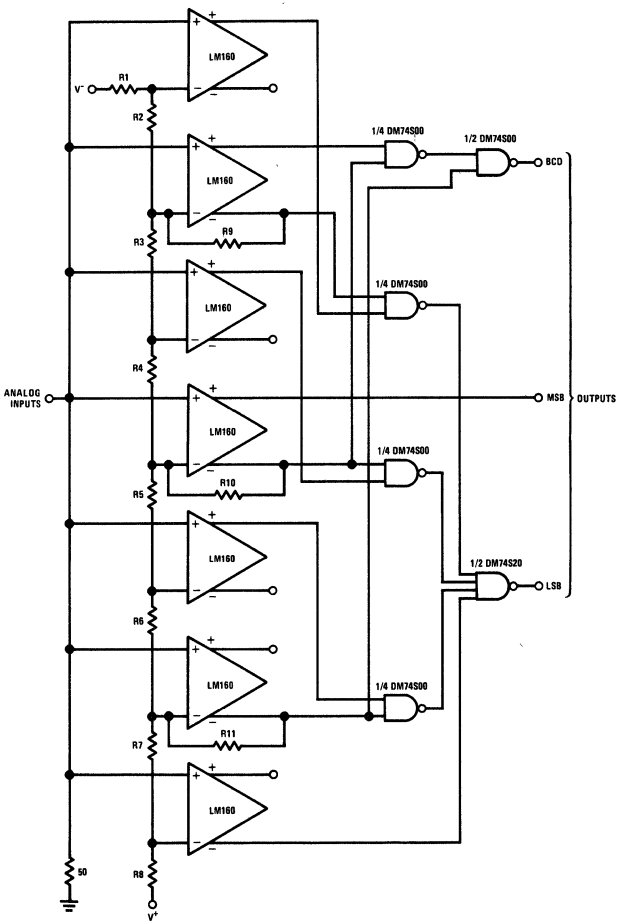


FIGURE 8. High Speed 3-bit A to D Converter

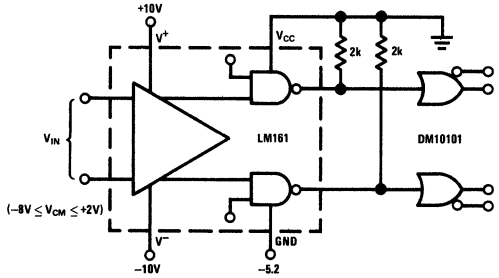
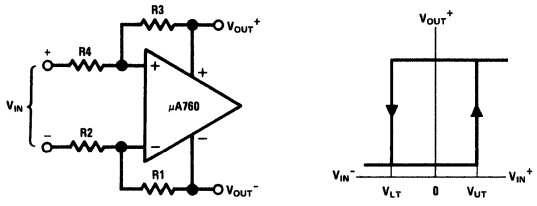


FIGURE 9. Direct Interfacing to ECL



$$V_{UT} = V_{OH}\left(\frac{R2}{R1}\right) - V_{OL}\left(\frac{R4}{R3}\right)$$

$$V_{LT} = V_{OL}\left(\frac{R2}{R1}\right) - V_{OH}\left(\frac{R4}{R3}\right)$$

FIGURE 10. Level Detector with Hysteresis

DRIVING 7-SEGMENT LED DISPLAYS WITH NATIONAL SEMICONDUCTOR CIRCUITS

INTRODUCTION

There are many different information display technologies available today, including liquid crystals, gas-discharge tubes, fluorescent tubes, incandescent lamps, and light emitting diodes (LEDs). Each technology has its own particular drive requirement. This note will focus on 7-segment LED display drive requirements and demonstrate that National Semiconductor has a full line of display drivers that meet the requirements for most any 7-segment LED drive application.

WHY ARE LED DRIVERS NEEDED?

The purpose of 7-segment LED drivers is to act as an interface element between data input and the display. This interface is necessary when either the input data format or circuitry current capabilities do not allow direct connection between input and display. To satisfy these needs, National's 7-segment LED drivers are divided into two basic categories.

1. Internally decoded (BCD to 7-segment)
   DM5446A/DM7446A
   DM5447A/DM7447A
   DM5448/DM7448
   DM7856/DM8856
   DM8857
   DM7858/DM8858
2. Non-decoding, direct drive (MOS to 7-segment)
   DM75491 DM8864
   DM75492 DM8865
   DM8861 DM8866
   DM8863

Thus, National has circuits that will drive 7-segment LEDs from either fully decoded circuits or from non-decoded outputs.

CONFIGURATIONS AND CONSTRUCTION OF 7-SEGMENT LEDs

LEDs are segregated into two groupings with regard to construction, see Figure 1.

Common anode displays are constructed on a common substrate which forms the anode of the diodes, while each of the seven cathodes are bonded out to separate pins. The second type, common cathode, has the cathode fabricated on a common substrate with the anodes bonded out to individual pins. Due to these radically different configurations, drive circuits are usually tailored in their design for one or the other type. Tailoring in this respect means either sinking current (active low) or sourcing current (active high) when referenced to segment drive. In addition, drive requirements are quite variable because of LED light intensity requirements as well as digit size

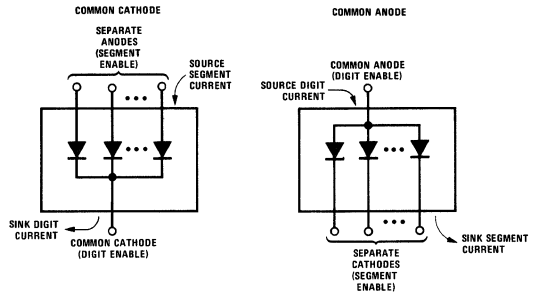


FIGURE 1. 7-Segment LED Construction

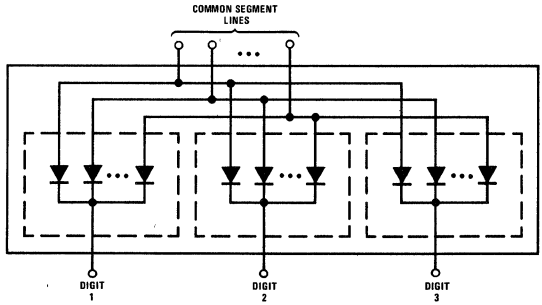


FIGURE 2. Multi-Digit 7-Segment LED

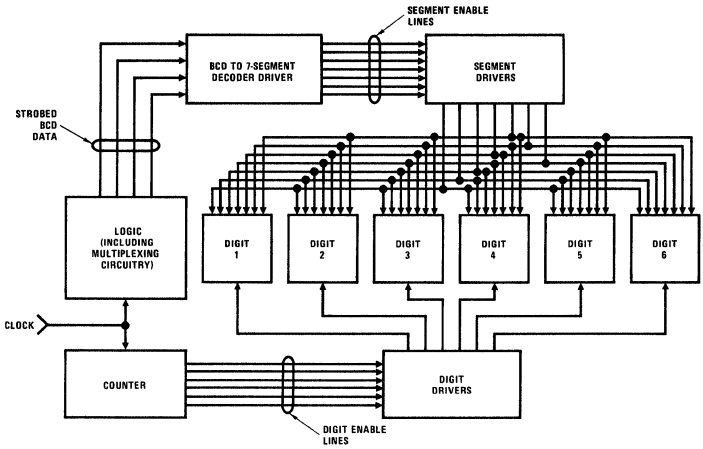


FIGURE 3. A Typical Multiplexing Scheme

and efficiency. Thus the system designer needs a degree of latitude not only with respect to the type of display used but also the drive current available.

7-segment LEDs can be purchased in either single or multi-digit display packages. Single digit displays have individual segment and common pins while multi-digits have paralleled segment pins and separate digit pins equal to the number of digits in the package, see Figure 2.

Multi-digit displays, due to their configuration, must be driven in a multiplex mode of drive, where segment drivers are time shared by all the digits. This is contrasted to the single digit displays which may be driven in either the multiplex or the non-multiplex (direct drive) mode. The nonmultiplex mode uses separate segment drivers for each digit of the display. Multiplex operation has a decided cost saving advantage over nonmultiplex operation especially when the number of digits being driven is large.

MODES OF 7-SEGMENT LED DRIVE

In the multiplex mode of drive the LED digits in a multi-digit format are driven by a single set of segment drivers while each digit is selected by its own digit driver. Figure 3 shows the circuitry needed to implement a typical six digit multiplexed display.

Each digit is selected individually by enabling its digit driver whose control is determined by a counter or equivalent circuitry operating at some clock frequency. Strobed data, by way of the counter and multiplex circuitry, is then displayed on the selected digit by the single set of segment drivers. If the strobe rate is high enough, from about 250 to 1,000 Hz depending on external conditions, the display will appear flicker free to the human eye. The BCD-to-7-segment decoder converts BCD data to the desired 7-segment output format.

In the multiplex mode each digit has a reduced duty cycle and is operated at somewhat higher than average or typical dc operating current levels. The amount of current will be a function of the number of digits, duty cycle, and the type and efficiency of the display used. Since currents are higher than average so also will be the LED brightness due to the nearly linear brightness versus current curve for most LEDs. The human eye will detect the brightness peaks and through a partially integrating and peak detecting action will perceive a higher display brightness at some average current level in the multiplex mode than the same average current in the nonmultiplex (direct drive) mode. The result is that a multiplexed display will operate at a lower total power than the same display operated in the nonmultiplex mode with the same apparent brightness.

In the nonmultiplex mode of 7-segment LED drive each digit has its own set of segment drivers thereby dropping the digit driver select requirement of multiplexed operation. In this case, the common digit pin may be tied to the highest potential if common anode or the lowest if common cathode. It is evident that in a nonmultiplexed display the driver package count would be high since each digit requires its own set of segment and possibly decoder drivers. If a large number of digits are used the segment driver package count would equal the number of digits while in the multiplex mode this count is equal to one. Granted, in the multiplex mode additional control circuitry is required. Consideration of the relative cost of this circuitry in comparison to the segment decoder driver circuitry in the nonmultiplex mode results, in general, in the fact that if the number of digits in the display equals or is more than four, total package count and/or cost is less in the multiplex mode of drive.

In most MOS circuits multiplex operation is ideal since the counter, multiplexer, and BCD to 7-segment decoders or equivalent circuitry can usually be incorporated on the same chip along with calculator, clock or other function. In this case the only external interface components required would be the digit and segment drivers since MOS circuits are generally unable to sink or source the higher current required for most multiplex operations.

In summary, LED driver requirements for multiplex or nonmultiplex drive operation require either segment, digit or BCD to 7-segment drivers. Analysis of the particular system needs with regard to the number of digits and relative circuit costs should be the determining factor for multiplex or nonmultiplex operation. Circuit requirements for multiplex operation will in general require relatively high current capabilities.

NATIONAL'S 7-SEGMENT LED DRIVERS

Table I lists the 7-segment LED drivers available from National. Each circuits application is divided into groupings with respect to common anode or cathode, digit or segment, multiplex or nonmultiplex areas. Additionally, current capabilities are also specified for each product.

From the table it is evident that some of the circuits may be used in dual roles – both multiplex or nonmultiplex; common cathode or anode. In general, what will determine whether one drivers application is multiplex or nonmultiplex is that drivers current capability. The direction of current flow through the driver (source or sink) is the determining factor in dual application with regard to common anode or cathode.

Table II lists the operating temperature range and package types for the 7-segment LED drivers.

In the following sections each circuit is described in greater detail and typical applications are given.

BCD TO 7-SEGMENT DECODER DRIVERS

DM5446A/DM7446A, DM5447A/DM7447A, DM5448/DM7448

This family of BCD to 7-segment decoder drivers was designed for the most general possible display drive applications including display technologies other than LEDs. The difference between the circuits is in their output stage configurations. These differences will be discussed separately later.

The circuits convert the standard 4-bit BCD input to the popular 7-segment output format. All input BCD codes above 9 are decoded into unique patterns that verify operation. The circuits are TTL-DTL compatible and operate off of a single 5.0V supply.

Added features included in all circuits are a ripple blanking input pin as well as a lamp test pin for display turn on. In addition the blanking input/ripple blanking output pin may be used to modulate display intensity.

TABLE I. National 7-Segment LED Drivers

DEVICE NUMBER	COMMON CATHODE		COMMON ANODE		DIGIT DRIVER	SEGMENT DRIVER	INTERNAL DECODING	CURRENT CAPABILITY AND FEATURES
	Multiplex	Nonmultiplex	Multiplex	Nonmultiplex				
DM5446A/DM7446A DM5447A/DM7447A			X	X		X	X	Up to 40 mA Sink, Open Collector High Breakdown (30/15V) TTL Input Compatibility
DM5448/DM7448		X	X*	X*		X	X	1 3 mA Source, Adjustable Externally, TTL Input Compatibility
DM7856/DM8856		X	X*	X*		X	X	6 0 mA Typical Source, TTL Input Compatibility
DM8857	X	X				X	X	50 mA Typical Source, Externally Adjustable, TTL Input Compatibility
DM7858/DM8858	X	X				X	X	Adjustable Source Current 0 to 50 mA, TTL Input Compatibility patibility
DM75491	X	X	X	X	X	X		50 mA Source/Sink, 4 Drivers per Package, MOS Input Compatibility
DM75492	X		X	X	X	X**		250 mA Sink, 6 Drivers per Package, MOS Input Compatibility
DM8861	X	X	X	X	X	X		50 mA Source/Sink, 5 Drivers per Package, MOS Input Compatibility
DM8863	X		X	X	X	X**		500 mA Sink, 8 Drivers per Package, MOS Input Compatibility
DM8864	X		X	X	X	X**		50 mA Sink, 9 Drivers per Package, MOS Input Compatibility
DM8865	X		X	X	X	X**		50 mA Sink, 8 Drivers per Package, MOS Input Compatibility
DM8866	X		X	X	X	X**		50 mA Sink, 7 Drivers per Package, MOS Input Compatibility

*With the use of an external transistor/segment

**For common anode LED's

TABLE II. Operating Temperature Range and Package Type

DEVICE NUMBER	OPERATING TEMPERATURE RANGE		NUMBER OF PINS			PACKAGE TYPE		
	0°C to +70°C	−55°C to +125°C	14	16	18	Plastic Molded DIP (N)	Ceramic DIP (J)	Flat Pack (W)
DM5446A, DM5447A		X		X			X	X
DM7446A, DM7447A	X			X		X	X	X
DM5448		X		X			X	X
DM7448	X			X		X	X	X
DM7856		X		X			X	X
DM8856	X			X		X	X	X
DM8857	X			X			X	
DM7858		X		X			X	X
DM8858	X			X		X	X	X
DM75491	X		X			X	X	X
DM75492	X		X			X	X	X
DM8861	X				X	X		
DM8863	X				X	X		
DM8865	X				X	X		
DM8866	X				X	X		
DM8864	X		22			X		

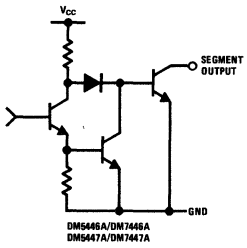


FIGURE 4a. Output Stage

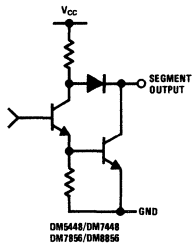
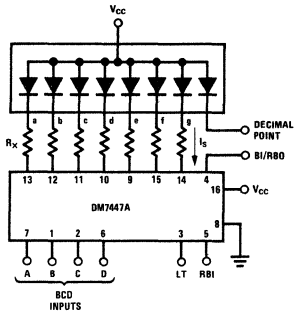


FIGURE 4b. Output Stage



THE FOLLOWING EQUATION MAY BE USED TO DETERMINE THE APPROPRIATE VALUE OF R_X (SEGMENT CURRENT LIMIT RESISTOR) FOR SOME LED CURRENT/SEGMENT I_S (mA).

$$R_X = \frac{V_{CC} - 0.3 - V_{LED\ (@\ I_S)}}{I_S}\ k\Omega$$

($I_S \leq 40$ mA)

WHERE $V_{LED\ (@\ I_S)}$ IS THE DIODE (LED) VOLTAGE DROP AT OPERATING CURRENT I_S

EXAMPLE:

$I_S = 20$ mA

$V_{LED\ (@\ I_S)} = 3.4V$*

$V_{CC} = 5.0V$

$R_X = 65\Omega$

*MAN-1 OR EQUIVALENT

FIGURE 5. Nonmultiplex Application of the DM7447A

DM5446A/DM7446A, DM5447A/DM7447A

These circuits feature active-low, open collector high current outputs (Figure 4a). Each output is capable of sinking up to 40 mA at a maximum internal drop of 0.4V. This high current capability makes these circuits particularly well suited for driving the large MAN-1 or equivalent type displays directly. The circuits are also applicable, with or without the use of external current limit resistors, to driving lower current displays in the multiplex mode of drive.

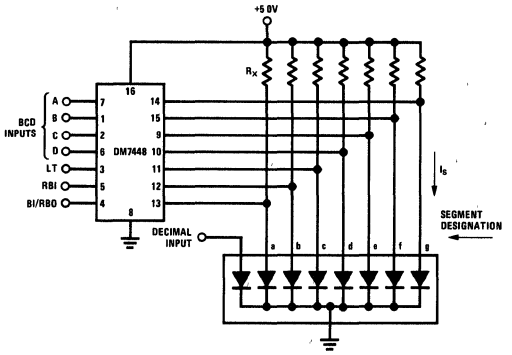
The DM5446A and DM7446A outputs are capable of withstanding 30V at a maximum leakage of 250μA over temperature. The DM5447A and DM7447A have a 15V output capability at a maximum leakage over temperature of 250μA. This standoff voltage ability makes the circuits applicable for direct drive to indicator lamp type displays. Figure 5 shows a typical application of the circuits with LEDs.

Refer to Table II for the operating temperature range and package types for the DM5446A/DM7446A and DM5447A/DM7447A.

DM5448/DM7448

The DM5448/DM7448 has active high passive pull-up outputs (Figure 4b) with a TTL fanout of 4. The typical output source current is 2.0 mA at an output voltage of 0.85V. Each output is capable of sinking 6.4 mA with a maximum internal drop of 0.4V. Since the output current level is low the circuit can be used to drive low current common cathode displays operating in the nonmultiplex mode.

The major application of the DM5448/DM7448 is to drive logic circuits, operate high-voltage loads such as electroluminescent displays through buffer transistors or SCR switches, or high-current



R_X MAY BE CALCULATED USING THE FOLLOWING EQUATION

$$R_X = \frac{5.0 - V_{LED}}{I_S - 1.6}\ k\Omega = \frac{3.3}{I_S - 1.6}\ k\Omega \quad \left[\begin{array}{l} V_{LED} = 1.7V\ @\ 5.0\ mA \\ R_X \geq 650\Omega \end{array}\right]$$

WHERE:

R_X = PULL-UP RESISTOR VALUE

I_S = CURRENT PER SEGMENT IN mA

EXAMPLE:

I_S = 5.0 mA

R_X = 970Ω

FIGURE 6. Nonmultiplex Application of the DM7448

loads through buffer transistors. Figure 6 shows the DM7448 in a low current direct drive LED application.

The operating temperature range and package types for the DM5448/DM7448 are given in Table II.

BCD TO 7-SEGMENT LED DRIVERS

DM7856/DM8856, DM8857, DM7858/DM8858

This series of three circuits was designed to provide a wide range of current capabilities in driving common cathode 7-segment LEDs operating in the multiplex or nonmultiplex mode. The circuits, discussed individually below, have output stages with varying source current capability designed for specific as well as general applications.

All circuits accept 4-bit BCD and decode this input to the desired 7-segment output format for direct drive to LEDs. In addition, the circuits feature a lamp test pin for display turn-on check, ripple blanking-input pin and blanking input/ripple blanking output pin which may be used to modulate display intensity.

The three circuits are TTL-DTL compatible and provide full decoding of the 16 possible input combinations. All parts operate off of a single 5.0V supply.

DM7856/DM8856

The DM7856/DM8856 output stages, passive-pullup (active high, Figure 4b), provide a typical source current of 6.0 mA at an output voltage of 1.7V. This current level was designed for directly driving, without the use of external current limit resistors, the MAN-4 or equivalent type displays in the nonmultiplex mode of operation.

Each output has a fan-out of 4 and is capable of sinking 6.4 mA with a maximum internal drop of 0.4V making the circuit suitable for use with logic circuits. With the use of an external buffer transistor per output the circuit may be used to drive high current common anode LED displays as well as high voltage electroluminescent displays. Figure 7 shows a typical application of the DM8856.

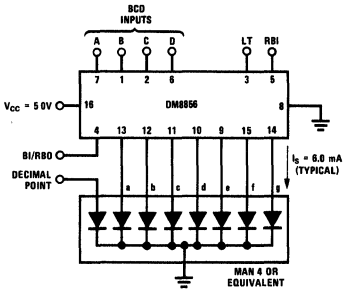


FIGURE 7. Nonmultiplex Application of the DM8856

Operating temperature range and package types for the DM7856/DM8856 are given in Table II.

DM8857

The output stages of the DM8857, active pull-up (active-high, Figure 4c), source a typical current

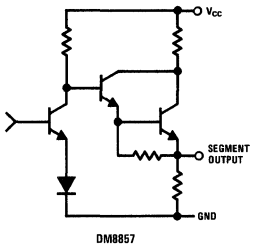


FIGURE 4c. Output Stage

of 50 mA at an output voltage of 2.3V. The circuit was designed to be used with MAN-4 or equivalent type displays operating in the multiplex mode of drive. With this high current capability the circuit can drive up to 16 such digits.

The applications of this circuit obviously are not limited to just the MAN-4 type of display. Common cathode displays with high dc current requirements or lower multiplex current levels may be driven by this circuit with the use of an external current limit resistor per segment. A typical application of the DM8857 is given in Figure 8.

Table II gives the operating temperature range and package type for the DM8857.

DM7858/DM8858

The DM7858/DM8858 output stages are active pull-up (active-high, Figure 4d) like those of the

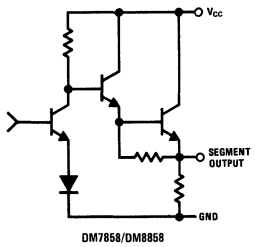
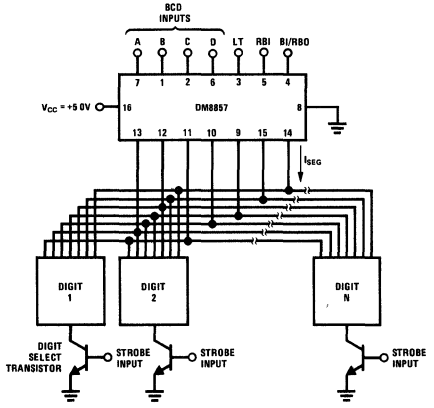


FIGURE 4d. Output Stage

DM8857. The output stages are exactly the same as the DM8857 except that the internal current limit resistor per output has been removed. External current limit resistors must then be used. This allows the circuit to be customized for a particular common cathode multiplex or non-multiplex application. Each output stage, through its own external resistor, can be programmed to some current from 50 mA down to 0 mA. Care must be taken in not shorting the outputs to ground because of the excessive current flow that would result from the Darlington upper stage. See Figure 9 for a typical application of the DM8858.



FOR MULTIPLEX OR NONMULTIPLEX APPLICATIONS WHERE AN EXTERNAL CURRENT LIMIT RESISTOR PER SEGMENT IS REQUIRED SEE THE OUTPUT CURRENT VS VOLTAGE CURVE FOR THE DM8857 AND USE THE EQUATION GIVEN IN FIGURE 9 TO CALCULATE THE RESISTOR VALUE

DM8857 Output Current vs Voltage

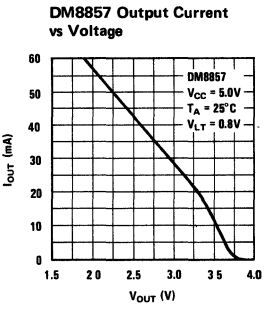


FIGURE 8. DM8857 Typical Multiplexing Scheme

Maximum output source current per segment for the DM7858/DM8858 is 50 mA. Operating temperature range and package types are given in Table II.

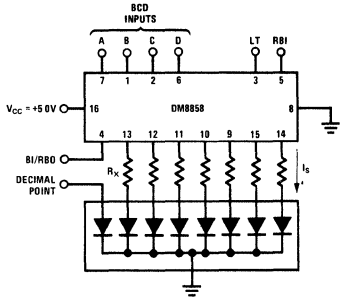
Special care must be taken in the use of the DM7858 ceramic and the DM8858 plastic DIP's with regard to not exceeding the maximum operating junction temperature of the devices. The maximum junction temperature of the DM7858J is 150°C and must be derated based on a thermal resistance of 80°C/Watt, junction to ambient. The maximum junction temperature for the DM8858N is 150°C and must be derated based on a thermal resistance of 140°C/Watt, junction to ambient.

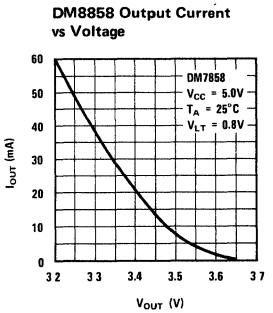
DM75491, DM8861 MOS TO LED SEGMENT DRIVERS

The DM75491 and DM8861 were designed for MOS calculator applications. Both circuits feature low input current, 3.3 mA maximum at 10V input, making them suitable for direct drive from MOS circuits. The circuits are used to drive the paralleled segments in multi-digit displays. Since both circuits feature accessable collectors and emitters they may be used as either common cathode or anode segment drivers. They feature a source or sink current capability of up to 50 mA with a maximum collector to emitter drop of 1.5V over the operating temperature range. In addition, each output is specified to have a maximum leakage of 100μA at an output voltage of 10V over temperature. Both circuits operate from a single supply that can have a maximum voltage of 10V.

DM75491 FOUR SEGMENT DRIVER

The DM75491 is a four segment driver whose main application is with multi-digit LEDs operating in the multiplex mode of drive. Each package contains four separate segment drivers, each driver





TO FIND THE APPROPRIATE VALUE OF THE SEGMENT CURRENT LIMIT RESISTOR R_X THE FOLLOWING EQUATION SHOULD BE USED

$$R_X = \frac{V_{OUT} - V_D}{I_S}$$

WHERE

I_S = SEGMENT CURRENT

V_D = LED DIODE DROP AT CURRENT I_S

V_{OUT} = DM8858 OUTPUT VOLTAGE AT CURRENT I_S (SEE GRAPH)

EXAMPLE

I_S = 50 mA

V_D = 1.7V (AT 50 mA)

FROM GRAPH (V_{CC} = 5.0V, T_A = 25°C)

V_{OUT} = 3.53V (AT 50 mA)

$$R_X = \frac{3.53V - 1.7V}{50\ mA}$$

R_X = 36Ω

THE SAME EQUATION MAY BE USED WHEN EITHER THE DM7858 OR THE DM8858 ARE OPERATING IN THE MULTIPLEX MODE OF DRIVE IF THE ADDITIONAL VOLTAGE DROP DUE TO THE DIGIT DRIVER IS TAKEN INTO CONSIDERATION THE NEW EQUATION WOULD HAVE THE FOLLOWING FORM

$$R_X = \frac{V_{OUT} - V_D - V_{DR}}{I_S}$$

V_{DR} = DIGIT DRIVER DROP AT CURRENT I_S

FIGURE 9. DM8858 Applications

with free collector and emitter points, see Figure 4e.

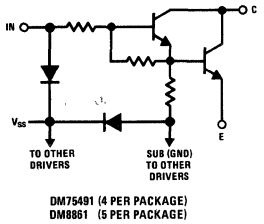


FIGURE 4e. Circuit Schematic

In the multiplex mode of drive, a six digit calculator needs only two DM75491's to drive the segments in the display, see Figure 10. The total of eight segment drivers allows drive to each of the individual seven segments plus logic control for the decimal point. Figure 11 shows the DM75491 used in an 8 digit calculator application.

Table II lists the package type and temperature range of the DM75491.

DM8861 FIVE SEGMENT DRIVER

The DM8861 is a five segment driver which like the DM75491 is used with multi-digit LEDs operating in the multiplex mode of drive. Each package contains five separate drivers, each driver with free collector and emitter points, Figure 4e.

A typical application of the DM8861 is given in Figure 11 where the DM8861 is combined with the DM75491 to provide a total of nine independent sources of LED segment current from an MOS calculator. This allows control of the 7-segments plus decimal point and minus sign. This combination of circuits is not solely applicable to just the 8 digit calculator configuration shown but can be used with a display having as many digits as desired as long as the multiplexed segment current requirement does not exceed 50 mA.

As with the DM75491, the DM8861 is also applicable to use with common anode displays as well as common cathode since each driver has its collector bonded out to a separate pin.

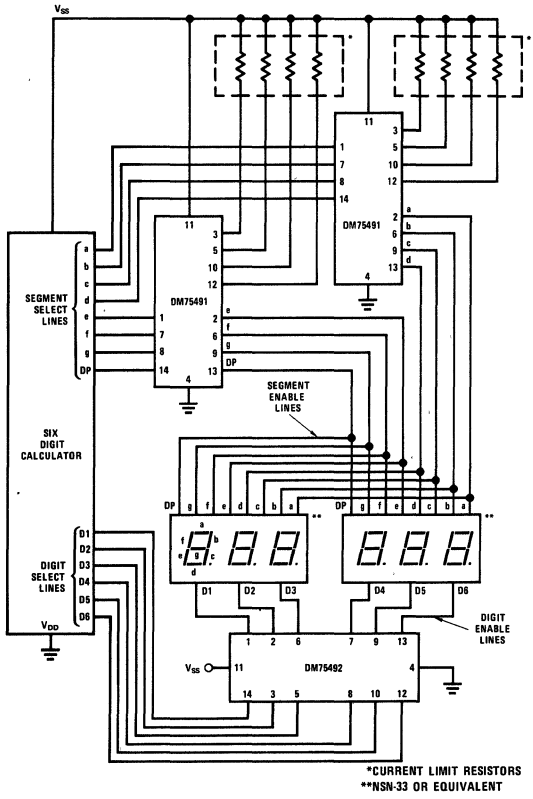


FIGURE 10. 6-Digit Calculator

Refer to Table II for operating temperature range and package type for the DM8861.

DM75492, DM8863 MOS TO LED DIGIT DRIVERS

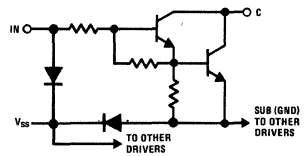
The DM75492 and DM8863 are digit drivers designed to drive multi-digit common cathode LEDs directly from MOS circuits. Since digit currents are quite high in multiplex operation MOS circuits usually cannot sink the required digit select current, therefore these circuits provide the required current buffering. The two circuits have different current handling capability as well as different numbers of drivers per package, each will be discussed individually later.

The circuits are totally compatible for use with both the DM75491 and the DM8861. The most common usage of the circuits is in MOS calculator applications where the DM75491 or the DM8861 source the segment current and either the DM75492 or the DM8863 sink the digit current.

DM75492 SIX DIGIT DRIVER

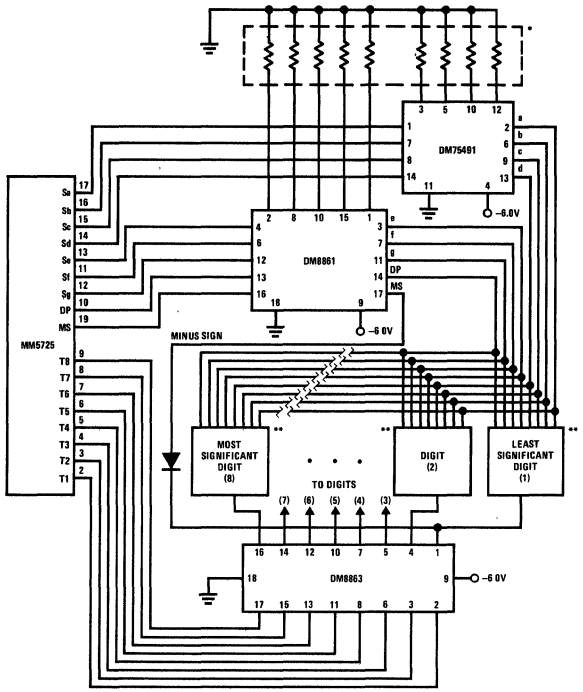
The DM75492 is a six digit LED driver designed to be used with common cathode multi-digit displays operating in the multiplex mode of drive.

The circuit features six high gain Darlington connected transistors, with collectors open and emitters tied to ground (Figure 4f), capable of sinking up to 250 mA with a maximum collector to ground drop of 1.5V over the operating temperature range. Low input current of 3.3 mA maximum at 10V makes the drivers suitable for direct connection to MOS circuits. Output leakage is 200μA maximum at 10V over temperature. Maximum V_{CC} is 10V.



DM75492 (6 PER PACKAGE)
DM8863 (8 PER PACKAGE)

FIGURE 4f. Circuit Schematic



*SEGMENT CURRENT LIMIT RESISTORS
**EITHER SINGLE DIGIT, MULTI-DIGIT, NSN 33, OR EQUIVALENT

FIGURE 11. 8-Digit Calculator

In Figure 10 the DM75492 is shown along with the DM75491 in a typical six digit calculator application. Since the calculator circuit shown is operated in the multiplex mode of drive only one DM75492 is required, replacing at least six transistors and resistors for the equivalent discrete circuit.

The operating temperature range and package type for the DM75492 is given in Table II.

DM8863 EIGHT DIGIT DRIVER

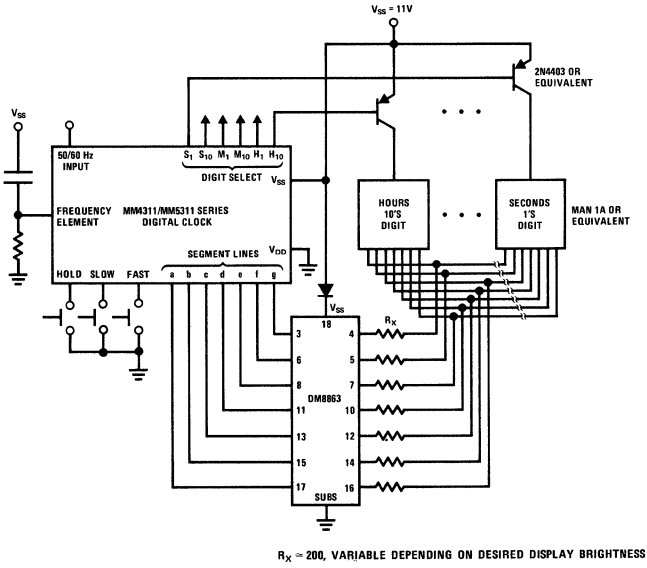
The DM8863 is an eight digit LED driver designed to be used in conjunction with either the DM75491 and/or the DM8861 in driving eight common cathode LED digits operating in the multiplex mode of drive.

This circuit features eight separate high gain Darlington connected transistor circuits, see Figure 4f. Each Darlington transistor pair is capable of sinking 500 mA with a maximum collector to ground drop of 1.6V. Each collector can withstand 10V at a maximum leakage of 250μA in the off state. Maximum input current is 2.0 mA at 10V, making the circuit particularly well suited for direct drive from MOS circuits.

Figure 11 shows the DM8863 used in a typical 8-digit calculator application. The important feature of the DM8863 is the very high sink current capability. This allows multiplex operation of large digits or large numbers of digits without the use of discrete high current transistors.

Another application of the DM8863 is shown in Figure 12. In this case the DM8863 is used along with the MM4311/MM5311 series digital clock circuits in the implementation of a 6-digit clock display. Here the DM8863 is used as a segment driver for a common anode display. The use of the DM8863 in this manner replaces a total of 14 resistors and 7 transistors.

The DM8863 uses a single supply with a maximum voltage of 10V. Table II specifies the operating temperature range and package type for the DM8863.



$R_X \approx 200$, VARIABLE DEPENDING ON DESIRED DISPLAY BRIGHTNESS

FIGURE 12. Digital Clock Using DM8863

DM8864, DM8865, DM8866 MOS TO LED DIGIT DRIVERS

The DM8864, DM8865, and DM8866 were designed to drive common cathode nine, eight, and seven digit displays respectively. The applications of these drivers are similar to those of the DM75492 and DM8863 except that operating current levels are lower.

All circuits feature maximum input current of 2.0 mA at a voltage of 6.5V. Output sink capability is 50 mA at a maximum collector to ground drop of 1.5V. Output leakage is 40μA (max) at an output voltage of 6.0V. All circuits operate from a supply that can vary from 5.0V to 9.5V.

DM8864 NINE DIGIT DRIVER

The DM8864 is a nine digit common cathode LED driver. Each package contains nine separate digit drivers. The circuit also features a "low battery" indicator driver which will light a decimal point whenever a 9.0V battery drops below 6.5V typical.

Figure 13 shows the DM8864 in a typical calculator drive application. The operating temperature range and package type for the DM8864 is given in Table II.

DM8865 EIGHT DIGIT DRIVER

The DM8865 is an eight digit common cathode LED driver. Eight separate drivers are contained within each package. As with the DM8864 and DM8866 the DM8865 can also be used as a segment driver for common anode displays in the multiplex or nonmultiplex mode as long as the segment current does not exceed 50 mA.

Table II gives the operating temperature range and package type for the DM8865.

DM8866 SEVEN DIGIT DRIVER

The DM8866 is a seven digit common cathode LED driver. Each package contains seven separate digit drivers. Logic is also provided for a "low battery" indicator which will detect a 9.0V battery drop to below 6.5V typical and drive a decimal point.

Table II lists the package type and temperature range of the DM8866.

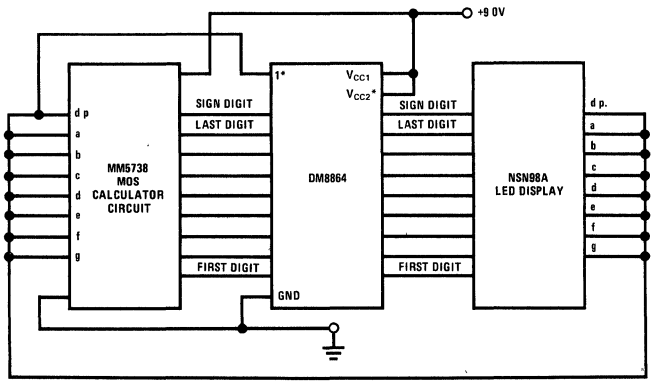


FIGURE 13. A Typical Application of the DM8864, Showing a Complete 8-Digit, 5 Function Calculator with Memory.

TRANSMISSION LINE CHARACTERISTICS

INTRODUCTION

Digital systems generally require the transmission of digital signals to and from other elements of the system. The component wavelengths of the digital signals will usually be shorter than the electrical length of the cable used to connect the subsystems together and, therefore, the cables should be treated as a transmissions line. In addition, the digital signal is usually exposed to hostile electrical noise source which will require more noise immunity then required in the individual subsystems environment.

The requirements for transmission line techniques and noise immunity are recognized by the designers of subsystems and systems, but the solution used vary considerably. Two widely used example methods of the solution are shown in *Figure 1*. The two methods

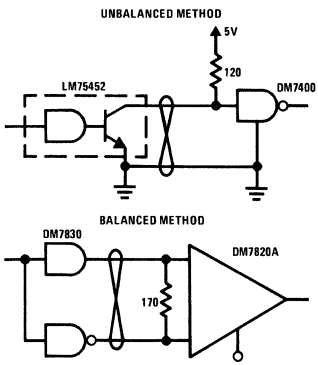


FIGURE 1.

illustrated use unbalanced and balanced circuit techniques. This application note will delineate the characteristics of digital signals in transmission lines and characteristics of the line that effect the quality, and will compare the unbalanced and balanced circuits performance in digital systems.

NOISE

The cables used to transmit digital signals external to a subsystem and in route between the subsystem, are exposed to external electromagnetic noise caused by switching transients from actuating devices of neighboring control systems. Also external to a specific subsystem, another subsystem may have a ground problem which will induce noise on the system, as indicated in *Figure 2*.

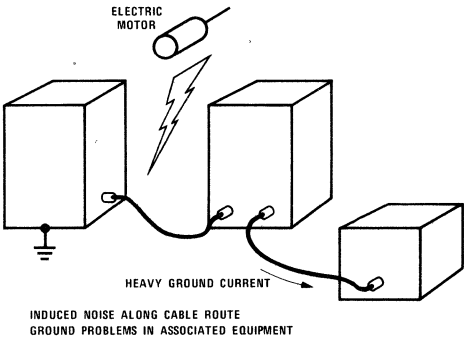


FIGURE 2. External Noise Sources

The signals in adjacent wires inside a cable may induce electromagnetic noise on other wires in the cable. The induced electromagnetic noise is worse when a line terminated at one end of the cable is near to a driver at the same end, as shown in *Figure 3*. Some noise may be

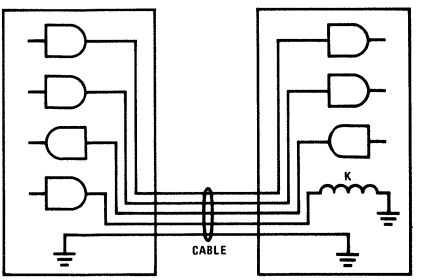


FIGURE 3. Internal Noise Sources

induced from relay circuits which have very large transient voltage swings compared to the digital signals in the same cable. Another source of induced noise is current in the common ground wire or wires in the cable.

DISTORTION

The objective is the transmission and recovery of digital intelligence between subsystems, and to this end, the characteristics of the data recovered must resemble the data transmitted. In *Figure 4* there is a difference in the pulse width of the data and timing signal transmitted, and the corresponding signal received. In addition there is a further difference in the signal when the data is "AND"ed with the timing signal. The distortion of the signal occurred in the transmission line and in the line driver and receiver.

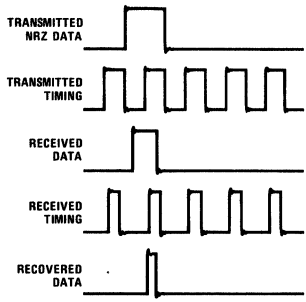


FIGURE 4. Effect of Distortion

A primary cause of distortion is the effect the transmission line has on the rise time of the transmitted data. *Figure 5* shows what happens to a voltage step from the driver as it travels down the line. The rise time of the signal increases as the signal travels down the line. This effect will tend to affect the timing of the recovered signal.

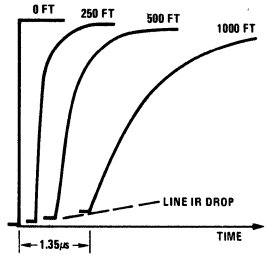


FIGURE 5. Signal Response at Receiver

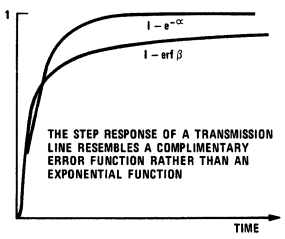


FIGURE 6. Signal Rise Time

The rise time in a transmission line is not an exponential function but a complementary error function. The high frequency components of the step input are attenuated and delayed more than the low frequency components. This attenuation is inversely proportional to the frequency. Notice in *Figure 6* particularly that the signal takes much longer to reach its final dc value. This effect is more significant for fast risetimes.

The Duty Cycle of the transmitted signal also causes distortion. The effect is related to the signal rise time as shown in *Figure 7*. The signal doesn't reach one logic level before the signal changes to another level. If the signal has a 1/2 (50%) Duty Cycle and the threshold of the receiver is halfway between the logic levels, the distortion is small. But if the Duty Cycle is 1/8 as shown in the second case the signal is considerably distorted. In some cases, the signal may not reach the receiver threshold at all.

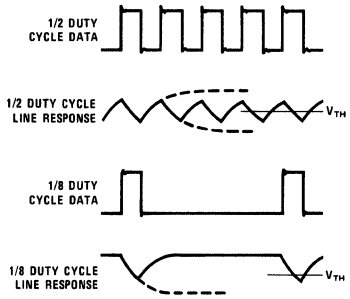


FIGURE 7. Signal Distortion Due to Duty Cycle

In the previous example, it was assumed that the threshold of the receiver was halfway between the ONE and ZERO logic levels. If the receiver threshold isn't halfway the receiver will contribute to the distortion of the recovered signal. As shown in *Figure 8*, the pulse time is lengthened or shortened, depending on the polarity of the signal at the receiver. This is due to the offset of the receiver threshold.

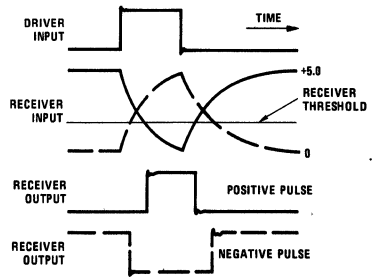


FIGURE 8. Slicing Level Distortion

UNBALANCED METHOD

Another source of distortion is caused by the IR losses in the wire. *Figure 9* shows the IR losses that occur in a thousand feet of no. 22 AWG wire. Notice in this

example that the losses reduce the signal below the threshold of the receiver in the unbalanced method. Also that part of the IR drop in the ground wire is common to other circuits—this ground signal will appear as a source of noise to the other unbalanced line receivers in the system.

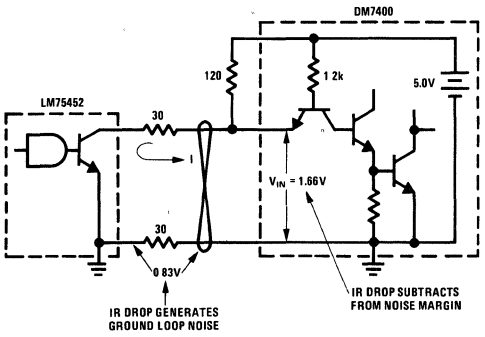


FIGURE 9. Unbalanced Method

Transmission lines don't necessarily have to be perfectly terminated at both ends, (as will be shown later) but the termination used in the unbalanced method will cause additional distortion. *Figure 10* shows the signal on the transmission line at the driver and at the receiver. In this case the receiver was terminated in 120Ω, but the characteristic impedance of the line is much less. Notice that the wave forms have significant steps due to the incorrect termination of the line. The signal is subject to misinterpretation by the line receiver during the period of this signal transient because of the distortion caused by Duty Cycle and attenuation. In addition, the noise margin of the signal is reduced.

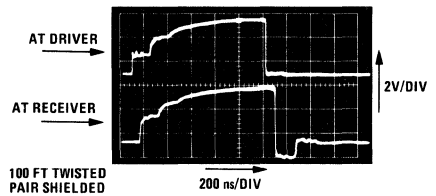


FIGURE 10. LM75451, DM7400 Line Voltage Waveforms

The signal waveforms on the transmission line can be estimated before hand by a reflection diagram. *Figure 11* shows the reflection diagram of the rise time wave forms. The voltage versus current plot on left is used to predict the transient rise time of the signal shown on the right. The initial condition on the transmission line is an IR drop across the line termination. The first transient on the line traverses from this initial point to zero current. The path it follows corresponds to the characteristic impedance of the line. The second transient on the diagram is at the line termination. As shown, the signal reflects back and forth until it reaches its final dc value.

Figure 12 shows the reflection diagram of the fall time. Again the signal reflects back and forth between the line termination until it reaches its final dc value. In both the rise and fall time diagrams, there are transient voltage and current signals that subtract from the particular signal and add to the system noise.

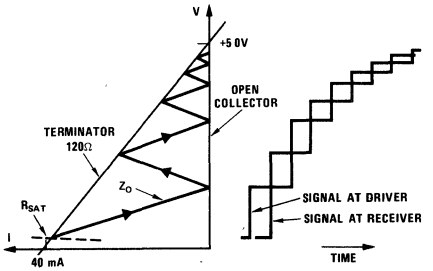


FIGURE 11. Line Reflection Diagram of Rise Time

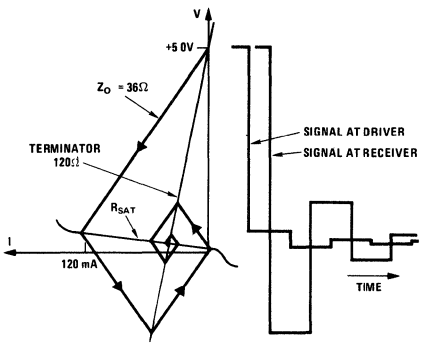
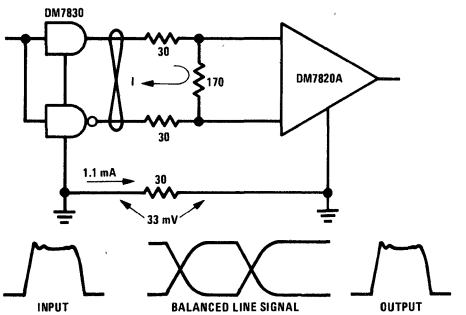


FIGURE 12. Line Reflection Diagram of Fall Time

BALANCED METHOD

In the balanced method shown in *Figure 13*, the transient voltages and currents on the line are equal and



THE GROUND LOOP CURRENT IS MUCH LESS THAN SIGNAL CURRENT

FIGURE 13. Cross Talk of Signals

opposite and cancel each others noise. Also unlike the unbalanced method, they generate very little ground noise. As a result, the balanced circuit doesn't contribute to the noise pollution of its environment.

The circuit used for a line receiver in the balanced method is a differential amplifier. *Figure 14* shows a noise transient induced equally on line A and line B from line C. Because the signals on line A and B are equal, the signals are ignored by the differential line receiver.

Likewise for the same reason, the differential signals on line A&B from the driver will not induce transients on line C. Thus, the balanced method doesn't generate noise and also isn't susceptible to noise. On the other hand the unbalanced method is more sensitive to noise and also generates more noise.

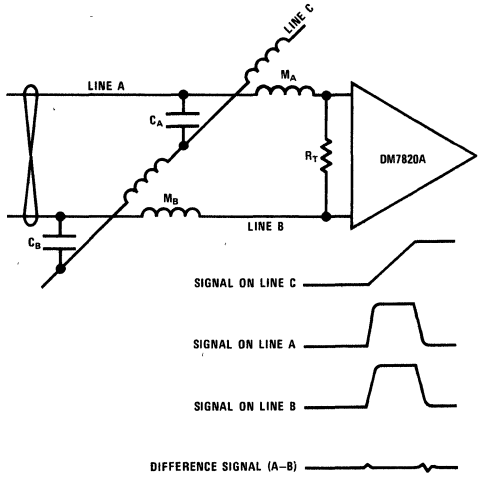


FIGURE 14. Cross Talk of Signals

The characteristic impedance of the unbalanced transmission line is less than the impedance of the balanced transmission line. In the unbalanced method there is more capacitance and less inductance than in the balanced method. In the balance method the Reactance to adjacent wires is almost cancelled (see *Figure 15*). As a result a transmission line may have a 60Ω unbalanced impedance and a 90Ω balanced impedance. This means that the unbalanced method, which is more susceptible to IR drop, must use a smaller value termination, which will further increase the IR drop in the line.

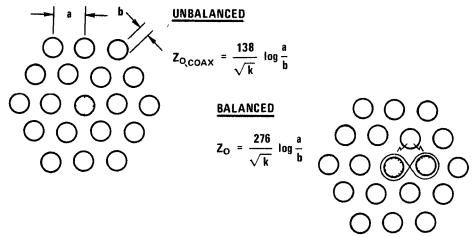


FIGURE 15. Z_O Unbalanced < Z_O Balanced

The impedance measurement of an unbalance and balance line must be made differently. The balanced impedance must be measured with a balanced signal. If there is any unbalance in the signal on the balanced line, there will be an unbalance reflection at the terminator. Therefore, the lines should also be terminated for unbalanced signals. *Figure 16* shows the perfect termination configuration of a balanced transmission line. This termination method is primarily required for accurate impedance measurements.

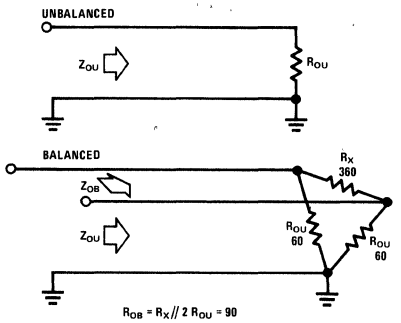


FIGURE 16. Impedance Measurement

The unbalanced method circuit used in this application note up to this point is the unbalanced circuit shown in *Figure 1*. The termination of its transmission line was greater than the characteristic impedance of the unbalanced line and the circuit had considerable threshold offset. The measured performance of the unbalanced circuit wasn't comparable to the balanced method. Therefore, for the following comparison of unbalanced and balanced circuits, an improved termination shown in *Figure 17* will be used. This circuit terminates the line in 60Ω and minimized the receiver threshold offset.

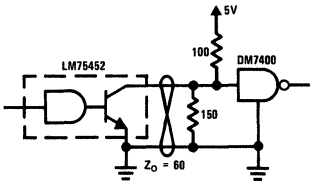


FIGURE 17. Improved Unbalanced Method

A plot of the Absolute Maximum Data Rate versus cable type is shown in *Figure 18*. The graph shows the different performances of the DM7820A line receiver and

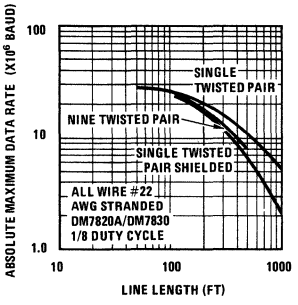


FIGURE 18. Data Rate vs Cable Type

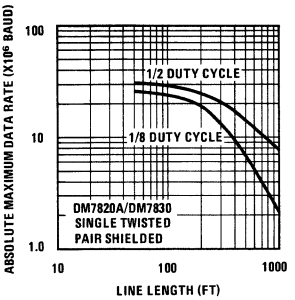


FIGURE 19. Data Rate vs Duty Cycle

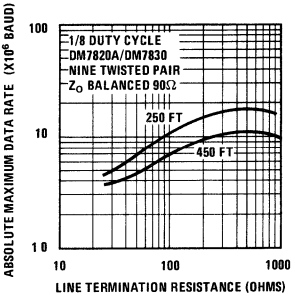


FIGURE 20. Data Rate vs Line Termination

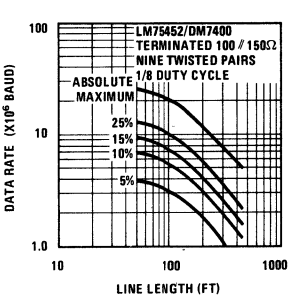


FIGURE 21. Data Rate vs Distorion of LM75452, DM7400

the DM7830 line driver circuits with a worse case 1/8 Duty Cycle in no. 22 AWG stranded wire cables. In a single twisted pair cable there is less reactance than in a cable having nine twisted pairs and in turn this cable has less reactance than shielded pairs. The line length is reduced in proportion to the increased line attenuation which is proportional to the line reactance. The plot shows that the reactance and attenuation has a significant effect on the cable length. Absolute Maximum Data Rate is defined as the Data Rate at which the output of the line receiver is starting to be degraded. The roll off of the performance above 20 mega baud is due to the circuit switching response limitation.

Figure 19 shows the reduction in Data Rate caused by Duty Cycle. It can be observed that the Absolute Maximum Duty Rate of 1/8 Duty Cycle is less than 1/2 Duty Cycle. The following performance curves will use 1/8 Duty Cycle since it is the worst case.

Absolute Maximum Duty Rate versus the Line Termination Resistance for two different lengths of cable is shown in *Figure 20*. It can be seen from the figure that the termination doesn't have to be perfect in the case of balanced circuits. It is better to have a termination resistor to minimize the extra transient signal reflecting between the ends of the line. The reason the Data Rate increases with increased Termination Resistance is that there is less IR drop in the cable.

The graphs in *Figure 21* shows the Data Rate versus the Line Length for various percentage of timing distortion using the unbalanced LM75452 and DM7400 circuits shown in *Figure 17*. The definition of Timing Distortion is the percentage difference in the pulse width of the data sent versus the data received.

Data Rate versus the Line Length for various percentage of timing distorition using the balanced DM7820A and DM7830 circuit is shown in *Figure 22*. The distortion of this method is improved over the unbalanced method, as was previously theorized.

The Absolute Maximum Data Rate versus Line Lengths shown in the previous two figures didn't include any induced signal noise. *Figure 23* shows the test configuration of the unbalanced circuits which was used to measure near end cross talk noise. In this configuration there are eight line drivers and one receiver at one end of the cable. The performance of the receiver measured in the presence of the driver noise is shown in *Figure 24*.

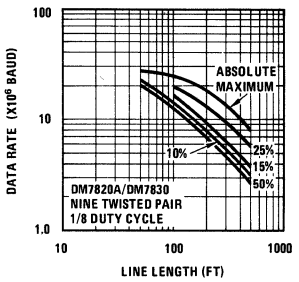


FIGURE 22. Data Rate vs Distorion of DM7820A, DM7830

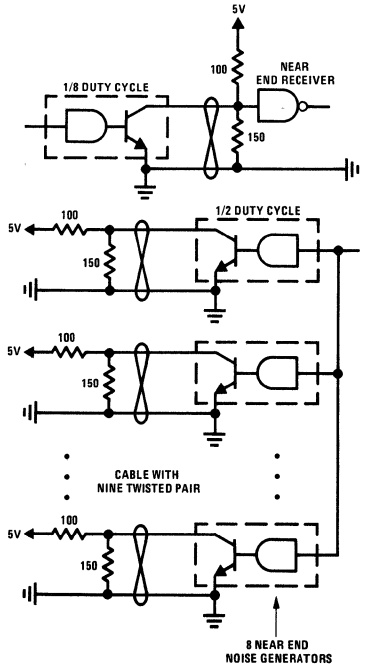


FIGURE 23. Signal Cross Talk Experiment Using DM75452, DM7400

Figure 24 shows the Absolute Maximum Duty Rate of the unbalanced method versus line length and versus the number of line drivers corresponding to the test configuration delineated in *Figure 23*. In the noise measurement set-up there was a ground return for each signal wire. If there is only one ground return in the cable the performance is worse. The graph shows that the effective line length is drastically reduced as additional Near End Drivers are added. When this performance is compounded by timing distortion the performance is further reduced.

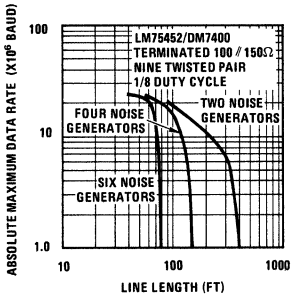


FIGURE 24. Data Rate vs Signal Cross Talk of LM75452, DM7400

Figure 25 shows the test configuration of the balanced circuit used to generate worst case Near End cross talk

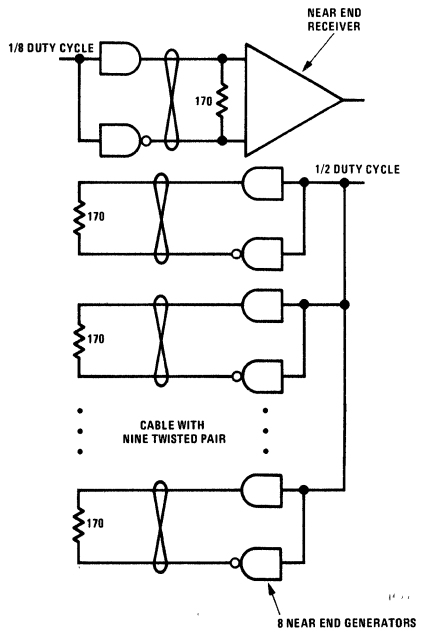


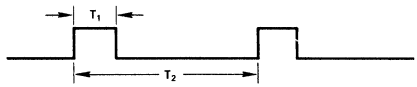
FIGURE 25. Signal Cross Talk Experiment Using DM7830, DM7820A

noise similar to the unbalance performance shown in the previous figure. Unlike the unbalanced case, there was no measurable degradation of the circuits Data Rate or distortion.

CONCLUSION

National has a full line of both Balanced and Unbalanced Line Drivers and Receivers. Both circuit types work well when used within their limitations. This application note shows that the balanced method is perferable for long lines in noisy electrical evironments. On the other hand the unbalanced circuit works perfectly well with shorter lines and reduced data rates. It should be kept in mind that when you are spending $500,000 for a CPU and $75,000 for peripherals, it pays to investigate the best way to transmit data between them.

DEFINITION OF BAUD RATE



$$\text{BIT RATE} = \frac{1}{\text{INTERVAL PER BIT}} = \frac{1}{T_2}$$

$$\text{BAUD RATE} = \frac{1}{\text{MINIMUM UNIT INTERVAL}} = \frac{1}{T_1}$$

The data in this note was plotted versus Baud Rate. The minimum unit interval reflected the worse case conditions and also normalized the diagrams so that the diagrams were independent of duty cycle. If the duty cycle is 50% then the Baud Rate is twice the Bit Rate.

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Reflection and Crosstalk in Logic, Circuit Interconnections, John DeFalco, Honeywell, Inc., *IEEE Spectrum*, July 1970.

MIL-STD-883/MIL-M-38510

MIL-STD-883

Mil-Standard-883 is a Test Methods and Procedures Document for Microelectronic Circuits. It was derived from MIL-S-19500, MIL-STD-750, and MIL-STD-202C for transistors and diodes at about the time that National Semiconductor Corporation was entering the military microelectronics market. As a result, our standard quality control operations are written around MIL-STD-883. The bonding control, visual inspections, and post seal screening requirements set forth by 883 (as well as added control procedures beyond the requirements of 883) have been part of National's quality control procedures almost from the start. Our Quality Assurance Procedures Manual is available upon request.

We offer a complete line of linear/883 (Class B) products as standard, off-the-shelf items. Special Linear/883 data sheets have been prepared to reflect this capability. They show process flow, electrical parameters, end of test criteria, and test circuits. We save you the problem of specifying test and inspection procedures, and offer significant cost savings by having an off-the-shelf, "to the letter" 883 program. In addition, we will test any of our integrated circuits to any class of MIL-STD-883.

The detailed information concerning MIL-STD-883 screening is contained in National's specification NSC10002.

MIL-M-38510

MIL-M-38510 specifies the general requirements for supplying microcircuits. These are; product assurance, which includes screening and quality conformance inspection; design and construction; marking; and workmanship. The screening and quality conformance inspection are conducted in accordance with MIL-STD-883.

SCREENING

All microcircuits delivered in accordance with MIL-M-38510 must have been subjected to, and passed all the screening tests detailed in Method 5004 of MIL-STD-883 for the type of microcircuit and product assurance level.

The device electrical and package requirements of MIL-M-38510 are detailed by a device specification referred to as a slash sheet. Each slash sheet defines the microcircuit electrical performance and mechanical requirements. Each device listed on a slash sheet is referred to as a slash number and the group of the microcircuits contained on a slash sheet is defined as a family of devices. The device may be Class B or C as defined by MIL-STD-883, Method 5004 and 5005. Three lead finishes are allowed by the slash sheet, pot solder dip, bright tin plate, and gold plate.

The MIL-M-38510 specs for standard linear devices require 100% DC testing at 25°C, −55°C and +125°C. AC testing is performed at +25°C. The electrical parameters specified are tighter than the normal data sheet guaranteed limits. Additionally, MIL-M-38510 requires device traceability, extensive documentation and closely matched maintenance.

QUALITY CONFORMANCE

Quality conformance inspection is conducted in accordance with the applicable requirements of Group A, (electrical test), Group B and C, (environmental test) of Method 5005, MIL-STD-883. These tests are conducted on a sample basis with Group A performed on each sublot, Group B on each lot, and Group C as specified (usually every three months).

To supply devices to MIL-M-38510, the IC manufacturer must quality the devices he plans to supply to the detail specifications. Qualification consists of notifying the qualifying activity of one's intent to qualify to MIL-M-38510. After passing comprehensive audits of facilities and documentation systems, the IC manufacturer will subject the device to and demonstrate that they satisfy all of

MIL-M-38510 (con't)

the Group A, B, and C requirements of Method 5005 of MIL-STD-883 for the specified classes and types of IC. The qualification tests shall be monitored by the qualifying agency. Finally the IC manufacturer shall prepare and submit qualification test data to the qualifying agency. Groups A, B, and C inspections then shall be performed at intervals no greater than three months.

The purpose of qualification testing is to assure that the device and lot quality conform to certain standard limits. In effect, lot qualification tests tend to ensure that once a particular device type is demonstrated to be acceptable, it's production, including materials, processing, and testing will continue to be acceptable. These limits are specified in MIL-STD-883 in terms of LTPD's (Lot Tolerance Percent Defective) for the various qualification test sub-groups. Qualification testing is performed on a sample of devices which are chosen at random from a lot of devices that has satisfactorily completed the screening of Method 5004 must be performed on each device, i.e. on a 100% basis as opposed to qualification testing (Method 5005) which occurs on a random sample basis.

In summary, the entire purpose of MIL-M-38510 and MIL-STD-883 is to provide the military, through its contractors with standard devices.

We at National Semiconductor have supplied and are supplying devices to the MIL-M-38510 specifications. To order a MIL-M-38510 microcircuit, specify the following:

For example; to specify an LM741 in a DIP processed to the requirements of MIL-M-38510, Class B, with gold plated leads, specify M-38510/10101BCC.

MM38510/	XXX	XX	X	X	X
Specifies the General Requirements of MIL-M-38510	Slash Sheet No.	Device Type	Device Class	Case Outline	Lead Finish

Definition of Terms

voltage comparators

Input Bias Current: The average of the two input currents.

Input Offset Current: The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

Input Offset Voltage: The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

Input Voltage Range: The range of voltage on the input terminals (common mode) over which the offset specifications apply.

Logic Threshold Voltage: The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

Negative Output Level: The negative DC output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

Output Leakage Current: The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

Output Resistance: The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

Output Sink Current: The maximum negative current that can be delivered by the comparator.

Positive Output Level: The high output voltage level with a given load and the input drive equal to or greater than a specified value.

Power Consumption: The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

Response Time: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Saturation Voltage: The low-output voltage level with the input drive equal to or greater than a specified value

Strobe Current: The current out of the strobe terminal when it is at the zero logic level.

Strobed Output Level: The DC output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

Strobe ON Voltage: The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

Strobe OFF Voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator

Strobe Release Time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

Supply Current: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

Voltage Gain: The ratio of the change in output voltage to the change in voltage between the input terminals producing it

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analog switches

Driver Leakage Current: The sum of the currents into the source and drain switch terminals, with both held at the same specified voltage.

Logic "1" Input Voltage: The voltage level which is guaranteed to be interpreted by the device as a logical "true" signal.

Logic "0" Input Voltage: The voltage level which is guaranteed to be interpreted by the device as a logical "false" signal.

Logic Input Slew Rate: The voltage difference between the logic "1" and logic "0" states divided by the transition time.

analog switches (con't)

Switch Leakage Current: The current seen when a specified voltage is applied between drain and source of a channel that is logically turned off.

Switch On Resistance: The equivalent resistance from source to drain, tested by forcing a specified current and measuring the resultant voltage drop.

Switch Turn-Off Time: The interval between the time that the logic input passes through the threshold voltage and the time that the output goes to a specified voltage level in the test circuit.

Switch Turn-On Time: The interval between the time that the logic input passes through the threshold voltage and the time that the output goes to 90% of its final value in the specified test circuit.

interface circuits

Common Mode Voltage: Arithmetic mean of voltages at the differential inputs referenced to ground pin at the receiver.

Common Mode Sensitivity: Rate of change of input differential voltage required to produce a given output level, against common mode voltage.

Supply Sensitivity: Rate of change of input differential voltage required to prodcue a given output level, against power supply voltage (V Pin 14 – V Pin 7).

Disabled Output Clamp Current: The current which flows from the output of a disabled TRI-STATE gate when it is dragged below ground (for instance by a transmission-line-associated transient). It is derived from the V_{CC} power rail.

sense amplifiers

AC Common-Mode Input Firing Voltage: The peak level of a common-mode pulse which will exceed the input dynamic range and cause the logic output to switch. Pulse characteristics: $t_r = t_f \leq 15$ ns, PW = 50 ns.

Common-Mode Input Overload Recovery Time: The time necessary for the device to recover from a ±2V common-mode pulse ($t_r = t_f = 20$ ns) prior to the strobe enable signal.

Differential Input Offset Current: The absolute difference in the two input bias currents of one differential input.

Differential Input Overload Recovery Time: The time necessary for the device to recover from a 2V differential pulse ($t_f = t_r = 20$ ns) prior to the strobe enable signal.

Differential Input Threshold Voltage: The DC input voltage which forces the logic output to the logic threshold voltage (~1.5V) level.

Input Bias Current: The DC current which flows into each input pin with differential input of 0V.

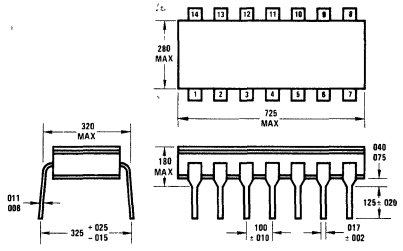
Supply Current: The total DC current per package drawn from the voltage supply.

Offset Voltage: Difference between the absolute values of threshold voltage in positive- and negative-going directions.

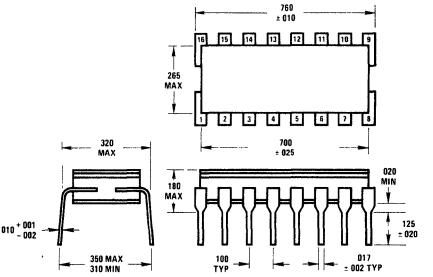
Propagation Delay Time: Interval from switching input through 1.5V to output traversing its 50% voltage point. Measured with 50Ω load to +10V 15 pF total capacitance.

Physical Dimensions

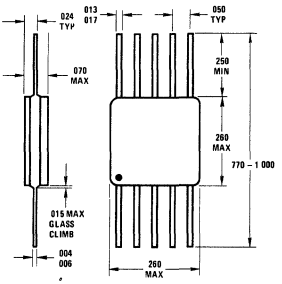
(All dimensions are in inches.)



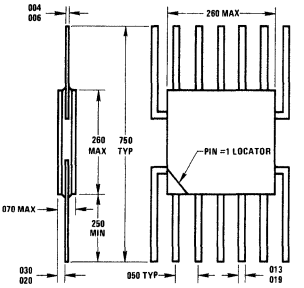
Package 1
14 Lead Cavity DIP (D)



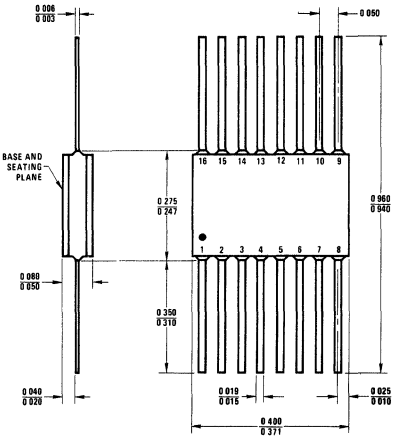
Package 2
16 Lead Cavity DIP (D)



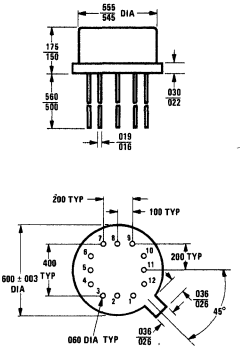
Package 3
10 Lead Flat Package (F)



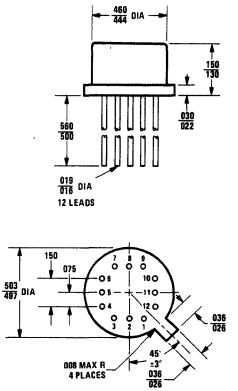
Package 4
14 Lead Flat Package (F)



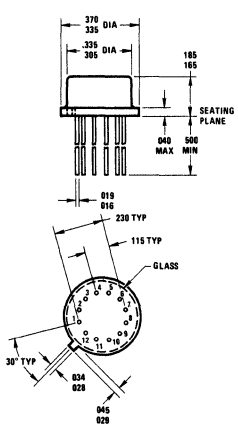
Package 5
16 Lead Flat Package (F)



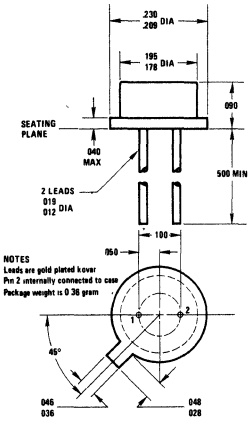
Package 6
12 Lead TO-8 Metal Can (G)



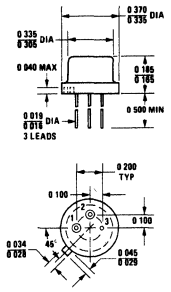
Package 6A
12 Lead TO-8 Metal Can (G)
(AH2114/AH2114C only)



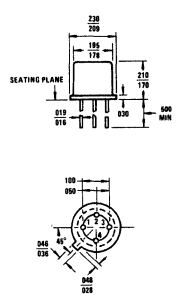
Package 7
12 Lead TO-8 Metal Can (H)



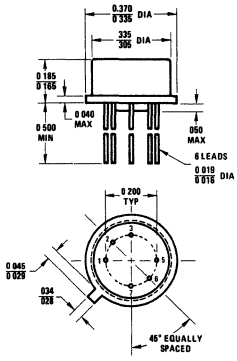
Package 8
2 Lead TO-46 Metal Can (H)



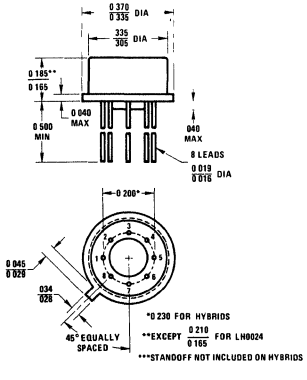
Package 9
3 Lead TO-5 Metal Can (H)



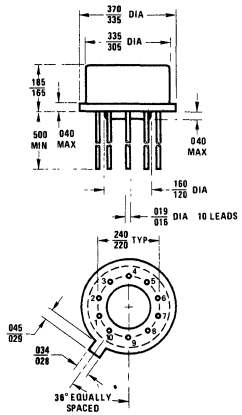
Package 9A
4 Lead TO-72 Metal Can (H)



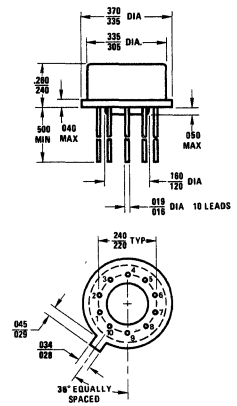
Package 10
6 Lead TO-5 Metal Can (H)



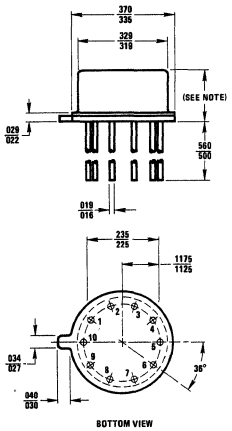
Package 11
8 Lead TO-5 Metal Can (H)



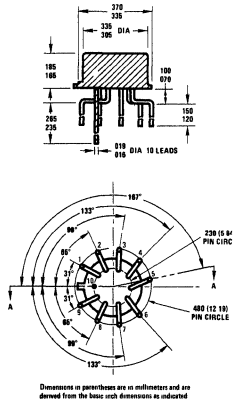
Package 12
10 Lead TO-5 Metal Can (H)
(Low Profile)



Package 13
10 Lead TO-5 Metal Can (H)
(High Profile)

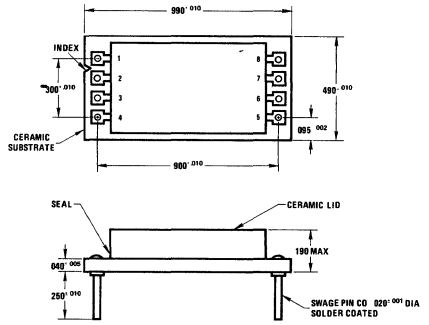


Package 14
10 Lead TO-5 Metal Can (H)

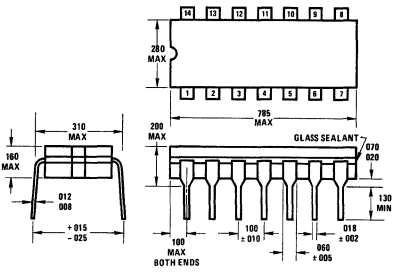


Package 14A
10 Lead Metal Can (H-03)

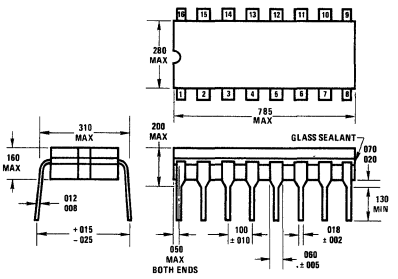
Note Dimension is $\frac{155}{185}$ for all products except as follows $\frac{260}{290}$ for LH0001H/LH0001CH,LH0003/LH000CH,and LH0004/LH0004CH $\frac{240}{260}$ for LH0005AH/LH0005H/LH0005CH, $\frac{180}{210}$ for MH0007H/MH0007CH



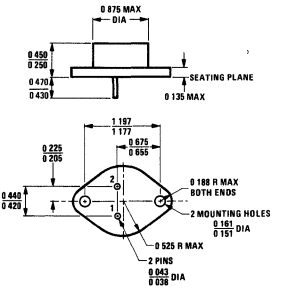
Package 15
8 Lead Cavity Package (J)



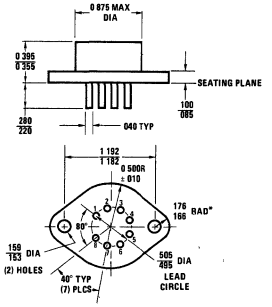
Package 16
14 Lead Cavity DIP (J)



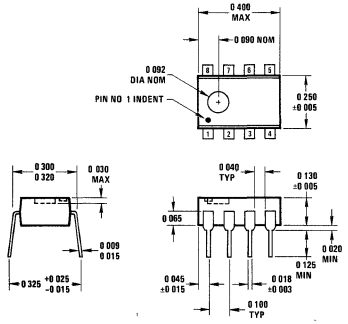
Package 17
16 Lead Cavity DIP (J)



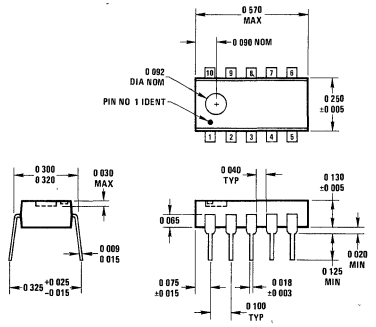
Package 18
2 Lead TO-3 Metal Can (K)



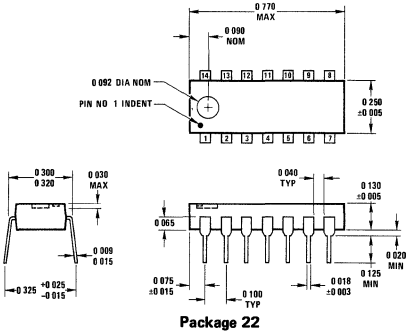
Package 19
8 Lead TO-3 Metal Can (K)



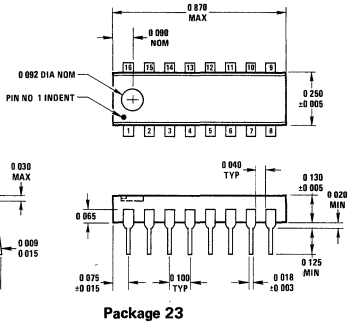
Package 20
8 Lead Molded Mini DIP (N)



Package 21
10 Lead Molded DIP (N)

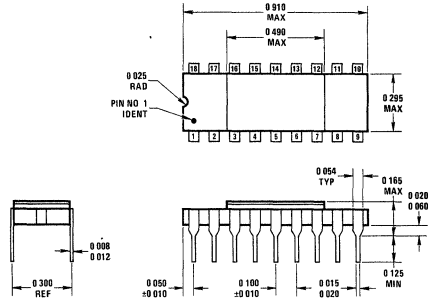


Package 22
14 Lead Molded DIP (N)

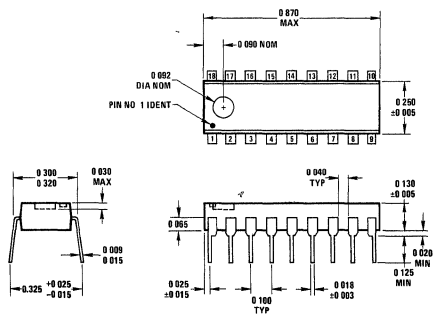


Package 23
16 Lead Molded DIP (N)

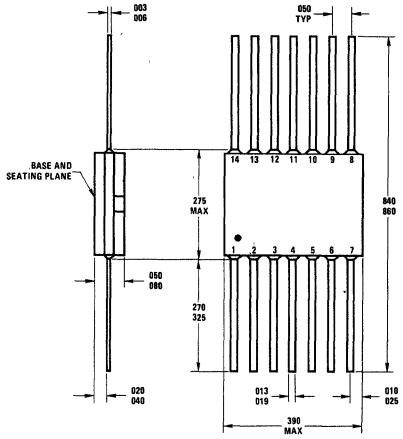
11



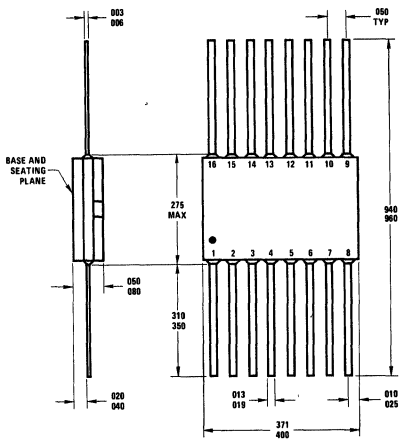
Package 24
18 Lead Cavity DIP (J)



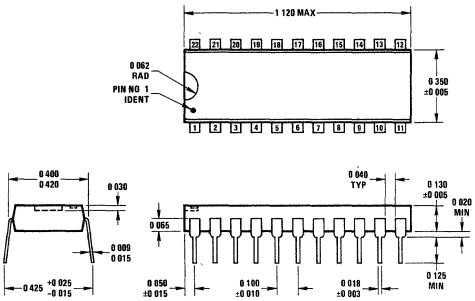
Package 25
18 Lead Molded DIP (N)



Package 27
14 Lead Flat Package (W)



Package 28
16 Lead Flat Package (W)



Package 29
22 Lead Molded DIP (N)

INCHES TO MILLIMETERS CONVERSION TABLE					
INCHES	MM	INCHES	MM	INCHES	MM
0 001	0 0254	0 010	0.254	0.100	2 54
0.002	0.0508	0.020	0 508	0.200	5 08
0.003	0.0762	0.030	0 762	0.300	7 62
0.004	0 1016	0 040	1.016	0 400	10 16
0.005	0.1270	0 050	1 270	0 500	12 70
0 006	0.1524	0 060	1 524	0 600	15.24
0.007	0 1778	0 070	1 778	0 700	17 78
0 008	0 2032	0 080	2 032	0 800	20.32
0 009	0 2286	0 090	2 286	0 900	22 86

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Telex: 778 632

NS Electronics (PTE) Ltd.
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Telephone: 630011
Telex: 21402

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