Signal Sources, Conditioners and Power Circuitry

Circuits of the Fall, 2004

Jim Williams

Introduction

Occasionally, we are tasked with designing circuitry for a specific purpose. The request may have customer origins or it may be an in-house requirement. Alternately, a circuit may be developed because its possibility is simply too attractive to ignore[1]. Over time, these circuits accumulate, encompassing a wide and useful body of proven capabilities. They also represent substantial effort. These considerations make publication an almost obligatory proposition and, as such, a group of circuits is presented here. This is not the first time we have displayed such wares and, given the encouraging reader response, it will not be the last[2]. Eighteen circuits are included in this latest effort, roughly arranged in the categories given in this publication's title. They appear at the next paragraph.

Voltage Controlled Current Source—Ground Referred Input and Output

A voltage controlled current source with ground referred input and output is difficult to achieve. Executions exist, but are often cumbersome, involving numerous components. Figure 1's conceptual design utilizes a differential amplifier featuring differential, uncommitted feedback inputs. The independent feedback inputs permit the differential signal inputs to operate anywhere inside their common mode range, unencumbered by feedback interaction. Similarly, the differential feedback ports may sense referred to any point within their common mode range. In both cases, common mode range extends from V^- to within 2V of the positive rail. Output swing extends to both rails.

The freedoms described above invite Figure 1's configuration. The amplifier is biased by a control voltage input, which feedback action impresses across the resistor. Scaling is set by the equation given, which will be recognized as a dressed version of Ohm's Law. Note that this

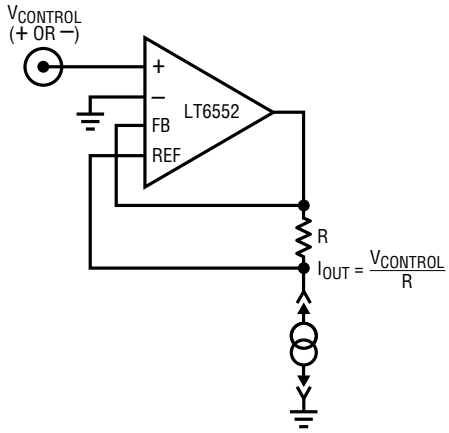


Figure 1. Conceptual Ground Referred Voltage Controlled Bipolar Current Source Utilizes Differential Amplifier's Separate Feedback Inputs. Compliance Limits are Imposed by Supply Voltage, Output Current Capacity and Input Common Mode Range

circuit will produce current outputs of either polarity, as dictated by the control input. Compliance limits are imposed by power supply voltage, output current capacity and input common mode range.

Figure 2 puts Figure 1's thesis to work. The test circuit (figure left) produces control signals to exercise the current source (figure right), which drives a capacitive load. Figure 3's waveforms describe circuit activity. Trace A is the clock, trace B A1's control input and trace C is capacitor voltage. The test circuit presents alternating polarity control inputs (trace B) after each Q1 directed capacitor reset to zero (trace C). The result, alternating, equal amplitude, opposed polarity linear capacitor ramps, clearly demonstrates the current sources capabilities.

Note 1. "When you see something technically sweet, you do it" (Robert J. Oppenheimer).

Note 2. Previous efforts of this ilk include AN45, AN52, AN61, AN66, AN67 and AN75. See References 14 to 19.

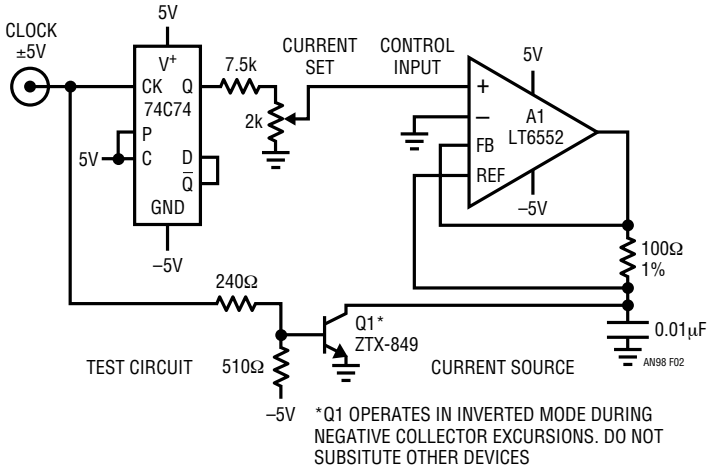


Figure 2. Practical Version of Figure 1 Sources Bipolar Current to Capacitive Load. Test Circuit Provides Bipolar Control Input and Resets Capacitor. Result is Alternating, Opposed Polarity Ramps Across Capacitor

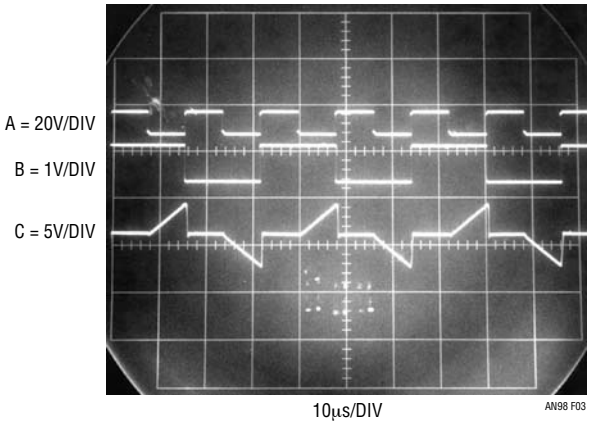


Figure 3. Voltage Controlled Current Source Test Circuit Waveforms Include Clock (Trace A), Control Input (Trace B) and Capacitor Voltage (Trace C). Bipolar Control Input Voltage Results in Complementary Capacitor Ramps

Stabilized Oscillator for Network Telephone Identification

Some telephone networks require an amplitude and frequency stabilized 100Hz carrier to indicate the status of any phone in the network. Figure 4, operating from a single 5V supply, provides this function using only two dual op amps and attendant discrete components. A1, a conventional multivibrator, operates at 100Hz. Its square and triangle outputs appear in Figure 5, traces A and B, respectively. The 100Hz triangle, heavily filtered by A2's 16Hz RC input pair, appears as a sine wave at A2's amplified output (trace C). A2's output, in turn, is applied to A3, configured as a half wave rectifier. A3's input attenuation keeps the sine wave's negative excursions within the amplifier's input range ($V_{CM(LIMIT)} = -0.3V$). Single rail powered A3's output can't track the sine wave's negative portion; it simply saturates within millivolts of ground, producing trace D's half-wave rectified output. This output, representing A2's amplitude, is compared to a DC reference by band-limited A4-Q1. Q1's collector biases A1's power pin, closing an amplitude stabilization loop which regulates the circuit's sine wave output. Sine wave distortion, appearing in trace E, is only 4% despite

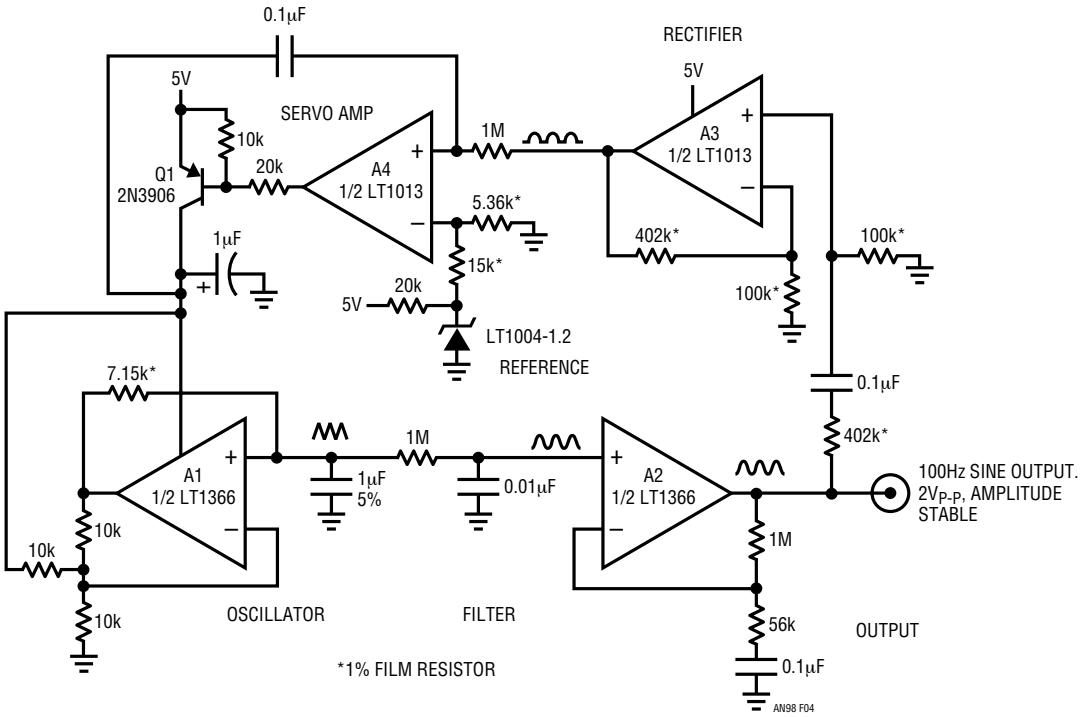


Figure 4. Amplitude/Frequency Stabilized Sine Wave Oscillator, Developed for Network Telephone Identification, Suits General Purpose Use. A1's Filtered Triangle Output Produces a $2V_{P-P}$ Sinewave at A2. A3's Rectified Output is Balanced Against Reference at A4. Q1 Closes Regulation Loop by Modulating A1's Power Pin

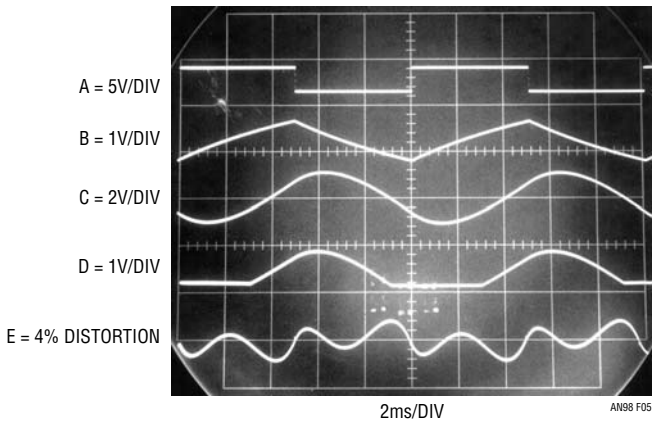


Figure 5. Figure 4's Waveforms Include A1's Square (Trace A) and Triangle (Trace B) Outputs, A2's Sinewave (Trace C), A3's Rectified Output (Trace D) and Distortion Residue (Trace E). 1M-0.01µF Filter at A2 Permits 4% Distortion, Despite Triangle Wave Infidelity

the originating triangle waves infidelity. Other specifications include less than 0.15% amplitude variation for supply shifts of 3.4V to 36V, frequency stability inside 0.01% over the same supply range and initial frequency accuracy of 6%.

Micro-Mirror Display Pulse Generator

Some "micro-mirror" displays require high voltage pulses for biasing. Pulse amplitude must be adjustable anywhere within a 0V to –50V window, with pulse top and bottom amplitude independently settable. Additionally, rise and fall times must be within 150ns into the 1500pF micro-mirror load, with absolutely no overshoot permissible. The input pulse is supplied from 5V powered positive going logic. These requirements dictate a very carefully considered level shifter.

Figure 6's circuit meets display requirements. The input pulse is applied to both sections of an LTC®1693 noninverting driver. The LTC1693 output reproduces the input pulse at a much lower source impedance. The LTC1693 output, referenced to the negative rail by the RC-diode combination, drives level shifter Q1. Q1, utilizing Baker clamping and base speed-up capacitance, provides wideband voltage gain with pulse amplitude set by collector and emitter supply potentials. Q1's collector capacitance is isolated by Q2-Q3. These transistors, in turn, drive output stage Q4-Q5 via a resistor. This resistor combines with Q4-Q5 input capacitance to control edge

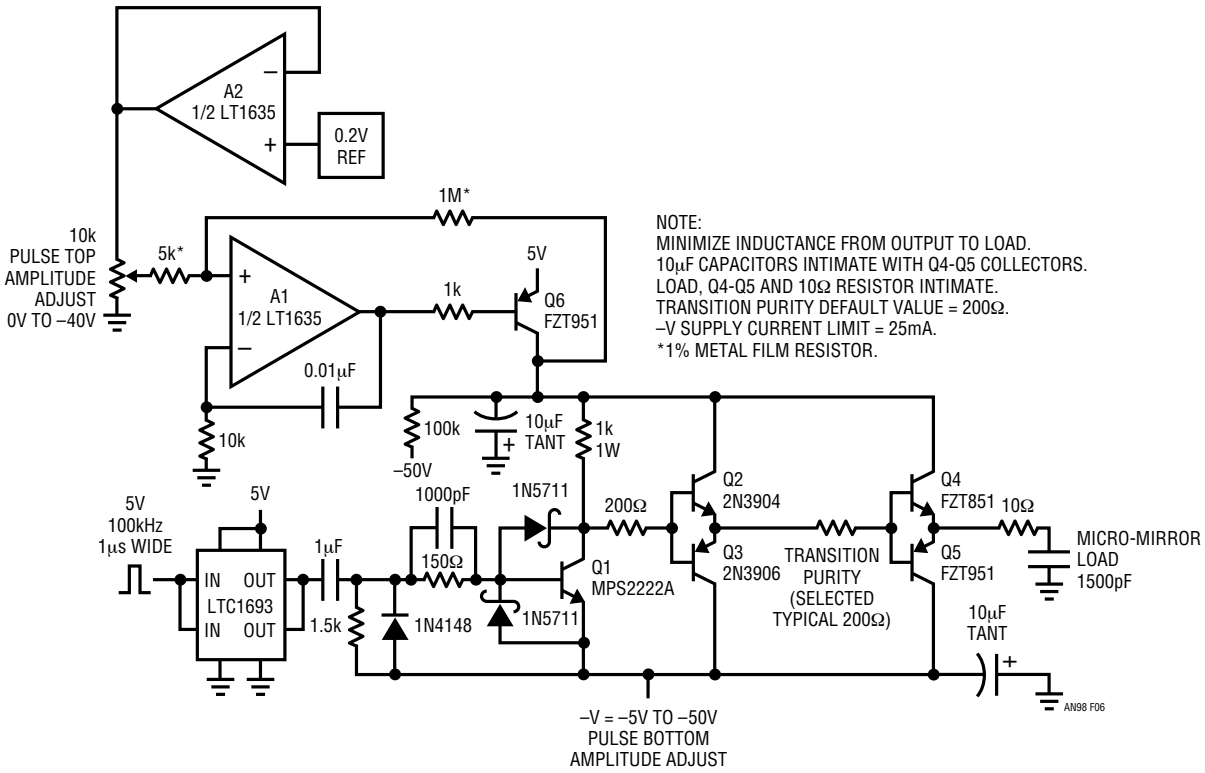


Figure 6. High Voltage, Wideband Level Shift for Micro-Mirror Biasing Precludes Overshoot. 5V Input Pulse Switches Q1 Voltage Gain Stage via LTC1693 Driver. Q2-Q3 Isolate Q1's Collector, Bias Q4-Q5 Output. A1-Q6 Regulate Pulse Top Amplitude; –V Potential Sets Pulse Bottom Voltage. Output Pulse Amplitude, Settable Anywhere Within These Limits, Has No Overshoot

times and overshoot. Its value, nominally 200Ω, will vary somewhat with layout and should be selected for best output waveform purity. Q4 and Q5, high current types, drive the capacitive load.

The 5-transistor stage swings to potentials established by Q1's emitter and collector rails[3]. Emitter rail voltage, hence "pulse bottom" amplitude, is set by the DC potential of its power supply, variable between –5V and –50V. The collector rail is controlled by A1, operating in the Wu configuration[4]. A1, containing an amplifier and a 0.2V reference, drives Q6 to regulate the collector rail anywhere between zero and –40V in accordance with the 10k potentiometer's setting. The settability of both power rails, combined with the transistor stages wide operating region, permits pulse amplitude control over the desired range.

Figure 7 shows the level shift output (trace B) responding to an input pulse (trace A) with amplitude limits adjusted for zero and –50V. The high voltage output transitions, occurring within 100ns, are exceptionally pure.

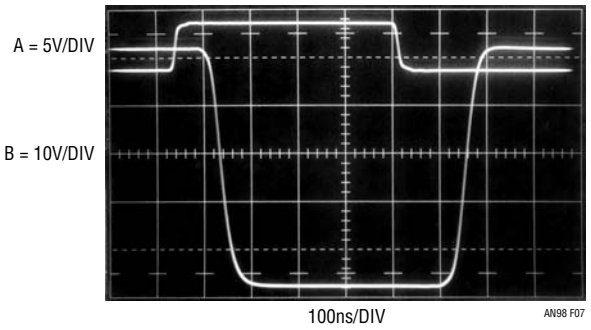


Figure 7. Level Shift Responds (Trace B) to Input Pulse (Trace A) with Amplitude Limits Adjusted for Zero and –50V. Fast, High Voltage Transitions are Exceptionally Pure

Note 3. Transistor data sheet aficionados may notice that the –50V potential exceeds Q1, Q2, Q3 V_{CEO} specifications. The transistors operate under V_{CER} conditions, where breakdown is considerably higher.

Note 4. The collector rail regulation scheme was suggested by Albert Wu of Linear Technology Corporation.

Simple Rise Time and Frequency Reference

A frequent requirement in wideband circuit work is a rise time/frequency reference. The LTC6905 oscillator provides a simple way to realize this. This device, programmable by pin strapping and a single resistor, achieves outputs over a continuous 17MHz to 170MHz range with accuracy inside 1%. Additionally, output stage transitions are typically within 500ps.

Figure 8's circuit is delightfully simple. The LTC6905 is set for 100MHz output by the pin strapping and resistor value shown. The 953Ω resistor isolates the IC's output from the 50Ω oscilloscope input and any parasitic capacitance, promoting the fastest possible transitions. Figure 9 shows circuit output in a 1GHz real-time bandwidth (t_{RISE} = 350ps). The 100MHz square wave displays sub-nanosecond transitions. Determining transition rise and fall times requires a faster oscilloscope[5]. Figures 10 and 11, measured in a 3.9GHz sampled bandpass, record a 400ps rise time (Figure 10) and a 320ps fall time (Figure 11).

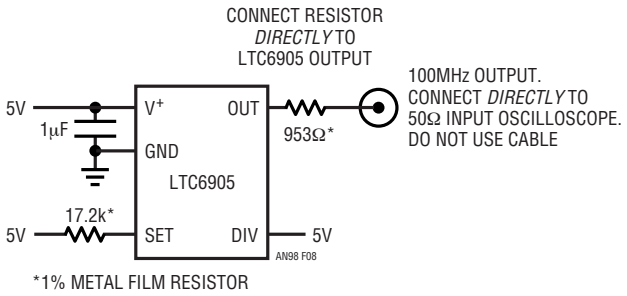


Figure 8. LTC6905 Oscillator Configured for Sub-Nanosecond Transitions and 100MHz Output is Rise Time/Frequency Reference

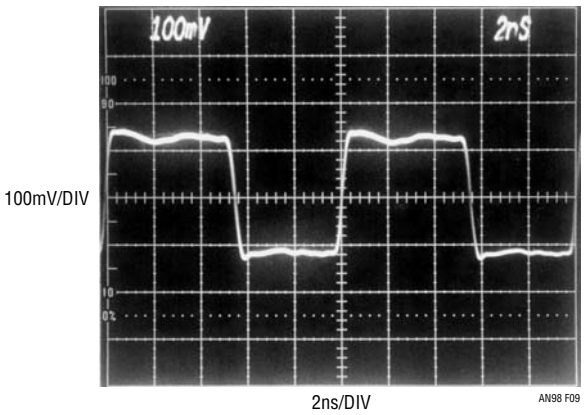


Figure 9. 100MHz Output Viewed in 1GHz Real-Time Bandwidth Displays Sub-Nanosecond Transitions

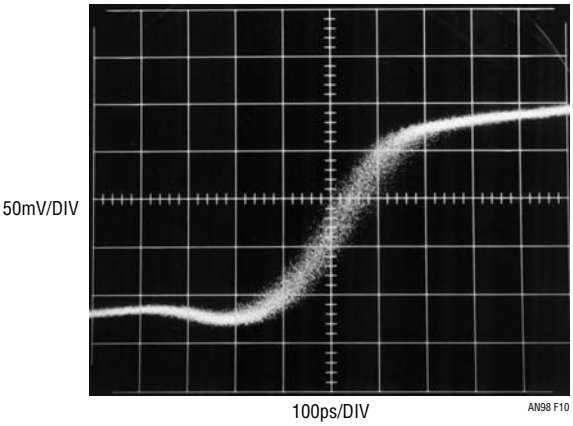


Figure 10. Transition Rise Time Measures 400ps in 3.9GHz (t_{RISE} = 90ps) Sampled Bandpass. Trace Granularity Derives from Sampling Oscilloscope Operation

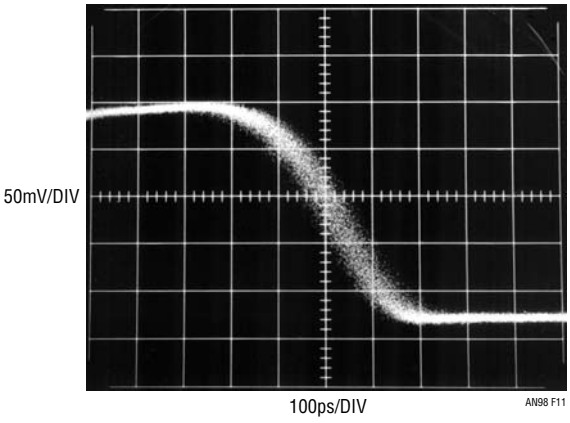


Figure 11. Transition Fall Time Measures 320ps in 3.9GHz (t_{RISE} = 90ps) Sampled Bandpass. Trace Granularity Derives from Sampling Oscilloscope Operation

Note 5. See Appendix A, "How Much Bandwidth is Enough?" and Appendix B, "Connections, Cables, Adapters, Attenuators, Probes and Picoseconds."

850 Picosecond Rise Time Pulse Generator with <1% Pulse Top Aberrations

Impulse response and rise time testing often require a fast rise time source with a high degree of pulse purity. These parameters are difficult to simultaneously achieve, particularly at sub-nanosecond speeds. Figure 12's circuit, derived from oscilloscope calibrators, meets these criteria, delivering an 850ps output with less than 1% pulse top aberrations.

Oscillator 01 delivers a 10MHz square wave to current mode switch Q2-Q3. Note that 01 is powered between ground and –5V to meet transistor biasing requirements. Q1 provides current drive to Q2-Q3. When 01 biases Q2, Q3 goes off. Q3's collector rises rapidly to a potential determined by Q1's collector current, D1, the resistors at the circuits output and the 50Ω termination. When 01 goes low, Q2 turns off, Q3 comes on and the output settles to zero. D2 prevents Q3 from saturating.

The circuit's positive output transition is extremely fast and singularly clean. Figure 13, viewed in a 1GHz real-time bandwidth, shows 850ps rise time with exceptionally pure pre- and post-transition characteristics[6]. Figure 14 details pulse top settling. The photo shows the pulse-top region immediately following the positive 500mV transition.

Note 6. The measured 850ps rise time, influenced by the monitoring 1GHz oscilloscopes 350ps rise time, is almost certainly pessimistic. A root-sum-square correction applied to the measurement indicates a 775ps rise time. See Appendix A for detailed discussion.

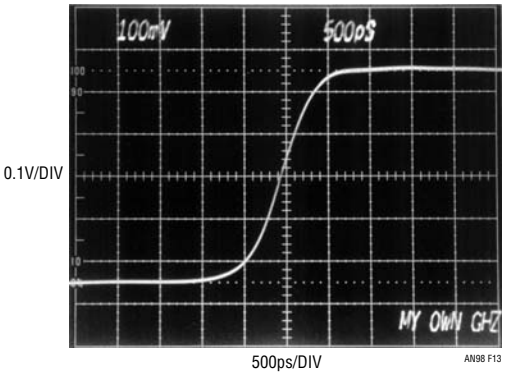


Figure 13. Figure 12's Displayed 850ps Transition Time is Free of Discontinuities when Viewed in a Real-Time 1GHz (t_{RISE} = 350ps) Bandwidth. Root-Sum-Square Correction Applied to Measurement Indicates 775ps Rise Time

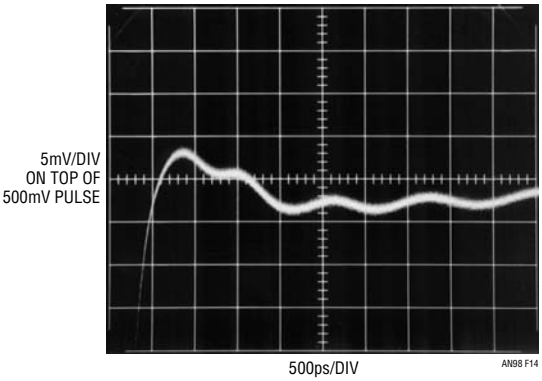


Figure 14. Pulse Top Aberrations Remain Inside 4mV Within 400ps of Transition Completion. 1GHz Ring-Off is Probably Due to Breadboard Limitations. Trace Granularity Derives from Sampling Oscilloscope Operation

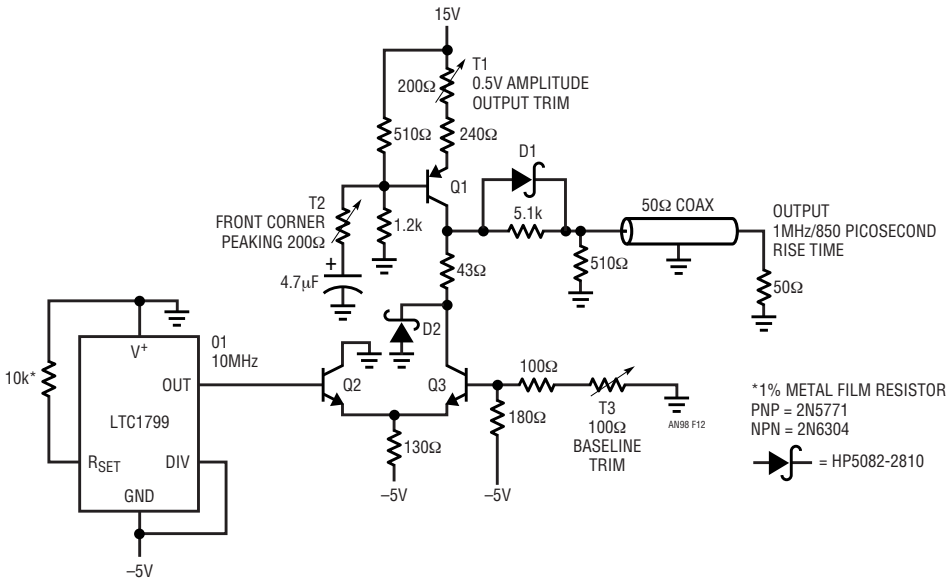


Figure 12. Oscillator 01 Drives Q2-Q3 Current Mode Switch, Producing 850ps Rise Time Output. Trims Facilitate Clean Transition with <1% Pulse Top Aberrations

Settling occurs within 400ps of the edge's completion, with all undesired activity within ±4mV. The 1mV, 1GHz ring-off is probably due to breadboard construction limitations, and could be eliminated with stripline layout techniques.

This level of performance requires trimming. The oscilloscope used should have at least 1GHz of bandwidth. T2 and T3 are adjusted for best pulse presentation while T1 sets 500mV output amplitude across the 50Ω termination. The trims are somewhat interactive, although not unduly so, converging quickly to give the results noted.

20 Picosecond Rise Time Pulse Generator

Figure 15, another fast rise time pulse generator, switches a high grade, commercially produced tunnel diode mount to produce a 20ps rise time pulse. 01's clocking (trace A, Figure 16) causes Q1's collector (trace B) to switch the capacitively loaded Q2-Q3 current source. The resultant repetitive ramp at Q3's collector (trace C), buffered by Q4, biases the tunnel diode mount via the output resistors. The tunnel diode driven output (trace D) follows the ramp until abruptly rising (trace D, just prior to 4th vertical division). This departure is caused by tunnel diode triggering. The edge associated with this triggering is extremely steep, with a specified rise time of 20ps and clean settling. Figure 17 examines this edge within the limitations of a 3.9GHz (t_{RISE} = 90ps) sampling oscilloscope. The trace shows the tunnel diode's switching, driving the oscilloscope to its

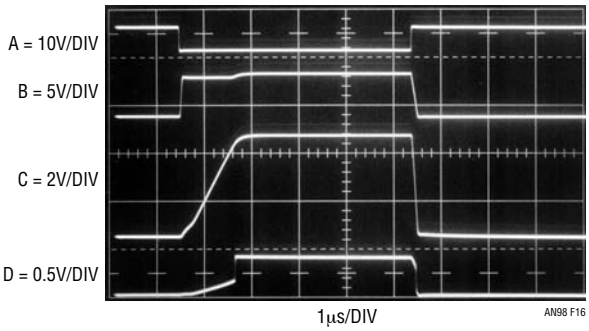


Figure 16. 01 (Trace A) Clocks Q1's Collector (Trace B), Switching Capacitively Loaded Q2-Q3 Current Source. Resultant Repetitive Ramp at Q3's Collector (Trace C), Buffered by Q4, Biases Tunnel Diode via Output Resistors. Tunnel Diode Output (Trace D) Follows Ramp Until Abruptly Triggering

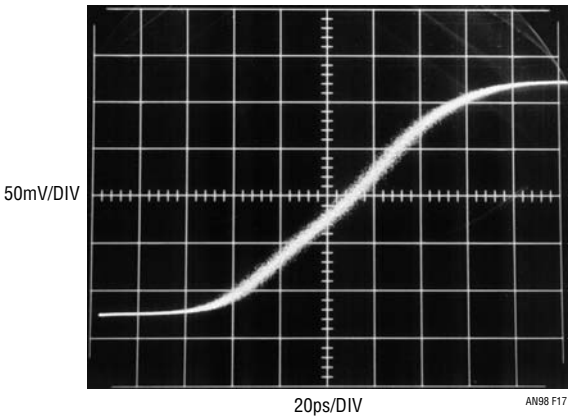


Figure 17. Figure 15's 20ps Edge Drives a 3.9GHz Sampling 'Scope to its 90ps Rise Time Limit. Trace Granularity is Characteristic of Sampling Oscilloscope Display

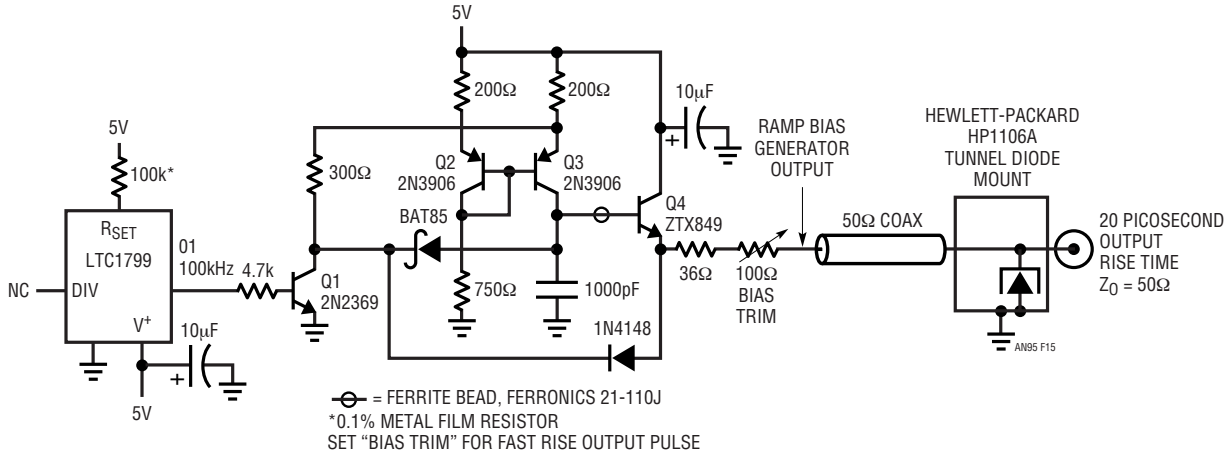


Figure 15. Current Ramps Into Tunnel Diode Until Switching Occurs, Producing a 20ps Edge. Q1, Squarewave Clocked from 01, Switches Q2-Q3 Capacitively Loaded Current Source, Producing Repetitive Ramps at Q4. Ascending Current Through Output Resistors Triggers Tunnel Diode

90ps rise time limit[7]. Figure 18, slowing sweep speed to 100ps/divison, shows pulse top settling (in a 3.9GHz bandwidth) within 4% inside 100ps[8].

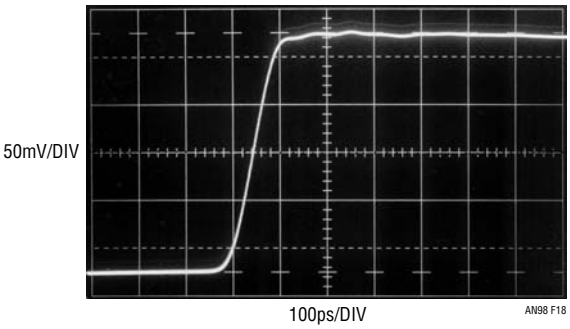


Figure 18. Reducing Sweep Speed Shows 4% Pulse Top Flatness Within Oscilloscope's 3.9GHz (t_{RISE} = 90ps) Bandwidth

Nanosecond Pulse Width Generator

The previous three circuits were optimized for fast rise time. It is sometimes desirable to produce extremely short width pulses in response to an input trigger. Such a predictable, programmable short time interval generator has broad use in fast pulse circuitry, particularly in sampling applications[9]. Figure 19, built around a quad high speed comparator and a fast gate, has a settable 0ns to 10ns output width with 520ps, 5V transitions. Pulse width varies less than 100ps with 5V supply variations of ±5%. Minimum input trigger width is 30ns and input-output delay is 18ns[10].

The input pulse (Figure 20, trace A) is inverted by C1, which also isolates the 50Ω termination. C1's output drives

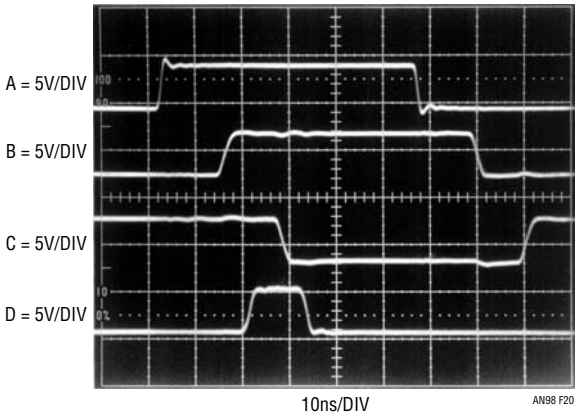


Figure 20. Pulse Generator Waveforms, Viewed in 400MHz Real-Time Bandwidth, Include Input (Trace A), C3 (Trace B) Fixed and C2 (Trace C) Variable Outputs. Circuit Output Pulse is Trace D. RC Network's Differential Delay Manifests as C2-C3 Positive Overlap. G1 Extracts This Interval, Presents Output

fixed and variable RC networks. The networks charge time difference, and hence delay, is primarily determined by programming resistor R, at a scale factor ≈80Ω/ns. C2 and C3, arranged as complementary output level detec-

Note 7. Sorry, but 3.9GHz is the fastest 'scope in my house. See Appendix A for relevant comment.

Note 8. The HP1106 is no longer produced, although available on the secondary market. The TD1107, currently manufactured by Picosecond Pulse Labs, is an equivalent unit, although we have no experience with it.

Note 9. Pedestrian laboratory argot for interval generator is "one-shot."

Note 10. This circuit is a considerably improved extension of earlier work. See References 4 and 5.

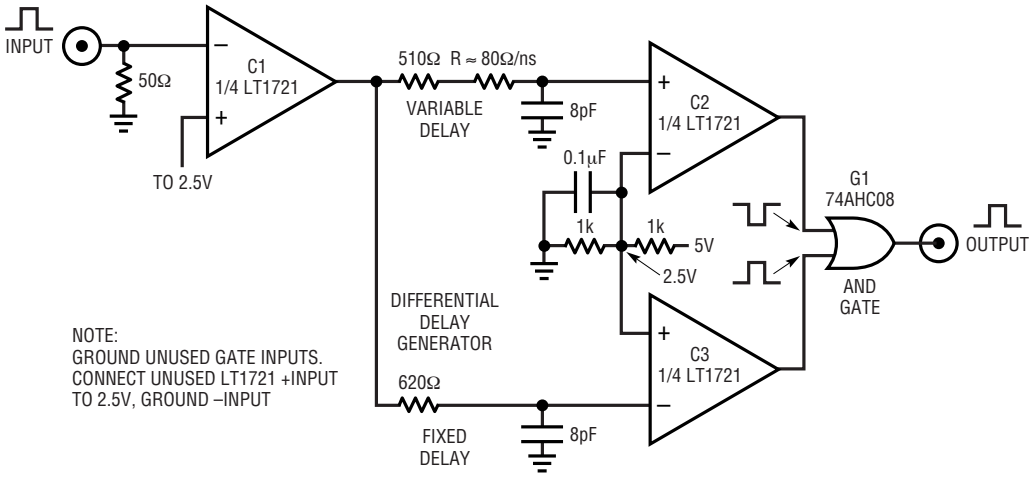


Figure 19. Pulse Generator Has 0ns to 10ns Width, 520ps Transitions. C1 Unloads Termination, Drives Differential Delay Network. C2-C3 Complementary Outputs Represent Delay Difference as Edge Timing Skew. G1, High During C2-C3 Positive Overlap, Presents Circuit Output

tors, represent the network's delay difference as edge time skew. Trace B is C3's ("fixed") output and trace C is C2's ("variable") output. Gate G1's output (trace D), high during C2-C3 positive overlap, presents the circuit's output pulse. Figure 21 shows a 5V, 5ns width (measured at 50% amplitude) output pulse with R = 390Ω. The pulse is clean, with well defined transitions. Post-transition aberrations, within 8%, derive from G1's bond wire inductance and an imperfect coaxial probing path. Figure 22 shows the narrowest full amplitude (5V) pulse obtainable. Width measures 1ns at the 50% amplitude point and 1.7ns at the base in a 3.9GHz bandwidth. Shorter widths are obtainable if partial amplitude pulses are acceptable. Figure 23 shows a 3.3V, 700ps width (50%) with a 1.25ns base. G1's rise time limits minimum achievable pulse width. Figure 24, taken in a 3.9GHz sampled bandpass, measures 520ps rise time. Fall time is similar.

Single Rail Powered Amplifier with True Zero Volt Output Swing

Many single supply powered applications require amplifier output swings within millivolt or even sub-millivolt levels of ground. Amplifier output saturation limitations normally preclude such operation. Figure 25's power supply bootstrapping scheme achieves the desired characteristics with minimal component addition[11].

A1, a chopper stabilized amplifier, has a clock output. This output switches Q1, providing drive to the diode-capacitor charge pump. The charge pump output feeds A1's V^- terminal, pulling it below zero, permitting output swing to (and below) ground. If desired, the negative output excursion can be limited by either clamp option shown.

Note 11. See Reference 8, Appendix D.

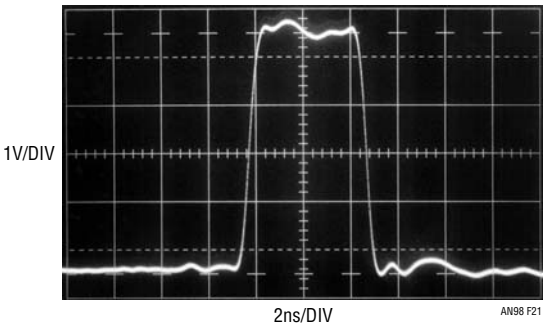


Figure 21. 5ns Wide Output with R = 390Ω is Clean, with Well Defined Transitions. Post-Transition Aberrations, Within 8%, Derive from G1 Bond Wire Inductance and Imperfect Coaxial Probe

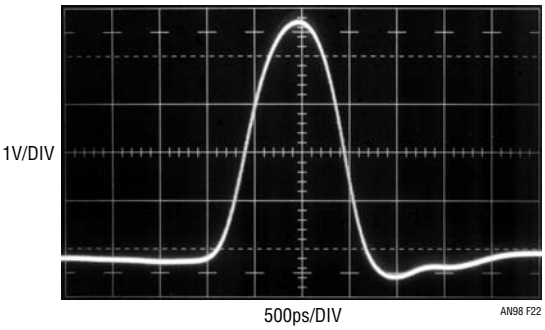


Figure 22. Narrowest Full Amplitude Pulse Width is 1ns; Base Width Measures 1.7ns. Measurement Bandwidth is 3.9GHz

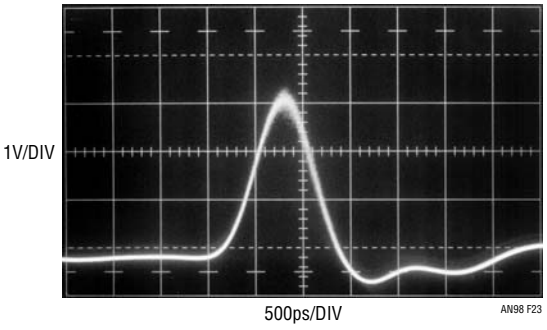


Figure 23. Partial Amplitude Pulse, 3.3V High, Measures 700ps Width with 1.25ns Base. Trace Granularity is Artifact of 3.9GHz Sampling Oscilloscope Operation

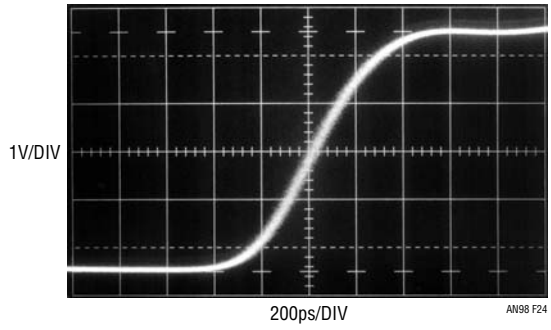


Figure 24. Transition Detail in 3.9GHz Bandpass (t_{RISE} = 90ps) Shows 520ps Rise Time. Fall Time is Similar. Trace Granularity Derives from Sampling Oscilloscope Operation

Reliable start-up of this bootstrapped power supply scheme is a valid concern, warranting investigation. In Figure 26, the amplifier's V^- pin (trace C) initially rises at supply turn-on (trace A) but heads negative when amplifier clocking (trace B) commences at about midscreen.

The circuit provides a simple way to obtain output swing to zero volts, permitting a true "live at zero" output.

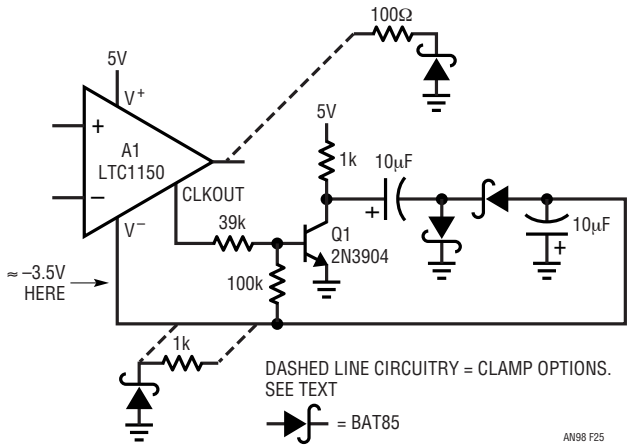


Figure 25. Single Rail Powered Amplifier Has True Zero Volt Output Swing. A1's Clock Output Switches Q1, Driving Diode-Capacitor Charge Pump. A1's V^- Pin Assumes Negative Voltage, Permitting Zero (and Below) Volt Output Swing

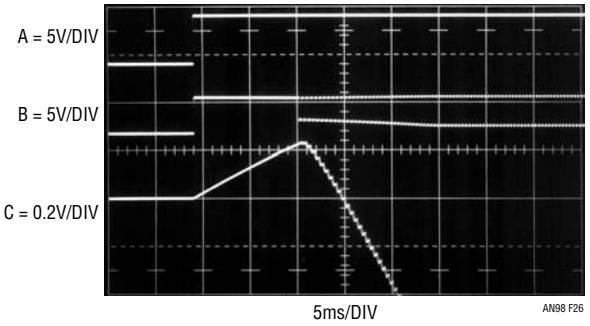


Figure 26. Amplifier Bootstrapped Supply Start-Up. Amplifier V^- Pin (Trace C) Initially Rises Positive at 5V Supply (Trace A) Turn-On. When Amplifier Internal Clock Starts (Trace B, 5th Vertical Division), Charge Pump Activates, Pulling V^- Pin Negative

Milliohmmeter

Resistance measurement of contacts, PC traces and vias requires a low resistance ohmmeter. Figure 27's 9V battery-powered design has a 1Ω full-scale range, with resolution down to 1mΩ. It produces a 0V to 1V output for a 0Ω to 1Ω resistance at its 4-terminal Kelvin sensed input with 0.1% accuracy over a 5.25V to 9.5V power supply range. An AC carrier modulation scheme is employed to reject noise and error inducing DC offsets due to parasitic thermocouples (Seebeck effect)[12].

A1 and associated components form a 10mA current source that is alternately steered between Rx, the unknown resistance, and ground by LTC6943 switch pins 10, 11 and 12. The LTC6943's control pin (Pin 14) is clocked at ≈45Hz from the CD4024 divider output. This action causes a carrier modulated 10mA current flow through Rx. Rx's value determines the resultant AC voltage across it. This AC signal is capacitively coupled to LTC6943 switch pins 1, 4 and 5, driven synchronously with the current source modulation. These pins switching forms a synchronous rectifier, demodulating the AC signal back to DC across A2's input capacitor. A2 amplifies this DC potential at a gain of 1mV per milliohm, or 1V full scale. Note that single-rail powered A2's output can swing to true "zero" because it utilizes a variant of the supply boostrapping scheme presented back in Figure 25. A2's clock output drives Q2, which pulses the CD4024 divider. One divider output switches the LTC6943 modulator-demodulator while another output drives the bootstrapped charge pump to supply A2's V^- pin with about –7V.

Diode clamps prevent accidental overvoltage at the probe inputs without introducing loading error to the 10mV maximum Rx carrier waveform. Circuit calibration involves placing a 1Ω, 0.1% resistor at Rx and adjusting the 200Ω trimmer for $1.000V_{OUT}$. The synchronously demodulated AC carrier technique displays the inherent narrow band noise rejection characteristics of "lock-in" type measurements. Figure 28 shows a normal waveform across Rx for Rx = 1Ω. The 10mV signal is clean, and circuit output reads 1.000V. In Figure 29 noise is deliberately injected into the Rx probes, burying the carrier in a 6× noise-to-signal ratio. Despite this, circuit output remains at 1.000V.

Note 12. This circuit's operation is derived from the Hewlett-Packard HP-4328A. See Reference 7.

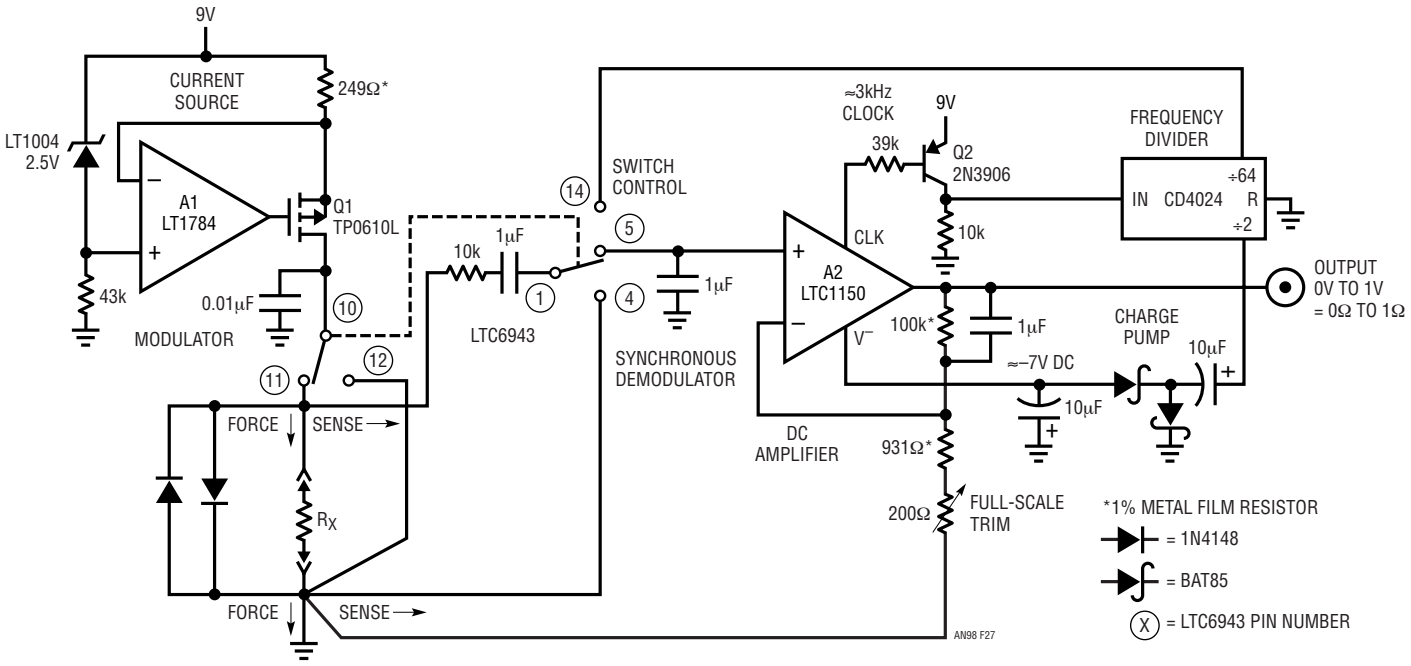


Figure 27. 1Ω Full-Scale Ohmmeter Accurately Resolves 0.001Ω for PC Board Trace/Via Resistance Measurement. Carrier Modulation of Unknown Resistance Permits Narrowband Synchronous Demodulation, Rejecting Noise and Parasitic DC Offsets. Kelvin Sensing at Rx Prevents Test Lead Induced Errors

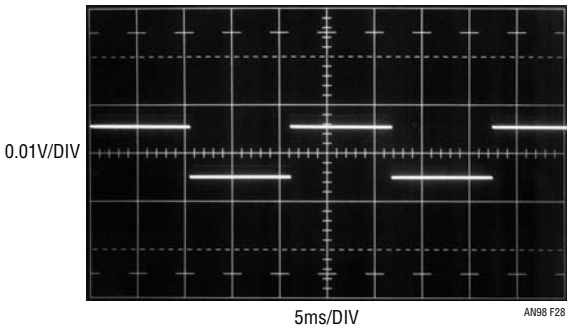


Figure 28. Normal Waveform at Rx with Rx = 1.000Ω. Circuit Output Correctly Reads 1.000V

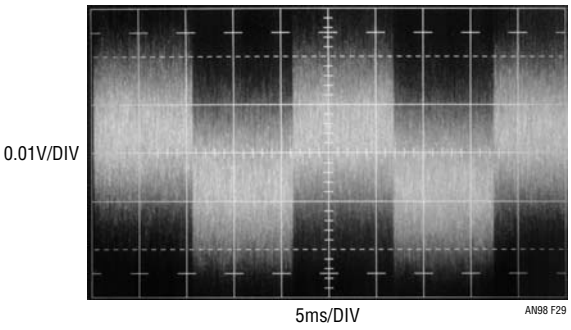


Figure 29. Rx Waveform with Rx = 1.000Ω and Noise Added. Circuit Output Remains 1.000V Despite 6× Noise-to-Signal Ratio

0.02% Accurate Instrumentation Amplifier with 125V_{CM} and 120dB CMRR

Figure 30's circuit may be used when high accuracy differential input measurement is required[13]. It is particularly suited to transducer signal conditioning where high common mode voltage may occur. The circuit has the low offset and drift of chopper stabilized A1, but also incorporates a novel optically coupled, switched capacitor input stage to achieve specifications unavailable in conventional designs. DC common mode rejection exceeds 120dB over a ±125V input range and gain accuracy and stability are set by A1. Error from all sources is inside 0.02%. The design's high common mode voltage capability allows it to reliably extract small signals while withstanding transient and fault conditions often encountered in industrial environments.

This scheme measures input difference voltage by switching (S1A, S1B) a capacitor across the input ("ACQUIRE"). After a time the capacitor charges to the voltage across the

Note 13. Sharp-eyed devotees of LTC publications will recognize this as a mildly modified variant of Reference 8 (pp. 10-11) and Reference 13 (pp. 1-2).

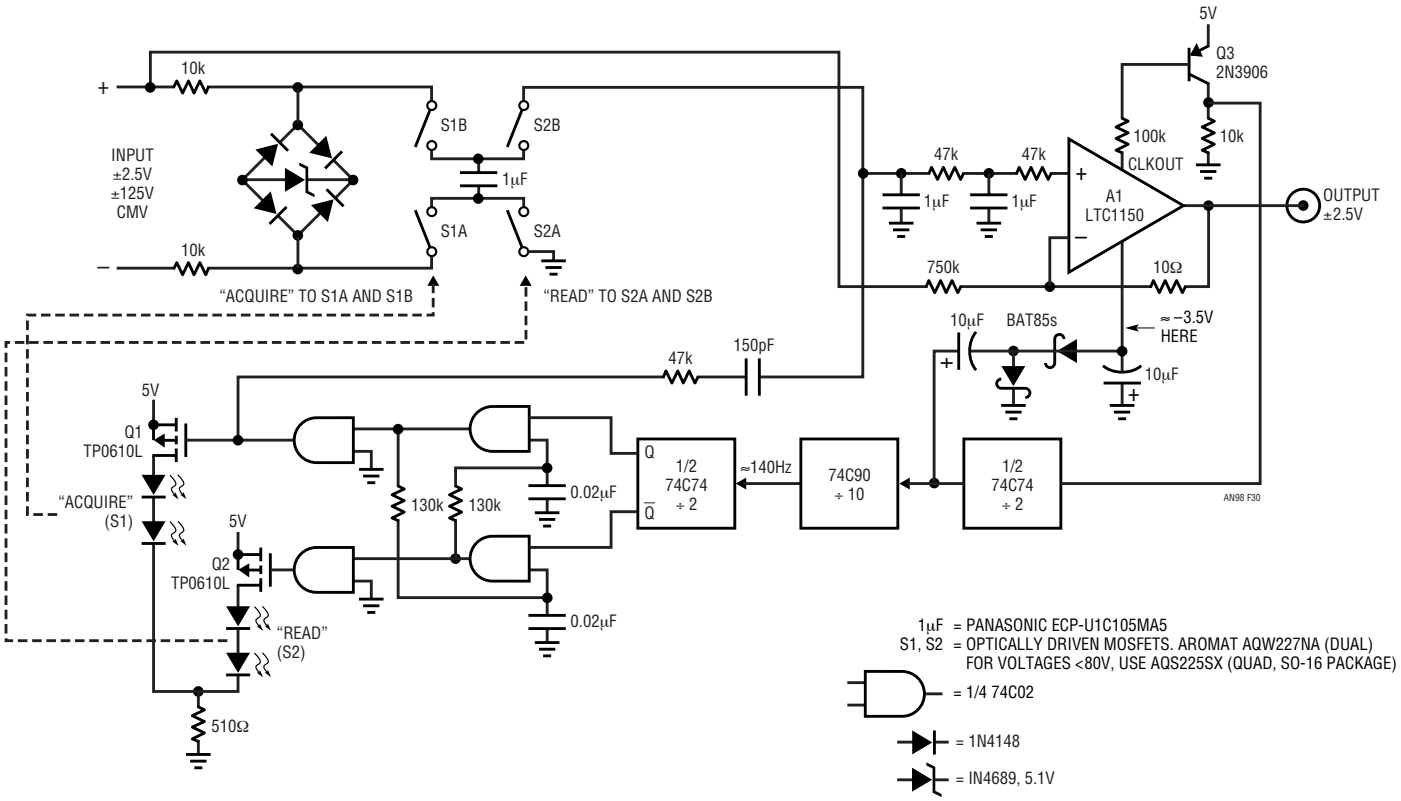


Figure 30. 0.02% Accurate, 125V Common Mode Range Instrumentation Amplifier Utilizes Optically Driven FETs and Flying Capacitor. Logic Driven Q1-Q2 Provides Nonoverlapping Clocking to S1-S2 LEDs. Clock Derives from A1's Internal Oscillator

input. S1A and S1B open and S2A and S2B close ("READ"). This grounds one capacitor plate and the capacitor discharges into the grounded 1µF unit at S2B. This switching cycle is continuously repeated, resulting in A1's ground referred positive input assuming the input difference voltage. The common mode voltage is rejected by the optical switching of the ungrounded 1µF capacitor. The LED driven MOSFET switches specified do not have junction potentials and the optical drive contributes no charge injection error. A nonoverlapping clock prevents simultaneous conduction in S1 and S2, which would result in charge loss, causing errors and possible circuit damage. The 5.1V zener prevents switched capacitor failure if the inputs are subjected to differential overvoltage.

A1, a chopper stabilized amplifier, has a clock output. This clock, level shifted and buffered by Q3, drives a logic divider chain. The first flip-flop activates a charge pump, pulling A1's V^- pin negative, permitting amplifier swing to (and below) zero volts[14]. The divider chain terminates into a logic network. This network provides phase opposed

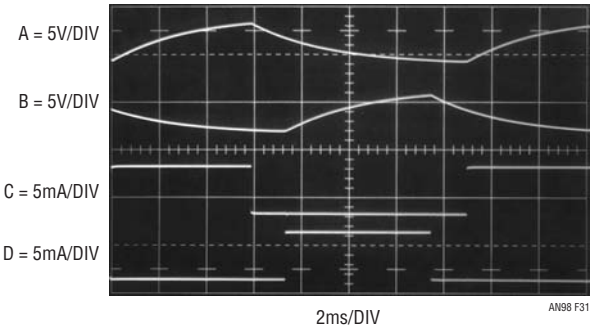


Figure 31. Clocked, Cross Coupled Capacitors (Traces A and B) in 74C02 Based Network Result in Nonoverlapping Drive (Traces C and D) to S1-S2 Actuation LEDs

charging of the 0.02µF capacitors (Traces A and B, Figure 31). The gating associated with these capacitors is arranged so the logic provides nonoverlapping, complementary biasing to Q1 and Q2. These transistors supply this nonoverlapping drive to the S1 and S2 actuating LEDs (Traces C and D).

Note 14. This arrangement will be recognized from Figures 25 and 27. See also Reference 8, Appendix D.

The extremely small parasitic error terms in the LED driven MOSFET switches results in nearly theoretical circuit performance. However, residual error (≈0.1%) is caused by S1A's high voltage switching pumping S2B's 3pF to 4pF junction capacitance. This results in a slight quantity of unwanted charge being transferred to the 1μF capacitor at S2B. The amount of charge transferred varies with the input common mode voltage and, to a lesser extent, the varactor-like response of S2B's off-state capacitance. These terms are partially cancelled by DC feedforward to A1's negative input and AC feedforward from Q1's gate to S2B. The corrections compensate error by a factor of five, resulting in 0.02% accuracy.

Optical switch failure could expose A1 to high voltage, destroying it and possibly presenting destructive voltages to the 5V rail. This most unwelcome state of affairs is prevented by the 47k resistors in A1's positive input.

Wideband, Low Feedthrough, Low Level Switch

Rapid switching of wideband, low level signals is complicated by switch control artifacts corrupting the signal channel. FET-based designs suffer large charge injection-based errors, often orders of magnitude larger than the signal of interest. The classic diode bridge switch has much lower error, but requires substantial support circuitry and careful trimming[15]. Figure 32's circuit takes a different approach to synthesize a switch with minimal control channel feedthrough. This design switches signals over a ±30mV range with peak control channel feedthrough of millivolts and settling times inside 40ns. This capability, developed for amplifier and data converter settling time measurement, has broad implication in instrumentation and sampling circuitry.

The circuit approximates switch action by varying the transconductance of an amplifier, the maximum gain of which is unity. At low transconductance, amplifier gain is nearly zero, and essentially no signal is passed. At maximum transconductance, signal passes at unity gain. The amplifier and its transconductance control channel are very wideband, permitting them to faithfully track rapid variations in transconductance setting. This characteristic means the amplifier is never out of control, affording clean response and rapid settling to the "switched" input's value.

A1A, one section of an LT®1228, is the wideband transconductance amplifier. Its voltage gain is determined by its output resistor load and the current magnitude into its "I_{SET}" terminal. A1B, the second LT1228 section, unloads A1A's output. As shown it provides a gain of two, but when driving a back-terminated 50Ω cable, its effective gain is unity at the cable's receiving end. Current source Q1, controlled by the "switch control input," sets A1A's transconductance, and hence gain. With Q1 gated off (control input at zero), the 10MΩ resistor supplies about 1.5μA into A1A's I_{SET} pin, resulting in a voltage gain of nearly zero, blocking the input signal. When the switch control input goes high, Q1 turns

Note 15. See References 20 and 21 for practical examples of diode bridge switches.

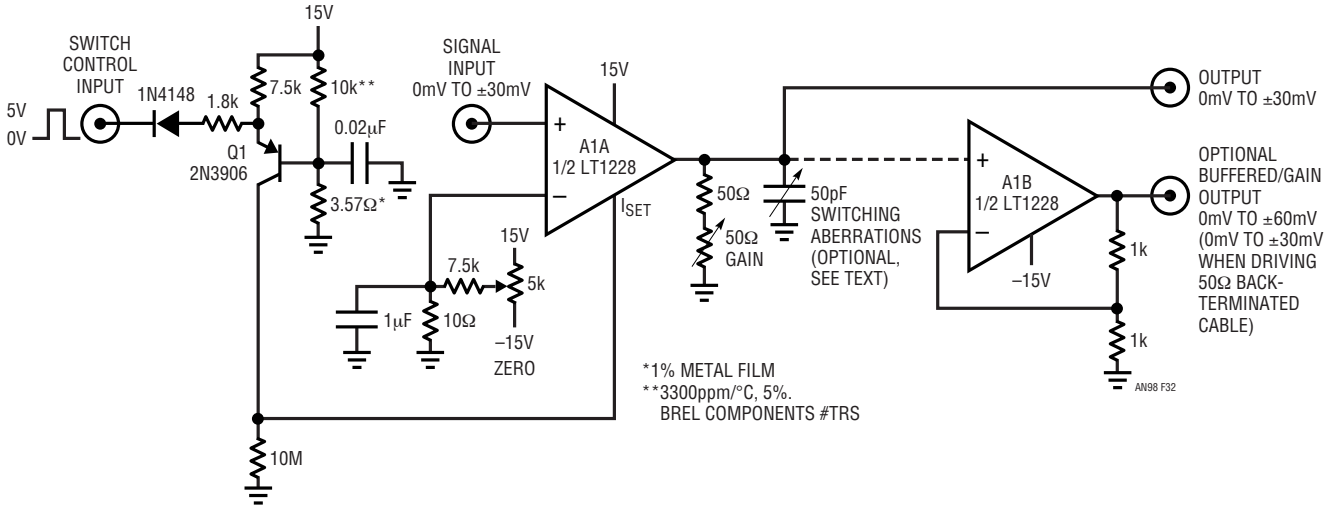


Figure 32. Transconductance Amplifier Based 100MHz Low Level Switch has Minimal Control Channel Feedthrough. A1A's Unity-Gain Output is Cleanly Switched by Logic Controlled Q1's Transconductance Bias. Optional A1B Provides Buffering and Signal Path Gain

on, sourcing ≈1.5mA into the I_{SET} pin. This 1000:1 set current change forces maximum transconductance, causing the amplifier to assume unity gain and pass the input signal. Trims for zero and gain ensure accurate input signal replication at the circuit's output. The optional 50pF variable capacitor can be used to damp residual settling transients. The specified 10k resistor at Q1 has a 3300ppm/°C temperature coefficient, compensating A1A's complementary transconductance tempco to minimize gain drift.

Figure 33 shows circuit response for a switched 10mV DC input and $C_{ABERRATION}$ = 35pF. When the control input (trace A) is low, no output (trace B) occurs. When the control input goes high, the output reproduces the input with "switch" feedthrough settling in about 20ns. Note that turn-off feedthrough is undetectable, due to the 1000× transconductance reduction and attendant 25× bandwidth drop. Figure 34 speeds the sweep up to 10ns/division to examine settling detail. The output (trace B) settles inside 1mV 40ns after the switch control (trace A) goes high. Peak feedthrough excursion, damped by $C_{ABERRATION}$, is only 5mV. Figure 35 was taken under identical conditions, except that $C_{ABERRATION}$ = 0pF. Feedthrough increases to ≈20mV, although settling time to 1mV remains at 40ns. Figure 36, using double exposure technique, compares signal channel rise times for

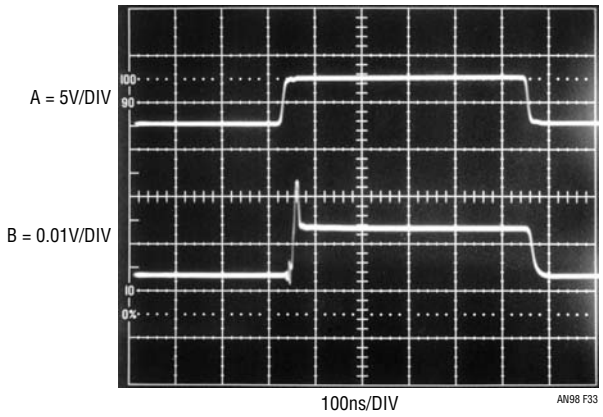


Figure 33. Control Input (Trace A) Dictates Switch Output's (Trace B) Representation of 0.01V DC Input. Control Channel Feedthrough, Evident at Switch Turn-On, Settles in 20ns. Turn-Off Feedthrough is Undetectable Due to Decreased Signal Channel Transconductance and Bandwidth. $C_{ABERRATION}$ ≈ 35pF for This Test

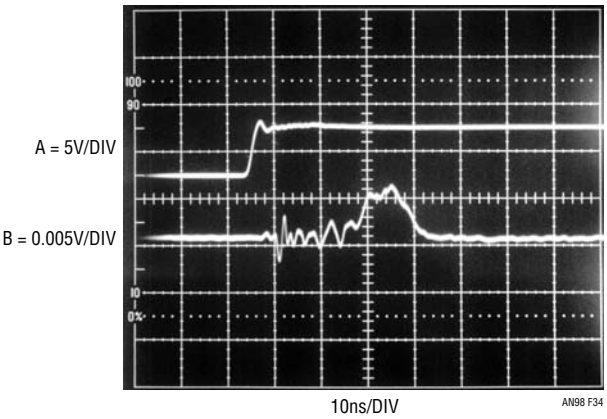


Figure 34. High Speed Delay and Feedthrough for 0V Signal Input. Output (Trace B) Peaks Only 0.005V Before Settling Inside 0.001V 40ns After Switch Control Command (Trace A). $C_{ABERRATION}$ ≈ 35pF for This Test

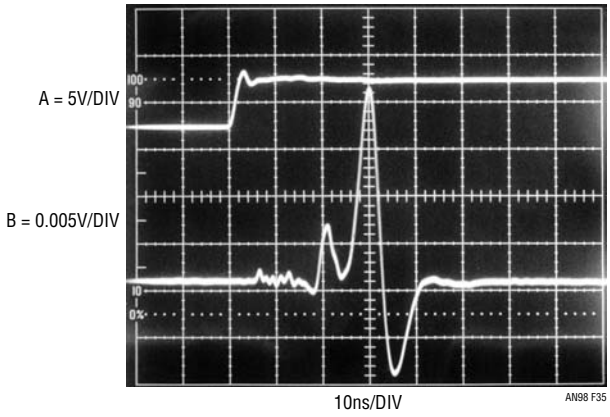


Figure 35. Identical Conditions as Figure 34 Except $C_{ABERRATION}$ = 0pF. Feedthrough Related Peaking Increases to ≈0.02V; 0.001V Settling Time Remains at 40ns

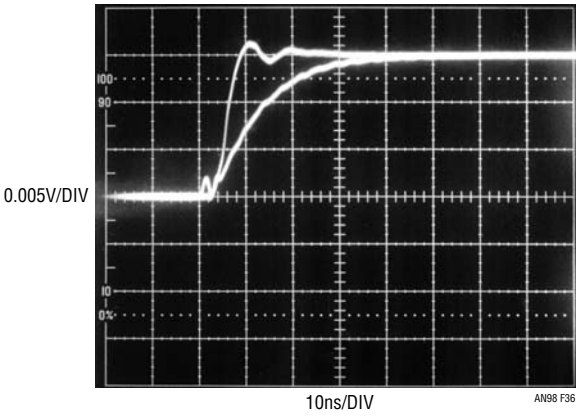


Figure 36. Signal Channel Rise Time for $C_{ABERRATION}$ = 0pF (Leftmost Trace) and ≈35pF (Rightmost Trace) Record 3.5ns and 25ns, Respectively. Switch Control Input High for this Measurement. Photograph Utilizes Double Exposure Technique

$C_{ABERRATION}$ = 0pF (leftmost trace) and ≈35pF (rightmost trace) with the control channel tied high. The larger $C_{ABERRATION}$ value, while minimizing feedthrough amplitude (see Figure 34), increases rise time by 7× versus $C_{ABERRATION}$ = 0pF.

To calibrate this circuit, ground the signal input and tie the control input to 5V. Set the "zero" trim for a zero volt output within 500μV. Next, put 30mV into the signal input and adjust the gain trim for exactly 60mV at A1B's unterminated output. Finally, if $C_{ABERRATION}$ is used, adjust it for minimum feedthrough amplitude with the signal input grounded and the control input fed with a 1MHz square wave.

5V Powered, 0.0015% Linearity, Quartz-Stabilized V→F Converter

Almost all precision voltage-to-frequency converters (V→F) utilize charge pump based feedback for stability. These schemes rely on a capacitor for stability. A great deal of effort towards this approach has resulted in high performance V→F converters (see Reference 31). Obtaining temperature coefficients below 100ppm/°C requires careful attention to compensating the capacitor's drift with temperature. Although this can be done, it complicates the design. Similarly, capacitor dielectric absorption causes errors, limiting linearity to typically 0.01%.

Figure 37's 5V powered design, derived from Reference 31's ±15V fed circuit, reduces gain TC to 8ppm/°C and achieves 15ppm linearity by replacing the capacitor with a quartz-stabilized clock.

In charge pump feedback-based circuits, the feedback is based on Q = CV. In a quartz-stabilized circuit, the feedback is based on Q = IT, where I is a stable current source and T is an interval of time derived from a clock. No capacitor is involved.

Figure 38 details Figure 37's waveforms of operation. A positive input voltage causes A1 to integrate in the negative direction (trace A, Figure 38). The flip-flop's Q1 output (trace B) changes state at the first positive-going clock edge (trace C) after A1's output has crossed the D input's switching threshold. C1 provides the quartz-stabilized clock. The flip-flop's Q1 output controls the gating of

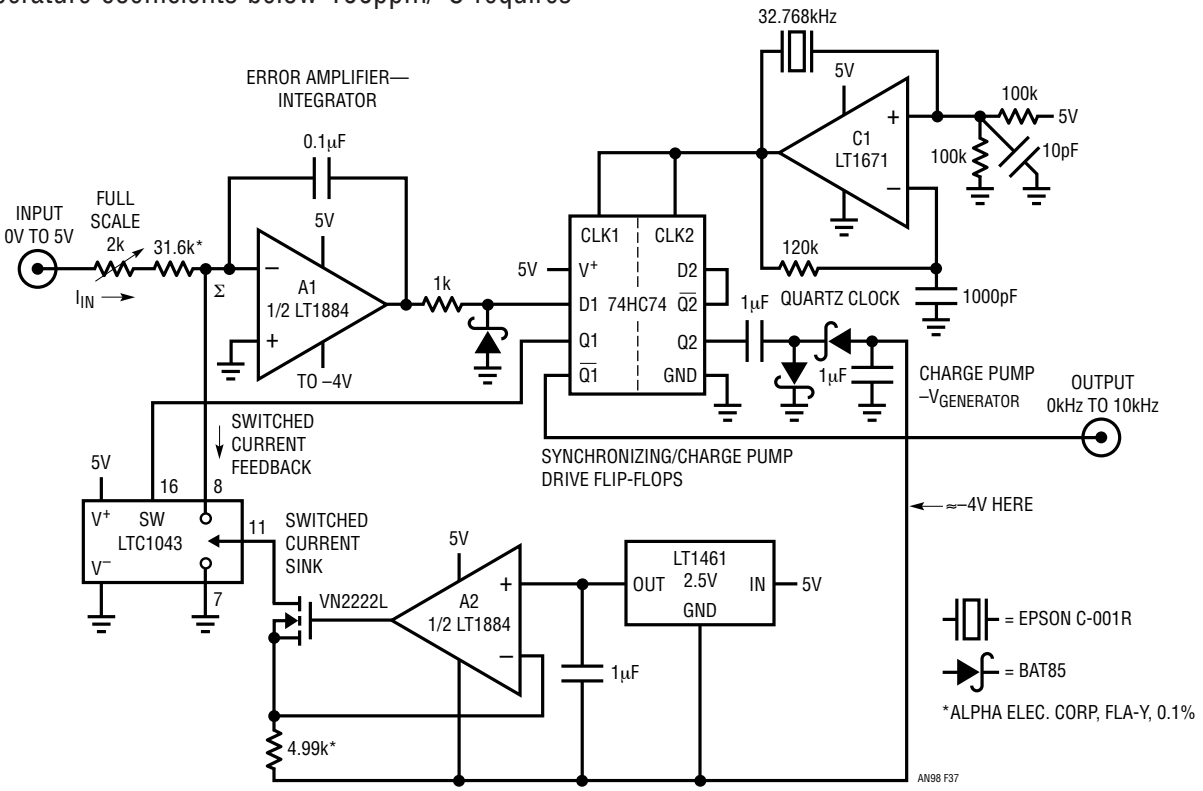


Figure 37. 5V Powered, Quartz-Stabilized 10kHz V→F Converter has 0.0015% Linearity and 8ppm/°C Temperature Coefficient. A1 Servo Controls A2 FET Switched Current Sink Via Clock Synchronized Flip-Flop to Maintain Zero Volt Summing Junction (Σ). Loop Repetition Frequency Directly Conforms to Input Voltage

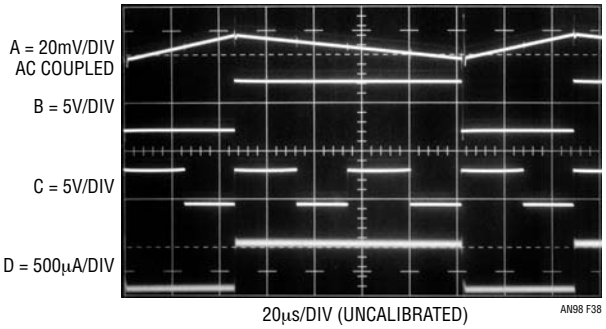


Figure 38. Quartz-Stabilized V→F Converter Waveforms Include A1 Output (Trace A), Flip-Flop Q1 Output (Trace B), Clock (Trace C) and Switched Current Feedback (Trace D). Current Removal (Trace D) from Summing Junction Commenses When Clock Goes High with Q1 Low

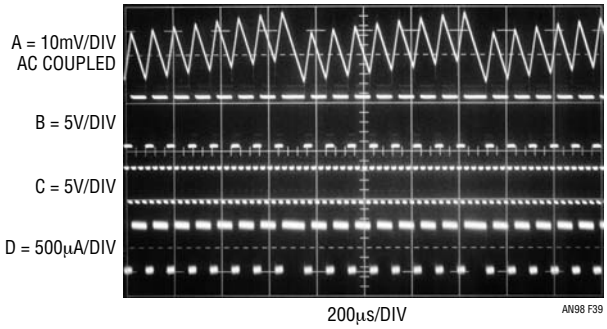


Figure 39. Same Trace Assignments as Figure 38. Reduced Oscilloscope Sweep Speed Shows Effect of Timing Uncertainty Between Loop and Clock. Loop Pulse Position is Occasionally Irregular, But Frequency is Constant Over Practical Measurement Intervals

a precision current sink composed of A2, the LT1461 voltage reference, a FET and the LTC1043 switch. A negative bias supply, derived from the flip-flop's Q2 output driving a charge pump, furnishes the sink current. When A1 is integrating negatively, Q1's output is high and the LTC1043 directs the current sink's output to ground via Pins 11 and 7. When A1's output crosses the D input's switching threshold, Q1 goes low at the first positive clock edge. LTC1043 Pins 11 and 8 close and a precise, quickly rising current flows out of A1's summing point (trace D).

This current, scaled to be greater than the maximum signal-derived input current, causes A1's output to reverse direction. At the first positive clock pulse after A1's output crosses the D input's trip point, switching again occurs and the entire process repeats. The repetition frequency depends on the input-derived current, hence the frequency of oscillation is directly related to the input voltage. The circuit's output is taken from the flip-flop's $\overline{Q1}$ output. Because this circuit replaces a capacitor with a quartz-locked clock, temperature drift is low, typically inside 8ppm/°C. The quartz crystal contributes about 0.5ppm/°C, with most drift contributed by the current source components, the input resistor and switching time variations.

Short term frequency jitter occurs because of the uncertain timing relationship between loop frequency and clock phase. This is normally not a problem because the circuit's output is usually read over many cycles, e.g., 0.1 to 1 second. Figure 39 shows the effects of the timing uncertainty. Reduced sweep speed allows viewing of phase uncertainty induced modulation of A1's output ramp (trace A). Note pulse position (traces B and D) irregularity during A1's major excursions. This behavior causes short term pulse displacement, but output frequency is constant over practical measurement intervals.

Circuit linearity is inside 0.0015% (0.15Hz), gain temperature coefficient is 8ppm/°C (0.08Hz/°C) and power supply rejection better than 100ppm (1Hz) over a 4V to 6V range. The LT1884's low input bias and drift reduce zero point originated errors to insignificant levels. To trim this circuit, apply 5.0000V in and adjust the 2kΩ potentiometer for 10.000kHz output.

Basic Flashlamp Illumination Circuit for Cellular Telephones/Cameras

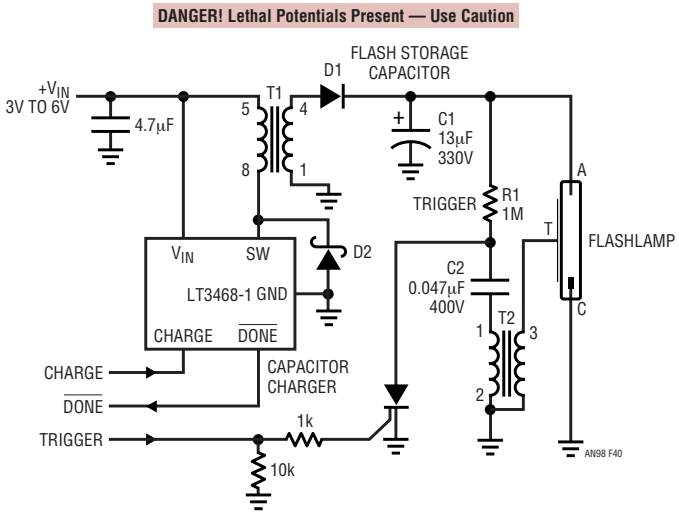
BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Next generation cellular telephones will include high quality photographic capability. Flashlamp-based lighting is crucial for good photographic performance. A previous full-length Linear Technology publication detailed flash illumination issues and presented flash circuitry equipped

with "red-eye" reduction capability.[16,17] Some applications do not require this feature; deleting it results in an extremely simple and compact flashlamp solution.

Figure 40's circuit consists of a power converter, flashlamp, storage capacitor and an SCR-based trigger. In operation the LT3468-1 charges C1 to a regulated 300V at about 80% efficiency. A "trigger" input turns the SCR on, depositing C2's charge into T2, producing a high voltage trigger event at the flashlamp. This causes the lamp to conduct high current from C1, resulting in an intense flash of light. LT3468-1 associated waveforms, appearing in Figure 41, include trace A, the "charge input," going high. This initiates T1 switching, causing C1 to ramp up (trace B). When C1 arrives at the regulation point, switching ceases and the resistively pulled-up "DONE" line drops low (trace C), indicating C1's charged state. The "TRIGGER" command (trace D), resulting in C1's discharge via the lamp, may occur any time (in this case ≈600ms) after "DONE" goes low. Normally, regulation feedback would be provided by resistively dividing down the output voltage. This approach is not acceptable because it would require excessive switch cycling to offset the feedback resistor's constant power drain. While this action would maintain regulation, it would also drain excessive power from the primary source, presumably a battery. Regulation is instead obtained by monitoring T1's flyback pulse characteristic, which reflects T1's secondary amplitude. The output voltage is set by T1's turns ratio. This feature permits tight capacitor voltage regulation, necessary to ensure consistent flash intensity without exceeding lamp energy or capacitor voltage ratings. Also, flashlamp energy is conveniently determined by the capacitor value without any other circuit dependencies.

Figure 42 shows high speed detail of the high voltage trigger pulse (trace A), the flashlamp current (trace B) and the light output (trace C). Some amount of time is required for the lamp to ionize and begin conduction after triggering. Here, 3μs after the 4kV$_{P-P}$ trigger pulse, flashlamp



C1: RUBYCON 330FW13AK6325
D1: TOSHIBA DUAL DIODE 1SS306, CONNECT DIODES IN SERIES
D2: PANASONIC MA2Z720
SCR: TOSHIBA S6A37
T1: TDK LDT565630T-002
T2: TOKYO COIL-BO-02
FLASHLAMP: PERKIN ELMER BGDC0007PKI5700

Figure 40. Complete Flashlamp Circuit Includes Capacitor Charging Components, Flash Capacitor C1, Trigger (R1, C2, T2, SCR) and Flashlamp. TRIGGER Command Biases SCR, Ionizing Lamp via T2. Resultant C1 Discharge Through Lamp Produces Light

Note 16. See References 9 and 10.

Note 17. "Red-eye" in a photograph is caused by the human retina reflecting the light flash with a distinct red color. It is eliminated by causing the eye's iris to constrict in response to a low intensity flash immediately preceding the main flash.

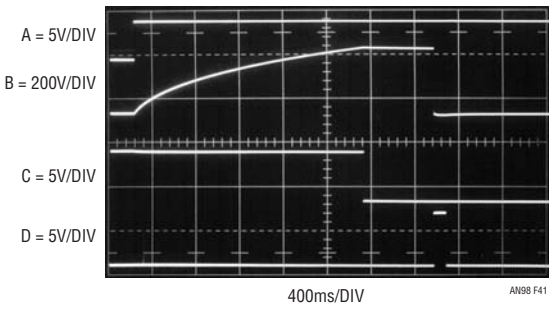


Figure 41. Capacitor Charging Waveforms Include Charge Input (Trace A), C1 (Trace B), DONE Output (Trace C) and TRIGGER Input (Trace D). C1's Charge Time depends Upon Its Value and Charge Circuit Output Impedance. TRIGGER Input, Widened for Figure Clarity, May Occur any Time After DONE Goes Low

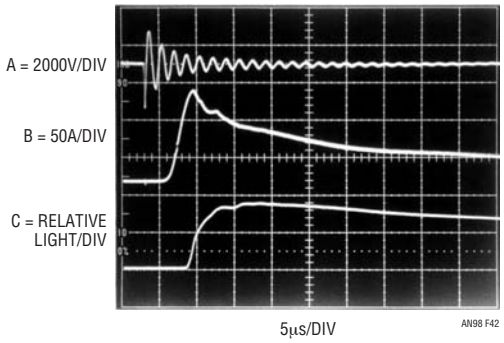


Figure 42. High Speed Detail of Trigger Pulse (Trace A), Resultant Flashlamp Current (Trace B) and Relative Light Output (Trace C). Current Exceeds 100A After Trigger Pulse Ionizes Lamp

current begins its ascent to over 100A. The current rises smoothly in 3.5μs to a well defined peak before beginning its descent. The resultant light produced rises more slowly, peaking in about 7μs before decaying. Slowing the oscilloscope sweep permits capturing the entire current and light events. Figure 43 shows that light output (trace B) follows lamp current (trace A) profile, although current peaking is more abrupt. Total event duration is ≈200μs with most energy expended in the first 100μs.

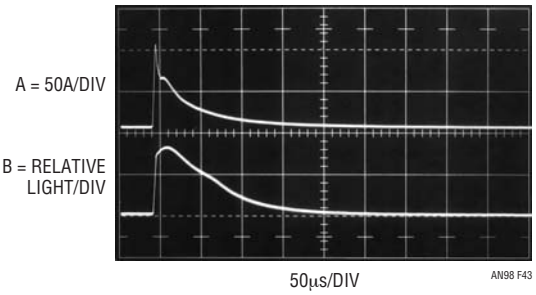


Figure 43. Photograph Captures Entire Current (Trace A) and Light (Trace B) Events. Light Output Follows Current Profile Although Peaking is Less Defined. Waveform Leading Edges Enhanced for Figure Clarity

0V to 300V Output DC/DC Converter

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 44 shows the LT3468 photoflash capacitor charger, described in the previous application, used as a general purpose, high voltage DC/DC converter. Normally, the LT3468 regulates its output at 300V by sensing T1's flyback pulse characteristic. This circuit forces the LT3468 to regulate at lower voltages by truncating its charge cycle before the output reaches 300V. A1 compares a resistively divided down portion of the output with the program input voltage. When the program input voltage (A1 + input) is exceeded by the output derived potential (A1 – input) A1's output goes low, shutting down the LT3468. The feedback capacitor provides AC hysteresis, sharpening A1's output to prevent chattering at the trip point. The LT3468 remains shut down until the output voltage drops low enough to

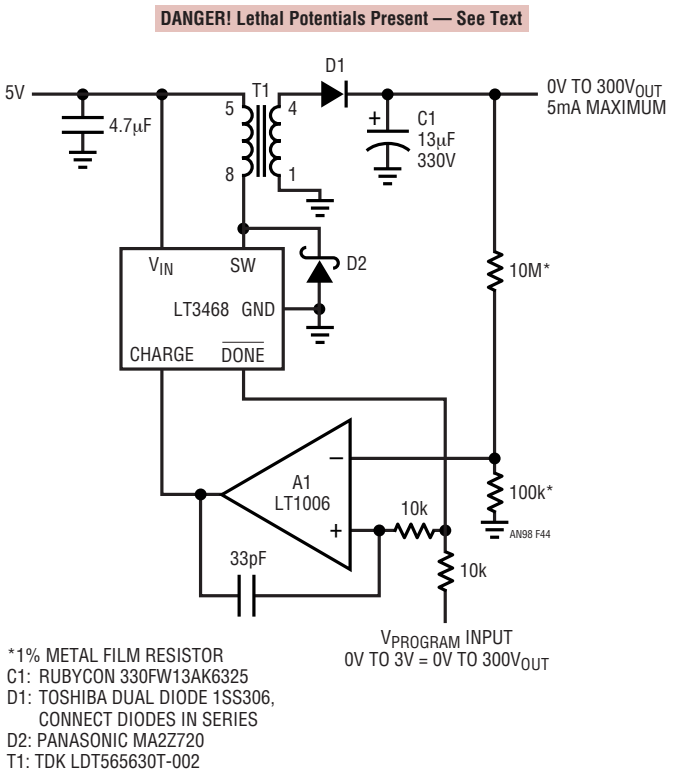


Figure 44. A Voltage Programmable 0V to 300V Output Regulator. A1 Controls Regulator Output by Duty Cycle Modulating LT3468/T1 DC/DC Converter Power Delivery

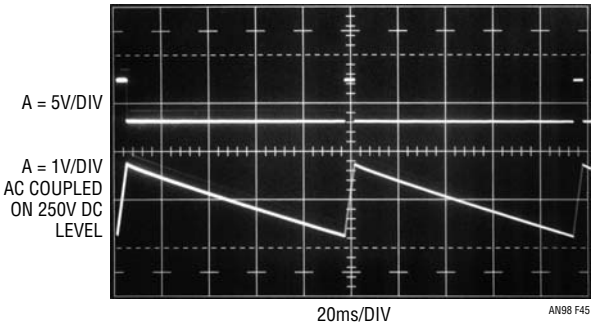


Figure 45. Details of Figure 44's Duty Cycle Modulated Operation. High Voltage Output (Trace B) Ramps Down Until A1 (Trace A) Goes High, Enabling LT3468/T1 to Restore Output. Loop Repetition Rate Varies with Input Voltage, Output Set Point and Load

trip A1's output high, turning it back on. In this way, A1 duty cycle modulates the LT3468, causing the output voltage to stabilize at a point determined by the program input. Figure 45 shows a 250V DC output (trace B) decaying down about 2V until A1 (trace A) goes high, enabling the LT3468 and restoring the loop. This simple circuit works well, regulating over a programmable 0V to

300V range, although its inherent hysteretic operation mandates the 2V output ripple noted. Loop repetition rate varies with input voltage, output set point and load but the ripple is always present. The next circuit essentially eliminates the ripple at the cost of increased complexity.

Low Ripple and Noise 0V to 300V Output DC/DC Converter

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 46 uses a post-regulator to reduce Figure 44's output ripple and noise to only 2mV. A1 and the LT3468 are identical to the pervious circuit, except for the 15V zener diode in series with the 10M-100k feedback divider. This component causes C1's voltage, and hence Q1's collector, to regulate 15V above the $V_{PROGRAM}$ inputs dictated point. The $V_{PROGRAM}$ input is also routed to the A2-Q2-Q1 linear post-regulator. A2's 10M-100k feedback divider does not include a zener, so the post-regulator follows the $V_{PROGRAM}$ input with no offset. This arrangement forces 15V across Q1 at all output voltages. This figure is high enough to eliminate undesirable ripple and noise from the output while keeping Q1 dissipation low.

Q3 and Q4 form a current limit, protecting Q1 from overload. Excessive current through the 50Ω shunt turns Q3 on. Q3 drives Q4, shutting down the LT3468. Simultaneously a portion of Q3's collector current turns Q2 on hard, shutting off Q1. This loop dominates the normal regulation feedback, protecting the circuit until the overload is removed.

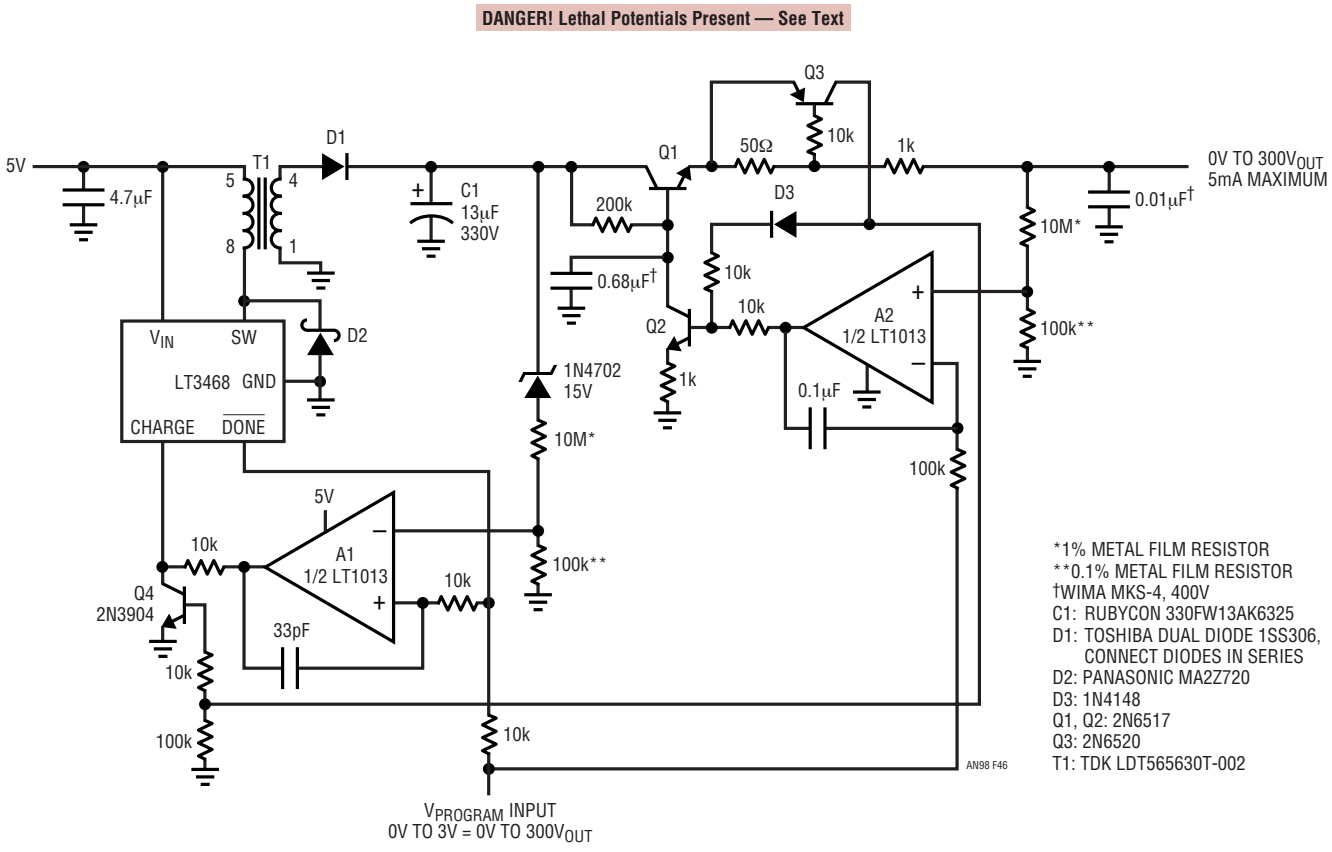


Figure 46. Post-Regulation Reduces Figure 44's 2V Output Ripple to 2mV. LT3468-Based DC/DC Converter, Similar to Figure 44, Delivers High Voltage to Q1 Collector. A2, Q1, Q2 Form Tracking, High Voltage Linear Regulator. Zener Sets Q1 V_{CE} = 15V, Ensuring Tracking with Minimal Dissipation. Q3-Q4 Limit Short-Circuit Output Current

Figure 47 shows just how effective the post regulator is. When A1 (trace A) goes high, Q1's collector (trace B) ramps up in response (note LT3468 switching artifacts on ramps upward slope). When the A1-LT3468 loop is satisfied, A1 goes low and Q1's collector ramps down. The circuits output post-regulator (trace C), however, rejects the ripple, showing only 2mV of noise. Slight trace blurring derives from A1-LT3468 loop jitter.

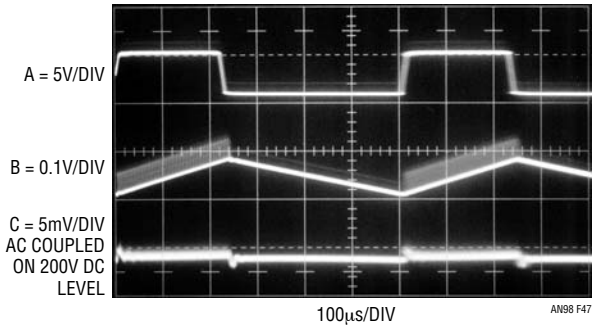


Figure 47. Low Ripple Output (Trace C) is Apparent in Post-Regulator's Operation. Traces A and B are A1 Output and Q1's Collector, Respectively. Trace Blurring, Right of Photo Center, Derives from Loop Jitter

5V to 200V Converter for APD Bias

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Avalanche photodiodes (APD) require high voltage bias. Figure 48's design provides 200V from a 5V input. The circuit is a basic inductor flyback boost regulator with a major important deviation. Q1, a high voltage device, has been interposed between the LT1172 switching regulator and the inductor. This permits the regulator to control Q1's high voltage switching without undergoing high voltage stress. Q1, operating as a "cascode" with the LT1172's internal switch, withstands L1's high voltage flyback events[18]. Diodes associated with Q1's source terminal

Note 18. See References 8 (page 8), 11 (Appendix D) and 22.

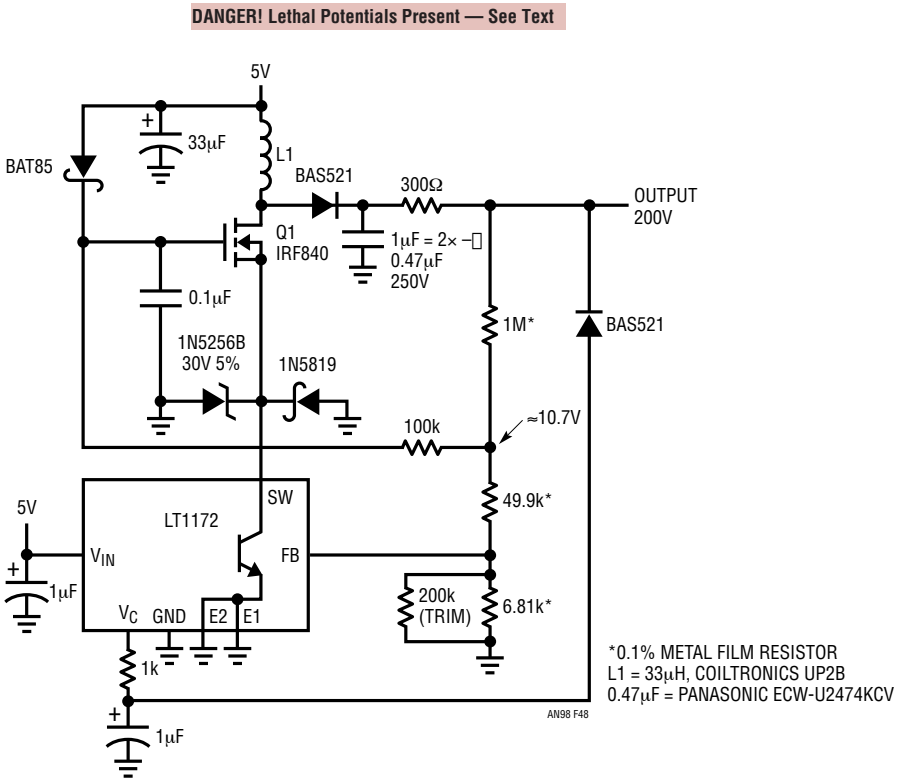


Figure 48. 5V to 200V Output Converter for APD Bias. Cascoded Q1 Switches High Voltage, Allowing Low Voltage Regulator to Control Output. Diode Clamps Protect Regulator from Transient Events; 100k Path Bootstraps Q1's Gate Drive from Output. Output Connected 300Ω-Diode Combination Provides Short-Circuit Protection

clamp L1 orginated spikes arriving via Q1's junction capacitance. The high voltage is rectified and filtered, forming the circuit's output. Feedback to the regulator stabilizes the loop and the RC at the V_C pin provides frequency compensation. The 100k path from the output divider bootstraps Q1's gate drive to about 10V, ensuring saturation. The output connected 300Ω-diode combination provides short-circuit protection by shutting down the LT1172 if the output is accidentally grounded. The 200k trim resistor sets the 200V output ±2% while using standard values in the feedback divider.

Figure 49 shows operating waveforms. Traces A and C are LT1172 switch current and voltage, respectively. Q1's drain is trace B. Current ramp termination results in a high voltage flyback event at Q1's drain. A safety attenuated version of the flyback appears at the LT1172 switch. The sinosoidal signature, due to inductor ring-off between conduction cycles, is harmless.

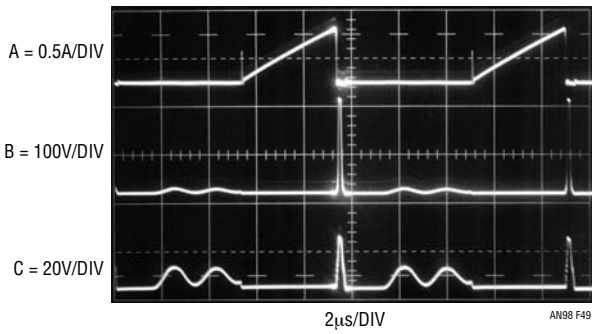


Figure 49. Waveforms for 5V to 200V Converter Include LT1172 Switch Current and Voltage (Traces A and C, Respectively) and Q1's Drain Voltage (Trace B). Current Ramp Termination Results in High Voltage Flyback Event at Q1 Drain. Safely Attenuated Version Appears at LT1172 Switch. Sinosoidal Signature, Due to Inductor Ring-Off Between Current Conduction Cycles, is Harmless. All Traces Intensified Near Center Screen for Photographic Clarity

Wide Range, High Power, High Voltage Regulator

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, LETHAL POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH, AND MAKING CONNECTIONS TO, THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, HIGH VOLTAGE POTENTIALS. USE CAUTION.

Figure 50 is an example of a monolithic switching regulator making a complex function practical. This regulator provides outputs from millivolts to 500V at 100W with 80% efficiency[19]. A1 compares a variable reference voltage with a resistively scaled version of the circuits output and biases the LT1074 switching regulator configuration. The switcher's DC output drives a DC/DC converter comprised of L1, Q1 and Q2. Q1 and Q2 receive out-of-phase square wave drive from the 74C74 ÷ 4 flip-flop stage and the LTC1693 FET drivers. The flip-flop is clocked from the LT1074 V_{SW} output via the Q3 level shifter. The LT3010 provides 12V power for A1, the 74C74 and the LTC1693. A1 biases the LT1074 regulator to produce the DC input at the DC/DC converter required to balance the loop. The converter has a voltage gain of about 20, resulting in high voltage output. This output is resistively divided down, closing the loop at A1's negative input. Frequency compensation for this loop must accommodate the significant phase errors generated by the LT1074 configuration, the DC/DC converter and the output LC filter. The 0.47μF roll-off term at A1 and the 100Ω-0.15μF RC lead network provide the compensation, which is stable for all loads.

Note 19. This circuit is an updated version of Reference 12.

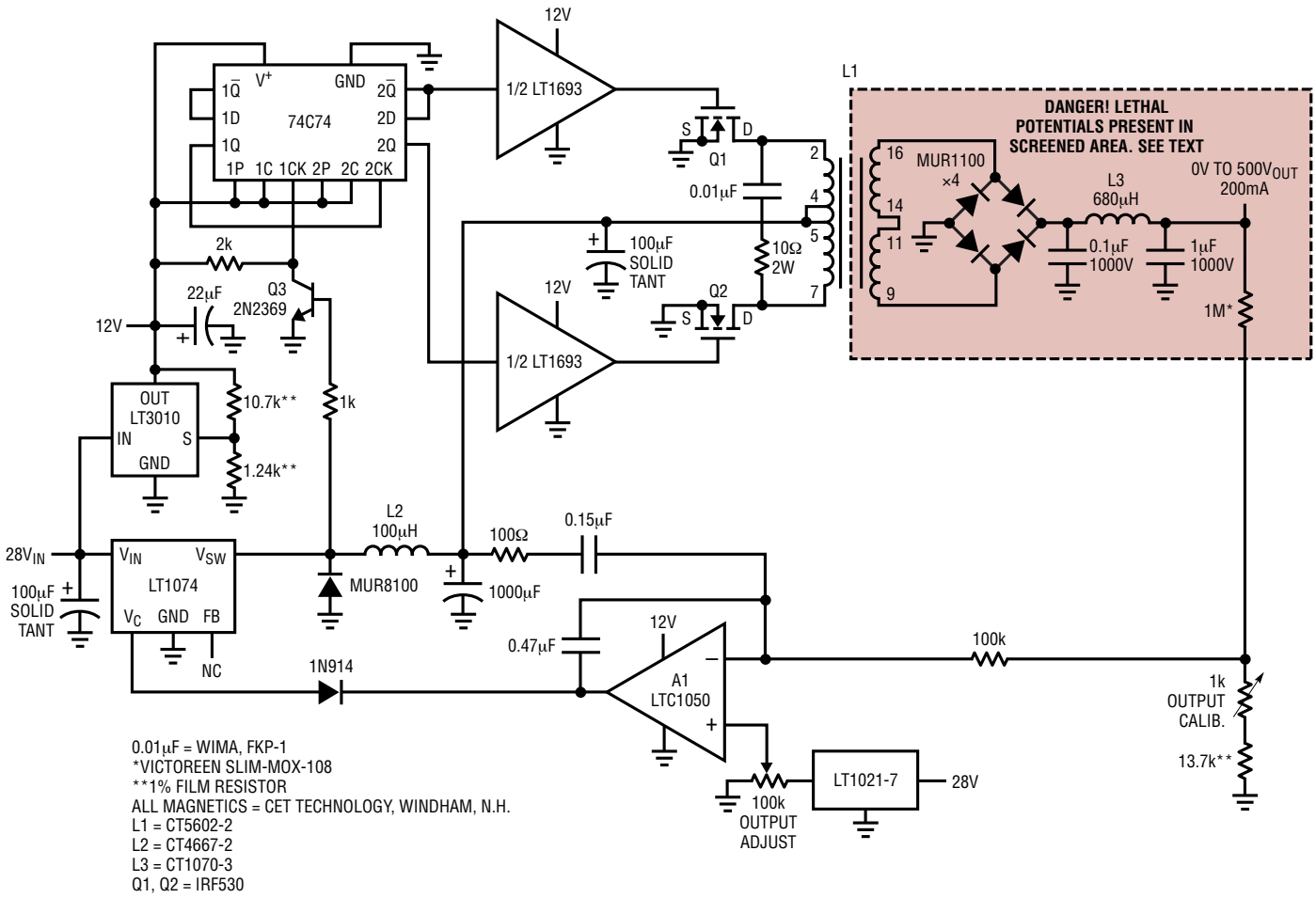


Figure 50. LT1074 Permits High Voltage Output Over 100dB Range with Power and Efficiency. DANGER! Lethal Potentials Present—See Text

Figure 51 gives circuit waveforms at 500V output into a 100W load. Trace A is the LT1074 V_{SW} pin while trace B is its current. Traces C and D are Q1 and Q2's drain waveforms. The disturbance at the leading edges is due to cross-current conduction, which lasts about 300ns—a small percentage of the cycle. Transistor currents during this interval remain within reasonable values, and no overstress or dissipation problems occur. This effect could be eliminated with non-overlapping drive to Q1 and Q2[20], although there would be no reliability or significant efficiency gain.

All waveforms are synchronous because the flip-flop drive stage is clocked from the LT1074 V_{SW} output. The LT1074's maximum 95% duty cycle means that the Q1-Q2 switches can never see destructive DC drive. The only condition allowing DC drive occurs when the LT1074 is at zero duty cycle. This case is clearly nondestructive, because L1 receives no power.

Figure 52 shows the same circuit points as Figure 51 but at only 5mV output. Here, the loop restricts drive to the DC/DC converter to small levels. Q1 and Q2 chop just 60mV into L1. At this level L1's output diode drops look large, but loop action forces the desired 0.005V output.

The LT1074's switched mode drive to L1 maintains high efficiency at high power, despite the circuits wide output range[21].

Note 20. See Reference 24 for an example of this technique.

Note 21. A circuit related to the one presented here appears in Reference 13. Its linear drive to the step-up DC/DC converter forces dissipation, limiting output power to about 10W.

Figure 53 shows output noise at 500V into a 100W load. Q1-Q2 chopping artifacts are clearly visible, although limited to about 50mV. The coherent noise characteristic is traceable to the synchronous clocking of Q1 and Q2 by the LT1074.

A 50V to 500V step command into a 100W load produces the response of Figure 54. Loop response on both edges is clean, with the falling edge slightly underdamped. This slew asymmetry is typical of switching configurations, because the load and output capacitor determine negative slew rate. The wide range of possible loads mandates a compromise when setting frequency compensation. The falling edge could be made critically or even over damped, but the response time for other conditions would suffer. The compensation used seems a reasonable compromise.

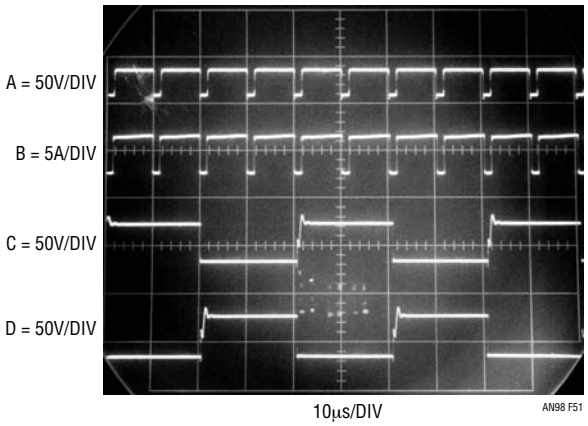


Figure 51. Figure 50's Operating Waveforms at 500V Output Into a 100W Load

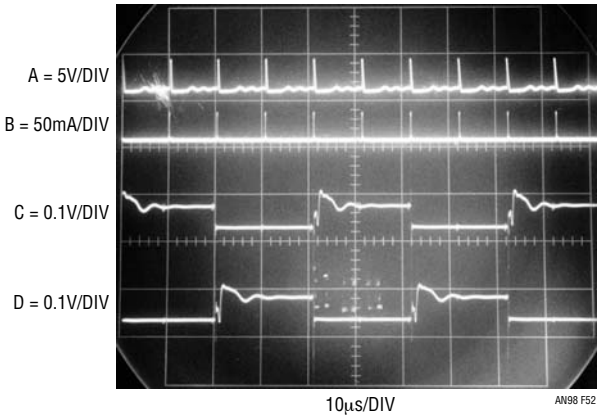


Figure 52. Operating Waveforms at 0.005V Output

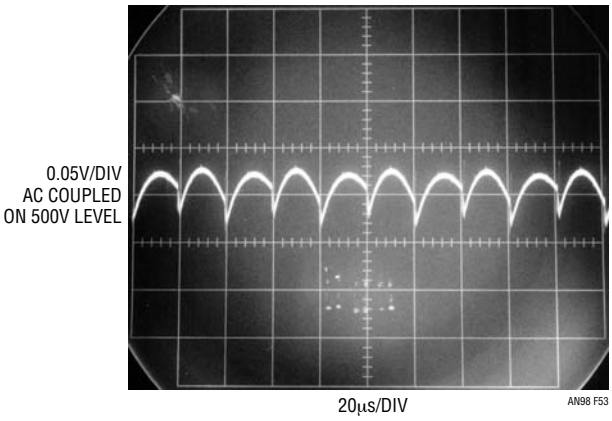


Figure 53. Output Noise at 500V into a 100W Load. Residue is Composed of Q1-Q2 Chopping Artifacts. DANGER! Lethal Potentials Present—See Text

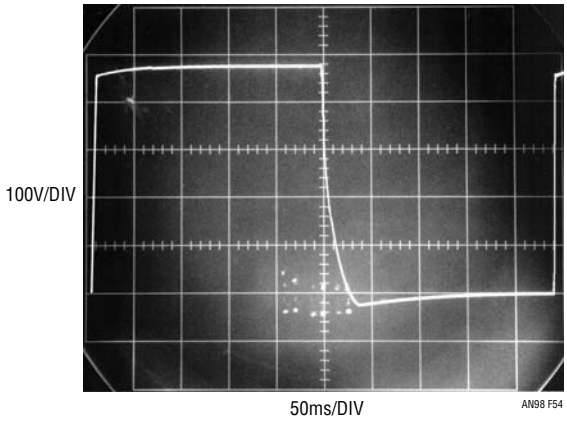


Figure 54. 500V Step Response with 100W Load (Photo Retouched for Clarity). DANGER! Lethal Potentials Present—See Text

5V to 3.3V, 15A Paralleled Linear Regulator

Figure 55 is another high power supply; unlike the previous example, it is a linear regulator. Two 7.5A regulators are paralleled in a "master-slave" arrangement. The "master" regulator is wired to produce a 3.3V output in the conventional manner. The 124Ω feedback resistor senses at the 0.001Ω shunt located directly before the circuit output. The "slave" regulator, also wired for a nominal 3.3V output, sources the circuit output in identical fashion. A1, sensing the regulators difference voltage, adjusts the "slave" regulator to equal the master's output voltage. This allows the regulators to equally share the load current. The 0.001Ω shunts cause negligible regulation loss, but provide adequate signal for A1.

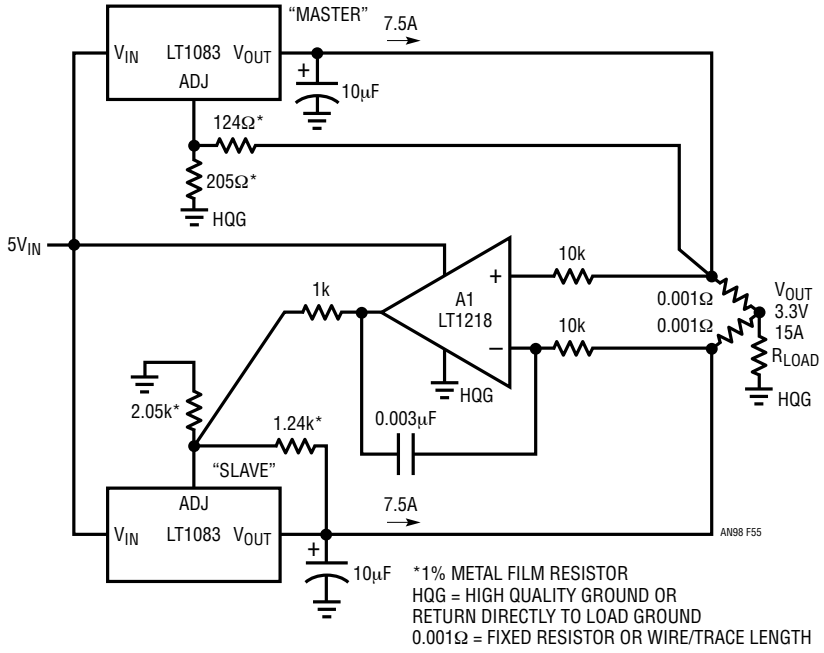


Figure 55. Paralleled Regulators Share Load Current. Amplifier Senses Differential Regulator Voltage; Biases "Slave" to Equalize Output Currents. Remote Sensing Negates Lead Wire Voltage Drops

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APPENDIX A

How Much Bandwidth is Enough?

Accurate wideband oscilloscope measurements require bandwidth. A good question is just how much is needed. A classic guideline is that "end-to-end" measurement system rise time is equal to the root-sum-square of the system's individual component's rise times. The simplest case is two components; a signal source and an oscilloscope. Figure A1's plot of $\sqrt{signal^2 + oscilloscope^2}$ rise time versus error is illuminating. The figure plots signal-to-oscilloscope rise time ratio versus observed rise time (rise time is bandwidth restated in the time domain, where:

$$Rise\,Time\ (nanoseconds) = \frac{350}{Bandwidth\ (MHz)}).$$

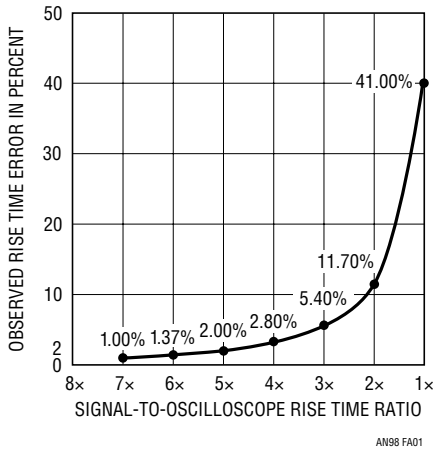


Figure A1. Oscilloscope Rise Time Effect on Rise Time Measurement Accuracy. Measurement Error Rises Rapidly as Signal-to-Oscilloscope Rise Time Ratio Approaches Unity. Data, Based on Root-Sum-Square Relationship, Does Not Include Probe, Which Does Not Follow Root-Sum-Square Law

The curve shows that an oscilloscope 3 to 4 times faster than the input signal rise time is required for measurement accuracy inside about 5%. This is why trying to measure a 1ns rise time pulse with a 350MHz oscilloscope (t_{RISE} = 1ns) leads to erroneous conclusions. The curve indicates a monstrous 41% error. Note that this curve does not include the effects of passive probes or cables connecting the signal to the oscilloscope. Probes do not necessarily follow root-sum-square law and must be carefully chosen and applied for a given measurement. For details, See Appendix B. Figure A2, included for reference, gives 10 cardinal points of rise time/bandwidth equivalency between 1MHz and 5GHz.

RISE TIME	BANDWIDTH
70ps	5GHz
350ps	1GHz
700ps	500MHz
1ns	350MHz
2.33ns	150MHz
3.5ns	100MHz
7ns	50MHz
35ns	10MHz
70ns	5MHz
350ns	1MHz

Figure A2. Some Cardinal Points of Rise Time/Bandwidth Equivalency. Data is Based on Rise Time/Bandwidth Formula in Text

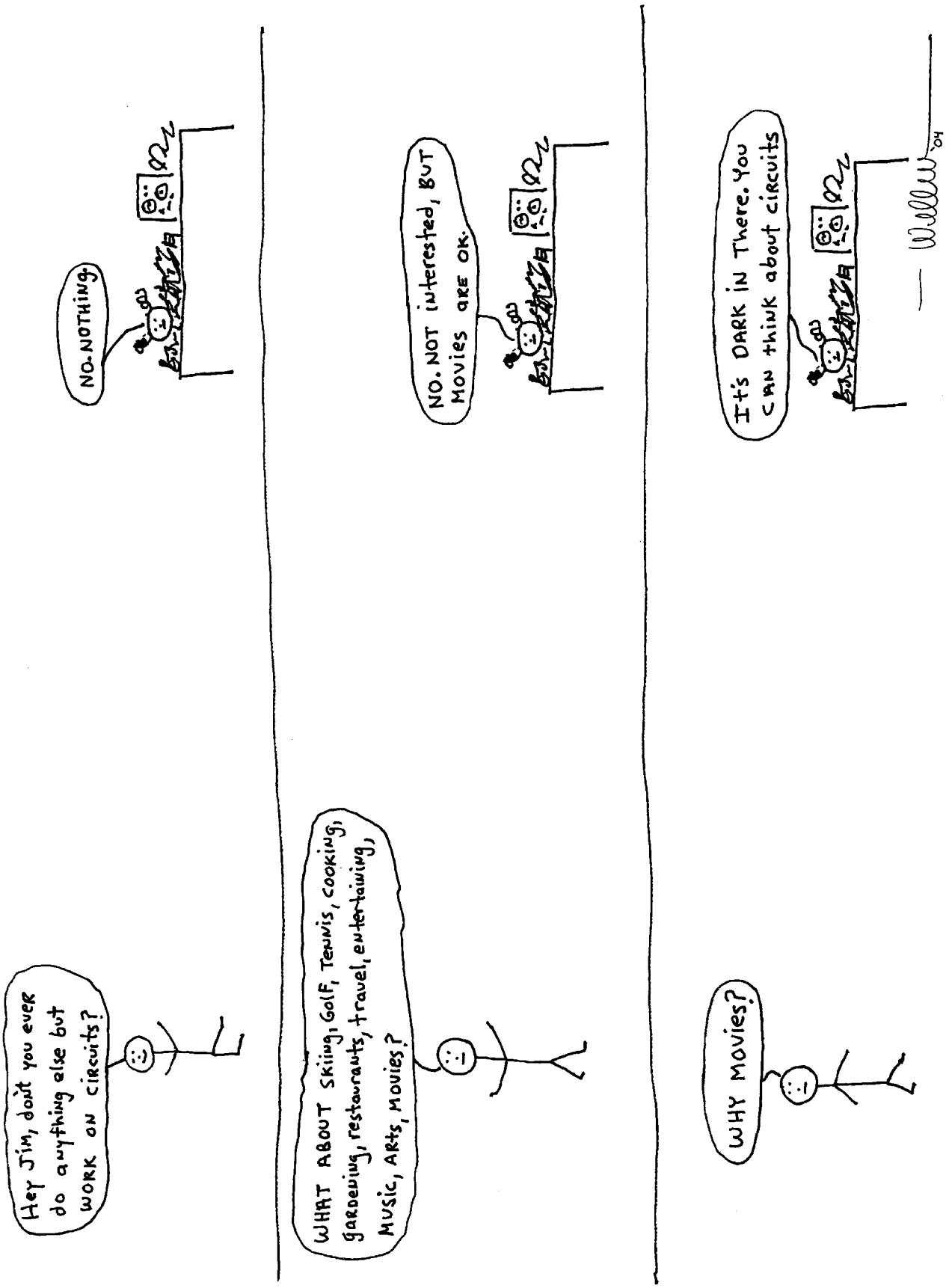
APPENDIX B

Connections, Cables, Adapters, Attenuators, Probes and Picoseconds

Subnanosecond rise time signal paths must be considered as transmission lines. Connections, cables, adapters, attenuators and probes represent discontinuities in this transmission line, deleteriously effecting its ability to faithfully transmit desired signal. The degree of signal corruption contributed by a given element varies with its deviation from the transmission lines nominal impedance. The practical result of such introduced aberrations is degradation of pulse rise time, fidelity, or both. Accordingly, introduction of elements or connections to the signal path should be minimized and necessary connections and elements must be high grade components. Any form of connector, cable, attenuator or probe must be fully specified for high frequency use. Familiar BNC hardware becomes lossy at rise times much faster than 350ps. SMA components are preferred for the rise times described in the text. Additionally, cable should be 50Ω "hard line" or, at least, teflon-based coaxial cable fully specified for high frequency operation. Optimal connection practice eliminates any cable by coupling the signal output *directly* to the measurement input.

Mixing signal path hardware types via adapters (e.g. BNC/SMA) should be avoided. Adapters introduce significant parasitics, resulting in reflections, rise time degradation, resonances and other degrading behavior. Similarly, oscilloscope connections should be made directly to the instrument's 50Ω inputs, avoiding probes. If probes must be used, their introduction to the signal path mandates attention to their connection mechanism and high frequency compensation. Passive "Z_0" types, commercially available in 500Ω (10x) and 5kΩ(100x) impedances, have input capacitance below 1pf. Any such probe must be carefully frequency compensated before use or misrepresented measurement will result. Inserting the probe into the signal path necessitates some form of signal pick-off which nominally does not influence signal transmission. In practice, some amount of disturbance must be tolerated and its effect on measurement results evaluated. High quality signal pick-offs always specify insertion loss, corruption factors and probe output scale factor.

The preceding emphasizes vigilance in designing and maintaining a signal path. Skepticism, tempered by enlightenment, is a useful tool when constructing a signal path and no amount of hope is as effective as preparation and directed experimentation.



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