Converting Light to Digits: LTC1099 Half Flash 8-Bit A/D Converter Digitizes Photodiode Array

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INTRODUCTION

Automated pricing at the supermarket check out counter has been around for years. A quick swipe across the bar code reader produces funny beeping noises, and as quickly as you can say "laser," the product is priced. Bar code readers are expensive since the A/D's required conversion time is usually too fast for inexpensive dual slope converters. This application note describes a Linear Technology "Half Flash" A/D converter, the LTC1099, being connected to a 256 element line scan photodiode array. This technology adapts itself to hand held (i.e. low power) bar code readers, as well as high resolution automated machine inspection applications. Many FAX machines and page scanners use photodiode arrays and A/D converters to transmit and/or store digitized data. For the esoteric at heart, the photodiode array may be digitized and used in astronomical applications such as star tracking.

The LTC1099 includes an internal sample-and-hold (S/H). This allows the A/D to sample the individual elements (pixels) of the photodiode array at rates which maintain 8-bit accuracy to 156kHz. This is fast enough to allow good throughput on machine vision or bar code scanner applications. Some video systems only require 6-bits of accuracy; in these cases the sample rate can be 215kHz (typical). Additional benefits may be derived from digital signal processing, allowing machine vision systems to do digital filtering, baseline correction, and correlated double sampling.

Figure 1 shows a block diagram of the system. The circuit, timing and some of the optical constraints are detailed in the following paragraphs.

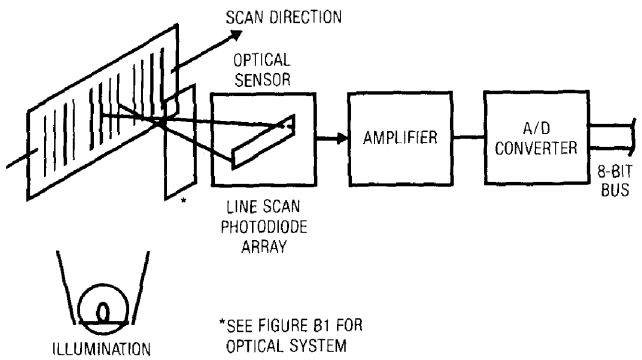


Figure 1. Optical–Digital Converter Block Diagram

ELECTRONIC SYSTEM DESIGN

Adding D/A to A/D System Makes Troubleshooting Easy

Finding bugs in an A/D system is never easy. When a photodiode array is added, system integration problems usually are very difficult to locate. In this application note, an inexpensive 12-bit D/A converter configured to accept only 8-bits was included as a troubleshooting aide. This D/A can be omitted in any final system design incorporating the LTC1099 and a photodiode array.

The schematic diagram for the system is shown in Figure 2. The LTC1099 (U3) is configured in $\overline{WR}$-RD Mode using the stand alone configuration. This allows the 8-bit digital output to be continuously input to a D/A. The amplified D/A output at U6, (8), is the reconstructed digital signal. That is, this output represents the analog signal

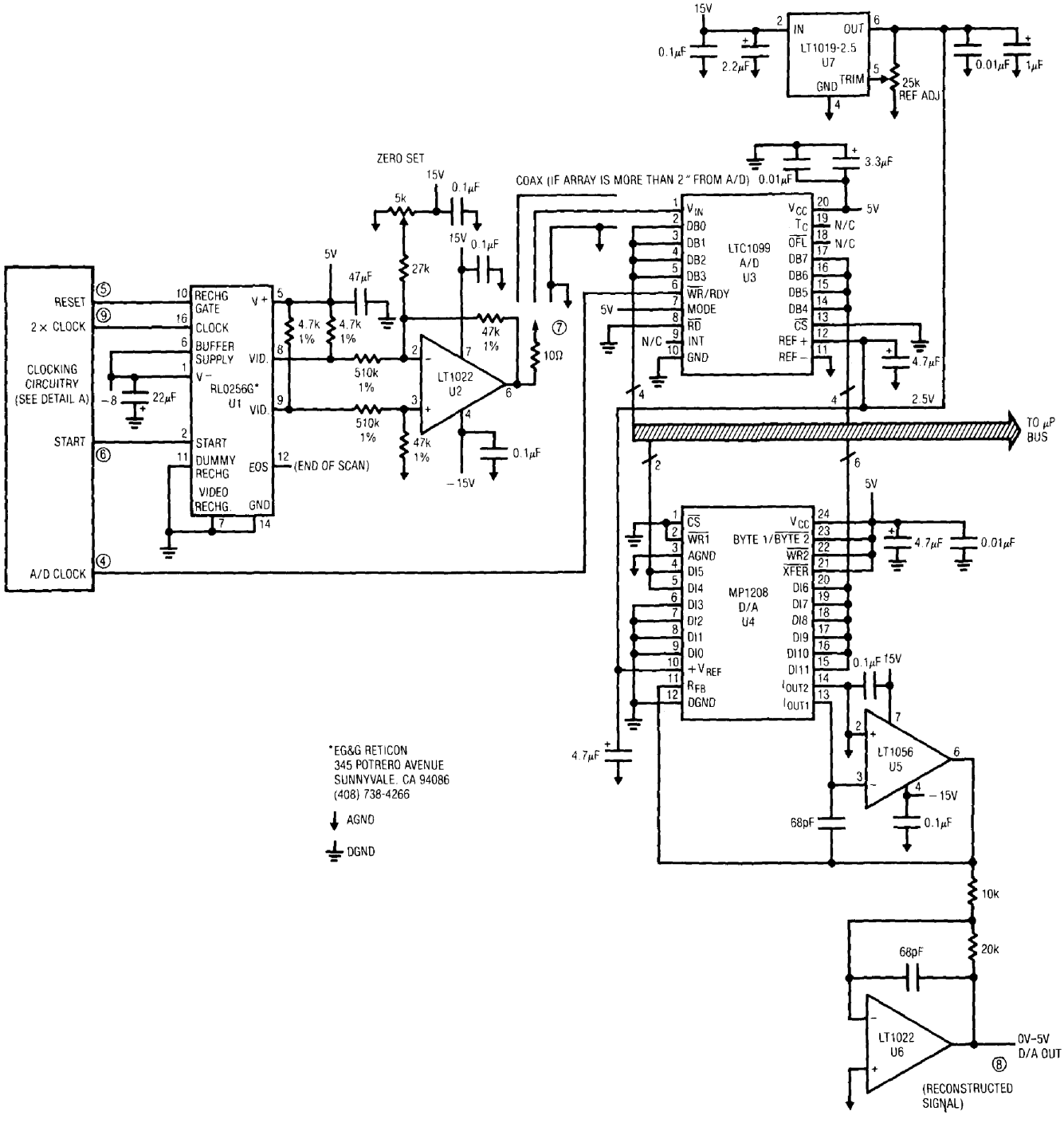
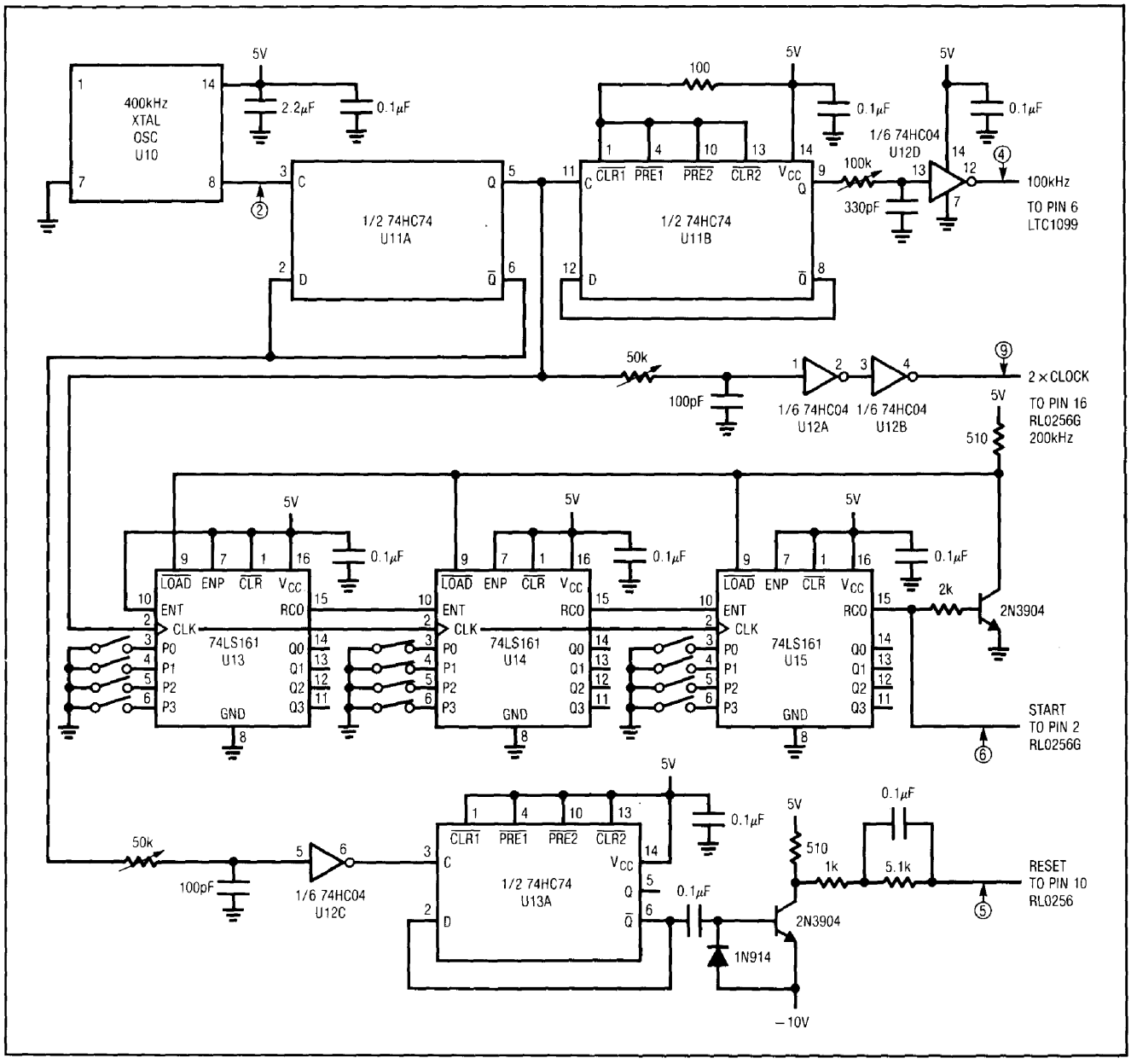


Figure 2. Schematic Diagram

that has been digitized and then converted back to analog by the D/A. This output allows the designer to directly compare the system output to the analog output of the photodiode array that is to be digitized.

As shown in Figure 2, the LTC1099 (U3) drives the 8-bit microprocessor bus and the D/A (U4). The current output of the D/A is converted to an output voltage by U5, an LT1056 JFET input operational amplifier. U6, an LT1022, amplifies and bandlimits the signal. Its output is 0 to 5V.

The system reference for the converters (both the A/D and the D/A) is an LT1019-2.5. This third generation bandgap voltage reference provides the 2.5V reference for the LTC1099 (which actually may be used with references as low as 1V) and the D/A.



Detail A of Schematic Diagram (Figure 2)

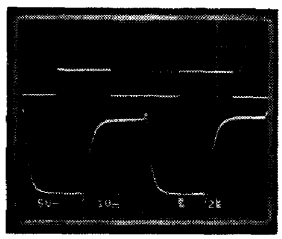
Figures 3 and 4 detail the A/D converter's operation. Figure 3 shows the $\overline{WR}$/RDY pulse from the clocking circuitry (top trace) and the analog output of the photodiode array at point (7). See Appendix A for discussion of clocking circuitry. The voltage output of the photodiode array is 256 "pulses" each of which represents the "exposure" of the individual photodiode. If a grating could be fabricated consisting of 128 black lines separated by 128 transparent spaces, and this grating could then be placed over the photodiode array with the proper magnification, the output pulses would represent alternating full scale and zero analog levels. Figures 3 and 4 show the analog and reconstructed digital outputs from a few pixels of the "evenly illuminated" array. Figure 3 details the timing required of the LTC1099. The falling edge of the $\overline{WR}$/RDY pulse initiates the conversion cycle of the LTC1099. As seen in the timing diagram, Figure 5, the analog input must be a stable 130ns before the falling edge of $\overline{WR}$/RDY occurs. Approximately 110ns after the falling edge, the internal sample-and-hold goes to hold mode and the analog input is ignored until the next conversion cycle. Figure 3 shows how this timing cycle is used to sample the output of the photodiode array.

The circuit as shown in Figure 2 allows easy interfacing to a microprocessor. The microprocessor system may contain, for example, a ROM with bar codes stored as they would appear when scanned optically and digitized. When an item is scanned, the microprocessor can compare (called a digital correlation) the scanned code to the stored codes and decide which product is being scanned.

Optical

The line scan array used in this application was an EG&G Reticon RL0256G photodiode array.* The array contains 256 photodiodes (also called pixels for "picture elements") on 25μm centers. See Figure 6 for more details. The device contains a row of silicon photodiodes, each with an associated storage capacitor on which to integrate photocurrent, and a multiplex switch for periodic readout. Readout is accomplished by an integrated shift register scanning circuit. A TTL clock is required for outputting the row of photodiodes to the output pin. A row of dummy photodiodes (photodiodes that have an opaque covering) is simultaneously read out with the active photodiodes to allow cancellation of multiplex switching transients. This array allows resolution to 25μm with standard optical techniques.

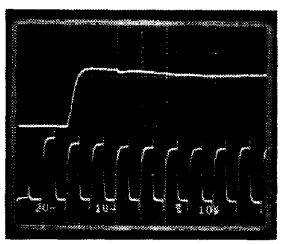
*The author would like to thank Mike Satterlund, Tom Silvey and Kevin Heher at EG&G Reticon for technical assistance with the Reticon part.



TOP-$\overline{WR}$/RDY SIGNAL TO LTC1099 (5V/CM) (4)

BOTTOM-ANALOG OUTPUT FROM PHOTODIODE ARRAY (1V/CM) (7)

Figure 3. A/D Clocking

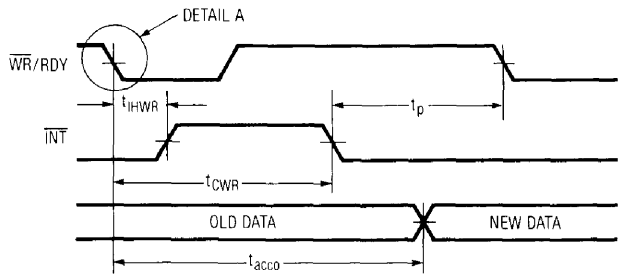


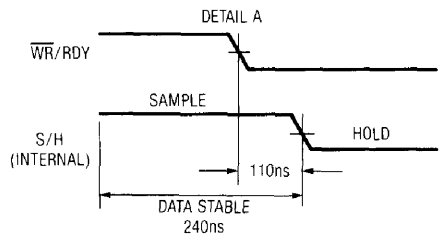
TOP-OUTPUT FROM D/A ILLUSTRATING PROPER DIGITIZATION (8)

BOTTOM-INPUT TO LTC1099 A/D FROM PHOTODIODE ARRAY THRU LT1022 BUFFER (7)

NOTE 1: CLOCK DELAY IN DAC RESPONSE.

Figure 4. Photodiode Array Output





t_{IHWR} = DELAY FROM $\overline{WR}$↓ TO $\overline{INT}$↓ = 240ns TYP
t_p = DELAY BETWEEN CONVERSIONS = 700ns TYP
t_{CWR} = CONVERSION TIME = 2.5μs TYP
t_{acco} = DELAY TIME $\overline{WR}$↓ TO NEW DATA VALID = t_{CWR} + 40ns TYP

Figure 5. Timing Diagram

Medium speed photodiode arrays have become inexpensive in recent years and, when connected to a "Half Flash" A/D converter like the LTC1099, provide an elegant, inexpensive solution to supermarket pricing, inventory control and other bar coding applications.

In the schematic of Figure 2 the photodiode array is shown as U1. It is clocked by a single phase TTL clock and associated driving signals which will be described later. The output of the array is a train of 256 charge pulses for each of the video and dummy video lines. The pulses on the dummy line contain switching transients only while those on the video line contain switching transients plus the video signal. The LT1022 FET input operational amplifier shown as U2 is used as a differential current amplifier. The output (as shown, for instance, in Figure 3) is a pulse whose peak amplitude has been scaled to a reasonable voltage (here it is 2.5V) to drive the A/D converter. Note that if the photodiode array amplifier (U2) is located any distance (greater than 3") from the A/D converter, a coaxial cable should be used to interconnect the two.

Figure 4 (bottom trace) shows a series of pulses output from operational amplifier U2. It is necessary to sample each pulse on the "flat top" to provide an accurate analog signal to the A/D converter. The top trace of Figure 4 is the reconstructed analog signal through the A/D—D/A chain, the test output. Note that it nicely follows the tops of the analog photodiode pulses (it is delayed one clock pulse).

The ease with which the A/D may be interfaced to a microprocessor and its speed makes the use of "baseline correction" easy. Baseline correction is an often used technique with photodiode arrays where the baseline or "dark" value of each photodiode is stored in memory. At power on, the dark value of each photodiode, or 256 individual 8-bit values are stored in memory. This allows the user greater dynamic range than by simply using an average of all the photodiodes "dark" values. The A/D converter's 156kHz maximum sampling rate allows the microprocessor to do baseline correction rapidly with little system "overhead."

Optical to Digital System Response

The photodiode array is clocked from the clocking circuitry as shown in the boxed section of Figure 2. U4, the D/A and operational amplifiers U5 and U6 provide a digitally reconstructed analog output which should closely resemble the analog pulse amplitudes at point (7).

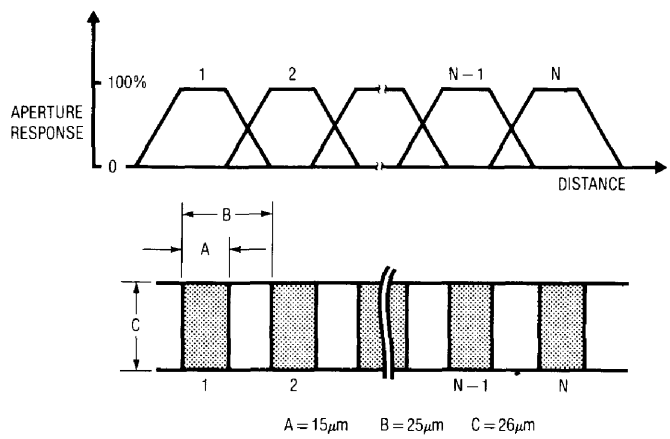


Figure 6. Sensor Geometry

Figure 7 shows the systems response to placing an optical grating directly on the glass window which covers the photodiode array. The bottom trace is the analog output from operational amplifier U2—point (7). The top trace is the output of the D/A taken at point (8). The linewidths that appear as "notches" in the traces are (from left to right): 400, 350, 300, 250 and 200μm (millionth of a meter). Similarly, Figure 8 shows the response to linewidths of 200, 150, 100, 90 and 80μm (from left to right in the photo). As before, the top trace is the output of the D/A taken at point (8), while the bottom trace is the analog output from operational amplifier U2 — point (7). It should be noted that this crude system only illustrates the power of the optical to digital concept. For an optimized system uniform illumination is required and a good optical system is needed to properly image the item to be inspected onto the line scan photodiode array. Some thoughts on an optical system are described in Appendix B.

The designer must be aware of the integration time of the photodiode array. Integration time is analogous to the shutter speed of a film camera. The longer the shutter is open, the more light is collected onto the film media, and hence the darker the film will be. Figure 9 shows two scans of the photodiode array. The integration time of the photodiode array or the "exposure time" is equivalent to the time between start pulses. Figure 9 shows the integration time to be about 6.4ms. This is not a fixed parameter, but varied by the settings of the DIP switches connected to U13, U14 and U15. It is recommended that integration times not exceed approximately 40ms (at room temperature) to prevent integrated dark current (the leakage current that flows in photodiode that is not illuminated) from making a significant contribution to the output charge. Cooling of the photodiode sensor may be used (as is always the case in astronomical applications) to lower the dark current and therefore allow an increase in integration time.

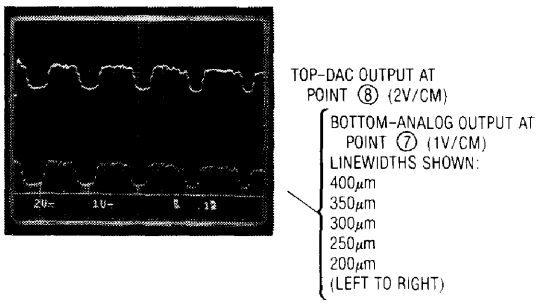


Figure 7. Optical Resolution

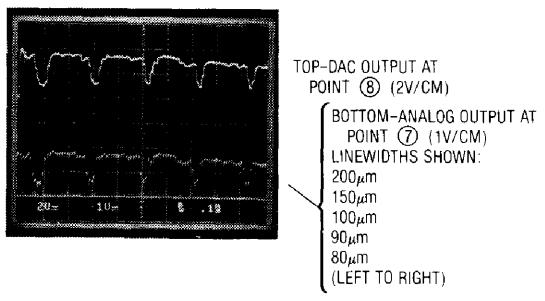


Figure 8. Resolution Photo

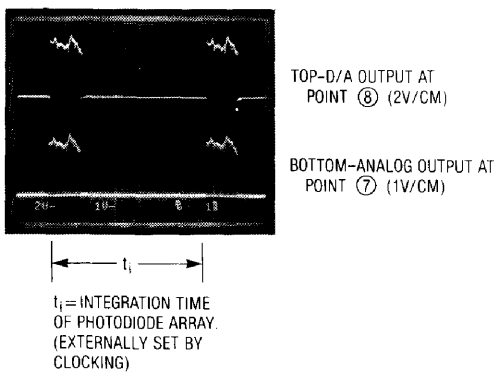


Figure 9. Photodiode Array Integration Time

APPENDIX A

Clocking Circuitry

The boxed section of Figure 2 details the clocking circuitry required to drive the photodiode array. There is nothing very unusual about the simple TTL circuitry required to drive the array. The clock signals are obtained from U10, a crystal oscillator. Counters U13 through U15 and the DIP switches set the number of clock periods between start pulses to any value up to 4096. This is the integration time, as described previously. The variable low pass filters (pots and capacitors) before the three sections of U12 allow delaying of the clocking signals to ensure that all the signals occur in the proper sequence. Figure A1 shows the reset pulse for the photodiodes (top) (5), the A/D $\overline{WR}$/RDY pulse (starts A/D conversion) (4) and the clock signal from the crystal oscillator (2).

Figure A2 details: the 2x clock to the photodiode array at (9), the A/D clock at (4) and the analog photodiode output at (7). Figure A3 shows the photodiode reset pulse signal at (5) along with the 2x clock at (9) and the A/D clock signal at (4).

Figure A4 shows the start pulse and the analog CCD output.

Note that for those intending on prototyping this circuitry, the EG&G Reticon data sheet on the RL0256G array is an absolute necessity to set up proper timing signals.

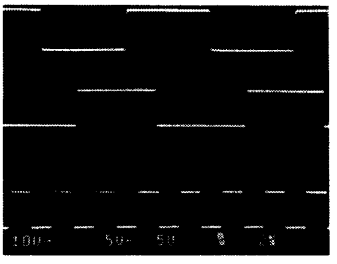


Figure A1. Timing Waveforms

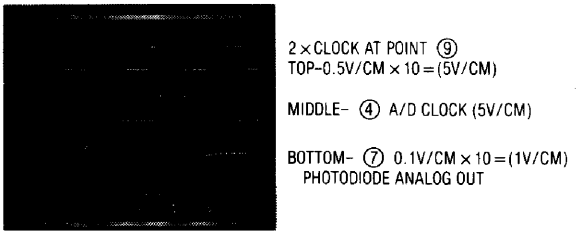


Figure A2. A/D "Convert" Signal Clock and Diode Array Output

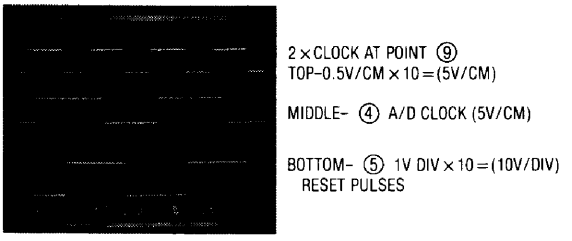


Figure A3. Timing Signals

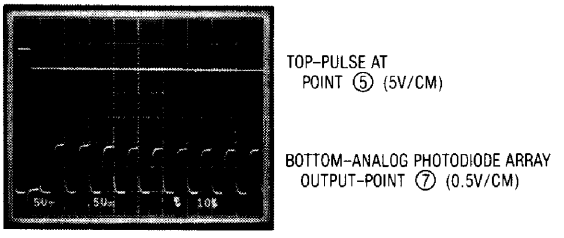


Figure A4. Start Pulse and Diode Array Output

APPENDIX B

Optical System Design

Optical system design is a complex subject in which one may obtain a Ph.D. In lieu of this option, Figure B1 shows in rough form the top view of an imaginary tin can inspection system. Lens A and lens B are two cylindrical lenses rotated 90 degrees from each other. Lens A as shown in the example system takes the columnated illumination and produces a line into the paper. When an object interrupts the illumination, the line imaged onto the photodiode array to be dark. In this way height can be measured.

Similarly, using lens B, a line of illumination may be formed parallel to the paper. When an object interrupts this illumination, a dark line is imaged onto a second photodiode array. In this way width may be measured.

Note carefully here, that we have not covered the issues of image magnification/demagnification. Obviously, an object 6 inches in height and 1 inch in width needs to be demagnified to fit the constraints of the photodiode aperture. These issues are beyond the scope of this Application Note.

**See for example:
Jenkins and White, "Fundamentals of Optics," McGraw Hill Book Co., NY, NY 1976
Hecht and Zajac, "Optics," Addison-Wesley Publishing Co., Reading, MASS Dec. 1976

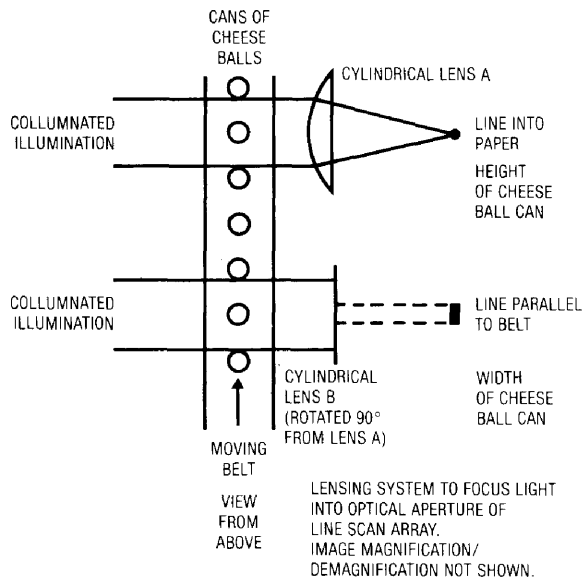


Figure B1. Optical System Design