Micropower Circuits for Signal Conditioning

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Low power operation of electronic apparatus has become increasingly desirable. Medical, remote data acquisition, power monitoring and other applications are good candidates for battery driven, low power operation. Micropower analog circuits for transducer-based signal conditioning present a special class of problems. Although micropower ICs are available, the interconnection of these devices to form a functioning micropower circuit requires care. (See Box Sections, "Some Guidelines for Micropower Design and an Example" and "Parasitic Effects of Test Equipment on Micropower Circuits.") In particular, trade-offs between signal levels and power dissipation become painful when performance in the 10-bit to 12-bit area is desirable. Additionally, many transducers and analog signals produce inherently small outputs, making micropower requirements complicate an already difficult situation. Despite the problems, design of such circuits is possible by combining high performance micropower ICs with appropriate circuit techniques.

Platinum RTD Signal Conditioner

Figure 1 shows a simple circuit for signal conditioning a platinum RTD. Correction for the platinum sensor's nonlinear response is included. Accuracy is 0.25°C over a 2°C to 400°C sensed range. One side of the sensor is grounded, highly desirable for noise considerations. For a 2°C sensed temperature, current consumption is 250µA, increasing to 335µA for a 400°C sensed temperature.

Figure 1. Platinum RTD Signal Conditioner with Curvature Correction

The platinum sensor is placed in a current driven bridge with the 1k resistors. The LM334 current source drives the bridge and its associated resistors set a 100µA operating level. The diode provides temperature compensation (see LM334 data sheet). The 39k resistor deliberately sustains voltage drop, minimizing LM334 die temperature rise to ensure good temperature tracking with the diode. The 100µA current is split by the bridge. This light current saves power, but restricts the platinum sensor's output to about 200µV/°C. The circuit's 0.25°C accuracy specification requires the LT®1006 low power precision op amp for stable gain. The LT1006 takes the signal differentially from the bridge to provide the circuit's output. Normally, the platinum sensor's slightly nonlinear response would cause several degrees error over the sensed temperature range. The 1.2M resistor gives slight positive feedback to correct for this. The amplifier's negative feedback path dominates, and the configuration is stable. The 1µF capacitors give a high frequency roll-off and the 180k resistor programs the LT1006 for 80µA quiescent current.

To calibrate this circuit, substitute a precision decade box (e.g., General Radio 1432) for R_P. Set the box to the 5°C value (1019.9Ω) and adjust the "5°C trim" for 0.05V output at the LT1006. Next, set the box for the 400°C value (2499.8Ω) and adjust the "400°C trim" for 4.000V output. Repeat this sequence until both points are fixed. The resistance values given are for a nominal 1000.0Ω (0°C) sensor. Sensors deviating from this nominal value can be used by factoring in the deviation from 1000.0Ω. This deviation, which is manufacturer-specified for each individual sensor, is an offset term due to winding tolerances during fabrication of the RTD. The gain slope of the platinum is primarily fixed by the purity of the material and is a very small error term.

Thermocouple Signal Conditioner

Figure 2 is another temperature sensing circuit, except the transducer is a thermocouple. Accuracy is within 1.5°C over a 0°C to 60°C sensed temperature and current consumption is about 125µA.

Thermocouples are inexpensive, have low impedances and feature self-generating outputs. They also produce low level outputs and require cold junction compensation, complicating signal conditioning. The bridge network, composed of the thermistor and R1-R4, provides cold junction compensation with the LT1004 acting as a voltage reference. The lithium battery noted allows the bridge to float and the thermocouple to be ground referred, eliminating the requirement for a differential amplifier. For the battery specified, life will approach 10 years. This is a good way to avoid the additional power drain of a multi-amplifier differential stage. The LT1006 is set up with a gain scaled to produce the output shown and the 270k resistor programs it for low current drain. Note that this circuit requires no trims.

Sampled Strain Gauge Signal Conditioner

Strain gauge bridge-based transducers present a challenge where low power operation is needed. The 350Ω impedance combined with low signal outputs (typically 1mV to 3mV output per volt of drive) presents problems. Even with only 1V of drive, bridge consumption still approaches 3mA. Dropping drive to 100mV reduces current to acceptable levels, but precludes high accuracy operation due to the miniscule output available. In many situations, continuous transducer information is unnecessary and sampled operation is viable. Short sampling duty cycle
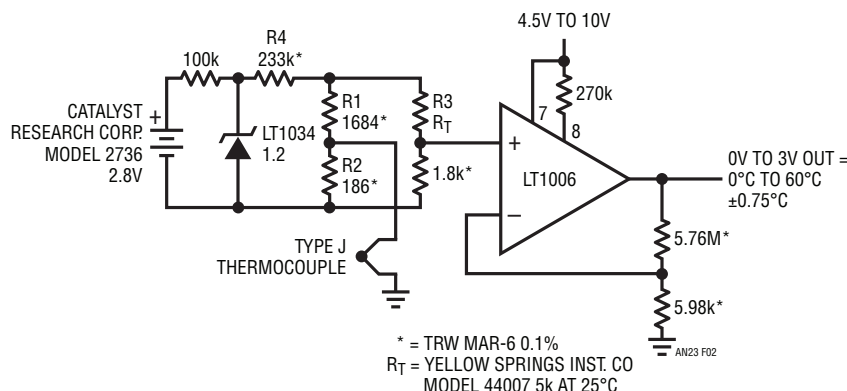

Figure 2. Thermocouple Signal Conditioner with Cold Junction Compensation

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permits high current bridge drive while maintaining low power operation. Figure 3 uses such a scheme to achieve dramatic power saving in a strain gauge bridge application (for a discussion of sampled operation considerations, see Box Section B, "Sampling Techniques and Components for Micropower Circuits").

In this circuit, Q2 is off when the "sample command" is low. Under these conditions only A4 and the CD4016 receive power, and current drain is inside 125µA. When the sample command is pulsed high, Q2's collector (Trace A, Figure 4) goes high, providing power to all other circuit elements. The 10Ω-1µF RC at the LT1021 prevents the strain bridge
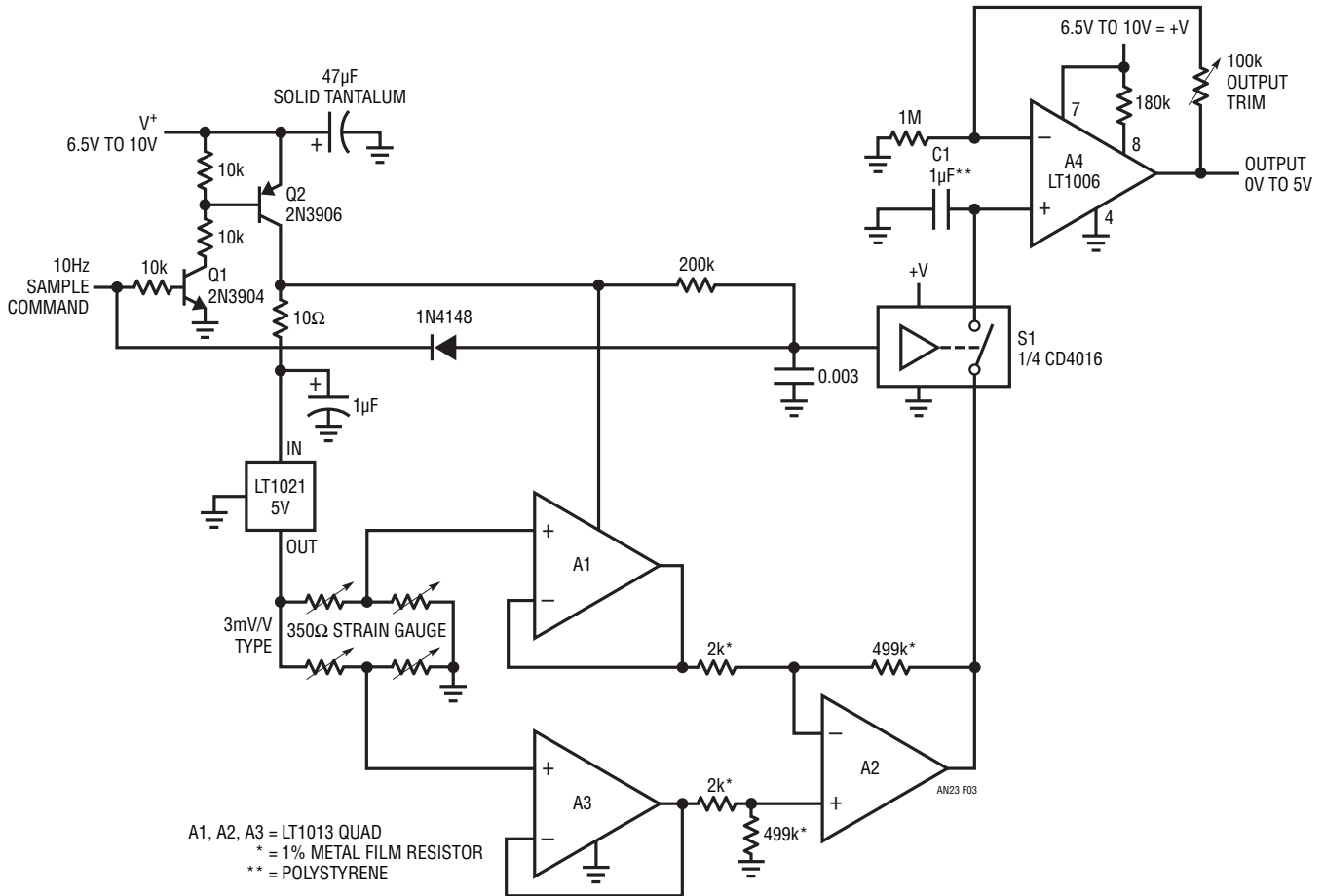
Figure 3. Sampled Strain Gauge Bridge Signal Conditioner

HORIZ = 200µs/DIV   AN23 F04
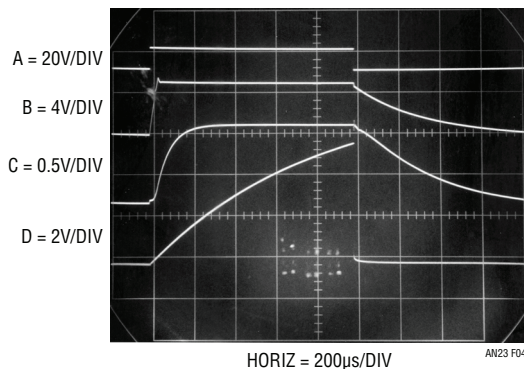
Figure 4. Waveforms for the Sampled Strain Gauge Signal Conditioner

from seeing a fast rise pulse which could cause long-term transducer degradation. The LT1021-5 reference output (Trace B) drives the strain bridge, and differential amplifier A1-A3's output appears at A2 (Trace C). Simultaneously, S1's switch control input (Trace D) ramps toward Q2's collector. At about one-half Q2's collector voltage (in this case just before mid-screen) S1 turns on, and A2's output is stored in C1. When the sample command drops low, Q2's collector falls, the bridge and its associated circuitry shut down and S1 goes off. C1's stored value appears at gain scaled A4's output. The RC delay at S1's control input ensures glitch-free operation by preventing C1 from updating until A2 has settled. During the 1ms sampling phase, supply current approaches 20mA, but a 10Hz sampling rate cuts effective drain below 200µA. Slower sampling rates will further reduce drain, but C1's droop rate (about 1mV/100ms) sets an accuracy constraint. The 10Hz rate provides adequate bandwidth for most transducers. For 3mV/V slope factor transducers, the gain trim shown allows calibration. It should be rescaled for other types. This circuit's effective current drain is about 300µA and A4's output is accurate enough for 12-bit systems.

Strobed Operation Strain Gauge Bridge Signal Conditioner

Figure 5's circuit also switches power to minimize strain bridge caused losses, but is not intended for continuously sampled operation. This circuit is designed to sit in the quiescent state for long periods with relatively brief on times. A typical application would be remote weight information in storage tanks where weekly readings are sufficient. This circuit has the advantage of not requiring a differential amplifier, despite the strain bridge's floating output. Additionally, it provides almost full rated drive to the strain bridge, enhancing accuracy. Quiescent current is about 150µA with on-state current typically 50mA.

With Q1's base unbiased, all circuitry is off except the LT1054 plus-to-minus voltage converter, which draws a 150µA quiescent current. When Q1's base is pulled low, its collector supplies power to A1 and A2. A1's output goes high, turning on the LT1054. The LT1054's output (Pin 5) heads toward –5V and Q2 comes on, permitting bridge current to flow. To balance its inputs, A1 servo controls the LT1054 to force the bridge's midpoint to 0V.
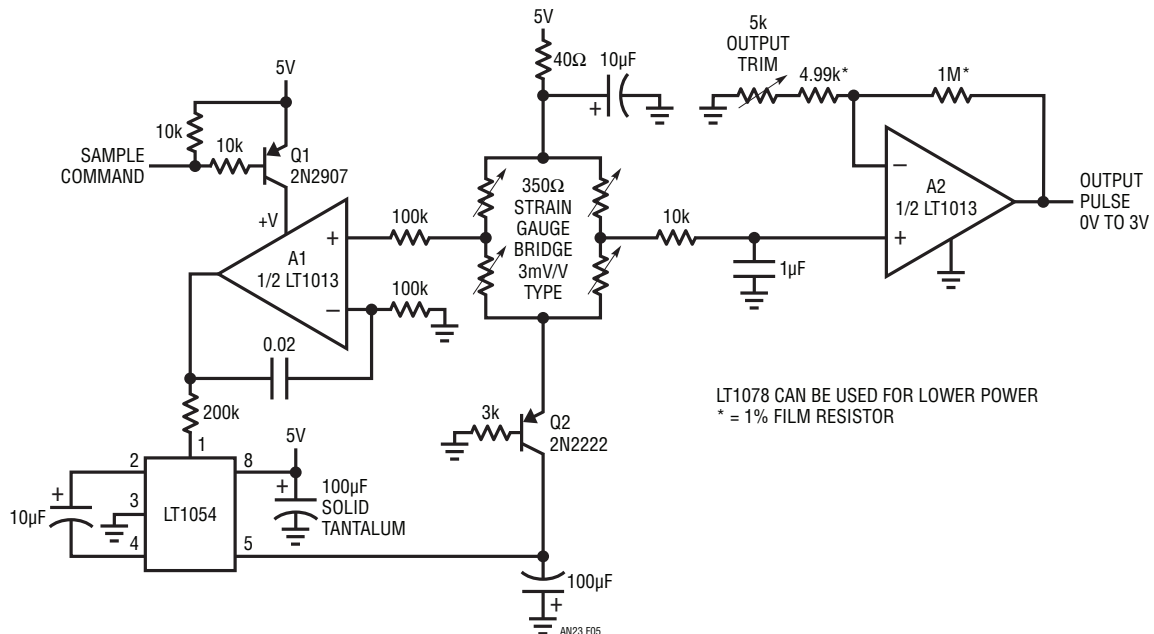

Figure 5. Strobed Power Strain Bridge Signal Conditioner

The bridge ends up with about 8V across it, requiring the 100mA capability LT1054 to sink about 24mA. The 0.02µF capacitor stabilizes the loop. The A1-LT1054 loop negative output sets the bridge's common mode voltage to zero, allowing A2 to take a simple single-ended measurement. The "output trim" scales the circuit for 3mV/V type strain bridge transducers, and the 100k-0.1µF combination provides noise filtering.

Thermistor Signal Conditioner for Current Loop Application

4mA to 20mA "current loop" control is common in industrial environments. Circuitry used to modulate transducer data into this loop must operate well below the 4mA minimum current.

Figure 6 shows a complete 2-wire thermistor temperature transducer interface with a 4mA to 20mA output. Over a 0°C to 100°C range, accuracy is ±0.3°C and the circuit is current loop powered. No external supply is required. The LM134 current source absorbs the 40V input, preventing

the LTC1040 from seeing too high a supply potential. It does this by fixing the current well below the 4mA loop minimum. The LTC1040 (detailed data on this device appears in Box Section B, "Sampling Techniques and Components for Micropower Circuits") senses the YSI thermistor network output and forces this voltage across the output resistor to set total circuit current. Current is adjusted by varying the gate voltage on the 2N6657 FET. Note that the comparator output operates in pulse-width modulation mode, with the FET gate voltage filtered to DC by the 1M-1µF combination. An important LTC1040 feature is that very little current, on the order of nanoamperes, flows from the V^- supply. This allows the V^- supply to be connected to ground with negligible current error in the output sensing resistor. The differential input of the LTC1040 can sense the current through R_{OUT} because its common mode range includes the V^- supply. Trims shown are for 0°C and 100°C and are made by exposing the thermistor to those temperatures or by electrically simulating the conditions (see manufacturer's data sheet).
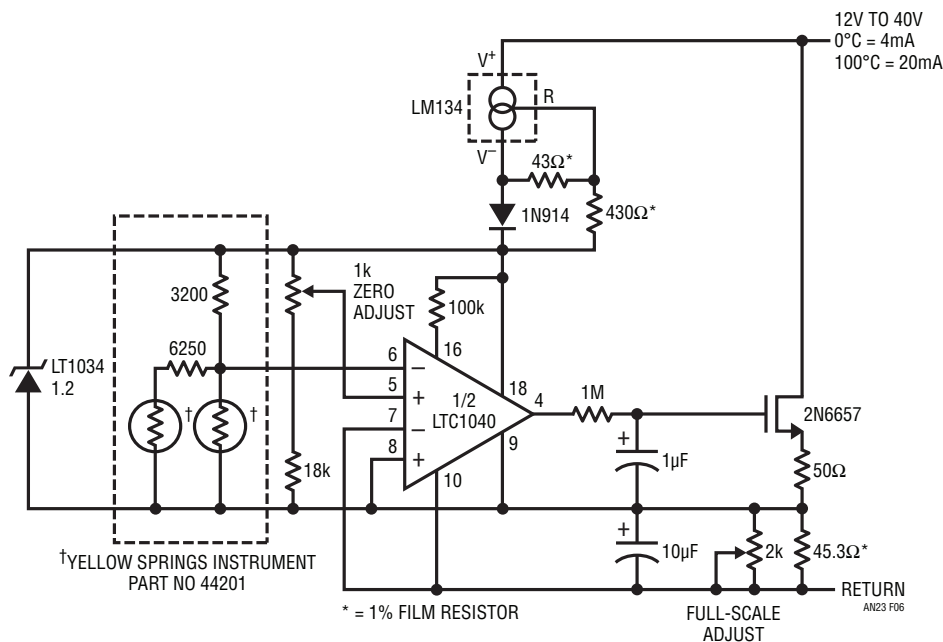

Figure 6. Thermistor-Based Current Loop Signal Conditioner

Microampere Drain Wall Thermostat

Figure 7 shows a battery-powered thermostat using the LTC1041 (see Box Section B for details on this device). Temperature is sensed using a thermistor connected in a bridge with a potentiometer to set the desired temperature.

The bridge is not driven from the battery but from Pin 7 on the LTC1041. Pin 7 is the pulsed power (V_{PP}) output and turns on only while the LTC1041 is sampling the inputs. With this pulse technique, average system power consumption is quite small. In this application the total system current is below 1μA! This is far less than the self discharge rate of the battery, meaning battery life is shelf life limited. A lithium battery will run this circuit for 10 to 20 years.

An external RC network sets the sampling frequency. When an internal sampling cycle is initiated, power is turned on to the comparators and to the V_{PP} output. The analog inputs are sampled and the resultant outputs are stored in CMOS latches. Power is then switched off although the outputs are maintained. The unclocked CMOS logic consumes almost no DC current. The sampling process takes approximately 80μs. During this 80μs interval, the LTC1041 draws typically 1.7mA of current at $V^+ = 6V$. Because the sample rate is low, average power is extremely small.

The low sample rate is adequate for a thermostat because of the low rate of change normally associated with temperature.

A power MOSFET in a diode bridge switches 26VAC to the heater control circuitry. The MOSFET is a voltage controlled device with no DC current required from the battery.

The voltage from DELTA (Pin 5) to GND (Pin 4) sets the dead-band. Dead-band is desirable to prevent excessive heater cycling. The dead-band equals two times DELTA and is independent of both V_{IN} (Pin 3) and SET POINT (Pin 2). This means that as the SET POINT is varied, the dead-band is fixed at two times DELTA. Conversely, as dead-band is varied, SET POINT does not move.

Freezer Alarm

Figure 8 shows a very simple configuration for a freezer alarm. Such circuits are used in industrial and home freezers as well as refrigerated trucks and rail cars. The LTC1042 is a sampled operation window comparator (for details on this device see Box Section B). The 10M-0.05μF combination sets a sample rate of 1Hz, and the bridge values program the internal window comparator for the outputs shown. For normal freezer operation, Pin 1 is high and Pin 6 is low. Overtemperature reverses this state and can trigger an alarm. Circuit current consumption is about 80μA.
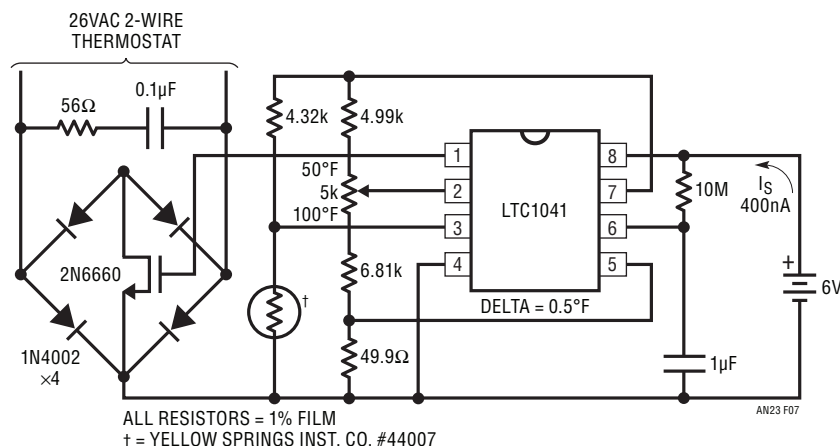

Figure 7. Wall Type Thermostat

12-Bit A/D Converter

Integrating A/D converters with low power consumption are available. Although capable of 12-bit measurements, they are quite slow, typically in the 100ms range. Higher speeds require a successive approximation (SAR) approach. No commercially produced 12-bit SAR converter features micropower (e.g., below 1mA) capability at the time of writing. Figure 9's design converts in 300µs, while consuming only 890µA.

† = YELLOW SPRINGS INST. CO. #44007
* = 1% METAL FILM RESISTOR

Figure 8. Freezer Alarm

= HP5082-2810
SOME SECOND SOURCE 7541A DEVICES
MAY NOT WORK IN THIS APPLICATION

* = 1% METAL FILM
SELECT AD7541A FOR REF IN > 10kΩ

Figure 9. Micropower 12-Bit, 300µs A/D

Conceptually, this design is a straightforward SAR type converter, although some special measures are needed to achieve low power operation. The SAR chip and the DAC are arranged in the standard fashion, with C1 closing a loop. Normally, CMOS DACs are not used for SAR applications because their output capacitance slows operation. In this case, the CMOS DAC's low power consumption is attractive and speed is traded away. This is not too great a penalty, because micropower comparator C1 is a good speed match for the DAC specified. A limitation with CMOS DACs is that their outputs must terminate into 0V. This mandates a current summing comparison, meaning the reference must be of opposite polarity to the input. Since most micropower systems run from single-sided positive rails, it is unrealistic to expect the user to supply the A/D with a negative input. To be readily usable, the converter should accept positive inputs and derive a negative reference internally. This issue is addressed by C2 and the LTC1044 plus-to-minus voltage converter, which form a negative reference.

C2, compensated as an op amp, servo controls the LTC1044 via the boost transistor. The LTC1044's negative output is fed back to C2's input, closing a regulation loop. Scaled current summing from the output and the LT1034 forces a 5.000V output. The Schottky diode prevents possible summing point negative overdrive during start-up. The choice of 5V for a reference maintains reasonable LSB overdrive for C1, but accounts for over half the circuit's current requirement. This limitation is set by the DAC's relatively low input impedance. Dropping the reference voltage would save significant power, but would also reduce LSB size below a millivolt. This would cause comparator offset and gain to become significant error sources.

Although the DAC has no negative supply, it can accept the negative reference because its thin film resistors are not intrinsic to the monolithic structure. Ground referred C1 cannot accept any negative voltages, however, and is Schottky clamped.

Performance includes a typical tempco of 30ppm/°C, 300µs conversion time, 890µA current consumption and an accuracy of ±2 LSBs. Trimming involves adjusting the 100k potentiometer for exactly –5V at V_{REF}. The DAC's internal feedback resistor serves as the input. Figure 10 shows operating waveforms. Trace A is the clock. Trace B is the convert command. The SAR is cleared on Trace B's falling edge and conversion commences on the rise. During conversion, C1's input (Trace C) sequentially converges towards zero. When conversion is complete, the status line (Trace D) drops low.

10-Bit, 100µA A/D Converter

Figure 11's A/D has less resolution than the previous circuit, but requires only 100µA. The design consists of a current source, an integrating capacitor, a comparator and some logic elements. When a pulse is applied to the convert command input (Trace A, Figure 12), the paralleled 74C906 sections reset the 0.075µF capacitor to zero (Trace B). Simultaneously, 74C14 inverter A goes low, biasing the 2N3809 current source on. During this interval the current source stabilizes, delivering its output to ground via the paralleled 74C906 sections. On the falling edge of the convert command pulse the 0.075µF capacitor begins to charge linearly. When the ramp voltage equals the input, C1 switches. Inverter A goes high, shutting off the current source. A small current is bled through the 10M diode connection to keep the ramp charging, but at a greatly reduced
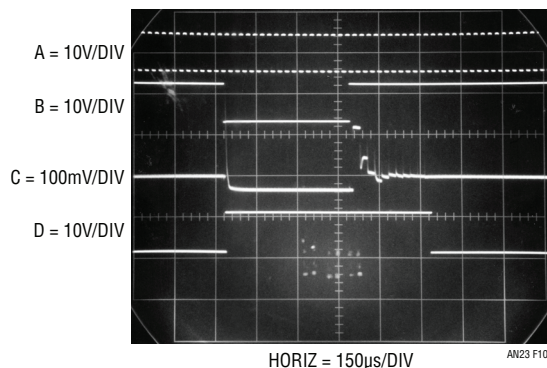

A = 10V/DIV

B = 10V/DIV

C = 100mV/DIV

D = 10V/DIV

HORIZ = 150µs/DIV

AN23 F10

Figure 10. Micropower SAR A/D Waveforms

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rate. This ensures overdrive for C1, but minimizes current source on-time, saving power. C1's output, a pulse (Trace C) width, is directly dependent on the value of Ex. This pulse width gates C2's clock output via the 74C00 configuration. The 74C00s also gate out the portion of C1's output due to the convert command pulse. Thus, the clock pulse bursts appearing at the output (Trace D) are proportional to Ex. For the arrangement shown, 1024 pulses appear for a 5V full-scale input. The current source scaling resistor and ramp capacitor specified provide good temperature compensation because of their opposing thermal coefficients. The circuit will typically hold ±1LSB accuracy over 0°C to 70°C with an additional ±1LSB due to the asynchronous relationship between the clock and the conversion sequence. If the conversion sequence is synchronized to the clock, the ±1LSB asynchronous limitation is removed, and total error falls to ±1LSB over 0°C to 70°C. The flop-flop shown in dashed lines permits such synchronization. Conversion

rate varies with input. At tenth-scale 150Hz is possible, decreasing to 20Hz at full-scale.

Power consumption of the A/D is extremely low, due to the CMOS logic elements and the LT1017 comparator. Quiescent (E_{IN} = 0V) current is 100µA at V_{SUPPLY} = 9V, decreasing to 80µA for V_{SUPPLY} = 7V. Because current source on-time varies with input, power consumption also varies. For E_{IN} = 5V, current consumption rises to 125µA for E_{SUPPLY} = 9V, and 105µA at E_{SUPPLY} = 7V. Additional power savings are possible by shutting off the current source during capacitor reset, but accuracy suffers due to current source settling time requirements. The 0.075µF capacitor's accumulated charge is thrown away at each reset. A smaller capacitor would help, but C1's bias currents would introduce significant error.

Turning off the current source after C1 switches saves significant power. Figure 13, taken at a 25mV input, shows
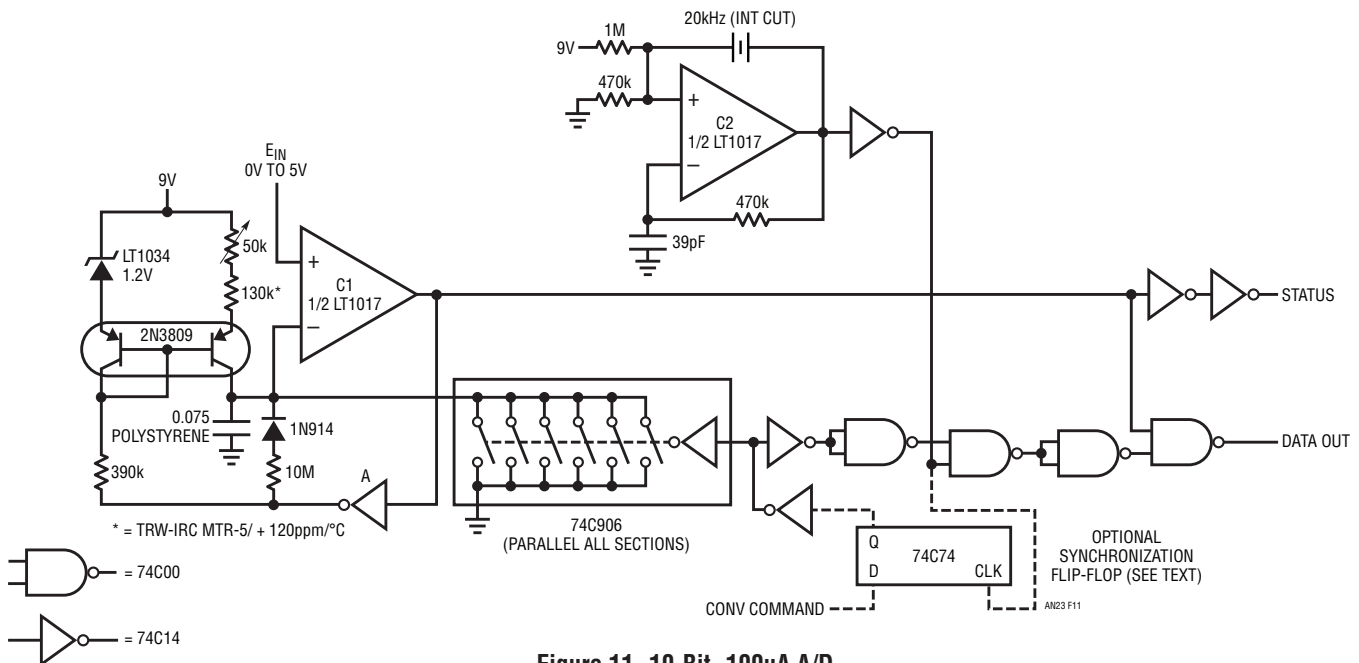
Figure 11. 10-Bit, 100µA A/D
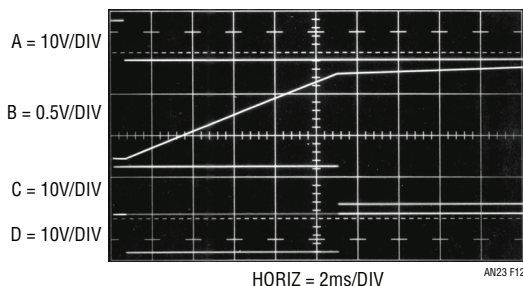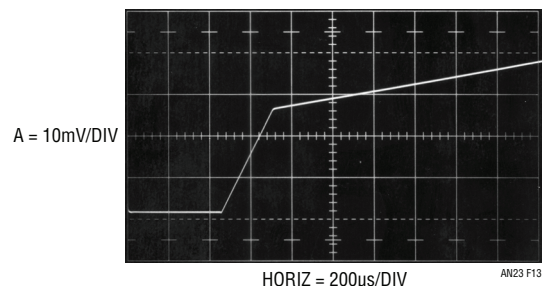

Figure 12. Waveforms for the 100µA A/D

Figure 13. Detail of the Switched Slope Capacitor Charging

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the ramp zero reset and the clean switching. When the current source switches off, the ramp slope decreases but continues to move upward, ensuring overdrive. The 10M diode pair provides the charge, but less than a microampere is lost.

20μs Sample-Hold

Figure 14 is a companion sample-hold for the SAR A/D. Acquisition time is 20μs, with low power operation (see Figure 14 table). This circuit takes full advantage of the programming pin on the LT1006 op amp to maximize speed-power performance. When the sample command (Trace A, Figure 15) is given, the CD4066 switches close. S1 and S2 allow A1's output (Trace B) to charge the capacitor (Trace C is capacitor current). Simultaneously S3 and S4 close, raising the op amp's internal bias network. This

puts both amplifiers into hyperdrive, boosting slew rate to speed acquisition time. A2 (Trace D) is seen to settle cleanly to 1mV in 20μs. When the sample command goes low, all switches go off, A2 follows the voltage stored on the capacitor, and supply current drops by a factor of five (see Figure 14 table). In normal operation, sample time is short compared to hold and current consumption is low. The 360k resistors set the circuit's hold mode quiescent current at the value noted in the table.

10kHz Voltage-to-Frequency Converter

Figure 16, another data converter, is a voltage-to-frequency converter. A 0V to 5V input produces a 0kHz to 10kHz output, with a linearity of 0.02%. Gain drift is 40ppm/°C. Maximum current consumption is only 145μA, far below currently available units.

ACQUISITION TIME	20μs
HOLD SETTLING TIME	10μs
S-H OFFSET	1mV
HOLD SUPPLY CURRENT	430μA
SAMPLE SUPPLY CURRENT	2.2mA
1kHz SAMPLE RATE CURRENT	875μA
DROOP RATE	1mV/ms
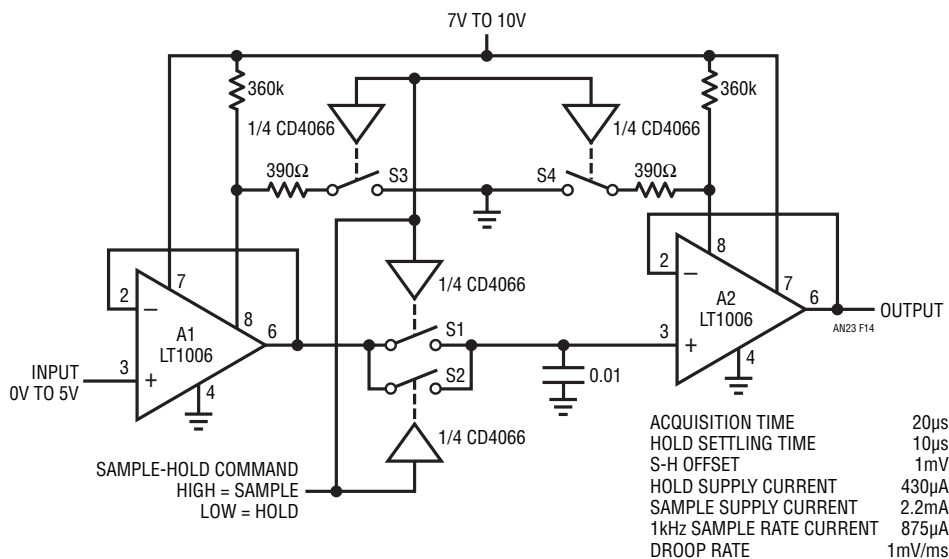
Figure 14. Micropower Sample-Hold

HORIZ = 10μs/DIV
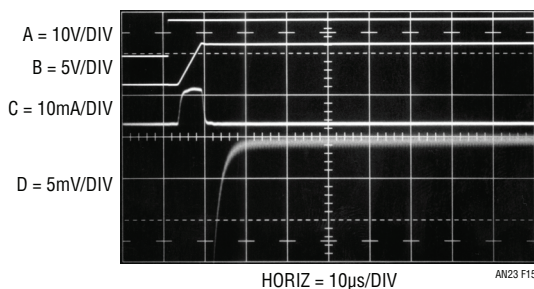
Figure 15. Figure 14's Waveforms

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The evolution of this circuit is described in Box Section A, "Some Guidelines for Micropower Design and an Example". To understand circuit operation, assume C1's positive input is slightly below its negative input (C2's output is low). The input voltage causes a positive going ramp at C1's positive input (Trace A, Figure 17). C1's output is low, biasing the CMOS inverter outputs high. This allows current to flow from Q1's emitter, through the inverter supply pin to the 0.001µF capacitor. The 10µF capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 provides a path to ground. The voltage to which the 0.001µF unit charges is a function of Q1's emitter potential and Q6's drop. When the ramp at C1's positive input goes high enough, C1's output goes high (Trace B) and the inverters switch low (Trace C). The Schottky clamp prevents CMOS inverter input overdrive. This action pulls current from C1's positive input capacitor via the Q5-0.001µF route (Trace D). This current removal resets C1's positive input ramp to a potential slightly below ground, forcing C1's output to go low. The 50pF capacitor connected to the circuit output furnishes AC positive feedback, ensuring that C1's output remains positive long enough for a complete discharge of the 0.001µF capacitor. The Schottky diode prevents C1's input from being driven
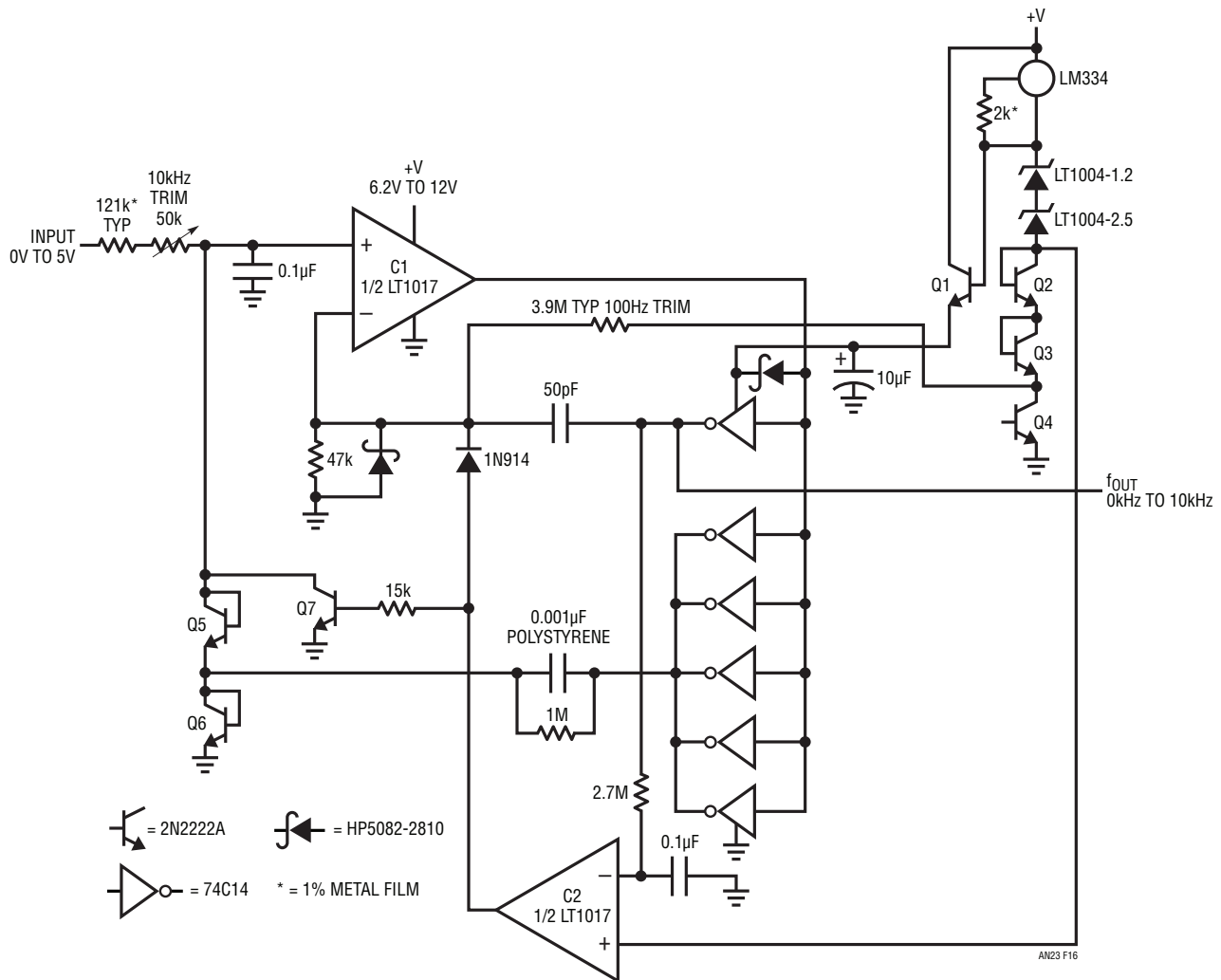
Figure 16. Micropower 10kHz V→F Converter

A = 50mV/DIV

B = 5V/DIV

C = 5V/DIV

D = 10mA/DIV

HORIZ = 20µs/DIV   AN23 F17
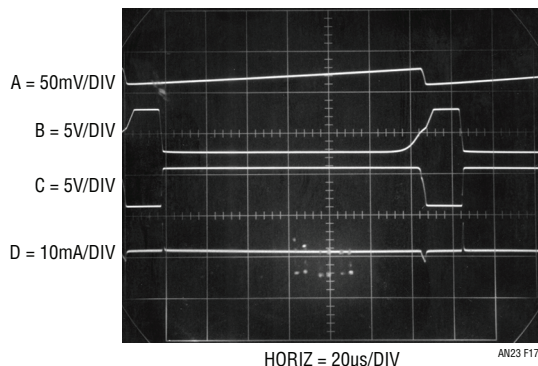
Figure 17. Figure 16's Waveforms

outside its negative common mode limit. When the 50pF unit's feedback decays, C1 again switches low and the entire cycle repeats. The oscillation frequency depends directly on the input voltage derived current.

Q1's emitter voltage must be carefully controlled to get low drift. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE}. The two LT1004s are the actual voltage reference and the LM334 current source provides 35µA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by utilizing the LM334's 0.3%/°C tempco to slightly temperature modulate the voltage drop in the Q2-Q4 trio. This correction's sign and magnitude directly oppose that of the −120ppm/°C 0.001µF polystyrene capacitor, aiding overall circuit stability.

The Q1 emitter-follower delivers charge to the 0.001µF capacitor efficiently. Both base and collector current end up in the capacitor. The paralleled CMOS inverters provide low loss SPDT reference switching without significant drive losses. The 0.001µF capacitor, as small as accuracy permits, draws only small transient currents during its charge and discharge cycles. The 50pF-47k positive feedback combination draws insignificantly small switching currents. Figure 18, a plot of supply current vs operating frequency, reflects the low power design. At zero frequency, the LT1017's quiescent current and the 35µA reference stack bias accounts for all current drain. There are no other paths for loss. As frequency scales up, the charge-discharge cycle of the 0.001µF capacitor introduces the 7µA/kHz increase shown. A smaller value capacitor would cut power, but the effects of stray capacitance, charge imbalance in the 74C14, and LT1017 bias currents would introduce accuracy errors.

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes high. C2, detecting this via the inverters and the 2.7M-0.1µF lag, also goes high. This lifts C1's negative input and grounds the positive input with Q7, initiating normal circuit action.

Because the charge pump is directly coupled to C1's output, response is fast. Figure 19 shows the output (Trace B) settling within one cycle for a fast input step (Trace A).
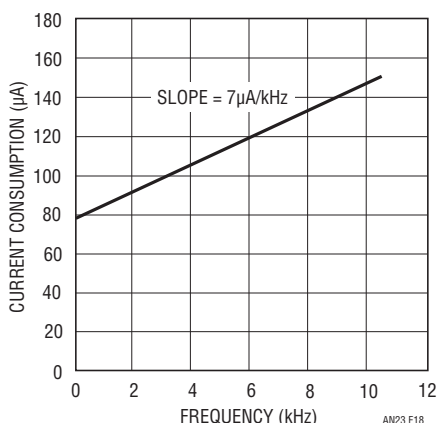

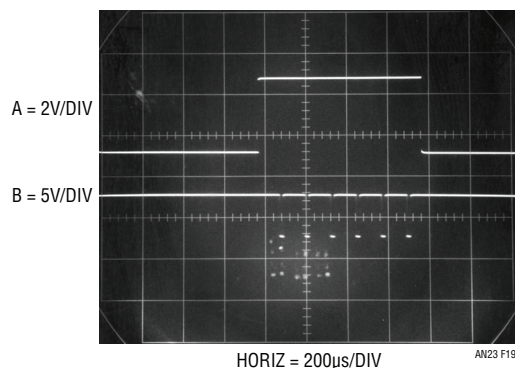**Figure 18. Current Consumption vs Frequency for Figure 16**

A = 2V/DIV

B = 5V/DIV

HORIZ = 200µs/DIV   AN23 F19

Figure 19. Figure 16's Step Response

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To calibrate this circuit, apply 50mV and select the value at C1's input for a 100Hz output. Then, apply 5V and trim the input potentiometer for a 10kHz output.

An evolutionary history of this design appears in Box Section A, "Some Guidelines for Micropower Design and an Example".

A nice day at the San Francisco Zoo with Celia Moreno M.D., instrumental in arriving at the final configuration, is happily acknowledged.

1MHz Voltage-to-Frequency Converter

Figure 20 is also a V→F converter, but runs at 1MHz full-scale. Quiescent current is 90µA, ascending linearly to 360µA at 1MHz output. Obtaining higher operating frequency requires trade-offs in power consumption and step response performance. Linearity is 0.02% over a 100Hz to 1MHz range, drift about 50ppm/°C and step response inside 350ms to full-scale.

This circuit has similarities to Figure 16, although operation is somewhat different. An input causes A1 to swing towards ground, biasing Q8. Q8's collector ramps (Trace A, Figure 21) as it charges the 3pF capacitor plus stray capacitance associated with Q7 and the 74C14 Schmitt input connected to the node. When the ramp hits the Schmitt's threshold its output (Trace B) goes low, turning on diode connected Q7. Q7's path discharges the node capacitances,
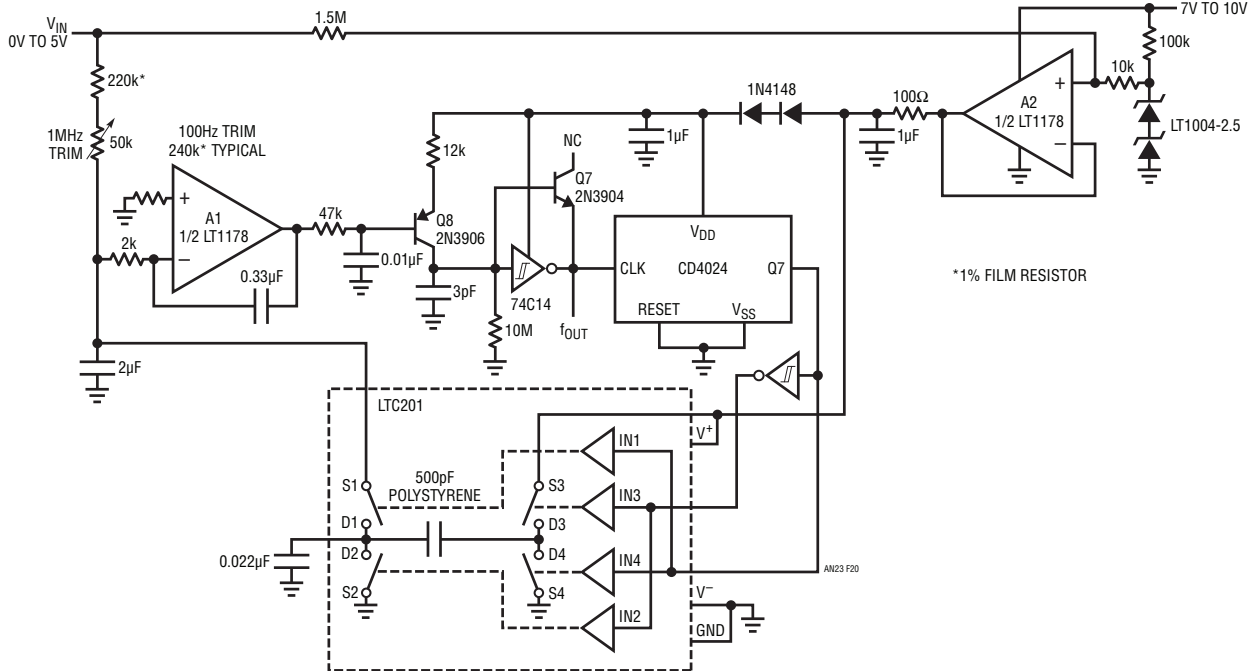
Figure 20. Micropower 1MHz V→F Converter

A AND B HORIZ = 500ns/DIV
C AND D HORIZ = 100µs/DIV
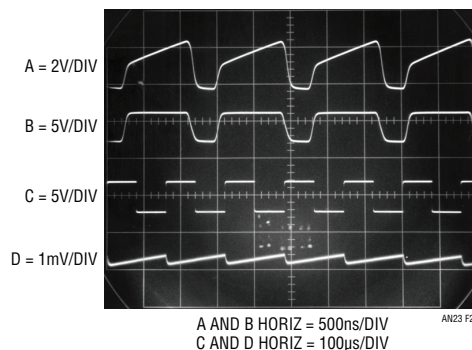
Figure 21. Figure 20's Waveforms

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forcing ramp reset. The 74C14 returns high, and oscillation commences. The 74C14 also drives the CD4024 divider, and serves as the circuit's output. The divider's ÷ 128 output (Trace C) controls a reference charge pump arrangement similar to Figure 16's. A2 furnishes a buffered reference. The 500pF capacitor is alternately charged and discharged by the LTC201 switch sections. The charge increments pulled through S1 continually force A1's 2µF capacitor to zero (Trace D), balancing the input derived current. The 0.022µF capacitor at the D1-D2 LTC201 node eliminates excessive differentiated response, preventing spurious modes. This action closes a loop around A1, and it servo controls the Q7, Q8, 74C14 oscillator to run at whatever frequency is required to maintain its negative input at zero. This servo behavior eliminates oscillator drift and nonlinearity as error terms, allowing the performance specifications noted. The 0.33µF capacitor at A1 stabilizes the loop. This capacitor accounts for the circuit's 350ms settling time.

The resistor from the input to A2 sums a small input related voltage to the reference, improving linearity. The 10M resistor at Q8's collector deliberately introduces leakage to ground, dominating all node leakages. This ensures low frequency operation by forcing Q8 to source current to maintain oscillations.

The circuit's current drain, while low, is larger than Figure 16's. The increase is primarily due to high frequency oscillator and divider operation. The series diodes in the oscillator-divider supply line lower supply voltage, decreasing current consumption. Oscillator current is also heavily influenced by the capacitance and swing at Q8's collector. The swing is fixed by the 74C14 thresholds. Capacitance has been chosen at the lowest possible value commensurate with desired low frequency operation.

To trim this circuit, put in 500µV and select the indicated value at A1's positive input for 100Hz out. Then, put in 5V and trim the 50k potentiometer for 1MHz out. Repeat this procedure until both points are fixed.

Switching Regulator

No discussion of micropower circuitry is complete without mention of switching regulators. Often, battery voltages must be efficiently converted to different potentials to meet circuit requirements. Figure 22 shows a micropower buck type switching regulator with a quiescent drain of 70µA and 20mA output current capability. When the output

voltage drops (Trace A, Figure 23) C1's negative input also falls, causing its output (Trace B) to rise. This turns on the paralleled 74C907 open-source buffers, and their outputs (Trace C) go high. Current ramps up through the inductor, maintaining the regulator output. When output voltage rises a small amount, C1's output returns low and the cycle repeats. This action maintains regulator output despite line and load changes. The LT1004 serves as a reference and the 5pF capacitor ensures clean switching at C1. The 2810 Schottky diode prevents negative overdrives due to the 5pF unit's differentiated response; the 1N5817 is a catch diode, preventing excessive inductor caused negative voltages.

This circuit's low quiescent drain is due to the LT1017's small operating currents and the 74C907's low input drive requirements. Circuit resistor values are kept high to save current. C2 shuts down the regulator when output current exceeds 50mA. It does this by comparing the potential across the 0.2Ω shunt to a resistively divided portion of the LT1004 reference. Excessive current drain trips C2 high, forcing C1's negative input high. This removes drive from the 74C907 buffers, shutting down the regulator.

Utilization of a CMOS buffer as a pass switch for a switching regulator is somewhat unusual, but performance is quite good. Figure 24 plots efficiency vs output current at two input voltages. Efficiencies above 90% are possible, with output current to 20mA depending on input.

Post Regulated Micropower Switching Regulator

Figure 25 is another buck type switching regulator, but features a low loss linear post regulator, quiescent current of 40µA and 50mA output capacity. The LT1020 linear regulator provides lower noise than a straight switching approach. Additionally, it offers internal current limiting and contains an auxiliary comparator which is used to form the switching regulator.

The switching loop is similar to Figure 22's circuit. A drop at the switching regulator's output (Pin 3 of the LT1020 regulator; Trace A, Figure 26) causes the LT1020's comparator to go high. The 74C04 inverter chain switches, biasing the P-channel MOSFET switch's grid (Trace B). The MOSFET comes on (Trace C), delivering current to the inductor (Trace D). When the voltage at the inductor-220µF junction goes high enough (Trace A), the comparator switches high, turning off MOSFET current flow. This switching

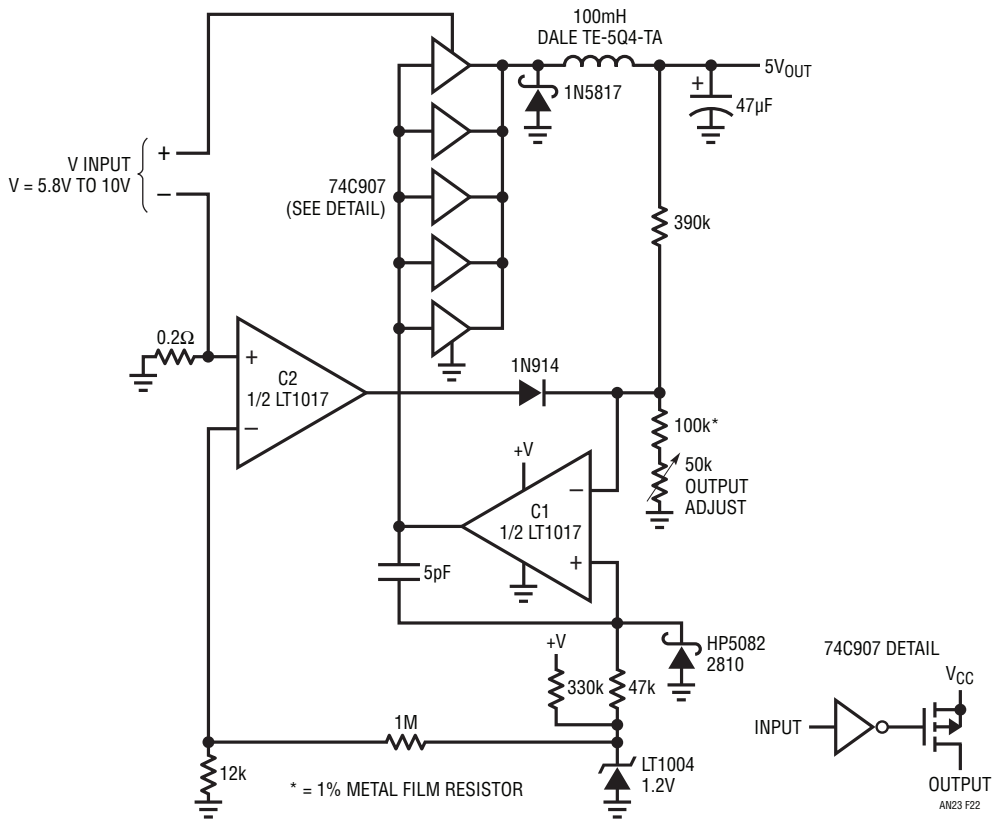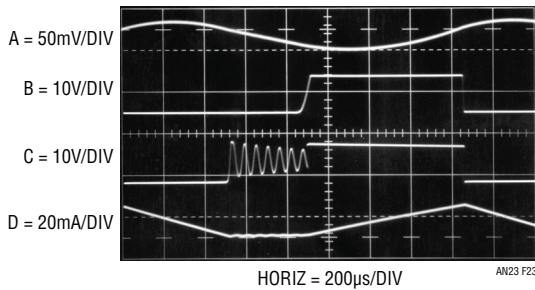**Figure 22. Micropower Switching Regulator**
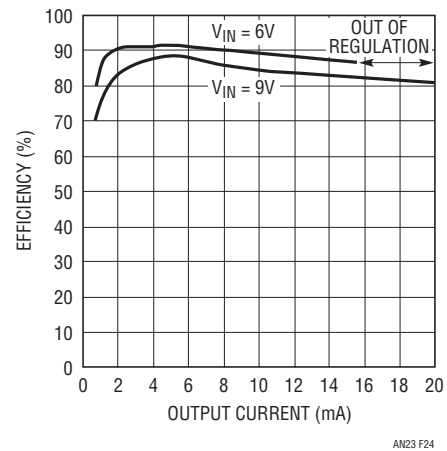

Figure 23. Figure 22's Waveforms

Figure 24. Figure 22's Efficiency vs Output Current

loop regulates the LT1020's input pin at a value set by the resistor divider in the comparator's negative input and the LT1020's 2.5V reference. The 680pF capacitor stabilizes the loop and the 1N5817 is the catch diode. The 270pF capacitor aids comparator switching and the 2810 diode prevents negative overdrives.

The low dropout LT1020 linear regulator smooths the switched output. Output voltage is set with the feedback pin associated divider. A potential problem with this circuit is start-up. The switching loop supplies the LT1020's input but relies on the LT1020's internal comparator to function. Because of this, the circuit needs a start-up mechanism. The 74C04 inverters serve this function. When power is applied, the LT1020 sees no input, but the inverters do. The 220k path lifts the first inverter high, causing the chain to switch, biasing the MOSFET and starting the circuit. The inverter's rail-to-rail swing also provides ideal MOSFET grid drive.

Even though this circuit's 40µA quiescent current is lower than Figure 22's, it can source more current. The extremely small quiescent current is due to the low LT1020 drain and the MOS elements. Figure 27 plots efficiency vs output current for two LT1020 input-output differential voltages. Efficiency exceeding 80% is possible, with outputs to 50mA available.

Figures 28 and 29 show two other LT1020 micropower regulator-based circuits. In many processor-based systems it is desirable to monitor or control the power-down sequence. Figure 28 produces a logical "1" output when the regulator output begins to drop out (e.g., battery is low). Here, the regulator is programmed for a 5V output with the 1M feedback resistors. The 0.001µF capacitor provides frequency compensation. The LT1020's internal comparator senses the difference between the chip's 2.5V reference and a small portion of the IC's pass transistor current (supplied at Pin 13). At the edge of dropout, the
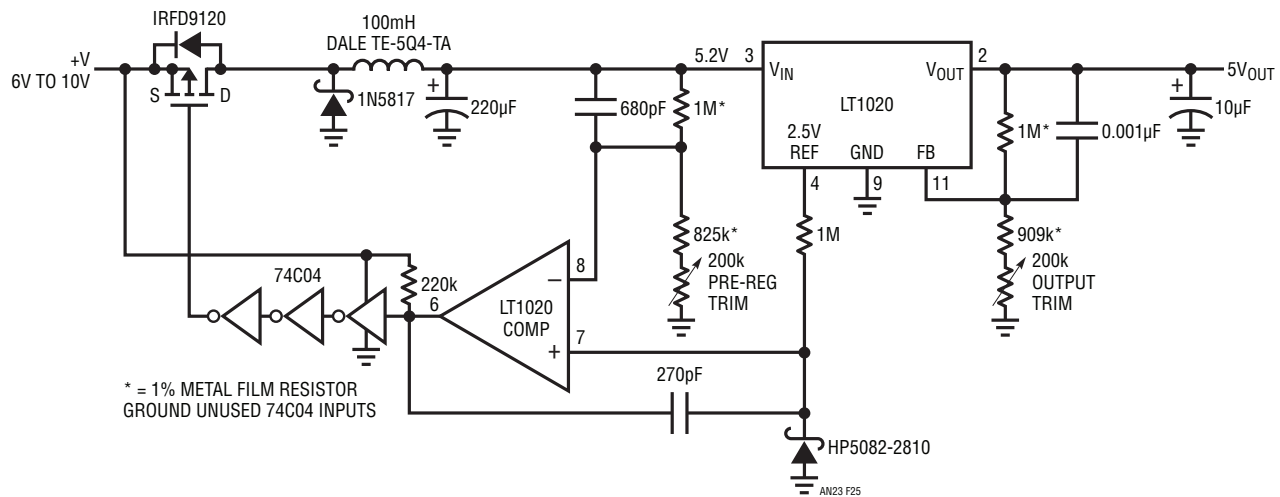

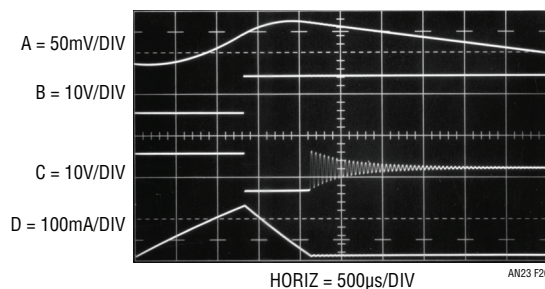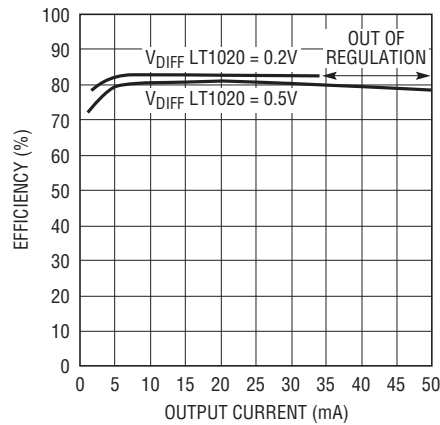**Figure 25. Micropower Post-Regulated Switching Regulator**

HORIZ = 500µs/DIV

Figure 26. Figure 25's Waveforms

Figure 27. Figure 25's Efficiency vs Output Current
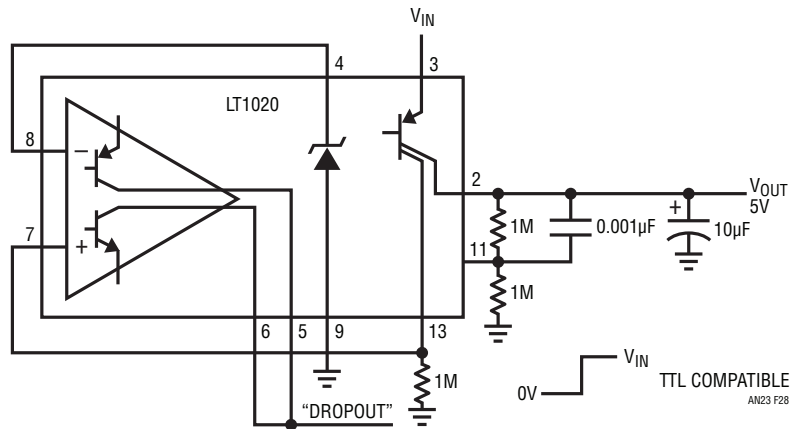

Figure 28. Regulator with Logic Output on Dropout

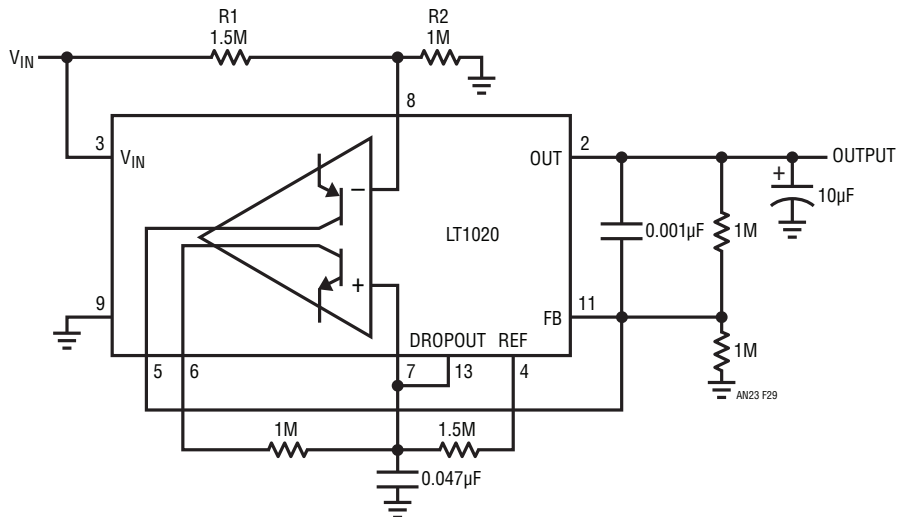Figure 29. Regulator with Output Shutdown on Dropout

LT1020's pass transistor goes towards saturation, raising Pin 13's voltage. This trips the comparator, and its output goes high. This signal can be used to alert a processor that power is about to go down.

Figure 29 is similar, except that power is turned completely off when dropout begins to occur, preventing unregulated supply conditions. The comparator feedback is arranged for a hysteresis type response. Although the output turns off at dropout, it will not turn on until:

$$\text{Turn On} = \frac{V_{IN} \cdot R2}{R1 + R2} = 2.5V$$

This prevents battery "creep back" from causing oscillation.

Figure 30 shows a simple way to shut the LT1020 down. In this state it draws only 40μA. The logic signal forces the feedback pin above the internal 2.5V reference, and all drive is removed from the output transistor. Figure 31 shows a low loss way to implement a "glitchless" memory battery backup. During line-powered operation, the right LT1020 does the work. The feedback string is arranged so that the left LT1020 does not conduct under line-powered conditions. When the line goes down, the associated LT1020 begins to go off, allowing the battery-driven regulator to turn on, maintaining the load.
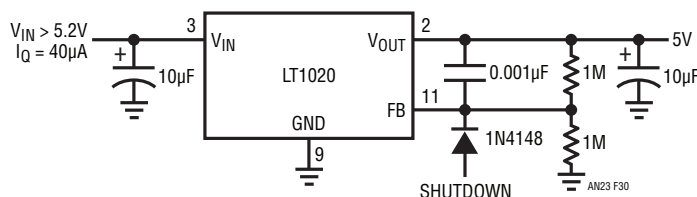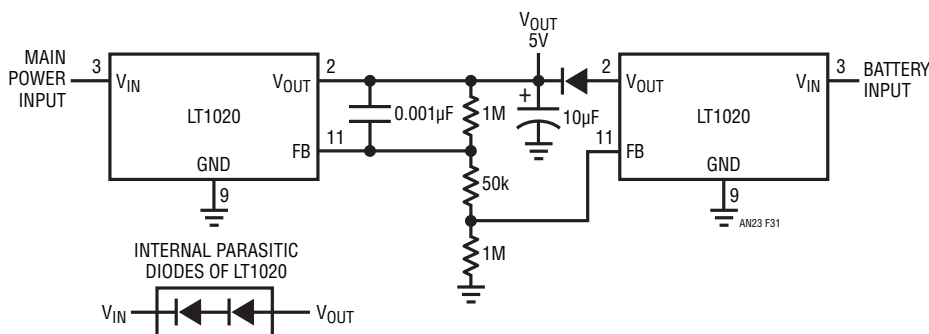

Figure 30. LT1020 Shutdown

Figure 31. Battery Backup Regulator

BOX SECTION A

Some Guidelines for Micropower Design and an Example

As with all engineering, micropower circuitry requires attention to detail, awareness of trade-offs and an opportunistic bent towards achieving the design goal.

The most obvious way to save power is to choose components which require little energy. Additional savings require more effort.

Circuits should be examined in terms of current flow. Consider such flow in all DC and AC paths. For example, do DC base currents go where they can do some useful work, or are they thrown away? Try to keep AC signal swings down, particularly if capacitors (parasitic or intended) must be continually charged and discharged.

Examine the circuit for areas where power strobing may be allowable.

Consider quiescent vs dynamic power requirements of components to avoid unpleasant surprises. Data sheets usually specify quiescent power because the manufacturer doesn't know what the user's circuit conditions are. For example, everyone "knows" that "MOS devices draw no current." Unfortunately, Mother Nature dictates that as frequency and signal swings go up, the capacitances associated with MOS devices begin to require more power. It is often a mistake to automatically associate low power operation with a process technology. While it's likely that CMOS will provide lower power operation for a given function than 12AX7s, a bipolar approach may be even better. Consider individual situations on the basis of their specific requirements before committing to a technology. Very often, circuits require several technologies (e.g., CMOS, bipolar and discrete) for best results.

Usually, achieving low power operation requires performance trade-offs. Minimizing signal swings and current saves power, but moves circuit operation closer to the noise floor. Offsets, drift, bias currents and noise become increasingly significant error factors as signal amplitudes are constricted to save power. This is a fundamental trade-off and must be carefully considered. Circuits employing power strobing can sometimes get around this problem by utilizing low duty cycles. Text Figure 3 uses this technique to achieve dramatic power savings in a circuit with an on-state drain approaching 20mA (see also Box Section B, "Sampling Techniques and Components for Micropower Circuits").

Text Figure 16, a voltage-to-frequency converter, furnishes an example of the evolution of a low power design. Design goals included a 10kHz maximum output, fast step response, linearity inside 0.05% and a maximum supply current of 150µA. Other specifications appear in the text.

Figure A1 shows an early version of this circuit. Operation is similar to the text described for Figure 16, but a brief description follows: When the input current-derived ramp at C1's negative input crosses zero, C1's output drops low, pulling charge through C1. This forces the negative input below zero. C2 provides positive feedback, allowing a complete discharge for C1. When C2 decays,

C1A's output goes high, clamping at the level set by D1, D2 and V_{REF}. C1 receives charge and recycling occurs when C1A's negative input again arrives at zero. The frequency of this action is related to the input voltage. Diodes D3 and D4 provide steering, and are temperature compensated by D1 and D2. C1A's sink saturation voltage is uncompensated, but small. C1B is a start-up loop.

Although the LT1017 and LT1034 have low operating currents, this circuit pulls almost 400µA. The AC current paths include C1's charge-discharge cycle, and C2's branch. The DC path through D2 and V_{REF} is particularly costly. C1's charging must occur quickly enough for 10kHz operation, meaning the clamp seen by C1A's output must have low impedance at this frequency. C3 helps, but significant current still must come from somewhere to keep impedance low. C1A's current-limited output cannot do the job unaided, and the resistor from the supply is required. Even if C1A could supply the necessary current, V_{REF}'s settling time would be an issue. Dropping C1's value will reduce impedance requirements proportionally, and would seem to solve the problem. Unfortunately, such reduction magnifies the effects of stray capacitance at the D3-D4 junction. It also mandates increasing R_{IN}'s value to keep scale factor constant. This lowers operating currents at C1A's negative input, making bias current and offset more significant error sources.

Figure A2 shows an initial attempt at dealing with these issues. This scheme is similar to Figure A1, except that Q1 and Q2 appear. V_{REF} receives switched bias via Q1, instead of being on all the time. Q2 provides the sink path for C1. These transistors invert C1A's output, so its input pin assignments are exchanged. R1 provides a light current from the supply, improving reference settling time. This arrangement decreases supply current to about 300µA, a significant improvement. Several problems do exist, however. Q1's switched operation is really effective only at higher frequencies. In the lower ranges, C1A's output is low most of the time, biasing Q1 on and wasting power. Additionally, when C1A's output switches, Q1 and Q2 simultaneously conduct during the transition, effectively shunting R2 across the supply. Finally, the base currents of both transistors flow to ground and are lost. The basic temperature compensation is as before, except that Q2's saturation term replaces the comparator's.

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Figure A3 is better. Q1 is gone, Q2 remains but Q3, Q4 and Q5 have been added. V_{REF} and its associated diodes are biased from R1. Q3, an emitter-follower, is used to source current to C1. Q4 temperature compensates Q3's V_{BE}, and Q5 switches Q3.

This method has some distinct advantages. The V_{REF} string can operate at greatly reduced current because of Q3's current gain. Also, Figure A2's simultaneous conduction problem is largely alleviated because Q5 and Q2 are switched at the same voltage threshold out of C1A. Q3's base and emitter currents are delivered to C1. Q5's currents are wasted, although they are much smaller than Q3's. Q2's small base current is also lost. The values for C2 and R3 have been changed. The time constant is the same, but some current reduction occurs due to R3's increase.

If C1 cannot be reduced for performance reasons, then its AC currents cannot be avoided. This leaves only the aforementioned Q5 and Q2 currents as significant wasted terms, along with R3's now smaller loss. Current drain for this circuit is about 200µA maximum. Text Figure 16's circuit is very similar, but eliminates Q5 and Q2's losses to achieve maximum operating current below 150µA with quiescent current under 80µA. Some other refinements are included, but the circuit is the final iteration of the three versions shown here. A complete description of Figure 16 appears in the text.
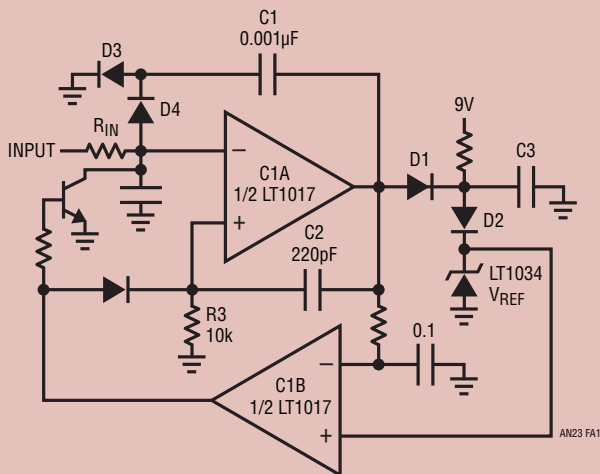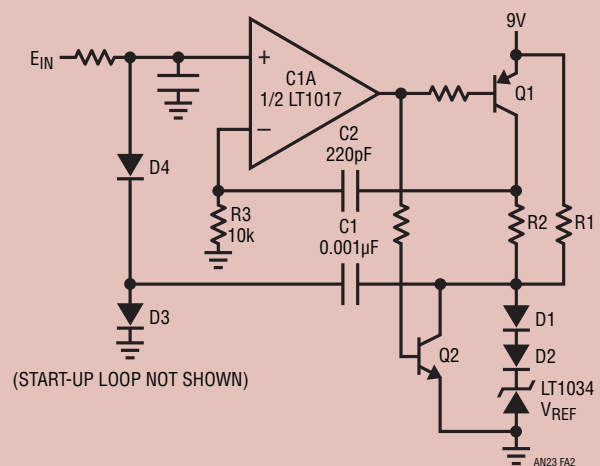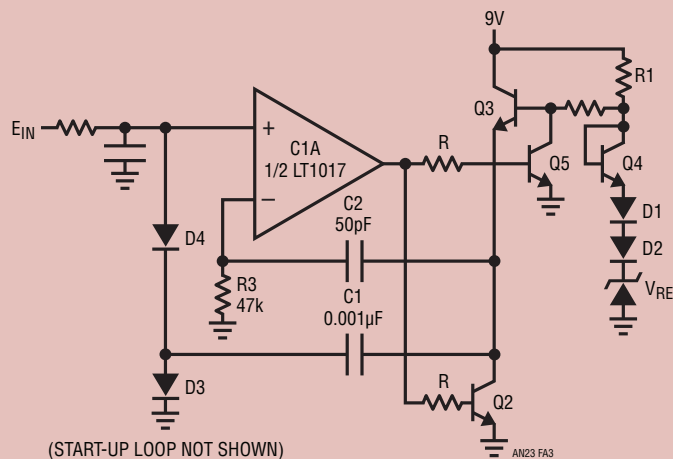

Figure A1

Figure A2

Figure A3

BOX SECTION B

Sampling Techniques and Components for Micropower Circuits

The best way to get low power circuit characteristics is to turn off the power. While there are some obvious problems with this approach, it does point a way towards minimizing power consumption. In many applications continuous circuit power is not necessary. If bandwidth requirements are low, sampling techniques offer a simple way to save power. With low duty cycles, instantaneous current can be relatively high while average drain remains low. When considering a sampled approach some issues should be examined. The required circuit bandwidth dictates the minimum sampling frequency in accordance with Nyquist criteria. The sampling interval's duration is determined by circuit settling time to the required accuracy. This settling time should be considered for all circuit elements (transducers, ICs and discrete components) singularly and together. Additionally, effects of sampled operation on component life and operating characteristics should be examined. This is particularly the case for transducers, which may be designed and tested under DC operating conditions.

Once these issues have been addressed, components can be selected. The LTC1040, LTC1041 and LTC1042 have been specifically designed for sampled operation. Figure B1 details the LTC1040, dual micropower comparator. Its programmable internal oscillator sets the sampling rate with a sampling interval lasting 80µs. The V_{PP} output supplies power during the sampling interval, allowing drive for external circuity or transducers. Note that the input common mode range includes both rails. Figure B2 plots supply current vs sampling frequency.

A related device is similar, but dedicated to "bang-bang" on-off type servo loops. The LTC1041 appears in Figure B3. Servo SET POINT and DELTA are controllable from the inputs. The associated diagram (Figure B4) graphically defines operation. Operating current is similar to the LTC1040.

A final device, the LTC1042, is also similar but is set up as a window comparator. Its internals appear in Figure B5 and the graphic operation description is shown in Figure B6. Operating current, input range and sampling characteristics are similar to the LTC1040 and LTC1041.
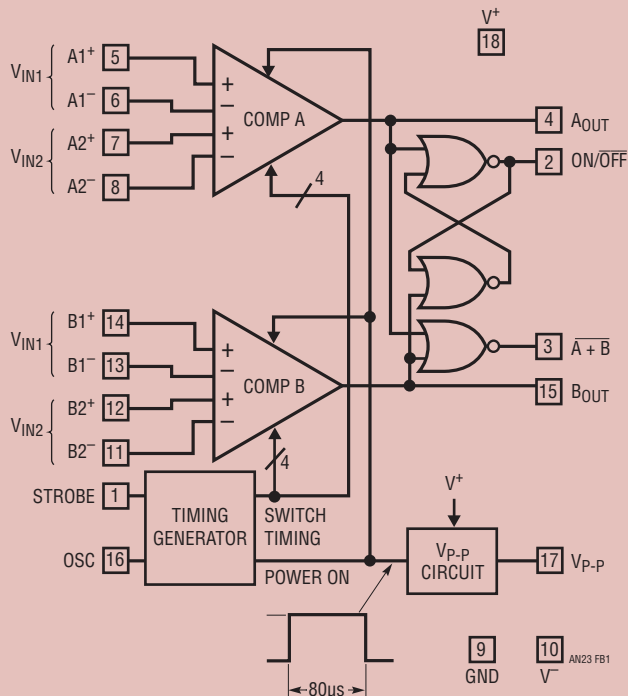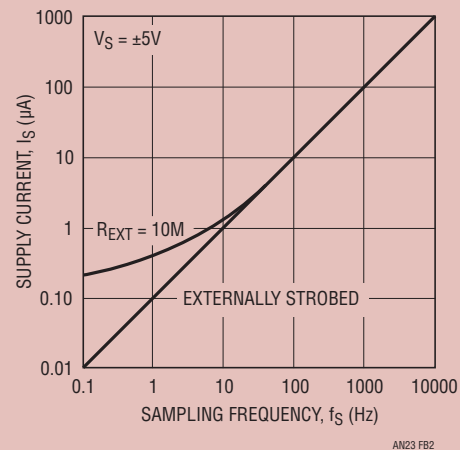

Figure B2. LTC1040 Power Consumption vs Sampling Frequency

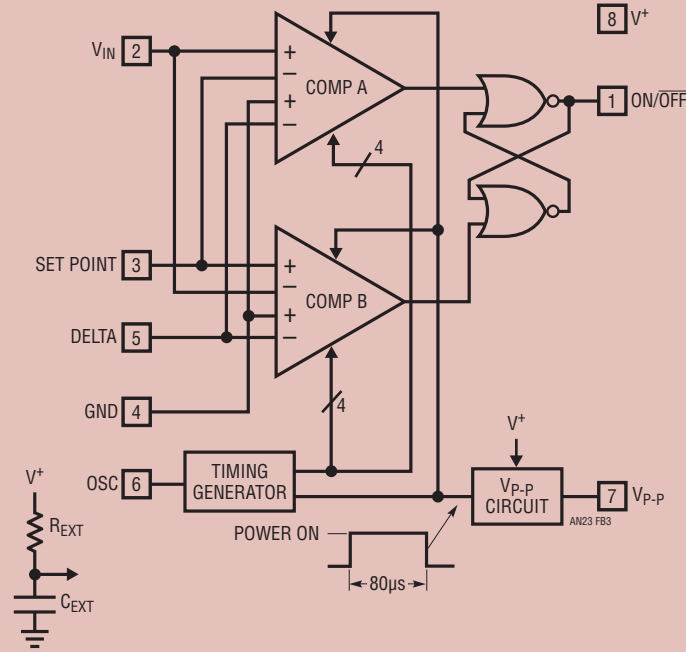**Figure B1. LTC1040 Internal Details**

Figure B3. LTC1041 Details

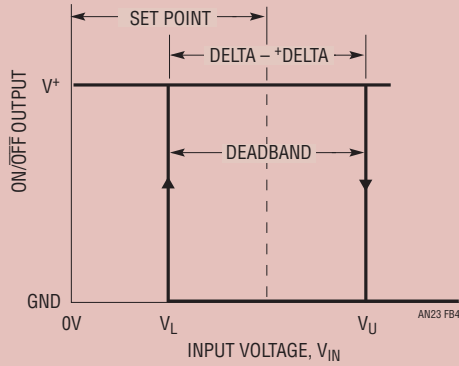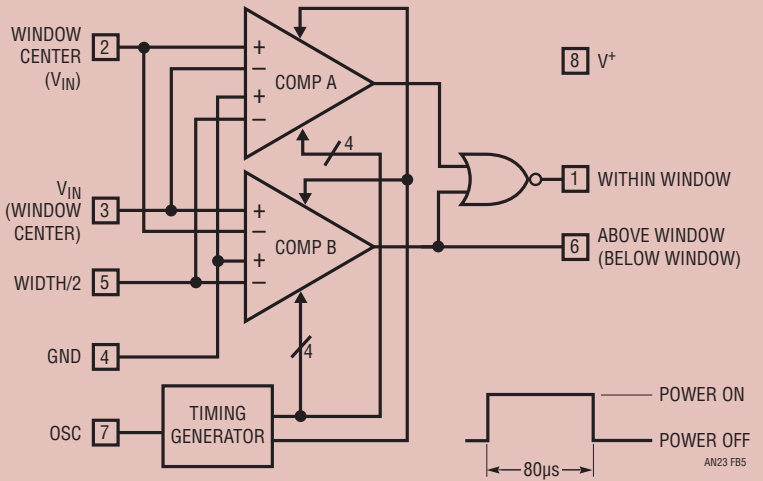**Figure B4. LTC1041 Operation Diagram**

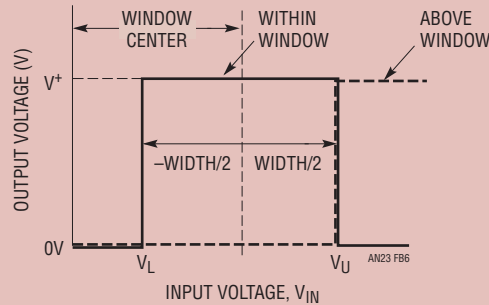**Figure B5. LTC1042 "Window" Comparator Details**

Figure B6. LTC1042 Operating Diagram

BOX SECTION C

Parasitic Effects of Test Equipment on Micropower Circuits

The energy absorbed by test equipment connections to micropower circuits can be significant. Under normal circumstances test equipment and probes have negligible power drain, but microampere level operating currents mandate care. Test instrumentation should be regarded as an integral part of the circuit. DC and AC loading and parasitic effects must be kept in mind to avoid unpleasant surprises. Such instrument connection errors can make the circuit under test look unfairly bad or good.

The DC resistance of oscilloscope probes varies from hundreds of ohms (1x types) to 10M (10x), with some 10x types as low as 1M. Contrary to some expectations, FET probes do not have high input resistance—some types are as low as 100k, although most are about 10M. The DC loading of a 10x 1M probe could introduce as much as 9µA of loss, almost 10% of Figure 11's total! The AC loading of a 10pF probe looking at Figure 11's 20kHz clock will cause apparent circuit consumption of 5µA, a significant loss in a low power circuit. 1x type probes present about 50pF of loading, with 1M DC resistance when connected to the 'scope. This kind of probe loading can cause large errors in micropower circuits, while virtually disabling some. Such a probe, introduced at Pin 6 of text Figure 7, would stop the circuit's oscillator. If placed across the supply of the same circuit it would consume 15 times the circuit's operating current. Similarly, the probe's 50pF input capacitance connected to Figure 20 (Q8's collector) results in a 25% apparent increase in circuit current at 1MHz output.

Probe AC and DC loading are not the only effects. Some DVMs produce "charge spitting" at their inputs. Such parasitic charge, introduced into high impedance nodes, can cause substantial errors. It's also worth remembering that DVM DC loading may change with range. Lower ranges may have very high input impedance, but higher ranges are typically 10MΩ. A 10MΩ DVM reading Figure 7's supply consumes 1 1/2 times the circuit current.

Figure C1 shows a way test equipment can make the circuit look too good, instead of too bad. If the pulse generator is adjusted more than a diode drop above the regulator's output, the bypass capacitor peak detects the charge delivered through the IC's internal diode. The regulator can't sink current, and with its output forced high it won't source anything. Under these conditions, the circuit functions while the current meter reads zero... a very low power circuit indeed!*

*Practically speaking, most regulators and power supplies can sink small amounts of current. Because of this, the current meter may actually read negative.

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Figure C2 shows a very simple, but useful, circuit which greatly aids probe loading problems in micropower circuits. The LT1022 high speed FET op amp drives an LT1010 buffer. The LT1010's output allows DVM cable and probe driving and also biases the circuit's input shield. This bootstraps the input capacitance, reducing its effect. DC and AC errors of this circuit are low enough for almost all work, with enough bandwidth for just about any low power circuit. Built into a small enclosure with its own power supply, it can be used ahead of a 'scope or DVM with good results. Pertinent specifications appear in the diagram.
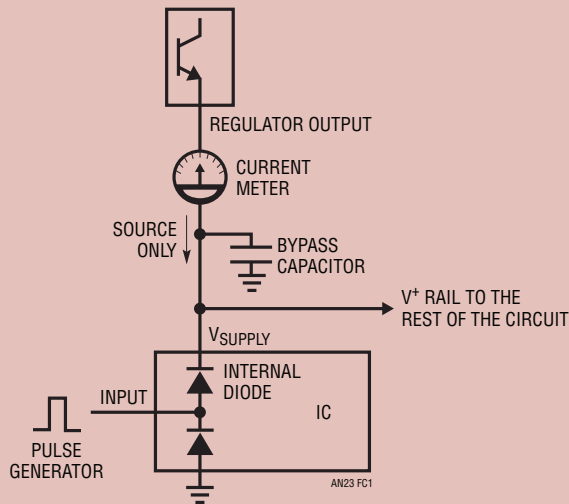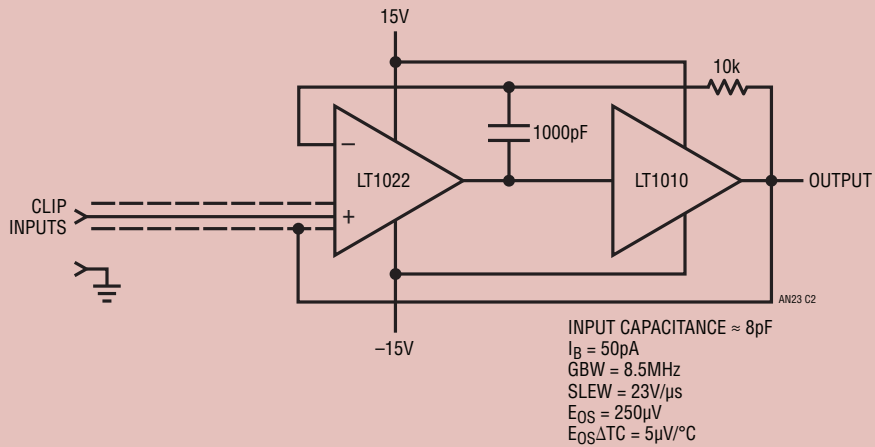
Figure C1

Figure C2

INPUT CAPACITANCE ≈ 8pF
I_B = 50pA
GBW = 8.5MHz
SLEW = 23V/µs
E_{OS} = 250µV
$E_{OS}\Delta TC$ = 5µV/°C

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