A Simple Method to Accurately Predict PLL Reference Spur Levels Due to Leakage Current

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Presented is a simple model that can be used to accurately predict the level of reference spurs due to charge pump and/or op amp leakage current in a PLL system. Knowing how to predict these levels helps pick loop parameters wisely during the early stages of a PLL system design.

Quick Review of PLLs

The phase locked loop (PLL) is a negative feedback system that locks the phase and frequency of a higher frequency device (usually a voltage controlled oscillator, VCO) whose phase and frequency are not very stable over temperature and time to a more stable and lower frequency device (usually a temperature compensated or oven controlled crystal oscillator, TCXO or OCXO). As a black box, the PLL can be viewed as a frequency multiplier.

A PLL is employed when there is the need for a high frequency local oscillator (LO) source. Example applications are numerous and include wireless communications, medical devices and instrumentation.

Figure 1 shows the building blocks of a PLL system used for generating an LO signal. The PLL integrated circuit (IC) usually contains all clock dividers (R and N), phase/frequency detector (PFD) and the charge pump, represented by the two current sources, ICP_UP and ICP_DN.

The VCO output is compared to the reference clock (the OCXO output here) after both signals are divided down in frequency by their respective integer dividers (N and R, respectively). The PFD block controls the charge pump to sink or source current pulses at the f_{PFD} rate into the loop filter to adjust the voltage on the tuning port of the VCO (V_TUNE) until the outputs of the clock dividers are equal in frequency and are in phase. When these are equal, it is said that the PLL is locked. The LO frequency is related to the reference frequency, f_{REF}, by the following equation:

$$f_{LO} = \frac{N}{R} \bullet f_{REF}$$

The PLL shown in Figure 1 is called an integer-N PLL because the feedback divider (the N-divider) can only assume integer values. When this divider can assume both integer and noninteger values, the loop is called a fractional-N PLL. The focus here will be only on integer-N PLLs, as different mechanisms are at work in fractional-N PLLs.

Integer-N PLL Nonidealities

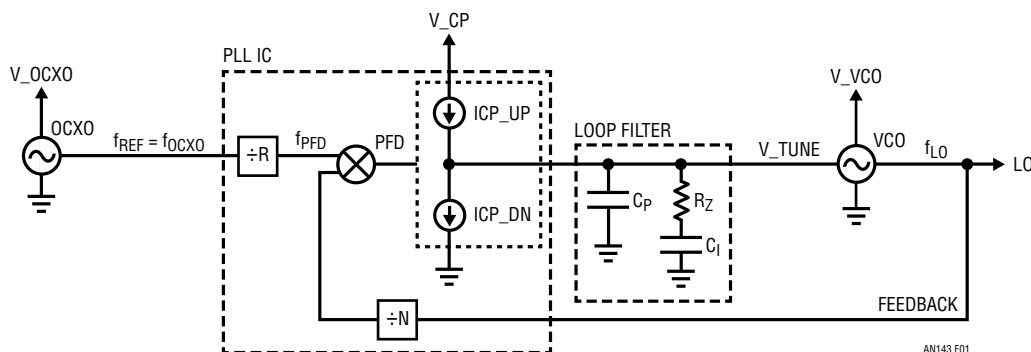The PLL IC contributes its own nonidealities to the system, principally phase noise and spurious.

**Figure 1. Basic Building Blocks of a PLL**

Phase Noise

The PLL system of Figure 1 acts as a low pass filter on the reference clock phase noise and as a high pass filter on that of the VCO. The low pass and high pass filter cutoff frequency is defined by the loop bandwidth (LBW) of the PLL. Ideally, the LO phase noise follows that of the reference clock converted to the LO frequency (that is, multiplied by N/R) up to the LBW and subsequently follows the phase noise of the VCO. The PLL IC's noise contribution elevates the phase noise in the transition area.

Figure 2 is a phase noise plot generated by PLLWizard™, a free PLL design and simulation tool from Linear Technology. The figure shows both the total output phase noise (TOTAL), and the individual noises at the output due to the reference (REF at RF) and the VCO (VCO at RF). The IC's noise contribution can easily be seen in the highlighted area.
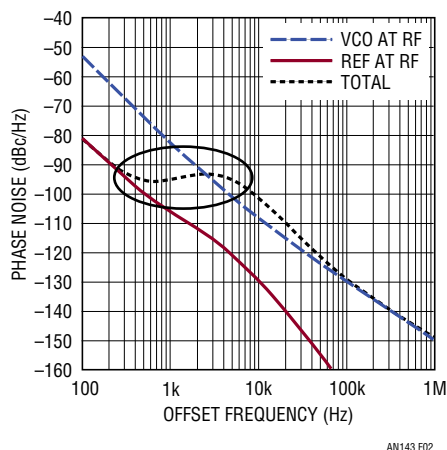

Figure 2. PLL IC Phase Noise Contribution Region as Highlighted by the Drawn Ellipse

Spurious

Any unwanted signals on the power supplies shown in Figure 1 (V_OCXO, V_CP and V_VCO) can translate into spurious (spurs) on the LO signal. Careful design of these supplies greatly reduces or even eliminates these spurs. Charge pump related spurs, however, are inevitable. But, they can be reduced with careful PLL system design. These spurs are commonly referred to as reference spurs, though reference here does not mean the reference clock frequency. Rather, it refers to f_{PFD}. An LO signal produced by an integer-N PLL has dual sideband spurs at f_{PFD} and its harmonics.

For example, Figure 3 shows the spectrum of a 2.1GHz LO signal. f_{PFD} is 1MHz (N = 2100) and the reference clock is 10MHz (R = 10). The loop bandwidth is 40kHz. As a side note, it is worth mentioning that the spurious level achieved in this measurement is world class due to the high performance of the LTC6945, an ultralow noise and spurious PLL IC from Linear Technology.
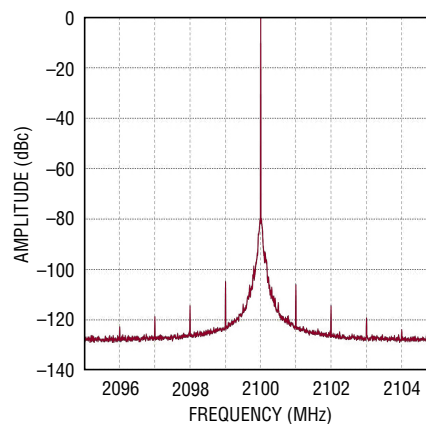
Figure 3. Reference Spurs of a 2100 MHz LO Signal with an f_{PFD} of 1MHz Generated Using the LTC6945 PLL IC from Linear Technology Along with the UMX-586-D16-G VCO from RFMD

Causes of Reference Spurs

In steady-state operation, the PLL is locked, and, theoretically, there is no more need to engage the ICP_UP and ICP_DN current sources of Figure 1 during every PFD cycle. However, doing so would create a dead zone in the loop response as there is a significant drop in the small-signal loop gain (practically, an open loop). This dead zone is eliminated by forcing ICP_UP and ICP_DN to produce extremely narrow pulses during every PFD cycle. These are commonly referred to as anti-backlash pulses. This produces energy content on the VCO tune line at f_{PFD} and its harmonics. The negative feedback cannot counteract these pulses since these frequencies are outside the loop bandwidth of a properly designed PLL. The VCO, then, is frequency modulated (FM) by this energy content, and related spurs appear at f_{PFD} and its harmonics, all centered around LO.

Between anti-backlash pulses, the charge pump current sources are off (tri-stated). Inherently, the charge pump has some leakage current when tri-stated. Using an op amp in an active loop filter (such as in Figure 7) introduces yet

another leakage current source due to the op amp's input bias and offset currents. The aggregate of these unwanted currents, whether sourcing or sinking, causes a drift in the voltage across the loop filter and, consequently, in the tune voltage of the VCO. The negative feedback of the loop will correct for this anomaly by introducing a unipolar current pulse from the charge pump once every PFD cycle so that the average tune line voltage produces the correct frequency out of the VCO. The pulses produce energy at f_{PFD}, which also causes spurs to appear centered around LO and offset by f_{PFD} and its harmonics as previously noted.

In integer-N PLLs, f_{PFD} is often chosen to be relatively small because of the system's frequency step size requirements. This means that the anti-backlash pulse width, especially with the present high speed IC technologies, is extremely small compared to the PFD period. As such, a large leakage current causes the total charge pump pulses to be unipolar and tends to be the dominant cause of reference spurs. This phenomenon will be examined in more depth.

Reference Spurs' Effect on System Performance

In a particular communications frequency band there are multiple channels that occupy equal bandwidths. The center-to-center frequency distance between two adjacent channels is equal among all channels and is denoted by channel spacing. Due to several factors, it is common to find large variations in signal strength between any two adjacent channels.

A typical scenario in a multi-channel wireless communications system where a stronger channel exists adjacent to the desired but weaker channel is shown in Figure 4. Only one of the LO reference spurs of concern is shown.

In an integer-N PLL, f_{PFD} is usually chosen to be equal to the channel spacing, which means that the reference spurs are positioned at the channel spacing from the LO. These spurs translate all adjacent and nearby channels to the center of the intermediate frequency (f_{IF}) along with the LO mixing the desired channel to the same frequency. These undesired channels, being uncorrelated to the signal in the desired channel, appear as an elevated noise floor to the desired signal and limit the signal-to-noise ratio.
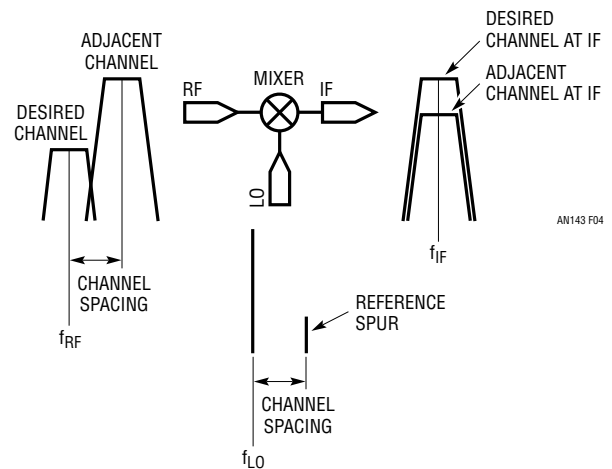
Figure 4. Illustration of Adjacent Channel Interference Due to Reference Spurs

Relationship Between Leakage Current and Reference Spur Levels

The mathematical prediction of a PLL IC's phase noise contribution is relatively straightforward and can be accurately determined by calculations. However, the prediction of reference spur levels is traditionally believed to be complex. This section derives a method to accurately predict reference spur levels due to leakage current using simple calculations. Two examples using different loop filters will be examined.

Passive Loop Filter Example

A PLL system with a typical passive loop filter is shown in Figure 5 along with a current source denoted I_LEAKAGE to represent the leakage current of the charge pump. Assuming the PLL is locked, I_LEAKAGE reduces the charge held by C_P during the time when the charge pump is off. When the charge pump turns on once every PFD cycle, ICP_UP replenishes the charge lost from C_P by applying a short pulse of current. Feedback forces the average voltage seen at V_TUNE (V_TUNE_AVG) to be constant, maintaining the correct LO frequency. Figure 6 depicts this visually.

The derivation of the resultant spurs involves some knowledge of loop stability requirements, the first being LBW

restrictions. The LBW of the PLL system is designed to be at least 10 times smaller than f_{PFD},

$$LBW \le \frac{f_{PFD}}{10}$$

This means that the period of the PFD is:

$$T_{PFD} = \frac{1}{f_{PFD}} \text{ and, hence, LBW} \le \frac{1}{10 \cdot T_{PFD}}$$

To create a stable loop with plenty of phase margin, a zero, consisting of R_Z and C_I in Figure 5, is inserted in the loop at about 1/3rd the LBW. That is,

$$\text{Zero Location} \approx \frac{LBW}{3} = \frac{1}{2\pi\tau_Z} \Rightarrow LBW \approx \frac{3}{2\pi\tau_Z},$$

where $\tau_Z = R_Z \cdot C_I$

Replacing LBW in the last equation with its equivalent in terms of T_{PFD} results in:

$$\frac{3}{2\pi\tau_Z} \le \frac{1}{10 \cdot T_{PFD}} \text{, or } T_{PFD} \le \frac{2\pi}{30}\tau_Z$$

This means that the PFD period is almost five times shorter than the time constant of the zero, τ_Z. This implies that the ripple produced at a period of T_{PFD} across C_P is mostly unseen by C_I. The closed-loop bandwidth LBW is approximately equal to the unity crossing of the open-loop gain. Since the zero is located within the loop bandwidth (it is located at 1/3rd the unity crossing of the open-loop gain), the voltage across C_I is dictated by the negative feedback and is mostly a DC value.

Practically speaking, only C_P is discharged and charged during the PFD cycles shown in Figure 6.

If a capacitor, C, is charged or discharged with a constant current source, I, over a period of time given by ΔT, the voltage delta across this capacitor is given by:

$$\Delta V = I\frac{\Delta T}{C}$$

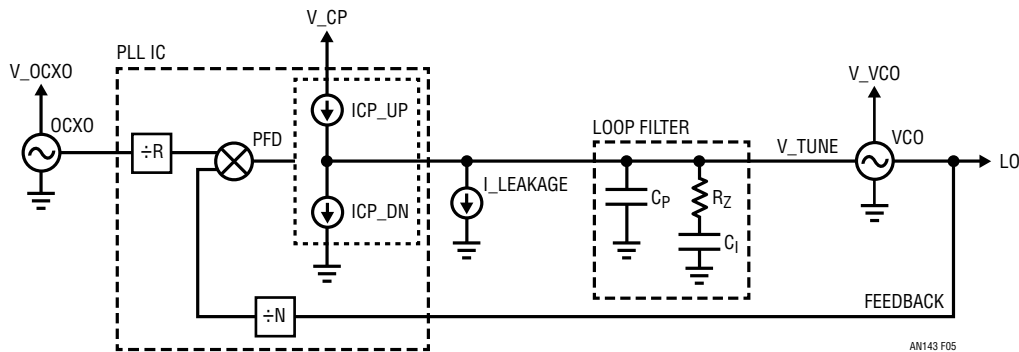To maintain a fixed output frequency at LO, the voltage droop that occurs during the discharge period is equal to

Figure 5. A PLL System with a Passive Loop Filter and I_Leakage Representing the Charge Pump Leakage Current

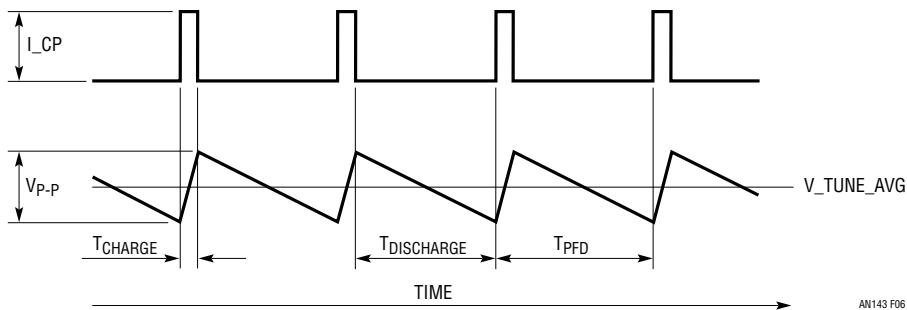

Figure 6. C_P Discharging Through I_Leakage and Charging Back Through ICP_UP Every PFD Cycle

the voltage buildup during the charging period of Figure 6. That is:

$$V_{P-P} = \frac{I\_LEAKAGE \cdot T_{DISCHARGE}}{C_P} = \frac{I\_CP \cdot T_{CHARGE}}{C_P}$$

where, T_{CHARGE} is the amount of time the charge pump current is active during every PFD cycle.

The charge pump current, I_CP, is usually in the mA range and I_LEAKAGE is usually in the nA range, which means that:

$$T_{CHARGE} \ll T_{PFD} \text{ and } T_{DISCHARGE} \approx T_{PFD}$$

This implies that the ripple voltage seen across C_P can be represented by a sawtooth waveform.

To study the effect of this sawtooth waveform on the spectrum of the LO signal, and since the waveform is a periodic function, it can be broken down into its frequency components using Fourier Series analysis.

$$SAWTOOTH\ FOURIER\ SERIES = DC\ VALUE - \frac{V_{P-P}}{\pi} \sum_{n=1}^{\infty} \frac{sin(2\pi nft)}{n}$$

where:

$$V_{P-P} = \frac{I\_LEAKAGE \cdot T_{PFD}}{C_P} = \frac{I\_LEAKAGE}{C_P \cdot f_{PFD}}$$

When n = 1, the fundamental peak is:

$$V_{P-FUND} = \frac{I\_LEAKAGE}{\pi C_P \cdot f_{PFD}}$$

the 2nd harmonic peak is:

$$V_{P-2ndHAR} = \frac{I\_LEAKAGE}{2\pi C_P \cdot f_{PFD}}$$

and so on.

The DC value, which is equal to V_TUNE_AVG in Figure 6, is set by the negative feedback per the requested LO frequency. The AC components, however, frequency modulate the VCO through its tune pin with a tuning sensitivity of K_{VCO} to produce dual sideband spurs with a fundamental of f_{PFD}. The Appendix derives the following equation that is going to be used next.

$$\frac{SIDEBAND}{CARRIER} = 20log_{10}\left(\frac{K_{VCO} \cdot E_m}{2f_m}\right), dB$$

The effect of the negative feedback on these AC components is negligible because f_{PFD}, being the fundamental and the lowest frequency component, is at least 10 times higher in frequency than the zero dB crossing of the open-loop gain by design.

To find the fundamental reference spur-to-carrier power ratio, $f_m = f_{PFD}$, $E_m = V_{P-FUND}$ and:

$$\frac{REF\_SPUR\_FUND}{CARRIER} = 20log_{10}\left(\frac{K_{VCO} \cdot I\_LEAKAGE}{2\pi C_P \cdot f_{PFD}^2}\right), dBc$$

For the 2nd harmonic reference spur, $f_m = 2 f_{PFD}$, $E_m = V_{P-2ndHAR}$ and:

$$\frac{REF\_SPUR\_2ndHAR}{CARRIER} = 20log_{10}\left(\frac{K_{VCO} \cdot I\_LEAKAGE}{8\pi C_P \cdot f_{PFD}^2}\right), dBc$$

Ratios for higher order harmonics are found using a similar approach.

Active Loop Filter Example

Figure 7 shows an example implementation of an active loop filter built around an op amp. I_LEAKAGE represents the combined leakage currents of the charge pump and the
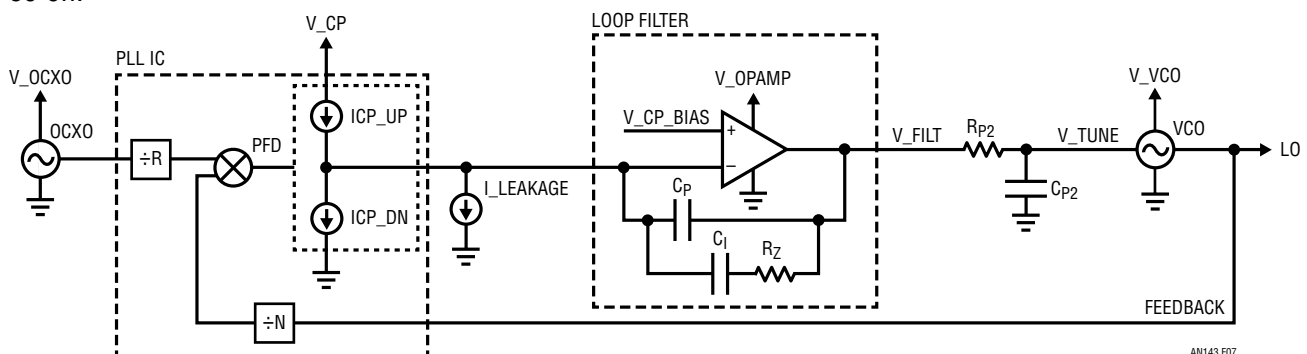

Figure 7. A PLL System with an Active Loop Filter and I_Leakage Representing the Charge Pump and Op Amp Leakage Currents

op amp. The same methodology used in the passive filter example applies here since the loop filters have a similar structure. The addition of the pole composed of R_{P2} and C_{P2} at the output of the op amp to limit the device's contribution of noise beyond 15 or 20 times the LBW reduces the amplitude of the sawtooth signal seen at the tuning node of the VCO. It should be noted that C_{P2} includes the input capacitance of the VCO tune port.

The sawtooth signal undergoes low pass filtering whose equation can be found using basic voltage division equations in the Laplace Transform domain and can be written as:

$$\left|\frac{V\_TUNE}{V\_FILT}\right| = \left|\frac{1}{1 + j2\pi f \cdot R_{P2} \cdot C_{P2}}\right|,$$

where f represents frequency in Hz.

Naturally, the sawtooth signal Fourier Series components get affected differently according to their frequency. The reference spur-to-carrier ratios become:

$$\frac{REF\_SPUR\_FUND}{CARRIER} = 20\log_{10}\left(\frac{K_{VCO} \cdot I\_LEAKAGE \cdot \left|\frac{V\_TUNE}{V\_FILT}\right|_1}{2\pi C_P \cdot f_{PFD}^2}\right),$$

dBc, where

$$\left|\frac{V\_TUNE}{V\_FILT}\right|_1 = \left|\frac{1}{1 + j2\pi \cdot f_{PFD} \cdot R_{P2} \cdot C_{P2}}\right|,$$

$$\frac{REF\_SPUR\_2ndHAR}{CARRIER} = 20\log_{10}\left(\frac{K_{VCO} \cdot I\_LEAKAGE \cdot \left|\frac{V\_TUNE}{V\_FILT}\right|_2}{8\pi C_P \cdot f_{PFD}^2}\right),$$

dBc, where

$$\left|\frac{V\_TUNE}{V\_FILT}\right|_2 = \left|\frac{1}{1 + j4\pi \cdot f_{PFD} \cdot R_{P2} \cdot C_{P2}}\right|, \text{ and so on.}$$

Lab Verification of the Theory

The PLL systems shown in Figures 5 and 7 were reproduced in the lab. External current was introduced at the charge pump node using a precision source meter to null the intrinsic fundamental reference spur caused by inherent leakages in the system. Then, specific additional current

values were injected into the loop while measuring the fundamental reference spur levels. Figure 8 compares the measured and calculated values for both filter types. The measured and calculated numbers agree to within the instrument accuracies and component tolerances.
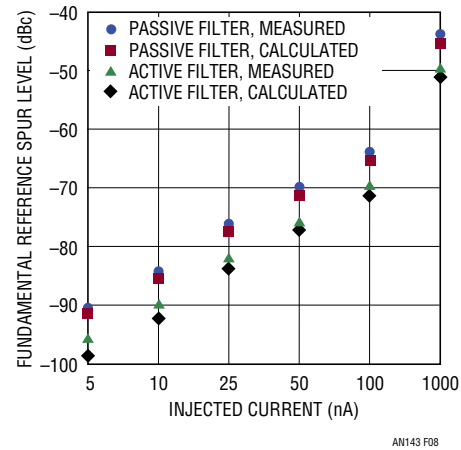
Figure 8. Comparison of Measured and Calculated Fundamental Reference Spur Levels Using Active and Passive Loop Filters

Table 1. Details About the PLL Systems Used to Generate the Measurements of Figure 8.

	PASSIVE LOOP FILTER	ACTIVE LOOP FILTER
PLL IC	LTC6945, 6GHz Integer-N Synthesizer from Linear Technology	LTC6945, 6GHz Integer-N Synthesizer from Linear Technology
Op Amp	N/A	LT1678, Low Noise, Rail-to-Rail Precision Op Amp from Linear Technology
VCO	CVCO55CL-0902-0928, 902 to 928 MHz VCO from Crystek	UMS-1400-A16-G, 700-1400 MHz VCO from RFMD
C_P (nF)	8.2	22
f_{PFD} (kHz)	250	250
K_{VCO} (MHz/V)	18	63
LBW (kHz)	7	7.6
R_{P2} (Ω)	N/A	100
C_{P2} (nF)	N/A	13.3

Summary of Results

Table 2 summarizes the equations derived in this application note.

Conclusion

Integer-N PLL operation and nonidealities are important topics in the design of RF systems. Reference spurs can have a significantly negative impact on overall system performance. The simple model shown here accurately predicts reference spur levels due to leakage current in PLLs and can be a useful design tool, significantly reducing the number of board revisions required to reach a desired solution.

Appendix: Derivation of Spur-to-Carrier Ratio Using Narrowband FM Equations

Consider an FM signal centered at an LO of frequency f_c in Hz. This signal can be written as:

$$e(t) = E_c \cos(2\pi f_c t + \theta(t)),$$

where E_c is the peak amplitude of e(t) in V.

The instantaneous frequency of e(t) is:

$$\omega_{inst} = \frac{d}{dt}(2\pi f_c t + \theta(t)) = 2\pi f_c + \theta'(t), \, rad/sec$$

Since e(t) is an FM signal, the modulating signal $e_m(t)$ modulates the instantaneous frequency of e(t) as follows:

$$\theta'(t) = K e_m(t), \, rad/sec$$

where K is the deviation sensitivity of frequency in rad/(sec • V):

$$\theta(t) = \int_0^t \theta'(t)dt = \int_0^t K e_m(t)dt = K\int_0^t e_m(t)dt$$

As far as this paper is concerned, the modulating signal is a tone—one of the Fourier Series components of the sawtooth waveform—which is given by:

$$e_m(t) = E_m \cos(2\pi f_m t),$$

where E_m is the peak amplitude of $e_m(t)$ in V and f_m is its frequency in Hz.

Table 2. Summary of Formulas to Predict Reference Spur Levels Up to the 3rd Harmonic

Loop Filter Type	Passive	Active
Reference to	Figure 5	Figure 7
$\dfrac{REF\_SPUR\_FUND}{CARRIER}$(dBc)	$20\log_{10}\left(\dfrac{K_{VCO} \bullet I\_LEAKAGE \bullet \left\lvert\frac{V\_TUNE}{V\_FILT}\right\rvert_1}{2\pi C_P \bullet f_{PFD}{}^2}\right)$	
$\left\lvert\dfrac{V\_TUNE}{V\_FILT}\right\rvert_1$	1	$\left\lvert\dfrac{1}{1+j2\pi \bullet f_{PFD} \bullet R_{P2} \bullet C_{P2}}\right\rvert$
$\dfrac{REF\_SPUR\_2ndHAR}{CARRIER}$(dBc)	$20\log_{10}\left(\dfrac{K_{VCO} \bullet I\_LEAKAGE \bullet \left\lvert\frac{V\_TUNE}{V\_FILT}\right\rvert_2}{8\pi C_P \bullet f_{PFD}{}^2}\right)$	
$\left\lvert\dfrac{V\_TUNE}{V\_FILT}\right\rvert_2$	1	$\left\lvert\dfrac{1}{1+j4\pi \bullet f_{PFD} \bullet R_{P2} \bullet C_{P2}}\right\rvert$
$\dfrac{REF\_SPUR\_3rdHAR}{CARRIER}$(dBc)	$20\log_{10}\left(\dfrac{K_{VCO} \bullet I\_LEAKAGE \bullet \left\lvert\frac{V\_TUNE}{V\_FILT}\right\rvert_3}{18\pi C_P \bullet f_{PFD}{}^2}\right)$	
$\left\lvert\dfrac{V\_TUNE}{V\_FILT}\right\rvert_3$	1	$\left\lvert\dfrac{1}{1+j6\pi \bullet f_{PFD} \bullet R_{P2} \bullet C_{P2}}\right\rvert$

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This means that the time varying component of e(t)'s phase is:

$$\theta(t) = K \int_0^t E_m \cos(2\pi f_m t) dt = \frac{K \cdot E_m}{2\pi f_m} \sin(2\pi f_m t)$$

$$= \frac{2\pi K_{VCO} \cdot E_m}{2\pi f_m} \sin(2\pi f_m t),$$

where K_{VCO}, in Hz/V, is the tuning sensitivity of the VCO used to generate e(t).

Define m as the modulation index, such as:

$$\theta(t) = \frac{K_{VCO} \cdot E_m}{f_m} \sin(2\pi f_m t) = m \cdot \sin(2\pi f_m t),$$

$$\text{where } m = \frac{K_{VCO} \cdot E_m}{f_m}$$

e(t), then, can be written as:

$$e(t) = E_c \cos(2\pi f_c t + m \cdot \sin(2\pi f_m t)).$$

Expanding using some basic trigonometric identities gives:

$$e(t) = E_c \cos(2\pi f_c t) \cdot \cos(m \cdot \sin(2\pi f_m t)) - E_c \sin(2\pi f_c t) \cdot \sin(m \cdot \sin(2\pi f_m t)),$$

m is much smaller than 1 as far as the reference spur generation is concerned. This implies that:

$$\cos(m \cdot \sin(2\pi f_m t)) \approx 1,$$

$$\text{and } \sin(m \cdot \sin(2\pi f_m t)) \approx m \cdot \sin(2\pi f_m t)$$

Then

$$e(t) \approx E_c \cos(2\pi f_c t) - m \cdot E_c \sin(2\pi f_c t) \cdot \sin(2\pi f_m t),$$

or

$$e(t) = E_c \cos(2\pi f_c t) + \frac{1}{2} m \cdot E_c (\cos(2\pi(f_c + f_m)t)$$

$$- \cos(2\pi(f_c - f_m)t)),$$

which is a narrow band FM signal composed of a carrier at f_c and two sidebands located at $\pm f_m$ centered around the carrier.

Based on the last representation of e(t), sideband-to-carrier power ratio in dBc is given by:

$$\frac{\text{SIDEBAND}}{\text{CARRIER}} = 20\log_{10}\left(\frac{m}{2}\right) = 20\log_{10}\left(\frac{K_{VCO} \cdot E_m}{2f_m}\right)$$

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