W65C265S DATA SHEET

March 1, 2000

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INTRODUCTION

The WDC W65C265S microcomputer is a complete fully static 16-bit computer fabricated on a single chip using a Hi-Rel low power CMOS process. The W65C265S complements an established and growing line of W65C products and has a wide range of microcomputer applications. The W65C265S has been developed for Hi-Rel applications and where minimum power is required.

The W65C265S consists of a W65C816S (Static) Central Processing Unit (CPU), 8K bytes of Read Only Memory (ROM), 576 bytes of Random Access Memory (RAM), Processor defined cache under software control, eight 16-bit timers with maskable interrupts, high performance interrupt-driven Parallel Interface Bus (PIB), four Universal Asynchronous Receivers and Transmitters (UART) with baud rate timers, Monitor "Watch Dog" Timer with "restart" interrupt, twenty-nine priority encoded interrupts, Built-in Emulation features, Time of Day (ToD) clock features, Twin Tone Generators (TGx), Bus Control Register (BCR) for external memory bus control, interface circuitry for peripheral devices, ABORT input for low cost virtual memory interface, and many low power features.

The innovative architecture and demonstrated high performance of the W65C265S CPU, as well as instruction simplicity, result in system cost-effectiveness and a wide range of computational power. These features make the W65C265S a leading candidate for 16-bit microcomputer applications especially where task oriented processing is desired.

This product description assumes that the reader is familiar with the W65C816S CPU hardware and programming capabilities. Refer to the W65C816S Data Sheet for additional information.

KEY FEATURES OF THE W65C265S

- Hi-Rel low power CMOS process
- Operating TA =0°C to +70°C
- Single 2.8V to 5.5V power supply
- Static to 8MHz clock operation
- W65C816S compatible CPU
  - 8- and 16-bit parallel processing
  - Variable length stack
  - True indexing capability
  - Twenty-four address modes
  - Decimal or binary arithmetic
  - Pipeline architecture
  - Fully static CPU
- Single chip microcomputer
  - 2 Tone Generators
  - 64 CMOS compatible I/O lines
  - 8K x 8 ROM on-chip
  - 576 x 8 RAM on-chip
  - WAIt for interrupt
  - SToP the clock
  - Fast oscillator start and stop feature
- 16Mbyte linear address space
- Twenty-nine priority encoded interrupts
  - BRK software interrupt
  - RESET "RESTART" interrupt
  - NMIB Non-Maskable interrupt
  - ABORT interrupt
  - COP software interrupt
  - IRQB level interrupt
  - 8 timer edge interrupts
  - 6 edge interrupts
  - PIB interrupt
  - 4 UART Receiver interrupts
  - 4 UART Transmitter interrupts
- Four UARTS's
- Time of Day (ToD) clock features
- 8 x 16 bit timer/counters
- Bus Control Register
- Many bus operating features and modes
- 8 Programmable chip select outputs
- Low cost surface mount 84 and 100 lead packages
- Macro and Cross assemblers available
- C compilers available

SECTION 1

W65C265S FUNCTION DESCRIPTION

1.1 The W65C816S Static 16-bit Microprocessor Core

The W65C816S 16-bit microprocessor is the fully static (may be stopped when PHI2 is high or low) version of the popular W65C816 microprocessor used in the Apple IIgs personal computer system. The W65C816S is compatible* with the NMOS 6502 and CMOS 65C02 used in many control applications and personal computers.

The small die size and low power consumption of the W65C816S offer an excellent choice as a cost effective 16-bit core microprocessor in one-chip microcomputers.

The W65C816S instruction set is compatible with the W65C02 and W65C02S, 8-bit microprocessors, W65C802 and W65C816, 16-bit microprocessors.

1.2 8K x 8 ROM ($E000-$FFFF)

The W65C265S 8K x 8 bit Read Only Memory (ROM) usually contains the user's program instructions, interrupt vectors, and other fixed constants. The rom is programmable into the ROM during fabrication of the W65C265S device.

1.3 576 x 8 RAM ($0000-$01FF,$DF80-$DFBF)

The 576 x 8 bit Random Access Memory (RAM) contains the user program stack and is used for scratch pad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data.

1.4 Bus Control Register (BCR)

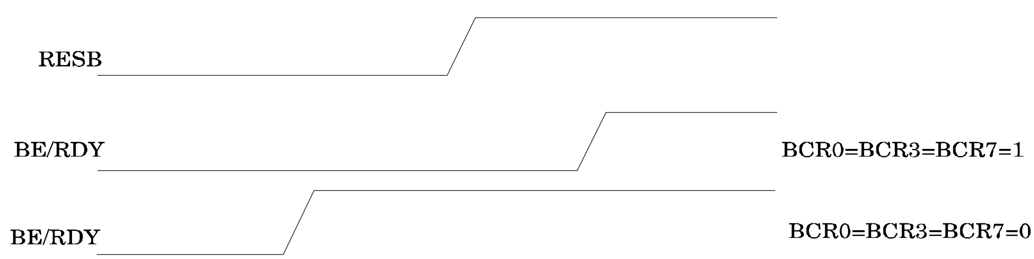
1.4.1 The Bus Control Register (BCR) controls the various modes of I/O and external memory interface.
1.4.2 During power-up the value of BE defines the initial values of BCR0, BCR3 and BCR7, three bits in the BCR that set up the W65C265S for In-Circuit-Emulation (ICE) or normal mode.
1.4.3 When BE goes high after RESB goes high the BCR sets up the W65C265S for emulation. Port 0 and 1 are the address outputs, Port 2 is the data I/O bus and RUN is the multiplexed RUN function. (see RUN pin function description).
1.4.4 When BE goes high before RESB goes high, all bits in the BCR are "0".
1.4.5 After RESB goes high BE no longer effects the BCR register, and BCR may be written under software control to reconfigure the W65C265S as desired.
1.4.6 Table 1-1 and Figure 1-1 (following page) indicate how BCR7 and BE define the W65C265S configuration.

*except for the bit manipulation instructions that do not exist for the W65C816S

Table 1-1 BCR7 and BE Control

BCR7	BE	W65C265S configuration
0	0	Internal ROM External Processor (DMA test mode)
0	1	Internal ROM Internal Processor
1	0	External ROM External Processor (DMA test mode)
1	1	External ROM Internal Processor

Figure 1-1 BE Timing Relative to RESB Input



7	6	5	4	3	2	1	0	BCRx ($DF40)

External Memory Bus Enable
0 = Ports 0,1,2,3 are I/O
1 = Ports 0,1,2,3 are address and data bus for external memory or I/O access

Toner Generator 0 (TG0) Enable
0 = Disable TG0
1 = Enable TG0

Tone Generator 1 (TG1) Enable
0 = Disable TG1
1 = Enable TG1

In-Circuit-Emulation (ICE) Enable
0 = RUN = RUN, BA = BA/1, W65C265S is in normal mode of operation
1 = RUN = RUN, BA = BA, All on-chip addressed memory or I/O for reads or writes are output on the data bus (this is the emulation mode of operation)

Monitor "Watch Dog" Enable
0 = disable
1 = enable

ABORTB enable
0 = disable ABORTB
1 = enable ABORTB on P40 See Note #1

NMIB enable
0 = disable NMIB
1 = enable NMIB on P40 See Note #1

External ROM Enable
0 = internal ROM ($E000-$FFFF)
1 = external ROM ($E000-$FFFF)

Note #1: Input is level sensitive, NMIB and ABORTB can not both be enabled at the same time.

Figure 1-2 Bus Control Register (BCR)

1.5 The Timers

1.5.1 Upon Timer clock input negative edge the timer counter is decremented by 1.
1.5.2 A write to the timer low counter writes the timer low latch.
1.5.3 A read of the timer high or low counter reads the timer high or low counter.
1.5.4 Upon Timer clock input negative edge when the timer low counter reaches zero, the timer high counter is decremented by 1. Upon Timer clock input positive edge, when the timer high counter reaches zero, this sequence occurs:
1.5.4.1 The Timer sets its associated interrupt flag. If the interrupt is enabled the MPU is then interrupted and control is transferred to the vector associated with the interrupt. When Timer 0 times out, the W65C265S is restarted: on-chip logic pulls RESB pin low for 2 CLK cycles and releases RESB to go high, "restarting" the W65C265S.
1.5.4.2 The Timer high counter is loaded from the timer high latch, and timer low counter is loaded from timer low latch.
1.5.5 A write to the Timer high counter writes to the timer high latch and this sequence occurs:
1.5.5.1 The timer high latch is loaded from data bus.
1.5.5.2 The timer low counter is loaded from the timer low latch, and the timer high counter is loaded from the timer high latch.
1.5.6 Timer 0 is disabled after RESB and is activated by the first TER0 transistion from "0" to "1" (the first load of Timer 0).
1.5.6.1 The Timer 0 counter is reloaded with the value in the Timer 0 latches when the TER0 bit 0 makes a transition from a "0" to "1". TER0 transition from a "1" to a "0" has no effect on the timer.
1.5.7 A timer must be reloaded after it is disabled with TERx for it could have been stopped with all $FFFF's and when restarted will require full length count down.

Table 1-2 The Timer Functions

Number	Timer Function	TCR0=0	TCR0=1
T7	Pulse Width Measurement	FCLK	-
T6	Tone Generator	FCLK	-
T5	Tone Generator	FCLK	-
T4	UART Baud Rate or Pulse, Input/Output	FCLK	P60
T3	UART Baud Rate	FCLK	-
T2	Prescaled Interrupt	FCLK/16	-
T1	Time of Day	CLK	-
T0	Monitor Watch Dog	CLK	-

7	6	5	4	3	2	1	0	TCRx ($DF42)

Timer 4 Input Clock Select
0 = FCLK
1 = P60

Timer 4 Output Enable
0 = disable
1 = enable output on P61

PWM Edge Interrupt Select on P62

0	0	disable
0	1	Positive Edge
1	0	Negative Edge
1	1	Both Edges

UART0 Timer Select
0 = Timer 3
1 = Timer 4

UART1 Timer Select
0 = Timer 3
1 = Timer 4

UART2 Timer Select
0 = Timer 3
1 = Timer 4

UART3 Timer Select
0 = Timer 3
1 = Timer 4

Figure 1-3 Timer Control Register (TCR)

7	6	5	4	3	2	1	0	TERx ($DF43)
Timer 7	Timer 6	Timer 5	Timer 4	Timer 3	Timer 2	Timer 1	Timer 0	

0=disable

1=enable

Figure 1-4 Timer Enable Register (TER)

1.6 Interrupt Flag Registers (TIFR,EIFR,UIFR)

1.6.1 A bit of these registers is set to a "1" in response to an interrupt signal from a source. Sources specified as level-triggered assert the corresponding IFR bit if an edge occurs and is held to a "1" as long as the IRQB input is held low. Sources specified as edge-triggered assert the corresponding IFR bit upon and only upon transition to the specified polarity. Note that changes for edge-triggered bits are asynchronous with PHI2.

1.6.1.1 Read of a IFR register. A read from an IFR register transfers its value to the internal data bus.

1.6.1.2 Write to an IFR register. A write of a "1" to any bits of these registers disasserts those bits but has no further effect when execution of that write instruction is completed; that is, the bit is reset by a pulse but not held reset. A write of a "0" to any bits of these registers has no effect. (Note that you must write a "1" to the corresponding IFR bit after the interrupt has been serviced; otherwise, the interrupt will continue to occur.)

1.6.1.3 Interrupt Priority. If more than one bit of the Interupt Flag Registers are set to a "1" and enabled, the vector corresponding to the highest memory map location and bit number asserted is used. For example, if both the TIFR1 and EIFR3 were asserted and enabled, then the vector corresponding to EIFR3 would be used. For another example, if both the TIFR3 and EIFR0 were asserted and enabled, then the vector corresponding to EIFR0 would be used.

1.7 Interrupt Enable Registers (TIER,EIER,UIER)

TIER, EIER, and UIER are the interrupt enable registers. Reading an IER register reads its contents and puts the value on the internal data bus. Writing an IER writes a value from the data bus into the register. Setting a bit in an IER to "1" permits the interrupt corresponding to the same bit in the IFR to cause a processor interrupt. If a WAI instruction has been executed prior to the interrupt occurring and the part is in the non-emulation mode (BCR3=0). The RUN pin will be low until the interrupt occurs and will then go high to indicate the part is running.

Note that the "I" flag in the microprocessor status register must be cleared with an instruction before any of the interrupts controlled by TIER, EIER, and UIER can occur.

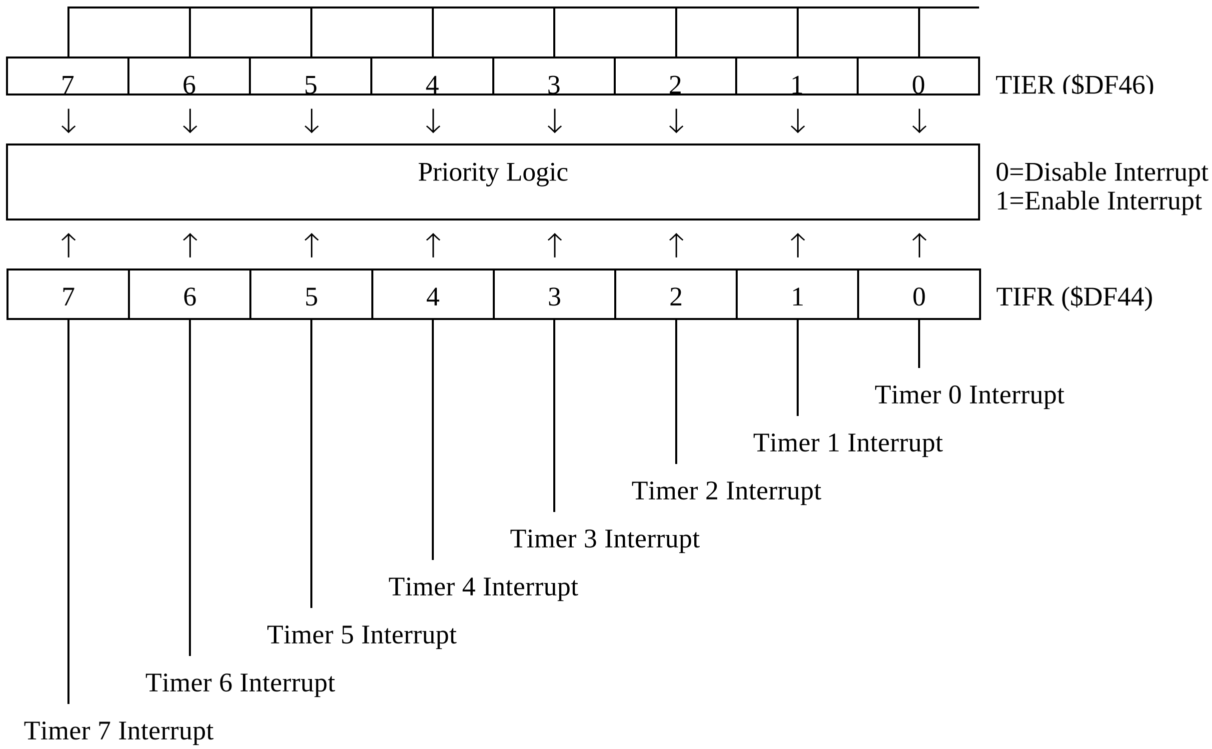


Figure 1-5 Timer Interrupt Enable Register (TIER) and Timer Interrupt Flag Register (TIFR)

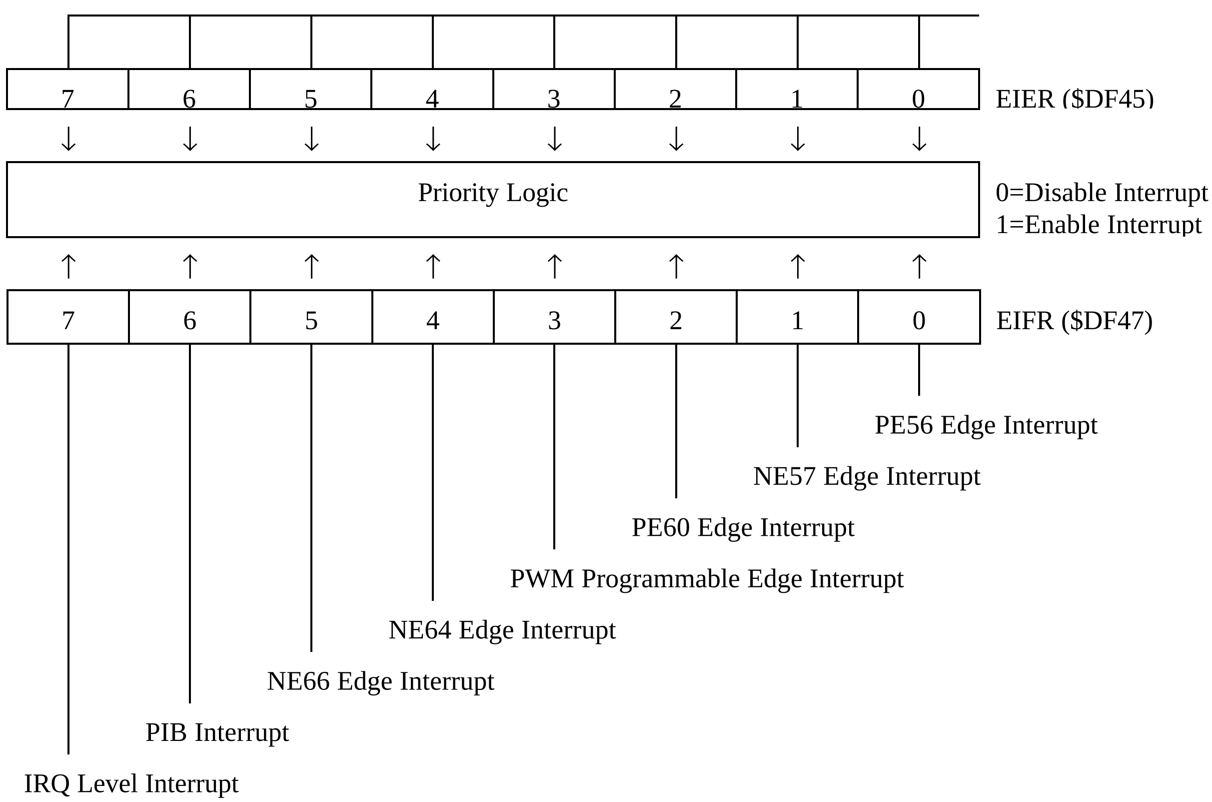


Figure 1-6 Edge Interrupt Enable Register (EIER) and Edge Interrupt Flag Register (EIFR)

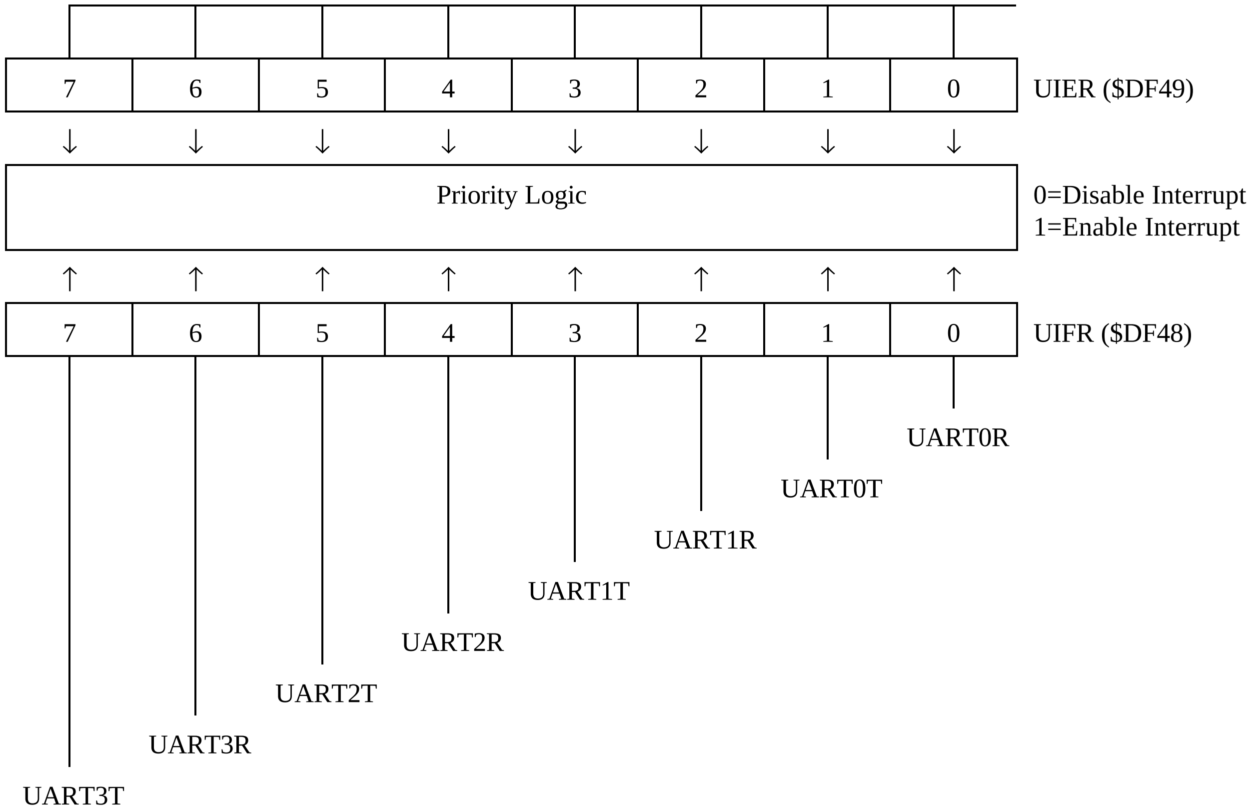


Figure 1-7 UART Interrupt Enable Register (UIER) and UART Interrupt Flag Register (UIFR)

1.8 Asynchronous I/O Data Rate Generation (Timer 3 and 4)

Timer 3 and 4 provide clock timing for the Asynchronous I/O and establishes the data rate for the Serial I/O port. Timer 3 and 4 operate as configured by TCRx and TERx (Timer Control Register and Timer Enable Register) and should be set up prior to enabling the UART.

Table 1-3 identifies the values to be loaded into Timer 3 and 4 to select standard data rates. Although Table 1-3 identifies only the more common data rates, any data rate can be selected by using the formula:

$$\text{where } N = \frac{FCLK}{16 \times bps} - 1$$

N decimal value to be loaded in to Timer A using its hexadecimal equivalent
FCLK the clock frequency
bps The desired data rate

Note: One may notice slight differences between the standard rate and the actual data rate. However, transmitter and receiver error of 1.5% or less is acceptable.

Table 1-3 Timer 3 and 4 Values for Baud Rate Selection

Standard Baud Rate	1.8432MHz	2.4576MHz	3.6864MHz	4.9152MHz	6.1440MHz
110	$0416	$0573	$082E	$0AE8	$0DA2
150	$02FF	$03FF	$05FF	$07FF	$09FF
300	$017F	$01FF	$02FF	$03FF	$04FF
600	$00BF	$00FF	$017F	$01FF	$027F
1200	$005F	$007F	$00BF	$00FF	$013F
1800	$003F	$0054	$007F	$00AA	$00DF
2400	$002F	$003F	$005F	$007F	$009F
4800	$0017	$001F	$002F	$003F	$004F
9600	$000B	$000F	$0017	$001F	$0027
19200	$0005	$0007	$000B	$000F	$0013
38400	$0002	$0003	$0005	$0007	$0009
57600	$0001	$0002	$0003	$0004	$0006

Note: Shading indicates transmitter or receiver error greater than 1.5%.

1.9 Universal Asynchronous Receiver/Transmitters (UARTs)

The W65C265S Microcomputer provides four full duplex Universal Asynchronous Receiver/Transmitters (UART) with programmable bit rates. The serial I/O functions are controlled by the Asynchronous Communication Control and Status Registers (ACSRx). The ACSRx bit assignment is shown in Figure 1-10. The serial bit rate is determined by Timer 3 or 4 for all modes for the UART's. The maximum data rate using the internal clock is 0.5MHz bits per second (FCLK = 8MHz). The Asynchronous Transmitter and Asynchronous Receiver can be independently enabled or disabled.

All transmitter and receiver bit rates will occur at one sixteenth of Timer 3 or 4 as selected.

Whenever Timer 3 or 4 is required as a timing source, it must be loaded with the hexadecimal code that selects the data rate for the serial I/O Port. Refer to Table 1-3 for a table of hexadecimal values that represent the desired data rate.

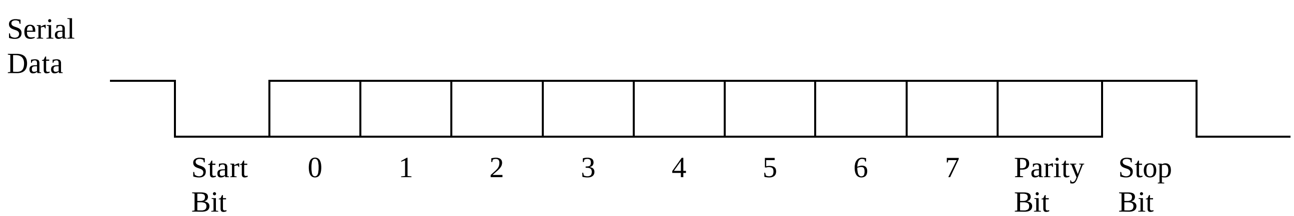
WDC Standard UART Features

- 7 or 8 bit data with or without Odd or Even parity.
- The Transmitter has 1 stop bit with parity or 2 stop bits without parity.
- The Receiver requires only 1 stop bit for all modes.
- Both the Receiver and Transmitter have priority encoded interrupts for service routines.
- The Receiver has error detection for parity error, framing error, or over-run error conditions that may require re-transmission of the message.
- The Receiver Interrupt occurs due to a receiver data register full condition.
- The Transmitter Interrupt can be selected to occur on either the data register empty (end-of-byte transmission) or both the data register empty and the shift register empty (end-of-message transmission) condition.

1.9.1 Asynchronous Transmitter Operation

The transmitter operation is controlled by the Asynchronous Control and Status Register (ACSRx. The transmitter automatically adds a start bit, parity bit and one or two stop bits as defined by the ACSRx. A word of transmitted data is 7 or 8 bits of data.

The Transmitter Data Register (ARTDx) is located at addresses $DF71, $DF73, $DF75, and $DF77 and is loaded on a write. The Receiver is read at this same address.



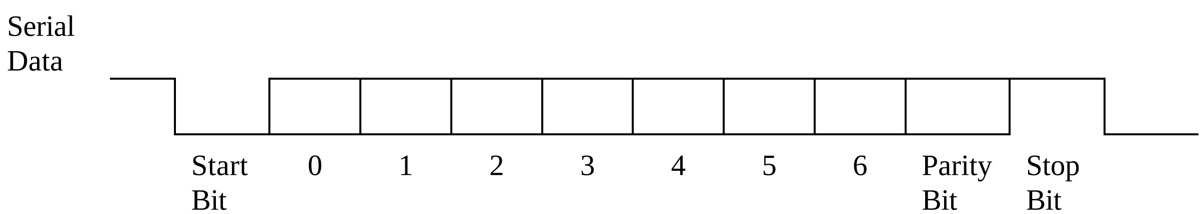
The Transmitter Interrupt is controlled by the Asynchronous Control Status Register bit ACSRx1.

IRQAT = ACSRx0((ACSRx1B)(DATA REGISTER EMPTY) + (ACSRx1)(DATA REGISTER AND SHIFT REGISTER EMPTY))

Figure 1-8 Asynchronous Transmitter Mode with Parity

1.9.2 Asynchronous Receiver Operation

The receiver and its selected control and status functions are enabled when ACSRx5 is set to a "1". The data format must have a start bit, 7 or 8 data bits, and one stop bit or one parity bit and one stop bit. The receiver bit period is divided into 16 sub-intervals for internal synchronization. The receiver bit stream is synchronized by the start bit, and a strobe signal is generated at the approximate center of each incoming bit. The character assembly process does not start if the start bit signal is less than one-half the bit time after a low level is detected on the Receive Data Input. A framing error, parity error or an over-run will set ASCRx7 the receiver error detection bit. An over-run condition occurs when the receiver data register has not been read and new data byte is transferred from the receiver shift register.



Note: The receiver requires only one stop bit but the transmitter supplies two stop bits for older system timing.

Figure 1-9 Asynchronous Data Timing for 7-bit Data without Parity

A receiver interrupt (IRQARx) is generated whenever the receiver shift register is transferred to the receiver data register.

1.9.3 Asynchronous Control and Status Registers (ACSRx)

The Asynchronous Control and Status Register (ACSRx) enables the Receiver and Transmitter and holds information on communication status error conditions.

Bit assignments and function of the ACSRx are as follows:

ACSRx0: Transmitter Enable. The Asynchronous Transmitter is enabled, the Transmitter Interrupt (IRQATx), and TXDx is enabled on P61, P63, P65 or P67 when ACSRx0=1. When ACSRx0 is cleared, the ACSRx1 is cleared, the transmitter will be disabled, the Transmitter Interrupt will not occur and TXDx will be disabled on P61, P63, P65 or P67. This bit is cleared by a RESET.

ACSRx1: Transmitter Interrupt Source Select. When ACSRx1=0, the Transmitter Interrupt occurs due to a Transmitter Data Register Empty condition (end-of-byte transmission). When ACSR=1 the Transmitter Interrupt occurs due to both the Transmitter Data and Shift register empty condition (end-of-message transmission). The Transmitter Interrupt is cleared by writing to the Transmitter Data Register.

ACSRx2: Seven- or Eight-Bit Data Select. When ACSRx2=0, the Transmitter and Receiver send and receive 7-bit data. The Transmitter sends a total of 10 bits of information (one start, 7 data, one parity and one stop or 2 stop bits). The Receiver receives 9 or 10 bits of information (one start, 7 data, and one stop or one stop and one parity bits). When writing to the Transmitter in seven bit mode, bit 7 is discarded. When reading from the receive data register during seven bit mode, bit 7 is always zero. When ACSRx2=1, the Transmitter and Receiver send and receive 8-bit data. The Transmitter sends 11 bits of information (one start, 8 data, one parity and one stop or two stop bits). The Receiver receives 10 or 11 bits of information (one start, 8 data, one stop or one parity and one stop bit). Reset clears ACSRx2.

ACSRx3: Parity Enable. When ACSRx3=0, parity is disabled. Reset clears ACSRx3. When ACSRx3=1, parity is enabled for both the Transmitter and Receiver.

ACSRx4: Odd or Even Parity. When ACSRx4=0 and parity is enabled, then Odd parity is generated where the number of ones is the data register plus parity bit equal an odd number of "1's". When ACSRx4=1 and parity is enabled, then Even parity is generated where the number of ones in the data register plus parity bit equal an even number of "1's". ACSRx4 is cleared by Reset.

ACSRx5: Receiver Enable. The Asynchronous Receiver is enabled when ACSRx5=1. Reset clears ACSRx5. When ACSRx5=1 the Receiver is enabled and Receiver Interrupts occur anytime the contents of the Receiver shift register contents are transferred to the Receiver Data Register. The Receiver Interrupt is cleared when the Receive Data Register is read. The Receive Data, RXDx, is enabled on Port 6 when ACSRx5=1. When ACSRx5=0, all Receiver operation is disabled and all Receive logic is cleared, the Receiver data register bits 0-6 are not affected and bit 7 is cleared.

ACSRx6: Software Semiphore. ACSRx6 may be used for communications among routines which access the UARTx. This bit has no effect on the UART operation and is cleared upon Reset. The bit can be thought of as a manually set busy signal.

ACSRx7: Receiver Error Flag. The Receiver logic detects three possible error conditions and sets ACSRx7: parity, framing or over-run. A parity error occurs when the parity bit received does not match the parity generated on the receive data. A framing error occurs when the stop bit time finds a "0" instead of a "1". An over-run occurs when the last data in the Receiver Data Register has not been read and new data is transferred from the Receive Shift Register. ACSRx7 is cleared by Reset or upon writing a "1" to ACSRx7. Writing a "0" to ACSR7 has not effect on ACSRx7.

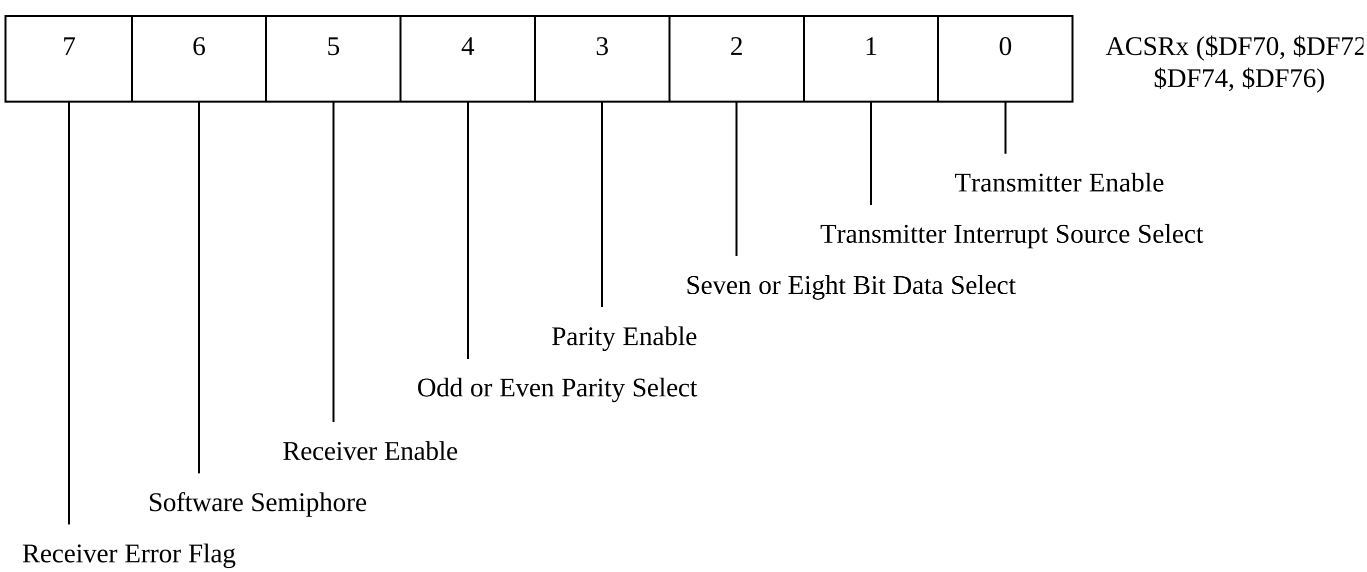


Figure 1-10 ACSRx Bit Assignments

1.10 The Parallel Interface Bus (PIB)

The Parallel Interface Bus (PIB) is used to communicate instructions and data to and from task oriented processors, smart peripherals, co-processors, and parallel processors.

PIRS 2,1,0 Register Address		
111	7	Automatic Handshake
110	6	
101	5	
100	4	
011	3	Automatic Handshake
010	2	
001	1	PIB Enable Register (PIBER)
000	0	PIB Flag Register (PRBFR)

Register 3 may have a primary role of communicating commands or opcodes between processors. Register 7 may have a primary role of communicating data or addresses between processors.

Figure 1-11 The PIB Registers

PIBER ($DF79)

0= Disable
1 = Enable

7 *3	6 *2	5 *3	4 *2	3 *3	2 *2	1 *3	0 *3

PIBFR ($DF78)

7 *1	6 *1	5 *2	4 *3	3 *1	2 *1	1 *4	0 *4

Bit 0: Enable Parallel Interface
0 = Disable PIB
1 = Enable PIB

Bit 1: Enable RDB and WRB
0 = CSB and WEB
1 = CS and WEB

Bit 2: Automatic Handshake Output Data Available in PIR3 (Reg. 3)
0 = Reset or Host Read of PIR3
1 = Processor Write to PIR3 and Interrupt Host

Bit 3: Automatic Handshake Input Data Available in PIR3 (Reg. 3)
0 = Reset or Processor Read of PIR3
1 = Host Write to PIR3 and Interrupt Processor

Bit 4: Manual Handshake from Processor
0 = Reset or Write "0" from Processor
1 = Write "1" from Processor and Interrupt Host

Bit 5: Manual Handshake from Host
0 = Reset or Write "0" from Host
1 = Write "1" from Host and Interrupt Processor

Bit 6: Automatic Handshake Output Data Available in PIR7 (Reg. 7)
0 = Reset or Host Read of PIR7
1 = Processor Write to PIR7 and Interrupt Host

Bit 7: Automatic Handshake Input Data Available in PIR7 (Reg. 7)
0 = Reset or Processor Read of PIR7
1 = Host Write to PIR7 and Interrupt Processor

Notes: *1 Read only from Host or Processor
*2 Read only from Processor, Read or Write from Host
*3 Read only from Host, Read or Write from Processor
*4 Read only from Host or Processor, will always read back a zero.

Figure 1-12 Parallel Interface Bus Enable (PIBER) and Flag (PIBFR) Registers

1.11 Twin Tone Generators

Each Tone Generator(TGx), as shown in figure 1-13 is comprised of a 16 bit timer and a 16 step divider circuit that selects the proper Digital to Analog (DA) output level. The enable bits for the tone generators are located in bits 1 and 2 of the BCR registers (see Figure 1-2).

$$\text{DA Level } n = E \cos(\pi \times (2n+1)/16) \quad 0 \leq n \leq 7$$

N=value loaded into timer latches

$$\text{Register Value } N = \frac{FCLK}{16xF} - 1$$

F=desired frequency

FCLK=FCLK input clock

FCLK ⇒ [16 bit Timerx] ⇒ [Divide by 16] ⇒ [DA Converter] ⇒ [TGx]

Figure 1-13 Tone Generator Block Diagram

Table 1-4 Communications Frequencies Generated by the Tone Generator Timers 5 and 6

	Standard Frequency (Hz)	Oscillator FCLK = 3.579545 MHz Register Value Hexi-decimal	Oscillator FCLK = 3.579545 MHz Register Value Decimal	Oscillator FCLK = 3.579545 MHz Actual Frequency (Hz)	Oscillator FCLK = 4.000000 MHz Register Value Hexi-decimal	Oscillator FCLK = 4.000000 MHz Register Value Decimal	Oscillator FCLK = 4.000000 MHz Actual Frequency (Hz)
DTMF Row	697 770 852 941	0140 0122 0106 00ED	320 290 262 237	697 769 851 940	0166 0144 0124 0109	358 324 292 265	696 769 853 940
DTMF Column	1209 1336 1477 1633	00B8 00A6 0096 0088	184 166 150 136	1209 1340 1482 1633	00CE 00BA 00AB 0098	206 186 168 152	1208 1337 1479 1634
Subscriber Tones	350 440 480 620	027E 01FB 01D1 0168	638 507 465 360	350 440 480 620	02C9 0237 0208 0192	713 567 520 402	350 440 480 620
US 110, 300 Baud Modem	1070 1270 2025 2225	00D0 00AF 006D 0064	208 175 109 100	1070 1271 2034 2215	00E9 00C4 007A 006F	233 196 122 111	1068 1269 2033 2232
European 110, 300 Baud Modem	980 1180 1650 1850	00E3 00BD 0087 0078	227 189 135 120	981 1177 1645 1849	00FE 00D3 0097 0086	254 211 151 134	980 1179 1645 1832
Teletext	390 450 1300 2100	023D 01F0 00AB 006A	573 496 171 106	390 450 1301 2091	0280 022B 00BF 0076	640 555 191 118	390 450 1302 2101
US 1200 Baud Modem	390 450 1200 2200	023D 01F0 00B9 0065	573 496 185 101	390 450 1203 2193	0280 022B 00CF 0071	640 555 207 113	390 450 1202 2193

1.12 Processor Defined Cache ControlT

The Processor Defined Cache Control allows the W65C265S to slow its clock rate. The idea of cache with the W65C265S is that all memory running at the FCLK rate is cache memory. When slower memories are addressed, the PHI2 clock rate is slowed. PHI2 is slowed by extending the PHI2 low and high times. Whether or not the clock rate is slowed down is determined by the System Speed Control (SSCR) Register.

7	6	5	4	3	2	1	0	SSCRx ($DF41)

Bit 0: FCLK Start and Stop Control
0 = Stop FCLK
1 = Start FCLK

Bit 1: PHI2 System Timing Clock Select
0 = PHI2 Clock source is CLK
1 = PHI2 Clock source is FCLK/4 or FCLK

Bit 2: External RAM Select
0 = Internal RAM (00)0000-01FF
1 = External RAM (00)0000-01FF

Bit 3: System (CS0B-CS7B Speed Select
0 = Slow (FCLK/4)
1 = Fast (FCLK)

Bit 4: CS4B Speed Select
0 = Slow
1 = Fast

Bit 5: CS5B Speed Select
0 = Slow
1 = Fast

Bit 6: CS6B Speed Select
0 = Slow
1 = Fast

Bit 7: CS7B Speed Select
0 = Slow
1 = Fast

Figure 1-14 System Speed Control Register (SSCR)

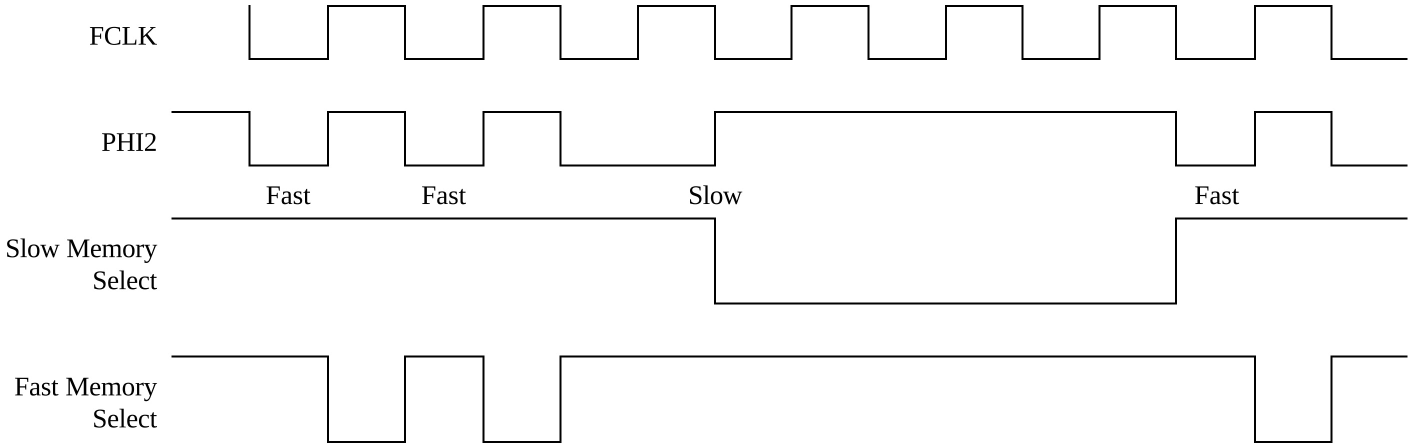


Figure 1-15 System Speed Change Timing Diagram

1.13 Programming Model and Memory Map

The W65C816S Microprocessor Programming Model, System Memory Map, I/O Memory Map, Vector Table, and Pin Map summarize the W65C265S Programming Model and gives the functional area where each memory and pin is defined.

The W65C265S completely decodes the entire 16 Mbyte address space of the on-chip W65C816S microprocessor. The System Memory Map is shown in Table 1-5. The on-chip I/O, Timers, Control Registers, Shift Registers, Interrupt Registers, and Data Registers are presented in Table 1-6A through 1-6D, I/O Memory Map, Control and Status Register Memory Map, Timer Register Memory May, and Communication Memory Map. The W65C265S has twenty-nine (29) priority encoded interrupts whose vector addresses are listed in Table 1-7A and B, Vector Table.

8 BITS	8 BITS	8 BITS
Data Bank Register (DBR)	X Register (XH)	X Register (XL)
Data Bank Register (DBR)	Y Register (YH)	Y Register (YL)
00	Stack Register (SH)	Stack Register (SL)
	Accumulator (B)	Accumulator (A)
Program Bank Register (PBR)	Program (PCH)	Counter (PCL)
00	Direct Register (DH)	Direct Register (DL)

Shaded blocks = 6502 registers

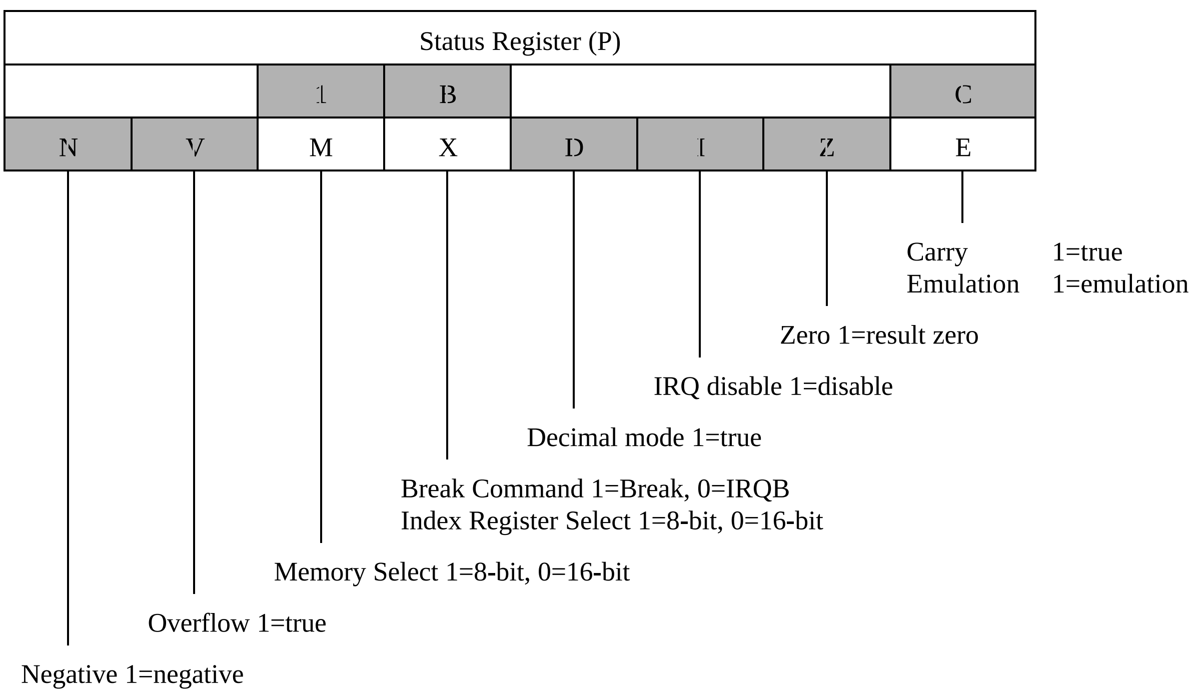


Figure 1-16 W65C816S Programming Model and Memory Map

Table 1-5 System Memory Map

Chip Select	Block Size	Address Range	Function
CS7B	4M	(C0-FF)	User Memory
CS6B	8M	(40-BF)	User Memory
CS5B	4M	(00-3F)	Memory (Note 2)
CS4B	8192 24320	(00)E000-FFFF (00)8000-DEFF	ROM Memory (Note 1) ROM Memory (Note 1)
CS3B	32256	(00)0200-7FFF	Cache Memory (Note 3)
CS2B	256 7936 64 16 32 16 8 8 512	(00)FF00-FFFF (00)E000-FEFF (00)DF80-DFBF (00)DF70-FF7F (00)DF50-FF6F (00)DF40-FF4F (00)DF20-DF27 (00)DF00-DF07 (00)0000-01FF	On-chip Interrupt Vectors On-chip ROM On-chip RAM On-chip Comm. Registers On-chip Timer Registers On-chip Control Registers On-chip I/O Registers On-chip I/O Registers On-chip RAM
CS1B	64	(00)DFC0-DFFF	COProcessor expansion
CS0B	32	(00)DF00-DF1F	Port replacement & Expansion (Note 4)

Note 1. When on-chip 8K bytes of ROM are enabled, addresses (00)E000-FFFF will not appear in CS4B chip select decode. On Chip addresses (00)DF00-DFFF never appear in CS4B or CS5B chip select decode.

Note 2. When on-chip ROM, CS3B and/or CS4B are enabled, then CS5B decode is reduced by the addresses used by same. CS0B and CS1B address space never appears in CS2B, CS4B or CS5B decoded space.

Note 3. When SSCR2 is "0" (internal RAM), then CS3B is active for addresses(00)0200-7FFF. When SSCR2 is "1" (external RAM), then CS3B is active for addresses (00)0000-7FFF.

Note 4. CS0B is inactive when 00DF00-00DF07 are used for internal I/O register select (BCR0=0) when (BCR0=1) external memory bus is enabled CS0B is active for addresses 00DF00-00DF1F.

Table 1-6A I/O Register Memory Map

Address	Label	Function	Reset Value
00DFC0-FF	CS1	COProcessor Expansion	uninitialized
00DF28-3F	---	Reserved	uninitialized
00DF27	PCS7	Port 7 Chip Select	$00
00DF26	PDD6	Port 6 Data Direction Register	$00
00DF25	PDD5	Post 5 Data Direction Register	$00
00DF24	PDD4	Port 4 Data Direction Register	$00
00DF23	PD7	Port 7 Data Register	$FF
00DF22	PD6	Port 6 Data Register	$00
00DF21	PD5	Port 5 Data Register	$00
00DF20	PD4	Port 4 Data Register	$00
00DF00-1F	CS0	Port Replacement & Expansion	uninitialized
00DF07	PDD3	Port 3 Data Direction Register	$00
00DF06	PDD2	Port 2 Data Direction Register	$00
00DF05	PDD1	Port 1 Data Direction Register	$00
00DF04	PDD0	Port 0 Data Direction Register	$00
00DF03	PD3	Port 3 Data Register	$00
00DF02	PD2	Port 2 Data Register	$00
00DF01	PD1	Port 1 Data Register	$00
00DF00	PD0	Port 0 Data Register	$00

Table 1-6B Control and Status Register Memory Map

Address	Label	Function	Reset Value
00DF4A-4F	---	Reserved	uninitialized
00DF49	UIER	UART Interrupt Enable Register	$00
00DF48	UIFR	UART Interrupt Flag Register	$00
00DF47	EIER	Edge Interrupt Enable Register	$00
00DF46	TIER	Timer Interrupt Enable Register	$00
00DF45	EIFR	Edge Interrupt Flag Register	$00
00DF44	TIFR	Timer Interrupt Flag Register	$00
00DF43	TER	Timer Enable Register	$00
00DF42	TCR	Timer Control Register	$00
00DF41	SSCR	System Speed Control Register	$00
00DF40	BCR	Bus Control Register	$00/$89

Table 1-6C Timer Register Memory Map

Address	Label	Function	Reset Value
00DF6F	T7CH	Timer 7 Counter High	uninitialized
00DF6E	T7CL	Timer 7 Counter Low	uninitialized
00DF6D	T6CH	Timer 6 Counter High	uninitialized
00DF6C	T6CL	Timer 6 Counter Low	uninitialized
00DF6B	T5CH	Timer 5 Counter High	uninitialized
00DF6A	T5CL	Timer 5 Counter Low	uninitialized
00DF69	T4CH	Timer 4 Counter High	uninitialized
00DF68	T4CL	Timer 4 Counter Low	uninitialized
00DF67	T3CH	Timer 3 Counter High	uninitialized
00DF66	T3CL	Timer 3 Counter Low	uninitialized
00DF65	T2CH	Timer 2 Counter High	uninitialized
00DF64	T2CL	Timer 2 Counter Low	uninitialized
00DF63	T1CH	Timer 1 Counter High	uninitialized
00DF62	T1CL	Timer 1 Counter Low	uninitialized
00DF61	T0CH	Timer 0 Counter High	uninitialized
00DF60	T0CL	Timer 0 Counter Low	uninitialized
00DF5F	T7LH	Timer 7 Latch High	uninitialized
00DF5E	T7LL	Timer 7 Latch Low	uninitialized
00DF5D	T6LH	Timer 6 Latch High	uninitialized
00DF5C	T6LL	Timer 6 Latch Low	uninitialized
00DF5B	T5LH	Timer 5 Latch High	uninitialized
00DF5A	T5LL	Timer 5 Latch Low	uninitialized
00DF59	T4LH	Timer 4 Latch High	uninitialized
00DF58	T4LL	Timer 4 Latch Low	uninitialized
00DF57	T3LH	Timer 3 Latch High	uninitialized
00DF56	T3LL	Timer 3 Latch Low	uninitialized
00DF55	T2LH	Timer 2 Latch High	uninitialized
00DF54	T2LL	Timer 2 Latch Low	uninitialized
00DF53	T1LH	Timer 1 Latch High	uninitialized
00DF52	T1LL	Timer 1 Latch Low	uninitialized
00DF51	T0LH	Timer 0 Latch High	uninitialized
00DF50	T0LL	Timer 0 Latch Low	uninitialized

Table 1-6D Communication Register Memory Map

Address	Label	Function	Reset Value
00DF80-BF	RAM	RAM Registers	uninitialized
00DF7F	PIR7	Parallel Interface Register 7	uninitialized
00DF7E	PIR6	Parallel Interface Register 6	uninitialized
00DF7D	PIR5	Parallel Interface Register 5	uninitialized
00DF7C	PIR4	Parallel Interface Register 4	uninitialized
00DF7B	PIR3	Parallel Interface Register 3	uninitialized
00DF7A	PIR2	Parallel Interface Register 2	uninitialized
00DF79	PIBER	Parallel Interface Enable Register	$00
00DF78	PIBFR	Parallel Interface Flag Register	$00
00DF77	ARTD3	UART 3 Data Register	uninitialized
00DF76	ACSR3	UART 3 Control/Status Register	$00
00DF75	ARTD2	UART 2 Data Register	uninitialized
00DF74	ACSR2	UART 2 Control/Status Register	$00
00DF73	ARTD1	UART 1 Data Register	uninitialized
00DF72	ACSR1	UART 1 Control/Status Register	$00
00DF71	ARTD0	UART 0 Data Register	uninitialized
00DF70	ACSRO	UART 0 Control/Status Register	$00

Table 1-7A Emulation Mode Vector Table

Address	Label	Function
00FFFE,F	IRQBRK	BRK - Software Interrupt
00FFFC,D	IRQRES	RES - "REStart" Interrupt
00FFFA,B	IRQNMI	Non-Maskable Interrupt
00FFF8,9	IABORT	ABORT Interrupt
00FFF6,7	IRQRVD	Reserved
00FFF4,5	IRQCOP	COP Software Interrupt
00FFF2,3	IRQRVD	Reserved
00FFF0,1	IRQRVD	Reserved
00FFEE,F	IRQAT3	UART3 Transmitter Interrupt
00FFEC,D	IRQAR3	UART3 Receiver Interrupt
00FFEA,B	IRQAT2	UART2 Transmitter Interrupt
00FFE8,9	IRQAR2	UART2 Receiver Interrupt
00FFE6,7	IRQAT1	UART1 Transmitter Interrupt
00FFE4,5	IRQAR1	UART1 Receiver Interrupt
00FFE2,3	IRQAT0	UART0 Transmitter Interrupt
00FFE0,1	IRQAR0	UART0 Receiver Interrupt
00FFDE,F	IRQ	IRQ Level Interrupt
00FFDC,D	IRQPIB	Parallel Interface Bus (PIB) Interrupt
00FFDA,B	IRNE66	Negative Edge Interrupt on P66
00FFD8,9	IRNE64	Negative Edge Interrupt on P64
00FFD6,7	IRPE62	Positive Edge Interrupt on P62 for PWM
00FFD4,5	IRPE60	Positive Edge Interrupt on P60
00FFD2,3	IRNE57	Negative Edge Interrupt on P57
00FFD0,1	IRPE56	Positive Edge Interrupt on P56
00FFCE,F	IRQT7	Timer 7 Interrupt
00FFCC,D	IRQT6	Timer 6 Interrupt
00FFCA,B	IRQT5	Timer 5 Interrupt
00FFC8,9	IRQT4	Timer 4 Interrupt
00FFC6,7	IRQT3	Timer 3 Interrupt
00FFC4,5	IRQT2	Timer 2 Interrupt
00FFC2,3	IRQT1	Timer 1 Interrupt
00FFC0,1	IRQT0	Timer 0 Interrupt

Table 1-7B Native Mode Vector Table

Address	Label	Function
00FFBE,F	IRQRVD	Reserved
00FFBC,D	IRQRVD	Reserved
00FFBA,B	IRQNMI	Non-Maskable Interrupt
00FFB8,9	IABORT	ABORT Interrupt
00FFB6,7	IRQBRK	BRK Software Interrupt
00FFB4,5	IRQCOP	COP Software Interrupt
00FFB2,3	IRQRVD	COP Software Interrupt
00FFB0,1	IRQRVD	Reserved
00FFAE,F	IRQAT3	UART3 Transmitter Interrupt
00FFAC,D	IRQAR3	UART3 Receiver Interrupt
00FFAA,B	IRQAT2	UART2 Transmitter Interrupt
00FFA8,9	IRQAR2	UART2 Receiver Interrupt
00FFA6,7	IRQAT1	UART1 Transmitter Interrupt
00FFA4,5	IRQAR1	UART1 Receiver Interrupt
00FFA2,3	IRQAT0	UART0 Transmitter Interrupt
00FFA0,1	IRQAR0	UART0 Receiver Interrupt
00FF9E,F	IRQ	IRQ Level Interrupt
00FF9C,D	IRQPIB	Parallel Interface Bus (PIB) Interrupt
00FF9A,B	IRNE66	Negative Edge Interrupt on P66
00FF98,9	IRNE64	Negative Edge Interrupt on P64
00FF96,7	IRPE62	Positive Edge Interrupt on P62 for
00FF94,5	IRPE60	Positive Edge Interrupt on P60
00FF92,3	IRNE57	Negative Edge Interrupt on P57
00FF90,1	IRPE56	Positive Edge Interrupt on P56
00FF8E,F	IRQT7	Timer 7 Interrupt
00FF8C,D	IRQT6	Timer 6 Interrupt
00FF8A,B	IRQT5	Timer 5 Interrupt
00FF88,9	IRQT4	Timer 4 Interrupt
00FF86,7	IRQT3	Timer 3 Interrupt
00FF84,5	IRQT2	Timer 2 Interrupt
00FF82,3	IRQT1	Timer 1 Interrupt
00FF80,1	IRQT0	Timer 0 Interrupt
00FF00-7F	IRQRVD	Reserved

Table 1-8A W65C265S 84 Lead Pin Map (continued on next 3 pages)

Pin	Name	Control Bit	Signal with Control Bit=0	Signal with Control Bit=1
1	VSS	---	VSS	VSS
2	P56	EIER0	P56	PE56
	PID6	PIBER0		PID6
3	P57	EIER1	P57	NE57
	PID7	PIBER0		PID7
4	P60	ACSR05	P60	RXD0
	TIN	TCR1		TIN
	PE60	EIER02	P60	PE60
5	P61	ACSR00	P61	TXD0
	TOUT	TCR0		TOUT
6	P62	ACSR15	P62	RXD1
	PWM	TCR2+TCR3		PWM
7	P63	ACSR10	P63	TXD1
	TOUT			
8	P64	ACSR25	P64	RXD2
	NE64	EIER4	P64	NE64
9	P65	ACSR20	P65	TXD2
10	P66	ACSR35	P66	RXD3
	NE66	EIER5	P66	NE66
11	P67	ACSR30	P67	TXD3
12	RESB	---	RESB	RESB
13	WEB	---	WEB	WEB
14	RUN	BCR3	RUN	RUN
15	FCLKOB	---	FCLKOB	FCLKOB
16	FCLK	---	FCLK	FCLK
17	BE	---	BE	BE
18	CLK	---	CLK	CLK
19	CLKOB	---	CLKOB	CLKOB
20	PHI2	---	PHI2	PHI2
21	BA	BCR3	BA/1	BA
22	VSS	---	VSS	VSS
23	VDD	---	VDD	VDD
24	A0	BCR0	P00	A0

25	A1	BCR0	P01	A1
26	A2	BCR0	P02	A2
27	A3	BCRO	PO3	A3
28	A4	BCR0	P04	A4
29	A5	BCR0	P05	A5
30	A6	BCR0	P06	A6
31	A7	BCR0	P07	A7
32	A8	BCR0	P10	A8
33	A9	BCR0	P11	A9
34	A10	BCR0	P12	A10
35	A11	BCR0	P13	A11
36	A12	BCR0	P14	A12
37	A13	BCR0	P15	A13
38	A14	BCR0	P16	A14
39	A15	BCR0	P17	A15
40	A16	BCR0	P30	A16
41	A17	BCR0	P31	A17
42	A18	BCR0	P32	A18
43	VSS	---	VSS	VSS
44	VDD	---	VDD	VDD
45	A19	BCR0	P33	A19
46	A20	BCR0	P34	A20
47	A21	BCR0	P35	A21
48	A22	BCR0	P36	A22
49	A23	BCR0	P37	A23
50	P70	PCS70	P70	CS0B
51	P71	PCS71	P71	CS1B
52	P72	PCS72	P72	CS2B
53	P73	PCS73	P73	CS3B
54	P74	PCS74	P74	CS4B
55	P75	PCS75	P75	CS5B
56	P76	PCS76	P76	CS6B
57	P77	PCS77	P77	CS7B
58	D0	BCR0	P20	D0

59	D1	BCR0	P21	D1
60	D2	BCR0	P22	D2
61	D3	BCR0	P23	D3
62	D4	BCR0	P24	D4
63	VDD	---	VDD	VDD
64	VSS	---	VSS	VSS
65	D5	BCR0	P25	D5
66	D6	BCR0	P26	D6
67	D7	BCR0	P27	D7
68	TG0	TCR31	---	TG0
69	TG1	TCR33	---	TG1
70	P40	BCR5 · BCR6	P40	NMIB
	ABORTB	BCR5 · BCR6B		ABORTB
71	P41	EIER3	P41	IRQB
72	P42	PIBER0	P42	PIIB
73	P43	PIBER0 · PIBER1B	P43	PIWEB
	PIWRB	PIBER0 · PIBER1		PIWRB
74	P44	PIBER0 · PIBER1B	P44	PICSB
	PIRDB	PIBER0 · PIBER1		PIRDB
75	P45	PIBER0	P45	PIRS0
76	P46	PIBER0	P46	PIRS1
77	P47	PIBER0	P47	PIRS2
78	P50	PIBER0	P50	PID0
79	P51	PIBER0	P51	PID1
80	P52	PIBER0	P52	PID2
81	P53	PIBER0	P53	PID3
82	P54	PIBER0	P54	PID4
83	P55	PIBER0	P55	PID5
84	VDD	---	VDD	VDD

SECTION 2

PIN FUNCTION DESCRIPTION

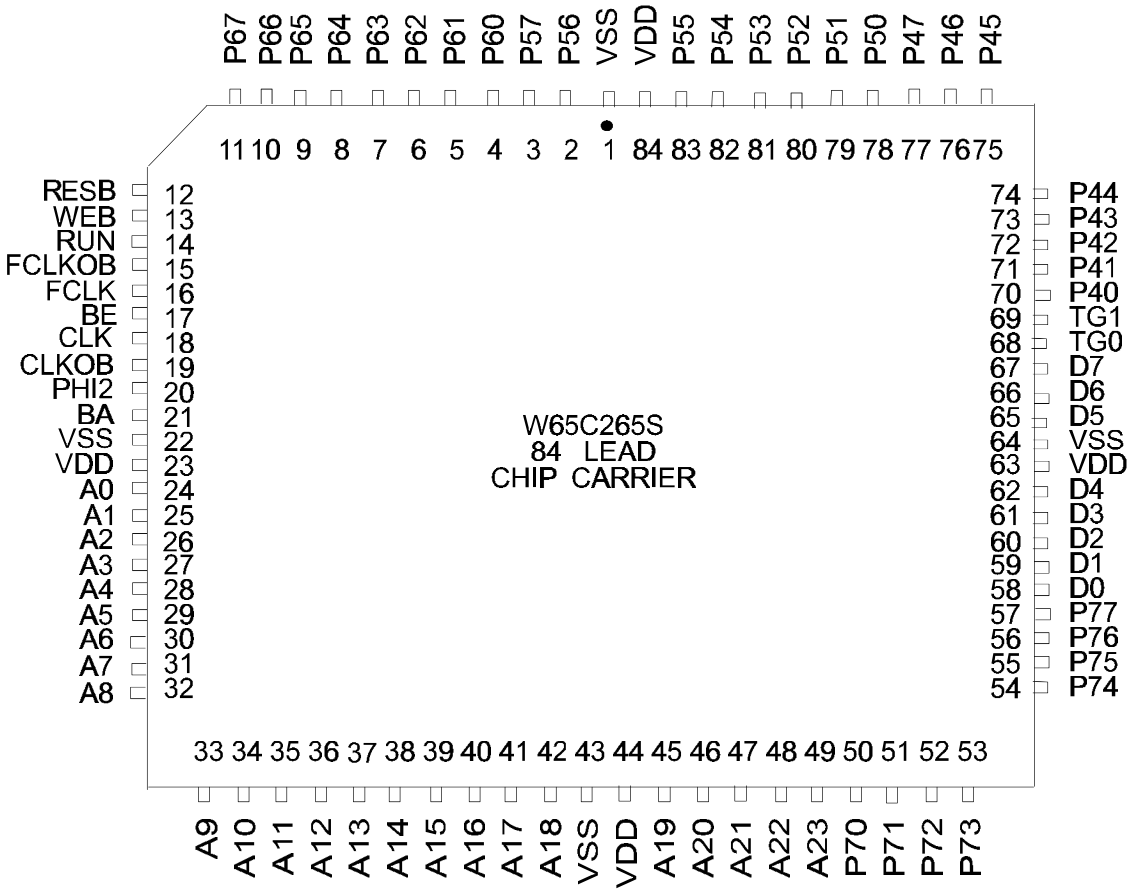
W65C265S Interface Requirements

This section describes the interface requirements for the W65C265S single chip microcomputer. Figure 2-1 is the Interface Diagram for the W65C265S and Figure 2-2 shows the 84 Lead Chip Carrier pin out configuration.

		W65C816S Static CPU	Port 0	<8>	P0x/Axx
		576 X 8 RAM	Port 1	<8>	P1x/Axx
VDD (4) RESB	⇒ ⇔	8192 X 8 ROM	Port 2	<8>	P2x/Dx
WEB RUN FCLKOB	⇔ ⇐ ⇐	Interrupt Registers & Logic	Port 3	<8>	P3x/Axx
FCLK BE CLK	⇒ ⇒ ⇒	Control Registers & Logic	Port 4	<8>	P4x/NMIB/ABORTB/IRQB/ PIB Control
CLKOB PHI2	⇐ ⇐	Clock Logic	Port 5	<8>	P5x/PE56/NE57/PIB data
VSS (4) BA	⇒ ⇐	8x16 bit Timers	Port 6	<8>	P6x/UARTx/TIN/TOUT/ PWM/PExx/NExx
		4 UART's	Port 7	8>	P7x/CSxB
		PIB	2 Tone Generators	2>	TGx

Figure 2-1 W65C265S Interface Diagram

Figure 2-2 W65C265S 84 Lead Chip Carrier Pinout



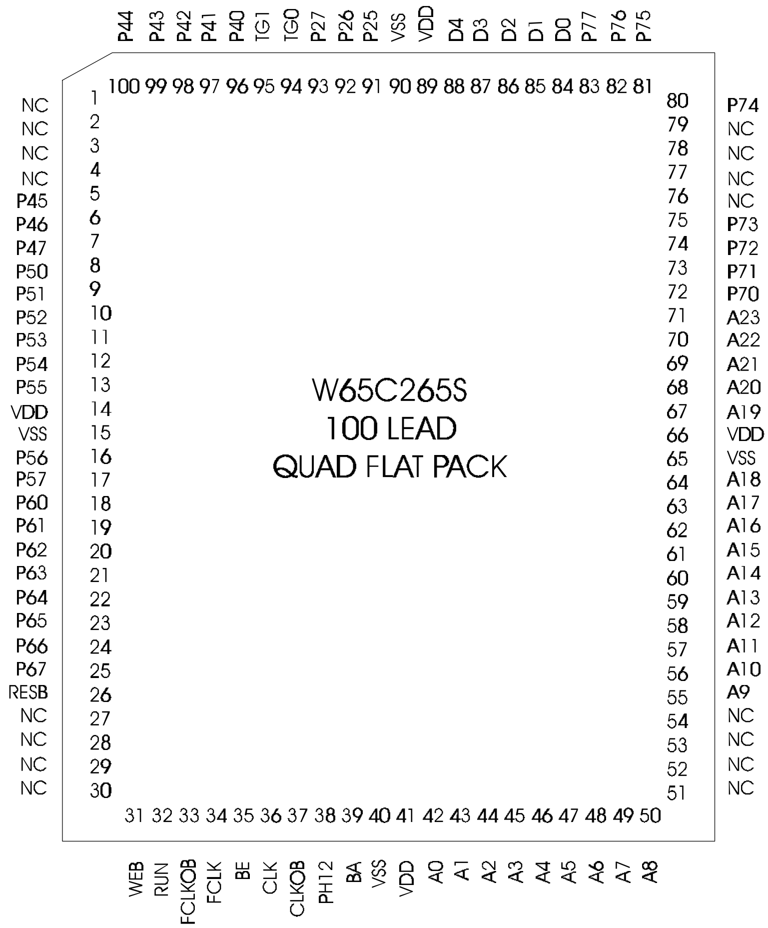


Figure 2-3 W65C265S 100 Lead Quad Flat Pack Pinout

2.1 Write Enable (active low) (WEB)

The WEB signal is high when the microprocessor is reading data from external memory or I/O and high when it is reading or writing to internal memory or I/O. When WEB is low the microprocessor is writing to external memory or external I/O. The WEB signal is bi-directional; when BE is low this is an input for DMA operations to on-chip RAM or I/O. When BE is high the internal microprocessor controls WEB.

2.2 RUN and SYNC outputs with WAI and STP defined (RUN)

2.2.1 The RUN function of the RUN output is pulled low as the result of a WAI or STP instruction. RUN is used to signal an external oscillator to start PHI2. The processor is stopped when RUN is low.

2.2.2 When BCR3=1 (emulation mode), the SYNC function (SYNC=1 indicates an opcode fetch) is multiplexed on RUN during PHI2 low time and RUN is multiplexed during PHI2 high time. When BCR3=0 (normal operating mode), the RUN function is output during the entire clock cycle. An ICE system can demultiplex RUN to provide full emulation capability for the RUN function.

2.2.3 The BE input has no effect on RUN.

2.2.4 When RUN goes low the PHI2 signal may be stopped when high or low; however, it is recommended PHI2 stop in the high state. When RUN goes high due to an enabled interrupt or reset, the internal PHI2 clock is requested to start. The clock control function is referred to as the RUN function of RUN.

2.2.5 The WAI instruction pulls RUN low during PHI2 high time. RUN stays low until an enabled interrupt is requested or until RESB goes from low to high, starting the microprocessor.

2.2.6 The STP instruction pulls RUN low during PHI2 high time and stops the internal PHI2 clock. RUN remains low and the clock remains stopped until RESB goes from low to high.

2.2.7 FCLK can be started or stopped by writing to System Speed Control Register (SSCR) bit 0. When SSCR0=0 (reset forces SSCR0=0), FCLK is stopped. When SSCR0=1, FCLK is started. When starting FCLK oscillator, the system software should wait (100 milliseconds or an appropriate amount of time) for the oscillator to be stable before using FCLK.

2.3 Phase 2 Clock Output (PHI2)

PHI2 output is the main system clock used by the microprocessor for instruction timing, general on-chip memory, and I/O timing. PHI2 also is used by the timers when enabled for counting PHI2 clock pulse. The PHI2 clock source is either CLK or FCLK depending on the value of System Speed Control Register bit 1 (SSCR1). When SSCR1=0, then CLK is the PHI2 clock source. When SSCR1=1, then FCLK is the PHI2 clock source.

2.4 Clock Inputs (CLKOB, FCLKOB Outputs) (CLK. FCLK)

CLK and FCLK inputs are used by the timers, for PHI2 system clock generation, counting events or implementing Real Time clock type functions. CLK should always be equal to or less than one-fourth the FCLK clock rate when FCLK is running (see the timer description for more information). CLKOB, FCLKOB outputs are the inverted CLK and FCLK inputs that are used for oscillator circuits that employ crystals or a resistor-capacitor time base.

2.5 Bus Enable and RDY Input (BE)

2.5.1 BE controls the address bus, data bus and WEB signals. When RESB goes high signaling in the power-up condition, the processor starts; and if BE was low when RESB went from low to high then the Bus Control Register (BCR) bits 0, 3, and 7 (BCR0, BCR3, and BCR7) are set to 1 (emulation mode). See Figure 1-1.

2.5.2 After RESB goes high BE controls the direction of the address bus (A0-A7, A8-A15, A16-A23), data bus (D0-D7) and WEB.

2.5.3 When BE goes low during PHI2 low time, the address bus and WEB are inputs, providing for DMA (direct memory and I/O access) for emulation purposes. Data from D0-D7 is written to any register addressed by A0-A15 when WEB is low. Data is read from D0-D7 when WEB is high. The W65C816S is stopped when BE is low, during PHI2 high time.

2.5.4 When BE is high, the A0-A15, D0-D7 and WEB are controlled by the on-chip microprocessor.

2.5.5 When BE is pulled low during PHI2 high time, BE does not affect the direction of the address, data BUS and WEB signals. When BE is pulled low in PHI2 high time, the W65C816S is stopped so that the processor may be single stepped in emulation.

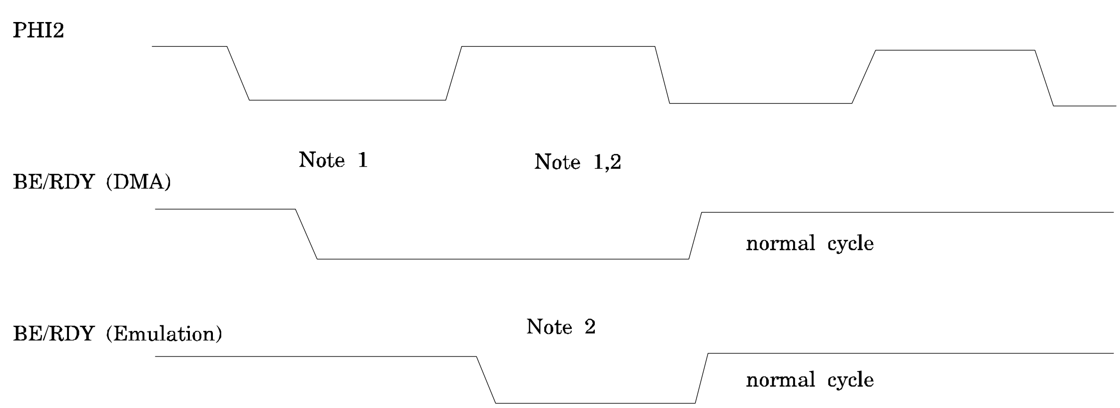


Figure 2-5 BE Timing Relative to PHI2

BE = BE · (RDY + PHI2B)

Notes:

1) Address and WEB are inputs with data bus input except when reading on-chip I/O registers or memory. Use this mode for DMA.

2) W65C816S stopped with RDY function of BE pin. When BCR3=1, the W65C816S read or write of internal I/O register or memory is output on the external data bus so that the internal data bus may be traced in emulation.

2.6 Reset Input/Output (active low) (RESB)

2.6.1 When RESB is low for 2 or more processor PHI2 cycles all activity on the chip stops and the chip goes into the static low power state.

2.6.2 After a Reset, all I/O pins become inputs. Because of NOR gates on the inputs, RESB disables all input buffers. The inputs will not float due to the bus holding devices while RESB is low. Inputs that are unaffected by RESB are BE and WEB.

2.6.3 When RESB goes from low to high, RUN goes high, the Bus Control Register is initialized to $89 if BE is low or to $00 if BE is high. The MPU then begins the power-up reset interrupt sequence in which the program counter is loaded with the reset vector that points to the first instruction to be executed. (See WDC's W65C816S microprocessor data sheet for more information and instruction timing.)

2.6.4 The reset sequence takes 9 cycles to complete before loading the first instruction opcode.

2.6.5 RESB is a bidirectional pin which is pulled low internally for "restarting" due to a "monitor time out", Timer M times out causing a system Reset. (See section 1.5, The Timers for more information.)

2.7 Positive Power Supply (VDD)

VDD is the positive power supply and has a range of 2.8V to 5.5V for use in a wide range of applications.

2.8 Internal Logic Ground (VSS)

VSS is the system logic ground. All voltages are referenced to this supply pin.

2.9 I/O Port Pins (Pxx)

2.9.1 All ports, except Port 7, which is an output Port, are bidirectional I/O ports. Each of these bidirectional Ports has a port data register (PDx) and port data direction register (PDDx). A zero ("0") in PDDxx defines the associated I/O pin as an input with the output transistors in the "off" high impedance state. A one ("1") in PDDxx defines the I/O pin as an output. A read of PDx always "reads" the pin. After reset, all Port pins become input pins with both the data and data direction registers reset to 0.

2.9.2 Port 7 has a Chip Select register (PCS) that is used to enable Chip Selects (CSxB). A "1" in bit x of PCSx enables Chip Select CSx- to be output over P7x while a "0" in PCSx specifies the value in the output data register is to be output on P7x. Port 7 data register is set to all "1's" after Reset, and PCS is cleared to all "0's" after Reset.

2.10 Address Bus (Axx)

Ports 0, 1, and 3 are also the address bus A0-A23 when configured by the Bus Control Register (BCR). When BCR0 and BCR7 are set to "1" and BCR3=0 (normal operating mode) for external memory addressing, Axx are all "1's" when addressing on-chip memory. When BCR3=1 (emulation mode), the address bus is always active so that an emulator can trace internal read and write operations.

2.11 Data Bus (Dx)

Port 2 is the data bus D0-D7 when configured by the Bus Control Register (BCR). (See section 1.4 for BCR mode selection.) When BCR0 and BCR7 are set to a "1" and BCR3=0 (normal operating mode) for external memory addressing, Dx are all "1's" when addressing on-chip memory. When BCR3=1 (emulation mode), the data bus is always active so that an emulator can trace internal read and write operations. During external memory cycles the data bus is in the Hi-Z state during PHI2 low time.

2.12 Positive Edge Interrupt inputs (PExx)

Port pin P56, P60 and P62 have Positive Edge sensitive interrupt inputs (PE56,PE60,PWM) multiplexed with the I/O. The associated bit is set (by an internal one-shot circuit) in the Interrupt Flag Register (IFRx) on a positive transition from "0" to "1". The transition from "1" to "0" has no effect on the IFR. When the associated Interrupt Enable Register bit (IERx) is set to a "1", the MPU will be interrupted provided the interrupt flag bit in the MPU status register P (I flag) is cleared to a "0". When the I flag is "1", interrupts are disabled.

2.13 Negative Edge Interrupt inputs (NExx)

Port pin P57, P62, P64 and P66 have Negative Edge sensitive interrupt inputs (NE57,PWM,NE64,NE66) multiplexed with the I/O. The associated bit is set (by an internal one-shot circuit) in the Interrupt Flag Register (IFRx) on a negative transition from "1" to "0". The transition from "0" to "1" has no effect on the IFR. When the associated Interrupt Enable Register bit (IERx) is set to a "1", the MPU will be interrupted provided the interrupt flag bit in the MPU status register P (I flag) is cleared to a "0". When the I flag is a "1", interrupts are disabled.

2.14 Chip Select outputs (active low) (CSxB)

The CSxB Chip Select outputs are enabled (individually) as outputs on Port 7 with the PCS register. Each of the eight chip selects is dedicated to one block of external memory defined by the programmable chip select registers; the mapping of each chip select to external addresses is given in Table 1-5, System Memory Map.

2.15 Level Sensitive Interrupt Request input (IRQB)

The I/O function of port pin P41 is multiplexed with IRQB Level Sensitive Interrupt input. When IRQB is held low the Edge Interrupt Flag Register Bit 7 (EIFR7) is set to a "1". When the Edge Interrupt Enable Register bit 7 (EIER7) is set to a "1" the MPU will be interrupted provided the I flag of the MPU is cleared to a "0" allowing interrupts. Unlike the edge interrupts, which do not hold the interrupt bit set, an interrupt will be generated as long as IRQB is low.

2.16 Non-Maskable Edge and ABORT Interrupt Input (NMIB/ABORTB)

The I/O Function of port pin P40 is multiplexed with both the NMIB edge triggered interrupt and the ABORT interrupt. When BCR6=1, the NMIB interrupt is enabled; the MPU will be interrupted on all negative edges of NMIB. Because the I flag cannot prevent NMIB from interrupting, NMIB is thought of as Non-Maskable. When BCR5=1, the ABORT interrupt is enabled. Should both BCR5 and BCR6 be set to "1", both NMIB and ABORT are enabled (normally, this is not desirable).

2.17 Asynchronous Receiver Inputs/Transmitter Outputs (RXDx, TXDx)

The W65C265S has four full duplex Universal Asynchronous Receivers and Transmitters (UARTx) that may be enabled by the Asynchronous Control and Status Registers (ACSRs). When a Receiver is enabled by ACSRx0=1 then port pin P60, P62, P64 or P66 becomes the Asynchronous Receiver Input (RXDx). When a Transmitter is enabled by ACSRx4=1, then port pin P61, P63, P65 or P67 becomes the Asynchronous Transmitter Output (TXDx).

2.18 Timer 4 Input and Output (TIN, TOUT)

Timer 4 is controlled by TCRx and TERx. When the UART is not in use, Timer 4 can be used for counting input negative pulses on TIN. Timer 4 can also be used to put out a square wave or rectangular wave form on TOUT. When counting negative pulses on TIN the TIN frequency should always be less than one-half the frequency of PHI2. TOUT changes state on every time-out of Timer 4; therefore, varying waveform and frequency depends on the timer latch values and may be modified under software control. TIN is multiplexed on P60 and TOUT is multiplexed on P61.

2.19 Bus Available/Disable Output Data (BA)

The BA output indicates the microprocessor is using the internal data and address buses when BA is high. The microprocessor is using the external bus when BA is low, then an external device can use the bus without slowing down processing. BE must be used to gain access to the WEB and address bus. When DODB is low (during PHI2 high) then the microprocessor is writing data to the external data bus. The other devices using the bus should disable their outputs. This signal could be thought of as a valid memory address negative edge for sampling the address bus on the negative edge. When BCR3=1(emulation mode) the DODB function is multiplexed on BA during PHI2 high time and BA is multiplexed during PHI2 low time. When BCR3=0 (normal mode) the BA is output during PHI2 low time and a 1 level is output during PHI2 high time.

2.20 Tone Generator Outputs (TGx)

The Twin Tone Generator outputs (TGx) are synthesized 16 step cosine waveform outputs as described in Section 1.11 Twin Tone Generators.

2.21 Parallel Interface Bus (PIB)

2.21.1 The Parallel Interface Bus (PIB) pins are used to communicate between processors in a "star" network configuration or as a co-processor on a "host" processor bus such as an IBM PC or compatible or an Apple II or Mac II personal computer. This PIB may also be used as part of the file server system for large memory systems.

2.21.2 The Parallel Interface Write Enable (PIWEB) input pin is used with the Parallel Interface Chip Select (low active)/Parallel Interface Chip Select (high active) (PICSB/PICS) signal to transfer data to and from the Parallel Interface Register selected by the Parallel Interface Register select (PIRSx) input pins. When PIWEB and PICSB are configured by the Parallel Interface Bus Enable Register bit 1 (PIBER1=0), then the PIB interface is compatible with WDC microprocessor WE- logical operation with the chip select PICSB input. The use of PIWEB and PICS are configured by PIBER1=1.

2.21.3 The PIB interrupt output to the "host" is generated on the Parallel Interface Interrupt (PII) pin. The "host" interrupt is suggested to be received on the IRQ level interrupt input pin of the "host" processor.

2.22 Pulse Width Measurement Input (PWM)

The Pulse Width Measurement (PWM) input will cause the Timer 7 (T7) counter contents to be transferred to the T7 output latches on the edge(s) selected by the Timer Control Register bits TCR2 and TCR3. The contents of the counter is transferred and an edge interrupt is generated resulting in the EIRF3 being set.

SECTION 3

TIMING, AC AND DC CHARACTERISTICS

3.1 Absolute Maximum Ratings (Note 1)

Table 3-1 Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	VDD	-0.3 to +7.0	V
Input Voltage	VIN	-0.3 to VDD +0.3	V
Storage Temperature	TS	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

3.2 DC Characteristics

VDD = 2.0V to 5.5V (except where noted), VSS = 0V, TA = 0°C to +70°C (except where noted)

Table 3-2 DC Characteristics

	Symbol	Min	Max	Unit
Input High Threshold Voltage CLK, FCLK, RESB, all other inputs	Vih	.9XVDD 0.7XVDD	VDD+0.3 VDD+0.3	V V
Input Low Threshold Voltage CLK, FCLK. RESB, all other inputs	Vil	VSS-0.3 VSS-0.3	.1XVDD .3XVDD	V V
Input Leakage Current (Vin=VSS to VDD, VDD=5.5V) all inputs	Iin	-1	+1	uA
Output High Voltage Ioh=-100uA, VDD=2.8V all outputs	Voh	0.9XVDD	-	V
Output Low Voltage Iol=100uA, VDD-2.8 all outputs	Vol	-	.1XVDD	V
Supply Current (No Load 2.8V and all on-chip 5.5V circuits operating)	Icc	- -	3 6	mA/MHz mA/MHz
Supply Current (No Load) TA=25EC Reset Condition RESB, BE=VSS; CLK=32768 Hz, VDD=5.5V FCLK=HI, PHI2=HI STP Condition CLK=HI, VDD=2.8V FCLK=HI, PHI2=HI Wait for Interrupt Condition CLK=32768 Hz FCLK=HI, VDD=2.8V	Ires Istp Iwai	- - -	5 1 5	uA uA uA
Capacitance (sample tested) (Vin=0, Ta=25EC, f=1MHz) all pins except VSS, VDD	Cin	-	10	pF

3.3 AC Characteristics

Table 3-3 AC Characteristics

Timing Parameter	Definition
tISA	Address input setup from PHI2
tIHA	Address input hold from PHI2
tODA	Address output delay from PHI2
tOHA	Address output hold from PHI2
tISD	Data input setup from PHI2
tIHD	Data input hold from PHI2
tODD	Data output delay from PHI2
tOHD	Data output hold from PHI2
tISB	BE input setup from PHI2
tIHB	BE input hold from PHI2
tODSY	SYNC output delay from PHI2
tISRR	RDY/RESB input setup from PHI2
tIHRR	RDY/RESB input hold from PHI2
tODRN	RUN output delay from PHI2
tOHRN	RUN output hold from PHI2
tISP	Port input setup from PHI2
tIHP	Port input hold from PHI2
tODP	Port output delay from PHI2
tOHP	Port output hold from PHI2
tISI	Interrupt input setup from PHI2
tIHI	Interrupt input hold from PHI2
tISU	UART Data input setup from PHI2
tIHU	UART Data input hold from PHI2
tODU	UART Data output delay from PHI2
tOHU	UART Data output hold from PHI2
tODD (DMA)	Data output delay from PHI2 (ROM read)
tODPH	PHI2 output delay from CLK/FCLK
tODCSR	CS output delay from PHI2 rising
tODCSF	CS output delay from PHI2 falling
tR	FCLK/CLK risetime
tF	FCLK/CLK falltime
tBR	BE to RESB
tBV	BE to D0-7, A0-15, WEB Valid
CEXT	External Capactive load
tCYC	CLK cycle time
tPWL	CLK low time
tPWH	CLK high time
tCYC2	PHI2 cycle time
tPWL2	PHI2 low time
tPWH2	PHI2 high time
tCYCF	FCLK cycle time
tPWLF	FCLK low time
tPWHF	FCLK high time

3.4 AC Parameters

Table 3-4 AC Parameters

Timing Parameter	VDD=2.8V 1 MHz		VDD=5V+/-10% 8MHz		Units
	Min	Max	Min	Max	
tISA	460	-	22	-	nS
tIHA	20	-	20	-	nS
tODA	-	280	-	90	nS
tOHA	20	-	10	-	nS
tISD	270	-	25	-	nS
tIHD	20	-	15	-	nS
tODD	-	330	-	85	nS
tOHD	10	-	0	-	nS
tISB	390	-	85	-	nS
tIHB	20	-	20	-	nS
tODSY	-	270	-	110	nS
tISRR	430	-	55	-	nS
tIHRR	20	-	20	-	nS
tODRN	-	330	-	110	nS
tOHRN	20	-	20	-	nS
tISP	270	-	60	-	nS
tIHP	20	-	20	-	nS
tODP	-	280	-	90	nS
tOHP	20	-	20	-	nS
tISI	80	-	25	-	nS
tIHI	20	-	20	-	nS
tISU	80	-	60	-	nS
tIHU	20	-	20	-	nS
tODU	-	300	-	90	nS
tOHU	10	-	10	-	nS
tODPH	-	200	-	35	nS
tODCSR	0	100	0	50	nS
tODCSF	0	100	0	50	nS
tR	-	25	-	15	nS
tF	-	25	-	15	nS
tBR	200	-	100	-	nS
tBV	-	190	-	30	nS
CEXT	50	-	50	-	pF
tCYC	4000	inf.	1000	-	nS
tPWL	2000	inf.	500	inf.	nS
tPWH	2000	inf.	500	inf.	nS
tCYC2	TCYCF	inf.	TCYCF	inf.	nS
tPWL2	.5*TCYC2	inf.	.5*TCYC2	inf.	nS
tPWH2	.5*TCYC2	inf.	.5*TCYC2	inf.	nS
tCYCF	1000	inf.	250	inf.	nS
tPWLF	500	inf.	125	inf.	nS
tPWHF	500	inf.	125	inf.	nS

3.5 AC Timing Diagram Notes

1. tCYC must always be equal to or greater than four times tCYCF when FCLK is running.

2. Rise and Fall Times for all signals are measured on a sample basis from .3xVDD to .7xVDD.

   The Rise and Fall times are not programmable on the automated test system that is used for production testing. A typical Rise and Fall time is 5-10ns; therefore, the spec indicates the duty cycle of the clock as tested (tPWL=tCYC/2-tF).

   The Rise and Fall times of indicate output Rise and Fall times. The most critical Rise and Fall times are for PHI2 because all timing is related to PHI2.

   The input Rise and Fall times can affect the input setup time (tIS), output delay time (tOD) and hold time (tH). This must be taken into account in an application. At 2MHz and 4MHz, the worst case input Rise and Fall times may prevent a system from working.

3. Hold Time for all inputs and outputs is relative to the associated clock edge.

3.6 AC Timing Diagrams

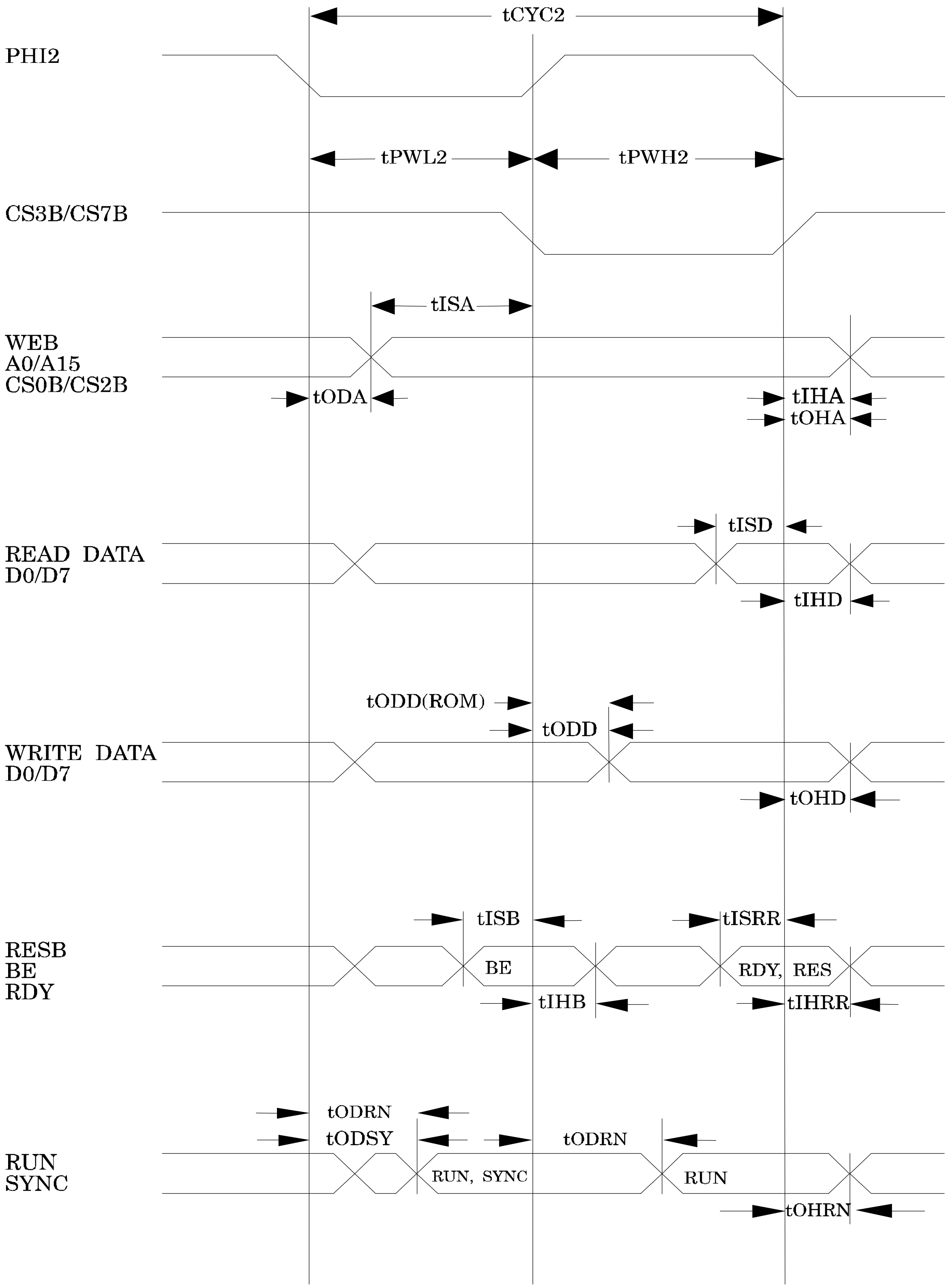
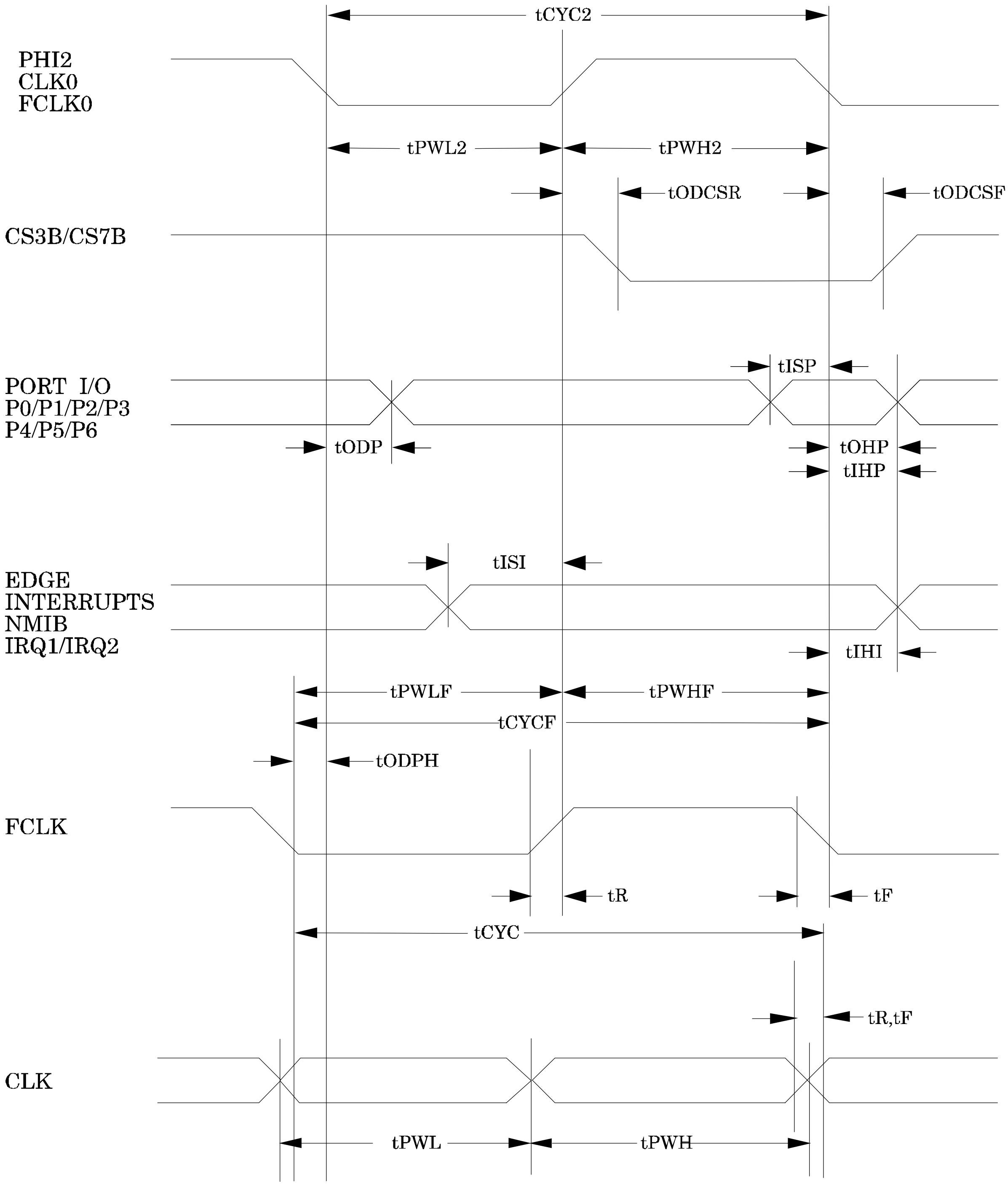


Figure 3-1 AC Timing Diagram #1



Notes:

1. Voltage levels shown are VL = VSS and VH = VDD.
2. Measurement points shown are .5xVDD and .5xVDD.
3. CLK can be asynchronous, tCYC equal or greater than 4xtCYCF.
4. Address and data hold time relative to PHI1 and/or CSxB is 20ns. The PHI2 and CSxB timing is controlled by TCR11. When TCR11=0 PHI12 and CSxB are related to CLK. When TCR11=1, PHI2 and CSxB are related to FCLK.

Figure 3-2 AC Timing Diagram #2

Figure 3-3 AC Timing Diagram #3

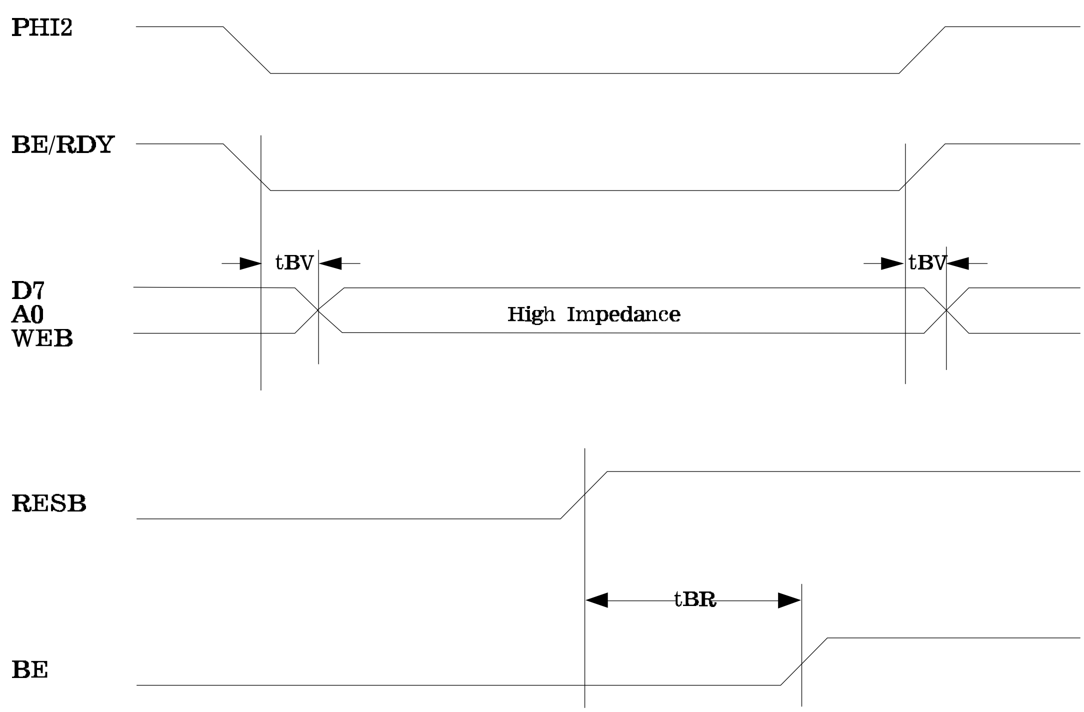
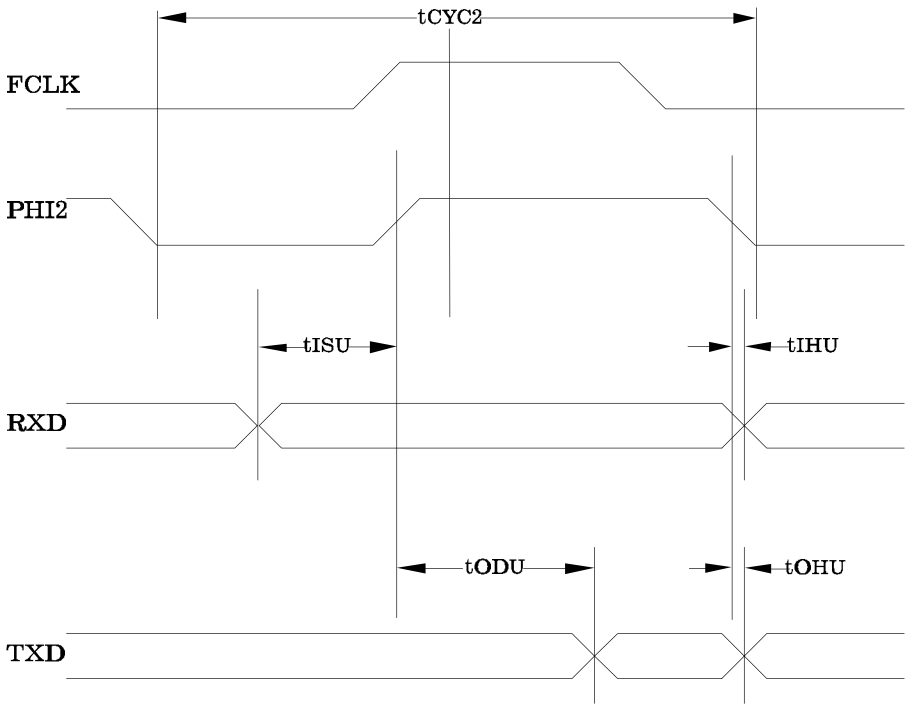


Figure 3-4 AC Timing Diagram #4



SECTION 4

ORDERING INFORMATION

W65C265S8PL-8	
Description W65C = standard product	W65C
Product Identification Number	265S
Foundry Process Blank = 1.2u 8 = .8u	8
Package PL = Plastic Leaded Chip Carrier, 84 pins Q = Quad Flat Pack, 100 pins	PL
Temperature/Processing Blank = 0°C to +70°C	
Speed Designator -8 = 8MHz	-8

To receive general sales or technical support on standard product or information about our module library licenses, contact us at:

The Western Design Center, Inc.
2166 East Brown Road
Mesa, Arizona 85213 USA
Phone: 602-962-4545 Fax: 602-835-6442
e-mail: information@wdesignc.com
WEB: http://www.wdesignc.com

WARNING: MOS CIRCUITS ARE SUBJECT TO DAMAGE FROM STATIC DISCHARGE

Internal static discharge circuits are provided to minimize part damage due to environmental static electrical charge build-ups. Industry established recommendations for handling MOS circuits include:

1. Ship and store product in conductive shipping tubes or conductive foam plastic. Never ship or store product in non-conductive plastic containers or non-conductive plastic foam material.
2. Handle MOS parts only at conductive work stations.
3. Ground all assembly and repair tools.

SECTION 5

APPLICATION INFORMATION

W65C265S Block Diagrams (following pages 51-56)

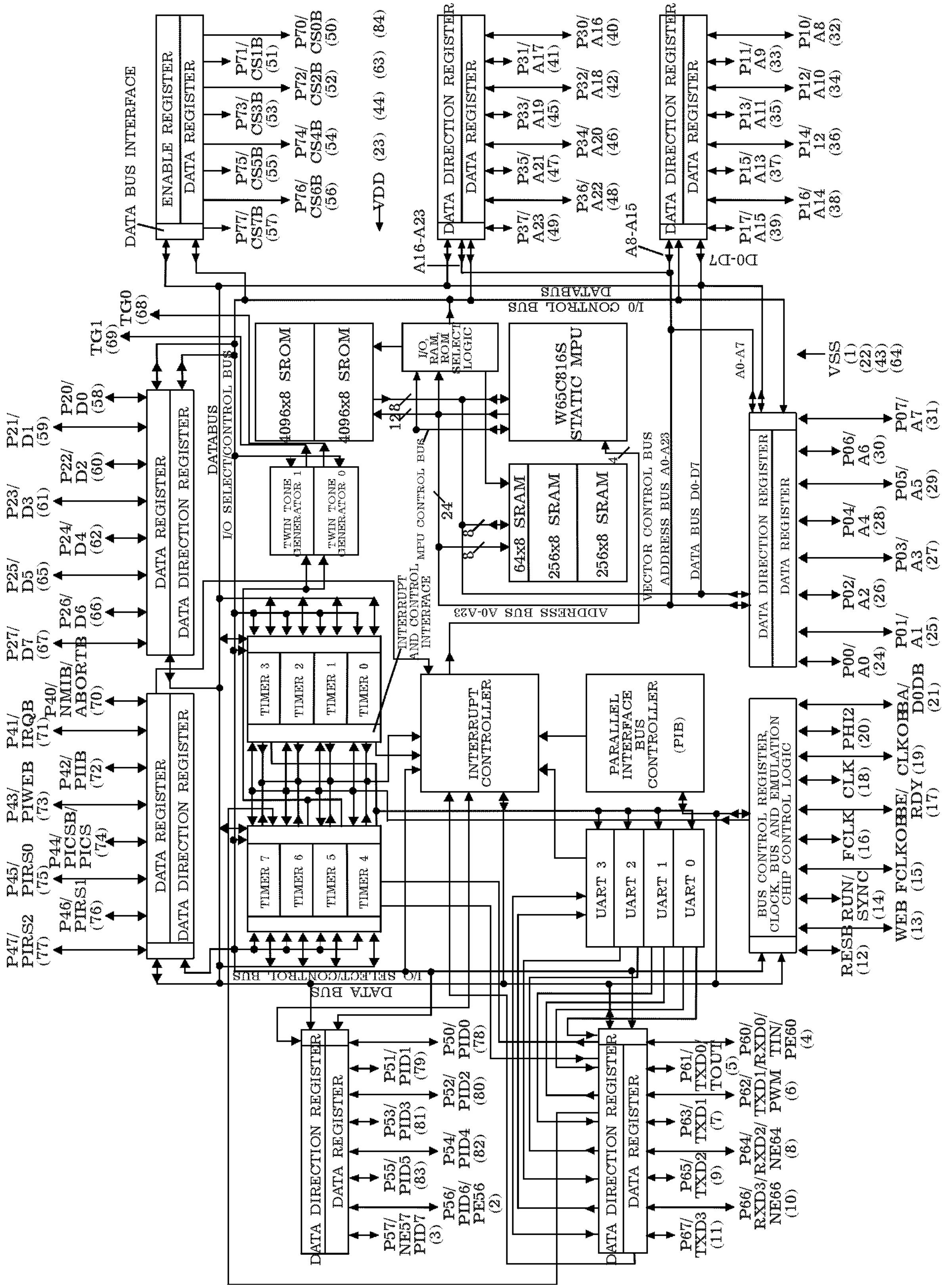


Figure 5-1 W65C265S Block Diagram (Note: Pin numbers apply to PLCC package only.)

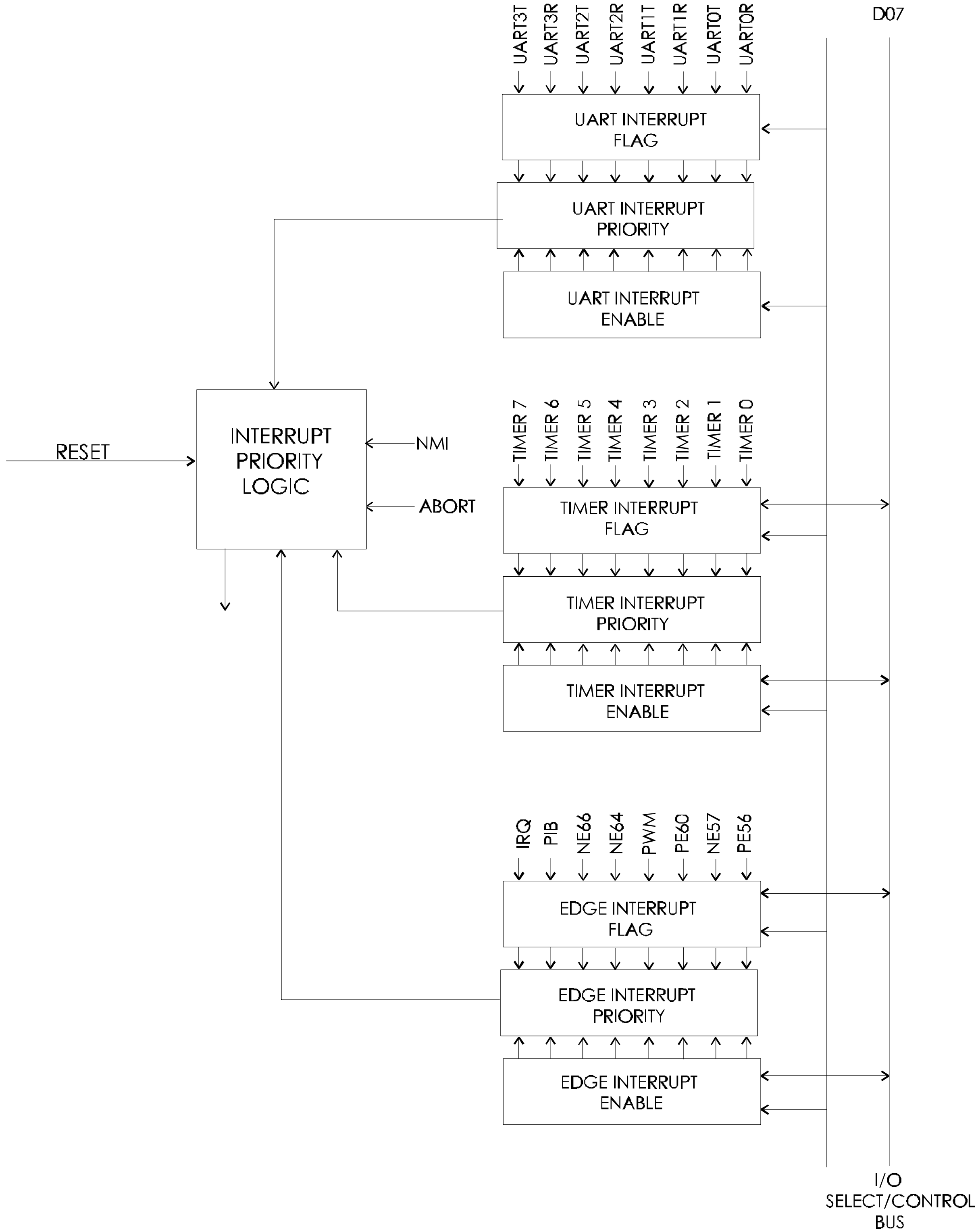


Figure 5-2 W65C265S Interrupt Controller Block Diagram

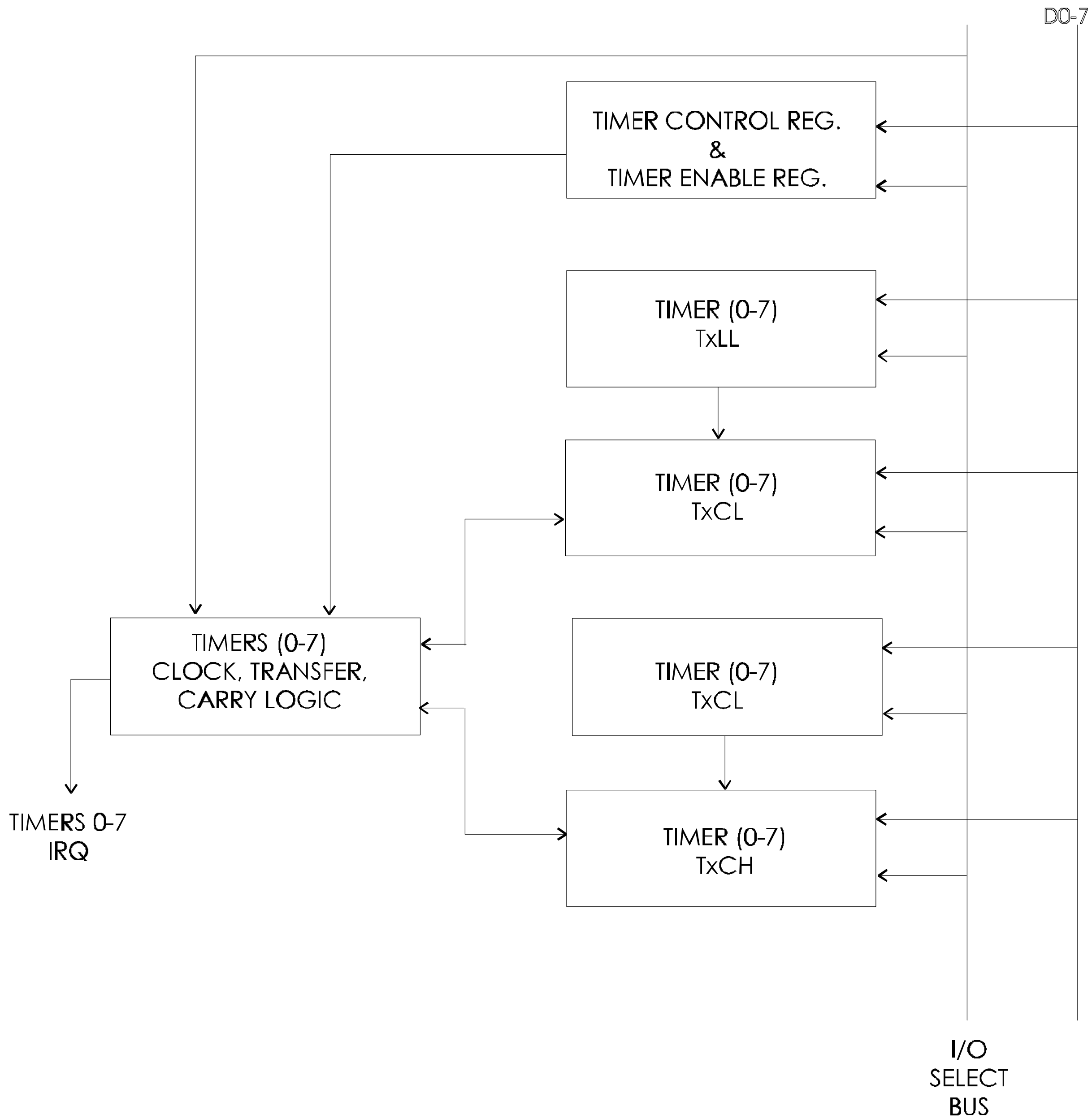


Figure 5-3 W65C265S Timers 0-7 Block Diagram

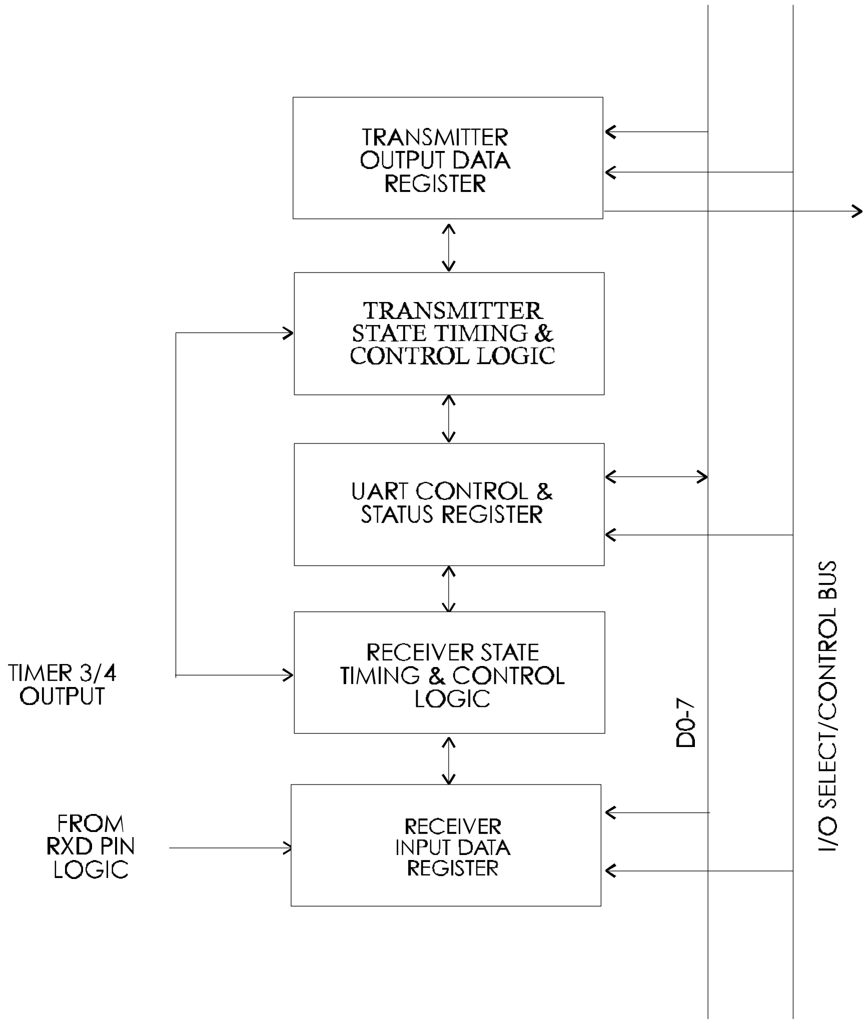
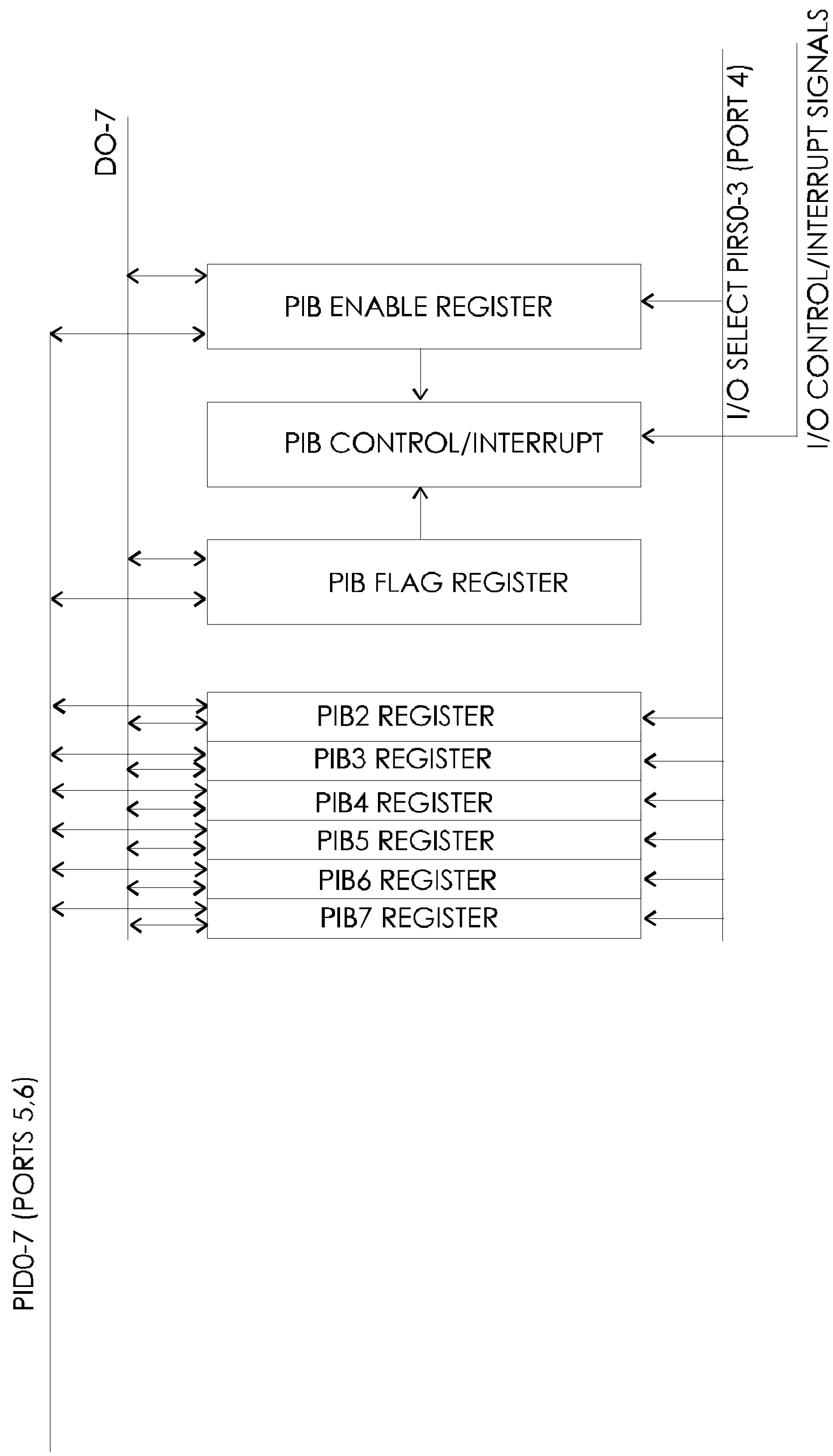


Figure 5-4 W65C265S UART Block Diagram

Figure 5-5 W65C265S Parallel Interface Bus (PIB) Diagram



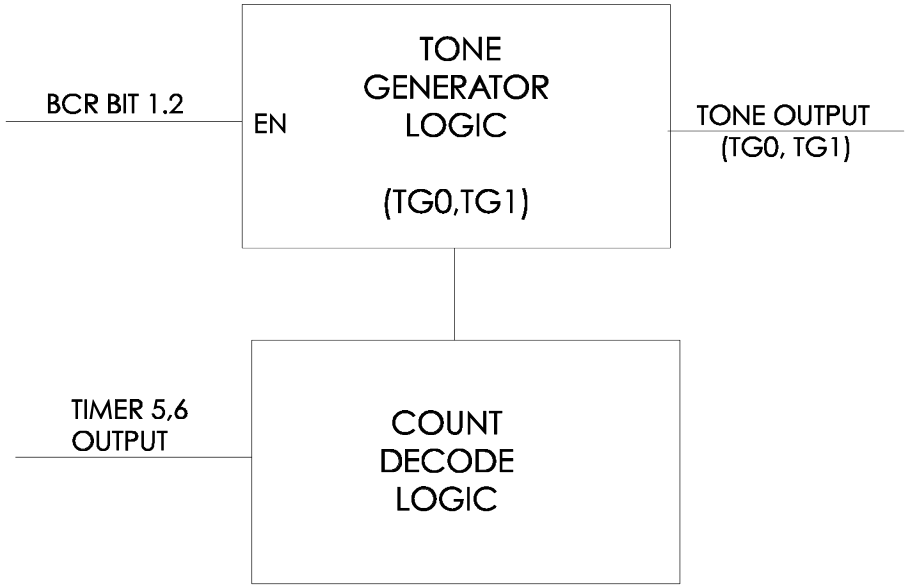


Figure 5-6 W65C265S Tone Generator (TGx) Block Diagram

5.2 W65C265DB Developer Board

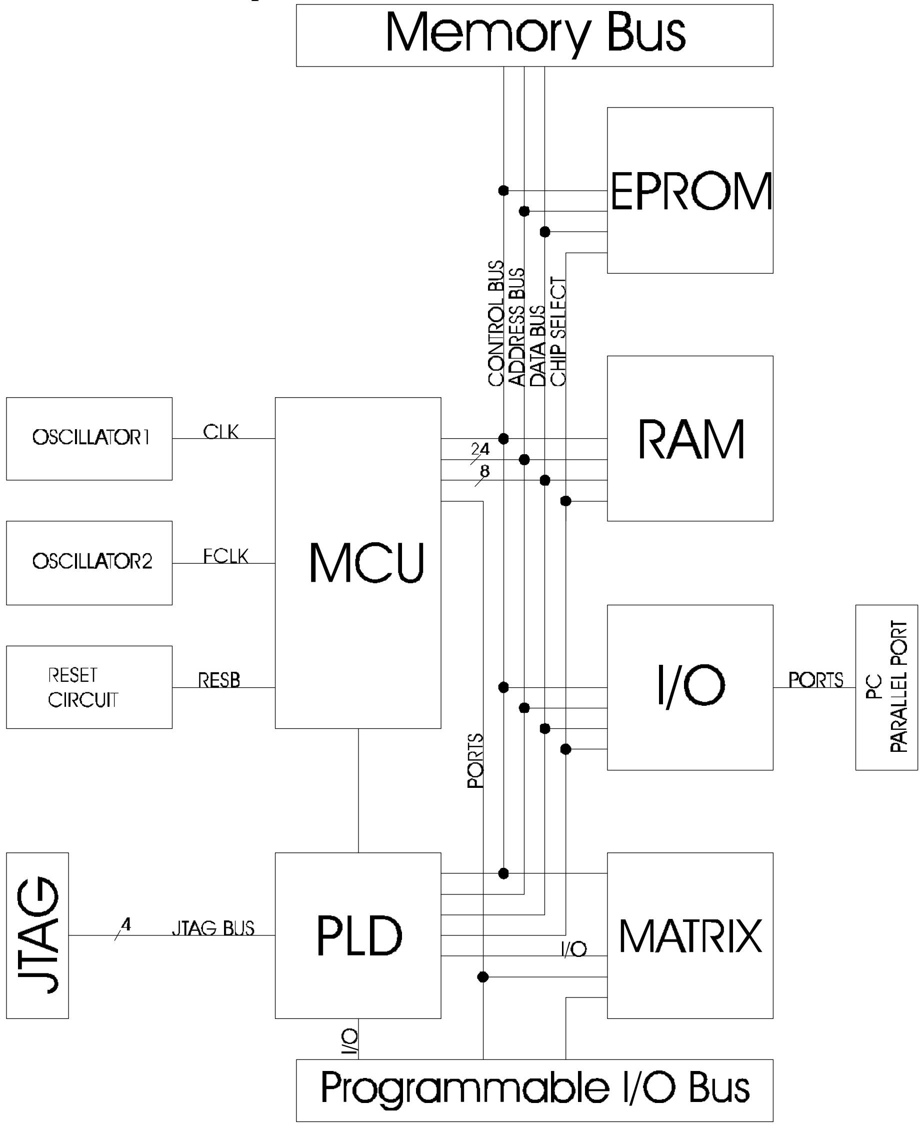


Figure 5-7 W65C265DB Developer Board

Features:

W65C265S 16-bit MCU, total access to all control lines, Memory Bus, Programmable I/O Bus, PC Interface, 20 I/O lines, two oscillators, 32K SRAM, 32K EPROM, W65C22S Versatile Interface Adapter VIA peripheral chip, on-board matrix, PLD for Memory map decoding and ASIC design.

The PLD chip is a XILINX XC9572 for changing the chip select and I/O functions if required. To change the PLD chip to suit your own setup, you need XILINX Data Manager for the XC9572 CPLD chip. The W65C265DB includes an on-board programming header for JTAG configuration. For more details refer to the circuit diagram. The on-board W65C265S and the W65C22S devices have measurement points for core power consumption. Power input is provided by an optional power board which plugs into the 10 pin power header.

An EPROM programmer or an EPROM emulator is required to use the board. WDC's Software Development System includes a W65C816S Assembler and Linker, W65C816S C-Compiler and Optimizer, and W65C816S Simulator/Debugger. WDC's PC IO daughter board can be used to connect the Developer Board to the parallel port of a PC.

Memory map:

CS1B:	8000-FFFF	⇒	EPROM (27C256)
CS3B:	0100-7FFF	⇒	SRAM (62C256)
CS2B:	0030-003F	⇒	VIA (W65C22S)

5.3 External ROM Startup with W65C265S Mask ROMs

Future versions of the W65C265S mask ROM may vary, but each version should contain standard machine code that allows startup to an external memory. Standard versions of the W65C265S will always contain such a startup option. Anyone writing a custom mask ROM for the 265 is encouraged to follow this standard.

The startup standard allows a program in an external memory to be executed after RESET if the startup code WDC (in ASCII, $57, $44, $43) is present at addresses $8000-$8002 or $0800-$0802. If the startup code is found at either set of addresses, the mask ROM does a JMP instruction to $8004 or $0804 respectively. W65C265S chip selects CS6 and CS7 can be used to address the memories.

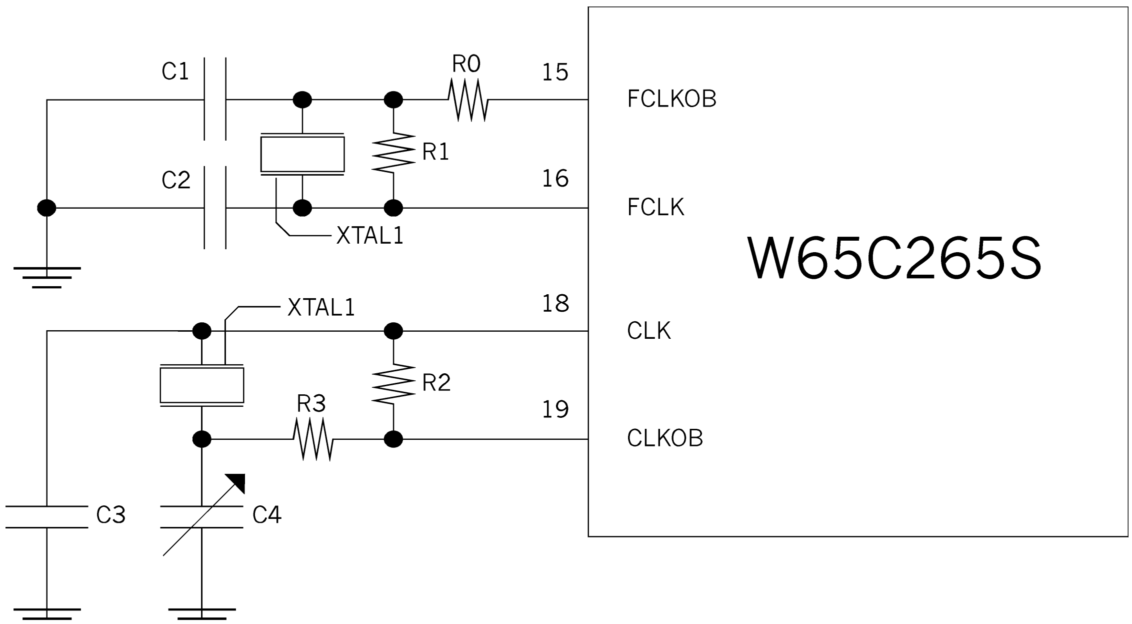
The startup standard was set (and will be followed) with the original mask ROM in the early W65C265S prototypes. A sample startup program appears below. The W65C02S emulation RESET vector ($FFFD) should be set to STARTUP.

```
STARTUP     LDA   #$01    ;ENABLE EXTERNAL MEMORY BUS
            TSB   BCR     ;(BCR=$001B)
            LDA   #$C0    ;ENABLE CHIP SELECTS CS6-, CS7-
            STA   PCS3    ;ON P36, P37 (PCS3=$0007)
;
TRY80       LDA   $8000   ;CHECK $8000 FOR 'WDC'
            CMP   #'W'
            BNE   TRY02
            LDA   $8001
            CMP   #'D'
            BNE   TRY02
            LDA   $8002
            CMP   #'C'
            BNE   TRY02
            JMP   $8004   ;EXECUTE EXTERNAL ROM PROGRAM
;
TRY02       LDA   $0800   ;CHECK $0800 FOR 'WDC'
            CMP   #'W'
            BNE   NOEXT
            LDA   $0801
            CMP   #'D'
            BNE   NOEXT
            LDA   $0802
            CMP   #'C'
            BNE   NOEXT
            JMP   $0804   ;EXECUTE EXTERNAL ROM PROGRAM
;
NOEXT       JMP   MASK_ROM_PROGRAM     ;EXECUTE PROGRAM IN MASK ROM
```

5.3 Recommended clock and fclock oscillators

The following circuit is a possible clocking system for the W65C265S providing both 32.768KHz and 2.0MHz frequencies. The 32.768KHz clock is well suited for setting up a time of day clock with one of the W65C265S's internal timers.

In constructing this oscillator circuit, components should be kept as physically close to the W65C134S as possible and any excess in component leads should be trimmed off.



C1 = 47pF	R0 = 100Ω
C2 = 27pF	R1 = 800KΩ
C3 = 22pF	R2 = 2.6MΩ
C4 = 5-30pF variable	R3 = 150KΩ
XTAL1 = 4 MHz	XTA L2 = 32.768 KHz

Note:

1. Depending on trace layout or construction techniques used, values may need to be altered slightly.
2. Pin numbers only apply to PLCC package only.

Figure 5-8 Oscillator Circuit

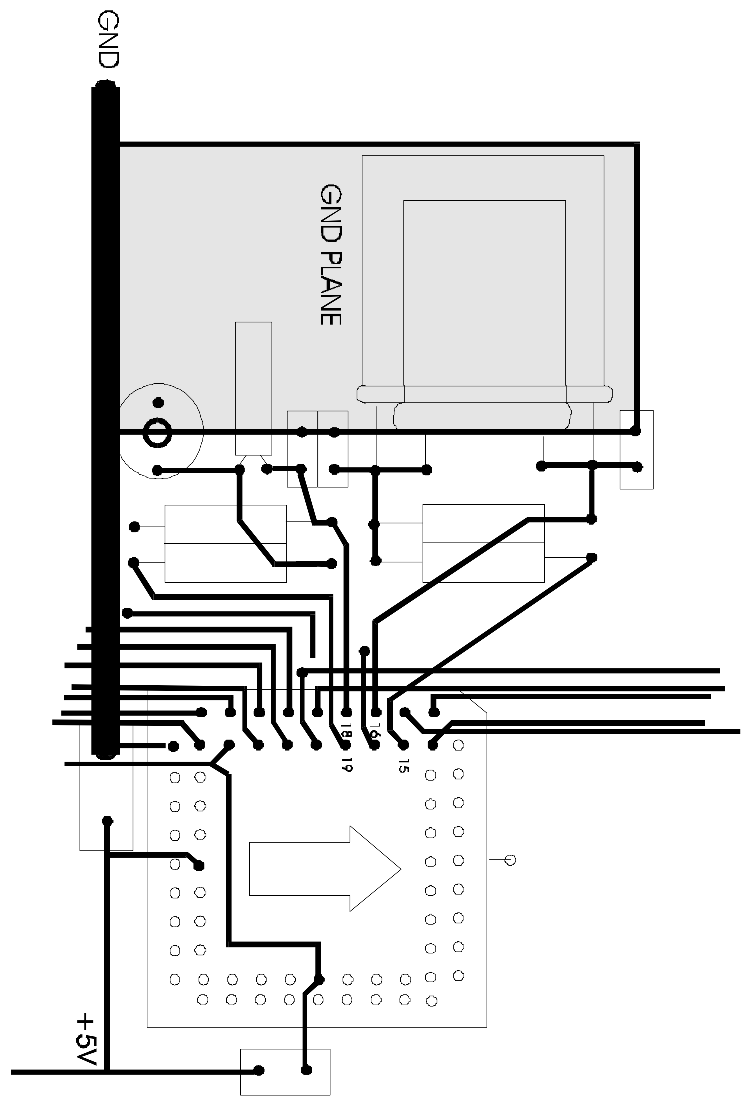


Figure 5-9 Circuit Board Layout for Oscillator Circuit

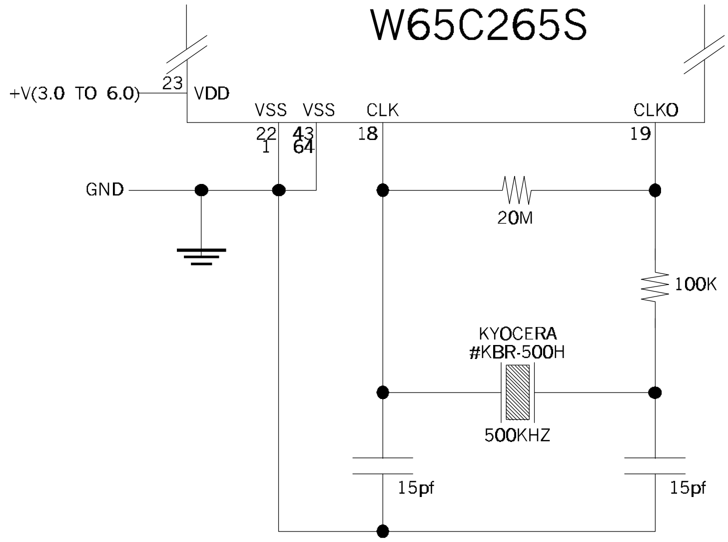


Figure 5-10 W65C265S Resonator Circuit

5.4 Wait state information and uses for the BE pin

The BE pin has two functions; allowing DMA into the W65C265S (BE function) and stopping the microprocessor (RDY function). Changing BE during PHI2 low time changes the BE function; changing BE during PHI2 high time changes RDY. If you want to stop the processor, you should pull BE low in the PHI2 high time for as many cycles as needed. Pulling the BE low in PHI2 high time does not tristate the memory bus. Note also that the PHI2 pin does not stay high while RDY is pulled low; PHI2 going out will continue normally regardless of BE.

Pulling BE low during PHI2 low time turns off the output buffers on the address pins; however, the pins do not float because of weak bus holding devices. Note that the addresses are really inputs to the W65C265S when BE is low. If an external driver puts an address on the bus while BE is low, internal memory (RAM, ROM, or memory-mapped registers) will be accessed depending on the state of WEB. If you have no desire to turn off the busses when you slow down for the peripheral chips, you should hold BE high while you hold RDY low. That is,

BE = (PHI2BAR or RDY)

where PHI2BAR is PHI2 inverted and delayed at least 10ns. RDY is your signal to request the microprocessor to stop. If you are not using the FCLK oscillator, another (less desirable) way to stop the microprocessor is to extend the low or high time of FCLK as long as you need to. This will work only if you know the microprocessor is using FCLK, not CLK.