Synertek

Price $ 2.00

INTRODUCTION

Synertek was founded in 1973 and in its brief history has developed a very broad line of MOS integrated circuits. These devices, including Shift Registers, RAMs, ROMs, Microprocessors and Timekeeping Circuits, are manufactured with Synertek's advanced N-Channel, P-Channel and CMOS depletion load, silicon gate processes. In addition, this process capability is currently being used for the manufacture of custom circuits designed by Synertek to meet specifications established by our customers.

Most Synertek devices are available with operation specified over the full Military temperature range and can be processed in accordance with Mil Standard 883, level B. In addition, less expensive processing plans have been developed for special products and special applications. Synertek has assembly capability meeting the requirements of Mil Standard 883 both in our main Santa Clara facility and at other offshore assembly areas.

Custom MOS circuit design and production is an integral part of Synertek's present and future business plans. Whether the custom design program starts at the feasibility stage or at the point where the customer provides tooling (reticles, tapes, etc.), Synertek is organized to quickly and efficiently handle the most difficult custom designs.

This catalog provides complete technical information on Synertek memories, microprocessors and timekeeping circuits. Additional information can be obtained by contacting Product Marketing in Santa Clara, California.

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1978 Data Catalog

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Shift Registers

Shift Registers

2

1024-Bit Dynamic Shift Registers Quad, Dual, Single

Synertek®

SY1402A SY1403A SY1404A

MEMORY PRODUCTS

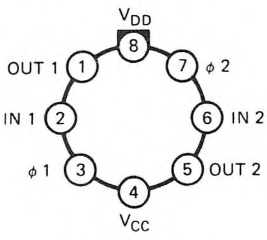
- Synertek ion implanted silicon gate process
- 5 MHz data rate—minimum
- 2.5 MHz clock rate
- TTL, DTL compatible
- Reduced clock capacitance, 85 pF
- Reduced power dissipation, 80 μW/bit at 1.0 MHz

The SY1402A, 1403A and 1404A 2ϕ dynamic shift registers utilize I/O multiplexing techniques to attain a 5.0 MHz data rate with a clock rate of only 2.5 MHz. The inputs and outputs are bipolar and MOS compatible for ease of implementation in a TTL, DTL and a high- or low-threshold MOS system.

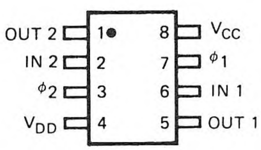
Clock power and V_{DD} current have been significantly reduced due to the advantages inherent in an ion implanted silicon gate design over a conventional silicon gate design. These savings directly affect the cost of the overhead circuitry (clock drivers, power supplies) for a shift register memory system.

The SY1402A, 1403A and 1404A are used effectively in applications requiring low cost serial memory such as CRT refresh, line and page storage for facsimile transmitters and receivers, and character storage for high speed printers.

PIN CONFIGURATION

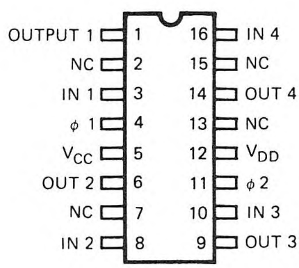


SYM1403A



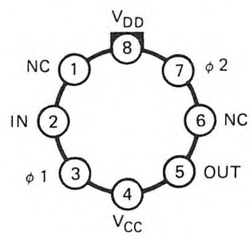
SYP1403A

PIN CONFIGURATION

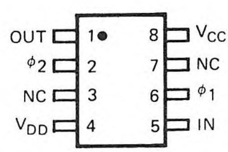


SYP1402A
SYC1402A

PIN CONFIGURATION



SYM1404A



SYP1404A

ORDERING INFORMATION

Order Number	Package Type	Organization	Temperature Range
SYP1404A	Plastic Dip	1024 x 1	0°C to +70°C
SYM1404A	TO Can	1024 x 1	0°C to +70°C
SYP1403A	Plastic Dip	512 x 2	0°C to +70°C
SYM1403A	TO Can	512 x 2	0°C to +70°C
SYP1402A	Plastic Dip	256 x 4	0°C to +70°C
SYC1402A	Ceramic Dip	256 x 4	0°C to +70°C

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ABSOLUTE MAXIMUM RATINGS [1]

Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +160°C
Power Dissipation [(2)]	1 Watt
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.5V to −20V

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = −5V ±5% or −9V ±5%

Symbol	Test	Min.	Typ.[(3)]	Max.	Unit	Conditions
I_{LI}	Input Load Current		<10	500	nA	T_A = 25°C
I_{LO}	Output Leakage Current		<10	1000	nA	V_{OUT} = 0.0V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	Max. V_{ILC}, T_A = 25°C
V_{IL}	Input "Low" Voltage	V_{CC}−10		V_{CC}−4.2	V	
V_{IH}	Input "High" Voltage	V_{CC}−2		V_{CC}+.3	V	

V_{DD} = −5V ±5%

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{DD1}	Power Supply Current		15	20	mA	T_A = 25°C } Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, V_{ILC} = V_{CC} −17V
I_{DD2}	Power Supply Current			22	mA	T_C = 0°C } (same as above)
V_{ILC}	Clock Input Low Voltage	V_{CC}−17		V_{CC}−15	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1} = 3K to V_{DD}, I_{OL} = 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1} = 3K to V_{DD}, I_{OH} = −100μA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.6	V_{CC}−1		V	R_{L2} = 4.7K to V_{DD} (See p. 4 for connection)

V_{DD} = −9V ±5%

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{DD3}	Power Supply Current		15	20	mA	T_A = 25°C } Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, V_{ILC} = V_{CC}−14.7V
I_{DD4}	Power Supply Current			22	mA	T_C = 0°C } (same as above)
V_{ILC}	Clock Input Low Voltage	V_{CC}−14.7		V_{CC}−12.6	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	R_{L1} = 4.7K to V_{DD}, I_{OL} = 1.6 mA
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1} = 4.7K to V_{DD}, I_{OL} = 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1} = 4.7K to V_{DD}, I_{OH} = −100 μA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.9	V_{CC}−1		V	R_{L2} = 6.2K to V_{DD}, R_{L3} = 3.9K to V_{CC} (See p. 4 for connection)

Note 1: Stresses listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 1 watt dissipation is not to be construed as an operating rating (see note 1). For operating at elevated temperatures the device must be derated based as shown on page 4. When operating at V_{DD} = −5V±5% the maximum duty cycle is 33% and at V_{DD} = −9V+5% the maximum duty cycle is 26%. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $[t_{\phi PW} + 1/2\,(t_R + t_F)]$ x clock rate.

Note 3: Typical values are at T_A = 25°C and at nominal voltages.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$

Symbol	Test	$V_{DD} = -5V \pm 5\%$ (Test Load 1) Min.	Max.	$V_{DD} = -9V \pm 5\%$ (Test Load 2) Min.	Max.	Unit
Frequency	Clock Rep Rate		2.5		1.5	MHz
Frequency	Data Rep Rate	Note 1	5.0	Note 1	3.0	MHz
$t_{\phi PW}$	Clock Pulse Width	.130	10	.170	10	μsec
$t_{\phi D}$	Clock Pulse Delay	10	Note 1	10	Note 1	nsec
t_R, t_F	Clock Pulse Transition		1000		1000	nsec
t_{DW}	Data Write Time (Set Up)	30		60		nsec
t_{DH}	Data To Clock Hold Time	20		20		nsec
t_{A+}, t_{A-}	Clock To Data Out Delay		90		110	nsec

CAPACITANCE [2] $V_{CC} = +5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$ or $-9V \pm 5\%$, $T_A = 25°C$

Symbol	Test	Typ.	Max.	Conditions	
C_{IN}	Input Capacitance	5 pF	10 pF	$V_{IN} = V_{CC}$	f = 1 MHz
C_{OUT}	Output Capacitance	5 pF	10 pF	$V_{OUT} = V_{CC}$	f = 1 MHz
C_{ϕ}	Clock Capacitance	70 pF	85 pF	$V_{\phi} = V_{CC}$	f = 1 MHz
$C_{\phi1\phi2}$	Clock to Clock Capacitance	11 pF	16 pF	$V_{\phi} = V_{CC}$	f = 1 MHz

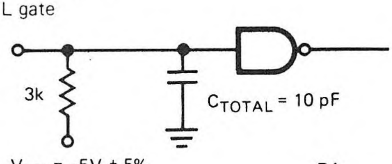
Note 1: See page 4 for guaranteed curve. Note 2: This parameter is periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS

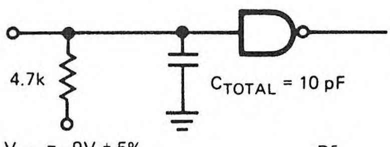
Conditions of Test

Input rise and fall times: 10 nsec

Output Load is 1 TTL gate

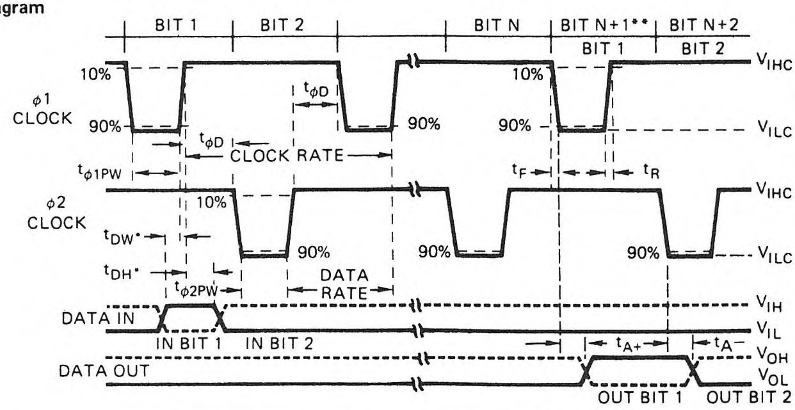


D4



D5

Timing Diagram

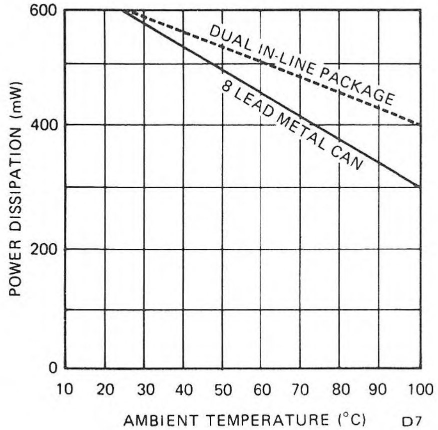


D6

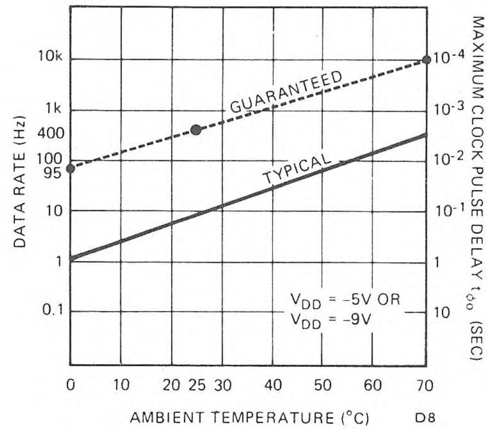
*t_{DW} and t_{DH} same for $t_{\phi 2}$ **N=256 for SY1402A, N=512 for SY1403A, N=1024 for SY1404A

SHIFT REGISTERS

TYPICAL CHARACTERISTICS

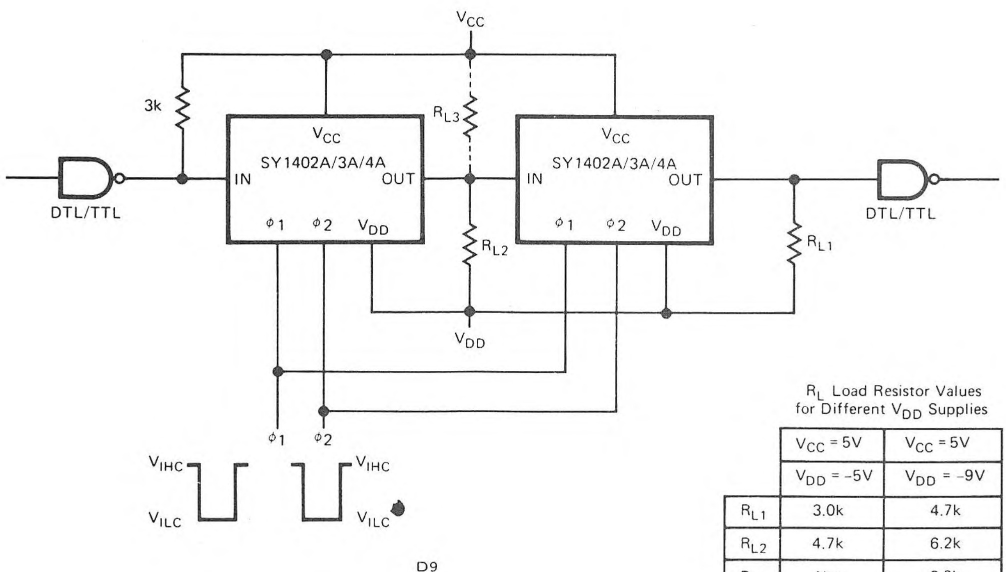


MAXIMUM ALLOWABLE POWER DISSIPATION



MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS. TEMPERATURE

DTL/TTL MOS Interfaces



R_L Load Resistor Values for Different V_{DD} Supplies

	V_{CC} = 5V	V_{CC} = 5V
	V_{DD} = −5V	V_{DD} = −9V
R_{L1}	3.0k	4.7k
R_{L2}	4.7k	6.2k
R_{L3}	Not required	3.9k

2048 - Bit Dynamic Recirculating Shift Registers

SY2401

Synertek®

MEMORY PRODUCTS

- Single Supply Voltage - +5V
- Fully TTL Compatible - Inputs, Outputs and Clock
- Guaranteed 1MHz Operation (SY2401) or 2.5MHz Operation (SY2401-1) With 100pF Load, Over Temperature
- Low Power Dissipation - 150 μW/Bit Typical at Maximum Clock Rate
- Low Clock Capacitance - 7pF
- Write/Recirculate and Chip Select Logic Incorporated on Chip
- Standard Configuration - Dual 1024 Bit

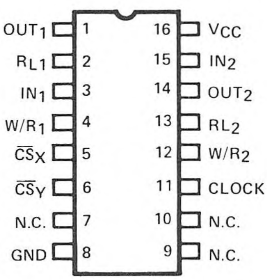
The SY2401 is a 2048-bit dynamic recirculating shift register. It is directly TTL compatible in all respects: inputs, outputs, clock and a single +5V power supply.

Write/recirculate controls are provided to eliminate the need for external logic elements when recirculating data.

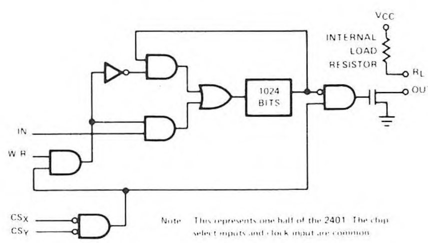
Two Chip Select inputs have been provided to allow easy selection of an individual package when outputs of several devices have been "OR-tied." A separate internal "pull-up" resistor (R_L) is provided which can be externally connected to the output pin to achieve full signal swing.

This shift register is fabricated with ion-implanted N-channel silicon gate technology. This technology provides the designer with high performance, easy to use MOS circuits. Only a single +5V Power supply is needed and all devices are directly TTL compatible, including clocks.

PIN CONFIGURATION



LOGIC DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Clock Frequency	Temperature Range
SYP2401	Plastic DIP	1 MHz	0°C to 70°C
SYC2401	Ceramic DIP	1 MHz	0°C to 70°C
SYP2401-1	Plastic DIP	2.5 MHz	0°C to 70°C
SYC2401-1	Ceramic DIP	2.5 MHz	0°C to 70°C

PIN NAMES

IN	Data Input	OUT	Data Output
W/R	Write/Recirculate Control	R_L	Internal Load Resistor
$\overline{CS}_X$, $\overline{CS}_Y$	Chip Select Input	N.C.	No Connection

TRUTH TABLE

FUNCTION	PIN SYMBOL		
	W/R	$\overline{CS}_X$	$\overline{CS}_Y$
WRITE MODE	H	L	L
RECIRCULATE	L	X	X
	X	H	X
	X	X	H
READ MODE	X	L	L

H = Logic High Level L = Logic Low Level
X = Don't Care Condition

SHIFT REGISTERS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to 150°C
Power Dissipation	1W
Voltage on Any Pin with Respect to Ground	-0.5V to +7V

*COMMENT:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

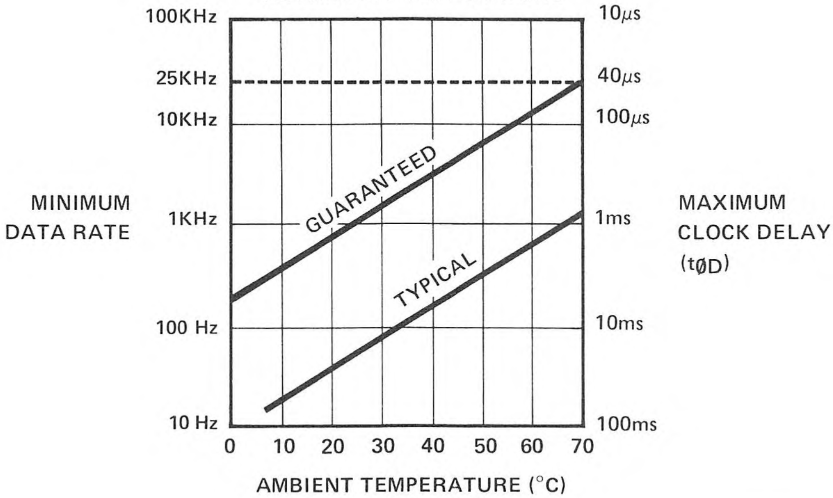
T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

Symbol	Parameter	SY2401 SY2401-1 Min.	Typ.(1)	Max.	Unit	Test Conditions
I_{LI}	Input Leakage			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage			100	μA	V_{OUT} = 5.25V
I_{CC}	Power Supply			70	mA	T_A = 25°C } V_{CC} = 5.25V;
	Current			80	mA	T_A = 0°C } 80% Duty Cycle
V_{IH}	Input High Level Voltage (All Inputs)	2.2		5.25	V	
V_{IL}	Input Low Level Voltage (All Inputs)	-0.3		0.65	V	
I_{OL}	Output Low Sink Current	6.3	10		mA	V_{OL} = 0.45V
V_{OH}	Output High Level Voltage	2.4		V_{CC}	V	I_{OH} = -1mA, R_L Connected
V_{OL}	Output Low Level Voltage	0		0.45	V	I_{OL} = 1.6mA, R_L Connected
R_L	Internal Load	0.8	1.3	2.2	KΩ	

NOTE: (1) Typical values are at 25°C and at nominal voltage.

A.C. CHARACTERISTICS

MINIMUM DATA RATE AND MAXIMUM CLOCK DELAY VS. AMBIENT TEMPERATURE



A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified.

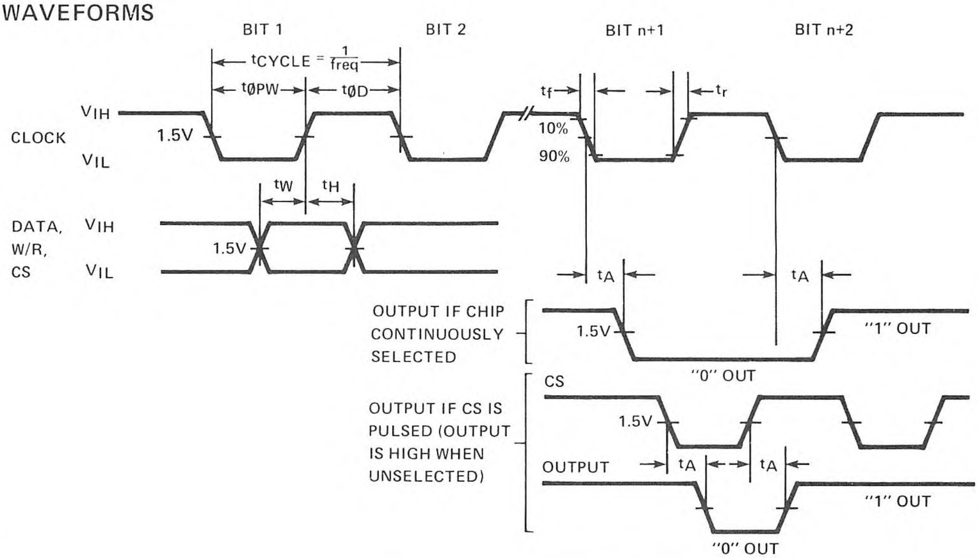
Symbol	Parameter	SY2401 Min	SY2401 Max	SY2401-1 Min	SY2401-1 Max	Units	Test Conditions
Freq. Max.	Max. Data Rep. Rate		1		2.5	MHz	
Freq. Min.	Min. Data Rep. Rate	1		1		KHz	T_A = 25°C
		25		25		KHz	T_A = 70°C
$t_{\phi pw}$	Clock Pulse Width	0.80	10	0.32	10	μs	
$t_{\phi D}$	Clock Pulse Delay	0.20	1000	0.08	1000	μs	T_A = 25°C
		0.20	40	0.08	40	μs	T_A = 70°C
t_r, t_f	Clock Rise and Fall Time		50		50	ns	
t_W	Write Time	200		80		ns	
t_H	Hold Time	150		60		ns	
t_A	Access Time From Clock or Chip Select		500		230	ns	R_L Connected, C_L = 100pF One TTL Load

CAPACITANCE

T_A = 25°C

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units	Test Conditions
C_{IN}	Data, W/R & CS Input Capacitance		4	7	pF	All Pins at AC Ground; 250 mV Peak to Peak, 1 MHz
C_{OUT}	Output Capacitance		10	14	pF	
C_{ϕ}	Clock Capacitance		4	7	pF	

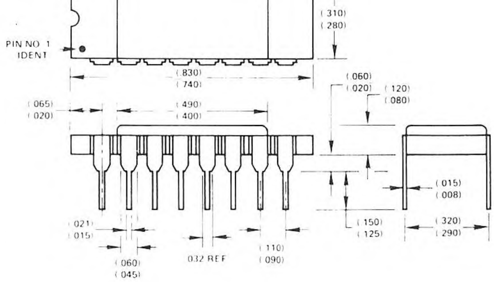
WAVEFORMS



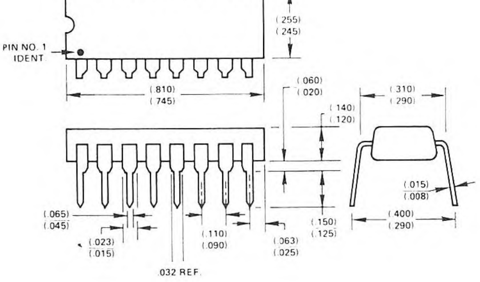
SHIFT REGISTERS

PACKAGE DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



1024 Bit Static Shift Registers

Synertek®

SY2533 SY2833 SY2833A/B/C

MEMORY PRODUCTS

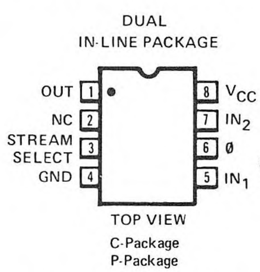
SHIFT REGISTERS

- Single +5V Power Supply
- High Speed Operation – 5.0 MHz
- Totally TTL compatible – inputs, output, clock
- Military temperature range operation
- 400 mvolt noise immunity
- Replaces AMD 2833 Series and Signetics 2533

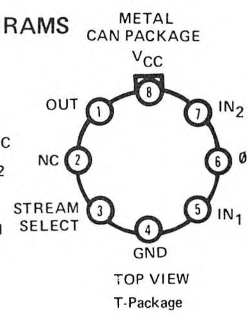
The SY2533/SY2833 Series of Static Shift Registers, organized 1024x1, are completely TTL compatible and capable of high speed operation. Only a single +5V power supply is needed, and all inputs, clock and outputs operate at TTL voltage levels. On chip logic is provided to accept input data from either of two inputs, allowing simple external system recirculate operation. Data is entered into the register on the positive to negative transition of the clock pulse, and 1023 clock cycles later, is available at the output, a delay time after the positive to negative transition of the clock pulse. Since all internal storage is implemented with static, DC logic, the clock input may be held indefinitely at a logic "0" state without loss of data.

The SY2533/SY2833 Static Shift Registers, manufactured with Synertek's ion-implanted silicon gate N-channel MOS technology, are totally compatible, plug in replacements for AMD's 2833 Series as well as Signetics 2533. These devices are intended for serial data storage in systems where single power supply, high speed operation and low system cost are important design parameters.

CONNECTION DIAGRAMS

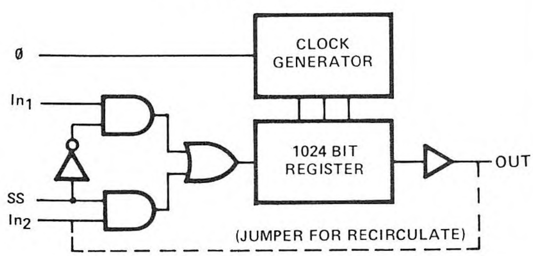


TOP VIEW
C-Package
P-Package



TOP VIEW
T-Package

BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Clock Frequency	Temperature Range
SYP2533	Plastic Dip	1.5 MHz	0°C to +70°C
SYT2533	TO-Can	1.5 MHz	0°C to +70°C
SYC2533	Ceramic Dip	1.5 MHz	0°C to +70°C
SYP2833	Plastic Dip	2 MHz	0°C to +70°C
SYT2833	TO-Can	2 MHz	0°C to +70°C
SYC2833	Ceramic Dip	2 MHz	0°C to +70°C
SYP2833A	Plastic Dip	3 MHz	0°C to +70°C
SYT2833A	TO-Can	3 MHz	0°C to +70°C
SYC2833A	Ceramic Dip	3 MHz	0°C to +70°C
SYP2833B	Plastic Dip	4 MHz	0°C to +70°C
SYT2833B	TO-Can	4 MHz	0°C to +70°C
SYC2833B	Ceramic Dip	4 MHz	0°C to +70°C
SYP2833C	Plastic Dip	5 MHz	0°C to +70°C
SYT2833C	TO-Can	5 MHz	0°C to +70°C
SYC2833C	Ceramic Dip	5 MHz	0°C to +70°C
SYMC2833	Ceramic Dip	2 MHz	-55°C to +125°C

TRUTH TABLE

STREAM SELECT	FUNCTION
0	IN 1
1	IN 2

NOTE: "0" = 0V, "1" = +5V

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ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C (SY2533, 2833, 2833A, 2833B, 2833C), -55°C to +125°C (SYM2833)
V_{CC} = +5V ± 5%

Parameters	Description	Min	Typ	Max	Units	Test Conditions	
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN, I_{OH} = -100 μA	
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN, I_{OL} = 1.6 mA	
V_{IH}	Input HIGH Level	2.0		V_{CC}+0.3	Volts	Guaranteed input logical HIGH voltage for all inputs	
V_{IL}	Input LOW Level	-0.3		0.8	Volts	Guaranteed input logical LOW voltage for all inputs	
I_{IL}	Input LOW Current			10	μA	V_{CC} = MAX, V_{IN} = 0V, T_A = 25°C	
I_{CC}	V_{CC} Power Supply Current (Note 1)		16	30	mA	f = 1.5 MHz	SY2533
			16	35/42		f = 2.0 MHz	SY2833/SYM2833
			20	40		f = 3.0 MHz	SY2833A
I_{CC}	V_{CC} Power Supply Current (Note 1)		40	60	mA	f = 4.0 MHz	SY2833B
			50	75		f = 5.0 MHz	SY2833C

Note 1: Power supply currents are with outputs open.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C (SY2533, 2833, 2833A), -55°C to +125°C (SYM2833)
V_{CC} = +5V ± 5%

Parameters	Description	SY2533			SY2833/SYM2833			SY2833A			Units	Test Conditions
		Min	Typ[1]	Max	Min	Typ[1]	Max	Min	Typ[1]	Max		
f_{max}	Maximum Clock Frequency	1.5	2.0		2.0	3.0		3.0	3.5		MHz	
$t_{\phi pwL}$	Clock LOW Time	0.250		∞	0.200		∞	0.170		∞	μs	
$t_{\phi pwH}$	Clock HIGH Time	0.350		100	0.250		100	0.165		100	μs	
t_r, t_f	Clock Rise and Fall Times			1			1			1	μs	
t_s (I)	Setup Time, I_0 or I_1 Input			50			50			50	ns	$t_r = t_f \leq 25ns$
t_h (I)	Hold Time, I_0 or I_1 Input			50			50			50	ns	
t_s (S)	Setup Time, S Input			80			80			80	ns	
t_h (S)	Hold Time, S Input			50			50			50	ns	
t_{pd}	Delay, Clock to Output LOW or HIGH			300			300			200	ns	R_L=2.9k,C_L=20pf
t_{pr}, t_{pf}	Output Rise and Fall Times			150			150			150	ns	10% to 90%
C_{in}	Capacitance, Any Input[2]		3	5		3	5		3	5	pF	f = 1 MHz

Note 1: Typical limits are at V_{CC} = 5.0V, and T_A = 25°C

Note 2: This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

SHIFT REGISTERS

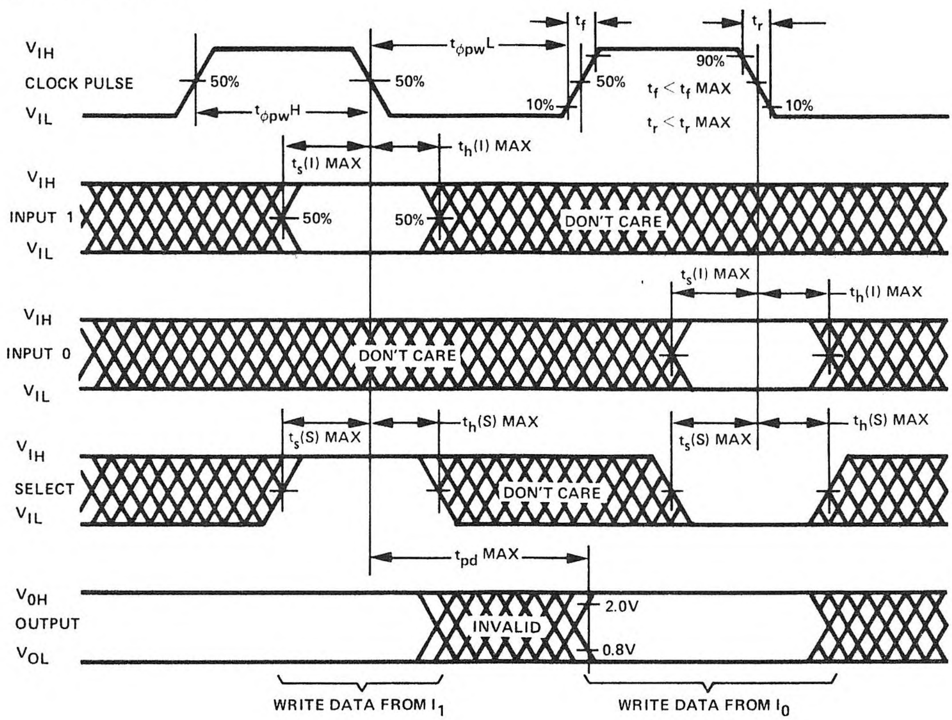
A.C. CHARACTERISTICS

T_A = 0°C to +70°C
V_{CC} = +5V ± 5%

Parameters	Description	SY2833B			SY2833C			Units	Test Conditions
		Min	Typ[1]	Max	Min	Typ[1]	Max		
f_{max}	Maximum Clock Frequency	4.0	5.0		5.0	6.0		MHz	
$t_{\phi pw}L$	Clock LOW Time	0.125		∞	0.100		∞	μs	
$t_{\phi pw}H$	Clock HIGH Time	0.125		100	0.100		100	μs	
t_r, t_f	Clock Rise and Fall Times			1			1	μs	
$t_s(I)$	Setup Time, I_0 or I_1 Input			30			30	ns	$t_r = t_f \leq 25$ns
$t_h(I)$	Hold Time, I_0 or I_1 Input			50			50	ns	
$t_s(S)$	Setup Time, S Input			50			50	ns	
$t_h(S)$	Hold Time, S Input			50			50	ns	
t_{pd}	Delay, Clock to Output LOW or HIGH			150			110	ns	R_L=2.9k, C_L=20pf
t_{pr}, t_{pf}	Output Rise and Fall Times			150			150	ns	10% to 90%
C_{in}	Capacitance, Any Input[2]		3	5		3	5	pF	f = 1 MHz

Note 1: Typical limits are at V_{CC}=5.0V, and T_A=25°C.
Note 2: This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

TIMING DIAGRAM



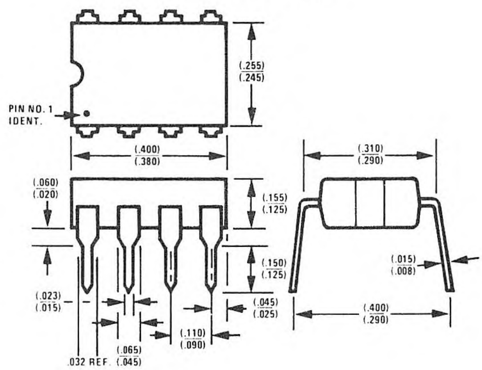
DEFINITION OF TERMS

Static Shift Register. A shift register capable of maintaining stored data without continuously being clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

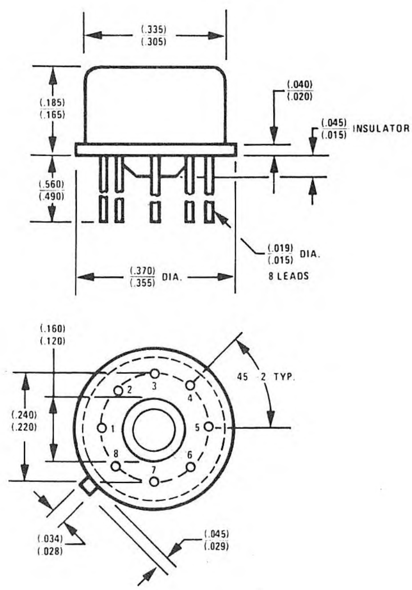
Setup and Hold Times. The shift register will accept the data present on its input around the time the clock goes from HIGH to LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The setup and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum setup time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

PHYSICAL DIMENSIONS

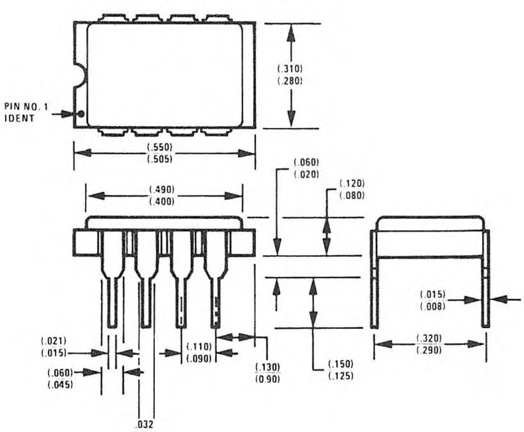
8 Lead Plastic Dip



8 Lead TO-Can



8 Lead Ceramic Dip



512 Bit and 480 Bit Dual Static Shift Registers

SY2534 SY2535

MEMORY PRODUCTS

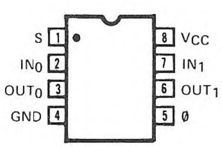
Synertek®

- +5 Volts Only—No Negative Power Supplies
- Reduce System Cost—Eliminate One Power Supply
- Available to 3.0 MHz
- Double Density Replacement For Signetics 2527/2529
- All Inputs, Outputs and Clocks TTL Compatible

These dual 512-bit and 480-bit static shift registers employ Synertek's ion-implanted silicon gate technology to achieve full TTL compatibility. All inputs and outputs are TTL levels and the only supply necessary is +5 volts. For applications requiring dynamic storage, these same compatibility features are available on the 2048-bit SY2401. Pinouts are essentially the same as Signetics' 2527/2529, allowing the user to reduce package count by a factor of two with the double density SY2534/SY2535.

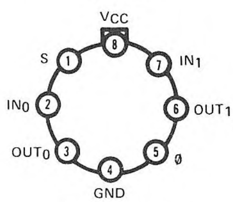
CONNECTION DIAGRAMS

TOP VIEW



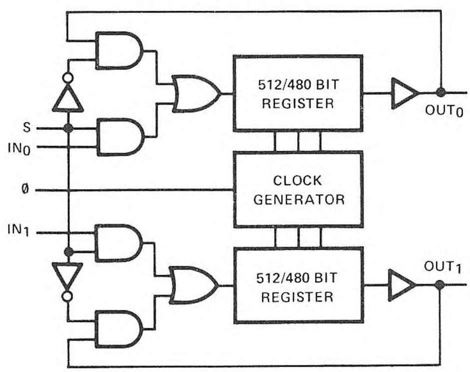
C = PACKAGE
P = PACKAGE

TOP VIEW



T = PACKAGE

BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Register Length	Clock Frequency	Temperature Range
SYP2534	Plastic DIP	512	1.5MHz	0°C to +70°C
SYT2534	TO Can	512	1.5MHz	0°C to +70°C
SYP2534A	Plastic DIP	512	3.0MHz	0°C to +70°C
SYT2534A	TO Can	512	3.0MHz	0°C to +70°C
SYP2535	Plastic DIP	480	1.5MHz	0°C to +70°C
SYT2535	TO Can	480	1.5MHz	0°C to +70°C
SYP2535A	Plastic DIP	480	3.0MHz	0°C to +70°C
SYT2535A	TO Can	480	3.0MHz	0°C to +70°C

TRUTH TABLE

S	Function
0	Recirculate
1	Write

Note: "0" = OV. "1" = +5V

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	0.6W

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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J-10K-11/77

SHIFT REGISTERS

OPERATING RANGE: V_{CC} = +5.0V ±5%; 0° to 70°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = -100μA	2.4	3.5		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 1.6mA		0.2	0.4	Volts
V_{IL}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0		V_{CC} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	-0.3		0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0V, T_A = 25°C			10	μA
I_{CC}	V_{CC} Power Supply Current (Note 1)	f = 1.5 MHz SY2534/2535		16	35	mA
		f = 3.0 MHz SY2534A/2535A		25	45	mA

Note 1: Power Supply currents are with inputs and outputs open.

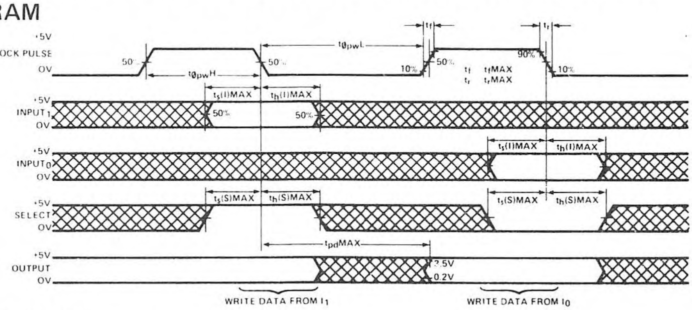
SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameters	Description	Test Conditions	SY2534, SY2535 Min	Typ[1]	Max	SY2534A, SY2535A Min	Typ[1]	Max	Units
f_{max}	Maximum Clock Frequency		1.5	2.0		3.0	3.5		MHz
$t_{\Phi pwL}$	Clock LOW Time		0.250		∞	0.170		∞	μS
$t_{\Phi pwH}$	Clock HIGH Time		0.350		100	0.165		100	μS
t_r, t_f	Clock Rise and Fall Times				1			1	μS
t_s (I)	Setup Time I_0 or I_1 Input	$t_r = t_f \leq 25$ns			50			50	ns
t_h (I)	Hold Time I_0 or I_1 Input	$t_r = t_f \leq 25$ns			50			50	ns
t_s (S)	Setup Time, S Input	$t_r = t_f \leq 25$ns			80			80	ns
t_h (S)	Hold Time, S Input	$t_r = t_f \leq 25$ns			50			50	ns
t_{pd}	Delay Clock to Output LOW or HIGH	R_L=2.9K, C_L=20pF			300			200	ns
t_{pr}, t_{pf}	Output Rise and Fall Times	10% to 90%			150			150	ns
C_{in}	Capacitance, Any Input[2]	f = 1 MHz		3	5		3	5	pF

Note 1: Typical limits are at V_{CC} = 5.0V, and T_A = 25°C.

Note 2: This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

TIMING DIAGRAM



DEFINITION OF TERMS

Static Shift Register. A shift register capable of maintaining stored data without continuously being clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

Setup and Hold Times. The shift register will accept the data present on its input around the time the clock goes from HIGH to LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The setup and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum setup time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

1024-Bit Dynamic Shift Registers Quad, Dual, Single

SY2802A
SY2803A
SY2804A

MEMORY PRODUCTS

Synertek®

SHIFT REGISTERS

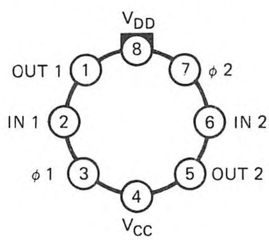
- Synertek ion implanted silicon gate process
- 10 MHz data rate--minimum
- 5 MHz clock rate
- TTL, DTL compatible
- Reduced clock capacitance, 85pF
- Reduced power dissipation, 80 μW/bit at 1.0 MHz

The SY2802A, 2803A and 2804A 2ϕ dynamic shift registers utilize I/O multiplexing techniques to attain a 10 MHz data rate with a clock rate of only 5 MHz. The inputs and outputs are bipolar and MOS compatible for ease of implementation in a TTL, DTL and a high- or low-threshold MOS system.

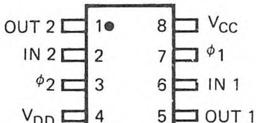
Clock power and V_{DD} current have been significantly reduced due to the advantages inherent in an ion implanted silicon gate design over a conventional silicon gate design. These savings directly affect the cost of the overhead circuitry (clock drivers, power supplies) for a shift register memory system.

The SY2802A, 2803A and 2804A are used effectively in applications requiring low cost serial memory such as CRT refresh, line and page storage for facsimile transmitters and receivers, and character storage for high speed printers.

PIN CONFIGURATION

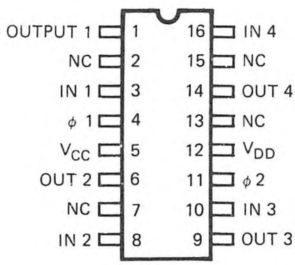


SYM2803A



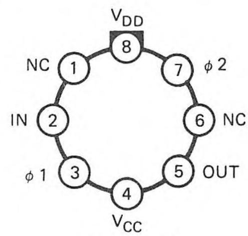
SYP2803A

PIN CONFIGURATION

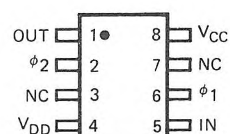


SYP2802A
SYC2802A

PIN CONFIGURATION



SYM2804A



SYP2804A

ORDERING INFORMATION

Order Number	Package Type	Organization	Temperature Range
SYP2804A	Plastic Dip	1024 x 1	0°C to +70°C
SYM2804A	TO Can	1024 x 1	0°C to +70°C
SYP2803A	Plastic Dip	512 x 2	0°C to +70°C
SYM2803A	TO Can	512 x 2	0°C to +70°C
SYP2802A	Plastic Dip	256 x 4	0°C to +70°C
SYC2802A	Ceramic Dip	256 x 4	0°C to +70°C

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SHIFT REGISTERS

ABSOLUTE MAXIMUM RATINGS [1]

Temperature Under Bias	$0°C$ to $70°C$	Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.5V to −20V
Storage Temperature	$-65°C$ to $+160°C$		
Power Dissipation [2]	1 Watt		

D.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise specified

$V_{DD} = -5V \pm 5\%$

Symbol	Test	Min.	Typ. [3]	Max.	Unit	Conditions
I_{LI}	Input Load Current		<10	500	nA	$T_A = 25°C$
I_{LO}	Output Leakage Current		<10	1000	nA	$V_{OUT} = 0.0V$, $T_A = 25°C$
I_{LC}	Clock Leakage Current		10	1000	nA	Max. V_{ILC}, $T_A = 25°C$
V_{IL}	Input "Low" Voltage	$V_{CC}-10$		$V_{CC}-4.2$	V	
V_{IH}	Input "High" Voltage	$V_{CC}-2$		$V_{CC}+.3$	V	

$V_{DD} = -5V \pm 5\%$

Symbol	Test	Min.	Typ. [3]	Max.	Unit	Conditions
I_{DD1}	Power Supply Current		35	40	mA	$T_A = 25°C$ } Output at Logic "0", 10 MHz Data Rate, 40% Duty Cycle, Continuous Operation, $V_{ILC} = V_{CC} - 17V$
I_{DD2}	Power Supply Current			45	mA	$T_C = 0°C$ } (same conditions)
V_{ILC}	Clock Input Low Voltage	$V_{CC}-17$		$V_{CC}-15$	V	
V_{IHC}	Clock Input High Voltage	$V_{CC}-1$		$V_{CC}+.3$	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	$R_{L1} = 3K$ to V_{DD}, $I_{OL} = 1.6$ mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	$R_{L1} = 3K$ to V_{DD}, $I_{OH} = -100\mu A$
V_{OH2}	Output High Voltage Driving MOS	$V_{CC}-1.6$	$V_{CC}-1$		V	$R_{L2} = 4.7K$ to V_{DD} (See p. 4 for connection)

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$

Symbol	Test	$V_{DD} = -5V \pm 5\%$ Min.	Max.	Unit
Frequency	Clock Rep Rate		5.0	MHz
Frequency	Data Rep Rate	Note 1	10.0	MHz
$t_{\phi PW}$	Clock Pulse Width	.07	10	μsec
$t_{\phi D}$	Clock Pulse Delay	10	Note 1	nsec
t_R, t_F	Clock Pulse Transition		1000	nsec
t_{DW}	Data Write Time (Set Up)	30		nsec
t_{DH}	Data To Clock Hold Time	20		nsec
t_{A+}, t_{A-}	Clock To Data Out Delay		90	nsec

Note 1: Stresses listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 1 watt dissipation is not to be construed as an operating rating (see note 1). For operating at elevated temperatures the device must be derated based as shown on page 4. When operating at $V_{DD} = -5V \pm 5\%$ the maximum duty cycle is 40%. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $[t_{\phi PW} + 1/2 (t_R + t_F)]$ x clock rate.

Note 3: Typical values are at $T_A = 25°C$ and at nominal voltages.

CAPACITANCE [2] V_{CC} = +5V ±5%, V_{DD} = −5V ±5%, T_A = 25°C

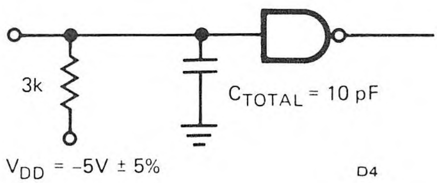
Symbol	Test	Typ.	Max.	Conditions
C_{IN}	Input Capacitance	5 pF	10 pF	$V_{IN} = V_{CC}$ (f = 1 MHz)
C_{OUT}	Output Capacitance	5 pF	10 pF	$V_{OUT} = V_{CC}$ (f = 1 MHz)
C_{ϕ}	Clock Capacitance	70 pF	85 pF	$V_{\phi} = V_{CC}$ (f = 1 MHz)
$C_{\phi1\phi2}$	Clock to Clock Capacitance	11 pF	16 pF	$V_{\phi} = V_{CC}$ (f = 1 MHz)

Note 1: See page 4 for guaranteed curve.
Note 2: This parameter is periodically sampled and is not 100% tested.

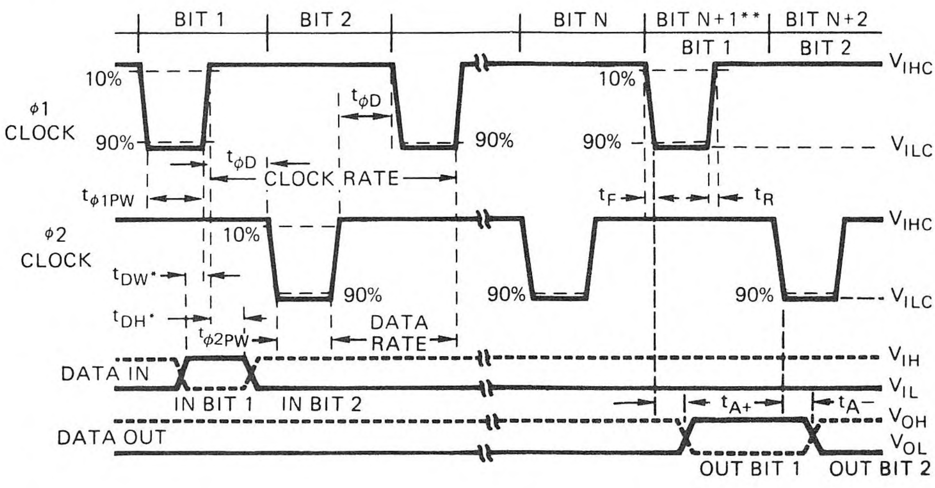
SWITCHING CHARACTERISTICS

Conditions of Test

Input rise and fall times: 10 nsec
Output Load is 1 TTL gate



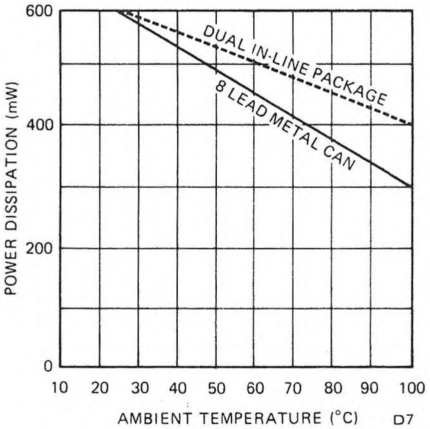
Timing Diagram



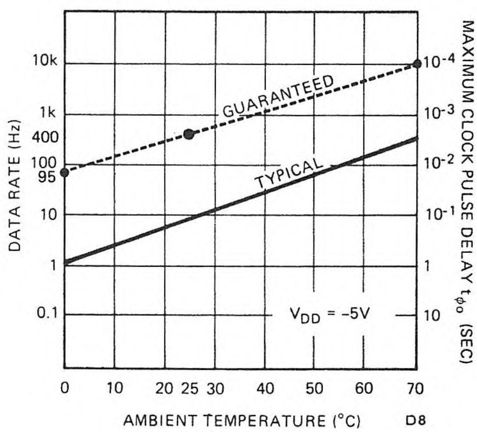
*t_{DW} and t_{DH} same for $t_{\phi 2}$
**N = 256 for SY2802A, N = 512 for SY2803A, N = 1024 for SY2804A

SHIFT REGISTERS

TYPICAL CHARACTERISTICS

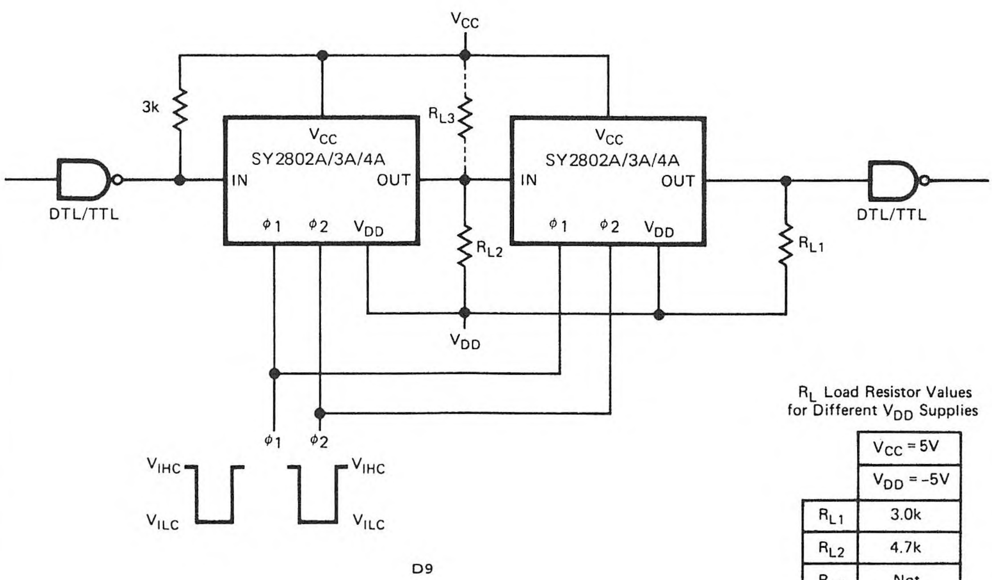


MAXIMUM ALLOWABLE POWER DISSIPATION



MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS. TEMPERATURE

DTL/TTL MOS Interfaces



R_L Load Resistor Values for Different V_{DD} Supplies

	$V_{CC} = 5V$
	$V_{DD} = -5V$
R_{L1}	3.0k
R_{L2}	4.7k
R_{L3}	Not required

2048-Bit Dynamic Shift Registers

SY2825A SY2826/7

Synertek®

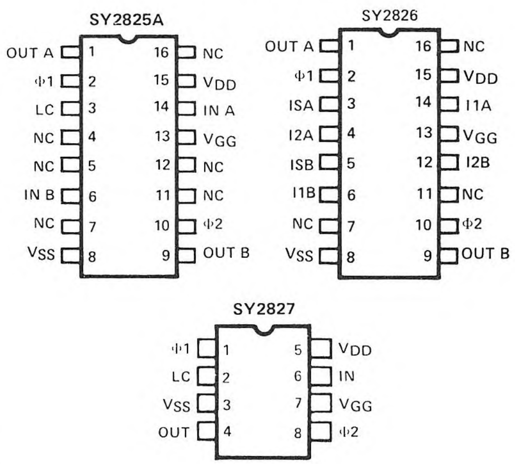
MEMORY PRODUCTS

SHIFT REGISTERS

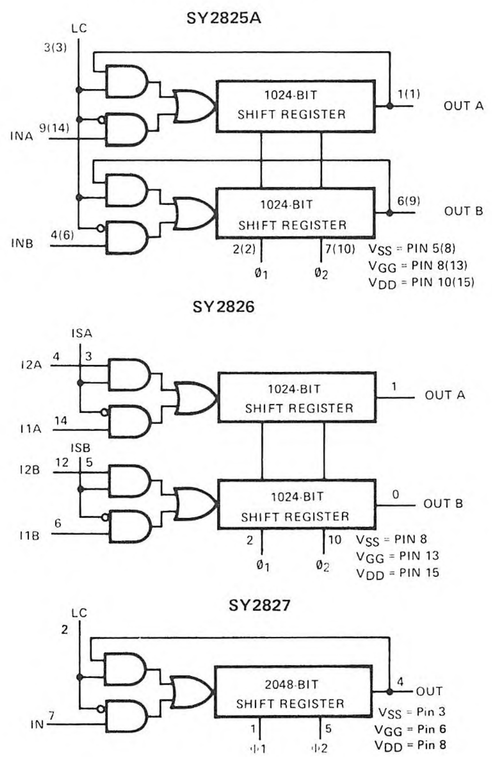
- 6 MH_Z Data Rate
- Recirculate Gates On Chip

The SY2825/26/27 are 2048-bit dynamic shift registers designed with Synertek's ion-implanted silicon gate technology. The 2825 is a dual 1024-bit device with on-chip recirculate and a load control (LC) common to both registers. When LC is HIGH, the two registers recirculate data; when LC is LOW new data is entered through the data inputs. The SY2826 is similar, but each register has two data inputs selected by separate input select (IS) signals. The SY2827 is a single 2048-bit register with on-chip recirculate and a load control. All the devices can drive one standard TTL load. The select, load command, and data inputs may be driven by TTL signals. Two high-voltage clock signals, $\phi 1$ and $\phi 2$, are required. Internally, each shift register consists of two multiplexed registers so that a data shift occurs on each $\phi 1$ or $\phi 2$ clock pulse. The data rate, therefore is double the frequency of either clock signal.

CONNECTION DIAGRAMS



BLOCK DIAGRAMS



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SYP2825A	Plastic DIP	0°C to 70°C
SYC2825A	Ceramic DIP	0°C to 70°C
SYP2826	Plastic DIP	0°C to 70°C
SYC2826	Ceramic DIP	0°C to 70°C
SYP2827	Plastic DIP	0°C to 70°C
SYC2827	Ceramic DIP	0°C to 70°C

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SHIFT REGISTERS

DEFINITION OF TERMS

Dynamic Shift Register A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

ϕ_1, ϕ_2 The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at V_{SS}. Data is accepted into the master of each bit during one phase and is transferred to the slave of each bit during the other phase.

$t_{\phi d}$ Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-to-LOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

$t_{\phi pw}$ Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and the data transfer between master and slave or slave and master occurs.

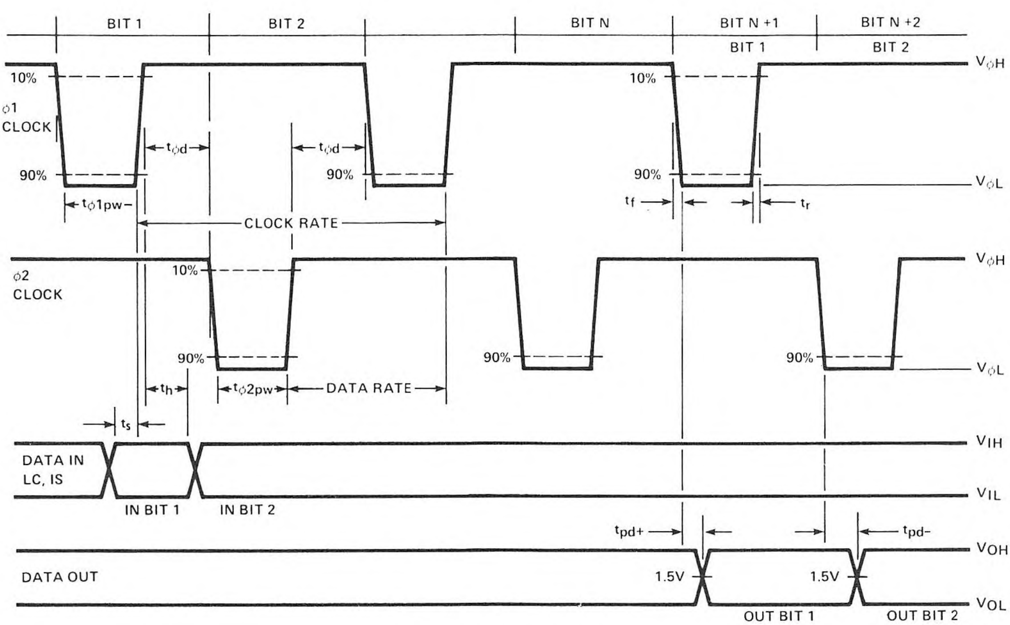
$t_{\Phi t}$ Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

$t_s(D)$ Data set-up time. The time prior to the LOW-to-HIGH transition of Φ during which the data on the data input must be steady to be correctly written into the memory.

$t_h(D)$ Data hold time. The time following rhe LOW-to-HIGH transition of Φ during which the data must be steady. To correctly write data into the register, the data must be applied by $t_s(D)$ before this transition and must not be changed until $t_h(D)$ after this transition.

t_{pd} The delay from a HIGH-to-LOW clock transition to correct data present at the register output.

SWITCHING WAVEFORMS



Clock Rise Time 20ns
Clock Fall Time 20ns
Output Load 1 TTL Load

SHIFT REGISTERS

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature . . . . -65°C to +150°C
Temperature (Ambient)
Under Bias . . . . -55°C to +125°C
DC Input Voltage
with Respect to V_{SS} . . . . -20V to +0.3V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. this is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

OPERATING RANGE

V_{SS} = +5.0V ±5%, V_{GG} = -10.0V to -11.0V, T_A = 0°C to +70°C.

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output High Voltage	I_{OH} = -0.5mA		2.4		V_{SS}	Volts
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA		0.0		0.4	Volts
V_{IH}	Input High Level	Guaranteed input logical High Voltage for all inputs except clocks		V_{SS} -1.0		V_{SS} +0.3	Volts
V_{IL}	Input Low Level	Guaranteed input logical Low Voltage for all inputs except clocks		V_{SS} -10		V_{SS} -4.2	Volts
I_I	Input Leakage Current	V_{IN} = -10V, T_A = 25°C			10	500	nA
I_ϕ	Clock Input Leakage Current	V_ϕ = -15V, T_A = 25°C			50	1000	nA
$V_{\phi H}$	Clock High Level			V_{SS} -1.0		V_{SS} +0.3	Volts
$V_{\phi L}$	Clock Low Level			V_{GG} -0.3		V_{GG} +0.8	Volts
I_{GG}	V_{GG} Current	T_A = 25°C	.01MHz<f_ϕ<0.1MHz		2.5	5	
		V_{SS} = 5.25V	f_ϕ = 1.0MHz		2.5	5	mA
		V_{GG} = -11.0V	f_ϕ = 3.0MHz		2.5	5	
I_{DD}	V_{DD} Current	$V_{\phi L}$ = -11.0V	.01MHz<$_\phi$<0.1MHz		3	4	
		$t_{\phi pw}$ = 115ns	f_ϕ = 1.0MHz		15	20	mA
		Data = 11110000...	f_ϕ = 3.0MHz		30	40	

Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = -10.5V and 25°C ambient.

SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS OVER OPERATING RANGE

Parameters	Definition	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
f_D	Data Rate (Note 2)		0.02		6.0	MHz
f_ϕ	Clock Frequency		0.01		3.0	MHz
$t_{\phi d}$	Delay Between Clocks (Note 3)		10			ns
$t_{\phi pw}$	Clock Low Time	$t_{\phi t}$ = 20ns	0.115		10	μs
$t_{\phi t}$	Clock Rise and Fall Times	10% to 90%			0.5	μs
t_s	Set-Up Time, Data and Select Inputs (See Definitions)				40	ns
t_h	Hold Time, Data and Select Inputs (See Definitions)				20	ns
t_{pd}	Delay, Clock to Data Out	C_L = 15pF			80	ns
$C_{(D)}$	Capacitance, Data Input				5	pF
$C_{(S)}$	Capacitance, Select Input or L_C	f = 1 MHz, V_{IN} = 0V			7	pF
$C_{(\phi)}$	Capacitance, Clock Input	All other pins at GND		80	110	pF

Note: 2. The Data Rate is twice the frequency of either clock phase.

TRUTH TABLES

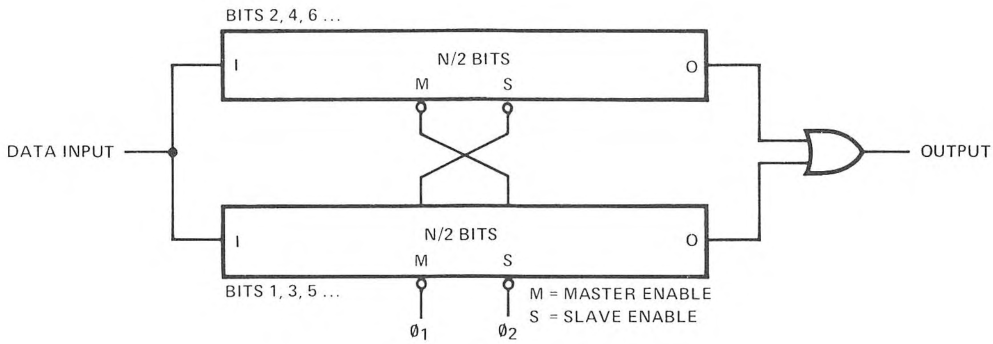
SY2825A and 2827

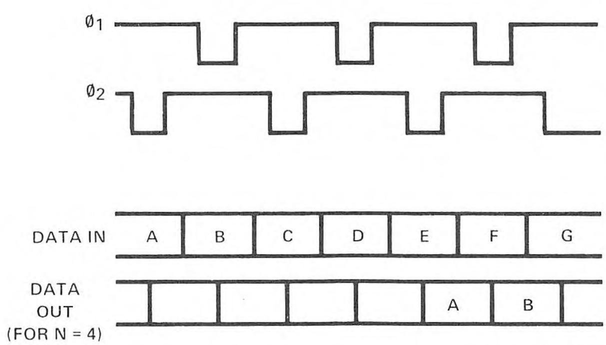
LC	IN	OUT	DATA ENTERED
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

SY2826

IS	INPUT 1	INPUT 2	DATA ENTERED
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

FUNCTIONAL EQUIVALENT OF EACH REGISTER





Since the two registers shift on opposite clock pulses, a new data bit is entered on both $\phi 1$ and $\phi 2$. Data entering the register on $\phi 1$ will appear at the output on $\phi 1$ (from the negative edge of $\phi 1$ to the negative edge of $\phi 2$).

Random Access Memories

Random Access Memories

Synertek®

1024x1 Dynamic Random Access Memory

SY1103A-1

MEMORY PRODUCTS

RAMs

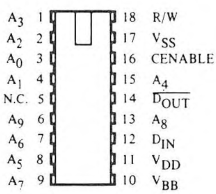
- No precharge clock
- Lower chip enable capacitance—reduces clock driver requirements
- Plug-in compatible with 1103 and 1103-1
- 145 ns access time
- 10-bit address register on-chip
- Simple memory expansion
- NDRO operation
- OR-tie capability

Synertek's SY1103A-1 is a fully decoded 1024-bit dynamic silicon gate RAM which uses ion implanted load devices for superior performance. The 1024 x 1 organization and the low capacitance cenable signal allow for easy expanion in both the word and bit directions. The critical precharge clock needed with standard 1103 RAMs has been eliminated in the SY1103A-1 design. System timing requirements have been further simplified by the incorporation of on-chip address holding registers which allow address stable timing to be only a small portion of the memory cycle. Memory refresh is required every 1 millisecond and can be readily accomplished by sequencing through the 32 combinations of address lines A_0 through A_4. Readout is non-destructive and the $\overline{D}_{out}$ line may be directly OR tied, reducing the number of sense amplifiers needed at the system level.

The high speed, ease of use, and low cost of the SY1103A-1 permit its use in a wide range of computer, minicomputer, and peripheral systems.

The SY1103A-1 is manufactured with ion implanted silicon gate technology which provides a dramatic improvement in features and functional density over standard MOS processes.

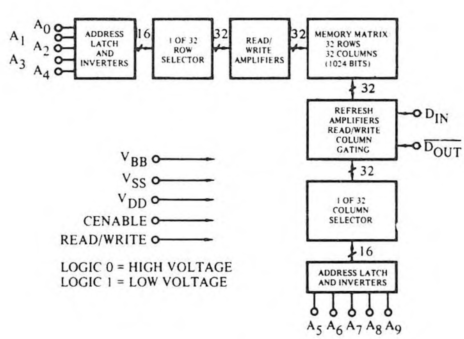
PIN CONFIGURATION



PIN NAMES

D_{IN}	DATA INPUT	NC	NO EXTERNAL CONNECTION REQUIRED (See Note 2, Page 3)
A_0-A_9	ADDRESS INPUTS	CE	CHIP ENABLE
R/W	READ/WRITE	$\overline{D_{OUT}}$	DATA OUTPUT

BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SYP1103A-1	Plastic Dip	0°C to + 70°C
SYC1103A-1	Ceramic Dip	0°C to + 70°C

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RAMs

Absolute Maximum Ratings*

Temperature Under Bias . . . . 0°C to 70°C
Storage Temperature . . . . 65°C to +150°C
Supply Voltages V_{DD} and V_{SS} with Respect to V_{BB} . -25V to 0.3V
All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB} . . . . -25V to 0.3V
Power Dissipation 1.0W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. and Operating Characteristics

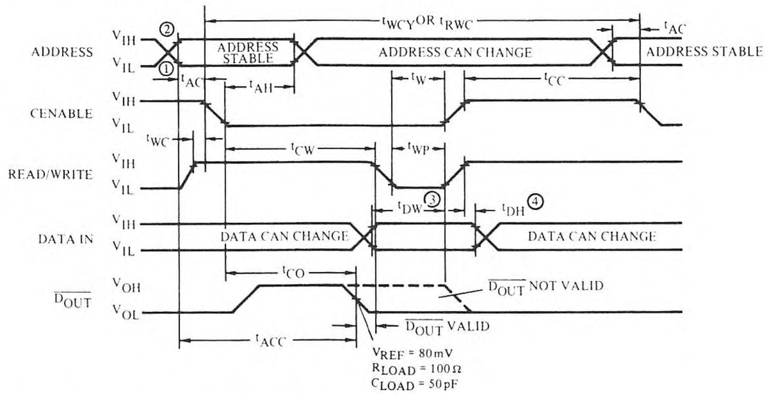
T_A = 0°C to +55°C, V_{SS}[1] = 19V ± 5%, $(V_{BB} - V_{SS})$[2] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			10	µA	V_{IN} = 0V
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0V
I_{BB}	V_{BB} Supply Current			100	µA	
I_{DD1}	Supply Current During Cenable On		4	11	mA	Cenable = 0V; T_A = 25°C
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; T_A = 25°C
I_{DDAV}	Average Supply Current		17	25	mA	Cycle Time = 340ns; T_A = 25°C
V_{IL}	Input Low Voltage	V_{DD}-1		V_{DD}+1	V	
V_{IH}	Input High Voltage	V_{SS}-1		V_{SS} +1	V	
I_{OH1}	Output High Current	1150	1300	7000	µA	T_A = 25°C; R_{LOAD}[4] = 100Ω
I_{OH2}	Output High Current	900	1150	7000	µA	T_A = 55°C; R_{LOAD}[4] = 100Ω
I_{OL}	Output Low Current		See Note Three			R_{LOAD}[4] = 100Ω
V_{OH1}	Output High Voltage	115	130	700	mV	T_A = 25°C; R_{LOAD}[4] = 100Ω
V_{OH2}	Output High Voltage	90	115	700	mV	T_A = 55°C; R_{LOAD}[4] = 100Ω
V_{OL}	Output Low Voltage		See Note Three			

NOTES:
1. The V_{SS} current drain is equal to $(I_{DD} + I_{OH})$.
2. $(V_{BB} - V_{SS})$ supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the SY1103A-1 plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



NOTES:

① V_{DD} + 2V
② V_{SS} - 2V
} t_T is defined as the transition between these two points.

③ t_{DW} is referenced to point ① of the rising edge of cenable or Read/Write, whichever occurs first.

④ t_{DH} is referenced to point ② of the rising edge of cenable or Read/Write, whichever occurs first.

A.C. Characteristics

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	50		ns	
t_{CC}	Cenable Off Time	120		ns	

READ CYCLE

Symbol	Test	Min	Max.	Unit	Conditions
t_{RC}	Read Cycle	300		ns	t_T = 20ns; C_{LOAD} = 50pF, R_{LOAD} = 100Ω, V_{REF} = 80mV
t_{CV}	Cenable on Time	140	500	ns	
t_{CO}	Cenable Output Delay		125	ns	
t_{ACC}	ADDRESS TO OUTPUT ACCESS		145	ns	t_{AC} min. + t_{CO} + 1t_T(20ns)

WRITE OR READ/WRITE CYCLE

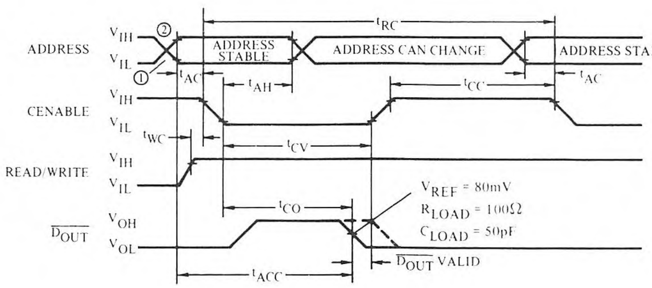
Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	340		ns	t_T = 20ns
t_{RWC}	Read/Write Cycle	340		ns	
t_{CW}	Cenable to Read/Write Delay	140	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	C_{LOAD} = 50pF; R_{LOAD} = 100Ω; V_{REF} = 80mV
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		125	ns	
t_{WC}	Read/Write to Cenable	0		ns	

CAPACITANCE [1] $T_A = 25°C$

Symbol	Test	Typ.	Max.	Unit	Conditions	
C_{AD}	Address Capacitance	5	7	pF	$V_{IN} = V_{SS}$	
C_{CE}	Cenable Capacitance	14	18	pF	$V_{IN} = V_{SS}$	f = 1 MHz. All unused pins are at A.C. ground. $V_{BB} = V_{SS}$ + 3V.
C_{RW}	Read/Write Capacitance	11	15	pF	$V_{IN} = V_{SS}$	
C_{IN1}	Data Input Capacitance	3	4	pF	Cenable = 0V, $V_{IN} = V_{SS}$	
C_{IN2}	Data Input Capacitance	3	4	pF	Cenable = V_{SS}	
C_{OUT}	Data Output Capacitance	2	3	pF	V_{OUT} = 0V	
[2]$C_{PIN\ 5}$	Dummy Clock Capacitance	12	18	pF		

NOTES: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.
2. When mixing SY1103A-1 in 1103-1 system, this load will preserve system clock timing.

READ CYCLE



NOTES:

① V_{DD} + 2V
② V_{SS} - 2V

t_T is defined as the transition between these two points.

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Printed in U.S.A. 175

1024 x 1 Dynamic Random Access Memory

SY1103A-X

Synertek®

MEMORY PRODUCTS

- No precharge clock
- Lower chip enable capacitance - reduces clock driver requirements
- Plug-in compatible with 1103-X & 1103-1
- t_{CO} = 90 ns
- 10-bit address register on-chip
- Simple memory expansion
- NDRO operation
- OR-tie capability

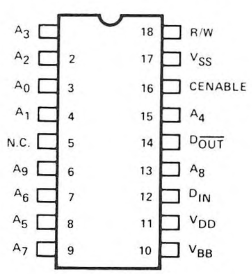
RAMs

Synertek's SY1103A-X is a fully decoded 1024-bit dynamic silicon gate RAM which uses ion implanted load devices for superior performance. The 1024 x 1 organization and the low capacitance cenable signal allow for easy expansion in both the word and bit directions. The critical precharge clock needed with standard 1103 RAMs has been eliminated in the SY1103A-X design. System timing requirements have been further simplified by the incorporation of on-chip address holding registers which allow address stable timing to be only a small portion of the memory cycle. Memory refresh is required every 1 millisecond and can be readily accomplished by sequencing through the 32 combinations of address lines A_0 through A_4. Readout is non-destructive and the D_{out} line may be directly OR tied, reducing the number of sense amplifiers needed at the system level.

The high speed, ease of use, and low cost of the SY1103A-X permit its use in a wide range of computer, minicomputer, and peripheral systems.

The SY1103A-X is manufactured with ion implanted silicon gate technology which provides a dramatic improvement in features and functional density over standard MOS processes.

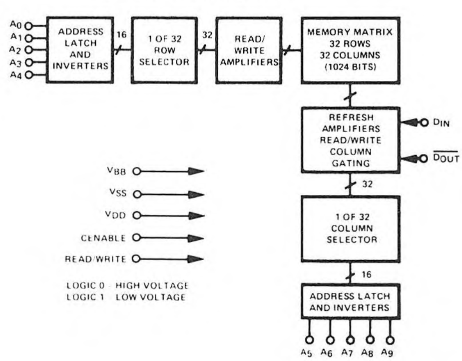
PIN CONFIGURATION



PIN NAMES

D_{IN}	Data Input	NC	No External Connection Required (See Note 2, Page 3)
A_0-A_9	Address Inputs	CE	Chip Enable
R/W	Read Write	D_{OUT}	Data Output

BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SYP1103A-X	Plastic DIP	0°C to 70°C
SYC1103A-X	Ceramic DIP	0°C to 70°C

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to 70°C
Storage Temperature	65°C to +150°C
Supply Voltages V_{DD} and V_{SS} with respect to V_{BB}	-25V to 0.3V
All Input or Output Voltages with Respect to the most Positive Supply Voltage, V_{BB}	-25V to 0.3V
Power Dissipation	1.0W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

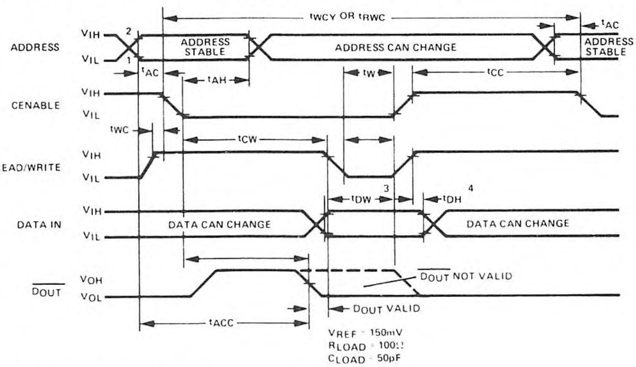
T_A = 0°C to 70°C, V_{SS}[1] = 19V ±5%, (V_{BB} - V_{SS})[2] = 3V to 4V, V_{DD} = 0V unless otherwise specified.

Symbol	Test	Min.	Typ.	Max.	Unit	Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0V
I_{BB}	V_{BB} Supply Current			100	μA	
I_{DD1}	Supply Current During Cenable On		6	11	mA	Cenable = 0V; T_A = 25°C
I_{DD2}	Supply Current During Cenable Off		0.01	0.5	mA	Cenable = V_{SS}; T_A = 25°C
I_{DDAV}	Average Supply Current		20	25	mA	Cycle Time = 300ns; T_A = 25°C
V_{IL}	Input Low Voltage	V_{DD}-1		V_{DD}+1	V	
V_{IH}	Input High Voltage	V_{SS}-1		V_{SS}+1	V	
I_{OH1}	Output High Current	2200	4500	7000	μA	T_A = 25°C, R_{LOAD}[4] = 100Ω
I_{OH2}	Output High Current	2000	4000	7000	μA	T_A = 70°C, R_{LOAD}[4] = 100Ω
I_{OL}	Output Low Current		See Note Three			R_{LOAD}[4] = 100Ω
V_{OH1}	Output High Voltage	220	450	700	mV	T_A = 25°C, R_{LOAD}[4] = 100Ω
V_{OH2}	Output High Voltage	200	400	700	mV	T_A = 70°C, R_{LOAD}[4] = 100Ω
V_{OL}	Output Low Voltage		See Note Three			

NOTES:

1. The V_{SS} current drain is equal to (I_{DD} + I_{OH}).
2. (V_{BB} - V_{SS}) supply should be applied at or before V_{SS}.
3. The output current when reading a low output is the leakage current of the SY1103A-X plus external noise coupled into the output line from the clocks. V_{OL} equals I_{OL} across the load resistor.
4. This value of load resistance is used for measurement purposes. In applications the resistance may range from 100Ω to 1 kΩ.

WRITE OR READ/WRITE CYCLE Timing illustrated for minimum cycle.



NOTES:

1. V_{DD} + 2V
2. V_{SS} - 2V

} t_T is defined as the transition between these two points.

3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of cenable or Read/Write, whichever occurs first.

A.C. CHARACTERISTICS

READ, WRITE, AND READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		1	ms	
t_{AC}	Address to Cenable Set Up Time	0		ns	
t_{AH}	Address Hold Time	50		ns	
t_{CC}	Cenable Off Time	110		ns	

READ CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{RC}	Read Cycle	260(3)		ns	t_T = 20ns
t_{CV}	Cenable on Time	110	500	ns	C_{LOAD} = 50pF
t_{CO}	Cenable Output Delay		90	ns	R_{LOAD} = 100Ω
t_{ACC}	ADDRESS TO OUTPUT ACCESS		110(3)	ns	t_{AC} min. $+t_{CO}$ $+1t_T$(20ns) V_{REF} = 150mV

WRITE CYCLE OR READ/WRITE CYCLE

Symbol	Test	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle	300(3)		ns	t_T = 20ns
t_{RWC}	Read/Write Cycle	300(3)		ns	
t_{CW}	Cenable to Read/Write Delay	110	500	ns	
t_{WP}	Read/Write Pulse Width	20		ns	
t_W	Read/Write Set Up Time	20		ns	
t_{DW}	Data Set Up Time	40		ns	
t_{DH}	Data Hold Time	10		ns	
t_{CO}	Output Delay		90	ns	C_{LOAD} = 50pF; R_{LOAD} = 100Ω V_{REF} = 150mV
t_{WC}	Read/Write to Cenable	0		ns	

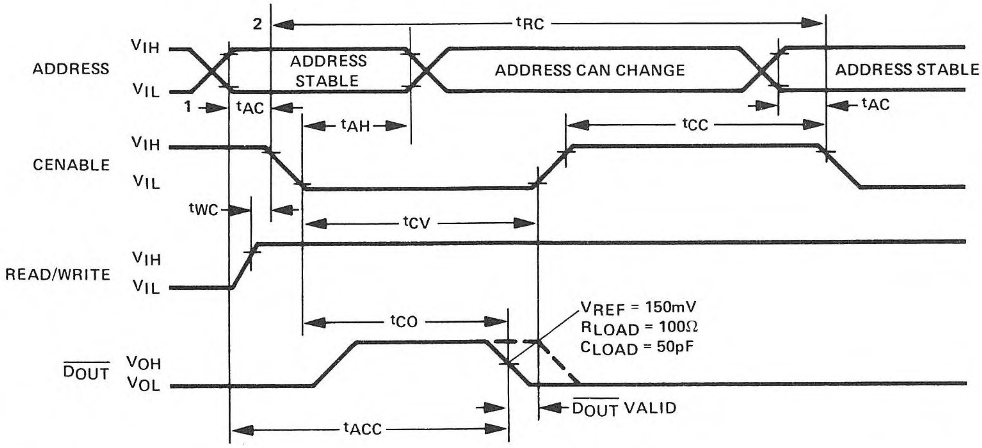
CAPACITANCE $T_A = 25°C$

Symbol	Test	Typ Plastic	Plastic Pkg Max	Ceramic Pkg Max	Unit	Conditions	
C_{AD}	Address Capacitance	5	7	7	pF	$V_{IN} = V_{SS}$	f = 1MHz. All Unused pins are at A.C. ground. $V_{BB} = V_{SS} + 3V$.
C_{CE}	Cenable Capacitance	14	18	18	pF	$V_{IN} = V_{SS}$	
C_{RW}	Read/Write Capacitance	11	15	15	pF	$V_{IN} = V_{SS}$	
C_{IN1}	Data Input Capacitance	2	5	5	pF	Cenable = 0V $V_{IN} = V_{SS}$	
C_{IN2}	Data Input Capcitance	2	5	5	pF	Cenable = V_{SS}	
C_{OUT}	Data Output Capacitance	2	3	5	pF	V_{OUT} = 0V	
[2] $C_{PIN\ 5}$	Dummy Clock Capacitance	10	15	15	pF		

NOTE: 1. These parameters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.
2. When mixing SY1103A-X in 1103-X system, this load will preserve system clock timing.
3. If t_T is reduced to 10ns, these parameters will change accordingly (t_{ACC} = 100ns).

RAMs

READ CYCLE



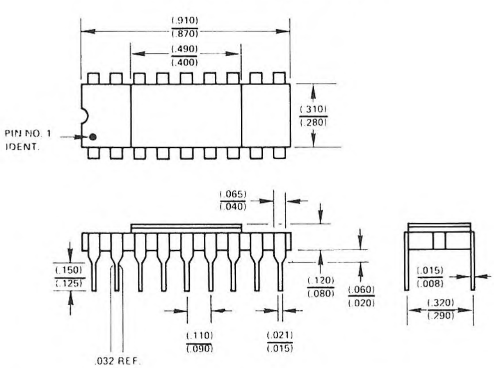
NOTES:

1. $V_{DD} + 2V$
2. $V_{SS} - 2V$

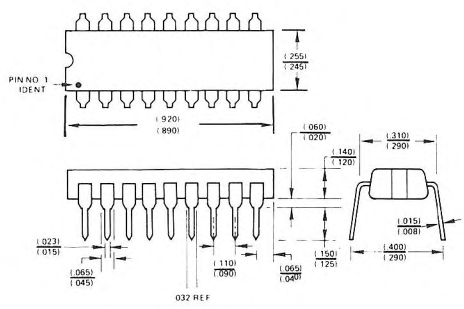
} t_T is defined as the transition between these two points.

PACKAGE DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



256x4 Static Random Access Memory

SY2101

MEMORY PRODUCTS

Synertek®

RAMs

- 256x4 Organization to Meet Needs For Small System Memories
- Access Time — 250/350/450/500/ns
- Single +5V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Simple Memory Expansion — Two Chip Enable Inputs
- Inputs Protected — All Inputs Have Protection Against Static Charge
- Low Cost Packaging — 22 Pin Plastic Dual-In-Line Configuration
- Low Power — Typically 150 mW
- Three-State Output — OR-Tie Capability
- Output Disable Provided For Ease of Use in Common Data Bus Systems

The SY2101 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

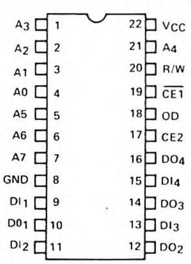
The SY2101 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two Chip Enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bi-directional logic.

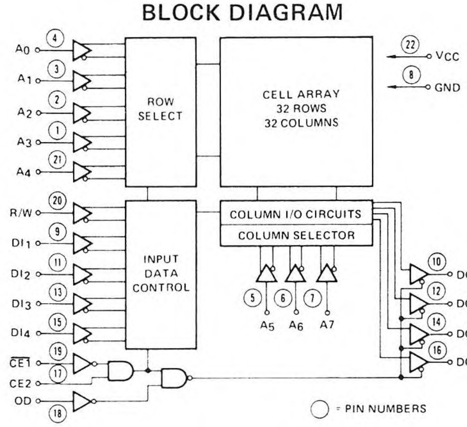
The SY2101 is fabricated with N-channel ion implanted silicon gate technology. This technology allows the design and production of high-performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SYP2101-1	Plastic DIP	0°C to 70°C
SYC2101-1	Ceramic DIP	0°C to 70°C
SYP2101A-2	Plastic DIP	0°C to 70°C
SYC2101A-2	Ceramic DIP	0°C to 70°C
SYP2101A	Plastic DIP	0°C to 70°C
SYC2101A	Ceramic DIP	0°C to 70°C
SYP2101A-4	Plastic DIP	0°C to 70°C
SYC2101A-4	Ceramic DIP	0°C to 70°C

PIN NAMES

D_{IN}	DATA INPUT	OD	OUTPUT DISABLE
A_0–A_7	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	2101-1 Min.	2101-1 Typ.(1)	2101-1 Max.	2101A-2 2101A, 2101A-4 Min.	2101A-2 2101A, 2101A-4 Typ.(1)	2101A-2 2101A, 2101A-4 Max.	Unit	Test Conditions
I_{LI}	Input Current			10			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current(2)			15			15	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	I/O Leakage Current(2)			-50			-50	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		30	60		30	50	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			70			55	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		+0.65	-0.5		+0.8	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			+0.45			+0.4	V	I_{OL} = 3.2mA (I_{OL} = 2.0mA 2101-1)
V_{OH}	Output High Voltage	2.2			2.4			V	I_{OH} = -150μA

NOTE: 1. Typical Values are for T_A = 25°C and nominal supply voltage.
2. Input and Output tied together.

A.C. CHARACTERISTICS — SY2101-1

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	500		ns
t_A	Access Time		500	ns
t_{CO}	Chip Enable To Output		350	ns
t_{OD}	Output Disable To Output		300	ns
t_{DF}[1]	Data Output to High Z State	0	150	ns
t_{OH}	Previous Data Read Valid after change of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	500		ns
t_{AW}	Write Delay	100		ns
t_{CW}	Chip Enable To Write	400		ns
t_{DW}	Data Setup	280		ns
t_{DH}	Data Hold	100		ns
t_{WP}	Write Pulse	300		ns
t_{WR}	Write Recovery	50		ns

A.C. CHARACTERISTICS – SY2101A-2

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	250		ns
t_A	Access Time		250	ns
t_{CO}	Chip Enable To Output		130	ns
t_{OD}	Output Disable To Output		100	ns
t_{DF}[1]	Data Output to High Z State	0	100	ns
t_{OH}	Previous Data Read Valid after change of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	250		ns
t_{AW}	Write Delay	0		ns
t_{CW}	Chip Enable To Write	150		ns
t_{DW}	Data Setup	150		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	200		ns
t_{WR}	Write Recovery	0		ns

A.C. CHARACTERISTICS – SY2101A

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	350		ns
t_A	Access Time		350	ns
t_{CO}	Chip Enable To Output		170	ns
t_{OD}	Output Disable To Output		140	ns
t_{DF}[1]	Data Output to High Z State	0	130	ns
t_{OH}	Previous Data Read Valid after change of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	350		ns
t_{AW}	Write Delay	0		ns
t_{CW}	Chip Enable To Write	200		ns
t_{DW}	Data Setup	200		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	250		ns
t_{WR}	Write Recovery	0		ns

NOTE: 1 t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.

RAMs

A.C. CHARACTERISTICS — SY2101A-4

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	450		ns
t_A	Access Time		450	ns
t_{CO}	Chip Enable To Output		200	ns
t_{OD}	Output Disable To Output		170	ns
t_{DF} [1]	Data Output to High Z State	0	150	ns
t_{OH}	Previous Data Read Valid after change of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	450		ns
t_{AW}	Write Delay	0		ns
t_{CW}	Chip Enable To Write	250		ns
t_{DW}	Data Setup	250		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	300		ns
t_{WR}	Write Recovery	0		ns

A.C. CONDITIONS OF TEST

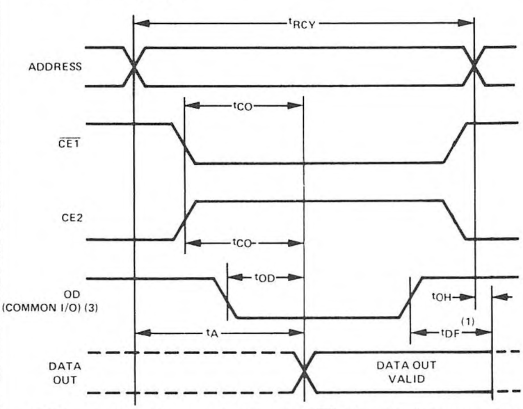
	2101A-2 2101A 2101A-4	2101-1
Input Pulse Levels:	+0.8V to 2.0V	+0.65V to 2.2V
Input Pulse Rise & Fall Times:	10ns	10ns
Timing Measurement Reference Level: Inputs:	1.5V	1.5V
Outputs:	0.8V & 2.0V	0.8V & 2.0V
Output Load:	1 TTL Gate & C_L = 100pF	1 TTL Gate & C_L = 100pF

CAPACITANCE T_A = 25°C, f = 1MHz

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8	pF
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12	pF

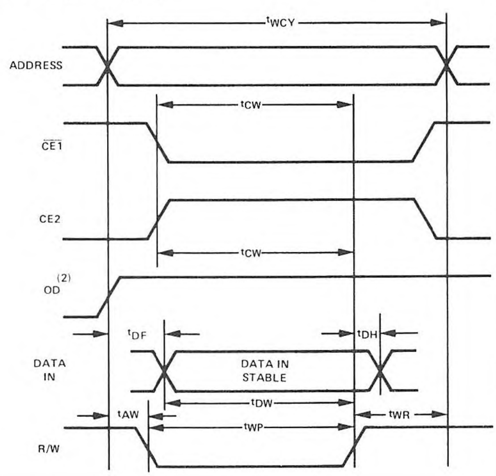
TIMING DIAGRAMS

READ CYCLE



NOTES:
1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.
2. During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
3. OD should be tied low for separate I/O operation.

WRITE CYCLE



256x4 Static Random Access Memory

Synertek®

SY21H01

MEMORY PRODUCTS

- 256x4 Organization to Meet Needs for Small System Memories
- Access Time – 175/200 ns
- Single +5V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Simple Memory Expansion – Two Chip Enable Inputs
- Inputs Protected – All Inputs Have Protection Against Static Charge
- Low Cost Packaging – 22 Pin Plastic Dual-In-Line Configuration
- Three-State Output – OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

RAMs

The SY21H01 is a 256-word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

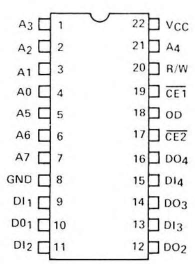
The SY21H01 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two Chip Enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. Output disable is then used to eliminate any bi-directional logic.

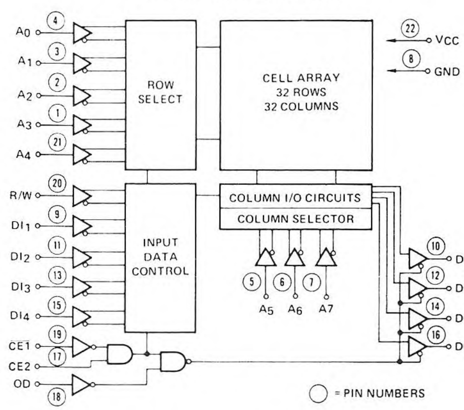
The SY21H01 is fabricated with N-channel ion implanted silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost packaging.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SYP21H01	Plastic DIP	0°C to 55°C
SYC21H01	Ceramic DIP	0°C to 55°C
SYP21H01-2	Plastic DIP	0°C to 55°C
SYC21H01-2	Ceramic DIP	0°C to 55°C

PIN NAMES

DIN	DATA INPUT	OD	OUTPUT DISABLE
A0–A7	ADDRESS INPUTS	DOUT	DATA OUTPUT
R/W	READ/WRITE INPUT	VCC	POWER (+5V)
CE1, CE2	CHIP ENABLE		

RAMs

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 55°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +55°C, V_{CC} = 5V ±5% (Unless Otherwise Specified)

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current[2]			15	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	I/O Leakage Current[2]			−50	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		50	80	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			90	mA	V_{IN} = 5.25V, I_O = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	−0.5		+0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.4	V	I_{OL} = 3.2mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = −150μA

NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Input and Output tied together.

A.C. CHARACTERISTICS – SY21H01

T_A = 0°C to 55°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Unit
READ CYCLE					
t_{RCY}	Read Cycle	175			ns
t_A	Access Time			175	ns
t_{CO}	Chip Enable to Output			110	ns
t_{OD}	Output Disable to Output			90	ns
t_{DF} [1]	Data Output to High Z State	0		70	ns
t_{OH}	Previous Data Read Valid after change of Address	0			ns
WRITE CYCLE					
t_{WCY}	Write Cycle	175			ns
t_{AW}	Write Delay	0			ns
t_{CW}	Chip Enable to Write	100			ns
t_{DW}	Data Setup	100			ns
t_{DH}	Data Hold	0			ns
t_{WP}	Write Pulse	150			ns
t_{WR}	Write Recovery	0			ns

NOTES: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.

A.C. CHARACTERISTICS — SY21H01-2

$T_A = 0°C$ to $+55°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
READ CYCLE					
t_{RCY}	Read Cycle	200			ns
t_A	Access Time			200	ns
t_{CO}	Chip Enable to Output			120	ns
t_{OD}	Output Disable to Output			100	ns
t_{DF} [1]	Data Output to High Z State	0		80	ns
t_{OH}	Previous Data Read Valid after change of Address	0			ns
WRITE CYCLE					
t_{WCY}	Write Cycle	200			ns
t_{AW}	Write Delay	0			ns
t_{CW}	Chip Enable to Write	120			ns
t_{DW}	Data Setup	120			ns
t_{DH}	Data Hold	0			ns
t_{WP}	Write Pulse	170			ns
t_{WR}	Write Recovery	0			ns

NOTE: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.

A.C. CONDITIONS OF TEST

Input Pulse Levels: . . . . +0.8V to 2.0V

Input Pulse Rise & Fall Times: . . . . 10 ns

Timing Measurement Reference Level — Input: 1.5V

Timing Measurement Reference Level — Output: . . . . 0.8V & 2.0V

Output Load: . . . . 1 TTL Gate & C_L = 100 pF

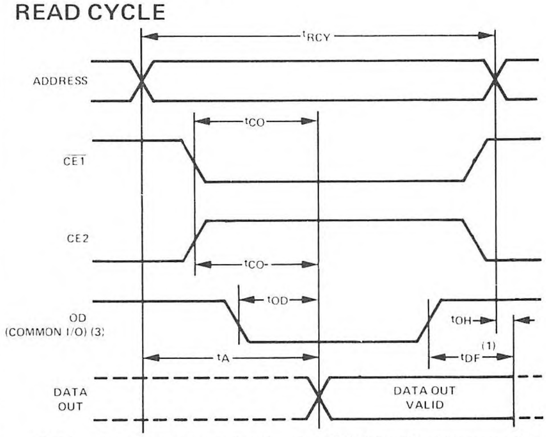
CAPACITANCE $T_A = 25°C$, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8	pF
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	8	12	pF

NOTE: This parameter is periodically sampled and not 100% tested.

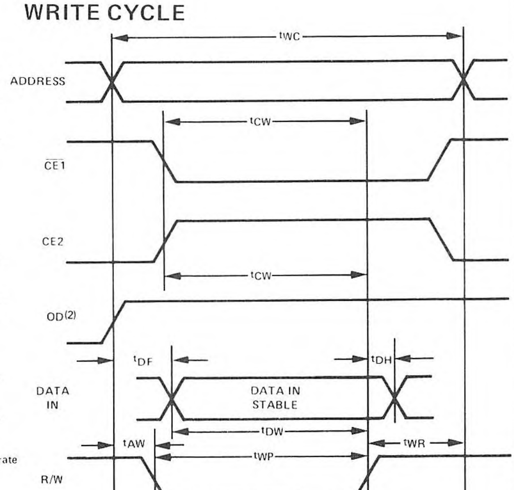
TIMING DIAGRAMS

READ CYCLE



NOTES:
1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, CE2, or OD, whichever occurs first.
2. During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
3. OD should be tied low for separate I/O operation.

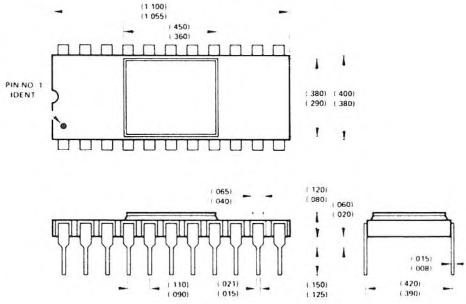
WRITE CYCLE



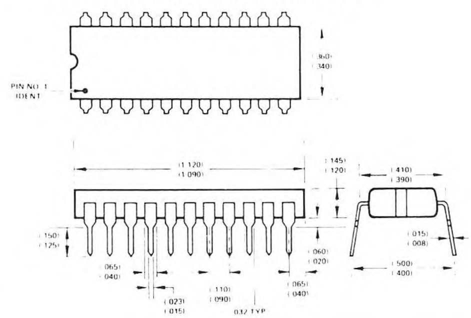
RAMs

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



1024x1 Static Random Access Memory

SY2102

MEMORY PRODUCTS

Synertek®

RAMs

- Single +5 Volt Operation
- Directly TTL Compatible
- Standby Power Mode
- 3-State Outputs
- Low Power Dissipation

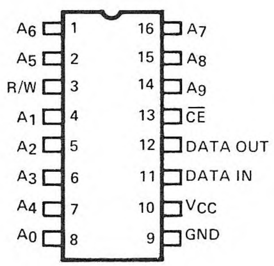
The 2102 family is a series of 1024 word by one bit static random access memory devices fabricated using Synertek's silicon gate technology. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The 2102 family is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

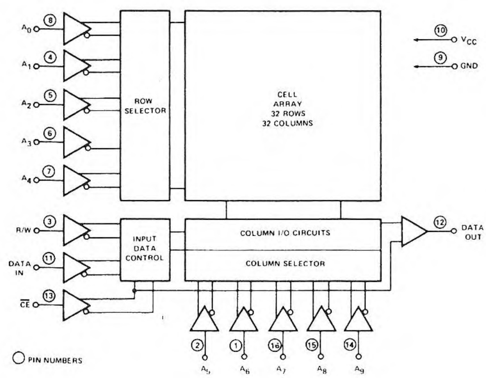
A low standby power version is also available. It has all the same operating characteristics of the 2102-1 with the added feature of 35mW maximum power dissipation in standby and 174mW in operations.

The family is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_{IN}	Data Input	$\overline{CE}$	Chip Enable
A_0-A_9	Address Inputs	D_{OUT}	Data Output
R/W	Read/Write Input	V_{CC}	Power (+5V)

ORDERING INFORMATION

Order Number	Package Type	Access Time	Standby	Temperature Range
SYP2102A-2	Plastic DIP	250nsec	No	0°C to 70°C
SYC2102A-2	Ceramic DIP	250nsec	No	0°C to 70°C
SYP2102A-4	Plastic DIP	450nsec	No	0°C to 70°C
SYC2102A-4	Ceramic DIP	450nsec	No	0°C to 70°C
SYP2102-1	Plastic DIP	500nsec	No	0°C to 70°C
SYC2102-1	Ceramic DIP	500nsec	No	0°C to 70°C
SYP2102-1L	Plastic DIP	500nsec	Yes	0°C to 70°C
SYC2102-1L	Ceramic DIP	500nsec	Yes	0°C to 70°C
SYP2102-6	Plastic DIP	650nsec	No	0°C to 70°C

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

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J-10K-11/77

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	-0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect To Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the divice at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

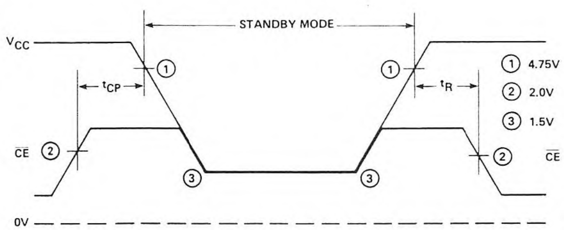
		2102A-4 Limits			2102A-2 Limits			2102-1, 2102-1L 2102A-6 Limits				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10		1	10		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current		1	5		1	5		1	5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current		-1	-10		-1	-10		-1	-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		33	55		45	65		33	55	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	-0.5		0.65	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			2.4			2.2			V	I_{OH} = 100μA

STANDBY CHARACTERISTICS – 2102-IL

T_A = 0°C to 70°C

		Limits				
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	1.5			V	
V_{CES}(1)	$\overline{CE}$ Bias in Standby	2.0			V	2.0V ≤ V_{PD} ≤ V_{CC} Max
		V_{PD}			V	1.5V ≤ V_{PD} < 2.0V
I_{PD1}	Standby Current		15	23	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current		20	30	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			ns	
t_R(2)	Standby Recovery Time	t_{RC}			ns	

STANDBY WAVEFORMS



NOTES:

1. Consider the test conditions as shown: if the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
2. t_R = t_{RC} (READ CYCLE TIME).

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

READ CYCLE

Symbol	Parameter	2102A-2 Limits (ns)		2102-1, 2102-1L Limits (ns)		2102A-4 Limits (ns)		2102A-6 Limits (ns)	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t_{RC}	Read Cycle	250		500		450		650	
t_A	Access Time		250		500		450		650
t_{CO}	Chip Enable to Output Time		130		350		230		400
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40		50	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0	

WRITE CYCLE

Symbol	Parameter	2102A-2 Min.	2102A-2 Max.	2102-1, 2102-1L Min.	2102-1, 2102-1L Max.	2102A-4 Min.	2102A-4 Max.	2102A-6 Min.	2102A-6 Max.
t_{WC}	Write Cycle	250		500		450		650	
t_{AW}	Address to Write Setup Time	20		150		20		200	
t_{WP}	Write Pulse Width	180		300		300		400	
t_{WR}	Write Recovery Time	0		50		0		50	
t_{DW}	Data Setup Time	180		330		300		450	
t_{DH}	Data Hold Time	0		100		0		20	
t_{CW}	Chip Enable to Write Setup Time	180		400		300		550	

A.C. CONDITIONS OF TEST

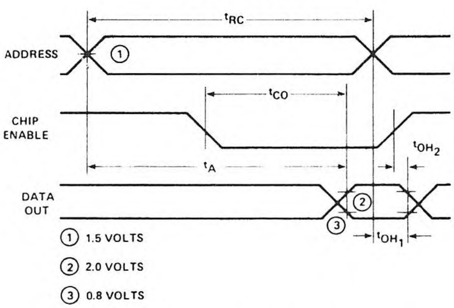
Input Pulse Levels . . . . 0.8 Volt to 2.0 Volt
Input Rise and Fall Times 10nsec
Timing Measurement Reference Levels Inputs . . . . 1.5 Volts
Outputs . . . . 0.8 and 2.0 Volts
Output Load . . . . 1 TTL Gate and $C_L = 100pF$

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

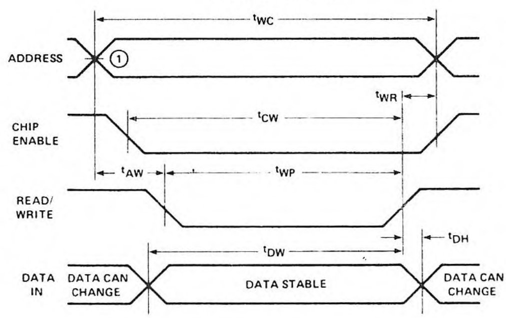
Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	3	5	pF
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	7	10	pF

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE

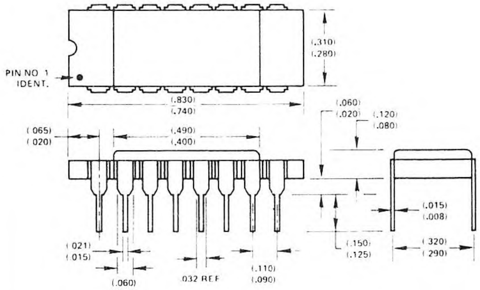


NOTE: 1. This parameter is periodically sampled and is not 100% tested.

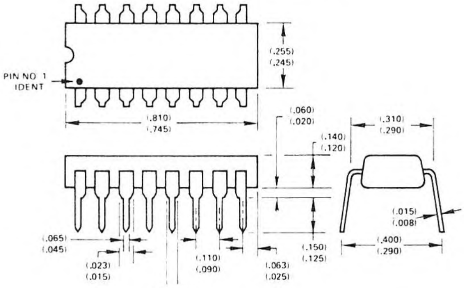
RAMs

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



1024 x 1 Static Random Access Memory

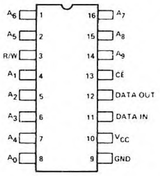
SY21H02

Synertek®

MEMORY PRODUCTS

- 175/200 nsec Maximum Access Times
- Maximum Times Apply over Temperature Range and Supply Voltage Variation

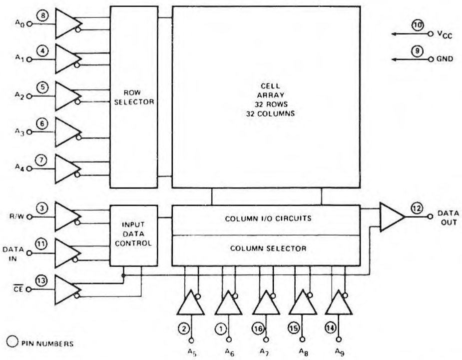
PIN CONFIGURATION



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SYP21H02	Plastic DIP	0°C to +55°C
SYC21H02	Ceramic DIP	0°C to +55°C
SYP21H02-2	Plastic DIP	0°C to +55°C
SYC21H02-2	Ceramic DIP	0°C to +55°C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin with Respect to Ground	-0.5V to +7V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $T_A = 0°C$ to $+55°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Limits Min.	Limits Typ. (1)	Limits Max.	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	Output Leakage Current			5	μA	$\overline{CE} = 2.0V$, $V_{OUT} = 2.4$ to V_{CC}
I_{LOL}	Output Leakage Current			-10	μA	$\overline{CE} = 2.0V$, $V_{OUT} = 0.4V$
I_{CC1}	Power Supply Current		50	80	mA	All Inputs = 5.25V, Data Out Open, $T_A = 25°C$
I_{CC2}	Power Supply Current			90	mA	All Inputs = 5.25V, Data Out Open, $T_A = 0°C$
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	$I_{OL} = 2.1mA$
V_{OH}	Output "High" Voltage	2.4			V	$I_{OH} = -100\mu A$

NOTE: 1. Typical values are for $T_A = 25°C$ and nominal supply voltage.

RAMs

A.C. CHARACTERISTICS $T_A = 0°C$ to $+55°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter (All Limits in ns)	SY21H02		SY21H02-2	
		Min.	Max.	Min.	Max.
READ CYCLE					
t_{RC}	Read Cycle	175		200	
t_A	Access Time		175		200
t_{CO}	Chip Enable to Output Time		110		120
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0	
WRITE CYCLE					
t_{WC}	Write Cycle	175		200	
t_{AW}	Address to Write Setup Time	20		20	
t_{WP}	Write Pulse Width	120		150	
t_{WR}	Write Recovery Time	0		0	
t_{DW}	Data Setup Time	120		150	
t_{DH}	Data Hold Time	0		0	
t_{CW}	Chip Enable to Write Setup Time	120		150	

A.C. TEST CONDITIONS

Input Pulse Levels . . . . 0.8 to 2.0 Volts
Input Rise and Fall Times . . . . 10 nsec
Timing Measurement Reference Levels: Inputs . . . . 1.5 Volts
Outputs . . . . 0.8 and 2.0 Volts
Output Load . . . . 1 TTL Gate and C_L = 100 pF

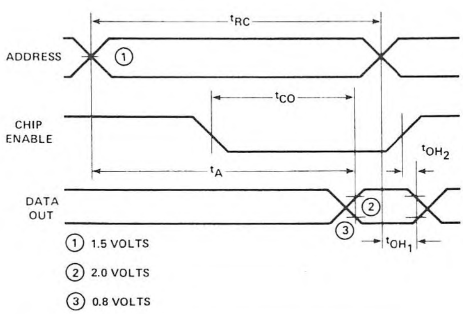
CAPACITANCE (1) $T_A = 25°C$, f = 1MHz

Symbol	Test	Typ (2)	Max	Unit
C_{IN}	Input Capacitance (All input pins) V_{IN} = 0V	3	5	pF
C_{OUT}	Output Capacitance V_{OUT} = 0V	7	10	pF

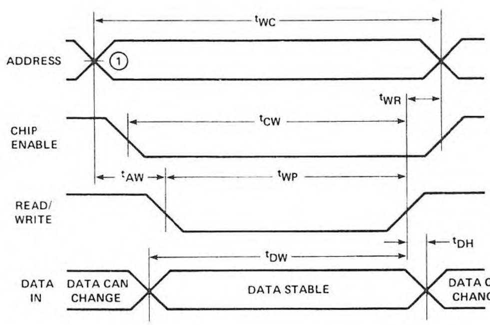
NOTE: 1. This parameter is periodically sampled and not 100% tested.
NOTE: 2. Typical values are for T_A = 25° C and nominal supply voltage.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE



1024 x 1 Static Random Access Memory

SY21L02

Synertek®

MEMORY PRODUCTS

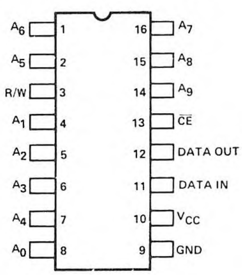
- Low Power Maximum I_{CC} = 15mA (SY21L02)
- Directly TTL Compatible
- 200mV Noise Immunity
- Single +5V Supply
- Standby Power Mode – 23mW

RAMs

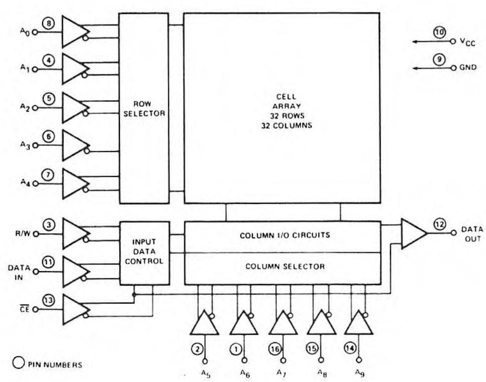
The Synertek SY21L02 is a 1024 word by one bit static random access memory element using N-channel depletion mode silicon gate devices. It uses fully stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

The SY21L02 is designed for memory applications where very low power dissipation is required in the operating and standby modes. It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable ($\overline{CE}$) lead allows easy selection of an individual package when outputs are OR-tied.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP21L02	Plastic DIP	1µsec	0°C to 70°C
SYC21L02	Ceramic DIP	1µsec	0°C to 70°C
SYP21L02-1	Plastic DIP	500nsec	0°C to 70°C
SYC21L02-1	Ceramic DIP	500nsec	0°C to 70°C
SYP21L02A	Plastic DIP	350nsec	0°C to 70°C
SYC21L02A	Ceramic DIP	350nsec	0°C to 70°C
SYP21L02B	Plastic DIP	400nsec	0°C to 70°C
SYC21L02B	Ceramic DIP	400nsec	0°C to 70°C

21L02 PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

NOTE: An "L" suffix (SYP21L02L, SYC21L02BL, etc.) indicates standby operation.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

*COMMENTS

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RAMs

DC AND OPERATING CHARACTERISTICS (SY21L02)

T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			10	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 4.0V
I_{LOL}	Output Leakage Current			–100	μA	$\overline{CE}$ = 2.2V, V_{OUT} = 0.45V
I_{CC1}	Power Supply Current		11	14	mA	All Inputs = 5.25V Data Out Open T_A = 25°C
I_{CC2}	Power Supply Current		12	15	mA	All Inputs = 5.25V Data Out Open T_A = 0°C
V_{IL}	Input "Low" Voltage	–0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 1.9mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = –100μA

(1) Typical values are for T_A = 25°C and nominal supply voltage.

DC AND OPERATING CHARACTERISTICS (SY21L02-1, SY21L02A, SY21L02B)

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.(1)	Max.		
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current			5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Output Leakage Current			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
V_{IL}	Input "Low" Voltage	-0.5		0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	I_{OL} = 3.2mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -100μA
I_{CC1}	Power Supply Current: SY21L02B		20	26	mA	All Inputs = 5.25V, Data
	SY21L02A		22	26	mA	Out Open, T_A = 25°C
	SY21L02-1		24	34	mA	
I_{CC2}	Power Supply Current: SY21L02B			30	mA	All Inputs = 5.25V, Data
	SY21L02A			30	mA	Out Open, T_A = 0°C
	SY21L02-1			40	mA	

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

STANDBY CHARACTERISTICS (SY21L02L, SY21L02-1L, SY21L02AL, SY21L02BL)

T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	1.5			V	
V_{CES}(2)	$\overline{CE}$ Bias in Standby	2.0			V	$2.0V \leqslant V_{PD} \leqslant V_{CC}$ Max.
		V_{PD}			V	$1.5V \leqslant V_{PD} < 2.0V$
I_{PD1}	Standby Current Drain		9	10	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current Drain		11	12	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			ns	
t_R(3)	Standby Recovery Time	t_{RC}			ns	

NOTE 1: Typical values are for T_A = 25°C and nominal supply voltage.

NOTE 2: Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min.), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.

NOTE 3: $t_R = t_{RC}$ (READ CYCLE TIME).

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	SY21L02		SY21L02-1		SY21L02A		SY21L02B		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
READ CYCLE										
t_{RC}	Read Cycle	1000		500		350		400		nsec
t_A	Access Time		1000		500		350		400	nsec
t_{CO}	Chip Enable to Output Time		500		350		180		150	nsec
t_{OH1}	Previous Read Data Valid with Respect to Address	50		50		40		40		nsec
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0		nsec
WRITE CYCLE										
t_{WC}	Write Cycle	1000		500		350		400		nsec
t_{AW}	Address to Write Setup Time	200		150		20		20		nsec
t_{WP}	Write Pulse Width	750		300		250		150		nsec
t_{WR}	Write Recovery Time	50		50		0		0		nsec
t_{DW}	Data Setup Time	800		330		250		125		nsec
t_{DH}	Data Hold Time	100		100		0		0		nsec
t_{CW}	Chip Enable to Write Setup Time	900		400		250		150		nsec

CAPACITANCE T_A = 25°C, f = 1MHz

Symbol	Test	Typ.	Max.	Units
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	3	5	pF
C_{OUT}	Output Capacitance V_{OUT} = 0V	7	10	pF

NOTE: This parameter is periodically sampled and is not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels: +0.65 Volt to 2.2 Volt

Input Pulse Rise and Fall Times: 20nsec

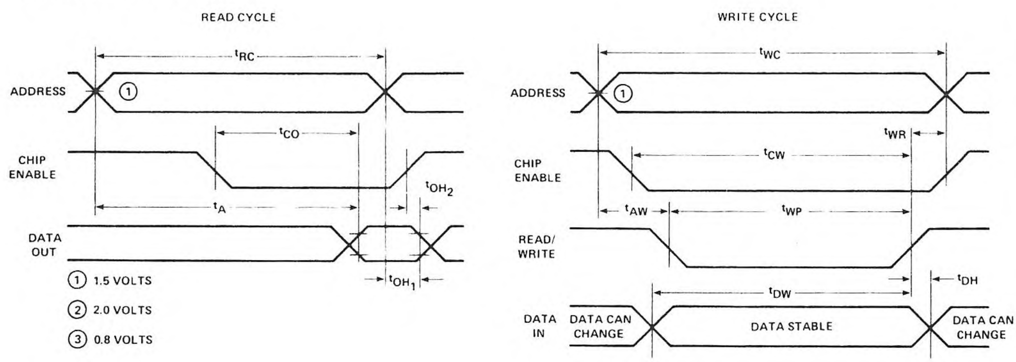
Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and C_L = 100 pF

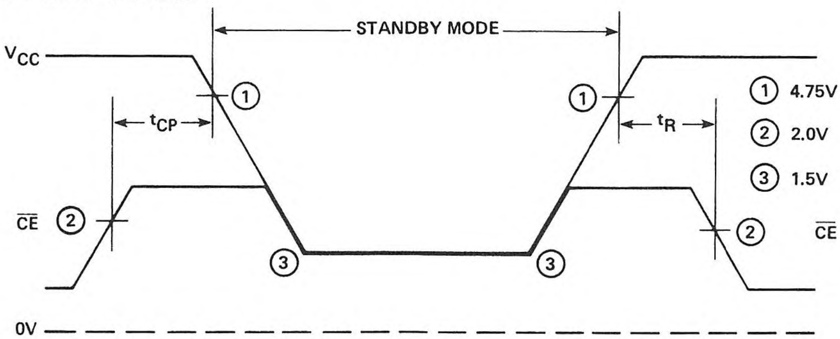
RAMs

RAMs

TIMING DIAGRAMS

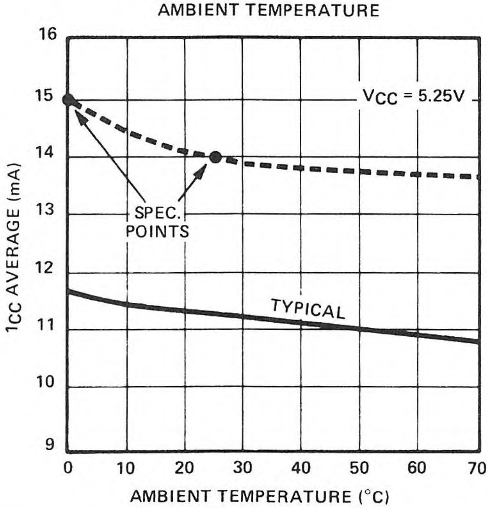


STANDBY WAVEFORMS



TYPICAL DC CHARACTERISTICS

POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



256x4 Static Random Access Memory

Synertek®

SY2111

MEMORY PRODUCTS

RAMs

- Organization 256 Words By 4 Bits
- Common Data Input And Output
- Single +5V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Access Time — 250/350/450/500ns
- Simple Memory Expansion — 2 Chip Enable Inputs
- Fully Decoded — On-Chip Address Decode
- Inputs Protected — All Inputs have Protection Against Static Charge
- Low Cost Packaging — 18 Pin Plastic Dual-In-Line Configuration
- Low Power — Typically 150mW
- Three - State Output — OR - Tie Capability

The SY2111 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

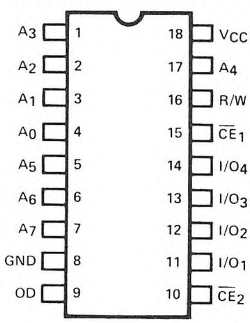
The SY2111 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate Chip Enable leads allow easy selection of an individual package when outputs are OR-tied.

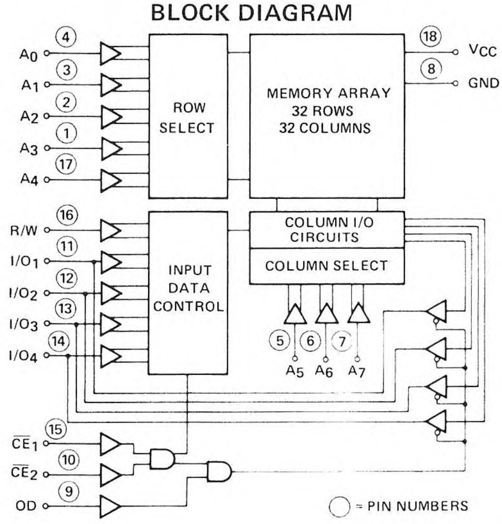
The SY2111 is fabricated with N-channel ion-implanted silicon gate technology, which allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SYP2111-1	Plastic DIP	0°C to 70°C
SYC2111-1	Ceramic DIP	0°C to 70°C
SYP2111A-2	Plastic DIP	0°C to 70°C
SYC2111A-2	Ceramic DIP	0°C to 70°C
SYP2111A	Plastic DIP	0°C to 70°C
SYC2111A	Ceramic DIP	0°C to 70°C
SYP2111A-4	Plastic DIP	0°C to 70°C
SYC2111A-4	Ceramic DIP	0°C to 70°C

PIN NAMES

A_0-A_7	ADDRESS INPUTS	$\overline{CE}_1$	CHIP ENABLE 1
OD	OUTPUT DISABLE	$\overline{CE}_2$	CHIP ENABLE 2
R/W	READ/WRITE INPUT	I/O_1-I/O_4	DATA INPUT/OUTPUT

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	2111-1 Min.	2111-1 Typ.(1)	2111-1 Max.	2111A, 2111A-2, 2111A-4 Min.	2111A, 2111A-2, 2111A-4 Typ.(1)	2111A, 2111A-2, 2111A-4 Max.	Unit	Test Conditions
I_{LI}	Input Load Current			10			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15			15	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-50			-50	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	60		30	50	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			70			55	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		+0.65	-0.5		+0.8	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45			0.4	V	I_{OL} = 3.2mA (I_{OL} = 2.0mA - 2111-1)
V_{OH}	Output High Voltage	2.2			2.4			V	I_{OH} = -150μA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARATERISTICS — SY2111-1

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	500		ns
t_A	Access Time		500	ns
t_{CO}	Chip Enable To Output		350	ns
t_{OD}	Output Disable To Output		300	ns
t_{DF}[1]	Data Output To High Z State	0	150	ns
t_{OH}	Previous Data Read Valid After Change Of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	500		ns
t_{AW}	Write Delay	100		ns
t_{CW}	Chip Enable To Write	400		ns
t_{DW}	Data Setup	280		ns
t_{DH}	Data Hold	100		ns
t_{WP}	Write Pulse	300		ns
t_{WR}	Write Recovery	50		ns

NOTE: 1. t_{DF} is with respect to the trailing edge of CE1, CE2, or OD, whichever comes first.

A.C. CHARACTERISTICS – SY2111A-2

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	250		ns
t_A	Access Time		250	ns
t_{CO}	Chip Enable To Output		130	ns
t_{OD}	Output Disable To Output		100	ns
t_{DF} [1]	Data Output To High Z State	0	100	ns
t_{OH}	Previous Data Read Valid After Change Of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	250		ns
t_{AW}	Write Delay	0		ns
t_{CW}	Chip Enable To Write	150		ns
t_{DW}	Data Setup	150		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	200		ns
t_{WR}	Write Recovery	0		ns

A.C. CHARACTERISTICS – SY2111A

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	350		ns
t_A	Access Time		350	ns
t_{CO}	Chip Enable To Output		170	ns
t_{OD}	Output Disable To Output		140	ns
t_{DF} [1]	Data Output To High Z State	0	130	ns
t_{OH}	Previous Data Read Valid After Change Of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	350		ns
t_{AW}	Write Delay	0		ns
t_{CW}	Chip Enable To Write	200		ns
t_{DW}	Data Setup	200		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	250		ns
t_{WR}	Write Recovery	0		ns

NOTE: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $\overline{CE2}$, or OD, whichever comes first.

RAMs

A.C. CHARACTERISTICS – SY2111A-4

T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
READ CYCLE				
t_{RCY}	Read Cycle	450		ns
t_A	Access Time		450	ns
t_{CO}	Chip Enable To Output		200	ns
t_{OD}	Output Disable To Output		170	ns
t_{DF} [1]	Data Output To High Z State	0	150	ns
t_{OH}	Previous Data Read Valid After Change Of Address	0		ns
WRITE CYCLE				
t_{WCY}	Write Cycle	450		ns
t_{AW}	Write Delay	0		ns
t_{CW}	Chip Enable To Write	250		ns
t_{DW}	Data Setup	250		ns
t_{DH}	Data Hold	0		ns
t_{WP}	Write Pulse	300		ns
t_{WR}	Write Recovery	0		ns

A.C. CONDITIONS OF TEST

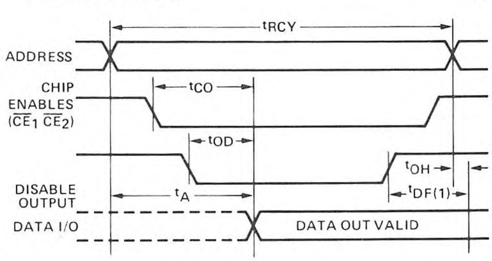
	2111A, 2111A-2, 2111A-4	2111-1
Input Pulse Levels	+0.8V to 2.0V	+0.65V to 2.2V
Input Pulse Rise & Fall Times:	10ns	10ns
Timing Measuremnt Reference Level — Inputs:	1.5V	1.5V
Outputs:	0.8V & 2.0V	0.8V & 2.0V
Output Load:	1 TTL Gate & C_L = 100pF	1 TTL Gate & C_L = 100pF

CAPACITANCE T_A = 25°C, f = 1 MHz

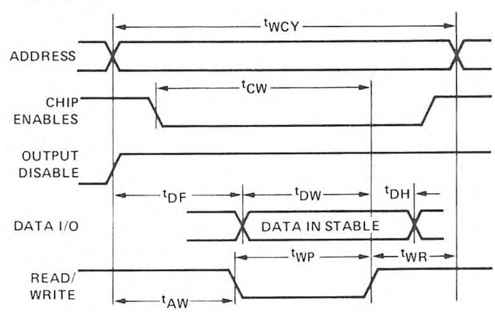
Symbol	Test	Typ.	Max	Unit
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8	pF
C_{OUT}	Output Capacitance V_{OUT} = 0V	10	15	pF

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE



NOTE: 1. t_{DF} is with respect to the trailing edge of CE1, CE2 or OD, whichever comes first.

256x4 Static Random Access Memory

SY21H11

MEMORY PRODUCTS

Synertek®

- Organization – 256 Words By 4 Bits
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Access Time – 175/200 ns
- Fully Decoded – On-Chip Address Decode
- Inputs Protected – All Inputs Have Protection Against Static Charge
- Low Cost Packaging – 18 Pin Plastic Dual-In-Line Configuration
- Three-State Output – OR-Tie Capability
- Simple Memory Expansion – 2 Chip Enable Inputs

RAMs

The SY21H11 is a 256-word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

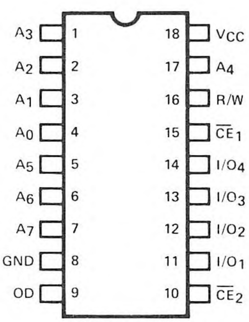
The SY21H11 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate Chip Enable leads allow easy selection of an individual package when outputs are OR-tied.

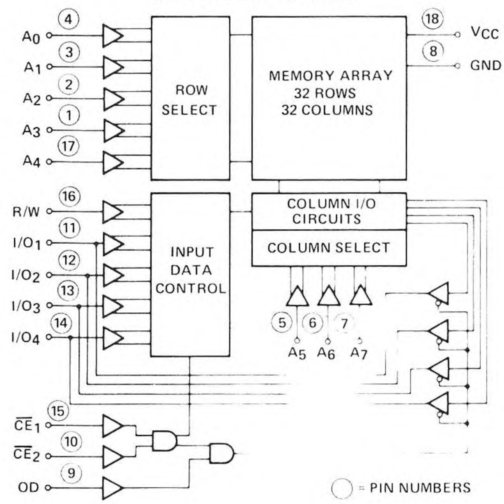
The SY21H11 is fabricated with N-channel ion-implanted silicon gate technology, which allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost packaging.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SYP21H11	Plastic DIP	0°C to 55°C
SYC21H11	Ceramic DIP	0°C to 55°C
SYP21H11-2	Plastic DIP	0°C to 55°C
SYC21H11-2	Ceramic DIP	0°C to 55°C

PIN NAMES

A_0-A_7	ADDRESS INPUTS	$\overline{CE}_1$	CHIP ENABLE 1
OD	OUTPUT DISABLE	$\overline{CE}_2$	CHIP ENABLE 2
R/W	READ/WRITE INPUT	I/O_1-I/O_4	DATA INPUT/OUTPUT

RAMs

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 55°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 55°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min	Typ.(1)	Max	Unit	Test Conditions
I_{LI}	Input Load Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			–50	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		50	80	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			90	mA	V_{IN} = 5.25V $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	–0.5		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –150μA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS – SY21H11

READ CYCLE T_A = 0°C to 55°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RCY}	Read Cycle	175			ns
t_A	Access Time			175	ns
t_{CO}	Chip Enable to Output			100	ns
t_{OD}	Output Disable to Output			90	ns
t_{DF}[1]	Data Output to High Z State	0		70	ns
t_{OH}	Previous Data Read Valid After Change of Address	0			ns

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WCY}	Write Cycle	175			ns
t_{AW}	Write Delay	0			ns
t_{CW}	Chip Enable to Write	100			ns
t_{DW}	Data Setup	100			ns
t_{DH}	Data Hold	0			ns
t_{WP}	Write Pulse	150			ns
t_{WR}	Write Recovery	0			ns

NOTE: 1. t_{DF} is with respect to the trailing edge of $\overline{CE1}$, $\overline{CE2}$, or OD, whichever comes first.

A.C. CHARACTERISTICS – SY21H11-2

READ CYCLE T_A = 0°C to 55°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RCY}	Read Cycle	200			ns
t_A	Access Time			200	ns
t_{CO}	Chip Enable to Output			120	ns
t_{OD}	Output Disable to Output			100	ns
t_{DF} [1]	Data Output to High Z State	0		80	ns
t_{OH}	Previous Data Read Valid After Change of Address	0			ns

WRITE CYCLE

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WCY}	Write Cycle	200			ns
t_{AW}	Write Delay	0			ns
t_{CW}	Chip Enable to Write	120			ns
t_{DW}	Data Setup	120			ns
t_{DH}	Data Hold	0			ns
t_{WP}	Write Pulse	170			ns
t_{WR}	Write Recovery	0			ns

RAMs

A.C. CONDITIONS OF TEST

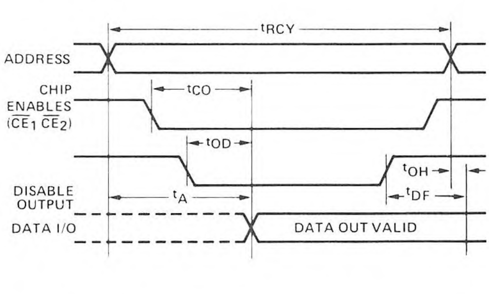
Input Pulse Levels: . . . . +0.8V to 2.0V
Input Rise & Fall Times: . . . . 10 ns
Timing Measurement Reference Level Input: 1.5V
Output: . . . . 0.8V & 2.0V
Output Load: . . . . 1 TTL Gate & C_L = 100pF

CAPACITANCE T_A = 25°C, f = 1 MHz

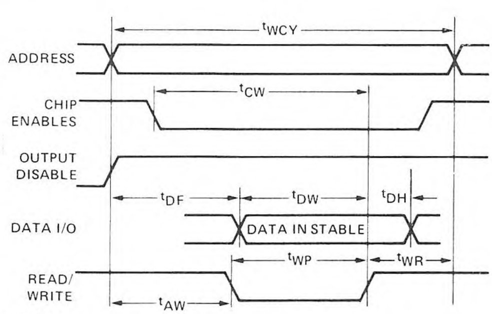
Symbol	Test	Typ.	Max	Unit
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8	pF
C_{OUT}	Output Capacitance V_{OUT} = 0V	10	15	pF

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE

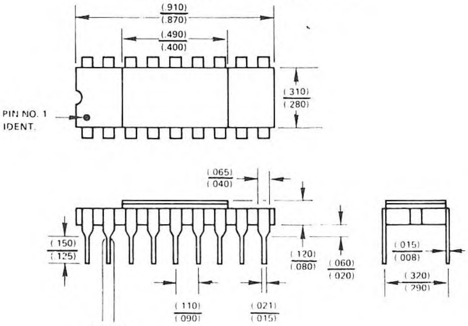


NOTE: 1. tDF is with respect to the trailing edge of $\overline{CE}_1$,$\overline{CE}_2$ or OD, whichever occurs first.

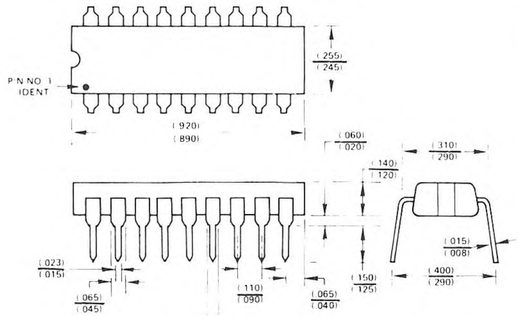
RAMs

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



256 x 4 Static Random Access Memory

SY2112

Synertek®

MEMORY PRODUCTS

RAMs

- Organization 256 Words by 4 Bits
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible - All Inputs and Outputs
- Static MOS - No Clocks or Refreshing Required
- Access Time - 250/350/450/500 ns
- Simple Memory Expansion - Chip Enable Input
- Fully Decoded - On-Chip Address Decode
- Inputs Protected - All Inputs Have Protection Against Static Charge
- Low Cost Packaging - 16 Pin Plastic Dual-In-Line Configuration
- Low Power - Typically 150 mW
- Three-State Output - OR-tie Capability

The SY2112 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

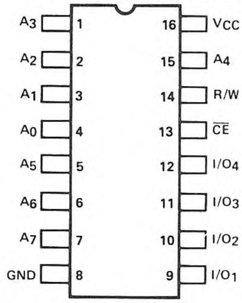
The SY2112 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Enable lead allows easy selection of an individual package when outputs are OR-tied.

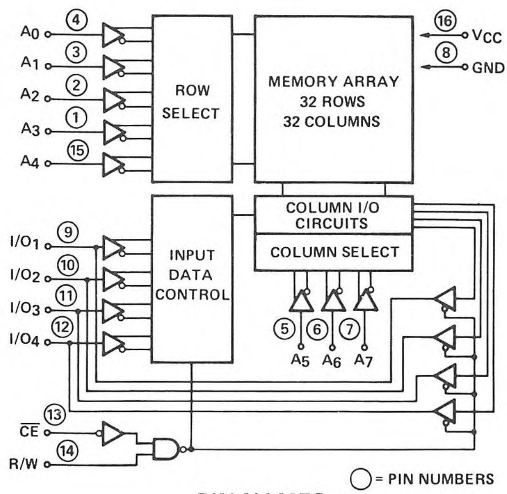
The SY2112 is fabricated with ion implanted N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



BLOCK DIAGRAM



○ = PIN NUMBERS

ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP2112A-2	Plastic DIP	250nsec	0°C to 70°C
SYC2112A-2	Ceramic DIP	250nsec	0°C to 70°C
SYP2112A	Plastic DIP	350nsec	0°C to 70°C
SYC2112A	Ceramic DIP	350nsec	0°C to 70°C
SYP2112A-4	Plastic DIP	450nsec	0°C to 70°C
SYC2112A-4	Ceramic DIP	450nsec	0°C to 70°C
SYP2112-1	Plastic DIP	500nsec	0°C to 70°C
SYC2112-1	Ceramic DIP	500nsec	0°C to 70°C

PIN NAMES

A_0-A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

RAMs

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. AND OPERATING CHARACTERISTICS — SY2112A, SY2112A-2, SY2112A-4

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	µA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-50	µA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	50	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			55	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.4	V	I_{OL} = 3.2mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -150µA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

D. C. AND OPERATING CHARACTERISTICS — SY2112-1

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ. (1)	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	µA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-50	µA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		30	60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA T_A = 25°C
I_{CC2}	Power Supply Current			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	I_{OL} = 2mA
V_{OH}	Output "High" Voltage	2.2			V	I_{OH} = -150µA

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. CHARACTERISTICS – SY2112A-2

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
t_{RCY}	Read Cycle	250		ns
t_A	Access Time		250	ns
t_{CO}	Chip Enable to Output Time		130	ns
t_{CD}	Chip Enable to Output Disable Time	0	100	ns
t_{OH}	Previous Read Data Valid After Change of Address	0		ns

WRITE CYCLE NO. 1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY1}	Write Cycle	250		ns
t_{AW1}	Address to Write Setup Time	0		ns
t_{DW1}	Write Setup Time	150		ns
t_{WP1}	Write Pulse Width	250		ns
t_{CS1}	Chip Enable Setup Time	0	100	ns
t_{CH1}	Chip Enable Hold Time	0		ns
t_{WR1}	Write Recovery Time	0		ns
t_{DH1}	Data Hold Time	0		ns
t_{CW1}	Chip Enable to Write Setup Time	150		ns

WRITE CYCLE NO. 2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY2}	Write Cycle	250		ns
t_{AW2}	Address to Write Setup Time	0		ns
t_{DW2}	Write Setup Time	150		ns
t_{WD2}	Write To Output Disable Time		100	ns
t_{CS2}	Chip Enable Setup Time	0		ns
t_{CH2}	Chip Enable Hold Time	0		ns
t_{WR2}	Write Recovery Time	0		ns
t_{DH2}	Data Hold Time	0		ns

A. C. CHARACTERISTICS – SY2112A

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
t_{RCY}	Read Cycle	350		ns
t_A	Access Time		350	ns
t_{CO}	Chip Enable to Output Time		170	ns
t_{CD}	Chip Enable to Output Disable Time	0	130	ns
t_{OH}	Previous Read Data Valid After Change of Address	0		ns

RAMs

A. C. CHARACTERISTICS – SY2112A (Cont.)

WRITE CYCLE NO. 1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY1}	Write Cycle	350		ns
t_{AW1}	Address to Write Setup Time	0		ns
t_{DW1}	Write Setup Time	200		ns
t_{WP1}	Write Pulse Width	300		ns
t_{CS1}	Chip Enable Setup Time	0	100	ns
t_{CH1}	Chip Enable Hold Time	0		ns
t_{WR1}	Write Recovery Time	0		ns
t_{DH1}	Data Hold Time	0		ns
t_{CW1}	Chip Enable to Write Setup Time	200		ns

WRITE CYCLE NO. 2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY2}	Write Cycle	350		ns
t_{AW2}	Address to Write Setup Time	0		ns
t_{DW2}	Write Setup Time	200		ns
t_{WD2}	Write To Output Disable Time		130	ns
t_{CS2}	Chip Enable Setup Time	0		ns
t_{CH2}	Chip Enable Hold Time	0		ns
t_{WR2}	Write Recovery Time	0		ns
t_{DH2}	Data Hold Time	0		ns

A. C. CHARACTERISTICS – SY2112A-4

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
t_{RCY}	Read Cycle	450		ns
t_A	Access Time		450	ns
t_{CO}	Chip Enable to Output Time		200	ns
t_{CD}	Chip Enable to Output Disable Time	0	150	ns
t_{OH}	Previous Read Data Valid After Change of Address	0		ns

WRITE CYCLE NO. 1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY1}	Write Cycle	450		ns
t_{AW1}	Address to Write Setup Time	0		ns
t_{DW1}	Write Setup Time	250		ns
t_{WP1}	Write Pulse Width	350		ns
t_{CS1}	Chip Enable Setup Time	0	100	ns
t_{CH1}	Chip Enable Hold Time	0		ns
t_{WR1}	Write Recovery Time	0		ns
t_{DH1}	Data Hold Time	0		ns
t_{CW1}	Chip Enable to Write Setup Time	250		ns

A. C. CHARACTERISTICS – SY2112A-4 (Cont.)

WRITE CYCLE NO. 2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY2}	Write Cycle	450		ns
t_{AW2}	Address to Write Setup Time	0		ns
t_{DW2}	Write Setup Time	250		ns
t_{WD2}	Write To Output Disable Time		150	ns
t_{CS2}	Chip Enable Setup Time	0		ns
t_{CH2}	Chip Enable Hold Time	0		ns
t_{WR2}	Write Recovery Time	0		ns
t_{DH2}	Data Hold Time	0		ns

RAMs

A. C. CHARACTERISTICS – SY2112-1

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{RCY}	Read Cycle	500		ns	t_r, $t_f \leq 20ns$
t_A	Access Time		500	ns	$0.65V \geq V_{IN} \geq 2.2V$
t_{CO}	Chip Enable To Output Time		350	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0	150	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	0		ns	$C_L = 100pF$

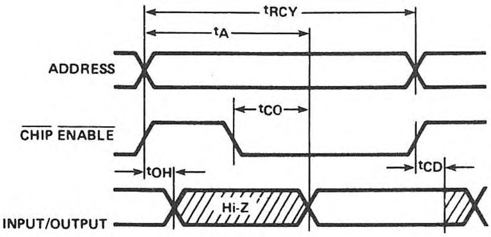
WRITE CYCLE NO. 1 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{WCY1}	Write Cycle	500		ns	t_r, $t_f \leq 20ns$
t_{AW1}	Address To Write Setup Time	100		ns	$0.65V \geq V_{IN} \geq 2.2V$
t_{DW1}	Write Setup Time	200		ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	300		ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0	100	ns	$C_L = 100pF$
t_{CH1}	Chip Enable Hold Time	0		ns	
t_{WR1}	Write Recovery Time	50		ns	
t_{DH1}	Data Hold Time	100		ns	
t_{CW1}	Chip Enable to Write Setup Time	200		ns	

WRITE CYCLE NO. 2 $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{WCY2}	Write Cycle	500		ns	t_r, $t_f \leq 20ns$
t_{AW2}	Address To Write Setup Time	100		ns	$0.65V \geq V_{IN} \geq 2.2V$
t_{DW2}	Write Setup Time	200		ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	100		ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0		ns	$C_L = 100pF$
t_{CH2}	Chip Enable Hold Time	0		ns	
t_{WR2}	Write Recovery Time	50		ns	
t_{DH2}	Data Hold Time	100		ns	

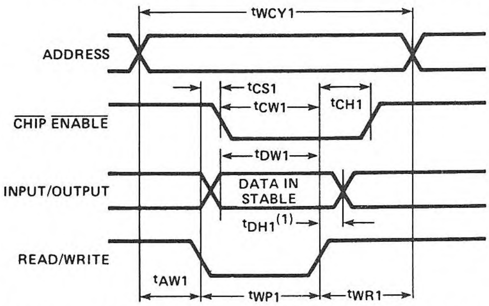
READ CYCLE WAVEFORMS



CAPACITANCE

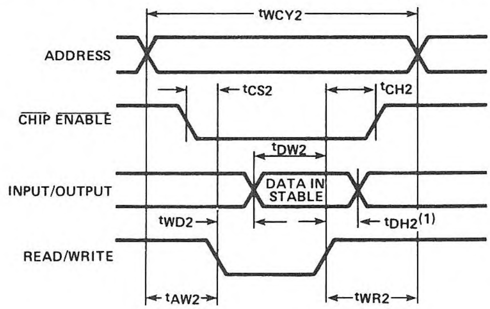
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O}$ = 0V	10	18

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V±5%



NOTE 1. Data Hold Time. (T_{OH}) is reference to the trailing edge of CHIP ENABLE (CE) or READ/WRITE (R/W) whichever comes first.

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V±5%

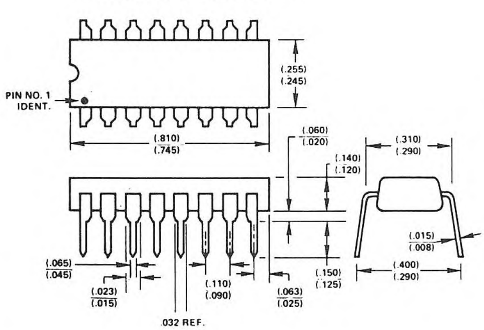


A.C. CONDITIONS OF TEST

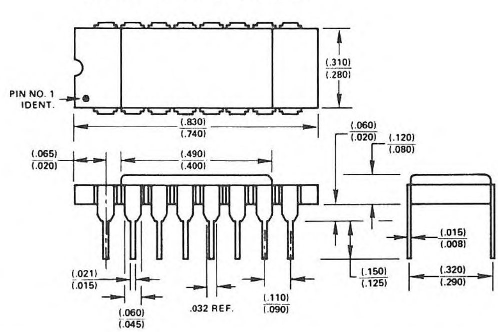
Input Pulse Leads . . . . 0.8 to 2.0 Volt
Input Pulse Rise and Fall Times . . . . 10 nsec
Timing Measurement Reference Level: Input . . . . 1.5 Volt
Output . . . . 0.8 and 2.0 Volt
Output Load . . . . 1 TTL Gate and C_L = 100 pF

PACKAGE DIAGRAM

CERAMIC PACKAGE



MOLDED PACKAGE



256 x 4 Static Random Access Memory

SY21H12

Synertek®

MEMORY PRODUCTS

- Organization-256 Words By 4 Bits
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible - All Inputs and Outputs
- Access Time - 175/200 ns
- Simple Memory Expansion - Chip Enable Input
- Fully Decoded - On-Chip Address Decode
- Inputs Protected - All Inputs Have Protection Against Static Charge
- Low Cost Packaging - 16 Pin Plastic Dual-In-Line Configuration
- Three-State Output - OR-Tie Capability

RAMs

The SY21H12 is a 256 word by 4 bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

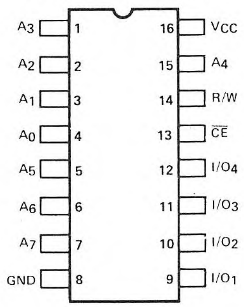
The SY21H12 is designed for memory applications in small systems where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Enable lead allows easy selection of an individual package when outputs are OR-tied.

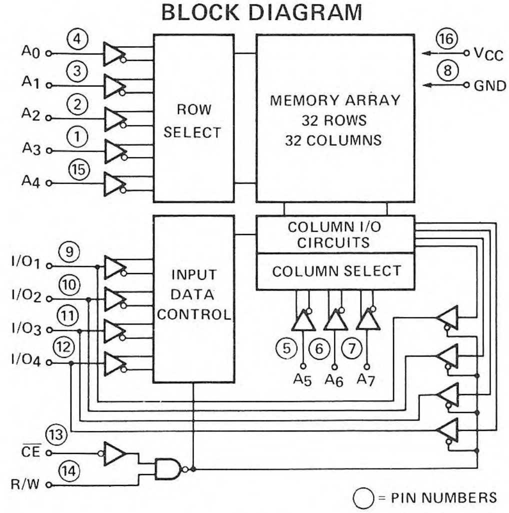
The SY21H12 is fabricated with ion implanted N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or N-channel silicon gate technology.

Synertek's ion implanted silicon gate technology also provides excellent protection against contamination. This permits the use of low cost packaging.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP21H12	Plastic DIP	175nsec	0°C to 55°C
SYC21H12	Ceramic DIP	175nsec	0°C to 55°C
SYP21H12-2	Plastic DIP	200nsec	0°C to 55°C
SYC21H12-2	Ceramic DIP	200nsec	0°C to 55°C

PIN NAMES

A_0-A_7	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

RAMs

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 55°C
Storage Temperature	-65°C to 150°C
Voltage On Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

*COMMENTS

Stresses above those liste under "Absolute Maximum Ratings" may cause damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 55°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current			15	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current			-50	μA	$\overline{CE}$ = 2.2V, $V_{I/O}$ = 0.45V
I_{CC1}	Power Supply Current		50	80	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current			90	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input "Low" Voltage	-0.5		+0.8	V	
V_{IH}	Input "High" Voltage	2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.4	V	I_{OL} = 3.2mA
V_{OH}	Output "High" Voltage	2.4			V	I_{OH} = -150μA

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A. C. CHARACTERISTICS – SY21H12

READ CYCLE T_A = 0°C to 55°C, V_{CC} = 5V ±5% unless otherwise specified

Symbol	Parameter	Min.	Max.	Unit
t_{RCY}	Read Cycle	175		ns
t_A	Access Time		175	ns
t_{CO}	Chip Enable to Output Time		110	ns
t_{CD}	Chip Enable to Output Disable Time	0	70	ns
t_{OH}	Previous Read Data Valid After Change of Address	0		ns

WRITE CYCLE NO. 1 T_A = 0°C to 55°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Max.	Unit
t_{WCY1}	Write Cycle	175		ns
t_{AW1}	Address to Write Setup Time	0		ns
t_{DW1}	Write Setup Time	100		ns
t_{WP1}	Write Pulse Width	150		ns
t_{CS1}	Chip Enable Setup Time	0	50	ns
t_{CH1}	Chip Enable Hold Time	0		ns
t_{WR1}	Write Recovery Time	0		ns
t_{DH1}	Data Hold Time	0		ns
t_{CW1}	Chip Enable to Write Setup Time	100		ns

WRITE CYCLE NO. 2 $T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY2}	Write Cycle	175		ns
t_{AW2}	Address to Write Setup Time	0		ns
t_{DW2}	Write Setup Time	100		ns
t_{WD2}	Write to Output Disable Time		70	ns
t_{CS2}	Chip Enable Setup Time	0		ns
t_{CH2}	Chip Enable Hold Time	0		ns
t_{WR2}	Write Recovery Time	0		ns
t_{DH2}	Data Hold Time	0		ns

RAMs

A. C. CHARACTERISTICS – SY21H12-2

READ CYCLE $T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min.	Max.	Unit
t_{RCY}	Read Cycle	200		ns
t_A	Access Time		200	ns
t_{CO}	Chip Enable to Output Time		120	ns
t_{CD}	Chip Enable to Output Disable Time	0	80	ns
t_{OH}	Previous Read Data Valid After Change of Address	0		ns

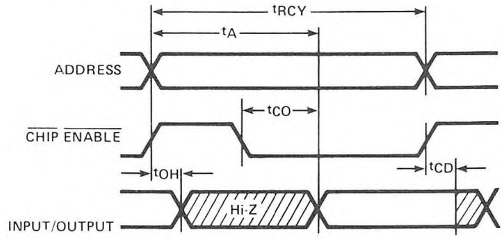
WRITE CYCLE NO. 1 $T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY1}	Write Cycle	200		ns
t_{AW1}	Address to Write Setup Time	0		ns
t_{DW1}	Write Setup Time	120		ns
t_{WP1}	Write Pulse Width	170		ns
t_{CS1}	Chip Enable Setup Time	0	50	ns
t_{CH1}	Chip Enable Hold Time	0		ns
t_{WR1}	Write Recovery Time	0		ns
t_{DH1}	Data Hold Time	0		ns
t_{CW1}	Chip Enable to Write Setup Time	120		ns

WRITE CYCLE NO. 2 $T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Unit
t_{WCY2}	Write Cycle	200		ns
t_{AW2}	Address to Write Setup Time	0		ns
t_{DW2}	Write Setup Time	120		ns
t_{WD2}	Write to Output Disable Time		80	ns
t_{CS2}	Chip Enable Setup Time	0		ns
t_{CH2}	Chip Enable Hold Time	0		ns
t_{WR2}	Write Recovery Time	0		ns
t_{DH2}	Data Hold Time	0		ns

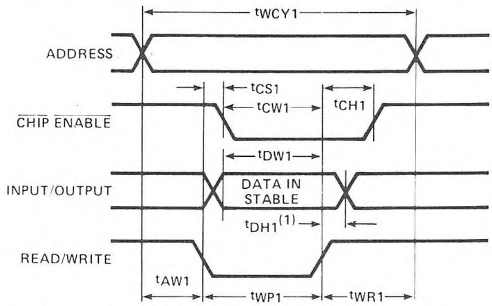
READ CYCLE WAVEFORMS



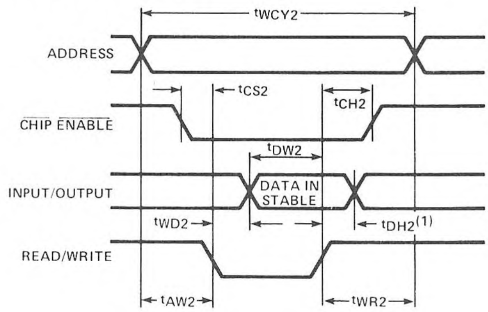
CAPACITANCE

Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8
$C_{I/O}$	I/O Capacitance $V_{I/O} = 0V$	10	18

WRITE CYCLE #1



WRITE CYCLE #2



NOTE 1. Data Hold Time. (T_{OH}) is reference to the trailing edge of CHIP ENABLE ($\overline{CE}$) or READ/WRITE (R/W) whichever comes first.

$T_A = 0°C$ to $55°C$, $V_{CC} = 5V \pm 5\%$

A.C. CONDITIONS OF TEST

Input Pulse Levels . . . . +0.8 Volt to 2.0 Volt

Input Rise and Fall Times . . . . 10 nsec

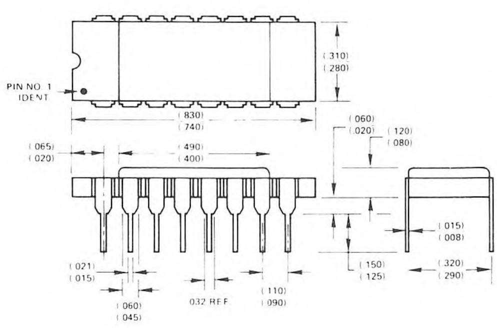
Timing Measurement Reference Levels: Input . . . . 1.5 Volt

Output . . . . 0.8 and 2.0 Volt

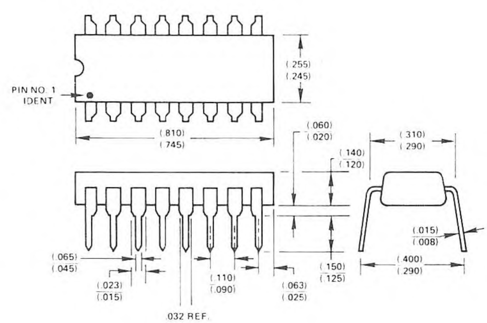
Output Load . . . . 1 TTL Gate and C_L = 100 pF

PACKAGE DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



1024x4 Static Random Access Memory

SY2114

MEMORY PRODUCTS

Synertek®

RAMs

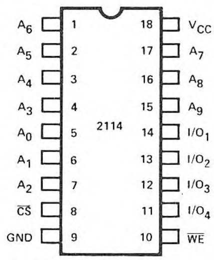
- 300 ns Maximum Access
- Low Operating Power Dissipation 0.1 mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible: All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

The SY2114 is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 2 TTL loads.

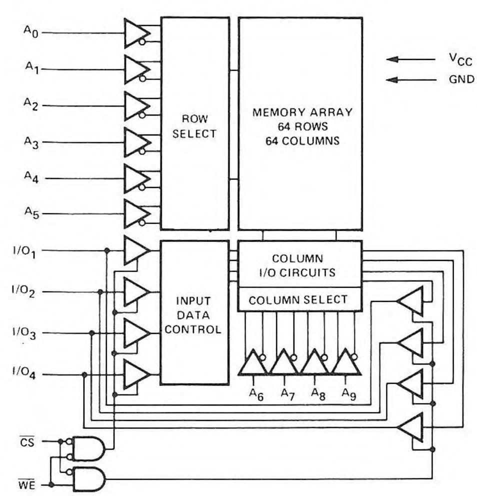
The SY2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are or-tied.

The SY2114 is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology – a technology providing excellent performance characteristics as well as protection against contamination allowing the use of low cost packaging techniques.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Supply Current (Max)	Temperature Range
SYC2114	Ceramic	450nsec	100mamp	0°C to 70°C
SYP2114	Molded	450nsec	100mamp	0°C to 70°C
SYC2114-3	Ceramic	300nsec	100mamp	0°C to 70°C
SYP2114-3	Molded	300nsec	100mamp	0°C to 70°C
SYC2114L	Ceramic	450nsec	70mamp	0°C to 70°C
SYP2114L	Molded	450nsec	70mamp	0°C to 70°C
SYC2114L-3	Ceramic	300nsec	70mamp	0°C to 70°C
SYP2114L-3	Molded	300nsec	70mamp	0°C to 70°C

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RAMs

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±5% (Unless Otherwise Specified)

Symbol	Parameter	2114-3, 2114 Min	2114-3, 2114 Max	2114L, 2114L-3 Min	2114L, 2114L-3 Max	Unit	Conditions
I_{LI}	Input Load Current (All input pins)		10		10	μA	V_{IN} = 0 to 5.25V
I_{LO}	I/O Leakage Current		10		10	μA	$\overline{CS}$ = 2.0V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		95		65	mA	V_{CC} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current		100		70	mA	V_{CC} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH} = -1.0 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz

Symbol	Test	Typ	Max	Units
$C_{I/O}$	Input/Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5% (Unless Otherwise Specified)

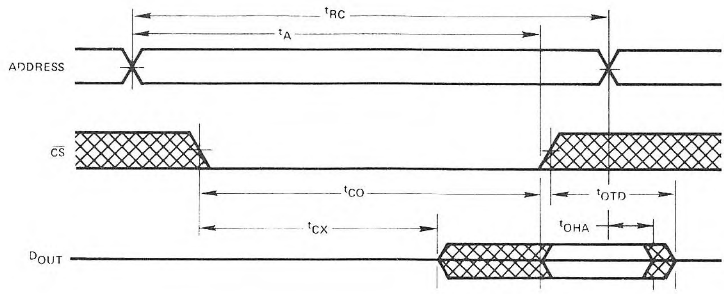
SYMBOL	PARAMETER	2114-3,2114L-3 MIN	2114-3,2114L-3 MAX	2114, 2114L MIN	2114, 2114L MAX	UNIT
READ CYCLE						
t_{RC}	Read Cycle Time	300		450		nsec
t_A	Access Time		300		450	nsec
t_{CO}	Chip Select to Output Valid		100		120	nsec
t_{CX}	Chip Select to Output Enabled	20		20		nsec
t_{OTD}	Chip Deselect to Output Off	0	80	0	100	nsec
t_{OHA}	Output Hold From Address Change	50		50		nsec
WRITE CYCLE						
t_{WC}	Write Cycle Time	300		450		nsec
t_{AW}	Address to Write Setup Time	0		0		nsec
t_W	Write Pulse Width	150		200		nsec
t_{WR}	Write Release Time	0		0		nsec
t_{OTW}	Write to Output Off	0	80	0	100	nsec
t_{DW}	Data to Write Overlap	150		200		nsec
t_{DH}	Data Hold	0		0		nsec

A.C. Test Conditions

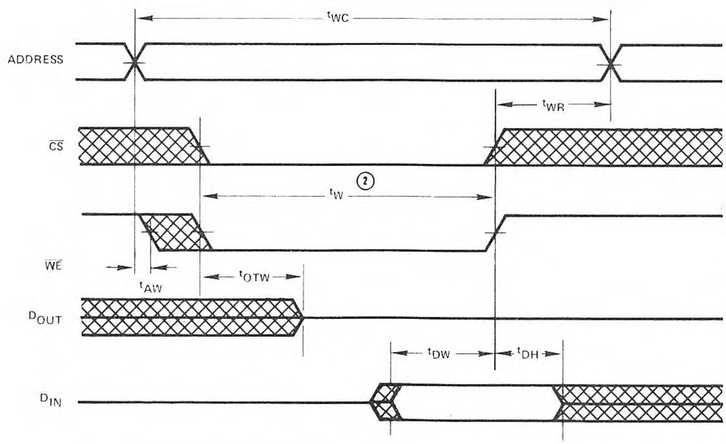
Input Pulse Levels . . . . .0.8V to 2.0V
Input Rise and Fall Time . . . . 10 n sec
Timing Measurement Levels: Input 1.5V
Output . . . . 0.8 and 2.0V
Output Load . . . . 1TTL Gate and 100pF

TIMING DIAGRAMS

Read Cycle ①



Write Cycle



NOTES:

① $\overline{WE}$ is high for a Read Cycle

② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

DATA STORAGE

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

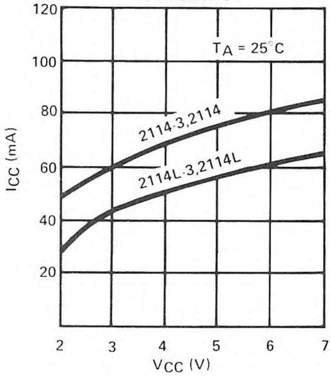
Data storage also cannot be affected by $\overline{WE}$, Addresses, or the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ or both can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during Write time – defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. The addresses must be properly established during the entire Write time plus t_{WR}.

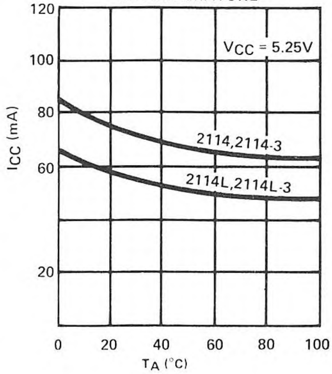
Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change. The data which is stable for t_{DW} at the end of the Write time will be written into the addressed location.

TYPICAL CHARACTERISTICS

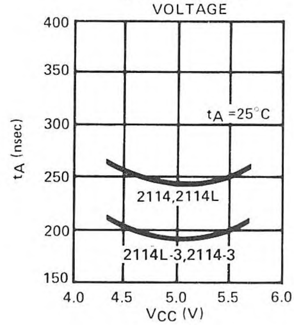
SUPPLY CURRENT VS VOLTAGE



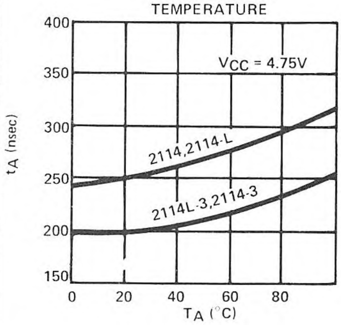
SUPPLY CURRENT VS TEMPERATURE



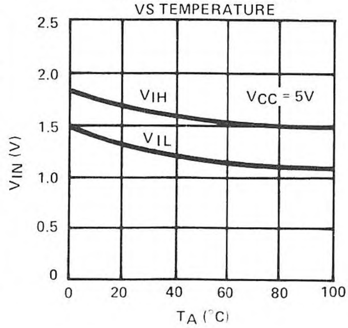
ACCESS TIME VS VOLTAGE



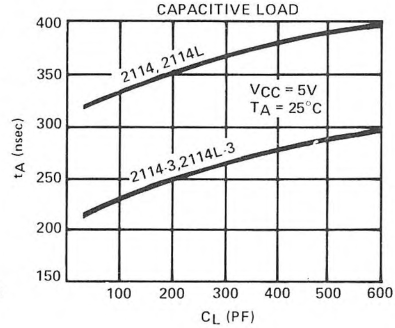
ACCESS TIME VS TEMPERATURE



INPUT VOLTAGE LIMITS VS TEMPERATURE

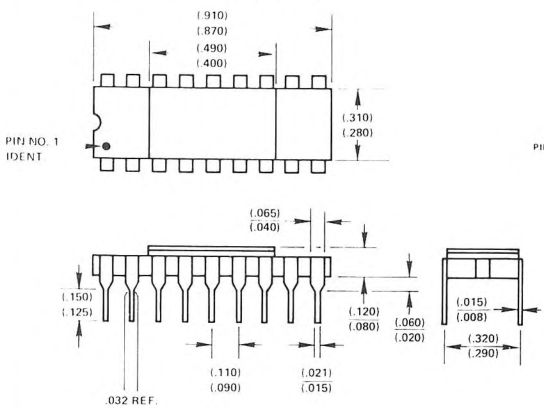


ACCESS TIME VS CAPACITIVE LOAD

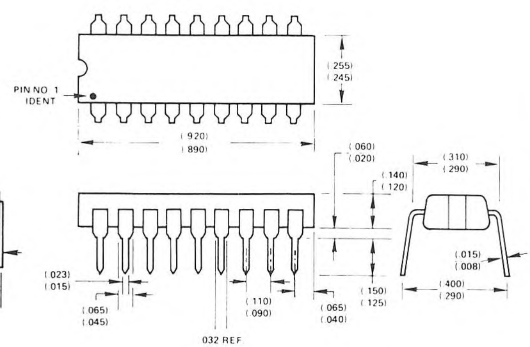


PACKAGE DIAGRAM

CERAMIC PACKAGE



MOLDED PACKAGE



4096 x 1 Dynamic Random Access Memory

SY4050

MEMORY PRODUCTS

Synertek®

- 4096 x 1 Organization
- 18-Pin Package
- Multiplexed Data Input/Output
  3 Performance Ranges:

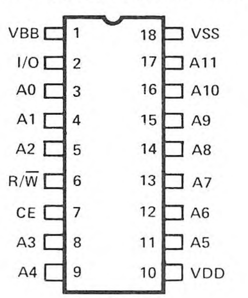
	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
SY4050	300ns	470ns	730ns
SY4050-1	250ns	430ns	660ns
SY4050-2	200ns	400ns	600ns

- Full TTL Campatibility on All Inputs (No Pull-Up Resistors Needed)
- Registers for Addresses Provided on Chip
- Open-Drain Output Buffer
- Single Low-Capacitance Clock
- Low-Power Dissipation
  – 420 mW Operating (Typical)
  – 0.1 mW Standby (Typical)
- N-Channel Silicon-Gate Technology

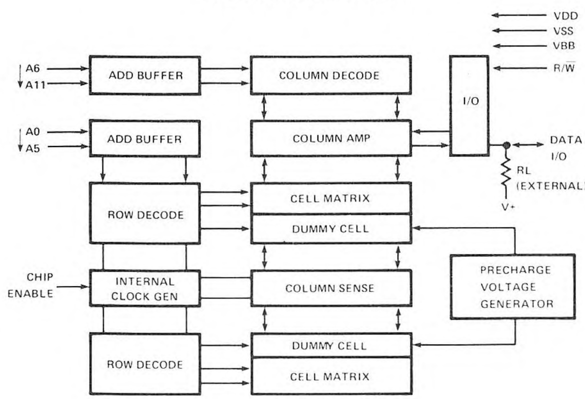
The SY4050 series is composed of high speed dynamic 4096-bit MOS random access memories, organized as 4096 one-bit words. N-channel silicon-gate technology is employed to optimize the speed/power/density trade-off. Three performance options are offered: 300ns access for the SY4050, 250ns for the SY4050-1, and 200ns for the SY4050-2. These options allow the system designer to more closely watch the memory performance to the capability of the processor.

All inputs except the chip enable are fully TTL-compatible and require no pull-up resistors. The input buffers allow a minimum 200 mV noise margin when driven by a series 74 TTL device. The TTL-compatible open-drain buffer is guaranteed to drive 1 series 74 TTL gate. The low capacitance of address and control inputs precludes the need for specializided drivers. The SY4050 series uses only one clock (chip enable) to simplify system design. The low-capacitance chip enable input requires a positive voltage swing (12 volts), which can be driven by a variety of widely available drivers. The data input and output are multiplexed to facilitate compatibility with a common bus system. A 12 line address is available, which minimizes external control logic and optimizes system performance.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYP4050	Plastic DIP	300nsec	0°C to 70°C
SYC4050	Ceramic DIP	300nsec	0°C to 70°C
SYP4050-1	Plastic DIP	250nsec	0°C to 70°C
SYC4050-1	Ceramic DIP	250nsec	0°C to 70°C
SYP4050-2	Plastic DIP	200nsec	0°C to 70°C
SYC4050-2	Ceramic DIP	200nsec	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD} (see Note 1) . . . . -0.3 to 20V
Supply voltage, V_{SS} (see Note 1) . . . . . -0.3 to 20V
All input voltages (see Note 1) . . . . . . -0.3 to 20V
Chip enable voltage (see Note 1) . . . . . . -0.3 to 20V
Output voltage (operating with
respect to V_{SS}) . . . . -2 to 7V
Operating free-air temperature range . . 0°C to 70°C
Storage temperature range . . . . . . -55°C to 150°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS T_A = 0° to 70°C

Parameter	Min.	Typ.	Max.	Units
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
Supply voltage, V_{BB}	-4.5	-5	-5.5	V
High-level input voltage, V_{IH} (all inputs except chip enable)	2.2		5.5	V
High-level chip enable input voltage, $V_{IH(CE)}$	V_{DD} -0.6		V_{DD} +1	V
Low-level input voltage, V_{IL} (all inputs except chip enable) (see Note 2)	-0.6		0.6	V
Low-level chip enable input voltage, $V_{IL(CE)}$ (see Note 2)	-1		0.6	V
Refresh time, $t_{refresh}$			2	ms

NOTE 2: The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

ELECTRICAL CHARACTERISTICS Over full ranges of recommended operating conditions, T_A = 0° to 70°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ (1)	Max.	Units
V_{OH}	High-level output voltage	t_a = guaranteed maximum access time,		2.4			V
V_{OL}	Low-level output voltage	R_L = 2.2 kΩ to 5.5V, C_L =50 pF, Load = 1 series 74 TTL gate		V_{SS}		0.4	V
I_{OL}	Low-level output current	t_a = guaranteed maximum access time, C_L = 50 pF, V_{OL} = 0.4V		5			mA
I_I	Input current (all inputs including I/O except chip enable)	V_I = -0.6 to 5.5V				10	μA
$I_{I(CE)}$	Chip enable input current	V_I = -1 to 13.2V				10	μA
I_{DD}	Supply current from V_{DD}	$V_{IH(CE)}$ = 13.2V	4050		35	60	mA
			4050-1				
			4050-2		35	70	
I_{DD}	Supply current from V_{DD}, standby	$V_{IL(CE)}$ = 0.6V			10	200	μA
$I_{DD(av)}$	Average supply current from V_{DD} during read or write cycle	Minimum cycle timing	4050		32		mA
			4050-1		35		
			4050-2		38		
$I_{DD(av)}$	Average supply current from V_{DD} during read, modify write cycle		4050		32		mA
			4050-1		35		
			4050-2		38		
I_{BB}	Supply current from V_{BB}	V_{BB} = -5.5V, V_{SS} = 0V	V_{DD} = 12.6V,		5	100	μA

NOTE 1: All typical values are at T_A = 25°C.

Capacitance at V_{DD} = 12V, V_{SS} = 0V, V_{BB} = -5V, $V_{I(CE)}$ = 0V, V_I = 0V, f = 1MHz, T_A = 0°C to 70°C (Unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ [1]	Max.	Unit
$C_{i(ad)}$	Input capacitance address inputs			5	7	pF
$C_{i(CE)}$	Input capacitance clock input	$V_{I(CE)}$ = 12V		24	28	pF
		$V_{I(CE)}$ = 0V		29	33	pF
$C_{i(R/\overline{W})}$	Input capacitance read/write input			5	7	pF
$C_{(I/O)}$	I/O terminal capacitance			7	9	pF

NOTE 1: All typical values are at T_A = 25°C.

Write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C.

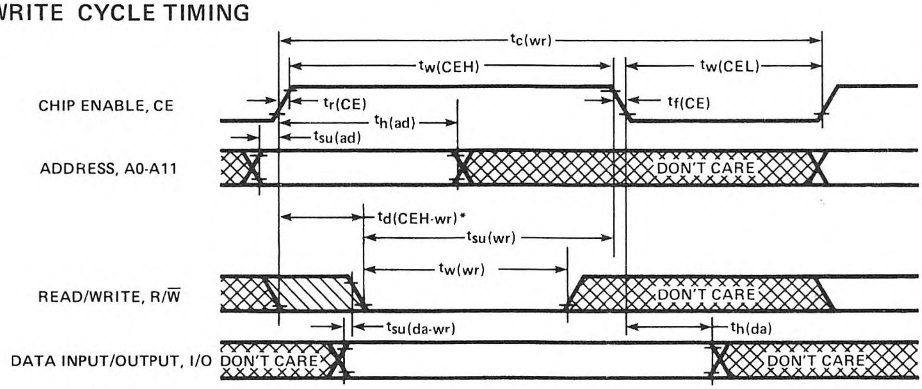
Symbol	Parameter	4050		4050-1		4050-2		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(wr)}$	Write cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(da\text{-}wr)}$	Data-to-write setup time*	0		0		0		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		220↓		210↓		ns
$t_{d(CEH\text{-}wr)}$	Chip-enable-high-to-write delay time†		40↑		40↑		40↑	ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

*If R/$\overline{W}$ is low before CE goes high, then I/O (data in) must be valid when CE goes high.

†The write pulse must go low at least $t_{su(wr)}$ minimum before CE goes low. If R/$\overline{W}$ remains high more than $t_{d(CEH\text{-}wr)}$ maximum (40 ns) after CE goes high, the data-in driver must be disabled until R/$\overline{W}$ goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices (see comments on Region 1 under read, modify write timing diagram).

WRITE CYCLE TIMING



NOTE: For the chip enable input, high and low timing points are 3.0V (high) and 1.0V (low). Other timing points are 0.6V (low) and 2.2V (high). Output timing points are 0.4V (low) and 2.4V (high).

*The write pulse must go low at least $t_{su(wr)}$ minimum before CE goes high. If R/W remains high more than $t_{d(CEL\ wr)}$ maximum (60 ns) after CE goes low, the data-in driver must be disabled until R/W goes low since additional power to overcome the output buffer may be required when writing in a high with some of the faster devices. During $t_{d(CEH\text{-}wr)}$, R/W is permitted to change from high to low only.

Read cycle timing requirements over recommended supply voltage range, $T_A = 0°C$ to $70°C$.

Symbol	Parameter	4050 Min.	4050 Max.	4050-1 Min.	4050-1 Max.	4050-2 Min.	4050-2 Max.	Unit
$t_{c(rd)}$	Read cycle time	470		430		400		ns
$t_{w(CEH)}$	Pulse width, chip enable high	300	4000	260	4000	230	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{r(CE)}$	Chip enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip enable fall time		40		40		40	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(rd)}$	Read setup time	0↑		0↑		0↑		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

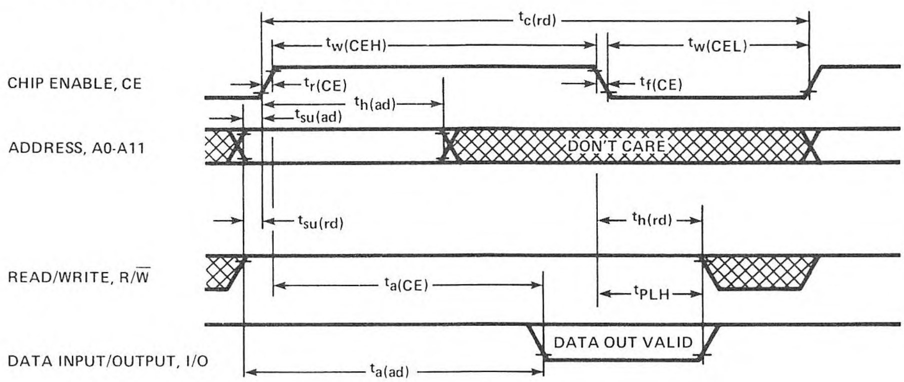
Read cycle switching characteristics over recommended supply voltage range, $T_A = 0°C$ to $70°C$.

Symbol	Parameter	4050 Min.	4050 Max.	4050-1 Min.	4050-1 Max.	4050-2 Min.	4050-2 Max.	Unit
$t_{a(CE)}$	Access time from chip enable*		280		230		180	ns
$t_{a(ad)}$	Access time from addresses†		300		250		200	ns
t_{PLH}	Propagation delay time, low-to-high level output from chip enable*	40		40		40		ns

*Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate.

†Test conditions: C_L = 50 pF, R_L = 2.2 kΩ to 5.5 V, Load = 1 Series 74 TTL gate, $t_{r(CE)}$ = 20 ns.

READ OR REFRESH CYCLE TIMING



NOTE: For the chip-enable input, high and low timing points are 3.0V (high) and 1.0V (low). Other timing points are 0.6V (low) and 2.2V (high). Output timing points are 0.4V (low) and 2.4V(high).
For minimum cycle, $t_{r(\overline{CE})}$ and $t_{f(\overline{CE})}$ are equal to 20 ns.

Read, modify write cycle timing requirements over recommended supply voltage range, T_A = 0°C to 70°C.

Symbol	Parameter	4050		4050-1		4050-2		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(RMW)}$	Read modify write cycle time†	730		660		600		ns
$t_{w(CEH)}$	Pulse width, chip enable high†	560	4000	490	4000	430	4000	ns
$t_{w(CEL)}$	Pulse width, chip enable low	130		130		130		ns
$t_{w(wr)}$	Write pulse width	200		190		180		ns
$t_{r(CE)}$	Chip enable rise time		40		40		40	ns
$t_{f(CE)}$	Chip enable fall time		40		40		40	ns
$t_{d(wr\text{-}da\ L)}$	Write to data-in-low delay time		20		20		20	ns
$t_{su(ad)}$	Address setup time	0↑		0↑		0↑		ns
$t_{su(daH)}$	Data-in-high setup time	240↓		220↓		210↓		ns
$t_{su(rd)}$	Read-pulse setup time	0↑		0↑		0↑		ns
$t_{su(wr)}$	Write-pulse setup time	240↓		240↓		240↓		ns
$t_{h(ad)}$	Address hold time	150↑		150↑		150↑		ns
$t_{h(rd)}$	Read hold time	300↑		250↑		200↑		ns
$t_{h(da)}$	Data hold time	40↓		40↓		40↓		ns

↑↓ The arrow indicates the edge of the chip enable pulse for reference: ↑ for the rising edge; ↓ for the falling edge.

† Test conditions: $t_{f(rd)}$ = 20 ns.

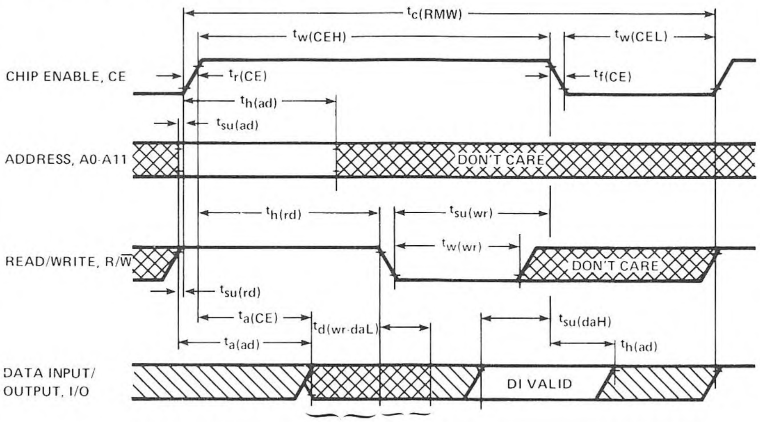
Read, modify write cycle switching characteristics over recommended supply voltage range, T_A = 0°C to 70°C.

Symbol	Parameter	4050		405-1		4050-2		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{a(CE)}$	Access time from chip enable*		280		230		180	ns
$t_{a(ad)}$	Access time from addresses†		300		250		200	ns

* Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate.

† Test conditions: C_L = 50 pF, R_L = 2.2 kΩ, Load = 1 Series 74 TTL gate. $t_{r(CE)}$ = 20 ns.

READ, MODIFY WRITE CYCLE TIMING



REGION 1 In region 1, data-out is valid until the I/O terminal is forced high or low by the data-in driver. A transition from low to high is permissible but additional power to overcome the output buffer is required. A transition from high to low is permitted without power penalty.

REGION 2 In region 2 a single transition is permitted. It is NOT a true "Don't Care" region. If a low is to be written it must be read by the end of region 2.

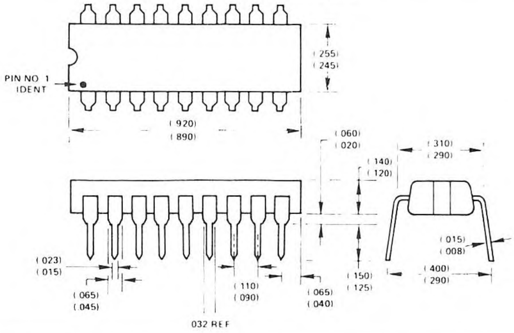
NOTE: For the chip enable input high and low timing points are 90% and 10% of $V_{IH(CE)}$. Other input timing points are 0.6V (low) 2.2V (high). Output timing points are 0.4V (low) and 2.4V (high).

For minimum cycle, $t_{r(CE)}$ and $t_{f(CE)}$ are equal to 20ns.

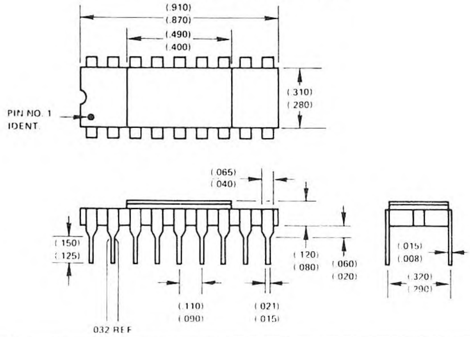
RAMs

PACKAGE DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



CMOS 256 x 4 Static Random Access Memory

SY5101

Synertek®

MEMORY PRODUCTS

- Very Low Power — 100mW operating — 50μW standby
- Pin compatible with SY2101 RAM-operates in same sockets
- Standby operation whenever chip is not selected
- Single +5V power supply
- Power Down (2 volt) memory retention
- Totally TTL compatible—inputs and outputs
- 3-state output

RAMs

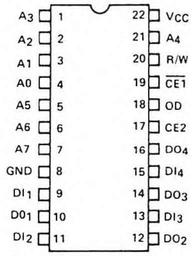
The SY5101, a 256 word x 4 bit CMOS static RAM is a low power pin-for-pin replacement for the industry standard 2101. The device is fabricated with Synertek's silicon gate, ion implanted CMOS process which allows production of very low power, high performance memories.

The 5101 is a completely static design, requiring no refresh or clocks. Low standby power can be achieved without external power down circuits—whenever the device is not enabled (CE2 = Logic 0) minimum standby current is drawn from the +5 volt supply. To simplify design of systems using battery backup for non volatility, the SY5101L will also maintain memory storage at supply voltages as low as 2.0 volts.

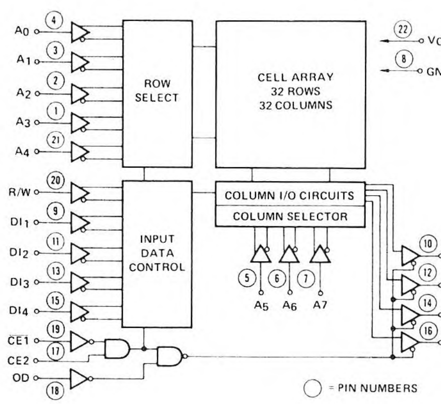
An output disable input controls the 3-state output to make construction of large memory systems simple. Write and Read cycles are selected by applying the appropriate logic signal to the R/W input with V_{CC} at +5 volts.

The 5101 is intended for use in memory systems using battery backup and/or power down techniques in order to reduce standby power dissipation and in battery powered systems where low operating power is needed. The 5101 will extend battery life in an existing 2101 design and will also permit the elimination of expensive power down circuits.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Access Time	Standby Current μA/Device	2.0 Volt Memory Retention
SYP5101L-3	650nsec	200	Yes
SYC5101L-3	650nsec	200	Yes
SYP5101L	650nsec	10	Yes
SYC5101L	650nsec	10	Yes
SYP5101L-1	450nsec	10	Yes
SYC5101L-1	450nsec	10	Yes
SYP5101-8	800nsec	500	No
SYC5101-8	800nsec	500	No

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ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to + 150°C
*Voltage on Any Pin With Respect to Ground	-0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage	+7.0V
Power Dissipation	1 Watt

*Note: During application of power care must be taken to assure that the input voltage on any pin (V_{IN}) is constrained as follows: $-0.3V \leqslant V_{IN} \leqslant V_{CC}+0.3V$

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

		5101L and 5101L-1 Limits			5101L - 3 Limits			5101-8 Limits				
Symbol	Parameter	Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	Units	Test Conditions
I_{L2}[2]	Input Current		.005	1		.005	1		.005	1	μA	V_{IN} = 0.0V to V_{CC}
I_{LO}[2]	Output Leakage Current			1			1			2	μA	$\overline{CE1}$ = 2.2V, V_{OUT} = 0 to V_{CC}
I_{CC1}	Operating Current		8	22		8	22		10	25	mA	V_{IN} = V_{CC}, Except $\overline{CE1} \leqslant$ 0.65V, Outputs, Open
I_{CC2}	Operating Current		11	27		11	27		13	30	mA	V_{IN} = 2.2V, Except $\overline{CE1} \leqslant$ 0.65V, Outputs Open
I_{CCL}[2]	Standby Current			10			200			500	μA	CE2 ⩽ 0.2V, T_A= 70°C
V_{IL}	Input Low Voltage	-0.3		0.65	-0.3		0.65	-0.3		0.65	V	
V_{IH}	Input High Voltage	2.2		V_{CC}	2.2		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4			2.4			2.4			V	I_{OH} = -1.0 mA

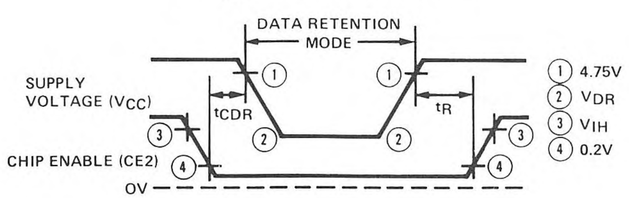
Low V_{CC} Data Retention Characteristics (For 5101L, 5101L-1 and 5101L-3) T_A = 0°C to 70°C

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	CE2⩽0.2V	
I_{CCDR1}	5101L or 5101L-1 Data Retention Current		0.14	10	μA		V_{DR}= 2.0 V, T_A= 70°C
I_{CCDR2}	5101L-3 Data Retention Current		0.70	200	μA		V_{DR}=2.0V, T_A=70°C
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[3]			ns		

NOTES:

1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

READ CYCLE

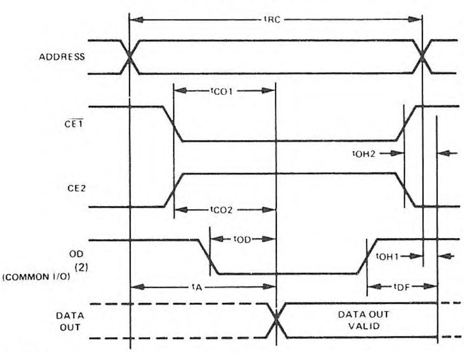
Symbol	Parameter	5101L-1 Limits (ns) Min.	5101L-1 Limits (ns) Max.	5101L and 5101L-3 Limits (ns) Min.	5101L and 5101L-3 Limits (ns) Max.	5101-8 Limits (ns) Min.	5101-8 Limits (ns) Max.
t_{RC}	Read Cycle	450		650		800	
t_A	Access Time		450		650		800
t_{CO1}	Chip Enable ($\overline{CE\ 1}$) to Output		500		600		800
t_{CO2}	Chip Enable (CE 2) to Output		500		700		850
t_{OD}	Output Disable to Output		250		350		450
t_{DF}	Data Output to High Z State	0	130	0	150	0	200
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0		0		0	
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0	

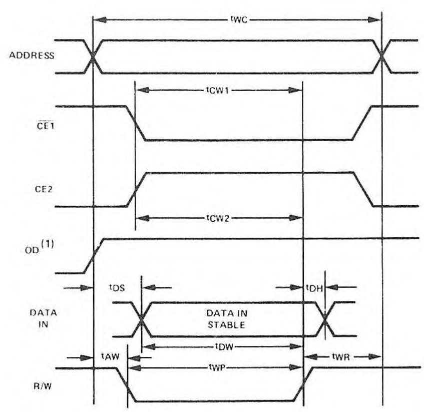
WRITE CYCLE

Symbol	Parameter	5101L-1	5101L and 5101L-3	5101-8
t_{WC}	Write Cycle	450	650	800
t_{AW}	Write Delay	130	150	200
t_{CW1}	Chip Enable ($\overline{CE\ 1}$) to Write	350	550	650
t_{CW2}	Chip Enable (CE 2) to Write	350	550	650
t_{DW}	Data Setup	250	400	450
t_{DH}	Data Hold	50	100	100
t_{WP}	Write Pulse	250	400	450
t_{WR}	Write Recovery	50	50	100
t_{DS}	Output Disable Setup	130	150	200

TIMING DIAGRAMS

READ CYCLE





NOTES:

1. During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
2. OD may be tied low for separate I/O operation.

CAPACITANCE[3] $T_A = 25°C$, f = 1 MHz

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	4	8	pF
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	8	12	pF

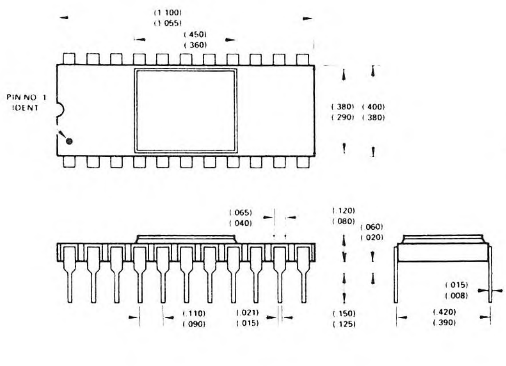
Note 3: This Parameter is periodically sampled and is not 100% tested.

RAMs

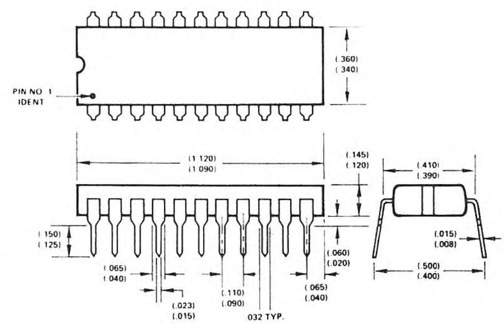
RAMs

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



CMOS 1024x1 Static Random Access Memory

SY5102

MEMORY PRODUCTS

Synertek®

- Very Low Power — 100mW operating
  — 1mW standby
- Pin compatible with SY2102 RAM-operates in same sockets
- Standby operation whenever chip is not selected
- Single +5V power supply
- Power Down (2 volt) memory retention
- Totally TTL compatible—inputs and outputs
- 3-state output

RAMs

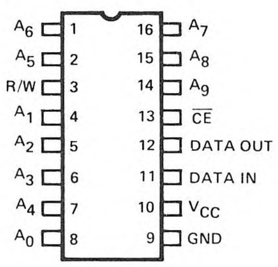
The SY5102, a 1024 word x 1 bit CMOS static RAM is a low power pin-for-pin replacement for the industry standard 2102. The device is fabricated with Synertek's silicon gate, ion implanted CMOS process which allows production of very low power, high performance memories.

The 5102 is a completely static design, requiring no refresh or clocks. Low standby power can be achieved without external power down circuits—whenever the device is not enabled ($\overline{CE}$ = Logic 1) minimum standby current is drawn from the +5 volt supply. To simplify design of systems using battery backup for non volatility, the SY5102L will also maintain memory storage at supply voltages as low as 2.0 volts.

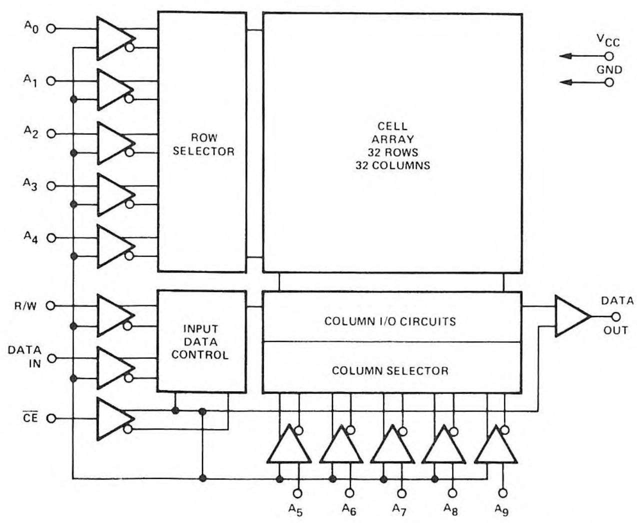
A Chip Enable input controls the 3-state output to make construction of large memory systems simple. Write and Read cycles are selected by applying the appropriate logic signal to the R/W input with V_{CC} at +5 volts.

The 5102 is intended for use in memory systems using battery backup and/or power down techniques in order to reduce standby power dissipation and in battery powered systems where low operating power is needed. The 5102 will extend battery life in an existing 2102 design and will also permit the elimination of expensive power down circuits.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package	Access Time	Temperature Range	2.0 Volt Memory Retention
SYC5102-3	Ceramic	650nsec	0°C to +70°C	No
SYC5102L-3	Ceramic	650nsec	0°C to +70°C	Yes
SYP5102-3	Plastic	650nsec	0°C to +70°C	No
SYP5102L-3	Plastic	650nsec	0°C to +70°C	Yes

PRELIMINARY DATA SHEET. Subject to change. Supplemental data may be released at a later date. Synertek reserves the right to make changes in these specifications at any time without notice.

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B-10K-6/77

RAMs

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to +150°C
*Voltage on Any Pin With Respect to Ground	−0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage	+7.0V
Power Dissipation	1 Watt

*Note: During application of power care must be taken to assure that the input voltage on any pin (V_{IN}) is constrained as follows: $-0.3V \leq V_{IN} \leq V_{CC} +0.3V$

COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ±5% (Unless Otherwise Specified) (For SY5102-3, 5102L-3)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{LI}	Input Current			5	μA	
I_{LO}	Output Leakage Current			±5	μA	$\overline{CE}$ = 2.0V; V_{OUT} = 0V to V_{CC}
I_{CC1}	Supply Current		10	20	mA	$V_{IN}=V_{CC}$ Except $\overline{CE} \leq 0.8V$ Output Open
I_{CC2}	Supply Current		14	25	mA	V_{IN}=2.0V Except $\overline{CE} \leq 0.8V$ Output Open
I_{CCL}[1]	Standby Supply Current		1	200	μA	$\overline{CE}$ = V_{CC}; V_{CC} = 5.25V
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 1.0mA

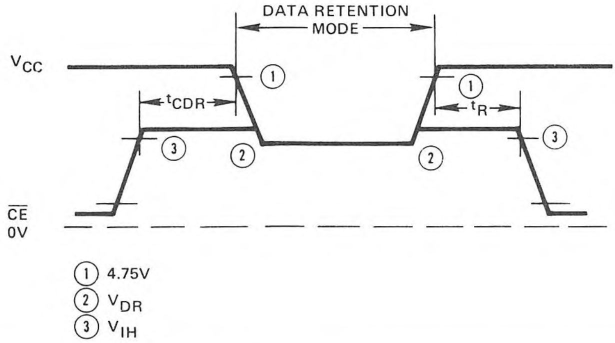
NOTE 1: Includes I_{LI} and I_{LO}

LOW V_{CC} DATA RETENTION CHARACTERISTICS

T_A = 0°C to +70°C (For SY5102L-3)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DR}	V_{CC}	2.0		V	$\overline{CE}$ = V_{DR}, V_{IN} = V_{DR}
I_{DR}	I_{CC}		200	μA	$\overline{CE}$ = V_{DR}, V_{IN}= V_{DR}
t_{CDR}	Data Retention Lead Time	0		nsec	
t_R	Operation Recovery Time	t_{RC}[2]			

NOTE 2: t_{RC} is Read Cycle Time



A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified

Symbol	Parameter	Min	Max	Unit
READ CYCLE				
t_{RC}	Read Cycle	650		ns
t_A	Access Time		650	ns
t_{CO}	Chip Enable to Output Time		650	ns
t_{OH1}	Previous Read Data Valid with Respect to Address Change	50		ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable Change	0		ns
WRITE CYCLE				
t_{WC}	Write Cycle	650		ns
t_{AW}	Address to Write Setup Time	150		ns
t_{WP}	Write Pulse Width	400		ns
t_{WR}	Write Recovery Time	50		ns
t_{DW}	Data Setup Time	400		ns
t_{DH}	Data Hold Time	100		ns
t_{CW}	Chip Enable to Write Setup Time	550		ns

A.C. TEST CONDITIONS

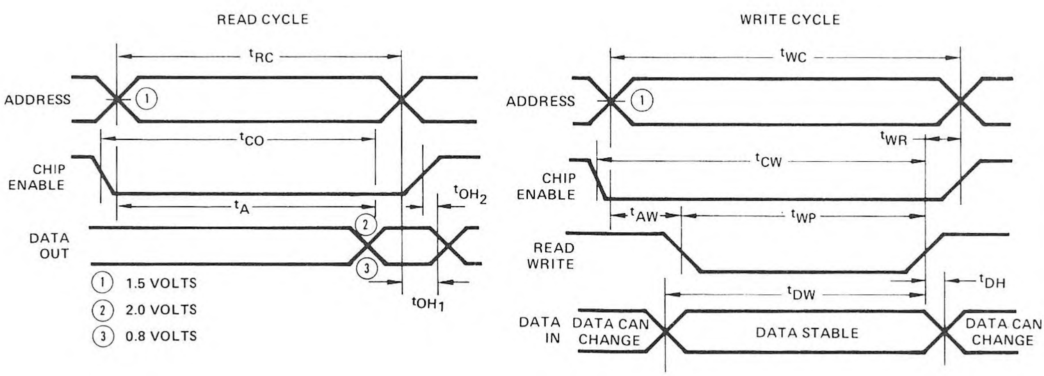
Input Pulse Levels: +0.8V to 2.0V

Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: INPUT: 1.5V
OUTPUT: 0.8 and 2.0V

Output Load: 1 TTL Gate and $C_L = 100$ pF

WAVEFORMS



CAPACITANCE[3] $T_A = 25°C$, f = 1 MHz

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0V$	3	5	pF
C_{OUT}	Output Capacitance $V_{OUT} = 0V$	7	10	pF

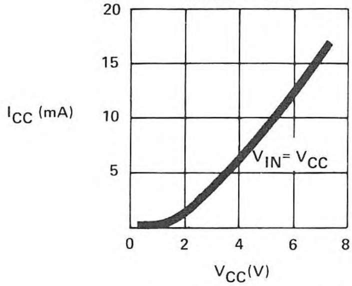
Note 3: This Parameter is periodically sampled and is not 100% tested.

RAMs

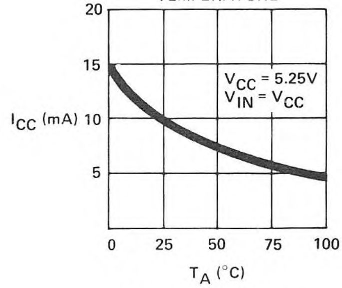
RAMs

TYPICAL CHARACTERISTICS

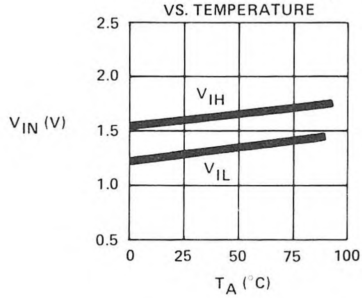
SUPPLY CURRENT VS. VOLTAGE



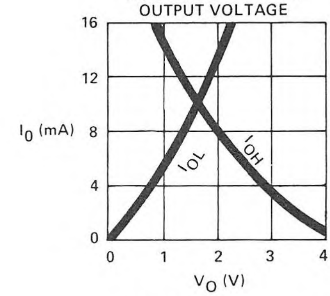
SUPPLY CURRENT VS. TEMPERATURE



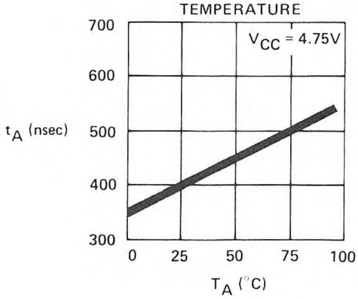
INPUT VOLTAGE LIMITS VS. TEMPERATURE



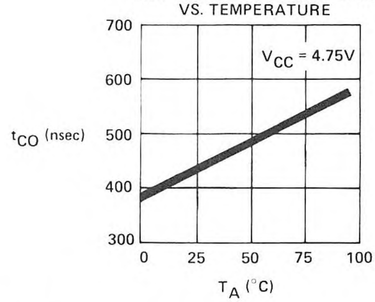
OUTPUT CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. TEMPERATURE

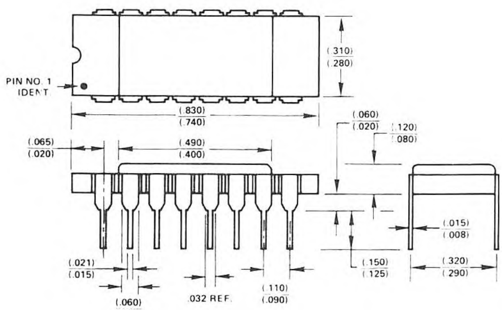


CHIP SELECT TO OUTPUT TIME VS. TEMPERATURE

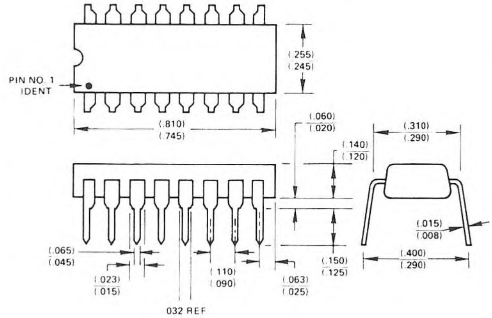


PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



Read Only Memories

Read Only Memories

4

512x8 Static Read Only Memory

Synertek®

SY2530

MEMORY PRODUCTS

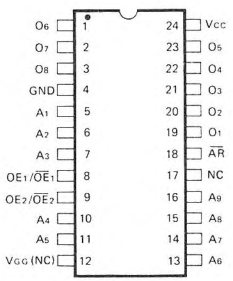
- Single +5 Volt Supply – No –12 Volt Supply
- Up to 75% Power Reduction Over PMOS Part
- Two Week Prototype Turnaround
- 512x8 Bit Organization
- Access Time – 550ns. (max.)
- Synchronous or Asynchronous Operation
- Totally Static Operation
- Completely TTL Compatible
- On-Chip Address Registers
- Two Programmable Output Enables
- Three-State Output for Wire-OR Expansion
- Replaces Signetics 2530

The SY2530 high performance read only memory is organized 512 words by 8 bits. This device is designed to be compatible with all microprocessor and similar memory applications where large bit storage and simple interfacing are important. Synertek's N-channel ion-implanted silicon gate process eliminates the –12 Volt supply requirement, producing a completely TTL compatible ROM without increasing the +5 Volt supply current. This SY2530 dissipates only 30% on the power of the P-channel competitive device.

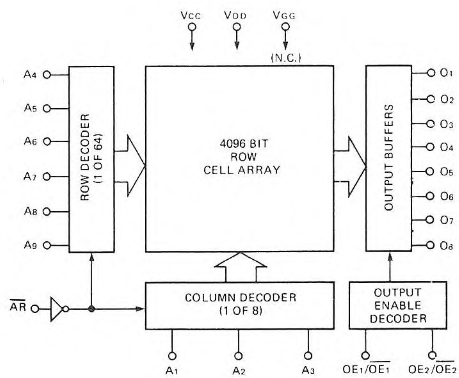
Clocking the Address Read ($\overline{AR}$) input stores the applied address information in the address registers. The outputs appear and remain stable until a new address is read. If the $\overline{AR}$ input is tied LOW, output data asynchronously appear 550ns after the application of a new address.

ROMs

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2530	Ceramic	500ns	0°C to +70°C
SYP2530	Plastic	500ns	0°C to +70°C

A custom number will be assigned by Synertek.

Synertek • P.O. Box 552 • Santa Clara, CA 95051 • Telephone (408) 984-8900 • TWX: 910-338-0135

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0° to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	Vcc = 4.75V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	Vcc = 4.75V, I_{OH} = 2.4 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current	−1.0	+1.0	uA	Vcc = 5.25V, 0V ≤ V_{in} ≤ 5.25V
I_{LO}	Output Leakage Current	−1.0	+1.0	uA	Chip Deselected V_{out} = +0.4V to Vcc
I_{CC}	Power Supply Current		50	mA	Output Unloaded Vcc = 5.25V, V_{in} = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

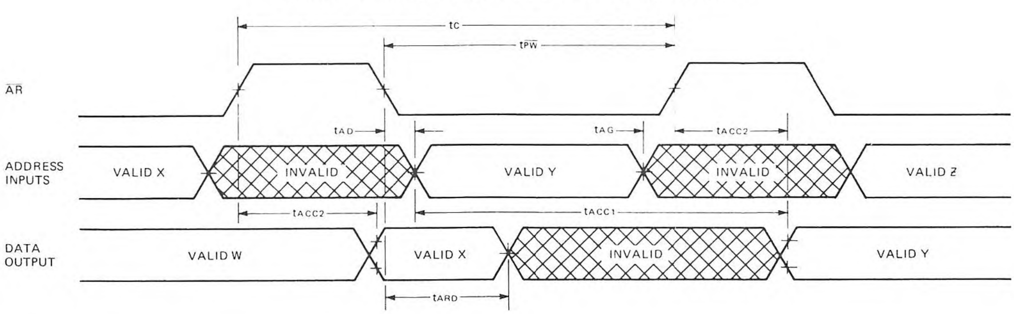
A.C. CHARACTERISTICS

T_A = 0°C to +70°C, Vcc = 5.0 V ± 5% (unless otherwise specified)

CLOCKED MODE TIMING SPECIFICATIONS (See Figure 1)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_C	Cycle Time	700		ns	Output load: 1.5 TTL gates and 100pf
t_{ACC1}	Address to Output Access Time		550	ns	Input transition time: 20ns
t_{ACC2}	End of AR to Output Delay		100	ns	Timing reference levels:
t_{PW}	AR LOW Pulse Width	500		ns	Input: 1.5V
t_{AD}	Address Delay Time	0	50	ns	Output: 0.4V and 2.4V
t_{AG}	Address to AR Gap	0	50	ns	
t_{ARD}	Previous Data Valid After AR Negative Transition	20		ns	

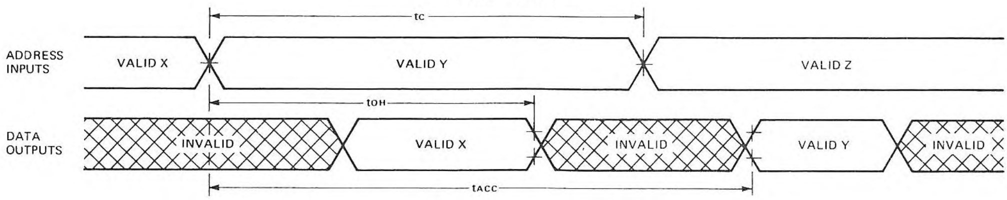
FIGURE 1 — CLOCKED MODE TIMING DIAGRAM



UNCLOCKED MODE TIMING SPECIFICATIONS (See Figure 2)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_C	Cycle Time	550		ns	AR = Vcc
t_{ACC}	Address Access Time		550	ns	See clocked mode timing specifications
t_{OH}	Previous Data Valid After Address Change Delay	20		ns	

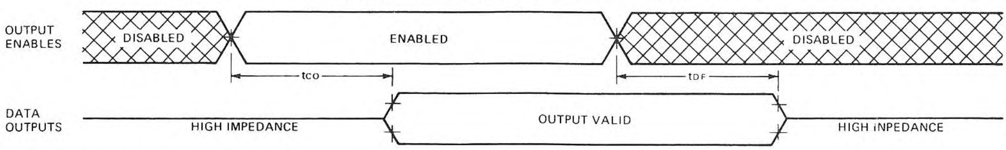
FIGURE 2 – UNCLOCKED MODE TIMING DIAGRAM
(AR = Vcc)



OUTPUT ENABLE TIMING SPECIFICATIONS (CLOCKED OR UNCLOCKED) (See Figure 3)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{CO}	Output Enable Delay		300	ns	See clocked mode timing specifications
t_{DF}	Output Disable Delay		300	ns	

FIGURE 3 – OUTPUT ENABLE TIMING DIAGRAM
(CLOCKED OR UNCLOCKED MODES)



CAPACITANCE

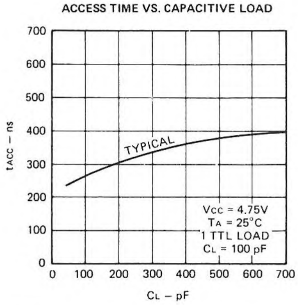
t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		6	pF	All pins except pin under test tied to AC ground
C_O	Output Capacitance		10	pF	

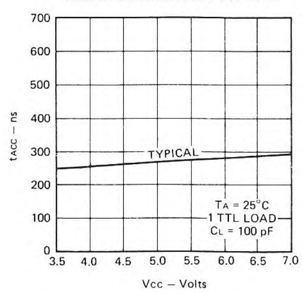
Note 2: This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

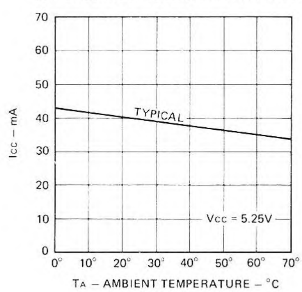
ACCESS TIME VS. CAPACITIVE LOAD



ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ROMs

PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–10	Data format, Signetics punched card format may be used. Specify by punching "SIGNETICS," starting name at column one.
Second Card	1–10	CARD
Third Card	1–10	Synertek part number; punch "2530."
Fourth Card	1–10	Leave blank – pattern number to be assigned by Synertek
Fifth Card	1–5	"2530N" or "2530I"
	15–19	Punch "CODED"
	21	$CS_2/\overline{CS_2}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	22	$CS_1/\overline{CS_1}$ chip select logic level
	24–71	Customer company name
	73–80	Date
Sixth Card	1	"C"
	3–80	Person responsible for reviewing truth table and company name
Seventh Card	1	"C"
	3–80	Customer street address
Eighth Card	1	"C"
	3–80	Customer city, state, zip

SIGNETICS DATA CARD FORMAT

All addresses are coded in decimal form (0 through 511). All output words are coded in binary form. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB. The eight Title Cards listed above must accompany the card deck:

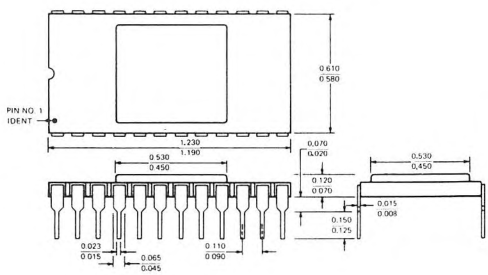
	COLUMN	INFORMATION
Data Cards	1–3	Decimal address (blank, blank, 0).
	5–12	8-digit binary output (MSB-left)
	21–23	Decimal address, (blank, blank, 1).
	25–32	8-digit binary output (MSB-left)
	41–43	Decimal address, (blank, blank, 2).
	45–52	8-digit binary output (MSB-left)
	61–63	Decimal address, (blank, blank, 3).
	65–72	8-digit binary output (MSB-left)

Send bit pattern data to the following special address:

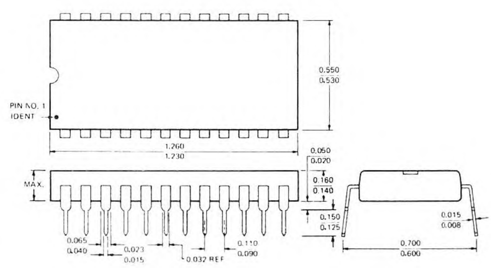
Synertek – ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



2048x8 Static Read Only Memory

SY2316A SY2316B

MEMORY PRODUCTS

Synertek®

- 2048x8 Bit Organization
- Single +5 Volt Supply
- Metal Mask Programming
- Two Week Prototype Turnaround
- Access Time–550ns /450ns (max.)
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- SY2316A – Replacement for Intel 2316A
- SY2316B – Pin Compatible with 2708 EPROM
  – Replacement for Two 2708s

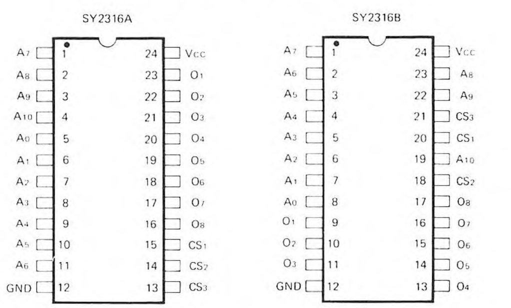
The SY2316A and SY2316B high performance read only memories are organized 2048 words by 8 bits with access times of less than 550 ns and 450 ns. These ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

The SY2316A/B operate totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

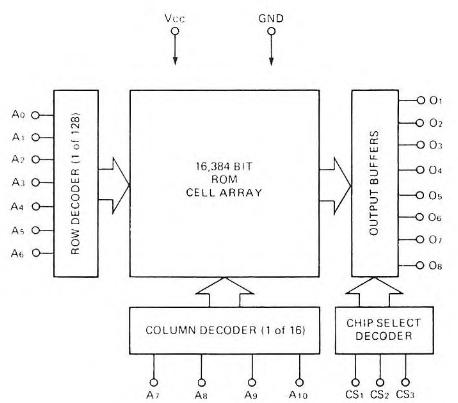
Designed to replace two 2708 8K EPROMs, the SY2316B can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

ROMs

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2316A	Ceramic	550ns	0°C to +70°C
SYP2316A	Plastic	550ns	0°C to +70°C
SYC2316B	Ceramic	450ns	0°C to +70°C
SYP2316B	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

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B-10K-7/76

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0° to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	V_{CC} = 4.75V, I_{OH} = −200 μA
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	V_{CC} = 5.25V, 0V ⩽ V_{in} ⩽ 5.25V
I_{LO}	Output Leakage Current		10	uA	Chip Deselected V_{out} = +0.4V to Vcc
I_{CC}	Power Supply Current		98	mA	Output Unloaded V_{CC} = 5.25V, V_{in} = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	SY2316B		SY2316A		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Address Access Time		450		550	ns	Output load: 1 TTL load and 100 pf
t_{CO}	Chip Select Delay		250		300	ns	Input transition time: 20ns
t_{DF}	Chip Deselect Delay		250		300	ns	Timing reference levels:
t_{OH}	Previous Data Valid After Address Change Delay	20		20		ns	Input: 1.5V Output: 0.8V and 2.2V

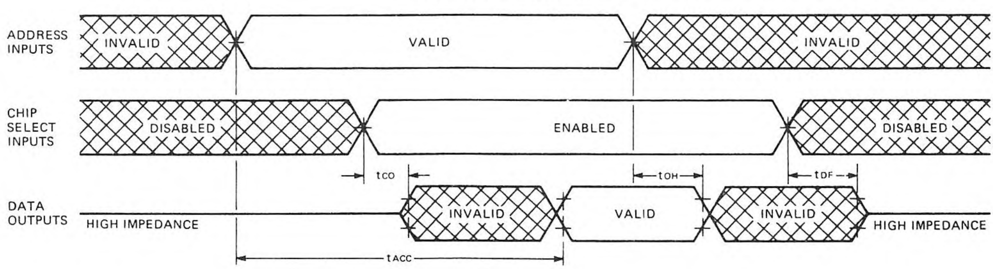
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under test tied to AC ground
C_O	Output Capacitance		10	pF	

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "2316A" or "2316B")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	30	$CS_3/\overline{CS_3}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	31	$CS_2/\overline{CS_2}$ chip select logic level.
	32	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1–8	Data Format. Synertek, or Intel data card format may be used. Specify format by punching "Synertek," or "Intel" starting in column one.
	15–28	Logic format; punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH, and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

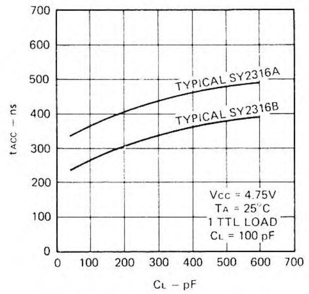
	COLUMN	INFORMATION
Data Cards	1–5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the initial input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7–14	Output data (MSB-LSB) for initial input address.
	16–23	Output data for initial input address +1
	25–32	Output data for initial input address +2
	34–41	Output data for initial input address +3
	43–50	Output data for initial input address +4
	52–59	Output data for initial input address +5
	61–68	Output data for initial input address +6
	70–77	Output data for initial input address +7
	79–80	ROM pattern number (may be left blank)

Send bit pattern data to the following special address:

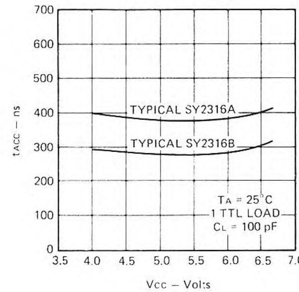
Synertek – ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

TYPICAL CHARACTERISTICS

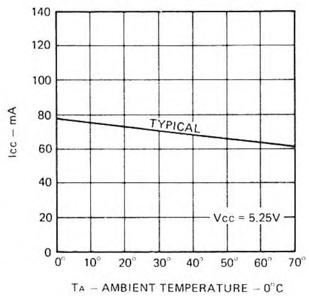
ACCESS TIME VS. CAPACITIVE LOAD



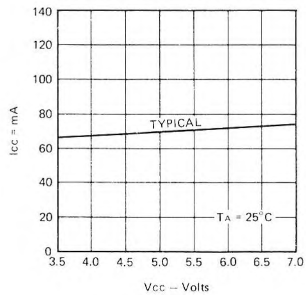
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

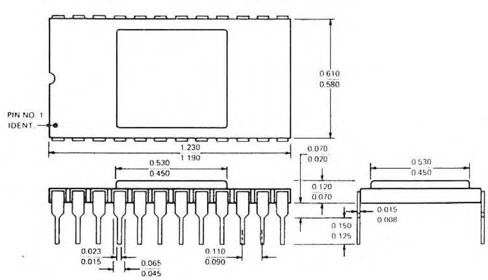


SUPPLY CURRENT VS. SUPPLY VOLTAGE

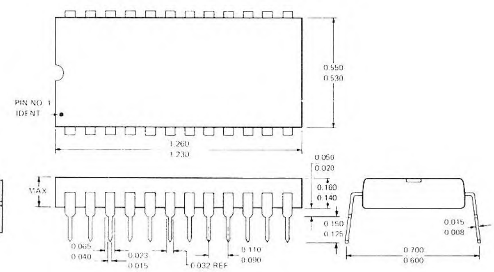


PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



4096 x 8 Static Read Only Memory

SY2332

Synertek®

MEMORY PRODUCTS

- 4096 x 8 Bit Organization
- Single +5 Volt Supply
- Three Week Prototype Turnaround
- Access Time—450ns (max)
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- Pin Compatible with 2716 EPROM
- Replacement for Two 2716s
- 2708/2716 EPROMs Accepted as Program Data Inputs

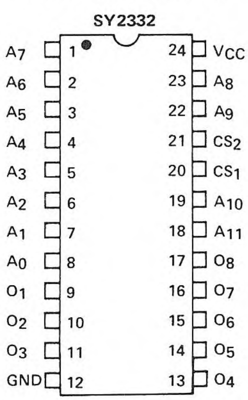
The SY2332 high performance read only memory is organized 4096 words by 8 bits with access times of less than 450 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

The SY2332 operates totally asynchronously. No clock input is required. The two programmable Chip Select inputs allow four 32K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

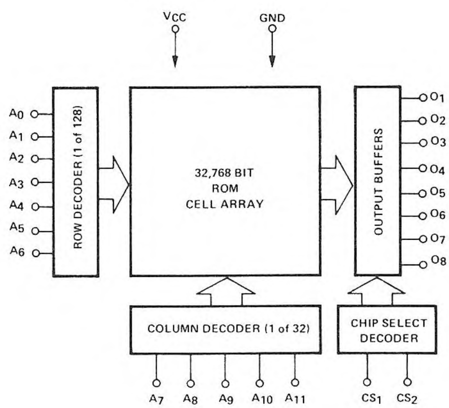
Designed to replace two 2716 16K EPROMs, the SY2332 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

ROMs

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC2332	Ceramic	450ns	0°C to +70°C
SYP2332	Plastic	450ns	0°C to +70°C

A custom number will be assigned by Synertek.

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B-10K-8/77

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	Volts	V_{CC} = 4.75V, I_{OH} = -200µA
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = 4.75V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	Volts	
V_{IL}	Input LOW Voltage	-0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	µA	V_{CC} = 5.25V, 0V ≤ V_{IN} ≤ 5.25V
I_{LO}	Output Leakage Current		10	µA	Chip Deselected V_{OUT} = +0.4 V to V_{CC}
I_{CC}	Power Supply Current		100	mA	Output Unloaded, Chip Enabled V_{CC} = 5.25V, V_{IN} = V_{CC}

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% (unless otherwise specified)

Symbol	Parameter	SY2332		Units	Test Conditions
		Min.	Max.		
t_{ACC}	Address Access Time		450	ns	Output load: 1 TTL load and 100pF
t_{CO}	Chip Select Delay		150	ns	
t_{DF}	Chip Deselect Delay		150	ns	Input transition time: 20ns
t_{OH}	Previous Data Valid After Address Change Delay	20		ns	Timing reference levels: Input: 1.5V Output: 0.8V and 2.0V

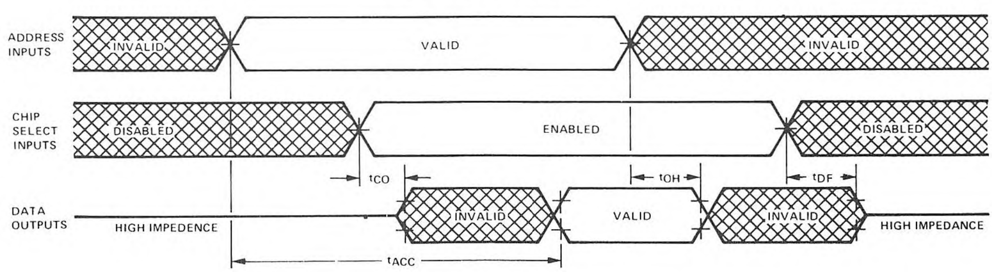
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under test tied to AC ground
C_O	Output Capacitance		10	pF	

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards or 1" wide paper tape.

CARD FORMAT

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMs. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMs. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1-30	Customer name
	31-50	Customer part number
	60-72	Synertek part number (punch "2332")
Second Card	1-30	Customer contact (name)
	31-50	Customer telephone number
Third Card	1-6	Leave blank — pattern number to be assigned by Synertek
	30	$CS_2/\overline{CS_2}$ chip select logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1"; if DON'T CARE, punch "2"
	31	$CS_1/\overline{CS_1}$ chip select logic level.
Fourth Card	1-8	Data Format. Punch "Intel" starting in column one.
	15-28	Logic Format; punch "POSITIVE LOGIC" or NEGATIVE LOGIC."
	35-37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck)

INTEL DATA CARD FORMAT

Output data is punched as either a "P" or an "N"; a "P" is defined as a HIGH and an "N" is defined as a LOW. Output 8 (O_8) is the MSB and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the Intel card deck.

	COLUMN	INFORMATION
Data Cards	1-5	Punch the 5-digit decimal equivalent of the binary coded address which begins each card. This is the inital input address. The address is right justified, i.e. 00000, 00008, 00016, etc.
	7-14	Output data (MSB-LSB) for initial input address.
	16-23	Output data for initial input address +1
	25-32	Output data for initial input address +2
	34-41	Output data for initial input address +3
	43-50	Output data for initial input address +4
	52-59	Output data for initial input address +5
	61-68	Output data for initial input address +6
	70-77	Output data for initial input address +7
	79-80	ROM pattern number (may be left blank)

INTEL PAPER TAPE FORMAT

The paper tape which should be used is 1" wide paper tape using 7 or 8 bit ASCII code, such as a model 33 ASR teletype produces.

BPNF Format

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field Ø (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F for the N x 8 organization.
   NO OTHER CHARACTERS, SUCH AS RUBOUTS, ARE ALLOWED ANYWHERE IN A WORD FIELD. If in preparing a tape, an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high tape level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes)
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc. are inserted, the tape may be easily listed on the teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number and if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bit of the device outputs. Refer to the data sheet for the pin numbers.

HEXADECIMAL PROGRAM TAPE FORMAT

The hexadecimal tape format used by the INTELLEC 8 system is a modified memory image, blocked into discrete records. Each record contains record length, record type, memory address, and checksum information in addition to data. A frame by frame description is as follows:

Frame 0	Record mark. Signals the start of a record. The ASCII character colon (":" HEX 3A) is used as the record mark.
Frames 1, 2 (0-9, A-F)	Record length. Two ASCII characters representing a hexadecimal number in the range 0 to 'FF' (0 to 255). This is the count of the actual data bytes in the record type or checksum. A record length of 0 indicates end of file.
Frames 3 to 6	Load Address. Four ASCII characters that represent the initial memory will be loaded. The first data byte is stored in the location pointed to by the load address, succeeding data bytes are loaded into ascending addresses.

ROMs

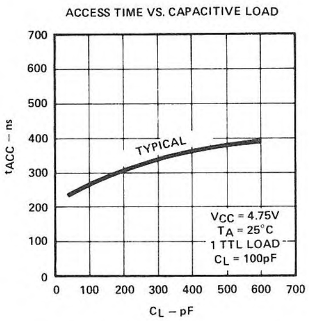
Frames 7, 8	Record type. Two ASCII characters. Currently all records are type 0, this field is reserved for future expansion.
Frames 9 to 9+2* (Record Length) -1	Data. Each 8 bit memory word is represented by two frames containing the ASCII characters (0 to 9, A to F) to represent a hexadecimal value 0 to 'FF' (0 to 255).
Frames 9+2* (Record Length) to 9+2* (Record Length) +1	Checksum. The checksum is the negative of the sum of all 8 bit bytes in the record since the record mark (":") evaluated modulus 256. That is, if you add together all the 8 bit bytes, ignoring all carries out of an 8-bit sum, then add the checksum, the result is zero.

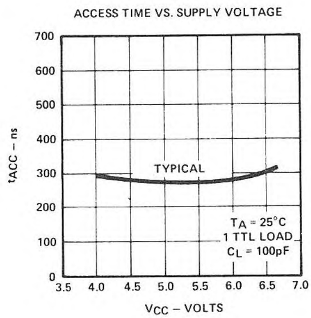
Example: If memory locations 1 through 3 contain 53F8EC, the format of the hex file produced when these locations are punched is:

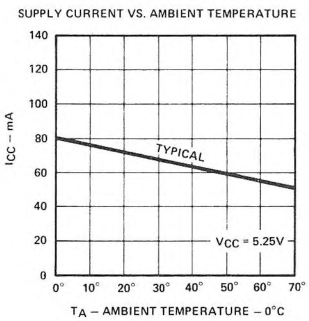
:0300010053F8ECC5

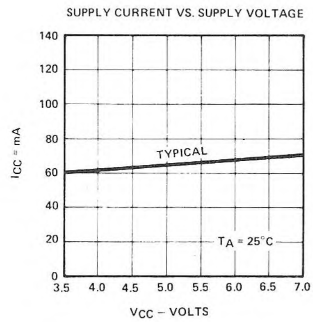
Send bit pattern data to the following special address:
Synertek — ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

TYPICAL CHARACTERISTICS



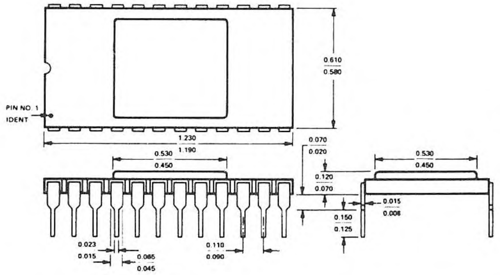




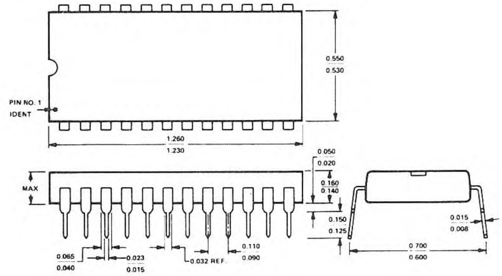


PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



512x8 Static Read Only Memory

Synertek®

SY3514 SY3515

MEMORY PRODUCTS

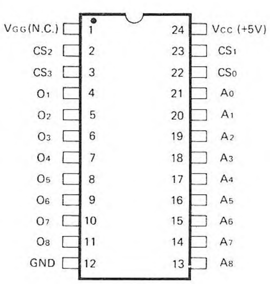
ROMs

- Single +5 Volt Supply—No −12 Volt Supply
- Up to 70% Power Reduction over PMOS Part
- Metal Mask Programming
- Two Week Prototype Turnaround
- 512x8 Bit Organization
- Access Time—700 ns/500 ns (max.)
- Totally Static Operation
- Completely TTL Compatible
- Four Programmable Chip Selects
- Pin-for-Pin and Functional Replacement for:
  - Fairchild 3514/15
  - NSC MM5233
  - Mostek MK2600P
  - AMD Am9214/Am3514

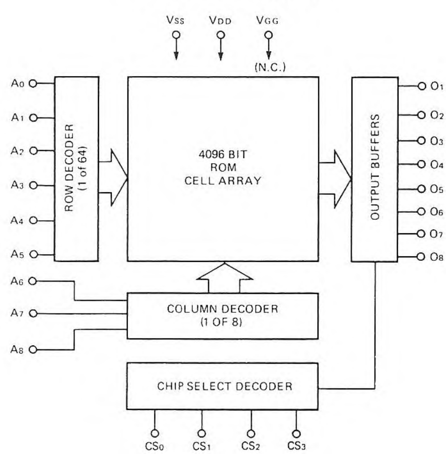
The SY3514 and SY3515 high performance read only memories are organized 512 words by 8 bits with access times of 700 ns, and 500 ns, respectively. Synertek's N-channel ion-implanted silicon gate process eliminates the −12 Volt supply requirement, producing a completely TTL compatible ROM without increasing the +5 Volt supply current. The net result being that overall power dissipation is only 30% of the P-channel competitive devices.

With four programmable Chip Selects, as many as 16 devices may wire-ORed to achieve 8K bytes of Read Only Memory storage. The outputs of unselected devices are in a high impedance state permitting the selected device to control the 8 bit bus. The TTL compatible input and output voltage and current levels offer a worst-case noise immunity of a full 400 mV for simplified system interfacing. There is no connection to the −12 Volt supply pin.

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC3514	Ceramic	700ns	0°C to +70°C
SYP3514	Plastic	700ns	0°C to +70°C
SYC3515	Ceramic	500ns	0°C to +70°C
SYP3515	Plastic	500ns	0°C to +70°C

A custom number will be assigned by Synertek.

ROMs

ABSOLUTE MAXIMUM RATINGS*

Ambient Operating Temperature	0° to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Output Voltage	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V
Power Dissipation	1.0W

COMMENT*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	V_{CC} = 4.75V, I_{OH} = −500 μA
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = 4.75V, I_{OL} = 2.4 mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current	−1.0	+1.0	uA	V_{CC} = 5.25V, 0V ≤ V_{in} ≤ 5.25V
I_{LO}	Output Leakage Current	−1.0	+1.0	uA	Chip Deselected V_{out} = +0.4V to Vcc
I_{CC}	Power Supply Current		50	mA	Output Unloaded V_{CC} = 5.25V, V_{in} = Vcc

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	SY3515		SY3514		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Address Access Time		500		700	ns	Output load: 1 TTL load and 100 pf
t_{CO}	Chip Select Delay		300		500	ns	Input transition time: 20ns
t_{DF}	Chip Deselect Delay		300		500	ns	Timing reference levels:
t_{OH}	Previous Data Valid After Address Change Delay	20		20		ns	Input: 1.5V Output: 0.4V and 2.4V

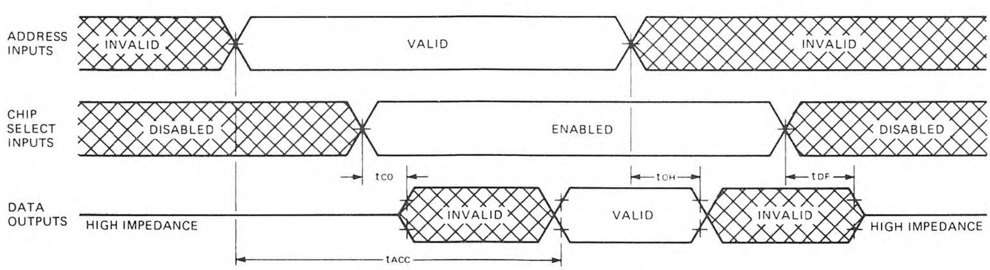
CAPACITANCE

t_A = 25°C, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		6	pF	All pins except pin under test tied to AC ground
C_O	Output Capacitance		10	pF	

Note 2: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–10	Data format, Fairchild or Mostek punched card formats may be used. Specify which data format is being used by punching either "FAIRCHILD" or "MOSTEK" by starting name at column one.
Second Card	1–10	CARD
Third Card	1–10	Synertek part number; if a Fairchild format, punch "3514" or "3515," and if a Mostek format, punch "2600."
Fourth Card	1–10	Leave blank – pattern number to be assigned by Synertek

FAIRCHILD DATA CARD FORMAT

All addresses are coded in binary form (0 = 000000000, and 511 = 111111111 with the MSB first). Output words are also coded in binary form. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the card deck.

	COLUMN	INFORMATION
Fifth Card	10–29	Customer name
	50–62	Punch "3514" (700 ns) or "3515" (500 ns)
	65–80	Customer comments
Sixth Card	29	$CS_3/\overline{CS_3}$ chip select logic level. (Punch "0", if LOW selects chip; punch "1" if HIGH selects chip).
	31	$CS_2/\overline{CS_2}$ chip select logic level.
	33	$CS_1/\overline{CS_1}$ chip select logic level.
	35	$CS_0/\overline{CS_0}$ chip select logic level.
Data Cards	10, 12, 14, 16, 18, 20, 22, 24, 26	Address input pattern. The most significant bit (A_8) is in column 10.
	40, 42, 44, 46, 48, 50, 52, 54	Output pattern. The most significant bit (O_7) is in column 40
	73–80	Coding these columns is optional

SYNERTEK AND MOSTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 511). All output words are coded both in binary and octal forms. Output 8 (O_8) is the MSB, and Output 1 (O_1) is the LSB. The four Title Cards listed above must accompany the card deck.

	COLUMN	INFORMATION
Fifth Card	1–30	Customer
	31–50	Customer part number
	60–72	Synertek or Mostek part number
Sixth Card	1–30	Engineer at customer site
	31–50	Direct phone number for engineer
Seventh Card	1–5	Synertek or Mostek part number
	10–16	Organization
	29	$CS_3/\overline{CS_3}$ chip select logic level. (Punch "0", if LOW selects chip; punch "1" if HIGH selects chip.)
	30	$CS_2/\overline{CS_2}$ chip select logic level.
	31	$CS_1/\overline{CS_1}$ chip select logic level.
	32	$CS_0/\overline{CS_0}$ chip select logic level.
	33	Active pull ups
Eighth Card	1–9	Data format
	15–28	Logic – "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–57	Verification code

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output B8-B1 (MSB thru LSB)
	15–17	Octal equivalent of output data
	⋮	⋮
	64–67	Decimal Address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

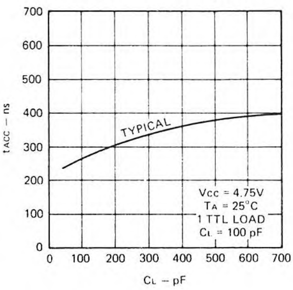
Send bit pattern data to the following special address:

Synertek – ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

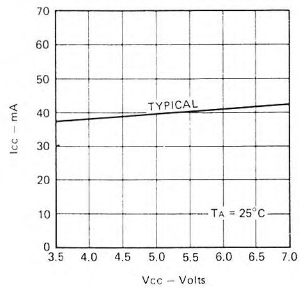
ROMs

TYPICAL CHARACTERISTICS

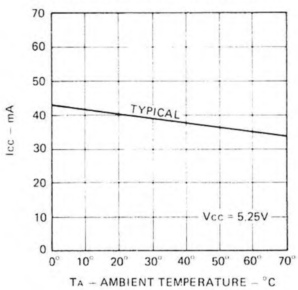
ACCESS TIME VS. CAPACITIVE LOAD



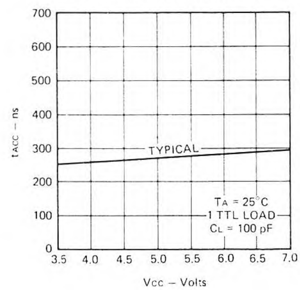
SUPPLY CURRENT VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

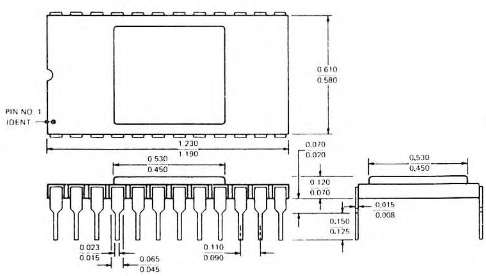


ACCESS TIME VS. SUPPLY VOLTAGE

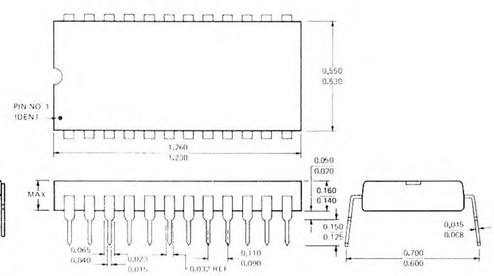


PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



ROMs

2048x8 Static Read Only Memory

SY4600

Synertek®

MEMORY PRODUCTS

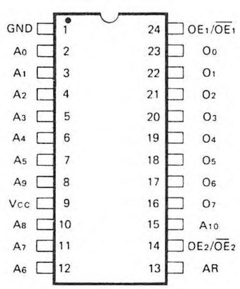
- 2048x8 or 4096x4 Bit Organizations
- Single +5 Volt Supply
- Two Week Prototype Turnaround
- Access Time — 550 ns. (max.)
- Totally Static Operation
- Synchronous or Asynchronous Operation
- Completely TTL Compatible
- Two Programmable Output Enables
- Three-State Outputs for Wire-OR Expansion
- On-Chip Address Registers
- Low Power Dissipation — 31 μW/Bit (max.)
- Pin-for-Pin Replacement for EA4600

The SY4600 is a high performance 16,384 bit static read only memory organized 2048 words by 8 bits or 4096 words by 4 bits. The device is designed to be compatible with all microprocessor and similar applications where large bit storage and simple interfacing are important design considerations. Synertek's N-channel ion-implanted silicon gate process produces a +5 Volt TTL compatible ROM with a minimum noise immunity of 0.4 Volt.

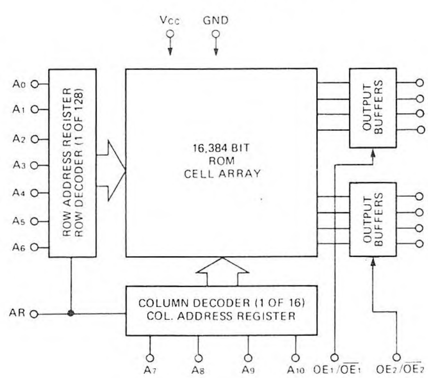
Synchronous or asynchronous operation offers maximum design flexibility. Clocking the Address Read (AR) input stores the applied address information. The outputs appear and remain stable until a new address is read. With the AR input HIGH, output data asynchronously appear 550ns after the application of a new address. Two programmable Output Enables control four outputs each permitting 4 bit or 8 bit operation.

ROMs

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Order Number	Package Type	Access Time	Temperature Range
SYC4600	Ceramic	550ns	0°C to +70°C
SYP4600	Plastic	550ns	0°C to +70°C

A custom number will be assigned by Synertek.

Synertek • P.O. Box 552 • Santa Clara, CA 95051 • Telephone (408) 984-8900 • TWX: 910-338-0135

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0° to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
Applied Output Voltage	−0.5V to +7.0V
Applied Input Voltage	−0.5V to +7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	Vcc	Volts	$V_{CC} = 4.75V$, $I_{OH} = -200\ \mu A$
V_{OL}	Output LOW Voltage		0.4	Volts	$V_{CC} = 4.75V$, $I_{OH} = 2.4$ mA
V_{IH}	Input HIGH Voltage	2.0	Vcc	Volts	
V_{IL}	Input LOW Voltage	−0.5	0.8	Volts	See Note 1
I_{LI}	Input Load Current		10	uA	$V_{CC} = 5.25V$, $0V \leqslant V_{in} \leqslant 5.25V$
I_{LO}	Output Leakage Current		10	uA	Chip Deselected $V_{out} = +0.4V$ to Vcc
I_{CC}	Power Supply Current		98	mA	Output Unloaded $V_{CC} = 5.25V$, $V_{in} = V_{CC}$

Note 1: Input levels that swing more negative than −0.5V will be clamped and may cause damage to the device.

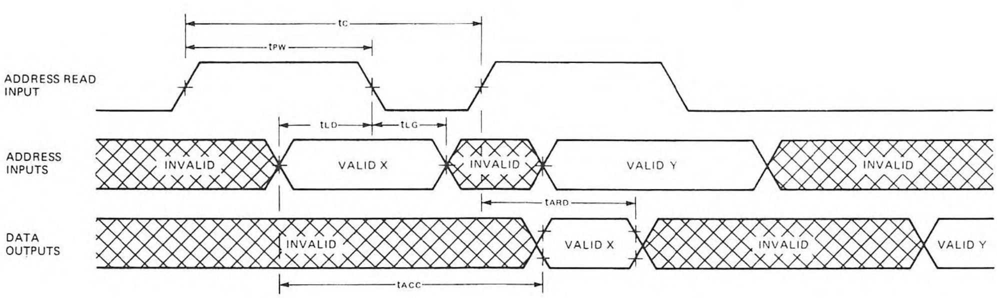
A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\ V \pm 5\%$ (unless otherwise specified)

CLOCKED MODE TIMING SPECIFICATIONS (See Figure 1)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_C	Cycle Time	500		ns	Output load: 1 TTL load and 100 pf
t_{ACC}	Address to Output Delay Time		550	ns	Input transition time: 20 ns
t_{PW}	Address Read Pulse Width	300		ns	Timing reference levels:
t_{LD}	Address Lead Time	100		ns	Input: 1.5V
t_{LG}	Address Lag Time	150		ns	Output: 0.8V and 2.2 V
t_{ARD}	AR Input to Output Disturb Delay	75		ns	

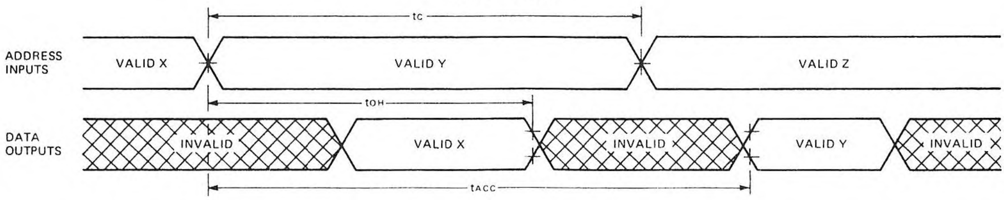
FIGURE 1 — CLOCKED MODE TIMING DIAGRAM



UNCLOCKED MODE TIMING SPECIFICATIONS (See Figure 2)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_C	Cycle Time	500		ns	AR = Vcc
t_{ACC}	Address Access Time		550	ns	See clocked mode timing specifications
t_{OH}	Previous Data Valid After Address Change Delay	75		ns	

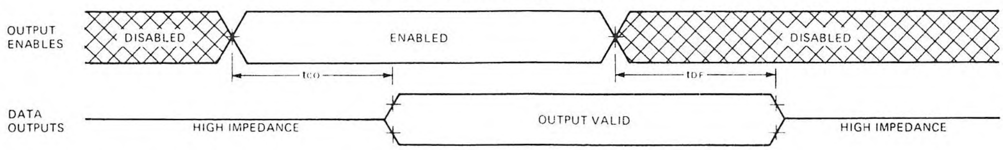
FIGURE 2 – UNCLOCKED MODE TIMING DIAGRAM (AR = Vcc)



OUTPUT ENABLE TIMING SPECIFICATIONS (CLOCKED OR UNCLOCKED) (See Figure 3)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{CO}	Output Enable Delay		300	ns	See clocked mode timing specifications
t_{DF}	Output Disable Delay		300	ns	

FIGURE 3 – OUTPUT ENABLE TIMING DIAGRAM (CLOCKED OR UNCLOCKED MODES)



CAPACITANCE

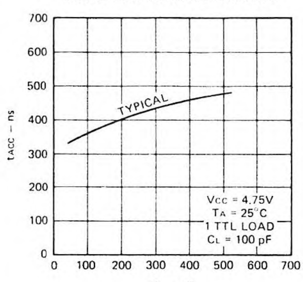
$t_A = 25°C$, f = 1.0MHz, See Note 2

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under test tied to AC ground
C_O	Output Capacitance		10	pF	

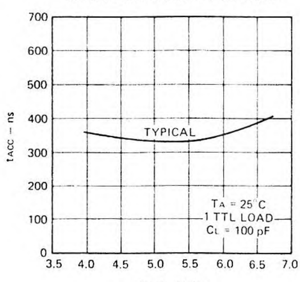
Note 2: This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

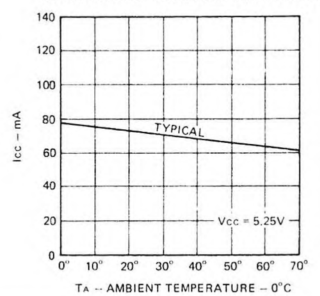
ACCESS TIME VS. CAPACITIVE LOAD



ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE



PROGRAMMING INSTRUCTIONS

All Synertek read only memories utilize computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on standard 80 column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Each deck of cards defining a specific ROM bit pattern consists of 1) four Title Cards and 2) address and bit pattern Data Cards. Positive logic is generally used on all input cards: a logic "1" is the most positive or HIGH level, and a logic "0" is the most negative or LOW level. Synertek can also accept ROM data in other formats, compatible with most microprocessors and PROMS. Consult your Synertek representative for details.

TITLE CARDS

A set of four Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These four Title Cards must contain the following information:

	COLUMN	INFORMATION
First Card	1–30	Customer name
	31–50	Customer part number
	60–72	Synertek part number (punch "4600")
Second Card	1–30	Customer contact (name)
	31–50	Customer telephone number
Third Card	1–6	Leave blank – pattern number to be assigned by Synertek
	31	$OE_2/\overline{OE_2}$ output enable logic level (if LOW selects chip, punch "0"; if HIGH selects chip, punch "1")
	32	$OE_1/\overline{OE_1}$ output enable logic level.
Fourth Card	1–8	Data Format. Synertek, or Electronic Arrays data card format may be used. Specify format by punching "Synertek" or "EA" starting in column one.
	15–28	Logic format: punch "POSITIVE LOGIC" or "NEGATIVE LOGIC."
	35–37	Truth table verification code; punch either "VERIFICATION HOLD" (manufacturing starts after customer approval of bit pattern data supplied by Synertek) or "VERIFICATION NOT NEEDED" (manufacturing starts immediately upon receipt of customer card deck).

SYNERTEK DATA CARD FORMAT

All addresses are coded in decimal form (0 through 2047). All output words are coded both in binary and octal forms. Output 7 (O_7) is the MSB, and Output 0 (O_0) is the LSB.

	COLUMN	INFORMATION
Data Cards	1–4	Decimal address
	6–13	Output (MSB-LSB)
	15–17	Octal equivalent of output data
	22–25	Decimal address
	27–34	Output (MSB-LSB)
	36–38	Octal equivalent of output data
	43–46	Decimal address
	48–55	Output (MSB-LSB)
	57–59	Octal equivalent of output data
	64–67	Decimal address
	69–76	Output (MSB-LSB)
	78–80	Octal equivalent of output data

ELECTRONIC ARRAYS DATA CARD FORMAT

All addresses are coded in octal form (address 0 = 0000, address 2047 = 3777, A_{10} = MSB and A_0 = LSB). All output words are also coded in octal. Output 7 (O_7) is the MSB, and Output 0 (O_0) is the LSB. The four Title Cards discussed above must accompany the EA card deck.

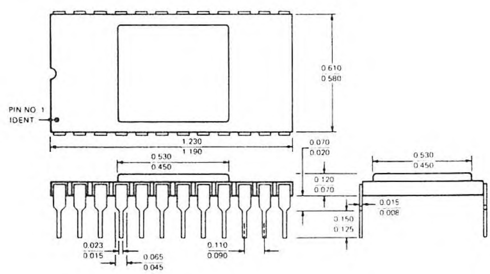
	COLUMN	INFORMATION
Data Cards	1–4	Octal equivalent of initial input address.
	5–7	Octal equivalent of output data for initial input address.
	8–10	Octal equivalent of output data for initial input address +1.
	11–13	Octal equivalent of output data for initial address +2
	⋮	⋮
	50–52	Octal equivalent of output data for initial address +15.
	69–80	ROM pattern number (may be left blank).

Send bit pattern data to the following special address:

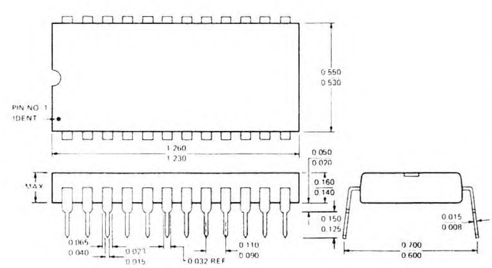
Synertek – ROM
P.O. Box 552
3050 Coronado Drive
Santa Clara, CA 95051

PACKAGING DIAGRAM

CERAMIC PACKAGE



PLASTIC PACKAGE



Microprocessors

Microprocessors

Synertek®

3050 Coronado Drive, Santa Clara, CA. 95051
(408) 984-8900 TWX 910-338-0135

SY6500 MICROPROCESSORS

The SY6500 Microprocessor Family Concept ----

The SY6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock osscillators and drivers. All of the microprocessors in the SY6500 group are software compatible within the group and are bus compatible with the M6800 product offering.

The family includes five microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for the multi processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz and 2 MHz ("A" suffix on product numbers) maximum operating frequencies.

Features of the SY6500 Family

- Single five volt supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- Bi-directional Data Bus
- Instruction decoding and control
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1MHz and 2MHz operation
- On-the-chip clock options
  * External single clock input
  * RC time base input
  * Crystal time base input
- 40 and 28 pin package versions
- Pipeline architecture

Members of the Family

Microprocessors with On-Board Clock Oscillator

- SY6502
- SY6503
- SY6504
- SY6505
- SY6506

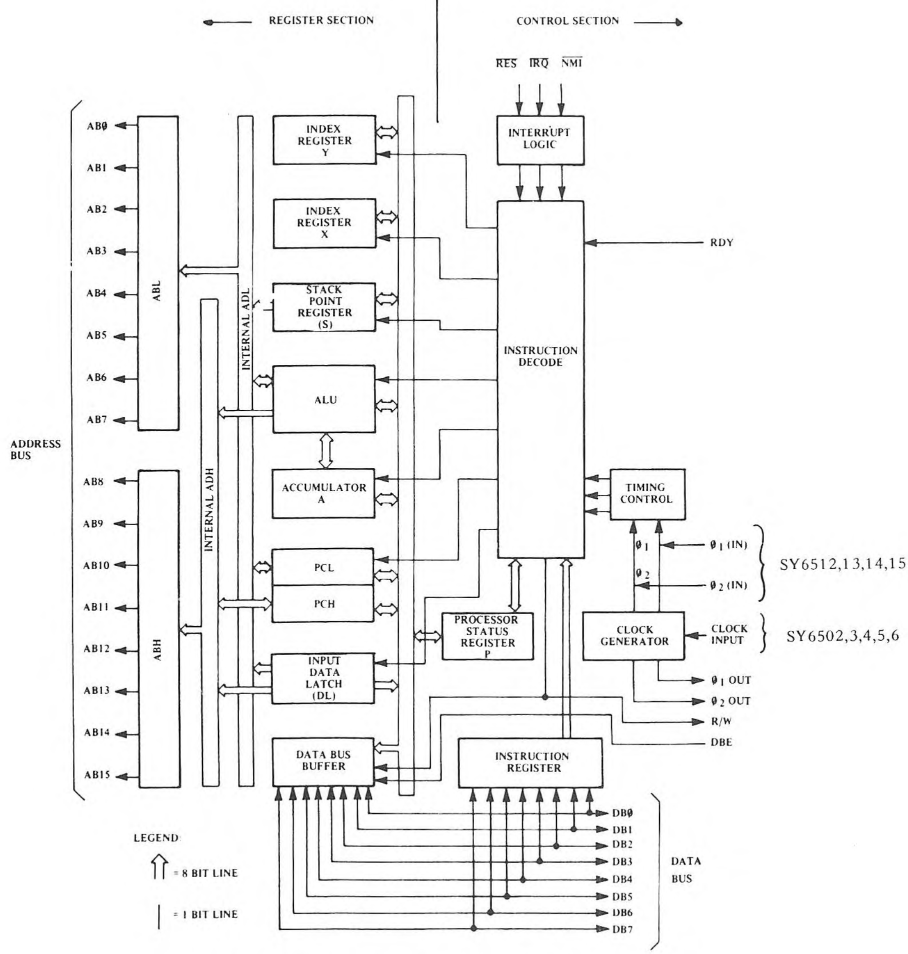
Microprocessors with External Two Phase Clock Input

- SY6512
- SY6513
- SY6514
- SY6515

Comments on the Data Sheet

The data sheet is constructed to review first the basic "Common Characteristics" - those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

COMMON CHARACTERISTICS



Note: 1. Clock Generator is not included on SY6512,13,14,15
2. Addressing Capability and control options vary with each of the SY6500 Products.

SY6500 Internal Architecture

MICRO-PROCESSORS

COMMON CHARACTERISTICS

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	Vcc	-0.3 to +7.0	Vdc
INPUT VOLTAGE	Vin	-0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T_A	0 to +70	°C
STORAGE TEMPERATURE	T_{STG}	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

LECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, Vss = 0, T_A = 25° C)

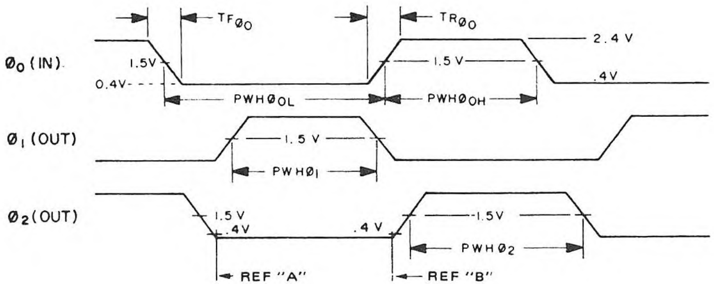
$\emptyset_1$, $\emptyset_2$ applies to SY6512, 13, 14, 15, $\emptyset_{o(in)}$ applies to SY6502, 03, 04, 05 and 06

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}				Vdc
Logic, $\emptyset_{o(in)}$		Vss + 2.4	-	Vcc	
$\emptyset_1$, $\emptyset_2$		Vcc - 0.2	-	Vcc + 0.25	
Input Low Voltage	V_{IL}				Vdc
Logic, $\emptyset_{o(in)}$		Vss - 0.3	-	Vss + 0.4	
$\emptyset_1$, $\emptyset_2$		Vss - 0.3	-	Vss + 0.2	
Input High Threshold Voltage	V_{IHT}				
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		Vss + 2.0	-	-	Vdc
Input Low Threshold Voltage	V_{ILT}				
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		-	-	Vss + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25V, Vcc = 0)	I_{in}				
Logic (Excl. RDY, S.O.)		-	-	2.5	μA
$\emptyset_1$, $\emptyset_2$		-	-	100	μA
$\emptyset_{o(in)}$		-	-	10.0	μA
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4V, Vcc = 5.25V)	I_{TSI}				μA
Data Lines		-	-	10	
Output High Voltage (I_{LOAD} = -100μAdc, Vcc = 4.75V)	V_{OH}				
SYNC, Data, A0-A15, R/W		Vss + 2.4	-	-	Vdc
Output Low Voltage (I_{LOAD} = 1.6mAdc, Vcc = 4.75V)	V_{OL}				
SYNC, Data, A0-A15, R/W		-	-	Vss + 0.4	Vdc
Power Dissipation	P_D	-	.25	.70	W
Capacitance (V_{in} = 0, T_A = 25°C, f = 1MHz)	C				pF
Logic	C_{in}	-	-	10	
Data		-	-	15	
A0-A15, R/W, SYNC	C_{out}	-	-	12	
$\emptyset_{o(in)}$	$C_{\emptyset_{o(in)}}$	-	-	15	
$\emptyset_1$	$C_{\emptyset_1}$	-	30	50	
$\emptyset_2$	$C_{\emptyset_2}$	-	50	80	

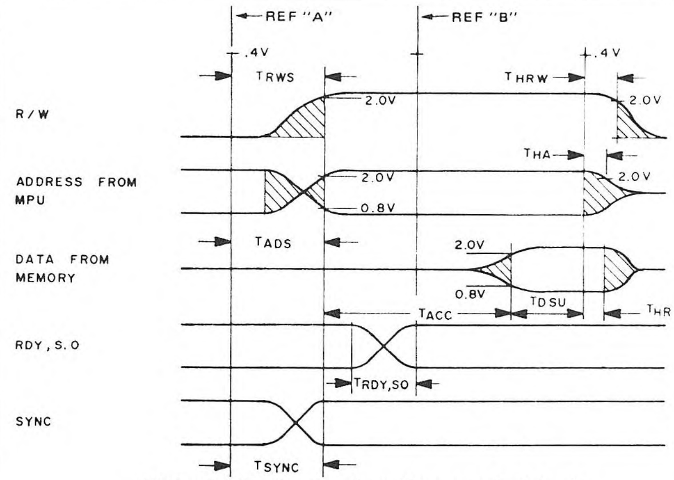
nte: $\overline{IRQ}$ and $\overline{NMI}$ require 3K pull-up resistors.

MICRO-PROCESSORS

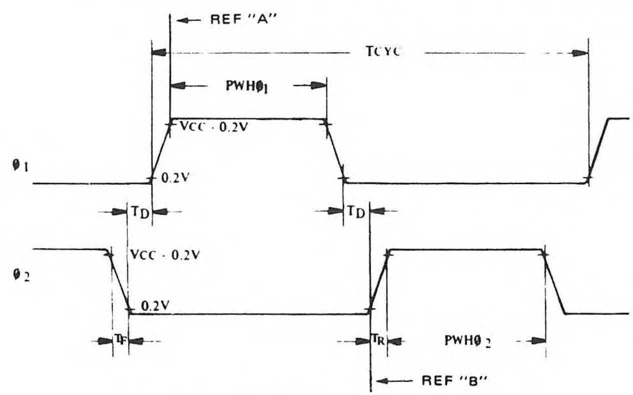
COMMON CHARACTERISTICS



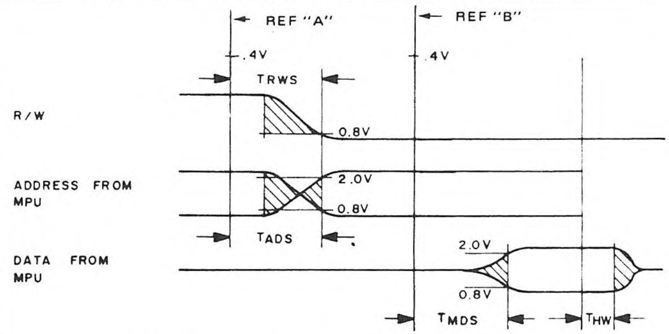
CLOCK TIMING – SY6502, 03, 04, 05, 06



Timing for Reading Data from Memory or Peripherals



CLOCK TIMING – SY6512, 13, 14, 15



Timing for Writing Data to Memory or Peripherals

Note: "REF." means Reference Points on clocks.

CLOCK TIMING – SY6512, 13, 14, 15

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Cycle Time	T_{CYC}	1000	---	---	nsec
Clock Pulse Width Ø1 (Measured at Vcc – 0.2v) Ø2	PWH Ø1 PWH Ø2	430 470	---	---	nsec
Fall Time (Measured from 0.2v to Vcc – 0.2v)	T_F	---	---	25	nsec
Delay Time between Clocks (Measured at 0.2v)	T_D	0	---	---	nsec

CLOCK TIMING – SY6502, 03, 04, 05, 06

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	1000	--	--	ns
$\phi_{o(IN)}$ Pulse Width (measured at 1.5V)	$PWH\phi_o$	460	--	520	ns
$\phi_{o(IN)}$ Rise, Fall Time	$TR\phi_o, TF\phi_o$	--	--	10	ns
Delay Time Between Clocks (measured at 1.5V)	T_D	5	--	--	ns
$\phi_{1(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\phi_1$	$PWH\phi_{oL}$-20	--	$PWH\phi_{oL}$	ns
$\phi_{2(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\phi_2$	$PWH\phi_{oH}$-40	--	$PWH\phi_{oH}$-10	ns
$\phi_{1(OUT)}$, $\phi_{2(OUT)}$ Rise, Fall Time (measured .8V to 2.0 V) (Load = 30pf + 1 TTL)	T_R, T_F	--	--	25	ns

READ/WRITE TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from SY6500	T_{RWS}	--	100	300	ns
Address Setup Time from SY6500	T_{ADS}	--	100	300	ns
Memory Read Access Time	T_{ACC}	--	--	575	ns
Data Stability Time Period	T_{DSU}	100	--	--	ns
Data Hold Time - Read	T_{HR}	10	--	--	ns
Data Hold Time - Write	T_{HW}	30	60	--	ns
Data Setup Time from SY6500	T_{MDS}	--	150	200	ns
RDY, S.O. Setup Time	T_{RDY}	100	--	--	ns
SYNC Setup Time from SY6500	T_{SYNC}	--	--	350	ns
Address Hold Time	T_{HA}	30	60	--	ns
R/W Hold Time	T_{HRW}	30	60	--	ns

CLOCK TIMING – SY6512,13,14,15,16

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Cycle Time	T_{CYC}	500	---	---	nsec
Clock Pulse Width Ø1 (Measured at Vcc – 0.2v) Ø2	PWH Ø1 PWH Ø2	215 235	---	---	nsec
Fall Time (Measured from 0.2v to Vcc – 0.2v)	T_F	---	---	12	nsec
Delay Time between Clocks (Measured at 0.2v)	T_D	0	---	---	nsec

CLOCK TIMING – SY6502, 03, 04, 05, 06

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	500	--	--	ns
$\phi_{o(IN)}$ Pulse Width (measured at 1.5V)	$PWH\phi_o$	240	--	260	ns
$\phi_{o(IN)}$ Rise, Fall Time	$TR\phi_o, TF\phi_o$	--	--	10	ns
Delay Time Between Clocks (measured at 1.5V)	T_D	5	--	--	ns
$\phi_{1(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\phi_1$	$PWH\phi_{oL}$-20	--	$PWH\phi_{oL}$	ns
$\phi_{2(OUT)}$ Pulse Width (measured at 1.5V)	$PWH\phi_2$	$PWH\phi_{oH}$-40	--	$PWH\phi_{oH}$-10	ns
$\phi_{1(OUT)}$, $\phi_{2(OUT)}$ Rise, Fall Time (measured .8V to 2.0 V) (Load = 30pf + 1 TTL)	T_R, T_F	--	--	25	ns

READ/WRITE TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from SY6500 A	T_{RWS}	--	100	150	ns
Address Setup Time from SY6500 A	T_{ADS}	--	100	150	ns
Memory Read Access Time	T_{ACC}	--	--	300	ns
Data Stability Time Period	T_{DSU}	50	--	--	ns
Data Hold Time - Read	T_{HR}	10	--	--	ns
Data Hold Time - Write	T_{HW}	30	60	--	ns
Data Setup Time from SY6500 A	T_{MDS}	--	75	100	ns
RDY, S.O. Setup Time	T_{RDY}	50	--	--	ns
SYNC Setup Time from SY6500 A	T_{SYNC}	--	--	175	ns
Address Hold Time	T_{HA}	30	60	--	ns
R/W Hold Time	T_{HRW}	30	60	--	ns

COMMON CHARACTERISTICS

Clocks ($\emptyset_1$, $\emptyset_2$)

The SY651X requires a two phase non-overlapping clock that runs at the Vcc voltage level.

The SY650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Details of this feature are discussed in the SY6502 portion of this data sheet.

Address Bus (A_0-A_{15}) (See sections on each micro for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130pf.

Data Bus (D_0-D_7)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130pf.

Data Bus Enable (DBE)

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two ($\emptyset_2$) clock, thus allowing data output from microprocessor only during $\emptyset_2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)

This input signal allows the user to single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one ($\emptyset_1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\emptyset_2$) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If Ready is low during a write cycle, it is ignored until the following read operation.

Interrupt Request ($\overline{IRQ}$)

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ register to Vcc for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during $\emptyset_2$ (phase 2) and will begin the appropriate interrupt routine on the $\emptyset_1$ (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)

A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $\emptyset_1$.

SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\emptyset_1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\emptyset_1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

SY6500 Signal Description

INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive-or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Pointer
TYA	Transfer Index Y to Accumulator

ADDRESSING MODES

ACCUMULATOR ADDRESSING - This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING - In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING - In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING - The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING - (X, Y indexing) - This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING - (X, Y indexing) - This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING - In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING - Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

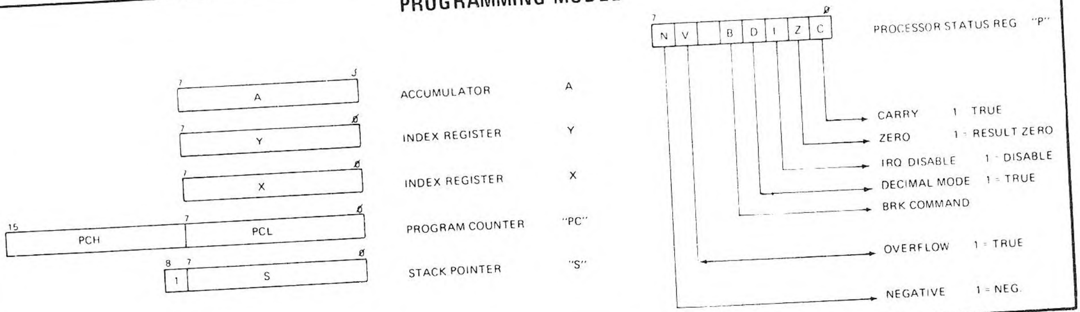
INDEXED INDIRECT ADDRESSING - In indexed indirect addressing (referred to as (Indirect,X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING - In indirect indexed addressing (referred to as (Indirect),Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT - The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

COMMON CHARACTERISTICS

PROGRAMMING MODEL



INSTRUCTION SET – OP CODES, Execution Time, Memory Requirements

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND,X)			(IND),Y			Z,PAGE,X			ABS,X			ABS,Y			RELATIVE			INDIRECT			Z,PAGE,Y			CONDITION CODES					
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
ADC	A+M+C→A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										√	√	√	—	—	√
AND	A∧M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										√	√	—	—	—	—
ASL	C←[7…0]←Ø				ØE	6	3	Ø6	5	2	ØA	2	1										16	6	2	1E	7	3													√	√	√	—	—	—
BCC	BRANCH ON C=Ø (2)																															9Ø	2	2							—	—	—	—	—	—
BCS	BRANCH ON C=1 (2)																															BØ	2	2							—	—	—	—	—	—
BEQ	BRANCH ON Z=1 (2)																															FØ	2	2							—	—	—	—	—	—
BIT	A∧M				2C	4	3	24	3	2																															M_7	√	—	—	—	M_6
BMI	BRANCH ON N=1 (2)																															3Ø	2	2							—	—	—	—	—	—
BNE	BRANCH ON Z=Ø (2)																															DØ	2	2							—	—	—	—	—	—
BPL	BRANCH ON N=Ø (2)																															1Ø	2	2							—	—	—	—	—	—
BRK	(See Fig. 1)													ØØ	7	1																									—	—	—	1	—	—
BVC	BRANCH ON V=Ø (2)																															5Ø	2	2							—	—	—	—	—	—
BVS	BRANCH ON V=1 (2)																															7Ø	2	2							—	—	—	—	—	—
CLC	Ø→C													18	2	1																									—	—	Ø	—	—	—
CLD	Ø→D													D8	2	1																									—	—	—	—	Ø	—
CLI	Ø→I													58	2	1																									—	—	—	Ø	—	—
CLV	Ø→V													B8	2	1																									—	—	—	—	—	Ø
CMP	A−M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										√	√	√	—	—	—
CPX	X−M	EØ	2	2	EC	4	3	E4	3	2																															√	√	√	—	—	—
CPY	Y−M	CØ	2	2	CC	4	3	C4	3	2																															√	√	√	—	—	—
DEC	M−1→M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													√	√	—	—	—	—
DEX	X−1→X													CA	2	1																									√	√	—	—	—	—
DEY	Y−1→Y													88	2	1																									√	√	—	—	—	—
EOR	A⊻M→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										√	√	—	—	—	—
INC	M+1→M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													√	√	—	—	—	—
INX	X+1→X													E8	2	1																									√	√	—	—	—	—
INY	Y+1→Y													C8	2	1																									√	√	—	—	—	—
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				—	—	—	—	—	—
JSR	(See Fig. 2) JUMP SUB				2Ø	6	3																																		—	—	—	—	—	—
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										√	√	—	—	—	—

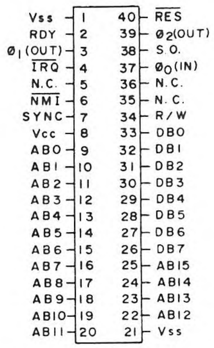
INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND,X)			(IND),Y			Z,PAGE,X			ABS,X			ABS,Y			RELATIVE			INDIRECT			Z,PAGE,Y			CONDITION CODES					
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	√	√	—	—	—	—
LDY	M→Y (1)	AØ	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													√	√	—	—	—	—
LSR	Ø→[7…0]→C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													Ø	√	√	—	—	—
NOP	NO OPERATION													EA	2	1																									—	—	—	—	—	—
ORA	A∨M→A	Ø9	2	2	ØD	4	3	Ø5	3	2							Ø1	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										√	√	—	—	—	—
PHA	A→Ms S−1→S													48	3	1																									—	—	—	—	—	—
PHP	P→Ms S−1→S													Ø8	3	1																									—	—	—	—	—	—
PLA	S+1→S Ms→A													68	4	1																									√	√	—	—	—	—
PLP	S+1→S Ms→P													28	4	1																									(RESTORED)					
ROL	←[7…0]←C←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													√	√	√	—	—	—
ROR	→C→[7…0]→				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													√	√	√	—	—	—
RTI	(See Fig. 1) RTRN INT													4Ø	6	1																									(RESTORED)					
RTS	(See Fig. 2) RTRN SUB													6Ø	6	1																									—	—	—	—	—	—
SBC	A−M−C̄→A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										√	√	(3)	—	—	√
SEC	1→C													38	2	1																									—	—	1	—	—	—
SED	1→D													F8	2	1																									—	—	—	—	1	—
SEI	1→I													78	2	1																									—	—	—	1	—	—
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										—	—	—	—	—	—
STX	X→M				8E	4	3	86	3	2																												96	4	2	—	—	—	—	—	—
STY	Y→M				8C	4	3	84	3	2													94	4	2																—	—	—	—	—	—
TAX	A→X													AA	2	1																									√	√	—	—	—	—
TAY	A→Y													A8	2	1																									√	√	—	—	—	—
TSX	S→X													BA	2	1																									√	√	—	—	—	—
TXA	X→A													8A	2	1																									√	√	—	—	—	—
TXS	X→S													9A	2	1																									—	—	—	—	—	—
TYA	Y→A													98	2	1																									√	√	—	—	—	—

(1) ADD 1 TO "N" IF PAGE BOUNDRY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER
+ ADD
− SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
√ MODIFIED
— NOT MODIFIED
M_7 MEMORY BIT 7
M_6 MEMORY BIT 6
N NO. CYCLES
NO. BYTES

MICRO-PROCESSORS

SY6502 – 40 Pin Package

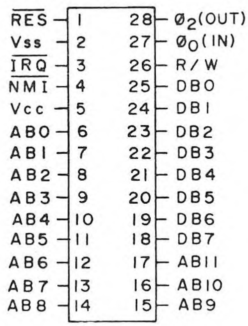


SY6502

* 65K Addressable Bytes of Memory
* $\overline{\text{IRQ}}$ Interrupt
* $\overline{\text{NMI}}$ Interrupt
* On-the-chip Clock
  - ✓ TTL Level Single Phase Input
  - ✓ RC Time Base Input
  - ✓ Crystal Time Base Input
* SYNC Signal (can be used for single instruction execution)
* RDY Signal (can be used for single cycle execution)
* Two Phase Output Clock for Timing of Support Chips

Features of SY6502

SY6503 – 28 Pin Package

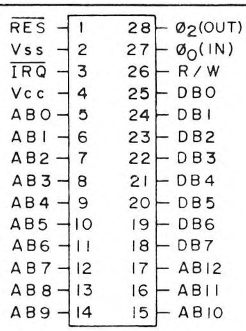


SY6503

* 4K Addressable Bytes of Memory (AB00-AB11)
* On-the-chip Clock
* $\overline{\text{IRQ}}$ Interrupt
* $\overline{\text{NMI}}$ Interrupt
* 8 Bit Bi-Directional Data Bus

Features of SY6503

SY6504 – 28 Pin Package



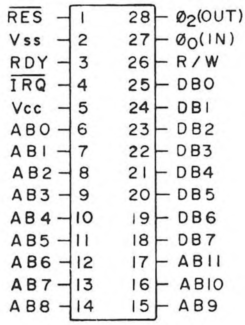
SY6504

* 8K Addressable Bytes of Memory (AB00-AB12)
* On-the-chip Clock
* $\overline{\text{IRQ}}$ Interrupt
* 8 Bit Bi-Directional Data Bus

Features of SY6504

MICRO-PROCESSORS

SY6505 – 28 Pin Package

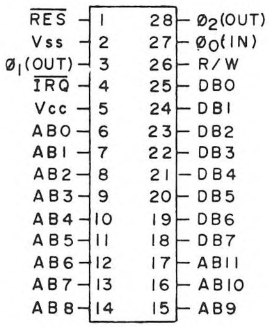


SY6505

* 4K Addressable Bytes of Memory (AB00-AB11)
* On-the-chip Clock
* $\overline{IRQ}$ Interrupt
* RDY Signal
* 8 Bit Bi-Directional Data Bus

Features of SY6505

SY6506 – 28 Pin Package



SY6506

* 4K Addressable Bytes of Memory (AB00-AB11)
* On-the-chip Clock
* $\overline{IRQ}$ Interrupt
* Two phases off
* 8 Bit Bi-Directional Data Bus

Features of SY6506

SY6512 – 40 Pin Package

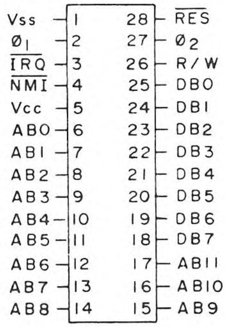
SY6512

* 65K Addressable Bytes of Memory
* $\overline{IRQ}$ Interrupt
* $\overline{NMI}$ Interrupt
* RDY Signal
* 8 Bit Bi-Directional Data Bus
* SYNC Signal
* Two phase input
* Data Bus Enable

Features of SY6512

MICRO-PROCESSORS

SY6513 – 28 Pin Package

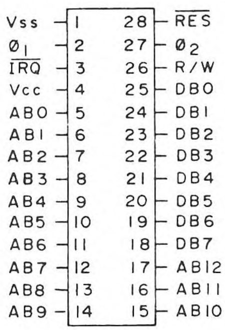


SY6513

* 4K Addressable Bytes of Memory (AB00-AB11)
* Two phase clock input
* $\overline{IRQ}$ Interrupt
* $\overline{NMI}$ Interrupt
* 8 Bit Bi-Directional Data Bus

Features of SY6513

SY6514 – 28 Pin Package

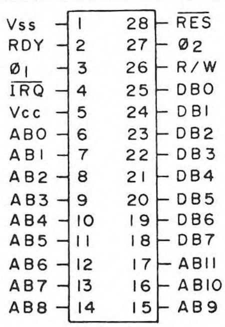


SY6514

* 8K Addressable Bytes of Memory (AB00-AB12)
* Two phase clock input
* $\overline{IRQ}$ Interrupt
* 8 Bit Bi-Directional Data Bus

Features of SY6514

SY6515 – 28 Pin Package



SY6515

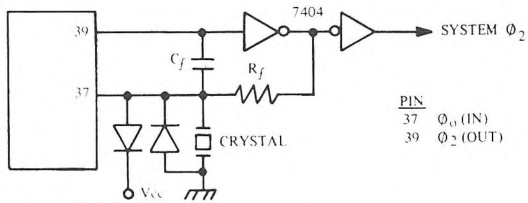
* 4K Addressable Bytes of Memory (AB00-AB11)
* Two phase clock input
* $\overline{IRQ}$ Interrupt
* 8 Bit Bi-Directional Data Bus

Features of SY6515

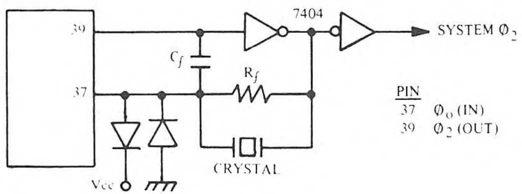
MICRO-PROCESSORS

TIME BASE GENERATION OF INPUT CLOCK

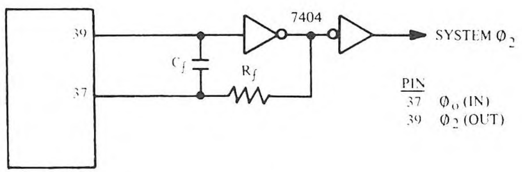
SY6502



SY6502 Parallel Mode Crystal Controlled Oscillator

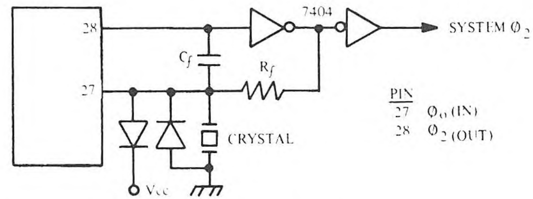


SY6502 Series Mode Crystal Controlled Oscillator

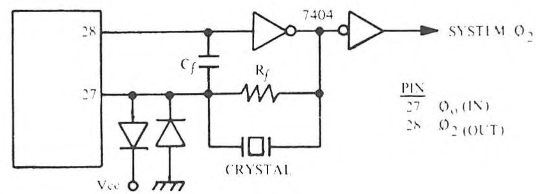


SY6502 Time Base Generator – RC Network

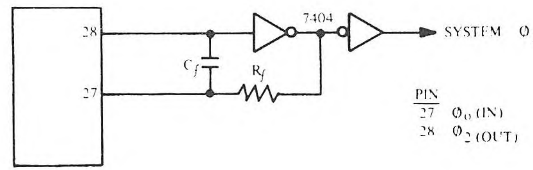
SY6503, SY6504, SY6505, SY6506



SY6503,4,5,6 Parallel Mode Crystal Controlled Oscillator



SY6503,4,5,6 Series Mode Crystal Controlled Oscillator



SY6503,4,5,6 Time Base Generation RC Network

Synertek®

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(408) 984-8900 TWX 910-338-0135

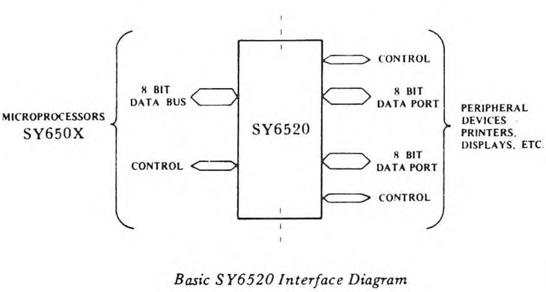
SY6520 PERIPHERAL ADAPTER

DESCRIPTION

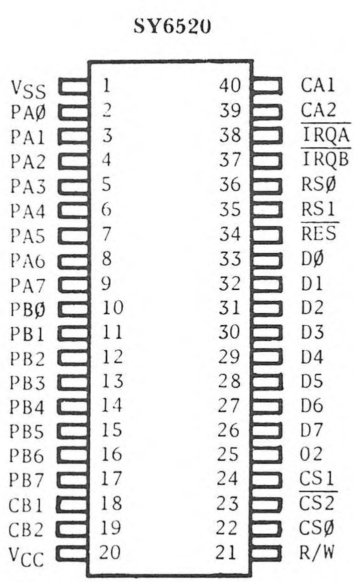
The SY6520 Peripheral Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the SY6500 family of microprocessors, the SY6520 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.

- High performance replacement for Motorola/AMI/MOSTEK/Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows very positive control of data transfers between processor and peripheral devices.



Basic SY6520 Interface Diagram



MICRO-PROCESSORS

SUMMARY OF SY6520 OPERATION

See SYNERTEK Microcomputer Hardware Manual for detailed description of SY6520 operation.

CA1/CBI CONTROL

CRA (CRB) Bit 1	CRA (CRB) Bit 0	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
0	0	negative	Disable--remain high
0	1	negative	Enable--goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	positive	Disable--remain high
1	1	positive	Enable--as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB) Bit 5	CRA (CRB) Bit 4	CRA (CRB) Bit 3	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Output
0	0	0	negative	Disable--remains high
0	0	1	negative	Enable--goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	positive	Disable--remains high
0	1	1	positive	Enable--as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

CRA Bit 5	CRA Bit 4	CRA Bit 3	Mode	Description
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB Bit 5	CRB Bit 4	CRB Bit 3	Mode	Description
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

STATIC D.C. CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	-	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	-	+.8	Vdc
Input Threshold Voltage	V_{IT}	0.8	-	2.0	Vdc
Input Leakage Current	I_{IN}				μAdc
V_{in} = 0 to 5.0 Vdc R/W, $\overline{Reset}$, RSØ, RS1, CSØ, CS1, $\overline{CS2}$, CA1, CB1, Φ2		-	±1.0	±2.5	
Three-State (Off State Input Current)	I_{TSI}				
(V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) DØ-D7, PBØ-PB7, CB2		-	±2.0	±10	μAdc
Input High Current	I_{IH}				
(V_{IH} = 2.4 Vdc) PAØ-PA7, CA2		-100	-250	-	μAdc
Input Low Current	I_{IL}				
(V_{IL} = 0.4 Vdc) PAØ-PA7, CA2		-	-1.0	-1.6	mAdc
Output High Voltage	V_{OH}				
(V_{CC} = min, I_{Load} = -100 μAdc)		2.4	-	-	Vdc
Output Low Voltage	V_{OL}				
(V_{CC} = min, I_{Load} = 1.6 mAdc)		-	-	+0.4	Vdc
Output High Current (Sourcing)	I_{OH}				
(V_{OH} = 2.4 Vdc)		-100	-1000	-	μAdc
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base) PBØ-PB7, CB2		-1.0	-2.5	-	mAdc
Output Low Current (Sinking)	I_{OL}				
(V_{OL} = 0.4 Vdc)		1.6	-	-	mAdc
Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$	I_{off}	-	1.0	10	uAdc
Power Dissipation	P_D	-	200	500	mW
Input Capacitance	C_{in}				pF
(V_{in} - 0, T_A = 25°C, f = 1.0 MHz) DØ-D7, PAØ-PA7, PBØ-PB7, CA2, CB2		-	-	10	
R/W, $\overline{Reset}$, RSØ, RS1, CSØ, CS1, CS2,		-	-	7.0	
CA1, CB1, Φ2		-	-	20	
Output Capacitance	C_{out}				
(V_{in} - 0, T_A = 25°C, f = 1.0 MHz)		-	-	10	pF

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

MICRO-PROCESSORS

FIGURE 1 – READ TIMING CHARACTERISTICS

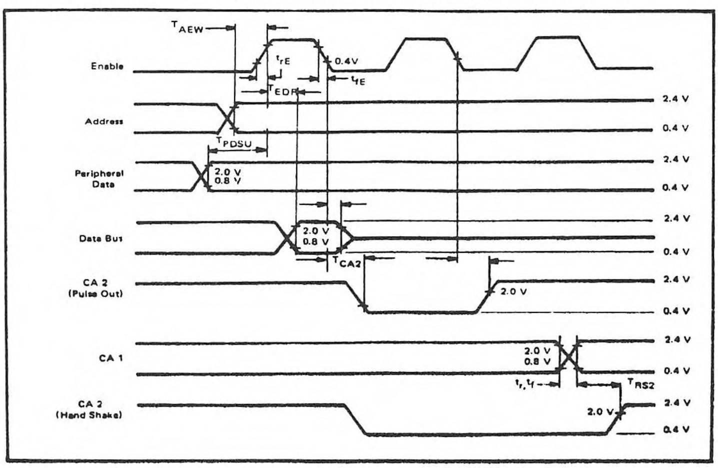
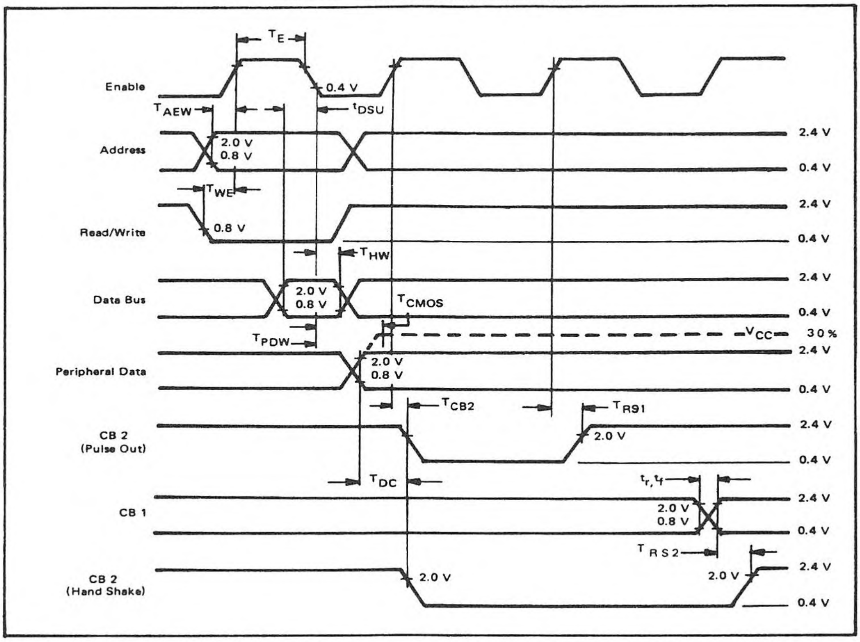


FIGURE 2 – WRITE TIMING CHARACTERISTICS



A.C. CHARACTERISTICS

Read Timing Characteristics (Figure 1, Loading 130 pF and one TTL load)

Characteristics	Symbol	Min	Typ	Max	Unit
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	-	-	ns
Delay Time, Enable positive transition to Data valid on bus	T_{EDR}	-	-	395	ns
Peripheral Data Setup Time	T_{PDSU}	300	-	-	ns
Data Bus Hold Time	T_{HR}	10	-	-	ns
Delay Time, Enable negative transition to CA2 negative transition	T_{CA2}	-	-	1.0	us
Delay Time, Enable negative transition to CA2 positive transition	T_{RS1}	-	-	1.0	us
Rise and Fall Time for CA1 and CA2 input signals	t_r, t_f	-	-	1.0	us
Delay Time from CA1 active transition to CA2 positive transition	T_{RS2}	-	-	2.0	us
Rise and Fall Time for Enable input	t_{rE}, t_{fE}	-	-	25	us

Write Timing Characteristics (Figure 2)

Characteristics	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T_E	0.470	-	25	μs
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	-	-	ns
Delay Time, Data valid to Enable negative transition	T_{DSU}	300	-	-	ns
Delay Time, Read/Write negative transition to Enable positive transition	T_{WE}	130	-	-	ns
Data Bus Hold Time	T_{HW}	10	-	-	ns
Delay Time, Enable negative transition to Peripheral Data valid	T_{PDW}	-	-	1.0	μs
Delay Time, Enable negative transition to Peripheral Data Valid, CMOS (V_{CC} - 30%) PAØ-PA7, CA2	T_{CMOS}	-	-	2.0	μs
Delay Time, Enable positive transition to CB2 negative transition	T_{CB2}	-	-	1.0	μs
Delay Time, Peripheral Data valid to CB2 negative transition	T_{DC}	0	-	1.5	μs
Delay Time, Enable positive transition to CB2 positive transition	T_{RS1}	-	-	1.0	μs
Rise and Fall Time for CB1 and CB2 input signals	t_r, t_f	-	-	1.0	μs
Delay Time, CB1 active transition to CB2 positive transition	T_{RS2}	-	-	2.0	μs

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SY6522

SY6522 (VERSATILE INTERFACE ADAPTER)

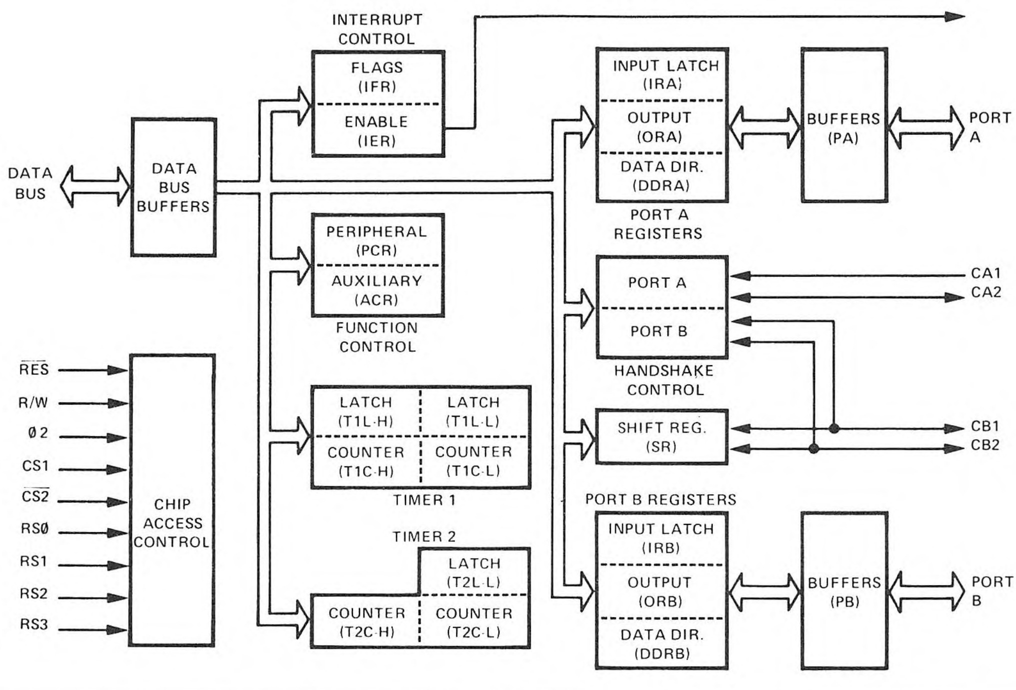
The SY6522 Versatile Interface Adapter (VIA) provides all of the capability of the SY6520. In addition, this device contains a pair of very powerful interval timers, a serial-to-parallel/parallel-to-serial shift register and input data latching on the peripheral ports. Expanded handshaking capability allows control of bi-directional data transfers between VIA's in multiple processor systems.

Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. Also, several peripheral I/O lines can be controlled directly from the interval timers for generating programmable frequency square waves and for counting externally generated pulses. To facilitate control of the many powerful features of this chip, the internal registers have been organized into an interrupt flag register, an interrupt enable register and a pair of function control registers.

- Very powerful expansion of basic SY6520 capability.
- N channel, depletion load technology, single +5V Supply.
- Completely static and TTL compatible.
- CMOS compatible peripheral control lines.
- Expanded "handshake" capability allows very positive control of data transfers between processor and peripheral devices.

MICRO-PROCESSORS

Figure 1. SY6522 BLOCK DIAGRAM



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MAXIMUM RATINGS

	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to +7.0	Vdc
Input Voltage	Vin	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

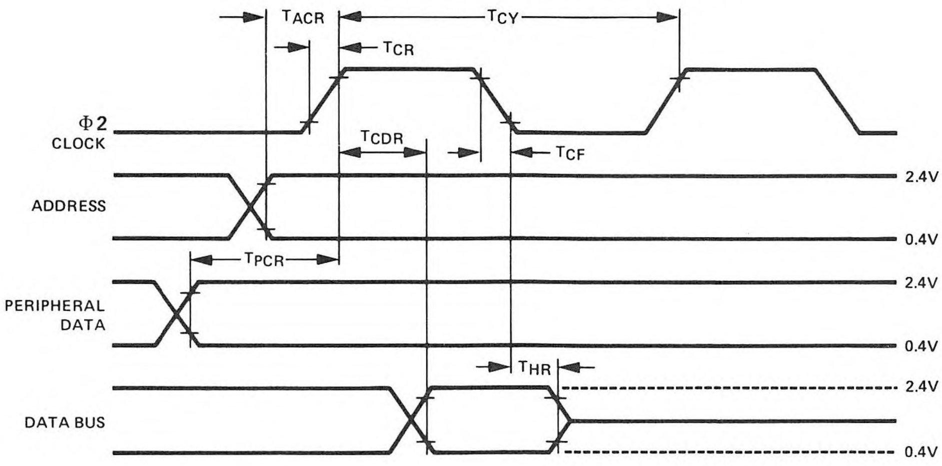
This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

Electrical Characteristics (V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input high voltage (normal operation)	V_{IH}	+2.4	–	Vcc	Vdc
Input Low Voltage (normal operation)	V_{IL}	-0.3	–	+0.4	Vdc
Input Leakage current - V_{IN} = 0 to 5 Vdc R/W, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$, CA1, Φ2	I_{IN}	–	±1.0	±2.5	μAdc
Off-state input current - V_{IN} = .4 to 2.4 V Vcc = Max, D0 to D7	I_{TSI}	–	±2.0	±10	μAdc
Input high current - V_{IH} = 2.4 V PA0 - PA7, CA2, PB0 - PB7, CB1, CB2	I_{IH}	-100	-250	–	μAdc
Input low current - V_{IL} = 0.4 Vdc PA0 - PA7, CA2, PB0 - PB7, CB1, CB2	I_{IL}	–	-1.0	-1.6	mAdc
Output high voltage Vcc = min, I_{load} = -100 μAdc PA0 - PA7, CA2, PB0 -PB7, CB1, CB2	V_{OH}	2.4	–	–	Vdc
Output low voltage Vcc = min, I_{load} = 1.6 mAdc	V_{OL}	–	–	+0.4	Vdc
Output high current (sourcing)	I_{OH}				
V_{OH} = 2.4 V		-100	-1000	–	μAdc
V_{OH} = 1.5 V, PB0 - PB7, CB1, CB2		-3.0	-5.0	–	mAdc
Output low current (sinking) V_{OL} = 0.4 Vdc	I_{OL}	1.6	–	–	mAdc
Output leakage current (off state) $\overline{IRQ}$	I_{off}	–	1.0	10	μAdc
Input capacitance - T_A = 25°C, f = 1 Mhz	C_{in}				
R/W, $\overline{RES}$, RS0, RS1, RS2, RS3, CS1, $\overline{CS2}$		–	–	7.0	pF
DO - D7, PA0 - PA7, CA1, CA2, PB0 - PB7, CB1, CB2		–	–	10	pF
Φ2 input		–	–	20	pF
Output capacitance - T_A = 25°C, f = 1 Mhz	C_{out}	–	–	10	pF
Power dissipation	P_d	–	–	1000	MW

MICRO-PROCESSORS

Figure 2. READ TIMING CHARACTERISTICS



DYNAMIC CHARACTERISTICS

Read Timing Characteristics (Figure 2, loading 130 pF and one TTL load)

Characteristic	Symbol	Min	Typ	Max	Unit
Cycle time	T_{CY}	1	–	50	μs
Delay time, address valid to clock positive transition	T_{ACR}	180	–	–	nS
Delay time, clock positive transition to data valid on bus	T_{CDR}	–	–	395	nS
Peripheral data setup time	T_{PCR}	300	–	–	nS
Data bus hold time	T_{HR}	10	–	–	nS
Rise and fall time for clock input	T_{CR} T_{CF}	–	–	25	nS

Write Timing Characteristics (Figure 3)

Characteristic	Symbol	Min	Typ	Max	Unit
Cycle Time	T_{CY}	1	–	50	μS
Enable pulse width	T_C	0.47	–	25	μS
Delay time, address valid to clock positive transition	T_{ACW}	180	–	–	nS
Delay time, data valid to clock negative transition	T_{DCW}	300	–	–	nS
Delay time, read/write negative transition to clock positive transition	T_{WCW}	180	–	–	nS
Data bus hold time	T_{HW}	10	–	–	nS
Delay time, Enable negative transition to peripheral data valid	T_{CPW}	–	–	1.0	μS
Delay time, clock negative transition to peripheral data valid CMOS (Vcc - 30%)	T_{CMOS}	–	–	2.0	μS

Figure 3. WRITE TIMING CHARACTERISTICS

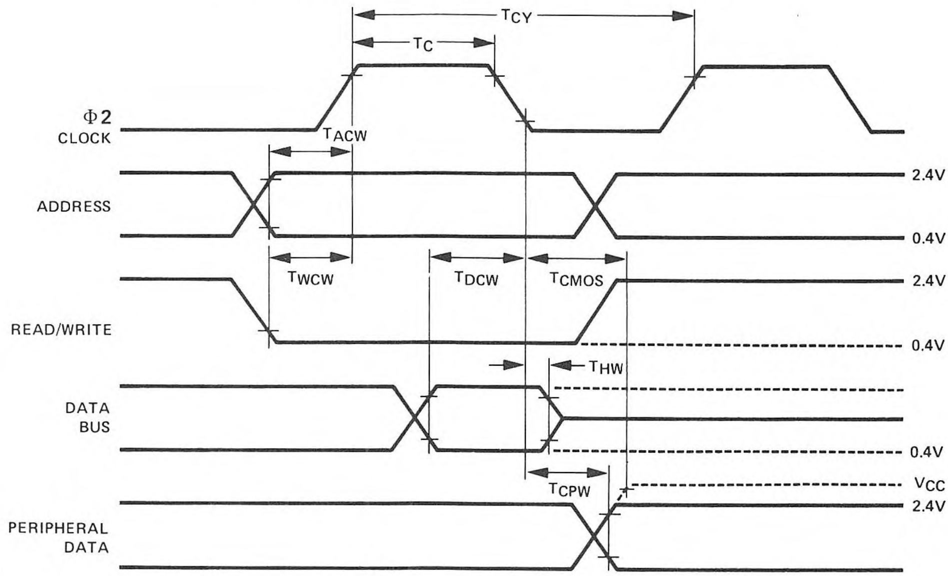
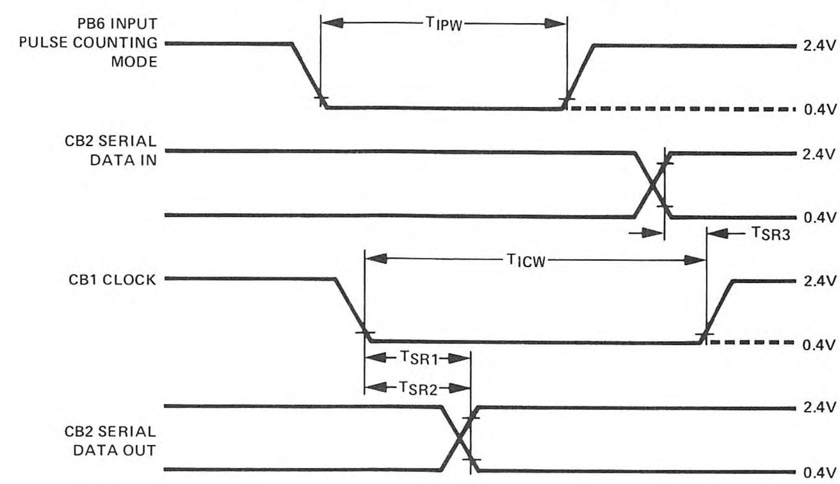


Figure 4. I/O TIMING CHARACTERISTICS



MICRO-PROCESSORS

PERIPHERAL INTERFACE CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Rise and fall time for CA1, CB1, CA2, and CB2 input signals.	T_{RF}	–	–	1.0	μS
Delay time, clock negative transition to CA2 negative transition (read handshake or pulse mode).	T_{CA2}	–	–	1.0	μS
Delay time, clock negative transition to CA2 positive transition (pulse mode).	T_{RS1}	–	–	1.0	μS
Delay time, CA1 active transition to CA2 positive transition (handshake mode).	T_{RS2}	–	–	2.0	μS
Delay time, clock positive transition to CA2 or CB2 negative transition (write handshake).	T_{WHS}	–	–	1.0	μS
Delay time, peripheral data valid to CB2 negative transition.	T_{DC}	0	–	1.5	μS
Delay time, clock positive transition to CA2 or CB2 positive transition (pulse mode).	T_{RS3}	–	–	1.0	μS
Delay time, CB1 active transition to CA2 or CB2 positive transition (handshake mode).	T_{RS4}	–	–	2.0	μS
Delay time, peripheral data valid to CA1 or CB1 active transition (input latching).	T_{IL}	300	–	–	nS
Delay time, CB1 negative transition to CB2 data valid (internal SR clock, shift out).	T_{SR1}	–	–	300	nS
Delay time, negative transition of CB1 input clock to CB2 data valid (external clock, shift out).	T_{SR2}	–	–	300	nS
Delay time, CB2 data valid to positive transition of CB1 clock (shift in, internal or external clock)	T_{SR3}	–	–	300	nS
Pulse Width - PB6 Input Pulse	T_{IPW}	2	–	–	μS
Pulse Width - CB1 Input Clock	T_{ICW}	2	–	–	μS
Pulse Spacing - PB6 Input Pulse	I_{IPS}	2	–	–	μS
Pulse Spacing - CB1 Input Pulse	I_{ICS}	2	–	–	μS

PROCESSOR INTERFACE

This section contains a description of the buses and control lines which are used to interface the SY6522 to the system processor. Electrical parameters associated with this interface are specified elsewhere in this document.

1. Phase Two Clock (Φ2)

Data transfers between the SY6522 and the system processor take place only while the Phase Two Clock is high. In addition, Φ2 acts as the time base for the various timers, shift registers, etc. on the chip.

2. Chip Select Lines (CS1, $\overline{CS2}$)

The two chip select inputs are normally connected to processor address lines either directly or through decoding. The selected SY6522 register will be accessed when CS1 is high and $\overline{CS2}$ is low.

3. Register Select Lines (RS0, RS1, RS2, RS3)

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal SY6522 register which is to be accessed. The sixteen possible combinations access the registers as follows:

RS3	RS2	RS1	RS0	REGISTER	REMARKS
L	L	L	L	ORB, IRB	
L	L	L	H	ORA, IRA	Controls Handshake
L	L	H	L	DDRB	
L	L	H	H	DDRA	
L	H	L	L	T1L-L	Write Latch Read Counter
L	H	L	H	T1C-H	Trigger T1L-L/ T1C-L Transfer
L	H	H	L	T1L-L	
L	H	H	H	T1L-H	
H	L	L	L	T2L-L T2C-L	Write Latch Read Counter
H	L	L	H	T2C-H	Triggers T2L-L/ T2C-L Transfer
H	L	H	L	SR	
H	L	H	H	ACR	
H	H	L	L	PCR	
H	H	L	H	IFR	
H	H	H	L	IER	
H	H	H	H	ORA	No Effect on Handshake

NOTE: $L \leqslant 0.4V$
$H \geqslant 2.4V$

4. Read/Write Line (R/W)

The direction of the data transfers between the SY6522 and the system processor is controlled by the R/W line. If R/W is low, data will be transferred out of the processor into the selected SY6522 register (write operation). If R/W is high and the chip is selected, data will be transferred out of the SY6522 (read operation).

5. Data Bus (DB0 - DB7)

The 8 bi-directional data bus lines are used to transfer data between the SY6522 and the system processor. The internal drivers will remain in the high-impedance state except when the chip is selected (CS1=HI, $\overline{CS2}$=LO), Read/Write is high and the Phase Two Clock is high. At this time, the contents of the selected register are placed on the data bus. When the chip is selected, with Read/Write low and Φ2 = 1, the data on the data bus will be transferred into the selected SY6522 register.

6. **Reset ($\overline{RES}$)**

The reset input clears all internal registers to logic 0 (except T1, T2 and SR). This places all peripheral interface lines in the input state, disables the timers, shift register, etc. and disables interrupting from the chip.

7. **Interrupt Request ($\overline{IRQ}$)**

The Interrupt Request output goes low whenever an internal interrupt flag is set and the corresponding interrupt enable bit is a logic 1. This output is "open-drain" to allow the interrupt request signal to be "wire-or'ed" with other equivalent signals in the system.

PERIPHERAL INTERFACE

This section contains a brief description of the buses and control lines which are used to drive peripheral devices under control of the internal SY6522 registers.

1. **Peripheral A Port (PA0 - PA7)**

The Peripheral A port consists of 8 lines which can be individually programmed to act as an input or an output under control of a Data Direction Register. The polarity of output pins is controlled by an Output Register and input data can be latched into an internal register under control of the CA1 line. All of these modes of operation are controlled by the system processor through the internal control registers. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode.

2. **Peripheral A Control Lines (CA1, CA2)**

The two peripheral A control lines act as interrupt inputs or as handshake outputs. Each line controls an internal interrupt flag with a corresponding interrupt enable bit. In addition, CA1 controls the latching of data on Peripheral A Port Input lines. The various modes of operation are controlled by the system processor through the internal control registers. CA1 is a high-impedance input only while CA2 represents one standard TTL load in the input mode. CA2 will drive one standard TTL load in the output mode.

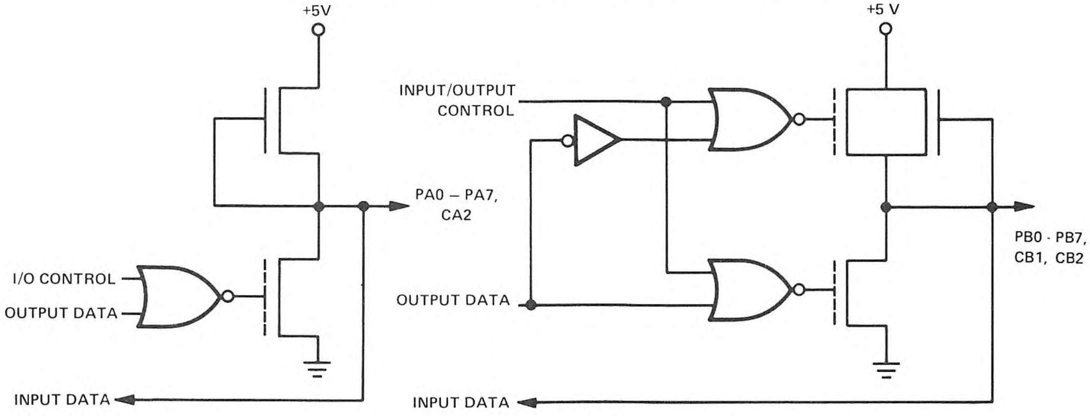
3. **Peripheral B Port (PB0 - PB7)**

The Peripheral B Port consists of 8 bi-directional lines which are controlled by an output register and a data direction register in much the same manner as the PA port. In addition, the polarity of the PB7 output signal can be controlled by one of the interval timers while the second timer can be programmed to count pulses on the PB6 pin. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 3.0 ma at 1.5 VDC in the output mode to allow the outputs to directly drive Darlington transistor switches.

4. **Peripheral B Control Lines (CB1, CB2)**

The Peripheral B control lines act as interrupt inputs or as handshake outputs. As with CA1 and CA2, each line controls an interrupt flag with a corresponding interrupt enable bit. In addition, these lines act as a serial port under control of the Shift Register. These lines represent one standard TTL load in the input mode and will drive one standard TTL load in the output mode. In addition, they are capable of sourcing 3.0 ma at 1.5 VDC in the output mode to allow the outputs to directly drive Darlington transistor switches.

Figure 5. PERIPHERAL DATA OUTPUT BUFFERS



MICRO-
PROCESSORS

SY6522 OPERATION

This section contains a discussion of the various blocks of logic shown in Figure 1. In addition, the internal operation of the SY6522 is described in detail.

A. Data Bus Buffers (DB), Peripheral A Buffers (PA), Peripheral B Buffers (PB)

The characteristics of the buffers which provide the required voltage and current drive capability were discussed in the previous section. Electrical paramenters for these buffers are specified elsewhere in this document.

B. Chip Access Control

The Chip Access Control contains the necessary logic to detect the chip select condition and to decode the Register Select inputs to allow accessing the desired internal registers. In addition, the R/W and $\Phi 2$ signals are utilized to control the direction and timing of data transfers. When writing into the SY6522, data is first latched into a data input register during $\Phi 2$. Data is then transferred into the desired internal register during $\Phi 2 \cdot$ Chip Select. This allows the peripheral I/O lines to change states cleanly. When the processor reads the SY6522, data is transferred from the desired internal register directly onto the Data Bus during $\Phi 2$.

C. Port A Registers, Port B Registers

Three registers are used in accessing each of the 8-bit peripheral ports. Each port has a Data Direction Register (DDRA, DDRB) for specifying whether the peripheral pins are to act as inputs or outputs. A 0 in a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A 1 causes the pin to act as an output.

Each peripheral pin is also controlled by a bit in the Output Register (ORA, ORB) and an Input Register (IRA, IRB). When the pin is programmed to act as an output, the voltage on the pin is controlled by the corresponding bit of the Output Register. A 1 in the Output Register causes the pin to go high, and a 0 causes the pin to go low. Data can be written into Output Register bits corresponding to pins which are programmed to act as inputs; however, the pin will be unaffected.

Reading a peripheral port causes the contents of the Input Register (IRA, IRB) to be transferrred onto the Data Bus. With input latching disabled, IRA will always reflect the data on the PA pins. With input latching enabled, IRA will reflect the contents of the Port A prior to setting the CA1 Interrupt Flag (IFR1) by an active transition on CA1.

The IRB register operates in a similar manner. However, for output pins, the corresponding IRB bit will reflect the contents of the Output Register bit instead of the actual pin. This allows proper data to be read into the processor if the output pin is not allowed to go to full voltage. With input latching enabled on Port B, setting CB1 interrupt flag will cause the IRB to latch this combination of input data and ORB data until the interrupt flag is cleared.

D. Handshake Control

The SY6522 allows very positive control of data transfers between the system processor and peripheral devices through the operation of "handshake" lines. Port A lines (CA1, CA2) handshake data on both a read and a write operation while the Port B lines (CB1, CB2) handshake on a write operation only.

Read Handshake

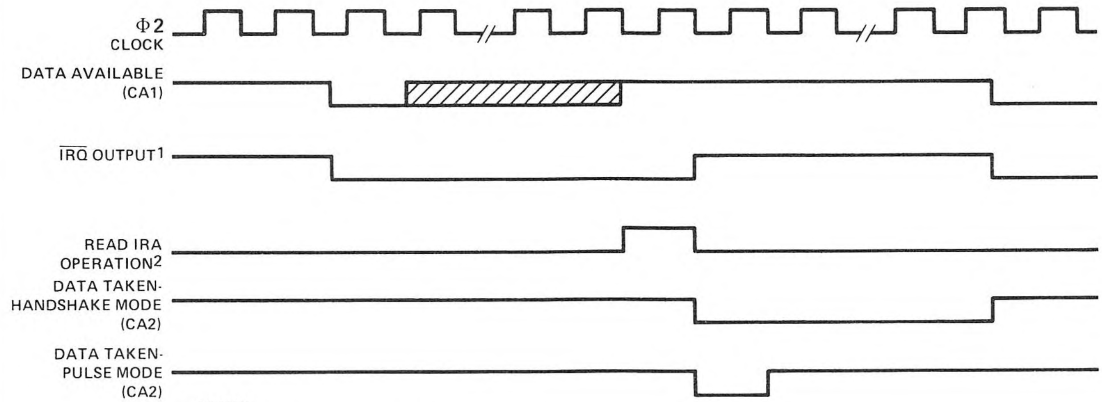
Positive control of data transfers from peripheral devices into the system processor can be accomplished very effectively using "Read" handshaking. In this case, the peripheral device must generate "Data Ready" to signal the processor that valid data is present on the peripheral port. This signal normally interrupts the processor, which then reads the data, causing generation of a "Data Taken" signal. The peripheral device responds by making new data available. This process continues until the data transfer is complete.

In the SY6522, automatic "Read" handshaking is possible on the Peripheral A port only. The CA1 interrupt input pin accepts the "Data Ready" signal and CA2 generates the "Data Taken" signal. The Data Ready signal will set an internal flag which may interrupt the processor or which can be polled under software control. The Data Taken signal can either be a pulse or a level which is set low by the system processor and is cleared by the Data Ready signal. These options are shown in Figure 6 which illustrates the normal Read Handshaking sequence.

Write Handshake

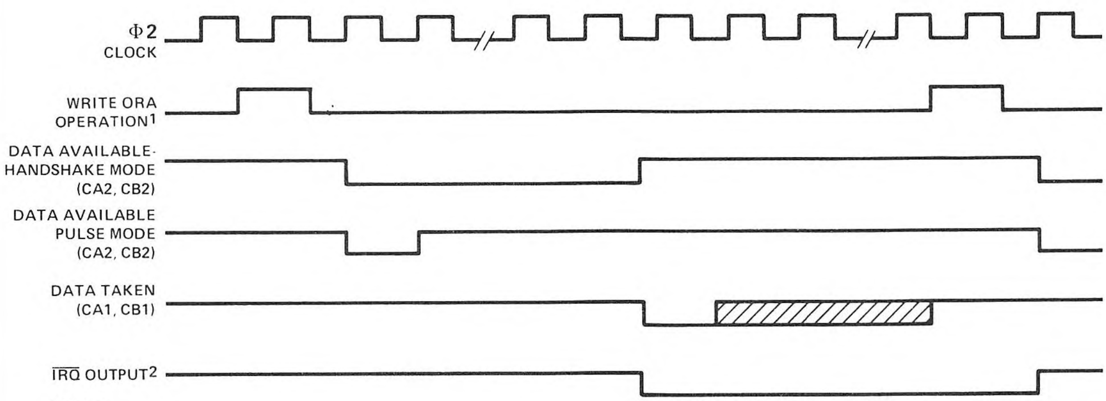
The sequence of operations which allows handshaking data from the system processor to a peripheral device is very similar to that described in Section A for Read Handshaking. However, for "Write" handshaking, the processor must generate the "Data Ready" signal (through the SY6522) and the peripheral device must respond with the "Data Taken" signal. This can be accomplished on both the PA port and the PB port on the SY6522. CA2 or CB2 acts as a Data Ready Output in either the DC level of pulse mode and CA1 or CB1 accepts the "Data Taken" signal from the peripheral device, setting the interrupt flag and clearing the "Data Ready" output. This sequence is shown in Figure 7.

Figure 6. READ HANDSHAKE TIMING SEQUENCE



NOTES:
1. Signals "data available" to the system processor.
2. R/W = 1, $\overline{CS2}$ = 0, CS1 = 1, RS2 = 0, RS3 = 0, RS0 = 1.

Figure 7. WRITE HANDSHAKE TIMING SEQUENCE



NOTES:
1. R/W = 0, $\overline{CS2}$ = 0, CS1 = 1, RS3 = 0, RS2 = 0, RS1 = 0, RS0 = 1.
2. Signals "data taken" to the system processor.

E. Timer 1

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches are used to store data which is to be loaded into the counter. After loading, the counter decrements at system clock rate, i.e., under control of the clock applied to the Phase Two input pin. Upon reaching zero, an interrupt flag will be set, and $\overline{IRQ}$ will go low. The timer will then disable any further interrupts, or will automatically transfer the contents of the latches into the counter and will continue to decrement. In addition, the timer can be instructed to invert the output signal on a peripheral pin each time it "times-out". Each of these modes is dicussed separately below.

Writing the Timer 1 Registers

The operations which take place when writing to each of the four T1 addresses are as follows:

RS3	RS2	RS1	RS0	Operation (R/W =L)
L	H	L	L	Write into low order latch.
				Write into high order latch.
L	H	L	H	Write into high order counter. Transfer low order latch into low order counter. Reset T1 interrupt flag.
L	H	H	L	Write into low order latch.
L	H	H	H	Write into high order latch. Reset T1 interrupt flag.

Note that the processor does not write directly into the low order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low order latch when the processor writes into the high order counter. In fact, it may not be necessary to write to the low order counter in some applications since the timing operation is triggered by writing to the high order counter.

The second set of addresses allows the processor to write into the latch register without affecting the count-down in progress. This is discussed in detail below.

Reading the Timer 1 Registers

For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows.

RS3	RS2	RS1	RS0	Operation (R/W = H)
L	H	L	L	Read T1 low order counter. Reset T1 interrupt flag.
L	H	L	H	Read T1 high order counter.
L	H	H	L	Read T1 low order latch.
L	H	H	H	Read T1 high order latch.

Timer 1 Operating Modes

Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are as follows:

ACR7 Output Enable	ACR6 "Free-Run" Enable	Mode
0	0	Generate a single time-out interrupt each time T1 is loaded. PB7 disabled.
0	1	Generate continuous interrupts. PB7 disabled.
1	0	Generate a single interrupt and an output pulse on PB7 for each T1 load operation.
1	1	Generate continuous interrupts and a square wave output on PB7.

TIMER 1 ONE-SHOT MODE

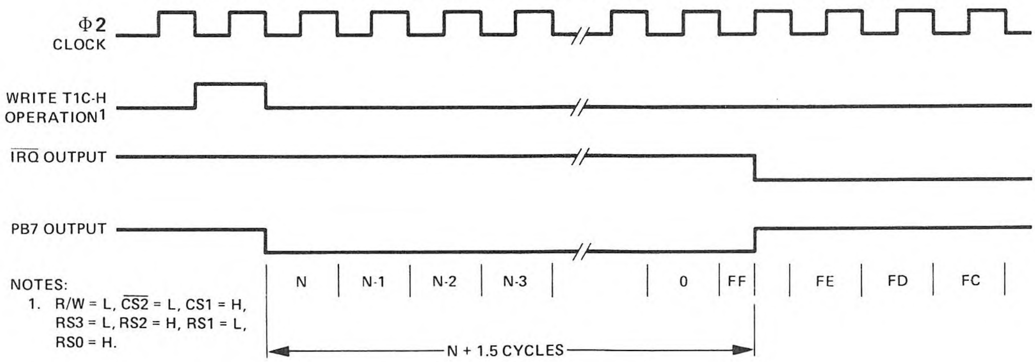
The interval timer one-shot mode allows generation of a single interrupt for each timer load operation. As with any interval timer, the delay between the "write T1C-H" operation and generation of the processor interrupt is a direct function of the data loaded into the timing counter. In addition to generating a single interrupt, Timer 1 can be programmed to produce a single negative pulse on the PB7 peripheral pin. With the output enabled (ACR7=1) a "write T1C-H" operation will cause PB7 to go low. PB7 will return high when Timer 1 times out. The result is a single programmable width pulse.

> **NOTE**
>
> PB7 will act as an output if DDRB7 = 1 or if ACR7 = 1. However, if both DDRB7 and ACR7 are logic 1, PB7 will be controlled from Timer 1 and ORB7 will have no effect on the pin.

In the one-shot mode, writing into the high order latch has no effect on the operation of Timer 1. However, it will be necessary to assure that the low order latch contains the proper data before initiating the count-down with a "write T1C-H" operation.When the processor writes into the high order counter, the T1 interrupt flag will be cleared, the contents of the low order latch will be transferred into the low order counter, and the timer will begin to decrement at system clock rate. If the PB7 output is enabled, this signal will go low on the phase two following the write operation. When the counter reaches zero, the T1 interrupt flag will be set, the $\overline{IRQ}$ pin will go low (interrupt enabled), and the signal on PB7 will go high. At this time the counter will continue to decrement at system clock rate. This allows the system processor to read the contents of the counter to determine the time since interrupt. However, the T1 interrupt flag cannot be set again unless it has been cleared as described elsewhere in this specification.

Timing for the SY6522 interval timer one-shot modes is shown in figure 8.

Figure 8. INTERVAL TIMER "ONE-SHOT" MODE TIMING SEQUENCE



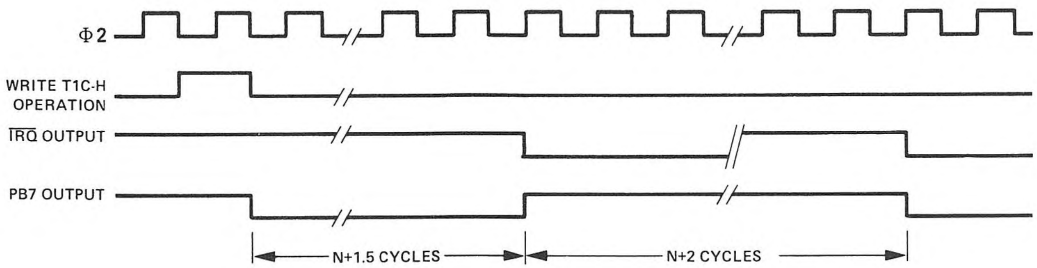
TIMER 1 FREE-RUNNING MODE

The most important advantage associated with the latches in T1 is the ability to produce a continuous series of evenly spaced interrupts and the ability to produce a square wave on PB7 whose frequency is not affected by variations in the processor interrupt response time. This is accomplished in the "free-running" mode.

In the free-running mode (ACR6 = 1), the interrupt flag is set and the signal on PB7 is inverted each time the counter reaches zero. However, instead of continuing to decrement from zero after a time-out, the timer automatically transfers the contents of the latch into the counter (16 bits) and continues to decrement from there. The interrupt flag can be cleared by writing T1C-H, by reading T1C-L, or by writing directly into the flag as described below. However, it is not necessary to rewrite the timer to enable setting the interrupt flag on the next time-out.

All interval timers in the SY6500 family devices are "re-triggerable". Rewriting the counter will always re-initialize the time-out period. In fact, the time-out can be prevented completely if the processor continues to rewrite the timer before it reaches zero. Timer 1 will operate in this manner if the processor writes into the high order counter (T1C-H). However, by loading the latches only, the processor can access the timer during each down-counting operation without affecting the time-out in process. Instead, the data loaded into the latches will determine the length of the next time-out period. This capability is particularly valuable in the free-running mode with the output enabled. In this mode, the signal on PB7 is inverted and the interrupt flag is set with each time-out. By responding to the interrupts with new data for the latches, the processor can determine the period of the next half cycle during each half cycle of the output signal on PB7. In this manner, very complex waveforms can be generated. Timing for the free-running mode is shown in Figure 9.

Figure 9. TIMER 1 "FREE-RUNNING" MODE



F. Timer 2

Timer 2 operates as an interval timer (in the "one-shot" mode only), or as a counter for counting negative pulses on the PB6 peripheral pin. A single control bit is provided in the Auxiliary Control Register to select between these two modes. This timer is comprised of a "write-only" low-order latch (T2L-L), a "read-only" low-order counter and a read/write high order counter. The counter registers act as a 16-bit counter which decrements at Φ2 rate.

Timer 2 addressing can be summarized as follows:

RS3	RS2	RS1	RS0	R/W = 0	R/W = 1
H	L	L	L	Write T2L-L	Read T2C-L Clear Interrupt flag
H	L	L	H	Write T2C-H Transfer T2L-L to T2C-L Clear Interrupt flag	Read T2C-H

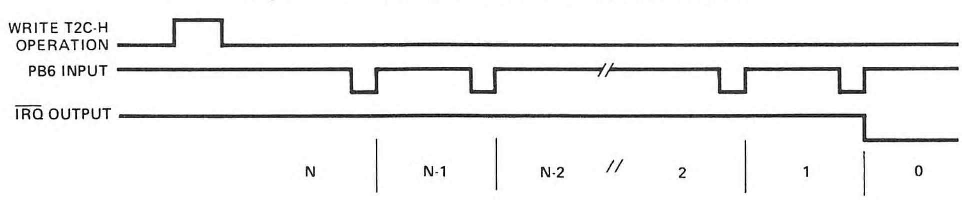
Timer 2 Interval Timer Mode

As an interval timer, T2 operates in the "one-shot" mode similar to Timer 1. In this mode, T2 provides a single interrupt for each "write T2C-H" operation. After timing out, the counter will continue to decrement. However, setting of the interrupt flag will be disabled after initial time-out so that it will not be set by the counter continuing to decrement through zero. The processor must rewrite T2C-H to enable setting of the interrupt flag. The interrupt flag is cleared by reading T2C-L or by writing T2C-H. Timing for this operation is shown in Figure 8.

Timer 2 Pulse Counting Mode

In the pulse counting mode, T2 serves primarily to count a predetermined number of negative-going pulses on PB6. This is accomplished by first loading a number into T2. Writing into T2C-H clears the interrupt flag and allows the counter to decrement each time a pulse is applied to PB6. The interrupt flag will be set when T2 reaches zero. At this time the counter will continue to decrement with each pulse on PB6. However, it is necessary to rewrite T2C-H to allow the interrupt flag to set on subsequent down-counting operations. Timing for this mode is shown in Figure 10. The pulse must be low on the leading edge of Φ2.

Figure 10. TIMER 2 PULSE COUNTING MODE



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G. Shift Register

The Shift Register (SR) performs serial data transfers into and out of the CB2 pin under control of an internal modulo-8 counter. Shift pulses can be applied to the CB1 pin from an external source or, with the proper mode selection, shift pulses generated internally will appear on the CB1 pin for controlling external devices.

The control bits which select the various shift register operating modes are located in the Auxiliary Control Register. These bits can be set and cleared by the system processor to select one of the operating modes discussed in the following paragraphs.

Shift Register Input Modes

Bit 4 of the Auxiliary Control Register selects the input or output modes. There are three input modes and four output modes, differing primarily in the source of the pulses which control the shifting operation. With ACR4 = 0 the input modes are selected by ACR3 and ACR2 as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register Disabled
0	0	1	Shift in under control of Timer 2
0	1	0	Shift in at System Clock Rate.
0	1	1	Shift in under control of external input pulses

Mode 000 - Shift Register Disabled

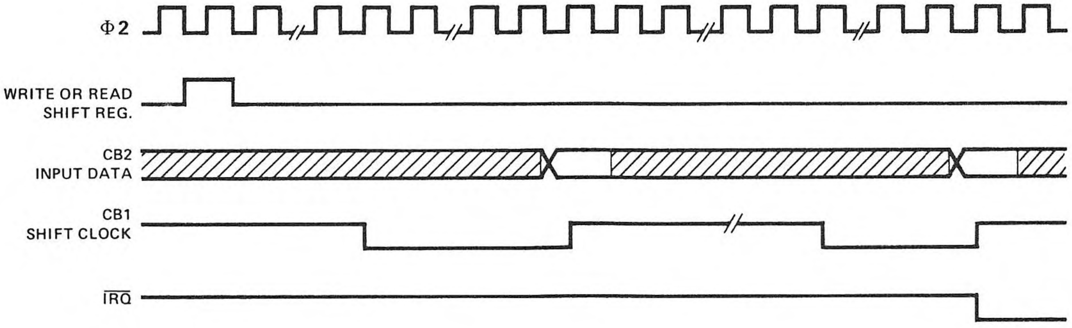
The 000 mode is used to disable the Shift Register. In this mode the microprocessor can write or read the SR, but the shifting operation is disabled and operation of CB1 and CB2 is controlled by the appropriate bits in the Peripheral Control Register (PCR). In this mode the SR Interrupt Flag is disabled (held to a logic 0).

Mode 001 - Shift in Under Control of Timer 2

In this mode the shifting rate is controlled by the low order 8 bits of T2. Shift pulses are generated on the CB1 pin to control shifting in external devices. The time between transitions of this output clock is a function of the system clock period and the contents of the low order T2 latch.

The shifting operation is triggered by writing or reading the shift register. Data is shifted first into the low order bit of SR and is then shifted into the next higher order bit or the shift register on the trailing edge of each clock pulse. As shown in Figure 11, the input data should change before the leading edge of the clock pulse. This data is loaded into the shift register during the system clock cycle following the trailing edge of the clock pulse. After 8 clock pulses, the shift register interrupt flag will be set and IRQ will go low.

Figure 11. SHIFTING IN UNDER CONTROL OF T2



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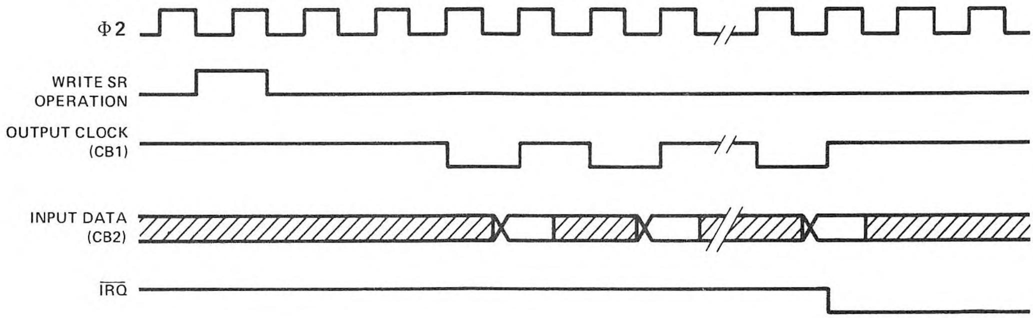
Mode 010 - Shift in at System Clock Rate

In this mode the shift rate is a direct function of the system clock frequency. CB1 becomes an output which generates shift pulses for controlling external devices. Timer 2 operates as an independent interval timer and has no effect on SR. The shifting operation is triggered by reading or writing the Shift Register. Data is shifted first into bit 0 and is then shifted into the next higher order bit of the shift register on the trailing edge of each clock pulse. After 8 clock pulses, the shift register interrupt flag will be set, and the output clock pulses on CB1 will stop.

Figure 12. TIMING SEQUENCE FOR SHIFTING IN AT SYSTEM CLOCK RATE

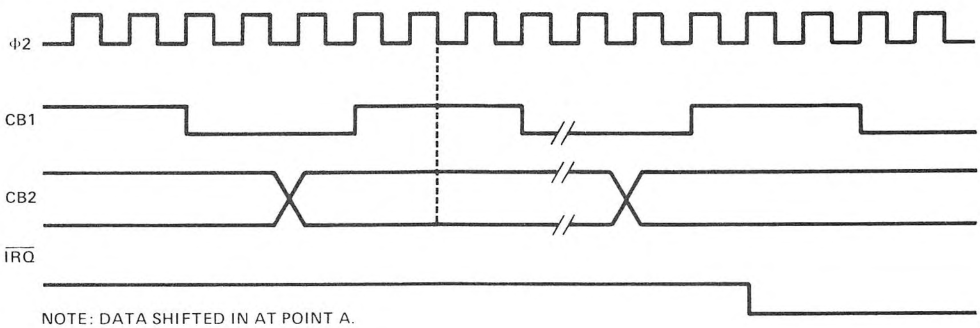


Mode 011 - Shift in Under Control of External Clock

In this mode CB1 becomes an input. This allows an external device to load the shift register at its own pace. The shift register counter will interrupt the processor each time 8 bits have been shifted in. However, the shift register counter does not stop the shifting operation; it acts simply as a pulse counter. Reading or writing the Shift Register resets the Interrupt flag and initializes the SR counter to count another 8 pulses.

Note that the data is shifted during the first system clock cycle following the leading edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. Timing for this operation is shown in Figure 13.

Figure 13. TIMING SEQUENCE FOR SHIFTING IN UNDER CONTROL OF EXTERNAL CLOCK



Shift Register Output Modes

The four Shift Register Output Modes are selected by setting the Input/Output Control Bit (ACR4) to a logic 1 and then selecting the specific output mode with ACR3 and ACR2. In each of these modes the Shift Register shifts data out of bit 7 to the CB2 pin. At the same time the contents of bit 7 are shifted back into bit 0. As in the input modes, CB1 is used either as an output to provide shifting pulses out or as an input to allow shifting from an external pulse. The four modes are as follows:

ACR4	ACR3	ACR2	Mode
1	0	0	Shift out - Free-running mode. Shift rate controlled by T2.
1	0	1	Shift out - Shift rate controlled by T2. Shift pulses generated on CB1.
1	1	0	Shift out at system clock rate.
1	1	1	Shift out under control of an external pulse.

Mode 100 Free-Running Output

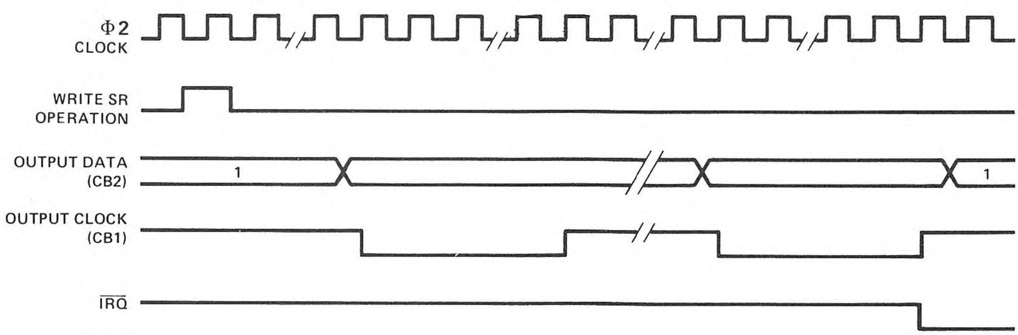
This mode is very similar to mode 101 in which the shifting rate is set by T2. However, in mode 100 the SR Counter does not stop the shifting operation. Since the Shift Register bit 7 (SR7) is recirculated back into bit 0, the 8 bits loaded into the shift register will be clocked onto CB2 repetitively. In this mode the shift register counter is disabled.

Mode 101 - Shift out Under Control of T2

In this mode the shift rate is controlled by T2 (as in the previous mode). However, with each read or write of the shift register the SR Counter is reset and 8 bits are shifted onto CB2. At the same time, 8 shift pulses are generated on CB1 to control shifting in External devices. After the 8 shift pulses, the shifting is disabled, the SR Interrupt Flag is set and CB2 goes to a state determined by the CB2 Control bit (PC5) in the Peripheral Control Register.

The CB2 Control bits (PC7, PC6, and PC5) must be used to set CB2 to a manual output selecting either a high or low polarity. If the shift register is reloaded before the last time-out, the shifting will continue. This sequence is illustrated in Figure 14.

Figure 14. SHIFTING OUT UNDER CONTROL OF T2

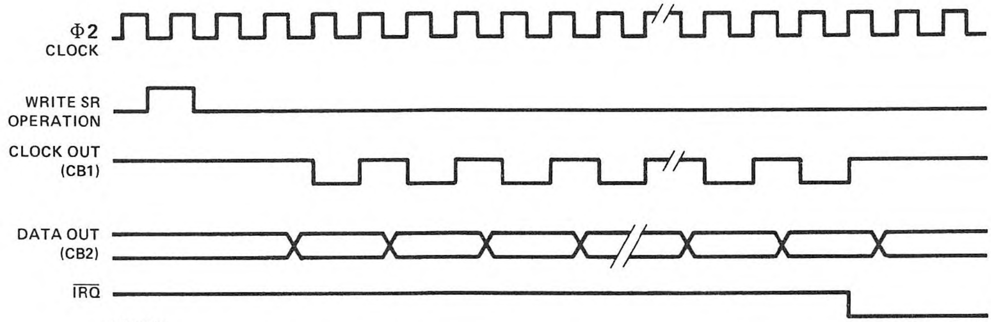


NOTES:
1. DATA OUT DETERMINED BY CB2 CONTROL IN PCR.

Mode 110 - Shifting out at System Clock Rate

In this mode the shift register operation is similar to that shown in Figure 11. However, the shifting rate is a function of the system clock on the chip enable pin (Φ2) and is independent of T2. Timer 2 resumes its normal function as an independent interval timer. Figure 15 illustrates the timing sequence for mode 110.

Figure 15. SHIFTING OUT UNDER CONTROL OF SYSTEM CLOCK

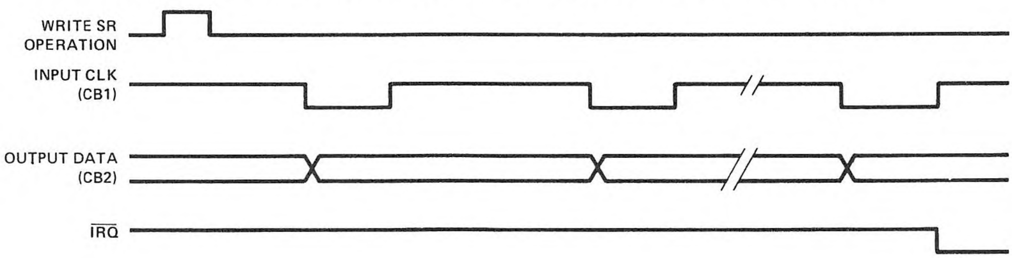


NOTES:
1. Data out determined by CB2 control in PCR.

Mode 111 - Shift out under Control of an External Pulse

In this mode, shifting is controlled by pulses applied to the CB1 pin by an external device. The SR counter sets the SR Interrupt flag each time it counts 8 pulses but it does not disable the shifting function. Each time the microprocessor writes or reads the shift register, the SR Interrupt flag is reset and the SR counter is initialized to begin counting the next 8 shift pulses on pin CB1. After 8 shift pulses, the interrupt flag is set. The microprocessor can then load the shift register with the next byte of data.

Figure 16. SHIFTING OUT UNDER CONTROL OF EXTERNAL CLOCK



H. Interrupt Control

Controlling interrupts within the SY6522 involves three principal operations. These are flagging the interrupts, enabling interrupts and signalling to the processor that an active interrupt exists within the chip. Interrupt flags are set by interrupting conditions which exist within the chip or on inputs to the chip. These flags normally remain set until the interrupt has been serviced. To determine the source of an interrupt, the microprocessor must examine these flags in order from highest to lowest priority. This is accomplished by reading the flag register into the processor accumulator, shifting this register either right or left and then using conditional branch instructions to detect an active interrupt.

Associated with each interrupt flag is an interrupt enable bit. This bit can be set or cleared by the processor to enable interrupting the processor from the corresponding interrupt flag. If an interrupt flag is set to a logic 1 by an interrupting condition, and the corresponding interrupt enable bit is set to a 1, the Interrupt Request Output ($\overline{IRQ}$) will go low. $\overline{IRQ}$ is an "open-collector" output which can be "wire-or'ed" with other devices in the system to interrupt the processor.

In the SY6522, all the interrupt flags are contained in one register. In addition, bit 7 of this register will be read as a logic 1 when an interrupt exists within the chip. This allows very convenient polling of several devices within a system to locate the source of an interrupt.

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REGISTER NAME	REGISTER BIT							
	7	6	5	4	3	2	1	0
Interrupt Flag Register (IFR)	IRQ	T1	T2	CB1	CB2	SR	CA1	CA2
Interrupt Enable Register (IFR)	Set/ clear control	T1	T2	CB1	CB2	SR	CA1	CA2

Interrupt Flag Register

The IFR is a read/bit-clear register. When the proper chip select and register signals are applied to the chip, the contents of this register are placed on the data bus. Bit 7 indicates the status of the $\overline{IRQ}$ output. This bit corresponds to the logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: X = logic AND, + = Logic OR.

Bits six through zero are latches which are set and cleared as follows:

Bit #	Set by	Cleared By
0	Active transition of the signal on the CA2 pin.	Reading or writing the A port Output Register (ORA) using address 0001.
1	Active transition of the signal on the CA1 pin.	Reading or writing the A Port Output Register (ORA) using address 0001.
2	Completion of eight shifts.	Reading or writing the Shift Register.
3	Active transition of the signal on the CB2 pin.	Reading or writing the B Port Output Register.
4	Active transition of the signal on the CB1 pin.	Reading or writing the B Port Output Register.
5	Time-out of Timer 2.	Reading T2 low order counter. Writing T2 high order counter.
6	Time-out of Timer 1.	Reading T1 low order counter. Writing T1 high order counter.

The IFR bit 7 is not a flag. Therefore, this bit is not directly cleared by writing a logic 1 into it. It can only be cleared by clearing all the flags in the register or by disabling all the active interrupts as discussed in the next section.

Interrupt Enable Register (IER)

For each interrupt flag in IFR, there is a corresponding bit in the Interrupt Enable Register. The system processor can set or clear selected bits in this register to facilitate controlling individual interrupts without affecting others. This is accomplished by writing to address 1110 (IER address). If bit 7 of the data placed on the system data bus during this write operation is a 0, each 1 in bits 6 through 0 clears the corresponding bit in the Interrupt Enable Register. For each zero in bits 6 through 0, the corresponding bit is unaffected.

Setting selected bits in the Interrupt Enable Register is accomplished by writing to the same address with bit 7 in the data word set to a logic 1. In this case, each 1 in bits 6 through 0 will set the corresponding bit. For each zero, the corresponding bit will be unaffected. This individual control of the setting and clearing operations allows very convenient control of the interrupts during system operation.

In addition to setting and clearing IER bits, the processor can read the contents of this register by placing the proper address on the register select and chip select inputs with the R/W line high. Bit 7 will be read as a logic 0.

I. Function Control

Control of the various functions and operating modes within the SY6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR) and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the interval timers (T1, T2), and the serial port (SR).

Peripheral Control Register

The Peripheral Control Register is organized as follows:

Bit #	7	6	5	4	3	2	1	0
Function		CB2 Control		CB1 Control		CA2 Control		CA1 Control

Each of these functions is discussed in detail below.

1. CA1 Control

Bit 0 of the Peripheral Control Register selects the active transition of the input signal applied to the CA1 interrupt input pin. If this bit is a logic 0, the CA1 interrupt flag will be set by a negative transition (high to low) of the signal on the CA1 pin. If PCR0 is a logic 1, the CA1 interrupt flag will be set by a positive transition (low to high) of this signal.

2. CA2 Control

The CA2 pin can be programmed to act as an interrupt input or as a peripheral control output. As an input, CA2 operates in two modes, differing primarily in the methods available for resetting the interrupt flag. Each of these two input modes can operate with either a positive or a negative active transition as described above for CA1.

In the output mode, the CA2 pin combines the operations performed on the CA2 and CB2 pins of the SY6522. This added flexibility allows processor to perform a normal "write" handshaking in a system which uses CB1 and CB2 for the serial operations described above. The CA2 operating modes are selected as follows:

PCR3	PCR2	PCR1	Mode
0	0	0	Input mode—Set CA2 interrupt flag (IFR0) on a negative transition of the input signal. Clear IFR0 on a read or write of the Peripheral A Output Register.
0	0	1	Independent interrupt input mode—Set IFR0 on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 Interrupt flag.
0	1	0	Input mode—Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFR0 with a read or write of the Peripheral A Output Register.
0	1	1	Independent Interrupt input mode—Set IFR0 on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag.
1	0	0	Handshake output mode—Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1.
1	0	1	Pulse Output mode—CA2 goes low for one cycle following a read or write of the Peripheral A Output Register.
1	1	0	Manual output mode—The CA2 output is held low in this mode.
1	1	1	Manual output mode—The CA2 output is held high in this mode.

In the independent input mode, writing or reading the ORA register has no effect on the CA2 interrupt flag. This flag must be cleared by writing a logic 1 into the appropriate IFR bit. This mode allows the processor to handle interrupts which are independent of any operations taking place on the peripheral I/O ports.

The handshake and pulse output modes have been described previously. Note that the timing of the output signal varies slightly depending on whether the operation is initiated by a read or a write.

3. CB1 Control

Control of the active transition of the CB1 input signal operates in exactly the same manner as that described above for CA1. If PCR4 is a logic 0 the CB1 interrupt flag (IFR4) will be set by a negative transition of the CB1 input signal and cleared by a read or write of the ORB register. If PCR4 is a logic 1, IFR4 will be set by a positive transition of CB1.

If the Shift Register function has been enabled, CB1 will act as an input or output for the shift register clock signals. In this mode the CB1 interrupt flag will still respond to the selected transition of the signal on the CB1 pin.

4. CB2 Control

With the serial port disabled, operation of the CB2 pin is a function of the three high order bits of the PCR. The CB2 modes are very similar to those decribed previously for CA2. These modes are selected as follows:

PCR7	PCR6	PCR5	Mode
0	0	0	Interrupt input mode–Set CB2 interrupt flag (IFR3) on a negative transition of the CB2 input signal. Clear IFR3 on a read or write of the Peripheral B Output Register.
0	0	1	Independent interrupt input mode–Set IFR3 on a negative transition of the CB2 input signal. Reading or writing ORB does not clear the interrupt flag.
0	1	0	Input mode–Set CB2 interrupt flag on a positive transition of the CB2 input signal. Clear the CB2 interrupt flag on a read or write of ORB.
0	1	1	Independent input mode–Set IFR3 on a positive transition of the CB2 input signal. Reading or writing ORB does not clear the CB2 interrupt flag.
1	0	0	Handshake output mode–Set CB2 low on a write ORB operation. Reset CB2 high with an active transition of the CB1 input signal.
1	0	1	Pulse output mode–Set CB2 low for one cycle following a write ORB operation.
1	1	0	Manual output mode–The CB2 output is held low in this mode.
1	1	1	Manual output mode–The CB2 output is held high in this mode.

AUXIALIARY CONTROL REGISTER

Many of the functions in the Auxiliary Control Register have been discussed previously. However, a summary of this register is presented here as a convenient reference for the SY6522 user. The Auxiliary Control Register is organized as follows:

Bit #	7 6	5	4 3 2	1	0
Function	T1 Control	T2 Control	Shift Register Control	PB Latch Enable	PA Latch Enable

1. PA Latch Enable

The SY6522 provides input latching on both the PA and PB ports. In this mode, the data present on the peripheral A input pins will be latched within the chip when the CA1 interrupt flag is set. Reading the PA port will result in these latches being transferred into the processor. As long as the CA1 interrupt flag is set, the data on the peripheral pins can change without affecting the data in the latches. This input latching can be used with any of the CA2 input or output modes.

It is important to note that on the PA port, the processor always reads the data on the peripheral pins (as reflected in the latches). For output pins, the processor still reads the latches. This may or may not reflect the data currently in the ORA. Proper system operation requires careful planning on the part of the system designer if input latching is combined with output pins on the peripheral ports.

Input latching is enabled by setting bit 0 in the Auxiliary Control Register to a logic 1. As long as this bit is a 0, the latches will directly reflect the data on the pins.

2. PB Latch Enable

Input latching on the PB port is controlled in the same manner as that described for the PA port. However, with the peripheral B port the input latch will store either the voltage on the pin or the contents of the Output Register (ORB) depending on whether the pin is programmed to act as an input or an output. As with the PA port, the processor always reads the input latches.

3 Shift Register Control

The Shift Register operating mode is selected as follows:

ACR4	ACR3	ACR2	Mode
0	0	0	Shift Register Disabled.
0	0	1	Shift in under control of Timer 2.
0	1	0	Shift in under control of system clock.
0	1	1	Shift in under control of external clock pulses.
1	0	0	Free-running output at rate determined by Timer 2.
1	0	1	Shift out under control of Timer 2.
1	1	0	Shift out under control of the system clock.
1	1	1	Shift out under control of external clock pulses.

4. T2 Control

Timer 2 operates in two modes. If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

5. T1 Control

Timer 1 operates in the one-shot or free-running mode with the PB7 output control enabled or disabled. These modes are selected as follows:

ACR7	ACR6	Mode
0	0	One-shot mode–Output to PB7 disabled
0	1	Free-running mode–Output to PB7 disabled.
1	0	One-shot mode–Output to PB7 enabled.
1	1	Free-running mode–Output to PB7 enabled.

APPLICATION OF THE SY6522

The SY6522 represents a significant advance in general-purpose microprocessor I/O. Unfortunately, its many powerful features, coupled with a set of very flexible operating modes, cause this device to appear to be very complex at first glance. However, a detailed analysis will show that the VIA is organized to allow convenient control of these powerful features. This section seeks to assist the system designer in his understanding of the SY6522 by illustrating how the device can be used in microprocessor-based systems.

A. Control of the SY6522 Interrupts

Organization of the SY6522 interrupt flags into a single register greatly facilitates the servicing of interrupts from this device. Since there is only one $\overline{IRQ}$ output for the seven possible sources of interrupt within the chip, the processor must examine these flags to determine the cause of an interrupt. This is best accomplished by first transferring the contents of the flag register into the accumulator. At this time it may be necessary to mask off these flags which have been disabled in the Interrupt Enable Register. This is particularly important for the edge detecting inputs where the flags may be set whether or not the interrupting function has been enabled. Masking off these flags can be accomplished by performing an AND operation between the IER and the accumulator or by performing an "AND IMMEDIATE". The second byte of this AND # instruction should specify those flags which correspond to interrupt functions which are to be serviced.

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If the N flag is set after these operations, an active interrupt exists within the chips. This interrupt can be detected with a series of shift and branch instructions.

Clearing interrupt flags is accomplished very conveniently by writing a logic 1 directly into the appropriate bit of the Interrupt Flag Register. This can be combined with an interrupt enable or disable operation as follows:

```
LDA #@10010000  ; initialize accumulator
STA IFR         ; clear interrupt flag
STA IER         ; set interrupt enable flag
```

or:

```
LDA #@00001000  ; initialize accumulator
STA IFR         ; clear interrupt flag
STA IER         ; disable interrupt
```

Another very useful technique for clearing interrupt flags is to simply transfer the contents of the flag register back into this register as follows:

```
LDA IFR   ; transfer IFR to accumulator
STA IFR   ; clear flags corresponding to active interrupts
```

After completion of this operation the accumulator will still contain the interrupt flag information. Most important, writing into the flag register clears only those flags which are already set. This eliminates the possibility of inadvertently clearing a flag while it is being set.

B. Use of Timer 1

Timer 1 represents one of the most powerful features of the SY6522. The ability to generate very evenly spaced interrupts and the ability to control the voltage on PB7 makes this timer particularly valuable in various timing, data detection and waveform generation applications.

Time-of-Day Clock Applications

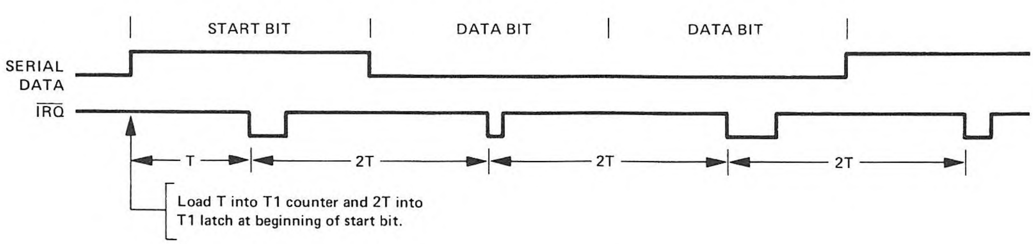
An important feature of many systems is the time-of-day clock. In microprocessor-based systems the time of day is usually maintained in memory and is updated in an interrupt service routine. A regular processor interrupt will then assure that this time of day will always be available when it is needed in the main program.

Generating very regular interrupts using previously available timers presented difficulties because of the need to re-load the timer for each interrupt. Unfortunately, the time between the interrupts will fluctuate due to variations in the interrupt response time. This problem is eliminated in the Timer 1 "free-running" mode. The accuracy of these "free-running" interrupts is only a function of the system clock and is not affected by interrupt response time.

Asynchronous Data Detection

The extraction of clock and data information from serial asynchronous ASCII signals or from any single channel data recording device relies on the ability to establish accurate strobes. As discussed previously, the period of these strobes can be seriously affected by the interrupt response time using conventional timers. However, T1 again allows generation of very accurate interrupts. The processor responds to these interrupts by strobing the input data. The ability to reload the T1 latches without affecting the count-down in progress is very useful in this application. This allows the strobe time to be doubled or halved during data detection. This sequence of operation is as follows:

Figure 17. DETECTING ASYNCHRONOUS DATA USING TIMER 1



MICRO-PROCESSORS

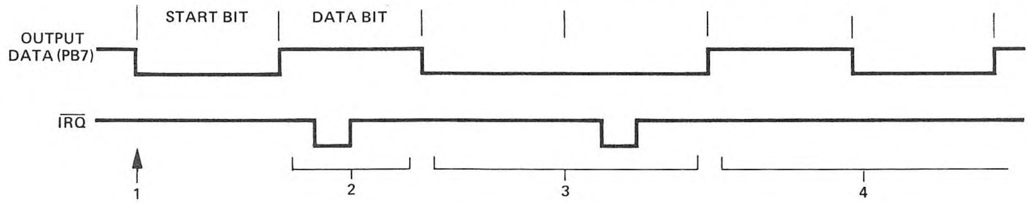
Waveform Generation with Timer 1

In addition to generating processor interrupts, Timer 1 can be used to control the output voltage on peripheral pin PB7 (output mode). In this mode a single negative pulse can be generated on PB7 (one-shot mode) or, in the free-running mode, a continuous waveform can be generated. In this latter mode the voltage on PB7 will be inverted each time T1 times out.

A single solenoid can be triggered very conveniently in the one-shot mode if the PB7 signal is used to control the solenoid directly. With this configuration the solenoid can be triggered by simply writing to T1C-H.

Generating very complex waveforms can be a simple problem if T1 is used to control PB7 in the free-running mode. During any count-down process the latches can be loaded to determine the length of the next count-down period. Figure 18 shows this timing sequence for generating ASCII serial data.

Figure 18. ASCII SERIAL DATA GENERATION USING T1



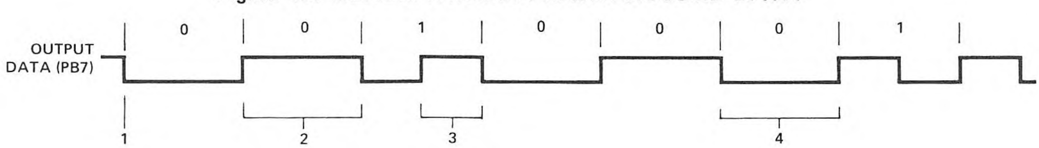
1. Load T into T1 counter and latch. Load T into T2 to trigger T1 latch reload.
2. Load 2T into T1 latch during this bit time. Load 2T into T2, as before.
3. Load T into T1 latch anytime during this period. Load NT into T2. N = number of 1's or 0's which follow.
4. A series of 1's and 0's will be generated until the T1 latch is again changed. Note that the use of T2 to control reloading the T1 latch eliminates the need to interrupt on each transition.

MICRO-
PROCESSORS

An application where this mode of operation is also very powerful is in the generation of bi-phase encoded data for tape or disk storage. This encoding technique and the sequence of operations which would take place are illustrated in Figure 19.

These applications represent only a tiny portion of the potential T1 applications. Some other possibilities are pulse width modulation waveforms, sound generation for video games, A/D techniques requiring very accurate pulse widths, and waveform synthesis in electronic games.

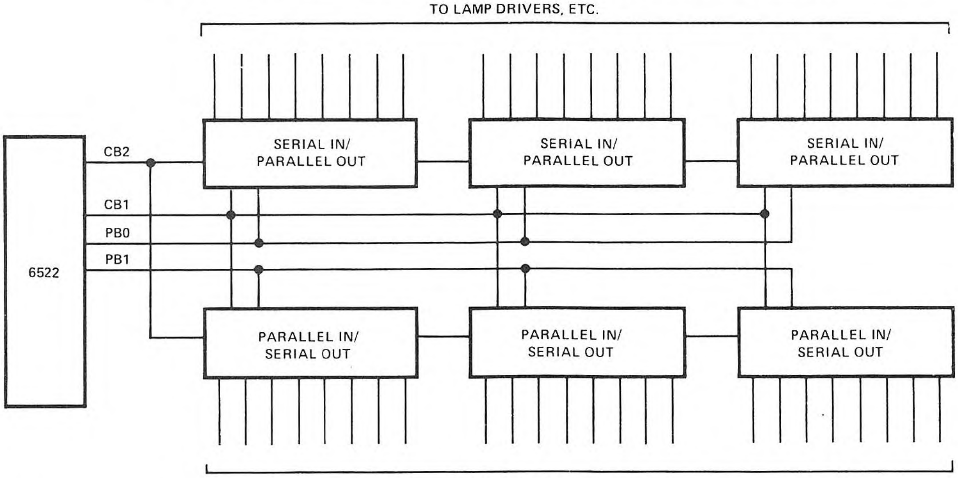
Figure 19. GENERATING BI-PHASE ENCODED DATA



1. Load T1 counter and latch.
2. Shift T1 latch one bit to the right during this period.
3. Shift T1 latch left during this period.
4. Shift T1 latch right during this period.

Note that T1 must be accessed only when the output data changes. A string of 1's or 0's can be generated without processor intervention.

Figure 22. EXPANDING SYSTEM I/O USING SHIFT REGISTER

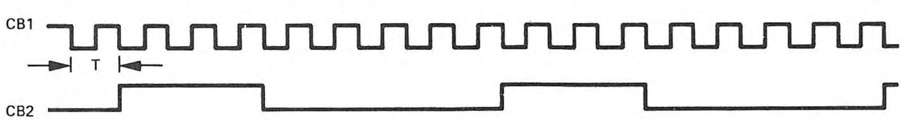


Clock Generation Using the Shift Register

In all output modes the data shifted out of bit 7 will also be shifted into bit 0. For this reason the Shift Register need not be re-loaded if the same data is to be shifted out each time. A Shift Register read operation can be used to trigger the shifting operation.

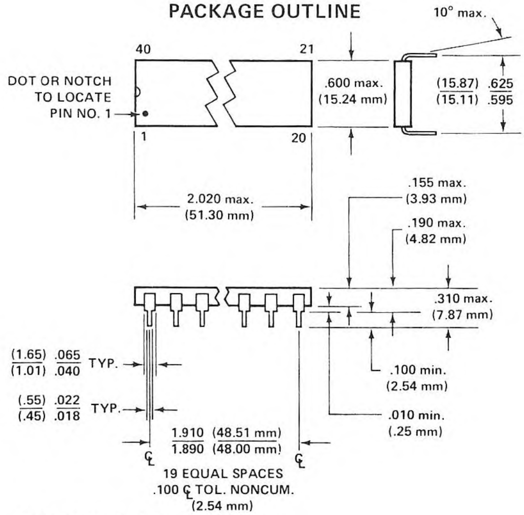
This capability is very useful for generating peripheral clocks in the continuous output mode. This mode allows an 8-bit pattern to be shifted out continuously. This is illustrated in Figure 23. Note that in this mode the shifting operation is controlled by Timer 2. A single bit time can therefore be up to 256 clock cycles in length.

Figure 23. CLOCK GENERATION USING SR FREE-RUNNING MODE

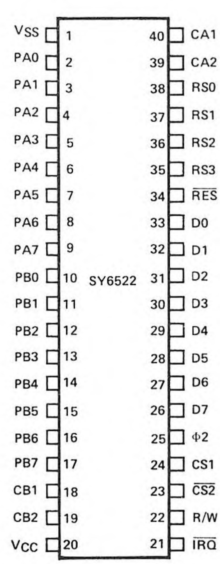


NOTES:
1. Shift Register loaded with 1110 0000_2 initially. 2. T determined by Timer 2.

PACKAGE OUTLINE



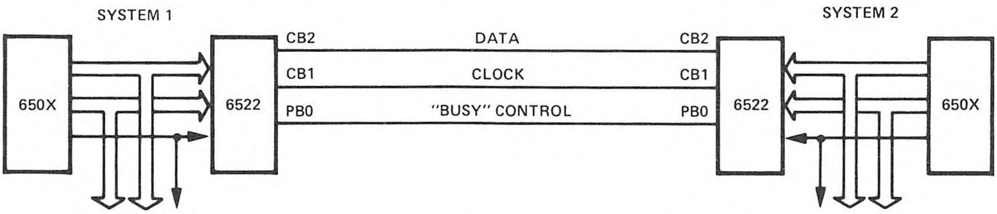
NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation



Using the SY6522 Shift Register

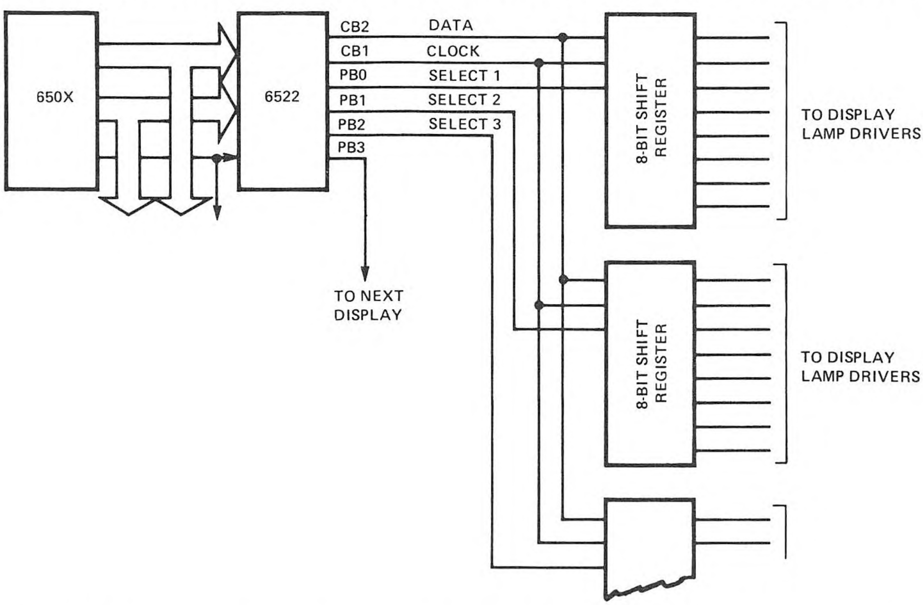
The Shift Register in the SY6522 is designed primarily as a synchronous serial communications port for distributed systems. These systems can be either single-processor with distributed peripheral controllers or distributed processor systems. The most important characteristic of the Shift Register in these applications is its ability to transfer information at relatively slow data rates to allow the use of R-C noise suppression techniques. This transfer can be accomplished while the processor is servicing other aspects of the system. An example of a simple 2-processor distributed system is shown in Figure 20. Use of the SY6522 Shift Register allows effective communication between the two systems without the use of relatively complex asynchronous communications techniques.

Figure 20. USING SHIFT REGISTER FOR INTER-SYSTEM COMMUNICATION



In a system with distributed peripherals, the Shift Register can be used to transfer data to the peripheral interface devices. This is illustrated in Figure 21 for a system with a number of distributed status displays. These displays are serviced by stand-alone controllers which actuate the lamps in the status displays with simple drivers. The data and clock lines are wired in parallel to each unit. In addition, a single SY6522 peripheral port allows selection of the display to be loaded. These select lines can be eliminated if all displays are to contain the same information. With the system shown, the status display can be updated at any time by simply selecting the desired display and then writing to the Shift Register.

Figure 21. USING THE SHIFT REGISTER FOR SERVICING REMOTE STATUS DISPLAYS



Remote input devices can be serviced in much the same manner by shifting data into the Shift Register under control of a peripheral port output as shown in Figure 21. Each set of input switches can be polled by first selecting the set to be polled and then triggering the shifting operation with a Shift Register read operation. A shift register interrupt can be used to cause the processor to read the resulting input information after shifting is complete.

The techniques described above can be utilized to expand I/O capability in a microprocessor based system. In a system with many status lamps or many input switches, simple TTL shift registers will provide the necessary I/O in a very cost effective manner. This is illustrated in Figure 22.

Synertek®

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(408) 984-8900 TWX 910-338-0135

SY6530

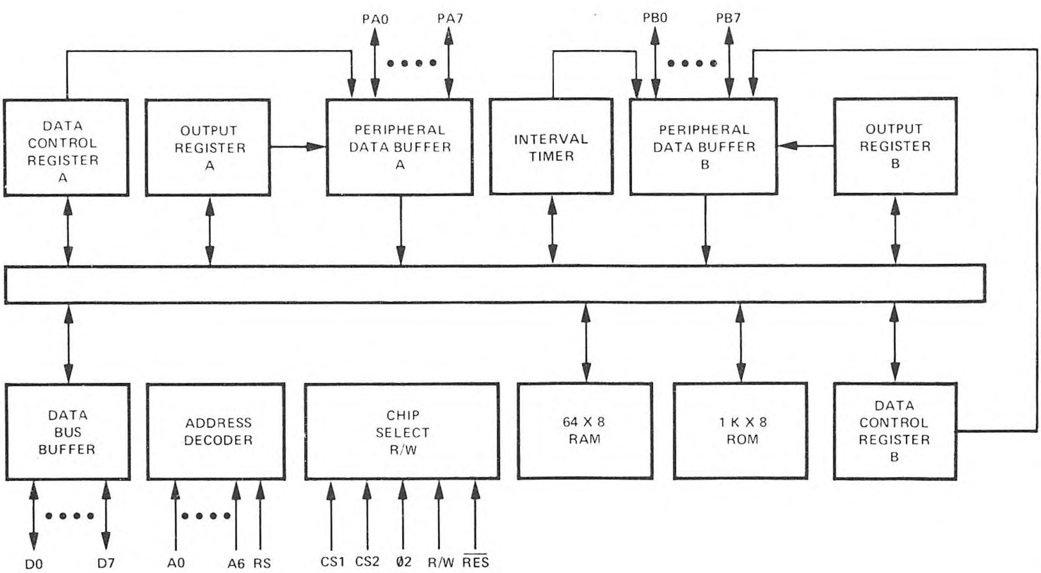
SY6530 (MEMORY, I/O, TIMER ARRAY)

The SY6530 is designed to operate in conjunction with the SY650X microprocessor Family. It is comprised of a mask programmable 1024 x 8 ROM, a 64 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- 1024 x 8 ROM
- 64 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedence Three-State Data Pins
- Allows up to 7K contiguous bytes of ROM with no external decoding

MICRO-PROCESSORS

FIGURE 1. SY6530 BLOCK DIAGRAM



B-15K-11/77

MAXIMUM RATINGS

RATING	SYMBOL	VOLTAGE	UNIT
Supply Voltage	V_{CC}	-.3 to +7.0	V
Input/Output Voltage	V_{IN}	-.3 to +7.0	V
Operating Temperature Range	T_{OP}	0 to 70	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 25°C)

	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	V_{SS}+2.4		V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}-.3		V_{SS}+.4	V
Input Leakage Current; V_{IN} = V_{SS} +5V AØ-A9, RS, R/W, $\overline{RES}$, Ø2, PB6*, PB5*	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedence State (Three State); V_{IN} = .4V to 2.4V; DØ-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PAØ-PA7, PBØ-PB7	I_{IH}	-100.	-300.		μA
Low Input Current; V_{IN} = .4V PAØ-PA7, PBØ-PB7	I_{IL}		-1.0	-1.6	mA
Output High Voltage V_{CC} = MIN, $I_{LOAD} \leqslant -100\mu A$ (PAØ-PA7, PBØ-PB7, DØ-D7) $I_{LOAD} \leqslant$ -3mA (PAØ-PBØ)	V_{OH}	 V_{SS}+2.4 V_{SS}+1.5			V
Output Low Voltage V_{CC} = MIN, $I_{LOAD} \leqslant$ 1.6mA	V_{OL}			V_{SS}+.4	V
Output High Current (Sourcing); $V_{OH} \geqslant$ 2.4V (PAØ-PA7, PBØ-PB7, DØ-D7) $\geqslant$ 1.5V Available for other than TTL (Darlingtons) (PAØ, PBØ)	I_{OH}	 -100 -3.0	 -1000 -5.0		 μA mA
Output Low Current (Sinking); $V_{OL} \leqslant$ .4V	I_{OL}	1.6			mA
Clock Input Capacitance	C_{CLK}			30	pF
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF
Power Dissipation	P_D		500	1000	mW

*When Programmed as address pins
All values are D.C. readings

WRITE TIMING CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Period	T_{CYC}	1		10	μs
Rise & Fall Times	T_R, T_F			25	ns
Clock Pulse Width	T_C	470			ns
R/W valid before positive transition of clock	T_{WCW}	180			ns
Address valid before positive transition of clock	T_{ACW}	180			ns
Data bus valid before negative transition of clock	T_{DCW}	300			ns
Data Bus Hold Time	T_{HW}	10			ns
Peripheral data valid after negative transition of clock	T_{CPW}			1	μs
Peripheral data valid after negative transition of clock driving CMOS (Level = V_{CC} -30%)	T_{CMOS}			2	μs

MICRO-PROCESSORS

READ TIMIMG CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
R/W valid before positive transition of clock	T_{WCR}	180			ns
Address valid before positive transition of clock	T_{ACR}	180			ns
Peripheral data valid before positive transition of clock	T_{PCR}	300			ns
Data bus valid after positive transition of clock	T_{CDR}			395	ns
Data Bus Hold Time	T_{HR}	10			ns
$\overline{IRQ}$ (Interval Timer Interrupt) valid before positive transition of clock	T_{IC}	200			ns

Loading = 30 pF + 1 TTL load for PAØ-PA7, PBØ-PB7
= 130 pF + 1 TTL load for DØ-D7

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a low ($\leqslant$0.4V) on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$ or high level clock $V_{IL} < 0.2$, $V_{IH} = V_{CC}\ ^{+.3}_{-.2}$).

Read/Write (R/W)

The R/W is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the SY6530. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the SY6530. A low on the R/W pin allows a write (with proper addressing) to the SY6530.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the data direction register. The pin will be normally high with a low indicating an interrupt from the SY6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pullup may be omitted with a mask option.

Data Bus (D0-D7)

The SY6530 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports

The SY6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PB5, PB6 and PB7 also have other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the SY6530 it receives data stored in the data register. The microproccessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volts for a "0" as the peripheral pins are all TTL compatible. Pins PA0 and PB0 are also capable of sourcing 3 ma at 1.5V, thus making them capable of direct transistor drive.

Address Lines (A0-A9)

There are 10 address pins. In addition to these 10, there is the ROM SELECT (RS) pin. The above pins, A0-A9 and ROM SELECT, are always used as addressing pins. There are 2 additional pins which are mask programmable and can be used either individually or together as CHIP SELECTS. They are pins PB5 and PB6. When used as peripheral data pins they cannot be used as chip selects.

FIGURE 2. WRITE TIMING CHARACTERISTICS

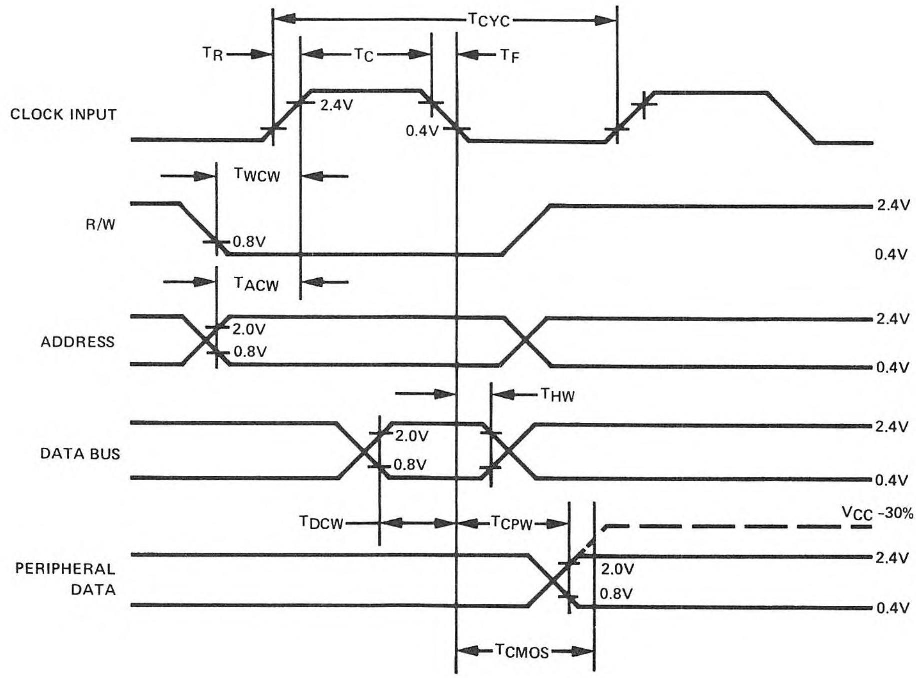
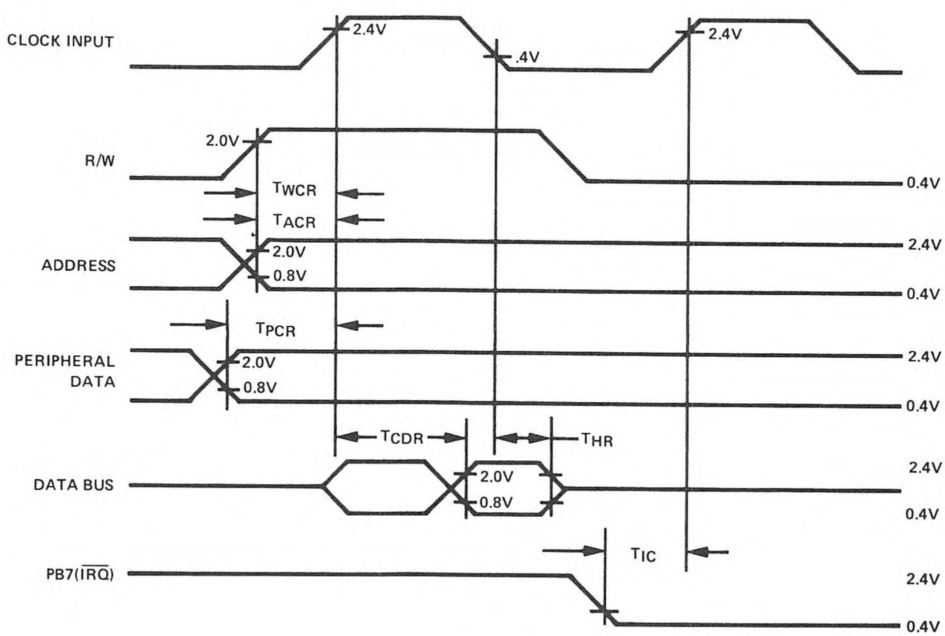


FIGURE 3. READ TIMING CHARACTERISTICS



MICRO-PROCESSORS

INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The SY6530 is divided into four basic sections, RAM, ROM, I/O and TIMER. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of 2 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O Register.

ROM 1 K Byte (8 K Bits)

The 8K ROM is in a 1024 x 8 configuration. Address lines A0-A9, as well as RS are needed to address the entire ROM. With the addition of CS1 and CS2, seven SY6530's may be addressed, giving 7168 x 8 bits of contiguous ROM.

RAM - 64 Bytes (512 Bits)

A 64 x 8 static RAM is contained on the SY6530. It is addressed by A0-A5 (Byte Select), RS, A6, A7, A8, A9, and, depending on the number of chips in the system, CS1 and CS2.

Internal Peripheral Registers

There are four internal registers, two data direction registers and two peripheral I/O data registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Therefore, anything then written into the I/O Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data to or from the I/O Register. For example, a "1" loaded into data direction A, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two data I/O registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor array.

During a read operation the microprocessor is not reading the I/O Registers but in fact is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the I/O Register. The only way the I/O Register data can be changed is by a microprocessor Write operation. The I/O Register is not affected by a Read of the data on the peripheral pins.

Interval Timer

The Timer section of the SY6530 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 4.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervls were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written into the Interval Timer, the counting intervals of 1, 8 64, 1024T are decoded from address lines A0 amd A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A_3 = 1 enables $\overline{IRQ}$ on PB7, A_3 = 0 disables $\overline{IRQ}$ on PB7. When PB7 is used as an interrupt flag with the interval timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 1 1 is read, the time since interrupt is 28T. The value read is in two's complement.

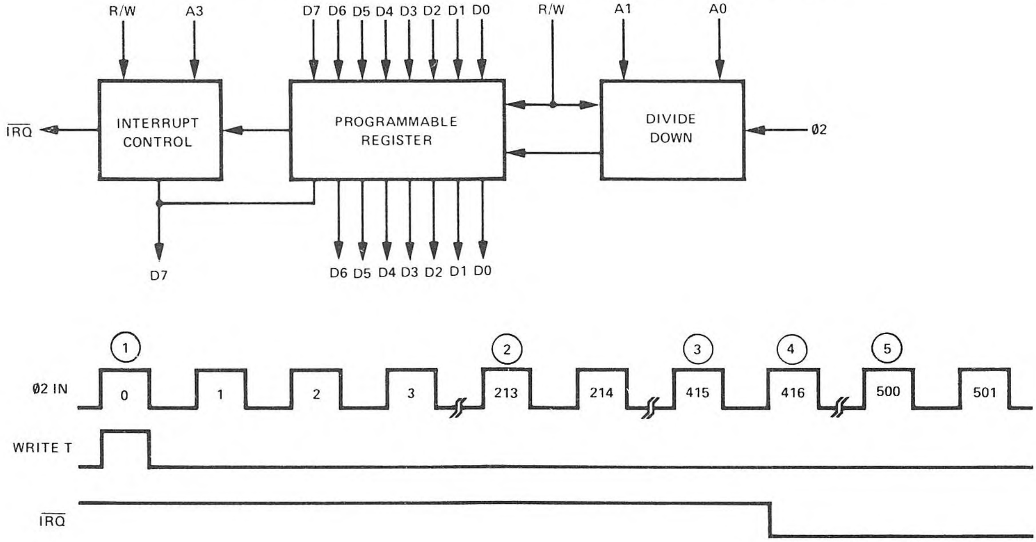
Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
ADD 1 = 0 0 0 1 1 1 0 0 = 28.

Thus to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrup is (52 x 8) +1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 5 illustrates an example of interrupt.

FIGURE 4. BASIC ELEMENTS OF INTERVAL TIMER



1. Data written into Interval timer is 0 0 1 1 0 1 0 0 = 52_{10}
2. Data in Interval timer is 0 0 0 1 1 0 0 1 = 25_{10}

   $$52 - \frac{213}{8} - 1 = 52-26-1 = 25$$

3. Data in Interval timer is 0 0 0 0 0 0 0 0 = 0_{10}

   $$52 - \frac{415}{8} - 1 = 52-51-1 = 0$$

4. Interrupt has occured at ϕ_2 pulse #416
   Data in Interval timer = 1 1 1 1 1 1 1 1
5. Data in Interval timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 1 0 0 = 84_{10}
   $84 + (52 \times 8) = 500_{10}$

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until another Write timer operation.

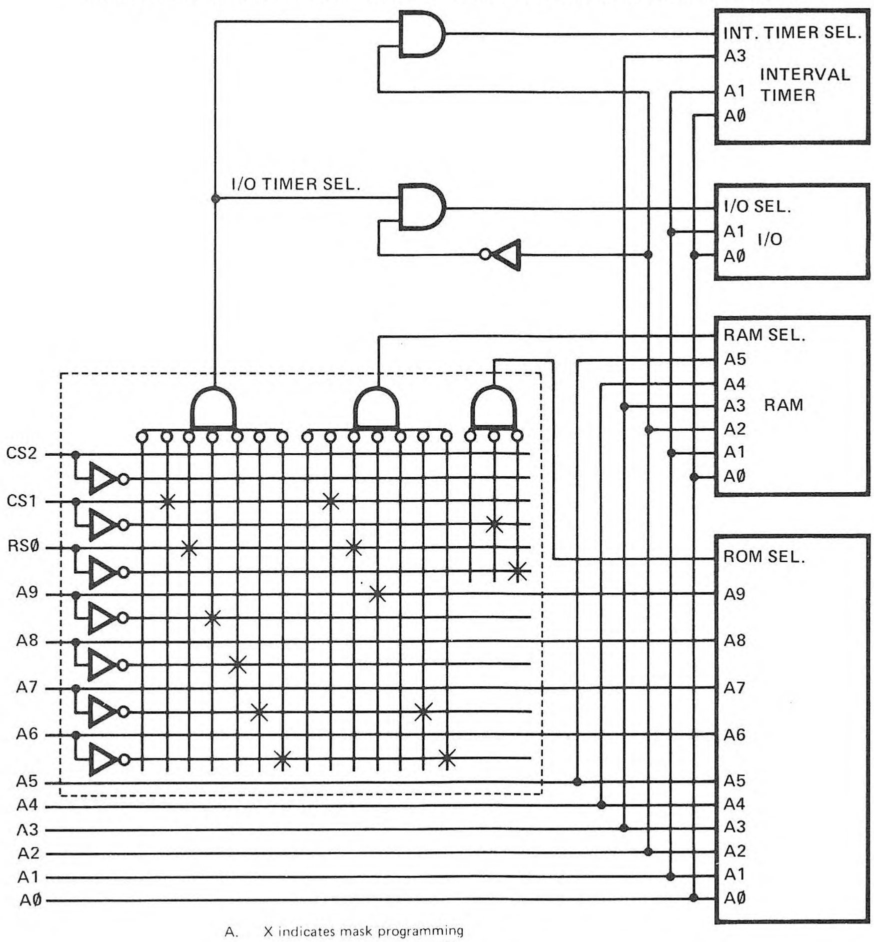
ADDRESSING

Addressing of the SY6530 offers many variations to the user for greater flexibility. The user may configure his system with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0-A9). In addition there is the possibility of 3 additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are CS1 and CS2. The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as chip-select. The third additional address line is RS. In a 2-chip system, RS would be used to distinguish between ROM and non-ROM sections of the SY6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Below is an example of a 1-chip and a 7-chip SY6530 addressing scheme.

One-Chip Addressing

Figure 6 illustrates a 1-chip system for the SY6530.

FIGURE 6. SY6530 ONE CHIP ADDRESS ENCODING DIAGRAM



A. X indicates mask programming
i.e. ROM select = CS1•RSO
RAM select = CS1•RSO•A9•A6
I/O TIMER SELECT = CS1•RSO•A9•A8•A7•A6

B. Notice that A8 is a don't care for RAM select

C. CS2 can be used PB5 in this example.

Seven-Chip Addressing

In the 7-chip system the objective would be to have 7K of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14, and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between addresses 65,535 and 58,367. The 2 pins designated as chip-select or I/O would be mask programmed as chip-select pins. Pin RS would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12 respectively. See Figure 7.

The two examples shown would allow addressing of the ROM and RAM; however, once the I/O or timer has been addressed, further decoding is necessary to select which of the I/O registers is desired, as well as the coding of the interval timer.

I/O Register - Timer Addressing

Figure 8 illustrates the address decoding for the internal elements and timer programming. Address lines A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the divide by matrix. This decoding is defined in Figure 8. In addition, address A3 is used to enable the interrupt flag to PB7.

The addressing of the ROM select, RAM select and I/O timer select lines would be as follows:

FIGURE 7. SY6530 SEVEN CHIP ADDRESSING SCHEME

		CS2 A12	CS1 A11	RSØ A10	A9	A8	A7	A6
SY6530 #1,	ROM SELECT	0	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	0
	I/O TIMER	0	0	0	1	0	0	0
SY6530 #2,	ROM SELECT	0	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	1
	I/O TIMER	0	0	0	1	0	0	1
SY6530 #3,	ROM SELECT	0	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	0
	I/O TIMER	0	0	0	1	0	1	0
SY6530 #4,	ROM SELECT	1	0	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	1
	I/O TIMER	0	0	0	1	0	1	1
SY6530 #5,	ROM SELECT	1	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	0
	I/O TIMER	0	0	0	1	1	0	0
SY6530 #6,	ROM SELECT	1	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	1
	I/O TIMER	0	0	0	1	1	0	1
SY6530 #7,	ROM SELECT	1	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	1	0
	I/O TIMER	0	0	0	1	1	1	0

* RAM select for SY6530 #5 would read = A12 • A11 • A10 • A9 • A8 • A7 • A6

FIGURE 8. ADDRESSING DECODE FOR I/O REGISTER AND TIMER

ADDRESSING DECODE

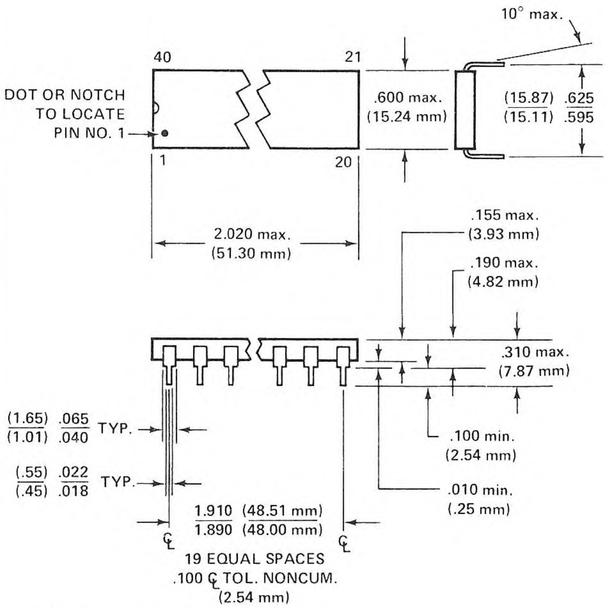
	ROM SELECT	RAM SELECT	I/O TIMER SELECT	R/W	A3	A2	A1	A0
READ ROM	1	0	0	1	–	–	–	–
WRITE RAM	0	1	0	0	–	–	–	–
READ RAM	0	1	0	1	–	–	–	–
WRITE DDRA	0	0	1	0	–	0	0	1
READ DDRA	0	0	1	1	–	0	0	1
WRITE DDRB	0	0	1	0	–	0	1	1
READ DDRB	0	0	1	1	–	0	1	1
WRITE PER. REG. A	0	0	1	0	–	0	0	0
READ PER. REG. A	0	0	1	1	–	0	0	0
WRITE PER. REG. B	0	0	1	0	–	0	1	0
READ PER. REG. B	0	0	1	1	–	0	1	0
WRITE TIMER								
÷ 1T	0	0	1	0	X	1	0	0
÷ 8T	0	0	1	0	X	1	0	1
÷ 64T	0	0	1	0	X	1	1	0
÷ 1024T	0	0	1	0	X	1	1	1
READ TIMER	0	0	1	1	X	1	–	0
READ INTERRUPT FLAG	0	0	1	1	–	1	–	1

– = Don't care condition

X A_3 = 1 Enables IRQ to PB7

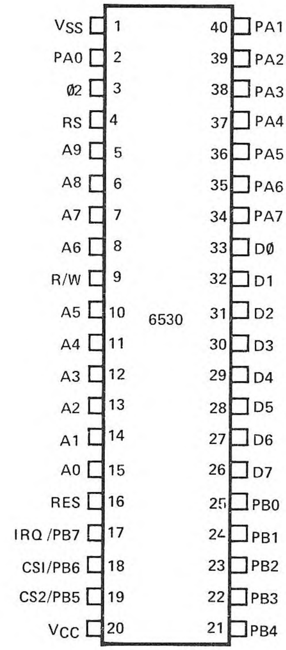
A_3 = 0 Disables IRQ to PB7

Addressing Decode for I/O Register and Timer



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

PACKAGE OUTLINE



PIN DESIGNATION

PROGRAMMING INSTRUCTIONS

The SY6530 utilizes computer aided techniques to manufacture and test custom ROM patterns. The pattern and address coding is supplied to Synertek in any of several formats.

1) 2708-type EPROMs.
2) Synertek data card formats.
3) Other input formats, providing they can be translated into one of the above.

Synertek Data Card Format

A. The format for the first and all succeeding records, except for the last record, in a file is as follows:

; N_1N_0 $A_3A_2A_1A_0$ $(D_1D_0)_1$ $(D_1D_0)_2$ $X_3X_2X_1X_0$

where:

1. All characters (N,A,D,X) are the ASCII characters 0 through F, each representing a hexadecimal digit.
2. ; is a record mark indicating the start of a record.
3. N_1N_0 = the number of bytes of data in this record (in hexadecimal). Each pair of hexadecimal characters (D_1D_0) represents a single byte in the record.
4. $A_3A_2A_1A_0$ = the hexadecimal starting address for the record. A_3 represents address bits 15 through 12, etc. The 8-bit byte represented by $(D_1D_0)_1$ is stored in address $A_3A_2A_1A_0$; $(D_1D_0)_2$ is stored in $(A_3A_2A_1A_0)$ + 1, etc.
5. (D_1D_0) = two hexadecimal digits representing an 8-bit byte of data. (D_1 = high order 4 binary bits and D_0 = low-order 4 bits). A maximum of 18 (Hex) or 24 (decimal) bytes of data per record is permitted.
6. $X_3X_2X_1X_0$ = record check sum. This is the hexadecimal sum of all characters in the record, including N_1N_0 and $A_3A_2A_1A_0$ but excluding the record mark and the check sum characters. To generate the check sum, each byte of data (represented by two ASCII characters), is treated as 8 binary bits. The binary sum of these 8-bit bytes is truncated to 16 binary bits (4 hexadecimal digits) and is then represented in the record as four ASCII characters $(X_3X_2X_1X_0)$.

B. The format for the last record in a file is as follows:

; 00 $C_3C_2C_1C_0$ $X_3X_2X_1X_0$

1. 00 = zero bytes of data in this record. This identifies this as the final record in a file.
2. $C_3C_2C_1C_0$ = the total number of records (in hexadecimal) in this file, including the last record.
3. $X_3X_2X_1X_0$ = check sum for this record.

C. Example

The following example illustrates the exact format of the hex interface file in both listing and punched paper tape form.

```
;18F000CA86004C00F0FDF9212D21FF292DBF2161F5F7FF657D677D0D40
;18F018E564672DFD7575E50000CF4112F800925198D200539192F20C98
;18F03008DB02880810DE12D894189AC2830E9800FBB6232F087F650AA5
;18F048036E20EF2FA58D4465E8FDF93DE775EF257FB520ED64657C0DEB
;18F0607F11D05A1EDF0250B0DAFE00925290991 2DB108A0298DE080C0D
;18F078D95058DF82D2D79A00ED65E68724EE05212764A5F5BDA9050E2C
;18F090EC20FF6525252469332 13F20FF31293B7E18D65042DE40500A92
;18F0A81E5E5B02534A53DE4A9B189259969F589E5E92DF52DE9E9A0CA2
;18F0C000B3268D2400EF6765E7A0B56067252 17D20AF35EDF5202F0C08
;18F0D8692525342B35256CDF12F2785FFF547FD2E2D6525BDF5A720D26
;10F0F012DB020F1A1ABF86D2DA9ADAC8DECA1B0A12
;00000B000B
```

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ADDITIONAL PATTERN INFORMATION

In addition to the ROM data patterns, it is necessary to provide the information outlined below.

CUSTOMER NAME
CUSTOMER PART NO.
CUSTOMER CONTACT (NAME)
CUSTOMER TELEPHONE NO.
CS1/PB6 (ENTER "CS1" OR "PB6")
CS2/PB5 (ENTER "CS2" OR "PB5")
PULL-UP RESISTOR ON PB7 ("YES" OR "NO")
LOGIC FORMAT ("POS" OR "NEG")

DEVICE ADDRESSING (Enter "H" for High, "L" for Low, or "N" for don't care)

	RS	CS1	CS2	A9	A8	A7	A6
ROM SELECT							
RAM SELECT							
I/O TIMER SELECT							

Send Information To:

Synertek — ROM
P.O. Box 552
3050 Coronado Dr.
Santa Clara, CA 95051

SY6530 CUSTOMER SPECIFICATION FORM

1. Date.
2. Customer name.
3. Customer part no.
   (maximum 10 digits)
4. Synertek "C" number.
5. Customer Contact.
6. Customer phone number
7. Chip Select Code
   (Check one square in each block)

CS1	
PB6	

CS2	
PB5	

PULL UP	YES	
ON PB7	NO	

8. ROM/RAM/I-O SELECTS (Specify H or L or N (don't care) in each box.

	RS	CS1	CS2	A9	A8	A7	A6
ROM SELECT				N	N	N	N
RAM SELECT							
I/O SELECT							

9. Customer's Input

   Punched Cards ☐
   Punched Tape ☐

10. Data Format

    MOS Technology ☐
    Intel Hex ☐
    Intel BPNF ☐
    Binary ☐

11. Logic Format

    Positive ☐
    Negative ☐

12. Verification Status

    Hold ☐
    Not Required ☐

MICRO-PROCESSORS

Synertek®

3050 Coronado Drive, Santa Clara, CA. 95051
(408) 984-8900 TWX 910-338-0135

SY6532

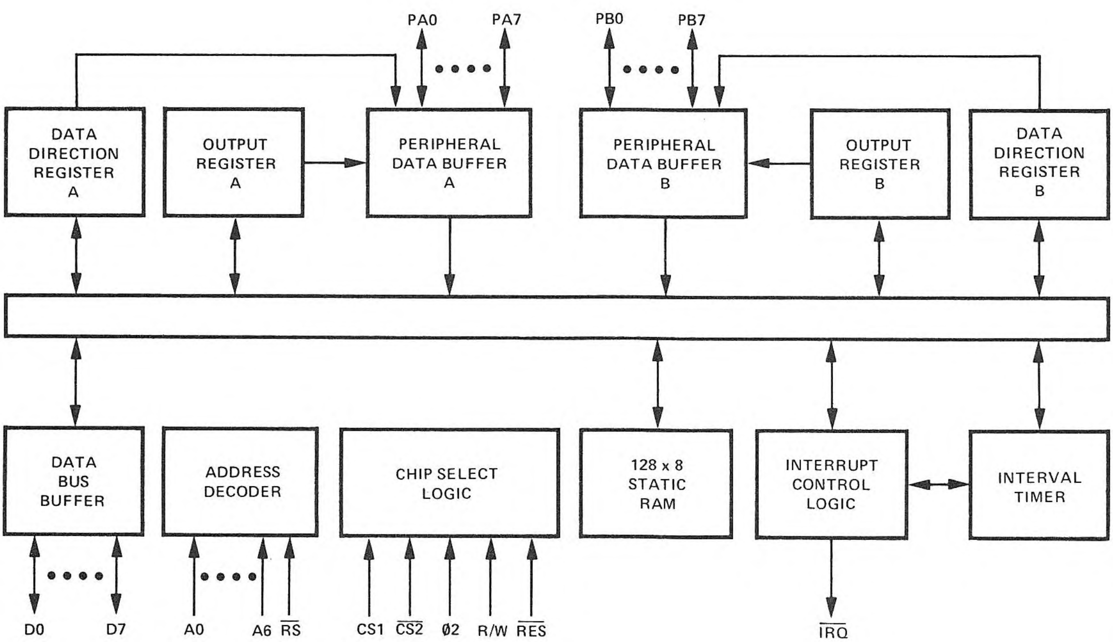
SY6532 (RAM, I/O, TIMER ARRAY)

The SY6532 is designed to operate in conjuction with the SY6500 Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, a software programmable interval timer with interrupt capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge-detect interrupt circuit.

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- Programmable edge-sensitive interrupt
- 128 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins

MICRO-PROCESSORS

Figure 1. 6532 BLOCK DIAGRAM



B-5K-10/77

MAXIMUM RATINGS

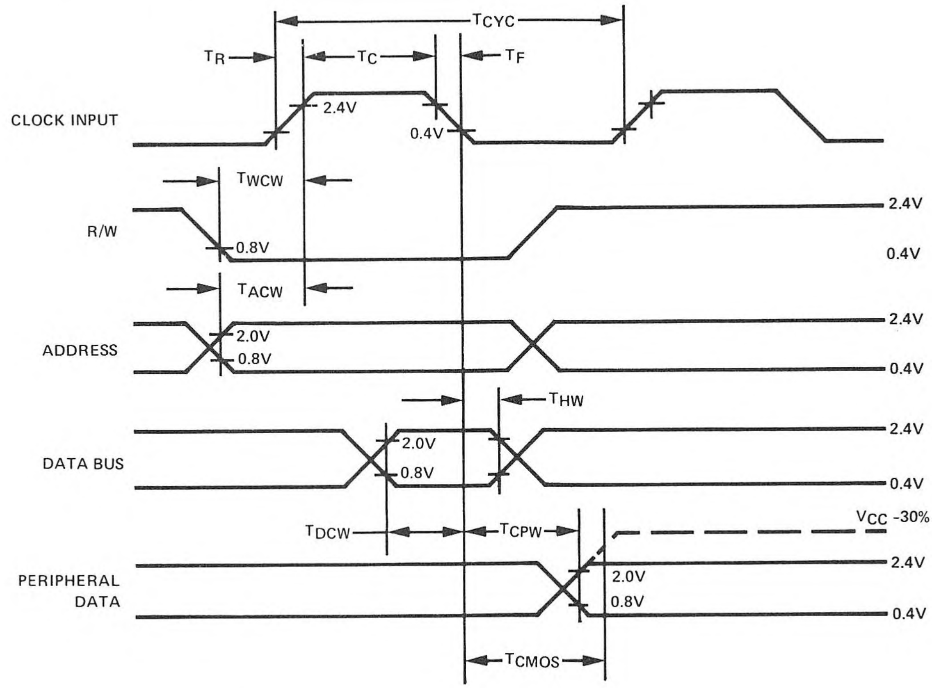
RATING	SYMBOL	VOLTAGE	UNIT
Supply Voltage	V_{CC}	-.3 to +7.0	V
Input/Output Voltage	V_{IN}	-.3 to +7.0	V
Operating Temperature Range	T_{OP}	0 to 70	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

ELECTRICAL CHARATERISTICS (V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 25° C)

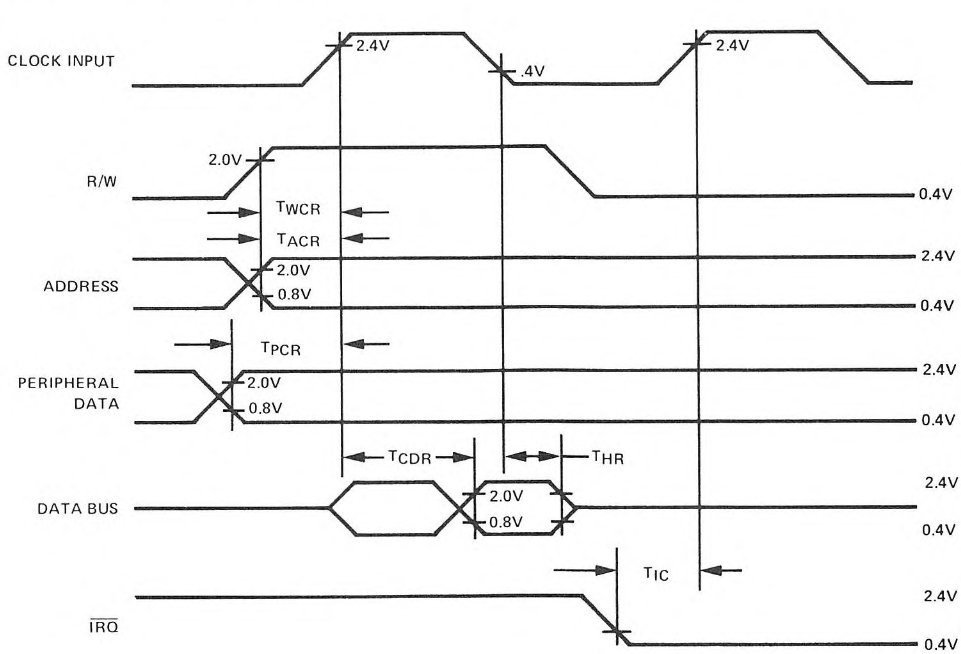
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}	V_{SS} + 2.4		V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS} - .3		V_{SS} + .4	V
Input Leakage Current; $V_{IN} = V_{SS}$ + 5V AØ-A6, $\overline{RS}$, R/W, $\overline{RES}$, Ø2, CS1, $\overline{CS2}$	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedance State (Three State); V_{IN} = .4V to 2.4V; DØ-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PAØ-PA7, PBØ-PB7	I_{IH}	-100.	-300.		μA
Input Low Current; V_{IN} = .4V PAØ-PA7, PBØ-PB7	I_{IL}		-1.0	-1.6	MA
Output High Voltage V_{CC} = MIN, $I_{LOAD} \leqslant$ -100μA (PAØ-PA7, PBØ-PB7, DØ-D7) $I_{LOAD} \leqslant$ 3 MA (PBØ-PB7)	V_{OH}	 V_{SS} + 2.4 V_{SS} + 1.5			V
Output Low Voltage V_{CC} = MIN, $I_{LOAD} \leqslant$ 1.6MA	V_{OL}			V_{SS} + .4	V
Output High Current (Sourcing); $V_{OH} \geqslant$ 2.4V (PAØ-PA7, PBØ-PB7, DØ-D7) $\geqslant$ 1.5V Available for direct transistor drive (PBØ-PB7)	I_{OH}	 -100 3.0	 -1000 5.0		 μA MA
Output Low Current (Sinking); $V_{OL} \leqslant$ .4V	I_{OL}	1.6			MA
Clock Input Capacitance	C_{Clk}			30	pf
Input Capacitance	C_{IN}			10	pf
Output Capacitance	C_{OUT}			10	pf
Power Dissipation	I_{CC}		100	125	mA

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

WRITE TIMING CHARACTERISTICS



READ TIMING CHARACTERISTICS



MICRO-PROCESSORS

WRITE TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Period	T_{CYC}	1			µS
Rise & Fall Times	TR, TF			25	NS
Clock Pulse Width	TC	470			NS
R/W valid before positive transition of clock	TWCW	180			NS
Address valid before positive transition of clock	TACW	180			NS
Data Bus valid before negative transition of clock	TDCW	300			NS
Data Bus Hold Time	THW	10			NS
Peripheral data valid after negative transition of clock	TCPW			1	µS
Peripheral data valid after negative transition of clock driving CMOS (Level = V_{CC} = 30%)	TCMOS			2	µS

READ TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
R/W valid after positive transition of clock	TWCR	180			NS
Address valid before positive transition of clock	TACR	180			NS
Peripheral data valid before positive transition of clock	TPCR	300			NS
Data Bus valid after positive transition of clock	TCDR			395	NS
Data Bus Hold Time	THR	10			NS
$\overline{IRQ}$ (Interval Timer Interrupt) valid before positive transition of clock	TIC	200			NS

Loading = 30 pf + 1 TTL load for PAØ-PA7, PBØ-PB7
= 130 pf + 1 TTL load for DØ-D7

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or high level clock ($V_{IL} < 0.2$, $V_{IH} = Vcc^{+.3}_{-.2}$).

Read/Write (R/W)

The R/W signal is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the SY6532. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the SY6532. A low on the R/W pin allows a write (with proper addressing) to the SY6532.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. It will be normally high with a low indicating an interrupt from the SY6532. $\overline{IRQ}$ is an open-drain output, permitting several units to be wire-or'ed to the common $\overline{IRQ}$ microprocessor input pin. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

Data Bus (D0-D7)

The SY6532 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports

The SY6532 has 16 pins available for peripheral I/O operations. Each pin is individually programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0-PA7 and PB0-PB7. PA7 may also function as an interrupt input pin. This feature is described in another section. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the SY6532 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.4 volts for a "1" and less than 0.4 volts for a "0" as the peripheral pins are all TTL compatible. Pins PB0-PB7 are also capable of sourcing 3 ma at 1.5 v thus making them capable of direct transistor drive.

Address Lines (A0-A6)

There are 7 address pins. In addition to these, there is the $\overline{RS}$ pin. The above pins, A0-A6 and $\overline{RS}$, are always used as addressing pins. There are 2 additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$.

INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The SY6532 is divided into four basic sections: RAM, I/O, Timer, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O register.

RAM 128 Bytes (1024 Bits)

A 128 x 8 static RAM is contained on the SY6532. It is addressed by A0-A6 (Byte Select), $\overline{RS}$, CS1, and $\overline{CS2}$.

Internal Peripheral Registers

There are four 8-bit internal registers: two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of data into and out of the peripheral I/O pins. A logic zero in a bit of the data direction register (DDRA and DDRB) causes the corresponding pin of the I/O port to act as an input. A logic one causes the corresponding pin to act as an output. The voltage on any pin programmed as an output is determined by the corresponding bit in the output register (ORA and ORB).

Data is read directly from the PA pins during a peripheral read operation. Thus, for a PA pin programmed as an output, the data transferred into the processor will be the same as the data in the ORA only if the voltage on the pin is allowed to be ≥ 2.4 volts for a logic one and ≤ 0.4 volts for a zero. If the loading on the pin does not allow this, then the data resulting from the read operation may not match the contents of ORA.

The output buffers for the PB pins are somewhat different from the PA buffers. The PB buffers are push-pull devices which are capable of sourcing 3ma at 1.5 volts. This allows for these pins to directly drive transistor circuits. To assure that the processor will read the proper data when performing a peripheral read operation, logic is provided in the peripheral B port to permit the processor to read the contents of ORB, instead of the PB pins as is the case for the PA port.

Interval Timer

The timer section of the SY6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 2.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, and interrupt flag is set to a logic "1." After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

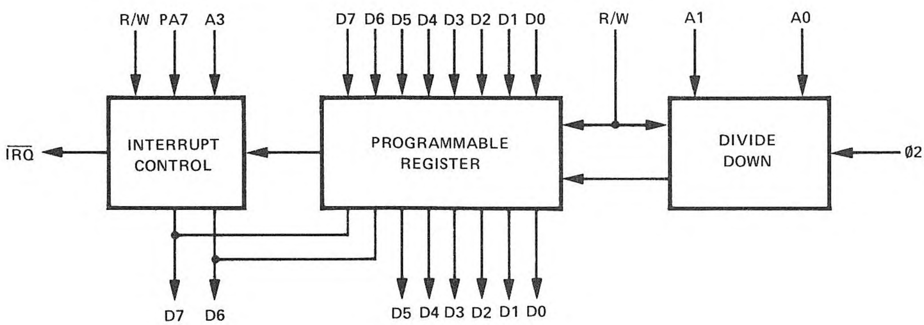
The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of $\overline{IRQ}$, i.e., $A_3 = 1$ enables $\overline{IRQ}$, $A_3 = 0$ disables $\overline{IRQ}$. In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set..This flag is cleared when the Timer register is either read from or written to by the processor. If $\overline{IRQ}$ is enabled by A3 and an interrupt occurs $\overline{IRQ}$ will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read	= 1 1 1 0 0 1 0 0
Complement	= 0 0 0 1 1 0 1 1
Add 1	= 0 0 0 1 1 1 0 0 = 28.

Figure 2. BASIC ELEMENTS OF INTERVAL TIMER

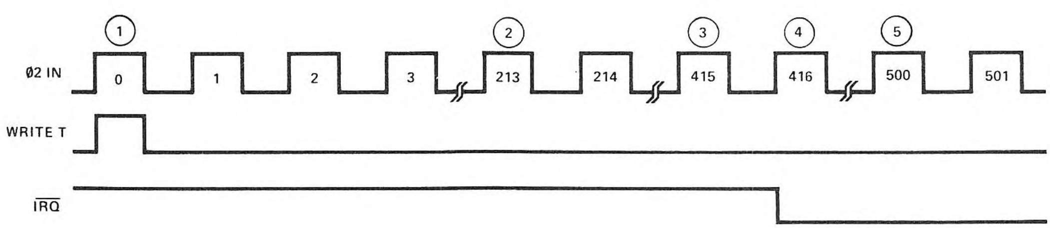


Thus, to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 3 illustrates an example of interrupt.

Figure 3. TIMER INTERRUPT TIMING



1. Data written into interval timers is 0 0 1 1 0 1 0 0 = 52_{10}
2. Data in Interval timer is 0 0 0 1 1 0 0 1 = 25_{10}

   $$52 - \frac{213}{8} - 1 = 52\text{-}26\text{-}1 = 25$$

3. Data in Interval timer is 0 0 0 0 0 0 0 0 = 0_{10}

   $$52 - \frac{415}{8} - 1 = 52\text{-}51\text{-}1 = 0$$

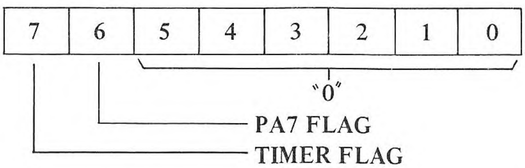
4. Interrupt has occurred at Ø2 pulse #416
   Data in Interval timer = 1 1 1 1 1 1 1 1
5. Data in Interval timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 1 0 0 = 84_{10}
   $84 + (52 \times 8) = 500_{10}$

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write operation.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits: the timer interrupt flag and the PA7 interrupt flag. When a read operation is performed on the Interrupt Flag Register, the bits are transferred to the processor on the data bus, as the diagram below, indicates.

Figure 4. INTERRUPT FLAG REGISTER



The PA7 flag is cleared when the Interrupt Flag Register is read. The timer flag is cleared when the timer register is either written or read.

ADDRESSING

Addressing of the SY6532 is accomplished by the 7 addressing pins, the $\overline{RS}$ pin and the two chip select pins CS1 and $\overline{CS2}$. To address the RAM, CS1 must be high with $\overline{CS2}$ and $\overline{RS}$ low. To address the I/O and Interval timer CS1 and $\overline{RS}$ must be high with $\overline{CS2}$ low. As can be seen to access the chip CS1 is high and $\overline{CS2}$ is low. To distinguish between RAM or I/O Timer the $\overline{RS}$ pin is used. When this pin is low the RAM is addressed, when high the I/O Interval timer section is addressed. To distinguish between timer and I/O address line A2 is utilized. When A2 is high the interval timer is accessed. When A2 is low the I/O section is addressed. Table 1 illustrates the chip addressing.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, the PA7 pin can function as an edge sensitive input. In this mode, an active transition on PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, and providing the PA7 interrupt is enabled, the $\overline{IRQ}$ output will go low.

Control of the PA7 edge detecting logic is accomplished by performing a write operation to one of four addresses. The data lines for this operation are "don't care" and the addresses to be used are found in Figure 4.

The setting of the internal interrupt flag by an active transition on PA7 is always enabled, no matter whether PA7 is set up as an input or an output.

The $\overline{RES}$ signal disables the PA7 interrupt and sets the active transition to the negative edge-detect state. During the reset operation, the interrupt flag may be set by a negative transition. It may, therefore, be necessary to clear the flag before its normal use as an edge detecting input is enabled. This can be achieved by reading the Interrupt Flag Register, as defined by Figure 4 immediately after reset.

I/O Register - Timer Addressing

Table 1 illustrates the address decoding for the internal elements and timer programming. Address line A2 distinquishes I/O registers from the timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the "divide-by" matrix. This decoding is defined in Table 1. In addition, Address A3 is used to enable the interrupt flag to $\overline{IRQ}$.

Table 1 ADDRESSING DECODE

OPERATION	$\overline{RS}$	R/W	A4	A3	A2	A1	A0
Write RAM	0	0	–	–	–	–	–
Read RAM	0	1	–	–	–	–	–
Write DDRA	1	0	–	–	0	0	1
Read DDRA	1	1	–	–	0	0	1
Write DDRB	1	0	–	–	0	1	1
Read DDRB	1	1	–	–	0	1	1
Write Output Reg A	1	0	–	–	0	0	0
Read Output Reg A	1	1	–	–	0	0	0
Write Output Reg B	1	0	–	–	0	1	0
Read Output Reg B	1	1	–	–	0	1	0
Write Timer							
÷ 1T	1	0	1	(a)	1	0	0
÷ 8T	1	0	1	(a)	1	0	1
÷ 64T	1	0	1	(a)	1	1	0
÷ 1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	–	(a)	1	–	0
Read Interrupt Flag	1	1	–	–	1	–	1
Write Edge Detect Control	1	0	0	–	1	(b)	(c)

NOTES: – = Don't Care, "1" = High level (≥2.4V), "0" = Low level (≤0.4V)

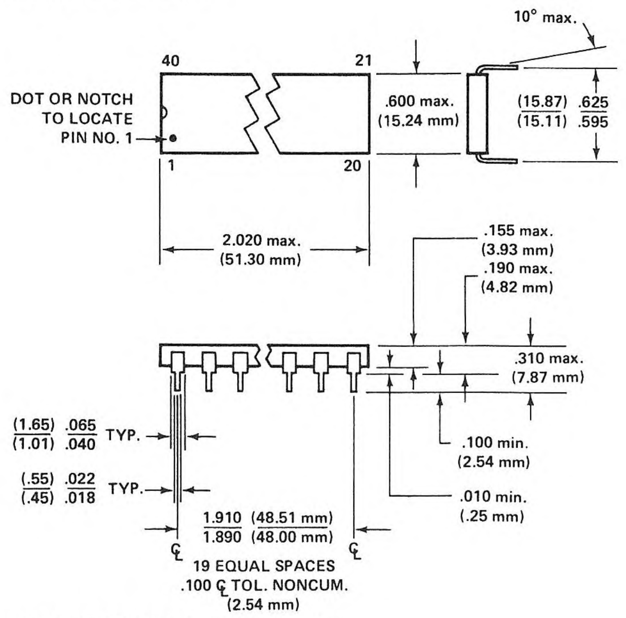
(a) A3 = 0 to disable interrupt from timer to $\overline{IRQ}$
A3 = 1 to enable interrupt from timer to $\overline{IRQ}$

(b) A1 = 0 to disable interrupt from PA7 to $\overline{IRQ}$
A1 = 1 to enable interrupt from PA7 to $\overline{IRQ}$

(c) A0 = 0 for negative edge-detect
A0 = 1 for positive edge-detect

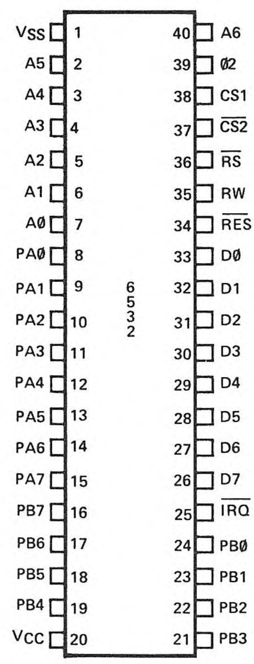
MICRO-PROCESSORS

PACKAGE OUTLINE



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

PIN DESIGNATION



System 65 Microcomputer Development System

Synertek®

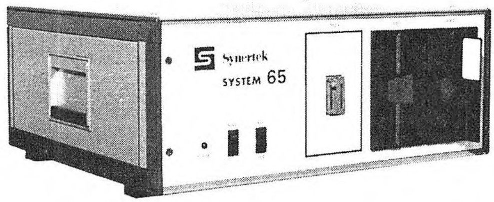
SYSTEM 65, the fully integrated microcomputer development system, built for expansion. START WITH IT, GROW WITH IT, STAY WITH IT.

SYSTEM 65

SYSTEM 65 is a new, easy to use, powerful, complete development system for the 6500 family of microcomputers. The basic configuration includes two **built-in mini-floppy disc drives,** 16K bytes of user memory and 16K bytes of resident operating system. Monitor commands are self-prompting whenever memory, peripheral, or disk file assignment is required. Text editor provides line, string, and character editing functions. A resident two-pass assembler and dynamic debug package complete the operating system. Both source and object code may be maintained in memory for fast editing, assembling, and checkout. Since the total monitor, editor debugger and assembler are resident in ROM, 100% of the disk storage and drive utilization is available to the user. The mini-floppy diskettes may be used as storage for source and object code and documentation. Each diskette has the capacity for 78K bytes of information in a maximum of 60 files.

SYSTEM 65 supports a variety of terminals with serial data from 110 baud to 9600 baud. Connectors are provided for both RS-232C and current loop interfacing. Reader ON/OFF signals and RTS/CTS control signals are standard. Included is a parallel port providing automatic control to high speed printers, such as Diablo, Centronics, and Tally.

FUTURE GROWTH is the key to the SYSTEM 65 architecture and design philosophy. SYNERTEK realizes that requirements change and therefore we want the System to grow with you. That is why the System has been incorporated with extra card slots for systems expansion.



GROWTH IS IN THE CARDS. In coming months the following new optional printed circuit cards will become available: PROM Memory Module, PROM Programmer, ADD-ON Memory, System Evaluator Module and Card Extenders.

SYNERTEK is aware that major enhancements will be provided by the users themselves in the form of user-generated software. That's why SYNERTEK has provided the flexible and versatile tools necessary to promote efficiency and productivity. Our DEBUG Monitor provides eight (8) software breakpoints, one hardware breakpoint with Scope Sync, a single-step feature, and a versatile TRACE output with OP Code mnemonics and Symbolic names. Other DEBUGGER features include Execution Path History, Register and memory display, as well as memory write protect. The System 65 resident text editor will provide the users with facilitated control at their fingertips.

The resident two-pass Assembler provides the programmer with powerful software tools. The Assembler gives the user control of the output which may optionally be spooled to the diskettes or print out only error messages or list the entire program. Errors in listings are "chained" together and highlighted by arrows. The user may optionally relocate the code to another location. A powerful link capability is also provided which will allow multiple files on different media to be treated as a single assembler.

MICRO-PROCESSORS

STANDARD PERIPHERAL INTERFACES

The System 65 offers the user the option to incorporate his own set of standard peripheral interfaces. The user then has the ability to place units of their own choosing and familiarity onto the system. The RS-232 port provides the capability for the placement of most Keyboard Printers or Display Terminals onto the System 65. If a high speed printer is required the parallel port connector located on the rear panel of the unit provides that interface flexibility.

EASE OF USE is a major feature of the System 65. The front panel controls are minimal consisting of a RESET Switch, RUN/SINGLE-STEP Switch and a "power on" indicator. System operation is straight forward with the majority of command functions being entered from the terminal. A PROM socket conveniently located on the front panel allows programming of 2708/2716 erasable PROMS.

System 65

KIM-1 Microcomputer Development Board

For: Educators/Students/Hobbyists/Engineers - - - for you!

Synertek®

MICROPROCESSOR APPLICATIONS

- Experimentation / Training / Engineering / Prototyping / Instrumentation / Testing

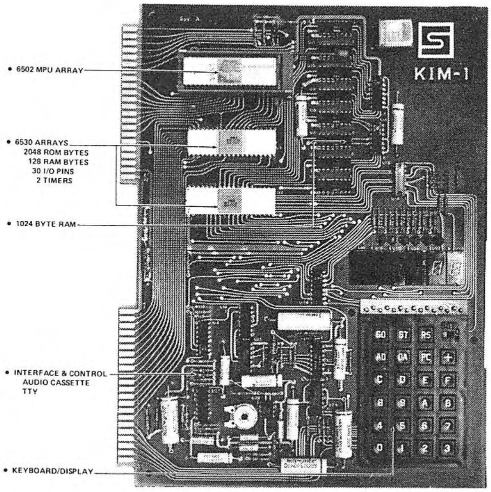
FEATURES

- Complete Fully-integrated, Microcomputer Development Board
- Ready-to-use (user merely provides the power)
- Multiple on-board Interval Timer
- 23-Key on-board Keyboard (including 6 function keys)
- 6-Digit on-board hexadecimal LED Display
- ROM-Resident operating program
- 1024 Bytes of Static Random access memory for data and program storage (Expandable to 65,536 bytes)
- High speed, high performance, 6502 Microprocessor, with powerful instruction set.
- Built-in Interfaces
  - Low Cost Audio Cassette
  - Full Duplex Teletype (20 mA loop)
  - Paper Tape Punch/Paper Tape Reader
- Connector included to interface to external equipment.
- Complete Documentation
  Manuals include: User, Programming, and Hardware Manual; Full Wall-Size Schematics.
- Full 90 day warranty against defects in materials and workmanship.
- Any table or counter top becomes a work bench for the KIM-1.
- Interface provided for Bus expansion.

GENERAL DESCRIPTION

- The KIM-1 Microcomputer Module is a fully integrated development board, that will allow the first-time computer user "hands-on" experience within minutes after unpacking the unit.

A 5-volt power supply is all the user must supply to operate with the basic system. (12 volts are required if an audio cassette recorder is used.)



By following the easy-to-read, easy-to-understand USER'S MANUAL, supplied with each unit, the KIM-1 user will be guided through the use and understanding of Machine Language Programming and its relationship to the on-board microprocessor family. By using Machine Language Programming rather than higher-level language, the user achieves a better grasp and familiarization with both the microprocessor hardware and microprocessor system design, as he is closer to the inner workings of the system.

As the basic operating program is resident in on-board ROM, the user has at his disposal nearly 1024 bytes of **Static RAM** (expandable with additional memory). The KIM-1 is unique in that it allows the user to operate the system without the addition of any external peripherals. The KIM-1's advanced design, however, provides a direct interface to any low cost AUDIO CASSETTE RECORDER, which can then be used for file creation and storage. Other standard on-board interfaces include a 20-mA interface to a model 33 teletype (optionally equipped with paper tape reader and paper tape punch).

MICRO-PROCESSORS

MEMORY and I/O EXPANSION

In the KIM-1 system, the management of input/output data is handled exactly the same as transfers to or from any other memory location in the system. There are no instructions dealing specifically with input/output transfers. Instead, transfer of data is accomplished by reading from or writing to registers connected to the data bus and to I/O pins in specific I/O interface devices. These registers have a specific address in the system just as does any other memory location. Therefore, when speaking of expanding the memory of the KIM-1 system, we are defining the methods of expanding both the real memory (RAM, ROM, PROM, etc.) as well as the I/O ports, since they are treated alike as far as address assignments are concerned.

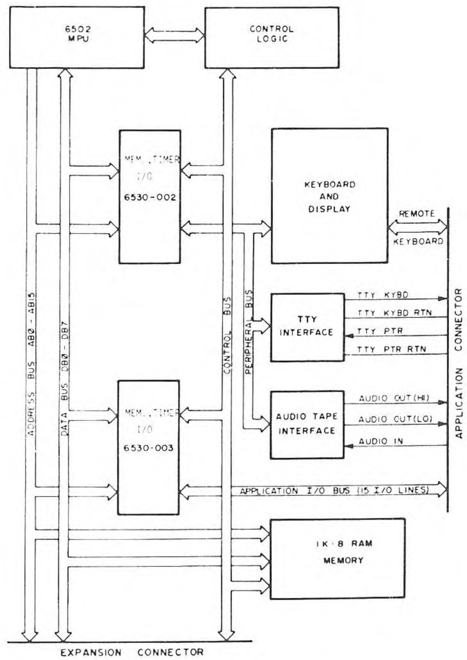
USING THE KIM-1

Stand-alone microcomputer: With the addition of a user-provided 5-volt power supply, the KIM-1 becomes a functional stand-alone microcomputer development system. In this configuration the user can select any Memory Addresses; Read/Modify Data, and execute or single-step programs.

Audio Tape Cassette: By providing a 12-volt power supply capability, together with any audio cassette recorder the user will have enhanced his system to include low-cost File Capability and External Memory Store. The KIM-1 user can Create Files, Block Data into Records on tape from KIM-1 Memory, Read Data records from tape into KIM-1 Memory (with error detection). The user can now maintain a **library** of pre-recorded programs. As the use of Audio Cassette recorders allows VOICE messages to be interspersed with Data records, by the single installation of an earphone or speaker, the user can have "Voice" messages automatically guide any operator through operation of a pre-recorded program.

TELEPRINTER INTERFACE: The standard 20-mA Teleprinter interface which is on-board KIM-1 allows for the easy installation of a Model 33 Teletype, or equivalent typeprinter. Once interfaced, the user can now LIST programs, and maintain permanent records of user's data. The use of the full Alpha-numeric keyboard expands the character set available to the user. The paper tape reader/punch options allow the user alternate methods for storing programs and data. The KIM-1 automatically adjusts for a variety of baud rates.

MICRO-PROCESSORS



KIM-1 Block Diagram

SPECIFICATIONS

Operating Temp. Range	10° - 40°C
Power Supply Req.:	+5 volts ±5% @ 1.2 amps
If audio tape option:	+12 volts ±5% @ 0.1 amps
Board Size	10¾" x 8" x 1"
Connectors	Two 44-pin edge connectors (one external connector included)

Timekeeping Products

Seven Function LCD Watch Circuit (Hours, Minutes, Seconds, Month, Date, Day, Leap Year)

Synertek®

SY5001

WATCH PRODUCTS

- Single Button Operation (Display And Set)
- Six Digit Display (Two Alpha-Numeric)
- Automatic Calendar Update
- 12/24 Hour Display and European Date Option
- 32768 Hz Crystal Oscillator
- Silicon Gate C-MOS Technology

GENERAL DESCRIPTION

The Synertek SY5001 is a single button seven function low power CMOS watch circuit which counts and displays: seconds, minutes, hours, date, days of week, months and leap year. It is designed to drive a six digit, nine segment alpha-numeric liquid crystal (LCD) display.

This circuit has a bonding pad option that allows watch operation in the 12 hour counting system with AM/PM identification or alternative operation in the 24 hour counting system with the symbol HR displayed instead of AM/PM. 12 hour operation displays month, date, day, in that order, from left to right. 24 hour operation causes reversal of the display to show date, month, and day for European watch applications.

The SY5001 incorporates several features which simplify module design. The chip provides two outputs PULSE and $\overline{\text{PULSE}}$ for use with an external voltage doubler or tripler circuit. Button is activated when it touches the case. The case polarity (0.0V or -1.5V) is selected by the manufacturer. A bonding pad will relate this voltage to the internal circuit. No electrical connection is required to substrate (back of the die) so die mounting can be done using non-conductive material.

DISPLAY AND TIME SET

The display normally shows hours, minutes and seconds continuously. A button push causes display of month, date and day. This display will remain as long as the button is held pushed. Two seconds after release the display will return to its normal condition.

Pushing and releasing the button five times (with less than two seconds between pushes) puts the watch into the first set mode. The requirement for five pushes insures that the set mode will not be entered accidentally. Once the watch has entered the first set mode (months set), it will automatically advance through each subsequent set mode (date, day, hour, and minute). The watch will remain in each set mode for six seconds unless the button is pushed. If the button is pushed and held during any set mode, then the displayed function will advance continuously at a 1 Hz rate. A single push and release of the button in the set mode will advance the displayed function by one count. If the button is not pushed for six seconds during a set mode, then the subsequent set mode will automatically appear.

The watch will return to its normal display condition after the minutes set mode. If the button was pushed during the minutes set mode, the next button push will clear the seconds to zero and suppress counting until the button is released.

CIRCUIT TESTING

Additional pads are provided for ease of testing. The TEST input will speed the counting sequence. The DT input when activated will turn on all segments of all digits for display testing. All internal counters are reset to the initialized condition (MCL) by activating DT and BUT inputs simultaneously. Additional test details are available from Synertek.

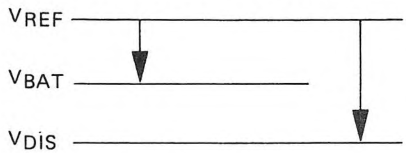
TIMEKEEPING PRODUCTS

Synertek® • P.O. Box 552 • Santa Clara, CA 95052 • Telephone (408) 984-8900 • TWX: 910-338-0135

J-5K-10/77

DEVICE SPECIFICATIONS

SUPPLY VOLTAGE DEFINITION



V_{REF}: Reference voltage - positive battery terminal.

V_{BAT}: Negative battery terminal.

V_{DIS}: Negative display operating voltage.

ABSOLUTE MAXIMUM RATINGS*

Input and Output Voltages	+.3V to -10V
Supply Voltages	+.3V to -10V
Storage Temperature	-55°C to 100°C

* Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions not specified in section 3.0 is not implied. Extended periods of exposure to absolute maximum ratings may affect device reliability.

ELECTRICAL AND OPERATING CHARACTERISTICS

T_A = -20°C to 60°C, V_{BAT} = V_{REF} -1.5V, V_{DIS} = V_{REF} -3.0V unless otherwise specified.

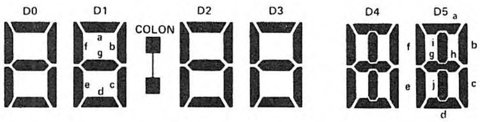
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{BAT}	Battery Operating Voltage	-1.35		-1.60	V	Note 1
I_{BAT}	Average Supply Current		-1.5	-3.0	μA	V_{BAT} = -1.6V T_A = 25°C Note 1
V_{DIS}	Display Operating Voltage	-2.2		-4.5	V	Note 1
I_{DIS}	Average Supply Current		-0.3	-0.5	μA	V_{DIS} = -4.5V T_A = 25°C Note 2
I_{IN} (1)	Input Current (TEST, DT, BUT)		0.5	1.5	μA	V_{BAT} = 1.6V, CASE = V_{IN} = V_{REF}, T_A = 25°C
I_{IN} (0)	Input Current (BUT)		-0.5	-1.5	μA	CASE = V_{BAT} = V_{IN} = -1.6V, T_A = 125°C
V_{PULSE} (1)	Output Voltage (PULSE, $\overline{\text{PULSE}}$)		V_{REF}		V	V_{BAT} = -1.4V
V_{PULSE}(0)	Output Voltage (PULSE, $\overline{\text{PULSE}}$)		V_{BAT}		V	V_{BAT} = -1.4V
f_{PULSE}	Output Frequency (PULSE, $\overline{\text{PULSE}}$)		2048		Hz	50% duty cycle
I_L	Input Leakage (CASE, 12HR, OSC IN)		0.1	0.5	μA	V_{IN} = 1.6V, T_A = 25° Note 3

Note 1: Oscillator operating at 32768 Hz. 12 HR and CASE inputs connected to V_{REF} or V_{BAT}, all other pins floating.

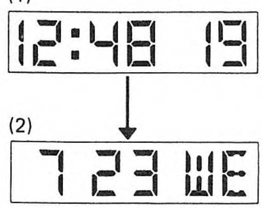
Note 2: All LCD segment outputs floating.

Note 3: OSC IN, CASE, 12 HR connect to V_{IN}, all other pins grounded.

DISPLAY DEFINITION



FUNCTIONAL DESCRIPTION



(1) Continuous display of hours, minutes, seconds and colon.

Push button once

(2) 2 sec display of month, date and day.

SET MODES

GENERAL

Set mode is entered by pressing button 5 times in succession. Flashing colon will appear on display until release of fifth button push. At release of fifth button push, first set mode is entered with present status of watch displayed with flashing colon. The next four set modes will be entered automatically at six second intervals. During the set intervals, button pushes will advance the time displayed and watch will stay in that set mode until six seconds has elapsed from last button push. If minutes were advanced during minutes set mode, seconds can be set and held at "00" for time synchronization if button is pushed and held once just after watch has advanced from minutes set mode to time of day. Release of button will start seconds counting from "00".

DESCRIPTION	TYPICAL DISPLAY	ENTERED BY
Initiating Set Mode	:	Button pushed 5 times (colon is flashing every second in all set modes)
Month and Leap Year Set	6: 4 MO	Release of 5th button push. Warning: if button is pushed during any of the following set modes the displayed time will be advanced.
Date Set	:29 CA	Automatically from above 6 seconds after any button release.
Day Set	: TH	Automatically from above 6 seconds after any button release.
Hour Set	10: AM	Automatically from above 6 seconds after any button release.
Minute Set	:34 MI	Automatically from above 6 seconds after any button release.
Hours - Min. - Sec.	10:34 00	If button was pushed during minutes set mode the first push of button will clear and hold seconds at zero.
Hours - Min. - Sec.	10:34 01	Release of first button push (seconds begin to count)

Note 1: Months and leap year (1 through 4) are shown during months set mode. In leap year (4) February has 29 days instead of 28. The year advances every time the month rolls from 12 back to 1.

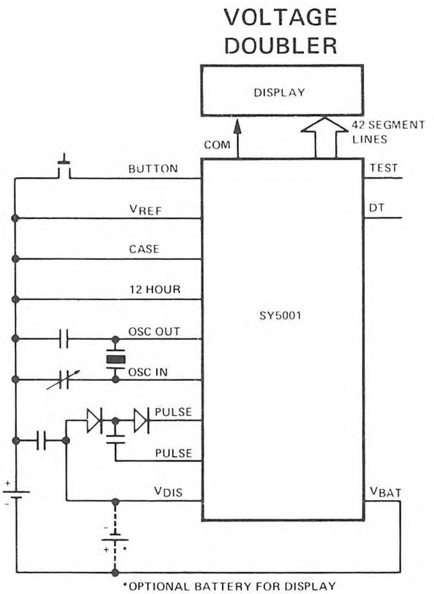
Note 2: 12 hour option shows AM or PM. 24 hour option shows HR instead.

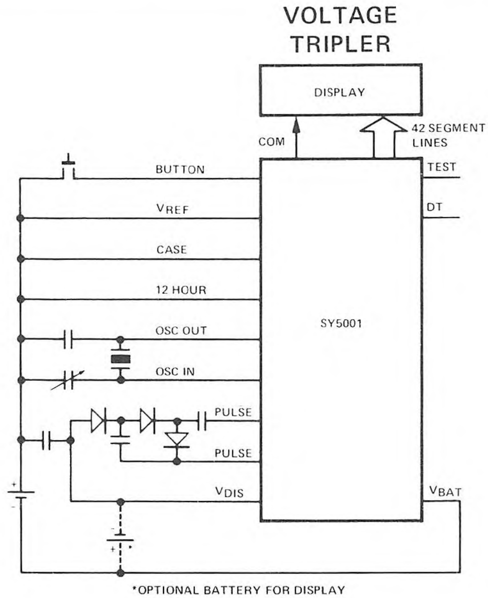
Note 3: Leading zeros in hours, date and month are blanked.

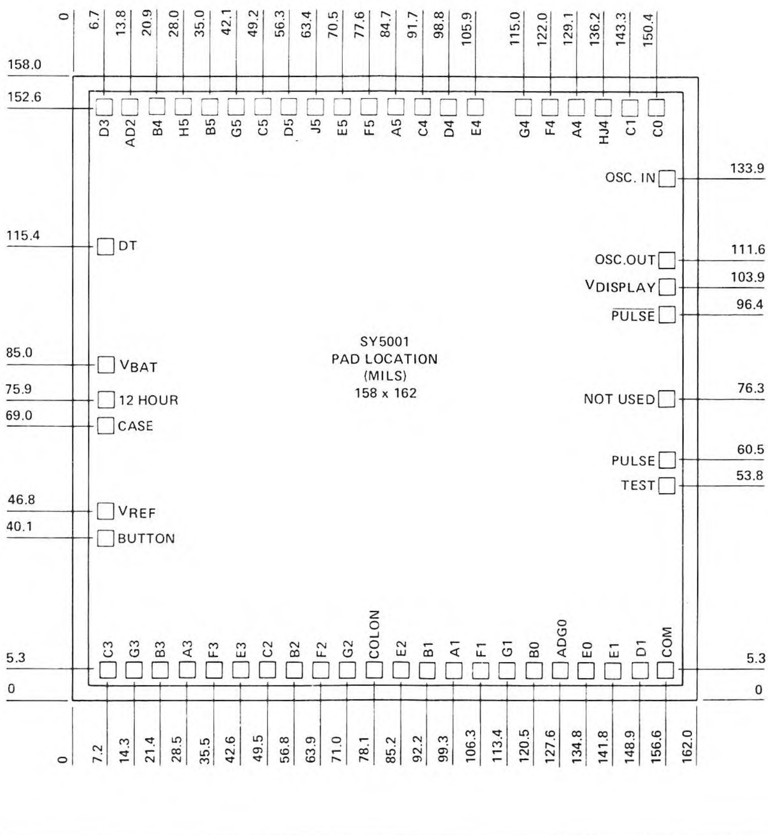
■ = Colon On

□ = Colon Flashing

TIMEKEEPING PRODUCTS







TIMEKEEPING PRODUCTS

Synertek®
3050 CORONADO DRIVE
SANTA CLARA, CA 95051
TELEPHONE (408) 984-8900
TWX: 910-338-0135

SY 5002

SEVEN FUNCTION LED WATCH CIRCUIT
(HOURS, MINUTES, SECONDS, MONTH, DATE, DAY, LEAP YEAR)

WATCH PRODUCTS

- SINGLE BUTTON OPERATION (DISPLAY AND SET)
- SIX DIGIT DISPLAY (TWO ALPHA-NUMERIC)
- ON CHIP SEGMENT DRIVERS
- AUTOMATIC CALENDAR UPDATE
- 12/24 HOUR DISPLAY OPTION
- EUROPEAN DATE OPTION
- TWO OPTIONAL BRIGHTNESS CONTROLS
- 3V BATTERY OPERATION
- NON-FLICKER 170 HZ MULTIPLEX DISPLAY RATE
- INTERDIGIT SEGMENT AND DIGIT BLANKING
- CRYSTAL FREQUENCY 32, 768 HZ
- SILICON GATE C-MOS TECHNOLOGY

GENERAL DESCRIPTION

The Synertek 5002 is a single button seven function low power CMOS watch circuit which counts and displays; seconds, minutes, hours, date, days of the week, months and leap year. It is designed to drive a six digit, nine segment alpha-numeric light emitting diode (LED) display.

This circuit normally operates in the 12 hour counting system with AM/PM identification. A control pad allows 24 hour counting with the symbol HR instead of AM/PM. Also the circuit normally displays month, date, day, in that order, from left to right. A control pad allows reversal of the display to show date, month, day, for European watch applications.

The brightness of the display may be selected by the optional use of two control pads OP1 and $\overline{AL}$. Normally the display drivers activate each of the six digits sequentially giving a duty cycle of 1/6. One of the control pads can be used to shorten the width of the digit select pulse by a factor of 2. This will reduce the average display current by a factor of 2 and is useful for higher efficiency display and to conserve battery life. The other control pad shortens the width of the digit select pulse by a factor of 4. This pad can be driven by a phototransistor to reduce the display brightness in low ambient light conditions.

Additional pads are provided for ease of testing. $\overline{LT}$ is used to turn all segments during any display mode. $\overline{MCL}$ is used to initialize all FF's on the chip. $\overline{Test}$ is used to speed up the counting sequence. 1024 output provides a 1024 Hz pulse for trimming the oscillator input capacitor. Additional testing information is available from Synertek.

DISPLAY AND TIME SET

The display is normally blank. The first button push causes display of hours, minutes, seconds. A second button causes display of month, date, and day. Either display will remain as long as the button is held pushed, two seconds after release, display will return to its normal blank condition.

Pushing and releasing the button five times (with less than two seconds between pushes) puts the watch in the first setting condition or "set mode". The requirement for five pushes insures the "set mode" will not be entered accidentally. Once the watch has entered the first set mode (months) it will automatically advance through each subsequent set mode (calendar, day, hour and minute) remaining in each mode for 4/6/8 six second. If the button is pushed during any set mode the displayed time will be advanced. If the button is then not pushed for six seconds the subsequent "set mode" will automatically appear.

The watch will return to its normal blank condition after the minutes set mode. If the button was pushed during the minutes set mode, the next button push (to display hours, minutes, seconds) will clear the seconds to zero until the button is released.

TIMEKEEPING PRODUCTS

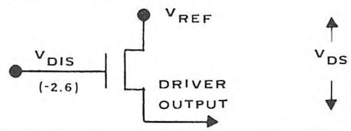
ELECTRICAL SPECIFICATIONS

1.0 VOLTAGE DEFINITION

V_{REF}: Reference voltage, most positive voltage - connected to chip substrate (OV)

V_{BAT}: Battery voltage (−2.6V to −3.2V)

V_{DS}: Output voltage drop



2.0 ABSOLUTE MAXIMUM RATINGS

V_{BAT}	+ .3 to −4V
All inputs	+ .3 to −4V
Operating temp.	−20°C to +60°C
Storage temp.	−55°C to 100°C

3.0 ELECTRICAL CHARACTERISTICS (T_A= 25°C)

V_{BAT} = −2.6V

Parameter	Min	Typ	Max	Unit	Condition
Digit output current	1.5	2.0		MA	V_{DS} = 1.1V
Segment output current	6	10		MA	V_{DS} = .95V
Digit or segment output leakage		1.0		µA	
Switch input current		3.0		µA	V_{IN} = V_{BAT}
1024 Output current		5.0		µA	
Total current (Display off)		1.5	10	µA	V_{BAT} = −3.0B

SET MODE ADVANCE FEATURE

A unique feature of this circuit is the ability to "single step" the count when setting time. When the circuit is in one of the time setting modes the button has two functions. When pushed repeatedly it will "single step" increasing the count, once for each push. If the button is pushed and not released for one second, the count will commence to automatically increase (roll) twice per second. The "single step" feature will then return whenever the button is released.

OPTIONS VIA BONDING

Pad Name	Pad Condition	Option
12 HR	Bonded to VR	12 Hour operation (AM,PM)
12 HR	Bonded to VB	24 hour operation (HR)
MDO	Not Bonded	Month - Date - Day Display
MDO	Bonded to VB	Date - Month - Day Display
OP1	Not Bonded	Brightest Display 15.6% Duty Cycle
$\overline{AL}$	Bonded to VB or transistor on	
OP1	Not Bonded	4.2% Duty Cycle
$\overline{AL}$	Not Bonded or transistor off	
OP1	Bonded to VB	8.3% Duty Cycle
$\overline{AL}$	Bonded to VB or transistor on	
OP1	Bonded to VB	Dimmest Display 2.1% Duty Cycle
$\overline{AL}$	Not Bonded or transistor off	

TYPICAL EXTERNAL COMPONENTS

Crystal: Bulova WA - 32 - 10 - 2A
Display: Monsanto RV - 31 or Litronix RW - 62 (Alpha-numeric)
Drivers: Litronix LBC - 1060

TIMEKEEPING PRODUCTS

OPERATING SEQUENCE

DESCRIPTION	ENTERED BY	TYPICAL DISPLAY
HOURS - MIN. - SEC.	FIRST PUSH OF BUTTON	10:34 57
MONTH - DATE - DAY	SECTION PUSH OF BUTTON	6 27TH
BLANK	FROM EITHER OF ABOVE STATES IF BUTTON NOT PUSHED FOR 2 SECONDS.	
BEGINNING SET MODE	BUTTON PUSHED 5 TIMES (COLON IS FLASHING EVERY SECOND IN ALL SET MODES)	:
MONTH AND LEAP YEAR SET	RELEASE OF 5TH BUTTON PUSH. WARNING: IF BUTTON IS PUSHED DURING ANY OF THE FOLLOWING SET MODES THE DISPLAYED TIME WILL BE ADVANCED.	6: 4 [1] MO
DATE SET	AUTOMATICALLY FROM ABOVE 6 SECONDS AFTER ANY BUTTON RELEASE.	:27CA
DAY SET	AUTOMATICALLY FROM ABOVE 6 SECONDS AFTER ANY BUTTON RELEASE.	: TH
HOUR SET	AUTOMATICALLY FROM ABOVE 6 SECONDS AFTER ANY BUTTON RELEASE.	10: AM [2]
MINUTE SET	AUTOMATICALLY FROM ABOVE 6 SECONDS AFTER ANY BUTTON RELEASE.	:34MI
BLANK	AUTOMATICALLY FROM ABOVE 6 SECONDS AFTER ANY BUTTON RELEASE.	
HOURS - MIN. - SEC.	IF BUTTON WAS PUSHED DURING MINUTES SET MODE THE FIRST PUSH OF BUTTON WILL CLEAR AND HOLD SECONDS AT ZERO.	10:34 00
HOURS - MIN. - SEC.	RELEASE OF FIRST BUTTON PUSH (SECONDS BEGIN TO COUNT)	10:34 01

NOTE 1: Months and leap year (1 through 4) are shown during months set mode. In leap year (4) February has 29 days instead of 28. The year advances everytime the month rolls from 12 back to 1.

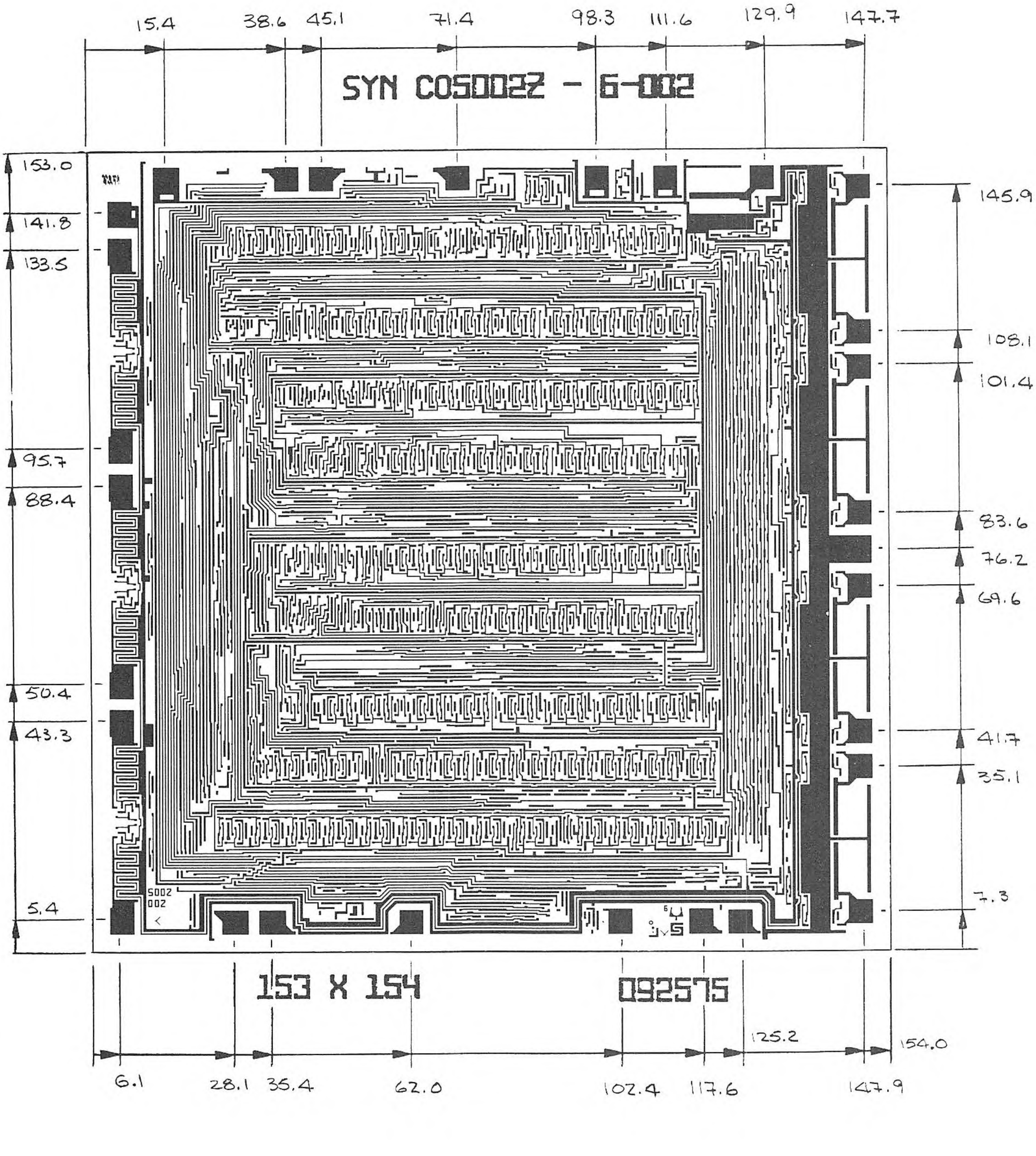
NOTE 2: 12 hour option shows AM or PM. 24 hour option shows HR instead.

NOTE 3: Leading zero's in hours, date, and month are blanked.

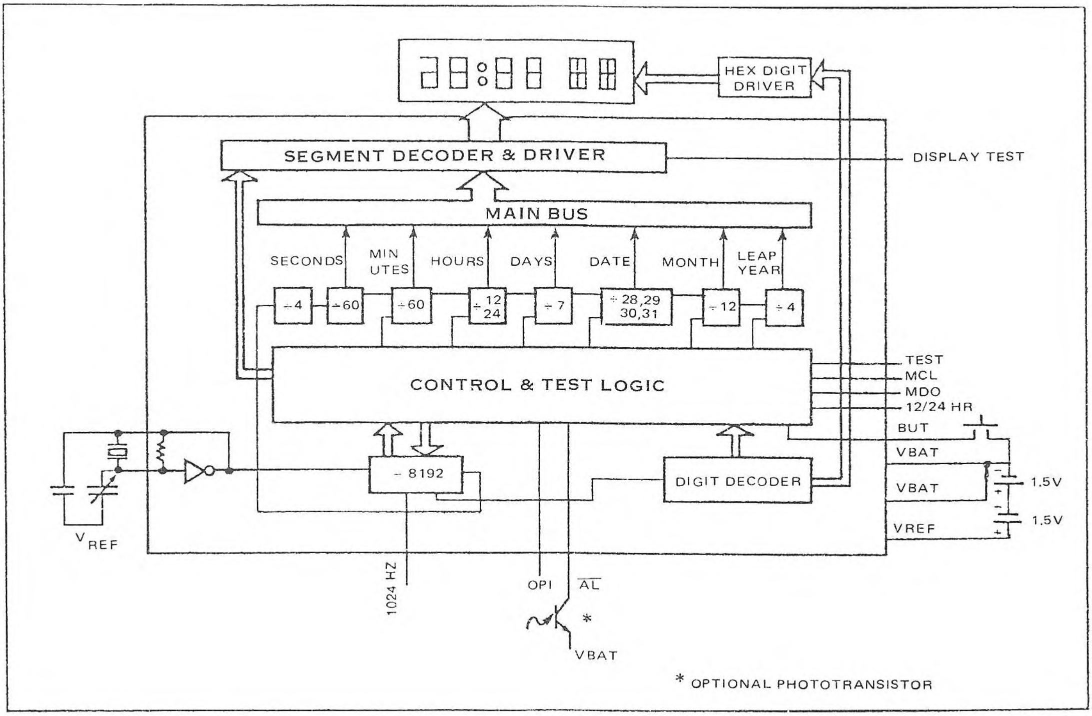
● = Colon on
○ = Colon Flashing

TIMEKEEPING PRODUCTS

CHIP DIMENSIONS



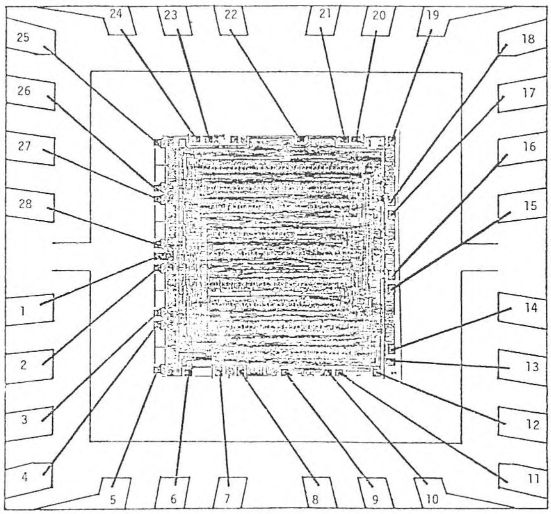
TIMEKEEPING PRODUCTS



TIMEKEEPING PRODUCTS

COMMENTS: PACKAGE MUST HAVE NO PIN TO DIE ATTACH PAD.
BONDING DIAGRAM TO BE USED FOR ENGINEERING PURPOSES ONLY.

PACKAGE 232,800



Scale 20:1

Basic Die Type 5002-002	Wire Bond 1.25 mil aluminum U.S.
Die Size X = 153 Y = 154	Die Attach Cavity 230 sq.
Process Flow [x] Standard 100,006	Die Attach Preform 60 x 60 min.
[ ] Process per	

PIN LIST

1.	VREF	21.	OSO	41.	
2.	SH	22.	OSI	42.	
3.	SC	23.	$\overline{BUT}$	43.	
4.	SJ	24.	$\overline{LT}$	44.	
5.	SD	25.	SF	45.	
6.	SE	26.	SG	46.	
7.	$\overline{MCL}$	27.	SA	47.	
8.	$\overline{AL}$	28.	SB	48.	
9.	MDO	29.		49.	
10.	OP1	30		50.	
11.	12/24 HR	31.		51.	
12.	V_{BAT}	32.		52.	
13.	V_{BAT}	33.		53.	
14.	D1	34.		54.	
15.	D2	35.		55.	
16.	D3	36.		56.	
17.	D5	37.		57.	
18.	D6	38.		58.	
19.	D4	39.		59.	
20.	$\overline{TEST}$	40.		60.	

Frequency Divider and Stepper Motor Driver

SY5008

WATCH PRODUCTS

Synertek®

- One Button Synchronization
- On Chip Seconds Hand Stepping Motor Driver
- Optional 1/12 Hz Output For Watches Without Seconds Hand
- Mask Programmable Output Polarity And Pulse Width
- 32768 Hz Crystal Frequency
- Low Power Oscillator Circuit And Front Dynamic Dividers
- On Chip Oscillator Capacitor And Feedback Resistor
- Single 1.5V Supply Voltage

The SY5008 divides a crystal oscillator frequncy of 32768 Hz to produce a two phase 1 Hz buffered output that can drive the seconds hand stepping motor of an analog watch. A two phase output of 1/12 Hz is available for watches without seconds hand and output pulse width and polarity can be selected by a metal mask option.

Low power operation is achieved by using a low current oscillator circuit and front dynamic dividers.

The oscillator capacitor and feedback resistor are on the chip to reduce external component count. A 1024 Hz or 512 Hz output (DIV) is provided to facilitate adjusting the external trimmer capacitor.

A test input is also provided on the chip to permit rapid testing of the device. On chip substrate connection is provided, which eliminates the need for conductive die attach epoxy.

AVAILABLE 5008 OPTIONS

1. Pulse Width (0.5 to 125 msec)
2. Output Polarity at Non-Active State [High (+V), Low (-V)]
3. Oscillator Output Adjustment Frequency (1024 Hz or 512 Hz)
4. Output Frequency (1 Hz or 1/12 Hz)

Available for sampling is the 5008 option 02 which incorporates the following:

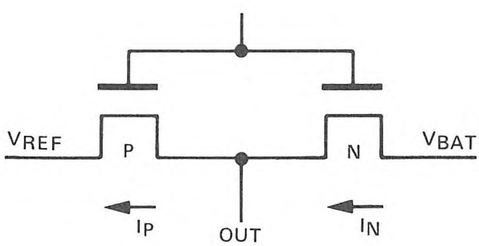
Pulse Width 35 msec
Output Polarity High (+V)
Oscillator Output Adjustment Frequency 1024 Hz
Output Frequency 1/12 Hz

VOLTAGE DEFINITION

V_{REF}: Reference voltage, most positive voltage connected to chip substrate (ØV)

V_{BAT}: Battery voltage

V_{DS}: Voltage drop across output drivers



ABSOLUTE MAXIMUM RATINGS

V_{BAT}	+.3 to -2V
All Inputs	+.3 to -2V
Operating Temperature	-20°C to +60°C
Storage Temperature	-55°C to +100°C

COMMENTS

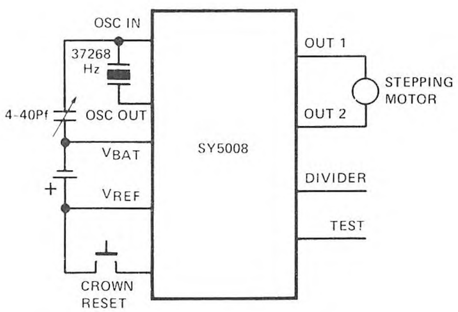
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

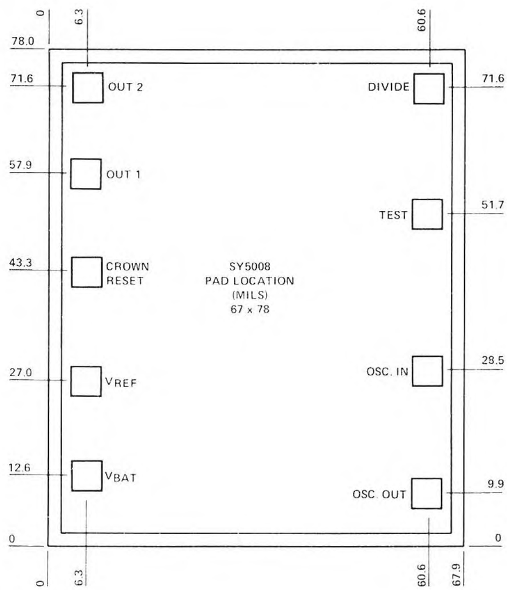
TIMEKEEPING PRODUCTS

ELECTRICAL CHARACTERISTICS

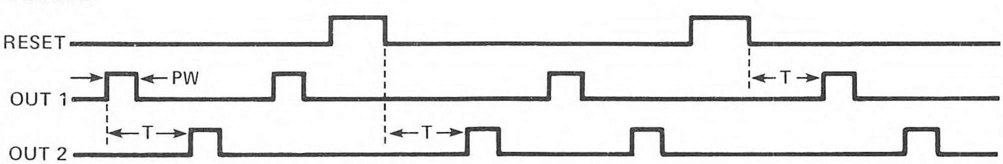
T_A = 25°C, V_{BAT} = 1.5V unless specified

Parameter	Min	Typ	Max	Unit	Condition
V_{BAT}	-1.35	-1.5	-1.6	V	
I_{BAT}		1	3	μA	Outputs Floating
I_P	-340			μA	V_{BAT} = -1.35; V_{DS} = .1V
I_N	+340			μA	V_{BAT} = -1.35; V_{DS} = .1V
Crown Input		.2		μA	V_{IN} = 0V
Test Input		.6		μA	V_{IN} = 0V
DIV		15		μA	
Output Pulse Width	0.5		125.0	msec	Metal Mask Programmable
Oscillator Feedback Resistor		10		MegΩ	
Internal Oscillator Capacitor		15		pF	Biased at 0.65V





TIMING



T = 1 sec or 12 sec
PW = Programmable 0.5ms to 125.0ms
Reset is inhibited during outputs.
Output activation sequence will be maintained after reset.

Multi-Function, Six Digit LCD Watch Circuit With Alarm, Three Stopwatch Modes, and Event Counter

SY5009A

Synertek®

WATCH PRODUCTS

BASIC FUNCTIONS

- Six Digit LCD display (2 alphanumerics)
- Low power (one 1.5V battery operation)
- On chip voltage doubler and tripler
- Hours/minutes/seconds
- Month/date/day
- 100 year calendar
  - Automatic leap year update
- 12 and/or 24 hour operation
- Complete stopwatch functions
  - Time accumulation (start/stop, start/stop . . . .)
  - Standard split
  - Taylor split
  - Seconds/100 or minutes/100 resolution
- Event counter
- Alarm
  - Hours/minutes - 24 hour alarm
  - 7 minutes snooze control
  - Momentary warning of pending alarm
  - Alarm output for either coil or ceramic resonator
- User adjustable frequency correction
- Single step and fast roll in set modes

The SY5009A is a six digit LCD drive chip containing the complete circuitry required for time display, chronograph/stop watch, event count and alarm functions. Additional functional flexibility is obtained by mask options allowing the customer to define a product most suitable for his unique requirements. The circuit is fabricated with Synertek's high density Silicon Gate CMOS process resulting in a reliable and cost effective product.

ADDITIONAL FEATURES

The following items may be programmed by a mask option:

- Order and number of set modes
- Crystal frequency
- European date option
- Stopwatch resolution (sec/100 or min/100)
- User selectable or mask preset 12/24 hour operation
- Month/date/day or promotional display
- Alarm frequency (250 H_Z, 500 H_Z, 1 KH_Z or 2 KH_Z)
- Alarm output polarity
- Positive or negative case
- Additional segment identifiers
  - Stopwatch mode indicator
  - Alarm indicator
  - Month/date/day or promotional indicator
- Leading zero suppression on hours, month and date display
- No rollover in set mode
- Debounce protection on all button inputs

Five basic watches may be obtained by using only certain combinations of the four buttons available as follows:

FEATURES	BUTTONS REQUIRED
Time + Date	Time (T), Set (S)
Time + Date + Stopwatch (no split)	Time (T), Set (S), Start/Stop (S/S)
Time + Date + Alarm	Time (T), Set (S), Split (C)
Time + Date + Stopwatch (with split)	Time (T), Set (S), Split (C), Start/Stop (S/S)
Time + Date + Alarm + Stopwatch (with split)	Time (T), Set (S), Split (C), Start/Stop (S/S)

TIMEKEEPING PRODUCTS

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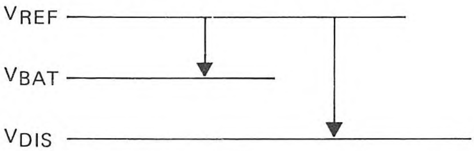
B-15K-10/77

ELECTRICAL AND OPERATING CHARACTERISTICS

SUPPLY VOLTAGE DEFINITION



V_{REF}: Reference Voltage - positive battery terminal
V_{BAT}: Negative battery terminal
V_{DIS}: Negative display operating voltage

ABSOLUTE MAXIMUM RATINGS*

Input and Output Voltages	+.3 to -5V
Supply Voltages	+.3 to -5V
Storage Temperature	-55°C to 100°C

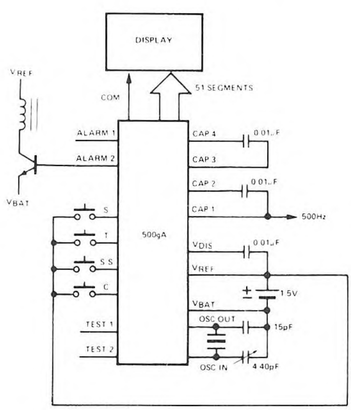
* Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions not specified in section 3.0 is not implied. Extended periods of exposure to absolute maximum ratings may affect device reliabity.

T_A = 25°C, V_{BAT} = V_{REF} -1.5V, V_{DIS} = V_{REF} -3.0V unless otherwise specified.

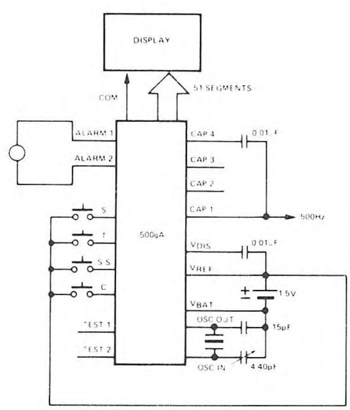
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
V_{BAT}	Battery operating voltage	-1.35	-1.5	-1.6	V	
I_{BAT}	Supply current		-3.0	-5.0	μA	Oscillator running at 32768 Hz. All inputs and outputs floating.
V_{DIS}	Display operating voltage	-2.2	-3.0	-5.0	V	
I_{DIS}	On chip display current		-1.0		μA	V_{DIS} = -4.5V
I_L, O_L	Inputs/outputs leakage			1.0	μA	
I_C	Input pull-up current		1.0		μA	Inputs activated
V_D	Doubler voltage		-3.0		V	
V_T	Tripler voltage		-4.5		V	
V_A	Alarm output voltage		1.0		V	
I_A	Alarm output current		1.0		mA	V_A = 1.0V

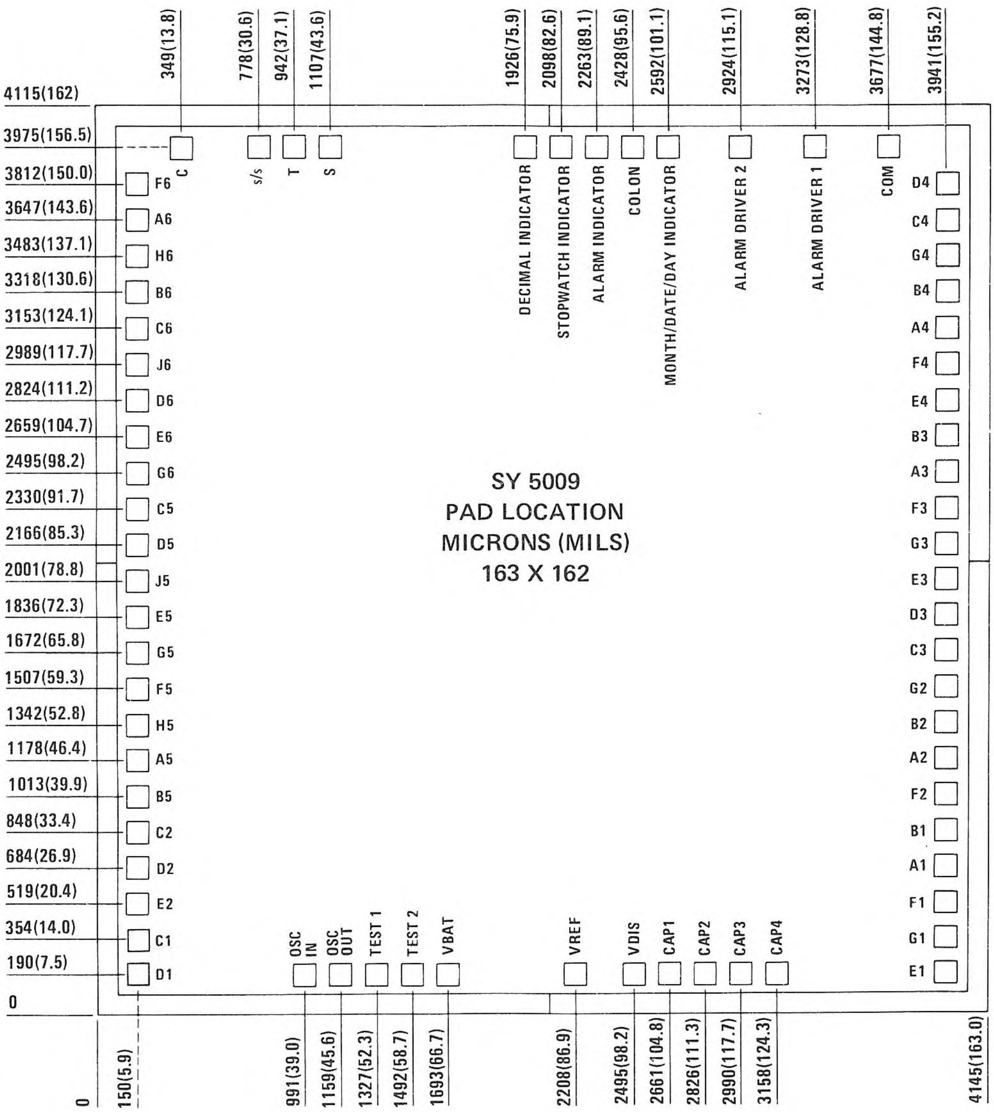
SYSTEM CONNECTIONS

VOLTAGE TRIPLER AND COIL ALARM



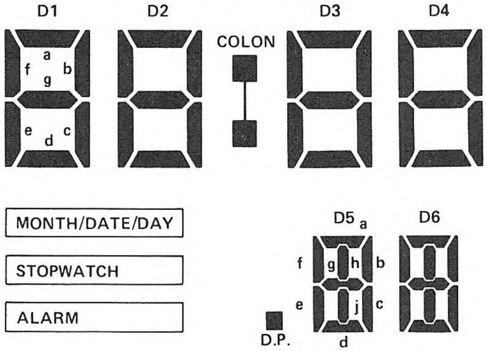
VOLTAGE DOUBLER AND CERAMIC RESONATOR ALARM





TIMEKEEPING PRODUCTS

DISPLAY DEFINITION



FUNCTIONAL DESCRIPTION

Basic Time Functions

(1)

Continous display of hours, minutes, seconds, and colon. Alarm indicator will be shown only when buzzer is armed (see: Alarm Functions).

T

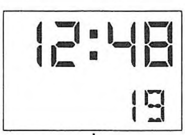
Push T button and hold

(2)

For as long as T is held, continous display of month, date, weekday and month/date/weekday identifier. Alarm identifier will be shown only when alarm is armed. As soon as T is released, the display will revert to (1).

Alarm Functions:

(3)

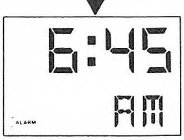


Continous time display

Push T button twice and hold

T-T

(4)

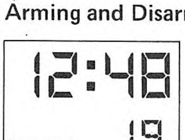


Continous display of alarm set time in hours and minutes, AM/PM or HR indicator (on digits 5 and 6), and colon. Alarm indicator is flashing regardless of whether or not the buzzer is armed.

As soon as T is released, the display will revert to (3).

Arming and Disarming the Buzzer

(5)



During the display mode, if the alarm indicator is on the alarm mechanism (coil or piezoelectric disk) is armed and alarm will sound when preset time is reached.

C

Push C button once

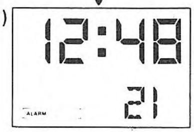
(6)

Alarm indicator is turned off and buzzer is disarmed. Alarm will not go off at the preset time.

Push C button once

C

(7)



Alarm indicator is on again. Buzzer is armed and alarm will sound at preset time. Continous pushes of button "C" will toggle the watch between states (6) and (7).

At the preset time, and with buzzer armed, the alarm will sound in the following manner:

60 seconds:

1 second beep - a warning that alarm is about to go off
7 seconds silence - allowing the user to turn off the alarm before it goes off

If alarm was not turned off during the 7 seconds interval

For a total of 52 seconds:

1 second on
1 second off
1 second on
1 second off
1 second on
1 second off
1 second on
1 second off
1 second on

At any time after the first beep is heard, the user has three courses of action:

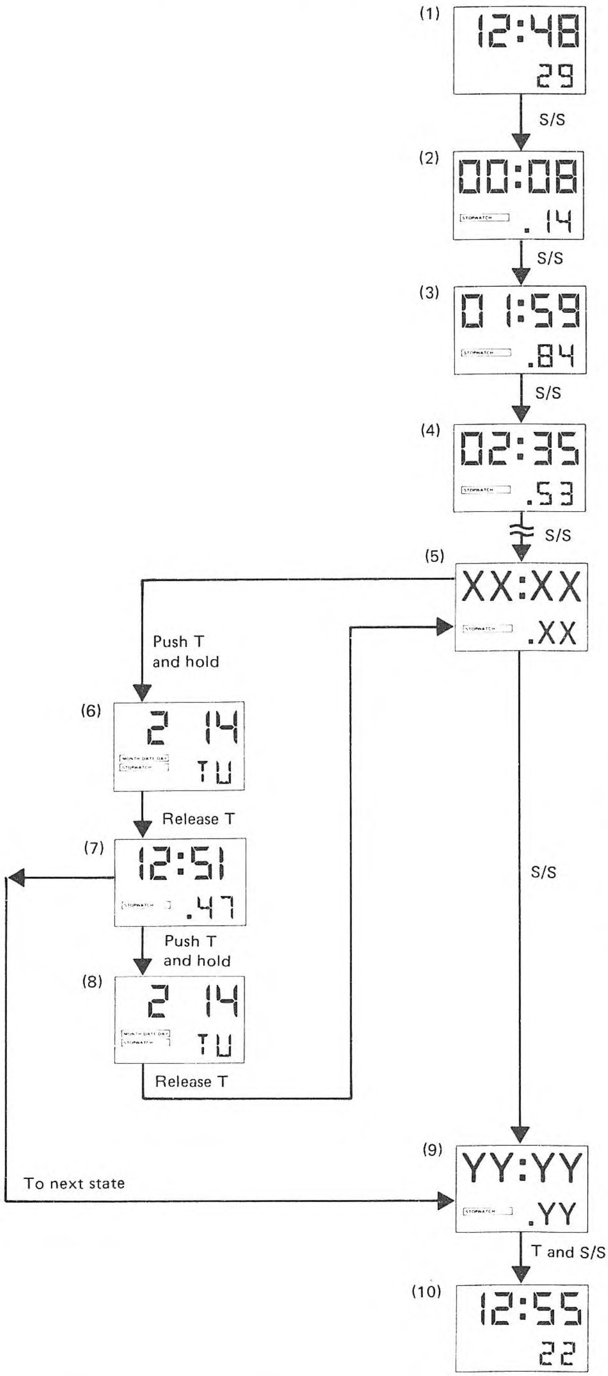
1. Push button T once	This will activate snooze control. The alarm sound will stop and the alarm sequence will repeat 7 minutes later. This snooze sequence can be repeated every 7 minutes for as many times as desired.
2. Push button C once	Alarm sequence is terminated and the buzzer is disarmed.
then	
Push button C again	Buzzer rearmed. Alarm will resound 24 hours later.
3. No action	The alarm mechanism will complete the 60 seconds sequence and will then turn itself off. Next alarm sequence will sound 24 hours later, or at a newly preset alarm time.

CUSTOM

STOPWATCH FUNCTIONS

Basic Stopwatch Mode

Basic stopwatch (no split) capability is achieved through addition of the start/stop (S/S) button.



(1) Normal time of day display – hours/minutes/seconds.

Push S/S button once (start)

(2) Stopwatch starts counting. Display shows running elapsed time in minutes, seconds and seconds/100. Stopwatch indicator is on.

Push S/S button once (stop)

(3) Stopwatch and display are stopped. Display is showing elapsed time.

Push S/S button once (start)

(4) Stopwatch and display continue to run from last stopped time value. Sequence (3) (4) may be continued indefinitely.

While in any stopwatch state (5), the user may request and obtain the time of day display or the month/date/weekday by using the T button as described in the flow chart to the left (states [6], [7], [8]). The stopwatch indicator will remain on during this mode.

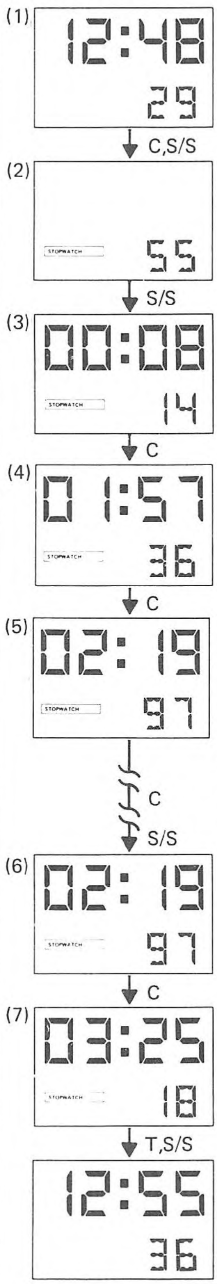
Acquiring time of day during stopwatch mode will not interfere with the running stopwatch. Button S/S will override during stopwatch mode. Activating this button will always take the watch to the next stopwatch state (9), i.e. stop or restart the stopwatch. Alarm set time can also be obtained as described in **ALARM FUNCTIONS.**

Push T and S/S simultaneously.

(10) The stopwatch is reset to zero. Stopwatch indicator is turned off and display reverts to normal time of day display.

TIMEKEEPING PRODUCTS

STOPWATCH – STANDARD SPLIT MODE



Normal time of day display - hours/minutes/seconds.

Hold button "C" down and push button S/S once.

The stopwatch is now in the standard split mode. No counting started. Stopwatch indicator is on and digits 5 and 6 show the display indicating standard split.

Push S/S button once (start).

The stopwatch starts counting. Display shows running time in minutes, seconds and seconds /100.

Push "C" button once (capture)

The display will stop at the captured time while the stopwatch keeps running.

Push "C" button once (capture)

A new captured time value will be displayed. The stopwatch keeps running uninterrupted.

Any time "C" is pushed, a new captured time will be displayed. This can be repeated indefinitely.

Push S/S once.

Stopwatch stops running. Display still retains the previous captured time (5).

Push C button once (recall).

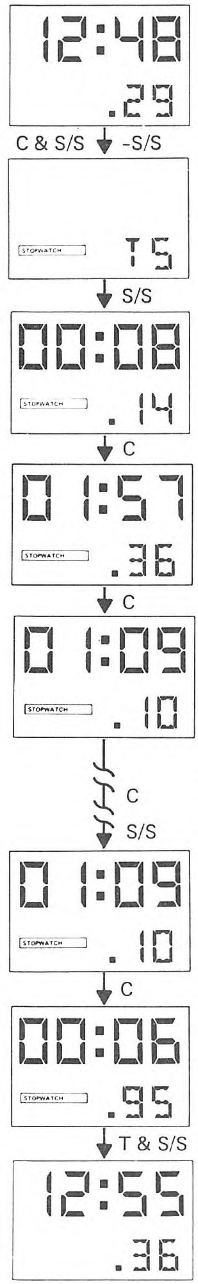
The display will show the stopped time. Thus, the user may record two events which are very close together by sequences 6 and 7.

Push T and S/S button simultaneously.

Stopwatch is reset to zero. The display reverts to the normal time of day display.

While in this stopwatch mode (anywhere in states 2 through 7), the time of day can be displayed using the T button in the manner shown in the flow chart of the basic stopwatch, states 5,6, and 7. This acquisition of time will not interfere with the stopwatch operation, but will erase the last captured time.

STOPWATCH – TAYLOR SPLIT MODE



Normal time of day display – hours/minutes/seconds.

Hold down button "C" and push button S/S twice.

The display will indicate (TS on digits 5 and 6) that the watch is in Taylor Split Mode. Stopwatch indicator is on.

Push button S/S once (start).

The stopwatch starts counting. The display is showing the running time in minutes, seconds, and seconds/100.

Push button "C" once (capture).

The display will show captured time. The stopwatch is reset to zero and counting from zero again.

Push button "C" once (capture).

Again captured time is displayed indicating the time difference between this capture and the previous capture. The stopwatch again is reset to zero and counting up.

Any time "C" is pushed, a new capture time will be displayed showing the difference between the latest capture and the one preceding it.

Push S/S once (stop).

Stopwatch stops running. The display still shows last captured time.

Push C once.

The display will show the difference between the stopped time and last captured time.

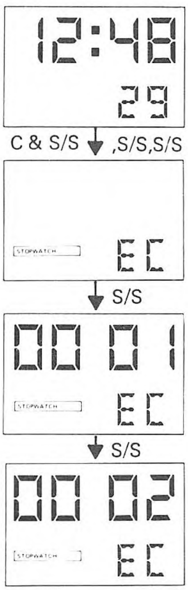
Push T and S/S simultaneously (reset).

Stopwatch is reset to zero. The display reverts to the normal time of day.

As in the other stopwatch modes, the time of day display and month/date/weekday display can be obtained by using button T without interfering with the stopwatch operation. (see description: states 6,7, and 8 - basic stopwatch model). Although the last captured time will be erased.

TIMEKEEPING PRODUCTS

EVENT COUNT MODE



Normal time of day display—hours/minutes/seconds.

Hold down button "C" and push button S/S three times.

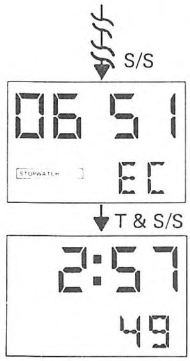
The display will indicate EC on digits 5 and 6 for "Event Count". Stopwatch indicator will be on.

Push button S/S once.

The display will indicate "1" count.

Push button S/S once.

The display will indicate the count of 2.



Push S/S any number of times.

Each subsequent push of S/S will increase the count by one to a maximum of 5999.

Push buttons T and S/S simultaneously.

The event counter is reset to zero and the display will revert to the normal time of day.

As in the previous stopwatch modes, here too, the time of day display may be obtained using button T in the manner described in states 6, 7, and 8 of the basic stopwatch mode. Doing so will not interfere with the event counter.

FREQUENCY CORRECTION

During the Frequency correction set mode, the user may choose to speed up or slow down the watch to compensate for an inaccurate time keeping. The correction range is plus or minus 1 second per day and it is achieved as follows:

Each digit increment in this set mode will speed up the watch by 0.1 seconds per day. Each digit decrement will slow down the watch by the same amount.

Direction of Count →

.0- .1- .2- .3- .4- .5- .6- .7- .8- .9- 0+ .1+ .2+ .3+ .4+ .5+ .6+ .7+ .8+ .9+ .0- . . . .

↑ Center Position — Each increment equals 0.1 seconds per day

Example

The user finds out that his watch is fast by 1 second in 5 days (or 0.2 seconds per day). When getting into the set mode the display indicates .7+; to slow down the watch by 0.2 seconds he must subtract two (2) increments from the display shown or change the setting to .5+. The user holds down button T for the following count and releases T when desired display is reached.

.7+ .8+ .9+ .0- .1- .2- . . . . . . .9- .0+ .1+ .2+ .3+ .4+ .5+

↑ Initial Value — ↑ Final (corrected) Value

SET MODES

General

Entering the set mode is achieved by using the set (S) button (normally recessed).

The SY5009 has 16 set states (not all being used). Since the order of the set states is programmable, the customer may place blank states anywhere in the sequence as well as determine the last set state at which the watch will return to the rest mode, i.e. time of day display. Modification of the set information is done by button T in either single step or fast roll manner (2HZ rate when T is held down. At any time during the set mode, a push on the "C" button will return the watch to the rest mode (time of day display) even if the set sequence was not completed. A typical set sequence is shown in the flow chart below:

Set State No.	Mode	Typical Display	Comments
0	Rest	12:48 12	Time of day display — Hours/minutes/seconds
1	Set alarm hours	6: AM	Display shows hours set for alarm (AM, PM or HR). Colon and alarm indicator are flashing.
2	Set alarm minutes	:45 MI	Display shows minutes set. MI indicator is on. Colon and alarm indicator are flashing.
3	Blank	:	Flashing colon.
4	Set month	12: 2 MO	Digits 1 and 2 display the month. Digit 4 displays the year (in a 4 year cycle, leap year is number 4). Colon flashing. Rotate months through 12 to change year.
5	Set date	:27 CA	Display CA in digits 5 and 6 for calendar. Digits 3 and 4 show the date and colon is flashing.
6	Set weekday	: TH	Flashing colon. Digits 5 and 6 display weekday: Monday-MO Wednesday-WE Friday-FR Sunday-SU Tuesday-TU Thursday-TH Saturday-SA
7	Set hour	9: PM	Flashing colon. Digits 5 and 6 display AM, PM, or HR if the watch is in 24 hour mode.
8	Set minutes	:57 MI	Flashing colon. Digits 5 and 6 indicates MI for "minutes". For synchronization to a time standard, set minutes to next minute and push "C" or "S" button at time signal to set seconds to 00.
9	Blank	:	Flashing colon.
10	Blank	:	Flashing colon.
11	Set frequency correction	: .8+	Flashing colon. Decimal point is on. Digit 5 will show a number between 0 and 9. Digit 6 will show (+) or (-) signs. See instructions on preceeding page for set procedures.
12	Blank	:	Flashing colon.
13	Blank	:	Flashing colon.
14	Blank	:	Flashing colon.
15	Blank	:	Flashing colon.

Custom Capabilities

Custom Capabilities

CUSTOM

Custom MOS/LSI

Synertek®

Since the inception of the company, Synertek has played a very active role in the CUSTOM MOS marketplace. We have found that by maintaining a leadership position in high-technology standard products, we are able to offer our custom product customers the most competitive design/process solutions available in the industry. Our standard products employ the latest in design and process techniques in the P-Channel, N-Channel and CMOS silicon gate technologies including the use of ion implanted, depletion-mode devices and on-chip substrate bias generators. These same techniques allow the design of the most competitive custom circuits which in turn gives the desired overall result for our customer..... an advantage in his marketplace.

The use of custom MOS and CMOS circuits has been so pervasive that it is impossible to discuss the full range of potential applications. A sampling of Synertek's experience illustrates the extremes:

- Two different 16-bit microprocessors: one program's purpose was to reduce the cost of a top line Minicomputer, and the other for use in a Distributed Process Control System.
- A printer and keyboard controller in a microprocessor-based Word Processing System.
- All the digital logic for an electric utility two-way Load Management System.
- The CMOS logic for a Pocket Paging System.
- The analog and digital circuitry for a Tire Pressure Sensing System.
- The digital circuitry for a Bell-system approved Touch-Tone Receiver and Repertory Dialer.

This list could go on but the point is that CUSTOM MOS is being used in almost every sector of the electronics market and the applications are steadily advancing into the electromechanical and mechanical strongholds as well. If the production volume is sufficient, the lower cost and higher reliability of a custom MOS solution cannot be ignored.

There are several possible levels of interface between Synertek and our Customers in the design of a custom product. Some companies prefer that Synertek design the entire electronic subsystem so that they are free to concentrate on system design. Other companies have in-house MOS design groups and they prefer to provide us with working plates and test tapes. We prefer to work closely with each customer to evolve the best interface for a specific program at a specific point in time. The best interface point depends on many factors including (a) technical difficulty and performance requirements of the chip, (b) anticipated production volume, (c) availability of customer's design engineers when the program must begin, and so on. Synertek has the ability to work at any of the interface levels and indeed that is the first topic of discussion on any program. The flow chart on the next page shows the activities that must be executed promptly and accurately for a successful program. The amount of time required for each task depends on the complexity of the circuit; a realistic range is shown next to each activity. Before a program is begun, however, our customer knows the exact schedule for his particular circuit.

A. CONCEPT REVIEW

The initial step in the development of a custom circuit is a concept review meeting which consists of detailed discussions reviewing system requirements. The purpose of this meeting is to assure that Synertek's MOS-LSI Design Engineers fully understand all pertinent system requirements such as:

- Functional Operation.
- Subsystem, or chip, interface requirements, especially those that may determine which process (P, N, or CMOS), must be used.
- Environmental or packaging requirements.

B. SYSTEM DEFINITION

The block diagrams/flow charts and electrical specifications are established in this phase. These are a result of contributions by both Synertek and the customer.

C. LOGIC DESIGN

Conversion of the system functions to MOS logic implementation is done entirely by Synertek Design Engineers. This logic is optimized for the particular process and application involved and will differ substantially from any prior (e.g. TTL) implementation.

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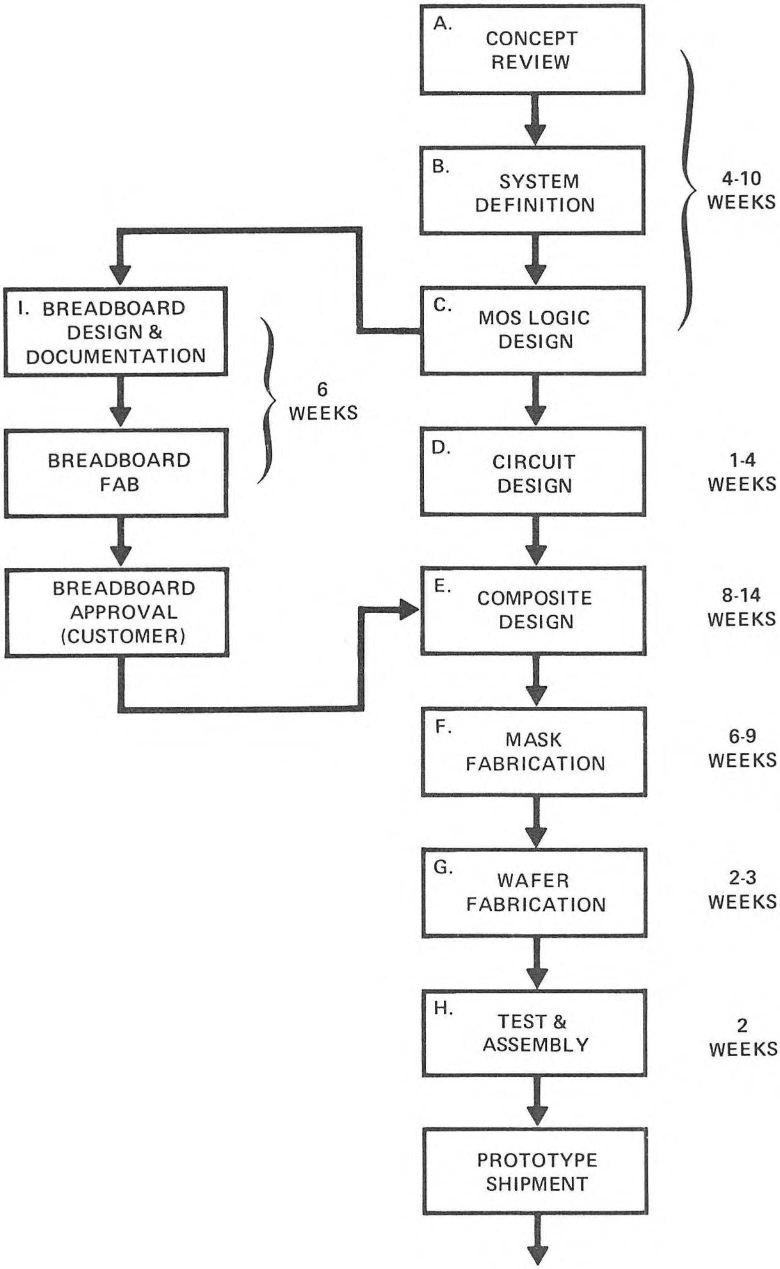

A. CONCEPT REVIEW
B. SYSTEM DEFINITION
C. MOS LOGIC DESIGN
4-10 WEEKS
I. BREADBOARD DESIGN & DOCUMENTATION
BREADBOARD FAB
6 WEEKS
BREADBOARD APPROVAL (CUSTOMER)
D. CIRCUIT DESIGN
1-4 WEEKS
E. COMPOSITE DESIGN
8-14 WEEKS
F. MASK FABRICATION
6-9 WEEKS
G. WAFER FABRICATION
2-3 WEEKS
H. TEST & ASSEMBLY
2 WEEKS
PROTOTYPE SHIPMENT

CUSTOM

D. CIRCUIT DESIGN

During this phase the individual transistors are designed to implement the logic, to have the proper I/O characteristics, and to execute the intended function at the proper speed. Particular attention is paid to critical speed paths in this phase as well as in composite design.

E. COMPOSITE DESIGN

This is the most time-consuming phase since the overall chip size directly affects the cost of the final device. The composite is designed, usually at 1000X, "by hand" as opposed to using a computer aided placement and wiring program. Creative layout designers are still far superior to computers and the smaller chips result in very real production savings. Composite design and circuit design overlap somewhat, especially in the area of critical speed paths.

F. MASK FABRICATION

This phase actually consists of three separate critical activities.

Digitizing - As sections of the circuit become complete they are digitized on Synertek's Calma system. The digitized information is then used to generate check plots which then are compared to the original section of the composite to assure no errors. This is an iterative procedure which usually requires several interactions before the data base tape is approved for the entire composite.

Pattern Generation - All Synertek circuits are, and always have been, produced without the use of rubilith (rubies). We go directly from digitizing to reticle generation, or pattern generation. The reticle is usually manufactured at 10X. Photographic "blowbacks" are then compared, once again, to the original composite as one last check to assure that the tooling is correct.

Working Plate Manufacture - The approved reticle is then used to step-and-repeat a master plate which is ultimately used for generation of the working plates.

G. WAFER FABRICATION

Fabrication of wafers will be performed in one of Synertek's modern manufacturing areas. Exactly which area will be used for a particular device is determined mainly by the process technology involved. During the fabrication phase, numerous quality and electrical inspections are performed on each wafer to assure that each wafer run is within the allowable bounds of Synertek's manufacturing process.

H. TEST AND ASSEMBLY

Following the fabrication of devices, wafers are then tested using computer controlled state-of-the art LSI testers. Each of these machines contains its own mini-computer and, after being properly programmed, is capable of doing both functional and parametric tests. Initial prototype devices will then be assembled in Santa Clara and subjected to a complete final test prior to shipment.

I. BREADBOARD

Since many of our custom circuits contain on the order of 4,000 gates, a great deal of attention is required to assure that these chips work right the first time out. The checking required in composite design and mask fabrication was touched on above. We have found, however, that computer-aided programs for checking logic and circuit design are not adequate in verifying proper operation of the entire chip.

In parallel with the logic and circuit design, Synertek constructs a breadboard which is essentially a transistor-for-transistor duplicate of the circuit being designed. The breadboard is checked out by Synertek and then given to the customer for approval. The breadboard can be wired into the customer's system, for example, and the whole system can be checked out for proper performance. Perhaps features are added or deleted at this point, since the customer's engineering and marketing people get their first "hands on" exposure to this new product. After approval, the breadboard is then used by Synertek's Test Program Development group to generate and debug the test program prior to the time wafers are available.

To determine if your application is technically and/or economically a realistic candidate for Custom MOS implementation, Synertek can perform a preliminary analysis in approximately one week. Such items as functional specifications, logic diagrams if the equipment is already in production using standard components, and/or block diagrams improve the accuracy of the preliminary analysis. If the analysis is promising, Synertek will then issue a firm quotation.

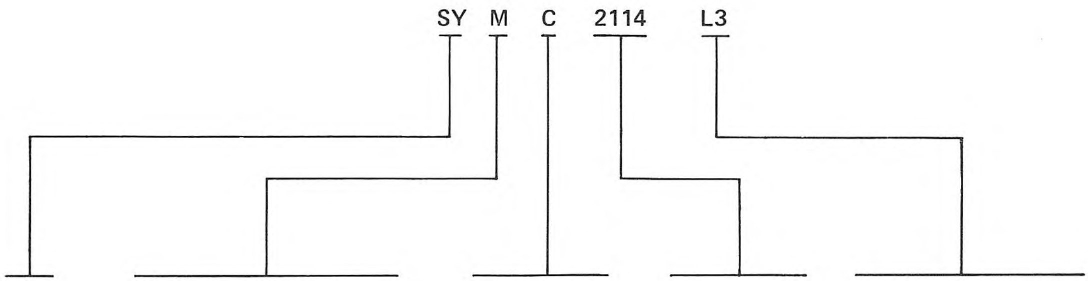
CUSTOM

General Information

General Information

8

ORDERING INFORMATION

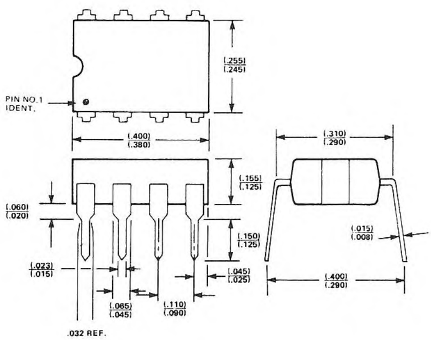


Prefix	Temperature Range	Package Type	4 Digit Device Code	3 Digit Performance or Processing Designator
	No Designator — 0°C to 70°C	C - Ceramic		
	M — -55°C to +125°C	P - Molded		
	X — Special	D - Cerdip		
		X - Dice		
		F - Flat Pac		
		T - TO Can		

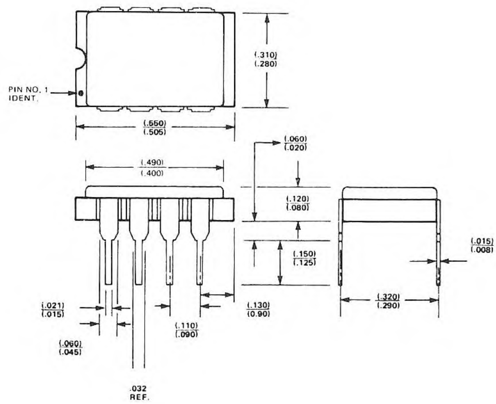
For specially programmed devices (ROM's, 6530 Combo, etc.) Synertek will assign a special custom number. This number must be used when ordering these devices.

EXAMPLE: SYP 2316B, C28000: 2048 x 8 Read Only Memory, plastic 24 pin Dip, 0°C to +70°C, bit pattern as defined by C28000.

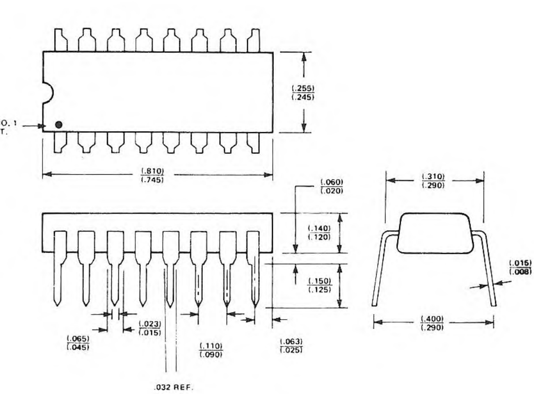
Packaging Information



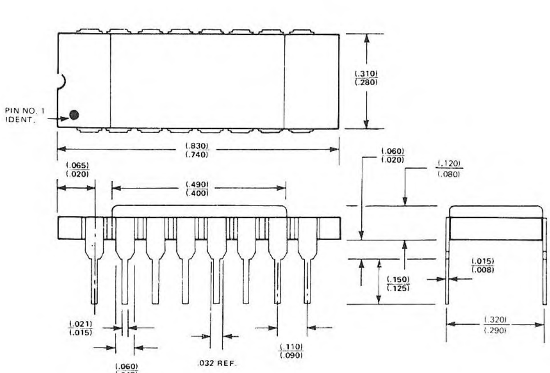
Plastic Dual In-Line — 8 Leads



Ceramic Dual In-Line — 8 Leads



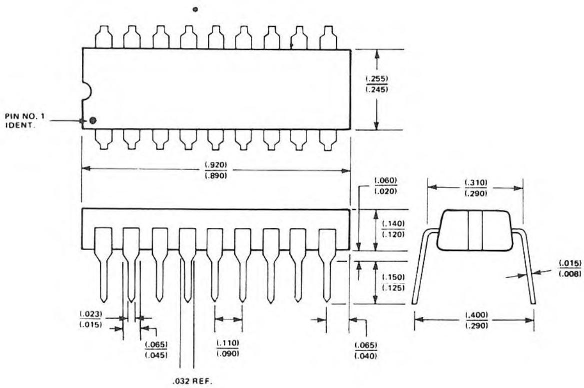
Plastic Dual In-Line — 16 Leads



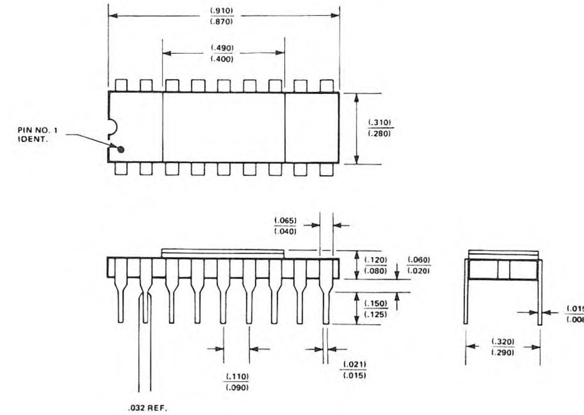
Ceramic Dual In-Line — 16 Leads

GENERAL

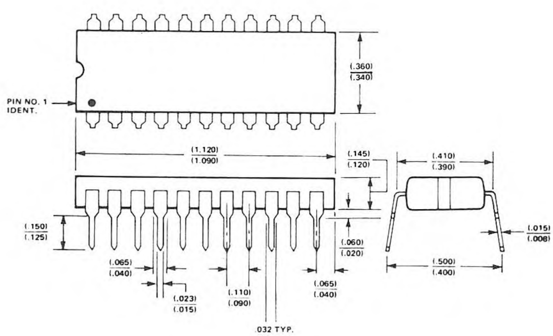
Packaging Information



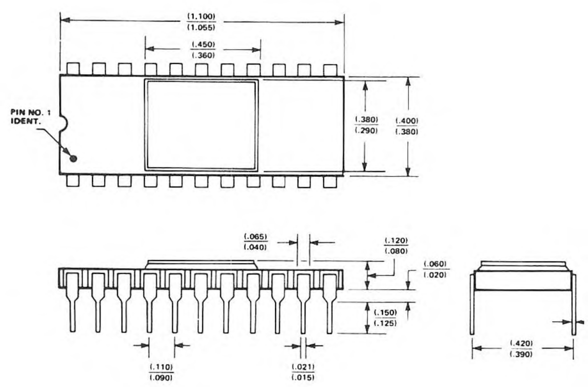
Plastic Dual In-Line – 18 Leads



Ceramic Dual In-Line – 18 Leads



Plastic Dual In-Line – 22 Leads



Ceramic Dual In-Line – 22 Leads

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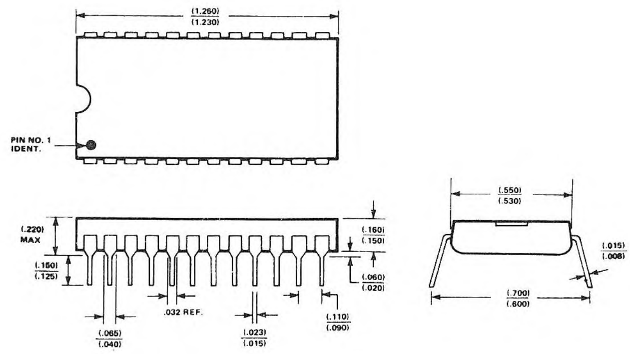
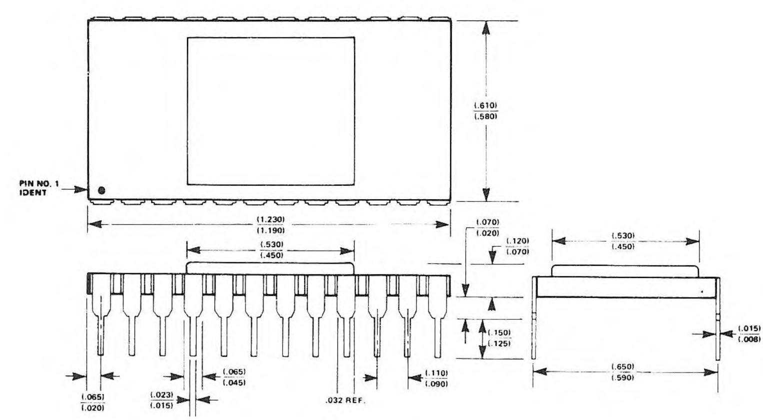
Packaging Information

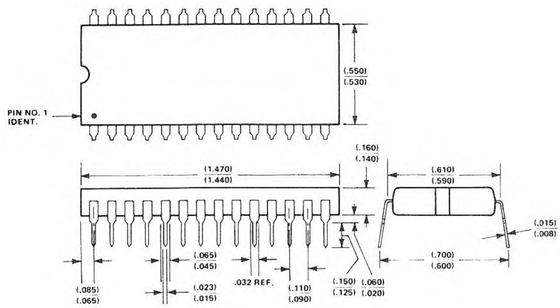


Plastic Dual In-Line – 24 Leads

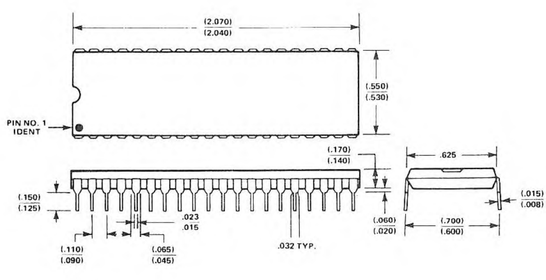


Ceramic Dual In-Line – 24 Leads

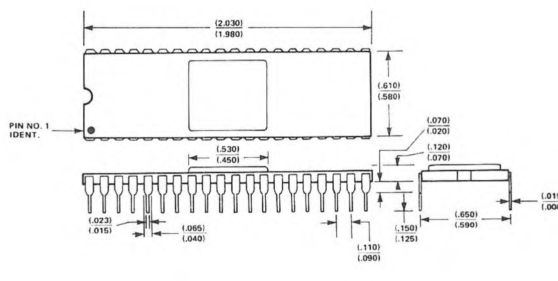
Packaging Information



Plastic Dual In-Line – 28 Lead

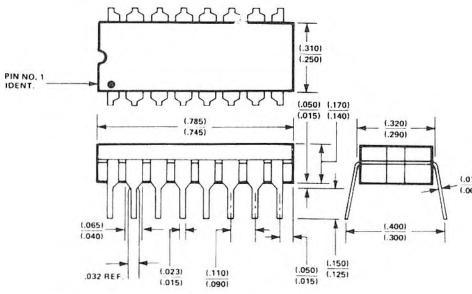


Plastic Dual In-Line – 40 Lead

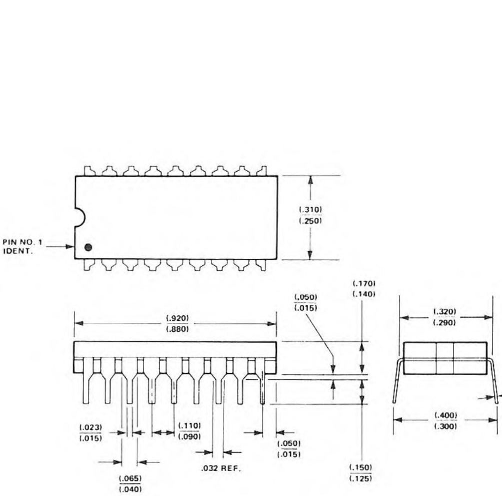


Ceramic Dual In-Line – 40 Lead

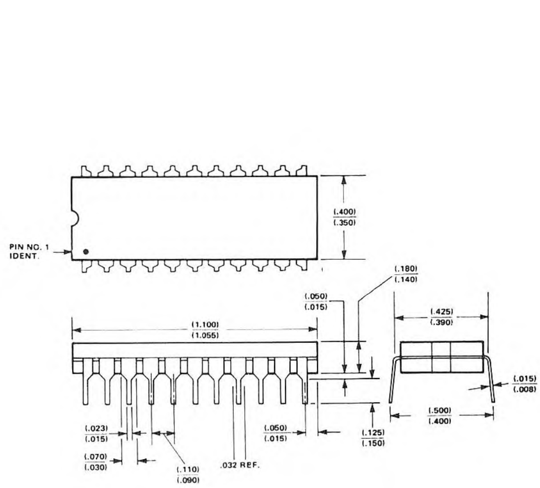
Packaging Information



Cerdip Dual In-Line – 16 Lead



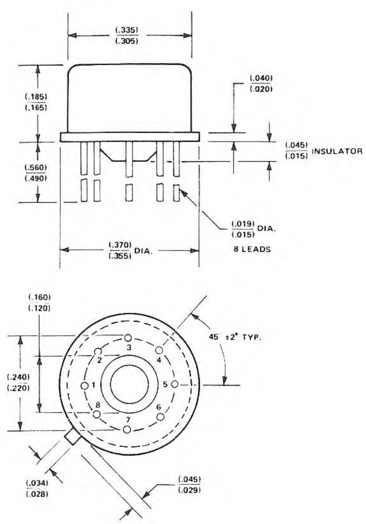
Cerdip Dual In-Line – 18 Lead



Cerdip Dual In-Line – 22 Lead

GENERAL

Packaging Information



Metal Can — 8 Leads

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Notes

Notes

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