Memory, I/O, Timer Array

SY6530

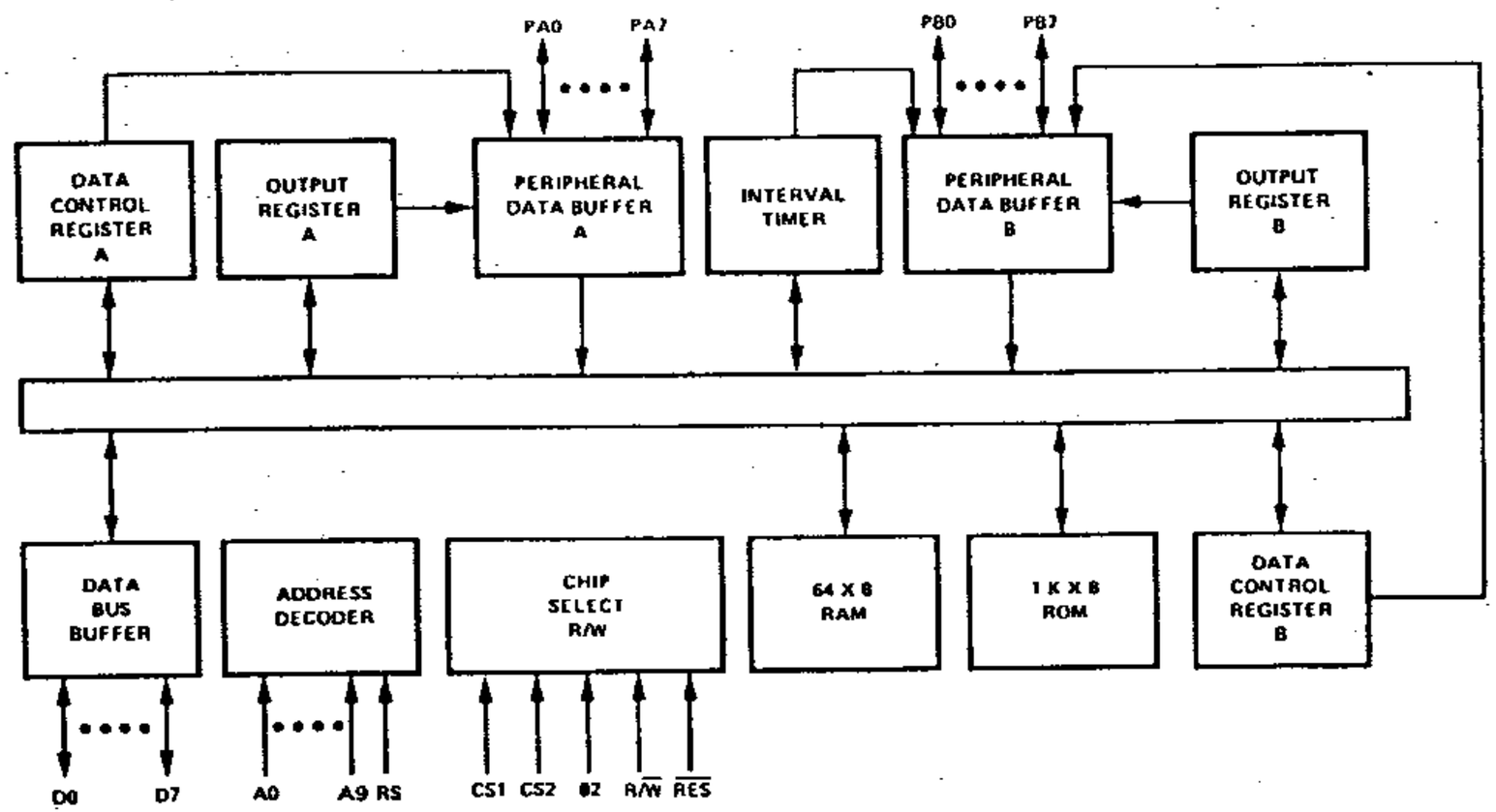
MICROPROCESSOR PRODUCTS

APRIL 1979

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- 1024 x 8 ROM
- 64 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedence Three-State Data Pins
- Allows up to 7K contiguous bytes of ROM with no external decoding

The SY6530 is designed to operate in conjunction with the SY6500 microprocessor Family. It is comprised of a mask programmable 1024 x 8 ROM, a 64 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

FIGURE 1. SY6530 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) ..... -.3 to +7.0V
Input/Output Voltage (V_{IN}) ..... -.3 to +7.0V
Operating Temperature (T_{OP}) ..... 0 to 70°C
Storage Temperature Range (T_{STG}) ..... -55 to +150°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to 70°C)

	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage	V_{IH}	2.4		V_{CC}	V
Input Low Voltage	V_{IL}	-0.3		0.4	V
Input Leakage Current: V_{IN} = V_{SS} +5V A0-A9, RS, R/$\overline{W}$, $\overline{RES}$, Ø2, PB6*, PB5*	I_{IN}		1.0	2.5	μA
Input Leakage Current for High Impedence State (Three State); V_{IN} = .4V to 2.4V; D0-D7	I_{TSI}		±1.0	±10.0	μA
Input High Current; V_{IN} = 2.4V PA0-PA7, PB0-PB7	I_{IH}	-100.	-300.		μA
Low Input Current; V_{IN} = .4V PA0-PA7, PB0-PB7	I_{IL}		-1.0	-1.6	mA
Output High Voltage V_{CC} = MIN, $I_{LOAD} \leq$ -100μA (PA0-PA7, PB0-PB7, D0-D7) $I_{LOAD} \leq$ -3mA (PA0, PB0)	V_{OH}	2.4 1.5			V
Output Low Voltage V_{CC} = MIN, $I_{LOAD} \leq$ 1.6mA	V_{OL}			0.4	V
Output High Current (Sourcing): $V_{OH} \geq$ 2.4V (PA0-PA7, PB0-PB7, D0-D7) $\geq$ 1.5V Available for other than TTL (Darlingtons) (PA0, PB0)	I_{OH}	-100 -3.0	-1000 -5.0		μA mA
Output Low Current (Sinking); $V_{OL} \leq$ .4V	I_{OL}	1.6			mA
Clock Input Capacitance	C_{CLK}			30	pF
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF
Power Dissipation	P_D		500	700	mW

*When Programmed as address pins All values are D.C. readings

WRITE TIMING CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Period	T_{CYC}	1		10	μs
Rise & Fall Times	T_R, T_F			25	ns
Clock Pulse Width	T_C	470			ns
R/$\overline{W}$ valid before positive transition of clock	T_{WCW}	180			ns
Address valid before positive transition of clock	T_{ACW}	180			ns
Data bus valid before negative transition of clock	T_{DCW}	300			ns
Data Bus Hold Time	T_{HW}	10			ns
Peripheral data valid after negative transition of clock	T_{CPW}			1	μs
Peripheral data valid after negative transition of clock driving CMOS (Level = V_{CC} -30%)	T_{CMOS}			2	μs
R/$\overline{W}$ hold time after negative clock transition	T_{CWW}	0			ns
Address hold time	T_{CAH}	0			ns

READ TIMIMG CHARACTERISTICS

Characteristic	Symbol	Min.	Typ.	Max.	Unit
R/$\overline{W}$ valid before positive transition of clock	T_{WCR}	180			ns
Address valid before positive transition of clock	T_{ACR}	180			ns
Peripheral data valid before positive transition of clock	T_{PCR}	300			ns
Data bus valid after positive transition of clock	T_{CDR}			395	ns
Data Bus Hold Time	T_{HR}	10			ns
$\overline{IRQ}$ (Interval Timer Interrupt) valid before positive transition of clock	T_{IC}	200			ns
R/$\overline{W}$ hold time after negative clock transition	T_{CWR}	0			ns
Address hold time	T_{CAH}	0			ns

Loading = 30 pF + 1 TTL load for PA0-PA7, PB0-PB7
= 130 pF + 1 TTL load for D0-D7

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a low ($\leqslant$0.4V) on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock (ϕ_2)

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$ or high level clock $V_{IL} < 0.2$, $V_{IH} = V_{CC}\ ^{+.3}_{-.2}$).

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the SY6530. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the data supplied by the SY6530. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the SY6530.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the data direction register. The pin will be normally high with a low indicating an interrupt from the SY6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pullup may be omitted with a mask option.

Data Bus (D0-D7)

The SY6530 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports (PA0–PA7, PB0–PB7)

The SY6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PB5, PB6 and PB7 also have other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the SY6530 it receives data stored in the data register. The microproccessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volts for a "0" as the peripheral pins are all TTL compatible. Pins PA0 and PB0 are also capable of sourcing 3 ma at 1.5V, thus making them capable of direct transistor drive.

Address Lines (A0-A9)

There are 10 address pins. In addition to these 10, there is the ROM SELECT (RS) pin. The above pins, A0-A9 and ROM SELECT, are always used as addressing pins. There are 2 additional pins which are mask programmable and can be used either individually or together as CHIP SELECTS. They are pins PB5 and PB6. When used as peripheral data pins they cannot be used as chip selects.

FIGURE 2. WRITE TIMING CHARACTERISTICS

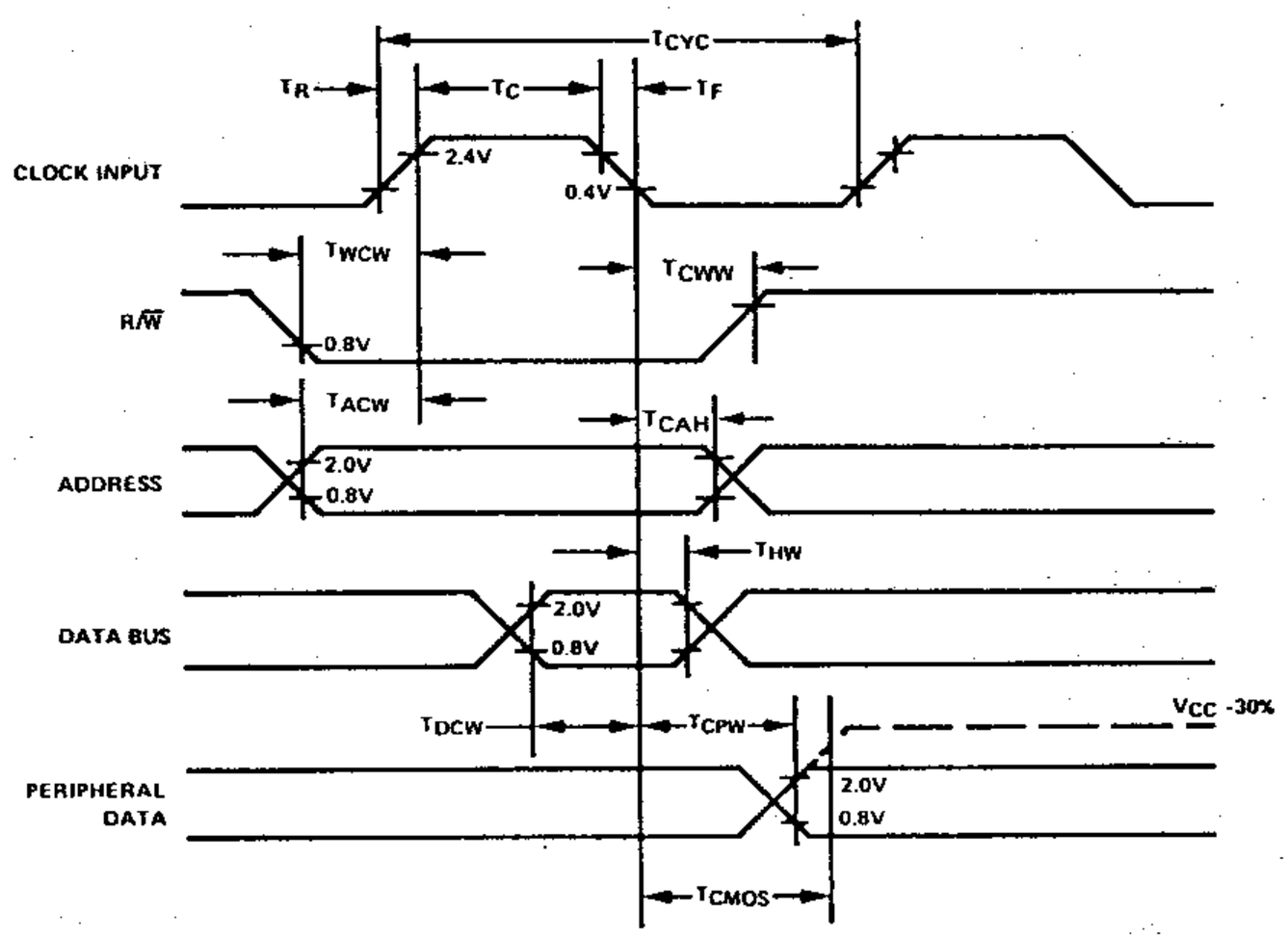
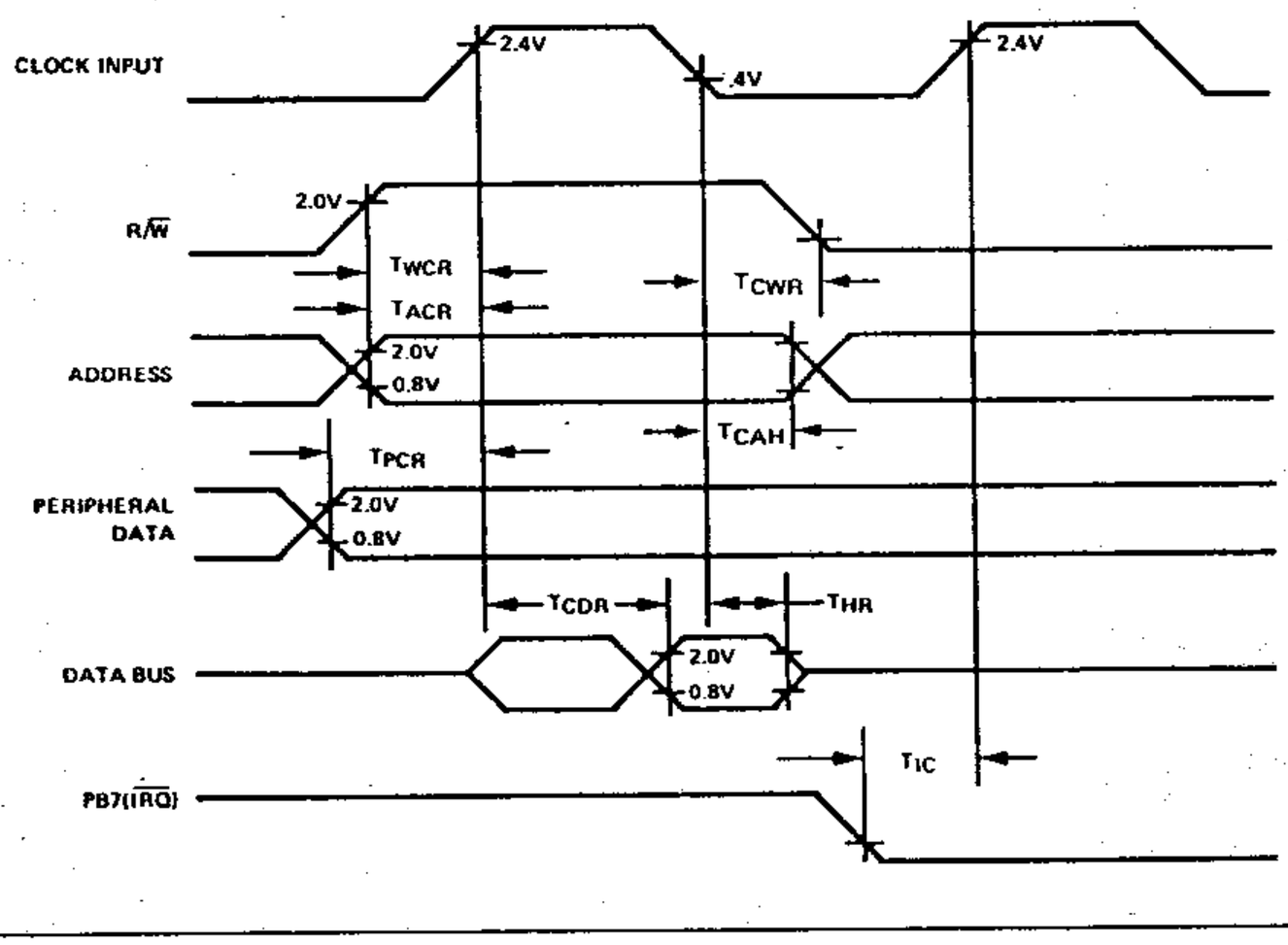


FIGURE 3. READ TIMING CHARACTERISTICS



INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The SY6530 is divided into four basic sections, RAM, ROM, I/O and TIMER. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of 2 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O Register.

ROM 1 K Byte (8 K Bits)

The 8K ROM is in a 1024 x 8 configuration. Address lines A0-A9, as well as RS are needed to address the entire ROM. With the addition of CS1 and CS2, seven SY6530's may be addressed, giving 7168 x 8 bits of contiguous ROM.

RAM - 64 Bytes (512 Bits)

A 64 x 8 static RAM is contained on the SY6530. It is addressed by A0-A5 (Byte Select), RS, A6, A7, A8, A9, and, depending on the number of chips in the system, CS1 and CS2.

Internal Peripheral Registers

There are four internal registers, two data direction registers and two peripheral I/O data registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Therefore, anything then written into the I/O Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data to or from the I/O Register. For example, a "1" loaded into data direction A, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two data I/O registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor array.

During a read operation the microprocessor is not reading the I/O Registers but in fact is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the I/O Register. The only way the I/O Register data can be changed is by a microprocessor Write operation. The I/O Register is not affected by a Read of the data on the peripheral pins.

Interval Timer

The Timer section of the SY6530 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 4.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervls were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written into the Interval Timer, the counting intervals of 1, 8 64, 1024T are decoded from address lines A0 amd A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., $A_3 = 1$ enables $\overline{IRQ}$ on PB7, $A_3 = 0$ disables $\overline{IRQ}$ on PB7. When PB7 is used as an interrupt flag with the interval timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 1 1 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
ADD 1 = 0 0 0 1 1 1 0 0 = 28.

Thus to arrive at the total elapsed time; merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrup is (52 x 8) +1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag.

Figure 5 illustrates an example of interrupt.

FIGURE 4. BASIC ELEMENTS OF INTERVAL TIMER

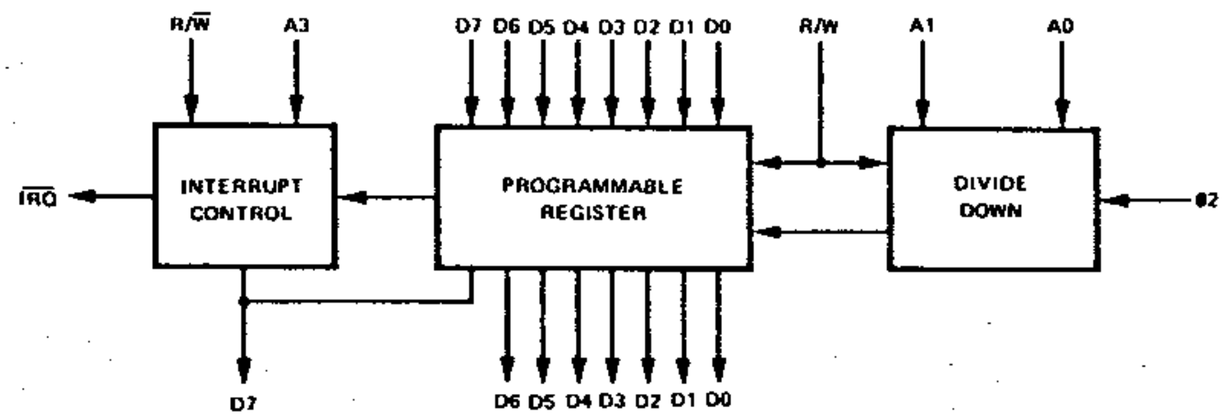
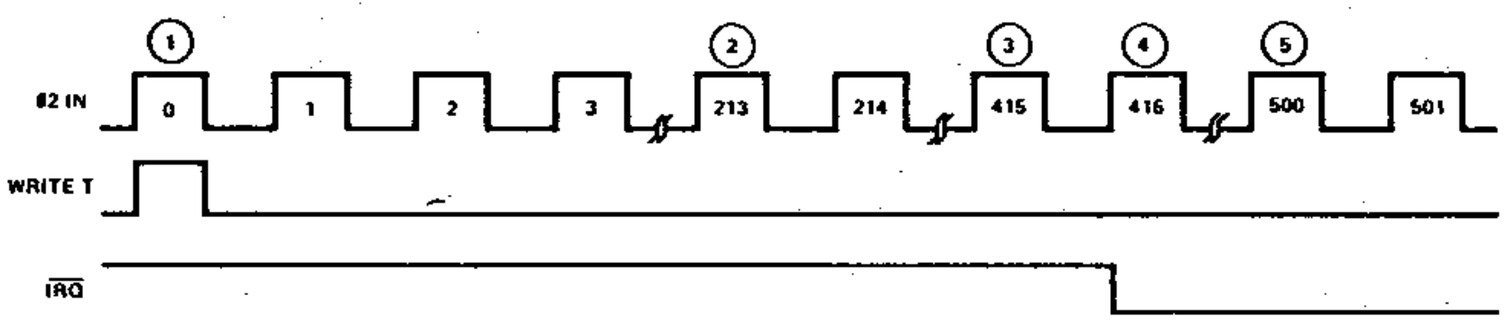


FIGURE 5. TIMER INTERRUPT TIMING



1. Data written into Interval timer is 0 0 1 1 0 1 0 0 = 52_{10}
2. Data in Interval timer is 0 0 0 1 1 0 0 1 = 25_{10}

$$52 - \frac{213}{8} - 1 = 52\text{-}26\text{-}1 = 25$$

3. Data in Interval timer is 0 0 0 0 0 0 0 0 = 0_{10}

$$52 - \frac{415}{8} - 1 = 52\text{-}51\text{-}1 = 0$$

4. Interrupt has occured at ϕ_2 pulse #416
   Data in Interval timer = 1 1 1 1 1 1 1 1
5. Data in Interval timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 1 0 0 = 84_{10}
   $84 + (52 \times 8) = 500_{10}$

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until another Write timer operation.

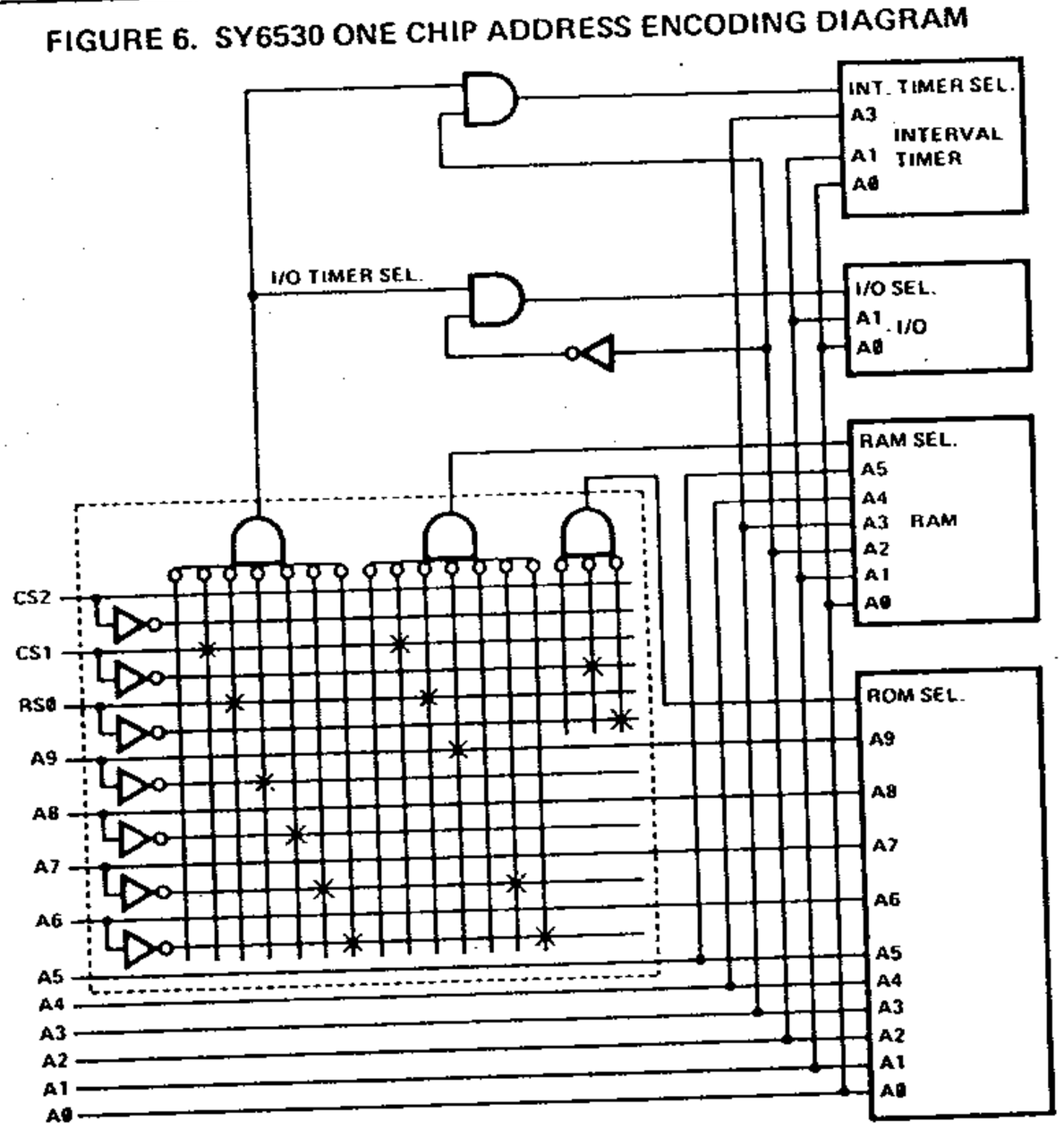
ADDRESSING

Addressing of the SY6530 offers many variations to the user for greater flexibility. The system may be configured with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0-A9). In addition there is the possibility of 3 additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are CS1 and CS2. The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as chip-select. The third additional address line is RS. In a 2-chip system, RS would be used to distinguish between ROM and non-ROM sections of the SY6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Below is an example of a 1-chip and a 7-chip SY6530 addressing scheme.

One-Chip Addressing

Figure 6 illustrates a 1-chip system for the SY6530.

FIGURE 6. SY6530 ONE CHIP ADDRESS ENCODING DIAGRAM



A. X indicates mask programming
   i.e. ROM select = CS1•RSO
   RAM select = $\overline{CS1}$•$\overline{RSO}$•$\overline{A9}$•A7•A6
   I/O TIMER SELECT = $\overline{CS1}$•$\overline{RSO}$•A9•A8•A7•A6

B. Notice that A8 is a don't care for RAM select

C. The CS2/PB5 pin functions as PB5 in this example.

Seven-Chip Addressing

In the 7-chip system the objective would be to have 7K of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14, and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between addresses 65,535 and 58,367. The 2 pins designated as chip-select or I/O would be mask programmed as chip-select pins. Pin RS would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12 respectively. See Figure 7.

The two examples shown would allow addressing of the ROM and RAM; however, once the I/O or timer has been addressed, further decoding is necessary to select which of the I/O registers is desired, as well as the coding of the interval timer.

I/O Register - Timer Addressing

Figure 8 illustrates the address decoding for the internal elements and timer programming. Address lines A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the divide by matrix. This decoding is defined in Figure 8. In addition, address A3 is used to enable the interrupt flag to PB7.

The addressing of the ROM select, RAM select and I/O timer select lines would be as follows:

FIGURE 7. SY6530 SEVEN CHIP ADDRESSING SCHEME

		CS2 A12	CS1 A11	RSØ A10	A9	A8	A7	A6
SY6530 #1,	ROM SELECT	0	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	0
	I/O TIMER	0	0	0	1	0	0	0
SY6530 #2,	ROM SELECT	0	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	1
	I/O TIMER	0	0	0	1	0	0	1
SY6530 #3,	ROM SELECT	0	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	0
	I/O TIMER	0	0	0	1	0	1	0
SY6530 #4,	ROM SELECT	1	0	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	1
	I/O TIMER	0	0	0	1	0	1	1
SY6530 #5,	ROM SELECT	1	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	0
	I/O TIMER	0	0	0	1	1	0	0
SY6530 #6,	ROM SELECT	1	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	1
	I/O TIMER	0	0	0	1	1	0	1
SY6530 #7,	ROM SELECT	1	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	1	0
	I/O TIMER	0	0	0	1	1	1	0

* RAM select for SY6530 #5 would read = $\overline{A12} \cdot \overline{A11} \cdot \overline{A10} \cdot \overline{A9} \cdot A8 \cdot \overline{A7} \cdot \overline{A6}$

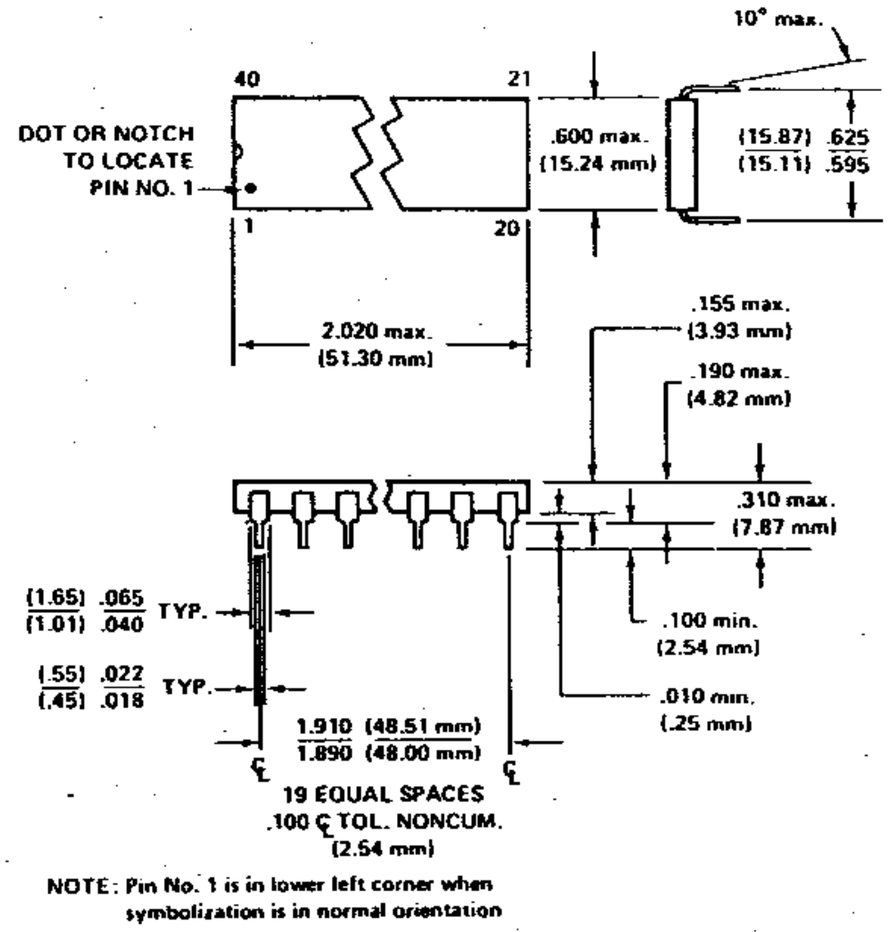
FIGURE 8. ADDRESSING DECODE FOR I/O REGISTER AND TIMER

	ADDRESSING DECODE							
	ROM SELECT	RAM SELECT	I/O TIMER SELECT	R/$\overline{W}$	A3	A2	A1	A0
READ ROM	1	0	0	1	–	–	–	–
WRITE RAM	0	1	0	0	–	–	–	–
READ RAM	0	1	0	1	–	–	–	–
WRITE DDRA	0	0	1	0	–	0	0	1
READ DDRA	0	0	1	1	–	0	0	1
WRITE DDRB	0	0	1	0	–	0	1	1
READ DDRB	0	0	1	1	–	0	1	1
WRITE PER. REG. A	0	0	1	0	–	0	0	0
READ PER. REG. A	0	0	1	1	–	0	0	0
WRITE PER. REG. B	0	0	1	0	–	0	1	0
READ PER. REG. B	0	0	1	1	–	0	1	0
WRITE TIMER								
÷ 1T	0	0	1	0	X	1	0	0
÷ 8T	0	0	1	0	X	1	0	1
÷ 64T	0	0	1	0	X	1	1	0
÷ 1024T	0	0	1	0	X	1	1	1
READ TIMER	0	0	1	1	X	1	–	0
READ INTERRUPT FLAG	0	0	1	1	–	1	–	1

– = Don't care condition

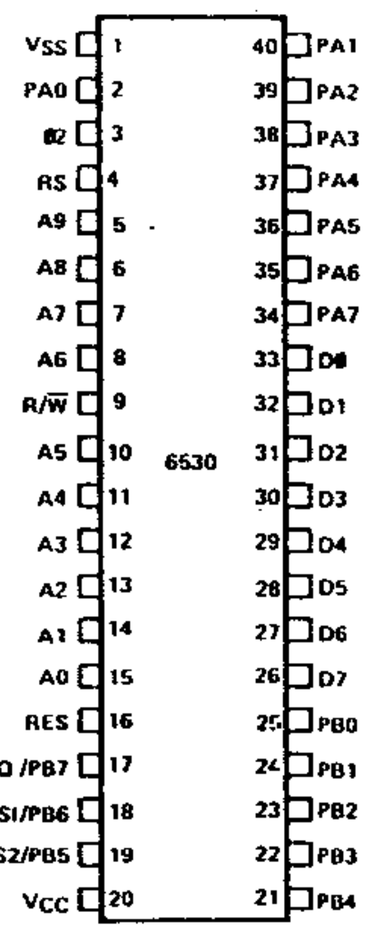
X A_3 = 1 Enables IRQ to PB7

A_3 = 0 Disables IRQ to PB7



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

PACKAGE OUTLINE



PIN DESIGNATION

PROGRAMMING INSTRUCTIONS

The SY6530 utilizes computer aided techniques to manufacture and test custom ROM patterns. The pattern and address coding is supplied to Synertek in any of several formats.

1) 2708-type EPROMs.
2) Synertek data card formats.
3) Other input formats, providing they can be translated into one of the above.

Synertek Data Card Format

A. The format for the first and all succeeding records, except for the last record, in a file is as follows:

$;N_1N_0 \quad A_3A_2A_1A_0 \quad (D_1D_0)_1 \quad (D_1D_0)_2 \quad X_3X_2X_1X_0$

where:

1. All characters (N,A,D,X) are the ASCII characters 0 through F, each representing a hexadecimal digit.
2. ; is a record mark indicating the start of a record.
3. N_1N_0 = the number of bytes of data in this record (in hexadecimal). Each pair of hexadecimal characters (D_1D_0) represents a single byte in the record.
4. $A_3A_2A_1A_0$ = the hexadecimal starting address for the record. A_3 represents address bits 15 through 12, etc. The 8-bit byte represented by $(D_1D_0)_1$ is stored in address $A_3A_2A_1A_0$; $(D_1D_0)_2$ is stored in $(A_3A_2A_1A_0) + 1$, etc.
5. (D_1D_0) = two hexadecimal digits representing an 8-bit byte of data. (D_1 = high order 4 binary bits and D_0 = low-order 4 bits). A maximum of 18 (Hex) or 24 (decimal) bytes of data per record is permitted.
6. $X_3X_2X_1X_0$ = record check sum. This is the hexadecimal sum of all characters in the record, including N_1N_0 and $A_3A_2A_1A_0$ but excluding the record mark and the check sum characters. To generate the check sum, each byte of data (represented by two ASCII characters), is treated as 8 binary bits. The binary sum of these 8-bit bytes is truncated to 16 binary bits (4 hexadecimal digits) and is then represented in the record as four ASCII characters ($X_3X_2X_1X_0$).

B. The format for the last record in a file is as follows:

; 00 $C_3C_2C_1C_0$ $X_3X_2X_1X_0$

1. 00 = zero bytes of data in this record. This identifies this as the final record in a file.
2. $C_3C_2C_1C_0$ = the total number of records (in hexadecimal) in this file, including the last record.
3. $X_3X_2X_1X_0$ = check sum for this record.

C. Example

The following example illustrates the exact format of the hex interface file in both listing and punched paper tape form.

```
;18F000CA86004C00F0FDF9212D21FF292DBF2161F5F7FF657D677D0D40
;18F018E564672DFD7575E50000CF4112F800925198D200539192F20C98
;18F03008DB028808 10DE12D894189AC2830E9800FBB6232F087F650AA5
;18F048036E20EF2FA58D4465E8FDF93DE775EF257FB520ED64657C0DEB
;18F0607F11D05A1EDF0250B0DAFE0092529099 12DB108A0298DE080C0D
;18F078D95058DF82D2D79A00ED65E68724EE05212764A5F5BDA9050E2C
;18F090EC20FF6525252469332 13F20FF3129 3B7E18D65042DE40500A92
;18F0A81E5E5B02534A53DE4A9B189259969F589E5E92DF52DE9E9A0CA2
;18F0C000B3268D2400EF6765E7A0B560672521 7D20AF35EDF5202F0C08
;18F0D8692525342B35256CDF12F2785FFF547FD2E2D6525BDF5A720D26
;10F0F012DB020F1A1ABF86D2DA9ADAC8DECA1B0A12
:00000B000B
```

ADDITIONAL PATTERN INFORMATION

In addition to the ROM data patterns, it is necessary to provide the information outlined below.

CUSTOMER NAME
CUSTOMER PART NO.
CUSTOMER CONTACT (NAME)
CUSTOMER TELEPHONE NO.
CS1/PB6 (ENTER "CS1" OR "PB6")
CS2/PB5 (ENTER "CS2" OR "PB5")
PULL-UP RESISTOR ON PB7 ("YES" OR "NO")
LOGIC FORMAT ("POS" OR "NEG")

DEVICE ADDRESSING (Enter "H" for High, "L" for Low, or "N" for don't care)

	RS	CS1	CS2	A9	A8	A7	A6
ROM SELECT							
RAM SELECT							
I/O TIMER SELECT							

Send Information To:

Synertek – ROM
P.O. Box 552
Santa Clara, CA 95052

SY6530 CUSTOMER SPECIFICATION FORM

1. Date.

2. Customer name.

3. Customer part no.
   (maximum 10 digits)

4. Synertek "C" number.

5. Customer Contact.

6. Customer phone number

7. Chip Select Code
   (Check one square in each block)

CS1	
PB6	

CS2	
PB5	

PULL UP ON PB7	YES	
	NO	

8. ROM/RAM/I-O SELECTS (Specify H or L or N (don't care) in each box.

	RS	CS1	CS2	A9	A8	A7	A6
ROM SELECT				N	N	N	N
RAM SELECT							
I/O SELECT							

9. Customer's Input

   Punched Cards ☐
   Punched Tape ☐

10. Data Format

    MOS Technology ☐
    Intel Hex ☐
    Intel BPNF ☐
    Binary ☐

11. Logic Format

    Positive ☐
    Negative ☐

12. Verification Status

    Hold ☐
    Not Required ☐