

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

EIA-232-D/V.28 Driver/Receiver
(Formerly RS-232-C)

The MC145406 is a silicon-gate CMOS IC that combines 3 drivers and 3 receivers to fulfill the electrical specifications of standards EIA-232-D and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate-limited output, 300 ohms power-off source impedance, and output typically switching to within 25 percent of the supply rails. The receivers can handle up to ± 25 volts while presenting 3 to 7 kilohms impedance. Hysteresis in the receivers aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-D and V.28 applications.

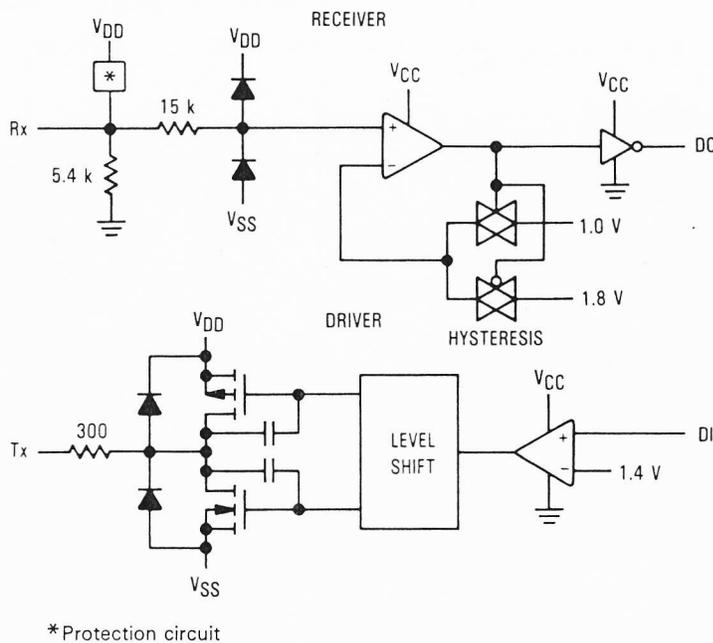
Drivers

- ± 5 to ± 12 V Supply Range
- 300 Ohms Power-Off Source Impedance
- Output Current Limiting
- TTL Compatible
- Maximum Slew Rate = $30 \text{ V}/\mu\text{s}$

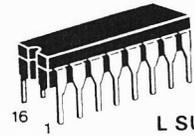
Receivers

- ± 25 V Input Voltage Range When $V_{DD} = 12 \text{ V}$, $V_{SS} = -12 \text{ V}$
- 3 to 7 Kilohms Input Impedance
- Hysteresis on Input Switchpoint

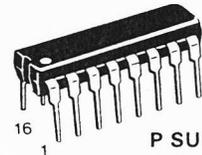
FUNCTION DIAGRAM



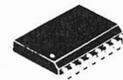
MC145406



L SUFFIX
CASE 620
CERAMIC

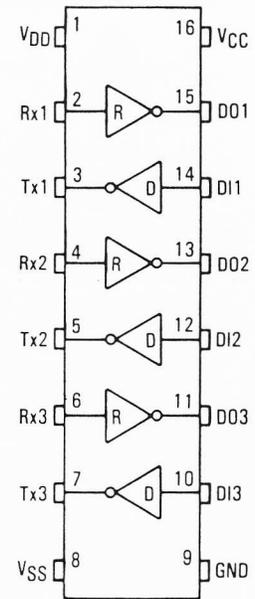


P SUFFIX
CASE 648
PLASTIC



DW SUFFIX
CASE 751G
SOIC

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER



MOTOROLA

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	-0.5 to +13.5 +0.5 to -13.5 -0.5 to 6.0	V
Input Voltage Range Rx1-3 Inputs DI1-3 Inputs	V_{IR}	$(V_{SS} - 15)$ to $(V_{DD} + 15)$ -0.5 to $(V_{CC} + 0.5)$	V
DC Current Per Pin		± 100	mA
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_A	-40 to +85	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-85 to +150	$^{\circ}\text{C}$

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \leq V_{DI} \leq V_{DD}$ and $GND \leq V_{DO} \leq V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS} - 15 \text{ V}) \leq V_{Rx1-3} \leq (V_{DD} + 15 \text{ V})$, and Tx should be constrained to $V_{SS} \leq V_{Tx1-3} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and V_{SS} or V_{DD} for Rx.)

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V, $T_A = -40$ to 85°C)

Parameter	Symbol	MC145406			Unit
		Min	Typ	Max	
DC Supply Voltage V_{DD} V_{SS} V_{CC} ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	4.5 -4.5 4.5	5 to 12 -5 to -12 5.0	13.2 -13.2 5.5	V
Quiescent Supply Current (Outputs unloaded, inputs low) $V_{DD} = +12 \text{ V}$ $V_{SS} = -12 \text{ V}$ $V_{CC} = +5 \text{ V}$	I_{DD} I_{SS} I_{CC}	— — —	140 340 300	400 600 450	μA

RECEIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V, $V_{DD} = +5$ to $+12 \text{ V}$, $V_{SS} = -5$ to -12 V , $V_{DD} \geq V_{CC}$, $T_A = -40$ to 85°C)

Characteristic	Symbol	MC145406			Unit
		Min	Typ	Max	
Input Turn-on Threshold $V_{DO1-3} = V_{OL}$, $V_{CC} = 5.0 \text{ V} \pm 5\%$	Rx1-3 V_{on}	1.35	1.80	2.35	V
Input Turn-off Threshold $V_{DO1-3} = V_{OH}$, $V_{CC} = 5.0 \text{ V} \pm 5\%$	Rx1-3 V_{off}	0.75	1.00	1.25	V
Input Threshold Hysteresis $V_{CC} = 5.0 \text{ V} \pm 5\%$	Rx1-3 $V_{on} - V_{off}$	0.6	0.8	—	V
Input Resistance $(V_{SS} - 15 \text{ V}) \leq V_{Rx1-3} \leq (V_{DD} + 15 \text{ V})$	Rx1-3 R_{in}	3.0	5.4	7.0	k Ω
High-Level Output Voltage $V_{Rx1-3} = -3 \text{ V}$ to $(V_{SS} - 15 \text{ V})^*$ $I_{OH} = -20 \mu\text{A}$, $V_{CC} = +5.0 \text{ V}$ $I_{OH} = -1 \text{ mA}$, $V_{CC} = +5.0 \text{ V}$	DO1-3 V_{OH}	4.9 3.8	4.9 4.3	— —	V
Low-Level Output Voltage $V_{Rx1-3} = +3 \text{ V}$ to $(V_{DD} + 15 \text{ V})^*$ $I_{OL} = +20 \mu\text{A}$, $V_{CC} = +5.0 \text{ V}$ $I_{OL} = +2 \text{ mA}$, $V_{CC} = +5.0 \text{ V}$ $I_{OL} = +4 \text{ mA}$, $V_{CC} = +5.0 \text{ V}$	DO1-3 V_{OL}	— — —	0.01 0.02 0.5	0.1 0.5 0.7	V

*This is the range of input voltages as specified by EIA-232-D to cause a receiver to be in the high or low logic state.

DRIVER ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V, $V_{CC} = +5\text{ V} \pm 5\%$, $T_A = -40$ to 85°C)

Characteristic	Symbol	MC145406			Unit
		Min	Typ	Max	
Digital Input Voltage Logic 0 Logic 1	DI1-3 V_{IL} V_{IH}	— 2.0	— —	0.8 —	V
Input Current $V_{DI1-3} = V_{CC}$	DI1-3 I_{in}	—	—	± 1.0	μA
Output High Voltage $V_{DI1-3} = \text{Logic 0}$, $R_L = 3.0\text{ k}\Omega$ $V_{DD} = +5.0\text{ V}$, $V_{SS} = -5.0\text{ V}$ $V_{DD} = +6.0\text{ V}$, $V_{SS} = -6.0\text{ V}$ $V_{DD} = +12.0\text{ V}$, $V_{SS} = -12.0\text{ V}$	Tx1-3 V_{OH}	3.5 4.3 9.2	3.9 4.7 9.5	— — —	V
Output Low Voltage* $V_{DI1-3} = \text{Logic 1}$, $R_L = 3.0\text{ k}\Omega$ $V_{DD} = +5.0\text{ V}$, $V_{SS} = -5.0\text{ V}$ $V_{DD} = +6.0\text{ V}$, $V_{SS} = -6.0\text{ V}$ $V_{DD} = +12.0\text{ V}$, $V_{SS} = -12.0\text{ V}$	Tx1-3 V_{OL}	-4.0 -4.5 -10.0	-4.3 -5.2 -10.3	— — —	V
Off Source Resistance (Figure 1) $V_{DD} = V_{SS} = \text{GND} = 0\text{ V}$, $V_{Tx1-3} = \pm 2.0\text{ V}$	Tx1-3	300	—	—	Ω
Output Short-Circuit Current $V_{DD} = +12.0\text{ V}$, $V_{SS} = -12.0\text{ V}$ Tx1-3 shorted to GND** Tx1-3 shorted to $\pm 15.0\text{ V}$ ***	Tx1-3 I_{SC}	— —	± 22 ± 60	± 60 ± 100	mA

*The voltage specifications are in terms of absolute values.

**Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.

***This condition could exceed package limitations.

SWITCHING CHARACTERISTICS ($V_{CC} = +5\text{ V} \pm 5\%$, $T_A = -40$ to 85°C ; See Figures 2 and 3)

Characteristic	Symbol	MC145406			Unit
		Min	Typ	Max	
Drivers					
Propagation Delay Time Low-to-High $R_L = 3\text{ k}\Omega$, $C_L = 50\text{ pF}$	Tx1-3 t_{PLH}	—	300	500	ns
High-to-Low $R_L = 3\text{ k}\Omega$, $C_L = 50\text{ pF}$	t_{PHL}	—	300	500	
Output Slew Rate Minimum Load $R_L = 7\text{ k}\Omega$, $C_L = 0\text{ pF}$, $V_{DD} = 6$ to 12 V , $V_{SS} = -6$ to -12 V	Tx1-3 SR	—	± 6	± 30	$\text{V}/\mu\text{s}$
Maximum Load $R_L = 3\text{ k}\Omega$, $C_L = 2500\text{ pF}$ $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$ $V_{DD} = 5\text{ V}$, $V_{SS} = -5\text{ V}$		— —	± 3.0 —	— —	
Receivers ($C_L = 50\text{ pF}$)					
Propagation Delay Time Low-to-High	DO1-3 t_{PLH}	—	150	425	ns
High-to-Low	t_{PHL}	—	150	425	
Output Rise Time	DO1-3 t_r	—	250	400	ns
Output Fall Time	DO1-3 t_f	—	40	100	ns

PIN DESCRIPTIONS

V_{DD}—POSITIVE POWER SUPPLY (PIN 1)

The most positive power supply pin, which is typically 5 to 12 volts.

V_{SS}—NEGATIVE POWER SUPPLY (PIN 8)

The most negative power supply pin, which is typically -5 to -12 volts.

V_{CC}—DIGITAL POWER SUPPLY (PIN 16)

The digital supply pin, which is connected to the logic power supply (maximum +5.5 volts). V_{CC} must be less than or equal to V_{DD}.

GND—GROUND (PIN 9)

Ground return pin is typically connected to the signal ground pin of the EIA-232-D connector (connector pin 7) as well as to the logic power supply ground.

Rx1, Rx2, Rx3—RECEIVE DATA INPUT (PINS 2, 4, 6)

These are the EIA-232-D receive signal inputs whose voltages can range from (V_{DD} + 15 V) to (V_{SS} - 15 V). A voltage between +3 and (V_{DD} + 15 V) is decoded as a space and causes the corresponding DO pin to swing to ground (0 V); a voltage between -3 and (V_{SS} - 15 V) is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8 volts above ground, and includes 800 millivolts of hysteresis for noise rejection. The nominal input impedance is 5 kilohms. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.

DO1, DO2, DO3—DATA OUTPUT (PINS 11, 13, 15)

These are the receiver digital output pins, which swing from V_{CC} to ground. A space on the Rx pin causes DO to produce a logic zero; a mark produces a logic one. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3—DATA INPUT (PINS 10, 12, 14)

These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4 volts above ground. However, 5-volt CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and ground.

Tx1, Tx2, Tx3—TRANSMIT DATA OUTPUT (PINS 3, 5, 7)

These are the EIA-232-D transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic one at a DI input causes the corresponding Tx output to swing toward V_{SS}. A logic zero causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30 volts per microsecond. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300 ohms.

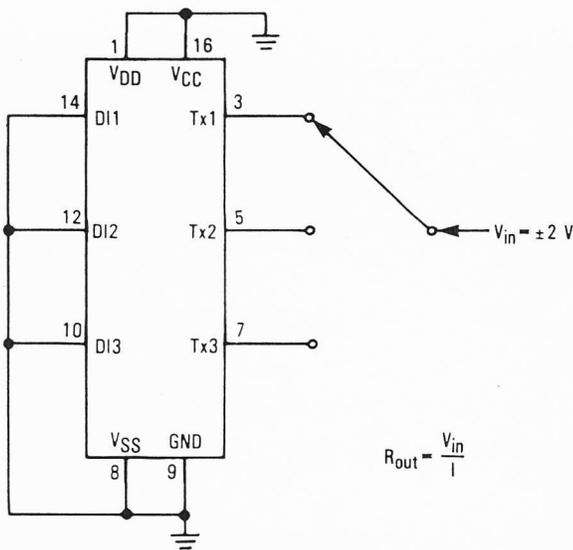


Figure 1. Power-Off Source Resistance (Drivers)

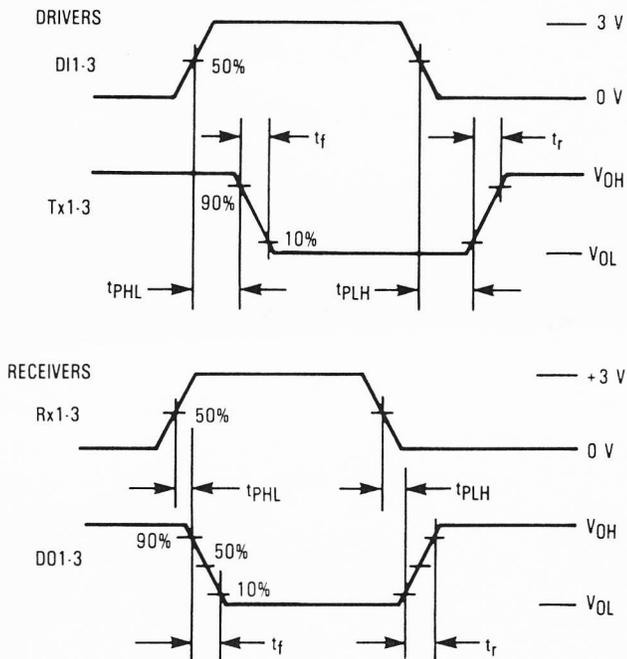


Figure 2. Switching Characteristics

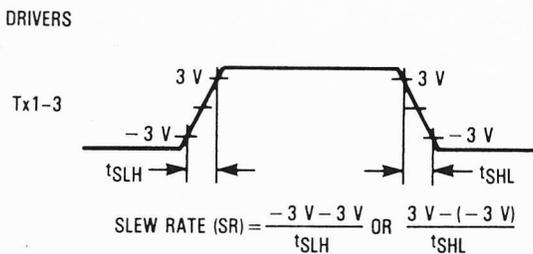


Figure 3. Slew Rate Characterization

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-D and CCITT V.28. EIA-232-D defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads. These leads, referred to as interchange circuits, allow the transfer of timing, data, control, and test signals. Electrically this transfer requires level shifting between the TTL/CMOS logic levels of the computer or modem and the high voltage levels of EIA-232-D, which can range from ± 3 to ± 25 volts. The MC145406, provides the necessary level shifting as well as meeting other aspects of the EIA-232-D specification.

DRIVERS

As defined by the specification, an EIA-232-D driver presents a voltage of between ± 5 to ± 15 volts into a load of between 3 to 7 kilohms. A logic one at the driver input results in a voltage of between -5 to -15 volts. A logic zero results in a voltage between $+5$ to $+15$ volts. When operating V_{DD} and V_{SS} at ± 7 to ± 12 volts, the MC145406 meets this requirement. When operating at ± 5 volts, the MC145406 drivers produce less than ± 5 volts at the output (when terminated), which does not meet EIA-232-D specification. However, the output voltages when using a ± 5 volt power supply are high enough (around ± 4 volts) to permit proper reception by an EIA-232-D receiver, and can be used in applications where strict compliance to EIA-232-D is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-D cable. The worst-case condition that is permitted by EIA-232-D is a ± 15 volt source that is current limited to 500 milliamperes. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300 ohm output impedance needed to satisfy the EIA-232-D driver requirements. This will reduce the short circuit current to under 40 mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30 volts per microsecond.

RECEIVERS

The job of an EIA-232-D receiver is to level-shift voltages in the range of -25 to $+25$ volts down to TTL/CMOS logic levels (0 to $+5$ volts). A voltage of between -3 and -25 volts on Rx1 is defined as a mark and produces a logic one at DO1. A voltage between $+3$ and $+25$ volts is a space and produces a logic zero. While receiving these signals, the Rx inputs must present a resistance between 3 and 7 kilohms. Nominally, the input resistance of the Rx1-3 inputs is 5.4 kilohms.

The input threshold of the Rx1-3 inputs is typically biased at 1.8 volts above ground (GND) with typically 800 millivolts of hysteresis included to improve noise immunity. The 1.8 volt bias forces the appropriate DO pin to a logic one when its Rx input is open or grounded as called for in the EIA-232-D specification. Notice that TTL logic levels can be applied to the Rx inputs in lieu of normal EIA-232-D signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-D connector is necessary with TTL devices. However, it is important not to connect the EIA-232-D outputs (Tx1-3) to TTL inputs since TTL operates off $+5$ volts only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from digital power supply. The Tx and Rx sections are independently powered by V_{DD} and V_{SS} so that one may run logic at $+5$ volts and the EIA-232-D signals at ± 12 volts.

POWER SUPPLY CONSIDERATIONS

V_{CC} should not exceed V_{DD} by more than 0.5 volts. Due to an internal diode between V_{DD} and V_{CC} , the power-up or power-down power supply sequences may permit V_{CC} to be greater than V_{DD} for a short period of time. This condition could cause parts to fail for longer periods of time. A diode as shown in Figure 4 can be used to protect the device from this condition.

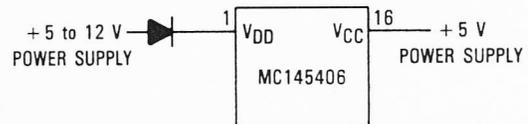
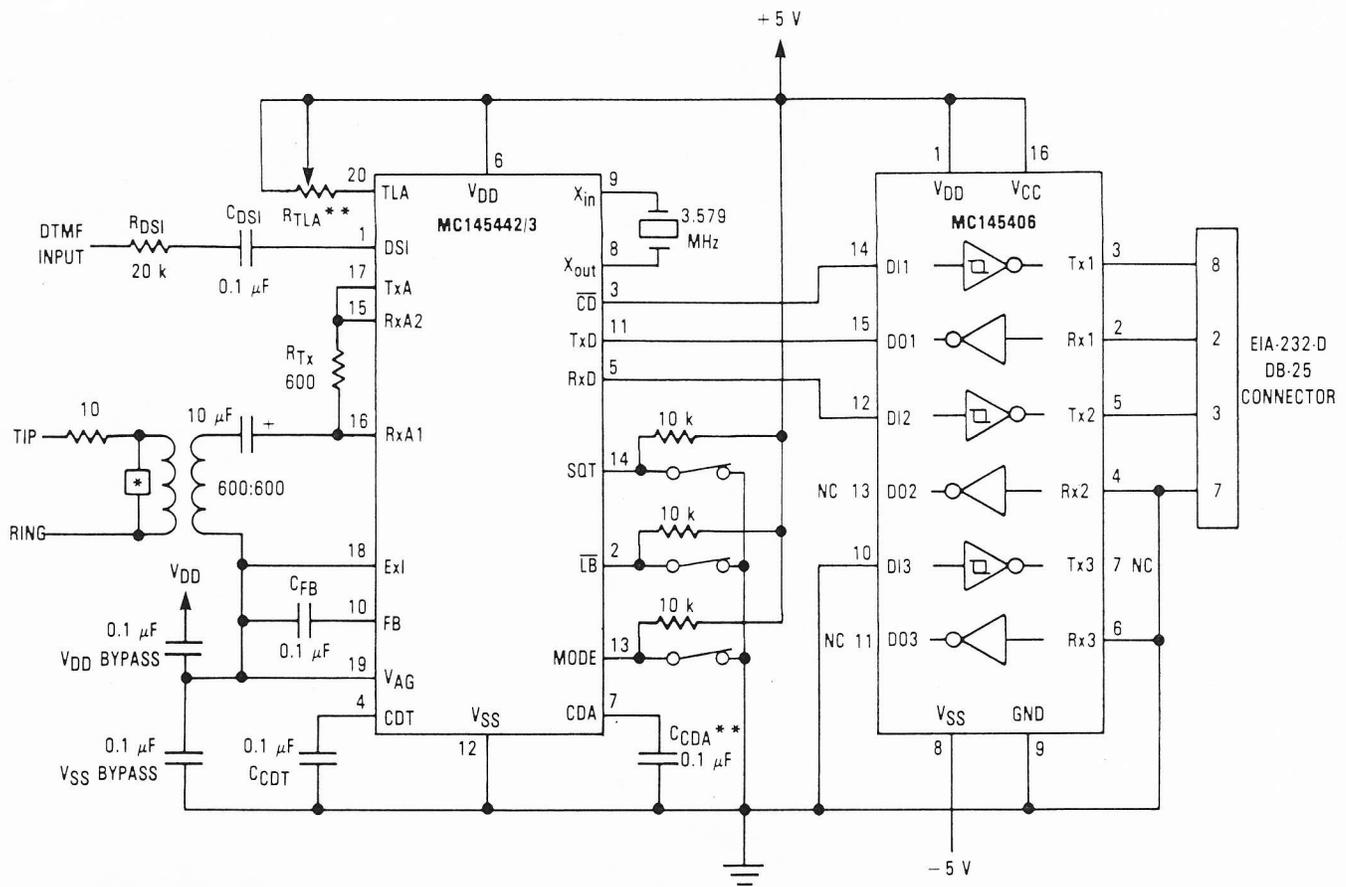


Figure 4. Protection Diode for $V_{CC} > V_{DD}$ Condition



*Line protection circuit

**Refer to the applications information for values of C_{CDA} and R_{TLA}

Figure 5. 5-Volt 300-Baud Modem with EIA-232-D Interface

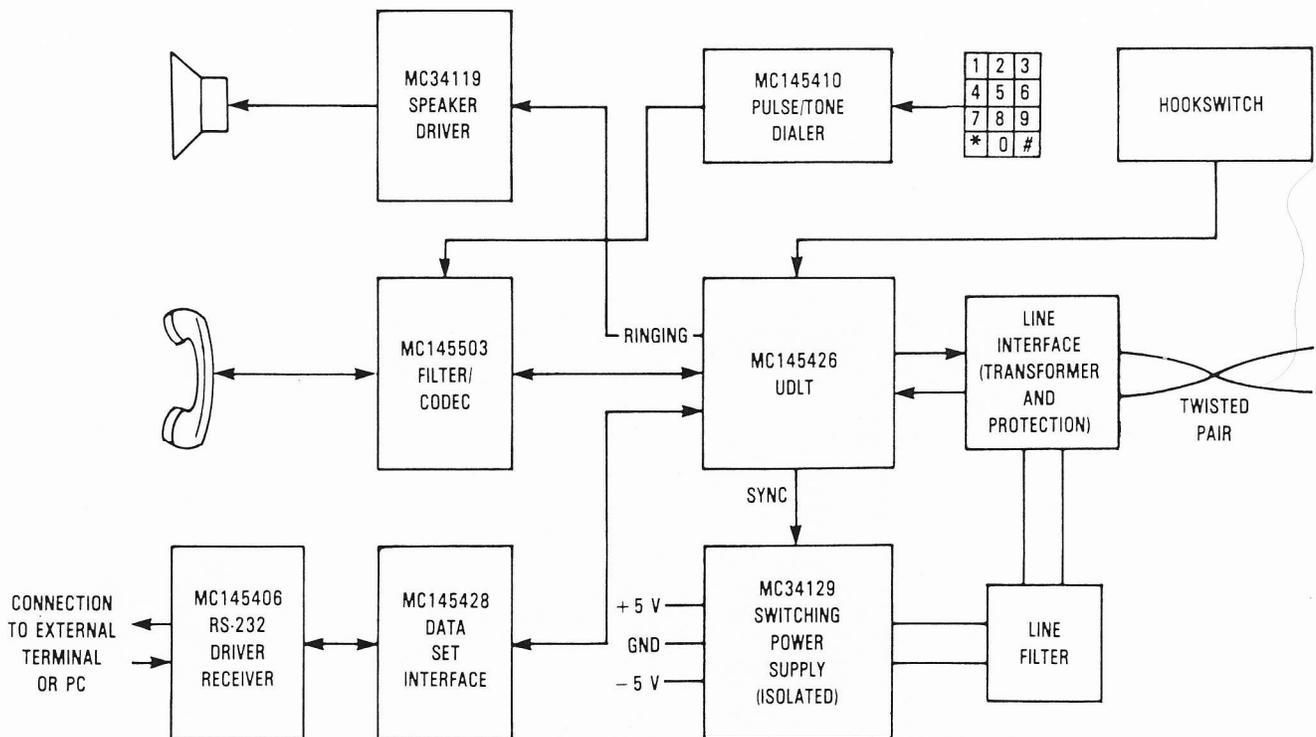


Figure 6. Line-Powered Voice/Data Telephone with Electrically Isolated EIA-232-D Interface

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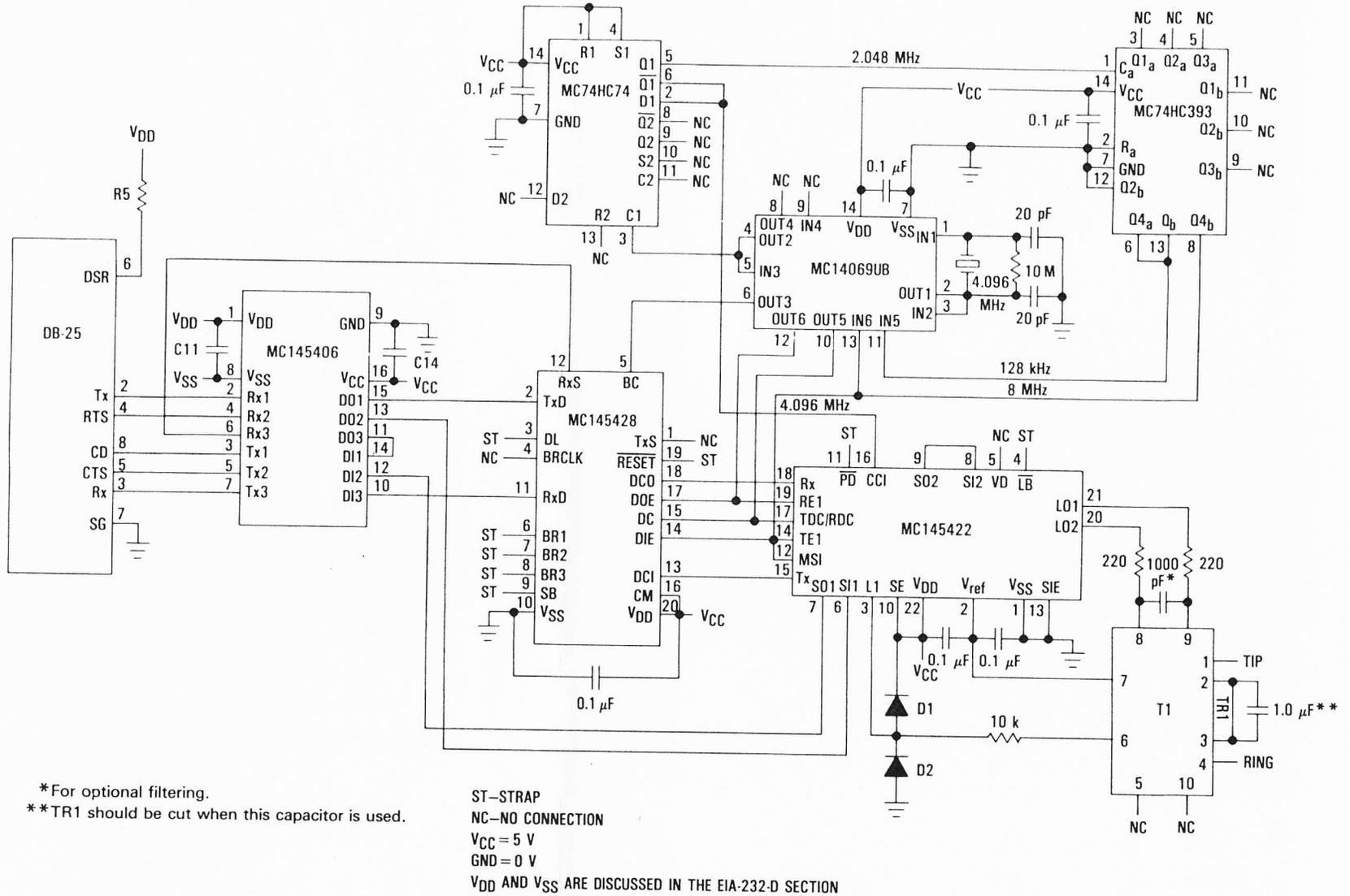
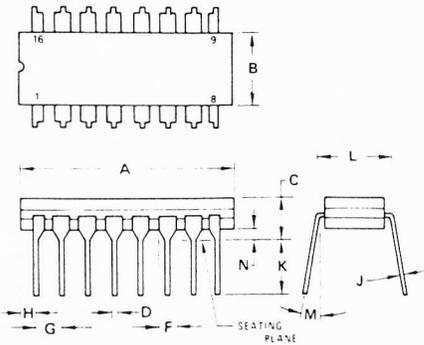


Figure 7. 80 kbps Limited Distance Modem with EIA-232-D Interface (Master)

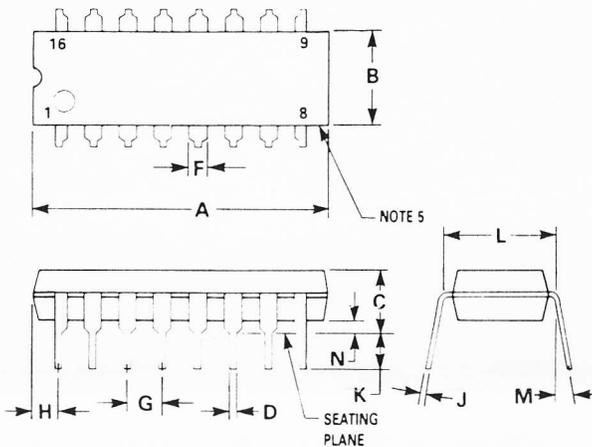
PACKAGE DIMENSIONS



- 1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- 2 PACKAGE INDEX NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
- 3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 4 DIM "A" AND "B" DO NOT INCLUDE GLASS RUN-OUT.
- 5 DIM "F" MAY NARROW TO 0.76 mm (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

L SUFFIX CERAMIC CASE 620-08

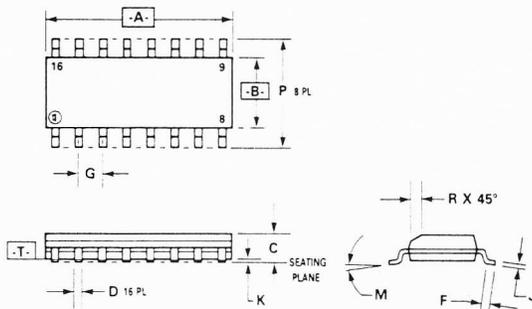
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	-	5.08	-	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	-	15°	-	15°
N	0.51	1.02	0.020	0.040



- NOTE 5
- 1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 - 2 DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - 3 DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
 - 4 "F" DIMENSION IS FOR FULL LEADS.
 - 5 ROUNDED CORNERS OPTIONAL.

P SUFFIX PLASTIC CASE 648-06

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0	10	0	10
N	0.39	1.01	0.015	0.040



- 1 DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
- 2 POSITIONAL TOLERANCE FOR D DIMENSION (16 PLACES):
 $\pm 0.25 (0.010) \text{ M T B S A S}$
- 3 POSITIONAL TOLERANCE FOR P DIMENSION (8 PLACES):
 $\pm 0.25 (0.010) \text{ M B M}$
- 4 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 5 CONTROLLING DIMENSION: MILLIMETER.
- 6 DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 7 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

DW SUFFIX SOIC CASE 751G-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
	0.25	0.75	0.010	0.029

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