commodore
semiconductor group
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6523 TRI-PORT INTERFACE

CONCEPT . . .

The 6523 TRI-PORT Interface (TPI) is designed to simplify the implementation of complex I/O operations in microcomputer systems. It has three dedicated 8-bit I/O ports which provide 24 individually programmable I/O lines.

FEATURES:

- 24 individually programmable I/O lines
- Completely static operation
- Two TTL Drive Capability
- 6 directly addressable registers
- 1 MHz, 2MHz and 3MHz operation

6523 Addressing

6523 REGISTERS/(Direct Addressing)		
*000	R0	PRA — Port Register A
001	R1	PRB — Port Register B
010	R2	PRC — Port Register C
011	R3	DDRA — Data Direction Register A
100	R4	DDRB — Data Direction Register B
101	R5	DDRC — Data Direction Register
110	}	Illegal States
111	}	Illegal States

*NOTE: RS2, RS1, RS0 respectively

ORDER NUMBER:

MXS 6523

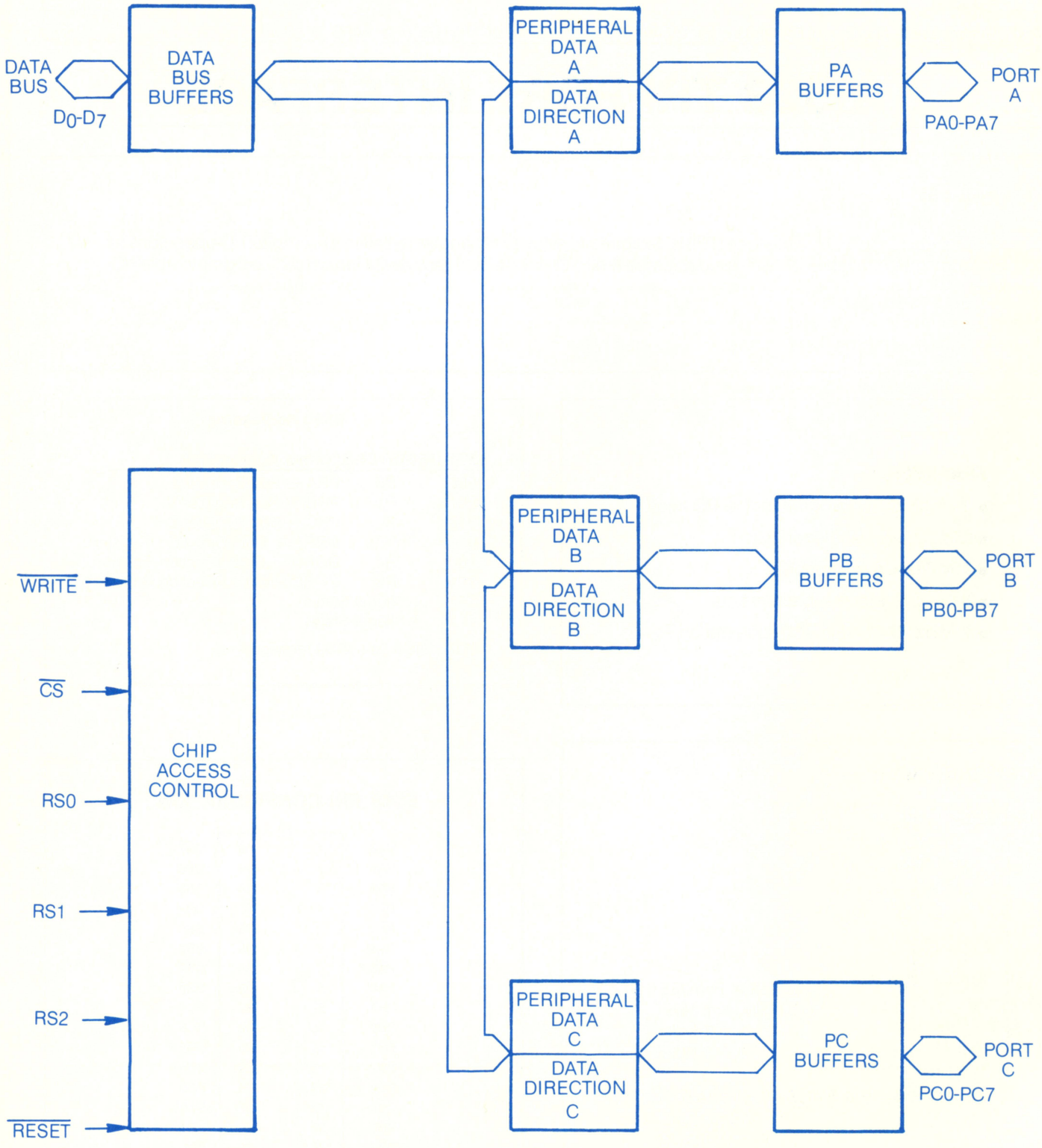
FREQUENCY RANGE
NO SUFFIX = 1 MHz
A = 2 MHz
B = 3 MHz

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

6523 PIN CONFIGURATION

V_{SS}	1	40	DB7
PA0	2	39	DB6
PA1	3	38	DB5
PA2	4	37	DB4
PA3	5	36	DB3
PA4	6	35	DB2
PA5	7	34	DB1
PA6	8	33	DB0
PA7	9	32	PC7
PB0	10	31	PC6
PB1	11	30	PC5
PB2	12	29	PC4
PB3	13	28	PC3
PB4	14	27	PC2
PB5	15	26	PC1
PB6	16	25	PC0
PB7	17	24	RS0
$\overline{CS}$	18	23	RS1
$\overline{WRITE}$	19	22	RS2
V_{DD}	20	21	$\overline{RST}$

6523 INTERNAL ARCHITECTURE



MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	−0.3 to +7.0	V_{dc}
INPUT VOLTAGE	V_{in}	−0.3 to +7.0	V_{dc}
OPERATING TEMPERATURE RANGE	T_A	0 to +70	°C
STORAGE TEMPERATURE RANGE	T_{stg}	−55 to +150	°C

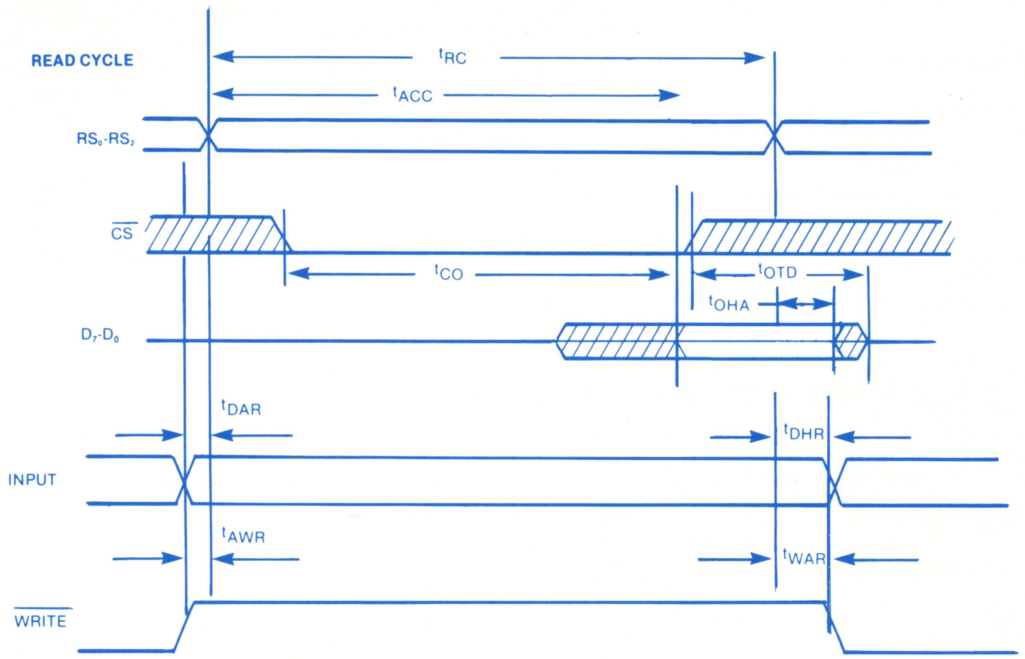
This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0V, T_A = 0° to 70°C)

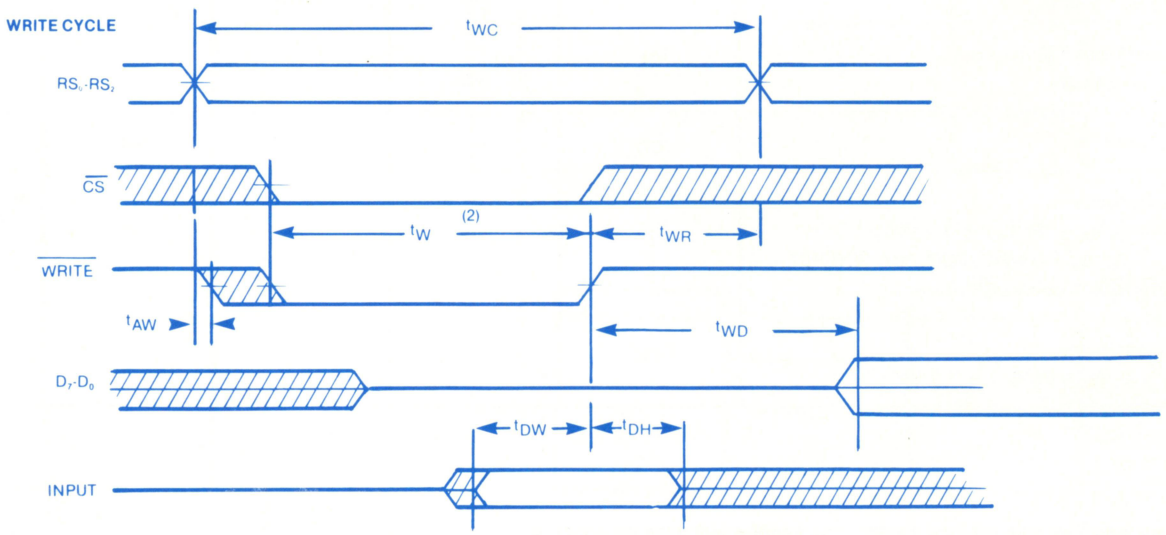
CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	—	+.8	Vdc
Input Leakage Current V_{in} = 0 to 5.0 Vdc $\overline{WRITE}$ $\overline{RST}$, $\overline{CS}$, RS_0-RS_2	I_{IN}	—	±1.0	±2.5	μAdc
Three-State (Off State Input Current) (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) DØ-D7	I_{TSI}	—	±2.0	±10	μAdc
Output High Voltage (V_{CC} = min, Load = 200 μAdc)	V_{OH}	2.4	—	—	Vdc
Output Low Voltage (V_{CC} = min, Load = 3.2 mAdc)	V_{OL}	—	—	+0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 Vdc)	I_{OH}	−200	−1000	—	μAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	3.2	—	—	mAdc
Supply Current	I_{CC}	—	50	100	mA
Input Capacitance (V_{in} = O, T_A = 25°C, f = 1.0 MHz) DØ-D7, PAØ-PA7, PBØ-PB7, PCO-PC7, $\overline{WRITE}$ $\overline{RST}$, RS_0-RS_2, $\overline{CS}$	C_{in}	—	—	10	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	—	—	10	pF

Note: Negative sign indicates outward current flow, positive indicates inward flow.

READ CYCLE



WRITE CYCLE



READ CYCLE

Symbol	Parameter	1MHz MIN	1MHz MAX	2MHz MIN	2MHz MAX	3MHz MIN	3MHz MAX	UNITS
t_{RC}	Read Cycle Time	700		350		220		nS
t_{ACC}	Access time	450		200		130		nS
t_{CO}	Chip Select to Output Valid	450		200		130		nS
t_{OTD}	Chip Deselected to Output Off	0	100	0	100	0	100	nS
t_{OHA}	Output Hold From Address Change	50		50		50		nS
t_{DAR}	Peripheral Data Set-Up	90		80		60		nS
t_{DHR}	Peripheral Data Hold	0		0		0		nS
t_{AWR}	Write to Address Setup	0		0		0		nS
t_{WAR}	Write to Address Hold	0		0		0		nS

WRITE CYCLE

Symbol	Parameter	1MHz MIN	1MHz MAX	2MHz MIN	2MHz MAX	3MHz MIN	3MHz MAX	UNITS
t_{WC}	Write Cycle Time	700		350		220		nS
t_{AW}	Address to write set-up time	0		0		0		nS
t_{W}	Write Pulse Width	450		200		130		nS
t_{WR}	Write Release Time	250		150		90		nS
t_{DW}	Data to Write Overlap	150		75		75		nS
t_{DH}	Data Hold	50		50		50		nS
t_{WD}	Write to Peripheral Output	1000		500		330		nS