commodore
semiconductor group
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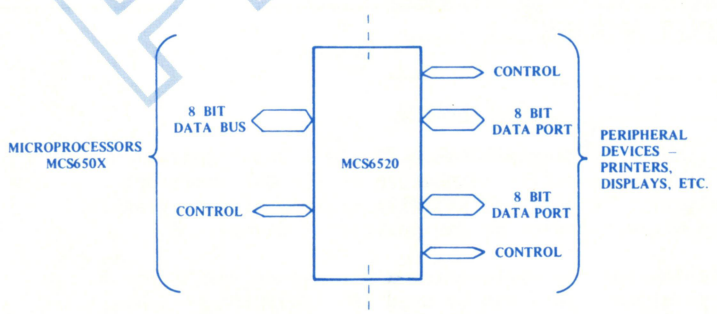
MCS6520 PERIPHERAL ADAPTER

DESCRIPTION

The MCS6520 Peripheral Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the MCS6500 family of microprocessors, the MCS6520 allows implementation of very complex systems at a minimum overall cost.

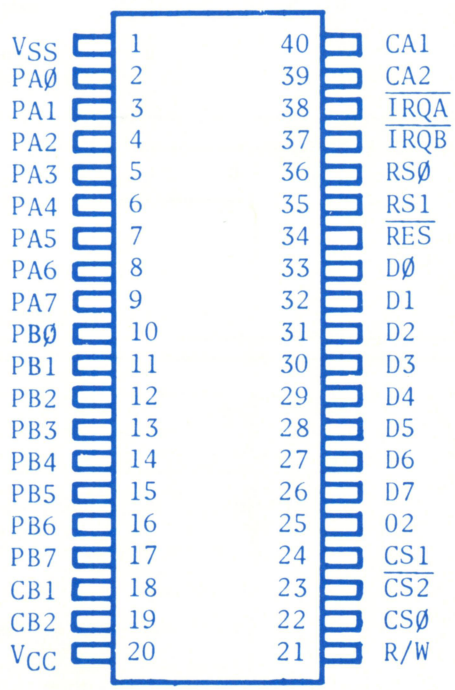
Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.

- High performance replacement for Motorola/AMI/MOSTEK/Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows very positive control of data transfers between processor and peripheral devices.



Basic MCS6520 Interface Diagram

MCS6520



SUMMARY OF MCS6520 OPERATION

See MOS TECHNOLOGY Microcomputer Hardware Manual for detailed description of MCS6520 operation.

CA1/CBI CONTROL

CRA (CRB) Bit 1	CRA (CRB) Bit 0	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
0	0	negative	Disable--remain high
0	1	negative	Enable--goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	positive	Disable--remain high
1	1	positive	Enable--as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB) Bit 5	CRA (CRB) Bit 4	CRA (CRB) Bit 3	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Output
0	0	0	negative	Disable--remains high
0	0	1	negative	Enable--goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	positive	Disable--remains high
0	1	1	positive	Enable--as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

CRA Bit 5	CRA Bit 4	CRA Bit 3	Mode	Description
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB Bit 5	CRB Bit 4	CRB Bit 3	Mode	Description
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V_{dc}
Input Voltage	V_{in}	-0.3 to +7.0	V_{dc}
Operating Temperature Range	T_A	0 to +70	^oC
Storage Temperature Range	T_{stg}	-55 to +150	^oC

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

STATIC D.C. CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage (Normal Operating Levels)		V_{IH}	+2.0	-	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)		V_{IL}	-0.3	-	+.8	Vdc
Input Threshold Voltage		V_{IT}	0.8	-	2.0	Vdc
Input Leakage Current		I_{IN}				µAdc
(V_{in} = 0 to 5.0 Vdc)	R/W,$\overline{Reset}$,RSØ,RS1,CSØ,CS1,$\overline{CS2}$,CA1,CB1,Φ2		-	±1.0	±2.5	
Three-State (Off State Input Current		I_{TSI}				
(V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max)	DØ-D7,PBØ-PB7,CB2		-	±2.0	±10	µAdc
Input High Current		I_{IH}				
(V_{IH} = 2.4 Vdc)	PAØ-PA7,CA2		-100	-250	-	µAdc
Input Low Current		I_{IL}				
(V_{IL} = 0.4 Vdc)	PAØ-PA7,CA2		-	-1.0	-1.6	mAdc
Output High Voltage		V_{OH}				
(V_{CC} = min, I_{Load} = -100 µAdc)			2.4	-	-	Vdc
Output Low Voltage		V_{OL}				
(V_{CC} = min, I_{Load} = 1.6 mAdc)			-	-	+0.4	Vdc
Output High Current (Sourcing)		I_{OH}				
(V_{OH} = 2.4 Vdc)			-100	-1000	-	µAdc
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base)	PBØ-PB7,CB2		-1.0	-2.5	-	mAdc
Output Low Current (Sinking)		I_{OL}				
(V_{OL} = 0.4 Vdc)			1.6	-	-	mAdc
Output Leakage Current (Off State)	$\overline{IRQA}$, $\overline{IRQB}$	I_{off}	-	1.0	10	uAdc
Power Dissipation		P_D	-	200	500	mW
Input Capacitance		C_{in}				pF
(V_{in} - 0, T_A = 25°C, f = 1.0 MHz)	DØ-D7, PAØ-PA7,PBØ-PB7,CA2,CB2		-	-	10	
	R/W,$\overline{Reset}$,RSØ,RS1,CSØ,CS1,CS2,		-	-	7.0	
	CA1,CB1,Φ2		-	-	20	
Output Capacitance		C_{out}				
(V_{in} - 0, T_A = 25°C, f = 1.0 MHz)			-	-	10	pF

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

FIGURE 1 – READ TIMING CHARACTERISTICS

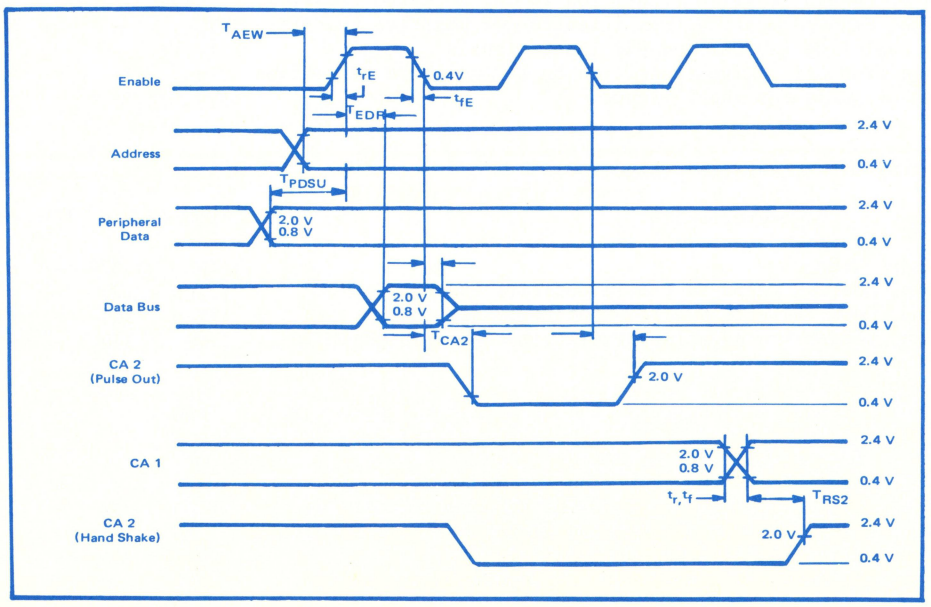
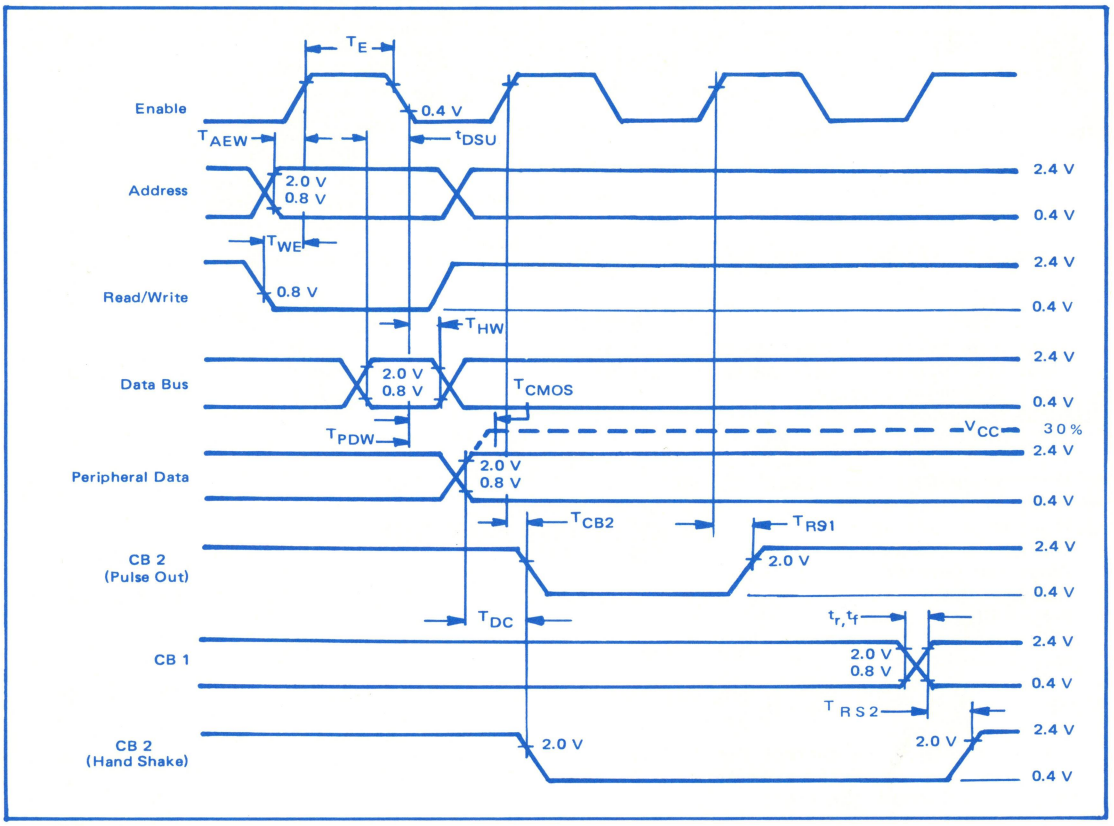


FIGURE 2 – WRITE TIMING CHARACTERISTICS



A.C. CHARACTERISTICS

Read Timing Characteristics (Figure 1, Loading 130 pF and one TTL load)

Characteristics	Symbol	Min	Typ	Max	Unit
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	-	-	ns
Delay Time, Enable positive transition to Data valid on bus	T_{EDR}	-	-	395	ns
Peripheral Data Setup Time	T_{PDSU}	300	-	-	ns
Data Bus Hold Time	T_{HR}	10	-	-	ns
Delay Time, Enable negative transition to CA2 negative transition	T_{CA2}	-	-	1.0	us
Delay Time, Enable negative transition to CA2 positive transition	T_{RS1}	-	-	1.0	us
Rise and Fall Time for CA1 and CA2 input signals	t_r, t_f	-	-	1.0	us
Delay Time from CA1 active transition to CA2 positive transition	T_{RS2}	-	-	2.0	us
Rise and Fall Time for Enable input	t_{rE}, t_{fE}	-	-	25	us

Write Timing Characteristics (Figure 2)

Characteristics	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T_E	0.470	-	25	µs
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	-	-	ns
Delay Time, Data valid to Enable negative transition	T_{DSU}	300	-	-	ns
Delay Time, Read/Write negative transition to Enable positive transition	T_{WE}	130	-	-	ns
Data Bus Hold Time	T_{HW}	10	-	-	ns
Delay Time, Enable negative transition to Peripheral Data valid	T_{PDW}	-	-	1.0	µs
Delay Time, Enable negative transition to Peripheral Data Valid, CMOS (V_{CC} - 30%) PAØ-PA7, CA2	T_{CMOS}	-	-	2.0	µs
Delay Time, Enable positive transition to CB2 negative transition	T_{CB2}	-	-	1.0	µs
Delay Time, Peripheral Data valid to CB2 negative transition	T_{DC}	0	-	1.5	µs
Delay Time, Enable positive transition to CB2 positive transition	T_{RS1}	-	-	1.0	µs
Rise and Fall Time for CB1 and CB2 input signals	t_r, t_f	-	-	1.0	µs
Delay Time, CB1 active transition to CB2 positive transition	T_{RS2}	-	-	2.0	µs