Data Book

GTE MICROCIRCUITS

GTE Microcircuits

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1 Microprocessors Microcomputers Peripherals

GTE MICROCIRCUITS

GTE Microcircuits

G65SCXX Series
G65SC1XX Series

Microcircuits

CMOS G65SCXXX 8-Bit Microprocessor Family

Features

- CMOS family that is compatible with NMOS 6500 series microprocessors
- Uses single +5 volt power supply
- Low power consumption (4mA @ 1 MHz) allows battery-powered operation
- Enhanced instruction set: 27 additional op codes encompassing eight new instructions enhance software performance compared to existing NMOS 6500 microprocessor instruction set
  —64 microprocessor instructions
  —178 operational codes
  —15 addressing modes
- Choice of 4K, 8K or 65K-byte addressable memory
- 1, 2, 3 or 4 MHz operation
- Choice of external or on-board clock generator operation
- On-board clock generator/oscillator can be driven by an external single-phase clock input, an RC network, or a crystal circuit
- Advanced memory access timing (ϕ4) on selected versions
- Early address valid allows use with slower memories
- Early write data for dynamic memories
- 8-bit parallel processing
- Decimal and binary arithmetic
- Pipeline architecture
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800
- Available on selected versions, a memory lock output and bus enable input signals simplify multiprocessor designs
- Available in either 28 or 40 pin dual-in-line packaging

General Description

The G65SCXXX is a totally software-compatible microprocessor family manufactured using the state-of-the-art silicon gate CMOS process. The family consists of two series of devices: one series, designated G65SCXX is pin-to-pin compatible with NMOS versions of the 6500 currently on the market; the other series, designated G65SC1XX includes several enhancements not available with other designs. The family provides the designer with a wide selection of addressable memory ranges, on-board or external clocks, and input interrupt options. All of the microprocessors are software compatible within the group and all are bus compatible with MC6800 products.

As shown in Table I, the family includes 18 microprocessors of which three have on-chip oscillators while the others require an external clock generator. The G65SC02, G65SC102 or G65SC112 clock generator circuit may be driven by an external crystal (Figure 2a), an RC network (Figure 2b) or by an external clock source. The versions of the microprocessor which require an external clock source are generally intended for multiprocessor applications where maximum timing control is necessary. The three family members with on-chip oscillators are intended for high performance, low cost operations where single phase inputs, crystals, or RC inputs provide the time base.

Ten of the microprocessors in the G65SCXX Series are pin-to-pin compatible with the NMOS 6500 microprocessors offered by several other manufacturers. However, the use of the leading-edge CMOS process technology ensures several software or programming enhancements not available to users of the NMOS 6500. The enhancements include two additional addressing modes, an expanded microprocessor instruction set (from 56 to 64 instructions), and expanded operational codes (from 151 to 178). In addition, a series of operational enhancements are provided which materially improve the effective use of the microprocessor. These enhancements are explained in Table V of the section of this data sheet devoted to system software and programming. This series of microprocessors provides the user an architecture and instruction set with which he is basically familiar (6502), the several operational enhancements notwithstanding, plus all of the advantages of leading edge CMOS technology; i.e., increased noise immunity, higher reliability, and greatly reduced power consumption, (Continued on page 2)

TABLE I. G65SCXXX FAMILY MICROPROCESSOR CAPABILITIES

ITEM NO.	PART NUMBER	DIP PINS	ADDRESSABLE MEMORY (BYTES)	ON-BOARD CLOCK OSCILLATOR (SEE NOTE)	EXTERNAL CLOCK GENERATOR REQUIRED	ADVANCED MEMORY ACCESS (ϕ4)	$\overline{IRQ}$	$\overline{NMI}$	$\overline{SO}$	DBE	BE	SYNC	RDY	$\overline{ML}$	$\overline{RES}$
1	G65SC02	40	65K	•			•	•	•			•	•		•
2	G65SC03	28	4K		•		•	•							•
3	G65SC04	28	8K		•		•								•
4	G65SC05	28	4K		•		•						•		•
5	G65SC06	28	4K		•		•								•
6	G65SC07	28	8K		•								•		•
7	G65SC12	40	65K		•		•	•	•	•		•			•
8	G65SC13	28	4K		•		•	•							•
9	G65SC14	28	8K		•		•								•
10	G65SC15	28	4K		•		•						•		•
11	G65SC102	40	65K	•		•	•	•	•		•	•	•	•	•
12	G65SC103	28	4K		•	•	•	•							•
13	G65SC104	28	8K		•	•	•								•
14	G65SC105	28	4K		•	•	•						•		•
15	G65SC106	28	4K		•	•	•								•
16	G65SC107	28	8K		•	•							•		•
17	G65SC112	40	65K	•			•	•	•		•	•	•	•	•
18	G65SC115	28	4K		•		•						•	•	•

NOTE: These devices can operate in any of the following clock generation modes: 1. External crystal 2. External RC network 3. ϕ0(IN) from external clock source

PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

General Description (Continued)

In addition to enhanced software programming, the use of CMOS processing also allows several hardware enhancements that are not available to users of the NMOS 6500 products. These hardware enhancements are listed and explained in Table II.

The G65SC1XX Series microprocessors (the "one-hundred" series) are a natural evolution of the 6500 product line. Basically, these products (G65SC102-107) have the same features as the G65SCXX Series, except these products also offer the designer the advantage of an on-board divide-by-four oscillator. The divide-by-four network permits the use of an economical television crystal (3.579545 MHz), plus the added advantage of increasing the access time (t_{ACC}) by approximately 25 percent.

On the G65SC102, additional features include memory lock output ($\overline{ML}$) and bus enable (BE), both of which will tend to simplify system applications. These functions are explained in the section of this data sheet entitled "Signal Description."

All versions of the G65SCXXX microprocessor family are available in plastic, ceramic, cerdip, or leadless chip carrier packaging. All versions are available in 1, 2, 3 and 4 MHz maximum operating frequencies.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_S	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = -40°C to +85°C

Parameter	Symbol	Min	Max	Unit
Input High Voltage				
ϕ0(IN), CLK (IN)		2.4	V_{DD} + 0.3	V
ϕ2 (IN)	V_{IH}	V_{DD} - 0.2	V_{DD} + 0.3	V
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, $\overline{SO}$, DBE, BE		2.0	V_{DD} + 0.3	V
Input Low Voltage				
ϕ0 (IN), CLK (IN)		-0.3	0.4	V
ϕ2 (IN)	V_{IL}	-0.3	0.2	V
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, $\overline{SO}$, DBE, BE		-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD})				
$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, $\overline{SO}$, DBE, BE (Internal Pull-Up)	I_{IN}		1.0/-100	μA
ϕ2 (IN), ϕ0 (IN), CLK (IN)			±1.0	μA
Three-State Leakage Current				
Address, Data, R/$\overline{W}$	I_{TSI}		±10.0	μA
Output High Voltage (I_{OH} = -100 μA, V_{DD} = 4.75V)				
SYNC, Data, A0-A15, R/$\overline{W}$	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 1.6 mA, V_{DD} = 4.5V)				
SYNC, Data, A0-A15, R/$\overline{W}$	V_{OL}	—	0.4	V
Supply Current f = 1 MHz	I_{CC}	—	4	mA
(No Load) f = 2 MHz			8	
f = 3 MHz			12	
f = 4 MHz			16	
Standby Power Dissipation (ϕ2 = V_{IH}, Inputs = V_{SS} or V_{DD}	P_{SBY}		50.0	μW
Outputs Unloaded)				
Capacitance (V_{IN} = 0, T_A = 25°C, f = 1 MHz)				pF
Logic, ϕ0(IN), CLK (IN)	C_{IN}	—	10	
A0-A15, R/$\overline{W}$ Data (Three-State)	C_{TS}	—	15	
ϕ2 (IN)	C2 (IN)	—	40	

AC Characteristics, G65SC02-07, G65SC12-15, G65SC112, 115: V_{DD} = 5.0V ±10%, T_A = -40° C to +85° C

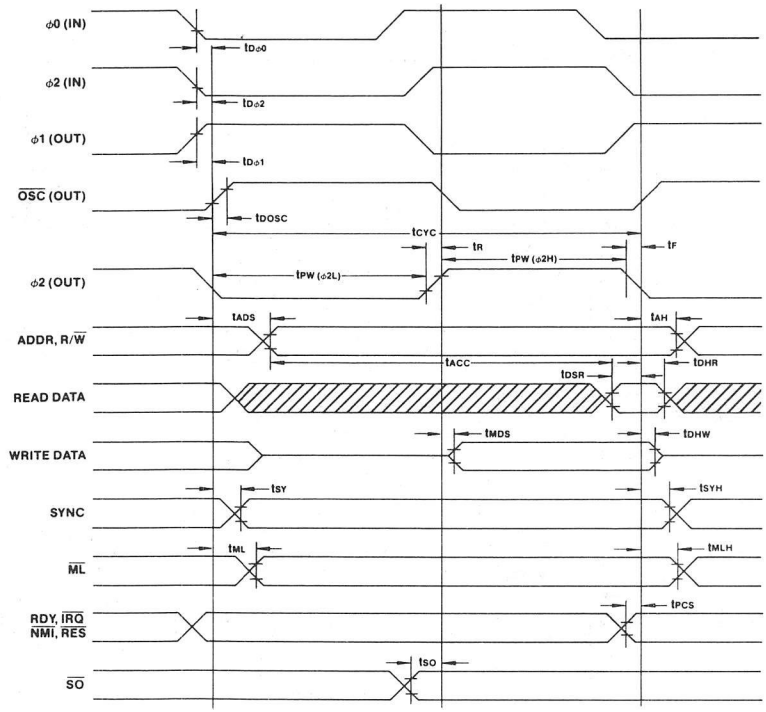
		1 MHz		2 MHz		3 MHz		4 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Delay Time, $\phi 0$ (IN) to $\phi 2$ (OUT)	$t_{D\phi 0}$	—	100	—	100	—	100	—	100	nS
Delay Time, $\phi 2$ (IN) to $\phi 2$ (OUT)	$t_{D\phi 2}$	—	75	—	75	—	75	—	75	nS
Delay Time, $\phi 1$ (OUT) to $\phi 2$ (OUT)	$t_{D\phi 1}$	—	50	—	50	—	50	—	50	nS
Delay Time, $\phi 2$ (OUT) to $\overline{OSC}$ (OUT)	t_{DOSC}	—	50	—	50	—	50	—	50	nS
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	0.33	DC	0.25	DC	μS
Clock Pulse Width Low	$t_{PW(\phi 2L)}$	470	—	240	—	160	—	115	—	nS
Clock Pulse Width High	$t_{PW(\phi 2H)}$	470	—	240	—	160	—	115	—	nS
Fall Time, Rise Time	t_F, t_R	—	25	—	25	—	15	—	15	nS
Address Hold Time	t_{AH}	15	—	15	—	15	—	10	—	nS
Address Setup Time	t_{ADS}	—	225	—	140	—	110	—	90	nS
Access Time	t_{ACC}	675	—	310	—	170	—	110	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	nS
Read Data Setup Time	t_{DSR}	100	—	50	—	50	—	50	—	nS
Write Data Delay Time	t_{MDS}	—	175	—	100	—	75	—	70	nS
Write Data Hold Time	t_{DHW}	15	—	15	—	15	—	15	—	nS
SYNC, $\overline{ML}$ Setup Time	t_{SY}, t_{ML}	—	225	—	140	—	110	—	90	nS
SYNC, $\overline{ML}$ Hold Time	t_{SYH}, t_{MLH}	—	0	—	0	—	0	—	0	nS
$\overline{SO}$ Setup Time	t_{SO}	100	—	50	—	35	—	25	—	nS
Processor Control Setup Time	t_{PCS}	200	—	200	—	150	—	120	—	nS

AC Characteristics, G65SC102-107: V_{DD} = 5.0V ±10%, T_A = -40° C to +85° C

		1 MHz		2 MHz		3 MHz		4 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Delay Time, CLK (IN) to $\phi 2$ (OUT)	t_{DCLK}	—	100	—	100	—	100	—	100	nS
Delay Time, $\overline{OSC}$ (OUT) to $\phi 2$ (OUT)	t_{DOSC}	—	75	—	75	—	75	—	75	nS
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	0.33	DC	0.25	DC	μS
Clock Pulse Width Low	$t_{PW(\phi 2L)}$	470	—	240	—	160	—	115	—	nS
Clock Pulse Width High	$t_{PW(\phi 2H)}$	470	—	240	—	160	—	115	—	nS
Fall Time, Rise Time	t_F, t_R	—	25	—	25	—	15	—	15	nS
Delay Time, $\phi 2$ (OUT) to $\phi 4$ (OUT)	t_{AVS}	—	250	—	125	—	83	—	63	nS
Address Valid to $\phi 4$ (OUT)	$t_{A\phi 4}$	50	—	25	—	16	—	12	—	nS
Address Hold Time	t_{AH}	15	—	15	—	15	—	10	—	nS
Access Time	t_{ACC}	695	—	340	—	220	—	170	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	nS
Read Data Setup Time	t_{DSR}	80	—	40	—	30	—	20	—	nS
Write Data Hold Time	t_{DHW}	15	—	15	—	15	—	15	—	nS
Write Data Delay Time	$t_{DD\phi 4}$	—	200	—	110	—	70	—	30	nS
SYNC, $\overline{ML}$ Setup Time	t_{SY}, t_{ML}	—	225	—	140	—	110	—	90	nS
SYNC, $\overline{ML}$ Hold Time	t_{SYH}, t_{MLH}	—	225	—	140	—	110	—	90	nS
$\overline{SO}$ Setup Time	t_{SO}	100	—	50	—	35	—	25	—	nS
Processor Control Setup Time	t_{PCS}	100	—	50	—	35	—	25	—	nS

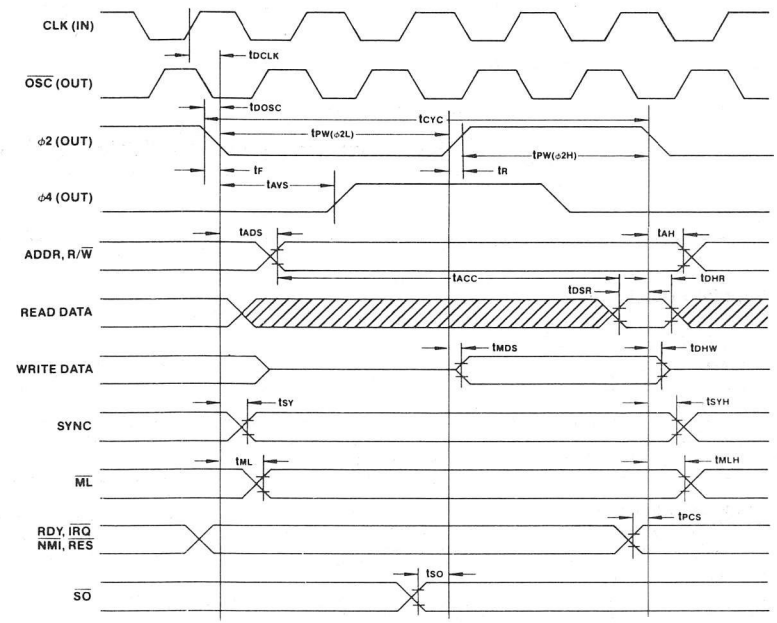
TIMING DIAGRAM:

G65SC02-07
G65SC12-15
G65SC112, 115

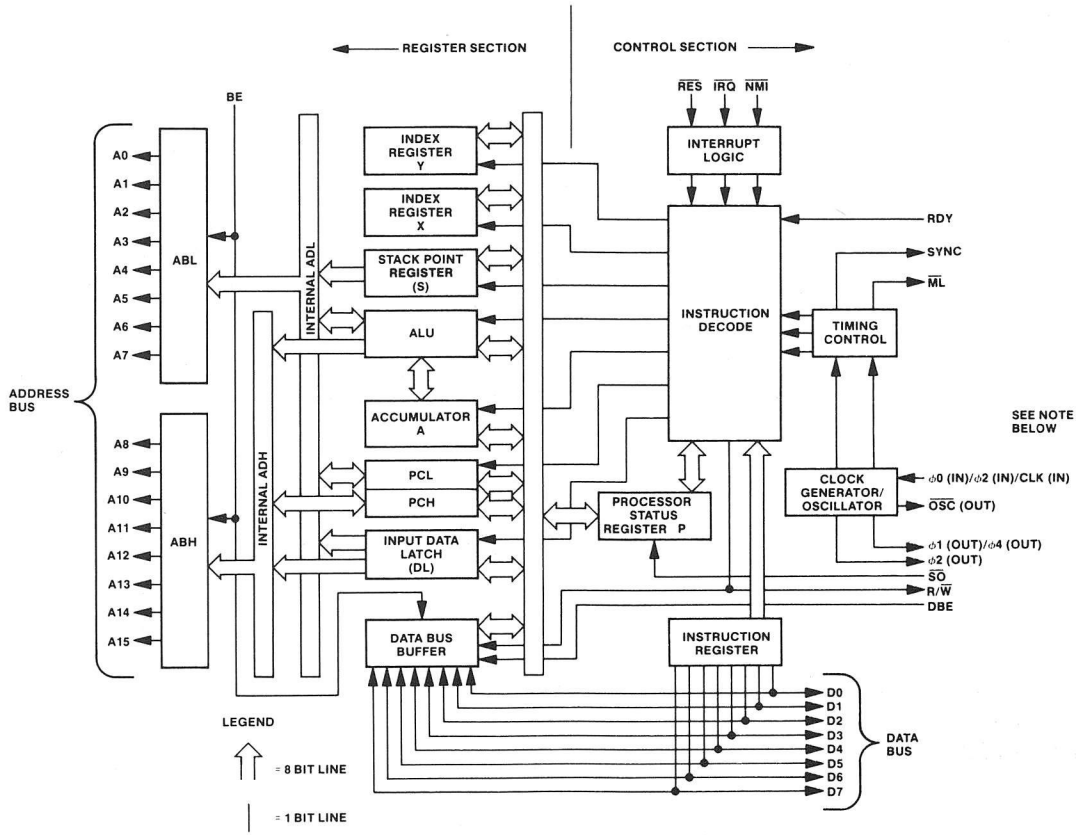


TIMING DIAGRAM:

G65SC102-107



Notes:
1. Load = 100 pF.
2. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
3. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.



Note: Refer to Table I for signal input/output applicability.

Figure 1. Internal Architecture Simplified Block Diagram

Functional Description

Timing Control
The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter
The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode
Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)
All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator
The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Functional Description (Continued)

Index Registers

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts.

Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

Signal Description

Address Bus (AO-AXX)

Refer to the particular package configuration for the respective number of address lines.

In the 40-pin package, A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The address lines are set (See BE below.) to the high impedance state by the bus enable (BE) signal. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130 pF.

Bus Enable (BE)

This signal allows external control of the data and the address output buffers and R/$\overline{W}$. For normal operation, BE is high causing the address buffers and R/$\overline{W}$ to be active and the data buffers to be active during a write cycle. For external control, BE is held low to disable the buffers.

Clock In (CLK (IN))

The 65SC10X Series is supplied with an internal clock generator operating at four times the $\phi 2$ frequency. The frequency of these clocks is externally controlled by the crystal or oscillator circuit shown in Figure 2.

Phase 0 In ($\phi 0$(IN))

This is the buffered clock input to the internal clock generator on the G65SC0X series. Clock outputs $\phi 1$(OUT) and $\phi 2$(OUT) are derived from this signal.

Phase 2 In ($\phi 2$(IN))

This is the unbuffered clock input to the internal clock generator on the G65SC1X and G65SC11X series. The clock output, $\phi 2$(OUT), is derived from this signal.

Data Bus Enable (DBE)

This TTL-compatible input allows external control of the three-state data output buffers. In normal operation, DBE would be driven by the phase two ($\phi 2$) clock, thus allowing data input from microprocessor only during $\phi 2$. During the read cycle, the data bus buffers are internally disabled, becoming essentially an open circuit. To disable the data bus externally, DBE should be held low.

Data Bus (D0-D7)

The data lines (D0-D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130 pF. The data lines are set to the high impedance state by BE or DBE.

Interrupt Request ($\overline{IRQ}$)

This TTL compatible signal requests that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ is sampled during $\phi 2$ operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during $\phi 1$. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire-OR operation.

Memory Lock ($\overline{ML}$)

In a multiprocessor system, $\overline{ML}$ indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB, TSB memory referencing instructions. This signal is low for the modify and write cycles.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The $\overline{NMI}$ is sampled during $\phi 2$; the current instruction is completed and the interrupt sequence begins during $\phi 1$. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine. However, it should be noted this is an edge-sensitive input. As a result, another interrupt will occur if there is another negative-going transition and the program has not returned from a previous interrupt. Also, no interrupt will occur if $\overline{NMI}$ is low and negative-going edge has not occurred since the last non-maskable interrupt.

Oscillator Out ($\overline{OSC}$ (OUT))

On the G65SC102 microprocessor, an internal inverter is connected between pins 35 and 37. The inverter has sufficient loop gain to provide oscillation using an external crystal.

Phase 1 Out ($\phi 1$(OUT))

This inverted $\phi 2$(OUT) signal provides timing for external R/$\overline{W}$ operations.

Phase 2 Out ($\phi 2$(OUT))

This signal provides timing for external bus R/$\overline{W}$ operations. Addresses are valid after the address setup time (t_{ADS}) from the falling edge of $\phi 2$(OUT).

Phase 4 Out ($\phi 4$(OUT))

This signal is delayed by t_{AVS} from $\phi 2$(OUT). The address output is valid prior to the rising edge of $\phi 4$(OUT).

Signal Description (Continued)

Ready (RDY)

This input signal allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state during or coincident with phase one ($\phi 1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\phi 2$) in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

Reset ($\overline{RES}$)

This input is used to reset the microprocessor. Reset must be held low for at least two clock cycles after V_{DD} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. After the system has been operating, a low on this line of at least two cycles will cease microprocessing activity.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. The previous program counter and status register values are written to the stack memory area. Then the interrupt mask flag is set, the decimal mode is cleared and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.

Read/Write (R/$\overline{W}$)

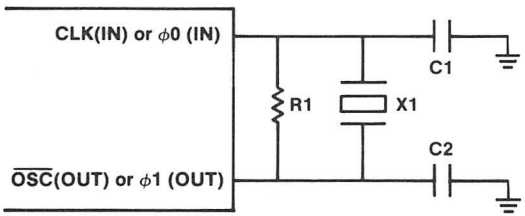
This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location. R/$\overline{W}$ is set to the high impedance state by BE.

Set Overflow ($\overline{SO}$)

A negative transition on this line sets the overflow bit in the status code register. The signal is sampled on the trailing edge of $\phi 1$

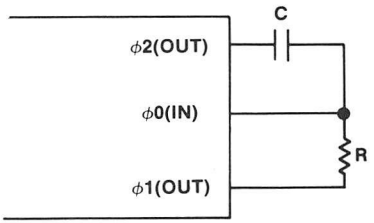
Synchronize (SYNC)

This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\phi 1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi 1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.



C1, C2 = 51pF
R1 = 200K
X1 = 1MHz

Figure 2(a). Crystal Circuit for Internal Oscillator



Suggested RC network configuration for internal oscillator.

Figure 2(b). RC Circuit for Internal Oscillator

Table II. Microprocessor Hardware Enhancements

Function	NMOS 6500	G65SCXXX Family
Oscillator.	Requires external active components.	Crystal or RC network will oscillate when connected between $\phi 0$ (IN) and $\phi 1$ (OUT).
Assertion of Ready (RDY) during write operations.	Ignored.	Stops processor during $\phi 2$.
1X series clock inputs.	Two non-overlapping clock inputs ($\phi 1$ and $\phi 2$) are required.	$\phi 2$ (IN) is the only required clock.
Unused input-only pins ($\overline{IRQ}$, $\overline{NMI}$, RDY, $\overline{RES}$, $\overline{SO}$, DBE, BE).	Must be connected to low impedance signal to avoid noise problems.	Connected internally by a high-resistance to V_{DD} (approximately 1 Megohm).

Addressing Modes

Fifteen addressing modes are available to the user of the GTE G65SCXXX family of microprocessors. The addressing modes are described in the following paragraphs:

Implied Addressing
In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Accumulator Addressing
This form of addressing is represented with a one byte instruction and implies an operation on the accumulator.

Immediate Addressing
With immediate addressing, the operand is contained in the second byte of the instruction; no further memory addressing is required.

Absolute Addressing
For absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Therefore, this addressing mode allows access to the total 65K bytes of addressable memory.

Zero Page Addressing
Zero page addressing allows shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. The careful use of zero page addressing can result in significant increase in code efficiency.

Absolute Indexed Addressing
Absolute indexed addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Zero Page Indexed Addressing
Zero page absolute addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page boundaries does not occur.

Relative Addressing
Relative addressing is used only with branch instruction; it establishes a destination for the conditional branch.

Zero Page Indexed Indirect Addressing
With zero page indexed indirect addressing (usually referred to as Indirect X) the second byte of the instruction is added to the contents of the X index register; the carry is discarded. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Absolute Indexed Indirect Addressing (Jump Instruction Only)
With absolute indexed indirect addressing, the contents of the second and third instruction bytes are added to the X register. The result of this addition points to a memory location containing the lower-order eight bits of the effective address. The next memory location contains the higher-order eight bits of the effective address.

Indirect Indexed Addressing
This form of addressing is usually referred to as Indirect, Y. The second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Zero Page Indirect Addressing
In this form of addressing, the second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits is always zero. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address.

Absolute Indirect Addressing (Jump Instruction Only)
The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the 16 bits of the program counter.

Figure 3. Microprocessor Programming Model

Table III. Instruction Set—Alphabetical Sequence

	ADC	Add Memory to Accumulator with Carry
	AND	"AND" Memory with Accumulator
	ASL	Shift One Bit Left
	BCC	Branch on Carry Clear
	BCS	Branch on Carry Set
	BEQ	Branch on Result Zero
	BIT	Test Memory Bits with Accumulator
	BMI	Branch on Result Minus
	BNE	Branch on Result Not Zero
	BPL	Branch on Result Plus
●	BRA	Branch Always
	BRK	Force Break
	BVC	Branch on Overflow Clear
	BVS	Branch on Overflow Set
	CLC	Clear Carry Flag
	CLD	Clear Decimal Mode
	CLI	Clear Interrupt Disable Bit
	CLV	Clear Overflow Flag
	CMP	Compare Memory and Accumulator
	CPX	Compare Memory and Index X
	CPY	Compare Memory and Index Y
	DEC	Decrement by One
	DEX	Decrement Index X by One
	DEY	Decrement Index Y by One
	EOR	"Exclusive-or" Memory with Accumulator
	INC	Increment by One
	INX	Increment Index X by One
	INY	Increment Index Y by One
	JMP	Jump to New Location
	JSR	Jump to New Location Saving Return Address
	LDA	Load Accumulator with Memory
	LDX	Load Index X with Memory
	LDY	Load Index Y with Memory
	LSR	Shift One Bit Right
	NOP	No Operation
	ORA	"OR" Memory with Accumulator
	PHA	Push Accumulator on Stack
	PHP	Push Processor Status on Stack
●	PHX	Push Index X on Stack
●	PHY	Push Index Y on Stack
	PLA	Pull Accumulator from Stack
	PLP	Pull Processor Status from Stack
●	PLX	Pull Index X from Stack
●	PLY	Pull Index Y from Stack
	ROL	Rotate One Bit Left
	ROR	Rotate One Bit Right
	RTI	Return from Interrupt
	RTS	Return from Subroutine
	SBC	Subtract Memory from Accumulator with Borrow
	SEC	Set Carry Flag
	SED	Set Decimal Mode
	SEI	Set Interrupt Disable Bit
	STA	Store Accumulator in Memory
	STX	Store Index X in Memory
	STY	Store Index Y in Memory
●	STZ	Store Zero in Memory
	TAX	Transfer Accumulator to Index X
	TAY	Transfer Accumulator to Index Y
●	TRB	Test and Reset Memory Bits with Accumulator
●	TSB	Test and Set Memory Bits with Accumulator
	TSX	Transfer Stack Pointer to Index X
	TXA	Transfer Index X to Accumulator
	TXS	Transfer Index X to Stack Pointer
	TYA	Transfer Index Y to Accumulator

Note: ● = New Instruction

LSD / MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK	ORA ind, X			TSB zpg	ORA zpg	ASL zpg		PHP	ORA imm	ASL A		TSB abs	ORA abs	ASL abs		0
1	BPL rel	ORA ind, Y	ORA ind		TRB zpg	ORA zpg, X	ASL zpg, X		CLC	ORA abs, Y	INC A		TRB abs	ORA abs, X	ASL abs, X		1
2	JSR abs	AND ind, X			BIT zpg	AND zpg	ROL zpg		PLP	AND imm	ROL A		BIT abs	AND abs	ROL abs		2
3	BMI rel	AND ind, Y	AND ind		BIT zpg, X	AND zpg, X	ROL zpg, X		SEC	AND abs, Y	DEC A		BIT abs, X	AND abs, X	ROL abs, X		3
4	RTI	EOR ind, X				EOR zpg	LSR zpg		PHA	EOR imm	LSR A		JMP abs	EOR abs	LSR abs		4
5	BVC rel	EOR ind, Y	EOR ind			EOR zpg, X	LSR zpg, X		CLI	EOR abs, Y	PHY			EOR abs, X	LSR abs, X		5
6	RTS	ADC ind, X			STZ zpg	ADC zpg	ROR zpg		PLA	ADC imm	ROR A		JMP ind	ADC abs	ROR abs		6
7	BVS rel	ADC ind, Y	ADC ind		STZ zpg, X	ADC zpg, X	ROR zpg, X		SEI	ADC abs, Y	PLY		JMP ind, X	ADC abs, X	ROR abs, X		7
8	BRA rel	STA ind, X			STY zpg	STA zpg	STX zpg		DEY	BIT imm	TXA		STY abs	STA abs	STX abs		8
9	BCC rel	STA ind, Y	STA ind		STY zpg, X	STA zpg, X	STX zpg, Y		TYA	STA abs, Y	TXS		STZ abs	STA abs, X	STZ abs, X		9
A	LDY imm	LDA ind, X	LDX imm		LDY zpg	LDA zpg	LDX zpg		TAY	LDA imm	TAX		LDY abs	LDA abs	LDX abs		A
B	BCS rel	LDA ind, Y	LDA ind		LDY zpg, X	LDA zpg, X	LDX zpg, Y		CLV	LDA abs, Y	TSX		LDY abs, X	LDA abs, X	LDX abs, Y		B
C	CPY imm	CMP ind, X			CPY zpg	CMP zpg	DEC zpg		INY	CMP imm	DEX		CPY abs	CMP abs	DEC abs		C
D	BNE rel	CMP ind, Y	CMP ind			CMP zpg, X	DEC zpg, X		CLD	CMP abs, Y	PHX			CMP abs, X	DEC abs, X		D
E	CPX imm	SBC ind, X			CPX zpg	SBC zpg	INC zpg		INX	SBC imm	NOP		CPX abs	SBC abs	INC abs		E
F	BEQ rel	SBC ind, Y	SBC ind			SBC zpg, X	INC zpg, X		SED	SBC abs, Y	PLX			SBC abs, X	INC abs, X		F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

Note: ▭ = New Op Codes

Figure 4. Microprocessor Op Code Table

Table IV. Operational Codes, Execution Time, and Memory Requirements

MNE-MONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	(4) IMPLIED OP	n	#	(IND, X) OP	n	#	(1) (IND), Y OP	n	#	ZPG,X OP	n	#	(1) ABS,X OP	n	#	(1) ABS,Y OP	n	#	RELATIVE (2) OP	n	#	INDIRECT OP	n	#	ZPG,Y OP	n	#	PROCESSOR STATUS CODE 7 6 4 3 2 1 0 N V B D I Z C	MNE-MONIC
ADC	A + M + C → A (3)	69	2	2	6D	4	3	65	3	2				61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3				72	5	2				N V • • • Z C	ADC
AND	A∧M → A	29	2	2	2D	4	3	25	3	2				21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3				32	5	2				N • • • • Z •	AND
ASL	C ← [7 0] ←0				0E	6	3	06	5	2	0A	2	1							16	6	2	1E	6	3												N • • • • Z C	ASL
BCC	BRANCH IF C=0																												90	2	2							• • • • • • •	BCC
BCS	BRANCH IF C=1																												B0	2	2							• • • • • • •	BCS
BEQ	BRANCH IF Z=1																												F0	2	2							• • • • • • •	BEQ
BIT	A ∧ M (5)	89	2	2	2C	4	3	24	3	2										34	4	2	3C	4	3												M_7 M_6 • • • Z •	BIT
BMI	BRANCH IF N=1																												30	2	2							• • • • • • •	BMI
BNE	BRANCH IF Z=0																												D0	2	2							• • • • • • •	BNE
BPL	BRANCH IF N=0																												10	2	2							• • • • • • •	BPL
BRA	BRANCH ALWAYS																												80	2	2							• • • • • • •	BRA
BRK	BREAK										00	7	1																									• • 1 0 1 • •	BRK
BVC	BRANCH IF V=0																												50	2	2							• • • • • • •	BVC
BVS	BRANCH IF V=1																												70	2	2							• • • • • • •	BVS
CLC	0 → C										18	2	1																									• • • • • • 0	CLC
CLD	0 → D										D8	2	1																									• • • 0 • • •	CLD
CLI	0 → I										58	2	1																									• • • • 0 • •	CLI
CLV	0 → V										B8	2	1																									• 0 • • • • •	CLV
CMP	A-M	C9	2	2	CD	4	3	C5	3	2				C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3				D2	5	2				N • • • • Z C	CMP
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																												N • • • • Z C	CPX
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																												N • • • • Z C	CPY
DEC	DECREMENT				CE	6	3	C6	5	2	3A	2	1							D6	6	2	DE	6	3												N • • • • Z •	DEC
DEX	X-1 → X										CA	2	1																									N • • • • Z •	DEX
DEY	Y-1 → Y										88	2	1																									N • • • • Z •	DEY
EOR	A ∀ M →A	49	2	2	4D	4	3	45	3	2				41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3				52	5	2				N • • • • Z •	EOR
INC	INCREMENT				EE	6	3	E6	5	2	1A	2	1							F6	6	2	FE	6	3												N • • • • Z •	INC
INX	X + 1 → X										E8	2	1																									N • • • • Z •	INX
INY	Y + 1 → Y										C8	2	1																									N • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3							7C	6	3																6C	6	3				• • • • • • •	JMP
JSR	JUMP SUB				20	6	3																															• • • • • • •	JSR
LDA	M → A	A9	2	2	AD	4	3	A5	3	2				A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3				B2	5	2				N • • • • Z •	LDA
LDX	M → X	A2	2	2	AE	4	3	A6	3	2																BE	4	3							B6	4	2	N • • • • Z •	LDX
LDY	M → Y	A0	2	2	AC	4	3	A4	3	2										B4	4	2	BC	4	3													N • • • • Z •	LDY
LSR	0→ [7 0]→ C				4E	6	3	46	5	2	4A	2	1							56	6	2	5E	6	3												0 • • • • Z C	LSR
NOP	NO OPERATION										EA	2	1																									• • • • • • •	NOP
ORA	AVM → A	09	2	2	0D	4	3	05	3	2				01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3				12	5	2				N • • • • Z •	ORA
PHA	A→Ms S-1→S										48	3	1																									• • • • • • •	PHA
PHP	P→Ms S-1→S										08	3	1																									• • • • • • •	PHP
PHX	X→Ms S-1→S										DA	3	1																									• • • • • • •	PHX
PHY	Y→Ms S-1→S										5A	3	1																									• • • • • • •	PHY
PLA	S+1→S Ms→A										68	4	1																									N • • • • Z •	PLA
PLP	S+1→S Ms→P										28	4	1																									N V 1 D I Z C	PLP
PLX	S+1→S Ms→X										FA	4	1																									N • • • • Z •	PLX
PLY	S+1→S Ms→Y										7A	4	1																									N • • • • Z •	PLY
ROL	[←[7 0]←C←]				2E	6	3	26	5	2	2A	2	1							36	6	2	3E	6	3												N • • • • Z C	ROL
ROR	[→C→[7 0]]				6E	6	3	66	5	2	6A	2	1							76	6	2	7E	6	3												N • • • • Z C	ROR
RTI	RTRN INT										40	6	1																									N V 1 D I Z C	RTI
RTS	RTRN SUB										60	6	1																									• • • • • • •	RTS
SBC	A-M-$\bar{C}$→A (3)	E9	2	2	ED	4	3	E5	3	2				E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3				F2	5	2				N V • • • Z C	SBC
SEC	1 → C										38	2	1																									• • • • • • 1	SEC
SED	1 → D										F8	2	1																									• • • 1 • • •	SED
SEI	1 → I										78	2	1																									• • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2				81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3				92	5	2				• • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																											96	4	2	• • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2										94	4	2																	• • • • • • •	STY
STZ	00 → M				9C	4	3	64	3	2										74	4	2	9E	5	3													• • • • • • •	STZ
TAX	A → X										AA	2	1																									N • • • • Z •	TAX
TAY	A → Y										A8	2	1																									N • • • • Z •	TAY
TRB	$\bar{A}$∧M → M (6)				1C	6	3	14	5	2																													• • • • • Z •	TRB
TSB	AVM → M (6)				0C	6	3	04	5	2																													• • • • • Z •	TSB
TSX	S → X										BA	2	1																									N • • • • Z •	TSX
TXA	X → A										8A	2	1																									N • • • • Z •	TXA
TXS	X → S										9A	2	1																									• • • • • • •	TXS
TYA	Y → A										98	2	1																									N • • • • Z •	TYA

Notes:

1. Add 1 to "n" if page boundary is crossed, except STA and STZ.
2. Add 1 to "n" if branch occurs to same page. Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. Accumulator address is included in Implied address.
5. "N" and "V" flags are unchanged in immediate mode.
6. "Z" flag indicates A∧M result (same as BIT instruction).

X Index X
Y Index Y
A Accumulator
M Memory per effective address
Ms Memory per stack pointer

\+ Add
\- Subtract
∧ And
∨ Or
∀ Exclusive or

n No. Cycles
No. Bytes
M_6 Memory Bit #6
M_7 Memory Bit #7

Enhanced Operational Characteristics

The GTE G65SCXXX family of microprocessors is a complete series of devices designed for building state-of-the-art microcomputer systems. Each member of the family is carefully designed to be hardware compatible, utilize the same basic software instruction set, and to be bus compatible with the MC6800 product line. Accordingly, the G65SCXX series is pin compatible with existing NMOS 6500 type microprocessors.

However, as stated previously, the CMOS design allows several operational enhancements to be incorporated in the current product. These operational enhancements are explained in Table V.

Table V. Microprocessor Operational Enhancements

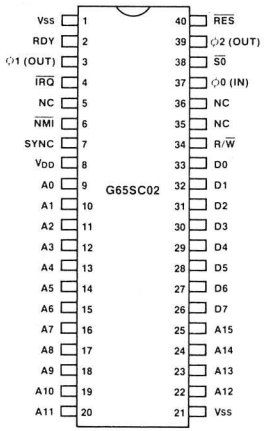
Function	NMOS 6500 Microprocessor	G65SCXXX Family Microprocessor
Indexed addressing across page boundary.	Extra read of invalid address.	Extra read of last instruction byte.
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use). Op Code — Bytes — Cycles X2 — 2 — 2 X3, X7, XB, XF — 1 — 1 44 — 2 — 3 54, D4, F4 — 2 — 4 5C — 3 — 8 DC, FC — 3 — 4
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments, one additional cycle.
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D=0) after reset and interrupts.
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flags. One additional cycle.
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded; BRK vector is ignored.	BRK is executed, then interrupt is executed.
Reset	Reads three stack locations.	Writes program counter and status register to stack
Read/Modify/Write instructions absolute indexed in same page.	Seven cycles.	Six cycles.

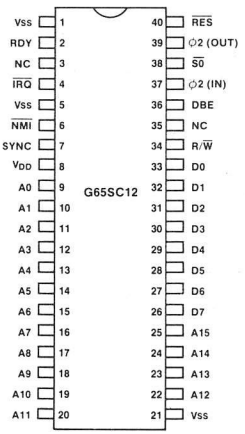
Pin Function

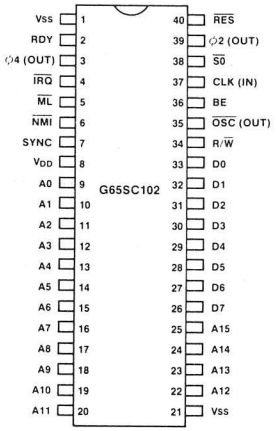
Pin	Description
A0-Axx	Address Bus
BE	Bus Enable
CLK (IN)	Clock Input
ϕ0(IN)	Phase 0 In
ϕ2(IN)	Phase 2 In
DBE	Data Bus Enable
D0-D7	Data Bus
$\overline{IRQ}$	Interrupt Request
$\overline{ML}$	Memory Lock
NC	No Connection
$\overline{NMI}$	Non-Maskable Interrupt

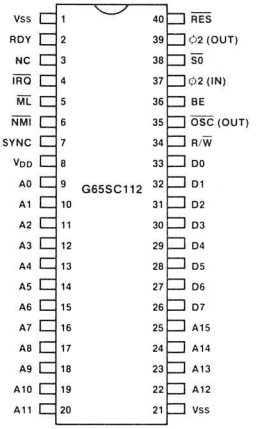
Pin	Description
$\overline{OSC}$ (OUT)	Oscillator Output
ϕ1(OUT)	Phase 1 Out
ϕ2(OUT)	Phase 2 Out
ϕ4(OUT)	Phase 4 Out
RDY	Ready
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{SO}$	Set Overflow
SYNC	Synchronize
V_{DD}	Positive Power Supply (+5.0 Volts)
V_{SS}	Internal Logic Ground

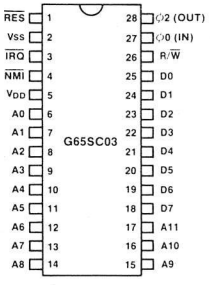
Pin Configuration

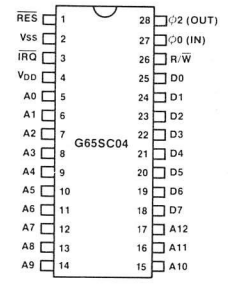




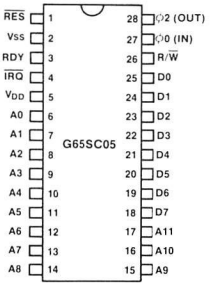


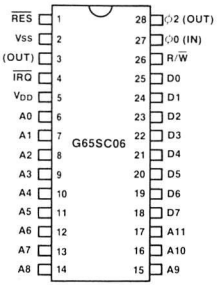


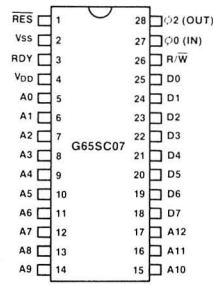


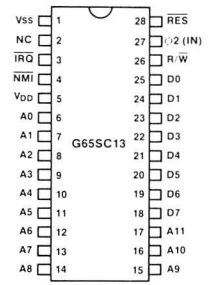


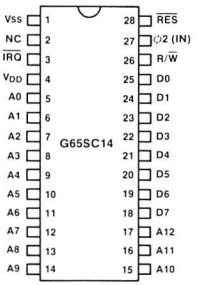
Pin Configuration Cont.

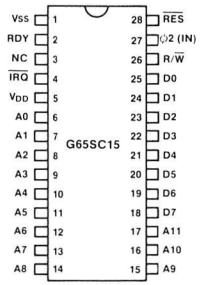


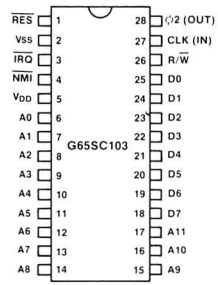


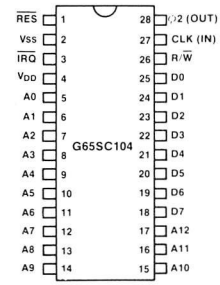


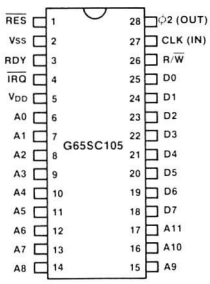


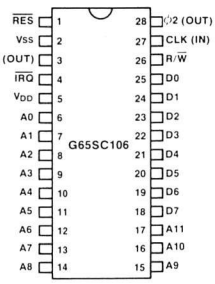


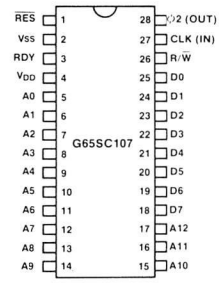


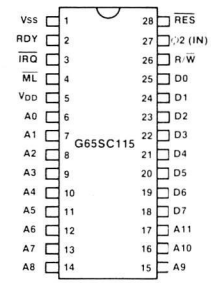












G65SC21

Microcircuits

CMOS Peripheral Interface Adapter

Features

- CMOS process technology for low power consumption
- Direct replacement for NMOS 6521 and 6821 devices manufactured by others
- Low power consumption (2 mA at 1MHz) allows battery powered operation
- Two programmable 8-bit bidirectional I/O Ports for peripheral device interfacing
- Individual Data Direction Registers for each I/O Port
- Microprocessor/peripheral "handshake" interrupt feature for enhanced data transfer control
- Programmable interrupt capability
- Four operating frequencies—1, 2, 3 and 4 MHz
- Automatic power-up initialization
- Single +5 volt power supply

General Description

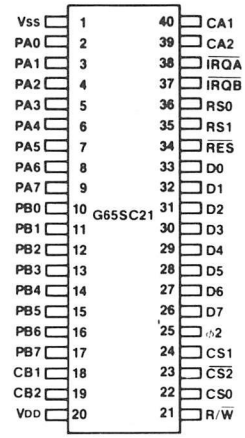
The GTE G65SC21 is a very flexible Peripheral Interface Adapter for use with GTE and other 8-bit microprocessor families. The G65SC21 provides programmed microprocessor control of up to two peripheral devices (Port A and Port B). Peripheral device control is accomplished through two 8-bit bidirectional I/O Ports, with individually assigned Data Direction Registers. The Data Direction Registers allow selection of data flow direction (input or output) at each respective I/O Port. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. The "handshake" interrupt control feature is provided by four peripheral control lines. This capability provides enhanced control over data transfer functions between the microprocessor and peripheral devices, as well as bidirectional data transfer between G65SC21 Peripheral Interface Adapters in multiprocessor systems.

Pin Function Table

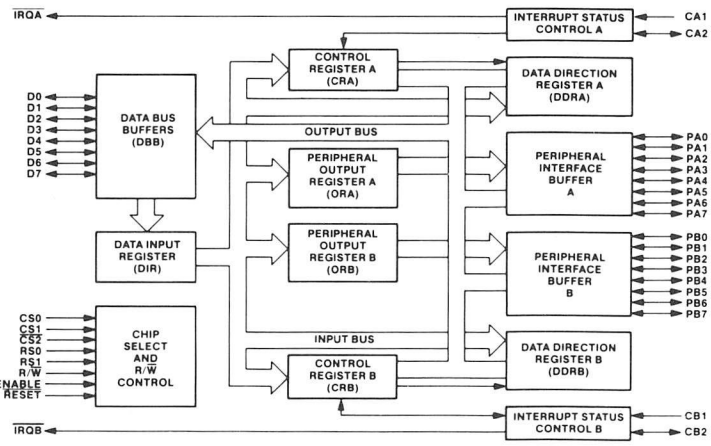
Pin	Description
D0-D7	Data Bus
PA0-PA7	Peripheral I/O Port A
PB0-PB7	Peripheral I/O Port B
$\phi 2$	Phase 2 Internal Clock
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{IRQA}$	Interrupt Request (Port A)

Pin	Description
$\overline{IRQB}$	Interrupt Request (Port B)
CS0, CS1, $\overline{CS2}$	Chip Select Inputs
RS0, RS1	Register Selects
CA1, CA2	Peripheral A Control Lines
CB1, CB2	Peripheral B Control Lines
VDD	Positive Power Supply (+5V)
VSS	Internal Logic Ground

Pin Configuration



Block Diagram



PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} +0.3V
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-55° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins, R/$\overline{W}$, $\overline{RES}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, ϕ2	I_{IN}		±1.0	μA
Three-State Leakage Current (V_{IN} = 0.4 to 2.4V), D0-D7, PB0-PB7, CB2, $\overline{IRQA}$, $\overline{IRQB}$	I_{TSI}		±10.0	μA
Input High Current (V_{IH} = 2.4V), Peripheral Inputs with Pullups, PA0-PA7, CA2	I_{IH}	-200		μA
Input Low Current (V_{IL} = 0.4V) Peripheral Inputs with Pullups, PA0-PA7, CA2	I_{IL}		-2.4	mA
Output Low Voltage (I_{OL} = 3.2 mA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB2, $\overline{IRQA}$, $\overline{IRQB}$	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB2, $\overline{IRQA}$, $\overline{IRQB}$	V_{OH}	2.4		V
Output High Current (Sourcing) (V_{OH} = 1.5V, Direct Transistor Drive), PB0-PB7, CB2	I_{OH}	-3.0		mA
Supply Current (No Load) f = 1 MHz f = 2 MHz f = 3 MHz f = 4 MHz	I_{DD} I_{DD} I_{DD} I_{DD}		2.0 4.0 6.0 8.0	mA mA mA mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz) Standby (Static)	P_D P_{DSB}		11.0 11.0	mW μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C

		G65SC21-1		G65SC21-2		G65SC21-3		G65SC21-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing (Figure 1)										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	nS

AC Characteristics: (Continued)

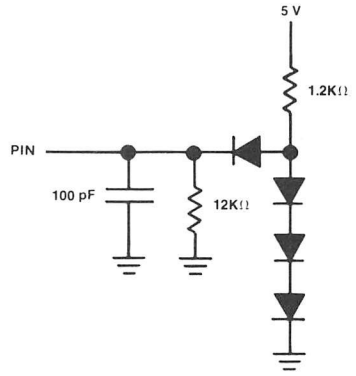
Parameter	Symbol	G65SC21-1 Min	G65SC21-1 Max	G65SC21-2 Min	G65SC21-2 Max	G65SC21-3 Min	G65SC21-3 Max	G65SC21-4 Min	G65SC21-4 Max	Unit
Write Timing (Figure 2)										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS
Peripheral Data Delay	t_{CPW}	—	1000	—	500	—	330	—	250	nS

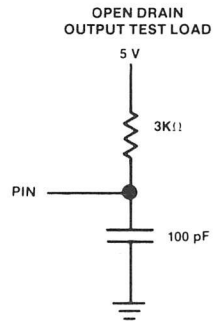
Note: Measurement points 0.8V and 2.0V unless otherwise specified.

AC Characteristics—Peripheral Interface Timing: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C

Parameter	Symbol	G65SC21-1 Min	G65SC21-1 Max	G65SC21-2 Min	G65SC21-2 Max	G65SC21-3 Min	G65SC21-3 Max	G65SC21-4 Min	G65SC21-4 Max	Unit
CA2 Delay Time, High-to-Low	t_{CA2}	—	1.0	—	0.5	—	0.33	—	0.25	μS
CA2 Delay Time, Low-to-High	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μS
CA2 Delay Time, Handshake Mode	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.50	μS
CB2 Delay Time, High-to-Low	t_{CB2}	—	1.0	—	0.5	—	0.33	—	0.25	μS
CB2 Delay Time, Low-to-High	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	μS
CB2 Delay Time, Handshake Mode	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.50	μS
CB2 Delay Time from Data Valid	t_{DC}	20	—	20	—	20	—	20	—	nS
Interrupt Input Pulse Width	P_{WI}	500	—	500	—	330	—	250	—	nS
Interrupt Response Time	t_{RS3}	—	1.0	—	1.0	—	0.67	—	0.33	μS
Interrupt Clear Delay	t_{IR}	—	1.6	—	0.85	—	0.67	—	0.33	μS
Rise and Fall Times— CA1, CA2, CB1, CB2	t_R, t_F	—	1.0	—	1.0	—	0.67	—	0.33	μS

Test Load





Timing Diagrams

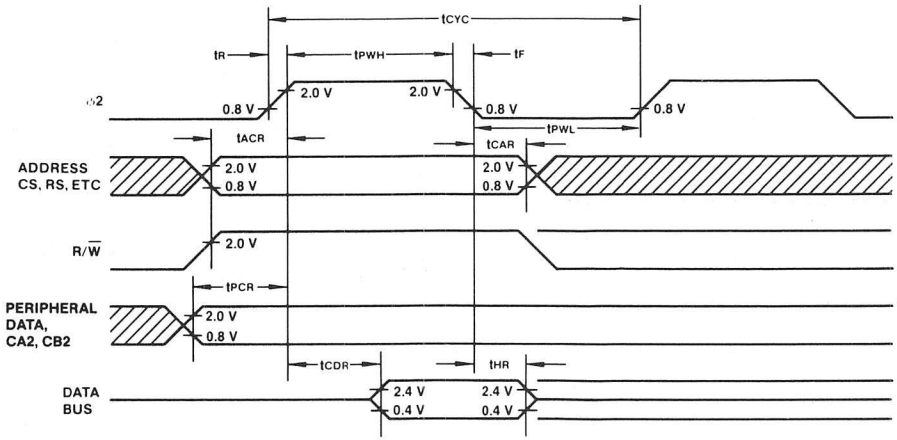


Figure 1. Read Timing

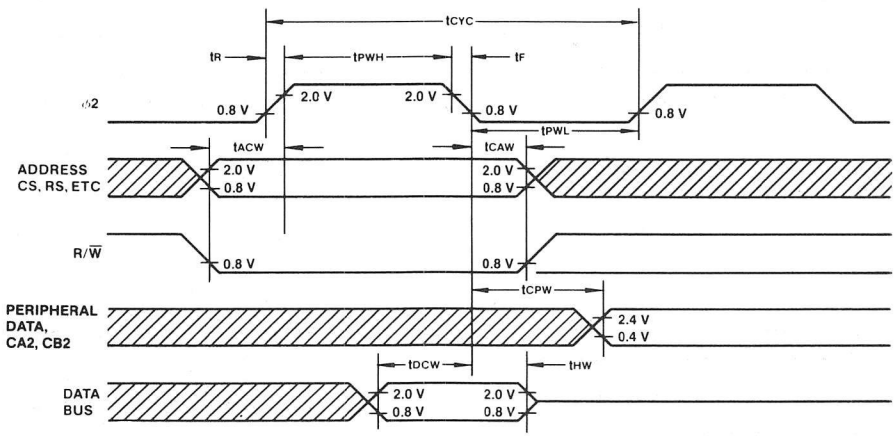


Figure 2. Write Timing

Timing Diagram (continued)

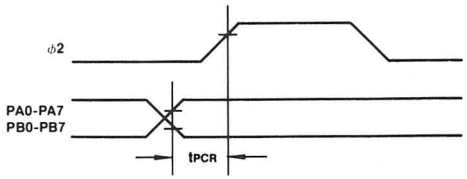


Figure 3. Peripheral Data Setup Time

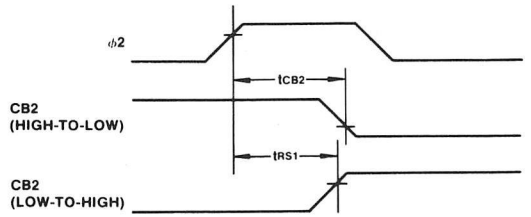


Figure 6. CB2 Timing

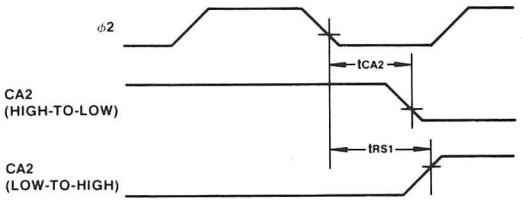


Figure 4. CA2 Timing

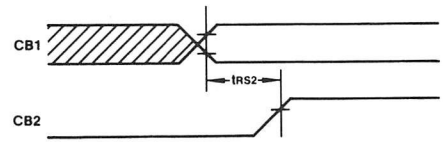


Figure 7. CB1/CB2 Handshake Timing

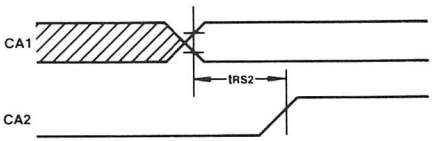


Figure 5. CA1/CA2 Timing

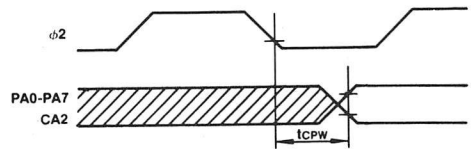


Figure 8. PA Port Delay Time

Timing Diagrams (continued)

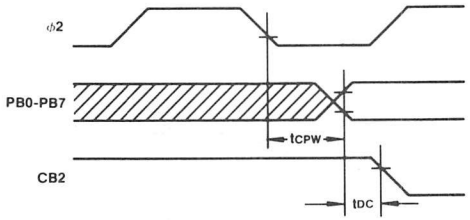


Figure 9. PB Port Delay Time

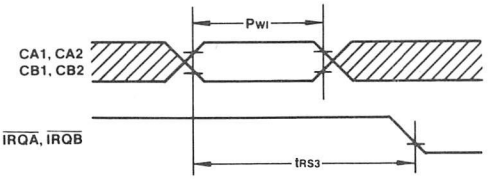


Figure 10. Interrupt Timing

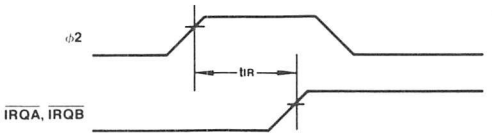


Figure 11. Interrupt Clear Timing

	7	6	5 4 3	2	1 0
CRA	IRQA1	IRQA2	CA2 Control	DDRA Access	CA1 Control
	7	6	5 4 3	2	1 0
CRB	IRQB1	IRQB2	CB2 Control	DDRB Access	CB1 Control

Figure 12. Control Registers

REGISTER SELECT PIN		DATA DIRECTION REGISTER ACCESS CONTROL BIT		
RS1	RS0	CRA-2	CRB-2	REGISTER SELECTED
0	0	1	—	Peripheral Interface A
0	0	0	—	Data Direction Register A
0	1	—	—	Control Register A
1	0	—	1	Peripheral Interface B
1	0	—	0	Data Direction Register B
1	1	—	—	Control Register B

Figure 13. Register Addressing

Signal Description

Data Bus (D0-D7)
The eight bidirectional data bus lines are used to transfer data between the G65SC21 and the microprocessor.

During a Read operation, the contents of the G65SC21 internal Data Bus Buffer (DBB) are transferred to the microprocessor via the Data Bus lines. During a Write operation, the Data Bus lines represent high impedance inputs over which data is transferred from the microprocessor to the Data Input Register (DIR). The Data Bus lines are in the high impedance state when the G65SC21 is unselected.

Chip Select (CS0, CS1, $\overline{CS2}$)
Normally, the three Chip Select lines are connected to the microprocessor address lines. This connection may be either direct or through an external decoder. To access the G65SC21, CS0 and CS1 must be high (Logic 1) and $\overline{CS2}$ must be low (Logic 0).

Register Select (RS0, RS1)
The Register Select inputs allow the microprocessor to select G65SC21 internal registers as presented in Figure 13.

Read/Write (R/$\overline{W}$)
The Read/Write signal is generated by the microprocessor and is used to control the transfer of data between the G65SC21 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic 1) and the chip is selected, data is transferred from the G65SC21 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the selected G65SC21 internal register (Write operation). Read/Write must always be preceded by Chip Select (CS0, CS1 and $\overline{CS2}$).

Input Clock (ϕ2)
The system ϕ2 Input Clock controls all data transfers between the G65SC21 and the microprocessor.

Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$)
The Interrupt Request ($\overline{IRQA}$ for Port A, and $\overline{IRQB}$ for Port B) output signals become true (Logic 0) whenever an internal interrupt condition is determined by Interrupt Status Control Registers A and B. These two signals are active low and have open-drain outputs. The open-drain configuration allows the Interrupt Request signals to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

Reset ($\overline{RES}$)
A low signal (Logic 0) on the Reset line serves to initialize the G65SC21, clearing all internal registers and placing all peripheral interface lines (PA and PB) in the input state.

Peripheral Data Port A (PA0-PA7)
Peripheral Data Port A is an 8-line, bidirectional bus used for the transfer of data, control and status information between the G65SC21 and a peripheral device. Each data port bus line may be individually programmed as either an input or output under control of the Data Direction Register (DDRA). Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port.

Peripheral Data Port B (PB0-PB7)
Peripheral Data Port B is an 8-line, bidirectional bus used for the transfer of data, control and status information between the G65SC21 and a peripheral device. Functional operation is identical to Peripheral Data Port A, thus allowing the G65SC21 to independently control two peripheral devices.

Interrupt Status Control—
CA1, CA2 (Port A) and CB1, CB2 (Port B)
The two Interrupt Status Control lines for each Data Port are controlled by the Interrupt Status Control logic (A and B). This logic interprets the contents of the corresponding Control Register (CRA and CRB), allowing the Interrupt Status Control lines to perform various peripheral control functions.

Functional Description

Organization of the G65SC21 consists of two independent control sections (A and B). Section A and Section B are identical—each consisting of a Control Register (CRA and CRB), Data Direction Register (DDRA and DDRB), Output Register (ORA and ORB), Interrupt Status Control (A and B) and Peripheral Interface Buffers (A and B). The Data Bus Buffers (DBB), Data Input Register (DIR) and the Chip Select and Read/Write control logic is common to both sections. Refer to the Block Diagram on Page 1.

Data Input Register (DIR)
During a Write data operation, the microprocessor writes data into the G65SC21 by placing data on the Data Bus. This data is then latched into the Data Input Register by the Phase Two (ϕ2) clock. Once in the Data Input Register, this data byte is transferred into one of six internal registers. This data transfer occurs after the trailing edge of the ϕ2 clock pulse that latched the data byte into the Data Input Register. This timing delay guarantees the data on the peripheral output lines (PA or PB) will make a smooth transition from low to high or high to low, and the output voltage will remain stable when there is to be no change in polarity.

Control Registers (CRA and CRB)
The individual Control Registers allow the microprocessor to program the operation of the Interrupt Control inputs (CA1, CA2, CB1, and CB2), and the Peripheral Control outputs (CA2 and CB2). Refer to Figure 4. Bit 2 in each Control Register controls the addressing of the Data Direction Registers (DDRA and DDRB) and also the Output Registers (ORA and ORB). Bits 6 and 7 are interrupt flag bits which indicate the status of the Interrupt Status Control input lines (CA1, CA2, CB1, and CB2). These two interrupt status flags are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These two interrupt lines drive the interrupt input ($\overline{IRQ}$ and $\overline{NMI}$) of the microprocessor.

Interrupt Status Control Logic (A and B)
The G65SC21 contains four interrupt/peripheral control lines (CA1, CA2, CB1, and CB2). These lines are controlled by the Interrupt Status Control logic (A and B). The Interrupt Status Control logic serves to interpret the contents of the corresponding Control Register, thus allowing these lines to perform various control functions as described in Figure 16.

Data Direction Registers (DDRA and DDRB)
By use of the Data Direction Registers (DDR), the microprocessor can program each individual peripheral I/O Port line as an input or output. Each bit within the register controls a corresponding line of the I/O Port, with DDRA controlling peripheral I/O Port A and DDRB controlling I/O Port B. A programmed "0" in any bit position of a DDR results in the corresponding I/O Port line being designated as an input. A "1" results in the line being an output.

Peripheral Output Registers (ORA and ORB)
All output data to a peripheral is stored in the corresponding Output Register (ORA or ORB). This data is then presented to the Peripheral Interface Buffer (A and B) and placed on the respective I/O Port lines. Writing a "0" into any bit position of ORA or ORB results in the corresponding peripheral I/O Port line going low ($<$0.4V), providing that particular line is programmed as an output. Writing a "1" into a bit position results in the corresponding output going high.

Register Access and Selection

Register Select lines RS0 and RS1 are used in combination with Chip Select to access the six function registers within the G65SC21. These lines are normally connected to the microprocessor address output lines. As can be seen from Figure 13, the Register Select lines are used in combination with bit 2 of the Control Registers (CRA and CRB) to access the Data Direction Registers (DDRA and DDRB) and the peripheral interface Output Registers (ORA and ORB). If bit 2 is a Logic 1, a Peripheral Output Register is selected, and if bit 2 is a Logic 0, a Data Direction Register is selected. Thus, with appropriate addressing the microprocessor can write directly into the Control Registers, the Data Direction Registers, and the peripheral interface Output Registers. Also, the microprocessor can read the contents of the Control Registers and the Data Direction Registers.

Data Access—Peripheral I/O Port A

Depending on the contents of Data Direction Register A, the eight lines of Peripheral I/O Port A may be programmed as either inputs or outputs. When a particular line(s) is programmed as an output, it will reflect the contents of the corresponding bit in peripheral Output Register A (ORA). When programmed as inputs, these lines will reflect the logic state of corresponding peripheral input data. Lines programmed as inputs are not affected by the peripheral Output Register (ORA). To perform a Read operation (RS1 = 0, RS0 = 0, and Data Direction Register Access Control bit (CRA-2) = 1), data on peripheral I/O Port A lines is directly transferred to the microprocessor via the Data Bus. The transferred byte will contain both input and output data from all eight I/O Port A lines. It is the responsibility of the microprocessor to recognize and interpret only those bits which are important to a particular peripheral operation being performed. Note that the microprocessor always reads the I/O Port A "pins" and not the contents of the ORA. This being the case, the actual data read into the microprocessor may differ from the contents of the peripheral ORA, i.e., for a particular data "output" line. This condition occurs when the I/O pin is not allowed to reach a full +2.4 volts DC for a Logic 1. When this occurs, the microprocessor will read a Logic 0, even though the corresponding bit in the peripheral ORA is a Logic 1.

Data Access—Peripheral I/O Port B

When reading peripheral I/O Port B, a combination of input and output data is read in a similar manner to peripheral I/O Port A above. The major difference is that for I/O Port B, data is read directly from peripheral Output Register B (ORB) for those lines programmed as outputs. This being the case, it is possible to load down I/O Port B lines without causing incorrect data to be transferred to the microprocessor during a Read operation.

Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$)

Both Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$) lines are active low, and serve to interrupt the microprocessor either directly or through external interrupt priority circuitry. Each line is "open drain" and is capable of sinking 3.2 milliamps from an external source, thus allowing all interrupts to be tied together in a wired-OR configuration. Each Interrupt Request line is assigned to a particular Peripheral Interface I/O Port ($\overline{IRQA}$ for Port A, and $\overline{IRQB}$ for Port B). Two interrupt flag bits are used with each Interrupt Request line. When true, these flag bits cause the Interrupt Request line to go low. The flag bits (bits 6 and 7 in each of the two Control Registers) act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the microprocessor to enable or disable the interrupts from each of the four interrupt inputs, i.e., CA1, CA2, CB1 and CB2. Each interrupt flag is set by an active transition on the interrupt input (CA1, CA2, CB1 and CB2).

Interrupt A Control ($\overline{IRQA}$)

Bit 7 of Control Register A is always set by an active transition of the CA1 interrupt control signal. This flag can be prevented from interrupting (disabled) by setting bit 0 of Control Register A to a Logic 0. Bit 6 of Control Register A is always set by an active transition of the CA2 interrupt control signal. This flag can be prevented from interrupting (disabled) by setting bit 3 of Control Register A to a Logic 0.

Both bit 6 and bit 7 in Control Register A are reset by a "Read Peripheral Output Register A" operation. To perform this Read operation, the proper Chip Select and appropriate Register Select signals must be present.

Interrupt B Control ($\overline{IRQB}$)

The control of Interrupt Request B ($\overline{IRQB}$) is performed in the same manner as that described above for $\overline{IRQA}$, except that for I/O Port B, Control Register bit 7 is set by an active transition on CB1 and interrupt enable/disable is controlled by Control Register bit 0. Control Register bit 6 is set by CB2 and its enable/disable is controlled by Control Register bit 3. Here again, both bit 6 and bit 7 in Control Register B are reset by a "Read Peripheral Output Register B" operation. Note that the interrupt disable bits (CRB bits 0 and 3) allow the microprocessor to control the interrupt function.

Interrupt Control Summary

$\overline{IRQA}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1
$\overline{IRQB}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1

Peripheral I/O Ports

The G65SC21 provides two 8-bit bidirectional Data Ports (PA and PB) and four interrupt/control lines (CA1, CA2, CB1 and CB2) for interfacing to peripheral devices. Peripheral I/O Port A and I/O Port B allow the microprocessor to interface the peripheral device input lines by loading data into the corresponding Peripheral Output Register. The microprocessor interfaces the peripheral device output lines by reading data on the I/O Port input lines directly onto the Data Bus and into the internal registers of the microprocessor.

Peripheral I/O Port A (PA0-PA7)

Each Peripheral I/O Port line can be programmed to act as an input or an output, as determined by the corresponding bits in the Data Direction Register. Within the Data Direction Register, a Logic 1 in a particular bit position represents an output line. Likewise, a Logic 0 in a particular bit position represents an input line. The Data Buffers which drive the I/O Port A lines contain "active" pull-up transistors as shown in Figure 14. Since these pull-ups are p-channel transistors they allow the output voltage to go to V_{DD} for a Logic 1. Also, since these switches can sink a full 3.2 milliamp, the buffers are capable of driving one standard TTL load. In the input mode, the pull-up devices shown in Figure 14 remain connected to the I/O pin and continue to supply current to the pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral I/O Port B (PB0-PB7)

The lines of Peripheral I/O Port B function in a similar manner to the discussion of I/O Port A above. Programmed selection for input/output function is identical. There are, however, several characteristics of the buffers driving these lines which affect their use in peripheral interfacing. Peripheral I/O Port B buffers are push-pull devices as shown in Figure 15.

The active pull-up devices can source up to 3 milliamp at 1.5 volts. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows

convenient control of relays, lamps, etc. Because the I/O Port B outputs are designed to drive transistors directly, the output data is read directly from Peripheral Output Register B for those lines programmed as inputs. The I/O Port B push-pull buffers also provide a high impedance input state. When these lines are programmed as inputs, the output buffer enters the high impedance state.

Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1 and CB2)

The G65SC21 contains four interrupt input/peripheral control lines (CA1, CA2, CB1 and CB2) which offer a number of special peripheral control functions. These functions greatly enhance the performance of the two I/O Ports. Refer to Figure 16 for a summary of control line operation.

I/O Port A Interrupt Input/Peripheral Control Lines (CA1, CA2)

Line CA1 is an interrupt input only. An active transition on this line will set bit 7 in Control Register A to a Logic 1. This flag bit (bit 7) can be programmed to set on either a positive or negative CA1 transition. Bit 7 will be set on a negative transition if bit 1 in the Control Register is set to a Logic 0. Likewise, bit 7 can be set on a positive transition if bit 1 in the Control Register is set to a Logic 1.

It should be noted that a negative transition is defined as a transition from high to low, and a positive transition is a transition from low to high.

Setting the interrupt flag (bit 7 or the Control Register) will interrupt the microprocessor via $\overline{IRQA}$ if bit 0 in Control Register A is a Logic 1 as described in earlier paragraphs.

Line CA2 can act as a totally independent interrupt input or as a peripheral control output. CA2 acts as an interrupt input when Control Register A bit 5 is a Logic 0. In this case, CA2 will set the interrupt flag (bit 6 of Control Register A) to a Logic 1 on the active transition as selected by bit 4 of the Control Register. The Control Register bits and interrupt inputs serve the same basic function as that described above for CA1. The input transition sets the interrupt flag which serves as the link between the microprocessor interrupt configuration and the peripheral device. The interrupt disable bit allows the microprocessor to exercise control over the system interrupts.

CA2 serves in the output control mode when Control Register A bit 5 is a Logic 1. In this case, CA2 can operate independently to generate a sample pulse each time the microprocessor reads data on I/O Port A. This mode is selected by setting bit 4 of the Control Register to a Logic 0 and bit 3 to a Logic 1. This pulse output is normally used to control counters, shift registers, etc. which provide sequential data to the peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the peripheral device and the microprocessor. With respect to I/O Port A, this "handshake" allows positive control of data transfers from the peripheral device into the microprocessor. The "handshake" function operates as follows:

The CA1 input signals the microprocessor that data is available by interrupting the microprocessor. The microprocessor then reads the data and sets CA2 to a Logic 0. This signals the peripheral device that it can now place new data on the I/O Port line.

A third output mode can be selected by setting Control Register bit 4 to a Logic 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of Control Register A to a Logic 1 or a Logic 0 respectively.

I/O Port B Interrupt Input/Peripheral Control Lines (CB1, CB2)

The CB1 line operates as an interrupt input only in the same manner as CA1 above. In this case, bit 7 of Control Register B is set by the active transition on CB1 as selected by bit 0 of the Control Register. The CB2 input modes operate identical to the CA2 input modes. However, the CB2 output modes (Control Register B bit 5 set to Logic 1) differ somewhat from those of CA2. That is, the pulse ouput occurs when the microprocessor writes data into Output Register B. Also, the "handshaking" operates on data transfers from the microprocessor into the peripheral device.

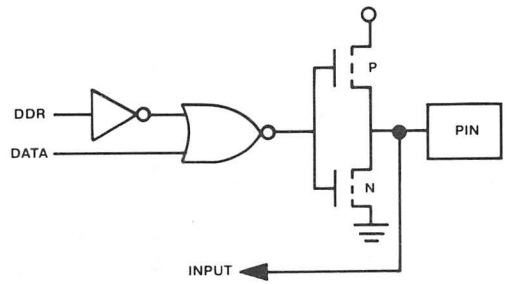


Figure 14. Port A Buffer Circuit (PA0-PA7)

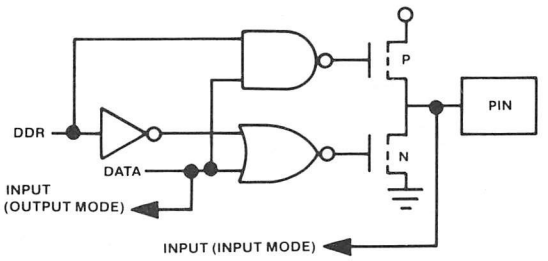


Figure 15. Port B Buffer Circuit (PB0-PB7)

CA1/CB1 CONTROL			
CRA (CRB)		ACTIVE TRANSITION OF INPUT SIGNAL*	$\overline{IRQA}$ ($\overline{IRQB}$) INTERRUPT OUTPUTS
BIT 1	BIT 0		
0	0	Negative	Disable—remain high
0	1	Negative	Enable—goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable—remain high
1	1	Positive	Enable—as explained above

*Note: Bit 7 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES				
CRA (CRB)			ACTIVE TRANSITION OF INPUT SIGNAL*	$\overline{IRQA}$ ($\overline{IRQB}$) INTERRUPT OUTPUTS
BIT 5	BIT 4	BIT 3		
0	0	0	Negative	Disable—remains high
0	0	1	Negative	Enable—goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable—remains high
0	1	1	Positive	Enable—as explained above

*Note: Bit 6 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of bit 0 in CRA (CRB).

CA2 OUTPUT MODES				
CRA			MODE	DESCRIPTION
BIT 5	BIT 4	BIT 3		
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES				
CRB			MODE	DESCRIPTION
BIT 5	BIT 4	BIT 3		
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

Figure 16. Interrupt Input/Peripheral Control Lines Operation

G65SC22

Microcircuits

CMOS Versatile Interface Adapter With Interval Timer/Counters

Features

- CMOS process technology for low power consumption
- Fully compatible with NMOS 6522 devices
- Low power consumption allows battery-powered operation (2 mA at 1 MHz)
- Two 8-bit, bidirectional peripheral I/O Ports
- Two powerful 16-bit programmable Interval Timer/Counters
- Serial bidirectional peripheral I/O Port
- Enhanced "handshake" feature
- Latched Input/Output Registers on both I/O Ports
- Programmable Data Direction Registers
- Four operating frequencies—1, 2, 3 and 4 MHz
- TTL compatible I/O peripheral lines
- Single +5 volts power supply
- Available in 40-pin dual-in-line package

General Description

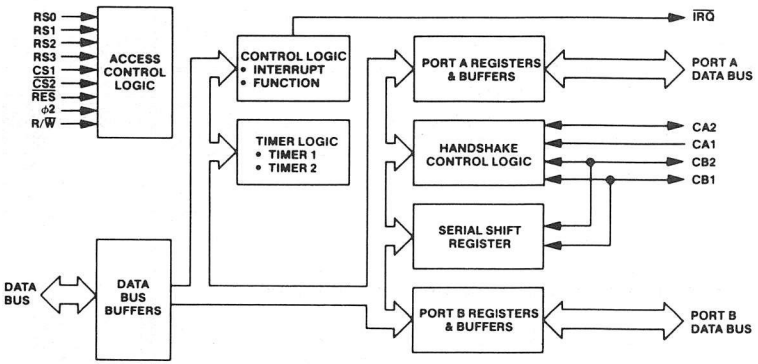
The GTE G65SC22 Versatile Interface Adapter (VIA) is a flexible I/O device for use with the GTE G65SCXXX series 8-bit microprocessor family. The G65SC22 includes functions for programmed control of up to two peripheral devices (Ports A and B). Two program controlled 8-bit bidirectional peripheral I/O ports allow direct interfacing between the microprocessor and selected peripheral units. Each port has input data latching capability. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on an individual line basis. Also provided are two programmable 16-bit Interval Timer/Counters with latches. Timer 1 may be operated in a One-Shot Interrupt Mode with interrupts on each count-to-zero, or in a Free-Run Mode with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register. Application versatility is further increased by various control registers, including—an Interrupt Flag Register, an Interrupt Enable Register and two Function Control Registers.

Pin Function Table

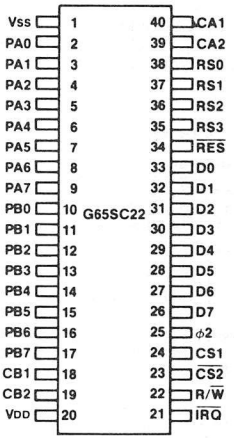
Pin	Description
DO-D7	Data Bus
PA0-PA7	Peripheral I/O Port A
PB0-PB7	Peripheral I/O Port B
$\phi 2$	Phase 2 Internal Clock
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{IRQ}$	Interrupt Request

Pin	Description
CS1, $\overline{CS2}$	Chip Select
RS0-RS3	Register Select
CA1, CA2	Peripheral A Control Lines
CB1, CB2	Peripheral B Control Lines
VDD	Positive Power Supply (+5V)
Vss	Internal Logic Ground

Block Diagram



Pin Configuration



PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} +0.3V
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-55° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins, R/$\overline{W}$, $\overline{RES}$, RS0-RS3, CS1, $\overline{CS2}$, CA1, ϕ2	I_{IN}		±1.0	μA
Three-State Leakage Current (V_{IN} = 0.4 to 2.4V), D0-D7, $\overline{IRQ}$	I_{TSI}		±10.0	μA
Input High Current (V_{IH} = 2.4V), Peripheral Inputs with Pullups, PA0-PA7, PB0-PB7, CA2, CB1, CB2	I_{IH}	-200		μA
Input Low Current (V_{IL} = 0.4V) Peripheral Inputs with Pullups PA0-PA7, PB0-PB7, CA2, CB1, CB2	I_{IL}		-1.6	mA
Output Low Voltage (I_{OL} = 3.2 mA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB1, CB2, $\overline{IRQ}$	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB1, CB2, $\overline{IRQ}$	V_{OH}	2.4		V
Output High Current (Sourcing) (V_{OH} = 1.5V, Direct Transistor Drive), PB0-PB7	I_{OH}	-3.0		mA
Supply Current (No Load) f = 1 MHz f = 2 MHz f = 3 MHz f = 4 MHz	I_{DD} I_{DD} I_{DD} I_{DD}		2.0 4.0 6.0 8.0	mA mA mA mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz) Standby (Static)	P_D P_{DSB}		11.0 11.0	mW μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C

		G65SC22-1		G65SC22-2		G65SC22-3		G65SC22-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing (Figure 2)										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	nS
Write Timing (Figure 3)										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS
Peripheral Data Delay	t_{CPW}	—	1000	—	500	—	330	—	250	nS

AC Characteristics—Peripheral Interface Timing: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C
(See Figures 4 through 12)

Parameter	Symbol	Min	Max	Unit	Figure
Rise and Fall Time for CA1, CB1, CA2 and CB2 Input Signals	t_R, t_F	—	1.0	μS	—
Delay Time, Clock Negative Transition to CA2 Negative Transition (Read Handshake or Pulse Mode)	t_{CA2}	—	1.0	μS	4,5
Delay Time, Clock Negative Transition to CA2 Positive Transition (Pulse Mode)	t_{RS1}	—	1.0	μS	4
Delay Time, CA1 Active Transition to CA2 Positive Transition (Handshake Mode)	t_{RS2}	—	2.0	μS	5
Delay Time, Clock Positive Transition to CA2 or CB2 Negative Transition (Write Handshake)	t_{WHS}		1.0	μS	6,7
Delay Time, Clock Positive Transition to CA2 or CB2 Positive Transition (Pulse Mode)	t_{RS3}	—	1.0	μS	6
Delay Time, CA1 or CB1 Active Transition to CA2 or CB2 Positive Transition (Handshake Mode)	t_{RS4}	—	2.0	μS	7
Delay Time Required from CA2 Output to CA1 Active Transition (Handshake Mode)	t_{21}	400	—	nS	7
Set-up Time, Peripheral Data Valid to CA1 or CB1 Active Transition (Input Latching)	t_{IL}	300	—	nS	8
Shift-Out Delay Time—Time from $\phi 2$ Falling Edge to CB2 Data Out	t_{SR1}	—	300	nS	9
Shift-In Set-up Time—Time from CB2 Data In to $\phi 2$ Rising Edge	t_{SR2}	300	—	nS	10
External Shift Clock (CB1) Set-up Time Relative to $\phi 2$ Trailing Edge	t_{SR3}	100	t_{CYC}	nS	10
Pulse Width—PB6 Input Pulse	t_{IPW}	2 x t_{CYC}	—		12
Pulse Width—CB1 Input Clock	t_{ICW}	2 x t_{CYC}	—		11
Pulse Spacing—PB6 Input Pulse	t_{IPS}	2 x t_{CYC}	—		12
Pulse Spacing—CB1 Input Pulse	t_{ICS}	2 x t_{CYC}	—		11
CA1, CB1 Set Up Prior to Transition to Arm Latch	t_{AL}	300	—	nS	8
Peripheral Data Hold After CA1, CB1 Transition	t_{PDH}	150	—	nS	8

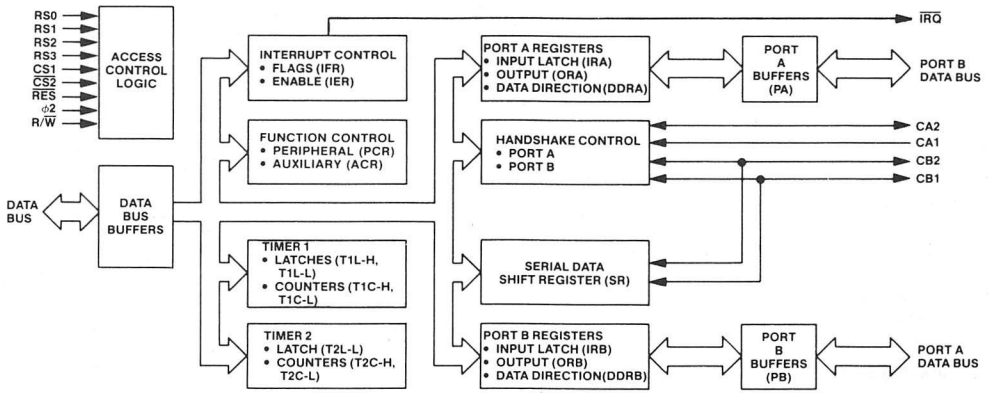


Figure 1. Functional Block Diagram

Timing Diagrams: Measurement points 0.8.V and 2.0V unless otherwise specified.

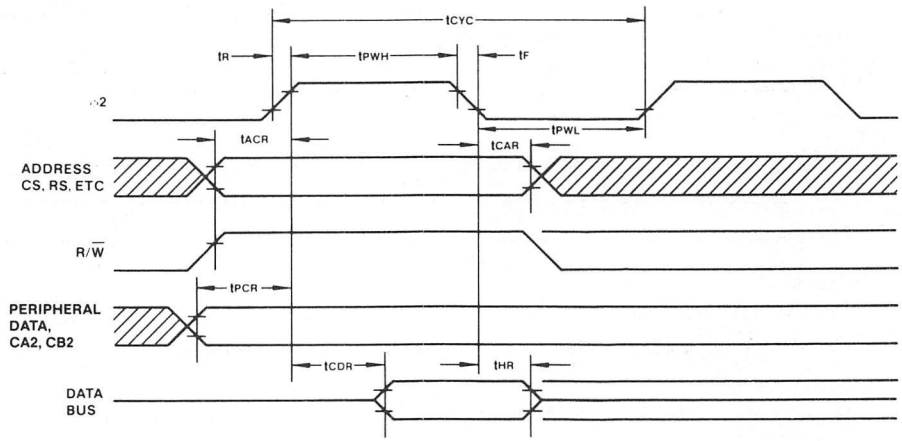


Figure 2. Read Timing

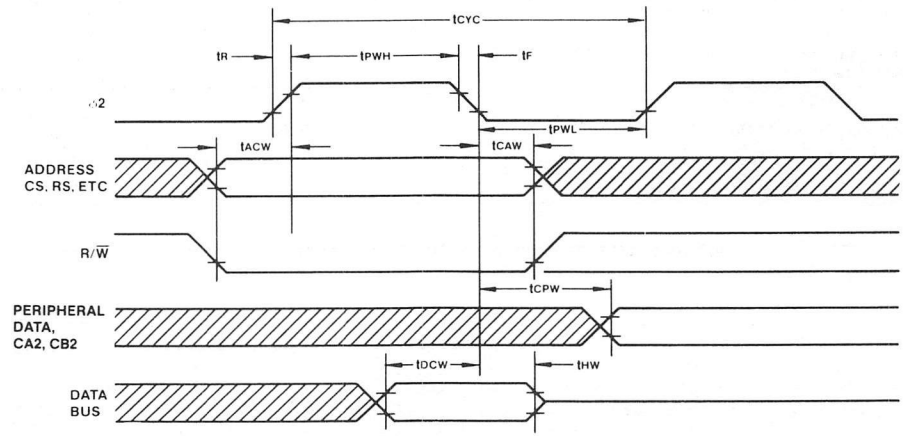


Figure 3. Write Timing

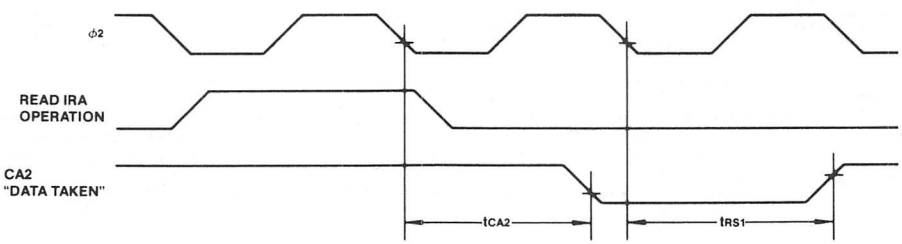


Figure 4. Read Handshake, Pulse Mode Timing (CA2)

Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

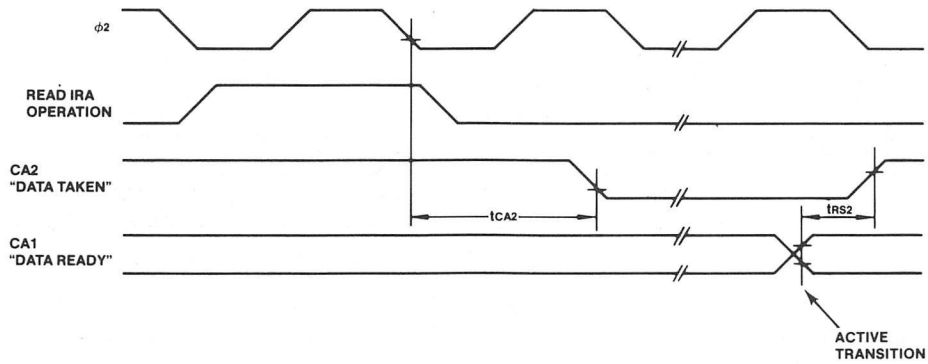


Figure 5. Read Handshake, Handshake Mode Timing (CA2)

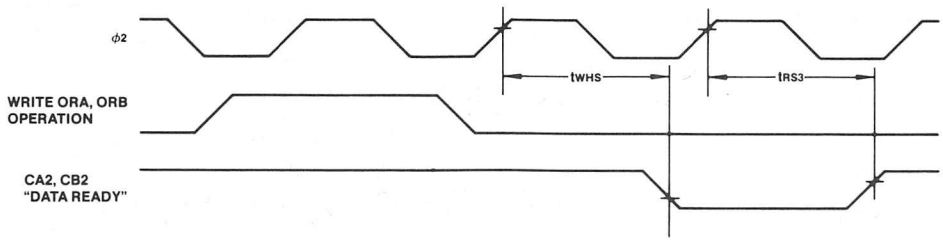


Figure 6. Write Handshake, Pulse Mode Timing (CA2, CB2)

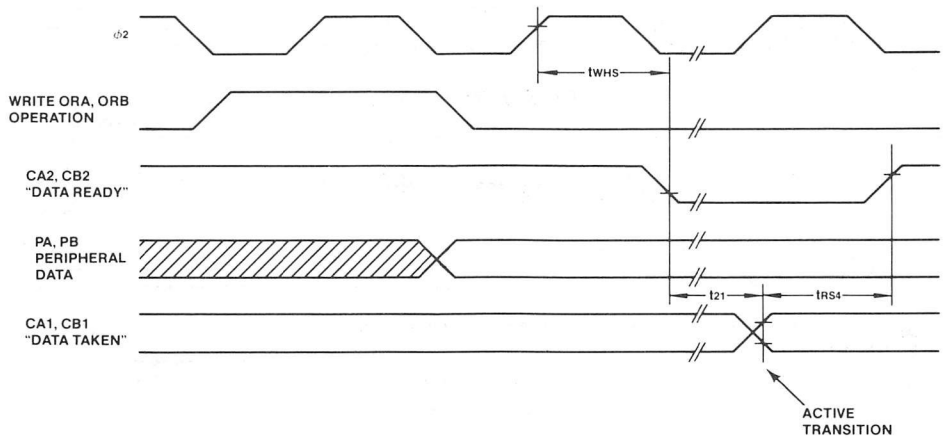


Figure 7. Write Handshake, Handshake Mode Timing (CA2, CB2)

Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

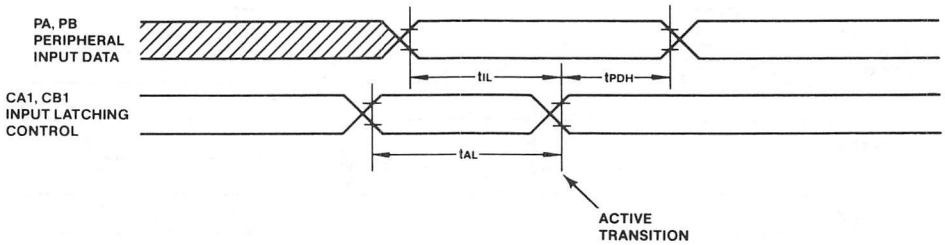


Figure 8. Peripheral Data, Input Latching Timing

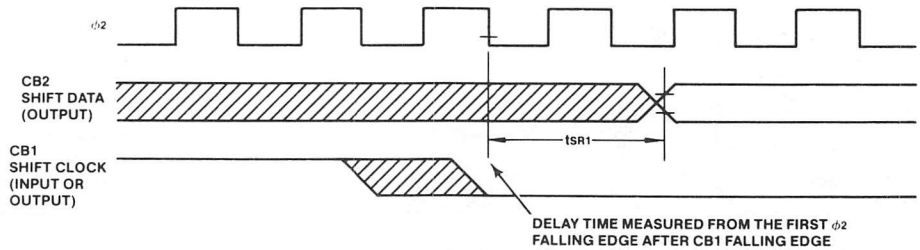


Figure 9. Data Shift Out, Internal or External Shift Clock Timing

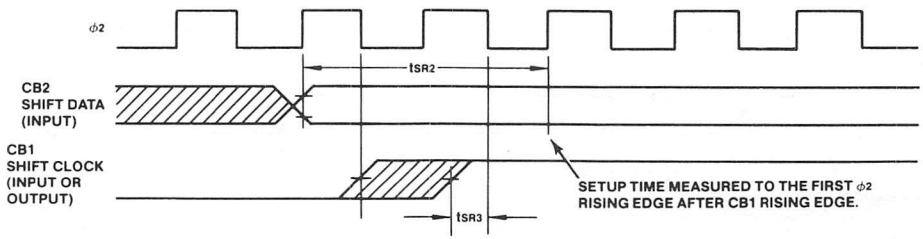


Figure 10. Data Shift In, Internal or External Shift Clock Timing

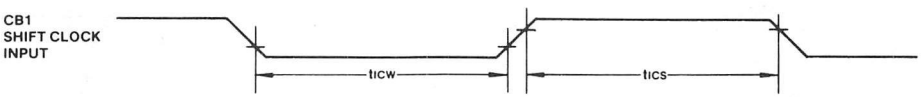


Figure 11. External Shift Clock Timing

Timing Diagrams (Continued): Measurement points 0.8V and 2.0V unless otherwise specified.

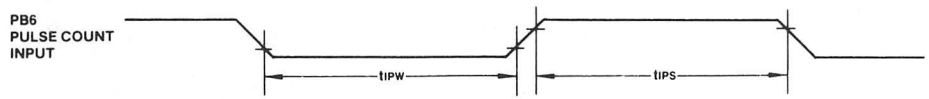


Figure 12. Pulse Count Input Timing

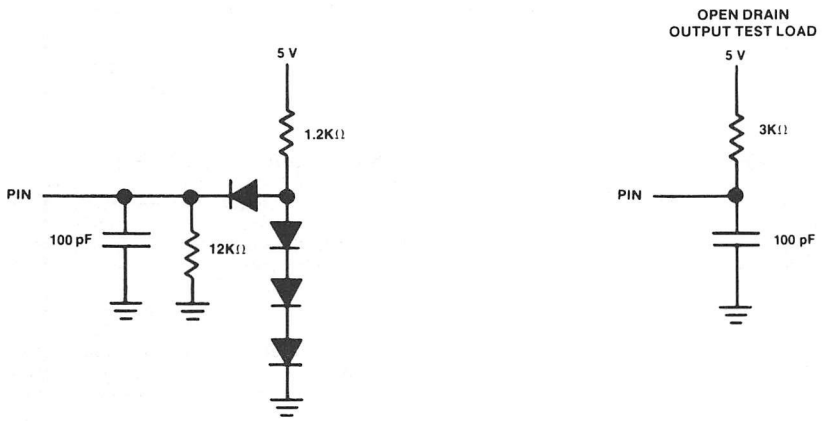


Figure 13. Test Load

Signal Description

Reset ($\overline{RES}$)

Reset ($\overline{RES}$) clears all internal registers (except T1 and T2 counters and latches, and the Shift Register (SR)). In the $\overline{RES}$ condition, all peripheral interface lines (PA and PB) are placed in the input state. Also, the Timers (T1 and T2), SR and interrupt logic are disabled from operation.

Input Clock ($\phi 2$)

The system $\phi 2$ Input Clock controls all data transfers between the G65SC22 and the microprocessor.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the transfer of data between the G65SC22 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic 1) and the chip is selected, data is transferred from the G65SC22 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the selected G65SC22 register (Write operation). Read/Write must always be preceded by a proper Chip Select (CS1, $\overline{CS2}$).

Data Bus (D0-D7)

The eight bidirectional Data Bus lines are used to transfer data between the G65SC22 and the microprocessor. During a Read operation, the contents of the selected G65SC22 internal register are transferred to the microprocessor via the Data Bus lines. During a Write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to a selected G65SC22 register. The Data Bus lines are in the high impedance state when the G65SC22 is unselected.

Chip Select (CS1, $\overline{CS2}$)

Normally, the two Chip Select lines are connected to the microprocessor address lines. This connection may be direct or through decoding. To access a selected G65SC22 register, CS1 must be high (Logic 1) and $\overline{CS2}$ must be low (Logic 0).

Register Select (RS0-RS3)

The Register Select inputs allow the microprocessor to select one of 16 internal registers within the G65SC22. Refer to Table 1 for Register Select coding and a functional description.

Interrupt Request ($\overline{IRQ}$)

The Interrupt Request ($\overline{IRQ}$) output signal is generated (Logic 0) whenever an internal Interrupt Flag bit is set (Logic 1) and the corresponding Interrupt Enable bit is a Logic 1. The Interrupt Request output is an open-drain configuration, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

Table 1. G65SC22 Internal Registers

Register Number	RS Coding				Register Designation	Description	
	RS3	RS2	RS1	RS0		Write	Read
0	0	0	0	0	ORB/IRB	Output Register "B"	Input Register "B"
1	0	0	0	1	ORA/IRA	Output Register "A"	Input Register "A"
2	0	0	1	0	DDRB	Data Direction Register "B"	
3	0	0	1	1	DDRA	Data Direction Register "A"	
4	0	1	0	0	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	0	1	0	1	T1C-H	T1 High-Order Counter	
6	0	1	1	0	T1L-L	T1 Low-Order Latches	
7	0	1	1	1	T1L-H	T1 High-Order Latches	
8	1	0	0	0	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	1	0	0	1	T2C-H	T2 High-Order Counter	
10	1	0	1	0	SR	Shift Register	
11	1	0	1	1	ACR	Auxiliary Control Register	
12	1	1	0	0	PCR	Peripheral Control Register	
13	1	1	0	1	IFR	Interrupt Flag Register	
14	1	1	1	0	IER	Interrupt Enable Register	
15	1	1	1	1	ORA/IRA	Same As Reg 1 Except No "Handshake"	

Peripheral Data Port A (PA0-PA7)

Peripheral Data Port A is an 8-line, bidirectional bus used for the transfer of data, control and status information between the G65SC22 and a peripheral device. Each Peripheral Data Port bus line may be individually programmed as either an input or output under control of a Data Direction Register. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. When a "0" is written to any bit position of the Data Direction Register, the corresponding line will be programmed as an input. Likewise, when a "1" is written into any bit position of the register, the corresponding data line will serve as an output. Polarity of the data output is determined by the Output Register, while input data may be latched into the Input Register under control of the CA1 line. All modes are program controlled by the microprocessor by way of the G65SC22's internal control registers. Each Peripheral Data Port line represents one TTL load in the input mode and will drive one standard TTL load in the output mode. A typical output circuit for Peripheral Data Port A is shown in Figure 14.

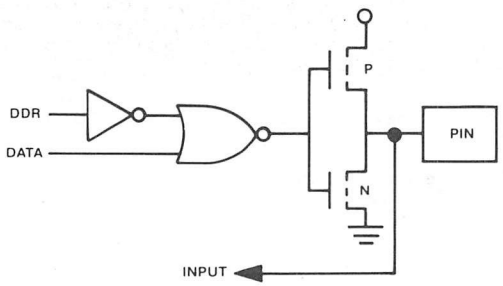


Figure 14. Port A Buffer Circuit (PA0-PA7, CA2)

Peripheral Data Port A Control Lines (CA1, CA2)

Control lines CA1 and CA2 serve as interrupt inputs or handshake outputs for Peripheral Data Port A. Each line controls an internal Interrupt Flag with a corresponding Interrupt Enable bit. CA1 also controls the latching of Input Data on Port A. CA1 is a high impedance input, while CA2 represents one standard TTL load in the input mode. In the output mode, CA2 will drive one standard TTL load.

Peripheral Data Port B (PB0-PB7)

Peripheral Data Port B is an 8-line, bidirectional bus which is controlled by an Output Register, Input Register and Data Direction Register in a manner much the same as Data Port A. With respect to Port B, the output signal on line PB7 may be controlled by Timer 1 while Timer 2 may be programmed to count pulses on the PB6 line. Port B lines represent one standard TTL load in the input mode and will drive one TTL load in the output mode. Port B lines are also capable of sourcing 3.0 mA at 1.5 Vdc in the output mode. This allows the outputs to directly drive Darlington transistor circuits. A typical output circuit for Port B is shown in Figure 15.

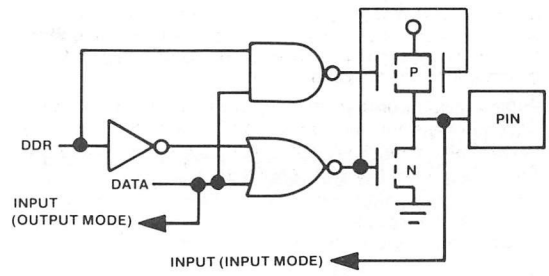


Figure 15. Port B Buffer Circuit (PB0-PB7, CB1, CB2)

Peripheral Data Port B Control Lines (CB1, CB2)

Control lines CB1 and CB2 serve as interrupt inputs or handshake outputs for Peripheral Data Port B. Like Port A, these two control lines control an internal Interrupt Flag with a corresponding Interrupt Enable bit. These lines also serve as a serial data port under control of the Shift Register (SR). Each control line represents one standard TTL load in the input mode and can drive one TTL load in the output mode. Note that CB1 and CB2 cannot drive Darlington transistor circuits.

Functional Description

Peripheral Data Ports (Port A, Port B)

Each Peripheral Data Port operates in conjunction with a Data Direction Register (DDRA or DDRB). Under program control, the Data Direction Registers specify which lines within the port bus are to be designated as inputs or outputs. A Logic 0 in any bit position of the register will cause the corresponding line to serve as an input, while a Logic 1 will cause the line to serve as an output.

When a line is programmed as an output, it is controlled by a corresponding bit in the Output Register (ORA & ORB). A Logic 1 in the Output Register will cause the corresponding output line to go high, while a Logic 0 will cause the line to go low. Under program control, data is written into the Output Register bit positions corresponding to the output lines which have been programmed as outputs. Should data be written into bit positions corresponding to lines which have been programmed as inputs, the output lines will be unaffected.

When reading a Peripheral Data Port, the contents of the corresponding Input Register (IRA or IRB) is transferred onto the Data Bus. When the input latching feature is disabled, Input Register A (IRA) will reflect the logic levels present on the Port A bus lines. However, with input latching enabled and the selected active transition on CA1 having occurred, Input Register A will contain the data present on the Port A bus lines at the time of the transition. In this case, once Input Register A has been read, it will appear transparent, reflecting the current state of the Port A bus lines until the next CA1 latching transition.

With respect to Input Register B, it operates similar to Input Register A except that for those Port B bus lines which have been programmed as outputs, there is a difference. When reading Input Register A, the logic level on the bus line determines whether a Logic 1 or 0 is sensed. However, when reading Input Register B, the logic level stored in Output Register B (ORB) is the logic level sensed. For this reason, those outputs which have large loading effects may cause the reading of Input Register A to result in the reading of a Logic 0 when a 1 was actually programmed, and reading a Logic 1 when a 0 was programmed. However, when reading Input Register B, the logic level read will be correct, regardless of loading on the particular bus line.

For information on formats and operation of the Peripheral Data Port registers, refer to Figures 16, 17 and 18. It should be noted that the input latching modes are controlled by the Auxiliary Control Register (See Figure 24).

Data Transfer—Handshake Control

A powerful feature of the G65SC22 is its ability to provide absolute control over data transfers between the microprocessor and peripheral devices. This control is accomplished by way of "handshake" lines. Port A lines (CA1, CA2) handshake data transfers on both Read and Write operations, while Port B lines (CB1, CB2) handshake data on Write operations only.

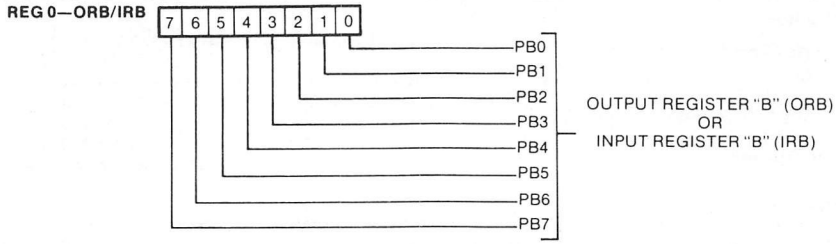
Read Handshake Control

Read Handshaking provides effective control of data transfers from a peripheral device to the microprocessor. To accomplish the Read Handshake, the peripheral device generates a Data Ready signal to the G65SC22 which indicates valid data is present on the Peripheral Data Port bus. In most cases, this Data Ready signal will interrupt the microprocessor, which will then read the data and generate a Data Taken signal. Once the peripheral senses the Data Taken signal, new data will be placed on the bus. This process continues until the data transfer is complete.

Automatic Read Handshaking applies to Peripheral Data Port A only. The Data Ready signal is transmitted by the peripheral device over the CA1 interrupt line, while the Data Taken signal is generated and transmitted to the peripheral device over the CA2 line. When the Data Ready signal is received, it sets an internal flag in the Interrupt Flag Register (IFR). This flag may interrupt the microprocessor or it may be polled under program control. As an option, the Data Taken signal may be either a pulse or a level. In either case, it is set low (Logic 0) by the microprocessor and is cleared by the next Data Ready signal. Refer to Figure 19 for Read Handshake timing and operating sequence.

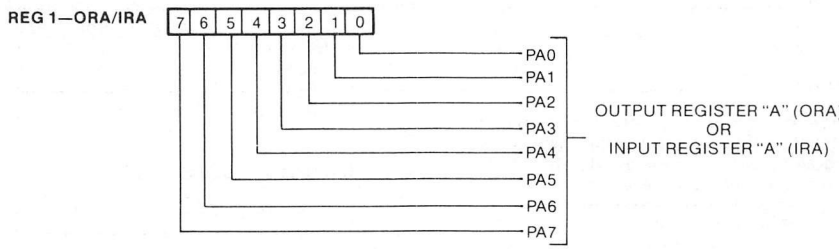
Write Handshake Control

The Write Handshake operation is similar to Read Handshaking. For Write Handshaking, however, the G65SC22 generates the Data Ready signal and the peripheral device must generate the Data Taken return signal. Note that Write Handshaking may occur on both Data Ports (A and B). For a Write Handshake, CA2 or CB2 serve as the Data Ready output and can operate in either the Handshake Mode or the Pulse Mode. The Data Taken signal is received by CA1 or CB1. The Data Taken signal sets a flag in the Interrupt Flag Register and clears the Data Ready output signal. Refer to Figure 20 for Write Handshake timing and operating sequence. Note that the selection of Read or Write Handshake operating modes (CA1, CA2, CB1 and CB2) is accomplished by the Peripheral Control Register (PCR). See Figure 21.



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRB = "1" (OUTPUT)	MPU writes Output Level (ORB)	MPU reads output register bit in ORB. Pin level has no effect
DDRB = "0" (INPUT) (Input latching disabled)	MPU writes into ORB, but no effect on pin level, until DDRB changed.	MPU reads input level on PB pin.
DDRB = "0" (INPUT) (Input latching enabled)		MPU reads IRB bit, which is the level of the PB pin at the time of the last CB1 active transition.

Figure 16. Output Register B (ORB), Input Register B (IRB)



PIN DATA DIRECTION SELECTION	WRITE	READ
DDRA = "1" (OUTPUT) (Input latching disabled)	MPU writes Output Level (ORA)	MPU reads level on PA pin.
DDRA = "1" (OUTPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.
DDRA = "0" (INPUT) (Input latching disabled)	MPU writes into ORA, but no effect on pin level, until DDRA changed.	MPU reads level on PA pin.
DDRA = "0" (INPUT) (Input latching enabled)		MPU reads IRA bit which is the level of the PA pin at the time of the last CA1 active transition.

Figure 17. Output Register A (ORA), Input Register A (IRA)

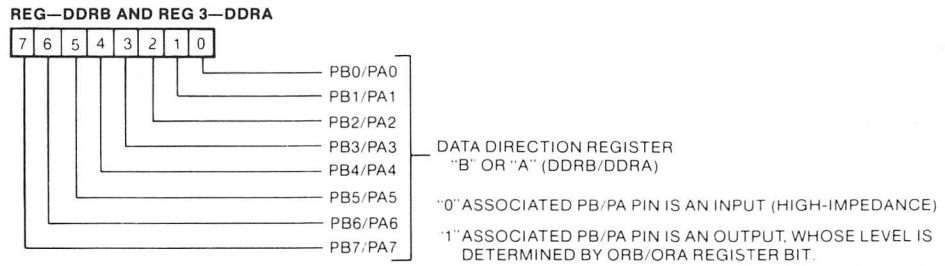


FIGURE 18. Data Direction Registers (DDRB, DDRA)

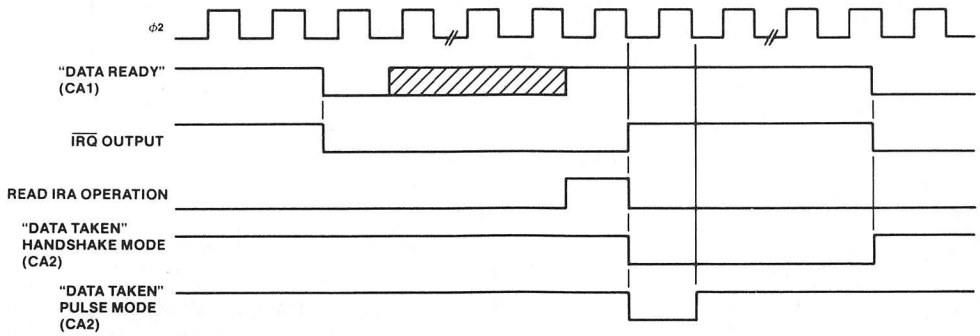


Figure 19. Read Handshake (Port A Only)

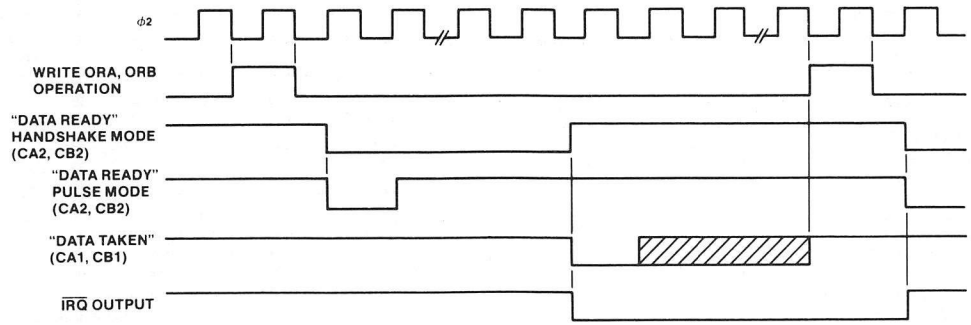


Figure 20. Write Handshake (Ports A and B)

REG 12—PERIPHERAL CONTROL REGISTER

7	6	5	4	3	2	1	0

CB2 CONTROL

7	6	5	Operation
0	0	0	Input-negative action edge
0	0	1	Independent interrupt input-negative edge*
0	1	0	Input-positive active edge
0	1	1	Independent interrupt input-positive edge*
1	0	0	Handshake output
1	0	1	Pulse output
1	1	0	Low output
1	1	1	High output

CB1 INTERRUPT CONTROL

0 = Negative Active Edge
1 = Positive Active Edge

CA1 INTERRUPT CONTROL

0 = Negative Active Edge
1 = Positive Active Edge

CA2 CONTROL

3	2	1	Operation
0	0	0	Input-negative action edge
0	0	1	Independent interrupt input-negative edge*
0	1	0	Input-positive active edge
0	1	1	Independent interrupt input-positive edge*
1	0	0	Handshake output
1	0	1	Pulse output
1	1	0	Low output
1	1	1	High output

*See Note Accompanying Figure 37.

Figure 21. CA1, CA2, CB1, CB2 Control

Timer 1 Operation

Interval Timer T1 consists of two 8-bit latches and a 16-bit counter. The latches serve to store data which is to be loaded into the counter. Once the counter is loaded under program control, it decrements at a Phase 2 ($\phi 2$) clock rate. Upon reaching zero, an Interrupt Flag is set, causing Interrupt Request ($\overline{IRQ}$) to go low (Logic 0) if the corresponding Interrupt Enable bit is set. Once the Timer reaches a count of zero, it will either disable any further interrupts (provided it has been programmed to do so), or it will automatically transfer the contents of the latches into the counter and proceed to decrement again. The counter may also be programmed to invert the output signal on PB7 each time it reaches a count of zero. Each of these counter modes is presented below. The T1 counter format and operation is shown in Figure 22, with corresponding latch format and operation in Figure 23. Additional control bits are provided in the Auxiliary Control Register (bits 6 and 7) to allow selection of Timer T1 operating modes. The four available modes are shown in Figure 24.

It should be noted that the microprocessor does not write directly into the low-order counter (T1C-L). Instead, this half of the counter is loaded automatically from the low-order register when the microprocessor writes into the high-order register and counter. In fact, it may not be necessary to write to the low-order register in some applications since the timing operation is triggered by writing to the high-order register and counter.

Timer 1 One-Shot Mode

Interval Timer T1 may operate in the One-Shot Mode which allows the generation of a single Interrupt Flag each time the Timer is loaded. The Timer can also be programmed to produce a single negative pulse on Data Port line PB7.

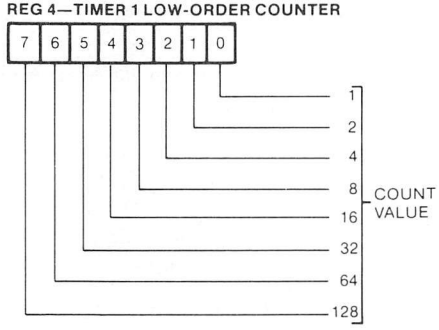
To generate a single interrupt, it is required that bits 6 and 7 of the Auxiliary Control Register be low (Logic 0). The low-order T1 counter (T1C-L) or the low-order T1 latch (T1L-L) must then be loaded with the low-order count value. Note that a load to T1C-L is effectively a load to T1L-L. Next, the high-order count value must be loaded into the high-order T1 counter (T1C-H), at which time the value is simultaneously loaded into high-order T1 latch (T1L-H). During this load sequence, the contents of T1L-L is transferred to T1C-L. The counter will start counting down on the next $\phi 2$ clock following the load sequence into T1C-H, and will decrement at the $\phi 2$ clock rate. Once the T1 counter reaches a zero count, the Interrupt Flag is set. To generate a negative pulse on Data Port line PB7, the sequence is identical to the above except bit 7 of the Auxiliary Control Register must be high (Logic 1). Data Port line PB7 will then go low (Logic 0) following the load to T1C-H, and will go high (Logic 1) again when the counter reaches a zero count.

Once set, the T1 Interrupt Flag is reset by either loading T1C-H, which starts a new count, or by reading T1C-L. Refer to Figure 25 for One-Shot Mode timing information.

Timer 1 Free-Run Mode

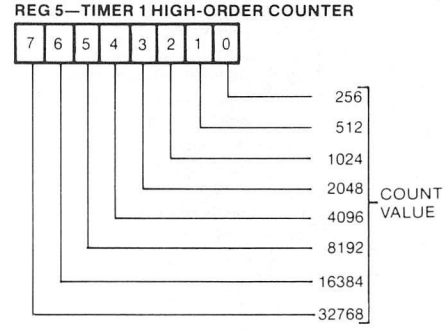
An important advantage within the G65SC22 is the ability of the latches associated with the T1 counter to provide a continuous series of evenly spaced interrupts or a square wave on Data Port line PB7. It should also be noted that the continuous series of interrupts and square waves are not affected by variations in the microprocessor interrupt response time. These advantages are all produced in the Free-Run Mode. When operating in the Free-Run Mode, the Interrupt Flag is set and the signal on PB7 is inverted each time the counter reaches a count of zero. In the Free-Run Mode, however, the counter does not continue to decrement after reaching a zero count. Instead, the counter automatically transfers to contents of the latch into the counter (16 bits) and then decrements from the new count value. As can be seen, it is not necessary to reload the timer in order to set the Interrupt Flag on the next count of zero. When set, the Interrupt Flag can be cleared by either reading T1C-L, by writing directly into the Interrupt Flag Register (IFR) as will be discussed later, or by a load into T1C-H when a new count value is desired.

Since the interval timers are all retriggerable, reloading the counter will always reinitialize the time-out period. Should the microprocessor continue to reload the counter before it reaches zero, counter time-out can be prevented. Timer 1 is able to operate in this manner provided the microprocessor writes into the high-order counter (T1C-H). By loading the latches only, the microprocessor can access the timer during each count-down operation without affecting the time-out in progress. In this way, data loaded into the latches will determine the length of the next subsequent time-out period. This capability is of value in the Free-Run Mode with the output enabled. In the Free-Run Mode, the signal on Data Port line PB7 is inverted and the Interrupt Flag is set with each counter time-out. When the microprocessor responds to the interrupts with new data for the latches, it can determine the period of the next half-cycle during each half-cycle of the output signal on line PB7. In this way, complex waveforms can be generated. Refer to Figure 26 for timing information on the Free-Run Mode.



WRITE—8 bits loaded into T1 low-order latches. Latch contents are transferred into low-order counter at the time the high-order counter is loaded (Reg. 5).

READ—8 bits from T1 low-order counter transferred to MPU. In addition, T1 interrupt flag is reset (bit 6 in interrupt flag register).

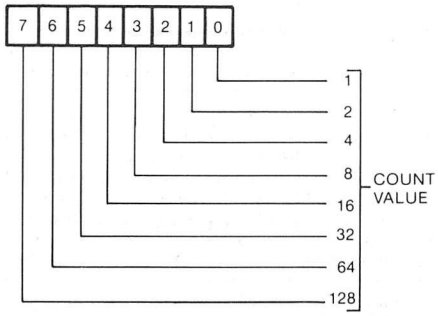


WRITE—8 bits loaded into T1 high-order latches. Also, at this time both high and low-order latches transferred into T1 counter, and initiates countdown. T1 interrupt flag also is reset.

READ—8 bits from T1 high-order counter transferred to MPU.

Figure 22. T1 Counter Format and Operation

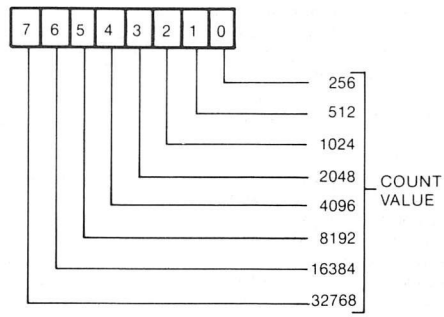
REG 6—TIMER 1 LOW-ORDER LATCHES



WRITE—8 bits loaded into T1 low-order latches. This operation is no different than a write into Reg. 4.

READ—8 bits from T1 low-order latches transferred to MPU. Unlike Reg. 4 operation, this does not cause reset of T1 interrupt flag.

REG 7—TIMER 1 HIGH-ORDER LATCHES

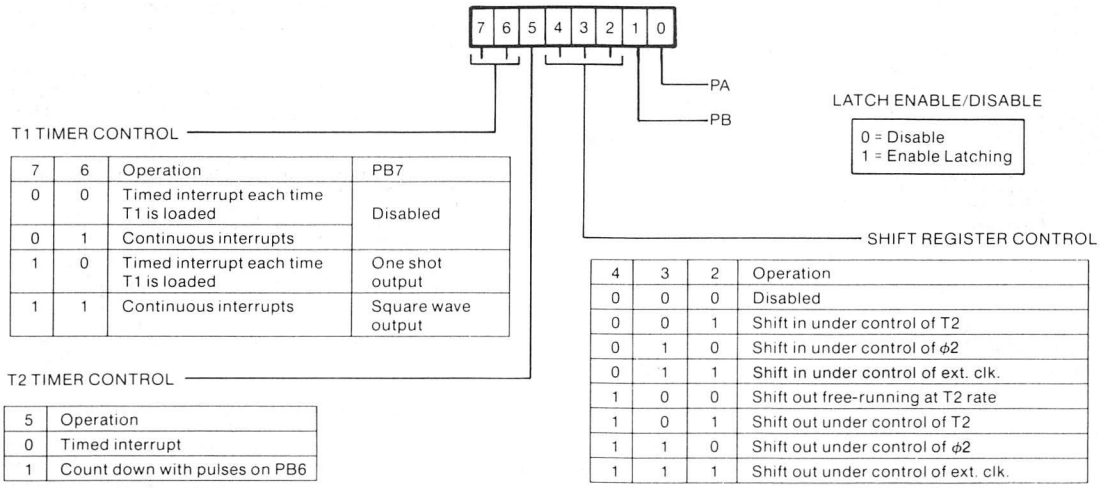


WRITE—8 bits loaded into T1 high-order latches. Unlike Reg. 4 operation no latch-to-counter transfers take place.

READ—8 bits from T1 high-order latches transferred to MPU.

Figure 23. T1 Latch Format and Operation

REG 11—AUXILIARY CONTROL REGISTER



7	6	Operation	PB7
0	0	Timed interrupt each time T1 is loaded	Disabled
0	1	Continuous interrupts	
1	0	Timed interrupt each time T1 is loaded	One shot output
1	1	Continuous interrupts	Square wave output

5	Operation
0	Timed interrupt
1	Count down with pulses on PB6

4	3	2	Operation
0	0	0	Disabled
0	0	1	Shift in under control of T2
0	1	0	Shift in under control of $\phi 2$
0	1	1	Shift in under control of ext. clk.
1	0	0	Shift out free-running at T2 rate
1	0	1	Shift out under control of T2
1	1	0	Shift out under control of $\phi 2$
1	1	1	Shift out under control of ext. clk.

Figure 24. Auxiliary Control Register Format and Operation

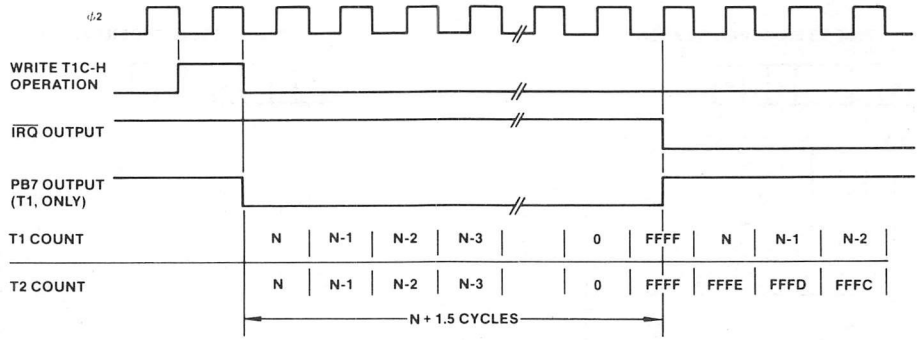
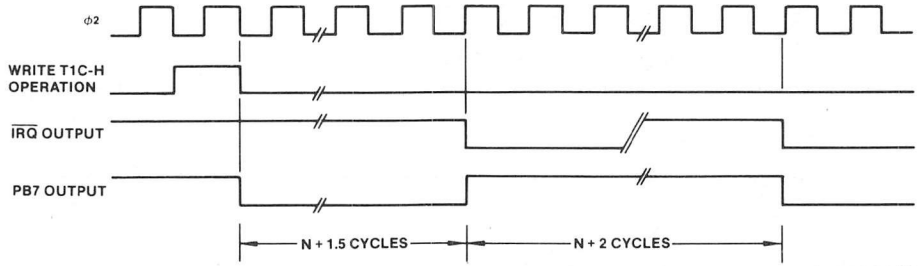


Figure 25. One-Shot Mode (Timer 1 and Timer 2)



Note: A precaution to take in the use of PB7 as the timer output concerns the Data Direction Register contents for PB7. Both DDRB bit 7 and ACR bit 7 must be 1 for PB7 to function as the timer output. If either is a 0, then PB7 functions as a normal output pin, controlled by ORB bit 7.

Figure 26. Free-Run Mode (Timer 1)

Timer 2 Operation

Timer 2 operates in the One-Shot Mode only (as an interval timer), or as a pulse counter for counting negative pulses on Data Port line PB6. A single control bit within the Auxiliary Control Register is used to select between these two modes. Timer 2 is made up of a write-only low-order latch (T2L-L), a read-only low-order counter (T2C-L), and a read/write high-order counter (T2C-H). This 16-bit counter decrements at a $\phi 2$ clock rate. Refer to Figure 27 for T2 counter format and operation.

Timer 2 One-Shot Mode

Operation of Timer 2 in the One-Shot Mode is similar to Timer 1. That is, for each load T2C-H operation, Timer 2 sets the Interrupt Flag for each countdown to zero. However, after a time-out, the T2 counters roll over to all 1s ($FFFF_{16}$) and continue to decrement. This two's complement decrement allows the user to determine how long the T2 Interrupt Flag has been set. Since the Interrupt Flag logic is disabled after the initial interrupt set (zero count), further interrupts cannot be set by a subsequent count to zero. To enable the Interrupt Flag logic, the microprocessor must reload T2C-H. The Interrupt Flag is cleared by either reading T2C-L or by loading T2C-H. Refer to Figure 25 for timing information on the One-Shot Mode.

Timer 2 Pulse Counting Mode

In the Pulse Counting Mode, Timer 2 counts a predetermined number of negative-going pulses on Data Port line PB6. To accomplish this, a count number is loaded into T2C-H, which clears the Interrupt Flag logic and starts the counter to decrement each time a negative pulse is applied to Data Port line PB6. When the T2 counter reaches a count of zero, the Interrupt Flag is set and the counter continues to decrement with each pulse on PB6. To enable the Interrupt Flag for subsequent countdowns, it is necessary to reload T2C-H. The decrement pulse on line PB6 must be low (Logic 0) during the leading edge of the $\phi 2$ clock. Refer to Figure 28 for timing information.

Shift Register Operation

The Shift Register performs bidirectional serial data transfers on line CB2. These transfers are controlled by an internal modulo-8 counter. Shift pulses can be applied to the CB1 line from an external source, or (with proper mode selection) shift pulses may be generated internally which will appear on the CB1 line for controlling external devices. Each Shift Register operating mode is controlled by control bits within the Auxiliary Control Register. Refer to Figure 29 for format and control bit information. Also refer to Figures 30 through 36 for operation of the various Shift Register modes.

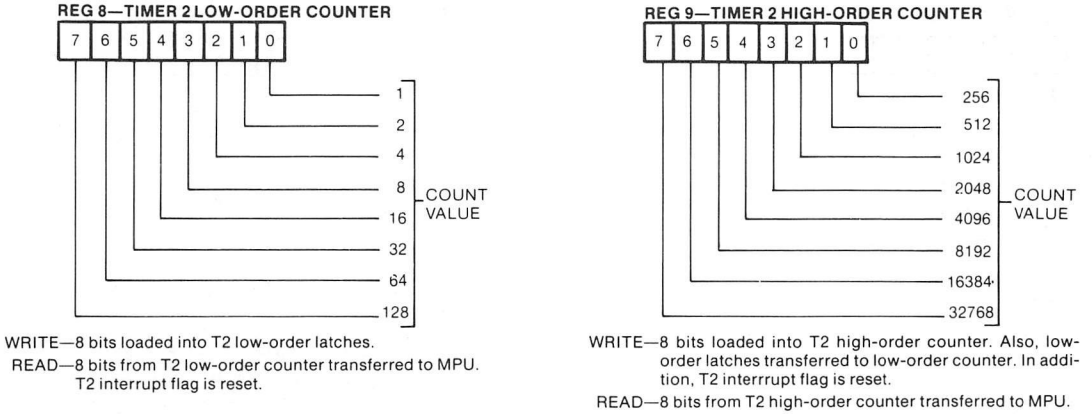


Figure 27. T2 Counter Format and Operation

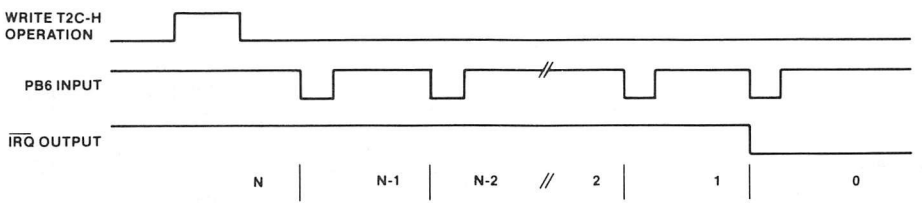


Figure 28. Pulse Counting Mode (Timer 2)

Shift Register Input Modes

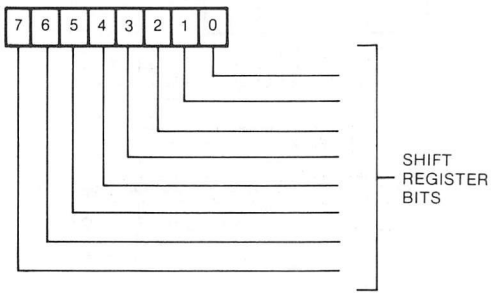
Shift Register Disabled (000)—In the 000 mode, the Shift Register is disabled from all operation. The microprocessor can read or write the Shift Register, but shifting is disabled and both CB1 and CB2 are controlled by bits in the Peripheral Control Register (PCR). The Shift Register Interrupt Flag is held low (disabled).

Shift In—Counter T2 Control (001)—In this mode, the shifting rate is controlled by the low order eight bits of counter T2. Shift pulses are generated on the CB1 line to control shifting in external devices. The time between transitions of the CB1 output clock is determined by the $\phi 2$ clock period and the contents of the low-order T2 latch (N). Shifting occurs by writing or reading the Shift Register. Data is shifted into the low-order bit first, and is then shifted into the next higher order bit on the negative-going edge of each clock pulse. Input data should change before the positive-going edge of the CB1 clock pulse. This data is then shifted into the Shift Register during the $\phi 2$ clock cycle following the positive-going edge of the CB1 clock pulse. After eight CB1 clock pulses, the Shift Register Interrupt Flag will set and $\overline{IRQ}$ will go low (Logic 0). Refer to Figure 30.

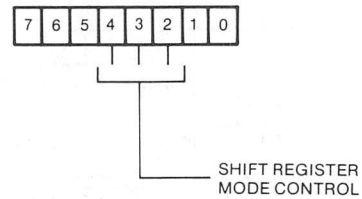
Shift In—$\phi 2$ Clock Control (010)—In this mode, the shift rate is controlled by the $\phi 2$ clock frequency. Shift pulses are generated on the CB1 line to control shifting in external devices. Timer 2 operates as an independent interval timer and has no influence on the Shift Register. Shifting occurs by reading or writing the Shift Register. Data is shifted into the low order bit first, and is then shifted into the next higher order bit on the trailing edge of the $\phi 2$ clock pulse. After eight clock pulses, the Shift Register Interrupt Flag will be set, and output clock pulses on the CB1 line will stop. Refer to Figure 31.

Shift In—External CB1 Clock Control (011)—In this mode, CB1 serves as an input to the Shift Register. In this way, an external device can load the Shift Register at its own pace. The Shift Register counter will interrupt the microprocessor after each eight bits have been shifted in. The Shift Register counter does not stop the shifting operation. Its function is simply that of a pulse counter. Reading or writing the Shift Register resets the Interrupt Flag and initializes the counter to count another eight pulses. Note that data is shifted during the first $\phi 2$ clock cycle following the positive-going edge of the CB1 shift pulse. For this reason, data must be held stable during the first full cycle following CB1 going high. Refer to Figure 32.

REG 10—SHIFT REGISTER



REG 11—AUXILIARY CONTROL REGISTER



4	3	2	Operation
0	0	0	Disabled
0	0	1	Shift in under control of T2
0	1	0	Shift in under control of $\phi 2$
0	1	1	Shift in under control of ext. clk
1	0	0	Shift out free-running at T2 rate
1	0	1	Shift out under control of T2
1	1	0	Shift out under control of $\phi 2$
1	1	1	Shift out under control of ext. clk.

Notes:
1. When shifting out, bit 7 is the first bit out and simultaneously is rotated back into bit 0.
2. When shifting in, bits initially enter bit 0 and are shifted towards bit 7.

Figure 29. Shift Register and Auxiliary Control Register Control Bits

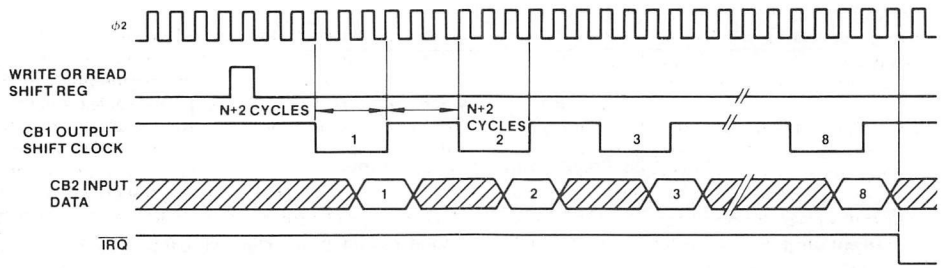


Figure 30. Shift In—Counter T2 Control

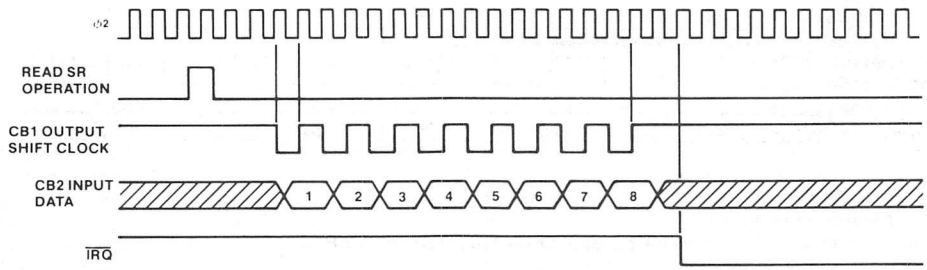


Figure 31. Shift In—$\phi 2$ Clock Control

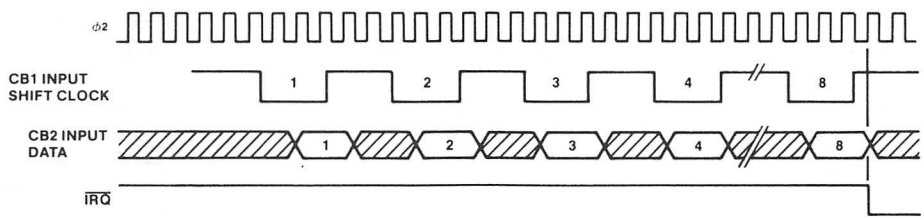


Figure 32. Shift In—External CB1 Clock Control

Shift Register Output Modes

Shift Out—Free Running at T2 Rate (100)—This mode is similar to mode 101 in which the shifting rate is determined by T2. However, in mode 100 the Shift Register Counter does not stop the shifting operation. Since Shift Register bit 7 (SR7) is recirculated back into bit 0, the eight bits loaded into the Shift Register will be clocked onto the CR2 line repetitively. In this mode, the Shift Register Counter is disabled and $\overline{IRQ}$ is never set. Refer to Figure 33.

Shift Out—T2 Control (101)—In this mode, the shift rate is controlled by T2 (as in mode 100). However, with each read or write of the Shift Register, the Shift Register Counter is reset and eight bits are shifted onto the CB2 line. At the same time, eight shift pulses are placed on the CB1 line to control shifting in external devices. After the eight shift pulses, the shifting is disabled, the Interrupt Flag is set, and CB2 will remain at the last data level. Refer to Figure 34.

Shift Out—ϕ2 Clock Control (110)—In this mode, the shift rate is controlled by the system ϕ2 Clock. Refer to Figure 35.

Shift Out—External CB1 Clock Control (111)—In this mode, shifting is controlled by external pulses applied to the CB1 line. The Shift Register Counter sets the Interrupt Flag for each eight-pulse count, but does not disable the shifting function. Each time the microprocessor reads or writes the Shift Register, the Interrupt Flag is reset and the counter is initialized to begin counting the next eight pulses on the CB1 line. After eight shift pulses, the Interrupt Flag is set. The microprocessor can then load the Shift Register with the next eight bits of data. Refer to Figure 36.

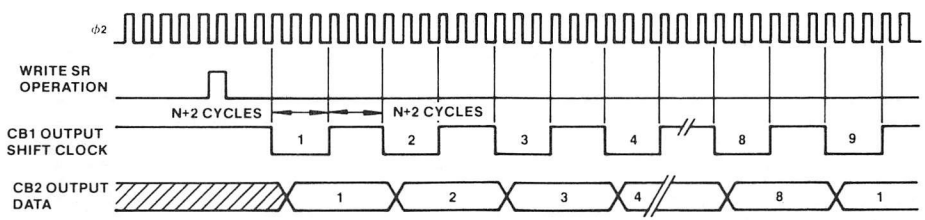


Figure 33. Shift Out—Free Running T2 Rate

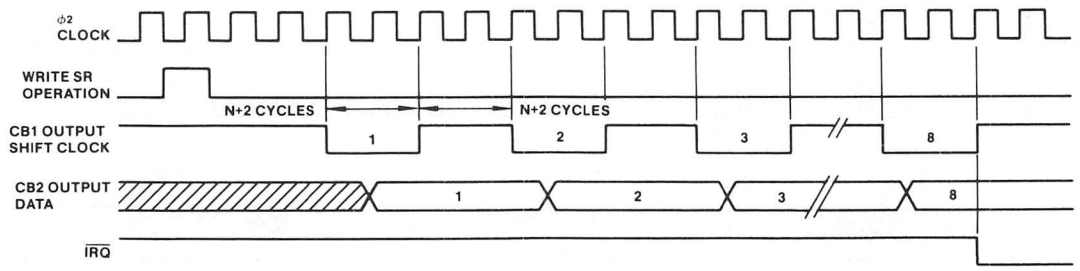


Figure 34. Shift Out—T2 Control

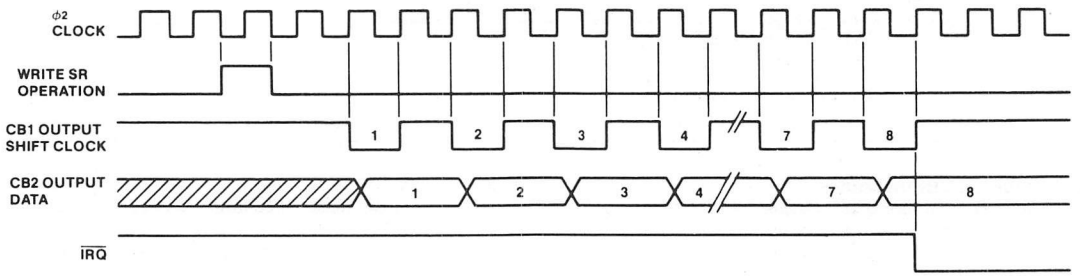


Figure 35. Shift Out—ϕ2 Control

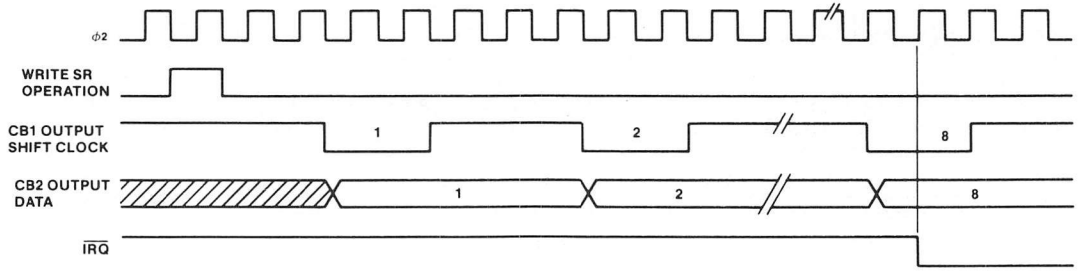


Figure 36. Shift Out—External CB1 Clock Control

Interrupt Operation

There are three basic interrupt operations, including: setting the interrupt flag within the Interrupt Flag Register (IFR), enabling the interrupt by way of a corresponding bit in the Interrupt Enable Register (IER), and signaling the microprocessor with an Interrupt Request ($\overline{IRQ}$). An Interrupt Flag can be set by conditions internal to the chip or by inputs to the chip from external sources. Normally, an Interrupt Flag will remain set until the interrupt is serviced. To determine the source of an interrupt, the microprocessor must examine each flag in order, from highest to lowest priority. This is accomplished by reading the contents of the Interrupt Flag Register into the microprocessor accumulator, shifting the contents either left or right and then using conditional branch instructions to detect an active interrupt. Each Interrupt Flag has a corresponding Interrupt Enable bit in the Interrupt Enable Register. The enable bits are controlled by the microprocessor (set or reset). If an Interrupt Flag is high (Logic 1), and the corresponding Interrupt Enable bit is high (Logic 1), the Interrupt Request ($\overline{IRQ}$) will go low (Logic 0). $\overline{IRQ}$ is an open-collector output which can be wire-ORed with other devices within the system.

All Interrupt Flags are contained within a single Interrupt Flag Register. Bit 7 of this register will be high (Logic 1) whenever an Interrupt Flag is set, thus allowing convenient polling of several devices within a system to determine the source of the interrupt.

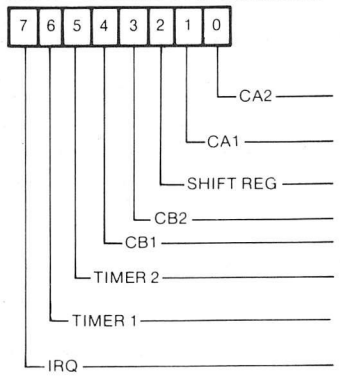
The Interrupt Flag Register (IFR) and Interrupt Enable Register (IER) format and operation is shown in Figures 37 and 38 respectively. The Interrupt Flag Register may be read directly by the microprocessor, and individual flag bits may be cleared by writing a "1" into the appropriate bit of the IFR. Bit 7 of the IFR indicates the status of the Interrupt Request ($\overline{IRQ}$) output. Bit 7 corresponds to the following logic function: IRQ = IFR6 x IER6 + IFR5 x IER5 + IFR4 x IER4 + IFR3 x IER3 + IFR2 x IER2 + IFR1 x IER1 + IFR0 x IER0. Note: x = Logic AND, + = Logic OR.

Bit 7 is not a flag. For this reason, bit 7 is not directly cleared by writing a "1" into its bit position. It can be cleared, however, by clearing all the flags within the register, or by disabling all active interrupts as presented in the next section.

Each Interrupt Flag within the IFR has a corresponding enable bit in the Interrupt Enable Register (IER). The microprocessor can set or clear selected bits within the IER. This allows the control of individual interrupts without affecting others. To set or clear a particular Interrupt Enable bit, the microprocessor must write to address 1110 (IER address). During this write operation, if bit 7 on the Data Bus is a "0", each "1" in bits 6 thru 0 will clear the corresponding bit in the Interrupt Enable Register. For each "0" in bits 6 thru 0, the corresponding bit in the IER will be unaffected.

Setting selected bits in the IER is accomplished by writing to the same address with bit 7 on the Data Bus set to a "1". In this case, each "1" in bits 6 thru 0 will set the corresponding bit to a "1". For each "0", the corresponding bit will be unaffected. This method of controlling the bits in the Interrupt Enable Register allows convenient user control of interrupts during system operation. The microprocessor can also read the contents of the IER by placing the proper address on the Register Select and Chip Select inputs with the R/$\overline{W}$ line high. Bit 7 will be read as a "1".

REG 13—INTERRUPT FLAG REGISTER

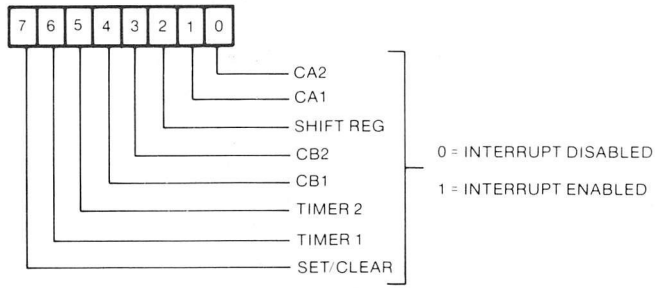


	SET BY	CLEARED BY
CA2	CA2 active edge	Read or write Reg. 1 (ORA)*
CA1	CA1 active edge	Read or write Reg. 1 (ORA)
SHIFT REG	Complete 8 shifts	Read or write Shift Reg.
CB2	CB2 active edge	Read or write ORB*
CB1	CB1 active edge	Read or write ORB
TIMER 2	Time-out of T2	Read T2 low or write T2 high
TIMER 1	Time-out of T1	Read T1 low or write T1 high
IRQ	Any enabled interrupt	Clear all interrupts

*If the CA2/CB2 control in the PCR is selected as "independent" interrupt input, then reading or writing the output register ORA/ORB will not clear the flag bit. Instead, the bit must be cleared by writing into the IFR, as described previously.

Figure 37. Interrupt Flag Register (IFR)

REG 14—INTERRUPT ENABLE REGISTER



Notes:
1. If bit 7 is a "0", then each "1" in bits 0-6 disables the corresponding interrupt.
2. If bit 7 is a "1", then each "1" in bits 0-6 enables the corresponding interrupt.
3. If a read of this register is done, bit 7 will be "1" and all other bits will reflect their enable/disable state.

Figure 38. Interrupt Enable Register (IER)

G65SC32

Microcircuits

CMOS RAM, I/O, Timer

Features

- CMOS process technology for low power consumption
- Fully compatible with NMOS 6532 devices
- Bus compatible with 6500 and 6800 microprocessors
- Low power consumption (2 mA at 1 MHz)
- 128 X 8 bit static RAM
- Two 8-bit bidirectional peripheral data ports
- Two programmable Data Direction Registers
- Programmable Edge Sense Interrupt function
- Interrupt Timer with programmable interrupt intervals
- Peripheral I/O Port B allows direct transister drive
- High impedance three-state Data Bus
- Available in 40-pin dual-in-line package

General Description

The G65SC32 is a programmable RAM, I/O, Timer device for use with the G65SCXXX series 8-bit microprocessor family. The G65SC32 includes functions for programmed control of up to two peripheral devices (Port A and Port B). These functions include:

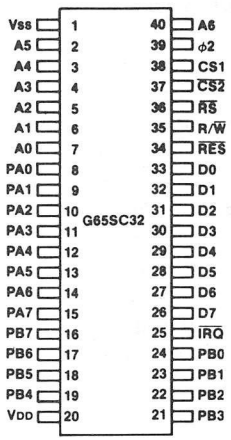
- 128 X 8 bit static RAM for microprocessor scratch pad activity.
- Two program controlled 8-bit bidirectional Data Ports for direct interfacing between the microprocessor and selected peripheral units.
- Two programmable Data Direction Registers (A and B) for data direction control at each peripheral Data Port.
- A programmable Interrupt Timer with interrupt timing capability in intervals ranging from 1 to 262,144 clock periods.
- Edge-detect interrupt circuitry for interrupt generation on active edge transitions.

The G65SC32 offers the many advantages of GTE's leading edge CMOS technology, i.e., increased noise immunity, higher reliability, and greatly reduced power consumption.

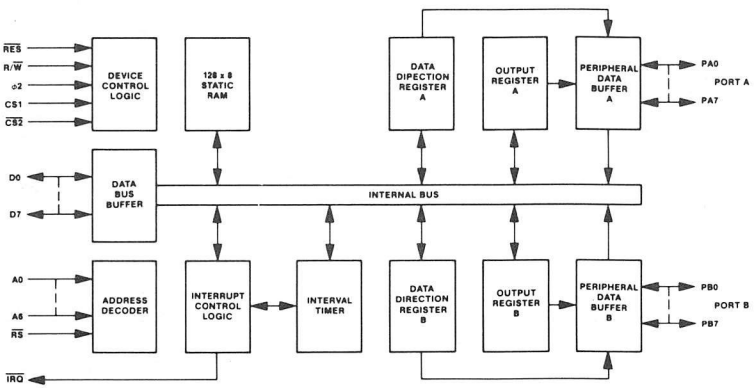
Pin Function Table

A0-A6	Address Bus	$\overline{RS}$	Function Select
D0-D7	Data Bus	R/$\overline{W}$	Read/Write
PA0-PA7	Peripheral I/O Port A	$\overline{RES}$	Reset
PB0-PB7	Peripheral I/O Port B	$\overline{IRQ}$	Interrupt
ϕ2	Phase 2 Internal Clock	VDD	Power Supply (+5V)
CS1/$\overline{CS2}$	Device Select	VSS	Internal Logic Ground

Pin Configuration



Block Diagram



PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input/Output Voltage	V_{IN}	-0.3V to V_{DD} + 0.3V
Operating Temperature	T_A	-40°C to +85°C
Storage Temperature	T_S	-55°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these rating may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40°C to +85°C

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins, A0-A6, ϕ2, CS1, $\overline{CS2}$, R/$\overline{W}$, $\overline{RES}$, $\overline{RS}$)	I_{IN}		±1.0	μA
Three-State, Leakage Current (V_{IN} = 0.4 to 2.4V), D0-D7, $\overline{IRQ}$	I_{TSI}		±10.0	μA
Input High Current (V_{IH} = 2.4V), Peripheral Inputs with Pullups, PA0-PA7, PB0-PB7	I_{IH}	-200		μA
Input Low Current (V_{IL} = 0.4V), Peripheral Inputs with Pullups, PA0-PA7, PB0-PB7	I_{IL}		1.6	mA
Output Low Voltage (I_{OL} = 3.2 mA), D0-D7, PA0-PA7, PB0-PB7, $\overline{IRQ}$	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA), D0-D7, PA0-PA7, PB0-PB7, $\overline{IRQ}$	V_{OH}	2.4		V
Output High Current (Sourcing) (V_{OH} = 1.5V, Direct Transistor Drive), PB0-PB7	I_{OH}	-3.0		mA
Supply Current (No Load) f = 1 MHz	I_{DD}		2.0	mA
f = 2 MHz	I_{DD}		4.0	mA
f = 3 MHz	I_{DD}		6.0	mA
f = 4 MHz	I_{DD}		8.0	mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz)	P_D		11.0	mW
Standby (Static)	P_{DSB}		11.0	μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40°C to +85°C

		G65SC32-1		G65SC32-2		G65SC32-3		G65SC32-4		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing (Figure 1)										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	nS
Write Timing (Figure 2)										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS
Peripheral Data Delay	t_{CPW}	—	1000	—	500	—	330	—	250	nS

Timing Diagrams

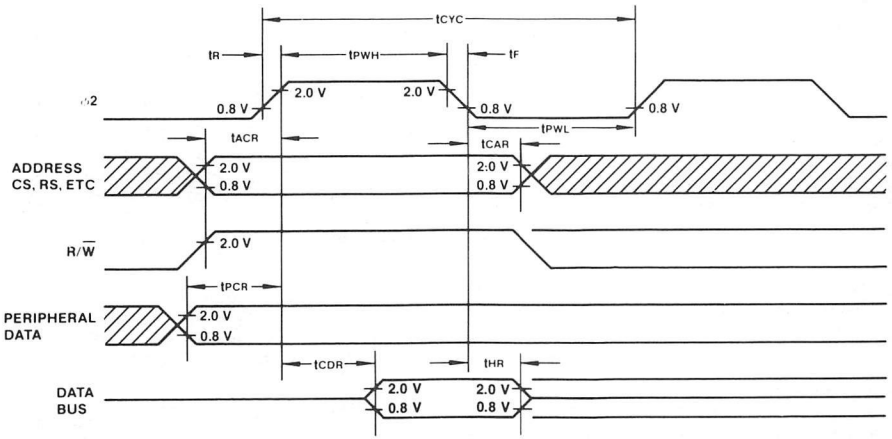


Figure 1. Read Timing

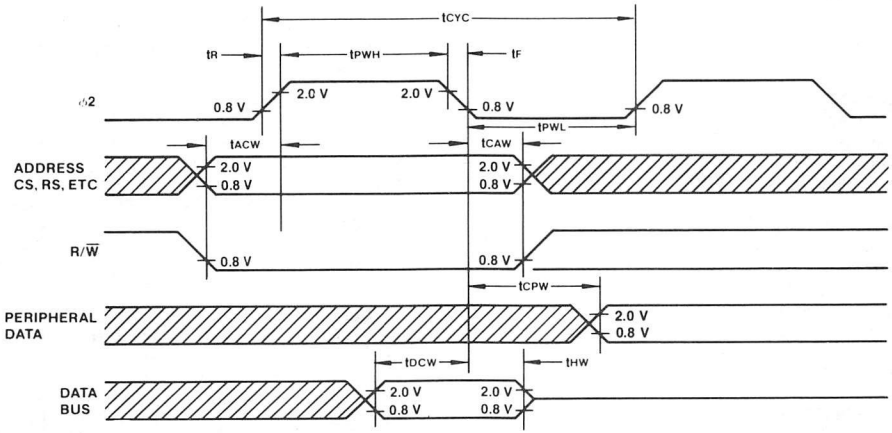
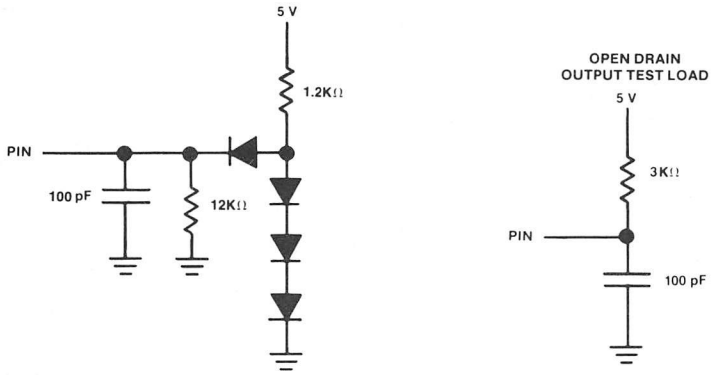


Figure 2. Write Timing

Test Load



Interface Signals

Input Clock ($\phi 2$)

The Input Clock consists of a system $\phi 2$ clock source. This clock can be either a low level clock ($V_{IL} < 0.4$, $V_{IH} > 2.4$) or a high level clock ($V_{IL} < 0.2$, $V_{IH} = V_{DD} + 0.3$ "or" $V_{DD} - 0.2$).

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause all four I/O registers to be zeroed. This in turn will cause all lines within the I/O bus to serve as inputs. This arrangement protects external components from possible damage and/or erroneous data being written during system configuration under software control. Also, the Data Bus Buffers are placed in an Off-State during any $\overline{RES}$. Interrupt capability is disabled during $\overline{RES}$. The $\overline{RES}$ signal must be held low for a minimum of one clock period during a $\overline{RES}$ function.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ output signal is derived from the Interrupt Control Logic, and is normally in the high state (Logic "1"). When in the low state (Logic "0"), $\overline{IRQ}$ indicates an interrupt exists within the G65SC32. This interrupt output may be activated (Logic "0") by a logical transition on line PA7 of peripheral I/O Bus A, or by timeout of the Interval Timer. Interrupt Request is an open-drain output, thus allowing several units to be wire-ORed to a common microprocessor $\overline{IRQ}$ input pin.

Data Bus (D0-D7)

The G65SC32 contains eight bidirectional data lines (D0-D7) for transfer of data to and from the microprocessor. The Data Buffer is active during a Read operation, and is held in the Off-State during all other operations.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the transfer of data to and from the G65SC32. When R/$\overline{W}$ is in the high state (Logic "1"), the microprocessor is allowed to read data from the G65SC32. Conversely, when R/$\overline{W}$ is in the low state (Logic "0"), the microprocessor may write data to the G65SC32. Read/Write functions must always be preceded by proper addressing.

Peripheral Data Ports (PA0-PA7 and PB0-PB7)

The G65SC32 contains two 8-bit peripheral I/O Ports... Port A (lines PA0-PA7) and Port B (lines PB0-PB7). An important feature of the G65SC32 is that each peripheral port bus line is individually programmable as either an input or an output. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. This feature is accomplished by the Data Direction Registers. When a "0" is written to any bit position of the Data Direction Register (DDRA or DDRB), the corresponding line will be programmed as an input. Likewise, when a "1" is written into any bit position of DDRA or DDRB, the corresponding data line will serve as an output.

When an I/O Port line has been programmed as an input and its Output Register (ORA or ORB) is read by the microprocessor, the TTL level on the I/O Port line will be transferred to the Data Bus (D0-D7). When programmed as outputs, the I/O Port lines will reflect data as written by the microprocessor into the Output Registers. I/O Port line PA7 also serves an Edge Sense Interrupt function as described in the following sections.

Address and Select Lines (A0-A6, $\overline{RS}$, CS1 and $\overline{CS2}$)

Address lines A0-A6 serve to address the RAM, I/O Registers, Timer and Flag Register. CS1 and $\overline{CS2}$ are used to select (enable access to) the G65SC32.

Functional Description

In reference to the Block Diagram on page one, the G65SC32 is shown to consist of four basic functions; that is, RAM, I/O, Timer and Interrupt Control. RAM interfaces directly with the microprocessor by way of the Data Bus and Address Lines. The peripheral I/O functions consist of two 8-bit I/O Ports. Each port is supported by a Data Direction Register and an Output Register.

RAM (128 Bytes, 1024 Bits)

Within the G65SC32 is a 128 X 8 bit static RAM. This RAM is used as a scratch pad or special data buffer, and is addressed by A0-A6 (Byte Select), $\overline{RS}$, CS1 and $\overline{CS2}$.

Peripheral I/O Port Registers

The peripheral I/O Port Registers consist of two Data Direction Registers and two data Output Registers. The Data Direction Register (A and B) controls the direction of data into and out of the peripheral I/O Ports as described under the Peripheral Data Ports Section above. The voltage level on any I/O Port line which has been programmed as an output, is determined by the corresponding bit in the Output Register (ORA or ORB).

During a peripheral Read operation over I/O Port A, data is read directly from the I/O Port bus (PA0-PA7). During this Read operation, should a particular PA line be programmed as an output, data transferred into the microprocessor will be identical to the corresponding data in Output Register A providing that line loading is such that the line voltage is $\geq$ 2.4 volts for a Logic "1", and $\leq$ 0.4 volts for a Logic "0". Under severe loading conditions where these voltage limits cannot be guaranteed, the resulting Read operation may not match the contents of Output Register A.

The output buffer which services I/O Port B (PB0-PB7) is different from the buffers for I/O Port A. The buffers for Port B are push-pull devices capable of sourcing 3 mA at 1.5 volts. This allows these lines to directly drive transistor circuits. To ensure valid data will be read during a peripheral Read operation, I/O Port B contains logic which allows the microprocessor to read the contents of Output Register B instead of reading directly from the Port B data bus.

Interval Timer

Figure 3 shows the three basic functions of the Interval Timer section. These functions include: a preliminary divide-down register, a programmable 8-bit register, and all necessary interrupt logic.

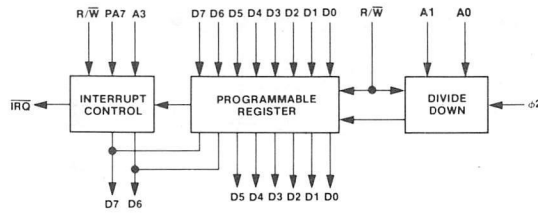


Figure 3. Basic Functions of Interval Timer

The Interval Timer can be programmed to count up to 256 time intervals. Each time interval can be selected as 1T, 8T, 64T, or 1024T increments, where T is the system clock ($\phi 2$) period. When a full interval count has been reached, the interrupt flag is set to the Logic "1" state. Once the flag has been set, the internal clock starts counting down at a 1T rate to a maximum count of -255T. This arrangement allows the user to read the counter and thus determine the elapsed time since the interrupt was set.

The G65SC32's internal Data Bus is used to transfer data to and from the Interval Timer. For example, if a count of 52 time intervals is desired, the pattern 00110100 would be put on the Data Bus and written into the Interval Time Register. During the time when data is being written into the Interval Timer, timing intervals 1,8,64 and 1024T are decoded from address lines A0 and A1. During Read and Write operations, address line A3 controls the interrupt capability of $\overline{IRQ}$. That is, when A3=1, $\overline{IRQ}$ is enabled. When A3=0, $\overline{IRQ}$ is disabled. In either case, when timeout occurs, bit 7 of the Interrupt Flag Register is set. This flag is cleared when the Timer register is either read to or written from by the microprocessor. When $\overline{IRQ}$ is enabled by A3 and an interrupt occurs, $\overline{IRQ}$ will go low. Should the Timer be read prior to the interrupt flag being set, the number of remaining time intervals will be read, i.e., 51, 50, 49, etc.

Once the Timer has counted down to 00000000, an interrupt will occur on the next count time which will result in the Timer reading 11111111. Following the interrupt, the Timer registers decrements at a divide by "1" rate of the clock system. After interrupt, should the Timer read a value of 11100100, then the time since the last interrupt is 28T. The value read is in two's complement as follows:

Value read = 11100100
Complement = 00011011
Add 1 = 00011100 = 28T (28 $\phi 2$ clock periods)

Thus, to arrive at the total elapsed time since the Timer count was originally program set, simply perform a two's complement of the Timer value and add this to the original time value written into the Timer. For example, assume the original time written was 00110100 (=52). With a divide-by-8T, total time to interrupt would be (52 X 8) + 1 = 417T. In this case, total elapsed time would then be 416T + 28T = 444T, assuming the value read after interrupt was 11100100.

Following an interrupt, whenever the Timer is read or written the interrupt is reset. However, should the Timer be read at the same time the interrupt occurs, the interrupt flag will not reset. Figure 4 is an example of Timer Interrupt Timing.

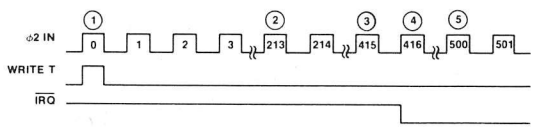


Figure 4. Timer Interrupt Timing

1. Data written into Interval Timers: $00110100 = 52_{10}$
2. Data in Interval Timer: $000110100 = 25_{10}$
   i.e., $52 - \frac{213}{8} - 1 = 52 - 26 - 1 = 25$
3. Data in Interval Timer: $00000000 = 0_{10}$
   i.e., $52 - \frac{415}{8} - 1 = 52 - 51 - 1 = 0$
4. Interrupt occurred at $\phi 2$ clock pulse number 416
   Data in Interval Timer = 11111111
5. Data in Interval Timer: 10101100
   Two's complement: $01010100 = 84_{10}$
   Therefore, $84 + (52 \times 8) = 500_{10}$

When reading the timer following an interrupt, address line A3 must be low such that $\overline{IRQ}$ will be disabled. This procedure prevents future interrupts until a future Write operation has occurred.

Interrupt Flag Register

The Interrupt Flag Register consists of two bits ... the Timer interrupt flag (bit 7) and the PA7 Edge Sense Interrupt flag (bit 6). Whenever a Read operation is performed on the Interrupt Flag Register, the two bits are transferred to the microprocessor via the internal Data Bus. Figure 5 shows the Interrupt Flag Register bit configuration.

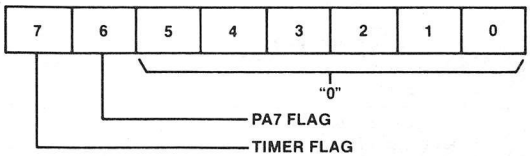


Figure 5. Interrupt Flag Register

It should be noted that the PA7 flag is cleared when the Interrupt Flag Register is read. Also, the Timer flag is cleared when the Timer is either read or written.

Addressing

The G65SC32 is addressed by way of the 7-bit Address Bus (A0-A6), the $\overline{RS}$ input, and the two Chip Select inputs ($\overline{CS1}$ and $\overline{CS2}$). To address the RAM, $\overline{CS1}$ must be high with $\overline{CS2}$ and $\overline{RS}$ both low. To address the I/O and Interval Timer, $\overline{CS1}$ and $\overline{RS}$ must be high with $\overline{CS2}$ low. It is apparent that in order to access the G65SC32 device, $\overline{CS1}$ must be high and $\overline{CS2}$ must be low. The $\overline{RS}$ input is used to distinguish between the RAM and the I/O — Interval Timer Sections. When $\overline{RS}$ is low, RAM is addressed. When $\overline{RS}$ is high, the I/O — Interval Timer Section is addressed. To distinguish between Interval Timer and I/O, address line A2 is used. With A2 high, the Interval Timer is accessed. With A2 low, the I/O registers are accessed. Table 1 provides addressing requirements for the G65SC32.

Edge Sense Interrupt

In addition to its use as a peripheral I/O line, PA7 can also function as an Edge Sense Interrupt input. In the interrupt mode, an active transition on line PA7 will set the internal interrupt flag (bit 6 of the Interrupt Flag Register). When this occurs, providing the PA7 interrupt has been enabled, the $\overline{IRQ}$ output will go low.

Control of the PA7 edge detection logic is accomplished by a Write operation to one of four addresses. The data lines for this Write operation are "don't care" and the addresses to be used can be found in Table 1.

Setting the internal interrupt flag by an active transition on PA7 is always enabled, independent of whether PA7 is set up as an input or output by the Data Direction Register.

The Reset signal ($\overline{RES}$) will disable the PA7 interrupt and at the same time set the active transition logic to the negative edge-detect state. During the $\overline{RES}$ operation, the interrupt flag may be set by a negative transition of PA7. This being the case, it may therefore be necessary to clear the interrupt flag prior to being enabled for its normal use as an edge detecting input. This special Reset can be achieved by reading the Interrupt Flag Register.

I/O Register—Timer Addressing

Table 1 provides the address decoding for all internal functions and Timer programming. Address line A2 distinguishes the I/O registers from the Timer. When A2 is low and $\overline{RS}$ is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 may be used to address the desired register.

With A2 high and $\overline{RS}$ high, the Timer is selected, and address lines A1 and A0 are available to decode the "divide-by" matrix as defined in Table 1. Address line A3 is used to enable the interrupt flag to the $\overline{IRQ}$ output.

Address Decoding

Table 1. G65SC32 Address Decoding

Operation	$\overline{RS}$	R/$\overline{W}$	A4	A3	A2	A1	A0
Write RAM	0	0	—	—	—	—	—
Read RAM	0	1	—	—	—	—	—
Write Output Reg A	1	0	—	—	0	0	0
Read Output Reg A	1	1	—	—	0	0	0
Write DDRA	1	0	—	—	0	0	1
Read DDRA	1	1	—	—	0	0	1
Write Output Reg B	1	0	—	—	0	1	0
Read Output Reg B	1	1	—	—	0	1	0
Write DDRB	1	0	—	—	0	1	1
Read DDRB	1	1	—	—	0	1	1
Write Timer							
÷ 1T	1	0	1	(a)	1	0	0
÷ 8T	1	0	1	(a)	1	0	1
÷ 64T	1	0	1	(a)	1	1	0
÷ 1024T	1	0	1	(a)	1	1	1
Read Timer	1	1	—	(a)	1	—	0
Read Interrupt Flag	1	1	—	—	1	—	1
Write Edge Detect Control	1	0	0	—	1	(b)	(c)

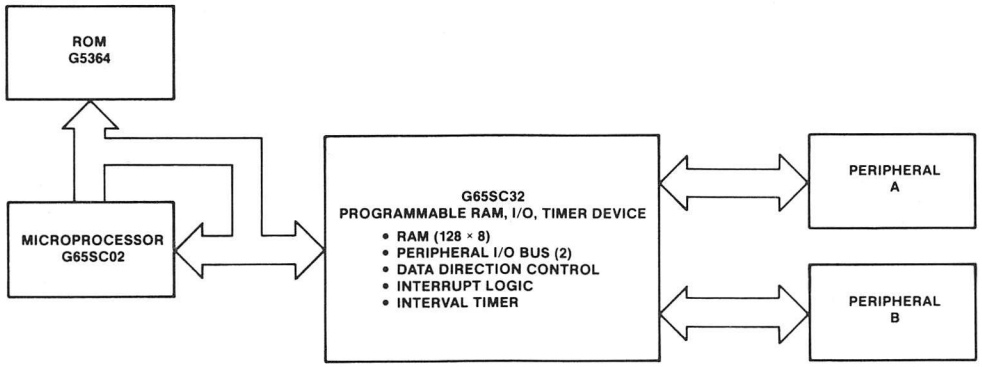
Notes: — = Don't Care, "1" = High Level ($\geq$ 2.4V), "0" = Low Level ($\leq$ 0.4V)

(a) A3 = 0 to Disable Interrupt from Timer to $\overline{IRQ}$
A3 = 1 to Enable Interrupt from Timer to $\overline{IRQ}$

(b) A1 = 0 to Disable Interrupt from PA7 to $\overline{IRQ}$
A1 = 1 to Enable Interrupt from PA7 to $\overline{IRQ}$

(c) A0 = 0 for Negative Edge-Detect
A0 = 1 for Positive Edge-Detect

Application Diagram



G65SC51

Microcircuits

CMOS Asynchronous Communications Interface Adapter

Features

- CMOS process technology for low power consumption
- 15 programmable baud rates (50 to 19,200 baud)
- External 16X clock input for nonstandard baud rates to 125,000 baud
- Programmable interrupt and status registers
- Full-duplex or half-duplex operating modes
- Selectable 5, 6, 7, 8 or 9 bit transmission rates
- Programmable word length, parity generation and detection, and number of stop bits
- Programmable parity options—odd, even, none, mark or space
- Includes data set and modem control signals
- False start bit detection
- Serial echo mode
- Four operating frequencies—1, 2, 3 and 4 MHz

General Description

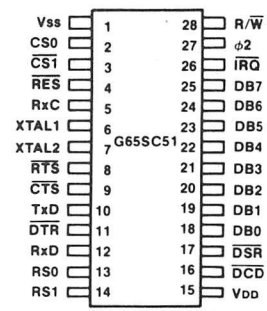
The GTE G65SC51 is an Asynchronous Communications Interface Adapter which offers many versatile features for interfacing 6500/6800 microprocessors to serial communication data sets and modems. The G65SC51's most significant feature is its internal baud rate generator, allowing programmable baud rate selection from 50 to 19,200 baud. This full range of baud rates is derived from a single standard 1.8432 MHz external crystal. For non-standard baud rates up to 125,000 baud, an external 16X clock input is provided. In addition to its powerful communications control features, the G65SC51 offers the advantages of GTE's leading edge CMOS technology, i.e., increased noise immunity, higher reliablity, and greatly reduced power consumption.

Pin Function Table

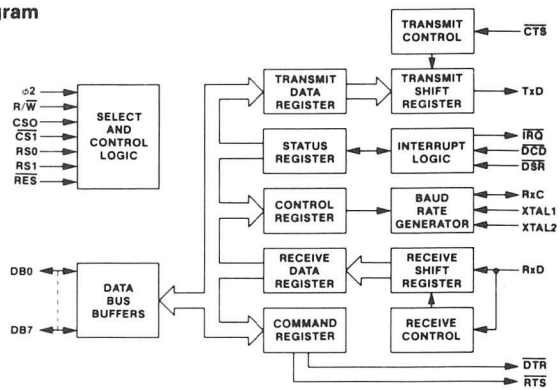
CS0, $\overline{CS1}$	Chip Select
$\overline{RES}$	Reset
$\phi 2$	Input Clock
R/$\overline{W}$	Read/Write
$\overline{IRQ}$	Interrupt Request
RS0, RS1	Register Selects
XTAL1, XTAL2	Crystal Inputs
TxD	Transmit Data
RxD	Receive Data

RxC	Receive Clock
$\overline{RTS}$	Request to Send
$\overline{CTS}$	Clear to Send
$\overline{DTR}$	Data Terminal Ready
$\overline{DSR}$	Data Set Ready
$\overline{DCD}$	Data Carrier Detect
DB0-DB7	Data Bus
V_{DD}	Positive Power Supply (+5.0 volts)
V_{SS}	Internal Logic Ground

Pin Configuration



Block Diagram



PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} + 0.3V
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-55° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum ratings.

NOTES:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage (Except XTAL1)	V_{IH}	2.0	V_{DD} + 0.3	V
Input High Voltage (XTAL1 only)	V_{IHX}	3.1		V
Input Low Voltage (Except XTAL1)	V_{IL}	-0.3	0.8	V
Input Low Voltage (XTAL1 only)	V_{ILX}		1.9	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins	I_{IN}		±1.0	μA
Three-State Leakage Current, (V_{IN} = 0.4 to 2.4V)	I_{TSI}		±10.0	μA
Output Low Voltage (I_{OL} = 3.2mA)	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 μA)	V_{OH}	2.4		V
Supply Current (No Loads) f = 1 MHz f = 2 MHz f = 3 MHz f = 4 MHz	I_{DD} I_{DD} I_{DD} I_{DD}		2.0 4.0 6.0 8.0	mA mA mA mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz) Standby (Static)	 PD PDSB		 11.0 300	 mW μW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40° C to +85° C

		G65SC51-1		G65SC51-2		G65SC51-3		G65SC51-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	470	—	240	—	160	—	120	—	nS
Phase 2 Pulse Width Low	t_{PWL}	470	—	240	—	160	—	120	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing										
Select, R/$\overline{W}$ Setup	t_{ACR}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	190	—	130	—	90	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Write Timing										
Select R/$\overline{W}$ Setup	t_{ACW}	160	—	90	—	65	—	45	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS

AC Characteristics—Transmit/Receive Timing: V_{DD} = 5.0V ± 10%, V_{SS} = OV, T_A = -40°C to +85°C

		G65SC51-1		G65SC51-2		G65SC51-3		G65SC51-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Transmit/Receive Clock Cycle Time (1)	tCCY	400	—	400	—	400	—	400	—	nS
Transmit/Receive Clock High Time	tCH	175	—	175	—	175	—	175	—	nS
Transmit/Receive Clock Low Time	tCL	175	—	175	—	175	—	175	—	nS
XTAL 1 to TxD Propagation Delay	tDD	—	500	—	500	—	330	—	250	nS
Propagation Delay ($\overline{RTS}$, $\overline{DTR}$)	tDLY	—	500	—	500	—	330	—	250	nS
$\overline{IRQ}$ Propagation Delay (Clear) (2)	tIRQ	—	500	—	500	—	500	—	500	nS

1. The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times t_{CCY}}$
2. Propagation Delay is a function of external RC time constant.

Timing Diagrams

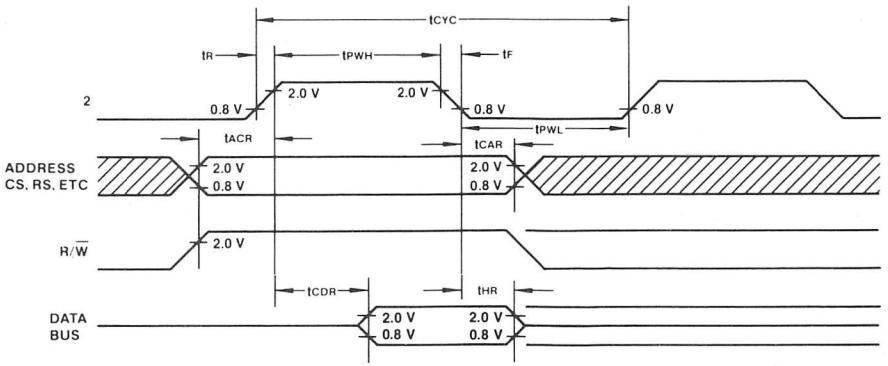


Figure 1. Read Timing

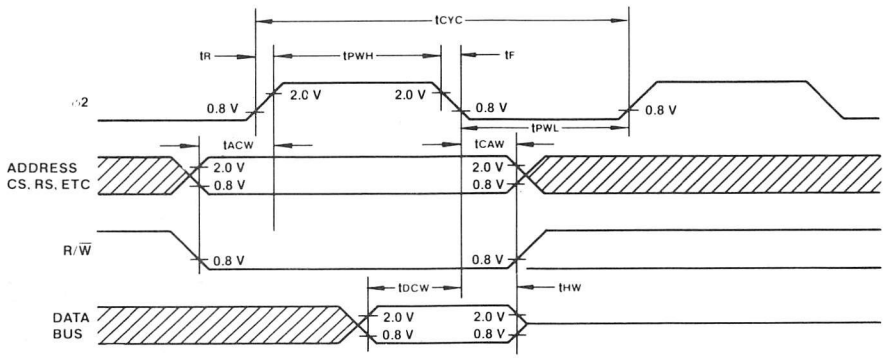
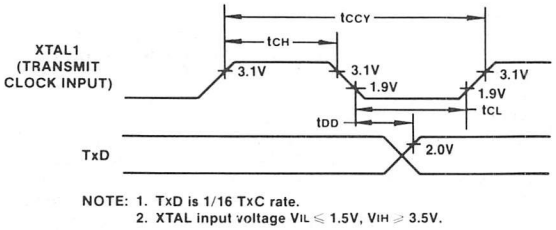


Figure 2. Write Timing

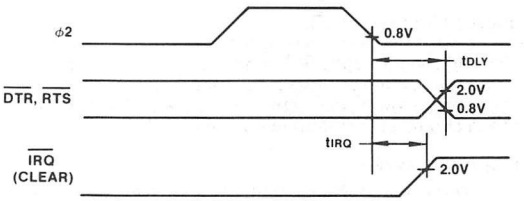
NOTE: Voltage levels shown are $V_{IL} \leq 0.4V$, $V_{IH} \geq 2.4V$.

Timing Diagrams (Continued)



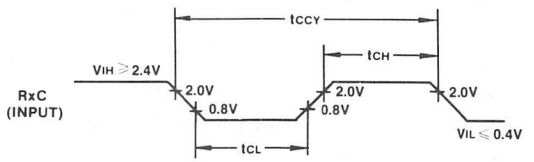
NOTE: 1. TxD is 1/16 TxC rate.
2. XTAL input voltage $V_{IL} \leq 1.5V$, $V_{IH} \geq 3.5V$.

Figure 3. Transmit Timing with External Clock



NOTE: 1. Voltage levels shown are $V_{IL} \leq 0.4V$, $V_{IH} \geq 2.4V$.

Figure 4. Interrupt and Output Timing



NOTE: 1. RxD rate is 1/16 RxC rate.
2. Voltage levels shown are $V_{IL} \leq 0.4V$, $V_{IH} \geq 2.4V$.

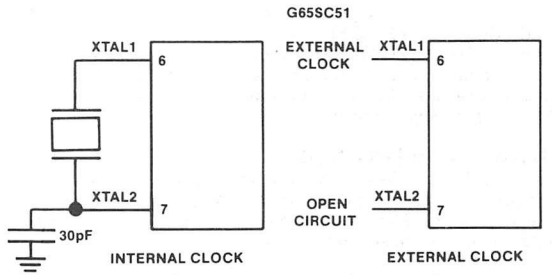
Figure 5. Receive External Clock Timing

Test and Crystal Specifications

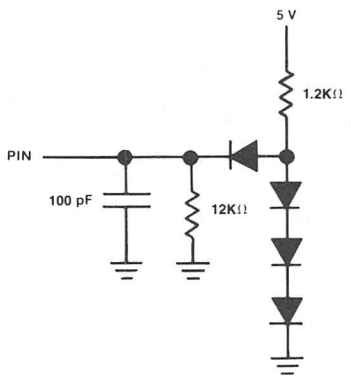
1. Temperature stability ± 0.01% (-40°C to +85°C)
2. Characteristics at 25°C ± 2°C

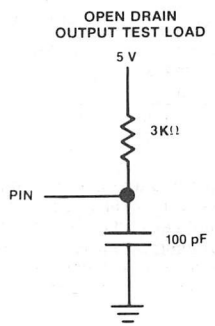
a.	Frequency (MHz)	1.8432
b.	Frequency tolerance (±%)	0.02
c.	Resonance mode	Series
d.	Equivalent resistance (ohm)	400 max.
e.	Drive level (mW)	2
f.	Shunt capacitance (pF)	7 max.
g.	Oscillation mode	Fundamental

Clock Generation



Test Load





Signal Description (Microprocessor Interface)

Reset ($\overline{RES}$)
Reset clears all internal registers during system initialization.

Interrupt Request ($\overline{IRQ}$)
The Interrupt Request ($\overline{IRQ}$) output signal is generated by the Interrupt Control Logic. $\overline{IRQ}$ is normally held to a high level and goes low when an interrupt occurs. $\overline{IRQ}$ is an open-drain output, thus allowing the $\overline{IRQ}$ signal to be wire-ORed to a common microprocessor Interrupt input line.

Read/Write (R/$\overline{W}$)
The R/$\overline{W}$ signal is generated by the microprocessor and is used to control the transfer of data between the G65SC51 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic 1) and the chip is selected, data is transferred from the G65SC51 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the G65SC51 (Write operation).

Input Clock ($\phi 2$)
The $\phi 2$ clock is used to trigger all data transfers between the microprocessor and the G65SC51.

Data Bus (DB0-DB7)
The eight bidirectional Data Bus lines are used to transfer data between the G65SC51 and the microprocessor. During a Read operation, data is transferred from the G65SC51 to the microprocessor. During a Write operation, the Data Bus lines serve as high impedance inputs over which data is transferred from the microprocessor to the G65SC51. The Data Bus lines are in the high impedance state when the G65SC51 is unselected.

Chip Select (CS0, $\overline{CS1}$)
The two Chip Select lines are normally connected to the processor address lines either directly or through decoders. To access a selected G65SC51, CS0 must be high (Logic 1) and $\overline{CS1}$ must be low (Logic 0).

Register Select (RS0, RS1)
The two Register Select lines are normally connected to the processor address lines. This allows the processor to select the various G65SC51 internal registers. Refer to Table 1 for internal register select coding.

Table 1. Register Select Coding

RS1	RS0	Write	Read
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

Note that only the Command and Control Registers can be accessed during both Read and Write operations. Programmed Reset operation does not cause data transfer, but is used to clear (reset) all G65SC51 internal registers. Programmed Reset is used in a slightly different way as compared to the hardware Reset ($\overline{RES}$). These differences are described under each individual register description.

Signal Description (Communications Interface)

Transmit Data (TxD)
TxD is an output line used to transfer NRZ (Non-Return-to-Zero) data to a modem. The LSB (Least Significant Bit) of the Transmit Data Register is the first data bit transmitted. The rate of data transmission (baud rate) is determined by the selected baud rate.

Receive Data (RxD)
RxD is an input line used to receive NRZ input data from a modem. The LSB is always the first data bit received. Received data will always be at the G65SC51's internally programmed baud rate or the baud rate of an externally generated receiver clock. The baud rate is a selection which is made by programming the Control Register. See Figure 6, Control Register Format.

Receive Clock (RxC)
RxC serves as a bidirectional "pin" which can be either the 16X Clock Input or the receiver 16X Clock Output. The 16X Clock Output mode results if the internal baud rate generator is selected for External Receiver Clocking. See Figure 6, Control Register Format.

Request to Send ($\overline{RTS}$)
$\overline{RTS}$ is an output line used as a control function to the modem. The state of $\overline{RTS}$ is determined by the contents of the Command Register. Refer to Figure 7, Command Register Format.

Data Carrier Detect ($\overline{DCD}$)
$\overline{DCD}$ is an input line used to indicate carrier-detect output status from the modem. A low level indicates the modem carrier signal is present, and a high level indicates the modem carrier signal is not present. $\overline{DSR}$ is a high impedance input and must not be used as a no-connect. That is, if unused, this pin must be driven high or low, but not switched.

NOTE: If Command Register Bit 0 is a high (Logic 1) and a change of state on $\overline{DCD}$ occurs, $\overline{IRQ}$ will be set, and the Status Register Bit 5 will reflect the new level. The state of $\overline{DCD}$ does not affect Transmitter operation, but must be low (Logic 0) for the Receiver to operate.

Clear to Send ($\overline{CTS}$)
$\overline{CTS}$ is an input used to control Transmitter operation. The Transmitter is enabled when $\overline{CTS}$ is low (Logic 0), and is automatically disabled when $\overline{CTS}$ is high (Logic 1).

Data Terminal Ready ($\overline{DTR}$)
$\overline{DTR}$ is an output line used to indicate G65SC51 status to the modem, and is controlled by the processor via Bit 0 of the Command Register. $\overline{DTR}$ low (Logic 0) indicates the G65SC51 is enabled, while $\overline{DTR}$ high (Logic 1) indicates the device is disabled.

Data Set Ready ($\overline{DSR}$)
$\overline{DSR}$ is an input line used to indicate modem status to the G65SC51. $\overline{DSR}$ low (Logic 0) indicates the modem is "ready", while a high (Logic 1) indicates the modem is in a "not ready" state. Like $\overline{DCD}$, $\overline{DSR}$ is a high impedance input and must not be used as a no-connect. If unused, this line must be driven either high or low, but not switched.

NOTE: If Command Register Bit 0 is high (Logic 1) and a change of state on $\overline{DSR}$ occurs, $\overline{IRQ}$ will be set, and Status Register Bit 6 will reflect the new level. The state of $\overline{DSR}$ does not affect either Transmitter or Receiver operation.

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 Stop Bit
1 = 2 Stop Bits
1 Stop Bit if Word Length
= 8 Bits and Parity*
1½ Stop Bits if Word Length
= 5 Bits and No Parity

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = External Receiver Clock
1 = Baud Rate Generator

*This allows for 9-bit transmission (8 data bits plus parity).

BAUD RATE GENERATOR

3	2	1	0	
0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	—	—	—	—	—	—	—	—

Figure 6. Control Register Format

COMMAND REGISTER

7	6	5	4	3	2	1	0

PARITY CHECK CONTROLS

BIT 7	BIT 6	BIT 5	OPERATION
—	—	0	Parity Disabled—No Parity Bit Generated—No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

NORMAL/ECHO MODE FOR RECEIVER

0 = Normal
1 = Echo (Bits 2 and 3 must be "0")

DATA TERMINAL READY

0 = Disable Receiver and All Interrupts ($\overline{DTR}$ high)
1 = Enable Receiver and All Interrupts ($\overline{DTR}$ low)

RECEIVER INTERRUPT ENABLE

0 = $\overline{IRQ}$ Interrupt Enabled from Bit 3 of Status Register
1 = $\overline{IRQ}$ Interrupt Disabled

TRANSMITTER CONTROLS

BIT 3	BIT 2	TRANSMIT INTERRUPT	$\overline{RTS}$ LEVEL	TRANSMITTER
0	0	Disabled	High	Off
0	1	Enabled	Low	On
1	0	Disabled	Low	On
1	1	Disabled	Low	Transmit BRK*

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	—	—	—	0	0	0	0	0

Figure 7. Command Register Format

External Crystal Pins (XTAL1, XTAL2)

These two crystal pins are normally used to connect an external crystal (1.8432 MHz) to the internal baud rate generator. This crystal is used to derive the full range of available baud rates. For nonstandard baud rates, an externally generated clock may be connected to the XTAL1 pin. In this case, the XTAL2 pin must float.

Internal Functions

Figure 8 shows the Transmitter/Receiver sections of the G65SC51. Bits 0-3 of the Control Register are used to select the "divisor" which in turn generates the selected baud rate for the Transmitter. Should the Receiver clock be using the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the G65SC51.

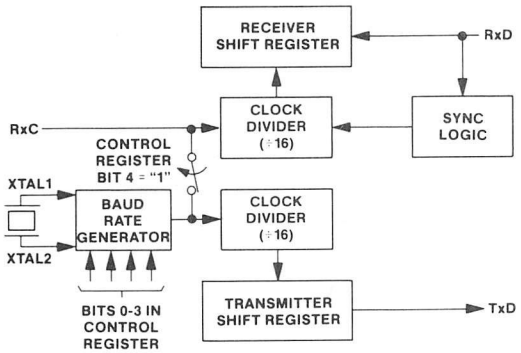


Figure 8. Transmitter/Receiver Clock Circuits

Control Register

The Control Register selects the various operating modes for the G65SC51. Note that the Baud Rate Generator, word length, number of stop bits and the Receiver Clock Source are all controlled by the Control Register. Refer to Figure 6, Control Register Format, for detailed operation and programming information.

Command Register

The Command Register is used to control Transmit/Receive functions. Refer to Figure 7, Command Register Format, for detailed operation and programming information.

Transmit and Receive Data Registers

The Transmit and Receive Data Registers are used as temporary data storage within the G65SC51. Transmit Data Register characteristics are as follows:

- Bit 0 is always the leading bit during any transmission.
- Unused data bits are always the high-order bits in the data word. These unused high-order bits are "don't care" during data transmission.

Receive Register characteristics are as follows:

- Bit 0 is always the leading bit received.
- Unused data bits are always the high-order bits and are "zeros" for the receiver.
- Parity bits are not stored in the Receive Register. The parity bits are stripped off after being used for external parity checking. Therefore, received data in the Receive Data Register will have all parity and unused high-order bits as "zeros."

Figure 9 shows an example of a transmitted or received data word which contains eight data bits, a parity bit and a single stop bit.

Status Register

The Status Register indicates to the processor the status of various G65SC51 functions. Refer to Figure 10 for detailed Status Register operation and programming information.

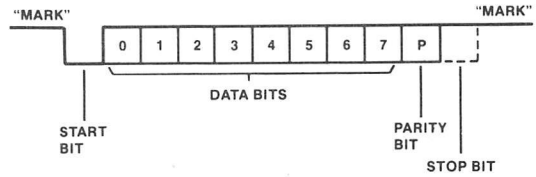


Figure 9. Serial Data Stream Example

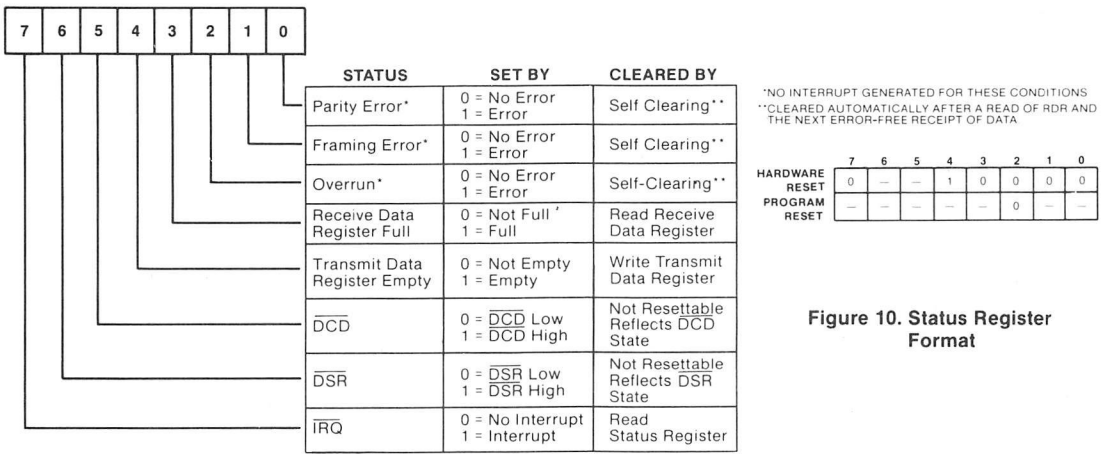


Figure 10. Status Register Format

G65SC150

Microcircuits

CMOS Communications Terminal Unit (Telecommunication Microcomputer)

Features

- Generates signals compatible with switched telephone networks or packet switched data networks
- Provides Dial Pulse (DP), Dual Tone Multi-Frequency (DTMF), and 0-600 baud modem signaling capabilities
- Low power mode (300 μA) enables telephone line-powered operation
- External microprocessor address and data bus facilitates memory and I/O expansion
- On-chip memory: 2K bytes ROM
  64 bytes RAM
- Standard DTMF and modem frequencies can be generated which are accurate to $\pm$1.0% with a 3.58 MHz crystal
- Two sine wave generators
- 6800 and 6500 bus compatibility
- Utilizes G65SC00 microprocessor as CPU
- 27 TTL compatible I/O lines
- Bus expandable to address 65K bytes of external memory
- Single +5 volt power supply
- Available in 68-pin chip carriers

General Description

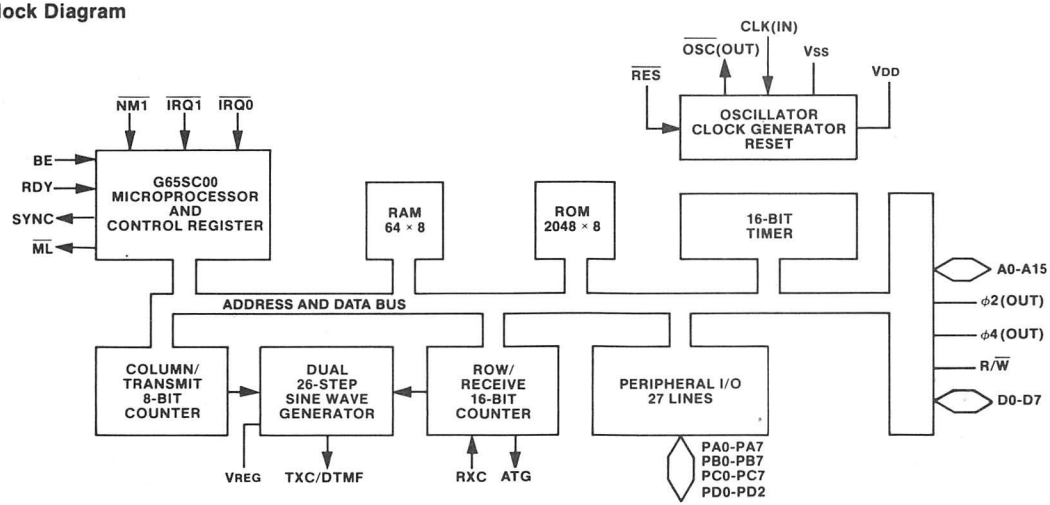
The GTE G65SC150 Communications Terminal Unit (CTU) is a single chip telecommunications microcomputer manufactured using state-of-the-art silicon gate CMOS process technology, which is optimized for telephone line signaling and data transmission applications. A functional block diagram is shown which illustrates the major system functions that are included on the integrated circuit.

The CTU uses the GTE G65SC00 8-bit microprocessor which executes the complete G65SC00 series instruction set. With 2K bytes of ROM and 64 bytes of RAM, the CTU operates as a single-chip microcomputer.

The internal bus interconnects all microcomputer functions. The address and data bus buffers permit expansion of ROM, RAM and memory mapped I/O using the full 65K addressing space of the microprocessor. A peripheral mode is available for use with multiprocessor systems. A test and prototyping mode switches internal ROM addresses to external access. An on-chip oscillator may be driven by an external clock source.

The telecommunications interface circuitry consists of a timer, row/receive counter, column/transmit counter and dual sine wave generators. In addition, 27 general purpose I/O lines can be used for keyboard, telephone Dial Pulse (DP) signaling, phone line control, and other peripheral devices.

Block Diagram



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +8.5	V
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_S	-65 to +150	°C
Regulated Voltage	V_{REG}	-0.3 to V_{DD} + 0.3	V

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

DC Characteristics: All signals except TXC/DTMF, V_{DD} = 5.0V ± 10% unless otherwise stated, T_A = -40°C to +85°C

Parameter	Symbol	Min	Max	Units
Input High Voltage	V_{IH}			
CLK (IN)		2.4	V_{DD} + 0.3	V
All Other Inputs		2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}			
CLK (IN)		-0.3	0.4	V
All Other Inputs		-0.3	0.8	V
Output High Voltage	V_{OH}	2.4		V
Address, Data, R/$\overline{W}$ (I_{OH} = -100μA)				
Peripheral I/O				
Option B (I_{OH} = -10μA)				
Option C (I_{OH} = -200μA)				
Option D (I_{OH} = -1.0mA)				
Output Low Voltage (I_{OL} = 3.2mA)	V_{OL}		0.4	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), No Pullup Option,	I_{IN}			
$\overline{RES}$, NMI, $\overline{IRQ0}$, $\overline{IRQ1}$, RDY, BE, CLK(IN)			±1.0	μA
Three-State Leakage Current (V_{IN} = 0.4 to 2.4V),	I_{TSI}			
I/O Ports, Address, Data, R/$\overline{W}$			±10.0	μA
Input Pullup Current (Inputs with Pullup Option),	I_{PLP}			
$\overline{RES}$, NMI, $\overline{IRQ0}$, $\overline{IRQ1}$, RDY, BE		-20.0		μA
Input High Current (V_{IH} = 2.4V)	I_{IH}			
Option A		0		μA
Option B		-10		μA
Option C		-200		μA
Input Low Current (V_{OL} = 0.4V)	I_{IL}			
Option B			-100	μA
Option C			-2.4	mA
Output Source Current (V_{OH} = 1.5V)	I_{OH}			
I/O Ports Option D		3.0		mA
Supply Current (V_{DD} = 4.5V)	I_{DD}			
ϕ2 = 2 MHz			8.6	mA
ϕ2 = 1 MHz			4.3	mA
ϕ2 = 10 KHz (Control Register TSC Bit = 0)			300	μA
Sine Wave Generator (V_{REG} = 2.75V)	I_{REG}		1.7	mA
Capacitance (V_{IN} = 0V, T_A = 25°C, F = 1 MHz)				
A0-A15, R/$\overline{W}$, Data (Off State)	C_{TS}		15	pF
All Other Signals	C_{IN}		10	pF

AC Characteristics: V_{DD} = 5.0 V ±10%, T_A = -40°C to +85°C

		1 MHz		2 MHz		Units
Parameter	Symbol	Min	Max	Min	Max	
Delay Time, CLK(IN) to ϕ2(OUT)	t_{DCLK}	—	100	—	100	nS
Delay Time, $\overline{OSC}$(OUT) to ϕ2(OUT)	t_{DOSC}	—	75	—	75	nS
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	μS
Clock Pulse Width Low	$t_{PW(\phi 2L)}$	470	—	240	—	nS
Clock Pulse Width High	$t_{PW(\phi 2H)}$	470	—	240	—	nS

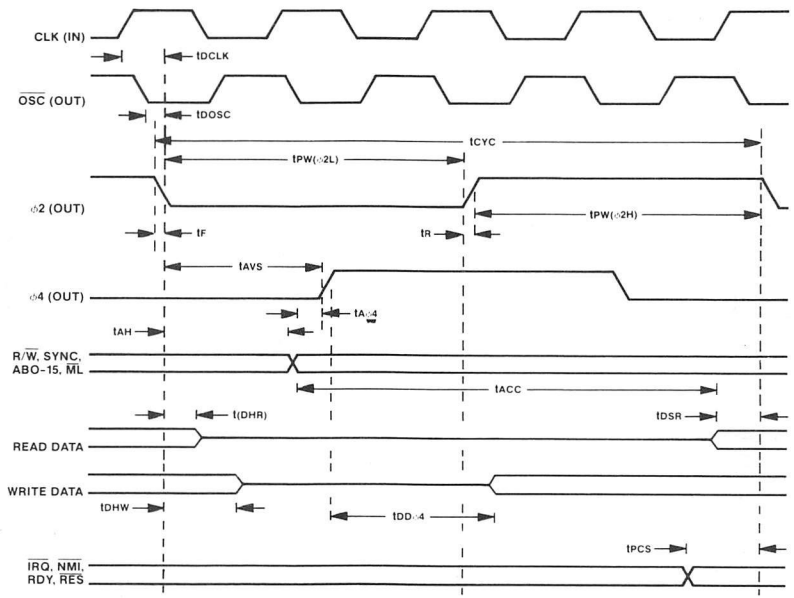
AC Characteristics: V_{DD} = 5.0 V ±10%, T_A = -40° C to +85° C (continued)

		1 MHz		2 MHz		Units
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	
Fall Time, Rise Time	t_F, t_R	—	25	—	25	nS
Delay Time, ϕ2(OUT) to ϕ4(OUT)	t_{AVS}	—	250	—	125	nS
Address Valid to ϕ4(OUT)	$t_{A\phi4}$	50	—	25	—	nS
Address Hold Time	t_{AH}	30	—	20	—	nS
Access Time	t_{ACC}	695	—	340	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	nS
Read Data Setup Time	t_{DSR}	80	—	40	—	nS
Write Data Hold Time	t_{DHW}	30	—	30	—	nS
Write Data Delay Time	$t_{DD\phi4}$	—	200	—	110	nS
Processor Control Setup Time	t_{PCS}	100	—	50	—	nS

AC Characteristics, TXC/DTMF Output: V_{REG} = 2.75, R_L = 10KΩ

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Row Tone	V_{OR}	196	220	247	mVrms	
Column and Transmit Tone	V_{OC}	267	300	337	mVrms	
Pre-emphasis, DTMF High Group	PE_{HB}	2.4	2.7	3.0	dB	
DTMF Total Distortion	DIST			-25	dB	Total out-of-band power relative to sum of Row and Column fundamental power.
DTMF Single Frequency Distortion	DISS			-33	dB	0 to 3.4 KHz band. (Any spectral component)
Idle Noise	V_{IDLE}			-80	dB	

Timing Diagram



Notes: 1. Load = 100 pF.
2. Voltage levels shown are $V_L < 0.4$ V, $V_H > 2.4$V, unless otherwise specified.
3. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

Characteristic Curve

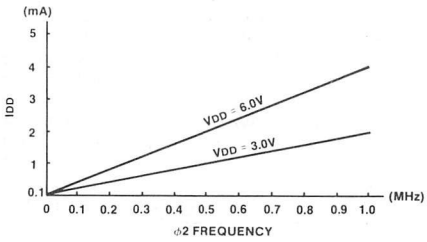


Figure 1. Typical Supply Current (I_{DD}) Versus $\phi 2$ Frequency — Microprocessor Only

Test Circuits

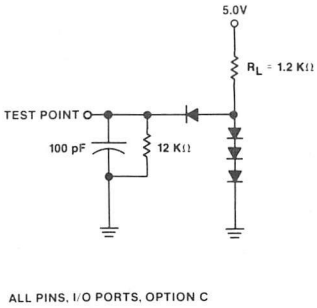


Figure 2(a). Test Load

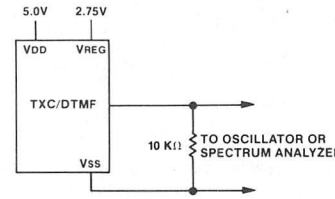


Figure 2(b). Audio Test Load

Signal Description

Microprocessor Signals

Interrupt Request ($\overline{IRQ0}$, $\overline{IRQ1}$)—These TTL compatible signals (bidirectional, active low—two lines) request that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ signals are sampled during $\phi 2$(OUT) operation. If the interrupt flag in the status register is zero, the current instruction is completed and the interrupt sequence begins when $\phi 2$(OUT) goes low. The program counter and processor status register are stored in the stack. The interrupt flag is set so that no other maskable interrupts occur. The program counter is loaded with the interrupt vector thereby transferring program control to an interrupt routine. Interrupt and vector addresses are shown in Figure 3. Note that this is a level sensitive input. As a result, another interrupt will occur as soon as the interrupt flag is cleared if $\overline{IRQ}$ remains low. No interrupt will occur when the interrupt flag is cleared and $\overline{IRQ}$ is high but was low prior to clearing the flag. Also note that these are bidirectional signals which are "wire-ORed" with both internal and external interrupt sources. The signals are decoded to form three separate interrupt vector addresses as shown in Figure 3. Since these signals are "wire-ORed" for both internal and external interrupts, the generation of internal interrupts will cause high and low logic level swings at the $\overline{IRQ}$ pins. As outputs, these signals serve to indicate that a specific internal interrupt has occurred. This being the case, caution should be used to prevent connecting these signals to external circuitry which could falsely respond to an internal interrupt condition.

Vector Address	Description	Comment
FFFE, F	Break	Software Interrupt
FFF8, 9	Row/Receive Counter	Pulls $\overline{IRQ0}$ and $\overline{IRQ1}$ Low
FFFA, B	External	$\overline{IRQ1}$
FFFC, D	Timer/Counter	Pulls $\overline{IRQ0}$ Low
FFEE, F	Reset	$\overline{RES}$
FFEC, D	Non-Maskable	$\overline{NMI}$

Figure 3. Interrupt and Vector Addresses

Non-Maskable Interrupt ($\overline{NMI}$)—A negative-going edge on this input, active low signal unconditionally starts a non-maskable interrupt sequence within the microprocessor. The $\overline{NMI}$ signal is sampled during $\phi 2$(OUT) operation. The current instruction is completed and the interrupt sequence begins when $\phi 2$(OUT) goes low. The program counter and processor status register are stored in the stack. The interrupt flag is set so that no maskable interrupts occur. The program counter is loaded with the interrupt vector from locations FFEC (low byte) and FFED (high byte), thereby transferring program control to the non-maskable interrupt routine. Note that this is an edge-sensitive input. As a result, another interrupt will occur if there is another negative-going transition and the program has not returned from a previous interrupt. No interrupt will occur if $\overline{NMI}$ is low and a negative-going edge has not occured since the last non-maskable interrupt.

Bus Enable (BE)—When this input, active high signal is high, (R/$\overline{W}$) is an output, indicating internal control of read and write operations. When BE is low, the address/data bus is reversed allowing access to internal ROM, RAM and I/O from an external device. R/$\overline{W}$ becomes an input, controlling the internal read and write operations. The $\phi 2$(OUT) and $\phi 4$(OUT) outputs are used for system timing. BE is also used to switch the computer to the test and prototype mode. During processor initialization, BE is high before Reset ($\overline{RES}$) goes high for normal operation. For test and prototype purposes, the internal ROM is disabled, allowing use of external memory at addresses F800 through FFFF. To disable internal ROM, BE is held low before $\overline{RES}$ goes high.

Synchronize (SYNC)—This output, active high signal identifies microprocessor op code fetches. Synchronize goes high after the start of an op code fetch cycle and stays high for the remainder of that cycle.

Ready (RDY)—This input, active high signal provides a single cycle stepping capability and allows operation with slow memory devices for read or write cycles. If this signal is low when $\phi 2$(OUT) is low, the processor will stop when $\phi 2$(OUT) goes high. The address and data lines remain at their current state. When RDY goes high, the processor resumes operation.

Memory Lock ($\overline{ML}$)—This signal is an active low output and, in a multiprocessor system, $\overline{ML}$ indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB and TSB memory referencing instructions. This signal is low for two cycles: the modify and write cycles, and is available as a metal mask option in place of PD2.

Bus Signals

Address Bus (A0-A15)

Output (BE = 1)
A0-A15 forms a three-state, 16-bit, input/output, active high address bus (65,536 locations) for memory and I/O exchanges on the data bus. If the TSC control register bit is set, these lines are pulled to the low state by a high resistance device.

Input (BE = 0)
These lines drive the internal address decoder to select internal ROM, RAM or I/O for external read and write cycles.

Clocks (ϕ2(OUT) and ϕ4(OUT))—These output, active high signals (2 lines) provide timing for external bus read and write operations. ϕ4(OUT) is a metal mask option in place of SYNC.

Data Bus (D0-D7)—D0-D7 constitute an 8-bit bidirectional active high, three-state data bus, used for data exchanges with memory and I/O. If the TSC control register bit is set, these lines are pulled to the low state by a high resistance device.

Read/Write (R/$\overline{W}$)

Output (BE = 1)
This output, active low signal is normally in the high state indicating that the CPU is reading data from memory or I/O. In the low state the data bus has valid data from the CPU to be stored at the addressed memory or I/O location. If the TSC control register bit is set, this line is pulled to ground by a high resistance device.

Input (BE = 0)
In systems where this part is used as a peripheral controller, R/$\overline{W}$ is an input, active low signal which controls the output data buffers. When R/$\overline{W}$ is high, the buffers are active and internal data is read by the external microprocessor.

Telecommunications Signals

Transmit Carrier and Dual Tone Multifrequency (TXC/DTMF)—This output signal is connected to the output of an operational amplifier which mixes the two sine wave generator outputs. In a telecommunication application, these signals may be the row and column tones used in DTMF signaling. The level of the dual-tone output is the sum of the levels of a single row and single column output. The modem Transmit Carrier (TXC) is generated by the column/transmit counter and sine wave generator. This signal level is controlled by VREG voltage reference supply and is gated by CC0, CC1, and CC2 control register bits.

Audible Tone Generator (ATG)—This output signal is derived from the carry output of the row/receive counter. The square wave output is gated by the ATG control register bit.

Receive Carrier (RXC)—When the row/receive counter is in the pulse width timer mode, this input signal generates a maskable interrupt after both positive and negative transitions. At the same time, the counter contents are transferred to the row/receive register. In this way, the time between transitions can be measured by an interrupt servicing program.

Peripheral Signals

There are 27 peripheral input/output lines: PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD2. Four memory addressable registers are associated with these signals. Depending upon the mask option chosen, the output can source either 0, 10 or 400 μA at V_{OH} = 2.4 volts. The higher sourcing current may be used to directly drive the base of an external NPN transistor having a grounded emitter, or in a Darlington configuration.

Miscellaneous Signals

Reset ($\overline{RES}$)—A positive transition of this input, active low signal causes an initialization sequence to begin. Reset must be held low for at least two clock cycles after VDD reaches operating voltage from a power down condition. After this time R/$\overline{W}$ is high. The I/O ports (PA, PB, PC and PD) are forced to the high state. All bits in the control register are set to zero. When a positive edge is detected, there is an initialization sequence lasting six clock cycles. The interrupt mask flag is set and the program counter is loaded with the restart vector from locations FFEE (low byte) and FFEF (high byte).

Clock In (CLK(IN))—The microcomputer contains an internal clock generator operating at four times the ϕ2 frequency. The frequency of these clocks is externally controlled by a crystal oscillator circuit as shown in Figure 4. The internal generator may also be controlled by an input signal from any external clock source.

Oscillator Out ($\overline{OSC}$(OUT))—An inverter whose input is CLK(IN) and output is $\overline{OSC}$(OUT) is connected between these two clock pins. This active low inverter has sufficient loop gain to provide oscillation using a crystal. Frequency deviation, usually less than 0.05%, will affect the tone output frequency. There is a bias resistor mask option between the two pins.

External ROM(EXTR)—Active high input during test and prototype mode selects external ROM. A low level at this input selects internal ROM only.

Regulated Supply Voltage (VREG)—The D-to-A resistor networks and summing amplifier are powered by a separate supply voltage. The TXC/DTMF output level is directly proportional to VREG.

Internal Logic Ground (VSS)—This connection is used for the power supply internal logic ground.

Positive Supply Voltage (VDD)—This connection serves as the positive power supply input. Reset ($\overline{RES}$) should be held low for at least two clock cycles after VDD reaches operating voltage from a power down condition.

Operating Modes

Normal Mode

In the normal mode, the internal microprocessor is operating and its memory map includes the internal 2K bytes of ROM, 64 bytes of RAM, four general purpose I/O registers, one control register and five timer/counter registers. The three-state control bit in the control register determines whether the external bus is active, thus allowing access to the full 65K addressing space.

Test and Prototype Mode

This mode allows use of external memory at addresses F800 through FFFF, disabling the internal ROM. To enable this mode, the Bus Enable (BE) signal is held low before Reset goes high. Once Reset is high, all memory references in the range F800 to FFFF will access external data. When using this mode, a program may be written using external memory for the prototype system. After the program is debugged and tested, it can be committed to internal ROM. PD1 becomes a control signal to select internal or external ROM.

Peripheral Mode

In the peripheral mode, internal ROM, RAM and I/O may be accessed from an external device. This mode is useful when the G65SC150 is used as a peripheral device in a microprocessor system. To enable this mode, the Bus Enable (BE) signal is held low. This stops the microprocessor and reverses the address and data buses. Read/Write becomes an input, thus allowing external control of internal read and write operations.

Low Power Mode

Since power consumption in CMOS circuits is directly related to operating frequency, this mode allows operation at greatly reduced power by reducing the microprocessor clock frequency. This mode is enabled by storing a value in the 16-bit Timer register and then setting the ϕ2 mode bit in the control register. The timer counter becomes a programmable clock divider. To further reduce power, the external address and data bus may be disabled by clearing the three-state control bit in the control register.

Functional Description

G65SC150 Microprocessor Unit

For a detailed functional and software programming description of the microprocessor, refer to the data sheet for the G65SCXXX family of 8-bit microprocessors. Figure 17 (page 11) illustrates a microprocessor programming model, while a complete listing of operational codes, execution times and memory requirements is provided in Figure 19 (page 12). A brief functional description of the G65SCXXX microprocessor is as follows:

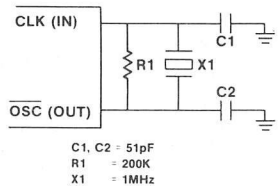


Figure 4. Crystal Circuit for Internal Oscillator

Timing Control—The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each $\phi 1$ clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter—The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode—Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)—All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator—The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers—There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer—The stack pointer is an 8-bit register used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts.

Processor Status Register—The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

Oscillator/Clock Generator

A functional block diagram of the oscillator/clock generator circuitry is shown in Figure 5. The circuits are described in the following three paragraphs:

Oscillator—The clock oscillator accommodates a crystal of up to 8 MHz. CLK(IN) and $\overline{OSC}$(OUT) are TTL compatible. An oscillator bias resistor between these pads is a mask option. With the resistor connected, the circuit requires only an external crystal. For an external oscillator, the resistor is disconnected to eliminate static current drain in low-power system.

Microcomputer Clock—In the maximum frequency mode ($\phi 2$ mode = 0) the oscillator frequency divided-by-four provides the microcomputer bus timing signals $\phi 2$(OUT) and $\phi 4$(OUT). The quadrature clock generator delays the $\phi 2$(OUT) signal by one oscillator period. The low-power mode ($\phi 2$ mode = 1) uses the timer counter as a programmable $\phi 2$(OUT) clock divider.

Timer and Counter Clock—A mask option determines whether a divide-by-two circuit is inserted in the counter and timer clocks. With the divider, a higher frequency crystal (8 MHz maximum) may be used to increase the microprocessor speed while the counter and timer speeds remain unchanged. The modem function is enabled by bits in the control register (CC2, CC1, CC0 = 101).

Random Access Memory (RAM)

The 64-byte memory resides in two ranges in the microcomputer address map. Address bit A8 is not decoded for the RAM, allowing addressing at both 01C0-01FF and 00C0-00EF (00F0-00FF is reserved for the telecommunication register set). In a typical program, the RAM would be partitioned for both stack addressing (01XX) and zero page addressing (00XX).

Read Only Memory (ROM)

The 2048-byte ROM is used for program and constant data storage in the microcomputer system. The ROM occupies addresses F800-FFFF in the microcomputer address map.

Control Register

The on-chip timer and counters with their associated interrupts are configured by setting bits in the control register at address 00F7 as shown in Figure 6.

A functional description of the various control register bits is contained in the following paragraphs:

Communication Mode Select—CC2, bit 2; CC1, bit 1; CC0, bit 0—These bits select one of eight operating modes for the row/receive and column/transmit registers and counters.

000—Idle Mode
Both the Row/Receive Counter (RRC) and Row/Receiver Register (RRR) are inactive, with no interrupt generated and no tone output.

001—Interval Timer Mode
In this mode, the row/receive counter is configured as an additional interval counter based on the contents of the row/receive register.

010—Pulse Width Timer Mode
In this mode, the row/receive counter is configured as a pulse width interval timer...measuring the period between transitions of the receive carrier input.

011—Single Tone Row/Tone Generator Mode
As determined by the ATG bit, a square wave is generated at the Audible Tone Generator (ATG), or a sine wave is generated which appears at the TXC/DTMF output.

100—Single Tone Column Mode
In this mode, a single frequency is generated at the TXC/DTMF output.

101—Modem
This mode is a concurrent application of the pulse width timer mode and the single tone column mode.

110—Modem—Divide-by-Two Prescaler Mode
This mode allows transmit and receive, plus low frequency transmit carrier generation.

111—Dual Tone Multifrequency Mode
This mode allows the generation of standard DTMF signaling tones.

Phase 2 Mode Select—Phase 2, Bit 3—This mode controls the frequency at which the microprocessor oscillator operates. Refer to Figure 5, Clock Functional Block Diagram.

0—Maximum Frequency Mode
The frequency at CLK (IN) divided by four is the microprocessor clock.

1—Low Power Mode
The timer overflow signal is the microprocessor clock. The timer clock input is the frequency CLK(IN) divided by either four or eight depending on a mask option in the clock circuitry. The timer divide ratio is the contents of the timer register plus two.

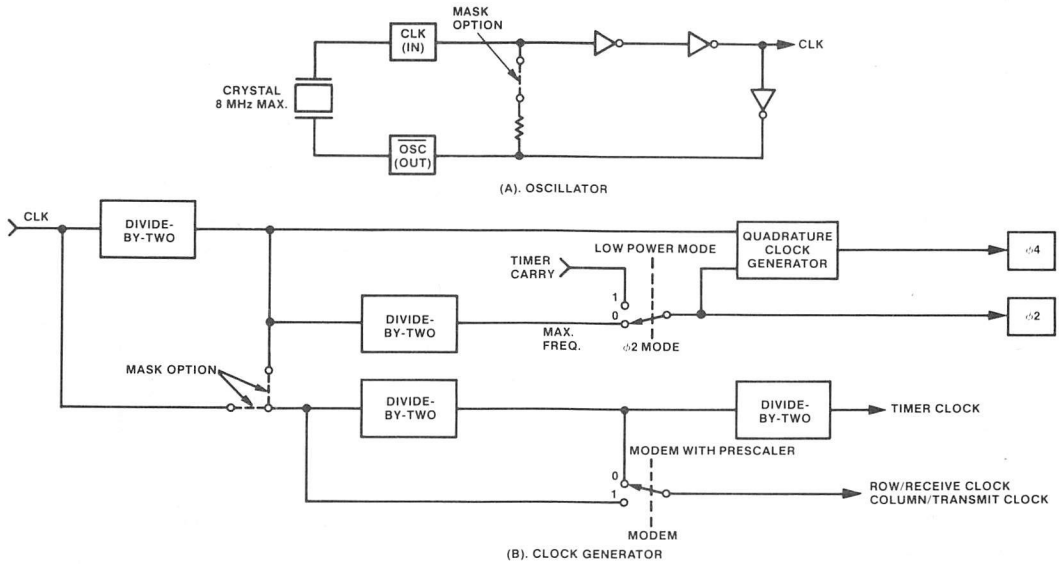


Figure 5. Clock Functional Block Diagram

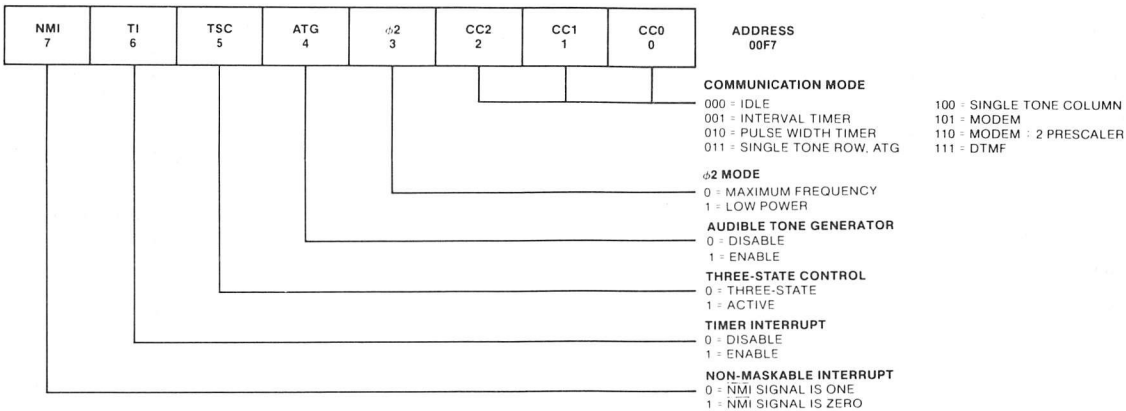


Figure 6. Control Register Functional Block Diagram

Audible Tone Generator Enable—ATG, Bit 4

0—Audible Tone Disabled

1—Audible Tone Enabled

Three-State Control Enable—TSC, Bit 5

0—Three-State
The external address and data buses and R/$\overline{W}$ are pulled to V_{SS} by a high resistance device. In a typical application TSC is set to zero when operating in low or back-up power condition. The bus is powered down and not driven externally.

1—Bus Active

Timer Interrupt Enable—TI, Bit 6

0—Timer Interrupt Disabled
The timer register value is transferred to the counter when changing to the enabled interrupt state.

1—Timer Interrupt Enabled

Non-Maskable Interrupt Input—$\overline{NMI}$, Bit 7

0—$\overline{NMI}$ Signal = One (No interrupt)

1—$\overline{NMI}$ Signal = Zero (Interrupt)
In a typical application this condition indicates low or back-up power system operation. The microprocessor program would monitor this condition to return to normal power operation.

Timer

The 16-bit free-running timer counter and register operates in one of two modes determined by timer interrupt signal and φ2 bits in the control register. Figure 7 illustrates the timer functional block diagram. With a 3.579545 MHz clock, the timer mode is capable of 1.1175 μS resolution. An interrupt is generated at intervals from 2.2349 μS to 73.234 mS. In the low power mode, the counter carry output becomes the microprocessor φ2(OUT) clock. Refer to Figure 18 (page 11), Microprocessor Clock Frequency and Timer Interval.

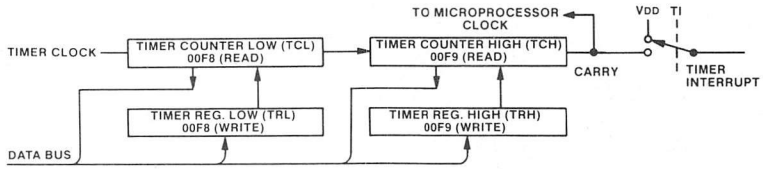


Figure 7. Timer Functional Block Diagram

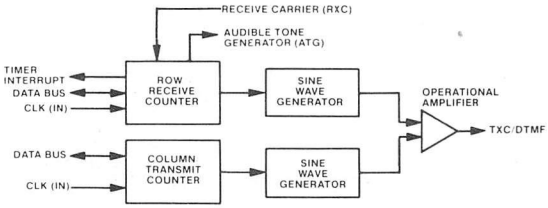


Figure 8. Frequency Detection/Generation Block Diagram

Timer Operation—The timer operating mode is enabled by setting the control register timer interrupt bit to one. The desired time interval is written in the 16-bit timer register (00F8,9). When the timer interrupt (TI) bit is set to one the timer carry interrupts the microprocessor; the counter decrements toward a zero value. When the counter generates a carry by counting past zero, the timer register is again transferred to the counter and interrupts the microprocessor if the interrupt bit in the status register is zero. A read operation will read the contents of the counter and reset the interrupt latch.

Low Power Operation—This mode is enabled by setting the control register $\phi 2$ mode bit to one. Since chip power consumption is directly related to operating frequency, power can be reduced by lowering the microprocessor clock frequency. The desired clock divide ratio is written in the 16-bit timer register at address 00F8 and 00F9. When the counter decrements from zero, the timer register is transferred to the counter. In this configuration, the counter carry output becomes the system $\phi 2$ clock (See Figure 5b).

Frequency Detection/Generation

The frequency detection/generation section of the G65SC150 contains the necessary circuitry to generate a wide range of sine waves, either singularly or in pairs. See Figure 8, Frequency Detection/Generation Block Diagram. In addition, a square wave may be generated as a separate frequency output. Furthermore, a frequency detection input (RXC) is provided for measurement or duplex communications. The row/receive counter and column/transmit counter operate independently or in conjunction with each other to perform the various communications modes as determined by bits CC0, CC1 and CC2 of the control register. The row/receive and column/transmit counters are programmable. Register values for typical applications are shown in Figure 16 (page 11).

Row/Receive Counter

The 16-bit Row/Receive Counter (RRC) and Row/Receive Register (RRR) (address 00F4, 5) operate as a tone generator, pulse width interval timer or interval timer as determined by CCX bits in the Control Register. Figure 9 illustrates the RRC/RRR functional block diagram for these three modes.

In the Idle Mode (CCX = 000), both the counter (RRC) and the register (RRR) are inactive, no interrupt is generated and there is no tone output. With the exception of the single tone column (CCX = 100), any change in CCX to any other state will cause the row/receive counter to be initialized with the current register value and the counter to begin counting.

In the Interval Timer Mode (CCX = 001), the row/receive counter serves as an additional interval timer. The counter interval is received from the row/receive register via the Data Bus. Upon generation of a carry, a timer interrupt is generated and the new contents of RRR is transferred to the counter (RRC). The counter continues counting and the process (cycle) continues until modified. In the interval timer mode, an interrupt is generated at intervals from 2.2349 microseconds to 73.234 milliseconds with a resolution of 1.1175 microseconds.

In the Pulse Width Timer Mode (CCX = 010), the row/receiver counter is used as a pulse width timer, measuring the period between Receive Carrier (RXC) transitions. In this case, both positive and negative transitions of the RXC input cause an interrupt and transfers the counter value to the row/receive register where it may be read by the microprocessor. Following each transfer, the counter continues counting. In telecommunications applications, receive carrier detect and dial tone detect functions can be accomplished.

In the Single Tone Row/Tone Generator mode (CCX = 011), a row/receive counter overflow reloads the counter from the row/receive register. No interrupt is generated. The overflow (carry signal) goes to either the ATG divide-by-two circuit, or to the sine wave generator and TXC/DTMF depending on the state of the ATG control register bit. With a clock frequency of 3.579545 MHz, a square wave with a frequency in the range of 13.7 Hz to 447 KHz may be generated at the Audible Tone Generator (ATG) output. For the same set of inputs, a sine wave with a frequency in the range of 1.05 Hz to 34.4 KHz appears at the TXC/DTMF output.

Column/Transmit Counter

The column/transmit counter circuit is enabled by the CC2 control register bit. A sine wave frequency in the range of 267.8 Hz to 34.4 KHz appears at the TXC/DTMF output. Figure 10 illustrates the column/transmit functional block diagram. For modem operation without the prescaler, the frequency range is 535.7 Hz to 68.8 KHz. A binary count is loaded into the register (CTR) at address location 00F6. The input is then transferred to the counter (CTC). As the counter continues to count, an overflow is generated which serves to reload the counter (CTC) from the contents of the register (CTR).

In the Single Tone Column Mode (CCX = 100), no interrupt is generated. In this mode, the overflow signal serves as one of the clock input signals to the sine wave generator. In this way, a single tone is generated at the TXC/DTMF output.

Combined Modes

In the Modem Mode (CCX = 101), both the pulse width timer mode of the row/receive counter and the single tone column mode are active. This allows simultaneous reception and transmission of data. In telecommunications applications such as duplex 300 bps modem, the row/receive circuitry demodulates the receive carrier at the RXC input while

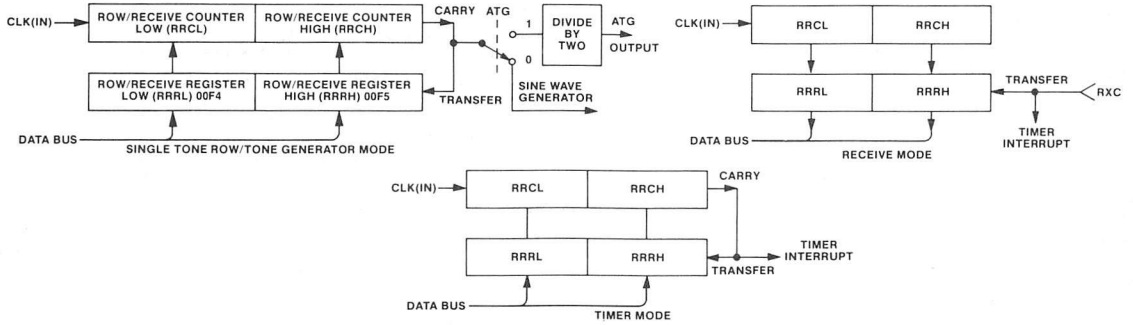


Figure 9. Row/Receive Functional Block Diagram

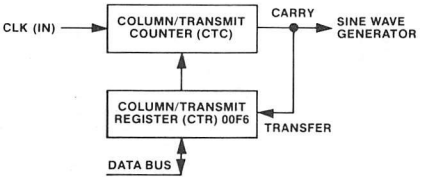


Figure 10. Column/Transmit Functional Block Diagram

the column/transmit circuitry generates the modulated transmit carrier at the TXC/DTMF output. Maximum clock frequency is applied to increase the precision of the transmit carrier frequencies.

In the Modem—Divide-by-Two Prescaler Mode (CCX = 110), operation is the same as the modem mode except that the divide-by-two prescaler is used. In this way, this mode allows low frequency transmit carrier generation.

In the Dual Tone Multifrequency Mode (CCX = 111), a combination of the single tone row mode and single tone column mode is used. In telecommunications applications, this arrangement allows standard DTMF signaling tones to be generated.

Sine Wave Generator

The modem and DTMF output signals are synthesized by the sine wave generator. An approximation of a sine wave is formed by a series of 26 voltage steps per cycle as shown in Figure 11. Figure 12 illustrates the sine wave generator functional block diagram. The two identical divide by 26 circuits are step counters that determine the fixed number of steps per cycle of the sine wave. The inputs to these counters are the outputs of the row/receive and column/transmit dividers that determine the variable step length, or frequency, of each sine wave.

A step select PLA translates the step number from the step counter to a number corresponding to the step voltage level. The D-to-A resistor networks convert these numbers to voltage levels to form the sine wave as shown in Figure 11. The column (high group) frequency amplitude is approximately 2.7 dB greater than the row frequency amplitude to compensate for the high frequency roll-off of the telephone circuit. The outputs of the two D-to-A converters are combined to drive the operational amplifier. V_{REG} is the power supply for the converters and amplifier to ensure a constant tone output level independent of V_{DD} variations. The amplifier output appears on the TXC/DTMF output depending on control register bits, CC0, CC1 and CC2.

To avoid transients when starting or stopping sine wave generation, the output remains at the voltage level defined by the step counters and D-to-A resistor networks when the step counters are stopped.

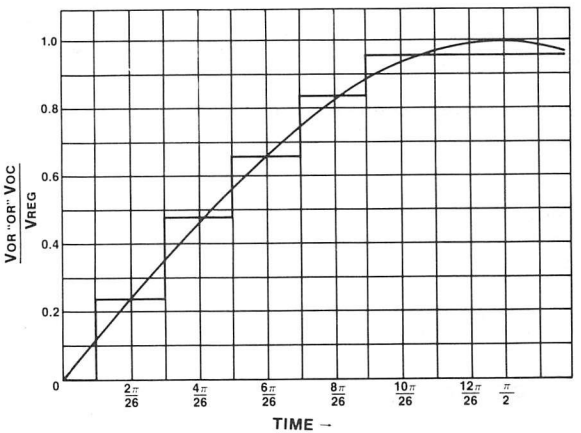


Figure 11. Sine Wave Generator Step Heights

General Formula for Determining Register Values

$$\text{Register Value} = \frac{OSC}{K \times F} - 2$$

$$\text{Register Value (Timer)} = \frac{OSC \times T}{K} - 2$$

OSC = Oscillator Frequency
F = Desired Frequency
T = Timer Period
K = Constant

		Desired Frequency (F) Limits
Modem	K = 26	Limit = 535.7 Hz to 68.8 KHz
Modem with Prescaler	K = 52	Limit = 267.8 Hz to 34.4 KHz
ATG	K = 4	Limit = 13.7 Hz to 447 KHz
μP Clock	K = 4	Limit = 13.7 Hz to 447 KHz
Timer	K = 4	Limits = 2.2349 μS to 73.234 mS

Input/Output Registers

Figure 13 illustrates the I/O registers and their addresses There are 27 I/O lines (PA0-PA7, PB0-PB7, PC0-PC7 and PD0-PD2) associated with four memory addressable registers (00F0-3).

Outputs are set by loading the desired bit pattern into the corresponding I/O register. A logic "1" selects a high output (or OFF), and a logic "0" selects a low output. A read operation always detects the logic state at the I/O pin, regardless of the previously loaded register value. When using the I/O pins as inputs, the I/O register should be loaded to provide the appropriate active level. When reset is active ($\overline{RES}$ = 0), all I/O registers and pins are initialized to a logic "1".

Figure 14 illustrates the circuitry associated with each I/O pin. Depending on the mask option chosen, the output can source either 0 μA, 10 μA, 200 μA, or 1.0mA at V_{OH} = 2.4 volts, or 3mA at 1.5 volts.

Address and Data Buffer

These buffers allow memory and I/O expansion of the microprocessor bus. Each buffer is TTL compatible. Control register bit TSC is set to one for normal operation (bus active). When TSC is set to zero, R/$\overline{W}$, and address lines AB0-AB15 and DB0-DB7 are pulled to ground by a high resistance device. In a typical application, TSC is set to zero when the external bus is not powered. Figure 15 illustrates a complete memory address map.

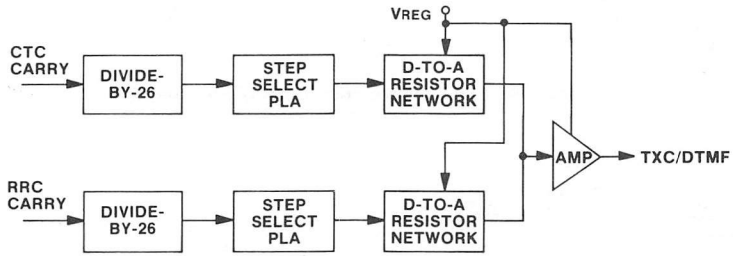


Figure 12. Sine Wave Generator Functional Block Diagram

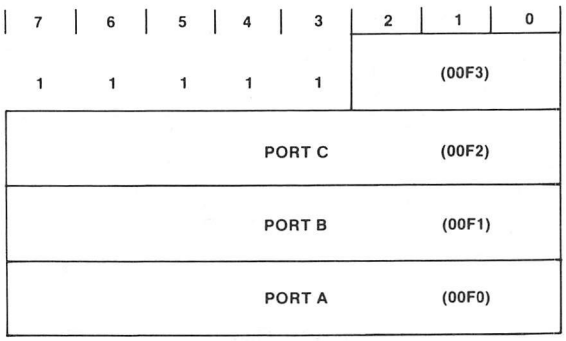


Figure 13. I/O Port Functional Block Diagram

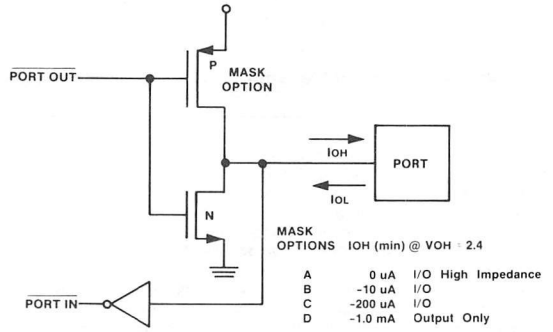


Figure 14. I/O Port Schematic

ADDRESS	DESCRIPTION		
FFFE, F	BREAK	INTERRUPT VECTORS	2048 BYTES ROM
FFFC, D	TIMER COUNTER		
FFFA, B	EXTERNAL		
FFF8, 9	ROW/RECEIVE COUNTER		
FFEE, F	RESET		
FFEC, D	NON-MASKABLE		
FFEB			
F800			
01FF			64 BYTES RAM
01C0			
00FF			TELECOM. REGS.
00F8, 9	TIMER		
00F7	CONTROL		
00F6	COLUMN/TRANSMIT		
00F4, 5	ROW/RECEIVE		
00F3	PD0-2 I/O		
00F2	PC0-7 I/O		
00F1	PB0-7 I/O		
00F0	PA0-7 I/O		
00EF	SEE RANDOM ACCESS MEMORY PARAGRAPH, PAGE 6	(SAME AS 01C0 THRU 01EF, 48 BYTES)	
00C0			

Figure 15. Memory Map

	Oscillator 3.579545 MHz		Oscillator 4.000000 MHz	
Standard Frequency (Hz)	**Register Value**	**Actual Frequency (Hz)**	**Register Value**	**Actual Frequency (Hz)**
	• DTMF Row			
697	97	695	108	699
770	87	773	98	769
852	79	850	88	855
941	71	943	80	938
	• DTMF Column			
1209	55	1208	62	1202
1336	50	1324	56	1326
1477	45	1465	50	1479
1633	40	1639	45	1637
	• Subscriber Tones			
350	195	349	218	350
440	154	441	173	440
480	141	481	158	481
620	109	620	122	620
	• U.S. 110,300 Baud Modem			
1070	62	1076	70	1068
1270	52	1275	59	1261
2025	32	2025	36	2024
2225	29	2221	33	2198
	• European 110,300 Baud Modem			
980	68	983	76	986
1180	56	1187	63	1183
1650	40	1639	45	1637
1850	35	1860	40	1832
	• Teletext			
390	175	389	195	390
450	151	450	169	450
1300	51	1299	57	1304
2100	31	2086	35	2079
	• U.S. 1200 Baud Modem			
390	175	389	195	390
450	151	450	169	450
1200	55	1208	62	1202
2200	29	2221	33	2198

Figure 16. Communications Frequency Generated by Row/Receive and Column/Transmit Counters

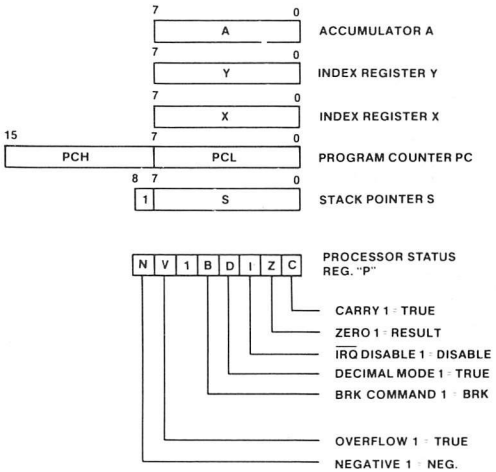


Figure 17. Microprocessor Programming Model

Maximum Frequency Mode (Phase 2, bit 3 is 0)				
Crystal Frequency			Microprocessor Clock	
8 MHz 4 MHz 3.579545 MHz			2 MHz 1 MHz 894.9 KHz*	
Low Power Mode (Phase 2, bit 3 is 1)				
Crystal Frequency	Divide-by-2 Mask Option	Timer Count	Microprocessor Clock	Timer Interrupt Interval (max. freq. mode)
8 MHz 4 MHz	Yes No	0 8 98 998 9998 65535	500 KHz 100 KHz 10 KHz 1 KHz 100 Hz 15.3 Hz*	2 μS 10 μS 100 μS 1 mS 10 mS 65.537 mS
3.579545 MHz	No	0 7 87 893 8947 65535	447.4 KHz* 99.4 KHz* 10.1 KHz* 999.8 Hz* 100.0 Hz* 13.7 Hz*	2.2 μS* 1.0 μS* 99.5 μS* 1.0 mS* 10.0 mS* 73.2 mS*

*Approximate value

Figure 18. Microprocessor Clock Frequency and Timer Interval

MNE-MONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	(4) IMPLIED OP	n	#	(IND, X) OP	n	#	(1) (IND), Y OP	n	#	ZPG,X OP	n	#	(1) ABS,X OP	n	#	(1) ABS,Y OP	n	#	RELATIVE (2) OP	n	#	INDIRECT OP	n	#	ZPG,Y OP	n	#	PROCESSOR STATUS CODE 7 6 4 3 2 1 0 N V B D I Z C	MNE-MONIC
ADC	A + M + C → A (3)	69	2	2	6D	4	3	65	3	2				61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3				72	5	2				N V • • • Z C	ADC
AND	A∧M → A	29	2	2	2D	4	3	25	3	2				21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3				32	5	2				N • • • • Z •	AND
ASL	C ← [7 0] ←0				0E	6	3	06	5	2	0A	2	1							16	6	2	1E	6	3												N • • • • Z C	ASL
BCC	BRANCH IF C=0																												90	2	2							• • • • • • •	BCC
BCS	BRANCH IF C=1																												B0	2	2							• • • • • • •	BCS
BEQ	BRANCH IF Z=1																												F0	2	2							• • • • • • •	BEQ
BIT	A ∧ M (5)	89	2	2	2C	4	3	24	3	2										34	4	2	3C	4	3												M7 M6 • • Z •	BIT
BMI	BRANCH IF N=1																												30	2	2							• • • • • • •	BMI
BNE	BRANCH IF Z=0																												D0	2	2							• • • • • • •	BNE
BPL	BRANCH IF N=0																												10	2	2							• • • • • • •	BPL
BRA	BRANCH ALWAYS																												80	2	2							• • • • • • •	BRA
BRK	BREAK										00	7	1																								• • 1 0 1 • •	BRK
BVC	BRANCH IF V=0																												50	2	2							• • • • • • •	BVC
BVS	BRANCH IF V=1																												70	2	2							• • • • • • •	BVS
CLC	0 → C										18	2	1																								• • • • • • 0	CLC
CLD	0 → D										D8	2	1																								• • • • 0 • •	CLD
CLI	0 → I										58	2	1																								• • • • 0 • •	CLI
CLV	0 → V										B8	2	1																								• 0 • • • • •	CLV
CMP	A-M	C9	2	2	CD	4	3	C5	3	2				C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3				D2	5	2				N • • • • Z C	CMP
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																												N • • • • Z C	CPX
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																												N • • • • Z C	CPY
DEC	DECREMENT				CE	6	3	C6	5	2	3A	2	1							D6	6	2	DE	6	3												N • • • • Z •	DEC
DEX	X-1 → X										CA	2	1																								N • • • • Z •	DEX
DEY	Y-1 → Y										88	2	1																								N • • • • Z •	DEY
EOR	A ⊻ M →A	49	2	2	4D	4	3	45	3	2				41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3				52	5	2				N • • • • Z •	EOR
INC	INCREMENT				EE	6	3	E6	5	2	1A	2	1							F6	6	2	FE	6	3												N • • • • Z •	INC
INX	X + 1 → X										E8	2	1																								N • • • • Z •	INX
INY	Y + 1 → Y										C8	2	1																								N • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3							7C	6	3																6C	6	3				• • • • • • •	JMP
JSR	JUMP SUB				20	6	3																															• • • • • • •	JSR
LDA	M → A	A9	2	2	AD	4	3	A5	3	2				A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3				B2	5	2				N • • • • Z •	LDA
LDX	M → X	A2	2	2	AE	4	3	A6	3	2																BE	4	3							B6	4	2	N • • • • Z •	LDX
LDY	M → Y	A0	2	2	AC	4	3	A4	3	2										B4	4	2	BC	4	3												N • • • • Z •	LDY
LSR	0→ [7 0] → C				4E	6	3	46	5	2	4A	2	1							56	6	2	5E	6	3												0 • • • • Z C	LSR
NOP	NO OPERATION										EA	2	1																								• • • • • • •	NOP
ORA	AVM → A	09	2	2	0D	4	3	05	3	2				01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3				12	5	2				N • • • • Z •	ORA
PHA	A →Ms S-1→S										48	3	1																								• • • • • • •	PHA
PHP	P →Ms S-1→S										08	3	1																								• • • • • • •	PHP
PHX	X →Ms S-1→S										DA	3	1																								• • • • • • •	PHX
PHY	Y →Ms S-1→S										5A	3	1																								• • • • • • •	PHY
PLA	S+1 →S Ms→A										68	4	1																								N • • • • Z •	PLA
PLP	S+1→S Ms→P										28	4	1																								N V 1 D I Z C	PLP
PLX	S+1→S Ms→X										FA	4	1																								N • • • • Z •	PLX
PLY	S+1→S Ms→Y										7A	4	1																								N • • • • Z •	PLY
ROL	← [7 0] ←C←				2E	6	3	26	5	2	2A	2	1							36	6	2	3E	6	3												N • • • • Z C	ROL
ROR	→C→ [7 0] →				6E	6	3	66	5	2	6A	2	1							76	6	2	7E	6	3												N • • • • Z C	ROR
RTI	RTRN INT										40	6	1																								N V 1 D I Z C	RTI
RTS	RTRN SUB										60	6	1																								• • • • • • •	RTS
SBC	A-M-C̄ →A (3)	E9	2	2	ED	4	3	E5	3	2				E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3				F2	5	2				N V • • • Z C	SBC
SEC	1 → C										38	2	1																								• • • • • • 1	SEC
SED	1 → D										F8	2	1																								• • • 1 • • •	SED
SEI	1 → I										78	2	1																								• • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2				81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3				92	5	2				• • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																												• • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2										94	4	2																• • • • • • •	STY
STZ	00 → M				9C	4	3	64	3	2										74	4	2	9E	5	3												• • • • • • •	STZ
TAX	A → X										AA	2	1																								N • • • • Z •	TAX
TAY	A → Y										A8	2	1																								N • • • • Z •	TAY
TRB	A∧M → M (6)				1C	6	3	14	5	2																												• • • • • Z •	TRB
TSB	AVM → M (6)				0C	6	3	04	5	2																												• • • • • Z •	TSB
TSX	S → X										BA	2	1																								N • • • • Z •	TSX
TXA	X → A										8A	2	1																								N • • • • Z •	TXA
TXS	X → S										9A	2	1																								• • • • • • •	TXS
TYA	Y → A										98	2	1																								N • • • • Z •	TYA

Notes:

1. Add 1 to "n" if page boundary is crossed, except STA and STZ.
2. Add 1 to "n" if branch occurs to same page. Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. Accumulator address is included in Implied address.
5. "N" and "V" flags are unchanged in immediate mode.
6. "Z" flag indicates A∧M result (same as BIT instruction).

X Index X
Y Index Y
A Accumulator
M Memory per effective address
Ms Memory per stack pointer

\+ Add
\- Subtract
∧ And
V Or
⊻ Exclusive or

n No. Cycles
No. Bytes
M6 Memory Bit #6
M7 Memory Bit #7

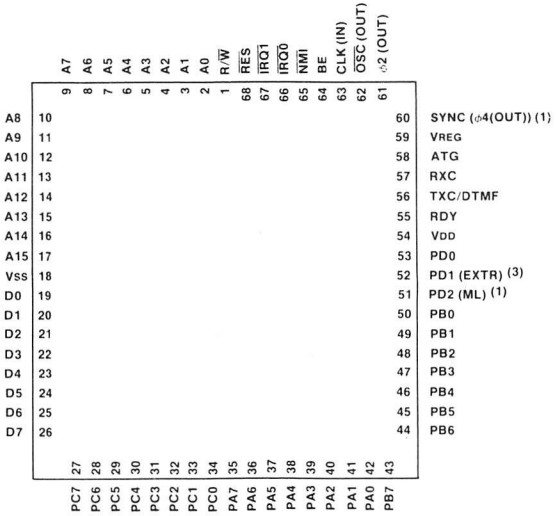
Figure 19. Operational Codes, Execution Times, and Memory Requirements

Pin Function Table

PIN	DESCRIPTION	PIN	DESCRIPTION
A0-Axx	Address Bus	PA0-PA7	Port A
ATG	Audible Tone Generator	PB0-PB7	Port B
BE	Bus Enable	PC0-PC7	Port C
D0-D7	Data Bus	PD0-PD2	Port D
TXC/DTMF	Transmit Carrier/Dial Tone Multifrequency	RDY	Ready
$\overline{IRQ}$	Interrupt Request	$\overline{RES}$	Reset
$\overline{ML}$	Memory Lock	RXC	Receive Carrier
EXTR	External ROM	R/$\overline{W}$	Read/Write
$\overline{NMI}$	Non-Maskable Interrupt	SYNC	Synchronize
CLK(IN)	Clock Input		
$\overline{OSC}$(OUT)	Oscillator Output	V_{DD}	Positive Power Supply (+5.0 volts)
ϕ2(OUT)	Phase 2 Out	V_{REG}	Regulated Supply Voltage
ϕ4(OUT)	Phase 4 Out	V_{SS}	Internal Logic Ground

Pin Configuration

68-Pin Leaded Plastic and Ceramic Chip Carrier



NOTES:
1. ϕ4(OUT) AND ML ARE METAL MASK OPTIONS
2. V_{REG} INTERNALLY CONNECTED TO V_{DD}
3. EXTR SELECTED ONLY IN TEST AND PROTOTYPE MODE

G65SC150 Mask Options

The following mask options are available for the G65SC150, and must be specified before an order can be placed. To ensure that the proper options are selected, always contact the nearest GTE Microcircuits Sales Office prior to placing an order.

1. Oscillator divider for counters and timer
   - Divide-by-two
   - No divider
2. Oscillator feedback resistor
   - Feedback resistor between CLK(IN) and $\overline{OSC}$(OUT)
   - No feedback resistor
3. The following signals are available with or without pull-up resistors:

BE	$\overline{NMI}$	RXC
$\overline{IRQ0}$	RDY	
$\overline{IRQ1}$	$\overline{RES}$	

4. Pin 51 is available with the following signal option:
   PD2 or $\overline{ML}$
5. Pin 60 is available with the following signal option:
   SYNC or $\phi 4$
6. Three optional I/O source currents are available for the following signals. These source currents include: 0μA, 10μA, 200μA @ 2.4V, and 1mA @ 2.4V or 3mA @ 1.5V.

   PA0-PA7
   PB0-PB7
   PC0-PC7
   PD0-PD2

2 Logic Products

GTE MICROCIRCUITS

GTE Microcircuits

Semicustom Design
GTE Gate Arrays

Macro Cells for Complex Logic Designs

When designing complex logic systems, there's but one way to go...and that's with GTE Gate Arrays. They're the perfect answer to logic simplification and component reduction. Chances are, your total design can be put into a single chip. GTE's Gate Arrays offer you a comprehensive family of advanced CMOS macro cell logic functions. You'll discover that with GTE Gate Arrays, you can configure your most complex SSI/MSI logic designs into a single integrated circuit with as many as 2000 gate-equivalent functions per chip. GTE Gate Arrays are the way to go.

As your Total Resource Company, there are three reasons why GTE Microcircuits has become the industry's first choice for Gate Array design, fabrication and production.

1. Total Capability...From Logic to Devices

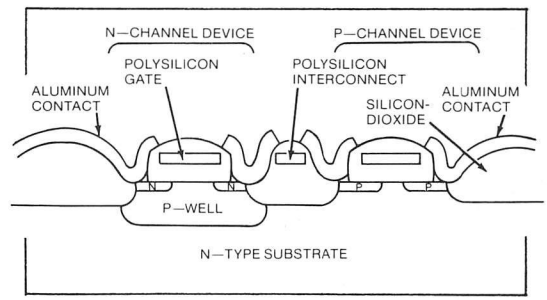
The designing and processing of a Gate Array chip is really quite simple. In fact, just provide us with your logic diagrams and interface specifications and GTE will do the rest. We will provide logic simplification or complexity reduction, simulation, timing analysis, interconnect place and route, prototype fabrication and testing, and final production integrated circuits. With this approach, you do what you do best and we'll do the rest. For minimum involvement, you do the logic and system design and we'll take it from there...reducing your design to an efficient, low cost and functionally equivalent integrated circuit.

2. Fully Automated Logic Integration System... It's a Step Ahead!

Once your logic design has been evaluated and reduced to macro logic functions, and a test plan developed, GTE's computerized system performs logic simulation, testing and pinout compatibility with the Gate Array macro structure. Your logic design is then ready for logic element placement and interconnection within the Gate Array matrix. Although this procedure can be accomplished by the customer, it can be performed much more efficiently by GTE's Automated Logic Integration System (ALIS). GTE's ALIS is a step ahead of the Gate Array industry. It not only relieves the burdensome job of manual logic element placement and interconnection, but also virtually eliminates the possibility of costly human error. Once the place and route is complete, the routed array is digitized and pattern generation tapes are produced for final mask tooling and prototype assembly.

3. Advanced CMOS Gate Array Technology...It's the Way of the Future!

GTE Microcircuits has the leading edge in Advanced CMOS Gate Array technology. Isolated Complementary Metal Oxide Semiconductors offers the speed and performance advantages of NMOS with the added benefits of increased reliability, greater noise immunity, and perhaps most important, significantly less power consumption. And furthermore, Advanced CMOS Gate Arrays are TTL/CMOS input/output compatible, and they require only a single supply voltage (+5V).



CMOS Topology

Technical Description

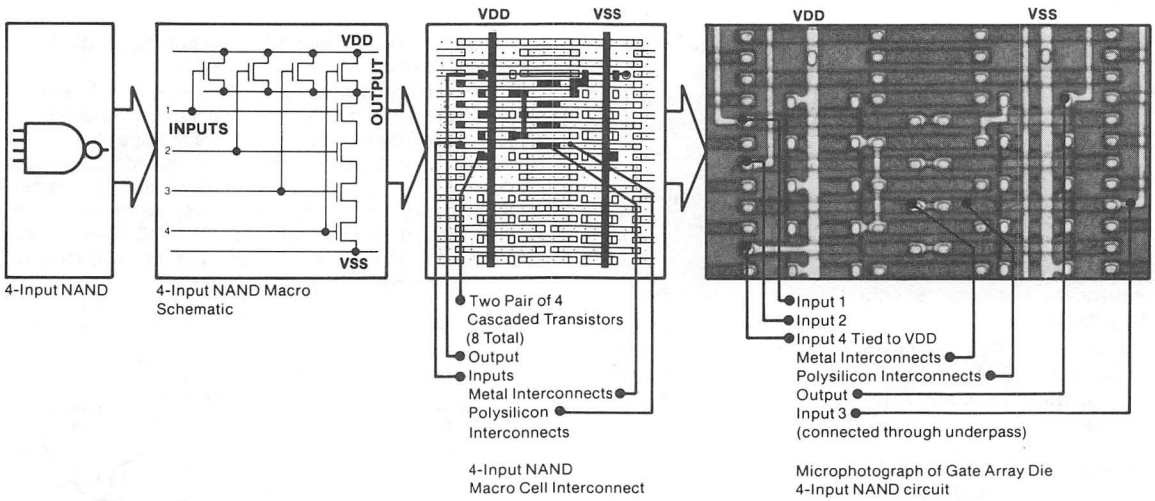
Features

- Advanced CMOS high speed, low power technology
- Gate propagation delays—2.9 nS (2-input NAND)
- Gate power dissipation—5 μW at 1 MHz typical
- CMOS or TTL interface
- Bus oriented interconnect paths
- On-chip resistors and capacitors
- Over 88 macro logic functions
- Array sizes from 500 to 2000 gates
- A wide range of packaging options
- Single power supply

The Transistor Array

Each macro function is implemented within a cell or by grouping multiple cells. Each array is based on a matrix of uncommitted cells, where each cell consists of eight transistors...four cascaded N-channel and four cascaded P-channel devices. These cells are arranged in rows, and when appropriately connected, make up the various logic functions found in the Macro Cell Library.

Gate Array Design Flow



Configuring a cell is accomplished by metal traces in the bus paths and by using polysilicon underpasses. These underpasses run horizontally between the cell rows as well as through the cells themselves. There are also vertical underpasses which serve to provide interconnection across a column of cells or bus paths without obstructing the bus paths. I/O pads, input protection circuitry, resistors, capacitors and output drivers are placed around the periphery of the array and are readily connected to the internal logic functions.

The Macro Cell Library

Table 1 provides a partial listing of currently available macro cell logic function. GTE offers over 88 different logic function configurations ranging from a simple 2-input NAND gate to cascadable shift registers. GTE's complement of macro logic functions will satisfy your most demanding system configuration and we're adding new functions all the time. As a special note, if you have a logic configuration which is not represented in our library, GTE will develop a custom macro cell for your requirement...and the cost is nominal.

Gate Array Configurations

GTE uses the "gate equivalent" method for describing the various array sizes. One "gate" is equivalent to a 2-input NAND/NOR gate. In this way, each macro cell function within the Macro Cell Library can be related to a "gate equivalent" (2-input NAND) requiring one-half cell, but an Edge-Triggered "D" Flip-Flop requires four cells. Therefore, the Flip-Flop requires array space equal to eight "gate equivalents". The "gate equivalent" method will help you in planning the array size needed for your application. GTE offers arrays in "gate equivalent" sizes ranging from 500 to 2000 gates, with up to 84 I/O bond pads per array.

I/O Configurations

Your Gate Array I/O configuration will vary with the array size and to some degree with its complexity. As shown in Table 2, all I/O pads except two predefined power supply connection pads (V_{SS} and V_{DD}) can be configured as Input or Outputs. I/O configuration characteristics include:

- Individually tailored input switching characteristics for either CMOS or TTL compatibility
- Low power Schottky output buffers for driving up to two "LS" TTL loads (CMOS level output)
- TTL output buffers for driving up to 1.5 standard TTL loads or six "LS" TTL loads (CMOS level outputs)
- All Gate Array output buffers can be configured for three-state or open-drain (open collector) operation

Table 1. GTE Macro Cell

Library Examples (Partial Listing)

Function	No. Cells Req'd
2-Input NAND	1/2
8-Input NAND	3
2-Input NOR	1/2
4-Input OR (High Speed)	1-1/2
Complementary Input Exclusive OR/NOR	1
Triple Inverter	1
Dual Inverter	1
Inverter	1/2
Break Before Make	2
Exclusive OR	1-1/2
Transmission Gate	1
Clock Driver	2
Output Driver (4 TTL Loads)	2
CMOS Input Buffer	Input
TTL Input Buffer	Input
Output Stage Pull-Up	Output
Output Stage Pull-Down	Output
Output Stage (Three-State)	Output
Output Stage (Totem Pole)	Output
Edge Triggered "D" Flip Flop	4
D-Type Flip-Flop With Cascadable Clock (Static Shift Register Element)	2
"D" Type Transparent Latch	2
Edge Triggered J-K Flip Flop	5
Cascadable Static Ripple Counter	2
CSSR, Asynchronous Parallel Load	4
CSSR, Asynchronous Clear	3

Table 2. GTE Gate Array Configurations

Device	No. of Gates (1)	No. of Pads (2)	Chip Size	Package Pins Required
G50500B	504	44	124 × 200	16—44
G51000B	960	54	175 × 223	24—68
G51500B	1512	70	228 × 247	24—68
G52000B	2024	82	245 × 289	24—84

1. Gates configured as 2-input NAND.
2. Includes one V_{DD} pad and one V_{SS} pad.

G50000B Series

Microcircuits

CMOS Gate Arrays

Features

- CMOS high speed, low power technology
- Gate propagation delay—2.9 nS (2-input NAND)
- Gate power dissipation—5 μW at 1 MHz typical
- CMOS or TTL interface
- Bus oriented interconnect paths
- On-chip resistors and capacitors
- Array sizes from 500 to 2000 gates
- Over 88 macro logic functions
- Single power supply (+5 Vdc)
- Wide range of packaging options

General Description

GTE's G50000B Series Gate Arrays are manufactured using CMOS high performance technology for higher speed and lower power operation. Each Gate Array cell consists of a matrix of four P-channel and four N-channel transistors which can be programmed for metal mask interconnection to provide virtually unlimited implementation of LSI logic designs. Within each logic cell and under the bus routes, polysilicon cross-unders provide logic interconnection with the metal layer. These crossunders, combined with vertical bus routes, allow both vertical and horizontal interconnection, thus providing highly efficient chip utilization and circuit complexity. Macro logic functions are selected from a standard library of over 88 preconnected logic functions. Each array contains a number of resistors and capacitors which provide the circuits with limited analog capability. GTE offers arrays in sizes ranging from 500 to 2000 equivalent 2-input NANDS, with up to 80 I/O pads per array.

GTE Gate Array Configurations

Device	No. of Gates (1)	No. of Pads (2)	Chip Size	Package Pins Required
G50500B	504	44	124×200	16—44
G51000B	960	54	175×223	24—68
G51500B	1512	70	228 × 247	24—68
G52000B	2024	82	245 × 289	24—84

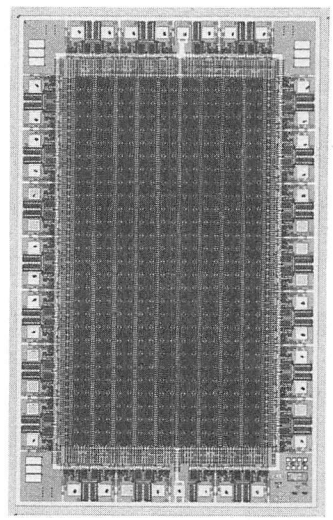
1. Gates configured as 2-input NAND.
2. Includes one V_{DD} pad and one V_{SS} pad.

On-Chip Resistors and Capacitors

On-chip resistors and capacitors are positioned around the array to allow connection to either I/O cells or function cells.

	Number of Components and Bond-Pads				Typ	
Component	G50500B	G51000B	G51500B	G52000B	Value	Unit
Resistors	12	12	12	12	40	KΩ
Capacitors	9	9	9	9	0.5	pF

Array Configuration



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Supply Voltage	V_{DD}	-0.5V to 7.0V
Input Voltage	V_I	-0.3V to V_{CC} + 0.3V
Output Current, Any Output	I_O	±50 mA
Operating Temperature	T_A	-55° C to 125° C
Storage Temperature	T_S	-65° C to 150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics, Low Power Schottky Compatible Configurations: V_{DD} = 5.0V ± 10%, V_{SS} = 0V, T_A = -40° C to +85° C

Parameter	Symbol	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0		V	V_{CC} = 4.75
Low Level Input Voltage	V_{IL}		0.8	V	V_{CC} = 4.75
High Level Output Voltage	V_{OH}	2.4		V	I_{OH} = 6.3 mA, V_{CC} = 4.75V
		4.5		V	I_{OH} = 2.0 mA, V_{CC} = 4.75V
Low Level Output Voltage	V_{OL}		0.4	V	I_{OL} = -3.9 mA
High Level Input Current	I_{IH}		10	μA	V_I = 2.7V
Low Level Input Current	I_{IL}		-10	μA	V_I = 0.4V
Off-State Output Current, High-Level Voltage Applied	I_{OZH}		20	μA	V_O = 2.7V
Off-State Output Current, Low-Level Voltage Applied	I_{OZL}		-20	μA	V_O = 0.4V

DC Characteristics, CMOS Compatible Configuration: V_{DD} = 5.0V ± 10%, V_{SS} = 0V, T_A = -40° C to +85° C

Parameter	Symbol	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	3.5		V	
Low Level Input Voltage	V_{IL}		1.5	V	
High Level Output Voltage	V_{OH}	4.95		V	I_{OH} = 1μA
Low Level Output Voltage	V_{OL}		0.05	V	I_{OL} = -1μA
High Level Input Current	I_{IH}		1	μA	V_I = 5.0V
Low Level Input Current	I_{IL}		-1	μA	V_I = 0V
Off-State Output Current, High-Level Voltage Applied	I_{OZH}		20	μA	V_O = 5.0V
Off-State Output Current, Low-Level Voltage Applied	I_{OZL}		-20	μA	V_O = 0V

AC Characteristics: V_{DD} = 5.0V, V_{SS} = 0V, T_A = 27° C, R = 0Ω, C_L = 1 Unit Load, Input Rise/Fall = 5 nS

Parameter	Macro Cell	Min	Max	Unit	Test Conditions
Single Inverter	GTE5002		1.7	nS	
2-Input NAND	GTE5005		2.9	nS	
Output Buffer, Non-Inverting Stage With Three-State Output	GTE5008		13.1	nS	R = 4000Ω, C_L = 15 pF
Input Buffer, TTL (Inverting)	GTE5102		2.2	nS	

Custom Products
Customer Furnished Tooling (CFT™)

GTE Makes It Easy!

GTE Microcircuit's CFT program is for those customers who have access to a MOS design group and wish to design their own devices, or for those who have already processed a MOS design and would like to tool up a second source. GTE's CFT program is easy to use, with many customer options. In fact, you can enter the program at any one of a variety of process points...just pick the entry level that best suits your needs. You will also find that GTE's processing capability is the best there is and we can do it all...from the latest in low power Advanced CMOS processing to conventional N-Channel and bipolar technologies.

Remember, your point of entry into the CFT program can be just about anywhere...and you can rely on GTE to take it from there.

As an example, let's take a look at the most basic entry level. In this case, the customer furnishes GTE with "working plates" or "masks" for his MOS design. We will then manufacture ten or more wafers using the customer-specified GTE process. These wafers can either be shipped directly to the customer for testing, or tested by GTE using a customer supplied Sentry VII, MTS77, or Fairchild Xincom 5580 test tape. Note that if the program is intended for high volume production, we recommend that GTE process control monitors and alignment marks be incorporated into the customer's master plates. This will provide significant diagnostic and test capabilities.

From this point, it's a matter of determining yields and establishing production requirements, packaging, etc. Although this example represents the most basic CFT program, it's quite typical of most second source program requirements.

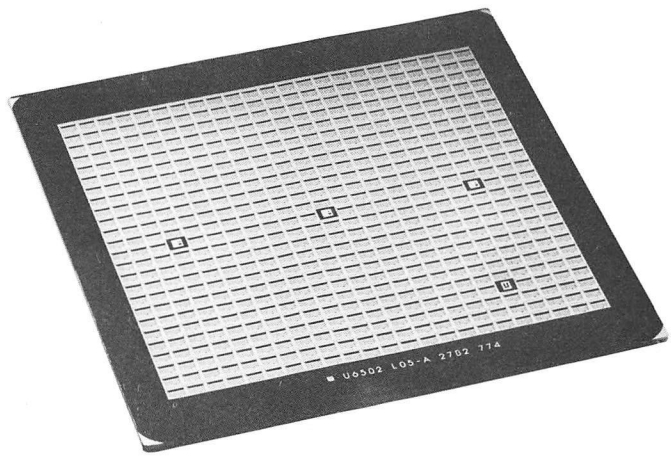
GTE can also assist you for entry at other levels, by providing:

- Composite Design and Digitizing
- Test Generation
- Pattern Generation
- Mask Fabrication
- Wafer Sort and Test
- Packaging

If you are engaged in a new design, GTE prefers to work with your design engineers at the earliest possible point in the design process. This allows GTE to provide the customer with specifications relative to design rules and process parameters. Design workshops can be provided to assist the customer in planning and optimizing his design for maximum yield and testability...each resulting in lower production cost.

So if you're considering a new MOS design, or you would like to establish a reliable, long term second source... GTE Microcircuits is your answer.

At GTE Microcircuits, no challenge is too great...we welcome your most complex designs!



Standard Cells

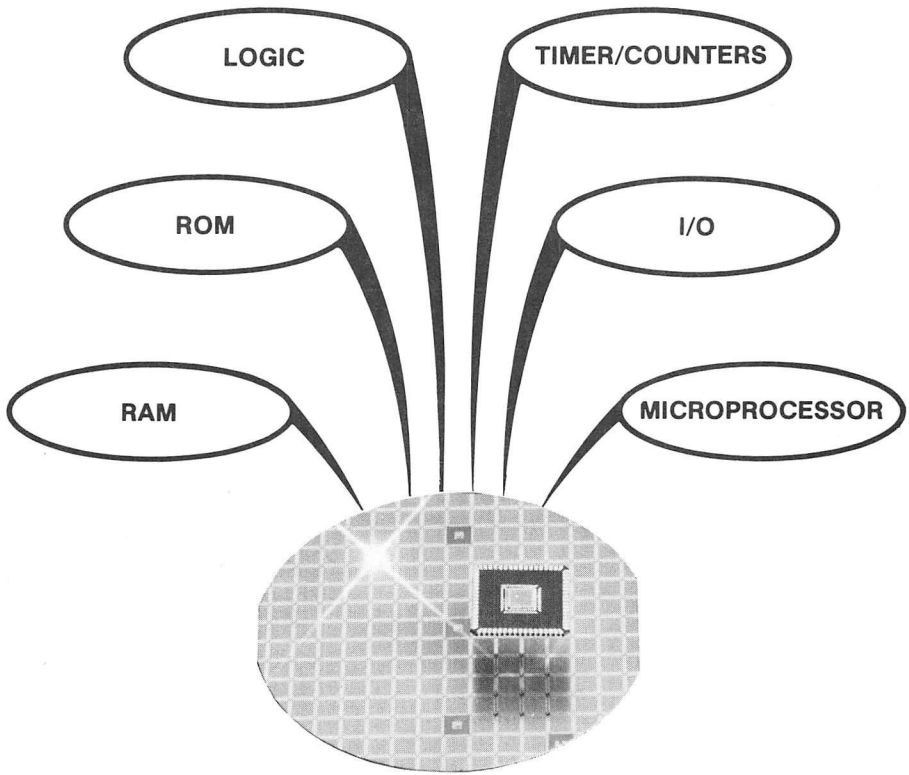
Building Blocks for Single Chip Designs

GTE Microcircuits offers a variety of Advanced CMOS Standard Cells. These cells are your building blocks for semicustom chip configurations. Many times, the needs of a particular application cannot support the expense and time of a full custom integrated circuit. When this is the case, GTE's Standard Cells provide the perfect solution...offering not only ease of implementation and design flexibility, but low cost and fast turnaround time. You'll find that your choice of internal functions and interface configurations is almost limitless...and it all takes place within a single chip. Internal design functions may include:

- Microprocessor—from the G65SC00 Microprocessor family
- ROM—for permanent data storage
- RAM—for temporary data storage
- I/O—special or expanded I/O configurations
- Logic—GTE Gate Array Macro Logic and other internal logic cells for logic control functions

So next time you have an application which requires multiple-chip functions, contact GTE Microcircuits. Chances are, we can put it ALL IN A SINGLE CHIP!

Semicustom Designs From Standard Cells



G74SC137
G74SC138
G74SC139

Microcircuits

CMOS Octal Decoders/Demultiplexers

Features

- Equivalent to 74LS series
- Low power oxide isolated silicon gate CMOS technology
- Short propagation delay
- Improved noise margins
- High current, sink/source capability

General Description

This family of CMOS decoders/demultiplexers is designed for use in high speed memory and peripheral address decoding systems. The G74SC138 decodes three binary inputs (A0, A1, A2) to select 1-of-8 mutually exclusive outputs ($\overline{00}$-$\overline{07}$). Three enable inputs, two active low ($\overline{E1}$, $\overline{E2}$) and one active high (E3), reduce the need for external gates in an expanded system. The G74SC137 features additional latches on A0, A1, and A2 for use in glitch free applications. When Latch Enable (LE) is low the device acts as a G74SC138. When LE is high, the address present at A0 to A2 is stored. A 1-of-32 decoder requires only four of these devices and one inverter. The G74SC139 features two individual, two line (A0, A1) to four line ($\overline{00}$-$\overline{03}$) decoders. Each decoder has an active low Enable (E) which can also be used as a data input in a full four-minterm, of two variables decode.

Pin Function Table

Pin	Description
A0, A1, A2 or A0a, A0b A1a, A1b	Address Inputs to be Decoded
$\overline{E1}$, $\overline{E2}$, E3 or $\overline{Ea}$, $\overline{Eb}$ or $\overline{E1}$, E2	Chip Enable Inputs

Pin	Description
LE	Latch Enable Input
$\overline{O0}$-$\overline{O7}$	Inverted Outputs to Peripheral
V_{CC}	Positive Supply Voltage
V_{SS}	System Ground

Device Selection

Part Number	Format	Data Output	Package	Temp. Range
G74SC137D	1-of-8 Latched Address	Inverted	16-Pin Cerdip	-40° C to +85° C
G74SC137P	1-of-8 Latched Address	Inverted	16-Pin Plastic	-40° C to +85° C
G74SC138D	1-of-8	Inverted	16-Pin Cerdip	-40° C to +85° C
G74SC138P	1-of-8	Inverted	16-Pin Plastic	-40° C to +85° C
G74SC139D	Dual 1-of-4	Inverted	16-Pin Cerdip	-40° C to +85° C
G74SC139P	Dual 1-of-4	Inverted	16-Pin Plastic	-40° C to +85° C

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Supply Voltage	V_{CC}	-0.5V to 7.0V
Input Voltage	V_I	-0.3V to V_{CC} + 0.3V
Output Current Each Output	I_O	±75mA
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-65° C to +150° C
Package Power Dissipation	P	450 mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated values.

Recommended Operating Conditions:
All Voltages Referenced to V_{SS}

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.0	5	6.5	V
Input Voltage	V_I	0		V_{CC}	V
Operating Free-air Temp.	T_A	-40		+85	°C

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.
2. Max. dissipation of 1mS should not be exceeded.
3. All typical values at T_A = 25° C, V_{CC} = 5V.

DC Characteristics: Full operating free-air temperature range unless otherwise noted.

Parameter	Symbol	Min	Typ[3]	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2			V	V_{CC} = 5.25V
Low Level Input Voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
High Level Output Voltage	V_{OH}	2.4			V	V_{CC} = 4.75V, I_{OH} = -14mA
		4.0			V	V_{CC} = 4.75V, I_{OH} = -3mA
Low Level Output Voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 8mA
Input Current at Maximum Input Voltage	I_I			15	μA	V_{CC} = 5.25V, V_I = 5.55V
High Level Input Current	I_{IH}			10	μA	V_{CC} = 5.25V, V_I = 2.7V
Low Level Input Current	I_{IL}			-10	μA	V_{CC} = 5.25V, V_I = 0.4V
Off-State Output Current High-Level Voltage Applied	I_{OZH}			20	μA	V_{CC} = 5.25V, V_O = 2.7V
Off-State Output Current Low-Level Voltage Applied	I_{OZL}			-20	μA	V_{CC} = 5.25V, V_O = 0.4V
Short Circuit Output Current (Note 2)	I_{OS}		-40		mA	V_{CC} = 5.25V
Quiescent Supply Current	I_{CC}			0.1	mA	V_{CC} = 5.25V, Outputs Disabled

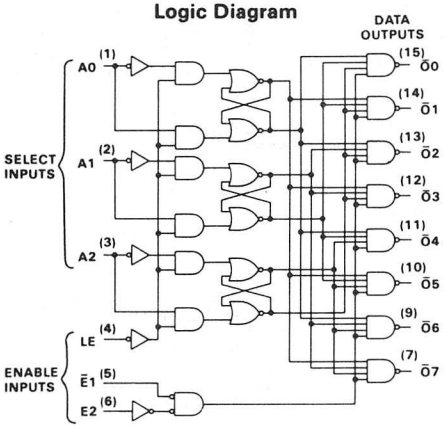
AC Characteristics: V_{CC} = 5V, T_A = 25° C.

Parameter	Symbol	Device	Min	Typ	Max	Unit	Test Conditions
Propagation Delay Time Address to Output	t_{PLH}	G74SC137 G74SC138 G74SC139		25 22 29	38 35 48	nS	
Propagation Delay Time Address to Output	t_{PHL}	G74SC137 G74SC138 G74SC139		31 24 30	52 42 50	nS	
Propagation Delay Time E to Output	t_{PLH}	G74SC137 G74SC138 G74SC139		31 31 22	44 44 35	nS	C_L = 15pF R_L = 2K Ω
Propagation Delay Time E to Output	t_{PHL}	G74SC137 G74SC138 G74SC139		31 33 30	48 48 53	nS	
Set Up Time, Address to Latch Enable Hold	t_{su}	G74SC137	10			nS	
Hold Time Output from Latch Disable	t_h	G74SC137	10			nS	
Input Capacitance	C_I	G74SC137 G74SC138 G74SC139		8 8 8		pF	

Logic and Connection Diagrams

G74SC137

Logic Diagram

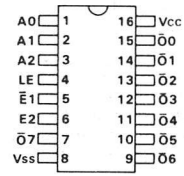


Truth Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
LE	E2	Ē1	A2	A1	A0	Ō0	Ō1	Ō2	Ō3	Ō4	Ō5	Ō6	Ō7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	OUTPUT CORRESPONDING TO STORED ADDR. L: ALL OTHERS H.							

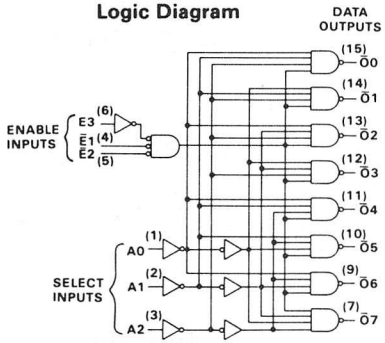
H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

Connection Diagram



G74SC138

Logic Diagram

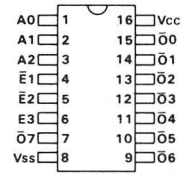


Truth Table

INPUTS					OUTPUTS							
ENABLE		SELECT										
E3	Ē½	A2	A1	A0	Ō0	Ō1	Ō2	Ō3	Ō4	Ō5	Ō6	Ō7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

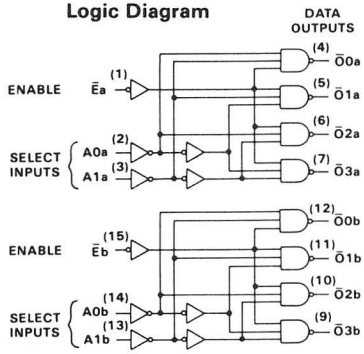
H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

Connection Diagram



G74SC139

Logic Diagram

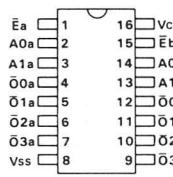


Truth Table

INPUTS			OUTPUTS			
ENABLE	SELECT					
Ē	A1	A0	Ō0	Ō1	Ō2	Ō3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

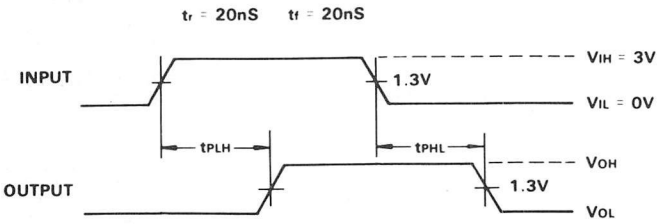
H = HIGH LEVEL, L = LOW LEVEL,
X = IRRELEVANT

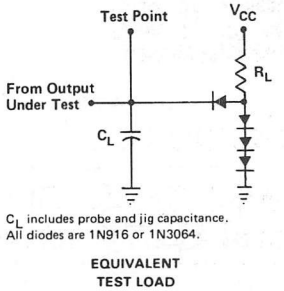
Connection Diagram



LOGIC PRODUCTS

Timing Diagrams





C_L includes probe and jig capacitance.
All diodes are 1N916 or 1N3064.

EQUIVALENT
TEST LOAD

Fig. 1 Propagation Delay Times

G74SC240
G74SC241
G74SC244

Microcircuits

CMOS Three-State Octal Buffers/Line Drivers

Features

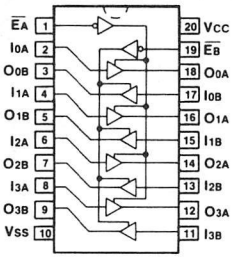
- Equivalent to 74LS series
- Low power oxide isolated silicon gate CMOS technology
- Short propagation delay
- Improved noise margins
- Bus oriented 3-state outputs
- High current, sink/source capability

General Description

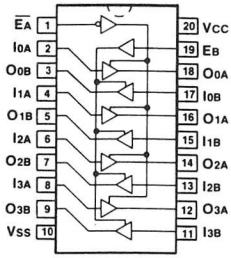
This family of CMOS octal buffers and line drivers are designed to improve circuit board density and performance in three-state memory address drivers, clock drivers and bus oriented receivers and transmitters. A comprehensive range of devices covers a selection of differing input/output pin layouts, inverting and non-inverting buffers, and a choice of similar or complementary output controls ($\overline{E_A}$, $\overline{E_B}$).

LOGIC PRODUCTS

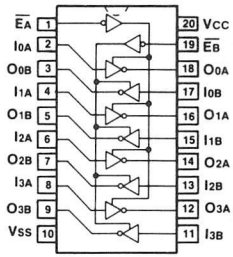
Logic and Connection Diagrams (Top View)



G74SC240



G74SC241



G74SC244

Truth Tables

Inputs		Output	
$\overline{E}$	I_{0-3}	G74SC240 O_{0-3}	G74SC244 O_{0-3}
L	L	H	L
L	H	L	H
H	X	Z	Z

A or B Buffers

G74SC241					
A Buffers			B Buffers		
Inputs		Output	Inputs		Output
$\overline{E_A}$	I_{0-3}	O_{0-3}	E_B	I_{0-3}	O_{0-3}
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

L Logic Low
H Logic High
X Don't Care
Z High Impedence

Pin Function Table

Pin	Description
$\overline{E_A}$, $\overline{E_B}$ or $\overline{E_A}$, E_B	Data Output Enable
I_{0A} - I_{3A} I_{0B} - I_{3B} or I_0 - I_7	Data Inputs
O_{0A} - O_{3A} O_{0B} - O_{3B} or O_0 - O_7	Data Outputs
V_{CC}	Positive Voltage Supply
V_{SS}	System Ground

Device Selection

Part Number	3-State Control	Data Outputs
G74SC240	$\overline{E_A}$, $\overline{E_B}$	Inverting
G74SC241	$\overline{E_A}$, E_B	Non-Inverting
G74SC244	$\overline{E_A}$, $\overline{E_B}$	Non-Inverting

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Supply Voltage	V_{CC}	-0.5V to 7.0V
Input Voltage	V_I	-0.3V to V_{CC} + 0.3V
Output Current	I_O	±75mA
Storage Temperature	T_S	-65° C to +150° C
Operating Temperature	T_A	-40° C to +85° C
Power Dissipation	P	450 mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated values.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.
2. Max. dissipation or 1mS duration should not be exceeded.
3. All typical values at T_A = 25° C, V_{CC} = 5V.

Recommended Operating Conditions: All voltages referenced to V_{SS}.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3	5	6.5	V
Input Voltage	V_I	0		V_{CC}	V
Operating Free-Air Temperature	I_A	-40		+85	°C

DC Characteristics: Full operating free-air temperature range unless otherwise noted. All voltages referenced to V_{SS}.

Parameter	Symbol	Min	Typ[3]	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low Level Input Voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
High Level Output Voltage	V_{OH}	2.4			V	V_{CC} = 4.75V, I_{OH} = -14mA
		4.0			V	V_{CC} = 4.75V, I_{OH} = -3mA
Low Level Output Voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 10mA
Input Current at Maximum Input Voltage	I_I			15	μA	V_{CC} = 5.25V, V_I = 5.55V
High Level Input Current	I_{IH}			10	μA	V_{CC} = 5.25V, V_I = 2.7V
Low Level Input Current	I_{IL}			-10	μA	V_{CC} = 5.25V, V_I = 0.4V
Off-State Output Current High-Level Voltage Applied	I_{OZH}			20	μA	V_{CC} = 5.25V, V_O = 2.7V
Off-State Output Current Low-Level Voltage Applied	I_{OZL}			-20	μA	V_{CC} = 5.25V, V_O = 0.4V
Short Circuit Output Current (Note 2)	I_{OS}		-40		mA	V_{CC} = 5.25V
Quiescent Supply Current	I_{CC}			0.1	mA	V_{CC} = 5.25V, Outputs Disabled

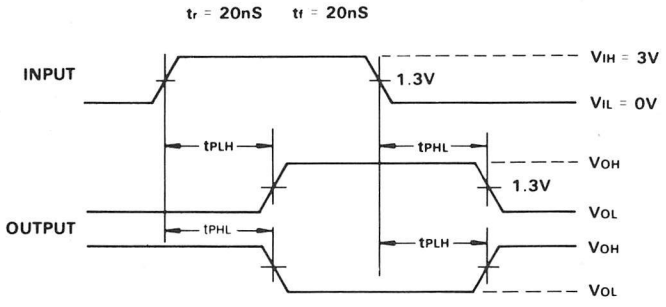
AC Characteristics: V_{CC} = 5V, T_A = 25° C.

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Propagation Delay Time Low to High Output	G74SC240	t_{PLH}		19	35	nS	R_L = 667 Ω, R_C = ∞, C_L = 45pF
	G74SC241/244			21	38		
Propagation Delay Time High to Low Input	G74SC240	t_{PHL}		20	35	nS	
	G74SC241/244			23	40		
Output Enable Time to Low Level	G74SC240	t_{PZL}		21	40	nS	R_L = 667 Ω, R_C = 5K Ω, C_L = 5pF
	G74SC241/244			22	42		
Output Enable Time to High Level	G74SC240	t_{PZH}		20	35	nS	
	G74SC241/244			21	38		
Output Disable Time from Low Level	G74SC240	t_{PLZ}		22	35	nS	
	G74SC241/244			24	38		
Output Disable Time from High Level	G74SC240	t_{PHZ}		42	55	nS	
	G74SC241/244			48	60		

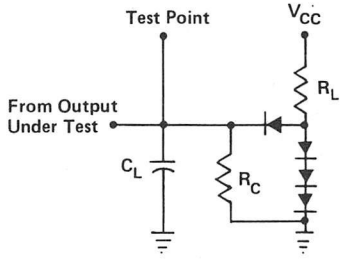
AC Characteristics: (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Disable Time from Low Level G74SC240	t_{PLZ}		22	35	nS	R_L = 667 Ω R_C = 1K Ω C_L = 5pF
Output Disable Time from Low Level G74SC241/244			24	38		
Output Disable Time from High Level G74SC240	t_{PHZ}		30	40	nS	
Output Disable Time from High Level G74SC241/244			33	45		
Input Capacitance G74SC240	C_I		8		pF	
Input Capacitance G74SC241/244			8			

Timing Diagrams

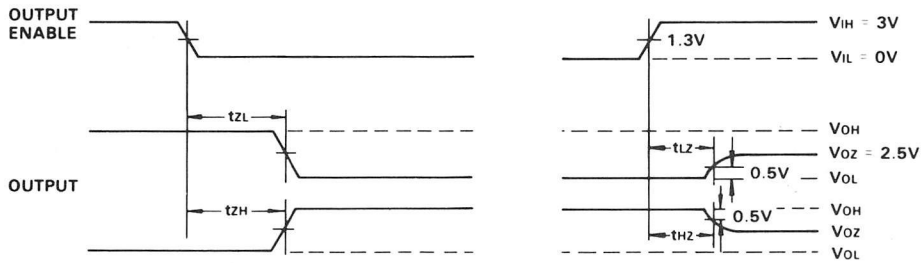


PROPAGATION DELAY TIMES



C_L includes probe and jig capacitance.
All diodes are 1N916 or 1N3064.

EQUIVALENT
TEST LOAD



ENABLE, DISABLE TIMES

G74SC245

Microcircuits

CMOS Octal Bus Transceivers with 3-State Buffered Outputs

Features

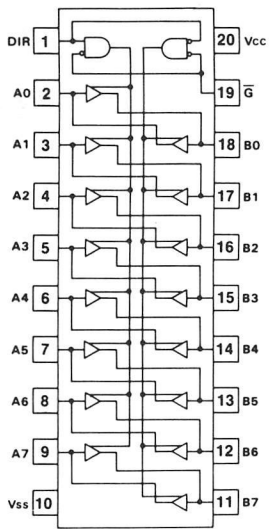
- Pin compatible with 74LS245
- Low power oxide isolated silicon gate CMOS technology
- Short propagation delay
- Bus oriented 3-state outputs
- CMOS inputs reduce DC loading
- High performance input/output clamping
- Fully TTL compatible inputs and outputs

General Description

This octal bus transceiver circuit is designed for high-speed asynchronous two-way communication between data buses. The control function inputs minimize external timing requirements.

The devices provide data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control input (DIR) pin. The enable input ($\overline{G}$) pin can be used to disable the device outputs so that the buses are effectively isolated from each other.

Logic and Connection Diagram (Top View)



Pin Function Table

Pin	Description
A0-A7	Bus A, Data Inputs/Outputs
B0-B7	Bus B, Data Inputs/Outputs
DIR	Direction Control Input
$\overline{G}$	Enable Input, Active LOW
VCC	Positive Supply Voltage
VSS	System Ground

Device Selection

Part Number	Package	Temp. Range
G74SC245D	20-Pin Cerdip	-40°C to +85°C
G74SC245P	20-Pin Plastic	-40°C to +85°C

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Supply Voltage	V_{CC}	-0.5V to 7.0V
Input Voltage	V_I	-0.3V to V_{CC} + 0.3V
Output Current	I_O	±75mA
Storage Temperature	T_S	-65° C to +150° C
Operating Temperature	T_A	-40° C to +85° C
Power Dissipation	P	450 mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

Recommended Operating Conditions: All voltages referenced to V_{SS}.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	5.0	6.5	V
Input Voltage	V_I	0.0		V_{CC}	V
Operating Free-Air Temperature	T_A	-40		+85	°C

DC Characteristics: Full operating free-air temperature range unless otherwise noted.

Parameter	Symbol	Min	Typ[3]	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2			V	V_{CC} = 5.25V
Low Level Input Voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
High Level Output Voltage	V_{OH}	2.4			V	V_{CC} = 4.75V, I_{OH} = -14mA
		4.0			V	V_{CC} = 4.75V, I_{OH} = -3mA
Low Level Output Voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 10mA
Input Current at Maximum Input Voltage	I_I			15	µA	V_{CC} = 5.25V, V_I = 5.55V
High Level Input Current	I_{IH}			10	µA	V_{CC} = 5.25V, V_I = 2.7V
Low Level Input Current	I_{IL}			-10	µA	V_{CC} = 5.25V, V_I = 0.4V
Off-State Output Current High-Level Voltage Applied	I_{OZH}			20	µA	V_{CC} = 5.25V, V_O = 2.7V
Off-State Output Current Low-Level Voltage Applied	I_{OZL}			-20	µA	V_{CC} = 5.25V, V_O = 0.4V
Short Circuit Output Current (Note 2)	I_{OS}		-40		mA	V_{CC} = 5.25V
Quiescent Supply Current	I_{CC}			0.1	mA	V_{CC} = 5.25V, Outputs Disabled

AC Characteristics: V_{CC} = 5V, T_A = 25° C.

Parameter	Symbol	Min	Typ[3]	Max	Unit	Test Conditions
Propagation Delay Time Low to High Output	t_{PLH}		22	33	nS	R_L = 667 Ω, C_L = 45pF, R_C = ∞
Propagation Delay Time High to Low Input	t_{PHL}		25	40	nS	
Output Enable Time to Low Level	t_{PZL}		31	46	nS	R_L = 667 Ω, C_L = 5pF, R_C = 5K Ω
Output Enable Time to High Level	t_{PZH}		30	40	nS	
Output Disable Time from Low Level	t_{PLZ}		31	42	nS	
Output Disable Time from High Level	t_{PHZ}		40	57	nS	

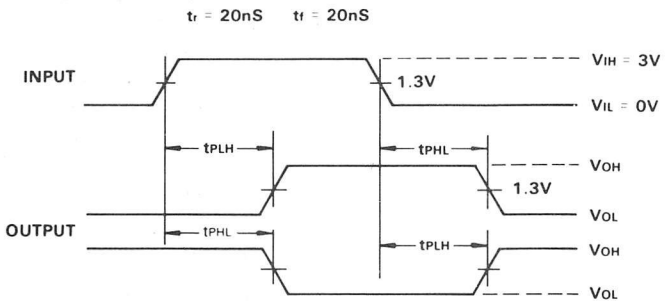
AC Characteristics: (Continued)

Parameter	Symbol	Min	Typ[3]	Max	Unit	Test Conditions
Output Disable Time from Low Level	tPLZ		31	42	nS	R_L = 667 Ω C_L = 5pF R_C = 1K Ω
Output Disable Time from High Level	tPHZ		21	30	nS	
Input Capacitance	CI		8		pF	

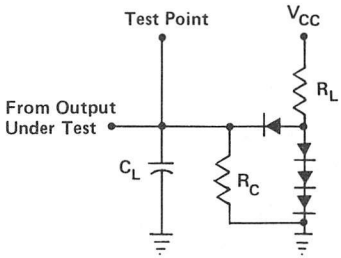
Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.
2. Max. dissipation of 1mS should not be exceeded.
3. All typical values at T_A = 25°C, V_{CC} = 5V.

Timing Diagrams

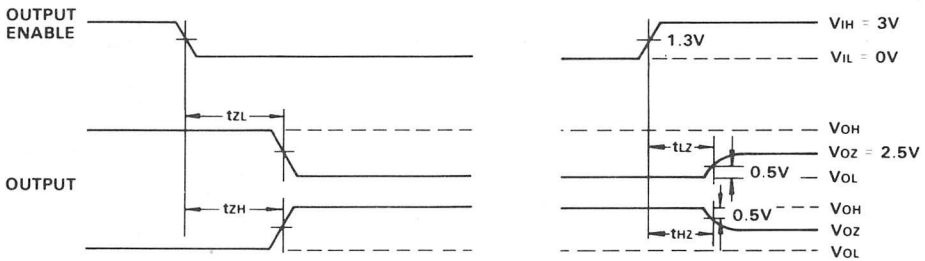


PROPAGATION DELAY TIMES



C_L includes probe and jig capacitance.
All diodes are 1N916 or 1N3064.

EQUIVALENT TEST LOAD



ENABLE, DISABLE TIMES

G74SC373
G74SC374

Microcircuits

CMOS, 3-State Octal D-Type Transparent Latches and Edge Triggered Flip-Flop Circuits

Features

- Equivalent to 74LS series
- Low power oxide isolated silicon gate CMOS technology
- Short propagation delay
- Improved noise margins
- Bus oriented 3-state outputs
- High current sink/source capability

General Description

This family of 8-bit latches feature 3-state operation and are designed for use in high speed, bus oriented systems. The G74SC373 appears transparent to data (outputs change asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, data meeting the set-up times becomes latched. G74SC374 latches hold their individual data when meeting set-up times with the clock (CK) LOW-to-HIGH transition. With both devices, $\overline{OE}$ does not affect the state of the latches, but when $\overline{OE}$ is HIGH the output is put into a high impedance state. Data may thus be latched even when the device is de-selected.

Pin Function Table

Pin	Description
D0-D7	Data Inputs
O0-O7	Non-Inverted Data Outputs
$\overline{OE}$	Output Enable
CK	Clock Input

Pin	Description
LE	Latch Enable
Vcc	Positive Supply Voltage
Vss	System Ground

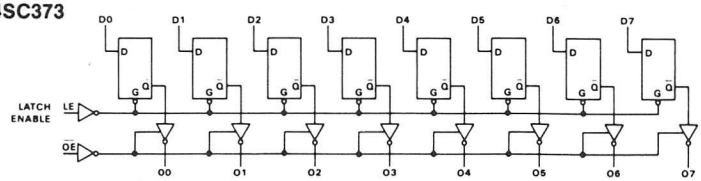
Pin Configuration

G74SC373

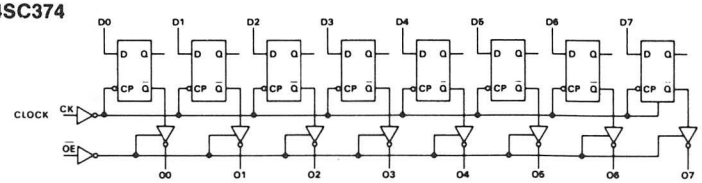
G74SC374

Logic and Connection Diagrams

G74SC373



G74SC374



Device Selection

Part Number	Format	Package	Temperature Range
G74SC373D	Transparent Latch	20-Pin Cerdip	-40° C to +85° C
G74SC373P	Transparent Latch	20-Pin Plastic	-40° C to +85° C
G74SC374D	D Type Flip-Flop	20-Pin Cerdip	-40° C to +85° C
G74SC374P	D Type Flip-Flop	20-Pin Plastic	-40° C to +85° C

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Supply Voltage	V_{CC}	-0.5V to 7.0V
Input Voltage	V_I	-0.3V to V_{CC} + 0.3V
Output Current	I_O	±75mA
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-65° C to +150° C
Package Power Dissipation	P	450 mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated values.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.
2. The arrow indicates clock/enable transition: ↑ LOW to HIGH, ↓ HIGH to LOW.
3. Max. dissipation or 1mS duration should not be exceeded.
4. All typical values at T_A = 25° C, V_{CC} = 5V.

Recommended Operating Conditions: All voltages referenced to V_{SS}.

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage		V_{CC}	3	5	6.5	V
Input Voltage		V_I	0		V_{CC}	V
Operating Free-Air Temperature		T_A	-40		+85	°C
Width of Clock/Enable Pulse		t_w	20			nS
Data Set Up Time (Note 2)	G74SC373	t_{su}	15↓			nS
	G74SC374		20↑			
Data Hold Time (Note 2)	G74SC373	t_h	15↓			nS
	G74SC374		15↑			

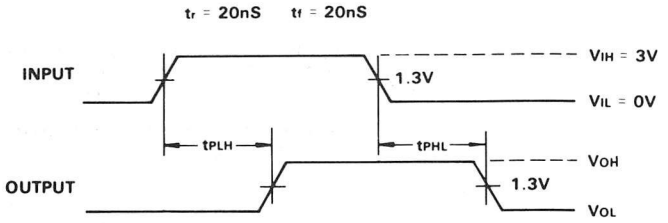
DC Characteristics: Full operating free-air temperature range unless otherwise noted. All voltages referenced to V_{SS}.

Parameter	Symbol	Min	Typ[4]	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low Level Input Voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
High Level Output Voltage	V_{OH}	2.4			V	V_{CC} = 4.75V, I_{OH} = -14mA
		4.0			V	V_{CC} = 4.75V, I_{OH} = -3mA
Low Level Output Voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 10mA
Input Current at Maximum Input Voltage	I_I			15	μA	V_{CC} = 5.25V, V_I = 5.55V
High Level Input Current Any Input	I_{IH}			10	μA	V_{CC} = 5.25V, V_I = 2.7V
Low Level Input Current	I_{IL}			-10	μA	V_{CC} = 5.25V, V_I = 0.4V
Off-State Output Current High-Level Voltage Applied	I_{OZH}			20	μA	V_{CC} = 5.25V, V_O = 2.7V
Off-State Output Current Low-Level Voltage Applied	I_{OZL}			-20	μA	V_{CC} = 5.25V, V_O = 0.4V
Short Circuit Output Current (Note 3)	I_{OS}		-40		mA	V_{CC} = 5.25V
Quiescent Supply Current	I_{CC}			0.1	mA	V_{CC} = 5.25V, Outputs Disabled

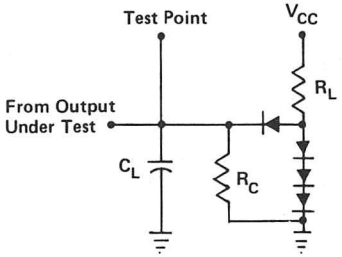
AC Characteristics: V_{CC} = 5V, T_A = 25° C.

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Propagation Delay Time Low to High Level Output	G74SC373	t_{PLH}		30	57	nS	R_L = 667 Ω, C_L = 45pF, R_C = ∞
	G74SC374			33	62		
Propagation Delay Time High to Low Level Output	G74SC373	t_{PHL}		30	56	nS	
	G74SC374			33	59		
Output Enable Time to Low Level		t_{PZL}		27	49	nS	R_L = 667 Ω, C_L = 5pF, R_C = 5K Ω
Output Enable Time to High Level		t_{PZH}		27	49	nS	
Output Disable Time from Low Level		t_{PLZ}		27	49	nS	
Output Disable Time from High Level		t_{PHZ}		40	69	nS	
Input Capacitance		C_I		8		pF	

Timing Diagrams

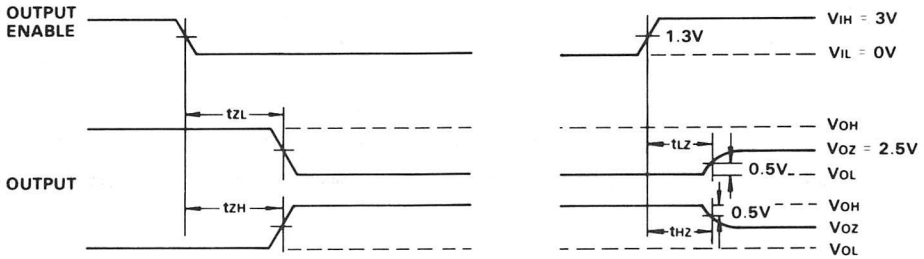


PROPAGATION DELAY TIMES



C_L includes probe and jig capacitance.
All diodes are 1N916 or 1N3064.

EQUIVALENT
TEST LOAD



ENABLE, DISABLE TIMES

LOGIC PRODUCTS

3 Communications

GTE MICROCIRCUITS

GTE Microcircuits

G8860
G8860X

Microcircuits

CMOS DTMF Decoder

Features

- 18 pin DIP package
- Central office quality detection
- Excellent voice talk-off
- Detect times down to 20mS
- Single supply 5V or 8 to 13V operation
- Latched 3 state buffered outputs
- Detects all 16 DTMF combinations
- Uses inexpensive 3.58MHz crystal
- Low power CMOS circuitry
- Adjustable acquisition & release times

Applications

Used in DTMF Receivers For:

- End to end signaling
- Control systems
- PABX
- Central office
- Mobile radio
- Key systems
- Tone to pulse converters

Description

The GTE G8860 and G8860X detects and decodes all 16 DTMF tone pairs. The device accepts the high group and low group square wave signals from a DTMF filter (G8865/G8865X) and provides a 3 state buffered 4 bit binary output. The clock signals are derived from an on chip oscillator requiring a single resistor and low cost TV crystal as external components. The G8860 and G8860X are produced using state-of-the-art CMOS technology and incorporate an on chip regulator, providing low power operation and power supply flexibility. The G8860X differs from the G8860 in that it contains an improved decode algorithm which provides enhanced talk-off performance. The G8860X also features faster and more closely-controlled response time. The G8860X may be used as a direct replacement for the G8860 in existing designs, provided consideration is given to the effect of shorter response time on system performance.

COMMUNICATIONS

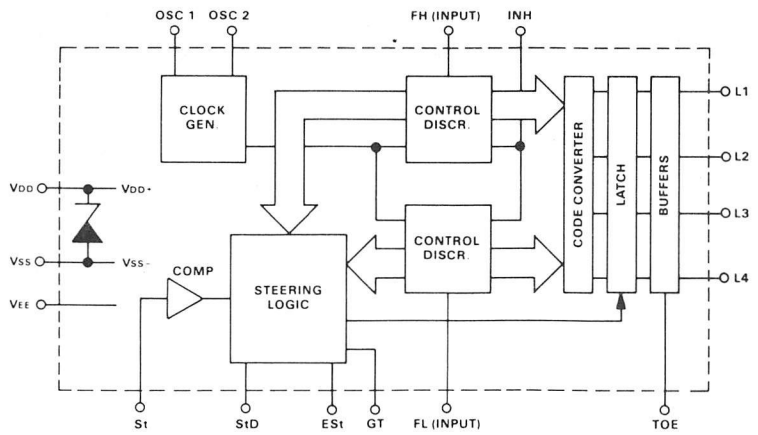
Pin Function

Pin	Description
OSC1	Clock Input
OSC2	Clock Output
IC	Internal Test Run
FH	High Freq. Group Input
L1-L4	Data Outputs

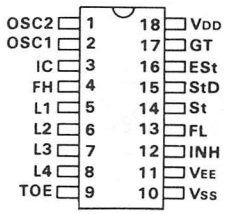
Pin	Description
TOE	Output Enable Input
INH	Inhibit Input
FL	Low Freq. Group Input
St	Steering Input
StD	Delayed Steering Output

Pin	Description
ESt	Early Steering Output
GT	Guard Time Output
V_{DD}	Positive Power Supply
V_{SS}	Internal Logic GND
V_{EE}	Neg. Supply

Block Diagram



Pin Configuration



PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
V_{DD} - V_{EE}	Vdc	15V Max.
V_{DD} - V_{SS} (Low Impedance Supply)	Vdc	5.5V Max.
Voltage on any pin except OSC1 and OSC2	Vdc	V_{EE} -0.3, V_{DD} +0.3
Voltage on OSC1 and OSC2	Vdc	V_{SS} -0.3, V_{DD} +0.3
Current on any pin except V_{DD} and V_{EE}	I_{DD}	10mA Max.
Operating temperature	T_A	-40°C to +85°C
Storage temperature	T_S	-65°C to +150°C
Power dissipation [2]	P	1000 mW Max.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

DC Characteristics: All voltages referenced to V_{EE} unless otherwise noted. V_{DD} (See Note 4), T_A = 25°C, f_C = 3.579545 MHz

Parameter	Symbol	Min	Typ [3]	Max	Unit	Test Conditions
Operating Supply Voltage	V_{DD}	4.75	5	5.25	V	Connections Fig. 2a
(V_{DD} - V_{EE})		8		13	V	Connections Fig. 2b
Internal Logic Ground Voltage	V_{DDSS}	4.75		5.25	V	Connections Fig. 2a
(V_{DD} - V_{SS})		6.0	6.5	7.5	V	I_{dd} = 7mA
Operating Supply Current	I_{DD}		1.3	4	mA	5V
			2.5	5	mA	12V, V_{DD} - V_{SS} = 5.5V
Internal Logic Ground Pin Current	I_{SS}		5.5	6.7	mA	12V, R_{SSEE} = 900 Ω
Operating Power Consumption	P_O		6.5		mW	5V
			66		mW	12V
High Level Input Voltage	V_{IH}	3.5			V	5V
(All Inputs Except OSC1)		8.5			V	12V
Low Level Input Voltage	V_{IL}			1.5	V	5V
(All Inputs Except OSC1)				3.5	V	12V
High Level Input Voltage	V_{IHO}	3.5			V	5V
OSC1		10.5			V	12V
Low Level Input Voltage	V_{ILO}			1.5	V	5V, Ref V_{SS}
OSC1				1.5	V	12V, Ref V_{SS}
Steering Input Threshold	V_{TSt}	2.04	2.27	2.5	V	5V
Voltage		5.4	6.0	6.6	V	12V
Pull Down Sink Current	I_{SI}	10	25	75	μA	5V
(INH)		10	190	400	μA	12V
Pull Up Source Current	I_{SO}	2	7	45	μA	5V + 12V
(TOE)						
Input High Leakage Current	I_{IH}		0.1	1.5	μA	5V or 12V
Input Low Leakage Current	I_{IL}		0.1	1.5	μA	
High Level Output Voltage	V_{OH}	4.9			V	5V
(All Outputs Except OSC2)		11.9			V	12V
Low Level Output Voltage	V_{OL}			0.1	V	5V
(All Outputs Except OSC2)				0.1	V	12V
High Level Output Voltage	V_{OHO}	4.9			V	5V
OSC2		11.9			V	12V

COMMUNICATIONS

DC Characteristics (Continued)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Low Level Output Voltage		V_{OL}			0.1	V	5V, Ref V_{SS}
OSC2					0.1	V	12V, Ref V_{SS}
Output Drive	P Channel	I_{OH}	0.4	0.6		mA	5V, V_{OH} = 4.6V
Current	Source		0.5	0.8		mA	12V, V_{OH} = 11.5V
(All Outputs	N Channel	I_{OL}	0.8	1.2		mA	5V, V_{OL} = 0.4V
Except OSC2)	Sink		1.0	1.6		mA	12V, V_{OL} = 0.5V
Output Drive	P Channel	I_{OH}	90	120		µA	5V, V_{OH} = 4.6V
Current	Source		90	120		µA	12V, V_{OH} = 11.5V
OSC2	N Channel	I_{OL}	100	160		µA	5V, V_{OL} = 0.5V
	Sink		100	160		µA	12V, V_{OL} = 0.5V
Tristate Output	L1-L4 = H			0.035	1.5	µA	5V, Appl V_{OL} = 0V
Current	L1-L4 = L			0.1	1.5	µA	5V, Appl V_{OH} = 5V
(High Impedance	L1-L4 = H	I_{OZ}		0.1	1.5	µA	12V, Appl V_{OL} = 0V
State)	L1-L4 = L			0.3	1.5	µA	12V, Appl V_{OH} = 12V

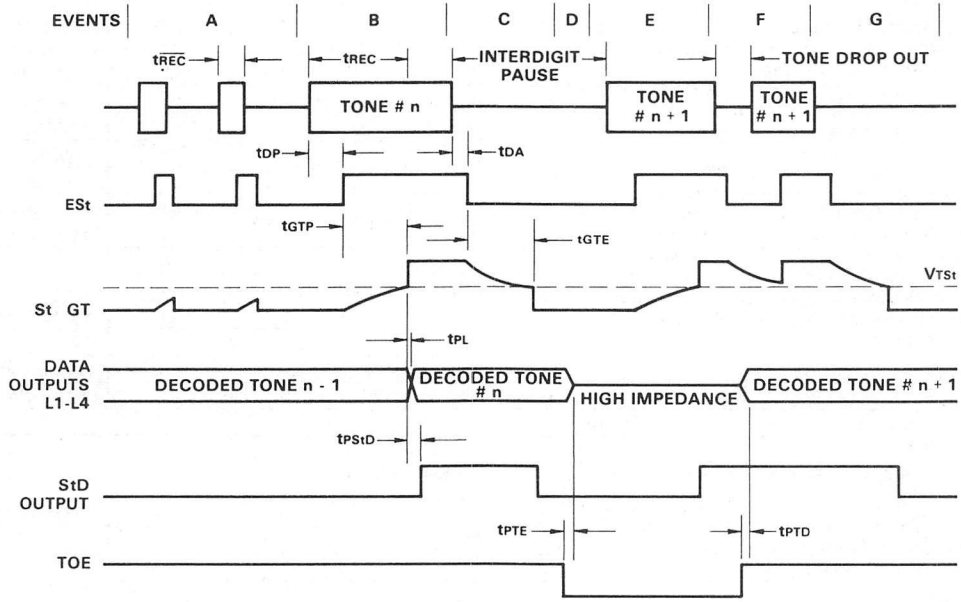
AC Characteristics: V_{DD} = 5V Unless Otherwise Noted, T_A = 25°C, f_c = 3.579545 MHz

Parameter		Symbol	Min	Typ[3]	Max	Unit	Test Conditions
Tone Frequency Deviation Accept		Δf_A			±2.5	% Nom.	
Tone Frequency Deviation Reject		Δf_R	±3.5			% Nom.	
Tone Present Detection Time (G8860)		t_{DP}	8	10	15	mS	
Tone Absent Detection Time (G8860)		t_{DA}	0.6	4	10	mS	
Tone Present Detection Time (G8860X)		t_{DP}	6		10	mS	
Tone Absent Detection Time (G8860X)		t_{DA}	0		6	mS	
Guard Time		$t_{GT(P\ or\ E)}$	Adjustable Functions of t_{GT}. See Figs. 3 and 4 and Timing Diagram				
Time to Receive = (t_{DP} + t_{GTP})		t_{REC}					
Invalid Tone Duration (f_n of t_{REC})		$\overline{t_{REC}}$					
Interdigit Pause = (t_{DA} + t_{GTA})		t_{ID}					
Acceptable Drop Out (f_n of t_{ID})		t_{DO}					
FL FH Input Transition Time		t_T			1.0	µS	10% - 90% V_{DD}
Capacitance Any Input		C		5	7.5	pF	
Propagation Delay St to L1-L4		t_{PL}		8	11	µS	5V or 12V
Propagation Delay St to StD		t_{PStD}		12	14	µS	5V or 12V
Synch. Delay L1-L4 to StD		t_{QStD}		3.43		µS	
Propagation	Enable	t_{PTE}		300		nS	5V
Delay TOE to				200		nS	12V
L1-L4	Disable	t_{PTD}		300		nS	5V
				200		nS	12V
Crystal/Clock Frequency		f_c	3.5759	3.5795	3.5831	MHz	OSC1 / OSC2
Clock	Rise Time	t_{LHCI}			110	nS	10%-90% V_{DD} - V_{SS} / Externally Applied Clock
Input	Fall Time	t_{HLCI}			110	nS	
(OSC1)	Duty Cycle	DC_{CI}	40	50	60	%	
Clock Output (OSC2)	Capacitive Load	C_{LO}			30	pF	

Notes:

1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Derate 16mW/°C above 75°C. All leads soldered to PC board.
3. All "typical" parametric information is for reference only, not guaranteed and not subject to production testing.
4. 5 V: V_{DD} - V_{EE} = 5V, V_{SS} = V_{EE} connection as Fig. 2a.
   12V: V_{DD} - V_{EE} = 12V, R_{SSEE} = 900 Ω connection as Fig. 2b.
5. Outputs are not loaded unless stated.
6. For input current parameters only V_{IH} - V_{IHO} = V_{DD}, V_{IL} = V_{EE}, V_{ILO} = V_{SS}.

Timing Diagram



EVENTS:

A) Short tone bursts: detected, tone duration is invalid.
B) Tone # n is detected, tone duration is valid, decoded to outputs.
C) End of Tone # n is detected and validated.
D) 3 stage outputs disabled (high impedance).
E) Tone # n + 1 is detected, tone duration is valid, decoded to outputs.
F) Tristate outputs are enabled. Acceptable drop out of Tone # n + 1 does not register at outputs.
G) End of Tone # n + 1 is detected and validated.

Pin Function Table

OSC2	CLOCK OUTPUT	3.58MHz crystal with parallel 5MΩ resistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
OSC1	CLOCK INPUT	
IC	Internal connection for testing only. Must be left open circuit.	
FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter.	
L1 L2 L3 L4	Data Outputs. 3 state buffered. Provides 4 bit binary word corresponding to the tone pair decoded, when enabled by TOE. See Coding Tables.	
TOE	3 state output enable input. Logic high on this input enables outputs L1-L4. Internal pull up.	
V_{SS}	Internal logic ground. For V_{DD}-V_{EE} = 5V V_{SS} connected to V_{EE}. For V_{DD}-V_{EE} > 8V, V_{SS} connected via resistor to V_{EE} see Fig. 2.	
V_{EE}	Negative power supply. External logic ground.	
INH	Inhibit input. Logic high inhibits detection of tones representing characters #, *, A, B, C, D. Internal pull down.	
FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter.	
St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs. Voltage < V_{TSt} on this pin frees the device to accept a new tone pair. See Coding Tables (c) and Functional Description.	
StD	Delayed Steering Output. Flags when a valid tone pair has been received. Presents logic high when output latch updated based on St voltage exceeding V_{TSt}. Returns to logic low when St voltage falls below V_{TSt}.	
ESt	Early Steering Output. Presents a logic high when the digital algorithm detects a recognizable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low.	
GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt. See Coding Tables (c).	
V_{DD}	Positive power supply.	

Functional Description

The GTE G8860 and G8860X are CMOS Digital DTMF detectors and decoders. Used in conjunction with a suitable DTMF filter (GTE G8865) it can detect and decode all 16 Standard DTMF tone pairs (Fig. 1), accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the G8860 must be preceded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sine wave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The High Group and Low Group rectangular waves are applied to the G8860 FH and FL inputs respectively. The G8865 DTMF Filter provides these functions.

Within the G8860 the FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators, Block Diagram—Page 1) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both High Group and Low Group signals have been simultaneously detected a flag ESt (Logic High) is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Timing Diagram) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of "tone absent" before a valid received tone is recognized as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig. 4a) is charged via resistor R from ESt when a DTMF tone pair is detected. After a period t_{GTP} Vc exceeds the St input threshold voltage V_{STt} setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (see Coding Tables) and Timing Diagram.

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents a 4 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs L1 to L4. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by Vc (Fig. 4a) falling below V_{TSt}.

Increasing the "time to receive" t_{REC} tends to further improve talk off performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal to noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTE} as shown in Fig. 4.

When L1-L4 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The G8860 may be operated from either a 5 volt or 8 to 13 volt supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig. 2. When using the G8860 with the G8865 DTMF Filter it is only necessary to use the G8865 crystal oscillator (see Fig. 3). When using the higher supply voltage range the G8865 OSC2 output should be capacitively coupled to the G8860 OSC1 input as shown in Fig. 3.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves talk off due to the reduced number of detectable tones.

Coding Tables

A. Output Coding

Original Tone Character		TOE	L4	L3	L2	L1
	X	L	Z	Z	Z	Z
	1	H	L	L	L	H
	2	H	L	L	H	L
	3	H	L	L	H	H
	4	H	L	H	L	L
DR	5	H	L	H	L	H
	6	H	L	H	H	L
	7	H	L	H	H	H
	8	H	H	L	L	L
	9	H	H	L	L	H
	0	H	H	L	H	L
	*	H	H	L	H	H
	#	H	H	H	L	L
D	A	H	H	H	L	H
	B	H	H	H	H	L
	C	H	H	H	H	H
	D	H	L	L	L	L

B. Inhibit Function

Detected Character	INH	ESt
None	0	L
X	L	H
DR	H	H
D	H	L

C. Steering

ESt	St	GT	StD(1)
L	L	L	L
H	L	Z	L
L	H	Z	H
H	H	H	H

Notes:
1. Delayed WRT St.
2. For the purpose of these tables consider:
   $V_{St} < V_{TSt}$ LOGIC LOW (L)
   $V_{St} > V_{TSt}$ LOGIC HIGH (H)

H = LOGIC HIGH
L = LOGIC LOW
O = "DON'T CARE" LOGIC HIGH OR LOW
Z = HIGH IMPEDANCE
X = ANY CHARACTER

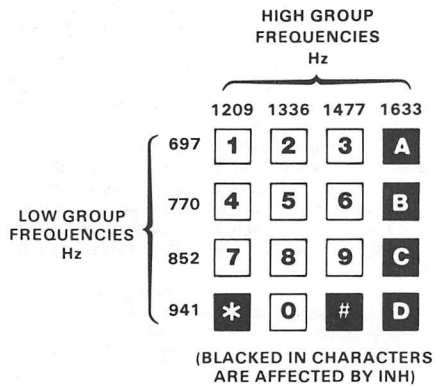


Fig. 1 DTMF Matrix Indicating Character—Tone Pair Correspondence.

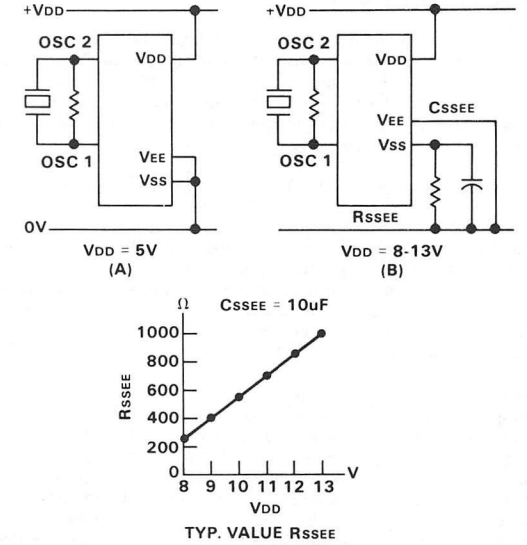
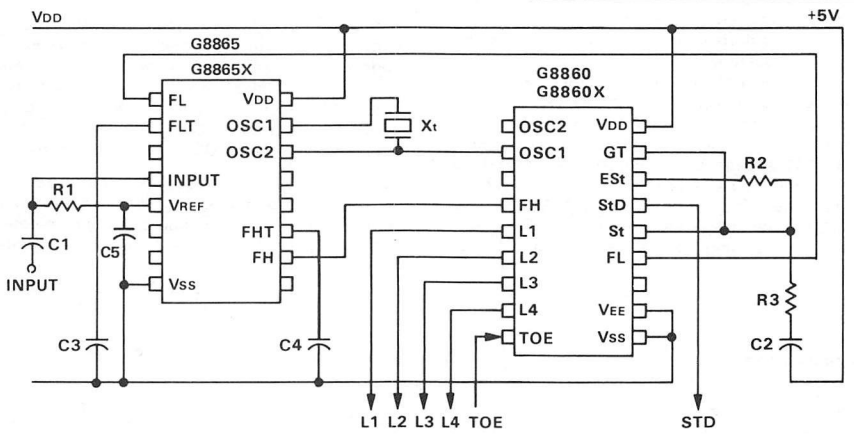
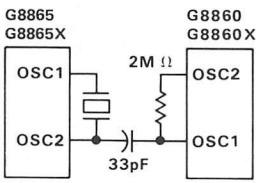


Fig. 2 Power Supply Connection Options





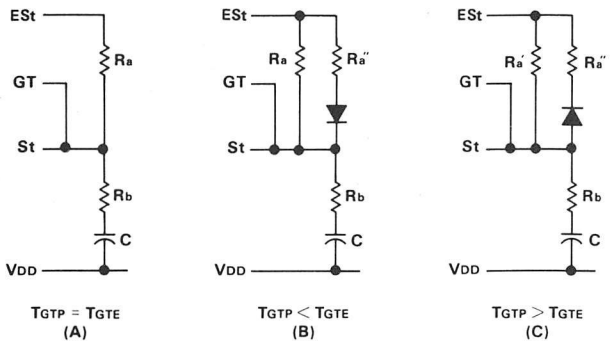
R1 = 2.0M Ω C2 = 0.1 μF
R2 = 300K Ω C3 = C4 = 680pF
R3 = 5K Ω Xt = 3.579MHz
C1 = 10nF
C5 = .3 μF

Note: For operation with VDD - VEE > 5.25V connect with power supply connections as Fig. 2B.

TYPICAL PERFORMANCE

Dynamic Range	30dB
Twist	±10dB
Acc. S/N Ratio	14dB
TREC (G8860)	28 to 35mS
TREC (G8860X)	26 to 30mS
Guard Time	20mS
Max. Invalid Tone Duration	20mS
Min. Interdigit Pause	30mS
Max. Acceptable Dropout	20mS

Fig. 3 Connection Diagram for Single Ended Input Receiver Using the G8865 (5V Operation)



$$T_{GTP} = C(R_a + R_b)\ \text{LOGn}\ \left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{DD} - V_{TSt}}\right)$$

$$T_{GTE} = C(R_a + R_b)\ \text{LOGn}\ \left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{TSt}}\right)$$

FOR V_{OHESt}, V_{OLESt} Symetric About $V_{TSt} = \frac{1}{2} V_{DD}$
WITH $R_b < 0.1\ R_a$ $\qquad R_b \geq V_{DD} - V_{EE}\ K\ \Omega$

$$R_b < 0.1\left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$$

A) $T_{GTP} = T_{GTE} \triangleq 0.69\ R_a\ C\left(1 - \frac{R_b}{2\ R_a}\right)$

B) T_{GTP} } $\triangleq 0.69\ C\left(\frac{R_a' R_a''}{R_a + R_a''}\right)$
C) T_{GTE} }

B) T_{GTE} }
C) T_{GTE} } $\triangleq 0.69\ R_a'\ C$

Fig. 4 Guard Time Adjustment

G8865X

Microcircuits

CMOS DTMF Filter

Features

- Provides DTMF high and low group filtering
- Hard limiting on filter outputs
- 6-pole band-pass high and low group filters
- 40 dB (typ) intergroup attenuation
- Dial tone suppression
- Single supply operation, +5V to +12V
- Logical power down
- Uses inexpensive 3.58 MHz crystal
- Wide dynamic 30dB range

Applications

Used in DTMF Receivers For:

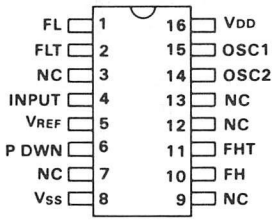
- End-to-end signaling
- Control systems
- PABX
- Central office
- Mobile radio
- Key systems
- Tone-to-pulse converters

General Description

The GTE G8865X contains both high group and low group filtering and comparator functions required to implement a dual tone multi-frequency (DTMF) tone receiver using a DTMF digital decoder (i.e. GTE G8860/G8860X). Switched capacitor techniques are used to implement the filters. The device is fabricated using the GTE high density ISO-CMOS technology. The filter clocks are derived from an on-chip oscillator requiring only a low cost TV crystal as an external component. The G8865X offers single supply operation over a wide supply voltage range and incorporates a logical power down facility.

COMMUNI-CATIONS

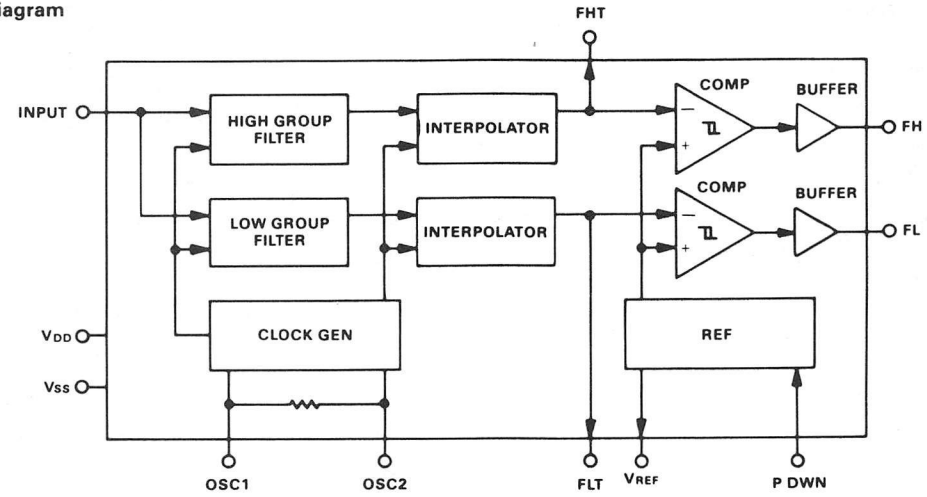
Pin Configuration



Pin Function

Pin	Description	Pin	Description
FL	Low group limiter output	OSC2	Clock Output
FLT	Low group test output	OSC1	Clock input
INPUT	Tone signal input	VDD	Positive power supply
P DWN	Power down function	VSS	Negative power supply
FH	High group limiter output	VREF	Internal reference
FHT	High group test output		

Block Diagram



PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
V_{DD}-V_{SS}	Vdc	15V Max.
Voltage on Any Pin	Vdc	V_{SS} -0.3, V_{DD} +0.3
Current on Any Pin	I_{DD}	10 mA Max.
Operating Temperature (D/P Package)	T_A	-40°C to +85°C
Storage Temperature (D Package)	T_S	-65°C to +150°C
Storage Temperature (P Package)	T_S	-65°C to +125°C
Power Dissipation (D Package) (2)	P	850 mW Max.
Power Dissipation (P Package) (3)	P	400 mW Max.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated values.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied..
2. Derate 16mW/°C above 75°C. All leads soldered to PC board.
3. Derate 6.3mW/°C above 25°C. All leads soldered to PC board.

DC Characteristics: All voltages referenced to V_{SS} unless otherwise noted, T_A = 25°C, f_c = 3.579545 MHz

Parameter			Symbol	V_{DD} = 5V			V_{DD} = 12V			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
Operating Supply Voltage			V_{DD}	4.75					13	V		
Operating Supply Current			I_{DD}		1.2	2.5		5	7.5	mA	PDWN = V_{SS}	
Standby Supply Current			I_{DDS}		100			300		μA	PDWN = V_{DD}	
Operating Power Consumption			P_O		6	12.5		60	90	mW	PDWN = V_{SS}	Fig. 4(c)
Standby Power Consumption			P_S		0.5			1.5		mW	PDWN = V_{DD}	C = 15pF
Low Level Input Voltage		PDWN & OSC1	V_{IL}			1.5			3.5	V		
High Level Input Voltage			V_{IH}	3.5			8.5			V		
Pull Down Sink Current		PDWN	I_{IH}		3	6		12	24	μA		
Input Current		OSC1	I_I		±2.5			±6		μA		
Low Level Output Voltage		FL, FH	V_{OL}			0.1			0.1	V	No load	
High Level Output Voltage		OSC2	V_{OH}	4.9			11.9			V		
Output Drive Current	N Channel Sink	FL, FH	I_{OL}	0.2			0.5			mA	V_{OL} = 0.4V (5V)	
		OSC2		0.1			0.25			mA	V_{OL} = 1.2V (12V)	
	P Channel Source	FL, FH	I_{OH}	0.2			0.5			mA	V_{OH} = 4.6V (5V)	
		OSC2		0.1			0.25			mA	V_{OH} = 10.8V (12V)	
Output Voltage		V_{REF}	V_{REF}	2.3		2.6	5.4		6.2	V	No Load	
Output Resistance			R_{OR}			16			8	kΩ		

AC Characteristics: V_{DD} = 4.75 to 13V, T_A = 25°C, f_c = 3.579545 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions	
Dynamic Range			30		36	dB		
Valid Input Signal Levels (Each tone of composite signal)					$V_{DD}/2$	V_{PP}		
			27.9		883	mVrms	V_{DD} = 5V	
			67.0		2120	mVrms	V_{DD} = 12V	
Input Impedance		Z_I	10			MΩ		
Passband Ripple		A_V		±0.3	±1.0	dB		
Low Group 1dB Bandwidth	Lower Limit	f_{LL}		670	684	Hz		
	Upper Limit	f_{LU}	958	990		Hz		
High Group 1dB Bandwidth	Lower Limit	f_{HL}		1162	1188	Hz		
	Upper Limit	f_{HU}	1660	1740		Hz		
Intergroup Rejection	Low Group with High Tone	IR_{L1209}	34	45		dB	1209Hz	w.r.t. 770Hz
		IR_{L1477}	36	40		dB	1477Hz	
	High Group with Low Tone	IR_{H941}	38	50		dB	941Hz	w.r.t. 1336Hz
		IR_{H770}	36	40		dB	770Hz	
Dial Tone Rejection	Low Group	DR_{L440}	40	60		dB	440Hz	w.r.t. 770Hz
		DR_{L350}	28	30		dB	350Hz	
	High Group	DR_{H440}	52	60		dB	440Hz	w.r.t. 1336Hz
		DR_{H350}	50	55		dB	350Hz	

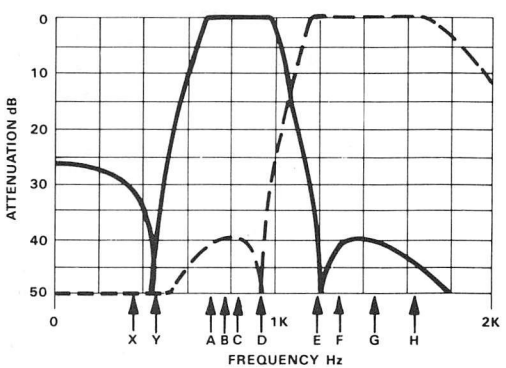
COMMUNICATIONS

AC Characteristics (cont.)

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions	
FHT FLT Maximum Permissible Load		RLFT	250			K Ω		
		CLFT			1000	pF		
Output Rise Time	FL, FH	tTLHO		90	150	nS	10% to	
Output Fall Time		tTHLO		60	100	nS	90% VDD	
Crystal/Clock Freq.	OSC1, OSC2	fc	3.5759	3.5795	3.5831	MHz		
Clock	Rise Time	tLHCI			110	nS	10% to	Externally
Input	Fall Time	tHLCI			110		90% VDD	Applied
(OSC 1)	Duty Cycle	DCCI	40	50	60	%		Clock
Clock Output OSC 2	Capacitive Load	CLOC			30	pF	Unbalanced load see Fig. 4	
Capacitance Any Input		CI		5	7.5	pF		

Pin Function Table

Name	Pin No.	Description
FL	1	Low group limiter output.
FLT	2	Test output. Monitors low group filter output. Decouple to Vss with 680 pF capacitor.
NC	3	Not connected.
INPUT	4	Tone signal input (single ended).
VREF	5	Internal reference, can be used to bias input via 2M Ω resistor and a 0.3 μF capacitor.
PDWN	6	Power down active high. Internal pull down transistor. A high level signal powers down the device and inhibits the oscillator.
NC	7	Not connected.
Vss	8	Negative (0V) power supply.
NC	9	Not connected.
FH	10	High group limiter output.
FHT	11	Test output. Monitors high group filter output. Decouple to Vss with 680pF capacitor.
NC	12	Not connected.
NC	13	Not connected.
OSC2	14	Clock Output. 3.5795 MHz crystal connected between these
OSC1	15	Clock Input. pins completes internal oscillator.
VDD	16	Positive power supply.



PRECISE DIAL TONES

X 350Hz
Y 440Hz

DTMF TONES

A = 697Hz
B = 770Hz
C = 852Hz
D = 941Hz
E = 1209Hz
F = 1336Hz
G = 1477Hz
H = 1633Hz

Fig. 1 Typical Filter Characteristics

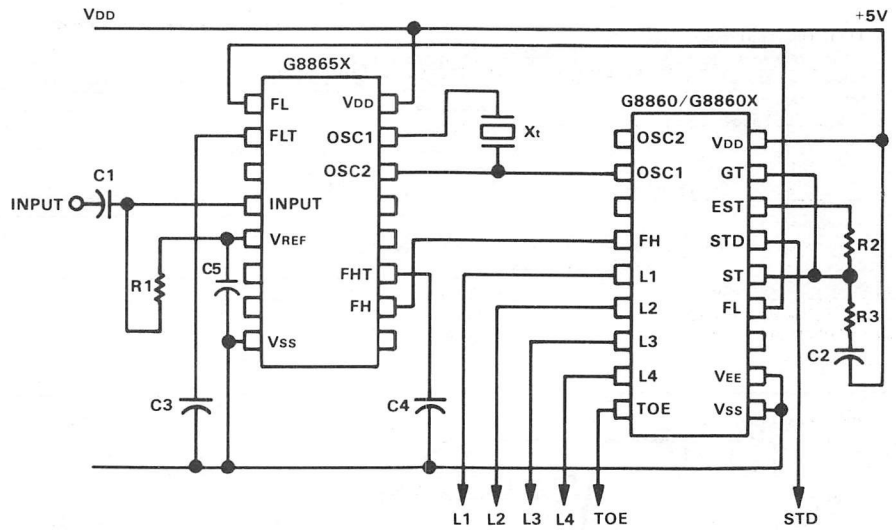
Functional Description

The G8865X separates high group and low group components of the dual tone signal, limits the resulting pair of sine waves, produces square waves having the same frequencies as the individual input tones. These limited low group and high group tones appear at the FL and FH outputs respectively. To implement a complete DTMF receiver, the FL and FH outputs are connected to the FL and FH inputs of the G8860/G8860X DTMF decoder. See Fig. 2.

Separation of the low group and high group tones is achieved by applying the dual tone signal simultaneously to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low group and high group tones. The frequency characteristic of each filter (see Fig. 1) also incorporates a notch at 440Hz to provide dial tone rejection. Each filter output is followed by a single order switched capacitor section which operates as an interpolator smoothing the signals prior to limiting. The limiting functions are performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals and noise. The comparator outputs are buffered to drive the FL and FH output pins and detector device inputs. The G8865X has a single ended input allowing connection either to a PCM decoder, radio receiver (Fig. 2) or via a differential buffer to a telephone line (Fig. 3). The signal input (Pin 4) should be biased at $V_{DD}/2$. With the input capacitively coupled, this is achieved by connecting the signal input to V_{REF} (Pin 5) via a 2MΩ resistor.

FLT and FHT allow the filter outputs to be monitored prior to limiting, and should each be decoupled to V_{SS} by 680 pF capacitors.

Presenting a high unbalanced capacitive load to the oscillator crystal can cause attenuation of the oscillator output signal and increased supply current (see Fig. 4). Where the 8865X oscillator is required to drive a high capacitive load such as a number of other 8865X/8860s it is desirable to connect a capacitor between OSC1 and V_{SS}. The value of this capacitor being equal to the capacitive loading at OSC2.



R1 = 2.0MΩ
R2 = 300KΩ
R3 = 5KΩ
C1 = 10nF
C2 = 0.1μF
C3 = 680pF
C4 = 680pF
C5 = 0.3μF
Xt = 3.5795MHz

Notes:
1. For device power supply > 5.25V See G8860 data sheet

TYPICAL PERFORMANCE

Dynamic Range	30dB
Twist	±10dB
ACC. S/N Ratio	14dB
T_{REC} (G8860)	28 to 35mS
T_{REC} (G8860X)	26 to 30mS
Guard Time	20mS
Max. Invalid Tone Duration	20mS
Min. Interdigit Pause	30mS
Max. Acceptable Dropout	20mS

Fig. 2 Connection Diagram for Single Ended Input Receiver Using the G8860/G8860X (5V Operation)

DIFFERENTIAL INPUT AMPLIFIER

$C_1 = C_2$

$R_4 = R_1$

$R_3 = \frac{R_2 R_5}{R_2 + R_5}$

VOLTAGE GAIN

$(A_{V\,diff}) = \frac{R_5}{R_1}$

INPUT IMPEDANCE

$(Z_{indiff}) = 2\sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$

TYPICAL VALUES

C1, C2 = 10nF
C3, C4 = 680pF
R1, R4 = 200KΩ
R2 = 60KΩ
R3 = 37.5KΩ
R5 = 100KΩ
R6 = 1MΩ
Av = –6 dB
Zindiff ≃ 400 KΩ (@650 Hz)

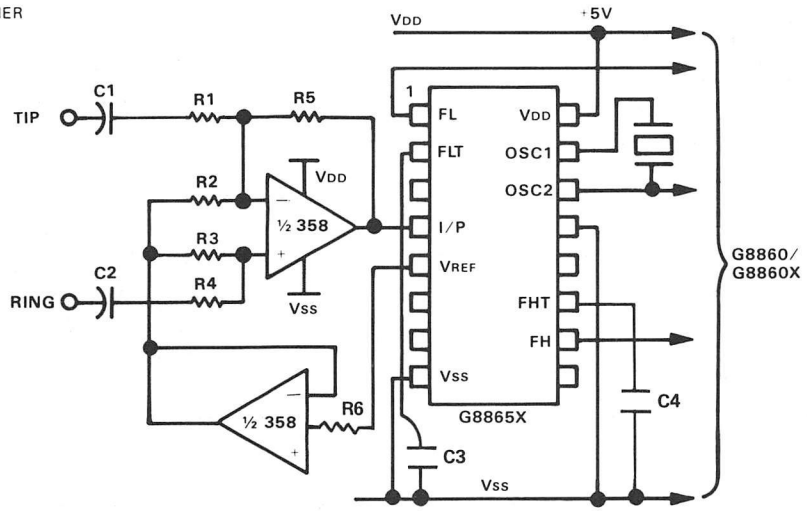
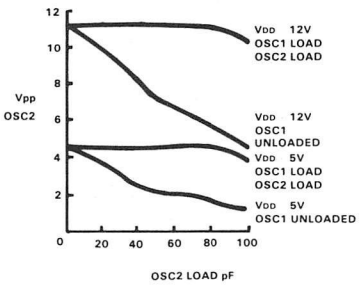
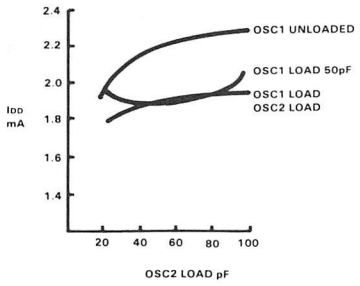


Fig. 3 Circuit for Connection to a Telephone Line

(A) 8865X OSC2 PEAK-PEAK OUTPUT VOLTAGE VARIATION WITH CAPACITIVE LOADING



(B) 8865X IDD CURRENT VARIATION WIH OSC2 CAPACITIVE LOADING



(C)

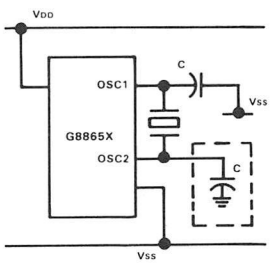


Fig. 4 Crystal Oscillator Loading

COMMUNICATIONS

G8870A

Microcircuits

CMOS DTMF Integrated Receiver

Features

- CMOS technology for low power consumption—35 mW max.
- Full DTMF receiver in a single 18-pin package
- Provides DTMF high and low group filtering
- Adjustable acquisition and release times
- Dial tone suppression
- Integrated bandsplit filter and digital decoder functions
- On-chip differential amplifier, clock oscillator, and latched three-state bus.
- Uses inexpensive 3.58 MHz crystal
- Central office quality and performance
- Single +5 volt power supply

Applications

- PABX
- Central office
- Key systems
- Mobile radio
- Remote control
- Remote data entry

General Description

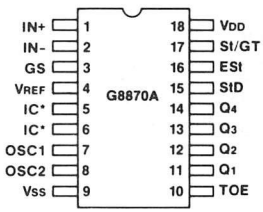
The GTE G8870A provides full DTMF receiver capability by integrating both the bandsplit filter and digital decoder functions into a single 18-pin chip. The G8870A is manufactured using state-of-the-art CMOS process technology for low power consumption (35 mW max.) and precise data handling. The filter section uses a switched capacitor technique for both high and low group filters and dial tone rejection. The G8870A decoder uses digital counting techniques for the detection and decoding of all 16 DTMF tone pairs into a 4-bit code. The G8870A minimizes external component count by providing an on-chip differential input amplifier, clock generator, and a latched three-state interface bus. The on-chip clock generator requires only a low cost TV crystal as an external component.

Pin Function

Pin	Description
IN+	Non-Inverting Input
IN-	Inverting Input
GS	Gain Select
IC	Internal Connection
OSC1	Clock Input
OSC2	Clock Output
TOE	Three-State Output Enable

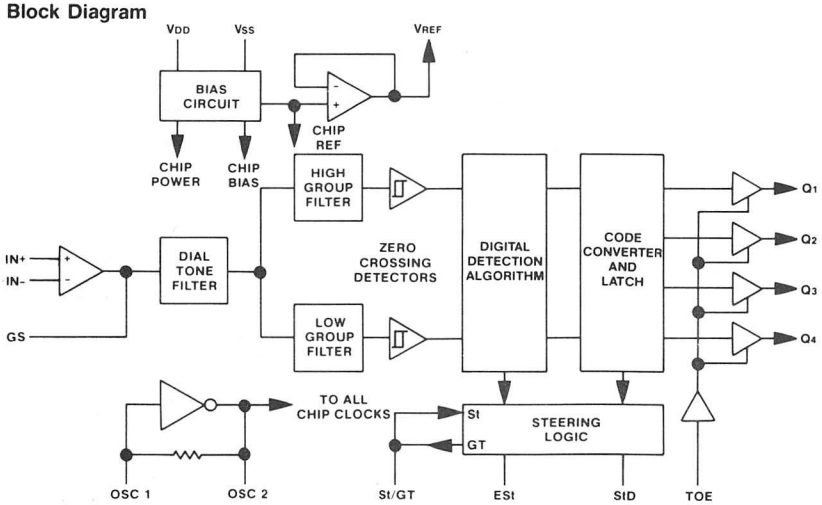
Pin	Description
Q_{1-4}	Three-State Data Outputs
StD	Delayed Steering Output
ESt	Early Steering Output
St/GT	Steering Input/Guard Time Input
V_{REF}	Reference Voltage Output
V_{SS}	Negative Power Supply
V_{DD}	Positive Power Supply

Pin Configuration



*CONNECT TO V_{SS}

Block Diagram



ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Power Supply Voltage (V_{DD}-V_{SS})	V_{DD}	6.0V Max
Voltage on any Pin	V_{dc}	V_{SS}-0.3, V_{DD}+0.3
Current on any Pin	I_{DD}	10 mA Max
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-65° C to +150° C
Power Dissipation (Note 2)	P	1000 mW Max

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.
2. Derate above 75° C at 16 mW/° C. All leads soldered to board.

DC Characteristics: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25° C.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Operating Supply Voltage	V_{DD}	4.75		5.25	V	
Operating Supply Current	I_{DD}		3.0	7.0	mA	
Power Consumption	P_O		15	35	mW	f = 3.579 MHz; V_{DD} = 5.0V
Low Level Input Voltage	V_{IL}			1.5	V	
High Level Input Voltage	V_{IH}	3.5			V	
Input Leakage Current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
Pull Up (Source) Current	I_{SO}		7.5	15.0	mA	TOE (Pin 10) = 0 V
Input Impedance, Signal Inputs 1,2	R_{IN}		10		Meg Ω	@ 1KHz
Steering Threshold Voltage	V_{Tst}	2.2	2.35	2.5	V	
Low Level Output Voltage	V_{OL}		0.03		V	No Load
High Level Output Voltage	V_{OH}		4.97		V	No Load
Output Low (Sink) Current	I_{OL}	1.0	2.5		mA	V_{OUT} = 0.4 V
Output High (Source) Current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6 V
Output Voltage (VREF)	V_{REF}	2.4		2.7	V	No Load
Output Resistance (VREF)	R_{OR}		10		KΩ	

Operating Characteristics: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25° C.

Gain Setting Amplifier

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Leakage Current	I_{IN}		±100		nA	$V_{SS} < V_{IN} < V_{DD}$
Input Resistance	R_{IN}		10		MΩ	
Input Offset Voltage	V_{os}		±25		mV	
Power Supply Rejection	PSRR		60		dB	1KHz
Common Mode Rejection	CMRR		60		dB	-3.0 V < V_{IN} < 3.0V
DC Open Loop Voltage Gain	A_{VOL}		65		dB	
Open Loop Unity Gain Bandwidth	fc		1.5		MHz	
Output Voltage Swing	V_O		4.5		V_{p-p}	$R_L \geq$ 100KΩ to V_{SS}
Tolerable Capacitive Load (GS)	C_L		100		pF	
Tolerable Resistive Load (GS)	R_L		50		KΩ	
Common Mode Range	V_{cm}		3.0		V_{p-p}	No Load

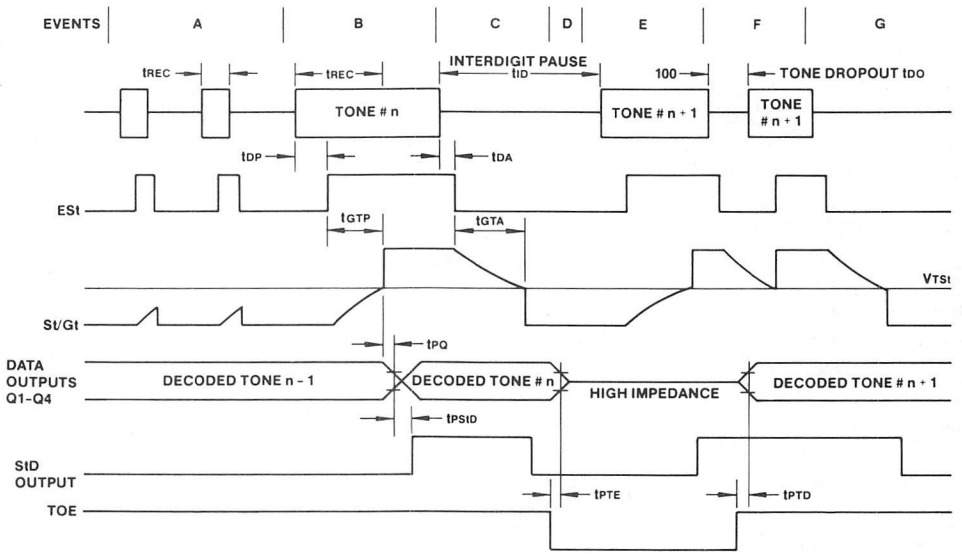
AC Characteristics: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25° C, f_{CLK} = 3.579545 MHz using test circuit (Fig. 1).

Parameter			Symbol	Min	Typ	Max	Units	Notes
Valid Input Signal Levels (each tone of composite signal)	MIN					-29	dBm	1,2,3,4,5,8
						27.5	mV_{RMS}	
	MAX			1			dBm	1,2,3,4,5,8
				883			mV_{RMS}	
Twist Accept Limit		Positive			10		dB	2,3,4,8
		Negative			10		dB	
Freq. Deviation Accept Limit						1.5%±2Hz	Nom.	2,3,5,8,10
Freq. Deviation Reject Limit				±3.5%			Nom.	2,3,5
Third Tone Tolerance					-16		dB	2,3,4,5,8,9
Noise Tolerance					-12		dB	2,3,4,5,6,8,9
Dial Tone Tolerance					+ 18		dB	2,3,4,5,7,8,9
Tone Present Detection Time			t_{DP}	6	11	14	mS	Refer to Timing Diagram
Tone Absent Detection Time			t_{DA}	1	4	8	mS	
Tone Duration Accept			t_{REC}			40	mS	(User Adjustable) Times shown are obtained with circuit in Fig. 1
Interdigit Pause Accept			t_{ID}			40	mS	
Propagation Delay (St to Q)			t_{PQ}		8	11	µS	TOE = V_{DD}
Propagation Delay (St to StD			t_{PStD}		12		µS	
Output Data Set Up (Q to Std)			t_{QStD}		3.4		µS	
Propagation Delay (TOE to Q)		Enable	t_{PTE}		50		nS	R_L = 10KΩ
		Disable	t_{PTD}		300		nS	C_L = 50pF
Crystal/Clock Frequency			f_{CLK}	3.5759	3.5795	3.581	MHz	
Clock Output (OSC2)	Capacitive Load		C_{LO}			30	pF	

NOTES to AC Characteristics

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3 KHz) Gausian Noise.
7. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2%.
8. For an error rate of better than 1 in 10,000.
9. Referenced to lowest level frequency component in DTMF signal.
10. Minimum signal acceptance level is measured with specified maximum frequency deviation.

Timing Diagram



A. Short tone bursts detected. Tone duration is invalid.
B. Tone # n is detected. Tone duration is valid. Decoded to outputs.
C. End of tone # n is detected and validated.
D. Three-State Outputs Disabled (High Impedance).
E. Tone # n + 1 is detected. Tone duration is valid. Decoded to outputs.
F. Three-state outputs are enabled. Acceptable drop out of tone # n + 1 does not register at ouputs.
G. End of tone # n + 1 is detected and validated.

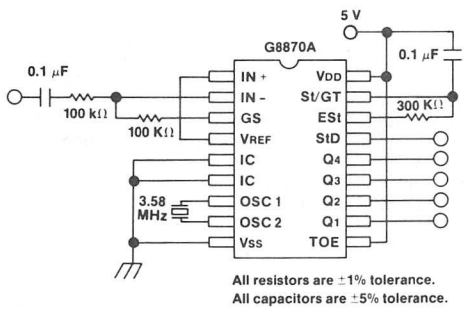


Figure 1. Single Ended Input Configuration

FLOW	FHIGH	KEY	TOE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
—	—	ANY	L	Z	Z	Z	Z
L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE							

Figure 2. Functional Decode Table

Pin Function Table

Pin	Name	Description	
1	IN+	Non-inverting input	Connections to the front-end differential amplifier
2	IN−	Inverting input	
3	GS	Gain Select. Gives access to output of front-end differential amplifier for connection of feedback resistor.	
4	V_{REF}	Reference voltage output (nominally $V_{DD}/2$). May be used to bias the inputs at mid-rail.	
5	IC	Internal connection. Must be tied to V_{SS}.	
6	IC	Internal connection. Must be tied to V_{SS}.	
7	OSC1	Clock input	3.579545 MHz crystal connected between these pins completes internal oscillator.
8	OSC2	Clock output	
9	V_{SS}	Negative power supply (Normally connected to 0V).	
10	TOE	Three-state output enable (input). Logic high enables the outputs Q_1–Q_4. Internal pull-up.	
11	Q_1	Three-state outputs. When enabled by TOE, provides the code corresponding to the last valid tone pair received. (See Fig. 2.)	
12	Q_2		
13	Q_3		
14	Q_4		
15	StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below V_{TSt}.	
16	ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.	
17	St/GT	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant, and its state is a function of ESt and the voltage on St. (See Fig. 2.)	
18	V_{DD}	Positive power supply	

COMMUNICATIONS

Functional Description

The GTE G8870A DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin package configuration. The G8870A's internal architecture consists of a bandsplit filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The G8870A decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period (t_{GTF}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch.

At this point, the GT output is activated and drives Vc to VDD. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{GTP} \simeq 0.67\ RC$$

The value of tDP is a parameter of the device and tREC is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a tREC of 40 milliseconds would be 300K.

A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard-times for tone-present (tGTP) and tone-absent (tGTA). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing tREC improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short tREC with a long tDO would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

Input Configuration

The input arrangement of the G8870A provides a differential input operational amplifier as well as a bias source (VREF) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1 with the op-amp connected for unity gain and VREF biasing the input at ½VDD. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor RS.

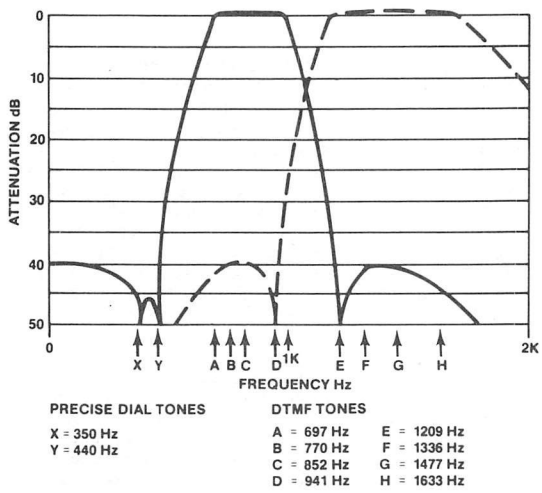


Figure 3. Typical Filter Characteristic

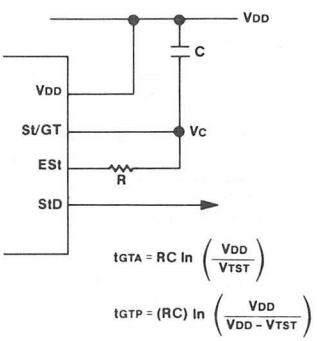
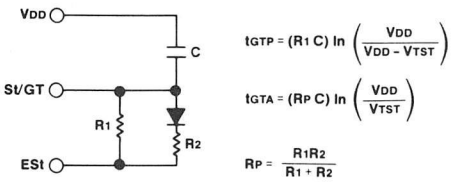
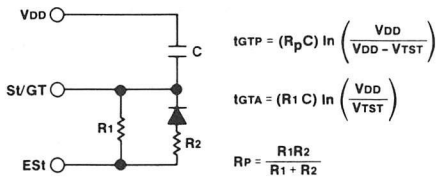


Figure 4. Basic Steering Circuit

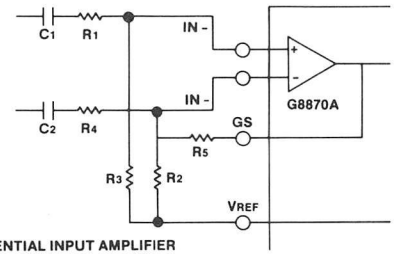


a) Decreasing t_{GTA} ($t_{GTP} > t_{GTA}$)



b) Decreasing t_{GTP} ($t_{GTP} < t_{GTA}$)

Figure 5. Guard Time Adjustment



DIFFERENTIAL INPUT AMPLIFIER

$C_1 = C_2 = 10$ nF

$R_1 = R_4 = R_5 = 100$ KΩ

$R_2 = 60$ KΩ, $R_3 = 37.5$ KΩ

$$R_3 = \frac{R_2R_5}{R_2 - R_5}$$

$$\text{VOLTAGE GAIN (Av diff)} = \frac{R_2}{R_1}$$

INPUT IMPEDANCE

$$(Z_{INDIFF}) = 2\sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$$

All resistors are — 1% tolerance.
All capacitors are — 5% tolerance.

Figure 6. Differential Input Configuration

COMMUNICATIONS

G8912B

Microcircuits

CMOS PCM Transmit/Receive Filters

Features

- Monolithic device includes both transmit and receive filters
- Compatible with Bell D3/D4 and CCITT G.712
- Transmit filter rejects 50/60Hz
- Receive filter includes Sin x/x correction
- External gain adjustment of both transmit and receive filters
- Direct interface with transformer or electronic 2-to-4 wire converters
- Low power consumption:
  20mW typical without power amps
  30mW typical with power amps
  0.4mW typical standby
- Anti-aliasing pre-filters on both transmit and receive filters
- Pin-for-pin compatible with Intel 2912

General Description

The GTE G8912B is a monolithic device containing both receive and transmit filters required for the analog termination of a PCM line or trunk. The transmit filter performs the 50/60 Hz power line frequency rejection and the antialiasing function needed for an 8KHz sampling system. The receive filter has a pre-filter to eliminate aliasable codec noise, a low pass transfer characteristic and provides the Sin x/x correction required after D/A signal conversion by a suitable codec.

The G8912B is fabricated using GTE double-poly CMOS technology. Switched capacitors are used for the filter design. The G8912B interfaces directly with an electronic or transformer 2-to-4 wire converter. When interfacing with an electronic converter, the on-chip power amplifiers may be deactivated, thus reducing power dissipation.

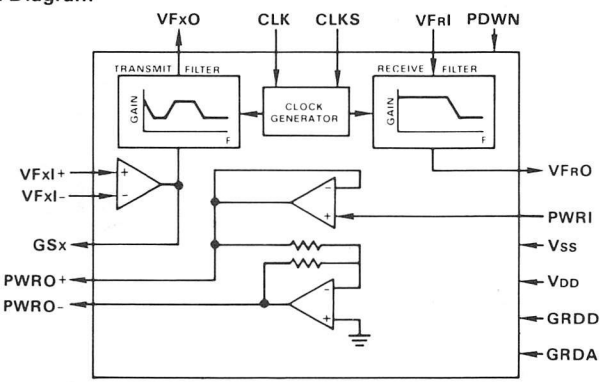
COMMUNICATIONS

Pin Function Table

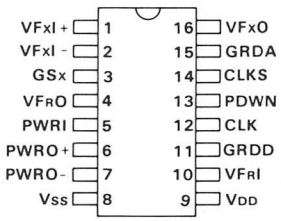
Pin	Description
VFxI+	Analog Input to Xmit Filter
VFxI–	Inverting Analog Input
GSx	Op Amp Output
VFRO	Analog Output From Receive Filter
PWRI	Pwr Amp Input
PWRO+ PWRO–	Pwr Amp Outputs
VSS	Neg Supply Voltage (–5V)

Pin	Description
VDD	Pos Supply Voltage (+5V)
VFRI	Analog Input to Receive Filter
GRDD	Digital Ground
CLK	Clock Input
PDWN	Standby Control
CLKS	Clock Freq. Select
GRDA	Analog Ground
VFXO	Analog Output From Xmit Filter

Block Diagram



Pin Configuration



PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
V_{DD} With Respect to V_{SS}	Vdc	-0.3V to +14V
Input/Output Voltages With Respect to V_{SS}	Vdc	-0.3V to V_{DD}
All Output Currents	I_{DD}/I_{SS}	±50 mA
Operating Temperature	T_A	-40°C to +85°C
Storage Temperature	Ts	-65°C to +150°C
Power Dissipation at 25°C (Note 2)	P	850 mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated values.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.
2. Derate 16 mW/°C above 75°C. All leads soldered to PC board.

DC and Operating Characteristics: GRDA = GRDD = OV unless otherwise noted, V_{DD} = +5V, V_{SS} = -5V, T_A = 0°C to 70°C

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Operating Supply Voltages	V_{SS}	-5.25	-5	-4.75	V	Ref. to GRDA
	V_{DD}	4.75	5	5.25	V	
V_{DD} Standby Current	I_{DDO}		40	100	μA	PDWN = V_{DD}
V_{SS} Standby Current	I_{SSO}		10	100	μA	
V_{DD} Operating Current	I_{DD1}		2.0	3.0	mA	PWRI = V_{SS}
V_{SS} Operating Current	I_{SS1}		2.0	3.0	mA	Power Amps Inactive
V_{DD2} Operating Current	I_{DD2}		3.0	5.0	mA	With Power Amps
V_{SS2} Operating Current	I_{SS2}		3.0	5.0	mA	(Outputs Unloaded)
Input Load Current, CLK	I_{LIC}	-10	1	+10	μA	V_{IN} = 0 to V_{DD}
Input Load Current, CLKS	I_{LIS}	-10	1	+10	μA	V_{IN} = V_{SS} to V_{DD}
Input Load Current, PDWN	I_{LIP}	-100	-1	+100	μA	V_{IN} = 0 to V_{DD}
Input Low Voltage, CLK, PDWN	V_{IL}	0		0.8	V	
Input Low Voltage, CLKS	V_{ILS}	V_{SS}		V_{SS} + 0.5	V	
Input High Voltage, CLK, PDWN	V_{IH}	2.2		V_{DD}	V	
Input High Voltage, CLKS	V_{IHS}	V_{DD} -0.5		V_{DD}	V	
Input Intermediate Voltage, CLKS	V_{IIS}	-1.0		1.0	V	

Transmit Filter Gain Setting Amplifier

Input Leakage Current, VFxI +, VFxI-	I_{BXI}	-100		100	nA	$V_{SS} < V_{IN} < V_{DD}$
Input Resistance, VFxI +, VFxI-	R_{IXI}	10			MΩ	
Input Offset Voltage, VFxI +, VFxI-	V_{OSXI}	-25		+25	mV	
Power Supply Rejection, GSx	PSRR1	50	70		dB	
Common Mode Rejection, VFxI +, VFxI-	CMRR	55	65		dB	-2.5V ≤ V_{IN} ≤ +2.5V
DC Open Loop Voltage Gain, GSx	A_{VOL}	60	70		dB	
Open Loop Unity Gain Bandwidth, GSx	fc		1.0		MHz	
Output Voltage Swing, GSx	V_{OXI}	±2.5	±3.5		V	R_L ≥ 10 KΩ
Load Capacitance, GSx	C_{LXI}			50	pF	
Minimum Load Resistance, GSx	R_{LXI}	10			KΩ	
Common-Mode Range, VFxI	V_{CM}	-2.5		+2.5	V	

Transmit Filter

Output Resistance, VFxO	R_{OX}		1	3	Ω	
Output DC Offset, VFxO	V_{OSX}	-150		+150	mV	VFxI + Connected to GRDA, Input Op Amp at unity gain
Power Supply Rejection of V_{DD} at 1KHz VFxO	PSRR2	33	38		dB	
Power Supply Rejection of V_{SS} at 1KHz VFxO	PSRR3	30	35		dB	
Load Capacitance, VFxO	C_{LX}			50	pF	
Minimum Load Resistance	R_{LX}	10			KΩ	
Output Voltage, 1KHz. VFxO	V_{OX}	±3.2	±3.8		V	R_L ≥ 10 KΩ

COMMUNICATIONS

DC and Operating Characteristics (Cont'd):

Receive Filter

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input Leakage Current, VFRI	I_{BR}			100	nA	$V_{SS} < V_{IN} < V_{DD}$
Input Resistance, VFRI	R_{IR}	10			MΩ	
Output Resistance, VFRO	R_{OR}		5	7	Ω	
Output DC Offset, VFRO	V_{OSR}	-150		+150	mV	VFRI Connected to GRDA
Power Supply Rejection of V_{CC} at 1KHz VFRO	PSRR4	35	40		dB	
Power Supply Rejection of V_{BB} at 1KHz, VFRO	PSRR5	35	40		dB	
Load Capacitance, VFRO	C_{LR}			50	pF	
Minimum Load Resistance, VFRO	R_{LR}	10			KΩ	
Output Voltage Swing, VFRO	V_{OR}	±3.2	±3.8		V	R_L = 10KΩ

Receive Filter Driver Amplifiers

Input Leakage Current, PWRI	I_{BRA}			3	μA	$V_{SS} < V_{IN} < V_{DD}$	
Input Resistance, PWRI	R_{IRA}	10			MΩ		
Output Resistance, PWRO +, PWRO-	R_{ORA}		1	2	Ω	$\lvert I_{OUT} \rvert < 5mA$ $-3.0V < V_{OUT} < 3.0V$	
Output DC Offset, PWRO +, PWRO-	V_{OSRA}	-50		+50	mV	PWRI Connected to GRDA	
Load Capacitance, PWRO +, PWRO-	C_{LRA}			100	pF		
Output Voltage Swing Across R_L, PWRO+, PWRO-, Single Ended Connection	V_{ORA1}	±3.2			V	R_L = 10KΩ	R_L Connected to GRDA
		±2.9			V	R_L = 600Ω	
		±2.5			V	R_L = 300Ω	
Differential Output Voltage Swing, PWRO+, PWRO-, Balanced Output Connection	V_{ORA2}	±6.4			V	R_L = 20KΩ	R_L Connected Between PWRO+ and PWRO-
		±5.8			V	R_L = 1200Ω	
		±5.0			V	R_L = 600Ω	

AC Characteristics:

GRDA = GRDD = OV unless otherwise noted, V_{DD} = +5V, V_{SS} = -5V, T_A = 0°C to 70°C

Clock Input Frequency: CLK = 1.536MHz ± 0.1%, CLKS = V_{SS}
CLK = 1.544MHz ± 0.1%, CLKS = GRDD
CLK = 2.048MHz ± 0.1%, CLKS = V_{DD}

Transmit Filter

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Gain Relative to Gain at 1KHz	G_{RX}					OdBmO Input Signal Gain Setting Op Amp at Unity Gain
Below 50Hz				-10	dB	
50Hz				-20	dB	
60Hz				-26	dB	
200Hz		-1.5		-0.125	dB	OdBmO Signal = 1.1 V_{RMS} Input at VFXI+
300Hz to 3000Hz		-0.125		+0.125	dB	
3300Hz		-0.35		0.03	dB	
3400Hz		-0.8		-0.1	dB	
4000Hz				-14	dB	
4600Hz and Above				-32	dB	
Absolute Passband Gain at 1KHz, VFXO	G_{AX}	2.9	3.0	3.1	dB	
Gain Variation with Temperature at 1KHz	G_{AXT}		0.0004		dB/°C	OdBmO Signal Level
Gain Variation with Supplies at 1KHz	G_{AXS}		0.01		dB/V	OdBmO Signal Level, Supplies ± 5%
Cross Talk, Receive to Transmit, Measured at VFXO. $20 \log \left[\frac{VFXO}{VFRO}\right]$	C_{TRT}		-85	-71	dB	VFRI = 2.20 V_{RMS}, 1KHz Input VFXI +, VFXI- Connected to GSX, GSX Connected through 10KΩ to GRDA
Total C Message Noise at Output, VFXO	N_{CS1}		6	11	dBrncO	Gain Setting Op Amp at Unity Gain
Total C Message Noise at Output, VFXO	N_{CX2}		7	13	dBrncO	Gain Setting Op Amp at 20dB Gain

COMMUNICATIONS

AC Characteristics: (Cont'd)

Transmit Filter (cont.)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Differential Envelope Delay, VFxO 1KHz to 2.6KHz	DDX			70	μs	
Absolute Delay at 1KHz, VFxO	DAX			185	μs	
Single Frequency Distortion Products	DPX1		-55	-48	dB	OdBm Input Signal at 1KHz
Single Frequency Distortion Products at Maximum Signal Level of + 3dBmO at VFxO	DPX2		-50	-48	dB	Gain Setting Op Amp at 20dB Gain. The +3dBmO signal at VFxO is 2.26 VRMS

Receive Filter

Gain Relative to Gain at 1KHz with Sin x/x Correction	GRR					OdBmO Input Signal
Below 200Hz				0.125	dB	OdBmO Signal ≅ 1.6 VRMSX $\left[\frac{\text{Sin}\frac{\pi F}{8000}}{\frac{\pi F}{8000}}\right]$
200Hz		-0.125		0.125	dB	
300Hz to 3000Hz		-0.125		0.125	dB	
3300Hz		-0.35		0.03	dB	
3400Hz		-0.8		-0.1	dB	Input at VFRI
4000Hz				-14	dB	
4600Hz and Above				-30	dB	
Absolute Passband Gain at 1KHz, VFRO	GAR	-0.1	0	+0.1	dB	
Gain Variation with Temperature at 1KHz	GART		0.0004		dB/°C	OdBmO Signal Level
Gain Variation with Supplies at 1KHz	GARS		0.01		dB/V	OdBmO Signal Level, Supplies ± 5%
Cross Talk, Transmit to Receive, Measured at VFRO	CTTR		-80	-71	dB	VFXO = 2.26 VRMS 1KHz Output VFRI Connected to GRDA
Total C Messages Noise at Output, VFRO	NCR		5	8	dBrncO	VFRO Output or PWRO+ and PWRO- Connected with Unity Gain
Differential Envelope Delay, VFRO 1KHz to 2.6KHz	DDR			85	μs	
Absolute Delay at 1KHz, VFRO	DAR			125	μs	
Single Frequency Distortion Products	DPR1		-55	-48	dB	OdBm Input Signal at 1KHz
Single Frequency Distortion Products at Maximum Signal Level of + 3dBmO at VFRO	DPR2		-50	-48	dB	+3dBmO Signal Level of 2.26 VRMS, 1KHz Output at VFRO

Pin Function Table

Name	Description
VFxI +	Analog input of the transmit filter from the 2 wire transmit output of a 2-to-4 wire converter
VFxI-	Inverting input of the gain adjustment op. amp on the transmit filter
GSX	Op. amp output used for gain setting of the transmit filter
VFRO	Analog output of the receive filter providing a direct interface to electronic 2-to-4 wire converter.
PWRI	Input to the power driver amplifiers. When tied to Vss these amplifiers are powered down.
PWRO+ PWRO-	Power amplifier outputs capable of directly driving transformer 2-to-4 wire converters.
VSS	Negative supply voltage (-5V)
VDD	Positive supply voltage (+5V)
VFRI	Analog input of the receive filter.
GRDD	Digital ground for internal clock generator.
CLK	Clock input. High impedance input. TTL-compatible voltage levels.
PDWN	Control input active high for the standby power down mode. Internal pull up to 5V. TTL-compatible voltage levels.
CLKS	Clock frequency select. CLK Input (Pin 12): 1.536MHz, 1.544MHz, 2.048MHz — CLKS Connection: VSS (-5V), GRDD, VDD (+5V)
GRDA	Analog ground for receive and transmit filters. Not internally connected to GRDD.
VFXO	Analog output of transmit filter.

Functional Description

Transmit Filter Input Stage

The input stage provides gain adjustment in the passband. The input operational amplifier has a common mode range of ±3.2 volts, a DC offset of less than 25mV, a voltage gain of typically 2000 and a unity gain bandwidth of 1.0 MHz. It can be connected to provide a gain of 20dB without degrading the noise performance of the filter. The load impedance connected to the amplifier output must be greater than 10KΩ. The input signal on lead VFxI + can be either AC or DC coupled. The input Op Amp can also be used in the inverting mode or differential amplifier mode. The remaining portion of the transmit filter provides a gain of + 3dB in the pass band.

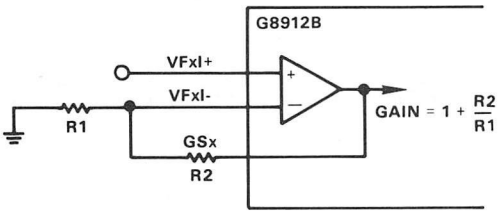


Fig. 1 Transmit Filter Gain Adjustment

50 Hz/60Hz Notch—Transmit Filter

The transmit filter has a notch section to reject 50Hz and 60Hz components of the input signal. A minimum attenuation of 26dB is provided at 60Hz. At 50Hz, the minimum attenuation is 20dB. The gain at 200Hz is between -0.125dB and -1.5dB. (All gain figures are relative to the gain at 1KHz.

An active RC low pass anti-aliasing filter is included on chip immediately in front of the 50Hz/60Hz notch section. This filter provides greater than 35dB attenuation at 64KHz. As a result no external anti-aliasing components are required to provide the necessary anti-aliasing function for the switched capacitor sections of the transmit filter which operate at an internal sampling rate of 128KHz.

Transmit Filter Transfer Characteristics

The transmit section of filter provides a passband flatness and stopband attenuation which exceeds the Bell D3 and D4 specifications and the CCITT G.712 recommendations. The transmit filter transfer characteristics and specifications are shown in Fig. 2.

Transmit Filter Output Stage

The voltage range of the output signal on the VFxO lead is ±3.2 volts. The DC offset is less than 150mV. The output stage includes an active RC post-filter to attenuate clock noise.

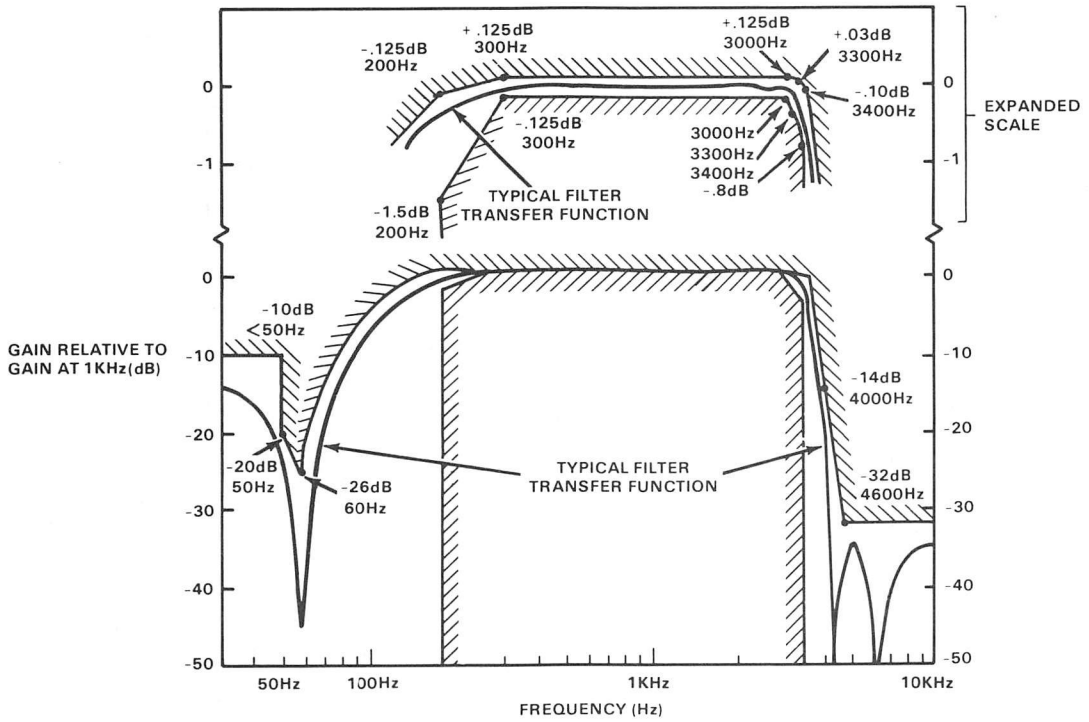


Fig. 2 Transmit Filter Transfer Characteristics

Receive Filter Anti-Aliasing Prefilter

An active RC low pass anti-aliasing filter is included on chip immediately preceding the receive filter section. This filter provides greater than 32dB rejection at 255KHz which is 1KHz below the receive filter effective sampling rate of 256KHz. This filter removes out-of-band noise generated by the codec which can be aliased in band by the filter. This results in significantly reduced harmonic distortion in the receive channel.

Receive Filter Transfer Characteristics

The receive section of the filter provides a passband flatness and stopband rejection which exceeds the Bell D3/D4 specifications and the CCITT G.712 recommendations, when used with a decoder which contains a sample/hold amplifier at its output. The filter contains the required compensation for the Sin x/x response of such decoders. The receive filter transfer characteristics and specifications, including the Sin x/x response of the decoder are shown in Fig. 3.

Receive Filter Output

The VFRO lead is capable of driving high impedance electronic hybrids. The gain of the receive section from VFRI TO VFRO is:

$$\frac{\left[\frac{\pi f}{8000}\right]}{\text{Sin}\left[\frac{\pi f}{8000}\right]}$$

which when multiplied by the output response of a suitable Codec results in a 0dB gain in the passband. The filter gain can be adjusted downward by a resistor voltage divider connected as shown in Fig. 4. The total resistive load RT on VFRO should not be less than 10KΩ. The output stage includes an active RC post filter to attenuate clock noise.

Receive Filter Output Driver Amplifier Stage

A balanced power amplifier is provided in order to drive low-impedance loads in a bridged configuration. The receive filter output VFRO is connected through gain setting resistors R1 and R2 to the amplifier input PWRI. The series combination of RS and the hybrid transformer must present a minimum AC load resistance of 600Ω to the amplifier in the bridged configuration. A typical connection of the output driver amplifiers is shown in Fig. 5. These amplifiers can also be used with loads connected to ground.

When the power amplifier is not needed it may be deactivated to save power. This is accomplished by tying the PWRI pin to VSS.

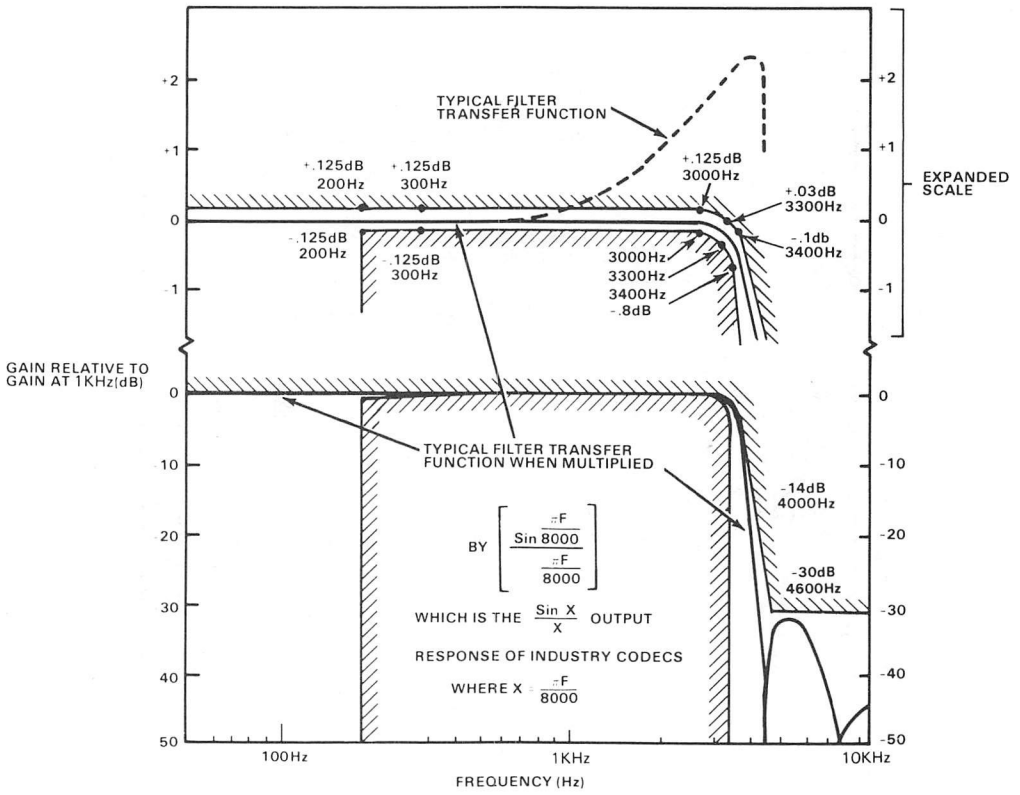


Fig. 3 Receive Filter Transfer Characteristics

$$R_T = R1 + \frac{R2Z}{R2 + Z} \geqslant 10K\Omega$$

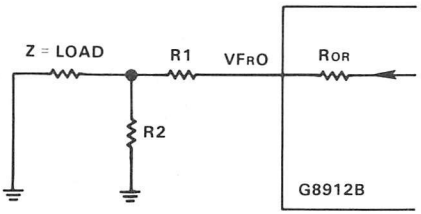


Fig. 4 Receive Filter Output Gain Adjustment

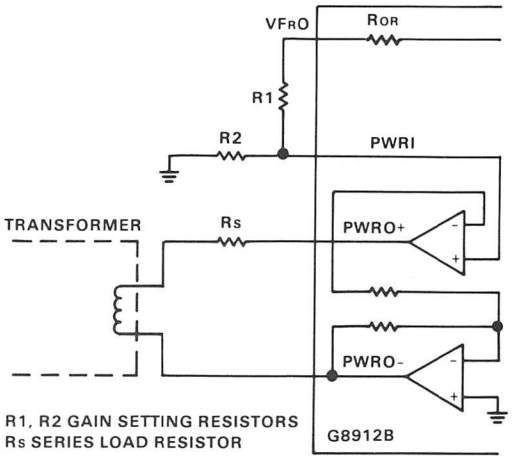


Fig. 5 Typical Connection of Output Driver Amplifier

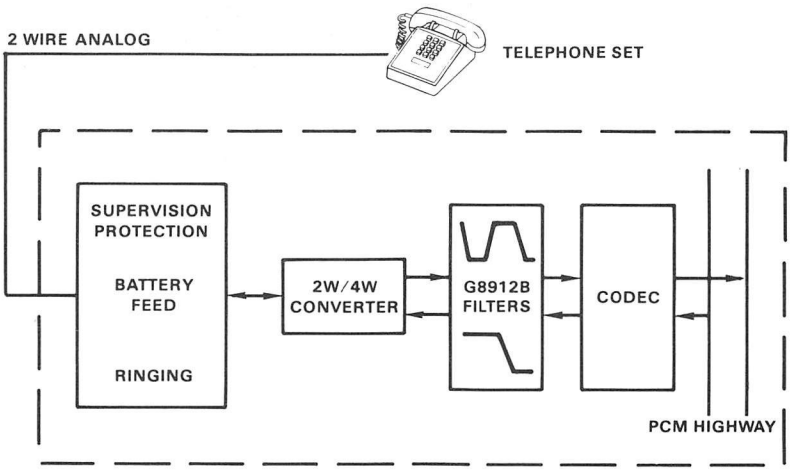


Fig. 6 Typical Line Termination

4 Memories

GTE MICROCIRCUITS

GTE Microcircuits

G2316B

Microcircuits

NMOS 2048 X 8 ROM

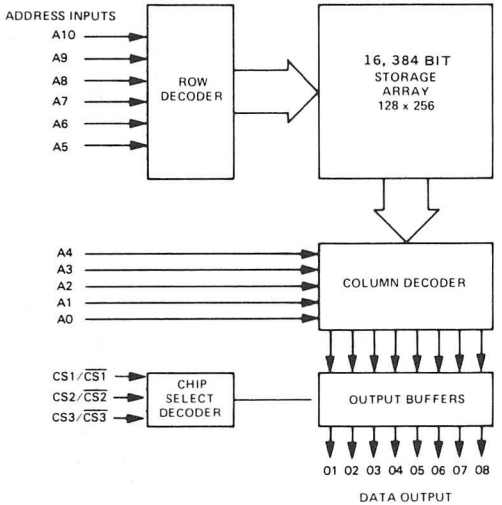
Features

- 2048 8-bit bytes (16K)
- Maximum Active Current: 100 mA
- Max. access time: 350 nS—G2316B—3
  450 nS—G2316B—4
- Output drive: one TTL load, plus 100 pF
- All input/outputs TTL compatible
- Three programmable Chip Select inputs
- Three-state outputs for memory expansion
- Single +5V power supply, ±5 percent
- Standard 24-pin plastic or cerdip package

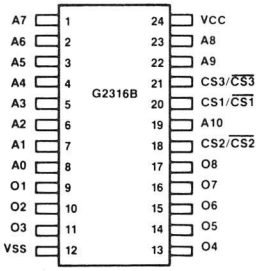
General Description

The GTE G2316B Read Only Memory is a 2048 word by 8 bit device with a maximum access time of 350 nanoseconds or 450 nanoseconds. The G2316B ROM is a mask-programmable, byte-organized memory designed for use in bus-oriented applications with all 8-bit N-channel microprocessors. Three Chip Select inputs provide convenient memory expansion—allowing up to 8 G2316B ROMs to be OR-tied without external coding. In addition, three-state output buffers allow simple parallel-busing for memory expansion. The G2316B is TTL compatible, requires only a single +5V power supply, no external clocks and no refresh circuitry. Packaging is standard 24-pin plastic or cerdip.

Block Diagram



Pin Configuration



Pin Function

Pin	Description
A0-A10	Address
O1-O8	Outputs
Vcc	+5V
Vss	Ground
CS	Chip Select

Ordering Information

Device	Access Time (nS)	Max. Active Current (mA)	Package	Temp. Range
G2316B-3CJ	350	100	Cerdip	0°C to 70°C
G2316B-3CK	350	100	Plastic	0°C to 70°C
G2316B-4CJ	450	100	Cerdip	0°C to 70°C
G2316B-4CK	450	100	Plastic	0°C to 70°C

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Voltage to Any Pin With Respect to Vss	V_{DC}	0.5V to 7.0V
Current Into/From Output	I_{DD}	50 mA
Operation Ambient Temp. Range	T_A	0°C to 70°C
Storage Temp. Range	T_S	-65°C to 150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum ratings.

NOTES:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Electrical Characteristics: Full Operating Voltage and Temperature Range

Characteristic	Symbol	Min	Max	Unit	Conditions
Input High Level	V_{IH}	2.0	V_{CC}	V	
Input Low Level	V_{IL}	-0.5	+0.8	V	
Input Leakage Current	I_{LI}	-10	+10	μA	
I/O Leakage Current	I_{LO}	-10	+10	μA	V_O = 0.4 to V_{CC}
Output Voltage High	V_{OH}	2.4	—	V	I_O = -0.2 mA
Output Voltage Low	V_{OL}	—	0.4	V	I_O = 2.1 mA
Power Supply Current	I_{CC}	—	100	mA	V_{CC} = 5.25, T_A = 0°C

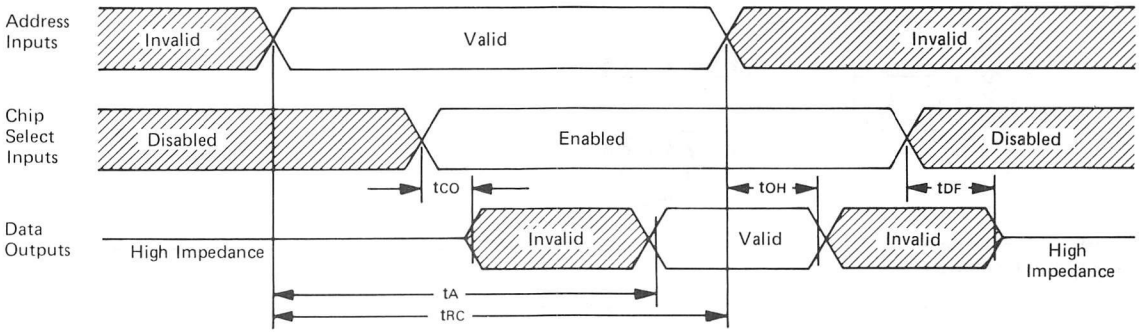
Read Cycle—AC Characteristics: Full Operating Voltage and Temperature Range

Parameter	Symbol	G2316B-3		G2316B-4		Units
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	350	–	450	–	nS
Address Access Time	t_A	–	350	–	450	nS
Chip Select Delay Time	t_{CO}	–	120	–	150	nS
Chip Deselect Delay Time	t_{DF}	–	120	–	150	nS
Data Valid After Address Change	t_{OH}	20	–	20	–	nS

Capacitance

Parameter	Symbol	Typ	Max	Unit	Conditions
Input Capacitance	C_{IN}	4	7	pF	
Output Capacitance	C_{OUT}	5	10	pF	V_O = OV

Timing Diagram



G2332

Microcircuits

NMOS 4096 X 8 ROM

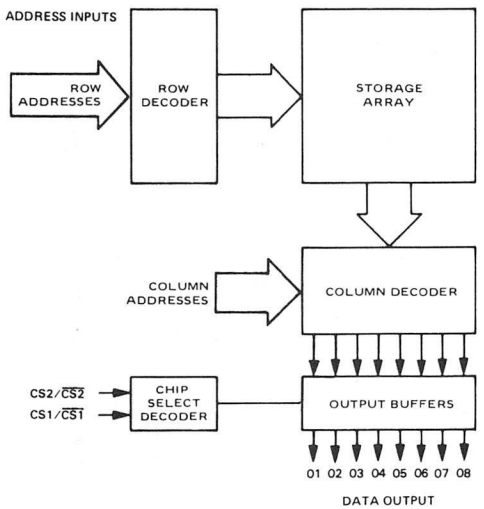
Features

- 4096 8-bit bytes (32K)
- Maximum Active Current: 100 mA
- Max. access time: 350 nS—G2332-3
  450 nS—G2332-4
- Output drive: one TTL load, plus 100 pF
- All input/outputs TTL compatible
- Two programmable Chip Select inputs
- Three-state outputs for memory expansion
- Single +5V power supply, ±5 percent
- Standard 24-pin plastic or cerdip package

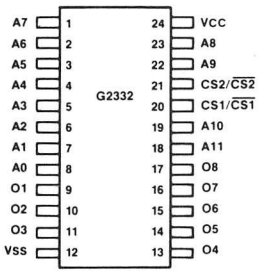
General Description

The GTE G2332 Read Only Memory is a 4096 word by 8 bit device with a maximum access time of 350 nanoseconds (G2332-3) or 450 nanoseconds (G2332-4). The G2332 ROM is a mask-programmable, byte-organized memory designed for use in bus-oriented applications with all 8-bit N-channel microprocessors. Dual Chip Select inputs provide convenient memory expansion—allowing up to four G2332 32K ROMs to be OR-tied without external coding. In addition, three-state output buffers allow simple parallel-busing for memory expansion. The G2332 is TTL compatible, requires only a single +5V power supply, requiring no external clocks and no refresh circuitry. Packaging is standard 24-pin plastic or cerdip.

Block Diagram



Pin Configuration



Pin Function

Pin	Description
A0-A11	Address
O1-O7	Outputs
Vcc	+5V
Vss	Ground
CS	Chip Select

Specifications

Device	Access Time	Max. Active Current	Package	Temp. Range
G2332-3CJ	350 nS	100 mA	Cerdip	0°C to 70°C
G2332-3CK	350 nS	100 mA	Plastic	0°C to 70°C
G2332-4CJ	450 nS	100 mA	Cerdip	0°C to 70°C
G2332-4CK	450 nS	100 mA	Plastic	0°C to 70°C

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Voltage to Any Pin With Respect to Vss	V_{DC}	0.5V to 7.0V
Current Into/From Output	I_{DD}	50 mA
Operation Ambient Temp. Range	T_A	0°C to 70°C
Storage Temp. Range	T_S	-65°C to 150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum ratings.

NOTES:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Electrical Characteristics: Full Operating Voltage and Temperature Range

Characteristic	Symbol	Min	Max	Unit	Conditions
Input High Level	V_{IH}	2.0	V_{CC}	V	
Input Low Level	V_{IL}	-0.5	+0.8	V	
Input Leakage Current	I_{LI}	-10	+10	μA	
Output Leakage Current	I_{LO}	-10	+10	μA	V_O = 0.4 to V_{CC}
Output Voltage High	V_{OH}	2.4	—	V	I_O = -0.2 mA
Output Voltage Low	V_{OL}	—	0.4	V	I_O = 2.1 mA
Power Supply Current	I_{CC}	—	100	mA	V_{CC} = 5.25, T_A = 0°C

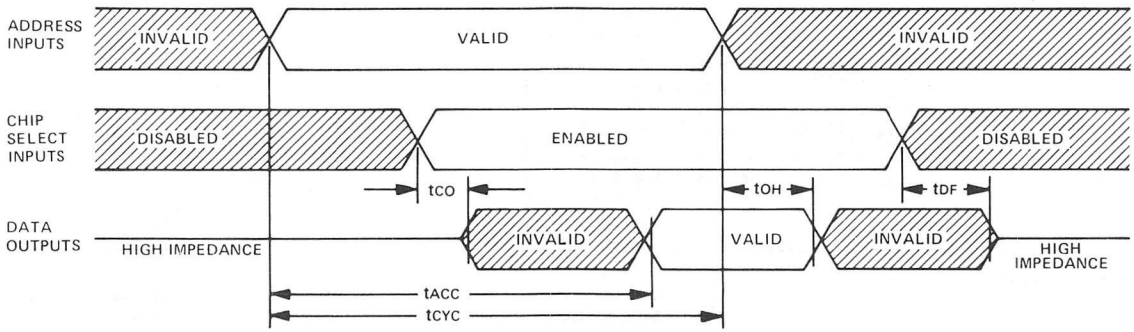
Read Cycle—AC Characteristics: Full Operating Voltage and Temperature Range

Parameter	Symbol	G2332-3		G2332-4		Units
		Min	Max	Min	Max	
Read Cycle Time	t_{CYC}	350	–	450	–	nS
Address Access Time	t_{ACC}	–	350	–	450	nS
Chip Select Delay Time	t_{CO}	–	120	–	150	nS
Chip Deselect Delay Time	t_{DF}	–	120	–	150	nS
Data Valid After Address Change	t_{OH}	20	–	20	–	nS

Capacitance

Parameter	Symbol	Typ	Max	Unit	Conditions
Input Capacitance	C_{IN}	4	7	pF	
Output Capacitance	C_{OUT}	5	10	pF	V_O = OV

Timing Diagram



MEMORIES

G5364
G5365

Microcircuits

CMOS 8192 x 8 ROM

Features

- Low power CMOS technology
  200 μA Standby
  15 mA Operating
- Single +5 volt power supply
- Three-state data outputs
- Fully TTL compatible
- User-selected power down
- Output Enable (G5365)
- Three programmable chip selects (G5365)
- Pin compatible with 2764 EPROM (G5365)

General Description

The GTE G5364/65 Read Only Memories are 8192-word by 8-bit devices with a maximum access time of 250 nanoseconds. The devices are manufactured using the state-of-the-art CMOS process. For both devices, a manufacturing mask stage defined by the user programs the non-volatile memory.

The 5364 is packaged in a 24-pin package which offers upward compatibility with the GTE 2316 and GTE 2332 ROMs. The user has the option of a $\overline{CE}$ pin, which offers a power down feature, or a CS/$\overline{CS}$ pin, which offers faster CS access times (t_{ACS}).

The 5365 is packaged in the industry standard 28-pin package which offers campatibility with 64K EPROMs (2764). The user has the option of three user programmed CS/$\overline{CE}$ pins.

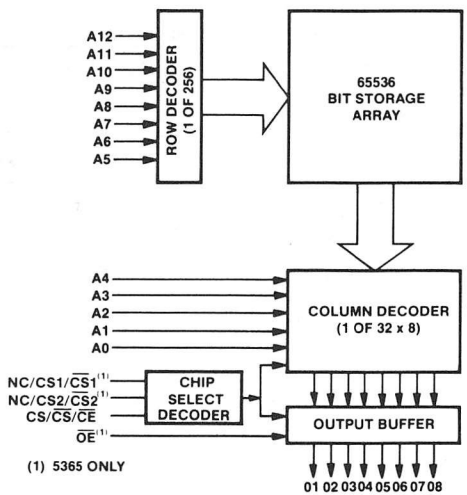
Bus-oriented application systems are catered for by the inclusion of three-state data outputs. The G5365 also provides an output enable to reduce system bus contention. The G5364/65s are available in both cerdip and plastic dual-in-line packages.

Pin Function

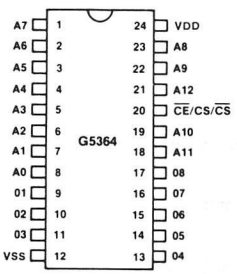
Pin	Description
A0-A12	Address
$\overline{CE}$	Chip Enable
CS/$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable

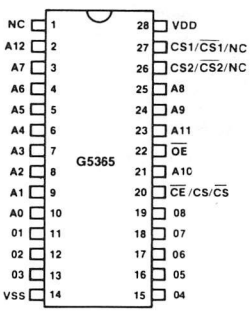
Pin	Description
01-08	Outputs
V_{DD}	+5 Volt Power Supply
V_{SS}	Ground
NC	No Connection

Block Diagram



Pin Configuration





MEMORIES

PRELIMINARY INFORMATION

Supplementary data may be published at a later date.

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Voltage to Any Pin With Respect to V_{SS} (Note 9)	V_{DC}	-0.5V to 7.0V
Current Into/From Output	I_{DD}	50 mA
Operation Ambient Temp. Range	T_A	0°C to 70°C
Storage Temp. Range	T_S	-65°C to 150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

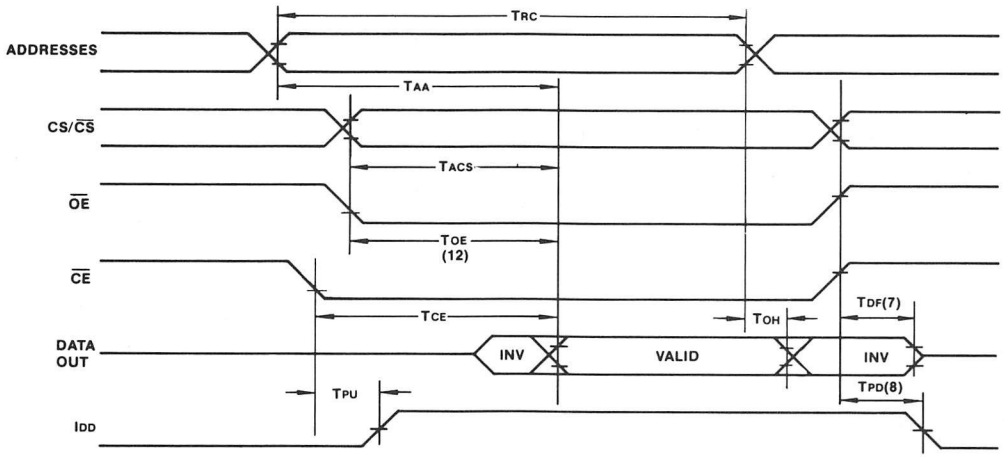
DC Characteristics: V_{DD} = 5.0V ±10%, T_A = 0°C to 70°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input High Level	V_{IH}	2.0		V_{DD}	V	
Input Low Level	V_{IL}	-0.5		+0.8	V	
Input Leakage Current	I_{LI}	-10		+10	µA	Note 2
Output Leakage Current	I_{LO}	-10		+10	µA	Note 3
Output Voltage High	V_{OH}	2.4			V	I_{OH} = -220 µA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 3.3 mA
Power Supply Current (Active)	I_{DD}		6	15	mA	Note 11
Power Supply Current (Standby)	I_{DD}			200	µA	Note 6
Input Capacitance	C_{IN}		4	7	pF	Note 5
Output Capacitance	C_{OUT}		5	10	pF	V_O = 0V, Note 5

AC Characteristics—Read Cycle: V_{DD} = 5.0V ±10%, T_A = 0°C to 70°C. See Notes 4, 10.

Parameter	Symbol	-25		-3		-4		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address Access Time	T_{AA}		250		300		450	nS	
Read Cycle Time	T_{RC}	250		300		450		nS	
Chip Select Access Time	T_{ACS}		100		120		150	nS	
Output Enable to Output Delay	T_{OE}		100		120		150	nS	Note 12
Chip Enable Access Time	T_{CE}		250		300		450	nS	
Power Up Time	T_{PU}	0		0		0		nS	
Data Valid After Address Change	T_{OH}	20		20		20		nS	
Chip Deselect Delay Time	T_{DF}	0	110	0	130	0	150	nS	Note 7
Power Down Time	T_{PD}		60		60		100	nS	Note 8

Timing Diagram



Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.
2. V_{IN} = 0V (V_{DD} = 5.5V)
3. Devices unselected, V_{OUT} =0V to 5.5V (V_{DD} = 5.5V)
4. Measured with two TTL loads and 100 pF (transition times = 10 nS)
5. Capacitance measured with Boonton meter or effective capacitance calculated from the equation:
   $C = \frac{\triangle Q}{\triangle V}$ with $\triangle V$ = 3.0 volts
6. $\overline{CE}$ is high, all address inputs at V_{SS} to V_{SS} + 0.5V, or V_{DD} to V_{DD} -0.5V
7. T_{DF} is specified from $\overline{OE}$, CS/$\overline{CS}$ or $\overline{CE}$ whichever occurs first.
8. T_{PD} is specified $\overline{CE}$ only
9. Output voltage minimum = -0.3V
10. Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Input timing reference level = 0.8V and 2.0V. Output timing reference = 0.8V and 2.0V.
11. Ouput load disconnected.
12. These AC characteristics are for the G5365 only.

Order Entry Information

GTE Microcircuits' preferred method of receiving a ROM code is by submittal of a set of programmed EPROM(s). Two sets of EPROMs must be submitted for each code. One set has the ROM code; the other set is blank. GTE Microcircuits will load the ROM code from the EPROM set into our computer system. This information will then be used to program the blank EPROM set, which will be sent back to the customer along with a listing of the code. The customer will approve this listing and return it to GTE.

Chip Select information must also be provided with the ROM code. For the G5364/G5365, Pin 20 may be programmed as a Chip Enable ($\overline{CE}$), high active Chip Select (CS), or a low active Chip Select ($\overline{CS}$). On the G5365, Pin 26 and Pin 27 may be programmed as a high active Chip Select (CS), low active Chip Select ($\overline{CS}$), or a No Connection (NC).

ROM code information may also be transmitted in the following optional methods:

1. ROMs
2. Paper Tape
3. Card Deck

Please consult the GTE Microcircuits factory for details.

G53128

Microcircuits

CMOS 16,384 x 8 ROM

Features

- Low power CMOS technology
  - 200 μA Standby
  - 20 mA Operating
- Single +5 volt power supply
- Three-state data outputs
- Output Enable function
- Two programmable Chip Select/Chip Enable inputs
- Pin compatible with 27128 EPROM
- Fully TTL compatible

General Description

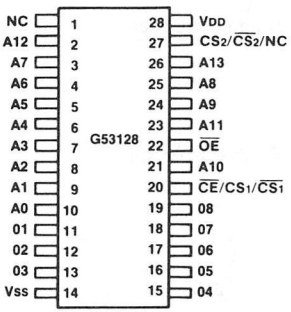
The GTE G53128 Read Only Memory (ROM) is a 16,384 word by 8-bit device with a maximum access time of 250 nanoseconds. The G53128 is manufactured using state-of-the-art CMOS process technology. This nonvolatile memory can be conveniently user programmed at the manufacturing mask stage. Its standard 28-pin package is fully compatible with both 64K and 128K EPROMs (i.e., 2764 and 27128 devices). Two user programmed Chip Select/Chip Enable pins are available as a user option. Three-state data outputs plus an Output Enable function allow convenient interfacing to bus-oriented systems. This TTL compatible device offers low power operation and standby modes and uses a single +5 volt supply. The G53128 is available in both cerdip and plastic dual-in-line packages.

Pin Function

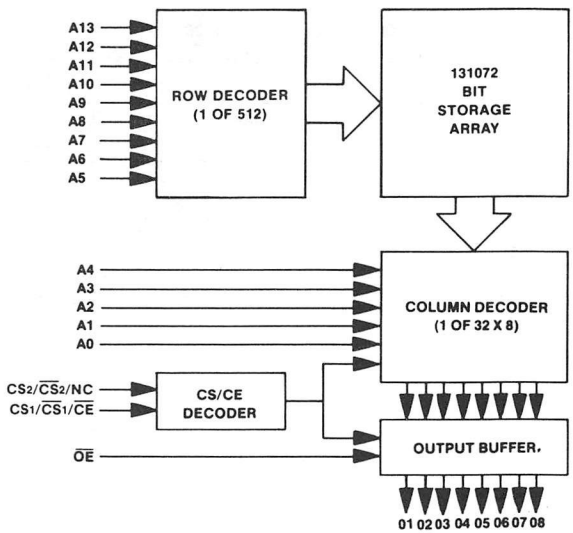
Pin	Description
A0-A13	Address
$\overline{CE}$	Chip Enable
CS/$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable

Pin	Description
01-08	Outputs
V_{DD}	+5 Volt Power Supply
V_{SS}	Ground
NC	No Connection

Pin Configuration



Block Diagram



PRODUCT PREVIEW

This document contains the design specifications for a product under development. Specifications may be changed in any manner without notice.

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Voltage to Any Pin With Respect to V_{SS} (Note 9)	V_{DC}	-0.5V to 7.0V
Current Into/From Output	I_{DD}	50 mA
Operation Ambient Temp. Range	T_A	0° C to 70° C
Storage Temp. Range	T_S	-65° C to 150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

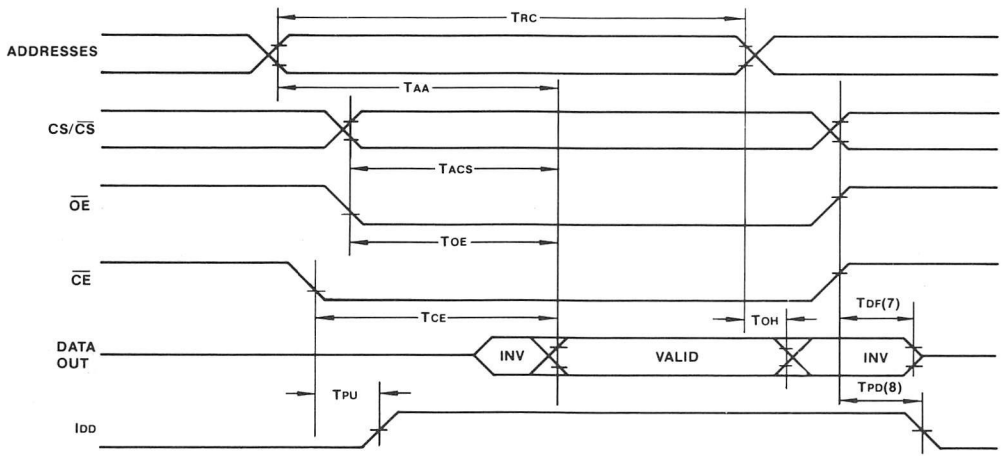
DC Characteristics: V_{DD} = 5V ±10%, T_A = 0° C to 70° C

Parameter	Symbol	Min	Max	Unit	Conditions
Input High Level	V_{IH}	2.0	V_{DD}	V	
Input Low Level	V_{IL}	-0.5	+0.8	V	
Input Leakage Current	I_{LI}	-10	+10	μA	Note 2
Output Leakage Current	I_{LO}	-10	+10	μA	Note 3
Output Voltage High	V_{OH}	2.4	—	V	I_{OH} = -220 μA
Output Voltage Low	V_{OL}	—	0.4	V	I_{OL} = 3.3 mA
Power Supply Current (Active)	I_{DD}	—	20	mA	Note 11
Power Supply Current (Standby)	I_{DD}	—	200	μA	Note 6
Input Capacitance	C_{IN}		7	pF	Note 5
Output Capacitance	C_{OUT}		10	pF	V_O = 0V, Note 5

AC Characteristics—Read Cycle: V_{DD} = 5V ± 10%, T_A = 0° C to 70° C See Notes 4, 10.

Parameter	Symbol	G53128-25		G53128-3		G53128-4		Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time	T_{AA}		250		300		450	nS
Read Cycle Time	T_{RC}	250		300		450		nS
Chip Select Access Time	T_{ACS}		100		120		150	nS
Output Enable to Output Delay	T_{OE}		100		120		150	nS
Chip Enable Access Time	T_{CE}		250		300		450	nS
Power Up Time	T_{PU}	0		0		0		nS
Data Valid After Address Change	T_{OH}	20		20		20		nS
Chip Deselect Delay Time (Note 7)	T_{DF}	0	110	0	130	0	150	nS
Power Down Time (Note 8)	T_{PD}		60		60		100	nS

Timing Diagram



Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.
2. V_{IN} = 0V (V_{DD} = 5.5V)
3. Devices unselected, V_{OUT} =0V to 5.5V (V_{DD} = 5.5V)
4. Measured with two TTL loads and 100 pF (transition times = 10 nS)
5. Capacitance measured with Boonton meter or effective capacitance calculated from the equation:
   $C = \frac{\triangle Q}{\triangle V}$ with $\triangle V$ = 3.0 volts
6. $\overline{CE}$ is high, all address inputs at V_{SS} to V_{SS} + 0.5V, or V_{DD} to V_{DD} -0.5V
7. T_{DF} is specified from $\overline{OE}$, CS/$\overline{CS}$ or $\overline{CE}$ whichever occurs first.
8. T_{PD} is specified $\overline{CE}$ only
9. Output voltage minimum = -0.3V
10. Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Input timing reference level = 0.8V and 2.0V. Output timing reference = 0.8V and 2.0V.
11. Output load disconnected.

Order Entry Information

GTE Microcircuits' preferred method of receiving a ROM code is by submittal of a set of programmed EPROM(s). Two sets of EPROMs must be submitted for each code. One set has the ROM code; the other set is blank. GTE Microcircuits will load the ROM code from the EPROM set into our computer system. This information will then be used to program the blank EPROM set, which will be sent back to the customer along with a listing of the code. The customer will approve this listing and return it to GTE.

Chip Select information must also be provided with the ROM code. For the G53128, Pin 20 may be programmed as a Chip Enable ($\overline{CE}$), high active Chip Select (CS), or a low active Chip Select ($\overline{CS}$). Pin 27 may be programmed as a high active Chip Select (CS), low active Chip Select ($\overline{CS}$), or a No Connection (NC).

ROM code information may also be transmitted in the following optional methods:

1. ROMs
2. Paper Tape
3. Card Deck

Please consult the GTE Microcircuits factory for details.

G53256

Microcircuits

CMOS 32,768 × 8 ROM

Features

- Low power CMOS technology
  200 μA Standby
  20 mA Operating
- Single +5 volt power supply
- Three-state data outputs
- Output Enable function
- A programmable Chip Select/Chip Enable input
- Pin compatible with 27128 and 27256 EPROMs
- Fully TTL compatible

General Description

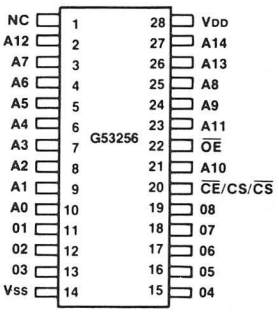
The GTE G53256 Read Only Memory (ROM) is a 32,768 word by 8-bit device with a maximum access time of 250 nanoseconds. The G53256 is manufactured using state-of-the-art CMOS process technology. This nonvolatile memory can be conveniently user programmed at the manufacturing mask stage. Its standard 28-pin package is fully compatible with 128K and 256K EPROMs. A single programmed Chip Select/Chip Enable pin is available as a user option. Three-state data outputs plus an Output Enable function allow convenient interfacing to bus-oriented systems. This TTL compatible device offers low power operation and standby modes and uses a single +5 volt supply. The G53256 is available in both cerdip and plastic dual-in-line packages.

Pin Function

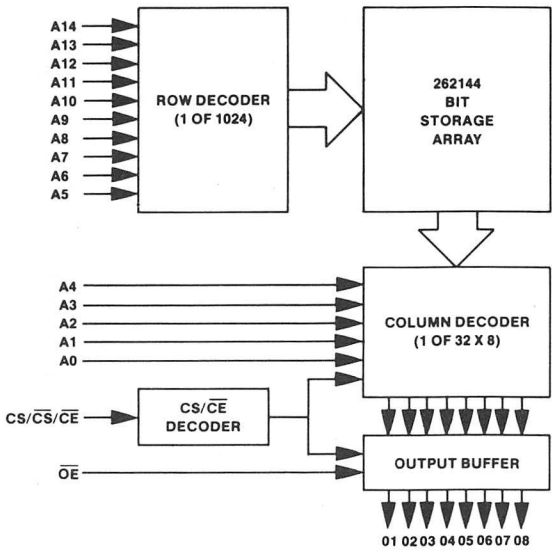
Pin	Description
A0-A14	Address
$\overline{CE}$	Chip Enable
CS/$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable

Pin	Description
01-08	Outputs
V_{DD}	+5 Volt Power Supply
V_{SS}	Ground
NC	No Connection

Pin Configuration



Block Diagram



PRODUCT PREVIEW

This document contains the design specifications for a product under development. Specifications may be changed in any manner without notice.

Absolute Maximum Ratings: (Note 1)

Parameter	Symbol	Value
Voltage to Any Pin With Respect to V_{SS} (Note 9)	V_{DC}	-0.5V to 7.0V
Current Into/From Output	I_{DD}	50 mA
Operation Ambient Temp. Range	T_A	0° C to 70° C
Storage Temp. Range	T_S	-65° C to 150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

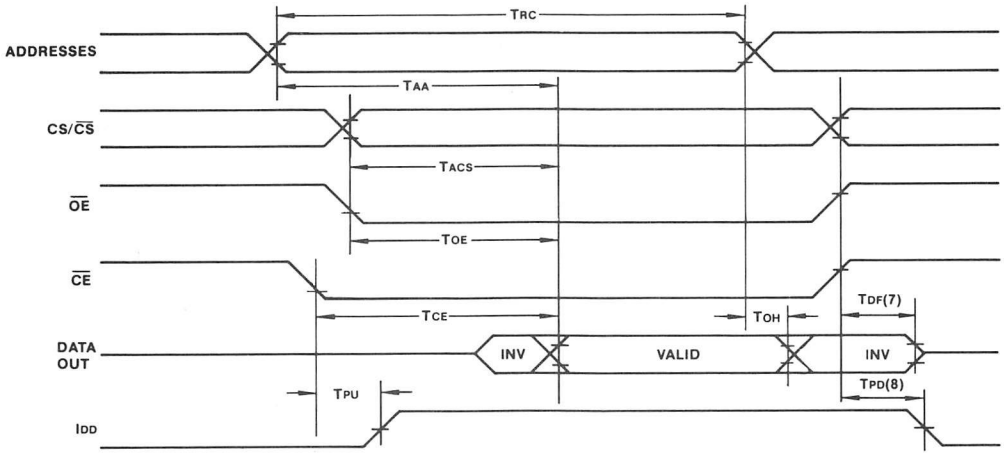
DC Characteristics: V_{DD} = 5V ±10%, T_A = 0° C to 70° C

Parameter	Symbol	Min	Max	Unit	Conditions
Input High Level	V_{IH}	2.0	V_{CC}	V	
Input Low Level	V_{IL}	-0.5	+0.8	V	
Input Leakage Current	I_{LI}	-10	+10	µA	Note 2
Output Leakage Current	I_{LO}	-10	+10	µA	Note 3
Output Voltage High	V_{OH}	2.4	—	V	I_{OH} = -220 µA
Output Voltage Low	V_{OL}	—	0.4	V	I_{OL} = 3.3 mA
Power Supply Current (Active)	I_{DD}	—	20	mA	Note 11
Power Supply Current (Standby)	I_{DD}	—	200	µA	Note 6
Input Capacitance	C_{IN}		7	pF	Note 5
Output Capacitance	C_{OUT}		10	pF	V_O = 0V, Note 5

AC Characteristics—Read Cycle: V_{DD} = 5V ± 10%, T_A = 0° C to 70° C. See Notes 4, 10.

Parameter	Symbol	G53256-25		G53256-3		G53256-4		Unit
		Min	Max	Min	Max	Min	Max	
Address Access Time	T_{AA}		250		300		450	nS
Read Cycle Time	T_{RC}	250		300		450		nS
Chip Select Access Time	T_{ACS}		100		120		150	nS
Output Enable to Output Delay	T_{OE}		100		120		150	nS
Chip Enable Access Time	T_{CE}		250		300		450	nS
Power Up Time	T_{PU}	0		0		0		nS
Data Valid After Address Change	T_{OH}	20		20		20		nS
Chip Deselect Delay Time (Note 7)	T_{DF}	0	110	0	130	0	150	nS
Power Down Time (Note 8)	T_{PD}		60		60		100	nS

Timing Diagram



Notes:

1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.
2. V_{IN} = 0V (V_{DD} = 5.5V)
3. Devices unselected, V_{OUT} =0V to 5.5V (V_{DD} = 5.5V)
4. Measured with two TTL loads and 100 pF (transition times = 10 nS)
5. Capacitance measured with Boonton meter or effective capacitance calculated from the equation:
   $C = \frac{\triangle Q}{\triangle V}$ with $\triangle V$ = 3.0 volts
6. $\overline{CE}$ is high, all address inputs at V_{SS} to V_{SS} + 0.5V, or V_{DD} to V_{DD} -0.5V
7. T_{DF} is specified from $\overline{OE}$, CS/$\overline{CS}$ or $\overline{CE}$ whichever occurs first.
8. T_{PD} is specified $\overline{CE}$ only
9. Output voltage minimum = -0.3V
10. Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Input timing reference level = 0.8V and 2.0V. Output timing reference = 0.8V and 2.0V.
11. Output load disconnected.

Order Entry Information

GTE Microcircuits' preferred method of receiving a ROM code is by submittal of a set of programmed EPROM(s). Two sets of EPROMs must be submitted for each code. One set has the ROM code; the other set is blank. GTE Microcircuits will load the ROM code from the EPROM set into our computer system. This information will then be used to program the blank EPROM set, which will be sent back to the customer along with a listing of the code. The customer will approve this listing and return it to GTE.

Chip Select information must also be provided with the ROM code. For the G53256, Pin 20 may be programmed as a Chip Enable ($\overline{CE}$), high active Chip Select (CS), or a low active Chip Select ($\overline{CS}$).

ROM code information may also be transmitted in the following optional methods:

1. ROMs
2. Paper Tape
3. Card Deck

Please consult the GTE Microcircuits factory for details.

G5116

Microcircuits

CMOS 2048 × 8 High Speed Static RAM

Features

- Low power CMOS technology
  - 15 mA Standby
  - 70 mA Operating
- Fast access time—90, 120, 150 nS
- Fully static RAM—no clock or timing strobe required
- Fully TTL compatible
- Pin compatible with 6116 RAMs
- Single +5 volt power supply

General Description

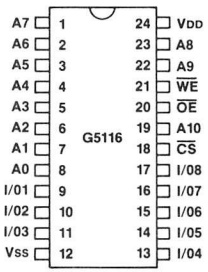
The GTE G5116 is a high-speed 2048-word by 8-bit static RAM with maximum access times of 90,120 or 150 nanoseconds. The G5116 is manufactured using GTE's advanced CMOS process. The G5116 is ideally suited for use with the GTE G65SC00 8-bit microprocessor family and other applications requiring high-speed static RAM. The Output Enable ($\overline{OE}$) function allows the output to be gated onto the I/O bus on command. All outputs represent a high impedance when in a disabled state. The G5116 requires very low current, 70mA (operating) and 15mA (standby), and operates from a single +5 volt power supply. The G5116 is available in standard 24-pin plastic or cerdip packages.

Pin Function

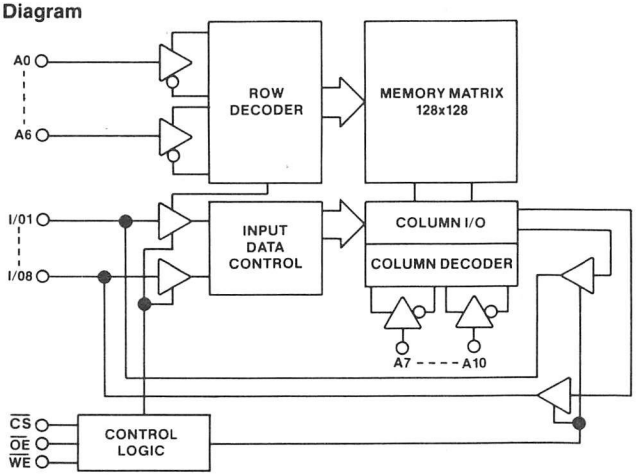
Pin	Description
A0-A10	Address Inputs
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable

Pin	Description
I/01-I/08	Input/Output
V_{DD}	+5V Power Supply
V_{SS}	Ground

Pin Configuration



Block Diagram



Specifications

Part Number	Organization and Description	Access Time	Icc
G5116P-90	2K × 8 Static RAM	90 nS	80 mA (Active) 15 mA (Standby)
G5116D-90	2K × 8 Static RAM	90 nS	
G5116P-2	2K × 8 Static RAM	120 nS	
G5116D-2	2K × 8 Static RAM	120 nS	
G5116P-3	2K × 8 Static RAM	150 nS	70 mA (Active) 15 mA (Standby)
G5116D-3	2K × 8 Static RAM	150 nS	

PRODUCT PREVIEW

This document contains the design specifications for a product under development. Specifications may be changed in any manner without notice.

Custom Memories

GTE Microcircuits offers a variety of custom memory products for special applications. Custom products may include:

- Special memory sizes
- Nonstandard word lengths
- Special pinout configurations
- Special logic for on-chip control functions
- RAM/ROM combinations, and other special circuit combinations
- Special on-chip drivers and buffers

Specific examples of GTE Custom Memory products include: The GTE G5362 which is a 64K ROM, partitioned into two totally independent 32K arrays (i.e., two 32K pages). To the user, the G5362 appears as two G2332 32K ROMs, but having the pinout of a single 32K ROM. Switching between the 32K pages is accomplished by selecting user-specified addresses.

In contrast, the GTE G5380 is an 8K × 10-bit ROM with a 16-bit multiplexed data output and address bus. This device is designed to interface with the GI CP1600 system bus.

GTE has the capability to produce a variety of Custom Memory products. If you have an unusual or custom application, you can count on GTE to provide the solution.

GTE Specializes in Custom Memory Products!

5 Support Systems

GTE MICROCIRCUITS

GTE Microcircuits

G65DS-001
GEM-1

Microcircuits

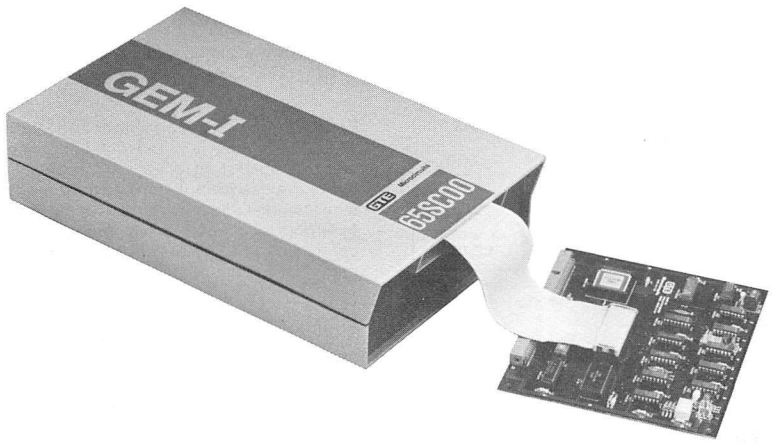
In-Circuit Emulator for 8-bit and Future 16-bit Microprocessor Systems

Features

- Transparent real time in-circuit microprocessor emulation with no wait states
- Operation at maximum rated target frequency
- Target system retains full memory and I/O capability
- Convenient 23-command single-character instruction set
- HELP command displays all commands and correct syntax
- Resident assembler and disassembler for software debugging
- Built-in memory diagnostics and block memory transfer
- Utility programs for downloading and uploading target programs
- Instruction-stepping or cycle-stepping through the program
- Expandable memory in 32K byte blocks (32K standard)
- Real time forward and backward trace modes
- Eight hardware trace points for examining logic status
- Up to 2048 cycles of recorded trace information on each of 34 channels
- Two breakpoints to halt emulation on a variety of conditions
- Crystal oscillator adapter—requires crystal and no other external components
- Disassembly of trace or memory for both step and list trace commands
- Convenient off-line debugging of the target program
- Internal oscillator with internal crystal or user-supplied external crystal
- Emulates future GTE products by simply changing the Personality Board
- RS-232C interface allows downloading and uploading of object code in Intel or Tektronix hex format
- Emulates all 18 GTE G65SC00 Series Microprocessors

General Description

GTE's GEM-I In-Circuit Emulator provides full in-circuit emulation for both 8 and future 16-bit microprocessor systems. GEM-I is ideally suited for not only hardware development programs, but also manufacturing and field service debugging of microprocessor systems. A wide range of future microprocessors can be emulated by simply changing the GEM-I Personality Board. In this way, multiple design projects can be under way at the same time. Also, since GTE's GEM-I contains its own resident assembler and disassembler, it can be minimally configured with only a display terminal and power supply. In this configuration, once the target program object code has been downloaded from the host computer to the GEM-I memory, hardware/software debugging or system development can be accomplished off-line, thus freeing the computer for other duties. This capability allows the development of a multi-workstation system with multiple emulators operating in conjunction with a single mini/microcomputer or a full-scale development system. GEM-I operation is straightforward and convenient. The operator can execute software in either a continuous or single-step mode and can substitute blocks of system memory for user or application equivalent memory. Two breakpoints allow the operator to stop emulation on prespecified addresses or conditions. GEM-I's trace capability (single step or list) provides a detailed history of program execution. Trace recordings can include up to 2048 cycles of information on each of 34 channels—16 for addresses, 8 for data, 2 for status, and 8 for spares.

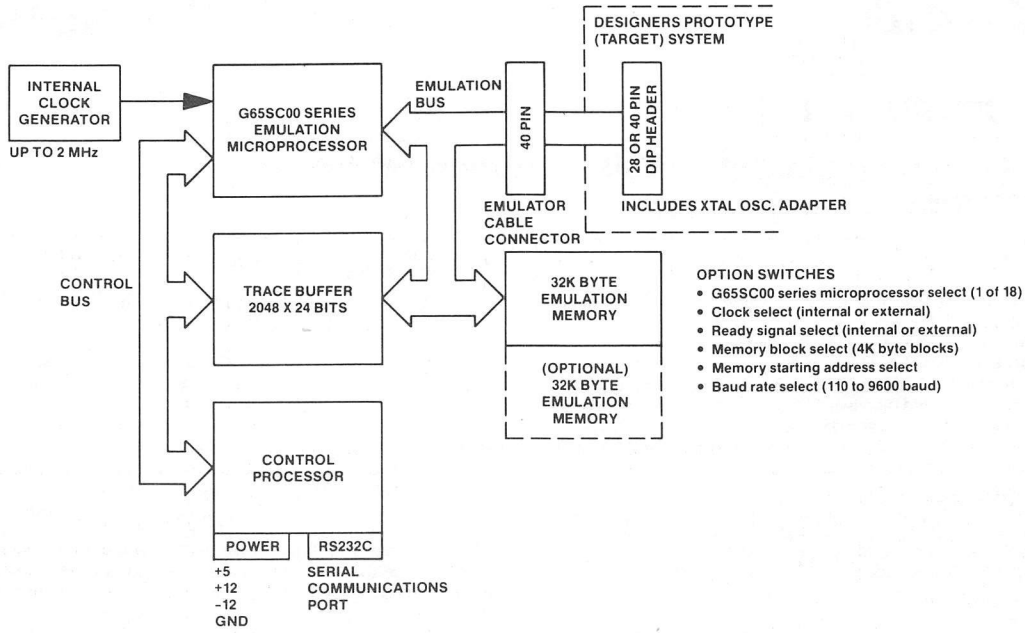


SUPPORT SYSTEMS

ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

Block Diagram



Total Hardware/Software Integration

The GEM-I In-Circuit Emulator allows the design engineer to integrate both hardware and software development concurrently. This interactive approach is a highly efficient method of system design. In this way, modular hardware design functions and software subroutines can be added and debugged as they become available. This progressive design approach results in considerable savings in both cost and development time. The GEM-I system can be configured as follows:

Stand Alone System

The GEM-I stand alone configuration is shown in Figure 1. In conjunction with a display terminal and power supply, the emulator can be used to perform comprehensive debugging by first downloading the resident program object code from the host computer system, or by loading the object code program from diskette or other storage device via a display terminal. This stand-alone configuration allows the host computer or full-scale development system to remain off-line and free for other uses, while the GEM-I maintains full hardware/software debugging capability.

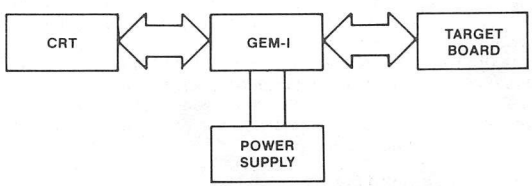


Figure 1. Stand-alone GEM-I Emulation System

GEM-I and the Host Computer

When connected to a dedicated host CPU, the display terminal is not normally required. In this case, the computer replaces the display terminal and all commands, programs and data transfers are executed from the CPU keyboard via a standard computer I/O channel as shown in Figure 2. In non-dedicated CPU systems, a dumb terminal is used for stand-alone operation, while the host computer serves for program storage and transfer only. When a host computer is interfaced to GEM-I, a driver program must be resident in the CPU. Driver programs and assemblers for various computer systems are available, including:

- Apple computers
- Intel development systems
- Digital Equipment mini and mainframe computers

For a current listing of supported computers, contact your nearest GTE Sales Office.

Field Service and Manufacturing Diagnostics

The GEM-I is ideally suited for field service, depot maintenance and manufacturing diagnostic applications. In these cases, microprocessor emulation can be achieved from simple stand-alone workstations communicating with either a dedicated mini/microcomputer or via modem communication from a central computer system. Figure 3 shows a typical field service/manufacturing configuration.

Functional Description

The GTE GEM-I emulator consists of three printed circuit boards—the Personality Board (CEP), the Real Time Trace Board (RTT), and the Memory Board (UEM). Cables are included for connection between the emlulator and the user's target system.

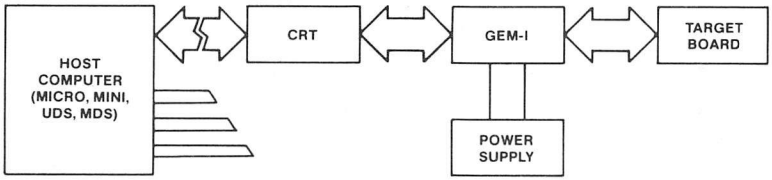


Figure 2. GEM-I Emulation System With Host Computer

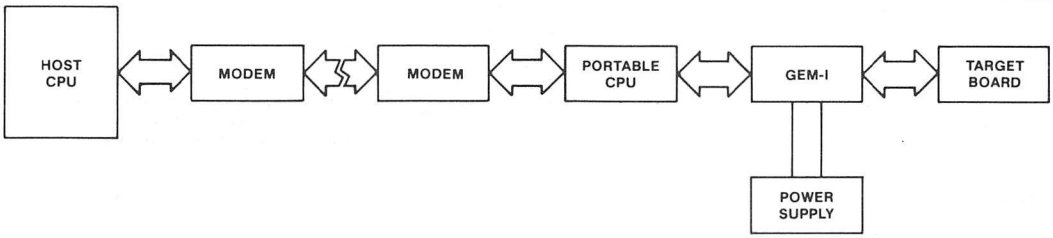


Figure 3. Field Service/Manufacturing Configuration

Microprocessor Emulation

GEM-I is capable of emulating all 18 GTE G65SC00 Series Microprocessors and future microprocessors as they become available. Selection of any one of the 18 G65SC00 Series Microprocessors is accomplished by switch selection on the GEM-I Personality Board. This change is easily performed by the user. The emulation of future microprocessors is a simple user task that requires changing only the Personality Board.

Memory Expansion

GEM-I contains a standard 32K byte memory. An additional 32K memory board can be user-installed to meet the needs of increased emulation memory requirements. The added memory board (32K) requires an additional 800 mA at +5 Vdc from the external power supply.

In-Circuit Emulator Cables

A cable is used to connect from the emulator to the user's target board. This cable consists of a flat ribbon cable with a 40-pin connector at the emulator end and either a 40-pin or a 28-pin header at the user end.

Computer Interface

The GEM-I can communicate with either a Data Terminal Equipment (DTE) interface or a Data Communications Equipment (DCE) interface. This capability allows convenient interfacing to virtually any display terminal, host computer, or modem system. Interfacing is via RS-232C cable. Modem communication is available at any of eight rates from 110 to 9600 baud.

Memory Mapping

The GEM-I can have up to 64K bytes of internal emulation memory. By switch selection, the user can enable or disable 4K byte blocks of memory depending on the amount of emulation memory needed. In addition, the user can select the starting address for a 32K byte emulation memory block. The ending address will be the starting address plus 32K bytes, with wrap around at the 64K boundary.

Operating Modes

GTE's GEM-I In-Circuit Emulator contains its own internal EPROM-based program for interactive emulation of the target microprocessor. This program provides the user with simple single-character commands for:

- Initiating emulation
- Defining breakpoints
- Establishing trace data collection
- Displaying and controlling system parameters

The emulation program is based on a 23-command structure. Command modifiers allow the user to further modify commands for maximum flexibility in establishing command operations.

Target Emulation

Emulation commands control the setting up, running and halting of the microprocessor emulation process. Within this command structure, user determined breakpoints and trace-points are used to halt the emulation and provide a detailed display of a particular execution or sequence within a user's application program. Trace commands can be performed on either a step or trace list basis. Emulation may be stopped at any user-defined address, and may be instruction-stepped, or cycle-stepped. Also, emulation may be recorded either forward or backward with respect to a user-defined trigger address, with up to 2048 trace steps being recorded during real time execution.

Breakpoints

GEM-I contains two real time breakpoints. The user can define the breakpoint address or condition which will halt emulation. The halt condition can be further qualified to stop only after a preset number of breakpoint address compare cycles, or on a selected type of processor activity.

Tracepoints

Within the GEM-I, both forward and backward trace commands start the real time emulation and recording of target status information. The start point is determined by a user defined trigger address. The trace will halt when the trace buffer is full or a breakpoint is reached, with up to 2048 trace cycles being recorded. Recorded information is then listed by use of the List Trace Buffer command. Modifier options allow the user to specify that the target processor continue running after the trace stops, or the user can specify that trace recording start after a preset number of cycles is reached following the trigger condition.

GEM-I Command Set

The GEM-I In-Circuit Emulator contains 23 commands, each identified by a single character. This command set is standard regardless of the target processor being emulated. Table 1 provides a listing of all GEM-I commands.

TABLE 1
GEM-I Commands

Type	Command	Character	Function
System	Help	?	Displays all commands and their syntax.
	Processor Type	!	Displays the μP currently being emulated.
Assembler/ Disassembler	Assembler	A	Allows line assembly of programs entered from a terminal.
	Disassembler	Z	Converts an existing machine code program back to assembly language mnemonics.
Trace	Forward Trace	F	Traces program information from a specified trigger point until the trace buffer is full, without interrupting the emulation.
	Backward Trace	B	Traces program information up to specified memory location without interrupting the emulation.
	List Trace	L	Lists Forward or Backward trace informations in Hex or Mnemonic format.
Execution Control	Jump	J	Causes the μP program to jump to a specified address.
	Go	G	Starts emulation.
	Halt	H	Supports two hardware breakpoints.
	Cycle Step	C	Steps the μP and displays its status as of the current machine cycle.
	Instruction Step	S	Steps the μP and displays its status as of the current instruction cycle.
	Reset	X	Resets the μP and enables various external control signals.
Enable/Disable	Enable	E	Enables various external control signals.
	Disable	D	Disables various external control signals.
Memory Manipulation	Memory Examine/Modify	M	Displays the content of a specified memory location and allows modification.
	Memory Display	M	Displays the contents of a specified range of memory locations.
	Memory Fill	M	Fills a specified range of memory locations with a given value.
	Memory Test/Transfer	T	Tests or transfers the contents of memory block.
Register Manipulation	Register Examine/Modify	R	Displays the contents of μP registers, and allows modification.
Input/Output	Input	I	Reads and displays a target port.
	Output	O	Writes to a target port.
File Management	Down-Load	: or /	Down-loads object code from a host computer to μP memory (in Intel or Tektronix hex format).
	Up-load	U	Up-loads object code from a μP memory to a host computer (in Intel or Tektronix hex format).

General Specifications

Physical Characteristics	
Height	8.0 cm (3.15 in)
Width	20.0 cm (7.87 in)
Depth	33.0 cm (13.00 in)
Weight	2.0 Kg (4.40 lb)
Electrical Characteristics	
Input Power	+ 5Vdc @ 4.0A
	+12Vdc @ 0.2A
	-12Vdc @ 0.2A
Environmental Characteristics	
Operating Temperature	-10°C to 65°C (14°F to 149°F)
Storage Temperature	0°C to 50°C (32°F to 122°F)
Relative Humidity	20 to 80%

Ordering Information

Item	Part Number
GEM-I In-Circuit Emulator Assembly (1-2 MHz)	G65DS-001
GEM-I In-Circuit Emulator	G65DS-005
40-pin signal cable (with crystal oscillator adapter)	G65DS-003
28-pin signal cable (with crystal oscillator adapter)	G65DS-004
Power supply cable	G65DS-006
GEM-I Power Supply	G65DS-007
Memory Expansion (32K byte)	G65DS-008
GEM-I User's Manual	3001-02-00

G65DS-150

Microcircuits

Evaluation Board for G65SC150 CTU

Features

- Emulates GTE's G65SC150 Communications Terminal Unit (CTU)
- Executes full G65SC150 instruction set
- Allows real-time G65SC150 emulation for in-circuit prototype debugging and program development using GEM-I In-Circuit Emulation system, or equivalent
- Can be configured for stand-alone, full capability CTU emulation in designer's prototype system
- 2K × 8 EPROM or RAM for use during program development (RAM supplied)
- Crystal oscillator (3 to 16 MHz) for driving CTU clock input (3.58 MHz supplied)
- Vectored interrupt logic for vector address translation

General Description

GTE's G65SC150 Communications Terminal Unit (CTU) is a single-chip microcomputer which incorporates a G65SC00 Series microprocessor, RAM, ROM and several I/O functions. When developing a CTU-based system, the design engineer requires a convenient means for not only prototype development and debugging, but also software development. The G65DS-150 Evaluation Board serves this purpose by providing G65SC150 CTU emulation during the various phases of system and software development. The Evaluation Board's primary features include:

- G65SC150 CTU
- 2K × 8 EPROM or RAM
- Internal oscillator (3 to 16 MHz)
- Vector translation logic
- Configuration switches for function selection

(continued on page 2)

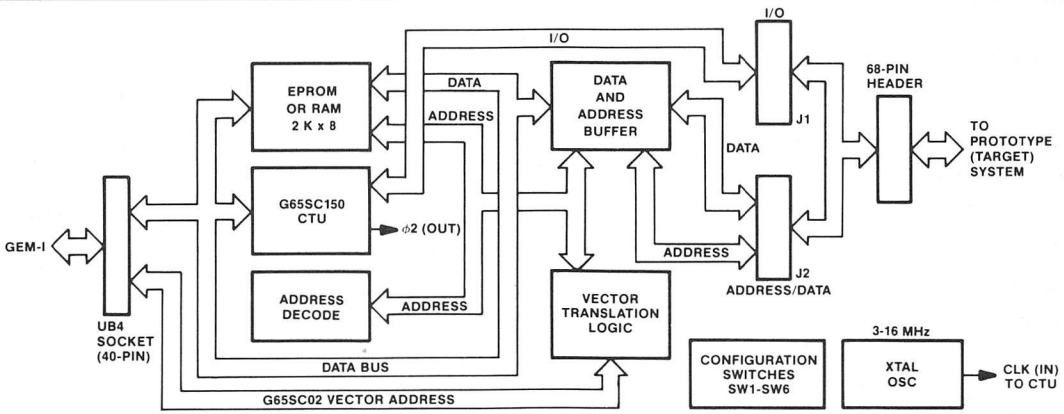
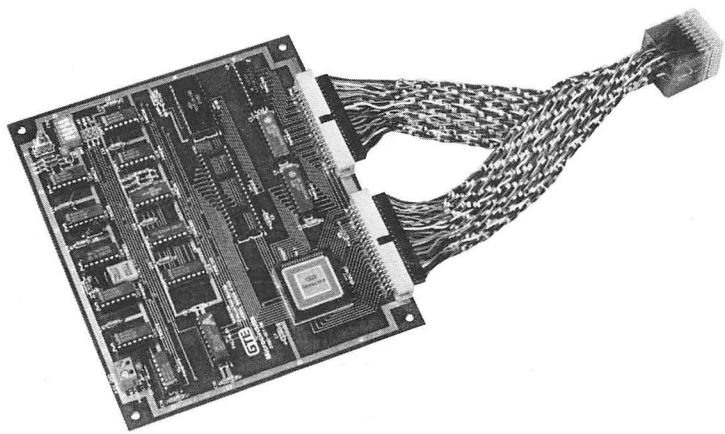


Figure 1. Evaluation Board Block Diagram



SUPPORT SYSTEMS

ADVANCE INFORMATION

This is advanced information and specifications are subject to change without notice.

- 40-pin socket for connection to the GEM-I In-Circuit Emulator, or equivalent
- 68-pin grid array header for connection to the prototype system

The G65SC150 CTU replaces the prototype system's CTU during the development and emulation phase. During initial hardware and software development, the Evaluation Board is normally used in conjunction with the GEM-I In-Circuit Emulator (or equivalent). With the G65SC150 CTU operating in the peripheral mode, the GEM-I serves to replace the CTU's internal microprocessor, thus allowing full emulation of all G65SC150 CTU functions—including its full instruction set. In this mode, the CTU's internal microprocessor is disabled. This way the GEM-I's debugging and software development capabilities can be used on the designer's CTU-based system.

Furthermore, the on-chip CTU ROM can be disabled during software development and replaced by a 2K × 8 EPROM or RAM (designer's choice) on the Evaluation Board. This feature allows the designer's program to be easily debugged and modified prior to committing the code to the CTU's mask-programmed ROM. Normally, RAM storage is used in the memory location during initial program development. Once the program is partially debugged, the RAM can be replaced with the less volatile EPROM for continued evaluation. Both RAM and EPROM plug into the same socket on the Evaluation Board.

Once the designer's prototype system and software has been partially debugged, the GEM-I In-Circuit Emulator is normally disconnected, the CTU microprocessor is enabled, and the CTU is switched from the peripheral mode to the CTU mode. In this arrangement, the Evaluation Board appears as a full-functioning CTU to the designer's prototype system. The Evaluation Board's EPROM will continue to be used until development is complete and the CTU ROM is masked for final coding.

Functional Configurations

Tables 1 and 2 provide a description of the G65DS-150 Configuration Switches and the various system configurations available.

Table 1. G65DS-150 Configuration Switches

Switch	Name	Function
SW1	Off-Board Memory	**Open**—CTU ROM, or on-board EPROM or RAM at memory addresses $F800 through $FFFF. **Closed**—Memory at $F800 through $FFFF is in prototype system.
SW2	Processor Select	**Open**—CTU microprocessor is enabled for use without GEM-I In-Circuit Emulator. **Closed**—CTU is in peripheral mode (BE = 0). GEM-I microprocessor is in use, replacing CTU microprocessor.
SW3	CTU ROM Enable	**Open**—On-board EPROM or RAM is enabled at addresses $F800 through $FFFF. PD1 (EXTR) = 1. Program control of PD1 is enabled. **Closed**—CTU ROM is enabled. PD1 (EXTR) = 0. Program control of PD1 is disabled.
SW4	Oscillator	**Open**—Prototype system oscillator is used as CTU clock input at J1, pin 5, CLK (IN). **Closed**—On-board oscillator is used as CTU clock input, CLK (IN). This signal drives J1, Pin 5.
SW5	EPROM Or RAM	**Open**—Memory socket at UB7 contains EPROM or write-protected RAM at addresses $F800 through $FFFF. **Closed**—Memory socket at UB7 contains write-enabled RAM at addresses $F800 through $FFFF.
SW6	R/$\overline{W}$ Select (Jumper)	**A-B**—CTU microprocessor is in use. R/$\overline{W}$ is an output. **B-C**—CTU is in peripheral mode. R/$\overline{W}$ is an input.

Table 2. System Configurations

Configuration	SW1	SW2	SW3	SW4	SW5	SW6
Processor						
GEM-I In-Circuit Emulator connected to socket UB4. CTU in peripheral mode.	X	Closed	X	X	X	B-C
Stand-alone CTU emulator mode. CTU microprocessor is in use. GEM-I disconnected from UB4 socket.	X	Open	X	X	X	A-B
Memory at $F800 Through $FFFF						
CTU ROM in use.	Open	X	Closed	X	X	X
On-board EPROM or write-protected RAM in use.	Open	X	Open	X	Open	X
On-board write-enabled RAM in use.	Open	X	Open	X	Closed	X
Prototype system memory in use.	Closed	X	Open	X	X	X
Clock Source						
On-board oscillator in use.	X	X	X	Closed	X	X
Prototype system clock in use (J1, Pin 5).	X	X	X	Open	X	X

Specifications

Input Voltage	5.0 Vdc ±5%
Input Current	200 mA Max.
Height	0.6 inches
Length	7.0 inches
Width	6.0 inches
Weight	0.3 pounds
Operating Temp.	0° C to 50° C
Storage Temp.	-40° C to 85° C
Relative Humidity	20 to 80 percent

Ordering Information

Item	Part Number
Evaluation Board for G65SC150 (Assembly)	G65DS-150
Evaluation Board for G65SC150 (Board Only)	G65DS-151
Interface Cable (Split Cable) for G65DS-151	G65DS-152
Instruction Guide for G65DS-150	3003-02-00

G65DS-500
Apple II Assembler

Microcircuits

Apple II Software Development Package for G65SC00 Series Microprocessors.

Features

- Apple II Software Development Package for G65SC00 microprocessors. Includes:
  - —Disk Operating System (DOS 3.3 compatible)
  - —Full Screen Text Editor
  - —Link Editor
  - —Command Monitor
  - —Macro Assembler
- Supports CMOS G65SC00 series microprocessors with enhanced instruction set
- Flexible, co-resident, full screen 80-column Text Editor with 51 editing commands
- Extensive Command Monitor with 39 monitor commands
- Operating system with low overhead disk access, date/calendar routines, and 80-column printer access
- Powerful Macro Assembler with 51 directives
- Relocatable Link Editor for added system power and flexibility
- Assembles programs of any size
- Includes a complete set of general purpose macros and sub-routines for:
  - —Displaying character strings
  - —Beeping the speaker
  - —Performing math operations
  - —High and low resolution graphics
  - —Logic and looping functions
  - —Single and double precision floating point math
  - —Transcendental functions
  - —Multiple precision integer math
  - —Apple graphics support

General Description

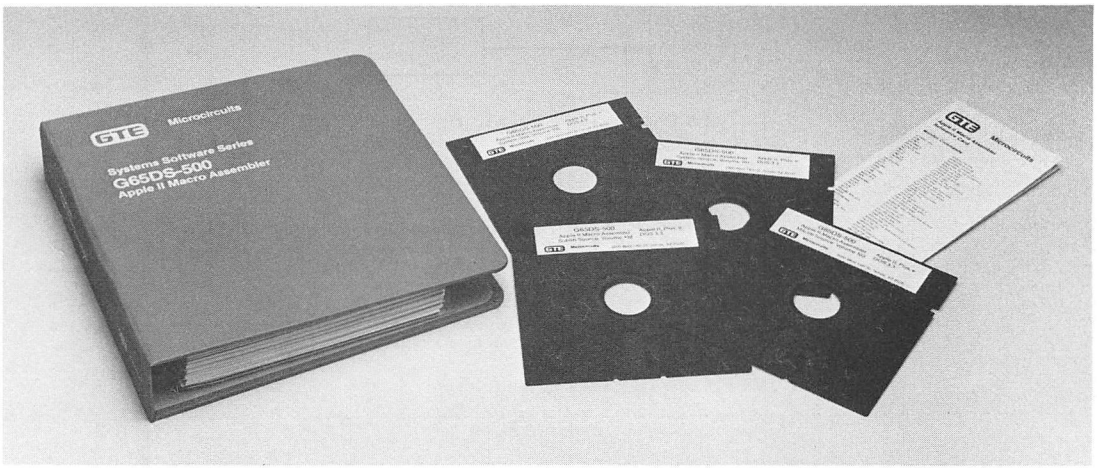
GTE's G65DS-500 Assembler is a G65SC00 series microprocessor-compatible program for routine as well as high-level software development. Included is a macro assembler, DOS 3.3 compatible disk operating system, full screen co-resident text editor, relocating link editor, and a highly flexible command monitor with 39 monitor commands. The G65DS-500 is a powerful development system that can be easily used for coding sophisticated, high-quality software.

The power of this program is not only as a standard systems programming language, but as a serious tool for the development of complex applications software. For example, it not only includes single and double-precision floating-point subroutines and macros, but supports them fully with floating-point "define constant" assembler directives.

The system's link editor relocates object modules created by the assembler and resolves external references by linking in routines from the system library, thus creating an executable binary file.

The co-resident text editor is screen-oriented with 51 flexible editing commands. Its features are comparable to editors found in sophisticated word-processing systems. Its commands provide a flexible and efficient means for preparing source files.

The operating system is fully compatible with DOS 3.3, but executes fully transparent file loading considerably faster than DOS 3.3. The G65DS-500 program is a disk-oriented



SUPPORT SYSTEMS

system. Disk access has been enhanced by eliminating considerable overhead as normally associated with DOS 3.3. The operating system contains all printer interface routines, a date input routine, and code to interface to a Videx 80-column circuit board.

The macro assembler supports the full G65SC00 series enhanced instruction set with 51 assembler directives. Also provided are conditional assembly directives and a comprehensive macro language.

The command monitor provides a set of commands which allow files on disk to be examined and modified, assembler source files to be loaded and saved, and the assembler, link editor and text editor programs to be executed. The command monitor is the first program entered when the system is first booted up.

The G65DS-500 Assembler supports all new op codes and addressing modes of CMOS G65SC00 series microprocessors. The assembler also implements a directive to disable the new instructions as necessary to maintain compatibility with the older NMOS microprocessor systems.

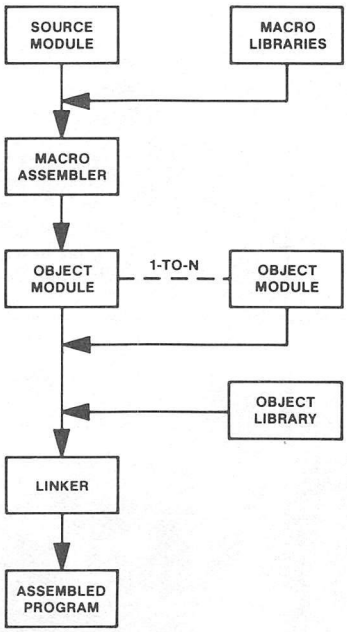
Specifications

Hardware Requirements
48K RAM and one disk drive (required)
64K RAM and two disk drives (recommended)

Computer System Compatibility
Apple II
Apple II+
Apple IIe
Franklin Ace

Included Media
Operating Instructions Manual (G65DS-500) and four 5-1/4 inch diskettes. These disks include the source code for the operating system, the macro libraries, and the subroutine libraries.

Assembler Flow Diagram



6 Quality Assurance

GTE MICROCIRCUITS

GTE Microcircuits

Quality Assurance

GTE Microcircuits' philosophy on Quality Assurance is to produce the highest quality and most reliable product possible...using the latest in technologies, instrumentation and procedures.

And at GTE Microcircuits we are continually striving to not only improve quality, but refine the empirical and statistical methods by which we measure quality and establish reliability. It is our goal to lead the way...setting standards for quality that are unsurpassed within the industry.

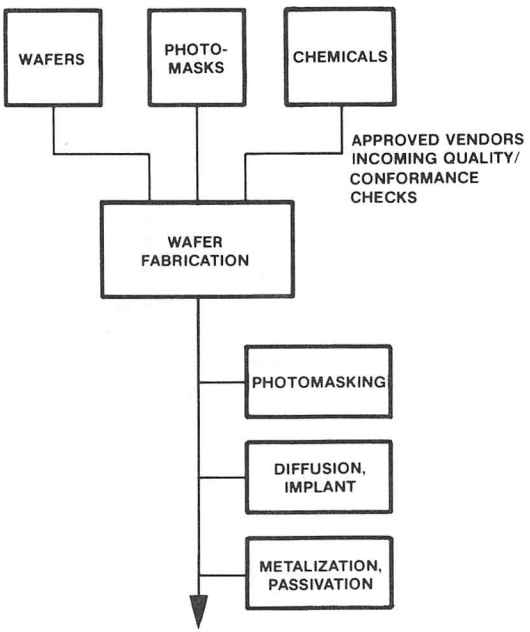


Figure 1. Process and Quality Checks

GTE Product Quality

Product quality is the ability of a product to perform as expected...to conform to its design specification without exception. It is a characteristic that must be consciously built into the product. And it starts with:

Quality Materials from Quality Vendors—Becoming a GTE supplier of raw materials is not easy. To become an approved vendor, one must first meet and maintain stringent standards and be willing to participate in periodic material specification reviews. During each review, materials such as wafers, masks and other piece parts are introduced into the manufacturing process through controlled experiments. The effect of these materials on overall quality and product reliability is evaluated by "split-lot" testing methods. At GTE, incoming inspection is a vital part of the quality program. Materials such as wafers and photomasks are inspected at a "receiving" gate.

Critical Checkpoints at the Photomask Stage—GTE processing maintains three critical inspection "gates" at the photomask stage. Each of these three gates involve visual inspections to not only guarantee correct mask alignment, but to check that critical dimensions fall within specified limits. See Figure 2.

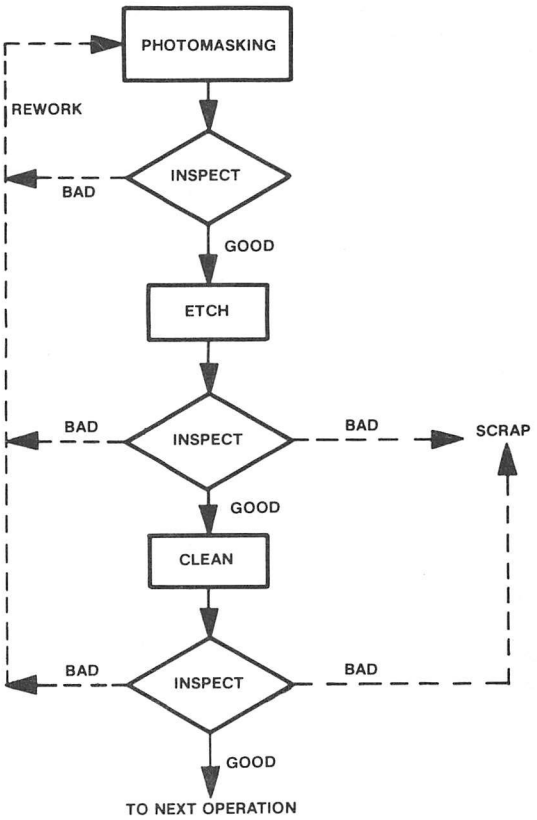
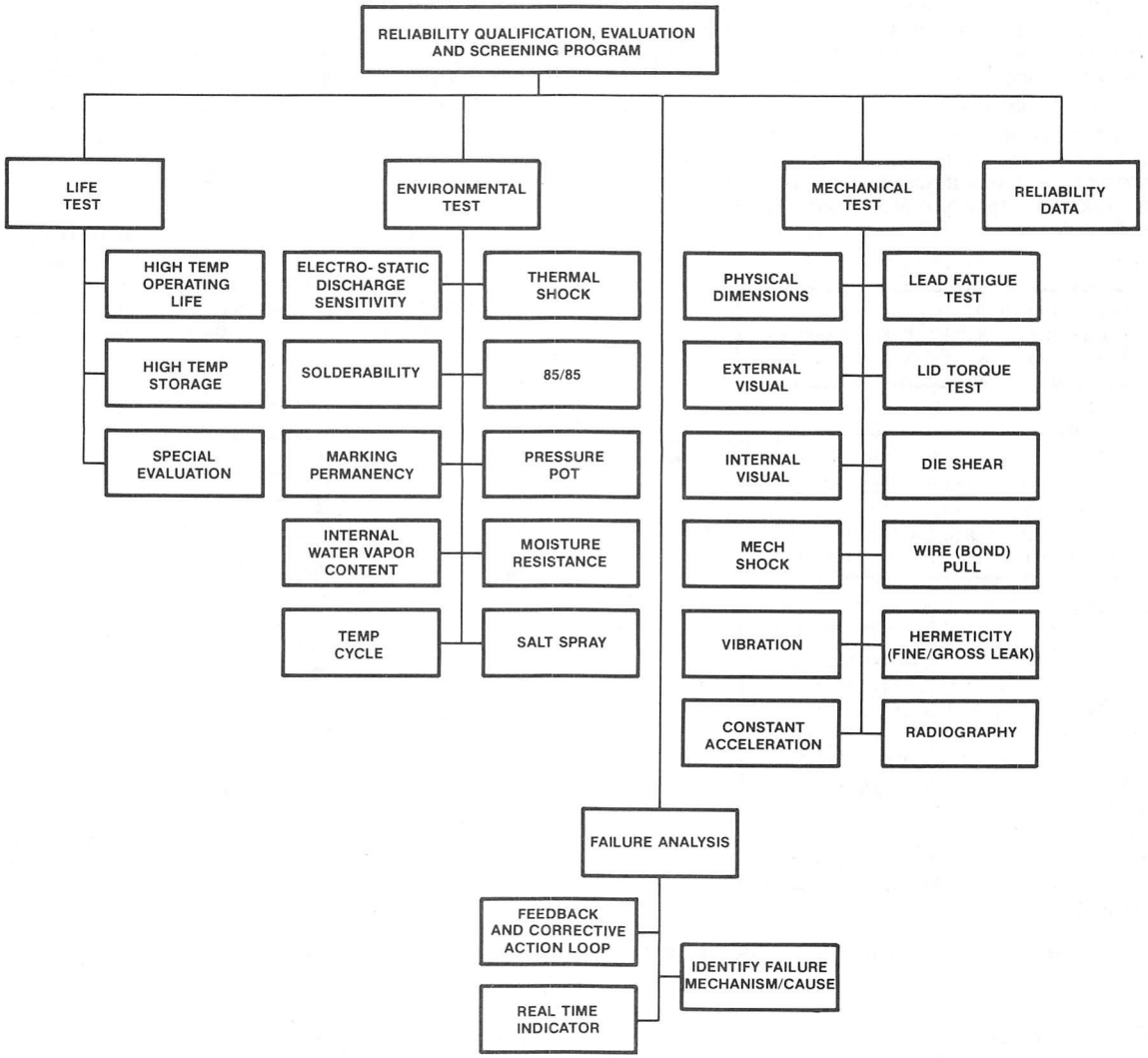


Figure 2. Process Quality Checkpoints

GTE Quality Assurance and Reliability Program



QUALITY ASSURANCE

Quality Monitors During Diffusion and Implantation—Quality monitors are used during diffusion and implantation processes. These monitors provide for Capacitance/Voltage (CV) measurements. CV analysis is a useful tool...providing measurements of how much phosphorus or boron is being "doped" into each wafer. Furthermore, CV analysis is used during the diffusion process to monitor oxide quality and system cleanliness. Another means of controlling quality consists of sheet resistance and layer thickness measurements. These measurements are continuously monitored and compared against established criteria.

Quality Monitors During Test and Assembly—Once wafer processing has been completed, the wafers are sent to the test area for electrical probing. Wafer probing consists of a 100 percent functional and parametric test of each wafer in preparation for final assembly.

During the assembly process, Quality Assurance procedures require various audit points. At least three audit points involve optical inspections at critical stages within the assembly process. These inspections ensure:

- Each wafer has been correctly and fully probed.
- Damage has not occurred as each wafer is sawed, cleaned and broken into individual dice.
- Quality is maintained during die attachment to the package and during wire bonding.

Once packaging has been completed, and the devices have been sealed, each ceramic and cerdip package is required to undergo a 100 percent gross leak test. And as a further check of package hermeticity, a sample fine leak test is conducted as a final check in the assembly process. At this point, each device is ready for final electrical (DIP) testing where worst case voltage and timing tests are performed.

Following DIP testing, all products are marked and, depending on the product, subjected to burn-in screening. Temperatures and burn-in times vary with product type and individual product specification. During the burn-in period, both voltage and temperature stresses are applied to weed out all possible "infant mortalities."

The Measure of Quality—At a given "window" in time, the number of parts which fail to meet specification can be expressed as a percentage or as PPM (Parts-Per-Million).

Example: 1.0% = 10,000 PPM
0.01% = 100 PPM

GTE Product Reliability

Product reliability is measured by the ability of a product to perform an intended function (conformance to specification) for a given period of time, and under specified environmental conditions.

To establish and maintain the highest standards of reliability, and to monitor the continued effectiveness of the production process and quality controls, GTE Microcircuits maintains an ongoing reliability assessment program as shown in Figure 3. A very important test within the reliability program is the "life test." This test is carefully designed to ensure specified component lifetime and to provide a prediction of failure rates.

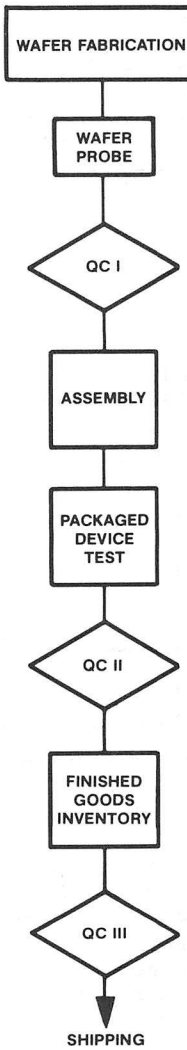


Figure 3. Quality Control Gates/Inspections

The Measure of Reliability—Reliability is measured as the number of units failing (or predicted to fail) in a given time period, and is typically expressed as a percent per 10^3 device-hours, or as "FITS" (Fails per 10^9 Hours). A more definitive description of "failure rate" is as follows:

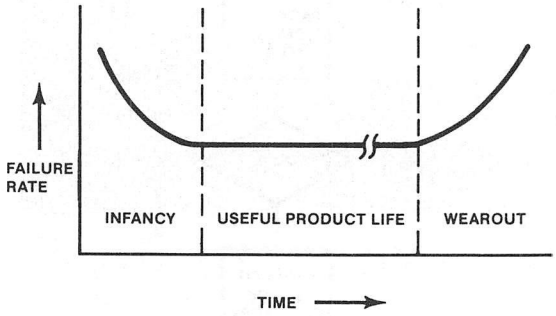
Failure Rates—Failure Rate is an alternative expression to MTTF (Mean Time To Failure). It is expressed, through statistical techniques, as the probability that a given product or component will fail within a given period of time and within specified environmental conditions. Failure

Rates may be presented in various ways, the more common being as follows:

TERM	SYMBOL	FAILS PER	EXPRESSED AS
Failure Rate	FR	10^5 Device Hours	% per 1000 Device Hours
Failure Units	FITS	10^9 Device Hours	FITS
Average Fail Rate	λ	10^6 Device Hours	—
Mean Time To Failure or Mean Time Between Failures	MTTF or MTBF	—	Time: Hours Years

The above failure-related terms may be interchanged according to the following relationship:

$$FR = \frac{FITS}{10^4} = \frac{1}{MTBF\ (10)} = \frac{\lambda}{10}$$



The familiar bathtub curve of product lifetime shows the regions of Infancy, Useful Product Life, and Wearout. These regions can be defined as follows:

Infancy—This region is the burn-in period. It is used to detect and eliminate early failures. Infant mortality is caused by early failure of weak components or is due to non-random events or causes. These conditions can cause early high failure rates which will fall off rapidly with time. Infant mortality is a quality-related issue.

Useful Product Life—Failures during product "middle age" are due to random causes which occur at random intervals, but with a fairly constant average rate of failure over a specified time period. Such failure rate is a reliability-related issue.

Wearout—Wearout normally occurs after a long period of useful life. During the Wearout period, failure rates will rise rapidly and failures will occur quite frequently. This marks the end of useful product life.

Customer Service is a QA Philosophy

GTE's Quality Assurance organization maintains a continuing awareness and concern about GTE product reliability. This concern extends far beyond our internal QA procedures and the examination of products that do not meet internal specifications. Although life tests are an effective check of product reliability, the crucial test begins after the parts have been installed into customer systems. Once in the customer environment, GTE's Quality Assurance program continues by monitoring and reacting to customer problems. Customer product experience is a vital link to our QA program.

Reliability Assessment Program

The purpose of this program is to provide a comprehensive and systematic procedure for the assessment of device reliability and product improvement.

This program includes the interdependent functions of Life Testing, Failure Analysis, and Special Evaluations as may be required. The program is an adjunct to our standard QA Qualification program, and serves as a follow-on effort for ongoing (generic) quality/reliability conformance verification. New product qualifications are conducted on die, process technologies, packages, process/design changes, new materials.

Product life testing is the primary means for determining reliability assessments. Devices are subjected to thermal stress to accelerate failure mechanisms. Data obtained from high temperature tests (typically +125°C) are "derated" to 50°C for the prediction of device failure rates. Life testing is performed as part of:

- New product qualifications
- Existing product verification (generic)
- The program to determine and monitor failure rates
- The program to determine infant mortality and failure rate predictions

New products are subjected to life testing as part of their acceptance qualification prior to being approved for standard production.

Each die process technology is routinely subjected to life tests. This is done by a rotating sampling of (generic) die types which represent each specific technology.

Failure Analysis

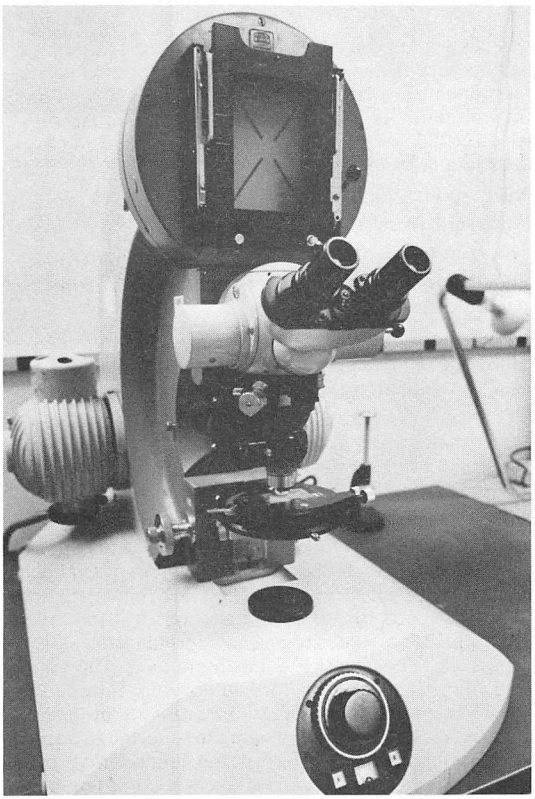
Devices which fail standard life tests or any other special testing are analyzed to determine the failure mechanism and cause. Each failure is classified and recorded. This information adds to our data base, aids in monitoring trends, and also provides the basic information for Pareto analysis, etc. These data are then summarized and published periodically...thus providing important information for ongoing product improvement programs. Furthermore, specific failure data are reported to appropriate groups (e.g., Design, Process Engineering, etc.) so that corrective action can be taken. It is this feedback

of failure analysis information which leads to improvements in testing, design and processing.

Intensive Failure Analysis... Let's Take a Look!

It can be said that analytical procedures are the reverse of the manufacturing process. Unacceptable devices are examined physically, optically and electrically on an individual basis. After identifying what caused the failure, Reliability Engineering analyzes the cause. The Microanalysis Laboratory at GTE Microcircuits is dedicated to failure analysis. This capability involves sensitive equipment which offers extensive analysis and problem solving capabilities. It is through precise optical and chemical analysis that miniscule metal lines and submicron geometries can be analyzed.

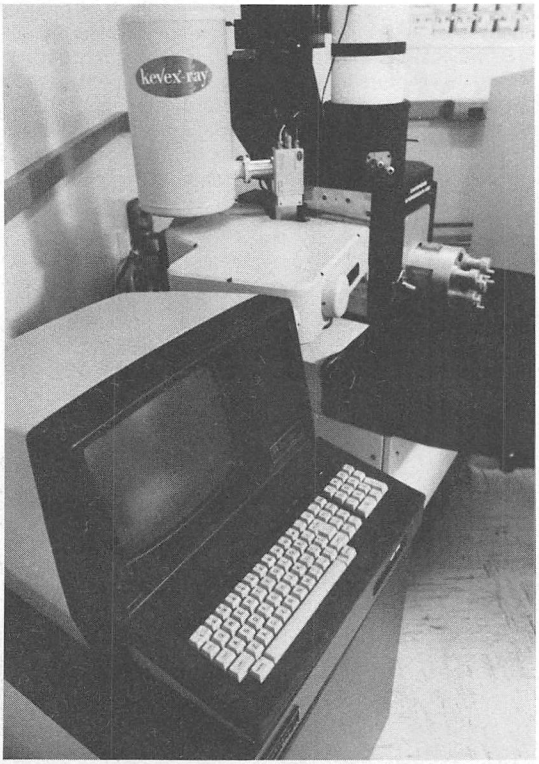
Optical Microscopes Provide Close-Up Color Photos— High power optical inspections are carried out with a Zeiss Ultaphot III® microscope. Cesium or halogen light sources, polarized light, interference contrast, and conventional bright field are among the techniques available. Extended magnification ranges of 10X to 1600X are used in combination with a 4" × 5" color photo format.



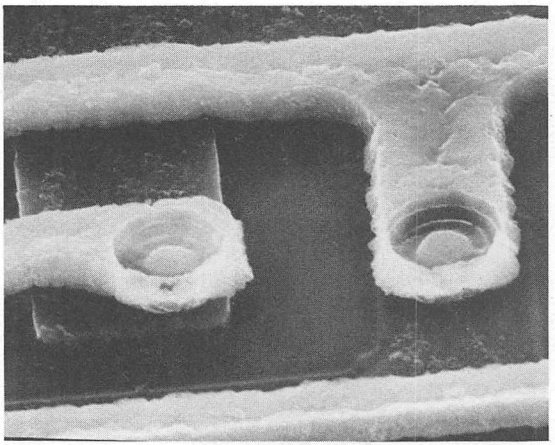
Cross Sectioning Provides a Detailed View of Internal Flaws—Cross sectioning is used extensively during failure analysis. Samples are cast in epoxy, cut or ground to the plane of interest, and then lapped and polished to a mirror-like surface. Cracks, voids and other internal flaws are easily observed in this way. Semiconductors can be stained to reveal junction depths or bulk defects. Samples can be observed by optical microscopy or with the SEM.

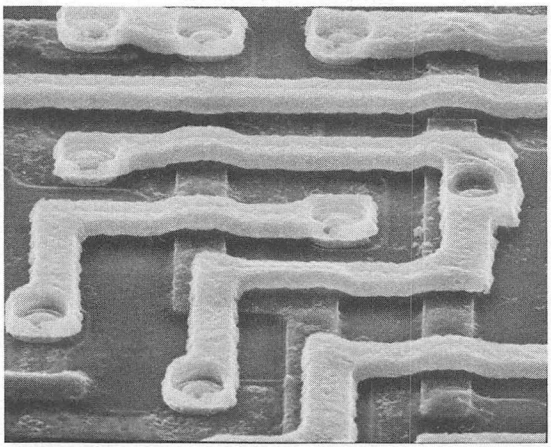
X-Ray Spectrometers Add Versatility to the SEM—Two x-ray spectrometers are attached to the SEM, thus allowing chemical analysis of the sample being observed. Chemi cal analysis is performed on a volume of material 1-2 micrometers in diameter where the electron beam strikes the sample. A large area can be analyzed by "rastering" the beam or a single spot analyzed by holding the beam stationary. X-ray maps can also be made which show the spatial distribution of an element within a sample. Energy Dispersive X-ray Spectrometry (EDS) is done with a Kevex Corporation system. Elements with atomic numbers of 11 (Sodium) and higher can be detected down to approximately 0.1% by weight. Extensive software exists for x-ray data analysis and processing.

Wavelength Dispersive X-ray Spectrometry (WDS) is performed with a Microspec WDX-2A®. Elements down to atomic number 5 (Boron) can be detected with a sensitivity of approximately 100 PPM. This system is primarily qualitative in nature and can also produce x-ray maps.



GTE's Scanning Electron Microscope—GTE's scanning electron microscope (SEM) is a vital instrument for visual failure analysis. The Cambridge Stereoscan 250® is capable of magnifications from 10X to 100,000X. Samples as large as an entire five-inch wafer can be accommodated intact with full 90° tilt and 360° rotation. In addition to the normal secondary electron image system, a high efficiency back scattered electron detector, cathodoluminescence detector, and specimen absorbed current system are fitted.



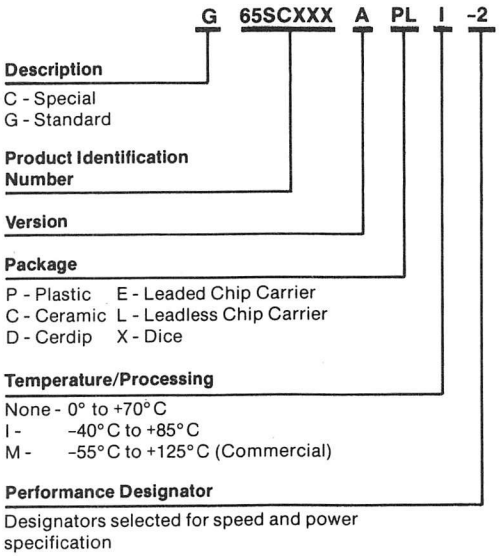


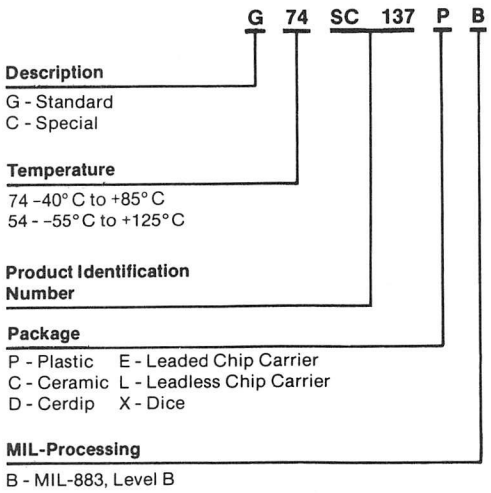
7 General Information

GTE MICROCIRCUITS

GTE Microcircuits

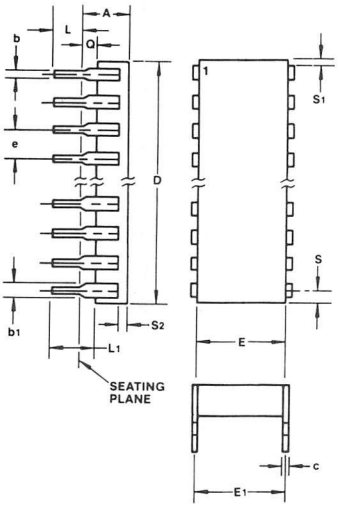
Ordering Information



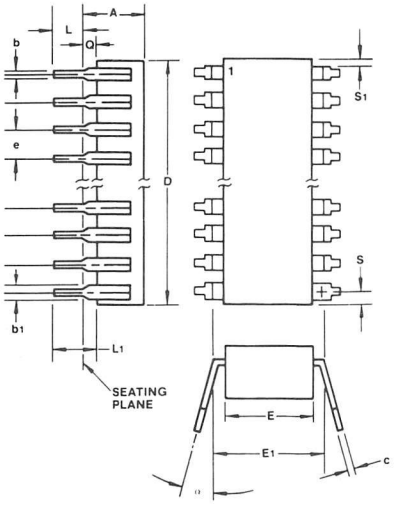


Packaging Information

Ceramic Dual In-Line



Plastic & Cerdip Dual In-Line



16-Pin Package

SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	0.840	—	21.34
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.080	—	2.03
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

18-Pin Package

SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	0.960	—	24.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

20-Pin Package

SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	1.060	—	26.92
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.060	0.38	1.52
S	—	0.080	—	2.03
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

22-Pin Package

SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	1.260	—	32.00
E	0.350	0.390	8.89	9.91
E1	0.390	0.420	9.91	10.67
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.015	0.075	0.38	1.91
S	—	0.080	—	2.03
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

24-Pin Package

SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	1.290	—	32.77
E	0.500	0.610	12.70	15.49
E1	0.590	0.620	14.99	15.75
e	0.100 BSC		2.54 BSC	
L	0.120	0.200	3.05	5.08
L1	0.150	—	3.81	—
Q	0.015	0.075	0.38	1.91
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

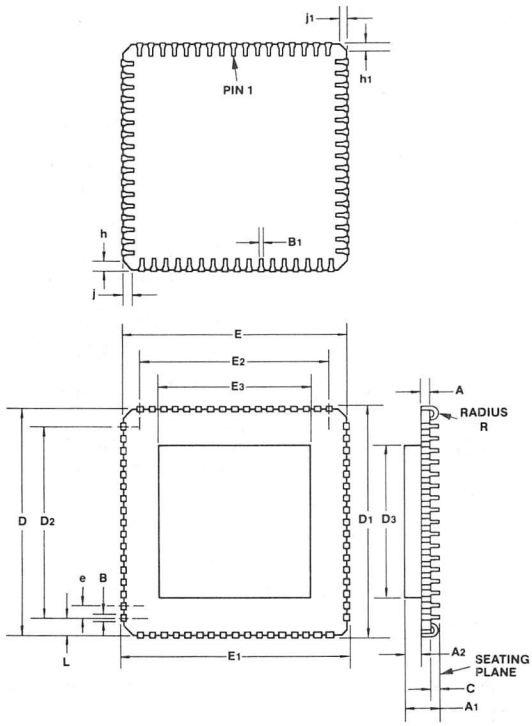
28-Pin Package

SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	1.490	—	53.24
E	0.510	0.620	12.95	15.75
E1	0.520	0.630	13.21	16.00
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.020	0.060	0.51	1.52
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

40-Pin Package

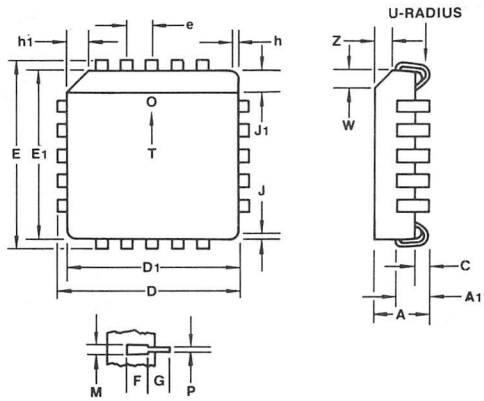
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.225	—	5.72
b	0.014	0.023	0.36	0.58
b1	0.030	0.070	0.76	1.78
c	0.008	0.015	0.20	0.38
D	—	2.096	—	53.24
E	0.510	0.620	12.95	15.75
E1	0.520	0.630	13.21	16.00
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	—	3.81	—
Q	0.020	0.060	0.51	1.52
S	—	0.098	—	2.49
S1	0.005	—	0.13	—
S2	0.005	—	0.13	—
α	0°	15°	0°	15°

68-Pin Leaded Ceramic Chip Carrier



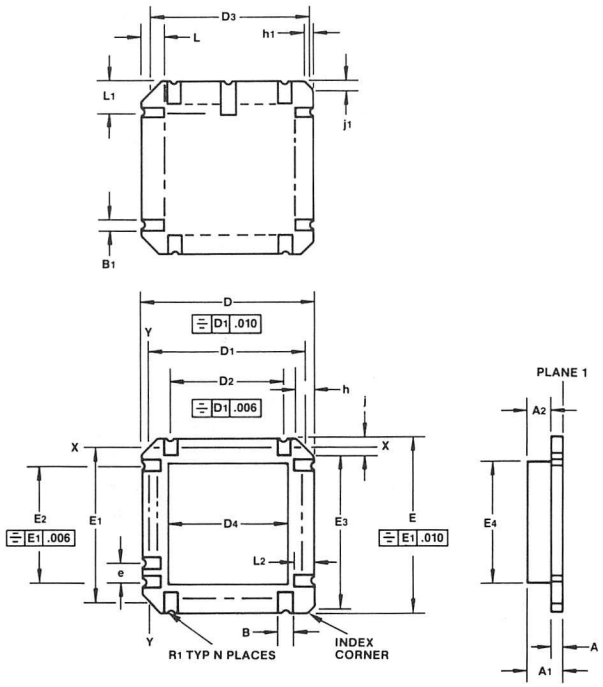
SYM-BOL	68-LEAD CARRIER INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.036	0.088	0.91	2.24
A1	—	0.200	—	5.08
A2	0.007	0.080	0.18	2.03
B	0.026	0.036	0.66	0.91
B1	0.013	0.021	0.33	0.53
C	0.020	—	0.51	—
D	0.945	0.965	24.00	24.51
D1	0.960	0.995	24.38	25.27
D2	0.800		20.32	
D3	0.495	0.862	12.57	21.89
E	0.945	0.965	24.00	24.51
E1	0.960	0.995	24.38	25.27
E2	0.800		20.32	
E3	0.495	0.862	12.57	21.89
e	0.050 BSC		1.27 BSC	
h	0.040 BSC		1.02 BSC	
h1	0.010	0.020	0.25	0.51
j	0.040 BSC		1.02 BSC	
j1	0.010	0.020	0.25	0.51
L	0.075 REF		1.91REF	
N	68		68	
R	0.020	0.045	0.51	1.14

68-Pin Leaded Plastic Chip Carrier



SYM-BOL	68-LEAD CARRIER INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.165	0.200	4.19	5.08
A1	0.095	—	2.41	—
C	0.020	—	0.51	—
D	0.975	0.995	24.77	25.27
D1	0.950	0.956	24.13	24.28
E	0.975	0.995	24.77	25.27
E1	0.950	0.956	24.13	24.28
e	0.050 BSC		1.27 BSC	
F	0.060	—	1.52	—
G	0.025	—	0.64	—
h	—	0.020	—	0.51
h1	0.042	0.048	1.07	1.22
j	—	0.020	—	0.51
j1	0.042	0.048	1.07	1.22
M	0.026	0.032	0.66	0.81
N	68		68	
P	0.013	0.021	0.33	0.53
S	0.075 REF		1.91 REF	
T	ADJ. PIN NO. 1		ADJ. PIN NO. 1	
U	0.020	0.045	0.51	1.14
W	0.020	0.045	0.51	1.14
Z	0.020	0.045	0.51	1.14

68-Pin Leadless Chip Carrier



68-LEAD CARRIER				
SYM-BOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.037	0.088	0.94	2.23
A1	0.082	0.120	2.09	3.04
A2	0.007	0.080	0.18	2.03
B	0.033 TYP	0.039 TYP	0.839 TYP	0.990 TYP
B1	0.022 TYP	0.028 TYP	0.559 TYP	0.711 TYP
D	0.938	0.962	23.83	24.43
D1	0.898	0.922	22.81	23.41
D2	0.800		20.32	
D3	0.920 REF		23.37 REF	
D4	0.495	0.862	12.6	21.8
E	0.938	0.962	23.83	24.43
E1	0.898	0.922	22.81	23.41
E2	0.800		20.32	
E3	0.920 REF		23.37 REF	
E4	0.495	0.862	12.6	21.8
e	0.050 BSC		1.27 BSC	
h	0.040 BSC		1.02 BSC	
h1	0.010	0.020	0.26	0.50
j	0.040 BSC		1.02 BSC	
j1	0.010	0.020	0.26	0.50
L	0.045	0.055	1.15	1.39
L1	0.077	0.093	1.96	2.36
L2	0.045	0.055	1.15	1.39
R1	0.007	0.011	0.178	0.279

Microcircuits

GTE Microcircuits

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